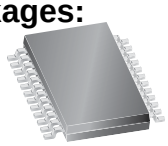
16-Channel Constant-Current LED Driver

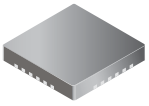
Features and Benefits

- 16 constant-current outputs, up to 50 mA each
- LED output voltage up to 12 V
- 3.0 to 5.5 V logic supply range
- Schmitt trigger inputs for improved noise immunity
- Power-On Reset (POR), all register bits = 0
- Low-power CMOS logic and latches
- High data input rate: 30 MHz
- Output current accuracy: between channels <±3% and between ICs ±7%, over the full operating temperature range
- Internal UVLO and thermal shutdown (TSD) circuitry

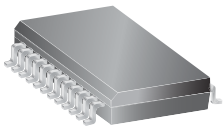
Packages:



24-pin TSSOP
with exposed thermal pad
(Package LP)



24-contact QFN
4 mm × 4 mm × 0.75 mm
(Package ES)



24-pin SOIC
(Package LW)

Not to scale

Description

The A6282 device is designed for LED display applications. This CMOS device includes an input shift register, accompanying data latches, and 16 MOS constant current sink drivers.

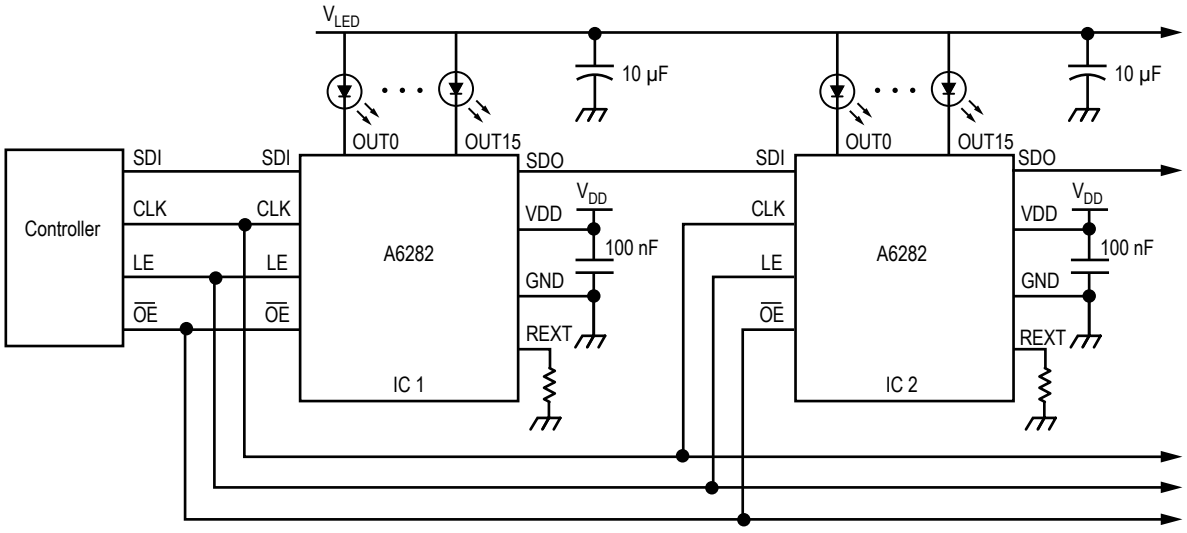
The CMOS shift registers and latches allow direct interfacing with microprocessor-based systems. With a 3.3 or 5 V logic supply, typical serial data input rates can reach up to 30 MHz. The LED drive current level can be set by a single external resistor, selected by the application designer. A serial data output permits cascading of multiple devices in applications requiring additional drive lines.

The A6282 is available in a variety of 24-terminal packages: QFN (package ES) and eTSSOP (LP), which have an exposed thermal pad, and SOIC (LW). All packages are lead (Pb) free with 100% matte tin leadframe plating.

Applications include the following:

- Monocolor, multicolor, or full-color LED display
- Monocolor, multicolor, or full-color LED signboard
- Display backlighting
- Multicolor LED lighting

Typical Application



Cascaded A6282 devices

Selection Guide

Part Number	Package	Packing
A6282EES-T	4 mm × 4 mm QFN, 24 pins, exposed thermal pad	92 pieces per tube
A6282EESTR-T		1500 pieces per 7-in. reel
A6282ELP-T	TSSOP, 24 pins, exposed thermal pad	62 pieces per tube
A6282ELPTR-T		4000 pieces per 13 in. reel
A6282ELW-T	SOICW, 24 pins	31 pieces per tube
A6282ELWTR-T		1000 pieces per 13-in. reel

Absolute Maximum Ratings

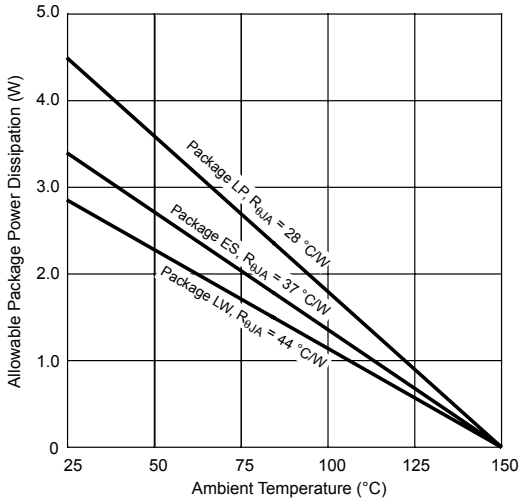
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage*	V_{DD}		–0.3 to 5.5	V
OUTx Current (any single output)	I_O		60	mA
Input Voltage Range*	V_I	V_{OE}, V_{LE}, V_{CLK}, V_{SDI}	–0.3 to V_{DD} + 0.3	V
LED Load Supply Range*	V_{LED}		–0.3 to 13.2	V
ESD Rating		HBM (JEDEC JESD22-A114, Human Body Model)	2.0	kV
		CDM (JEDEC JESD22-C101, Charged Device Model)	1.0	kV
Operating Temperature Range (E)	T_A		–40 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

*With respect to ground.

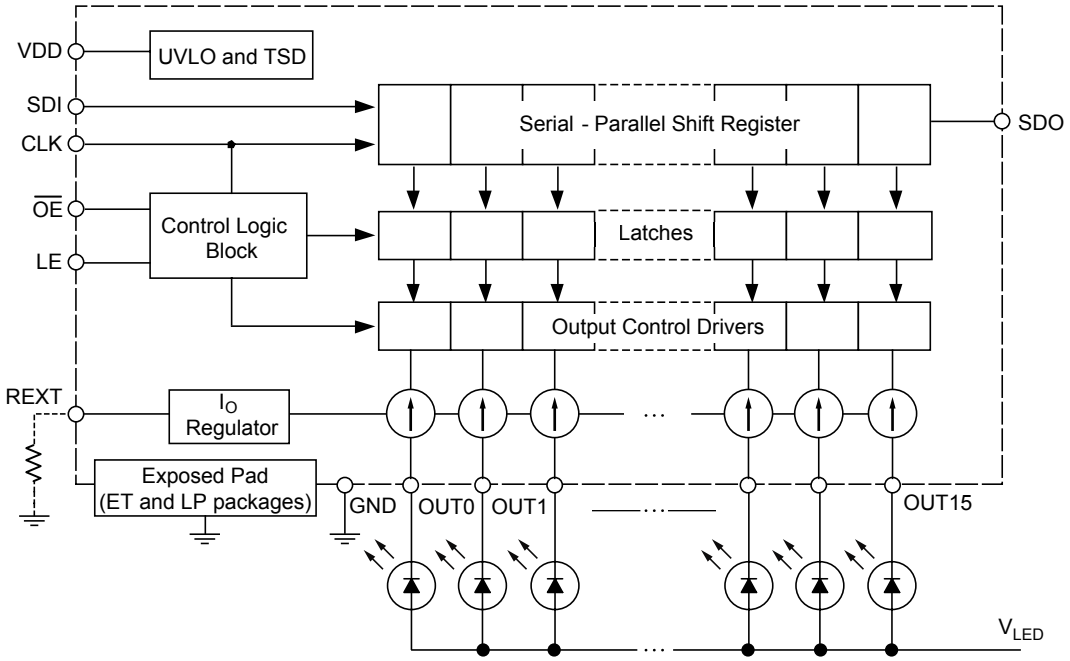
Thermal Characteristics

Characteristic	Symbol	Test Conditions[1]	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	ES package, 4-layer PCB based on JEDEC standard	37	°C/W
		LP packge, 4-layer PCB based on JEDEC standard	28	°C/W
		LW packge, 4-layer PCB based on JEDEC standard	44	°C/W

*Additional thermal information available on the Allegro website.

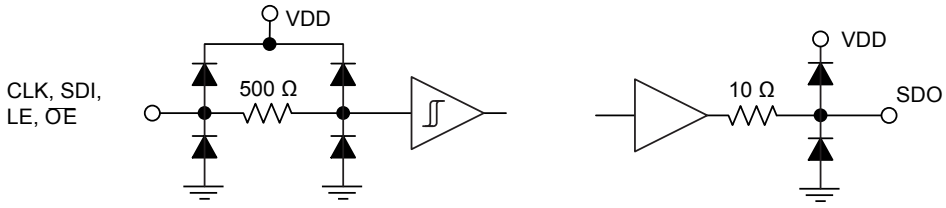


Functional Block Diagram



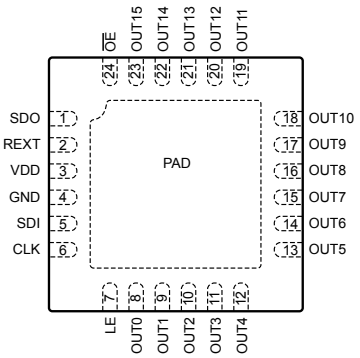
Inputs and Outputs Equivalent Circuits

Resistor values are equivalent resistance and not tested

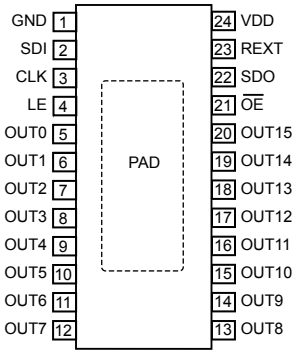


Pin-out Diagrams

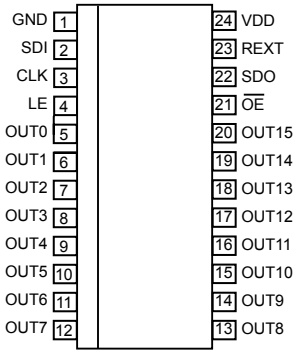
Top-down views



ES Package



LP Package



LW Package

Terminal List Table

Name	Number			Description
	ES	LP	LW	
CLK	6	3	3	Clock; data shift clock input terminal
GND	4	1	1	Logic supply ground and load supply ground
LE	7	4	4	Latch Enable input terminal
$\overline{OE}$	24	21	21	Output Enable input terminal, active low (when $\overline{OE}$ = high, all OUTx outputs are forced off; when $\overline{OE}$ = low, on/off status of OUTx outputs is controlled by the state of the latches
OUT0	8	5	5	Constant current outputs
OUT1	9	6	6	
OUT2	10	7	7	
OUT3	11	8	8	
OUT4	12	9	9	
OUT5	13	10	10	
OUT6	14	11	11	
OUT7	15	12	12	
OUT8	16	13	13	
OUT9	17	14	14	
OUT10	18	15	15	
OUT11	19	16	16	
OUT12	20	17	17	
OUT13	21	18	18	
OUT14	22	19	19	
OUT15	23	20	20	
PAD	–	–	n.a.	Exposed pad for enhanced thermal dissipation; not connected internally, connect to GND
REXT	2	23	23	Reference current terminal; sets output current for all channels
SDI	5	2	2	Serial Data In terminal
SDO	1	22	22	Serial Data Out terminal
VDD	3	24	24	Logic Supply terminal

ELECTRICAL CHARACTERISTICS at T_A[1] = 25°C, V_{DD} = 3.0 to 5.5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
LED Load Supply Output Voltage	V_{LED}	Operating	–	–	12.0	V
Undervoltage Lockout	$V_{DD(UV)}$	V_{DD} 0 → 5.0 V	2.5	2.7	2.9	V
		V_{DD} 5 → 0.0 V	2.3	2.5	2.7	V
Output Current	I_O	V_{DD} = 4.5 to 5.5 V, $V_{DS(x)}$ = 1 V, R_{EXT} = 374 Ω	47.4	51.1	54.5	mA
		V_{DD} = 3.0 to 3.6 V, $V_{DS(x)}$ = 1 V, R_{EXT} = 374 Ω	46.5	50.1	53.5	mA
		V_{DD} = 4.5 to 5.5 V, $V_{DS(x)}$ = 1 V, R_{EXT} = 910 Ω	19.8	21.4	22.8	mA
		V_{DD} = 3.0 to 3.6 V, $V_{DS(x)}$ = 1 V, R_{EXT} = 910 Ω	19.5	21.0	22.4	mA
Output Current Shift	$\%\Delta I_O$	V_{DD} = 5.5 V, $V_{DS(x)}$ = 1 V, R_{EXT} = 910 Ω, T_A = 25°C; between one output on and all outputs on	–	–	±1	%
Output to Output Matching Error[3]	Err	V_{DS} = 1 V, R_{EXT} = 374 Ω, all outputs on	–	±1.0	±3.0	%
		V_{DS} = 1 V, R_{EXT} = 910 Ω, all outputs on	–	±1.0	±3.0	%
Output Current Regulation	$\%I_{O(reg)}$	V_{DD} = 5.5 V, $V_{DS(x)}$ = 1 to 3 V, R_{EXT} = 374 Ω, all outputs on	–	1.7	3	%/V
		V_{DD} = 5.5 V, $V_{DS(x)}$ = 1 to 3 V, R_{EXT} = 910 Ω, all outputs on	–	2.4	4	%/V
		V_{DD} = 3.6 V, $V_{DS(x)}$ = 1 to 3 V, R_{EXT} = 374 Ω, all outputs on	–	1.2	2	%/V
		V_{DD} = 3.6 V, $V_{DS(x)}$ = 1 to 3 V, R_{EXT} = 910 Ω, all outputs on	–	1.8	3	%/V
Output Leakage Current	I_{DSS}	V_{OH} = 12 V	–	–	0.5	µA
Logic Input Voltage	V_{IH}		0.8×V_{DD}	–	V_{DD}	V
	V_{IL}		GND	–	0.2×V_{DD}	V
Logic Input Voltage Hysteresis	V_{Ihys}	All digital inputs	250	–	900	mV
Logic Input Current	I_I	All digital inputs	–1	–	1	µA
SDO Voltage	V_{OL}	I_{OL} = 1 mA	–	–	0.5	V
	V_{OH}	I_{OH} = –1 mA	V_{DD}–0.5	–	–	V
Supply Current[4]	$I_{DD(OFF)}$	R_{EXT} = 3.8 kΩ, V_{OE} = 5 V	–	–	6	mA
		R_{EXT} = 910 Ω, V_{OE} = 5 V	–	–	16	mA
		R_{EXT} = 374 Ω, V_{OE} = 5 V	–	–	40	mA
	$I_{DD(ON)}$	All outputs on, R_{EXT} = 910 Ω, V_O = 1 V, data transfer 30 MHz	–	–	20	mA
		All outputs on, R_{EXT} = 374 Ω, V_O = 1 V, data transfer 30 MHz	–	–	45	mA

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued), at T_A[1] = 25°C, V_{DD} = 3.0 to 5.5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	°C
Reference Voltage at External Resistor REXT	V_{EXT}	R_{EXT} = 374 Ω	–	1.21	–	V

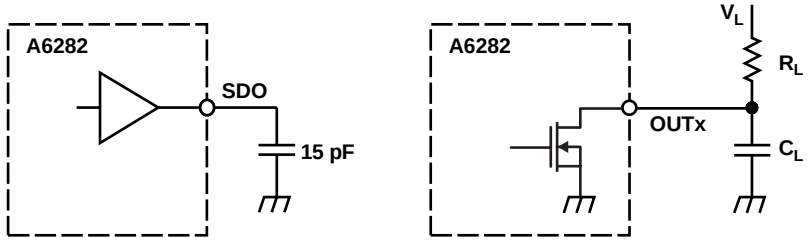
[1]Tested at 25°C. Specifications are assured by design and characterization over the operating temperature range of –40°C to 85°C.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[3]Err = (I_O(min or max) – I_O(av)) / I_O(av). I_O(av) is the average current of all outputs. I_O(min or max) is the output current with the greatest difference from I_O(av).
[4]Recommended operating range: V_O = 1.0 to 3.0 V.

SWITCHING CHARACTERISTICS at T_A[1] = 25°C, V_{DD} = V_{IH} = 5.0 V, V_{DS} = 1 V, V_{IL} = 0 V, R_{EXT} = 910 Ω, I_O = 21.4 mA, V_L = 2 V, R_L = 51 Ω, C_L = 15 pF (see also Timing Diagrams section)

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Clock Frequency	f_{CLK}	CLK	–	–	30	MHz
Clock Frequency (cascaded devices)	f_{CLKC}	CLK	–	–	25	MHz
Clock Pulse Duration	t_{wh0}	CLK = high	16	–	–	ns
LE Pulse Duration	t_{wh1}	LE = high	20	–	–	ns
Setup Time	t_{su0}	SDI to CLK↑	10	–	–	ns
	t_{su1}	CLK↑ to LE↑	10	–	–	ns
Hold Time	t_{h0}	CLK↑ to SDI	10	–	–	ns
	t_{h1}	LE↓ to CLK↑	10	–	–	ns
Rise Time	t_{r0}	SDO, 10/90% points (measurement circuit A)	–	–	16	ns
	t_{r1}	OUTx, V_{DD} = 5 V,10/90% points (measurement circuit B)	–	10	30	ns
Fall Time	t_{f0}	SDO, 10/90% points (measurement circuit A)	–	–	16	ns
	t_{f1}	OUTx, V_{DD} = 5 V,10/90% points (measurement circuit B)	–	10	30	ns
Propagation Delay Time	t_{pd0}	CLK↑ to SDO↑↓ (measurement circuit A)	–	–	30	ns
	t_{pd1}	$\overline{OE}$↓ to OUTx↑↓ (measurement circuit B)	–	–	60	ns
	t_{pd2}	LE↑ to OUTx↑↓ (measurement circuit B)	–	–	60	ns
Output Enable Pulse Duration	$t_{w(OE)}$	(see Timing Diagrams section)	60	–	–	ns

[1]Tested at 25°C. Specifications are assured by design and characterization over the operating temperature range of –40°C to 85°C.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

Parameter Measurement Circuits

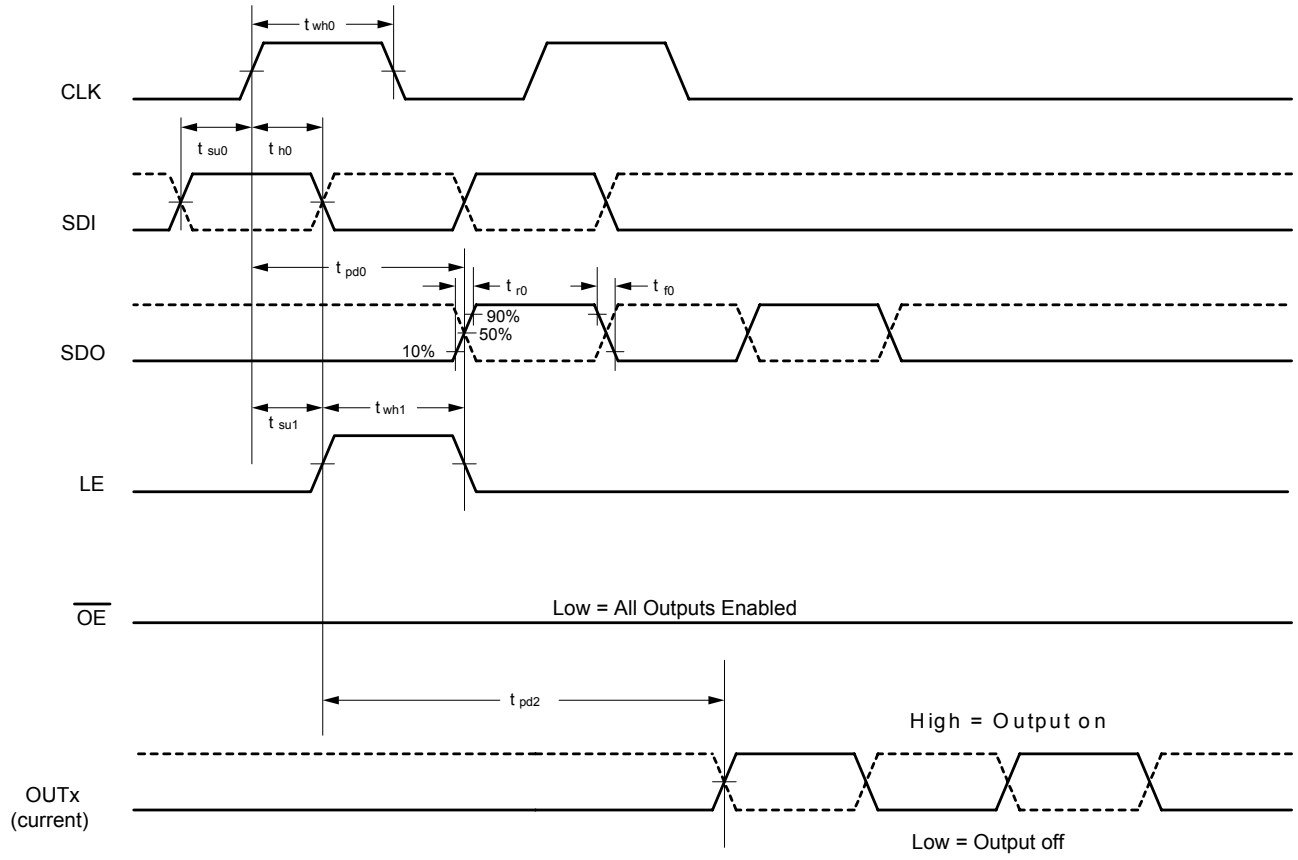


(A) Circuit for t_{f0}, t_{pd0}, and t_{r0}

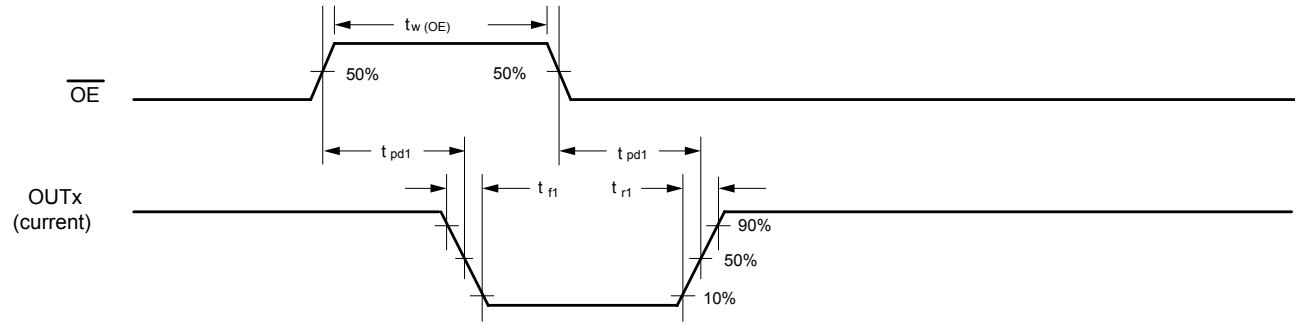
(B) Circuit for t_{f1}, t_{pd1}, t_{pd2}, and t_{r1}.

Timing Diagrams

Normal Operation

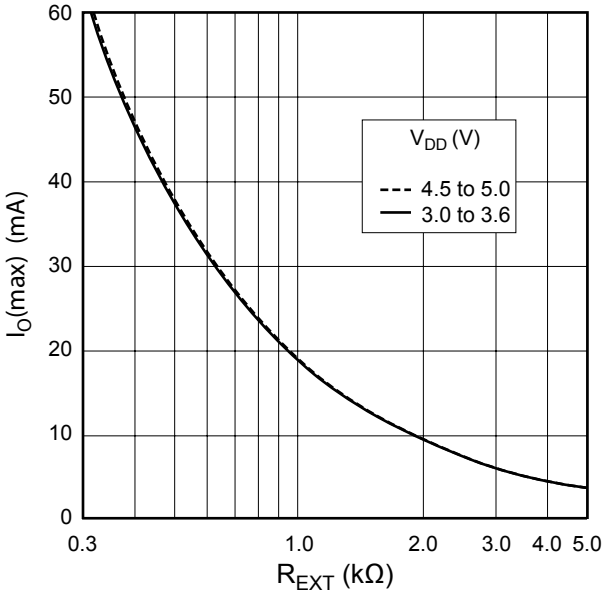


Disabling Outputs



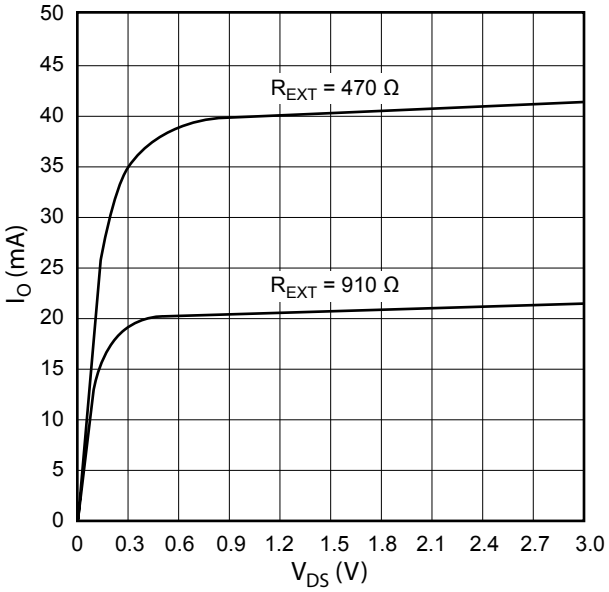
Operating Characteristics

Channel Maximum Constant Output Current versus External Reference Resistance



Channel Output Current versus Output Voltage

V_{DD} = 5.0 V



Input-Output Truth Table

Serial Data Input (SDI)	Clock Input (CLK)	Shift Register Contents	Serial Data Out (SDO)	Latch Enable Input (LE)	Latch Contents	Output Enable Input ($\overline{OE}$)	Output Contents
		I_0 I_1 I_2 … I_{15}			I_0 I_1 I_2 … I_{15}		I_0 I_1 I_2 … I_{15}
H	⌐‾	H R_0 R_1 … R_{15}	R_{14}				
L	⌐‾	L R_0 R_1 … R_{15}	R_{14}				
X	‾⌐	R_0 R_1 R_2 … R_{15}	R_{15}				
		X X X … X	X	L	R_0 R_1 R_2 … R_{15}		
		P_0 P_1 P_2 … P_{15}	P_{15}	H	P_0 P_1 P_2 … P_{15}	L (Outputs on)	P_0 P_1 P_2 … P_{15}
					X X X … X	H (Outputs off)	H H H … H

L = Low logic (voltage) level, H = High logic (voltage) level, X = Don't care, P = Present state, R = Previous state

Functional Description

Normal Operation

Serial data present at the SDI (Serial Data In) input is transferred to the shift register on the transition from logic 0 to logic 1 of the CLK (Clock) input pulse. On succeeding CLK pulses, the register shifts data towards the SDO (Serial Data Out) output. The serial data must appear at the input prior to the rising edge of the CLK waveform.

Data present in any register is transferred to the respective latch when the LE (Latch Enable) input is high (serial-to-parallel conversion). The latches continue to accept new data as long as LE is held high (level triggered).

Applications where the latches are bypassed (LE tied high) require that the $\overline{OE}$ (Output Enable) input be high during serial data entry. When $\overline{OE}$ is high, the output sink drivers are disabled (off). The data stored in the latches is not affected by the state of $\overline{OE}$. With $\overline{OE}$ active (low), the outputs are controlled by the state of their respective latches.

Setting Maximum Channel Current

The maximum output current per channel is set by a single external resistor, REXT, which is placed between the REXT pin and GND. The voltage on REXT, V_{EXT}, is set by an internal band gap and is 1.21 V, typical.

The maximum channel output current can be calculated as:

$$I_O(max) = (18483.1/ R_{EXT}) + 0.67 \text{ , for } V_{DD} = 3.0 \text{ to } 3.6 \text{ V ,}$$

or

$$I_O(max) = (18841.2/ R_{EXT}) + 0.68 \text{ , for } V_{DD} = 4.5 \text{ to } 5.5 \text{ V ,}$$

where R_{EXT} is the value of the user-selected external resistor, which should not be less than 374 Ω.

A chart of the maximum per channel (OUT0 to OUT15) constant output current, $I_O(max)$, at various values of R_{EXT}, is shown in the Operating Characteristics section.

Undervoltage Lockout

The A6282 includes an internal undervoltage lockout (UVLO) circuit that disables the outputs in the event that the logic supply voltage drops below a minimum acceptable level. This feature prevents the display of erroneous information, a necessary function for some critical applications. Upon recovery of the logic supply voltage after a UVLO event, all internal shift registers and latches are set to 0. The A6282 is then in normal mode.

Thermal Shutdown Protection

If the junction temperature exceeds the threshold temperature, T_{JTSD}, 165°C typical, the outputs will be turned off until the junction temperature cools down through the thermal shutdown hysteresis, 15°C typical. The shift register and output latches register will remain active during a thermal shutdown event. Therefore, there is no need to reset the data in the output latches.

Application Information

Load Supply Voltage (V_{LED})

This device is designed to operate with driver voltage drops (V_{DS}) of 1.0 to 3.0V. If higher voltages are dropped across the driver, package power dissipation will increase. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage, V_{LED}, or to set a series voltage drop, V_{DROP}, according to the following formula:

$$V_{DROP} = V_{LED} - V_F - V_{DS} \quad ,$$

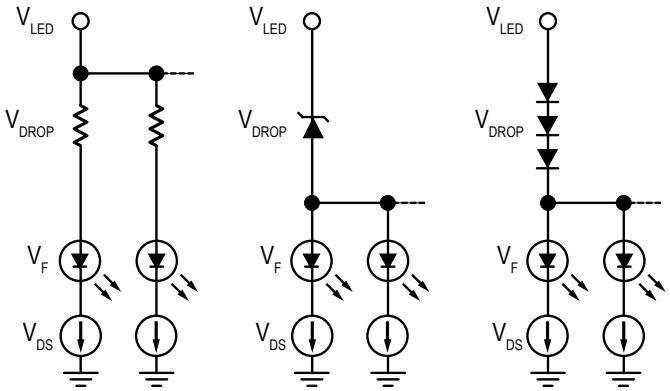
where V_F is the LED forward voltage. For reference, typical LED forward voltages are:

LED Type	V_F (V)
White	3.5 to 4.0
Blue	3.0 to 5.5
Green	1.8 to 2.5
Yellow	2.0 to 2.5
Amber	1.9 to 3.0
Red	1.6 to 2.5
Infrared	1.2 to 1.8
UV	3.0 to 4.0

$V_{DROP} = I_O \times R_{DROP}$ for a single driver, for a Zener diode (V_Z), or for a series string of silicon diodes (approximately 0.7 V per diode) for a group of drivers (these configurations are shown in the figure below). If the available voltage source will cause unacceptable power dissipation and series resistors or diodes are undesirable, a voltage regulator can be used to provide V_{LED}.

Pattern Layout

To save pins and board space, the A6282 uses one pin for both logic ground and power ground. Therefore, achieving optimal performance requires careful attention to layout. Following the suggestions below will improve the analog performance and logic noise immunity.



Typical application voltage drops

1. Place the REXT resistor as close as possible to the REXT pin and GND pin. This will minimize parasitic inductance and capacitance.

2. Use a separate line to the device GND pin for REXT, and separate lines for the decoupling capacitors. The lines should join at ground. This star grounding will improve output load regulation and minimize any chance of oscillation.

The REXT ground line should carry only the small current from the internal voltage reference at REXT. The high AC currents flowing through the decoupling capacitors and their resistive and inductive PCB lines cause noise (ground bounce) on the capacitor ground lines. Such noise could disturb the reference voltage at REXT and promote oscillation. Connect the exposed thermal pad of the ES and LP packages to the power ground, along with the decoupling capacitors, and not to the ground line for REXT.

3. Keep the output drive lines (OUT0 through OUT15) away from the REXT pin to avoid coupling of the output signal into the reference for the current sources. Output lines should not run adjacent to the REXT pin or directly under the REXT pin.

4. Use decoupling capacitors on the VDD pin and the LED supply bus. Place the logic decoupling capacitor (0.1 µF, one for each A6282) as close as possible to the VDD pin. Use at least one 10 µF capacitor from the LED supply line to device ground for at least every two A6282s.

5. Use multilayer boards if possible.

Package Power Dissipation

The maximum allowable package power dissipation based on package type is determined by:

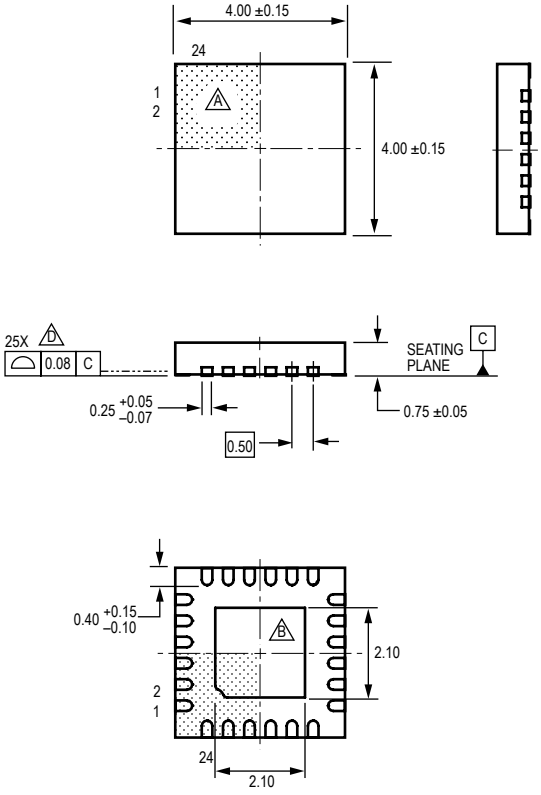
$$P_{D(max)} = (150 - T_A) / R_{\theta JA},$$

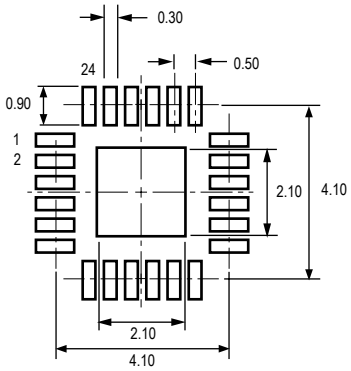
where $R_{\theta JA}$ is the thermal resistance of the package, determined experimentally. Power dissipation levels based on the package are shown in the Thermal Characteristics table.
The actual package power dissipation is determined by:

$$P_{D(act)} = DC \times (V_{DS} \times I_O \times 16) + (V_{DD} \times I_{DD}),$$

where DC is the duty cycle. The value *16* is the maximum number of available device outputs, representing the worst-case scenario (displaying all 16 LEDs). When the load supply voltage, V_{LED}, is greater than 3 to 5 V, and $P_{D(act)} > P_{D(max)}$, an external voltage reducer (V_{DROP}) must be used (figure at left). Reducing DC will also reduce power dissipation. The ES and LP packages contain an exposed thermal pad on the bottom of the package for enhanced heat dissipation. Connect this pad to a large power ground plane using thermal vias. JEDEC documents JESD51-3 and JESD51-5 give suggestions for PCB and thermal via designs.

Package ES, 4 mm x 4 mm, 24-pin QFN with Exposed Thermal Pad





C PCB Layout Reference View

For Reference Only
(reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

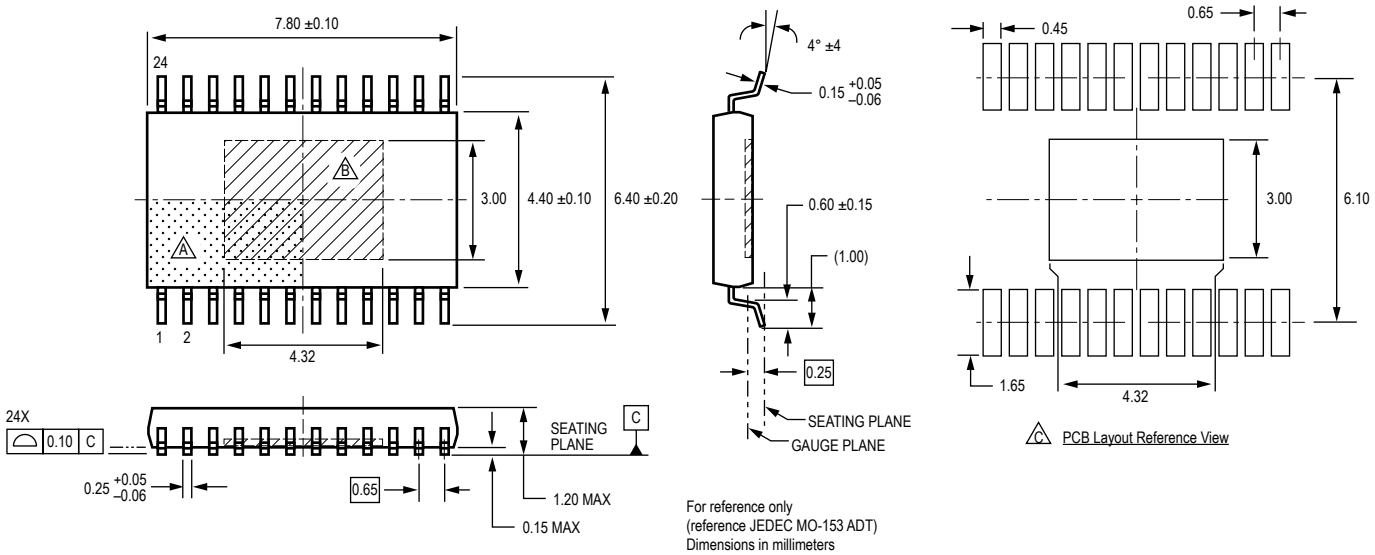
A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package LP, 24-pin TSSOP with Exposed Thermal Pad



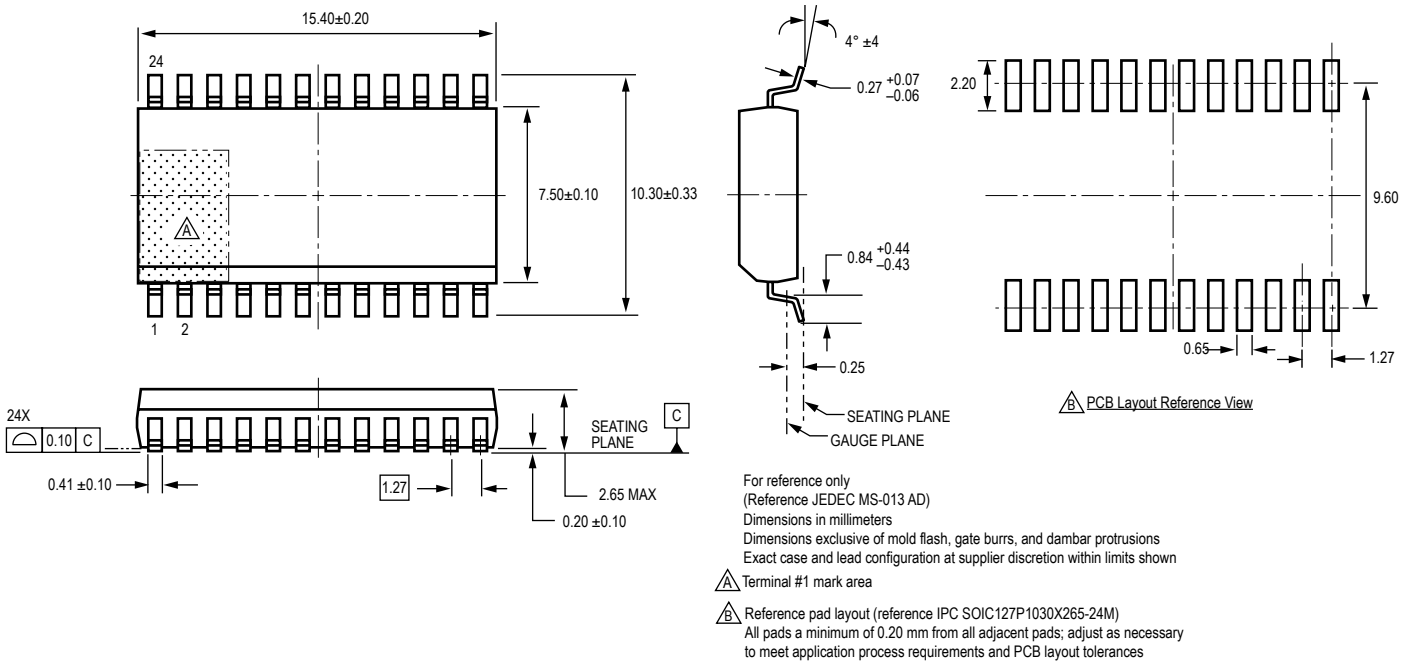
For reference only
(reference JEDEC MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LW, 24-pin SOICW



For reference only
(Reference JEDEC MS-013 AD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances

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