Constant-Current LED Drivers

Introduction

LEDs are current-driven devices that require current limiting when driven from a voltage source. In most applications, it is desirable to drive LEDs with a constant-current source. The current source is used to regulate the current through the LED regardless of power supply (voltage) variations or changes in forward voltage drops, V_F, between LEDs.

The devices in the Allegro® MicroSystems A62xx family of LED drivers are optimized for LED display-driving applications, lending cost-effectiveness and compactness to the solution. The family includes the A6275, A6276, A6277, A6278, and A6279 devices. These feature both 8-bit and 16-bit versions, and are available in standard plastic DIP, SOIC, MLP (A6279 only), and TSSOP packages.

The A6275, A6276, A6278, and A6279 can provide a maximum of 90 mA per output, and the A6277 can provide a maximum of 150 mA per output, making them suitable for various large display applications such as scoreboards and gaming equipment.

Constant Current

The Allegro A62xx family offers the designer the ability to configure displays with virtually no variation in brightness across the display. By the A62xx controlling typical output-to-output current variation to within ±1.5% (between any two outputs of a single device), noticeable variation in LED intensity is eliminated.

Table 1. Output options for A62xx familiy

Device	Current Mirror Ratio	Band Gap, V_{REF} (V)	Maximum Current per Output, I_O(max) (mA)
A6275	15.25:1	1.23	90
A6276	15.25:1	1.23	90
A6277	15.25:1	1.23	150
A6278	23.45:1	0.8	90
A6279	23.45:1	0.8	90

The devices also allow the user to set the magnitude of constant current to the LEDs. Once set, the current remains constant, regardless of the LED voltage variation, supply voltage variation, or other circuit parameters that could otherwise affect LED current.

The output current is controlled by a current mirror, a bandgap regulator, and an external current-control resistor, REXT. The values for the options are shown in table 1 and the combined effect is shown in figure 1, which is calculated using the following equation:

$$I_O(\text{max}) = \frac{CMR \times BG}{R_{EXT}} \quad , \tag{1}$$

where:

I_O(max) is the maximum per output current, in A,
CMR is the current mirror ratio from table 1,
BG is the band gap from table 1, and
R_{EXT} is the selected value for REXT, in Ω.

Note that the relationship of CMR and BG is fixed ($CMR \times BG = 18.76$), so to set a given I_O, select R_{EXT} using:

$$R_{EXT} = 18.76 \,/\, I_O(\text{max}) \quad . \tag{2}$$

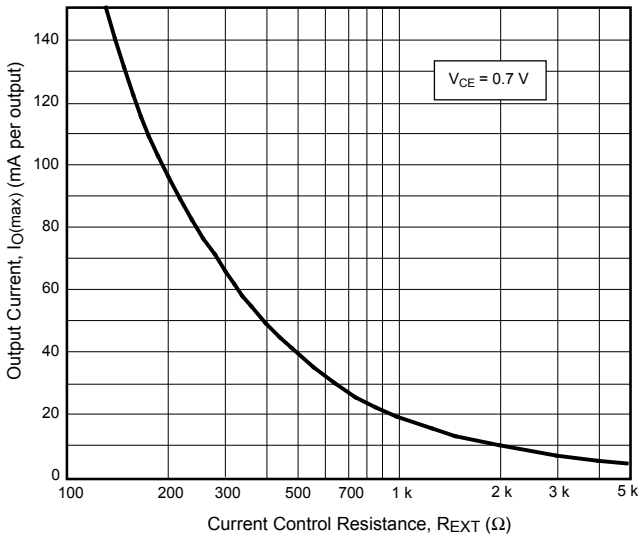

Figure 1. Output current at various values for the external current control resistor, REXT

8-Bit and 16-Bit Versions

The Allegro family of constant-current LED drivers is designed with shift registers and latches to allow direct interfacing with microprocessor-based systems, controlling outputs on the 8-bit level (A6275, A6277, and A6278) or 16-bit level (A6276 and A6279). All devices can be cascaded for additional drive lines when applications require more than 8 or 16 bits.

These alternatives offer the designer the flexibility to select the device best suited to a particular application. For example, the three 8-bit versions will find their way into LED indicators and bar graph displays. The two 16-bit versions will be employed in systems using displays ranging from 7-segment display elements to large programmable road signs and score boards.

Serial Input

To further reduce device terminal count and board space requirements, a serial input is utilized for direct interfacing with microprocessor-based systems, allowing data entry with only three terminals: SERIAL DATA IN, CLOCK, and LATCH ENABLE. These inputs drive the CMOS shift register and latches.

With the appropriate logic supply voltage, high data rates are possible, allowing use of a wide range of microprocessor products to perform the data input function. The maximum rates are shown in table 2.

The device SERIAL DATA OUT function enables the designer to cascade the devices for applications requiring more than 8 or 16 bits. With multiple devices, REXT can be trimmed to provide current matching between devices.

For applications requiring interdigit blanking, all output drivers can be disabled by setting the OUTPUT ENABLE input high (internal pull-up). The OUTPUT ENABLE input can also be used to operate the device at a duty cycle below 100%, allowing LEDs to be operated either for high peak currents or for power dissipation reduction—desirable features in some applications.

Table 2. Data input rate options for A62xx familiy

Device	Logic Supply, V_{DD} (V)	Maximum Data Rate (MHz)
A6275	5	10
A6276	5	10
A6277	5	10
A6278	3 to 5.5	25
A6279	3 to 5.5	25

Undervoltage Lockout

An A62xx feature that is not traditionally found on display drivers is internal undervoltage lockout (UVLO). This feature disables the driver outputs in the event that the logic supply voltage drops below a minimum acceptable level. This prevents the display of erroneous information, a necessary function for some critical applications.

Output Staggering Delay

The A6278 and A6279 have a 20 ns delay between each output. The staggering of the outputs reduces the in-rush of current on to the power and ground planes. This aids in power supply decoupling and EMI/EMC reduction.

The output staggering delay occurs under the following conditions:

- OUTPUT ENABLE is pulled low
- OUTPUT ENABLE is held low and LATCH ENABLE is pulled high
- OUTPUT ENABLE is held low, LATCH ENABLE is held high, and CLOCK is pulled high

The 20 ns delays are cumulative across all the outputs. Under any of the above conditions, the state of OUT0 gets set after a typical propagation delay, $t_{P(OE)}$. OUT1 will get set 20 ns after OUT0, and so forth. In the A6279, OUT15 will get set after 300 ns (15 × 20 ns) plus $t_{P(OE)}$.

Note: The maximum CLOCK frequency is reduced in applications where both the OUTPUT ENABLE pin is held low and the LATCH ENABLE pin is held high continuously, and the outputs change state on the CLOCK edges. The staggering delay could cause spurious output responses at CLOCK speeds greater than 1 MHz.

LED Open Circuit Detection Mode

The A6278 and A6279 also have LED Open Circuit Detection. When in this mode, an error bit is sent to the shift register corresponding to the open output where it can be clocked out of the SERIAL DATA OUT pin and read by a microprocessor (see the datasheet for a complete description of this feature).

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Thermal Considerations

The maximum allowable package power dissipation, $P_D(\text{max})$, is determined by the package thermal resistance, $R_{\theta JA}$, the operating ambient temperature, T_A (including factors such as heating from adjacent components, air circulation, etc.), and the maximum allowable junction temperature, $T_J(\text{max})$. The relationship between these parameters is:

$$P_D(\text{max}) = \frac{(T_J(\text{max}) - T_A)}{R_{\theta JA}} \quad . \tag{3}$$

Package thermal data is provided in the datasheets for the devices, and on the Allegro website, at http://www.allegromicro.com/techpub2/thrmlchr/thrmlchr.pdf. Although no strict rules exist regarding $T_J(\text{max})$, the absolute maximum allowable is 150°C. Typically, one should design for a maximum continuous junction temperature of 100°C to 130°C taking into consideration that every 10°C rise in junction temperature approximately halves the expected life of the device, and every 10°C decrease in junction temperature doubles the expected life of the device.

The actual package power dissipation, $P_{D(act)}$, is the sum of the power dissipation of the output drivers and of the logic elements, and is determined by:

$$P_{D(act)} = DC\,(V_{CE} \times I_O \times N) + (V_{DD} \times I_{DD}) \quad , \tag{4}$$

where

DC is the duty cycle,
V_{CE} is the difference between the LED supply voltage (V_{LED}) and the LED forward voltage (V_F), and
N is the quantity of device outputs (8 or 16).

When calculating power dissipation, the total quantity of available device outputs is usually used for the worst-case situation, and assuming all segments are illuminated (e.g., displaying all *8*s in a 7-segment display).

For circuit design, equations (3) and (4) can be combined and expanded as follows to calculate expected junction temperature:

$$T_J = R_{\theta JA}\{DC\,[(V_{LED} - V_F) \times I_O \times N] + [V_{DD} \times I_{DD}]\} + T_A \quad , \tag{5}$$

and simplified to:

$$T_J = R_{\theta JA} \times P_{D(act)} + T_A \quad . \tag{6}$$

Note that, except for V_{CE}, all of the quantities contributing to $P_{D(act)}$ (DC, I_O, N, V_{DD}, and I_{DD}) are generally defined by the requirements of the total system, rather than by the requirements of the A62xx device.

A Thermal Design Example

As a design example, an A6276xA (24-pin plastic DIP package) 16-bit (16-LED) driver is operated at an ambient temperature of 70°C. The design uses green LEDs, which have a forward voltage (V_F) of 2.0 V when operated at 15 mA (R_{EXT} = 1250 Ω) (see table 3 for typical V_F ratings for various LED colors). A 5.0 V supply provides the power for both the A6276 (at 20 mA) and the LEDs. From the datasheet, we see that $R_{\theta JA}$ = 50°C/W, so the junction temperature under these conditions can be calculated, using equation 5, as:

$$T_J \approx 50\{1[(5.0 - 2.0) \times 0.015 \times 16] + [5.0 \times 0.020]\} + 70 \approx 111°C \quad .$$

or, using formula 6:

$$T_J \approx 50°C/W \times 0.82\ W + 70°C \approx 111°C$$

With a junction temperature of 111°C, the device is well within its safe operating area. Conversely, the same equations can be used to calculate the maximum allowable output current under a given set of conditions.

To minimize the voltage drop across the driver output and thus reduce device power dissipation, it may be desirable to use external voltage dropping, using methods such as those shown in figure 2. Selection of the V_{DROP} value depends on the particular application and the level of LED current selected. In cases where the combination of supply voltage, V_{LED}, and LED voltage drop, V_F, results in a low voltage across the output driver, V_{CE}, external voltage dropping might not be required.

The A6275, 6276, and 6277 drivers are most effective when operated with a V_{CE} between 0.4 and 0.7 V. The 6278 and A6279 are most effective with a V_{CE} between 0.7 and 3.0 V. If the available voltage source will cause unacceptable dissipation and series resistors or diodes are undesirable, a regulator can be used.

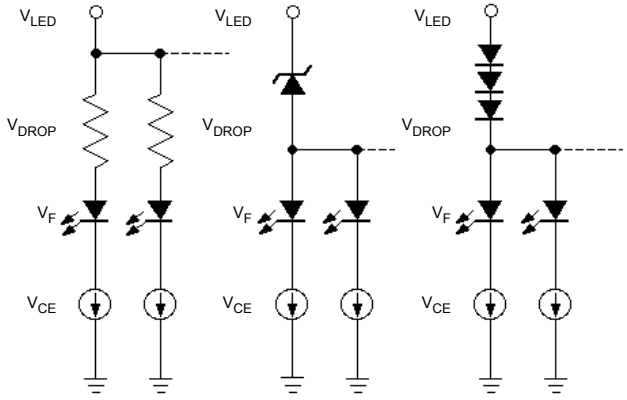

Figure 2. Methods of external voltage dropping that can be used to reduce package power dissipation

Table 3. Typical LED Forward Voltages

Color	Forward Voltage, V_F (V)
Amber	1.9 to 2.65
Blue	3.0 to 4.0
Green	1.8 to 2.2
Infrared	1.2 to 1.5
Red	1.6 to 2.25
White	3.5 to 4.0
Yellow	2.0 to 2.1

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In some applications it is desirable or required to operate the LEDs at a duty cycle below 100%, but with a higher peak current. Duty cycle control is achieved via the OUTPUT ENABLE terminal. Outputs are enabled when this input is pulled low.

Two-Digit Application

Figure 3 shows a two-digit application using the 16-bit A6276 and two 7-segment (plus decimal point) LEDs. In such an application, serial data is fed to the SERIAL DATA IN terminal, along with CLOCK and LATCH ENABLE signals. Additional digits can be driven by cascading drivers (SERIAL DATA OUT of one connected to SERIAL DATA IN of the next) with all CLOCK inputs tied together and all LATCH ENABLE inputs tied together.

Multiplexing Typical Application

Multiplexing is a popular solution for driving many digits. With the segments of all digits in parallel, only the desired digit is enabled (turned on) at one time. The array of digits is then scanned to sequentially enable each individual digit. Multiplexed displays must typically be operated at greatly increased current to obtain sufficient brightness.

Figure 4 shows a typical eight-digit, 7-segment application employing an A6275 with its output sink drivers controlling the segments and an Allegro source driver, UDN2981 or UDN2982, for digit control. Information to the display drivers is provided by a microprocessor or microcontroller that provides SERIAL DATA IN, CLOCK, and LATCH ENABLE signals.

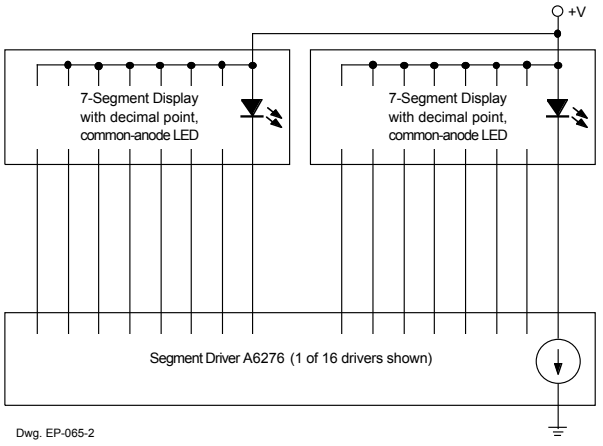

Figure 3. Typical application with 2 digits

In such a configuration, it is necessary to disable the display while the source driver switches from one digit to the next. This technique is called *interdigit blanking* and it is necessary in order to prevent partial illumination (ghosting) of segments intended to be off. This phenomena results from the source driver requiring more time to turn off than the sink driver takes to turn on. Blanking will delay the sink driver turn-on and will allow the source driver to turn off completely. This is performed with the OUTPUT ENABLE function.

More than eight digits, or more than 16 segments, will require additional source or sink drivers in a cascaded configuration.

REXT Selection

The A62xx family are constant-current output devices. To set the output current level, I_O, for all outputs, the value of the resistor used, REXT, can be selected based on either figure 1 or equation 2. In addition, the REXT resistor should be connected to ground as close as possible to the package.

Voltage Control of Output Current

In some applications, it may be desirable to control output current with a variable-voltage source. Alternatively, a voltage source can be used to drive several A62xx drivers at the same output currents. In either configuration, a microcontroller can provide digital information to a digital-to-analog converter (DAC), which provides an analog voltage to the A62xx driver in series with REXT (figure 5). With multiple devices, REXT can be trimmed to provide current-matching between devices.

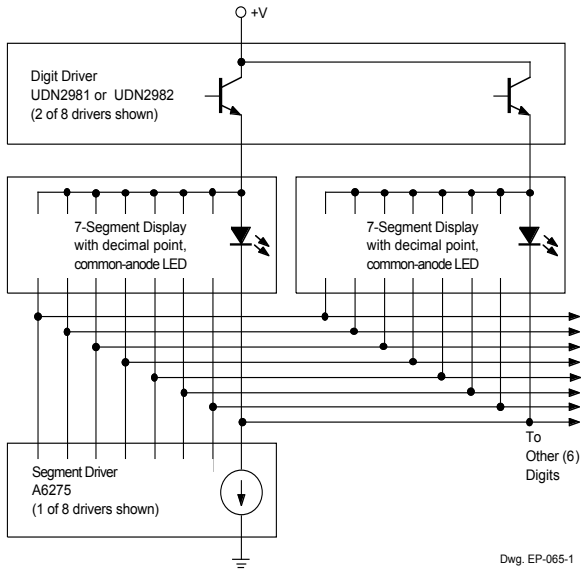

Figure 4. Typical application, multiplexed with 8 digits

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As determined in equation 1, the maximum output current, $I_O(max)$, is set by the series resistor REXT. From that level, the output current decreases as the control voltage, $V_{control}$, approaches the internal reference voltage, V_{REF}, according to the following relationship:

$$I_O(\text{max}) = \frac{CMR\,(V_{REF} - V_{control})}{R_{EXT}} \quad . \qquad (7)$$

where CMR and V_{REF} take the values shown in table 1. Note that, if $V_{control}$ is 0 V, I_O is determined by R_{EXT}, and if $V_{control}$ equals V_{REF}, I_O is zero. Again, special care must be taken to minimize capacitance from the REXT terminal, and the REXT resistor should be located as close as possible to the REXT terminal.

In addition to the above considerations, it is necessary that the DAC be capable of sinking the maximum mirrored load current for each LED driver, I_{EXT}, determined by the following formula:

$$I_{EXT} = I_O(\text{max}) \cdot CMR \; . \qquad (8)$$

For example, using the A6275, $I_{EXT} = I_O(max)/15.25$.

If an R_{EXT} of less than 250 Ω is required (>75 mA per driver output), then a small inductor in series with the resistor is usually advisable.

Pattern Layout

Except for the A6277, the A62xx devices have a common logic-ground (AGND) and power-ground (PGND) terminal. The A6277 has separate logic-ground and power-ground terminals that must be connected externally. R_{EXT} must be returned to the logic ground.

If the ground pattern layout contains large common-mode resistance, and the voltage between the system ground and the LATCH ENABLE or CLOCK terminals exceeds 2.5 V (because of switching noise), these devices may not operate correctly.

Separate AGND and PGND traces must be used to prevent unwanted PGND noise from affecting AGND. Examples are shown in figure 6.

Where multiple devices are cascaded, multilayer boards are recommended. Decoupling capacitors should be used liberally. Where multiple devices are cascaded, 0.1 µF should be placed on the logic supply pin of each device, and 10 µF placed between the common VLED line and the device ground at least every other device.

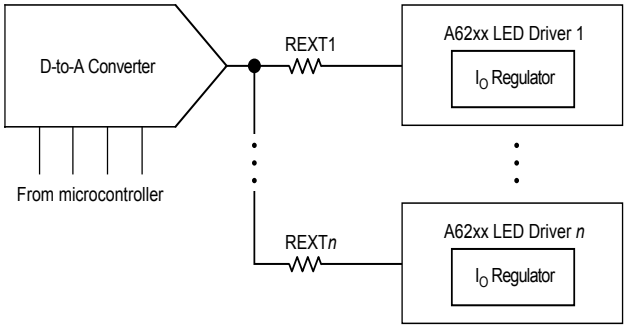

Figure 5. Voltage control of output current

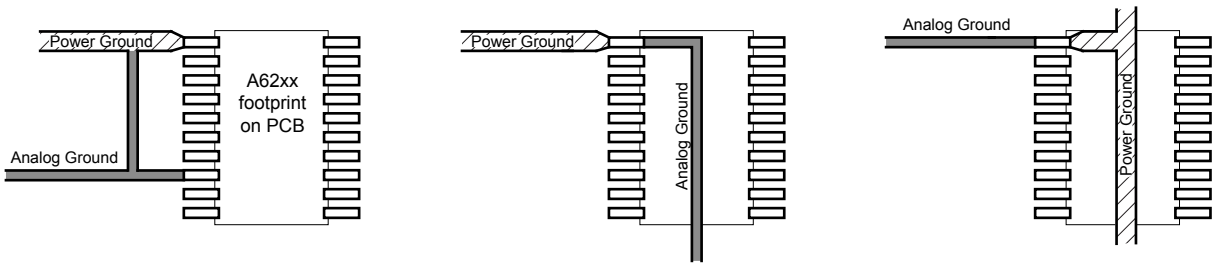

Figure 6. Examples of separate PGND and AGND traces

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