HDJD-J822

Method of Improving HDJD-J822 Brightness Change Response

AVAGO TECHNOLOGIES

Application Note 5272

Introduction

This application note describes a method to improve the brightness change response of the HDJD-J822 color management controller. This method is an extension to Application Note 5070 and can be optionally implemented. The color management system is fully functional with the instructions described in AN5070.

The benefit of implementing the described method is smoother change of brightness, especially when changing brightness levels by more than 10%. It does not significantly change the response time. So, it is still recommended that brightness changes are made with 10% steps (with 300~500ms duration between each step) even with this method in place. However, with this method, larger step changes are acceptable if a response time of a few seconds is allowed.

Description of Method

The objective of this method is to transfer the contents of six internal registers from one address to another. The transfer should take place at the start of step 38 described in AN5070; after RCAL bit 0 goes to '0', but before saving the calibration data into non-volatile memory.

Table 1. Register Transfer Steps

38.a1	Transfer register CALDATA19 (9Dh) to register TEMP1 (DAh).
38.a2	Transfer register CALDATA21 (9Fh) to register TEMP2 (DBh).
38.a3	Transfer register TEMP1 (DAh) to register CALDATA21 (9Fh).
38.a4	Transfer register TEMP2 (DBh) to register CALDATA19 (9Dh).
38.a5	Transfer register CALDATA20 (9Eh) to register TEMP1 (DAh).
38.a6	Transfer register CALDATA24 (A2h) to register TEMP2 (DBh).
38.a7	Transfer register TEMP1 (DAh) to register CALDATA24 (A2h).
38.a8	Transfer register TEMP2 (DBh) to register CALDATA20 (9Eh).
38.a9	Transfer register CALDATA23 (A1h) to register TEMP1 (DAh).
38.a10	Transfer register CALDATA25 (A3h) to register TEMP2 (DBh).
38.a11	Transfer register TEMP1 (DAh) to register CALDATA25 (A3h).
38.a12	Transfer register TEMP2 (DBh) to register CALDATA23 (A1h).

Use the I2C interface to perform the transfer.

TEMP1 and TEMP2 are temporary storage registers. The internal device registers located at addresses DAh and DBh can be used for TEMP1 and TEMP2. These two registers are spare registers only in open loop mode. Alternatively, TEMP1 and TEMP2 can be spare registers in the master controller.

After the transfer of the registers above is complete, the remainder step 38 of AN5070 can be executed. This is the complete instruction of this brightness change response improvement method.

I2C Command Interface Protocol

Figure 1 shows the structure of the command to specify the I2C write cycle and read cycle. This command structure will be used throughout the application note.

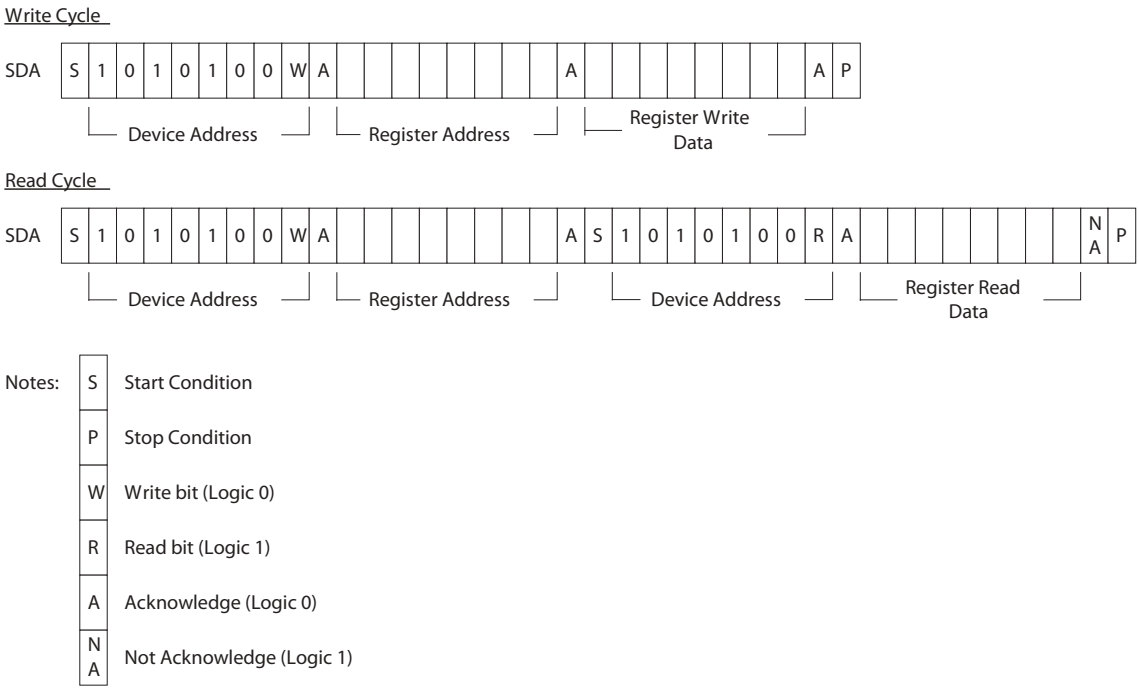

Figure 1. Write Cycle and Read Cycle Command Structure

Programming Guide

As shown in Figure 2, the transfer of the six internal registers should only start after RCAL (bit 0 of CTRL2 register) goes to "0". After transfer is completed, user should continue with the rest of Calibration Procedure Step 38 mentioned in AN5070, i.e. saving calibration data values to non volatile memory.

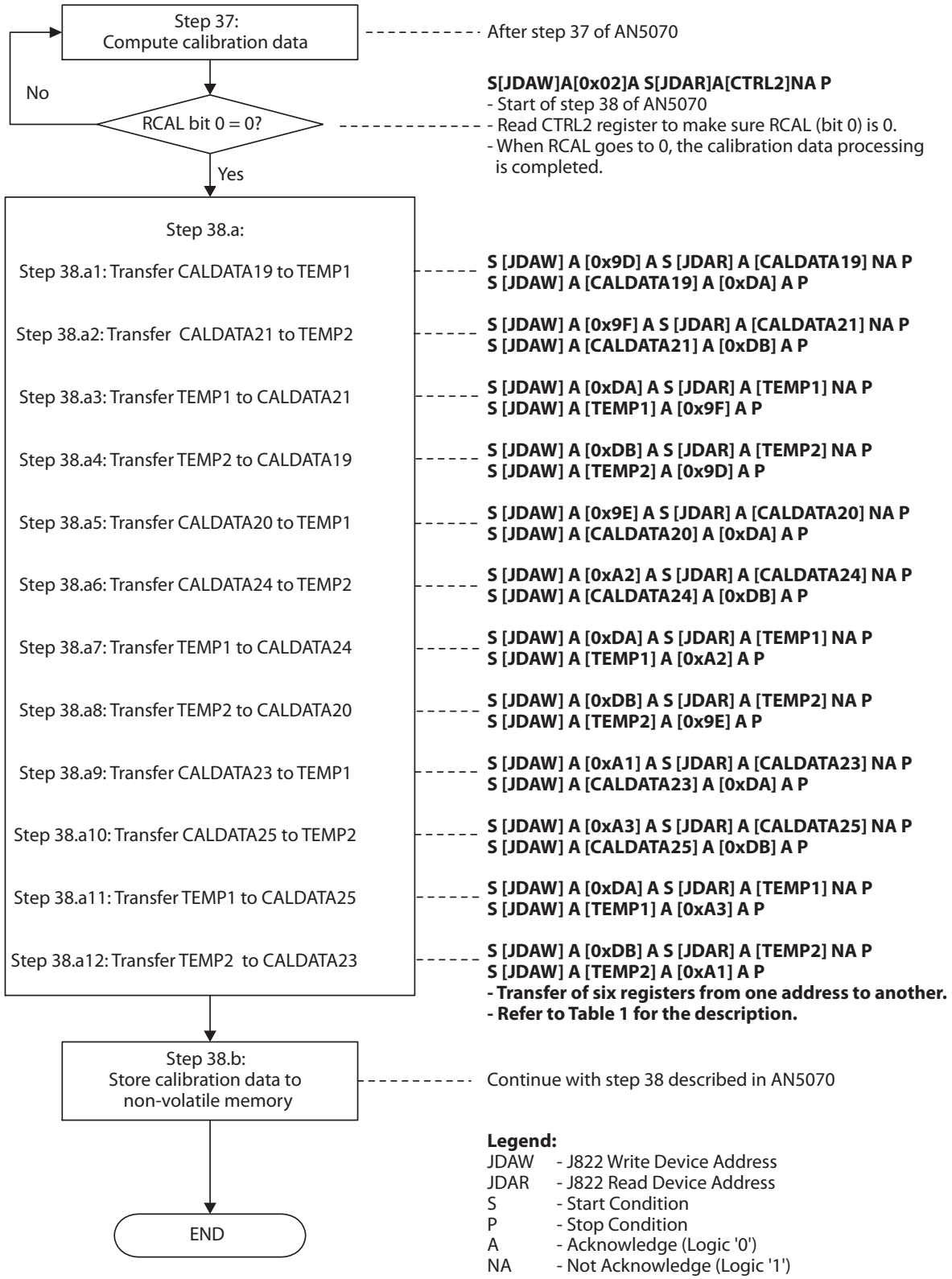

Figure 2. Register Transfer Flowchart

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AV01-0137EN - May 2, 2006