Using the HDJD-J822 Color Management System Feedback Controller ASIC

Application Note 5070

Introduction

The HDJD-J822 controls the proportion of light from three color light sources. These three color light sources come from red LED, green LED, and blue LED. Each color can be a single LED or an array of LEDs. These light sources are mixed to produce a resultant color. The mixing is done using optical components such as light guides or light panels. The light from all the LEDs must be thoroughly mixed. A sample of the mixed light provides the optical feedback, which is sensed by a color sensor with three channels, channel X, channel Y and channel Z. Normally, the channel X consists of the red part of the color sensor, channel Y consists of green part of the color sensor, and channel Z consists of blue part of the color sensor. The optical feedback allows the HDJD-J822 controller to produce a resultant color accurately. The color and brightness are maintained by adjusting each of the pulse width modulation, PWM_R, PWM_G, and PWM_B of the light sources.

A one time factory calibration provides the correlation between the CIE camera measurement and the color sensor used. The correlation will allow color to be specified in the CIE X, Y, Z color space, or related color spaces such as Yxy, Yu'v', and RGB. The calibration also ensures that accurate color and brightness matching is achieved when the same input set point is given to any HDJD-J822 based system.

For any application that does not require color accuracy or color matching between similar systems, the factory calibration may not be required and a default calibration can be used. The HDJD-J822 controls and maintains the color and brightness of the selected color. However, the color reproduced is not accurate when measured with a CIE camera. Also, between similar systems, the reproduced color may be different, although, the same color input is given to the HDJD-J822. The color difference is due to the variation in the three channel sensors (or color sensors), variation in the three channel color light sources, and hardware differences such as optical light guides etc.

Typical Design

A simplified design is shown in Figure 1. The only components needed are capacitors, resistors, and a color sensor. Push button switches will be needed only if the COLOR and BRIGHT button mode operation is needed. Otherwise, the push button switches can be omitted and both the COLOR and BRIGHT pins are tied directly to DVSS.

The control signals consist of SDA, SCL, XRST, SLEEP, and ERR_FLAG. The control signals SDA and SCL provide the I2C interface to read or write the internal registers.

SLEEP can be asserted when the HDJD-J822 is in idle mode in power sensitive application. The ERR_FLAG signals to the processor that there is an error and the type is determined by reading the ERROR register.

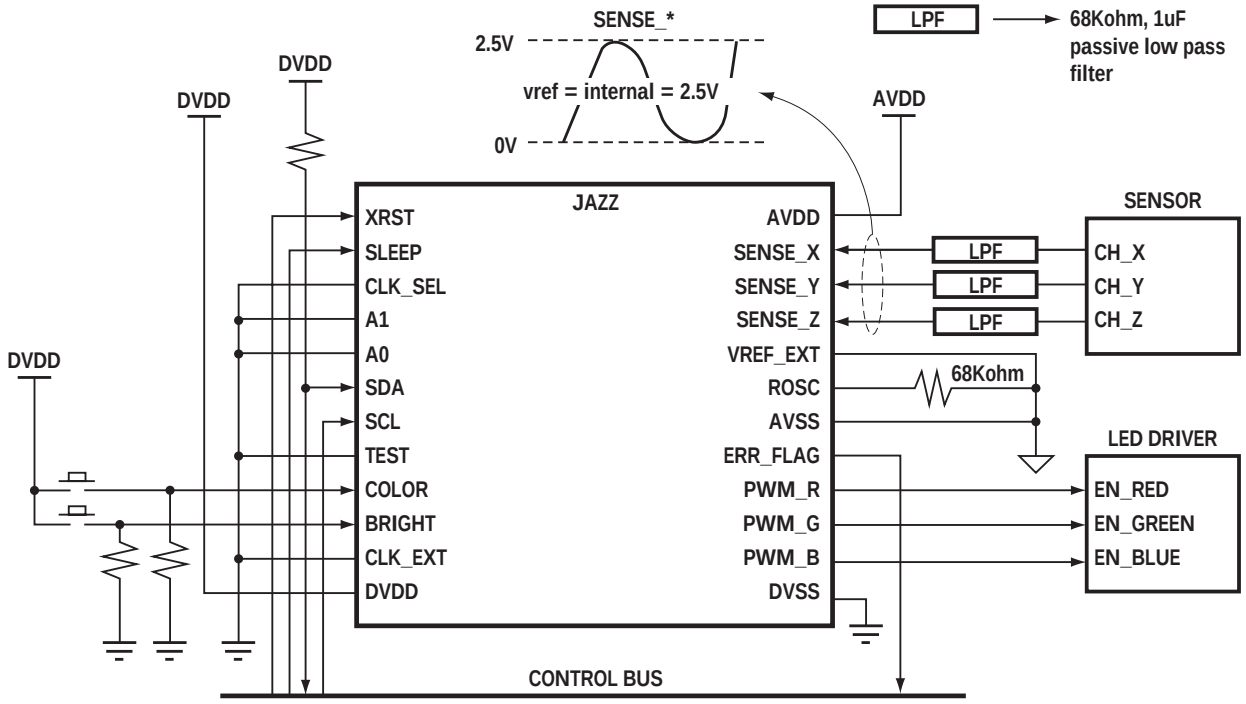

Figure 1. Typical design.

Sensor Circuit & Low Pass Filter

The sensor has three channels, CH_X (Channel_X), CH_Y (Channel_Y), and CH_Z (Channel_Z). Normally, channel X refers to red, channel Y refers to green, and channel Z refers to blue channel of the color sensor. Since the LEDs are controlled by pulse width modulation output from the HDJD-J822, the sensor output will also be pulse width modulated. Each sensor channel needs to be averaged by passing the sensor output voltage through a low pass filter. The selection of the RC components is done so that the base PWM frequency is suppressed at least –40 dB at the output of the low pass filter.

The cut-off frequency for a simple low pass filter, f_{3dB} is given by: $\frac{1}{2 \cdot \pi \cdot R \cdot C}$

This f_{3dB} should be at a minimum of –40 dB at the operating pulse width modulation frequency. Since the low pass filter cutoff roll off at –20 dB per decade, we need two decades to meet this requirement. f_{3dB} must be below 610/100 = 6.1 Hz.

Taking R value at 68 kΩ, C > 0.39 µF. A 1 µF capacitor should therefore be sufficient.

Color Sensor

The color sensor must be placed in a location where

a) All light from all the LEDs are thoroughly mixed, and
b) The position is best in achieving as equal as possible, light contribution from all LEDs to the color sensor.

When all the red, green, and blue LEDs are on, the SENSOR_ADCZ, SENSOR_ADCY, and SENSOR_ADCX registers value must be checked. These registers (84h-89h) store the analog to digital converter values of the three sensor voltages after the GSSR (bit 1) of the CTRL2 register is set to '1'. (Refer to step 8 and 9 of the calibration procedure). All the three analog to digital converter values should range from 190h to 320h or decimal 400 to 800 for proper operation.

If any of the sensor voltages is above the internal ADC voltage reference, or any of the SENSOR_ADC values are greater than 800, the following can be taken.

a) Decrease the peak LED current of the saturated channel.

b) Increase the distance between the sensing area and the sensor. Ensure no external ambient light interference if this is done.

c) Insert neutral density grey filter.

d) Reduce the gain of the sensor channel voltage.

e) Use a higher external voltage reference.

f) Use an external operational amplifier to get the sensor voltages below the voltage reference.

Oscillator Circuit

The HDJD–J822 require a resistor connection to AVSS if the internal oscillator is to be used. The recommended resistor is 68 kΩ for the nominal oscillator frequency of 2.5 MHz and a PWM frequency of 610 Hz.

LED Driver

A wide variety of LED drivers are available in the market. As long as the LED driver has an output enable input that can be pulse width modulated, it can be used.

The assertion level of the PWM signals can be changed by the user to support either active-low or active-high enable inputs pins at the LED driver side. This is done by programming the PWML (bit 1) of the CONFIG1 register.

After power on or software reset, the default PWML bit is set to '0'. The LEDs will be turned off for design which uses active high enable LED drivers. For active low LED driver enable design, the LED driver will turn on briefly until the PWML bit is set to '1'.

LEDs and Color Gamut

The red, green, and blue LEDs used will specify the color gamut of the system. The color gamut is measured during calibration. The three points obtained in step 17, 23, and 29 of the calibration procedure represent the color gamut on the CIE color chart.

Button Mode Operation

The button mode is applicable in only the RGB color space (default color space after power on or software reset).

The two buttons allow selection of color and brightness using the human eye.

If button control is the primary color and brightness selector, calibration is usually not needed. HDJD-J822 will maintain the color and brightness of the selected color.

The color button allows selection of color while maintaining the brightness. The color selected can start anywhere on the color path. Pressing color and bright buttons together for a short duration will change the path direction. If the path previously is from green to cyan to white to cyan to blue to purple to red to yellow and back to green again, the direction change means color will change from green to yellow to red to purple to blue to cyan to white to cyan and back to green. For faster color change, press and hold the color button.

The default direction after power on or software reset is green to cyan to white to cyan to blue to purple to red to yellow and back to green.

For brightness, the luminance will increase or decrease while maintaining the color set point. The direction is either increment or decrement. To toggle the direction, press both color and bright buttons together for a short duration. If the luminance has been increasing, pressing both the color and bright buttons together will change the direction to decrement. On releasing the color button and pressing the bright button, the brightness will be decreased. For faster change in brightness, press and hold the bright button.

The default brightness direction after power on or software reset is increment. Since the default brightness is already at maximum, pressing the bright button after power on or software reset will not produce any noticeable change in brightness.

Sleep Mode

The PWM generator for the LED drivers must be shut off before activating the Sleep mode by setting the Sleep pin to logic high. Write CTRL1 register with 00h to turn off the PWM generator. This will set the PWME bit to logic low.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	0

Figure 2. CTRL1 format. Address 01h.

Note: The current color and brightness set point will be maintained while the device is in sleep mode.

To turn sleep mode off, the sleep pin is set to logic low. The PWME bit in CTRL1 register may be set to logic high to turn on the PWM generator, by writing CTRL1 register with 02h. The previous set point prior to sleep mode will be displayed.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	1	0

Figure 3. CTRL1 format. Address 01h.

Programming Methodology

Before the HDJD-J822 can be used in controlling color and brightness, a one time calibration is generally required to obtain thirty-one calibration data values: CALDATA0 to CALDATA30. These values need to be saved in non volatile memory, as they need to be read back during normal operation. The method is described in Calibration Procedure section.

Figure 4 shows the flowchart for the calibration procedure.

After calibration, users need to read back the saved thirty-one calibration data from non volatile memory. The thirty-one calibration data from non-volatile memory are written to the corresponding thirty-one HDJD-J822 CALDATA0 to CALDATA30 registers. (address 8Ah to A8h). A color set point and a brightness scaling level is selected to obtain the color and brightness desired. This method is described in Normal Operating Procedure.

Calibration Procedure

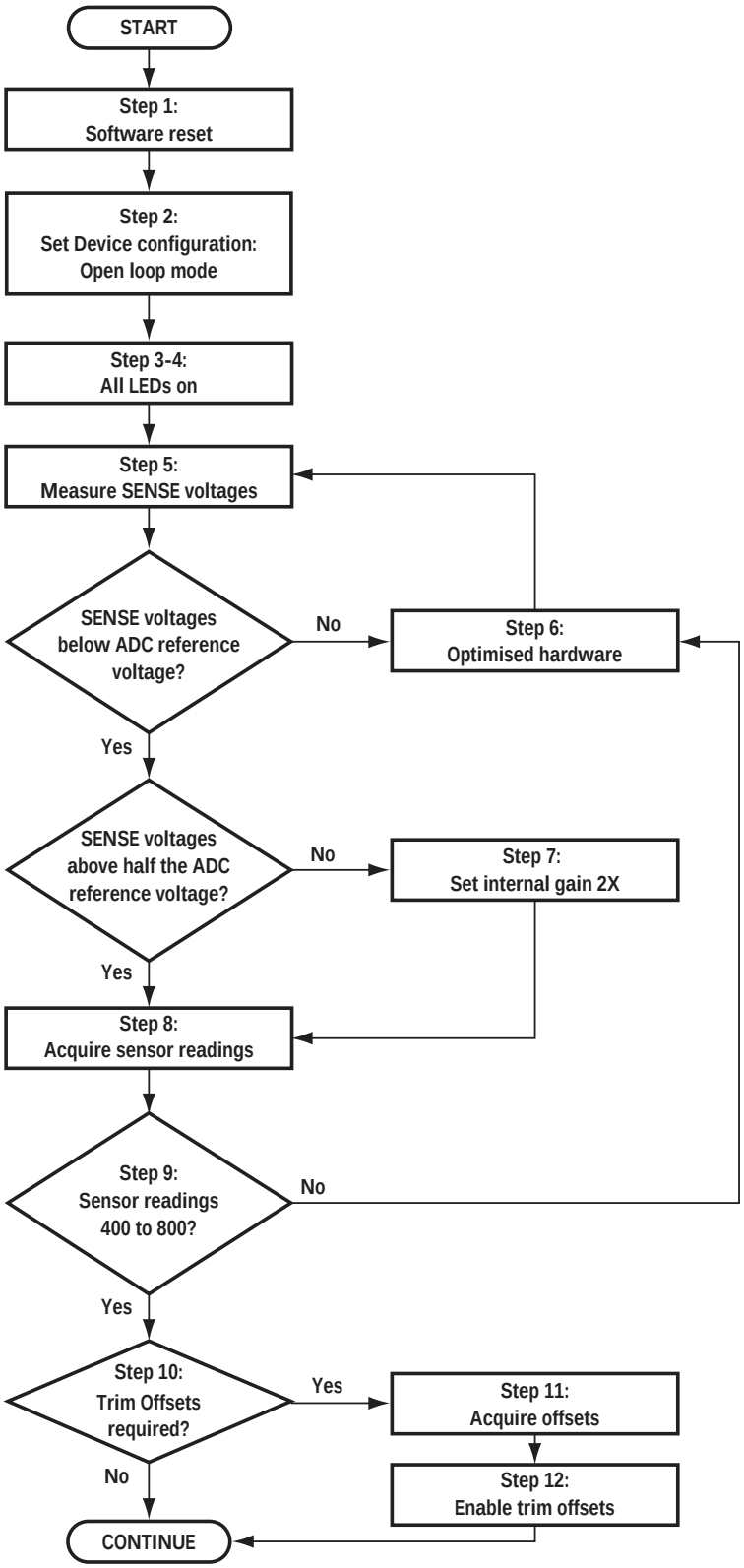

Figure 4. Calibration flow chart.

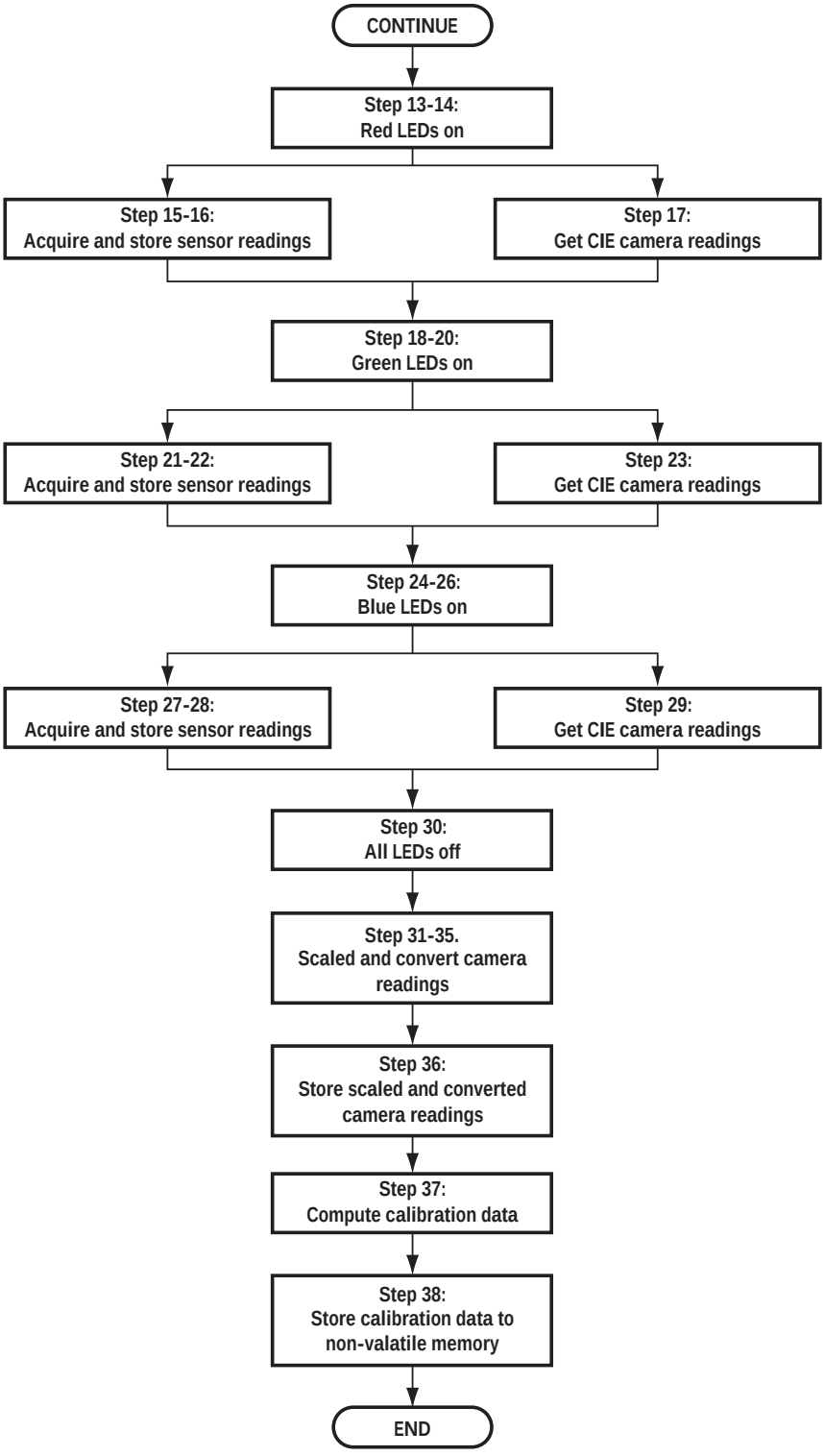

Figure 4. Calibration flow chart (continued).

The procedure for calibration is as follows.

1) First perform a power on reset or software reset by writing CTRL1 register with 01h.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	1

Figure 5. CTRL1 format. Address 01h.

Read the INIT (bit 0) value of the STATUS register, (address 09h). When INIT bit is '0', power on or software reset is completed. The DUTYR_LO, DUTYR_HI, DUTYG_LO, DUTYG_HI, DUTYB_LO, and DUTYB_HI register values will be set to '0'. The PWME bit of CTRL1 register will also be set to '0'. This should turn off all the red, green, and blue LEDs for active high LED driver design.

However, for active low LED driver design, all the red, green, and blue LEDs will turn on after power on or software reset. The PWML (bit 1) of CONFIG1 register must be set to '1'.

2) Write CONFIG1 register to set the device to open loop mode so that the calibration can be done. Note that TOFS bit is set to '0' as the offsets have not been measured.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	RSV	OPMD	TOFS	RSV	SSLP	PWML	VREFS
Value	0	0	1	0	0	Note a	Note b	Note c

Figure 6. CONFIG1 format. Address 03h.

Note:

a) Set SSLP bit: '0' for positive slope sensor, '1' for negative slope sensor.

b) Set PWML bit: '0' for PWM active high, '1' for PWM active low.

c) Set VREFS bit: '0' for internal voltage reference, '1' for external voltage reference.

d) RSV bit is reserved bit. Value is '0'.

After CONFIG1 register is written, all the red, green, and blue LEDs should turn off.

The status register (address 09h) can be read to verify that the OPENL (bit 2) is set to "1" before proceeding with the calibration.

3) Write DUTYR_LO, DUTYG_LO, and DUTYB_LO registers with FFh. Write DUTYR_HI, DUTYG_HI, and DUTYB_HI registers with 0Fh. I.e. The DUTYR, DUTYG, and DUTYB registers are written with 0FFFh or decimal 4095.

Bit	7	6	5	4	3	2	1	0
DUTYR_LO Value	1	1	1	1	1	1	1	1
DUTYR_HI Value	0	0	0	0	1	1	1	1
DUTYG_LO Value	1	1	1	1	1	1	1	1
DUTYG_HI Value	0	0	0	0	1	1	1	1
DUTYB_LO Value	1	1	1	1	1	1	1	1
DUTYB_HI Value	0	0	0	0	1	1	1	1

Figure 7. Address 0Bh to 10h.

4) Write CTRL1 register with 02h to enable PWM and all the LEDs will turn on at 100% duty cycle.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	1	0

Figure 8. CTRL1 format. Address 01h.

5) Measure the SENSE voltages at SENSE_X, SENSE_Y, and SENSE_Z pins. Check that the SENSE_X, SENSE_Y, and SENSE_Z voltages are below the ADC voltage reference.

6) If the sensor voltages are above the ADC voltage reference, optimized the hardware. Refer to sensor voltage requirement section for tips to get the SENSE voltages below the ADC voltage reference.

7) Decide whether to use the internal gain (i.e. GAINX, GAINY, or GAINZ bits of CONFIG2). If not used, set the gain bit to '0'. For color sensor with positive coefficient sensor slope, if the SENSE voltages are below 0.39 times the ADC voltage reference, the appropriate gain bit for that channel should be set to '1' to enable 2X gain. I.e.,
   If SENSE_X is below 0.39 times the ADC voltage reference, the GAINX should be set to '1'.
   If SENSE_Y is below 0.39 times the ADC voltage reference, the GAINY should be set to '1'.
   If SENSE_Z is below 0.39 times the ADC voltage reference, the GAINZ should be set to '1'.
   This is done by writing bit 5 to 7 of the CONFIG2 register with the value shown in Table 1.

   For color sensor with negative coefficient sensor slope, the gain bits are always set to '0'.

   The CONFIG2 register format is as follows.

Bit	7	6	5	4	3	2	1	0
Mnemonic	GAINX	GAINY	GAINZ	RSV	RGB	Yu'v'	Yxy	XYZ
Value	Refer to Table 1			0	0	0	0	0

Figure 9. CONFIG1 format. Address 04h.

Note:

a) RSV is reserved bit. Value is '0'.
b) Bit 0 to bit 3 of the CONFIG2 register is written '0' as they are not used in calibration mode.
c) **If the internal gain for any channel is used during calibration, it must also be used during normal operating mode for that channel.**

Table 1 shows the CONFIG2 values for the different setting of gain bits.

Table 1. Gain selector and CONFIG2 values.

GAINX	GAINY	GAINZ	CONFIG2 value
0	0	0	00h
0	0	1	20h
0	1	0	40h
0	1	1	60h
1	0	0	80h
1	0	1	A0h
1	1	0	C0h
1	1	1	E0h

8) After GAIN selector has been decided, write CTRL2 register with 02h.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL
Value	0	0	0	0	0	0	1	0

Figure 10. CTRL2 format. Address 02h.

9) When bit 1 (GSSR) of CTRL2 register goes '0', read SENSOR_ADCZ_LO, SENSOR_ADCZ_HI, SENSOR_ADCY_LO, SENSOR_ADCY_HI, SENSOR_ADCX_LO, and SENSOR_ADCX_HI. For proper operation, these sensor values should range from 190h and 320h, or decimal 400 to 800.

10) Write CTRL1 register with 00h to disable PWM and turn off all LEDs.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	0

Figure 11. CTRL1 format. Address 01h.

If offset trimming is not used, step 11 and 12 can be ignored.

11) Offsets are sensor channel values when all LEDs are off. If offset trimming is to be used, write CTRL1 register with 08h to measure the offsets.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	1	0	0	0

Figure 12. CTRL1 bit format. Address 01h.

12) Read CTRL1 register. When GOFS bit goes '0', offsets are stored in OFFSET_X, OFFSET_Y, and OFFSET_Z register. The bit 4 (TOFS) of CONFIG1 register has to be set to '1' if offset trimming is used.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	RSV	OPMD	TOFS	RSV	SSLP	PWML	VREFS
Value	0	0	1	1	0	Note a	Note b	Note c

Figure 13. CONFIG1 format. Address 03h.

Note:

a) Set SSLP bit: '0' for positive slope sensor, '1' for negative slope sensor.

b) Set PWML bit: '0' for PWM active high, '1' for PWM active low.

c) Set VREFS bit: '0' for internal voltage reference, '1' for external voltage reference.

d) RSV bit is reserved bit. Value is '0'.

13) Write DUTYR_LO with FFh. Write DUTYR_HI with 0Fh. Write DUTYG_HI, DUTYG_LO, DUTYB_HI, and DUTYB_LO with 00h. This will only turn on the red LEDs at 100% duty cycle. Green and blue LEDs will be turned off.

Bit	7	6	5	4	3	2	1	0
DUTYR_LO Value	1	1	1	1	1	1	1	1
DUTYR_HI Value	0	0	0	0	1	1	1	1
DUTYG_LO Value	0	0	0	0	0	0	0	0
DUTYG_HI Value	0	0	0	0	0	0	0	0
DUTYB_LO Value	0	0	0	0	0	0	0	0
DUTYB_HI Value	0	0	0	0	0	0	0	0

Figure 14. DUTY registers. Address 0Bh to 10h.

14) Write CTRL1 register with 02h to enable PWM and turn on red LEDs at 100% duty cycle.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	1	0

Figure 15. CTRL1 format. Address 01h.

15) Write CTRL2 register with 02h to set GSSR to ‘1’.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL
Value	0	0	0	0	0	0	1	0

Figure 16. CTRL2 format. Address 02h.

16) When bit 1 (GSSR) of CTRL2 register goes to '0', read SENSOR_ADCZ_LO, SENSOR_ADCZ_HI, SENSOR_ADCY_LO, SENSOR_ADCY_HI, SENSOR_ADCX_LO, and SENSOR_ADCX_HI. These values are obtained when red LEDs are on. These sensor values need to be written to input registers in Table 2 before calibration data processing.

Table 2. Sensor measurement and register storage before calibration data processing when red LEDs are on.

SENSOR Measurement	Register to Store for Processing
SENSOR_ADCZ_LO	CAL_SMZR_LO
SENSOR_ADCZ_HI	CAL_SMZR_HI
SENSOR_ADCY_LO	CAL_SMYR_LO
SENSOR_ADCY_HI	CAL_SMYR_HI
SENSOR_ADCX_LO	CAL_SMXR_LO
SENSOR_ADCX_HI	CAL_SMXR_HI

17) Obtain the CIE camera measurement in CIE Y, x, y, or X, Y, Z. If the measurement is in Y, x, y, it should be converted to X, Y, Z using the equations below.

$X = (Y/y) * x$
$Z = (Y/y) * (1 - x - y)$
$Y = Y$

18) Write CTRL1 register with 00h to disable PWM and turn off all LEDs.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	0

Figure 17. CTRL1 format. Address 01h.

19) Write DUTYG_LO with FFh. Write DUTYG_HI with 0Fh. Write DUTYR_HI, DUTYR_LO, DUTYB_HI, and DUTYB_LO with 00h. This will only turn on the green LEDs at 100% duty cycle. Red and blue LEDs will be turned off.

Bit	7	6	5	4	3	2	1	0
DUTYR_LO Value	0	0	0	0	0	0	0	0
DUTYR_HI Value	0	0	0	0	0	0	0	0
DUTYG_LO Value	1	1	1	1	1	1	1	1
DUTYG_HI Value	0	0	0	0	1	1	1	1
DUTYB_LO Value	0	0	0	0	0	0	0	0
DUTYB_HI Value	0	0	0	0	0	0	0	0

Figure 18. DUTY registers. Address 0Bh to 10h.

20) Write CTRL1 register with 02h to enable PWM and turn on green LEDs at 100% duty cycle.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	1	0

Figure 19. CTRL1 format. Address 01h.

21) Write CTRL2 register with 02h to set GSSR to '1'.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL
Value	0	0	0	0	0	0	1	0

Figure 20. CTRL2 format. Address 02h.

22) When bit 1 (GSSR) of CTRL2 register goes to '0', read SENSOR_ADCZ_LO, SENSOR_ADCZ_HI, SENSOR_ADCY_LO, SENSOR_ADCY_HI, SENSOR_ADCX_LO, and SENSOR_ADCX_HI. These values are obtained when green LEDs are on.
These sensor values need to be written to input registers in Table 3 before calibration data processing.

Table 3. Sensor measurement and register storage before calibration data processing when green LEDs are on.

SENSOR Measurement	Input Register to Store before Processing
SENSOR_ADCZ_LO	CAL_SMZG_LO
SENSOR_ADCZ_HI	CAL_SMZG_HI
SENSOR_ADCY_LO	CAL_SMYG_LO
SENSOR_ADCY_HI	CAL_SMYG_HI
SENSOR_ADCX_LO	CAL_SMXG_LO
SENSOR_ADCX_HI	CAL_SMXG_HI

23) Obtain the CIE camera measurement in CIE Y, x, y, or X, Y, Z. If the measurement is in Y, x, y, it should be converted to X, Y, Z.

24) Write CTRL1 register with 00h to disable PWM and turn off all LEDs.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	0

Figure 21. CTRL1 format. Address 01h.

25) Write DUTYB_LO with FFh and DUTYB_HI with 0Fh. Write DUTYR_HI, DUTYR_LO, DUTYG_HI and DUTYG_LO with 00h. This will only turn on the blue LEDs at 100% duty cycle. Red and green LEDs will be turned off.

Bit	7	6	5	4	3	2	1	0
DUTYR_LO Value	0	0	0	0	0	0	0	0
DUTYR_HI Value	0	0	0	0	0	0	0	0
DUTYG_LO Value	0	0	0	0	0	0	0	0
DUTYG_HI Value	0	0	0	0	0	0	0	0
DUTYB_LO Value	1	1	1	1	1	1	1	1
DUTYB_HI Value	0	0	0	0	1	1	1	1

Figure 22. DUTY registers. Address 0Bh to 10h.

26) Write CTRL1 register with 02h to enable PWM and turn on blue LEDs at 100% duty cycle.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	1	0

Figure 23. CTRL1 format. Address 01h.

27) Write CTRL2 register with 02h to set GSSR to ‘1’.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL
Value	0	0	0	0	0	0	1	0

Figure 24. CTRL2 format. Address 02h.

28) When bit 1 (GSSR) of CTRL2 register goes to ‘0’, read SENSOR_ADCZ_LO, SENSOR_ADCZ_HI, SENSOR_ADCY_LO, SENSOR_ADCY_HI, SENSOR_ADCX_LO, and SENSOR_ADCX_HI. These values are obtained when blue LEDs are on. These sensor values need to be written to input registers in Table 4 before calibration data processing.

Table 4. Sensor measurement and register storage before calibration data processing when blue LEDs are on.

SENSOR Measurement	Input Register to Store before Processing
SENSOR_ADCZ_LO	CAL_SMZB_LO
SENSOR_ADCZ_HI	CAL_SMZB_HI
SENSOR_ADCY_LO	CAL_SMYB_LO
SENSOR_ADCY_HI	CAL_SMYB_HI
SENSOR_ADCX_LO	CAL_SMXB_LO
SENSOR_ADCX_HI	CAL_SMXB_HI

29) Obtained the CIE camera measurement in CIE Y, x, y, or X, Y, Z. If the measurement is in Y, x, y, it should be converted to X, Y, Z.

30) Write CTRL1 register with 00h to disable PWM and turn off all LEDs.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	0

Figure 25. CTRL1 format. Address 01h.

31) The X, Y, Z values obtained in step 17 for red LED, step 23 for green LED, and step 29 for blue LED are tabulated in Table 5. The subscript represents the LED color that was turned on during measurement.

Table 5. Tabulated camera measurements.

Red LED on (step 17)	Green LED on (step 23)	Blue LED on (step 29)
X_R	X_G	X_B
Y_R	Y_G	Y_B
Z_R	Z_G	Z_B

32) The maximum value of the set $\{X_R, Y_R, Z_R, X_G, Y_G, Z_G, X_B, Y_B, Z_B\}$ is determined. Assume that the maximum value is V_M.

33) Decide on the camera scale depending on the application. Table 6 provides a guide on the selection of the camera scale.

Table 6. Camera scale selection guide.

Application	Camera scale
White only or several white points display	1000
Multi color display	700

The scale ratio is obtained by the equation below:

$$\text{Scale ratio} = \frac{\text{camera scale}}{V_M}$$

34) This scale ratio is saved for correlation to actual CIE values in normal operating mode.

35) All the elements of the set $\{X_R, Y_R, Z_R, X_G, Y_G, Z_G, X_B, Y_B, Z_B\}$ are multiplied by this scale ratio and converted to hexadecimal. Let the scaled and converted hexadecimal value be the set $\{X_{RH}, Y_{RH}, Z_{RH}, X_{GH}, Y_{GH}, Z_{GH}, X_{BH}, Y_{BH}, Z_{BH}\}$.

36) These values are stored to the following registers prior to calibration data processing as shown in Table 7.

Table 7. Camera measurements and register storage before calibration data processing.

Camera Value (step 31)	Scale and Converted Hexadecimal Value (step 35)	Input Register to Store	
		Upper 2 bits	Lower 8 bits
X_R	X_{RH}	CAL_CMXR_HI	CAL_CMXR_LO
Y_R	Y_{RH}	CAL_CMYR_HI	CAL_CMYR_LO
Z_R	Z_{RH}	CAL_CMZR_HI	CAL_CMZR_LO
X_G	X_{GH}	CAL_CMXG_HI	CAL_CMXG_LO
Y_G	Y_{GH}	CAL_CMYG_HI	CAL_CMYG_LO
Z_G	Z_{GH}	CAL_CMZG_HI	CAL_CMZG_LO
X_B	X_{BH}	CAL_CMXB_HI	CAL_CMXB_LO
Y_B	Y_{BH}	CAL_CMYB_HI	CAL_CMYB_LO
Z_B	Z_{BH}	CAL_CMZB_HI	CAL_CMZB_LO

The measured sensor values obtained in step 16, 22, and 28, and the scaled and converted hexadecimal camera values in step 36 have already been written to the HDJD-J822 registers listed in Table 14 of appendix 1. Table 14 consists of input data from Table 2, 3, 4, and 7 grouped together.

37) Write CTRL2 register with a value of 01h (i.e. RCAL bit 0 of CTRL2 register is set to '1'). This will start processing of the calibration data.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL
Value	0	0	0	0	0	0	0	1

Figure 26. CTRL2 format. Address 02h.

38) When RCAL bit 0 goes to '0', the calibration data processing is completed. Users should save the calibration data values to non volatile memory. The calibration data values consist of 31 registers: CALDATA0 to CALDATA30. (i.e. register address 8Ah to A8h). These data must be entered back in normal operating mode to overwrite the default value after power on reset or software reset.

Normal Operating Procedure

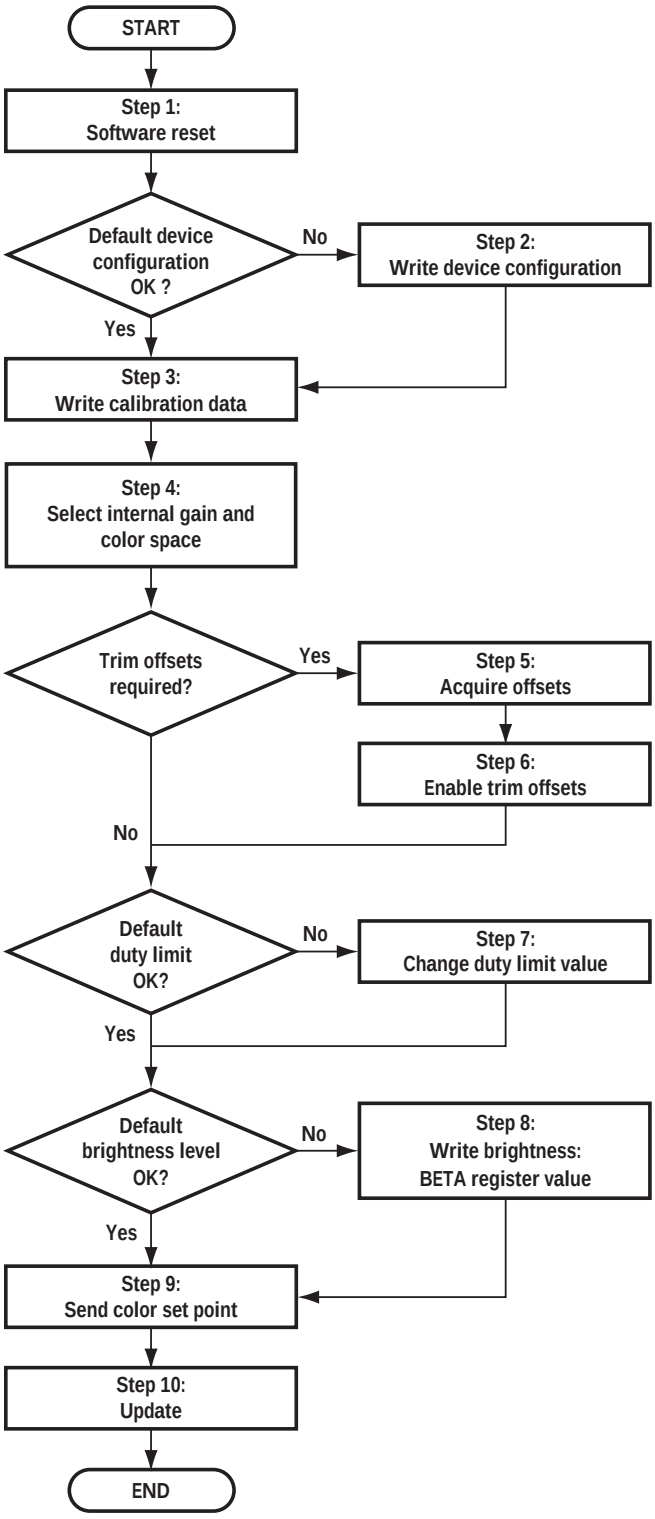

Figure 27. Flowchart for normal procedure.

The procedure for normal operating mode is as follows.

1) Do a power on reset or perform software reset. Software reset is done by writing CTRL1 with 01h (i.e. setting RSW to '1').

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	0	0	0	1

Figure 28. CTRL1 format. Address 01h.

Read the INIT (bit 0) value of the STATUS register, (address 09h). When INIT bit is '0', power on or software reset is completed. The PWME bit of CTRL1 register after reset will be set to '0'. This should turn off all the red, green, and blue LEDs for active high LED driver design.

However, for active low LED driver design, all the red, green, and blue LEDs will turn on after power on or software reset. The PWML (bit 1) of CONFIG1 register must be set to '1'.

2) Write the CONFIG1 register to change default value if necessary. The OPMD is set to '0' for normal operation. The TOFS bit is set to '0' as the offsets have not been measured.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	RSV	OPMD	TOFS	RSV	SSLP	PWML	VREFS
Value	0	0	0	0	0	Note a	Note b	Note c

Figure 29. CONFIG1 format. Address 03h.

Note:
a. Set SSLP bit: '0' for positive slope sensor, '1' for negative slope sensor
b. Set PWML bit: '0' for PWM active high, '1' for PWM active low
c. Set VREFS bit: '0' for internal voltage reference, '1' for external voltage reference
d. RSV bit is reserved bit. Value is '0'.
After CONFIG1 register is written, all the red, green, and blue LEDs should turn off.

3) Read the thirty-one calibration registers from non volatile memory. Write the values to the 31 calibration data registers (address 8Ah to A8h).

4) Write CONFIG2 register to select the internal gain and the color space.

Bit	7	6	5	4	3	2	1	0
Mnemonic	GAINX	GAINY	GAINZ	RSV	RGB	Yu'v'	Yxy	XYZ
Value	Refer to Table 1			0	Note b	Note b	Note b	Note b

Figure 30. CONFIG2 register. Address 04h.

a) GAINX, GAINY, and GAINZ with the setting chosen during calibration procedure in step 7 of calibration procedure.
b) Set ONLY one bit from RGB, Yu'v', Yxy and XYZ to '1' to select the set point color space. The rows in Table 8 show the color space and the value to be written for bit 0 to bit 3 of the CONFIG2 register.

Table 8. Color space selection and values for bit 0 to 3 of CONFIG2 register.

Chosen Color Space	CONFIG2 Bit Mnemonic	3 RGB	2 Yu'v'	1 Yxy	0 XYZ
RGB	Value	1	0	0	0
Yu'v'	Value	0	1	0	0
Yxy	Value	0	0	1	0
XYZ	Value	0	0	0	1

E.g. To select RGB, the CONFIG2 register will be written as follows.

Bit	7	6	5	4	3	2	1	0
Mnemonic	GAINX	GAINY	GAINZ	RSV	RGB	Yu'v'	Yxy	XYZ
Value	Refer to Table 1			0	1	0	0	0

Figure 31. CONFIG2 register. Address 04h.

If offset trimming is not used, step 5 and 6 can be ignored.

5) If offset trimming is to be used, write CTRL1 register with 08h.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	0	1	0	0	0

Figure 32. CTRL1 format. Address 01h.

When GOFS bit goes to '0', offsets are stored in OFFSET_X, OFFSET_Y, and OFFSET_Z register. The bit 4 (TOFS) of CONFIG1 register has to be set to '1' to use offset trimming.

6) Write CONFIG1 register to set TOFS bit to '1' if offset trimming is used.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	RSV	OPMD	TOFS	RSV	SSLP	PWML	VREFS
Value	0	0	0	Note a	0	Note b	Note c	Note d

Figure 33. CONFIG1 register. Address 03h.

a) Set TOFS: '0' for no offset trimming, '1' for offset trimming
b) Set SSLP bit: '0' for positive slope sensor, '1' for negative slope sensor
c) Set PWML bit: '0' for PWM active high, '1' for PWM active low
d) Set VREFS bit: '0' for internal voltage reference, '1' for external voltage reference
e) RSV bit is reserved and is set to '0'.

7) If the default DUTY_LIMIT value (0F32h) after power on or software reset is to be changed, write a new value to the DUTY_LIMIT_HI and DUTY_LIMIT_LO registers. This duty limit is the maximum duty cycle for each channel LED. If any of the channel PWM duty cycle reach this limit, clipping error take place and the chromaticity is maintained at the expense of brightness setting.

8) If the default BETA register value (FFh) after power on or software reset is to be changed, write the BETA (brightness scalar) register. Note FFh represents 100% brightness level.

9) Write COLOR_SETA, COLOR_SETB, and COLOR_SETC registers. COLOR_SETA consist of COLOR_SETA_HI and COLOR_SETA_LO register. COLOR_SETB consist of COLOR_SETB_HI and COLOR_SETB_LO register. COLOR_SETC consist of COLOR_SETC_HI and COLOR_SETC_LO register. Table 9 shows the data format.

Table 9. Color set point format for RGB, Yu'v', Yxy, and XYZ color space.

RGB Color Space		
COLOR_SETA_HI	0	
COLOR_SETA_LO	R value from 0 to 255	
COLOR_SETB_HI	0	
COLOR_SETB_LO	G value from 0 to 255	
COLOR_SETC_HI	0	
COLOR_SETC_LO	B value from 0 to 255	
Yu'v' Color Space		
COLOR_SETA_HI	Y value. Upper 2 bits	Y value range from 0 to 1000
COLOR_SETA_LO	Y value. Lower 8 bits	
COLOR_SETB_HI	Integer value (u' * 1000). Upper 2 bits	
COLOR_SETB_LO	Integer value (u' * 1000). Lower 8 bits	
COLOR_SETC_HI	Integer value (v' * 1000). Upper 2 bits	
COLOR_SETC_LO	Integer value (v' * 1000). Lower 8 bits	
Yxy Color Space		
COLOR_SETA_HI	Y value. Upper 2 bits	Y value range from 0 to 1000
COLOR_SETA_LO	Y value. Lower 8 bits	
COLOR_SETB_HI	Integer value (x * 1000). Upper 2 bits	
COLOR_SETB_LO	Integer value (x * 1000). Lower 8 bits	
COLOR_SETC_HI	Integer value (y * 1000). Upper 2 bits	
COLOR_SETC_LO	Integer value (y * 1000). Lower 8 bits	
XYZ Color Space		
COLOR_SETA_HI	X value. Upper 2 bits	X value range from 0 to 1000
COLOR_SETA_LO	X value. Lower 8 bits	
COLOR_SETB_HI	Y value. Upper 2 bits	Y value range from 0 to 1000
COLOR_SETB_LO	Y value. Lower 8 bits	
COLOR_SETC_HI	Z value. Upper 2 bits	Z value range from 0 to 1000
COLOR_SETC_LO	Z value. Lower 8 bits	

Note: All numbers are decimal.

10) After entering the data in COLOR_SETA, COLOR_SETB and COLOR_SETC, write CTRL1 register with 12h.

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Value	0	0	0	1	0	0	1	0

Figure 34. CTRL1 register. Address 01h.

11) When the UPD bit goes '0', the color set point is updated and the system will respond to your selected color.

12) If the ERR_FLAG pin is '1', read the ERROR register to determine the error.
If bit 2 (CLIP) is '1': CLIP error. The required brightness could not be achieved.
If bit 1 (NLOCK) is '1': No Lock error. The required color set point could not be achieved.

If bit 0 (RANGE) is '1': Out of Range error. Required color set point is outside the sensor measurement range.

13) Repeat step 8 to 11 to enter a new set point if necessary.

Correlation between set point values and actual values

For Yxy and Yu'v' color space, the actual CIE Y luminance value can be obtained by dividing the HDJD-J822 set point Y value by the scale ratio obtained in step 33 of the calibration procedure. For XYZ color space, the actual set point in CIE XYZ is obtained by dividing the HDJD-J822 set point X, Y, Z value by the scale ratio obtained in step 33 of the calibration procedure.

Appendix 1. Register List.

Table 10. General control, configuration, status and error register.
Note: Reset values refer to register values after completion of power on or software reset.

Address											Reset Value
Decimal	Hex	Register	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Hex
1	01	CTRL1	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW	0
2	02	CTRL2	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL	0
3	03	CONFIG1	N/A	RSV	OPMD	TOFS	RSV	SSLP	PWML	VREFS	0
4	04	CONFIG2	GAINX	GAINY	GAINZ	RSV	RGB	Yu'v'	Yxy	XYZ	08
9	09	STATUS	N/A	N/A	N/A	N/A	N/A	OPENL	NORM	INIT	02
10	0A	ERROR	N/A	N/A	N/A	N/A	N/A	CLIP	NLOCK	RANGE	0

Table 11. Offset registers.

Address				Reset Value
Decimal	Hex	Register	Description	Hex
129	81	OFFSET_Z	SENSE_Z offset value.	0
130	82	OFFSET_Y	SENSE_Y offset value.	0
131	83	OFFSET_X	SENSE_X offset value.	0

These are offset registers for storing sensor ADC values when all LEDs are off. Offset values are obtained when GOFS, bit 3 of the CTRL1 register is set to '1'.

Table 12. Duty registers (ONLY FOR CALIBRATION / OPEN LOOP OPERATION).

Address				Reset Value
Decimal	Hex	Register	Description	Hex
11	0B	DUTYB_LO	Blue LED duty. Lower 8 bits	0
12	0C	DUTYB_HI	Blue LED duty. Upper 4 bits.	0
13	0D	DUTYG_LO	Green LED duty. Lower 8 bits	0
14	0E	DUTYG_HI	Green LED duty. Upper 4 bits.	0
15	0F	DUTYR_LO	Red LED duty. Lower 8 bits	0
16	10	DUTYR_HI	Red LED duty. Upper 4 bits.	0

Duty registers controlled the pulse width duty factor of the three channels PWM_R, PWM_G, and PWM_B open loop mode.

Table 13. Sensor ADC output measurement registers (ONLY FOR CALIBRATION).

Address				Reset Value
Decimal	Hex	Register	Description	Hex
132	84	SENSOR_ADCZ_LO	Sensor channel Z ADC value. Lower 8 bits.	0
133	85	SENSOR_ADCZ_HI	Sensor channel Z ADC value. Upper 2 bits.	0
134	86	SENSOR_ADCY_LO	Sensor channel Y ADC value. Lower 8 bits.	0
135	87	SENSOR_ADCY_HI	Sensor channel Y ADC value. Upper 2 bits.	0
136	88	SENSOR_ADCX_LO	Sensor channel X ADC value. Lower 8 bits.	0
137	89	SENSOR_ADCX_HI	Sensor channel X ADC value. Upper 2 bits.	0

Sensors ADC output measurements are obtained when GSSR, bit 1 of CTRL2 register is set to ‘1’.

Table 14. Input registers for calibration data processing. (ONLY FOR CALIBRATION).

Address				Reset Value
Decimal	Hex	Register	Description	Hex
220	DC	CAL_CMZB_LO	Scaled camera Z value when only blue LED on. Lower 8 bits	0
221	DD	CAL_CMZB_HI	Scaled camera Z value when only blue LED on. Upper 2 bits	0
222	DE	CAL_CMYB_LO	Scaled camera Y value when only blue LED on. Lower 8 bits	0
223	DF	CAL_CMYB_HI	Scaled camera Y value when only blue LED on. Upper 2 bits	0
224	E0	CAL_CMXB_LO	Scaled camera X value when only blue LED on. Lower 8 bits	0
225	E1	CAL_CMXB_HI	Scaled camera X value when only blue LED on. Upper 2 bits	0
226	E2	CAL_CMZG_LO	Scaled camera Z value when only green LED on. Lower 8 bits	0
227	E3	CAL_CMZG_HI	Scaled camera Z value when only green LED on. Upper 2 bits	0
228	E4	CAL_CMYG_LO	Scaled camera Y value when only green LED on. Lower 8 bits	0
229	E5	CAL_CMYG_HI	Scaled camera Y value when only green LED on. Upper 2 bits	0
230	E6	CAL_CMXG_LO	Scaled camera X value when only green LED on. Lower 8 bits	0
231	E7	CAL_CMXG_HI	Scaled camera X value when only green LED on. Upper 2 bits	0
232	E8	CAL_CMZR_LO	Scaled camera Z value when only red LED on. Lower 8 bits	0
233	E9	CAL_CMZR_HI	Scaled camera Z value when only red LED on. Upper 2 bits	0
234	EA	CAL_CMYR_LO	Scaled camera Y value when only red LED on. Lower 8 bits	0
235	EB	CAL_CMYR_HI	Scaled camera Y value when only red LED on. Upper 2 bits	0
236	EC	CAL_CMXR_LO	Scaled camera X value when only red LED on. Lower 8 bits	0
237	ED	CAL_CMXR_HI	Scaled camera X value when only red LED on. Upper 2 bits	0
238	EE	CAL_SMZB_LO	SENSOR_ADCZ_LO value when only blue LED on. Lower 8 bits	0
239	EF	CAL_SMZB_HI	SENSOR_ADCZ_HI value when only blue LED on. Upper 2 bits	0
240	F0	CAL_SMYB_LO	SENSOR_ADCY_LO value when only blue LED on. Lower 8 bits	0
241	F1	CAL_SMYB_HI	SENSOR_ADCY_HI value when only blue LED on. Upper 2 bits	0
242	F2	CAL_SMXB_LO	SENSOR_ADCX_LO value when only blue LED on. Lower 8 bits	0
243	F3	CAL_SMXB_HI	SENSOR_ADCX_HI value when only blue LED on. Upper 2 bits	0
244	F4	CAL_SMZG_LO	SENSOR_ADCZ_LO value when only green LED on. Lower 8 bits	0
245	F5	CAL_SMZG_HI	SENSOR_ADCZ_HI value when only green LED on. Upper 2 bits	0
246	F6	CAL_SMYG_LO	SENSOR_ADCY_LO value when only green LED on. Lower 8 bits	0
247	F7	CAL_SMYG_HI	SENSOR_ADCY_HI value when only green LED on. Upper 2 bits	0
248	F8	CAL_SMXG_LO	SENSOR_ADCX_LO value when only green LED on. Lower 8 bits	0
249	F9	CAL_SMXG_HI	SENSOR_ADCX_HI value when only green LED on. Upper 2 bits	0
250	FA	CAL_SMZR_LO	SENSOR_ADCZ_LO value when only red LED on. Lower 8 bits	0
251	FB	CAL_SMZR_HI	SENSOR_ADCZ_HI value when only red LED on. Upper 2 bits	0
252	FC	CAL_SMYR_LO	SENSOR_ADCY_LO value when only red LED on. Lower 8 bits	0
253	FD	CAL_SMYR_HI	SENSOR_ADCY_HI value when only red LED on. Upper 2 bits	0
254	FE	CAL_SMXR_LO	SENSOR_ADCX_LO value when only red LED on. Lower 8 bits	0
255	FF	CAL_SMXR_HI	SENSOR_ADCX_HI value when only red LED on. Upper 2 bits	0

These are input registers that must be entered before calibration data processing. Calibration data processing is triggered by setting RCAL, bit 0 of CTRL2 register to '1'. Calibration data registers, CALDATA0 to CALDATA30 (Table 15) values are obtained once the processing is completed. These thirty-one calibration data registers (CALDATA0 to CALDATA30) are saved to non volatile memory after calibration data processing is completed.

Table 15. Calibration data registers.

Address				Reset Value
Decimal	Hex	Register	Description	Hex
138	**8A**	CALDATA0	Calibration Data 0	35
139	**8B**	CALDATA1	Calibration Data 1	0B
140	**8C**	CALDATA2	Calibration Data 2	A4
141	**8D**	CALDATA3	Calibration Data 3	05
142	**8E**	CALDATA4	Calibration Data 4	96
143	**8F**	CALDATA5	Calibration Data 5	01
144	**90**	CALDATA6	Calibration Data 6	70
145	**91**	CALDATA7	Calibration Data 7	01
146	**92**	CALDATA8	Calibration Data 8	53
147	**93**	CALDATA9	Calibration Data 9	17
148	**94**	CALDATA10	Calibration Data 10	4E
149	**95**	CALDATA11	Calibration Data 11	83
150	**96**	CALDATA12	Calibration Data 12	3E
151	**97**	CALDATA13	Calibration Data 13	84
152	**98**	CALDATA14	Calibration Data 14	47
153	**99**	CALDATA15	Calibration Data 15	85
154	**9A**	CALDATA16	Calibration Data 16	4C
155	**9B**	CALDATA17	Calibration Data 17	1B
156	**9C**	CALDATA18	Calibration Data 18	7F
157	**9D**	CALDATA19	Calibration Data 19	8E
158	**9E**	CALDATA20	Calibration Data 20	85
159	**9F**	CALDATA21	Calibration Data 21	A7
160	**A0**	CALDATA22	Calibration Data 22	77
161	**A1**	CALDATA23	Calibration Data 23	86
162	**A2**	CALDATA24	Calibration Data 24	8A
163	**A3**	CALDATA25	Calibration Data 25	9C
164	**A4**	CALDATA26	Calibration Data 26	51
165	**A5**	CALDATA27	Calibration Data 27	4B
166	**A6**	CALDATA28	Calibration Data 28	03
167	**A7**	CALDATA29	Calibration Data 29	9A
168	**A8**	CALDATA30	Calibration Data 30	11

The thirty-one calibration data registers, CALDATA0 to CALDATA30 are read from non volatile memory after power on or software reset in normal operating mode.

Table 16. Duty limit registers. (NORMAL MODE OPERATION ONLY).

Address				Reset Value
Decimal	Hex	Register	Description	Hex
230	E6	DUTY_LIMIT_LO	Maximum duty limit. Lower 8 bits	32
231	E7	DUTY_LIMIT_HI	Maximum duty limit. Upper 4 bits	0F

Duty limit register specifies the maximum PWM pulse width for all the channels before clipping error occurs.

Table 17. Brightness scalar and color set point registers.

Address				Reset Value
Decimal	Hex	Register	Description	Hex
196	C4	BETA	Brightness scalar	FF
232	E8	COLOR_SETC_LO	User color set point C. Lower 8 bits	0
233	E9	COLOR_SETC_HI	User color set point C. Upper 2 bits	0
234	EA	COLOR_SETB_LO	User color set point B. Lower 8 bits	0
235	EB	COLOR_SETB_HI	User color set point B. Upper 2 bits	0
236	EC	COLOR_SETA_LO	User color set point A. Lower 8 bits	0
237	ED	COLOR_SETA_HI	User color set point A. Upper 2 bits	0

Users should enter these registers to specify the brightness and color set point in normal operating mode.

Appendix 2. Register Map

Register addresses 01h to 04h, 09h to 0Ah, 81h to 83h, 8Ah to A8h have the same function and are used in both normal and open loop mode. Register addresses 0Bh to 10h, 84h to 89h, DCh to E5h, EEh to FFh are used in only calibration mode. Register address C4h is only used in normal mode. Register addrresses E6h to EDh have different function in calibration mode and normal mode.

Address	Calibration Mode	Normal Mode
01h	CTRL1	
02h	CTRL2	
03h	CONFIG1	
04h	CONFIG2	
09h	STATUS	
0Ah	ERROR	
0Bh	DUTYB_LO	
0Ch	DUTYB_HI	
0Dh	DUTYG_LO	
0Eh	DUTYG_HI	
0Fh	DUTYR_LO	
10h	DUTYR_HI	
81h	OFFSET_Z	
82h	OFFSET_Y	
83h	OFFSET_X	
84h	SENSOR_ADCZ_LO	
85h	SENSOR_ADCZ_HI	
86h	SENSOR_ADCY_LO	
87h	SENSOR_ADCY_HI	
88h	SENSOR_ADCX_LO	
89h	SENSOR_ADCX_HI	
8Ah	CALDATA0	
8Bh	CALDATA1	
8Ch	CALDATA2	
8Dh	CALDATA3	
8Eh	CALDATA4	
8Fh	CALDATA5	
90h	CALDATA6	
91h	CALDATA7	

Figure 35. Register address map.

Address	Calibration Mode	Normal Mode
92h	CALDATA8	
93h	CALDATA9	
94h	CALDATA10	
95h	CALDATA11	
96h	CALDATA12	
97h	CALDATA13	
98h	CALDATA14	
99h	CALDATA15	
9Ah	CALDATA16	
9Bh	CALDATA17	
9Ch	CALDATA18	
9Dh	CALDATA19	
9Eh	CALDATA20	
9Fh	CALDATA21	
A0h	CALDATA22	
A1h	CALDATA23	
A2h	CALDATA24	
A3h	CALDATA25	
A4h	CALDATA26	
A5h	CALDATA27	
A6h	CALDATA28	
A7h	CALDATA29	
A8h	CALDATA30	

C4h		BETA
DCh	CAL_CMZB_LO	
DDh	CAL_CMZB_HI	
DEh	CAL_CMYB_LO	
DFh	CAL_CMYB_HI	
E0h	CAL_CMXB_LO	
E1h	CAL_CMXB_HI	
E2h	CAL_CMZG_LO	
E3h	CAL_CMZG_HI	
E4h	CAL_CMYG_LO	
E5h	CAL_CMYG_HI	

Figure 35. Register address map (continued).

Address	Calibration Mode	Normal Mode
E6h	CAL_CMXG_LO	DUTY_LIMIT_LO
E7h	CAL_CMXG_HI	DUTY_LIMIT_HI
E8h	CAL_CMZR_LO	COLOR_SETC_LO
E9h	CAL_CMZR_HI	COLOR_SETC_HI
EAh	CAL_CMYR_LO	COLOR_SETB_LO
EBh	CAL_CMYR_HI	COLOR_SETB_HI
ECh	CAL_CMXR_LO	COLOR_SETA_LO
EDh	CAL_CMXR_HI	COLOR_SETA_HI
EEh	CAL_SMZB_LO	
EFh	CAL_SMZB_HI	
F0h	CAL_SMYB_LO	
F1h	CAL_SMYB_HI	
F2h	CAL_SMXB_LO	
F3h	CAL_SMXB_HI	
F4h	CAL_SMZG_LO	
F5h	CAL_SMZG_HI	
F6h	CAL_SMYG_LO	
F7h	CAL_SMYG_HI	
F8h	CAL_SMXG_LO	
F9h	CAL_SMXG_HI	
FAh	CAL_SMZR_LO	
FBh	CAL_SMZR_HI	
FCh	CAL_SMYR_LO	
FDh	CAL_SMYR_HI	
FEh	CAL_SMXR_LO	
FFh	CAL_SMXR_HI	

Figure 35. Register address map (continued).

Appendix 3. Register Information

CTRL1: Control 1 Register (01h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	UPD	GOFS	APDE	PWME	RSW
Reset Value	0	0	0	0	0	0	0	0

Figure 36. Control 1 register format.

Table 18. Control 1 register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	Not applicable. Value is ‘0’.
UPD	R/W	Color set point update. Set this bit ‘1’ once color set point is sent to Color_SETA, Color_SETB, and COLOR_SETC registers. This bit will reset to ‘0’ once color set point is updated.
GOFS	R/W	Acquire offset value. Set this bit ‘1’ to obtain the offset value from each SENSE_X, SENSE_Y, and SENSE_Z channel when all red, green, and blue light sources are off. This bit will reset back to ‘0’ once offset values are obtained. Offset values are stored in OFFSET_X, OFFSET_Y, and OFFSET_Z registers respectively.
APDE	R/W	Analog Power Down Enable. When “1”, device is configured to standby mode. When “0”, device is configured to normal mode. This function is useful in external clock mode only.
PWME	R/W	Pulse width modulation enable. When ‘1’, PWM generator is enabled and red, green, and blue light sources can turn on. When ‘0’, PWM generator is disabled and red, green, and blue light sources will turn off.
RSW	R/W	Reset software. Set this bit ‘1’ to perform software reset. The device clears this bit to ‘0’ during reset. INIT (bit 0) of STATUS register will be cleared to ‘0’ once reset is completed.

CTRL2: Control 2 Register (02h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	RSV	GSSR	RCAL
Reset Value	0	0	0	0	0	0	0	0

Figure 37. Control 2 register format.

Table 19. Control 2 register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
RSV	N/A	Reserved. Value is '0'.
GSSR	R/W	Acquire sensor value. Set this bit '1' to start sensor acquisition. This bit is reset '0' once sensor acquisition is completed. Sensor values are stored in SENSOR_ADCX, SENSOR_ADCY, and SENSOR_ADCZ registers respectively.
RCAL	R/W	Run calibration. Set this bit '1' to start calibration data processing, once input data have been entered in registers (address DCh to FFh) in Table 14 Appendix 1. This bit is reset '0' once processing is completed. The thirty-one calibration data, CALDATA0 to CALDATA30 (address 8Ah to A8h) must be stored in non volatile memory for read back in normal operating mode.

CONFIG1: Configuration 1 Register (03h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	RSV	OPMD	TOFS	RSV	SSLP	PWML	VREFS
Reset Value	0	0	0	0	0	0	0	0

Figure 38. Configuration 1 register format.

Table 20. Configuration 1 register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
RSV	N/A	Reserved. Value is '0'.
OPMD	R/W	Operation Mode. When '1', device is configured to operate in open loop mode for calibration. When '0', device is configured to operate in normal mode with sensor feedback.
TOFS	R/W	Trim Offset enable. When '1', device is configured to subtract offset from OFFSET_X, OFFSET_Y, and OFFSET_Z registers. When '0', device does not subtract offset value.
SSLP	R/W	Sensor Slope mode select. When '1', device operates with negative coefficient sensor slope, i.e., incident light is inversely proportional with the output sensor voltage. The GAINZ, GAINY and GAINX (bit 5 to 7) of CONFIG2 register must be set to '0' if the device operates with negative coefficient sensor slope. When '0', device operates with positive coefficient sensor slope, i.e., incident light is directly proportional with the output sensor voltage.
PWML	R/W	Pulse Width Modulation Level select. When '1', PWM output is active low. When '0', PWM output is active high.
VREFS	R/W	ADC Reference Voltage Select. When '1', device is configured to use external voltage reference. When '0', device is configured to use internal voltage reference.

CONFIG2: Configuration 2 Register (04h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	GAINX	GAINY	GAINZ	RSV	RGB	Yu'v'	Yxy	XYZ
Reset Value	0	0	0	0	1	0	0	0

Figure 39. Configuration 2 register format.

Table 21. Configuration 2 register bit description.

Mnemonic	Read / Write Control	Description
GAINX	R/W	SENSE_X gain setting. When '1', SENSE_X gain is configured to 2x. When '0', SENSE_X gain is configured to 1x.
GAINY	R/W	SENSE_Y gain setting. When '1', SENSE_Y gain is configured to 2x. When '0', SENSE_Y gain is configured to 1x.
GAINZ	R/W	SENSE_Z gain setting. When '1', SENSE_Z gain is configured to 2x. When '0', SENSE_Z gain is configured to 1x.
RSV	N/A	Reserve. Value is '0'.
RGB	R/W	CIE RGB color space with illuminant E as white reference. Select this color space by setting this bit '1'. Set all other color space selection bits, Yu'v', Yxy, XYZ to '0'.
Yu'v'	R/W	1976 Yu'v' color space. Select this color space by setting this bit '1'. Set all other color space selection bits RGB, Yxy, XYZ to '0'.
Yxy	R/W	1931 Yxy color space. Select this color space by setting this bit '1'. Set all other color space selection bits RGB, Yu'v', XYZ to '0'.
XYZ	R/W	1931 XYZ color space. Select this color space by setting this bit '1'. Set all other color space selection bits RGB, Yu'v', Yxy to '0'.

STATUS: Status Register (09h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	OPENL	NORM	INIT
Reset Value	0	0	0	0	0	0	1	0

Figure 40. Status register format.

Table 22. Status register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A
OPENL	R	Open Loop Mode Flag. '1' indicates device is in open loop operation and '0' indicates device is not in open loop mode.
NORM	R	Normal Loop Mode Flag. '1' indicates device is in normal operating mode and '0' indicates device is not in normal operating mode.
INIT	R	Initialization Mode Flag. '1' indicates device is performing initialization. '0' indicates initialization is completed. This bit can be checked after power on reset or software reset to ensure initialization is completed.

ERROR: Error flag register (0Ah)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A	N/A	N/A	N/A	N/A	CLIP	NLOCK	RANGE
Reset Value	0	0	0	0	0	0	0	0

Figure 41. Error flag register format.

Table 23. Error register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A
CLIP	R	Clipping Flag. When '1', the required brightness could not be achieved. When '0', the required brightness is achieved.
NLOCK	R	No Lock Flag. When '1', the required color set point cannot be achieved. When '0', the required color set point is achieved.
RANGE	R	Out of Range Flag. '1' indicates required color set point is lying outside the sensor measurement range and previous valid color set point is maintained. '0' indicates required color set point is lying within sensor measurement range.

OFFSET_Z: SENSE_Z Offset Register (81h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	OFFSET_Z[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 42. SENSE_Z offset register format.

Table 24. SENSE_Z offset register description.

Mnemonic	Read / Write Control	Description
OFFSET_Z[7:0]	R/W	SENSE_Z offset register. Default value is 0.

OFFSET_Y: SENSE_Y Offset Register (82h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	OFFSET_Y[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 43. SENSE_Y offset register format.

Table 25. SENSE_Y offset register description.

Mnemonic	Read / Write Control	Description
OFFSET_Y[7:0]	R/W	SENSE_Y offset register. Default value is 0.

OFFSET_X: SENSE_X Offset Register (83h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	OFFSET_X[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 44. SENSE_X offset register format.

Table 26. SENSE_X offset register description.

Mnemonic	Read / Write Control	Description
OFFSET_X[7:0]	R/W	SENSE_X offset register. Default value is 0.

DUTYB: Blue LED Duty Register (0Bh-0Ch)

DUTYB_LO: Blue LED Duty Low Byte Register (0Bh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	DUTYB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 45. Blue LED duty low byte register format.

DUTYB_HI: Blue LED Duty High Byte Register (0Ch)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A				DUTYB[11:8]			
Reset Value	0	0	0	0	0	0	0	0

Figure 46. Blue LED duty high byte register format.

Table 27. Blue LED duty register bit description

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
DUTYB[11:0]	R/W	Blue LED duty register. Should only be written in open loop mode during calibration.

DUTYG: Green LED Duty Register (0Dh-0Eh)

DUTYG_LO: Green LED Duty Low Byte Register (0Dh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	DUTYG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 47. Green LED duty low byte register format.

DUTYG_HI: Green LED Duty High Byte Register (0Eh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A				DUTYG[11:8]			
Reset Value	0	0	0	0	0	0	0	0

Figure 48. Green LED duty high byte register format.

Table 28. Green LED duty register bit description

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
DUTYG[11:0]	R/W	Green LED duty register. Should only be written in open loop mode during calibration.

DUTYR: Red LED Duty Register (0Fh-10h)

DUTYR_LO: Red LED Duty Low Byte Register (0Fh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	DUTYR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 49. Red LED duty low byte register format.

DUTYR_HI: Red LED Duty High Byte Register (10h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A				DUTYR[11:8]			
Reset Value	0	0	0	0	0	0	0	0

Figure 50. Red LED duty high byte register format.

Table 29. Red LED duty register bit description

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
DUTYR[11:0]	R/W	Red LED duty register. Should only be written in open loop mode during calibration.

SENSOR_ADCZ: Sensor Channel Z ADC Value Register (84h–85h)

SENSOR_ADCZ_LO: Sensor Channel Z ADC Low Byte Register (84h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	SENSOR_ADCZ[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 51. Sensor channel Z ADC low byte register format.

SENSOR_ADCZ_HI: Sensor Channel Z ADC High Byte Register (85h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV						SENSOR_ADCZ[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 52. Sensor channel Z ADC high byte register format.

Table 30. Sensor channel Z ADC value register bit description

Mnemonic	Read / Write Control	Description
RSV	N/A	Reserved
SENSOR_ADCZ[9:0]	R	Sensor channel Z ADC value register

SENSOR_ADCY: Sensor Channel Y ADC Value Register (86h–87h)

SENSOR_ADCY_LO: Sensor Channel Y ADC Low Byte Register (86h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	SENSOR_ADCY[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 53. Sensor channel Y ADC low byte register format.

SENSOR_ADCY_HI: Sensor channel Y ADC high byte register (87h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV						SENSOR_ADCY[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 54. Sensor channel Y ADC high byte register format.

Table 31. Sensor channel Y ADC value register bit description

Mnemonic	Read / Write Control	Description
RSV	N/A	Reserved
SENSOR_ADCY[9:0]	R	Sensor channel Y ADC value register

SENSOR_ADCX: Sensor Channel X ADC Value Register (88h–89h)

SENSOR_ADCX_LO: Sensor Channel X ADC Low Byte Register (88h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	SENSOR_ADCX[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 55. Sensor channel X ADC low byte register format.

SENSOR_ADCX_HI: Sensor channel X ADC high byte register (89h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV						SENSOR_ADCX[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 56. Sensor channel X ADC high byte register format.

Table 32. Sensor channel X ADC value register bit description.

Mnemonic	Read / Write Control	Description
RSV	N/A	Reserved
SENSOR_ADCX[9:0]	R	Sensor channel X ADC value register

CAL_CMZB: Scaled Camera Z Value when only Blue LED On. (DCh-DDh)

CAL_CMZB_LO: Scaled Camera Z Low Byte Value when only Blue LED On. (DCh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMZB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 57. Scaled camera Z low byte register format.

CAL_CMZB_HI: Scaled Camera Z High Byte Value when only Blue LED On. (DDh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMZB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 58. Scaled camera Z high byte register format.

Table 33. Bit description for scaled camera Z value register when only blue LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMZB[9:0]	R/W	Calibration input register for scaled camera Z value when only blue LED on. Maximum value is 1000.

CAL_CMYB: Scaled Camera Y Value when only Blue LED On. (DEh-DFh)

CAL_CMYB_LO: Scaled Camera Y Low Byte Value when only Blue LED On. (DEh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMYB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 59. Scaled camera Y low byte register format.

CAL_CMYB_HI: Scaled Camera Y High Byte Value when only Blue LED On. (DFh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMYB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 60. Scaled camera Y high byte register format.

Table 34. Bit description for scaled camera Y value register when only blue LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMYB[9:0]	R/W	Calibration input register for scaled camera Y value when only blue LED on. Maximum value is 1000.

CAL_CMXB: Scaled Camera X Value when only Blue LED On. (E0h-E1h)

CAL_CMXB_LO: Scaled Camera X Low Byte Value when only Blue LED On. (E0h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMXB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 61. Scaled camera X low byte register format.

CAL_CMXB_HI: Scaled Camera X High Byte Value when only Blue LED On. (E1h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMXB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 62. Scaled camera X high byte register format.

Table 35. Bit description for scaled camera X value register when only blue LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMXB[9:0]	R/W	Calibration input register for scaled camera X value when only blue LED on. Maximum value is 1000.

CAL_CMZG: Scaled Camera Z Value when only Green LED On. (E2h-E3h)

CAL_CMZG_LO: Scaled Camera Z Low Byte Value when only Green LED On. (E2h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMZG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 63. Scaled camera Z low byte register format.

CAL_CMZG_HI: Scaled Camera Z High Byte Value when only Green LED On. (E3h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMZG[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 64. Scaled camera Z high byte register format.

Table 36. Bit description for scaled camera Z value register when only green LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_CMZG[9:0]	R/W	Calibration input register for scaled camera Z value when only green LED on. Maximum value is 1000.

CAL_CMYG: Scaled Camera Y Value when Only Green LED On. (E4h-E5h)

CAL_CMYG_LO: Scaled Camera Y Low Byte Value when only Green LED On. (E4h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMYG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 65. Scaled camera Y low byte register format.

CAL_CMYG_HI: Scaled Camera Y High Byte Value when only Green LED On. (E5h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMYG[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 66. Scaled camera Y high byte register format.

Table 37. Bit description for scaled camera Y value register when only green LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMYG[9:0]	R/W	Calibration input register for scaled camera Y value when only green LED on. Maximum value is 1000.

CAL_CMXG: Scaled Camera X Value when only Green LED On. (E6h-E7h)

CAL_CMXG_LO: Scaled Camera X Low Byte Value when only Green LED On. (E6h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMXG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 67. Scaled camera X low byte register format.

CAL_CMXG_HI: Scaled Camera X High Byte Value when only Green LED On. (E7h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMXG[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 68. Scaled camera X high byte register format.

Table 38. Bit description for scaled camera X value register when only green LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMXG[9:0]	R/W	Calibration input register for scaled camera X value when only green LED on. Maximum value is 1000.

CAL_CMZR: Scaled Camera Z Value when only Red LED On. (E8h-E9h)

CAL_CMZR_LO: Scaled Camera Z Low Byte Value when only Red LED On. (E8h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMZR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 69. Scaled camera Z low byte register format.

CAL_CMZR_HI: Scaled Camera Z High Byte Value when only Red LED On. (E9h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMZR[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 70. Scaled camera Z high byte register format.

Table 39. Bit description for scaled camera Z value register when only red LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_CMZR[9:0]	R/W	Calibration input register for scaled camera Z value when only red LED on. Maximum value is 1000.

CAL_CMYR: Scaled Camera Y Value when only Red LED On. (EAh-EBh)

CAL_CMYR_LO: Scaled Camera Y Low Byte Value when only Red LED On. (EAh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMYR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 71. Scaled camera Y low byte register format.

CAL_CMYR_HI: Scaled Camera Y High Byte Value when only Red LED On. (EBh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMYR[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 72. Scaled camera Y high byte register format.

Table 40. Bit description for scaled camera Y value register when only red LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMYR[9:0]	R/W	Calibration input register for scaled camera Y value when only red LED on. Maximum value is 1000.

CAL_CMXR: Scaled Camera X Value when only Red LED On. (ECh-EDh)

CAL_CMXR_LO: Scaled Camera X Low Byte Value when only Red LED On. (ECh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_CMXR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 73. Scaled camera X low byte register format.

CAL_CMXR_HI: Scaled Camera X High Byte Value when only Red LED On. (EDh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_CMXR[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 74. Scaled camera X high byte register format.

Table 41. Bit description for scaled camera X value register when only red LED on.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_CMXR[9:0]	R/W	Calibration input register for scaled camera X value when only red LED on. Maximum value is 1000.

CAL_SMZB: SENSOR_ADCZ Value when only Blue LED On. (EEh-EFh)

CAL_SMZB_LO: SENSOR_ADCZ_LO Value when only Blue LED On. (EEh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMZB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 75. CAL_SMZB_LO register format.

CAL_SMZB_HI: SENSOR_ADCZ_HI Value when only Blue LED On. (EFh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMZB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 76. CAL_SMZB_HI register format.

Table 42. CAL_SMZB register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_SMZB[9:0]	R/W	Calibration input register for SENSOR_ADCZ values when only blue LED on. Maximum value is 1000.

CAL_SMYB: SENSOR_ADCY Value when only Blue LED On. (F0h-F1h)

CAL_SMYB_LO: SENSOR_ADCY_LO Value when only Blue LED On. (F0h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMYB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 77. CAL_SMYB_LO register format.

CAL_SMYB_HI: SENSOR_ADCY_HI Value when only Blue LED On. (F1h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMYB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 78. CAL_SMYB_HI register format.

Table 43. CAL_SMYB register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ’0’.
CAL_SMYB[9:0]	R/W	Calibration input register for SENSOR_ADCY values when only blue LED on. Maximum value is 1000.

CAL_SMXB: SENSOR_ADCX Value when only Blue LED On. (F2h-F3h)

CAL_SMXB_LO: SENSOR_ADCX_LO Value when only Blue LED On. (F2h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMXB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 79. CAL_SMXB_LO register format.

CAL_SMXB_HI: SENSOR_ADCX_HI Value when only Blue LED On (F3h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMXB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 80. CAL_SMXB_HI register format.

Table 44. CAL_SMXB register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_SMXB[9:0]	R/W	Calibration input register for SENSOR_ADCX values when only blue LED on. Maximum value is 1000.

CAL_SMZG: SENSOR_ADCZ Value when only Green LED On. (F4h-F5h)

CAL_SMZG_LO: SENSOR_ADCZ_LO Value when only Green LED On. (F4h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMZG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 81. CAL_SMZG_LO register format.

CAL_SMZG_HI: SENSOR_ADCZ_HI Value when only Green LED On. (F5h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMZG[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 82. CAL_SMZG_HI register format.

Table 45. CAL_SMZG register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is '0'.
CAL_SMZG[9:0]	R/W	Calibration input register for SENSOR_ADCZ values when only green LED on. Maximum value is 1000.

CAL_SMYG: SENSOR_ADCY Value when only Green LED On. (F6h-F7h)

CAL_SMYG_LO: SENSOR_ADCY_LO Value when only Green LED On. (F6h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMYG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 83. CAL_SMYG_LO register format.

CAL_SMYG_HI: SENSOR_ADCY_HI Value when only Green LED On. (F7h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMYG[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 84. CAL_SMYG_HI register format.

Table 46. CAL_SMYG register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0‘.
CAL_SMYG[9:0]	R/W	Calibration input register for SENSOR_ADCY values when only green LED on. Maximum value is 1000.

CAL_SMXG: SENSOR_ADCX Value when only Green LED On. (F8h-F9h)

CAL_SMXG_LO: SENSOR_ADCX_LO Value when only Green LED On. (F8h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMXG[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 85. CAL_SMXG_LO register format.

CAL_SMXG_HI: SENSOR_ADCX_HI Value when only Green LED On. (F9h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMXG[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 86. CAL_SMXG_HI register format.

Table 47. CAL_SMXG register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_SMXG[9:0]	R/W	Calibration input register for SENSOR_ADCX values when only green LED on. Maximum value is 1000.

CAL_SMZR: SENSOR_ADCZ Value when only Red LED On. (FAh-FBh)

CAL_SMZR_LO: SENSOR_ADCZ_LO Value when only Red LED On. (FAh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMZR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 87. CAL_SMZR_LO register format.

CAL_SMZR_HI: SENSOR_ADCZ_HI Value when only Red LED On. (FBh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMZR[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 88. CAL_SMZR_HI register format.

Table 48. CAL_SMZR register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_SMZR[9:0]	R/W	Calibration input register for SENSOR_ADCZ values when only red LED on. Maximum value is 1000.

CAL_SMYR: SENSOR_ADCY Value when only Red LED On. (FCh-FDh)

CAL_SMYR_LO: SENSOR_ADCY_LO Value when only Red LED On. (FCh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMYR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 89. CAL_SMYR_LO register format.

CAL_SMYR_HI: SENSOR_ADCY_HI Value when only Red LED On. (FDh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMYR[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 90. CAL_SMYR_HI register format.

Table 49. CAL_SMYR register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_SMYR[9:0]	R/W	Calibration input register for SENSOR_ADCY values when only red LED on. Maximum value is 1000.

CAL_SMXR: SENSOR_ADCX Value when only Red LED on. (FEh-FFh)

CAL_SMXR_LO: SENSOR_ADCX_LO Value when only Red LED On. (FEh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CAL_SMXR[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 91. CAL_SMXR_LO register format.

CAL_SMXR_HI: SENSOR_ADCX_HI Value when only Red LED On. (FFh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	N/A						CAL_SMXR[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 92. CAL_SMXR_HI register format.

Table 50. CAL_SMXR register bit description.

Mnemonic	Read / Write Control	Description
N/A	N/A	N/A. Value is ‘0’.
CAL_SMXR[9:0]	R/W	Calibration input register for SENSOR_ADCX values when only red LED on. Maximum value is 1000.

CALDATA0: Calibration Data 0 Register (8Ah)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA0[7:0]							
Reset Value	0	0	1	1	0	1	0	1

Figure 93. Calibration data 0 register format.

Table 51. Calibration data 0 register description.

Mnemonic	Read / Write Control	Description
CALDATA0[7:0]	R/W	Calibration data 0. Default value is 35h.

CALDATA1: Calibration Data 1 Register (8Bh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA1[7:0]							
Reset Value	0	0	0	0	1	0	1	1

Figure 94. Calibration data 1 register format.

Table 52. Calibration data 1 register description.

Mnemonic	Read / Write Control	Description
CALDATA1[7:0]	R/W	Calibration data 1. Default value is 0Bh.

CALDATA2: Calibration Data 2 Register (8Ch)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA2[7:0]							
Reset Value	1	0	1	0	0	1	0	0

Figure 95. Calibration data 2 register format.

Table 53. Calibration data 2 register description.

Mnemonic	Read / Write Control	Description
CALDATA2[7:0]	R/W	Calibration data 2. Default value is A4h.

CALDATA3: Calibration Data 3 Register (8Dh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA3[7:0]							
Reset Value	0	0	0	0	0	1	0	1

Figure 96. Calibration data 3 register format.

Table 54. Calibration data 3 register description.

Mnemonic	Read / Write Control	Description
CALDATA3[7:0]	R/W	Calibration data 3. Default value is 05h.

CALDATA4: Calibration Data 4 Register (8Eh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA4[7:0]							
Reset Value	1	0	0	1	0	1	1	0

Figure 97. Calibration data 4 register format.

Table 55. Calibration data 4 register description.

Mnemonic	Read / Write Control	Description
CALDATA4[7:0]	R/W	Calibration data 4. Default value is 96h.

CALDATA5: Calibration Data 5 Register (8Fh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA5[7:0]							
Reset Value	0	0	0	0	0	0	0	1

Figure 98. Calibration data 5 register format.

Table 56. Calibration data 5 register description.

Mnemonic	Read / Write Control	Description
CALDATA5[7:0]	R/W	Calibration data 5. Default value is 01h.

CALDATA6: Calibration Data 6 Register (90h)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA6[7:0]				
Reset Value	0	1	1	1	0	0	0	0

Figure 99. Calibration data 6 register format.

Table 57. Calibration data 6 register description.

Mnemonic	Read / Write Control	Description
CALDATA6[7:0]	R/W	Calibration data 6. Default value is 70h.

CALDATA7: Calibration Data 7 Register (91h)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA7[7:0]				
Reset Value	0	0	0	0	0	0	0	1

Figure 100. Calibration data 7 register format.

Table 58. Calibration data 7 register description.

Mnemonic	Read / Write Control	Description
CALDATA7[7:0]	R/W	Calibration data 7. Default value is 01h.

CALDATA8: Calibration Data 8 Register (92h)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA8[7:0]				
Reset Value	0	1	0	1	0	0	1	1

Figure 101. Calibration data 8 register format.

Table 59. Calibration data 8 register description.

Mnemonic	Read / Write Control	Description
CALDATA8[7:0]	R/W	Calibration data 8. Default value is 53h

CALDATA9: Calibration Data 9 Register (93h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA9[7:0]							
Reset Value	0	0	0	1	0	1	1	1

Figure 102. Calibration data 9 register format.

Table 60. Calibration data 9 register description.

Mnemonic	Read / Write Control	Description
CALDATA9[7:0]	R/W	Calibration data 9. Default value is 17h

CALDATA10: Calibration Data 10 Register (94h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA10[7:0]							
Reset Value	0	1	0	0	1	1	1	0

Figure 103. Calibration data 10 register format.

Table 61. Calibration data 10 register description.

Mnemonic	Read / Write Control	Description
CALDATA10[7:0]	R/W	Calibration data 10. Default value is 4Eh.

CALDATA11: Calibration Data 11 Register (95h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA11[7:0]							
Reset Value	1	0	0	0	0	0	1	1

Figure 104. Calibration data 11 register format.

Table 62. Calibration data 11 register description.

Mnemonic	Read / Write Control	Description
CALDATA11[7:0]	R/W	Calibration data 11. Default value is 83h.

CALDATA12: Calibration Data 12 Register (96h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA12[7:0]							
Reset Value	0	0	1	1	1	1	1	0

Figure 105. Calibration data 12 register format.

Table 63. Calibration data 12 register description.

Mnemonic	Read / Write Control	Description
CALDATA12[7:0]	R/W	Calibration data 12. Default value is 3Eh.

CALDATA13: Calibration Data 13 Register (97h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA13[7:0]							
Reset Value	1	0	0	0	0	1	0	0

Figure 106. Calibration data 13 register format.

Table 64. Calibration data 13 register description.

Mnemonic	Read / Write Control	Description
CALDATA13[7:0]	R/W	Calibration data 13. Default value is 84h.

CALDATA14: Calibration Data 14 Register (98h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA14[7:0]							
Reset Value	0	1	0	0	0	1	1	1

Figure 107. Calibration data 14 register format.

Table 65. Calibration data 14 register description.

Mnemonic	Read / Write Control	Description
CALDATA14[7:0]	R/W	Calibration data 14. Default value is 47h.

CALDATA15: Calibration Data 15 Register (99h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA15[7:0]							
Reset Value	1	0	0	0	0	1	0	1

Figure 108. Calibration data 15 register format.

Table 66. Calibration data 15 register description.

Mnemonic	Read / Write Control	Description
CALDATA15[7:0]	R/W	Calibration data 15. Default value is 85h.

CALDATA16: Calibration Data 16 Register (9Ah)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA16[7:0]							
Reset Value	0	1	0	0	1	1	0	0

Figure 109. Calibration data 16 register format.

Table 67. Calibration data 16 register description.

Mnemonic	Read / Write Control	Description
CALDATA16[7:0]	R/W	Calibration data 16. Default value is 4Ch.

CALDATA17: Calibration Data 17 Register (9Bh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA17[7:0]							
Reset Value	0	0	0	1	1	0	1	1

Figure 110. Calibration data 17 register format.

Table 68. Calibration data 17 register description.

Mnemonic	Read / Write Control	Description
CALDATA17[7:0]	R/W	Calibration data 17. Default value is 1Bh.

CALDATA18: Calibration Data 18 Register (9Ch)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA18[7:0]				
Reset Value	0	1	1	1	1	1	1	1

Figure 111. Calibration data 18 register format.

Table 69. Calibration data 18 register description.

Mnemonic	Read / Write Control	Description
CALDATA18[7:0]	R/W	Calibration data 18. Default value is 7Fh.

CALDATA19: Calibration Data 19 Register (9Dh)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA19[7:0]				
Reset Value	1	0	0	0	1	1	1	0

Figure 112. Calibration data 19 register format.

Table 70. Calibration data 19 register description.

Mnemonic	Read / Write Control	Description
CALDATA19[7:0]	R/W	Calibration data 19. Default value is 8Eh.

CALDATA20: Calibration Data 20 Register (9Eh)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA20[7:0]				
Reset Value	1	0	0	0	0	1	0	1

Figure 113. Calibration data 20 register format.

Table 71. Calibration data 20 register description.

Mnemonic	Read / Write Control	Description
CALDATA20[7:0]	R/W	Calibration data 20. Default value is 85h.

CALDATA21: Calibration Data 21 Register (9Fh)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA21[7:0]				
Reset Value	1	0	1	0	0	1	1	1

Figure 114. Calibration data 21 register format.

Table 72. Calibration data 21 register description.

Mnemonic	Read / Write Control	Description
CALDATA21[7:0]	R/W	Calibration data 21. Default value is A7h.

CALDATA22: Calibration Data 22 Register (A0h)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA22[7:0]				
Reset Value	0	1	1	1	0	1	1	1

Figure 115. Calibration data 22 register format.

Table 73. Calibration data 22 register description.

Mnemonic	Read / Write Control	Description
CALDATA22[7:0]	R/W	Calibration data 22. Default value is 77h.

CALDATA23: Calibration Data 23 Register (A1h)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA23[7:0]				
Reset Value	1	0	0	0	0	1	1	0

Figure 116. Calibration data 23 register format.

Table 74. Calibration data 23 register description.

Mnemonic	Read / Write Control	Description
CALDATA23[7:0]	R/W	Calibration data 23. Default value is 86h.

CALDATA24: Calibration Data 24 Register (A2h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA24[7:0]							
Reset Value	1	0	0	0	1	0	1	0

Figure 117. Calibration data 24 register format.

Table 75. Calibration data 24 register description.

Mnemonic	Read / Write Control	Description
CALDATA24[7:0]	R/W	Calibration data 24. Default value is 8Ah.

CALDATA25: Calibration Data 25 Register (A3h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA25[7:0]							
Reset Value	1	0	0	1	1	1	0	0

Figure 118. Calibration data 25 register format.

Table 76. Calibration data 25 register description.

Mnemonic	Read / Write Control	Description
CALDATA25[7:0]	R/W	Calibration data 25. Default value is 9Ch.

CALDATA26: Calibration Data 26 Register (A4h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA26[7:0]							
Reset Value	0	1	0	1	0	0	0	1

Figure 119. Calibration data 26 register format.

Table 77. Calibration data 26 register description.

Mnemonic	Read / Write Control	Description
CALDATA26[7:0]	R/W	Calibration data 26. Default value is 51h.

CALDATA27: Calibration Data 27 Register (A5h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA27[7:0]							
Reset Value	0	1	0	0	1	0	1	1

Figure 120. Calibration data 27 register format.

Table 78. Calibration data 27 register description.

Mnemonic	Read / Write Control	Description
CALDATA27[7:0]	R/W	Calibration data 27. Default value is 4Bh.

CALDATA28: Calibration Data 28 Register (A6h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA28[7:0]							
Reset Value	0	0	0	0	0	0	1	1

Figure 121. Calibration data 28 register format.

Table 79. Calibration data 28 register description.

Mnemonic	Read / Write Control	Description
CALDATA28[7:0]	R/W	Calibration data 28. Default value is 03h.

CALDATA29: Calibration data 29 Register (A7h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	CALDATA29[7:0]							
Reset Value	1	0	0	1	1	0	1	0

Figure 122. Calibration data 29 register format.

Table 80. Calibration data 29 register description.

Mnemonic	Read / Write Control	Description
CALDATA29[7:0]	R/W	Calibration data 29. Default value is 9Ah.

CALDATA30: Calibration Data 30 Register (A8h)

Bit	7	6	5	4	3	2	1	0
Mnemonic				CALDATA30[7:0]				
Reset Value	0	0	0	1	0	0	0	1

Figure 123. Calibration data 30 register format.

Table 81. Calibration data 30 register description.

Mnemonic	Read / Write Control	Description
CALDATA30[7:0]	R/W	Calibration data 30. Default value is 11h.

DUTY_LIMIT: Maximum Duty Limit Registers (E6h-E7h)

DUTY_LIMIT_LO: Maximum Duty Limit Low Byte Register (E6h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	DUTY_LIMIT[7:0]							
Reset Value	0	0	1	1	0	0	1	0

Figure 124. Maximum duty limit low byte register format.

DUTY_LIMIT_HI: Maximum Duty Limit High Byte Register (E7h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV				DUTY_LIMIT[11:8]			
Reset Value	0	0	0	0	1	1	1	1

Figure 125. Maximum duty limit high byte register format.

Table 82. Maximum duty limit registers description.

Mnemonic	Read / Write Control	Description
RSV	N/A	RSV. Value is '0'.
DUTY_LIMIT[11:0]	R/W	Maximum duty limit register. Default value is 0F32h (95% of 0FFFh). All three color's PWM, i.e., PWM_R, PWM_G, PWM_B, duty cycle will not exceed this register value.

BETA: Brightness Scalar Register (C4h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	BETA[7:0]							
Reset Value	1	1	1	1	1	1	1	1

Figure 126. Brightness scalar register format.

Table 83. Brightness scalar register description.

Mnemonic	Read / Write Control	Description
BETA[7:0]	R/W	Brightness scalar register. Default value is FFh. When BETA is loaded with FFh (maximum value), there will be no brightness scaling involved. When BETA is less than FFh, brightness (camera Y) will be scaled with BETA/FFh. For example, overall display brightness will be halved when BETA is loaded with 7Fh.

COLOR_SETC: User Color Set Point C Register (E8h-E9h)

COLOR_SETC_LO: User Color Set Point C Low Byte Register (E8h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	COLOR_SETC[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 127. User color set point C low byte register format.

COLOR_SETC_HI: User Color Set Point C High Byte Register (E9h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV						COLOR_SETC[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 128. User color set point C high byte register format.

Table 84. User color set point C register bit description.

Mnemonic	Read / Write Control	Description
RSV	N/A	Reserved. Value is '0'.
COLOR_SETC[9:0]	R/W	User color set point C register. Represents different values depending on the chosen color space: Color Space — Value CIE XYZ — Tristimulus Z value from 0 to 1000 CIE 1931 Yxy — Chromaticity y coordinate * 1000 CIE 1976 Yu'v' — Chromaticity v' coordinate * 1000 CIE RGB — B component value from 0 to 255

COLOR_SETB: User Color Set Point B Register (EAh-EBh)

COLOR_SETB_LO: User Color Set Point B Low Byte Register (EAh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	COLOR_SETB[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 129. User color set point B low byte register format.

COLOR_SETB_HI: User Color Set Point B High Byte Register (EBh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV						COLOR_SETB[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 130. User color set point B high byte register format.

Table 85. User color set point B register bit description.

Mnemonic	Read / Write Control	Description
RSV	N/A	RSV. Value is '0'.
COLOR_SETB[9:0]	R/W	User color set point B register. Represents different values depending on the chosen color space: Color Space — Value CIE XYZ — Tristimulus Y value from 0 to 1000 CIE 1931 Yxy — Chromaticity x coordinate * 1000 CIE 1976 Yu'v' — Chromaticity u' coordinate * 1000 CIE RGB — G component from 0 to 255

COLOR_SETA: User Color Set Point A Register (ECh-EDh)

COLOR_SETA_LO: User Color Set Point A Low Byte Register (ECh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	COLOR_SETA[7:0]							
Reset Value	0	0	0	0	0	0	0	0

Figure 131. User color set point A low byte register format.

COLOR_SETA_HI: User Color Set Point A High Byte Register (EDh)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RSV						COLOR_SETA[9:8]	
Reset Value	0	0	0	0	0	0	0	0

Figure 132. User color set point A high byte register format.

Table 86. User color set point A register bit description.

Mnemonic	Read / Write Control	Description
RSV	N/A	Reserved. Value is '0'.
COLOR_SETA[9:0]	R/W	User color set point A register. Represents different values depending on the chosen color space: Color Space — Value CIE XYZ — Tristimulus X value from 0 to 1000 CIE 1931 Yxy — Luminance Y value from 0 to 1000 CIE 1976 Yu'v' — Luminance Y value from 0 to 1000 CIE RGB — R component value from 0 to 255

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