

Application Note 5398

Introduction

This application note describes a method to speed up brightness change using BRIGHT register of the ADJD-J823 color management controller. This method is an extension to Application Note 5241 and can be optionally implemented. The color management system is fully functional with the instructions described in AN5241.

The benefit of implementing the described method is fast change of brightness level, especially when changing brightness level by big percentage. It does reduce brightness change response time significantly.

Description of Method

The flow of this method is to read out duty factor and internal state registers, scale those registers and write them back to ADJD-J823. The scale ratio of these registers will be determined by current BRIGHT value and new BRIGHT value. This method should only take place after target color point has settled down.

Table 1: Duty Factor and Internal State Register Address

Address		Register	Description	Reset Value
Decimal	Hex			
36	24	DUTYB_LO	Blue Duty Factor Low Byte Register	0
37	25	DUTYB_HI	Blue Duty Factor High Byte Register	0
38	26	DUTYG_LO	Green Duty Factor Low Byte Register	0
39	27	DUTYG_HI	Green Duty Factor High Byte Register	0
40	28	DUTYR_LO	Red Duty Factor Low Byte Register	0
41	29	DUTYR_HI	Red Duty Factor Low Byte Register	0
202	CA	INT_STATE_A[7:0]	Internal State Register A1	0
203	CB	INT_STATE_A[15:8]	Internal State Register A2	0
204	CC	INT_STATE_A[23:16]	Internal State Register A3	0
205	CD	INT_STATE_B[7:0]	Internal State Register B1	0
206	CE	INT_STATE_B[15:8]	Internal State Register B2	0
207	CF	INT_STATE_C[7:0]	Internal State Register C1	0
208	D0	INT_STATE_C[15:8]	Internal State Register C2	0
209	D1	INT_STATE_C[23:16]	Internal State Register C3	0
210	D2	INT_STATE_D[7:0]	Internal State Register D1	0
211	D3	INT_STATE_D[15:8]	Internal State Register D2	0
212	D4	INT_STATE_E[7:0]	Internal State Register E1	0
213	D5	INT_STATE_E[15:8]	Internal State Register E2	0
214	D6	INT_STATE_F[7:0]	Internal State Register F1	0
215	D7	INT_STATE_F[15:8]	Internal State Register F2	0
216	D8	INT_STATE_F[23:16]	Internal State Register F3	0
217	D9	INT_STATE_F[31:24]	Internal State Register F4	0
218	DA	INT_STATE_G[7:0]	Internal State Register G1	0
219	DB	INT_STATE_G[15:8]	Internal State Register G2	0
220	DC	INT_STATE_G[23:16]	Internal State Register G3	0
221	DD	INT_STATE_G[31:24]	Internal State Register G4	0
222	DE	INT_STATE_H[7:0]	Internal State Register H1	0
223	DF	INT_STATE_H[15:8]	Internal State Register H2	0
224	E0	INT_STATE_H[23:16]	Internal State Register H3	0
225	E1	INT_STATE_H[31:16]	Internal State Register H4	0
230	E6	INT_STATE_I[7:0]	Internal State Register I1	121
231	E7	INT_STATE_I[15:8]	Internal State Register I2	14

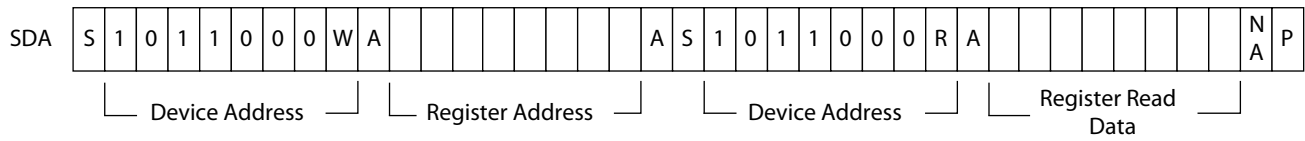
I²C Command Interface Protocol

Figure 1 describes the structure of the command to specify the I²C write cycle and read cycle. This command structure will be used throughout the application note.

Write Cycle



Read Cycle



- Notes:
- S Start Condition
 - P Stop Condition
 - W Write bit (Logic 0)
 - R Read bit (Logic 1)
 - A Acknowledge (Logic 0)
 - NA Not Acknowledge (Logic 1)

Figure 1. Write Cycle and Read Cycle Command Structure

Programming Guide

User communicates new BRIGHT value to ADJD-J823 through the System Controller. Figure 2 and Figure 3 explain the fast brightness change method flowchart. Examples given in Figure 3 only process duty factor registers for illustration. All internal state registers have to be processed using the same method.

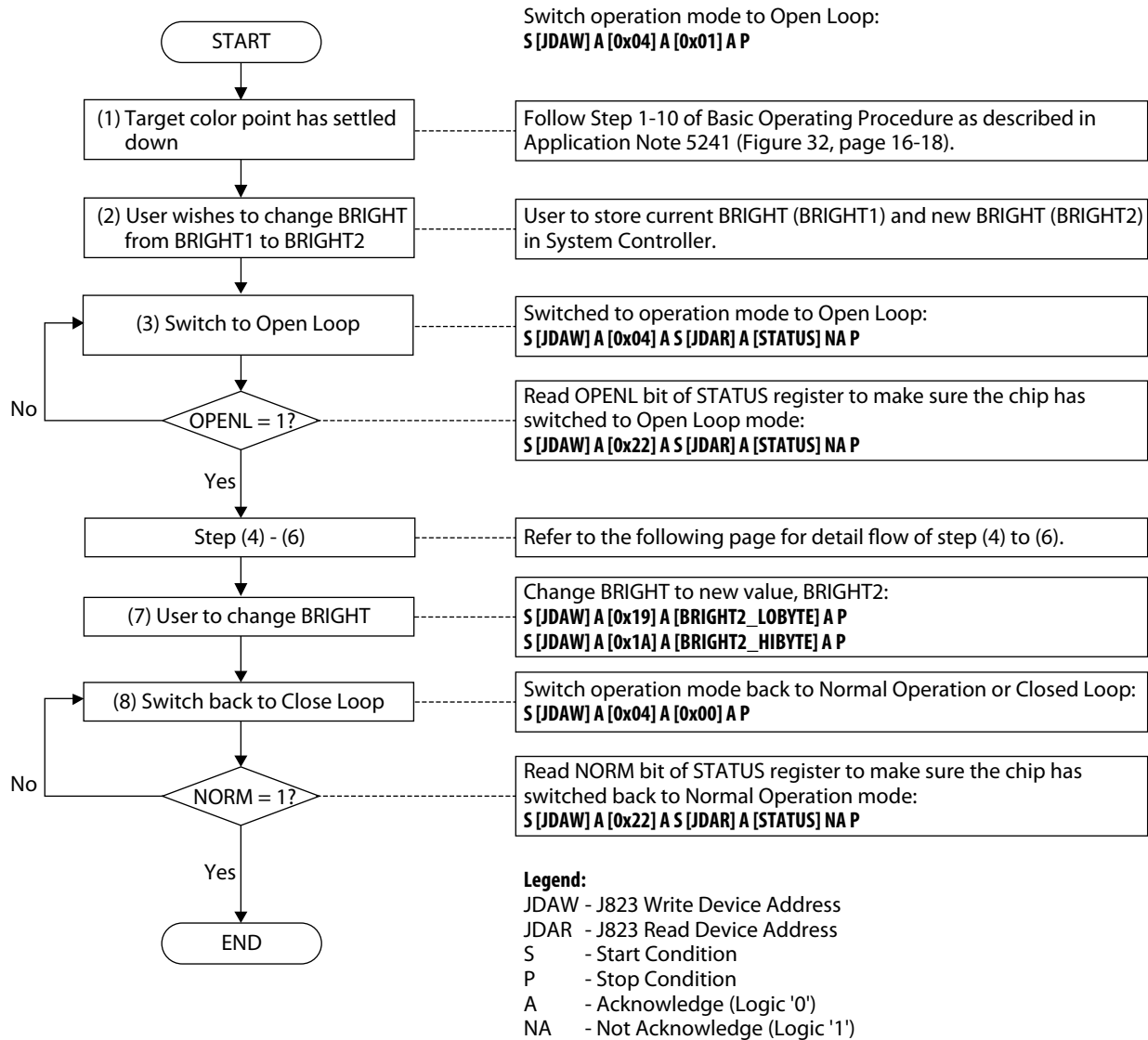


Figure 2. Fast brightness change using BRIGHT Flowchart

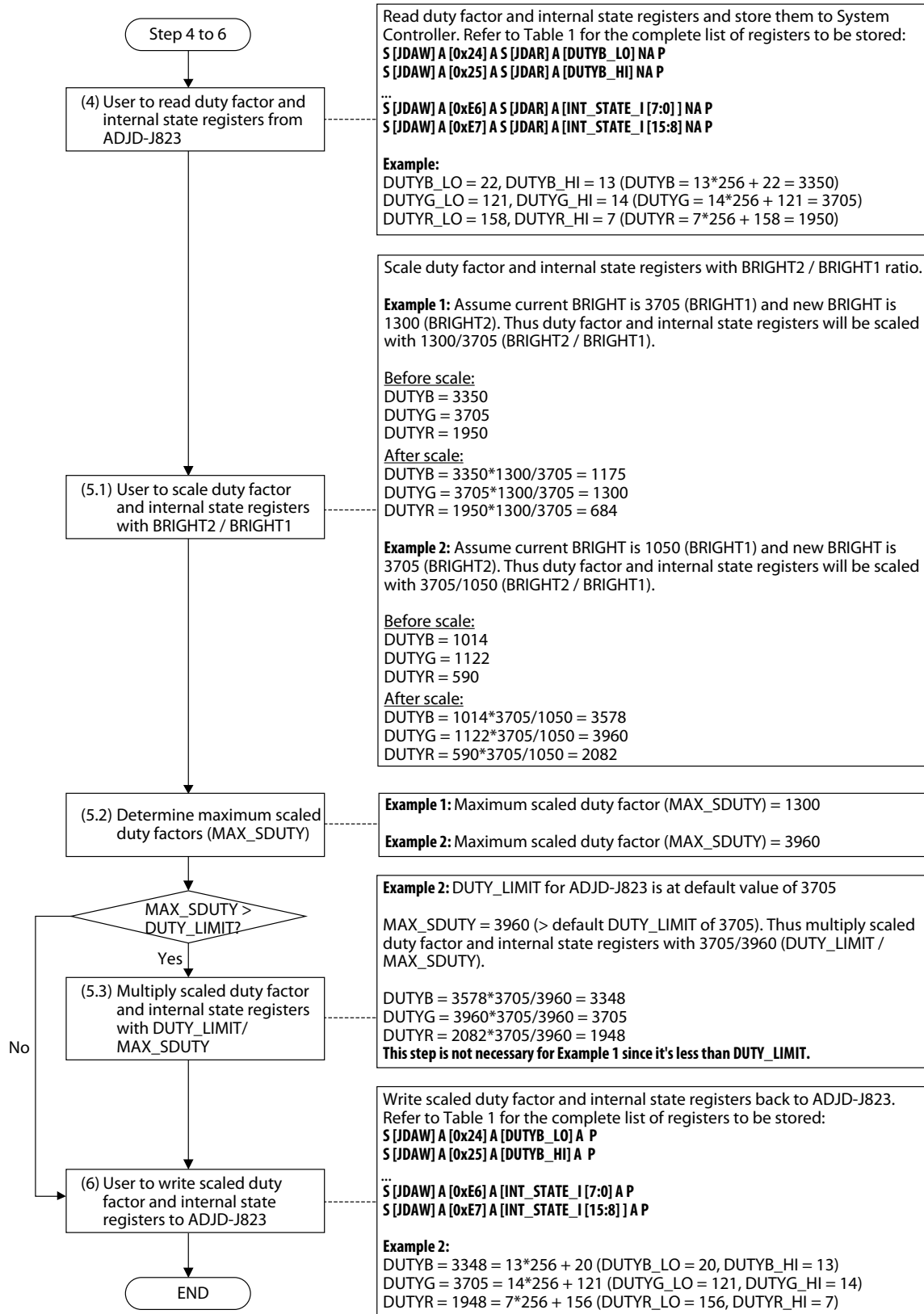


Figure 3. Step (4) to (6) Flowchart

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries.
Data subject to change. Copyright © 2005-2008 Avago Technologies. All rights reserved.
AV02-1422EN - July 17, 2008

