Designing a Boost LED Driver Using the LM5022

Introduction

This application note provides a component-by-component design guide for a boost converter-based LED driver using the LM5022. The converter operates from a 12V ±10% input and drives ten series connected white LEDs with a controlled current of 1.0A ±10% and an output ripple current of 200 mA$_{P-P}$ or less. The circuit schematic is shown in *Figure 1*. Details for the PCB and performance characteristics of this converter are available in AN-1605.
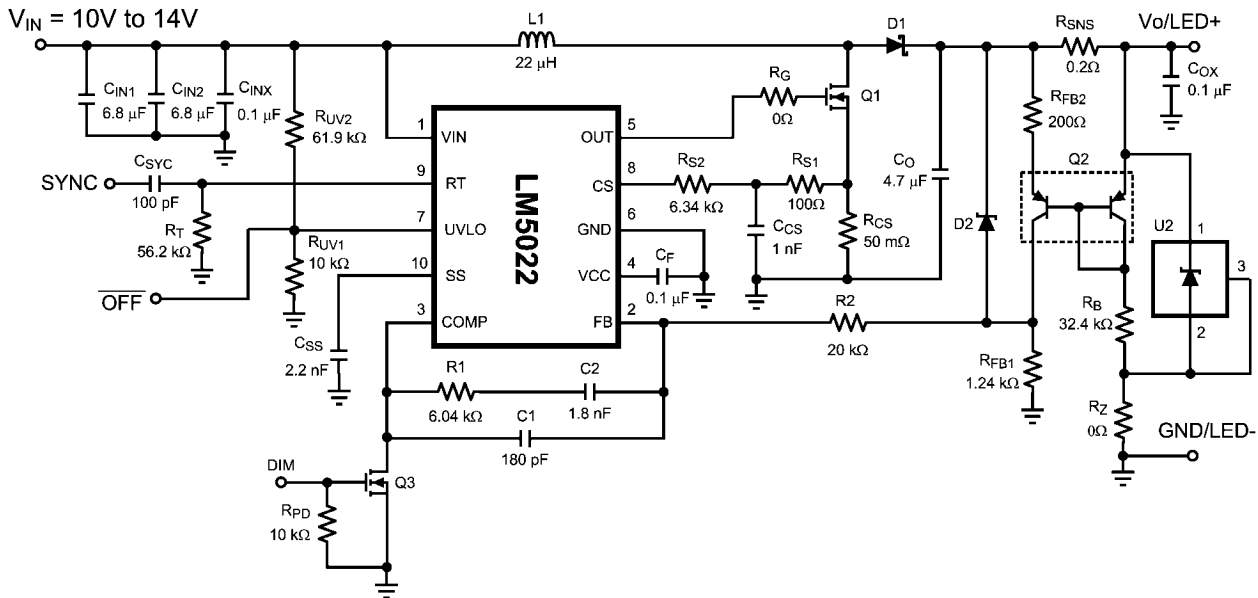

FIGURE 1. Circuit Schematic

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Output Voltage

The forward voltage, V_F, of each LED varies by manufacturer, by process and with temperature, so to simplify the design the maximum V_F of 4.0V at 1.0A has been selected. Using V_{F-MAX} ensures that the inductor and power MOSFET will meet the worst-case power dissipation requirements of the system. Some calculations will use the typical forward voltage of the LED array, which is 3.3V per LED.

The total output voltage, V_O, is equal to the number of series connected LEDs, n, multiplied by V_F plus the voltage dropped across the current sensing resistor (R_{SNS}) placed in series with the LED chain, V_{SNS}. For this example V_{SNS} will be 200 mV, a compromise between the power dissipated in R_{SNS} and the signal-to-noise ratio (SNR) of the current sensing circuit.

$$V_O = n \times V_F + V_{SNS}$$

$$V_{O-MAX} = 10 \times 4.0 + 0.2 = 40.2V \text{ (maximum)}$$

$$V_O = 10 \times 3.3 + 0.2 = 33.2V \text{ (typical)}$$

Duty Cycle

All boost regulators (voltage or current) step up the input voltage to produce a higher output voltage, and have a duty ratio D of:

$$D = \frac{V_O - V_{IN} + V_D}{V_O + V_D}$$

(V_D is the forward voltage drop of the output diode)

LED Current Sensing Resistor

R_{SNS} should be 0.2Ω to set an LED current of 1.0A with a sensing voltage of 200 mV. The power dissipated in R_{SNS} is $1.0^2 \times 0.2 = 200$ mW. A 0.33W, 1% resistor in 1206 will be used.

High-Side Current Sense

The LM5022 boost LED evaluation boards employs a level shift using a matched pair of PNP transistors. Matching of the base-to-emitter voltages helps ensure that the output current will meet the ±10% specification, as unmatched transistors can lead to output current errors greater than ±20%. This circuit, detailed in *Figure 2*, serves two purposes. First, it senses

the LED current differentially across R_{SNS} and level-shifts the signal to interface with the FB pin of the LM5022. Second, the transistors amplify the current sense voltage, V_{SNS}, reducing the power dissipated in R_{SNS} and allowing the user to select

the amplitude of V_{SNS}. A high-side current sense is helpful for applications where the cathode of the last LED connects to system ground.
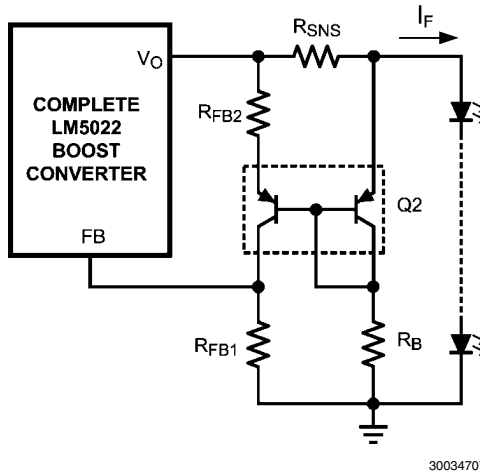

FIGURE 2. PNP Current Mirror for High-side Current Sensing

Resistor R_B sets a bias current through the right-hand transistor. The suggested bias current for the PNP transistors is 1 mA. R_B is selected by dividing the typical output voltage minus one diode drop by 1 mA.

$$R_B = (V_O - 0.6) / 0.001 = 32.6 \text{ k}\Omega$$

$$R_B = 32.4 \text{ k}\Omega \text{ 1\%}$$

R_{FB1} is set to bias the left-hand PNP at 1 mA, using the following expression.

$$R_{FB1} = 1.25 / 0.001 = 1.25 \text{ k}\Omega$$

$$R_{FB1} = 1.24 \text{ k}\Omega \text{ 1\%}$$

R_{FB2} is set to amplify the current sense signal to equal the feedback voltage:

$$R_{FB2} = (I_F \times R_{SNS} \times R_{FB1}) / 1.25$$

$$R_{FB2} = (1.0 \times 0.2 \times 1240) / 1.25 = 198\Omega$$

$$R_{FB2} \text{ is } 200\Omega \text{ 1\%}$$

Switching Frequency

The selection of switching frequency is based on the tradeoffs between size, cost, and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors will be needed. A higher switching frequency generally results in a smaller but less efficient solution because switching and gate charging losses increase with f_{SW}. 300 kHz will be used for this circuit, a good compromise between inductor size and system efficiency.

$$R_T = \frac{1 - 8 \times 10^{-8} \times f_{SW}}{f_{SW} \times 5.77 \times 10^{-11}}$$

(f_{SW} in Hz, R_T in Ω)

$$R_T = 56.2 \text{ k}\Omega \text{ 1\%}$$

MOSFET

Selection of the power MOSFET is also governed by tradeoffs between cost, size, and efficiency. Breaking down the losses in the MOSFET is one way to determine relative efficiencies between different devices. For this example, the SO-8 package provides the balance of a small footprint with the ability to dissipate at least 1W in steady state. Losses in the MOSFET can be broken down into conduction loss, gate charging loss, and switching loss.

Conduction, or I^2R, loss, P_C, is approximately:

$$P_C = D \times \left[\left(\frac{I_O}{1-D} \right)^2 \times R_{DSON} \times 1.3 \right]$$

The factor 1.3 accounts for the increase in MOSFET on resistance due to heating. Alternatively, the factor of 1.3 can be ignored and the maximum high temperature on-resistance of the MOSFET can be used.

Gate charging loss, P_G, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated as:

$$P_G = V_{CC} \times Q_G \times f_{SW}$$

Q_G is the total gate charge of the MOSFET. Gate charge loss differs from conduction and switching losses because the actual dissipation occurs in the LM5022 and not in the MOSFET itself. If no external bias is applied to the VCC pin, additional loss in the LM5022 IC occurs as the MOSFET driver supply

current flows through the V_{CC} regulator. The loss term P_G for this case becomes:

$$P_G = V_{IN} \times Q_G \times f_{SW}$$

Switching loss, P_{SW}, occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times [I_F / (1 - D)] \times (t_R + t_F) \times f_{SW}$$
(t_R and t_F are the rise and fall times of the MOSFET)

For this example, the maximum drain-to-source voltage applied across the MOSFET is 40.2V plus the ringing due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the high side MOSFET is VCC, or 7V typical. The MOSFET selected must be able to withstand 40.2V plus any ringing from drain to source, and be able to handle at least 7V plus ringing from gate to source. A minimum voltage rating of 50VDS and $10V_{GS}$ MOSFET will be used. Comparing the losses in a spreadsheet leads to a $60V_{DS}$ rated MOSFET in SO-8 with a maximum R_{DSON} of 31 $m\Omega$, a gate charge of 27 nC, and rise and falls times of 10 ns and 12 ns, respectively.

Output Diode

The boost regulator requires an output diode D1 (see *Figure 1*) to carry the inductor current during the MOSFET off-time. The most efficient choice for D1 is a Schottky diode due to low forward drop and zero reverse recovery time. D1 must be rated to handle the maximum output voltage plus any switch-node ringing when the MOSFET is on. In practice, all switching converters have some ringing at the switch-node due to the diode parasitic capacitance and the lead inductance.

D1 must also be rated to handle the average output current, I_F. The power dissipation can be calculating by checking the typical diode forward voltage, V_D, from the I-V curve on the diode's datasheet and then multiplying it by I_F. Diode datasheets will also provide a typical junction-to-ambient thermal resistance, θ_{JA}, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation ($P_D = I_F \times V_D$) by θ_{JA} gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum.

In this example a Schottky diode rated to 60V and 2A will be suitable, as the maximum LED current will be 1A. A small case such as SMA can be used if a small footprint is critical. Larger case sizes generally have lower θ_{JA} and lower forward voltage drop, so for better efficiency the larger SMB case size will be used.

Boost Inductor

The first criterion for selecting an inductor is the inductance itself. In fixed-frequency boost converters this value is based on the desired peak-to-peak ripple current, Δi_L, which flows in the inductor along with the average inductor current, I_L. For a boost converter in continuous conduction mode (CCM) I_L is greater than the LED current, I_F. The two currents are related by the following expression:

$$I_L = I_F / (1 - D)$$

As with switching frequency, the inductance used is a tradeoff between size and cost. Larger inductance means lower input ripple current, however because the inductor is connected to the output during the off-time only there is a limit to the reduction in output ripple voltage. Lower inductance results in smaller, less expensive magnetics. An inductance that gives a ripple current of 30% to 50% of I_L is a good starting point for a CCM boost converter. Minimum inductance should be calculated at the extremes of input voltage to find the operating condition with the highest requirement:

$$L_1 = \frac{V_{IN} \times D}{f_{SW} \times \Delta i_L}$$

By calculating in terms of amperes, volts, and megahertz, the inductance value will come out in microhenrys. In order to ensure that the boost regulator operates in CCM a second equation is needed, and must also be evaluated at the corners of input voltage to find the minimum inductance required:

$$L_2 = \frac{D(1-D) \times V_{IN}}{I_O \times f_{SW}}$$

By calculating in terms of volts, amps and megahertz the inductance value will come out in microhenrys.

For this design Δi_L will be set to 40% of I_L. First, duty cycle is evaluated at both V_{IN-MIN} and at V_{IN-MAX}. Second, the average inductor current is evaluated at the two input voltages. Third, the inductor ripple current is determined. Finally, the inductance can be calculated and a standard inductor value selected that meets all the criteria.

Inductance for Minimum Input Voltage

$$D = (40.2 - 10.8 + 0.5) / (40.2 + 0.5) = 73\%$$
$$I_L = 1.0 / (1 - 0.73) = 3.7A$$
$$\Delta i_L = 0.4 \times 3.7 = 1.5A$$
$$L_1 = (10.8 \times 0.73) / (0.3 \times 1.5) = 17.5 \ \mu H$$
$$L_2 = (0.73 \times 0.27 \times 10.8) / (1.0 \times 0.3) = 7.1 \ \mu H$$

Inductance for Maximum Input Voltage

$$D = (40.2 - 13.2 + 0.5) / (40.2 + 0.5) = 67\%$$
$$I_L = 1.0 / (1 - 0.67) = 3.0A$$
$$\Delta i_L = 0.4 \times 3.0 = 1.2A$$
$$L_1 = (13.2 \times 0.67) / (0.3 \times 1.2) = 24.6 \ \mu H$$
$$L_2 = (0.67 \times 0.33 \times 13.2) / (1.0 \times 0.3) = 9.7 \ \mu H$$

Maximum average inductor current occurs at V_{IN-MIN}, and the corresponding inductor ripple current is 1.5A$_{P-P}$. Selecting an inductance that exceeds the ripple current requirement at V_{IN-MIN} and the requirement to stay in CCM for V_{IN-MAX} provides a tradeoff that allows smaller magnetics at the cost of higher ripple current at maximum input voltage. For this example, a 22 μH inductor will satisfy these requirements.

The second criterion for selecting an inductor is the peak current carrying capability. This is the level above which the inductor will saturate. In saturation the inductance can drop off severely, resulting in higher peak current that may overheat the inductor or push the converter into current limit. In a

boost converter, peak inductor/switch current, I_{PK}, is equal to the maximum average inductor current plus one half of the ripple current. First, the ripple current must be determined under the conditions that give maximum average inductor current:

$$\Delta i_L = \frac{V_{IN} \times D}{f_{SW} \times L}$$

Maximum average inductor current occurs at V_{IN-MIN}. Using the selected inductance of 22 µH yields the following:

$$\Delta i_L = (10.8 \times 0.73) / (0.3 \times 22) = 1.2 A_{P-P}$$

The highest peak inductor current is therefore:

$$I_{PK} = I_L + \Delta i_L / 2 = 3.7 + 0.6 = 4.3A$$

Hence an inductor must be selected that has a peak current rating greater than 4.3A and an average current rating greater than 3.7A. One possibility is an off-the-shelf 22 µH ±20% inductor that can handle a peak current of 4.8A and an average current of 4.6A. Finally, the inductor current ripple is recalculated at the maximum input voltage. This value will be used later to select the input capacitors.

$$\Delta i_L = (13.2 \times 0.67) / (0.3 \times 22) = 1.3 A_{P-P}$$

Output Capacitor

The output capacitor in a current regulator is selected to control the output ripple current, Δi_F, as opposed to a voltage regulator, where Δv_O is controlled. As a constant current source, this application does not need bulk capacitance to supply the load during load transients. LED drivers rarely require more than 10 µF of output capacitance, making multilayer ceramic capacitors (MLCCs) an attractive choice. For the output capacitor of a switching regulator the minimum quality dielectric that should be used is X5R, and X7R or better is preferred.

One simple method to determine the required output capacitance is to first determine the desired output ripple current and then multiply by the load impedance, Z_O. The result is the output ripple voltage, which can then be used to select C_O. For an LED driver Z_O is equal to:

$$Z_O = n \times r_D + R_{SNS}$$

In this expression n is the number of LEDS in series, r_D is the dynamic resistance of each individual LED in the chain and R_{SNS} is the LED current sense resistor. Some LED manufacturers provide typical values for r_D, however in most cases it must be determined by taking the inverse of the slope I_F vs. V_F curve at the desired value of I_F. In practice r_D can differ from the stated value by 50% to 200%, and the best method to determine r_D is to measure the I-V characteristic of the entire array. A curve of V_F vs. I_F for the ten-LED chain is shown in *Figure 3*.
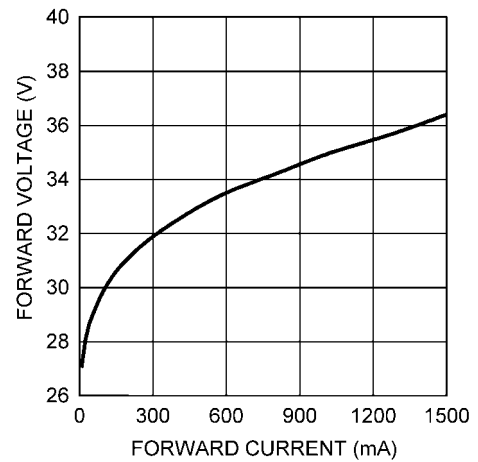
FIGURE 3. V_F vs. I_F for Ten White LEDs

The slope of the curve at 1.0A is approximately 3.2Ω.

The recommended range of Δi_F is from 10% to 40% of the average current. For this example the ripple current will be set to 20% of I_F, or 200 mA$_{P-P}$. Output impedance is therefore equal to 3.4Ω. Minimum output capacitance should be calculated using the maximum duty cycle (at minimum input voltage). Calculating in terms of amperes, megahertz and ohms will lead to results in microfarads.

$$C_{O-MIN} = \frac{I_F \times D}{f_{SW} \times \Delta i_F \times Z_O}$$

$$C_{O-MIN} = (1.0 \times 0.73) / (0.3 \times 0.2 \times 3.4) = 3.6 \ \mu F$$

MLCCs have low ESR, small size, and high ripple current capability, but they suffer a loss in capacitance when a DC bias is placed across them. For this example, the closest standard voltage rating above 40.2V is 50V. Consultation of several MLCC datasheets reveals that a 50V, 4.7 µF capacitor in an 1812 case size loses about 25% of its rated capacitance at 40V, yielding about 3.5 µF. This is close enough for this application. This device has an ESR, R_C, of 3 mΩ.

Output capacitors in boost regulators endure a large AC RMS current due to the discontinuous current from the inductor. The RMS value for the output capacitor AC current should be calculated at minimum input voltage using the following:

$$I_{O-RMS} = 1.13 \times I_L \times \sqrt{D \times (1 - D)}$$

$$I_{O-RMS} = 1.13 \times 3.6 \times \text{Sqrt}(0.73 \times 0.27) = 1.8A$$

The 4.7 µF, 50V capacitor in a 2220 case has a ripple current rating of over 3A.

Input Capacitor

The input capacitors in a boost regulator control the input voltage ripple, Δv_{IN}, and prevent impedance mismatch (also called power supply interaction) between the LM5022 and the inductance of the input leads. Selection of input capacitors is based on their capacitance, ESR, and RMS current rating.

The minimum input capacitance is based on Δv_{IN} or prevention of power supply interaction. In general, the requirement for greatest capacitance comes from the power supply interaction. The inductance, L_S, and resistance, R_S, of the input source must be estimated, and if this information is not available, they can be assumed to be 1 µH and 0.1Ω, respectively. Minimum capacitance is then estimated as:

$$C_{MIN} = \frac{2 \times L_S \times V_O \times I_F}{V_{IN}^2 \times R_S}$$

Calculation in microhenrys, volts, amperes and ohms will give a result in microfarads. The worst-case minimum capacitance calculation comes at the minimum input voltage. Using the default estimates for L_S and R_S, minimum capacitance is:

$$C_{MIN} = (2 \times 1 \times 40.2 \times 1.0) / (10.8^2 \times 0.1) = 6.9 \text{ µF}$$

The next closest standard 20% capacitor value is 6.8 µF. The final calculation is for the input RMS current. For boost converters operating in CCM this can be estimated as:

$$I_{IN\text{-}RMS} = 0.29 \times \Delta i_L$$

Maximum inductor ripple current is 1.3A, hence the input capacitor must be rated to handle 0.29 x 1.3 = 0.38A_{RMS}.

For this example, the input capacitor will be two 6.8 µF MLCCs rated to 25V, in the 1210 case size. The RMS current rating of these capacitors is over 2A each, more than enough for this application, and the 25V rating ensures that enough capacitance remains when the DC bias is applied.

Open Circuit Zener Diode

The broken/open LED protection zener diode D2 is selected to close the control loop at a voltage just above the steady state output voltage in the event the LEDs are disconnected or fail open circuit. For this example the maximum V_O in steady state is 40.2V, hence a zener diode with a minimum breakdown voltage V_Z of 44.65V will be used. Referring to Figure 1, the total output voltage when D2 breaks down will be V_Z plus 1.25V, or 46.0V. R_{FB1} limits the zener current to 1 mA, hence the approximate power dissipation in D2 will be 47 x 0.001 = 47 mW. A 0.25W device in the SOD-323 package will be used.

V_{IN} and V_O Decoupling Capacitors

All switching regulators benefit from low value MLCCs placed in parallel to their main input and output capacitors. For the LM5022, 100 nF, X7R, 100V rated capacitors in 0805 should be placed at both the input and output. The input capacitor, C_{INX}, should be placed closest to the VIN and GND pins of the LM5022. The output capacitor, C_{OX}, should be placed closest to the LEDs or the connector in applications where the LEDs are mounted on a separate PCB.

VCC Decoupling Capacitor

The VCC pin should be decoupled with a ceramic capacitor placed as close as possible to the VCC and GND pins of the LM5022. The decoupling capacitor should have a minimum X5R or X7R type dielectric to ensure that the capacitance remains stable over voltage and temperature, and be rated to a minimum of 470 nF. One good choice is a 1.0 µF device with X7R dielectric and 1206 case size rated to 25V.

Current Sense Filter

Parasitic circuit capacitance, inductance and gate drive current create a spike in the current sense voltage at the point where Q1 turns on. In order to prevent this spike from terminating the on-time prematurely, every circuit should have a low-pass filter that consists of C_{CS} and R_{S1}, shown in Figure 1. The time constant of this filter should be long enough to reduce the parasitic spike without significantly affecting the shape of the actual current sense voltage. The recommended range for R_{S1} is between 10Ω and 1 kΩ, and the recommended range for C_{CS} is between 100 pF and 2.2 nF. For this example, the values of R_{S1} and C_{CS} will be 100Ω and 1 nF, respectively.

R_{CS}, R_{S2} and Current Limit

The current sensing resistor R_{CS} is used for steady state regulation of the peak inductor current and to sense over-current conditions. The slope compensation resistor R_{S2} is used to ensure control loop stability, and both resistors affect the current limit threshold. R_{CS} must be low enough to keep the power dissipation to a minimum, yet high enough to provide good signal-to-noise ratio for the current sensing circuitry. R_{CS} and R_{S2} should be set so that the current limit comparator trips before the sensed current exceeds the peak current rating of the inductor, without limiting the output power in steady state.

For this example the peak current, at $V_{IN\text{-}MIN}$, is 4.3A, while the inductor peak current rating is 4.8A. The threshold for current limit, I_{LIM}, is set between these two values to account for tolerance of the circuit components, at a level of 4.5A. The required resistor calculation must take into account both the switch current through R_{CS} and the compensation ramp current flowing through R_{S1}, R_{S2} and an internal 2 kΩ resistor. (For more detail see the LM5022 datasheet.) R_{CS} is selected first because it is a power resistor with higher cost and limited selection. The following equation should be evaluated at $V_{IN\text{-}MIN}$:

$$R_{CS} = \frac{L \times f_{SW} \times V_{CL}}{(V_O - V_{IN}) \times 3 \times D + L \times f_{SW} \times I_{LIM}}$$

In this expression V_{CL} is the threshold of the current limit comparator, equal to 0.5V. Calculating with microhenrys, megahertz, volts and amperes will give the result in ohms.

$$R_{CS} = \frac{22 \times 0.3 \times 0.5}{(40.2 - 10.8) \times 3 \times 0.73 + 22 \times 0.3 \times 4.5} = 0.035\Omega$$

The limited selection of power resistors leads to a 50 mΩ device. Power dissipation in R_{CS} can be estimated by calculating the average current. The worst-case average current occurs at minimum input voltage/maximum duty cycle and can be calculated as:

$$P_{CS} = \left[\left(\frac{I_F}{1\text{-}D} \right)^2 \times R_{CS} \right] \times D$$

$$P_{CS} = [(1.0 / 0.27)^2 \times 0.05] \times 0.73 = 0.5W$$

For this example a 50 mΩ 1%, thick-film chip resistor in a 1210 case size rated to 0.5W will be used.

With R_{CS} selected, R_{S2} can be determined using the following expression:

$$R_{S2} = \frac{V_{CL} - I_{LIM} \times R_{CS}}{45\mu \times D} - 2000 - R_{S1}$$

$R_{S2} = (0.5 - 4.5 \times 0.05) / (45\mu \times 0.73) - 2100 \quad R_{S2} = 6270\Omega$

The closest 1% tolerance value is 6.34 kΩ.

UVLO Threshold

In this example the regulator begins to operate after the input voltage has risen above 9.0V. In the case of a brown-out or droop at the input, the UVLO function prevents the LM5022 from drawing high currents that could overheat the inductor or the MOSFET. The UVLO threshold is set with a standard resistor divider equation. With R_{UV1} set to 10 kΩ 1%, R_{UV2} is calculated as follows:

$$R_{UV2} = [(V_{IN} - 1.25) \times R_{UV1}] / 1.25$$
$$R_{UV2} = [(9.0 - 1.25) \times 10000] / 1.25 = 62 \text{ k}\Omega$$

The closest 1% tolerance value is 61.9 kΩ.

Soft-Start Capacitor

The possibility of PWM dimming puts greater importance on the soft-start circuitry than in a standard voltage regulator. Dimming is done by enabling and disabling the converter, and to achieve the highest possible dimming ratio, the soft-start time should be as short as possible. A good starting value is 2.2 nF, and laboratory testing is recommended to determine if this value can be reduced without causing too great of an overshoot in the LED current upon startup.

Control Loop Compensation

The LM5022 uses peak current-mode PWM control to correct changes in output current due to transients. Peak current-mode provides inherent cycle-by-cycle current limiting, improved line transient response, and easier control loop compensation than voltage-mode control. Although there are no load transients, PWM dimming requires a fast control loop so that the output can turn on and off quickly.

The control loop is comprised of two parts. The first is the power stage, which consists of the pulse width modulator, output filter, current sense circuitry, and the LEDs. The second part is the error amplifier, which is an op-amp configured as an inverting amplifier.

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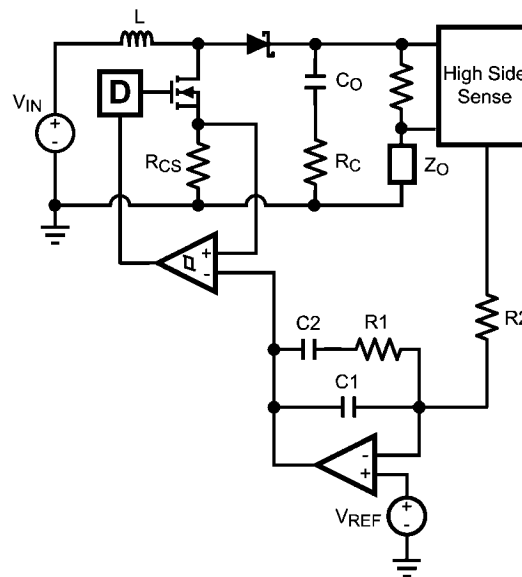
FIGURE 4. Power Stage and Error Amp

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to determine. Software tools such as Excel, MathCAD, and Matlab are useful for observing how changes in compensation or the power stage affect system gain and phase.

The power stage in a CCM peak current mode boost converter consists of the DC gain, A_{PS}, a load pole, f_P, the ESR zero, f_Z, a right-half plane zero, f_{RHP}, and a double pole resulting from the sampling of the peak inductor current. The

high-side current sense circuitry is treated as a DC gain and included in the expression for A_{PS}. The power stage transfer function (also called the control-to-output transfer function) can be written:

$$G_{PS} = A_{PS} \times \frac{\left(1 + \dfrac{s}{\omega_Z}\right)\left(1 - \dfrac{s}{\omega_{RHP}}\right)}{\left(1 + \dfrac{s}{\omega_P}\right)\left(1 + \dfrac{s}{Q_n \times \omega_n} + \dfrac{s^2}{\omega_n^2}\right)}$$

The DC gain term is:

$$A_{PS} = \frac{(1 - D) \times R_{SNS}}{G_i \times R_{CS} \left(1 + \dfrac{Z_O + R_{SNS}}{R_{OP}}\right)} \times A_{SNS}$$

The operating point resistance is:

$$R_{OP} = V_O / I_F$$

The current sense gain is:

$$A_{SNS} = R_{FB1} / R_{RFB2} = 6.25$$

The current sense gain is:

$$G_i = 3$$

The ESR zero is:

$$\omega_Z = \frac{1}{R_C \times C_O}$$

R_C for this example is 3 mΩ.

The load pole is:

$$\omega_P = \frac{\left(1 + \dfrac{Z_O + R_{SNS}}{R_{OP}}\right)}{(Z_O + R_{SNS} + R_C) \times C_O}$$

The right-half plane zero is:

$$\omega_{RHP} = \frac{R_{OP} \times \left(\dfrac{V_{IN}}{V_O}\right)^2}{L}$$

The sampling double pole quality factor is:

$$Q_n = \frac{1}{\pi \left[-D + 0.5 + (1 - D)\dfrac{S_e}{S_n}\right]}$$

The sampling corner frequency is:

$$\omega n = \pi \times f_{SW}$$

The inductor current slope is:

$$S_n = R_{CS} \times V_{IN} / L$$

The compensation ramp slope is:

$$S_e = 45\mu \times (2000 + R_{S1} + R_{S2}) \times f_{SW}$$

In the equation for A_{PS}, DC gain is highest when input voltage is at the maximum and output voltage at the minimum, therefore this worst-case analysis done for V_{IN} = 13.2V and V_O = 33.4V. DC gain is 9.2 dB. The load frequency pole $f_P = \omega_P$ / 2π is at 14 kHz (calculated with C_O = 3.5 μF), the ESR zero $f_Z = \omega_Z$ / 2π is at 22 MHz, and the right-half plane zero f_{RHP} = ω_{RHP} / 2π is at 38 kHz. The sampling double-pole occurs at one-half of the switching frequency. Proper selection of slope compensation (via R_{S2}) is most evident in the sampling double pole. A well-selected R_{S2} value eliminates peaking in the gain and reduces the rate of change of the phase lag. Gain

and phase plots for the power stage are shown in *Figure 5* and *Figure 6*.
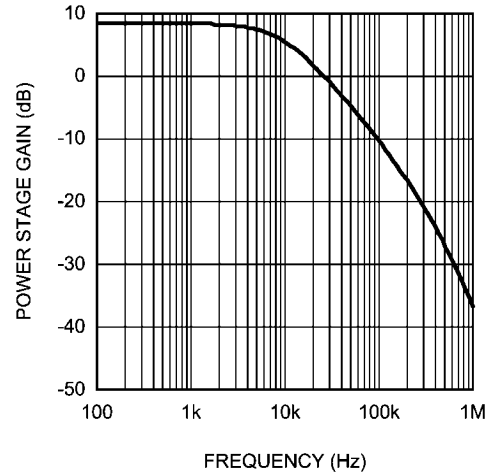
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FIGURE 5. Power Stage Gain
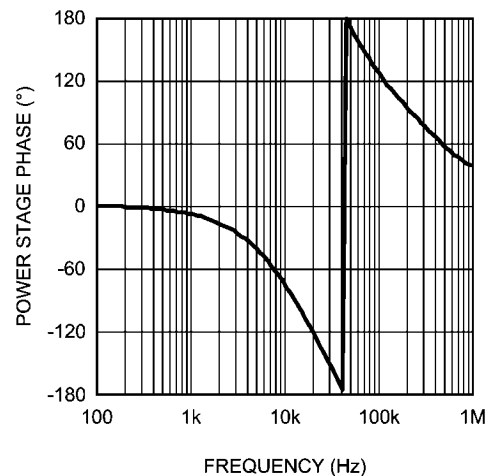
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FIGURE 6. Power Stage Phase

The load pole causes a roll-off in the gain of -20 dB/decade at lower frequencies. The combination of the RHP zero and sampling double pole maintain the slope out to beyond the switching frequency. The phase tends towards -90° at lower frequency but then increases to -180° and beyond from the RHP zero and the sampling double pole. The effect of the ESR zero is not seen because its frequency is several decades above the switching frequency. The combination of increasing gain and decreasing phase makes converters with RHP zeroes difficult to compensate. Setting the overall control loop bandwidth to 1/3 to 1/10 of the RHP zero frequency minimizes these negative effects, but requires a compromise in the control loop bandwidth.

Compensation is done with the error amplifier, and provides high DC gain (for output accuracy) and high phase margin (for control loop stability). The transfer function of the compensation block, G_{EA}, can be derived by treating the error amplifier as an inverting op-amp with input impedance Z_I and feedback impedance Z_F. The majority of applications will require a Type II, or two-pole one-zero amplifier, shown in *Figure 4*. The

LaPlace domain transfer function for this Type II network is given by the following:

$$G_{EA} = \frac{Z_F}{Z_I} = \frac{1}{R2\,(C1 + C2)} \times \frac{s \times R1 \times C1 + 1}{s\left(\dfrac{s \times R1 \times C1 \times C2}{C1 + C2} + 1\right)}$$

Control loop compensation is often set by fixing the mid-band gain of the error amplifier transfer function first and then positioning the compensation zero and pole. A stable control loop should have at least 45° of phase margin and 8 dB of gain margin.

1. **Fix the compensation zero frequency, f_{Z1}**: The suggested placement for this zero is at the load pole of the power stage, $f_P = \omega_P / 2\pi$. For this example, $f_{Z1} = f_P = 14$ kHz

2. **Fix the compensation pole frequency, f_{P1}**: The suggested placement for this pole is at half of the switching frequency, $f_{P1} = 150$ kHz

3. **Determine the desired control loop bandwidth, f_{0dB}**: For this example, f_{0dB} is set at approximately ¼ of the RHP zero frequency, 10 kHz

4. **Determine the gain of the power stage at f_{0dB}**: This value, A, can be read graphically from the gain plot of G_{PS} or calculated by replacing the 's' terms in G_{PS} with $2\pi f_{0dB}$. For this example the gain at 10 kHz is approximately 7.5 dB.

5. **Calculate the negative of A, subtract 3 dB and convert it to a linear gain**: Subtracting 3 dB accounts for the difference between the error amplifier gain at f_{Z1} and the actual mid-band gain. For this example, -7.5 -3 = -10.5 dB = 0.3V/V

6. Select the resistance of R2: This value is arbitrary, however selecting a resistance between 10 kΩ and 100 kΩ will lead to practical values of R1, C1 and C2. For this example, R2 = 20 kΩ 1%.

7. **Set R1 = A x R2**: For this example: R1 = 0.3 x 20000 = 6 kΩ

8. **Set C2 = 1 / (2π x R1 x f_{Z1})**: For this example, C2 = 1.81 nF

9. **Set:**

$$C1 = \frac{C2}{2\pi \times C2 \times R1 \times f_{P1} - 1}$$

For this example, C1 = 196 pF

10. **Substitute the closest 1% resistor values for R1 and R2, and the closest 10% capacitor values for C1 and C2**: For this example:

R1 = 20 kΩ 1%, R2 = 6.04 kΩ 1%, C1 = 180 pF 10%, C2 = 1.8 nF 10%

11. **Use the values of C1, C2, R1 and R2 to model the error amp**: The open-loop gain and bandwidth of the LM5022's internal error amplifier are 75 dB and 4 MHz, respectively. Their effect on G_{EA} can be modeled using the following expression:

$$OPG = \frac{2\pi \times GBW}{s + \dfrac{2\pi \times GBW}{A_{DC}}}$$

The error amplifier transfer function is:

$$R_{FB2} = \frac{I_F \times R_{SNS} \times R_{FB1}}{1.25}$$

A_{DC} is a linear gain, and the linear equivalent of 75 dB is approximately 5600V/V.

12. **Plot or evaluate the complete control loop transfer function**: The complete control loop transfer function is obtained by multiplying the power stage and error amplifier transfer functions together. The bandwidth and phase margin can then be read graphically or evaluated numerically.
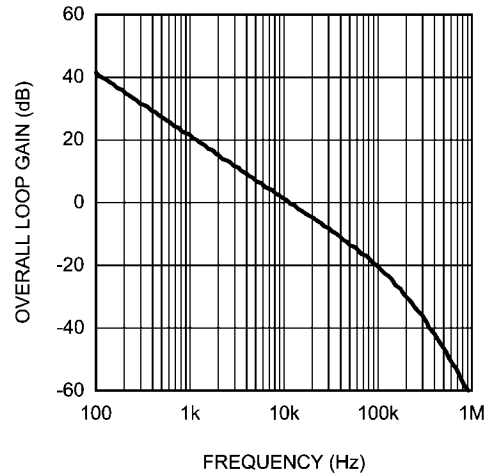
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FIGURE 7. Total Loop Gain
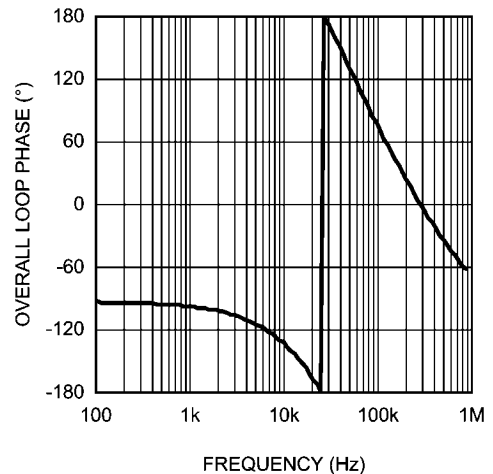
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FIGURE 8. Total Loop Phase

13. **Evaluate the bandwidth, phase margin, and gain margin**: For this example the bandwidth is 12.6 kHz, the phase margin is 48°, and the gain margin is 8.3 dB. All the conditions for stability have been met.

Control Loop Measurement

Control loop measurements like those shown in Figures 5-8 are taken using a network analyzer that requires a point to inject an AC signal. A small resistor, typically 20Ω to 50Ω, is placed in series with the control loop, and the AC source is injected across it. The injection node must be low impedance at one side and high impedance at the other to prevent measurement error. In voltage regulators the most common point is between the regulator output (low impedance) and the top feedback divider resistor (high impedance). For the LM5022 boost LED driver, however, the injection node should be between resistor R2 and the output of the PNP current mirror (shown as the 'High Side Sense' block in *Figure 4*). R2 provides the high impedance on one side, but the PNP current mirror has a high impedance as well. One solution to this problem is shown in *Figure 9*. A high-bandwidth op-amp can be used as a buffer. This technique should also be used in circuit simulators.

To measure the complete control loop, the network analyzer inputs A and R should be placed at the AC signal injection points, as shown in *Figure 9*. To measure the power stage only, input R should be moved to the COMP pin. The error amplifier can be measured by moving input A to the comp pin.
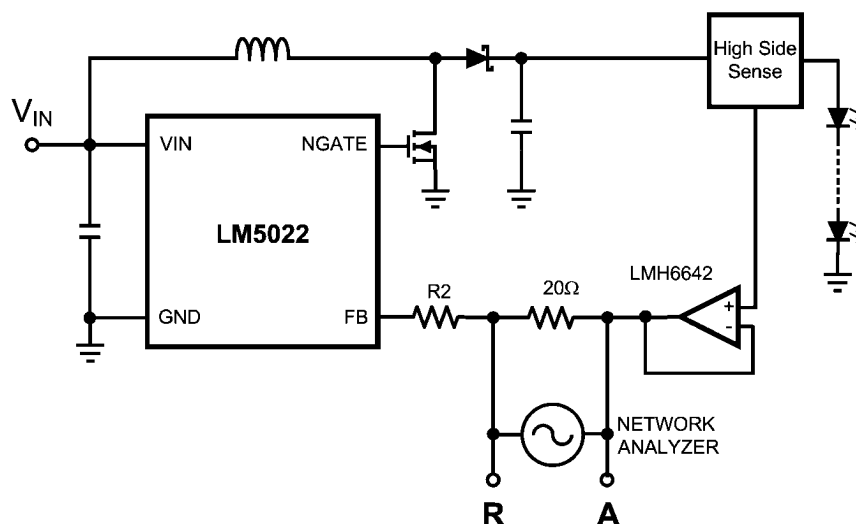
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FIGURE 9. Network Analyzer with Op-Amp Buffer

Bill of Materials

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM5022	Low-Side Controller	MSOP-10		1	NSC
Q1	Si4850EY	N-MOSFET	SO-8	60V, 31 mΩ, 27nC	1	Vishay
Q2	DMMT5401	Dual PNP	SOT-26	150V, 300 mW	1	Diodes, Inc
Q3	TN0200K	N-MOSFET	SOT-23	20V, 0.7A	1	Vishay
D1	CMSH2-60	Schottky Diode	SMB	60V, 2A	1	Central Semi
D2	CMDZ47L	Zener	SOD-323	47V, 50 μA	1	Central Semi
L1	PF0552.223NL	Inductor	12.5 x12.5 x 6.0mm	22 μH, 4.8A, 35 mΩ	1	Pulse
Cin1 Cin2	C3225X7R1E685M	Capacitor	1210	6.8 μF, 25V	2	TDK
Co	C4532X7R1H475M	Capacitor	1812	4.7 μF, 50V, 3 mΩ	1	TDK
Cf	C3216X7R1E105K	Capacitor	1206	1 μF, 25V	1	TDK
Cinx Cox	C2012X7R2A104M	Capacitor	0805	100 nF, 100V	2	TDK
C1	VJ0805Y181KXXAT	Capacitor	0805	180 pF 10%	1	Vishay
C2	VJ0805Y182KXXAT	Capacitor	0805	1.8 nF 10%	1	Vishay
Css	VJ0805Y222KXXAT	Capacitor	0805	2.2 nF 10%	1	Vishay
Ccs	VJ0805Y102KXXAT	Capacitor	0805	1 nF 10%	1	Vishay
Csyc	VJ0805A101KXXAT	Capacitor	0805	100 pF 10%	1	Vishay
R1	CRCW08056041F	Resistor	0805	6.04 kΩ 1%	1	Vishay
R2	CRCW08052002F	Resistor	0805	20 kΩ 1%	1	Vishay
Rb	CRCW08053242F	Resistor	0805	32.4 kΩ 1%	1	Vishay
Rfb1	CRCW08051241F	Resistor	0805	1.24 kΩ 1%	1	Vishay
Rfb2	CRCW08052000F	Resistor	0805	200Ω 1%	1	Vishay
Ruv1 Rpd	CRCW08051002F	Resistor	0805	10 kΩ 1%	2	Vishay
Rg,Rz	CRCW08050RJ	Resistor	0805	0Ω	2	Vishay
Rs1	CRCW0805101J	Resistor	0805	100Ω 5%	1	Vishay
Rs2	CRCW08056341F	Resistor	0805	6.34 kΩ 1%	1	Vishay
Rcs	ERJL14KF50M	Resistor	1210	50 mΩ, 0.5W 1%	1	Panasonic
Rsns	ERJ8BQFR20V	Resistor	1206	0.2Ω, 1%, 0.33W	1	Panasonic
Rt	CRCW08055622F	Resistor	0805	56.2 kΩ 1%	1	Vishay
Ruv2	CRCW08056192F	Resistor	0805	61.9 kΩ 1%	1	Vishay

Notes

Notes

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Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
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