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SSL2101 dimmable mains LED driver

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Application note

Document information

Info	Content
Keywords	LED, LED driver, mains, dimming, dimmable, LED lighting, LED lamp, SMPS, SSL2101, power conversion, flyback, power factor
Abstract	This document describes how to design a mains dimmable LED driver using the NXP SSL2101 LED Driver IC in flyback mode. It includes a description of how mains dimmer compatibility is achieved

Revision history

Rev	Date	Description
01	2009/01/30	First release

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1. Introduction

Light Emitting Diodes (LEDs) have been used in electronic systems for many years, primarily as indicator lights on electronic devices. Recent advances in terms of brightness and available colors mean that LEDs can now be used in a wide range of applications - from fun lighting in cell phones and media players to replacing conventional light sources in commercial and domestic lighting applications.

Key enablers driving the expansion of LED lighting are the availability of high brightness LEDs and intelligent LED controllers. Product designers incorporating high brightness LEDs face many challenges. Among them are thermal management, driver scheme/topology and existing infrastructure.

To replace an existing dimmable incandescent or halogen light source, an electronic lamp driver system must be implemented that can operate with the existing dimmer switch while replicating the dimming behavior of the existing light source. The NXP SSL2101 IC provides this functionality and, in addition, is an efficient power converter. It is the first IC to combine these capabilities, enabling the lamp/module designer to integrate electronics in a cost- and size-effective way, whilst benefitting from optimal thermal trade-off.

2. LED properties

LEDs need a completely different type of driver to the kind used with incandescent or halogen lamps. While incandescent lamps act as resistive loads with self stabilizing properties, LEDs require a current source. The amount of light generated by an LED is approximately proportional to the current flowing through the device. The voltage drop across the device increases with current but decreases with temperature. In this respect, LEDs behave like diodes. However, the voltage drop during operation (the forward voltage or V_F) is greater. This voltage drop is related to the amount of energy (eV) generated when an electron is converted into a photon, and the amount of energy generated is directly related to the color of the light. Additionally, V_f can vary greatly between batches due to production spread.

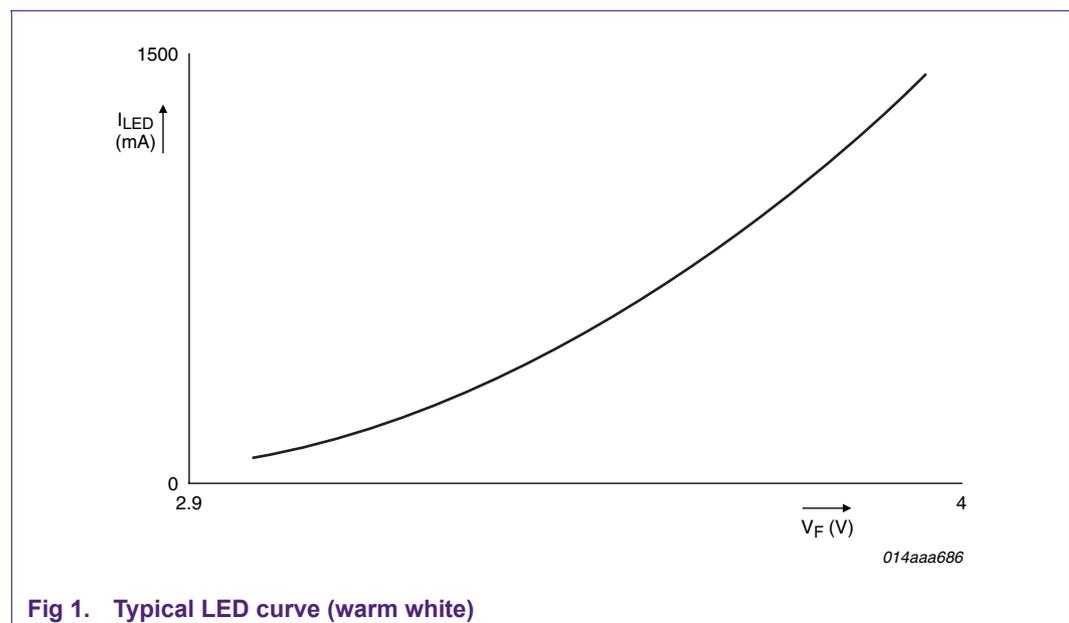


Fig 1. Typical LED curve (warm white)

2.1 Serial/parallel configuration

In most applications where LEDs replace existing lamps, multiple units need to be connected to the driver since a single LED would not generate enough light. The LEDs can be connected in series or in parallel.

If the LEDs are connected in series, the total voltage across the LED chain will be equal to the sum of the forward voltages (the current will be the same in all the LEDs).

If LEDs are connected in parallel, the current is distributed among the branches. However, because the forward voltage of an LED tends to fall as the temperature rises, this configuration is intrinsically unstable. As the temperature rises, more and more of the current generated will flow through the branches with the lower forward voltages - which will become brighter as the branches with the higher forward voltages get darker.

One reason for persisting with the parallel configuration (or a series-parallel combination), however, is that it allows a large number of LEDs to be combined at a safe supply voltage - an unacceptably high voltage might be needed to achieve the same degree of brightness with a series configuration.

The parallel configuration also offers the advantage of redundancy. If a single LED or connection in a series-connected LED chain fails, resulting in an open circuit, the light will go out in all the LEDs in the chain. This would not happen if the LEDs were connected in parallel. With a parallel configuration, it is recommended that current regulation be added at each branch to prevent thermal runaway and the unequal distribution of current and light. In general, power converters operate at optimal efficiency when the difference between output and input voltages is minimized. With mains powered drivers and LEDs, optimizing this aspect will generate higher output voltages, allowing more LEDs to be connected in series.

3. Flyback converter basics

In many applications, isolation from the mains is necessary for safety reasons. The flyback converter provides this isolation. It is also less expensive and simpler to implement than a push-pull or a forward converter, since it only requires a single inductive element and a switch.

[Figure 1](#) is a simplified application diagram of an isolated flyback converter connected to a supply and a load. The polarities of some relevant voltages and currents are included in this diagram. To help understand the application, V_I and V_O should be considered to be DC like. In a practical application, a MOSFET or bipolar transistor would replace switch S1 while a diode would replace S2.

The state of the switches determines the operation of the circuit. Two switches allow for four possible operating states (see [Table 1](#)). States 1 and 2 are the alternating primary and secondary conduction states. In State 3, there is no primary or secondary conduction. State 4, when both switches are closed, must be avoided.

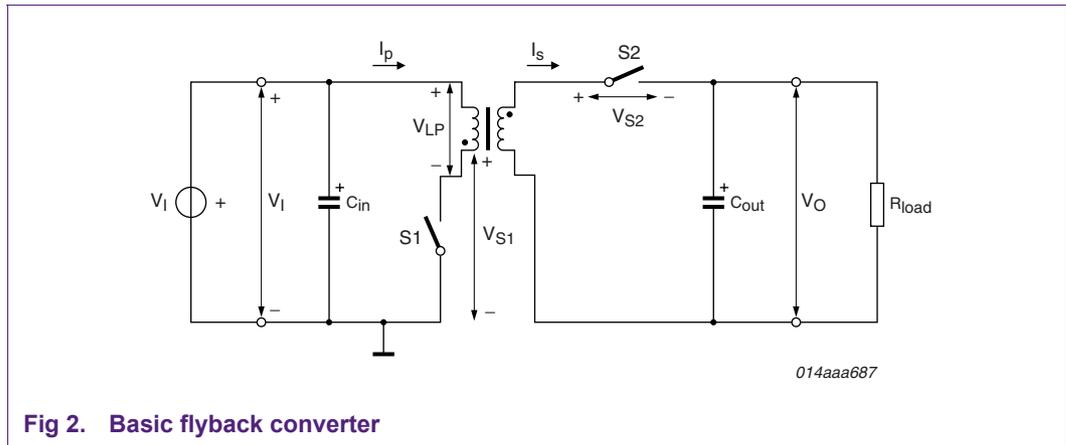


Fig 2. Basic flyback converter

Table 1. Flyback converter operating modes

State	S1	S2	Duration
1	closed	open	$\delta 1T$
2	open	closed	$\delta 2T$
3	open	open	$\delta 3T$
4	closed	closed	NA

Initially, switch S1 is closed (for $\delta 1T$) and a current starts to flow in the primary winding of the transformer (State 1), rising linearly. Then S1 is opened and S2 is closed (for $\delta 2T$) and the energy stored in the secondary winding of the transformer causes a current to flow in the load (State 2), which falls linearly as the energy is dissipated. The peak value of the load current is equal to the transformer primary-to-secondary turns ratio ($n = N_p/N_s$) multiplied by the primary peak current at the instant S1 is opened. While S2 is conducting, the output voltage is reflected in the primary side of the transformer. State 3 occurs when the secondary current falls to zero while S1 remains open (for $\delta 3T$). Primary and secondary currents are both zero.

This mode of operation, where the primary conducts for $\delta 1T$ (the primary stroke), the secondary conducts for $\delta 2T$ (the secondary stroke), then conduction is halted for $\delta 3T$ is called Discontinuous Conduction Mode (DCM). If a new cycle begins as soon as the secondary current falls to zero ($\delta 3T = 0$), the converter is operating in Boundary Conduction Mode (BCM).

Figure 3 shows the equivalent circuit diagrams for the three valid states when a converter is operating in DCM mode. Simplified waveforms for one complete switching cycle are also shown.

More detailed discussions of the operation of flyback converters can be found in electronic engineering reference books.

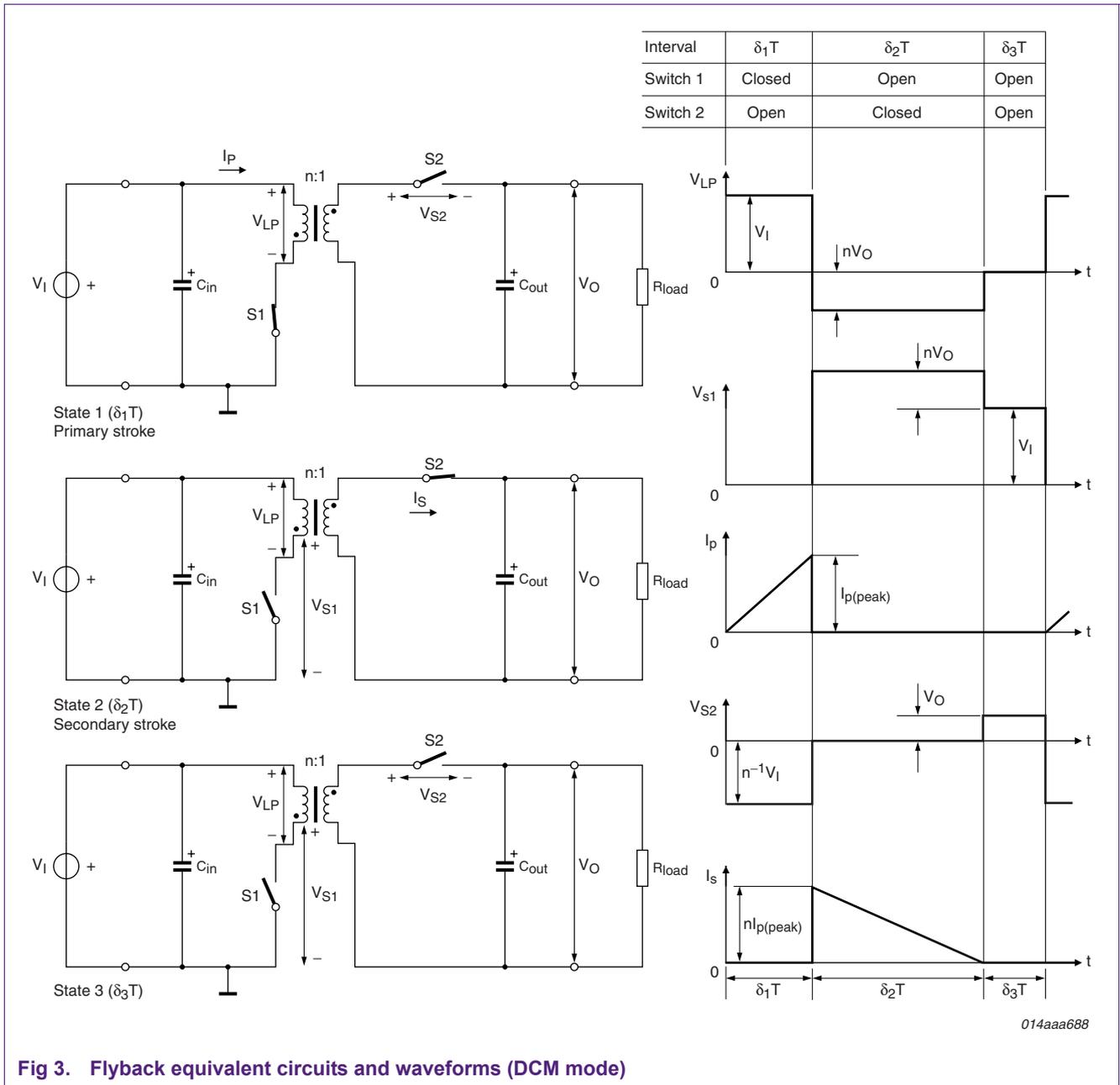


Fig 3. Flyback equivalent circuits and waveforms (DCM mode)

4. Mains dimming

Standard industrial and household dimmers were designed to be used with incandescent lamps. Some of the more advanced types can be used with transformers connected to halogen lamps. LED-specific mains dimmers are still rare.

The cost of buying and installing a new dedicated dimmer can easily surpass that of the light source itself. So an LED system that will work with the existing dimming infrastructure, such as that based around the NXP SSL2101, will open up this market segment.

Because existing dimmers were designed to be used with incandescent lamps (which approximate resistive loads dissipating between 20 W and 50 W), some additional circuitry will be needed to allow them to be used in an LED system. There is no standard for incandescent dimmers which, in practice, leads to a large spread in performance and parameter values.

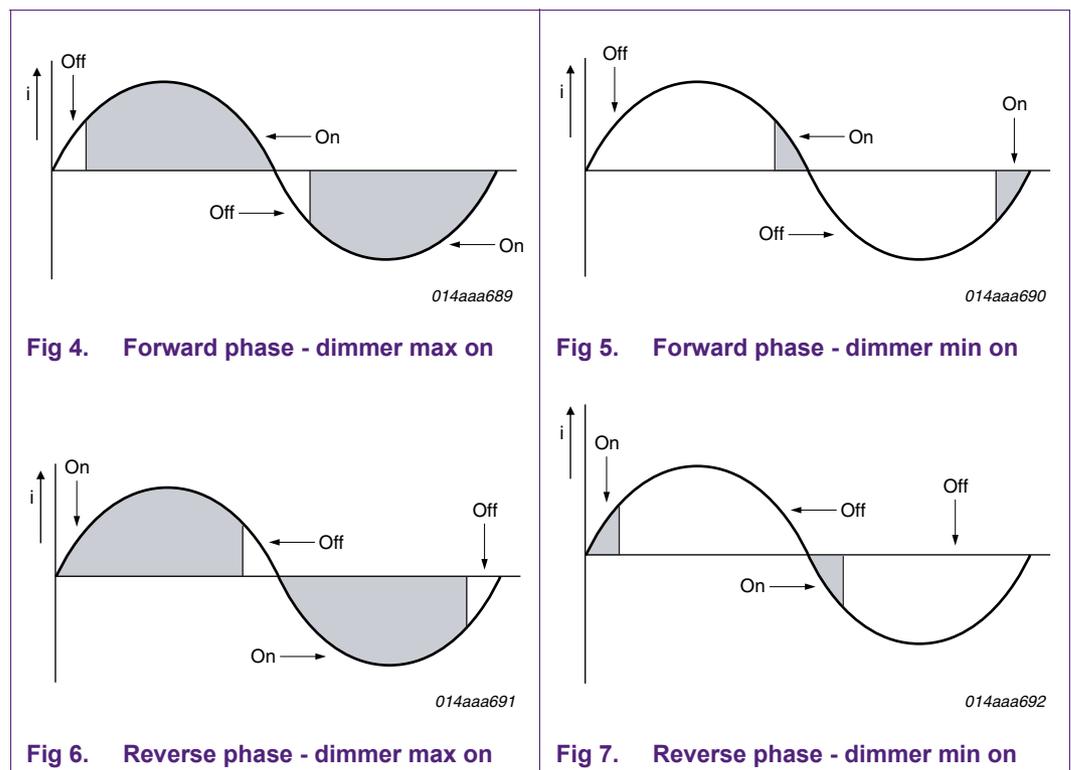
4.1 Dimmer switch classification

Dimmer switches work by turning off power to the lighting circuit during part of the supply cycle. By rapidly (twice for each cycle of the supply voltage, or 100/120 times per second) turning the light circuit on and off, the total energy delivered to the lighting element is reduced. The longer the power is off during each cycle, the dimmer the light will be. The thermal persistence of the filament smooths out the pulses, ensuring flickering due to the rapid switching is imperceptible.

Dimmers can be divided into two operational categories: positive angle/forward phase operation, also known leading edge dimming, and negative angle/reverse phase operation, or trailing edge dimming.

Forward phase dimmers work by varying the switch ON point of the supply current to a lighting circuit. They detect the start (zero-crossing point) of each half-cycle of the supply voltage, then wait for a predetermined period before switching on the current.

Reverse phase dimmers vary the switch OFF point, cutting off the supply current to the lighting circuit at predetermined intervals.



Two switching methodologies can be distinguished: triac dimming and transistor dimming. Triac switching is always used with forward phase dimmers. Transistor switching can be used with forward and reverse phase dimmers. Transistor dimmers have the advantage of being able to switch capacitive loads, but most existing dimmers are still triac based.

4.2 Triac dimmer

A triac is a bidirectional gated switching device with distinct latching properties. A number of conditions must be met to ensure reliable latching and to maintain current flow once the device has been latched:

- When the triac is triggered, the voltage across the device must be sufficient to enable the minimum latch current to flow. I_{latch} is the minimum current needed to hold the component in the conducting state after the trigger (or gate) current has been removed. I_{latch} must flow for long enough (the firing time) to completely latch the device.
- Once the device has been latched, a continuous current must flow through the device in one direction. This is the hold current, I_{hold} . If the polarity of I_{hold} changes (i.e. at a zero cross point), the triac will switch off.
- A triac is not a fully symmetrical device - the values of the above parameters depend on the direction of current flow and on temperature. A timing circuit inside the dimmer, usually consisting of a resistor/capacitor combination, must be reset at zero crossing (the capacitor must be fully discharged).

If the above conditions for stable dimmer operation are not met, problems may arise that can lead to unstable operation. LED systems without oversized buffering are unforgiving, because they respond a lot faster to changes in power dissipation than incandescent lamps. Even small variations in light output in the response frequency of the human eye (200 Hz to 120 Hz) can cause flickering and be disturbing. So the switching frequency should not be allowed to fall below 200 Hz. It should be noted that the human eye is more susceptible to variations in color than brightness.

4.3 Transistor dimmer

A transistor dimmer uses a rectifier bridge in combination with a switching device like a MOSFET or bipolar transistor to switch the main current. It contains additional circuitry to drive these devices, and this circuitry needs to be powered. The power is tapped from the switch while it is open, and stored in a capacitor. Though the energy dissipated in the dimmer electronics is not substantial, the current drawn over the switch can be a lot greater than the current required for a passive timing circuit.

5. Functional description

The SSL2101 is a Multi-Chip Module (MCM) in an SO16 package. It contains an efficient power converter and internal circuitry to achieve mains dimmer compatibility. It enjoys following advantages over existing solutions:

- Integrated power switch. This reduces component costs and also ensures optimal drive and switch protection.
- Valley detection. This feature reduces converter losses, because the switch is closed at the optimal time.

- Integrated bleeder switches and comparator. This reduces component count and size.
- Smart bleeder operation. The IC senses when bleeder action is not required (e.g. the LED chain provides sufficient load). This reduces power dissipation and increases system efficiency.
- Enhanced thermal lead frame. This can increase the lifetime of the IC and enable it to operate at higher ambient temperatures. For retrofit solutions, the lifetime of electronics at elevated temperatures can be a critical parameter.
- Dimming by duty factor control and by converter frequency. This allows the designer more freedom to define parameter values. More accurate control of low dim levels can be achieved, and audible transformer noise eliminated, by adjusting the parameters controlling both dimming systems.
- Logarithmic dimming correction. This enables the dimming behavior of the LEDs replicate that of an incandescent or halogen lamp.
- Built-in thermal protection, overcurrent protection, short-winding detection and maximum duty factor limiting. These features ensure the reliable operation of the IC with minimum failures, even when operating outside specifications.

Further details and full specifications can be found in the SSL2101 data sheet ([Ref. 1](#)).

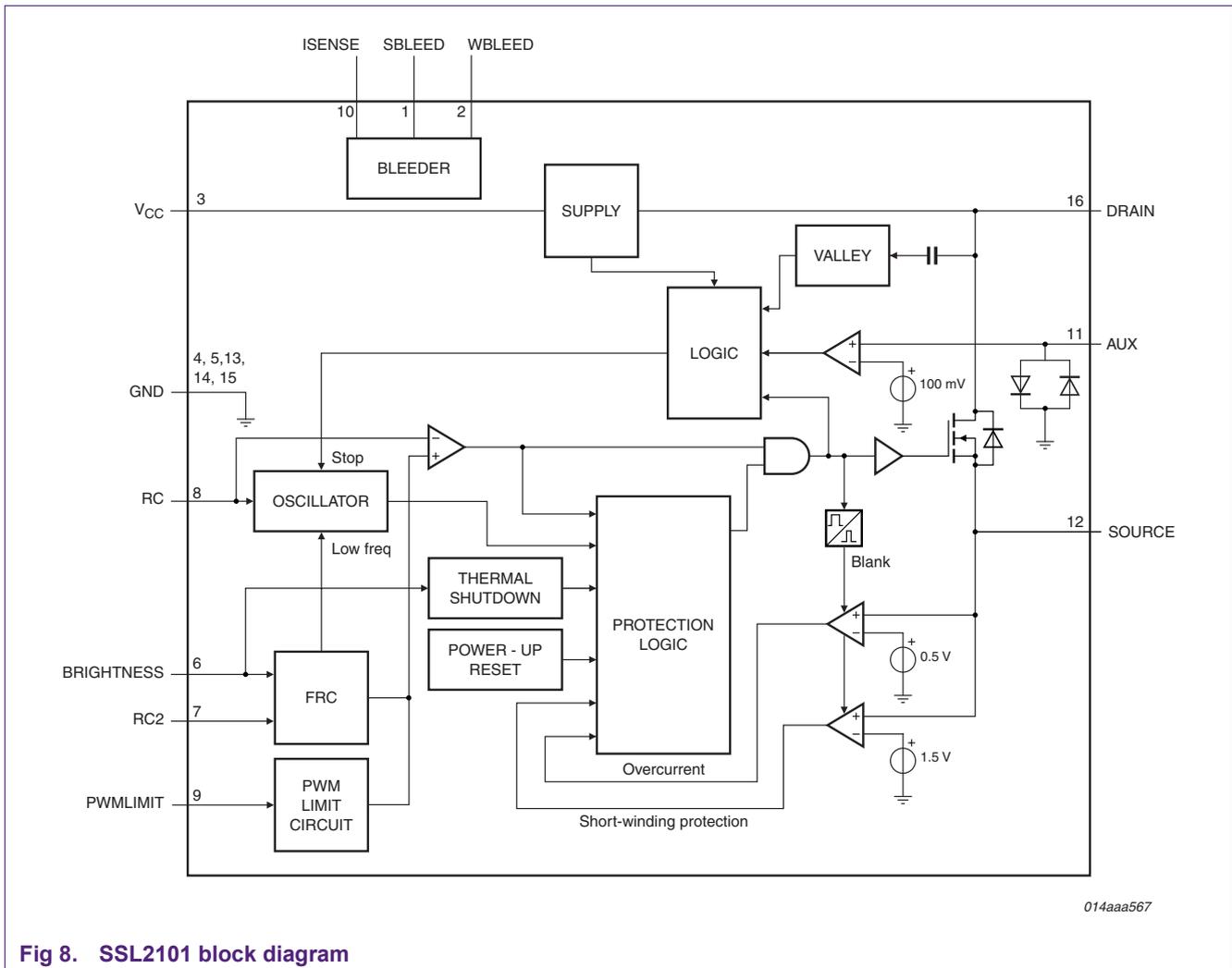


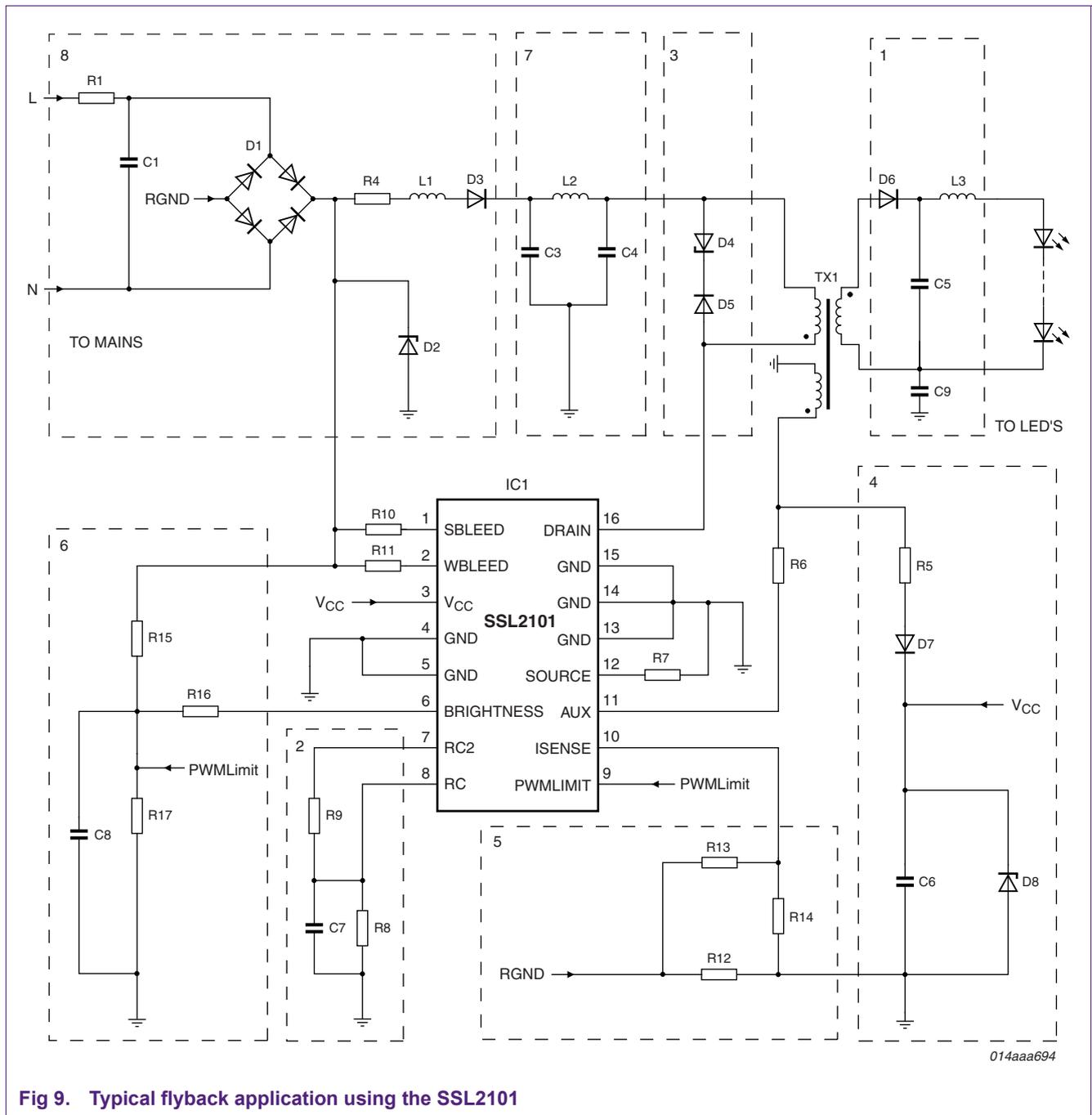
Fig 8. SSL2101 block diagram

6. Step-by-step design procedure

This sections provides a step-by-step guide to designing a basic flyback converter application incorporating the SSL2101. It should be noted that the derivation of the formulas applied is beyond the scope of this application note. Where values used in formulas are application specific, reasonable estimates have been made. Recommended component values were arrived at through extensive testing with a range of commercially available dimmers.

6.1 Basic configuration

A circuit for a typical flyback application driving a single LED chain is shown in [Figure 9](#):



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Fig 9. Typical flyback application using the SSL2101

The mains voltage is rectified, buffered and filtered in the input section and connected to the primary winding of the transformer. The following functional blocks can be identified in the SSL2101 application (refer to [Figure 9](#)):

1. Output circuit
2. Oscillator
3. Snubber
4. V_{CC} generation
5. Bleeder settings

6. Dimming detection
7. Mains buffer
8. Input circuit

In the output section, the transferred energy is stored in a capacitor (C5) and filtered (L3) before driving the LED chain. A clamp is added across the primary winding of the transformer to prevent a high voltage overshoot on the DRAIN pin of the SSL2101, at the moment the internal power MOS transistor is switched off. A dimming detection circuit divides and filters the mains rectified voltage to provide input for the generation of the dimming curve.

6.2 Output circuit

The values of components in the output circuit will depend on the number of LEDs in the chain, and on the voltage across and current through the chain. The current will have a ripple and the size of this ripple will dictate the size of the buffer capacitor (C5). The size for the buffer capacitor can be calculated from the following equation:

$$C5 = \frac{I_{led}}{\Delta I} \times \frac{I}{f_{conv(nom)} \times R} \quad (1)$$

where:

- I_{led} = LED current
- ΔI = change in LED current
- $f_{conv(nom)}$ = nominal converter frequency
- R = series resistance of LED chain.

In the example design ([Figure 9](#)):

We've assumed 10 LEDs in series at 350 mA with a forward voltage, V_f , of 3.5 V, allowed current ripple of 10 % and a nominal converter working frequency of 100 kHz.

The voltage across the LED chain will be $10 \times 3.5 \text{ V} = 35 \text{ V}$. Assuming the data sheet provided by the LED manufacturer specifies a differential resistance of 0.5Ω at 350 mA per LED, the resistance of the LED chain will be $10 \times 0.5 \Omega = 5 \Omega$.

This will give us a buffer capacitor size of $C5 = 10 \times I / (100000 \times 5) = 20 \mu\text{F}$.

When using an electrolytic capacitor for C5, it is recommended that a low ESR foil or ceramic capacitor be connected in parallel to improve EMC filtering and reduce dissipation. This capacitor should be mounted closer to D6 than the electrolytic capacitor, C5.

The output coil (L3) filters the high frequency signals from the converter. The size of this coil depends of the EMC norm to be applied on the final product and on the construction, grounding and screening. As a guideline, the cut-off frequency of the LR filter (consisting of the inductance of L3 and the resistance of the LED chain) can be chosen to be 1/20th of the converter frequency. The coil value can be calculated using the following equation:

$$L3 = \frac{20 \times R}{2\pi \times f_{conv(nom)}} \quad (2)$$

In the example:

This will give us an output coil value of $L3 = 20 \times 5 / (2\pi \times 100000) = 160 \mu H$.

Diode D6 must meet the following selection criteria:

1. Be able to withstand the peak current
2. Be able to withstand the maximum reverse voltage
3. Have a low voltage drop in forward mode
4. Have a low capacitance value in reverse mode

The peak diode current through D6 is determined by the secondary stroke time ($\delta 2T$) and the LED current. In the example, $\delta 2T$ lasts for 82 % of T (the period of the applied voltage; see [Section 7.4](#)). During $\delta 2T$, the diode current will have a declining sawtooth waveform with an average value of half the peak current. So half the diode peak current will be flowing in the LED chain for 82 % of T , or $I_{led} = (I_{D(peak)} / 2) \times 0.82 = I_{D(peak)} \times 0.41$. The peak diode current will be around 2.4 times the LED current. The average diode current will be 1.2 times the LED current.

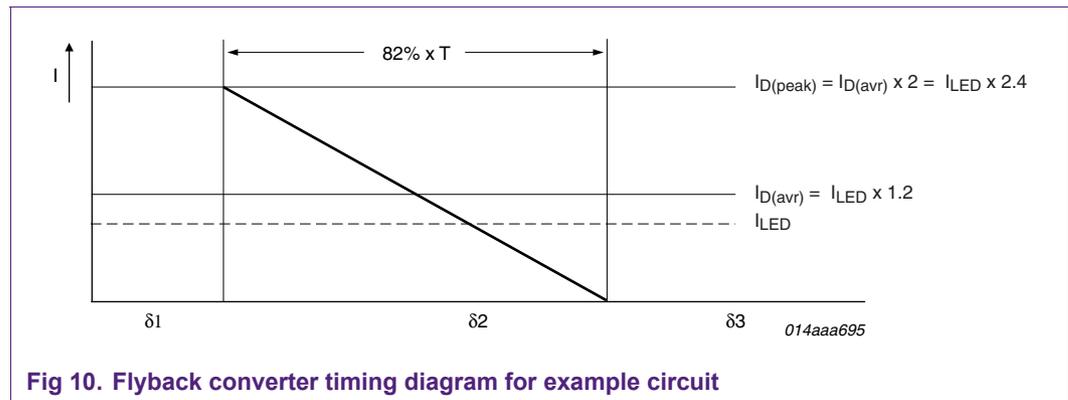


Fig 10. Flyback converter timing diagram for example circuit

The peak reverse voltage across D6 is determined by the primary-to-secondary turns ratio of the transformer and the maximum buffer voltage (the voltage across C3 and C4 in the mains buffer; see [Figure 9](#)). Some margin must be applied here to allow for oscillation effects.

$$V_{rev(peak)} = V_{buff(max)} / n + V_{osc} \tag{3}$$

where:

- $V_{rev(peak)}$ = peak reverse current across diode
- $V_{buff(max)}$ = maximum voltage across capacitors in buffer circuit
- n = transformer primary-to-secondary turns ratio
- V_{osc} = margin applied for oscillation effects.

D6 can be a Schottky diode with a V_f of between 0.15 V and 0.4 V or a silicium diode with a V_f of around 0.7 V. Note, however that Schottky diodes have a relatively low maximum reverse voltage. A suitable Schottky diode may not be available for a given application. One of the main parameters determining reverse capacitance is junction size, which is in

turn related to maximum current - oversizing D6 will result in unnecessary losses.

In the example:

$$n = 1.2 \text{ (see Section 7.4)}$$

$$V_{\text{buff(max)}} = 384 \text{ V (note that D2 is a 400 V Schottky diode; see Section 6.6)}$$

$$V_{\text{osc}} = 20 \text{ V (margin allowed for oscillation effects).}$$

The average diode current will be 1.2 times the LED current so:

$$I_{D6(\text{avr})} = 0.35 \text{ A} \times 1.2 = 0.42 \text{ A and}$$

$$I_{D6(\text{peak})} > 0.84 \text{ A and}$$

$$V_{\text{rev(peak)}} = 384 / 1.2 + 20 = 340 \text{ V.}$$

C9 is connected between ground and the secondary circuit to counter capacitive coupling between primary, auxiliary and secondary windings. To have an impact, the value of this capacitor should be much greater than the value of the capacitive coupling. As a rule of thumb, a factor of 20 is recommended. So if $C_{\text{coup}} = 100 \text{ pF}$, C9 should be $> 2 \text{ nF}$. In the example, C9 is 2.2 nF.

If safety isolation is needed, this capacitor should be able to withstand the applied voltages, as specified EN132400 (type Yn).

6.3 Oscillator components

The maximum converter frequency and the maximum oscillator frequency are determined by the primary inductance and the transformer input power (see Section 7). The transformer input power is the sum of the power dissipated in the output circuit, in the auxiliary circuit and the transformer losses. The primary inductance can be calculated using the following equation:

$$L_p = \frac{2 \times P_{\text{in(trans)}}}{I_{p(\text{peak})}^2 \times f_{\text{conv(nom)}}} \tag{4}$$

where:

L_p = inductance of transformer primary winding

$I_{p(\text{peak})}$ = primary peak current

$P_{\text{in(trans)}}$ = power dissipated in the output and auxiliary circuits, plus transformer losses

$f_{\text{conv(nom)}}$ = nominal converter frequency.

In the example, with the voltage across the LED chain = 35 V, $V_{D6} = 0.7 \text{ V}$ and V_{L3} estimated at 1 V:

$$P_{\text{out}} = (35 + 0.7 + 1) \times 0.35 = 12.5 \text{ W}$$

$$P_{\text{aux}} = 0.5 \text{ W (estimated)}$$

$$P_{\text{trans}} = 1 \text{ W (estimated)}$$

therefore:

$$P_{in(trans)} = 14 \text{ W}$$

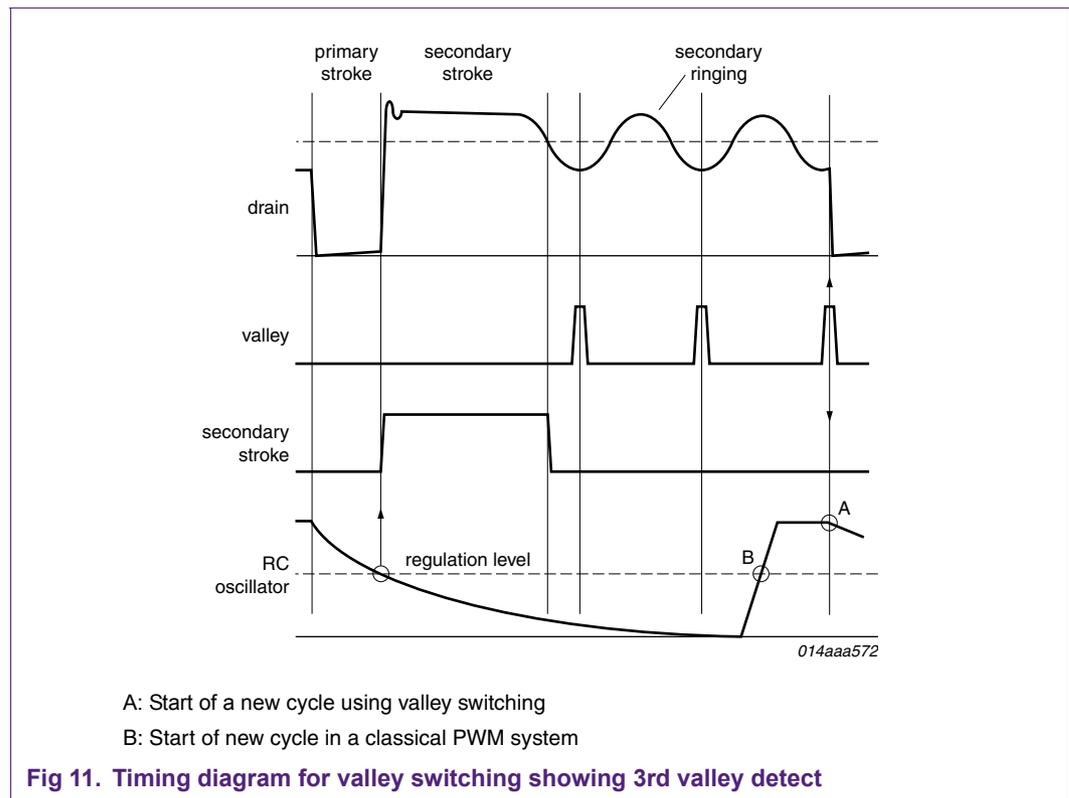
$$f_{conv(nom)} = 100 \text{ kHz}$$

$$I_{p(peak)} = 0.821 \text{ A (see Section 7.1).}$$

from Equation 4,

$$L_p = (2 \times 14) / 0.821^2 \times 100000 = 415 \mu\text{H}$$

After the secondary stroke, the drain voltage oscillates at a ringing frequency, f_{ring} . The oscillator waits until it has detected a low drain voltage (a valley) before initiating a new primary stroke. For maximum efficiency, the oscillator frequency is selected to guarantee first valley detect (the first valley occurs after 1/4 of the period of f_{ring}). The oscillator frequency can then be lowered using the brightness input for dimming. As the oscillator frequency is lowered, valley detection will be triggered at the second, third, fourth valleys, and so on - gradually increasing the off time ($\delta 3T$).



As can be seen from Equation 4, there is a trade-off between primary peak current, converter frequency and primary inductance. The primary peak current helps determine switching losses, as does the switching frequency. The ratio of the primary inductance to peak current determines the core size. Common frequencies are 50 kHz (in EMC-susceptible environments) and 100 kHz.

The ringing frequency at first valley detect is determined by the formula:

$$f_{ring} = \frac{1}{2 \times \pi \times \sqrt{L_p \times C_p}} \tag{5}$$

where:

L_p = inductance of primary winding

C_p = parasitic capacitance on drain node.

Note that the total primary capacitance is not only determined by the primary inductor but also by the switch, the snubber diode, and the capacitance of the rectifier diode divided by the primary-to-secondary turns ratio:

$$C_p = C_{lp} + C_{sw} + C_{D5} + \frac{1}{n} \times C_{D6} \tag{6}$$

where:

C_{lp} = capacitance of primary coil

C_{sw} = capacitance of the internal (MOSFET) switch

C_{D5} = capacitance of the snubber diode

C_{D6} = capacitance of the rectifier diode.

The time between transformer demagnetization and the first valley of f_{ring} is one quarter of the period of the ringing frequency.

In the example:

$$L_p = 415 \mu H$$

$$C_p = 20 + 70 + 10 + 1/1.2 \times 20 = 117 \text{ pF (estimated)}$$

from [Equation 5](#):

$$f_{ring} = 722 \text{ kHz}$$

so the first valley occurs $\Delta T = \frac{1}{4 \times f_{ring}} = 0.3 \mu s$ after the second stroke has ended.

A nominal converter frequency of 100 kHz has a period ($\delta 1T + \delta 2T$) of 10 μs . This gives an actual total period (including time to first valley detect) of 10.3 μs . So the actual converter frequency, and the oscillator frequency, will be 97 kHz ($f_{conv} = f_{osc} = 97 \text{ kHz}$).

The oscillator frequency is determined by the values of two parallel components - a resistor (R9) and a capacitor (C7). The capacitor is rapidly charged to $V_{RC(max)}$ (typically 2.5 V; see [Ref. 1](#)) and discharged via the resistor to $V_{RC(min)}$ (typical 75 mV; see [Ref. 1](#)). The discharge time has been calculated at $3.5 \times RC$ seconds (RC being the oscillator time constant). The oscillator time constant for our example can be calculated using the following equation:

$$RC = \frac{1}{3.5} \times \left(\frac{1}{f_{osc}} - t_{RC(ch)} \right) \tag{7}$$

The oscillator charge time is derived from the SSL2101 specification ($t_{ch(RC)} = 1 \mu s$; see [Ref. 1](#)). The values for both R9 and C7 can now easily be extracted from the RC time constant.

Using an oscillator capacitor of less than 220 pF is not recommended. The drain voltage might distort the oscillator voltage in this situation. From an efficiency point of view, a value for C7 of less than 1 nF is preferred.

In the example:

From [Equation 7](#), a switching frequency of 97 kHz would require an oscillator time constant of 2.66 μs . This time constant can be achieved by connecting a 3.9 k Ω resistor (R9) and a 680 pF capacitor (C7) in parallel.

Dimming can be implemented by lowering the oscillator frequency. The frequency reduction range is determined by the ratio of R8 to R9. Due to timing tolerance issues, it is recommended that R8 should not be greater than 220 k Ω .

In the example:

For a dimming range between 100 % and 5 %, the frequency range will be from 97 kHz down to 4.8 kHz (maximum dimming). Again applying [Equation 7](#), at a switching frequency of 4.8 kHz, R8 will be 87 k Ω . The nearest standard value is 91 k Ω .

6.4 Snubber circuit design

The snubber circuit (block 3 in [Figure 9](#)) uses a combination of a blocking diode (D5) and a Zener diode (D4). This approach is more efficient (lower losses) than alternative designs in the applied power range (see [Table 2](#)).

Table 2. Flyback converter operating modes

Method	Power range	Efficiency (% losses)
RC snubber	$P_O < 3 \text{ W}$	20 %
RCD clamp	full range	15 %
Zener clamp	full range	10 %

The maximum clamping voltage can be calculated using [Equation 8](#):

$$V_{zener} = V_{DRAIN(max)} - V_{buff(max)} - 25 \tag{8}$$

where:

V_{zener} = the breakdown voltage of the SSL2101 integrated power MOS transistor

$V_{DRAIN(max)}$ = maximum drain voltage = 600 V (see [Ref. 1](#)).

Since the power MOS transistor is not avalanche rugged, a small safety margin of 25 V is included.

In the example:

At a maximum buffer voltage of 384 V and a maximum drain voltage of 600 V, from [Equation 8](#): $V_{zener} = 600 - 384 - 25 = 191 \text{ V}$. A 200 V Zener diode was selected for D4.

6.5 V_{CC} generation

A circuit consisting of a capacitor, a rectifier diode, a peak current limiting resistor and a protection Zener diode is used to generate an external V_{CC} supply for the IC (see block 4 in [Figure 9](#)). The choice of component values involves a delicate trade-off between power dissipation and operation.

The values are determined by the output voltage, the transformer auxiliary-to-secondary turns ratio, the V_{CC} current and the lowest converter frequency: V_{CC} should be between 10.75 V (V_{CC(startup)(max)}; see [Ref. 1](#)) and 40 V and the current should be ≥ 2 mA. For the Zener, a value is required that ensures sufficient energy is stored in the buffering capacitor without exceeding V_{CC}. 30 V at 500 mW would be a practical value. The maximum dissipation is determined by the current delivered to the V_{CC} circuit at the highest converter frequency.

The auxiliary-to-secondary turns ratio can be calculated using the following equation:

$$m = \frac{N_a}{N_s} = \frac{V_{aux}}{V_{led} + V_{D6}} \quad (9)$$

where:

m = auxiliary-to-secondary turns ratio

N_a = the number of turns in the auxiliary winding

N_s = the number of turns in the secondary winding

V_{aux} = the voltage generated across the auxiliary winding

V_{D6} = the voltage across D6 when it is conducting (normally between 0.3 V and 0.8 V)

V_{led} = the voltage across the LED chain.

In the example:

A 30 V Zener diode was selected for D8, so we can assume V_{aux} ≅ 30 V. With V_{led} = 10 × 3.5 V and V_{D6} = 0.7 V, m = 30 / (35 + 0.7) = 0.8. So, with N_s = 58 (see [Section 7.4](#)), the number of turns in the auxiliary winding N_a = 0.8 × 58 = 46.

The value of R5 can be calculated using the following formula:

$$R5 = \delta 2 \times \frac{f_{min}}{f_{max}} \times \frac{\delta I_{min}}{\delta I_{nom}} \times \frac{(V_{CC(min)} - V_{D7})}{I_{VCC}} \quad (10)$$

where:

f_{min} = the minimum converter frequency during dimming

f_{max} = the maximum converter frequency during dimming

δ1_{min} = the minimum primary stroke duty factor at deepest dimming

δ1_{nom} = the nominal primary stroke duty factor

V_{CC(min)} = the nominal minimum value for V_{CC} (> V_{CC(startup)(max)}) - see [Ref. 1](#))

I_{VCC} = the minimum current to be delivered to the IC to ensure reliable operation.

In the example:

$$\begin{aligned} \delta 2 &= 0.82 \text{ (from Section 7.4); } f_{min} = 4.8 \text{ kHz; } f_{max} = 96.7 \text{ kHz} \\ \delta 1_{min} &= 0.03 \text{ (typical); } \delta 1_{nom} = 0.148 \text{ (from Section 7.1)} \\ V_{CC(min)} &= 12.75 \text{ V (} V_{CC(startup)(max)} + 2 \text{ V); } I_{VCC} = 2 \text{ mA (estimated) so} \\ R5 &= 0.82 \times \frac{4.8}{96.7} \times \frac{0.03}{0.148} \times \frac{11.3}{0.002} = 47 \text{ } \Omega . \end{aligned}$$

The peak power dissipated in R5 can be calculated from the following equation:

$$P_{R5(peak)} = \delta 2 \times \frac{(V_{aux} - V_{CC(min)} - V_{D7})}{R5} \quad (11)$$

In the example:

$$P_{R5(peak)} = 0.82 \times \frac{(30 - 12 - 0.7)^2}{47} = 5.2 \text{ W} .$$

D7 should be selected to withstand the peak current and reverse voltage, and the switching speed should be sufficient to operate at the converter working frequency.

The reverse voltage depends on the primary-to-auxiliary turns ratio, the maximum buffer voltage and the maximum V_{CC} voltage (which is equal to the Zener voltage of D8).

$$V_{revD7} = \left(\frac{N_p \times V_{buff(max)}}{N_a} \right) + V_{zener} \quad (12)$$

The maximum current through D7 is limited and can be calculated at start-up by dividing V_{aux} by the value of R5.

In the example:

With $N_p = 70$ (from Section 7.4) and $N_a = 46$, the primary-to-auxiliary turns ratio will be 1.52. At a buffer voltage of 384 V max and a Zener voltage of 30 V, the reverse voltage across D7 will be (from Equation 12): $V_{revD7} = 384 \times 1.5 + 30 = 614 \text{ V}$.

Capacitor C6 should provide sufficient buffering at the lowest frequency. This can be approximated with a linear model:

$$C6 = \frac{I_{VCC}}{\Delta V_{CC} \times f_{min}} \quad (13)$$

In the example:

Assuming a V_{CC} ripple voltage of 100 mV, I_{VCC} estimated at 2 mA and $f_{min} = 4.8 \text{ kHz}$, from Equation 13: $C6 = 0.002 / (0.1 \times 4800) = 4.2 \text{ } \mu\text{F}$.

6.6 Bleeder settings

The strong bleeder is designed to provide a low ohmic load for the dimmer to reset the dimmer timer and provide latch current. Tests have shown that the reset of the dimmer timing is related to a fixed charge transfer. With the SSL2101, this bleeder switches on

when the voltage on the SBLEED pin falls below $V_{th(SBLEED)}$, which is typically 52 V (see [Ref. 1](#)). The strong bleeder resistor R10 can be set to 1.5 Ω to allow the system to operate with the majority of field installed dimmers.

The weak bleeder is designed to maintain the hold current through the dimmer. It switches off when the voltage on the ISENSE pin drops below $V_{th(low)ISENSE}$, typically –250 mV (see [Ref. 1](#)). It switches on again when the voltage on the ISENSE pin rises above $V_{th(high)ISENSE}$, typically –100 mV (see [Ref. 1](#)). Hysteresis is included to prevent unwanted oscillations. The weak bleeder should switch on if the input current from the bleeder to the converter drops below the hold current of the dimmer. In practice, a value of 10 mA will be sufficient to operate with most dimmers. The weak bleeder resistor R11 should conduct this RMS current. R12 is included to dampen oscillations. [Table 3](#) shows typical values for these components with reference to the input voltage.

Table 3. Bleeder component settings

Input voltage	R10	R11	R12
120 V (AC)	1 k Ω	15 k Ω	100 Ω
230 V (AC)	1.5 k Ω	27 k Ω	200 Ω
277 V (AC)	1.5 k Ω	27 k Ω	220 Ω

The ratio between R13 and R14 can be calculated using this data: A dimmer requires a minimum hold current of 10 mA, which is maintained by means of the weak bleeder switch. Switch on at 10 mA over 200 Ω results in –2 V across R12 (or across R13 + R14). The weak bleeder switches on when the voltage on pin ISENSE (or across R14) is –100 mV. So $R14 / (R13 + R14) = 100 \text{ mV} / 2 \text{ V} = 1 / 20$, therefore:

$$\begin{aligned} R13 + R14 &= 20 \times R14 \Rightarrow \\ R13 &= (20 - 1)R14 \Rightarrow \\ R13 / 19 &= R14. \end{aligned}$$

I_{ISENSE} is protected by R13 and should not exceed –5 mA. The maximum peak voltage is limited to 400 V by D2, but a safety margin of 100 V is applied. So $R13 = 500 \text{ V} / 5 \text{ mA} = 100 \text{ k}\Omega$.

Therefore $R14 = 100 \text{ k}\Omega / 19 = 5.3 \text{ k}\Omega$. Note that all these resistors will need to be able to withstand peak power and peak voltage. R10 and R11 should be rated to withstand the voltage at which the TVS (D2) sets in. R12 should be rated to withstand the peak voltage and pulse energy at start-up. This pulse energy is listed in resistor data and can be calculated as follows:

$$E_{pulse} = 1/2 \times C_{3+4} \times V_{I(peak)}^2 \quad (14)$$

6.7 Dimming detection

The dimming reference voltage is derived from the non-buffered rectified mains voltage, and averaged using a capacitor. This voltage is input to the BRIGHTNESS and PWMLIMIT pins in the SSL2101 (see [Figure 9](#)). By balancing the voltage levels at these two inputs, the peak current through the inductor is reduced before the frequency of the converter falls. This eliminates audible noise from the transformer. The BRIGHTNESS and PWMLIMIT inputs have internal current sources, to which the working point of the converter is shifted. C8 provides filtering and has a recommended default value of 4.7 μF .

Table 4. Recommended dim-circuit values for continuous operation

Input voltage	R15	R16	R17
120 V (AC)	680 kΩ	15 kΩ	10 kΩ
230 V (AC)	1.5 MΩ	15 kΩ	10 kΩ
277 V (AC)	1.5 MΩ	15 kΩ	8.2 kΩ

R7 defines the dimming curve and regulates the maximum power delivered to the LEDs. It regulates the peak current through the inductor and thus the maximum power level. It also provides overcurrent protection to the converter. This technique removes the dependency between the output power and the mains voltage. The built-in overcurrent protection circuit triggers at 0.5 V. If the secondary losses and frequency are known, R7 can be calculated as follows:

$$R7 = \sqrt{\frac{P_{in}}{f_{conv} \times L_p}} \tag{15}$$

where:

$$P_{in} = P_{in(trans)} \text{ (see Section 6.3) } + \text{ snubber losses.}$$

In the example:

With $P_{in} = 14 \text{ W} + 0.1 \text{ W}$ (estimated), $f = 97 \text{ kHz}$ and $L_p = 415 \mu\text{H}$ (see Section 6.3), from Equation 15. $R7 = \sqrt{15 / (97000 \times 0.000415)} = 0.6 \Omega$.

R6 limits the current flowing into the AUX pin, typically to 100 μA. R6 can be calculated as follows: $R6 = V_{aux} / I_{aux} = 30 / 0.0001 = 300 \text{ k}\Omega$.

6.8 Buffer circuit

The buffer circuit is made out of two capacitors and an inductor. The circuit has dual functionality. The first function is to store energy to ensure the converter can transfer power continuously to the LED chain. LED operation becomes independent of dimmer operation and mains power fluctuations are filtered out. The second function is to filter ripple current generated by the converter to ensure compliance with legal requirements in relation to mains conducted emissions.

To implement the first function, the voltage across the converter should not fall below the minimum working voltage within a single mains cycle. The total capacitance (C3 + C4) can be estimated as follows.

First the minimum voltage at which the converter will still deliver full power needs to be calculated. This is either a duty-factor limit of 75% or the ratio of cycle time to cycle time minus secondary stroke time and is derived from the calculated primary inductance and peak current:

$$V_{buff(min)} = \frac{I}{\partial_{lmax}} \times f_{conv} \times I_p \times L_p \tag{16}$$

In the example:

At a converter frequency of 97 kHz and primary inductance of 415 μH (see [Section 6.3](#)), a maximum primary stroke of 14.8 % and primary peak current of 0.821 A (see [Section 7.1](#)), the minimum operating voltage will be:

$$V_{\text{buff}(\text{min})} = \frac{I}{0.148} \times 97000 \times 0.821 \times 0.000415 = 223 \text{ V}.$$

Next the time between the peak voltage and when the mains voltage has reached this minimum voltage needs to be calculated. Allow a margin of 10 V to allow for voltage drop during capacitor charging:

$$t_{\text{dis}} = \left(1 + \frac{2}{\pi} \times \arcsin\left(\frac{V_{\text{buff}(\text{min})} + 10}{V_{\text{mainspeak}}}\right) \right) \times \frac{1}{4 \times f_{\text{net}}} \quad (17)$$

where:

f_{net} = frequency of mains voltage

$$V_{\text{mainspeak}} = V(\text{AC})(\text{RMS}) \times \sqrt{2}.$$

In the example:

$$V_{\text{mainspeak}} = 230 \times \sqrt{2} = 325 \text{ V}.$$

At a mains voltage of 230 V (AC), 50 Hz, and a minimum operating voltage of 223 V, the capacitor discharge time is 7.53 ms.

Now take the transformer input power and add IC losses and snubber losses. The following equation can be used to calculate the total buffer capacitance:

$$C3 + C4 = \frac{2 \times P_{\text{tot}} \times t_{\text{dis}}}{V_{\text{mainspeak}}^2 - V_{\text{buff}(\text{min})}^2} \quad (18)$$

where

$$P_{\text{tot}} = P_{\text{in}} + \text{IC losses}.$$

In the example:

With $P_{\text{in}} = 15 \text{ W}$ (see [Section 6.7](#)) and IC losses of 700 mW, $P_{\text{tot}} = 15.7 \text{ W}$.

With $t_{\text{dis}} = 7.53 \text{ ms}$, $V_{\text{mainspeak}} = 325 \text{ V}$ and $V_{\text{buff}(\text{min})} = 223 \text{ V}$, the total calculated capacitance ($C3 + C4$) is 4.2 μF .

Using the nearest standard values gives $C3 = C4 = 2.2 \mu\text{F}$.

The combination of L2, C3 and C4 constitute a Pi-Filter that will help to filter out the high frequency currents generated by converter action. Although a single filter stage will not be enough to satisfy legal requirements in relation to mains conducted emissions, it will go some way to achieving these goals. The cut-off frequency of this filter should be a magnitude below the converter frequency:

$$f_{\text{cutoff}} = \frac{1}{2 \times \pi \times \sqrt{L_2 \times \frac{C3 \times C4}{C3 + C4}}} \quad (19)$$

assuming $C3 = C4$. If the cut-off frequency is selected to be a decade below the working frequency, the resulting formula for L2 becomes:

$$L2 = \frac{100}{C_S \times 4\pi^2 \times f_{conv}^2} \quad (20)$$

where:

$$C_S = C3 = C4.$$

In the example:

At a converter frequency of 97 kHz with $C3 = C4 = 2.2 \mu\text{F}$, L2 will be 122 μH .

It is recommended that a low-frequency absorbent soft ferrite material, like 3S1 (Ferroxcube) or 3W1200 (Würth), be used for this inductor in order to dissipate high frequency energy and block unwanted oscillations.

6.9 Input circuit

The input circuit rectifies the mains voltage and provides overcurrent and overvoltage protection. It has to be over-dimensioned to cope with overvoltage and overcurrent conditions on the input. Primary protection consists of a fuse or fusistor that breaks down when the current exceeds a specified value. If a fuse is used, a breakdown value should be selected that can handle inrush currents whilst still providing overcurrent protection. In practice, a value of between 1 A and 1.5 A is sufficient. If a fusistor is selected, the minimum value for this resistor can be calculated using [Equation 21](#). For almost all diode bridge rectifiers, the I_{FSM} parameter is around 20 A.

$$R1 = \frac{\sqrt{2} \times V_{AC(max)}}{I_{FSM}} \quad (21)$$

In the example:

At 230 V (AC) \pm 20 %, $V_{AC(max)} = 276$ V. Therefore $R1 = 19.5 \Omega$. The nearest E24 series standard value is 20 Ω .

Besides its ohmic value, the continuous power dissipation in R1 is an important characteristic. This value can be determined using the following equation:

$$P_{R1} = C_{crestfactor} \times R1 \times \frac{P_{tot}^2}{V(AC)^2} \quad (22)$$

where:

the crest factor is the ratio of RMS to average current, typically 4.

In the example:

With $V(AC) = 230$ V, $P_{tot} = 15.7$ W (see [Section 6.8](#)), $R1 = 20 \Omega$ and crest factor = 4, the power dissipated in R1 will be 370 mW.

Capacitor C1 (470 pF recommended) is added to improve differential mode filtering (in combination with L1; 2.2 mH recommended). By placing this component close to the mains input, the inductive coupling to mains is reduced. It also provides buffering against voltage spikes. The values of these input components are partly determined by the requirements of the dimmer. At low levels of output power, R4 can be added to reduce the audible noise generated by inrush current towards C3/C4.

Components D1 and D3 should be dimensioned to handle the peak current in the circuit. This peak current is restricted by the combination of R12, R1 and R4.

$$I_{peak} = \frac{\sqrt{2} \times V_{AC(max)}}{R12 + R1 + R4} \tag{23}$$

In the example:

At 230 V (AC) ± 20 %, R12 = 260 Ω, R1 = 20 Ω and R4 = 0 Ω, the peak current will be 1.4 A.

7. Transformer design parameters

One of the most challenging aspects of flyback design involves transformer calculations. A number of parameters affect the operation of the transformer - converter frequency, input/output voltage, input/output power, input peak current etc. In addition, a multitude of other factors, such as transformer size, material, core losses, proximity losses and ohmic losses can be optimized to maximize transformer efficiency. To complicate matters further, there are a number of models available on which to base these calculations - with no consensus within the scientific community as to which model produces the best results. With so many variables to consider and factors to trade off against one another, an optimal design can only be achieved through extensive prototyping and measuring.

The SL2101 cannot be used in flyback mode in applications greater than 25 W, because of the power dissipation versus peak current characteristics of the internal switch.

In addition to core size, careful consideration should be given to core geometry and core material. Core material should be selected for optimum (low) losses at the working temperature. For SSL2101 applications between 50 kHz and 200 kHz, the following core materials are recommended - 3C90 or 3F3 (Ferroxcube), N87 (Epcos) or TP4 (TDG).

For applications where cost is critical, e-cores are the most common choice. RM cores should be considered if shielding is critical.

Table 5. Comparative geometry considerations for ferrite cores

Aspect	Pot and RM core	Double stab core	E-core	Ec, ETD cores	PQ core	EP core	Toroid
core costs	high	high	low	medium	high	medium	very low
bobbin costs	low	low	low	medium	high	high	none
winding costs	low	low	low	low	low	low	high
winding flexibility	good	good	excellent	excellent	good	good	fair
assembly	simple	simple	simple	medium	simple	simple	none

Table 5. Comparative geometry considerations for ferrite cores

Aspect	Pot and RM core	Double stab core	E-core	Ec, ETD cores	PQ core	EP core	Toroid
mounting flexibility	good	good	good	fair	fair	good	poor
heat dissipation	poor	good	excellent	good	good	poor	good
shielding	excellent	good	poor	poor	fair	excellent	good

The application requires a transformer with three windings - a main or primary winding N_p , an output or secondary winding N_s and the auxiliary winding N_a . The number of turns required must be calculated for each of the three windings.

7.1 Calculating the primary inductance

To determine the optimal primary inductance, the minimum duty cycle at which the IC switch dissipation is acceptable needs to be calculated:

$$\delta I = \frac{2 \times R_{DSon} \times P_{in(trans)}^2}{V_{buff(eff)}^2 \times P_{sw}} \tag{24}$$

where:

- δI = minimum duty factor for acceptable switch dissipation
- P_{sw} = power budget for resistive losses in internal (MOSFET) switch
- R_{DSon} = drain-source on-state resistance = 10 Ω (see [Ref. 1](#))
- $V_{buff(eff)}$ = effective buffer voltage.

In the example:

R_{DSon} is, typically, 10 Ω (max); $P_{in(trans)} = 14$ W (see [Section 6.3](#)); $V_{buff(eff)} = 230$ V (effective); $P_{sw} = 500$ mW (estimated). From [Equation 24](#), the duty factor:

$$\delta I = \frac{2 \times 10 \times 196}{52900 \times 0.5} = 0.148 \text{ or } 14.8 \%$$

The inductance of the primary winding (L_p) can be calculated using the following equation:

$$L_p = \frac{R_{DSon} \times P_{in(trans)} \times \delta I}{P_{sw} \times f_{conv(nom)}} \tag{25}$$

In the example:

$R_{DSon} = 10$ Ω , $P_{in(trans)} = 14$ W, $P_{sw} = 500$ mW, $f_{conv(nom)} = 100$ kHz, $\delta I = 14.8$ %. So:

$$L_p = \frac{10 \times 14 \times 0.148}{0.5 \times 100000} = 415 \mu H.$$

The primary current can be calculated using the following equation:

$$I_{p(peak)} = \frac{V_{buff(eff)} \times \delta I}{L_p \times f_{conv(nom)}} = \sqrt{\frac{2 \times P_{in(trans)}}{L_p \times f_{conv(nom)}}} \tag{26}$$

In the example:

$V_{buff(eff)} = 230 \text{ V (estimated)}$; $P_{in} = 14 \text{ W}$, $f_{conv(nom)} = 100 \text{ kHz}$, $\delta 1 = 14.8 \%$, $L_p = 415 \mu\text{H}$.

$$\text{So: } I_{p(peak)} = \frac{230 \times 0.148}{0.000415 \times 100000} = \sqrt{\frac{2 \times 14}{0.000415 \times 100000}} = 0.821 \text{ A.}$$

7.2 Selecting the core type

The size of the core is determined by the maximum amount of energy to be stored in the transformer together with the required air gap. A core with a large air gap can store more energy in its air gap than a core with a small air gap. Also, the spread on the transformer's primary inductance (L_p) will be lower for wide air gaps. The disadvantage of a wide air gap is the high leakage inductance of the transformer. A trade-off has to be made between storable energy, leakage inductance and tolerances on the inductance. The maximum energy that can be stored in the transformer can be calculated from [Equation 27](#) (see also [Equation 4](#)):

$$E = 1/2 \times L_p \times I_p^2 \tag{27}$$

The output power range determines which core types are suitable, as detailed in [Table 6](#):

Table 6. Comparative geometry considerations for ferrite cores

O/P power range	Core type	A_e (mm ²)
0 W - 2 W	E13/6/3	10.1
2 W - 4 W	E13/6/6	20.2
4 W - 6 W	E16/8/5	20.1
6 W - 11 W	E20/10/6	32.0
12 W - 14 W	E25/10/6	37.0
14 W - 25 W	E25/13/7	52.0

7.3 Primary winding count

There is a dependency between the air gap and the number of primary turns. The air gap must be big enough to avoid tolerance issues and small enough to minimize proximity losses (caused by the fringing field). In practice, an air gap of between 100 μm and 1 mm is advisable.

[Equation 28](#) and [Equation 29](#) can be used to establish a suitable balance between the air gap and the number of turns. The parameter A_e represents the effective core area in square meters (m²) and B_{max} represents the maximum flux density in Tesla. For most ferrite materials, a B_{max} value of 275 mT is low enough to prevent saturation. These values can be obtained from the core material data sheet.

The number of turns in the primary winding can be calculated using the following empirical equation:

$$N_p = \frac{1}{22} \times \frac{\sqrt{L_p} \times I_p}{B_{max} \times A_e} \tag{28}$$

In the example:

With $L_p = 415 \mu\text{H}$, $I_p = 0.821 \text{ A}$, $B_{max} = 275 \text{ mT}$ $A_e = 39.5 \text{ mm}^2$, the number of turns in the primary winding will be 70 (rounded to the nearest integer).

The air gap can now be calculated using empirical [Equation 29](#):

$$l_{gap(M)} = \frac{18 \times A_e}{\left(\frac{9 \times 10^6 \times L_p}{N_p^{1.9}} \right) - 50 \times \sqrt{A_e}} \quad (29)$$

In the example:

With $L_p = 415 \mu H$, $N_p = 70$, $A_e = 39.5 \text{ mm}^2$ the air gap will be $837 \mu M$.

7.4 Secondary winding count

As a precondition to calculating the number of turns in the secondary winding, the following conditions must be met:

- At the minimum duty factor of the primary switch, the converter should operate at first valley detect
- The maximum reverse voltage on the switch should not be greater than 600 V ($V_{DRAIN(max)}$; see [Ref. 1](#)).

In relation to the first condition, the second stroke time, $\delta 2T$, can be calculated using [Equation 30](#):

$$\delta 2T = \frac{1 - \delta 1}{f_{conv(nom)}} - \frac{1}{4 \times f_{ring}} \quad (30)$$

In the example:

With $f_{ring} = 722 \text{ kHz}$ and $f_{conv(nom)} = 100 \text{ kHz}$ (see [Section 6.3](#)) and $\delta 1 = 0.148$ (see

[Section 7.1](#)): $\delta 2T = \frac{1 - 0.148}{100000} - \frac{1}{4 \times 722000} = 8.2 \mu s$. So $\delta 2 = 0.82$.

The time it will take to discharge the coil energy into the load can be estimated from [Equation 31](#).

$$\delta 2T = \frac{\hat{I}_s \times L_s}{V_{D6} + V_{led}} \quad (31)$$

The relationship between the secondary and primary peak currents is determined by the turns ratio between the windings:

$$n = \frac{\hat{I}_s}{\hat{I}_p} = \frac{N_p}{N_s} = \sqrt{\frac{L_p}{L_s}} \quad (32)$$

Given the above, the winding ratio (and therefore the number of secondary turns) can be derived from [Equation 31](#) and [Equation 32](#):

$$n = \frac{\hat{I}_p \times L_p}{\delta 2T \times (V_{D6} + V_{led})} \quad (33)$$

In the example:

With $\delta 2T = 8.2 \mu\text{s}$, $V_{D6} + V_{led} = 35.7 \text{ V}$, $I_p = 0.821 \text{ A}$ and $L_p = 415 \mu\text{H}$ ([Section 7.1](#)):

$$n = \frac{0.821 \times 415^{-6}}{8.2^{-6} \times 35.7} = 1.2.$$

So the winding ratio will be 1.2:1. If number of turns in the primary winding is 70, the secondary winding will have 58 turns. If the primary inductance is $415 \mu\text{H}$, the secondary inductance will be $314 \mu\text{H}$. The secondary peak current will be 985 mA.

The reflected voltage (nV_{out}) induced in the primary winding can be calculated as follows:

$$V_{reflect} = n \times (V_{D6} + V_{led}) \quad (34)$$

In the example:

$V_{reflect} = 1.2 \times 35.7 \text{ V} = 42.84 \text{ V}$. The maximum drain voltage, $V_{drain(max)}$, will be $384 \text{ V} + 42.84 \text{ V} = 427 \text{ V}$.

7.5 Auxiliary winding count

The number of turns in the auxiliary winding, $N_a = 46$, was calculated in [Section 6.5](#).

7.6 Selecting wire diameters

Wire diameter selection involves a trade-off between size, ohmic losses, proximity losses and skin losses. For SSL2101 applications, skin losses are generally negligible for wire sizes below 0.6 mm in diameter at operating frequencies below 200 kHz. For wire diameters above 0.6 mm diameter, the use of Litze wire or multiple strands is recommended.

Ohmic losses are related to the peak currents in the wire. These can be estimated by obtaining the wire resistance, then calculating the average power dissipation. As a rule of thumb, the current density should be between 300 CM and 500 CM (Circular Mills /Amp). [Table 7](#) gives appropriate wire sizes for a range of currents.

Table 7. Wire selection table

Diameter (mm)	Nearest AWG	Area (mm ²)	Area (CM)	DC Res. OHM/M	Typical current lvl (Amp)
0.1	38	0.008	15	2.195	0.04
0.2	32	0.031	62	0.549	0.15
0.25	30	0.049	97	0.351	0.24
0.315	28	0.078	154	0.221	0.38
0.355	27	0.099	195	0.174	0.49
0.4	26	0.126	248	0.137	0.62
0.56	23	0.246	486	0.070	1.22
0.71	21	0.396	781	0.044	1.95
16 × 0.2		0.503	992	0.034	2.48
37 × 0.2		1.162	2294	0.015	5.73
61 × 0.2		1.916	3782	0.009	9.45

7.7 Proximity losses

For proximity losses, the calculations are too complicated to be discussed in this application note. What should be clear, however, is that they are closely related to the skin depth and the number of windings.

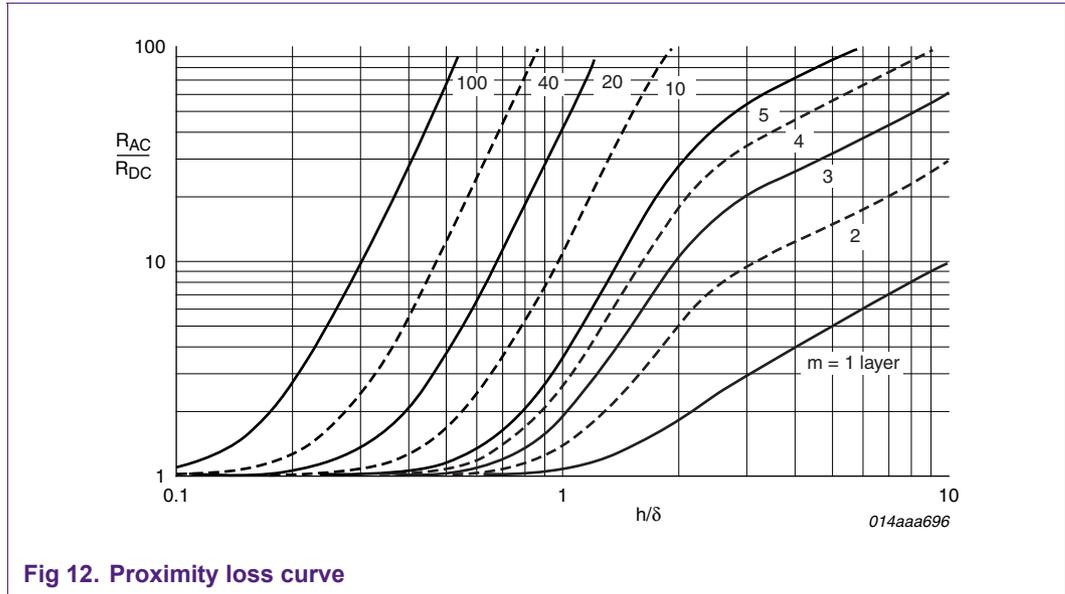


Fig 12. Proximity loss curve

The graph in [Figure 12](#) shows the ratio of AC-to-DC resistance for a section of a strip winding at different frequencies - δ represents skin depth, h is the height of a square conductor. It can be seen that increasing the number of layers dramatically increases the resistance at high frequencies. For the SSL2101 operating between 50 kHz and 200 kHz using copper wire, the skin depth should be between 0.3 mm to 0.15 mm. Since the h/δ ratio increases at higher currents, the number of winding layers should be minimized, even if it means selecting a higher current density.

8. Mains dimmer compatibility

8.1 Compatibility list

If the default values for the strong and weak bleeder resistors (R10 and R11) detailed in [Table 3](#) are used, the majority of existing wall mounted dimmers will be supported. The dimmers listed in [Table 8](#) were all successfully evaluated.

Table 8. Dimmer list

Manufacturer	Type	Voltage (AC)	Power range	Load	Fuse
Opus	852.390	230	60-400	Ha/Inc	F1.6
Opus	852.392	230	20-500	Inc	T2
Bush-Jaeger	2250U	230	20-600	Ha/Inc	T3.15
Bush-Jaeger	2247U	230	20-500	Ha/Inc	T3.15
Bush-Jaeger	6519U	230	40-550	Ha/Inc	-
Gira	1184	230	60-400	Inc	T1.6
Everflourish	EFO700D	230	50-300	Ha/Inc	T1.25

Table 8. Dimmer list

Manufacturer	Type	Voltage (AC)	Power range	Load	Fuse
Ehmann	10 UP-kpl	230	60-300	Ha/Inc	F1.25
Ehmann	39 Domus	230	20-500	Ha/Inc	T2A
Ehmann	4660	230	20-315	Ha/Inc	-
Lutron	TG-600PH-WH	120	600	Inc	-
Levitron	L12-6641-W	120	600	Inc	-
Levitron	L02-700-W	120	600	Inc	-
Levitron	6602-IW	120	600	Inc	-
Levitron	6683-W	120	600	Inc	-
Levitron	R12-6631-LW	120	600	Inc	-
Cooper	6001	120	600		-
Lutron	MIR-600THW-WH	120	600	Ha/Inc	-
Lutron	S-600PH-WH	120	600	Ha/Inc	-
GE	DI61-271	120	600	Inc	-
GE	DITC61-S71	120	600	Inc	-
GE	DIT61-71	120	600	Inc	-
GE	DIB61-71	120	600	Inc	-

The following problems may occur with some dimmers:

- At low dimming levels, a step function can be encountered in light output: the dimmer and converter interact and the dimmer output increases due to the increasing load.
- At certain dimming levels, the dimmer may react to an increase in load by reducing on time. This can lead to instability in the sensed voltage resulting in lamp flicker.

The effects of these problems can be minimized by weakening the relationship between the variable converter power and the load, as seen by the dimmer - either by increasing the load, or reducing the steepness of the dimming curve. This can be achieved by altering the values of R15 and R17. Note that the trade-off will be a reduced dimming range or an increase in power dissipation.

8.2 Transistor dimmers

A transistor dimmer may demand a higher load than can be realized with the standard bleeder values, to ensure the full voltage drop when dimming is turned off. Typically, a continuous load current of 10 mA or more is required.

The dimming range will be restricted with the standard dim-curve circuit, especially when deep dimming is combined with a low output load, because the average voltage drop will not be sufficient to detect dimming. To compensate for this, the dimming curve can be shifted - but the trade-off will be a lower dim-range with triac dimmers. This will not be a problem as long as the output load is > 2.3 W.

If the circuit needs to be compatible with both triac and transistor dimmers, and deep dimming is required at low output loads, an additional resistive bleeder can be connected in parallel with C1. A value of 22 k Ω /3 W at 230 V (AC) or 12 k Ω /1.5 W at 120 V (AC) would be appropriate.

A transistor dimmer with trailing edge operation doesn't need a hold current. Nor does it generate high inrush currents. These advantages over the standard triac dimmer can be exploited by omitting the damper network (R12/R13/R14). The ISENSE pin can be connected to GND. As a result, dissipation and audible noise will be reduced during dimming, and the inrush peak current will be reduced.

8.3 Multiple lamp circuits

The SSL2101 was designed to operate in a one-to-one situation - one lamp connected to one dimmer. However, it is possible to connect multiple lamps to a single dimmer. There is a restriction when using leading edge triac dimmers - the inrush current of all lamps must be combined if the dimmer is to withstand these inrush currents. Normal lamps and halogen lamps can generate inrush currents several times greater than the nominal current.

The inrush current can be calculated by subtracting the buffer voltage across C3/C4 at maximum input voltage from the input voltage, and dividing this by the value of R12:

$$\hat{I}_{inrush} = \frac{V_{in} - V_{buff}}{R12 + R1} \quad (35)$$

A standard value for this inrush current is 500 mA at 230 V (AC). This corresponds to a Halogen lamp of 50 W. When trailing edge dimmers are used, this inrush current is eliminated. The effective load of the lamp will be close to the nominal load.

9. Dimming curve calculations

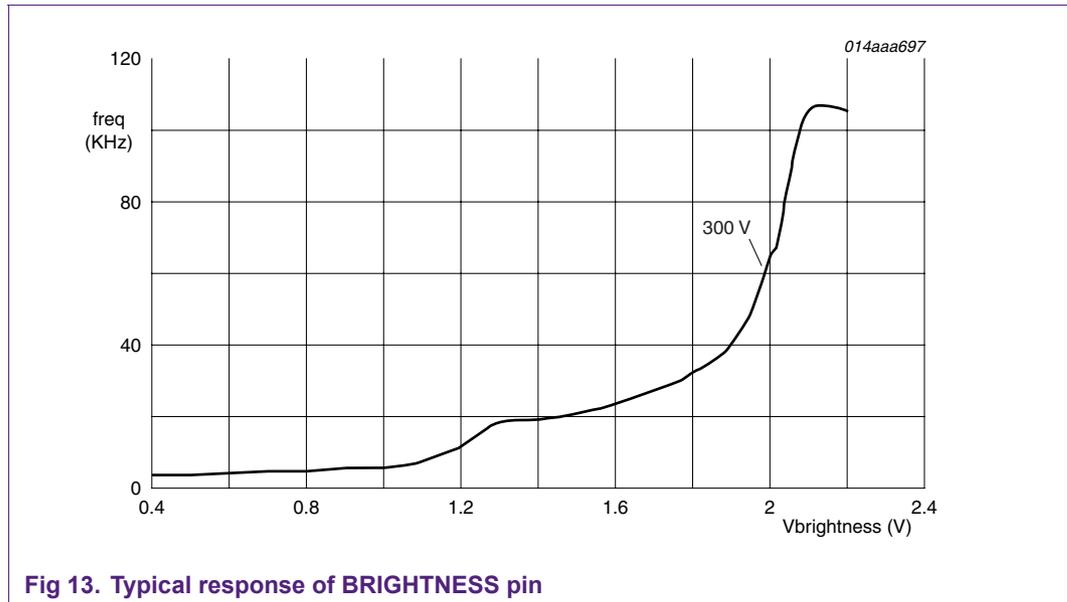
The dimming curve describes the relationship between light output and the dimmer setting. The SSL2101 offers a great deal of freedom in dimming curve selection. The typical flyback application is an example of power steering: The output power dissipated in the LEDs is regulated by the IC. The current is determined by the forward voltage of the LEDs. The relationship between light output and the dimmer setting is defined in the following equation:

$$P = \eta \times I/2 \times L_p \times I_p^2 \times f \quad (36)$$

where:

η = estimated converter efficiency.

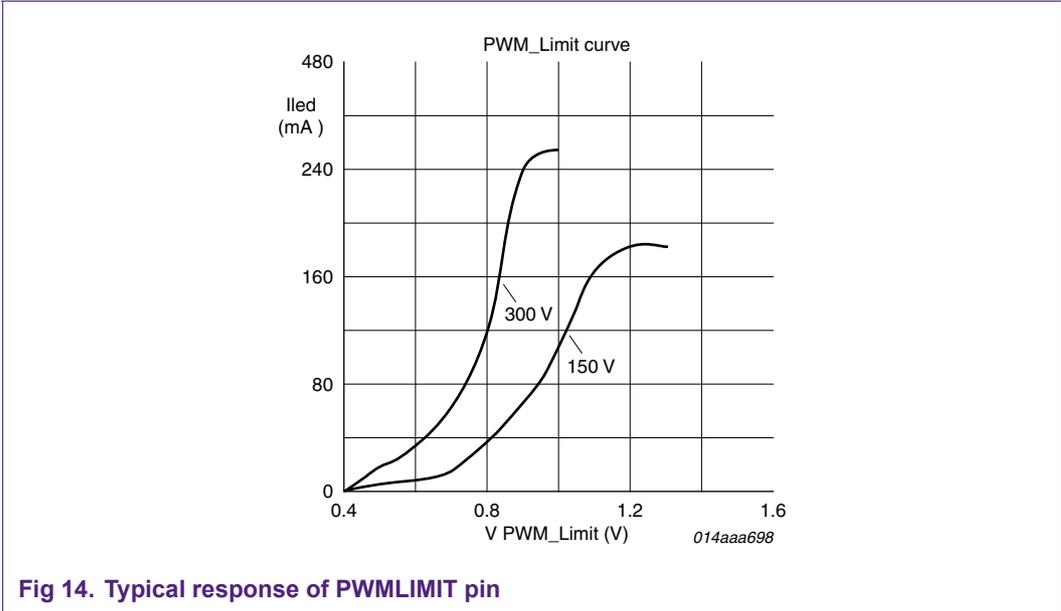
The SSL2101 has two control inputs: a BRIGHTNESS input that controls the output frequency and a PWMLIMIT pin that controls the on-time of the switch. If overcurrent protection is not enabled and/or the maximum duty factor of 75 % has not been exceeded, the LED power will correlate quadratically to the variation in duty factor. To enhance the performance of the system, a correction curve for the BRIGHTNESS pin voltage versus converter frequency was introduced. This correction curve compensates for the difference in light output between LEDs and incandescent/halogen lamps.



As can be seen in [Figure 13](#), the frequency of the converter varies between a minimum frequency determined by the values of C7 and R8, and a maximum frequency determined by C7 and R9. The frequency is independent of converter input voltage and load fluctuations.

For the PWMLIMIT input, a different set of rules applies. Here, the peak current level varies with buffer voltage. The buffer voltage, in turn, depends on the output load and dimmer setting. The resulting behavior is highly complex.

Although a dimming function can be implemented using only the PWMLIMIT input, for deep dimming the brightness modulation is also used. The result enables a dimming range from 100 % down to 0.1%. Resistor R16 is added to reduce audible noise. The internal 20 μ A current source raises the voltage on the BRIGHTNESS. This shifts the brightness curve to the left, lowering the frequency at low dimmer settings. At these levels, the current controlled by the PWMLIMIT pin has already been reduced. The peak current through the inductor is the main source of audible transformer noise.



10. Application diagram

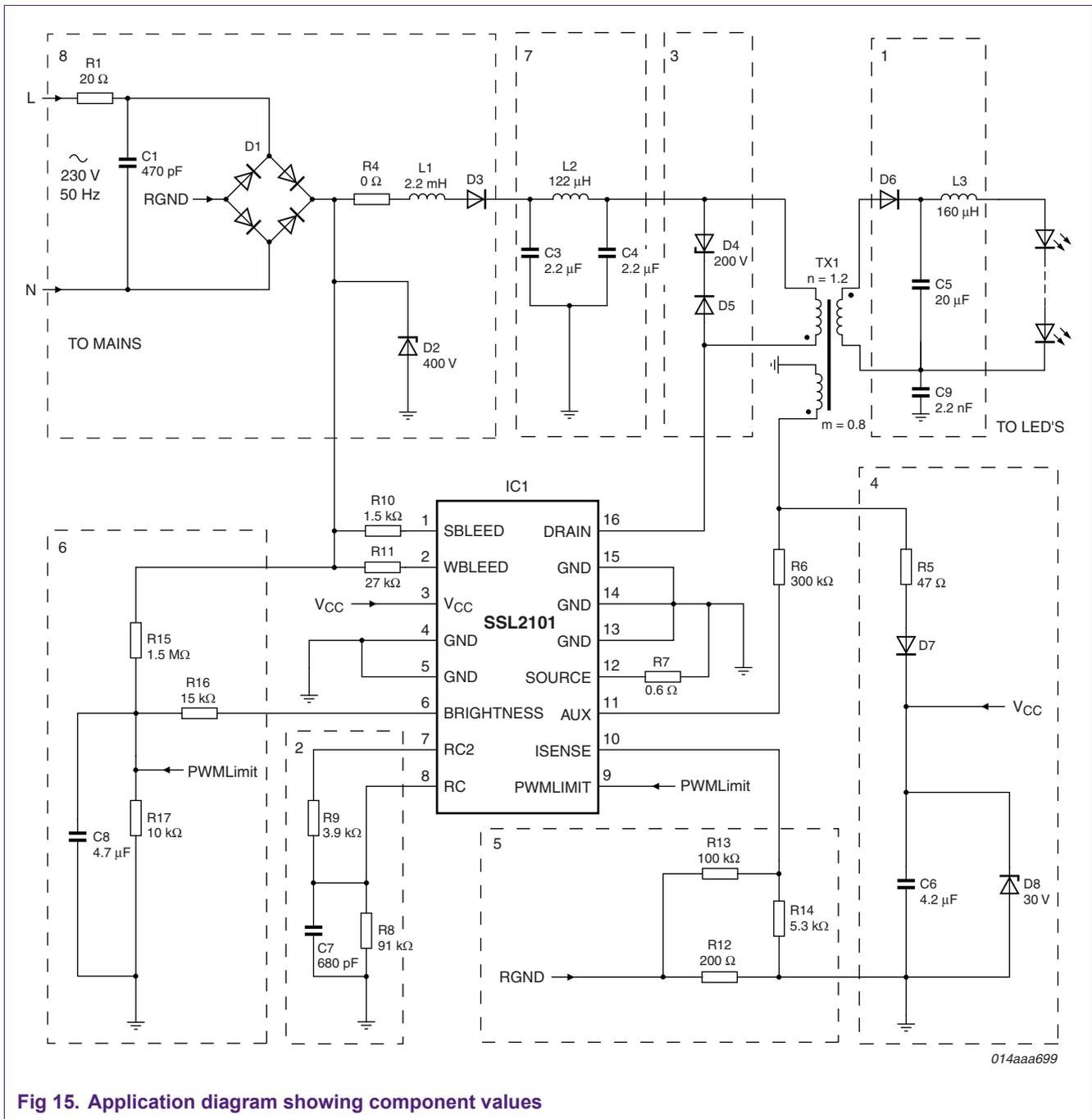


Fig 15. Application diagram showing component values

11. Summary

This document describes the construction of a flyback based converter - a typical application of the SSL mains dimmable LED driver: It provides some general information about LED properties, some converter basics and mains dimmer aspects. The step-by-step design procedure provides the designer with information on how to dimension the components in this application and the functionality of the circuit. It contains

a section on transformer design that should enable the designer to estimate values for the main transformer parameters such as core size, air gap, number of winding and wire size. It ends with a description of mains dimmer dependencies and advice on solving potential dimmer problems.

12. Appendix A: Additional information

12.1 Core materials overview:

<http://www.mhw-intl.com/products/tdgmaterialsguide.htm>

http://www.ferroxcube.com/prod/assets/sfmatgra_frnt.pdf

http://www.pe-coils.com/MnZn_Feirrite/MATERIAL%20COMPARES.pdf

12.2 Some Links to Magnetics vendors:

<http://www.mag-inc.com/pdf/ps-02.pdf>

http://magneticsinc.com/pdf/2006_Powder_Core_Selection.pdf

<http://www.ferroxcube.com/appl/info/PSG2003.pdf>

<http://www.ferroxcube.com>

<http://www.we-online.com>

<http://www.epcos.com>

12.3 About RFI capacitors:

http://www.evoxrifa.com/technote_pdf/rfi_fact.pdf

12.4 Pulse calculation resistors:

<http://www.welwyn-tt.co.uk/CalcTools.asp>

12.5 Wire selection table:

http://www.powerstream.com/Wire_Size.htm

Stealth 316 - Wire Resistance and Voltage Drop Calculator

12.6 About transformer design:

http://www.geofex.com/Article_Folders/xformer_des/xformer.htm

EDN Access--03.14.97 Spreadsheet simplifies switch-mode power-supply flyback-transformer design

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
LED	Light emitting diode
IC	Integrated circuit
MOSFET	Metal oxide semiconductor field effect transistor
MCM	Multi chip module
SO	Small outline
ESR	Equivalent series resistor
EMC	Electromagnetic compatibility
SSL	Solid state lighting
RMS	Root mean square
V (AC)	Voltage alternating current
PWM	Pulse width modulation
CM	Circular Mills
DC	Direct current
GND	Ground potential
OCP	Over current protection
OVP	Over voltage protection
SWP	Short winding protection
OTP	Over temperature protection
TLM	Temperature lumen management

14. References

- [1] **SSL2101** — SMPS IC for dimmable LED lighting data sheet Rev. 01.

15. Legal information

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16. Contents

1	Introduction	3	15.2	Disclaimers	38
2	LED properties	3	15.3	Trademarks	38
2.1	Serial/parallel configuration	4	16	Contents	39
3	Flyback converter basics	4			
4	Mains dimming	6			
4.1	Dimmer switch classification	7			
4.2	Triac dimmer	8			
4.3	Transistor dimmer	8			
5	Functional description	8			
6	Step-by-step design procedure	10			
6.1	Basic configuration	10			
6.2	Output circuit	12			
6.3	Oscillator components	14			
6.4	Snubber circuit design	17			
6.5	V _{CC} generation	18			
6.6	Bleeder settings	19			
6.7	Dimming detection	20			
6.8	Buffer circuit	21			
6.9	Input circuit	23			
7	Transformer design parameters	24			
7.1	Calculating the primary inductance	25			
7.2	Selecting the core type	26			
7.3	Primary winding count	26			
7.4	Secondary winding count	27			
7.5	Auxiliary winding count	28			
7.6	Selecting wire diameters	28			
7.7	Proximity losses	29			
8	Mains dimmer compatibility	29			
8.1	Compatibility list	29			
8.2	Transistor dimmers	30			
8.3	Multiple lamp circuits	31			
9	Dimming curve calculations	31			
10	Application diagram	34			
11	Summary	34			
12	Appendix A: Additional information	36			
12.1	Core materials overview:	36			
12.2	Some Links to Magnetics vendors:	36			
12.3	About RFI capacitors:	36			
12.4	Pulse calculation resistors:	36			
12.5	Wire selection table:	36			
12.6	About transformer design:	36			
13	Abbreviations	37			
14	References	37			
15	Legal information	38			
15.1	Definitions	38			

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