# 14W Off-line LED Driver,

## 120VAC, PFC, 14V, 1A Load

| Specifications | |
| --- | --- |
| AC Line Voltage | 100 - 135 VAC |
| LED (string) Voltage | 0 – 14V |
| LED Current | 1A |
| Switching Frequency | 70 – 120kHz |
| Efficiency | 74 % (@ 14V) |
| Open Circuit Protection | Yes (Output Voltage 33V) |
| Short Circuit Protection | Yes (Output Current 1A) |
| AC Line Undervoltage | LED and AC Line Current fall off gradually below 100 VAC |
| Light Dimmer Compatible | No |
| THD | ~ 16% (LED Voltage 14V) |
| Power Factor | > 95% (LED Voltage 14V) |

## General Description

This Design Notes describes the results of a 14W LED Driver Design. The design specifically forgoes the use of electrolytic capacitors which form a point of weakness in high reliability and high ambient temperature applications.

The design drives one or more high brightness LEDs, in parallel or series combinations, at a current of 1A and up to a voltage of 14V. This same design can be operated at lower voltage / power level as well, with slight loss of efficiency and THD.

The results, in particular the waveforms, documented in this note apply more broadly, i.e. at other output currents and voltage levels when appropriate adjustments are made to the size and value of certain components.

Efficiency can be increased, by using components having less ohmic resistance, particularly L1 and M1, and by lowering of the switching frequency.

The input line current features low harmonic distortion, satisfying the requirements of EN 61000-3-2 Class C (Lighting Equipment). Open circuit and in short circuit at the output can be sustained indefinitely. The AC line current is limited for an input voltage range from zero to 135VAC. Both the output

current and line current drop gradually as AC line voltage falls below 100VAC.

Please refer to application note AN-H52 for a detailed description of and design guidance for the HV9931LED driver control IC.

## Miscellaneous Notes

### EMI, Common Mode Filtering:
The magnitude and frequency dependency of the common mode current on the line input depends heavily on physical layout and location of the LED driver circuit and the attached load. As such the design may or may not require the addition of a common mode choke ahead of the bridge rectifier.

### Open Circuit Operation
During open circuit operation the HV9931 is made to run at minimum duty cycle through the action of CS2 and ZOV. Some energy transfer, as small as it may be, still occurs, which causes the voltage on C1, and thereby the peak drain voltage on M1, to rise to a higher level. Circuit losses keep this raise in check. From experimental data: peak $V_{C1}$ rises by about 35V from 120V to 155V, and maximum $V_{DS}$ rises by 60V from 270V to 330V. If this rise is undesirable, a zener diode or a bleeder resistor can be placed across C1 to limit the voltage rise across C1 and M1, or more sophisticated circuitry can be added to further limit switching activity.

### M1 Turn Off
An external pull down transistor was added to the gate drive circuit to speed up the turn off transition. Note that M1's drain current, which is more or less triangular in shape, is largest at turn off. Figures 19 and 20 illustrate the gain in turnoff speed that can be attained by this simple addition. Measurements showed an increase in efficiency by 0.5% from 73.2% to 73.7%, corresponding to a reduction in switching loss of 100mW. The small gain in efficiency may not warrant the addition of the pull down transistor, but may nevertheless be interesting when power levels are higher or a larger MOSFET having more gate and reverse transfer capacitance is in use.

### VDD at zero crossing
VDD may drop out at the AC line zero crossings, and cause a short

lived drop in LED current , if the capacitor at the VDD pin is made small. If this effect is undesirable, then the CDD should be chosen sufficiently large. Figures 5 and 6 demonstrate this effect.
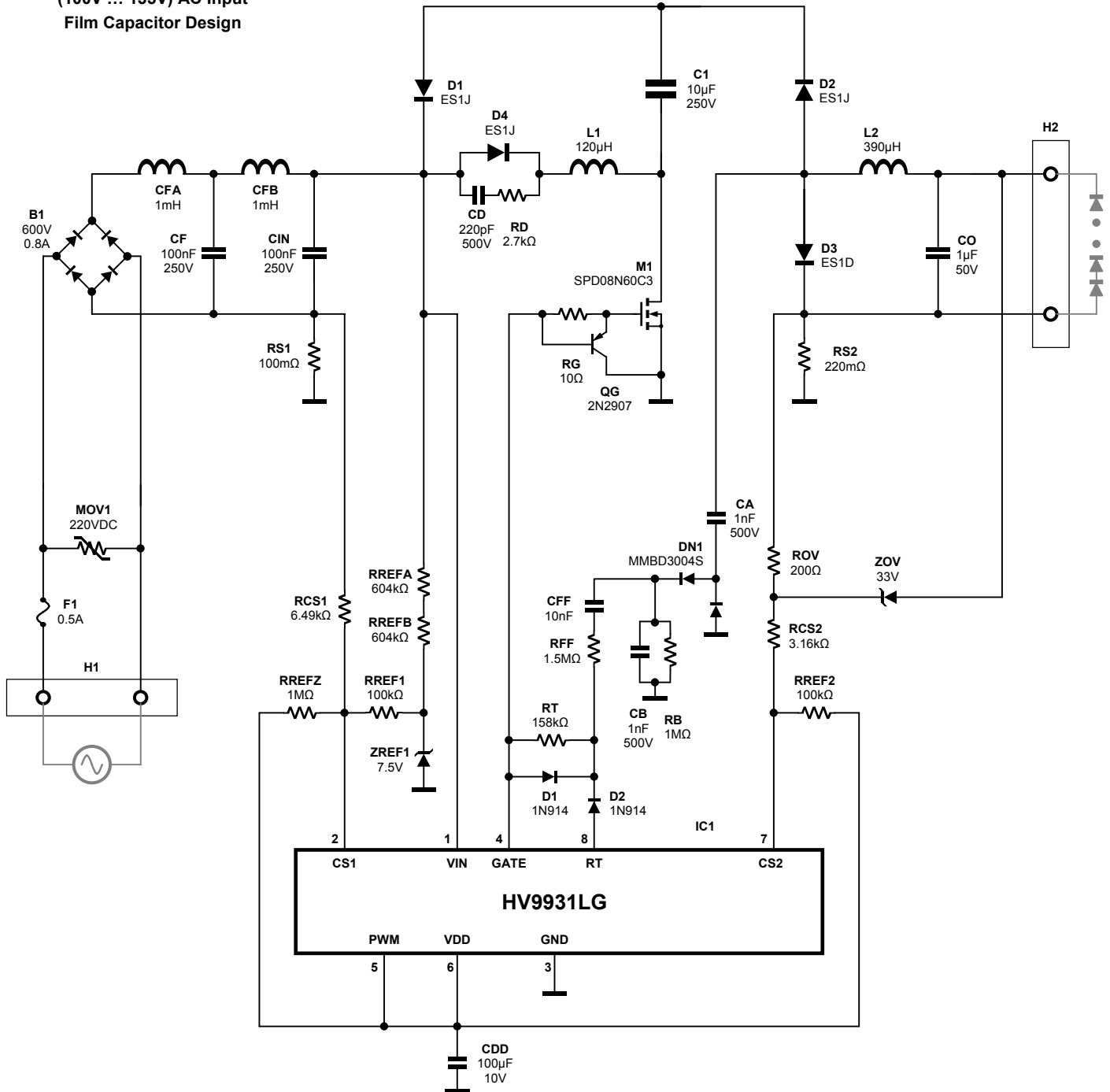
**CS1 Programming**

Control of M1 should, under regular circumstances, be governed by the action of comparator CS2, which provides regulation of the LED current. CS1 should regulate only if limitation of input stage current is necessary, as during AC line undervoltage or during transient conditions. CS1 is to remain inactive by programming an envelope for the input stage current with an adequate margin, such that CS1 does not interfere with the regulation of the output current under normal circumstances. A simple DC threshold of adequate value will suffice. This design employs a somewhat more sophisticated envelope for the purpose of limiting the AC line current when undervoltage occurs. The threshold is a scaled version of the input voltage, thus reducing input current as input voltage reduces. By proper choice of values, CS1 will thus become active for input voltages lower than 100VAC, and take over regulation by limiting input stage current to an approximate sinusoidal waveform. For line voltages larger than 100V, this scaled threshold will become unnecessarily accommodative, and zener diode ZREF1 will limit its rise.

**Diodes D1 and D2**

D1 and D2 are part of the RT oscillator circuit which determines the switching frequency, or more precisely, the off-time ($T_{OFF}$) of the switching period. The off time is determined by the oscillator discharge current which should appear when M1 is turned off, i.e. when the GATE pin is low. The main contribution to the discharge current is due to current in RT when the voltage at the GATE pin is low. Current originating at the RFF resistor is meant to modulate this discharge current in order to affect an increase or decrease of $T_{OFF}$. Note that RFF is driven by the ripple voltage across C1. As such, RFF carries an alternating current, which is present regardless of the timing needs of the RT pin. D1 and D2 resolve two issues depending on the polarity of the RFF current. When RFF sources current, it will overdrive the pin when GATE is high, which is undesirable. Diode D2 blocks this current, and the current will follow an the path through RT and the GATE pin. When RFF sinks current, diode D1 sources this current during the time that the RT discharge current should be zero (GATE pin high).

**Supertex inc.**

**HV9931DN14A**

**(14V, 1A) LED Driver**
**(100V ... 135V) AC Input**
**Film Capacitor Design**

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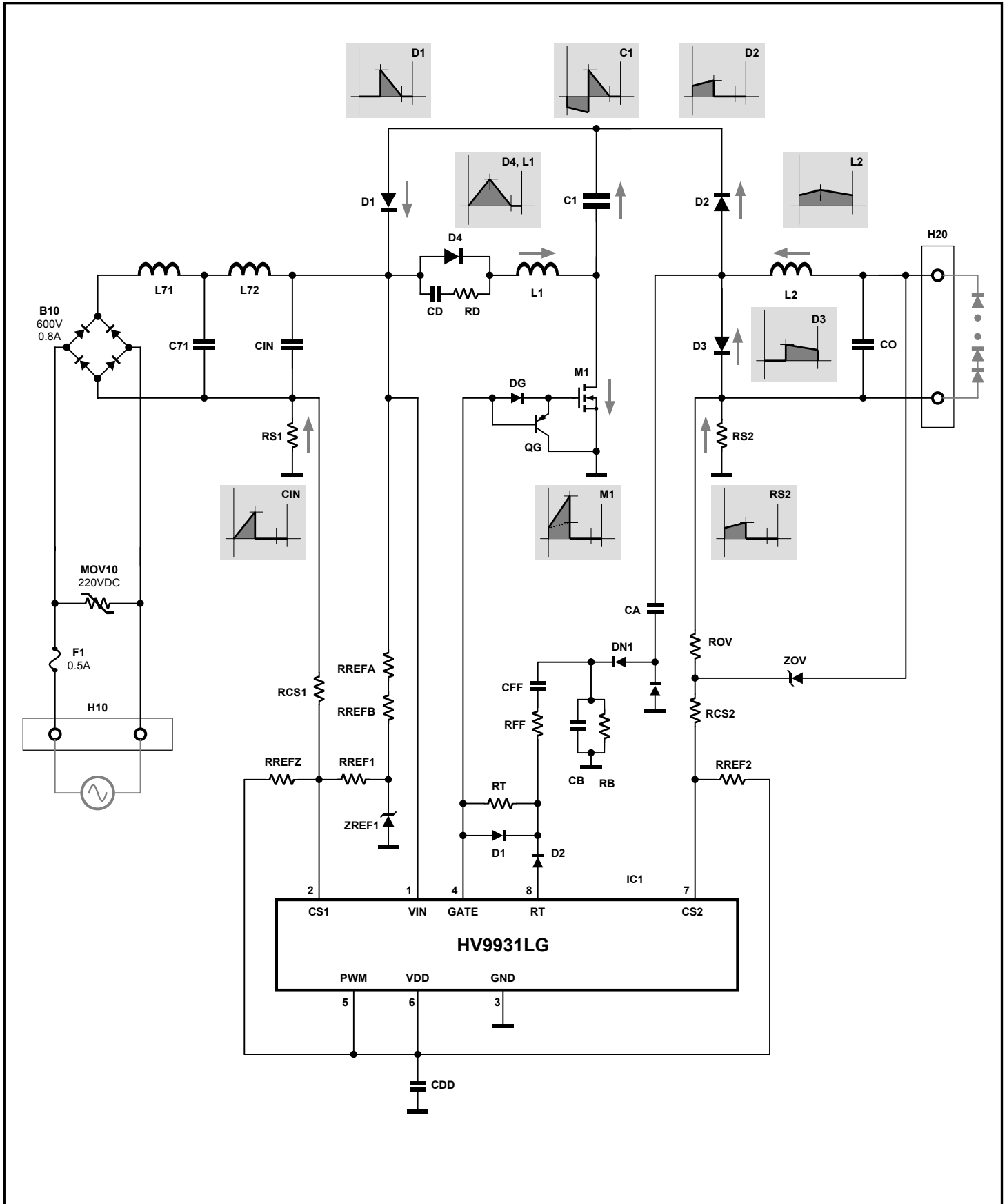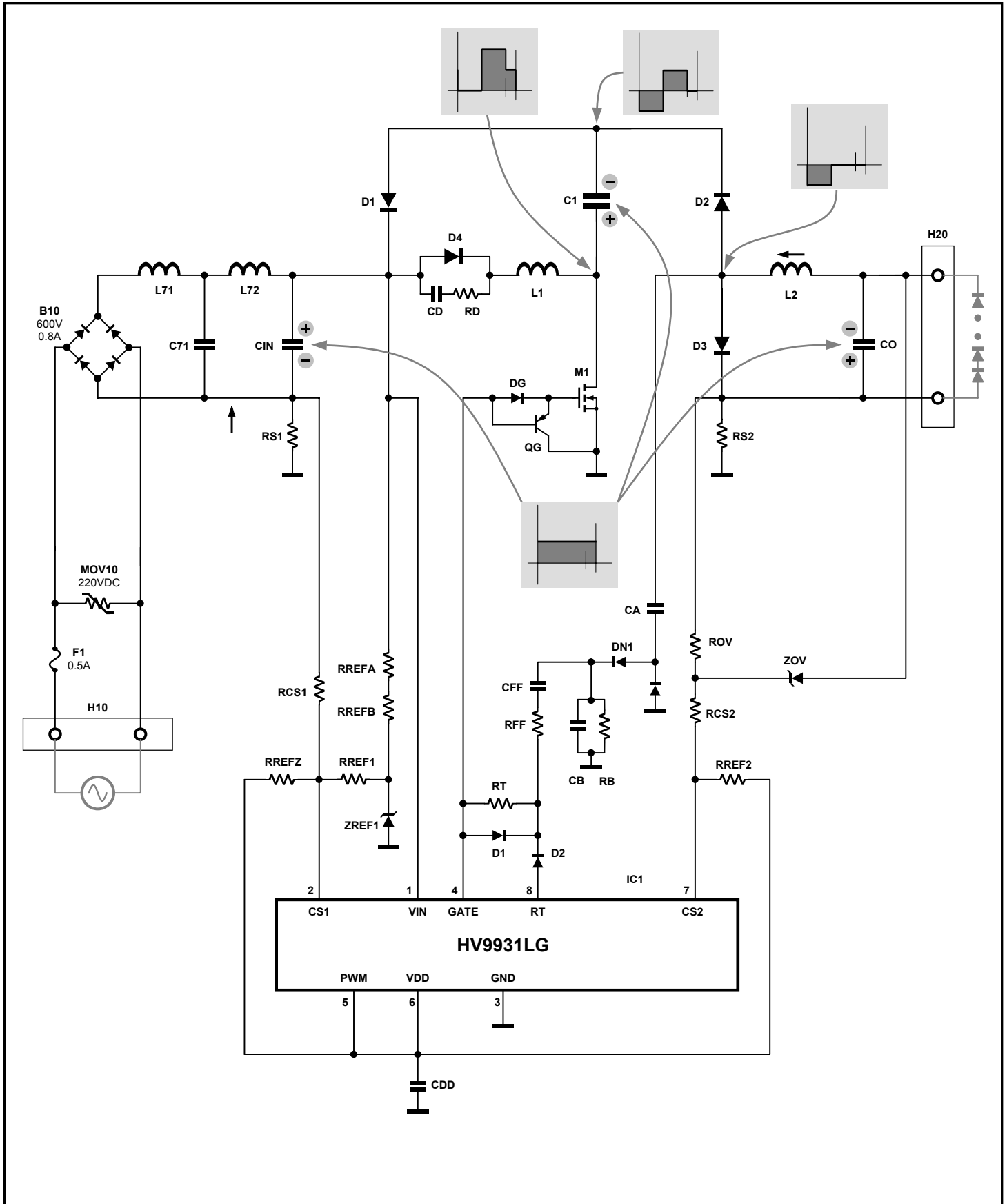
**Fig 1.   (V$_{AC}$, I$_{AC}$), Nominal (120V)**



THD:     15.3%

**Fig 2.   (V$_{AC}$, I$_{AC}$), Low Line (100V)**



THD:     22.5%
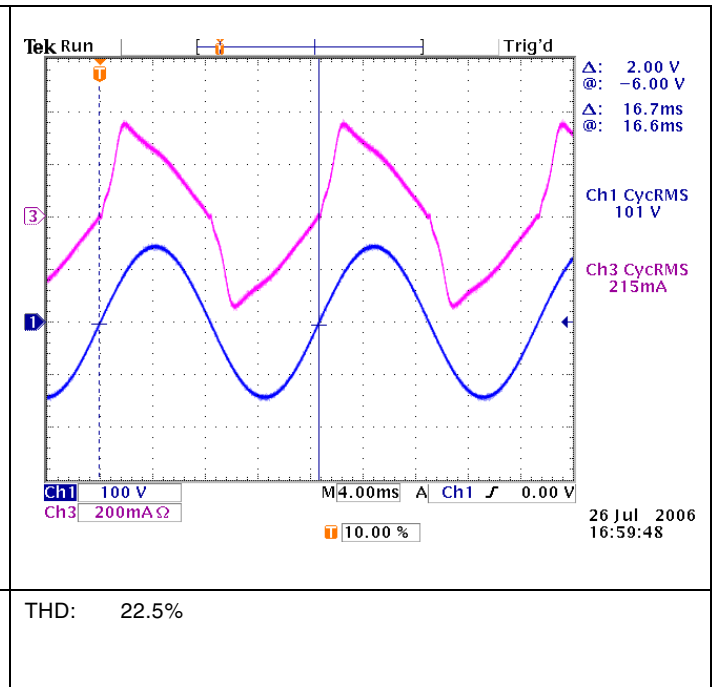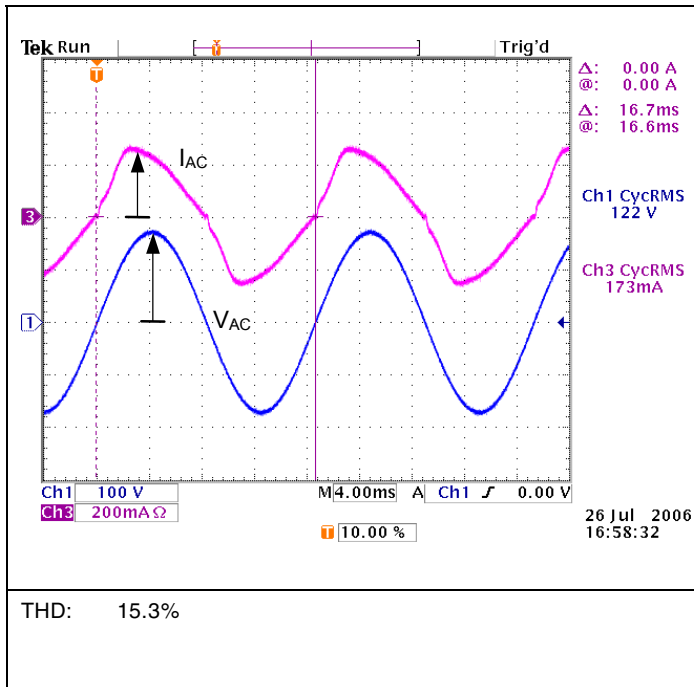
**Fig 3.   (V$_{AC}$, I$_{AC}$), High Line (135V)**



THD:     9.2%

**Fig 4.   V$_{AC}$ and I$_{AC}$, Undervoltage (90V)**



THD:     35.6%
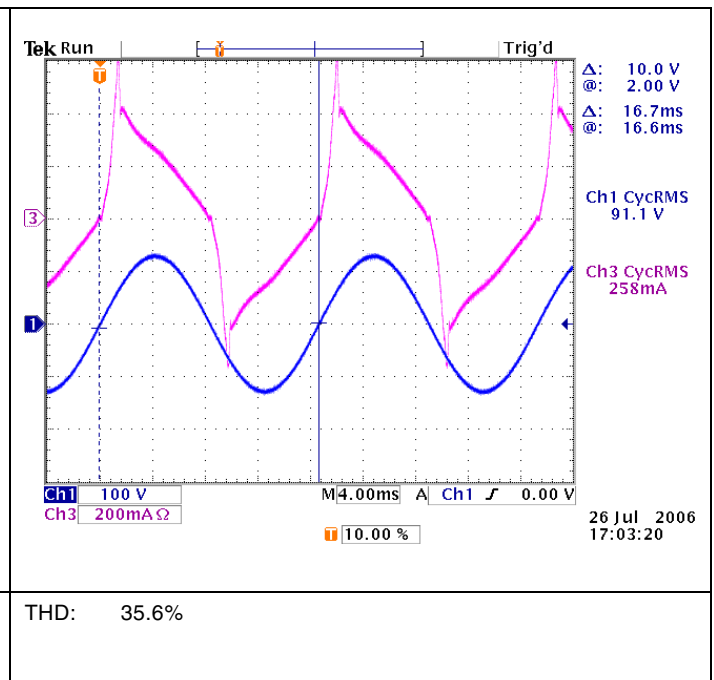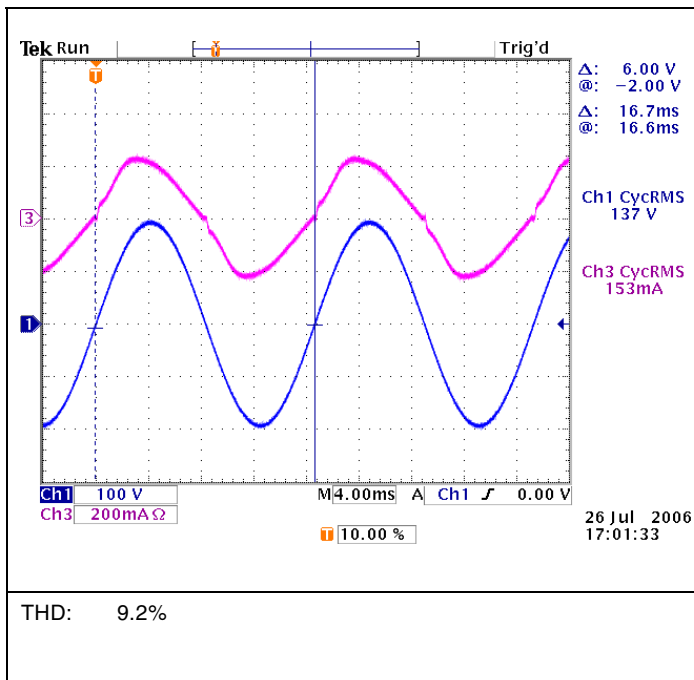
## Fig 5.  $V_{DD}$, $I_{LED}$ with Large $C_{DD}$ (100µF)



## Fig 6.  $V_{DD}$, $I_{LED}$ with Small $C_{DD}$ (1µF)
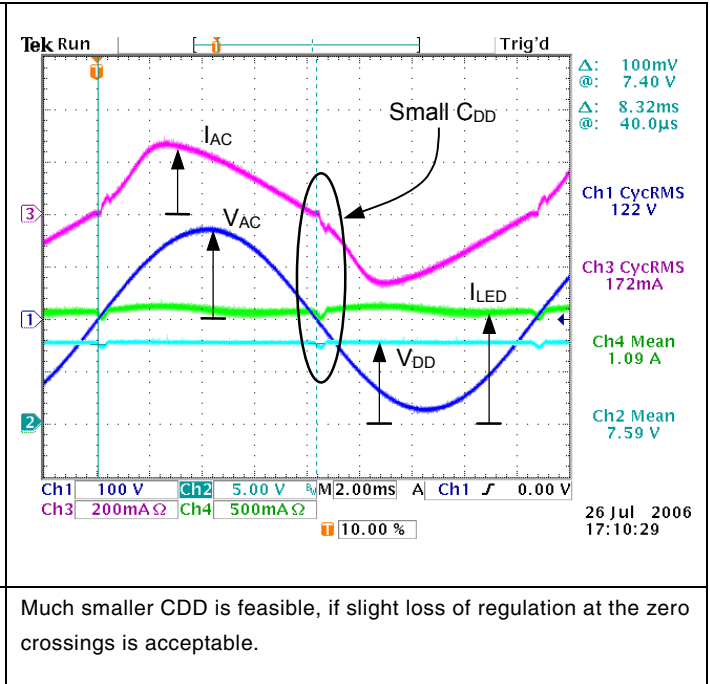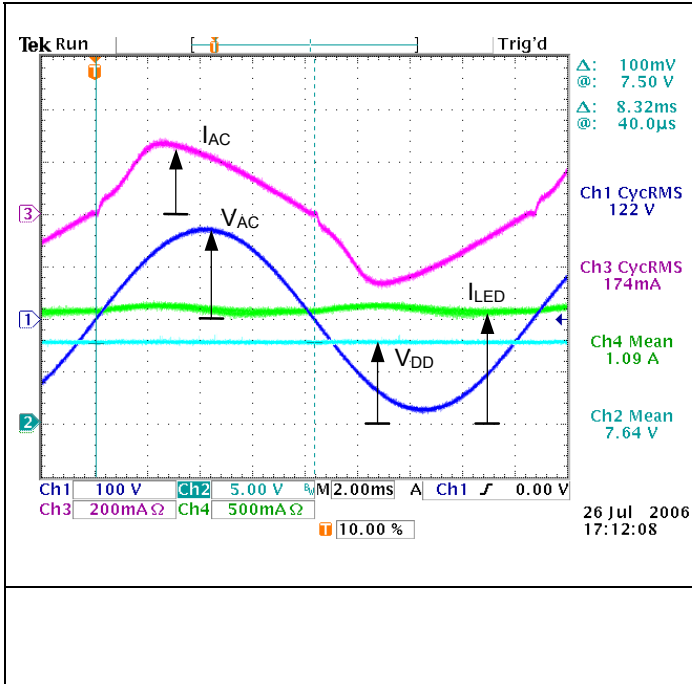


Much smaller CDD is feasible, if slight loss of regulation at the zero crossings is acceptable.

## Fig 7.  ($V_{AC}$, $I_{AC}$), $R_{FF}$ Removed, Low Line



THD:    Increases to 54.1% (from 22.5%)

## Fig 8.  ($V_{AC}$, $I_{AC}$), $R_{FF}$ Removed, Nominal



THD:    Increases to 31.5% (from 15.3%)

Fig 9.   (I$_{LED}$, I$_{AC}$, V$_{AC}$) when R$_{REFZ}$ Removed



R$_{REF3}$ is needed to prevent loss of I$_{LED}$ regulation at the zero crossings,  where CS1 not receive adequate bias from V$_{IN}$.
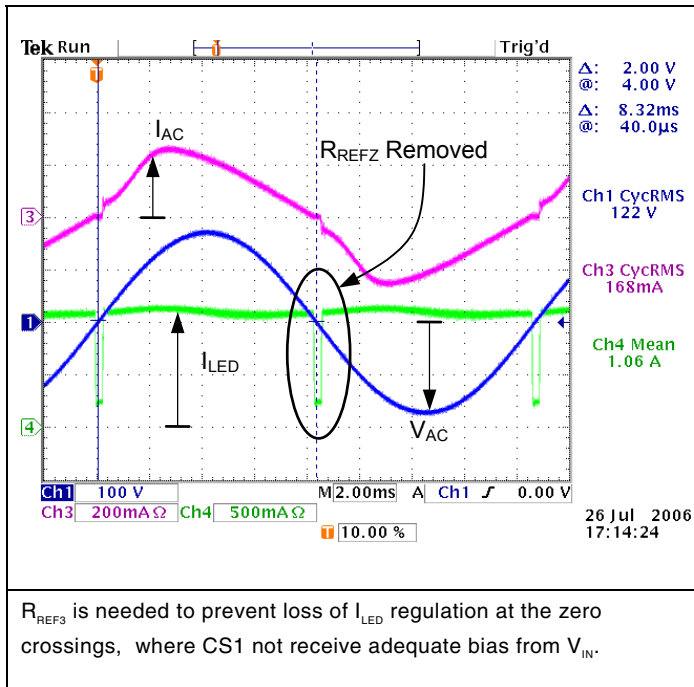
Fig 10. (V$_{IN}$, V$_{C1}$, I$_{L1}$) Detail, (2ms/div)
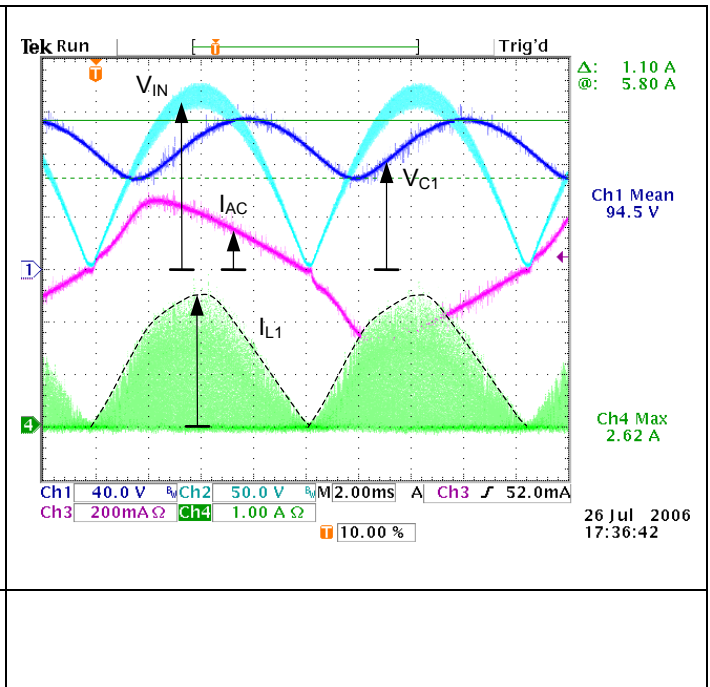


Fig 11. (V$_{IN}$, V$_{C1}$, I$_{L1}$) Detail, (1ms/div)
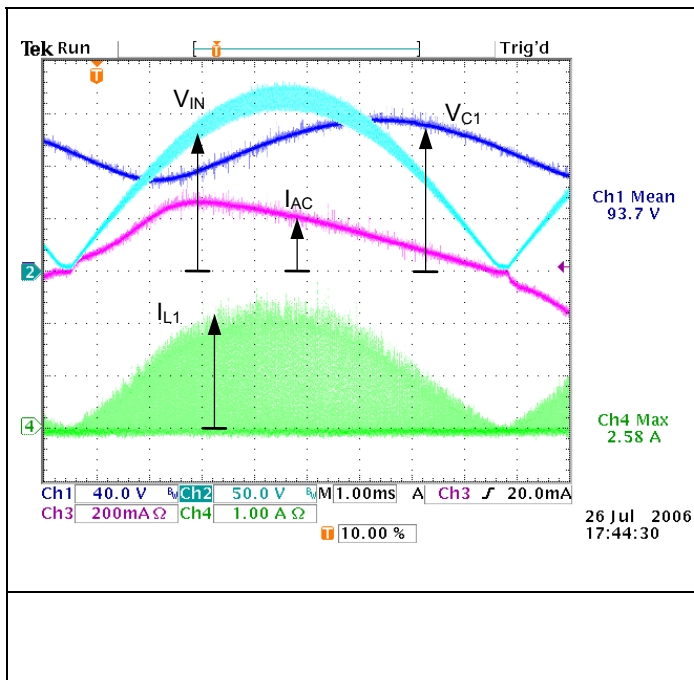


Fig 12. (V$_{IN}$, I$_{AC}$, I$_{L1}$) Detail, (100µs/div)
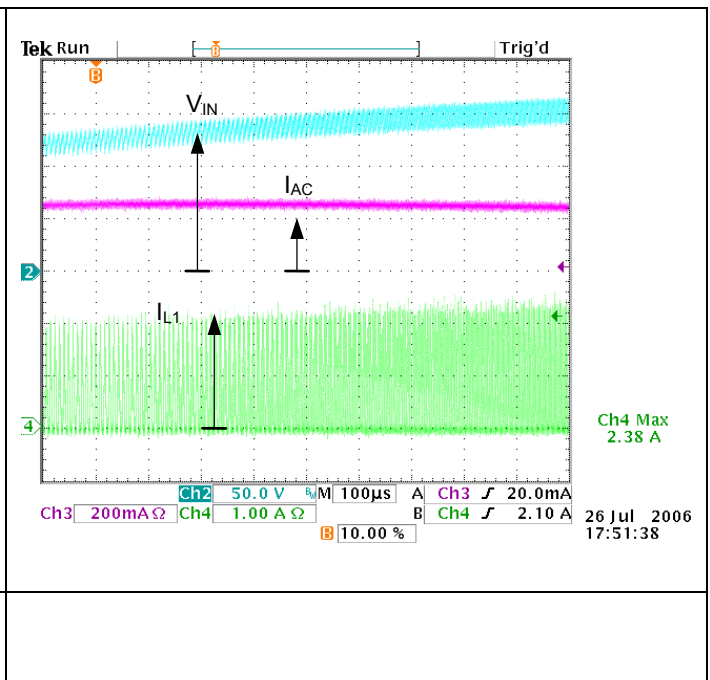
**Fig 13. (V$_{IN}$, I$_{AC}$, I$_{L1}$) Detail, (10µs/div)**
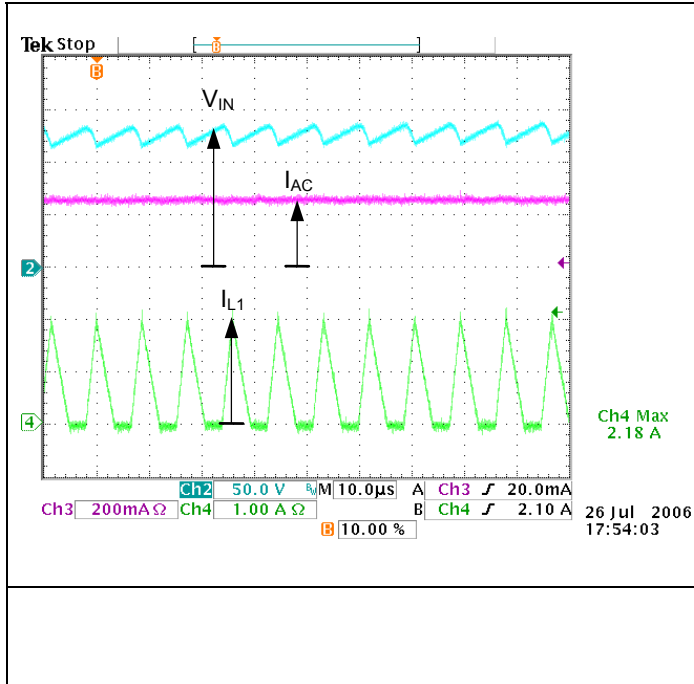
**Fig 14. (V$_{IN}$, I$_{AC}$, I$_{L1}$) Detail, Time Base (2µs/div)**
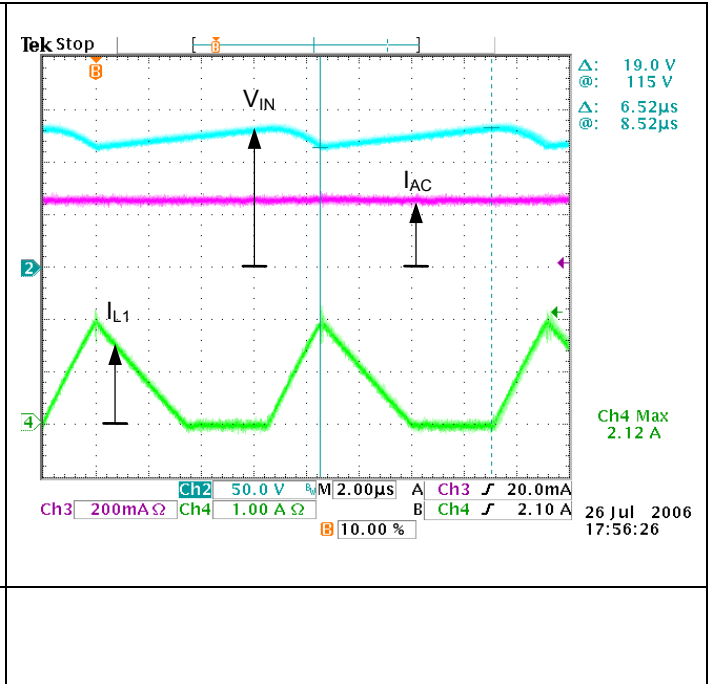




**Fig 15. M1 Drain Voltage, (2µs/div)**
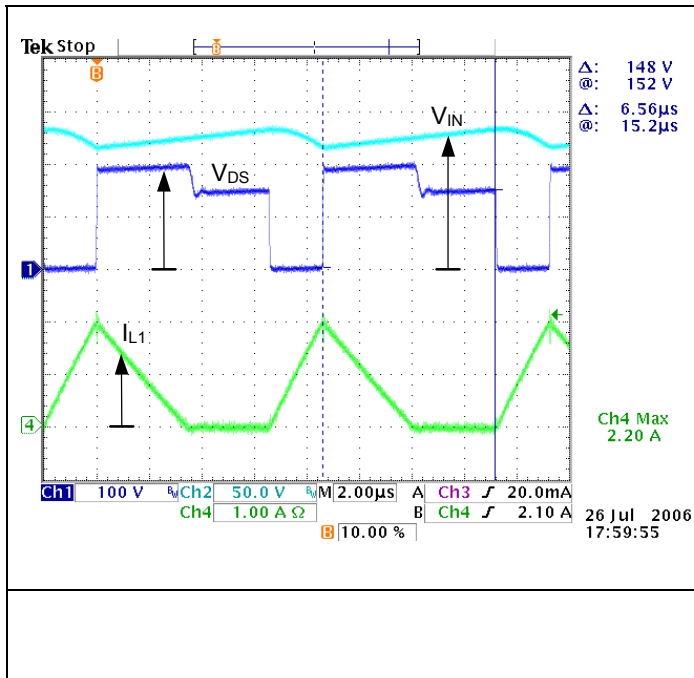
**Fig 16. M1 Drain Voltage, (20µs/div)**





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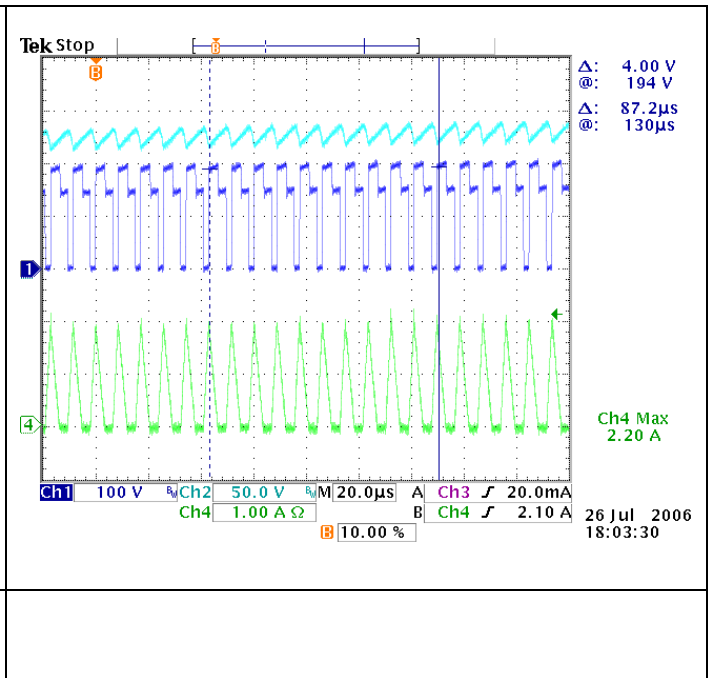
**Fig 17. M1 Drain Voltage, (2ms/div)**
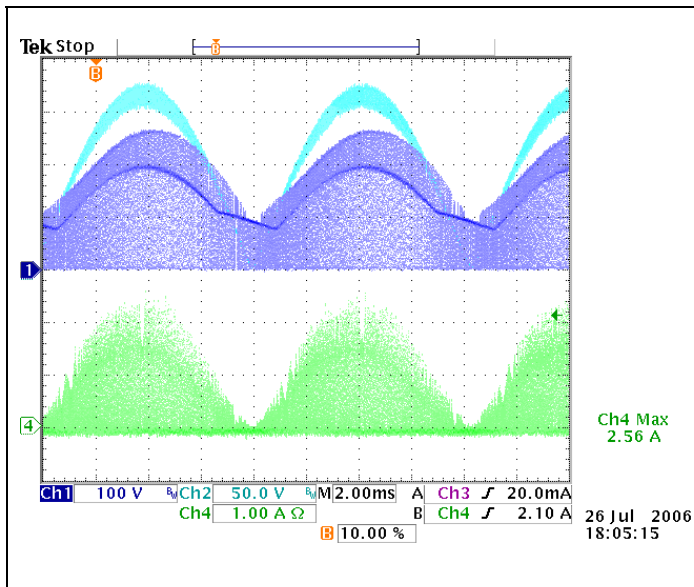
**Fig 18. M1 Turn on**
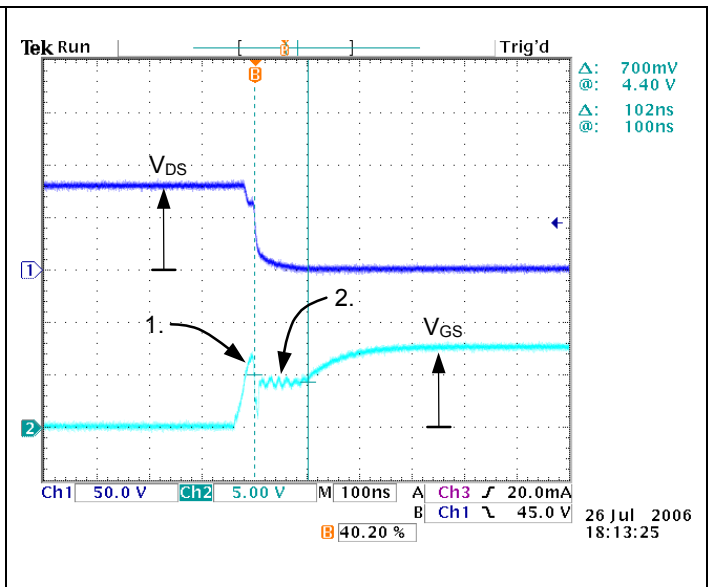




1.  $V_{GS}$ rises steadily;  Diode D3 recovers.
2.  $V_{GS}$ plateaus; Miller effect due to falling VDS.

**Fig 19. M1 Turn Off**

**Fig 20. M1 Turn Off,  Q1 Removed**
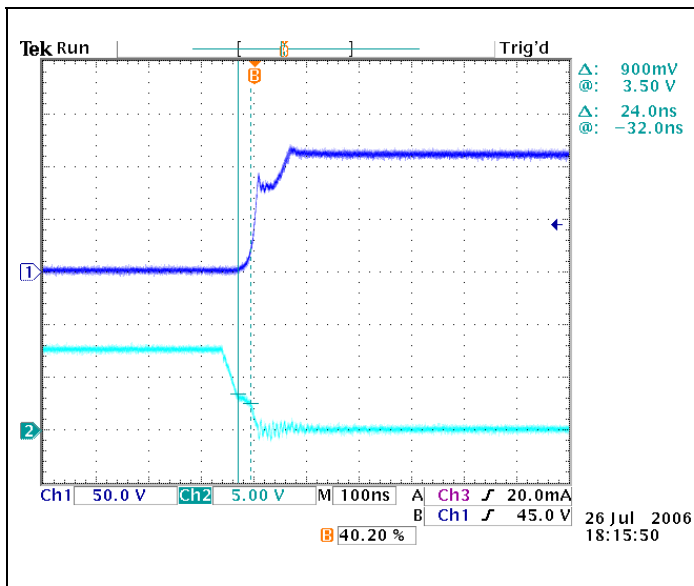




$V_{GS}$ plateau about 25ns.

Gate Turn-off assisted by external PNP Pull Down Transistor
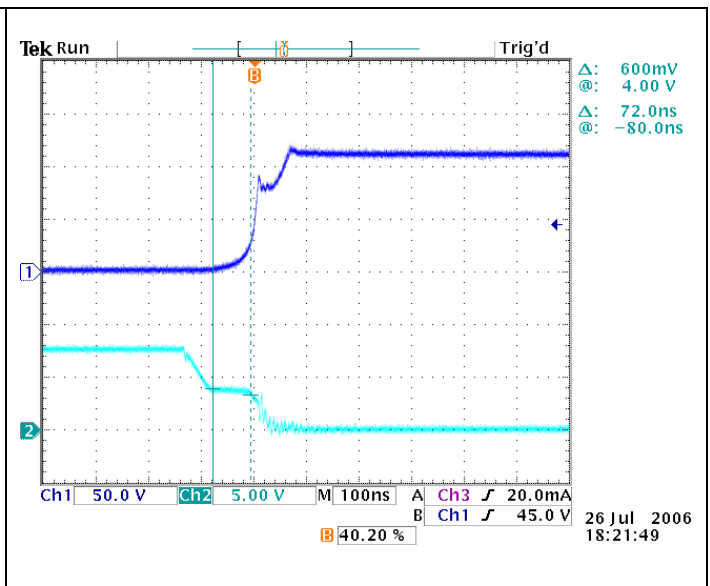
$V_{GS}$ plateau about 70ns.

Pull Down Transistor Q1 Removed, and Zero Ohm RG.

**Fig 21. Input Filter Detail, ($V_{IN}$, $V_{BR}$, $I_{BR}$)**       **Fig 22. CS1 Programming Detail, $V_{ZREF1}$**
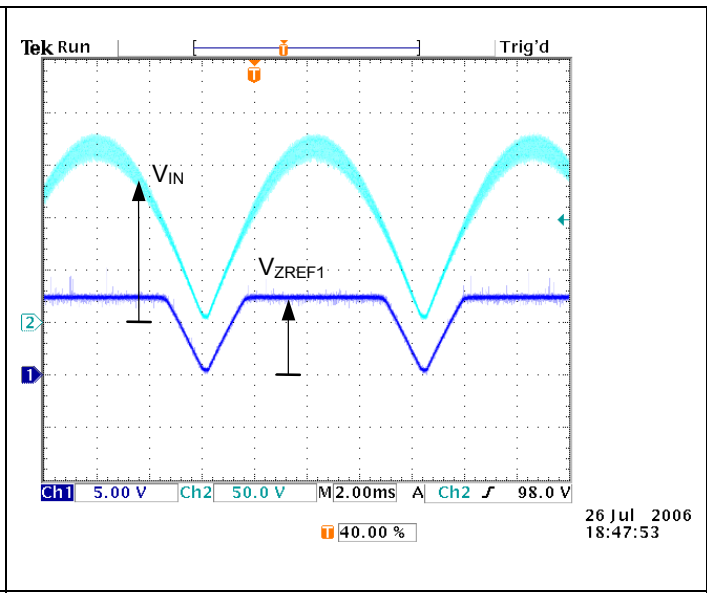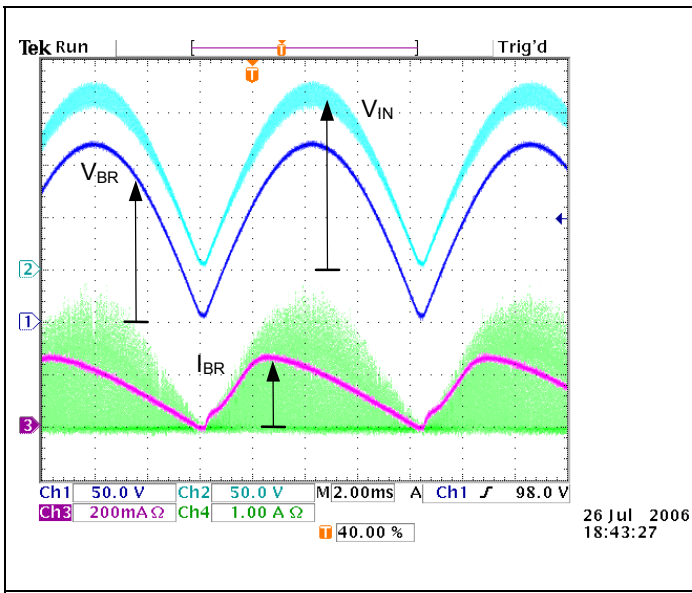


No ripple visible on $V_{BR}$;  Filter rejects voltage ripple of $V_{IN}$.

No Ripple visible on $I_{BR}$;  Filter rejects current ripple of $I_{L1}$.



Limit defined in part by DC level, in part by $V_{IN}$.
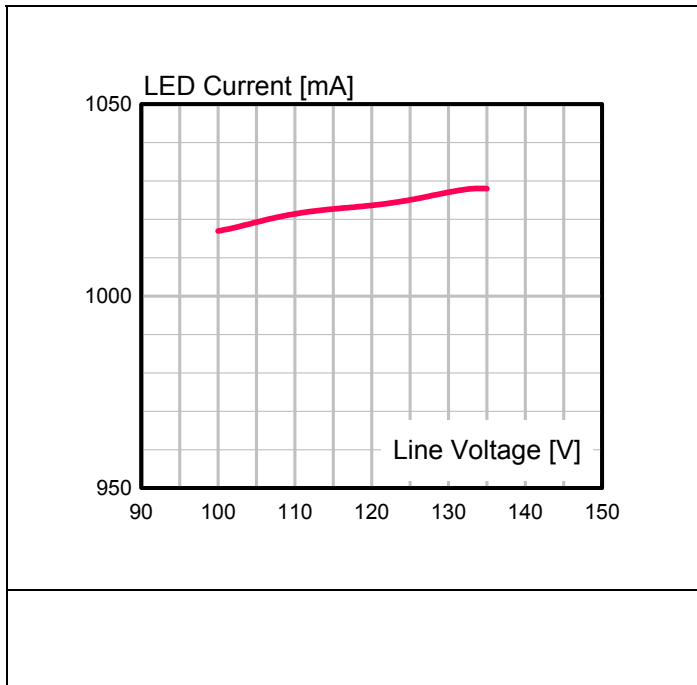
Limit never exceeds DC level,

**Fig 23. Line Regulation**
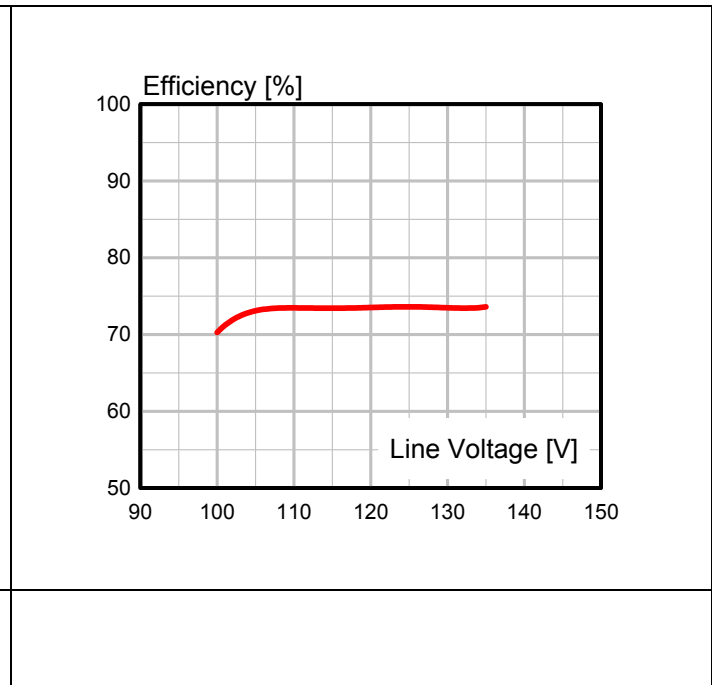


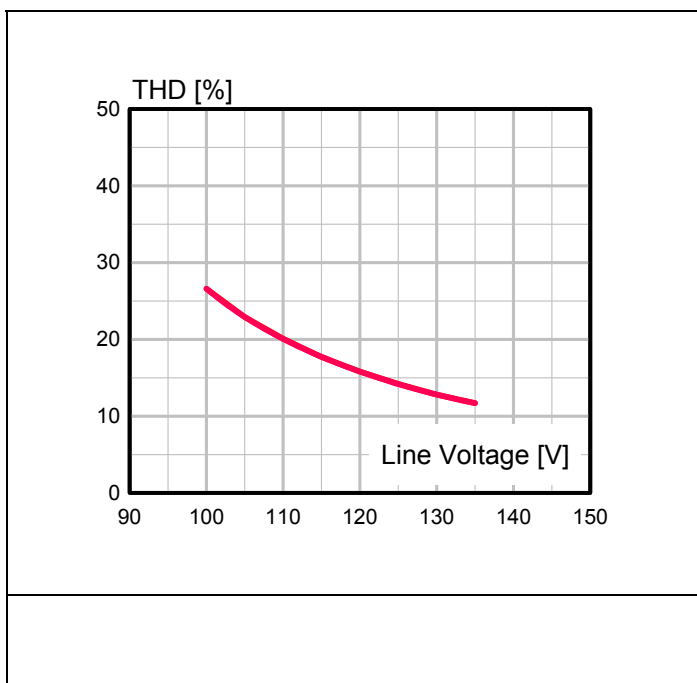**Fig 24. Efficiency vs Line Voltage**



**Fig 25. THD vs Line Voltage**



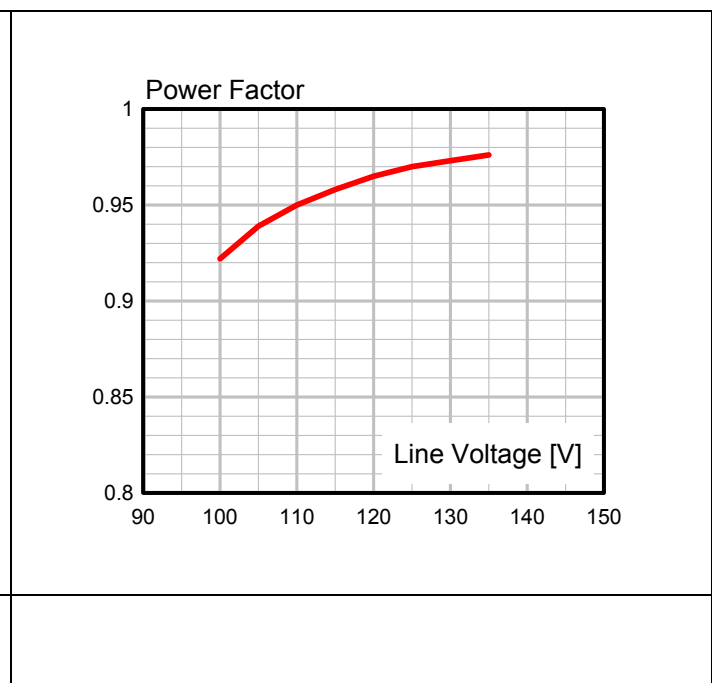**Fig 26. Power Factor vs Line Voltage**

**Fig 27. Load Regulation**



**Fig 28. Efficiency  vs  Load Voltage**



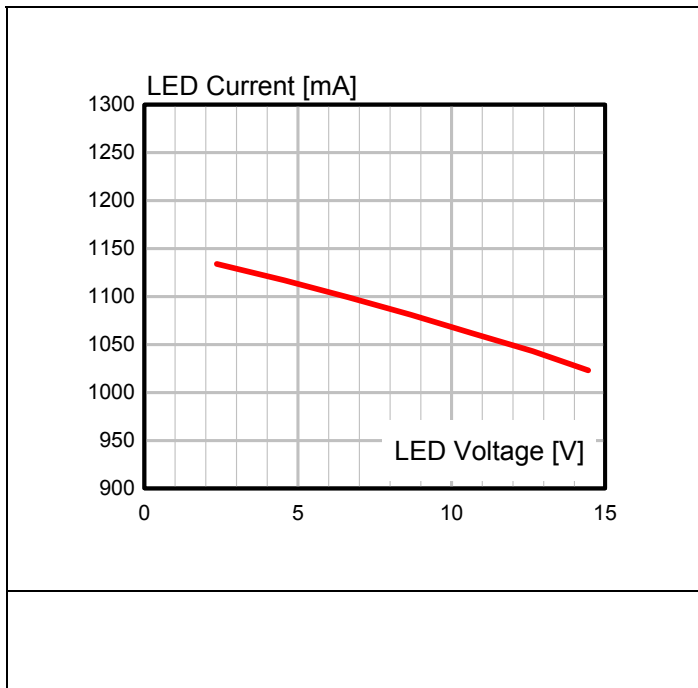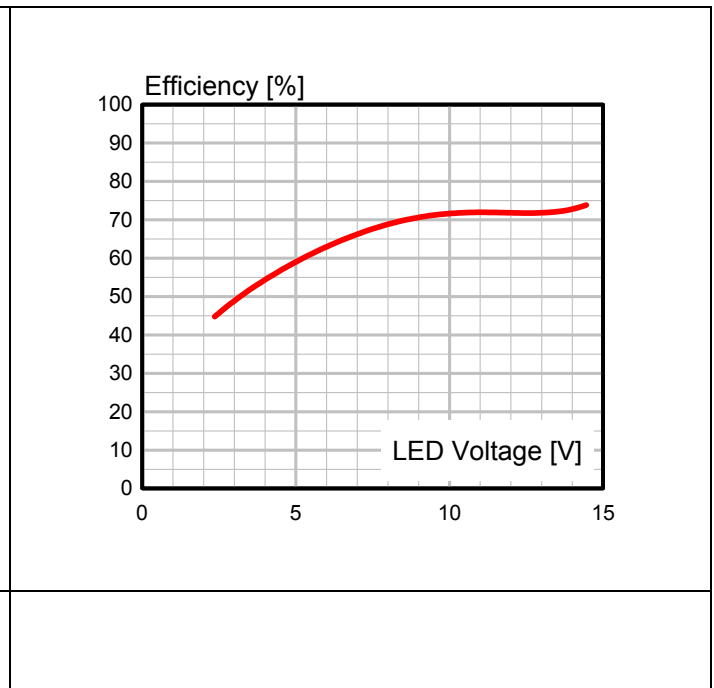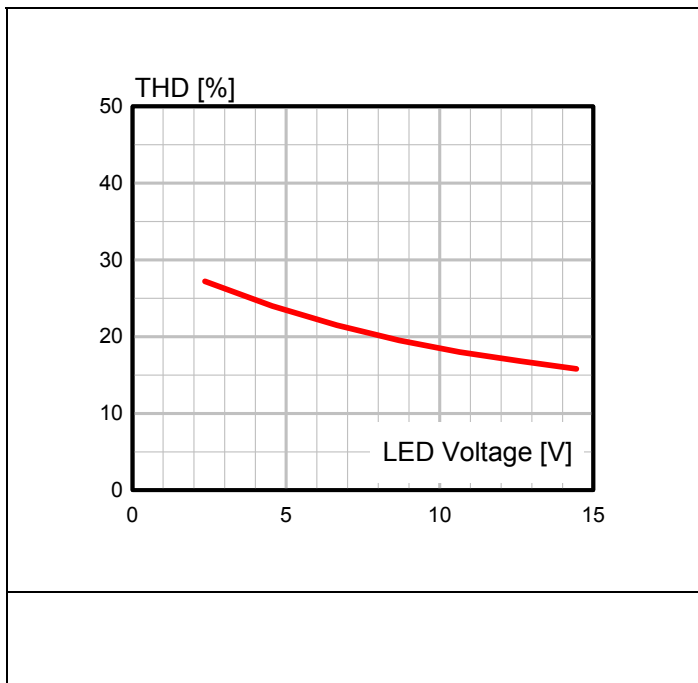**Fig 29. THD  vs  Load Voltage**



**Fig 30. Power Factor  vs  Load Voltage**