Single-Inductor, Multiple-Output (SIMO) Regulator for AMOLED

FEATURES

- 2.3-V to 5.5-V Input Voltage Range
- 1% Output Voltage Accuracy
- Low-Noise Operation
- 750-mW Output Power at V_{in} = 2.9 V
- SIMO Regulator Technology
- Fixed 4.6-V Positive Output Voltage
- Negative Output Voltage Down to –6 V
- Advanced Power-Save Mode for Light-Load Efficiency
- Out-of-Audio Mode
- Short-Circuit Protection
- Excellent Line Regulation
- Thermal Shutdown
- 3-mm × 3-mm Thin QFN Package

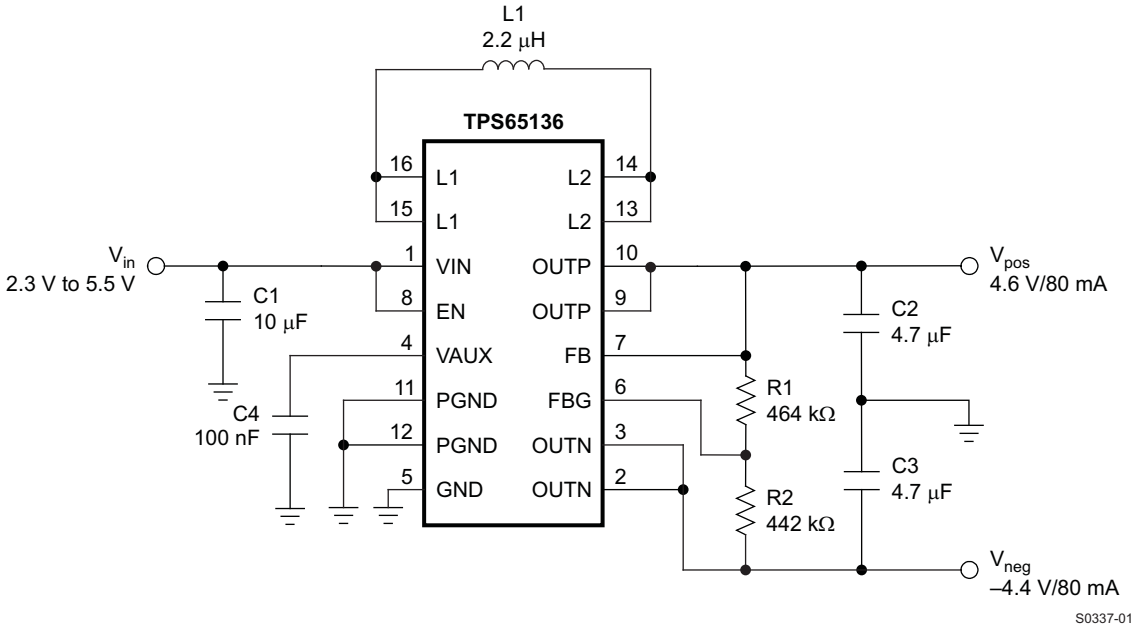
APPLICATIONS

- Active-Matrix OLED Power Supply

DESCRIPTION

The TPS65136 is designed to provide best-in-class picture quality for active-matrix OLED (AMOLED) displays that require positive and negative supply rails. With its wide input voltage range, the device is ideally suited for AMOLED displays, which are used in mobile phones or SmartPhone™ devices. With the new single-inductor multiple-output (SIMO) technology, the smallest possible solution size is achieved. The device operates with a buck-boost topology and generates both positive and negative output voltages above or below the input voltage rail. The SIMO technology enables excellent line and load regulation. Excellent line-transient regulation is required to avoid disturbance of the AMOLED display as a result of input voltage variations that occur during transmit periods in mobile communication systems.

TYPICAL APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

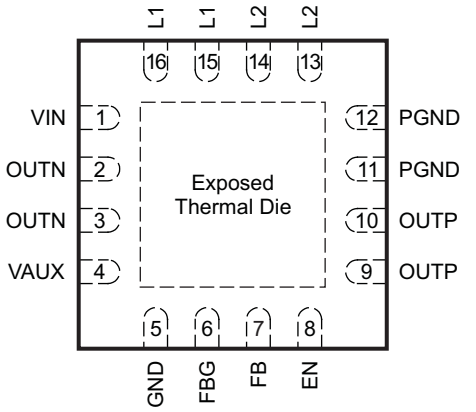
ORDERING INFORMATION(1)

T_A	OPTIONS	ORDERING P/N	PACKAGE	PACKAGE MARKING
–40°C to 85°C	4.6 V fixed(2)	TPS65136RTE	RTE	CCO

(1) The RTE package is available in tape and reel. Add R suffix (TPS65136RTER) to order quantities of 3000 parts per reel. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Contact the factory for other output voltage options.

16-Terminal TQFN PACKAGE

RTE Package
(Top View)



P0081-01

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	Input pin to enable the device. Pulling this pin high enables the device. This pin has an internal 500-kΩ pulldown resistor.
FB	7	I	Feedback regulation input for the positive output voltage rail
FBG	6	I	Feedback regulation input
GND	5	–	Analog ground
L1	13, 14	I/O	Inductor terminal
L2	15, 16	I/O	Inductor terminal
OUTN	2, 3	O	Negative output
OUTP	9, 10	O	Positive output
PGND	11, 12	–	Power GND
VAUX	4	O	Reference voltage output. This pin requires a 100-nF capacitor for stability.
VIN	1	I	Input supply
Exposed thermal die		–	Connect this pad to analog GND.

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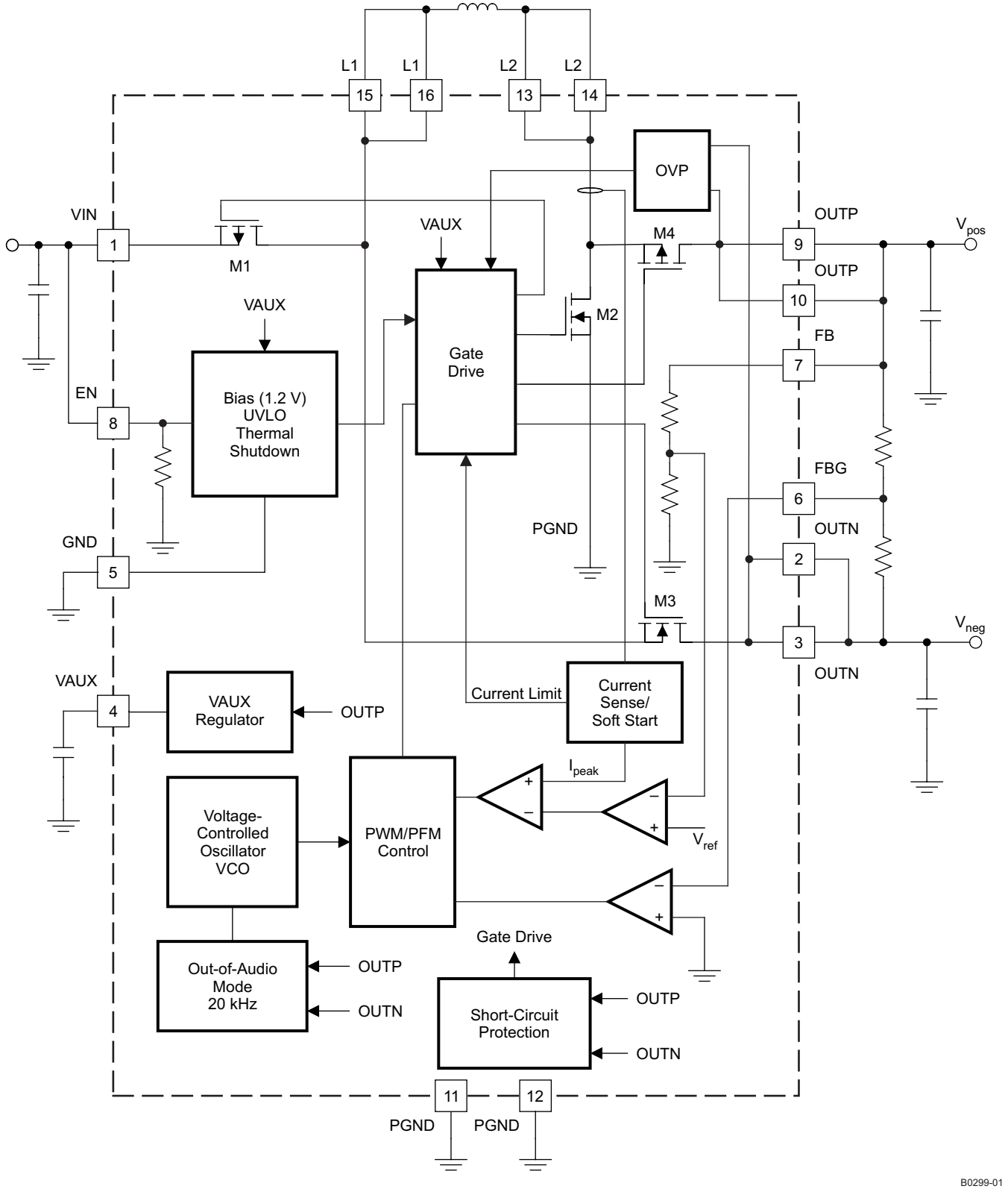
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
	Input voltage range VIN(2)	–0.3 to 7	V
	Voltage range at EN	–0.3 to 7	V
	Voltage range at L1, OUTN	–8 to 7	V
	Voltage range at FBG	–0.5 to 0.5	V
	Voltage range at L2, OUTP, FB	–0.3 to 7	V
	ESD rating, HBM	2	kV
	ESD rating, MM	200	V
	ESD rating, CDM	1	kV
	Continuous total power dissipation	See Dissipation Ratings Table	
T_J	Operating junction temperature range	–40 to 150	°C
T_A	Operating ambient temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$(1)	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RTE	40°C/W	2.5 W	1.37 W	1 W

(1) Thermal resistance measured on a printed circuit board using thermal vias.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{in}	Input voltage range	2.3		5.5	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{in} = 3.7 V, EN = VIN, OUTP = 4.6 V, OUTN = –5.4 V, T_A = –40°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{in}	Input voltage range		2.3		5.5	V
I_Q	Operating quiescent current into V_{in}			1.7		mA
I_{SD}	Shutdown current into V_{in}			0.1	2	µA
V_{UVLO}	Undervoltage lockout threshold	V_{in} falling		1.8	2	V
		V_{in} rising		2	2.3	
	Thermal shutdown			140		°C
	Thermal shutdown hysteresis			5		°C
ENABLE						
V_H	Logic high-level voltage	V_{in} = 2.5 V to 5.5 V	1.2			V
V_L	Logic low-level voltage	V_{in} = 2.5 V to 5.5 V			0.4	V
R	Pulldown resistor			500		kΩ
OUTPUT						
OVP_P	Positive overvoltage protection	I_{out} = 10 mA	5.5	7		V

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ELECTRICAL CHARACTERISTICS (continued)

V_{in} = 3.7 V, EN = VIN, OUTP = 4.6 V, OUTN = –5.4 V, T_A = –40°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{outn}	Negative output voltage range		–2.5		–6	V
OVP_N	Negative overvoltage protection			–7.6	–6	V
I_{mis}	Output current mismatch V_{pos}/V_{neg}		–30%		30%	
V_{outp}	Positive output voltage regulation		4.554	4.6	4.646	V
t_{dly}	Sequencing delay	V_{pos} start to V_{neg} start	6	8.7	11	ms
V_{FBG}	Feedback ground regulation		–10	0	10	mV
$r_{DS(on)}$	M1 MOSFET on-resistance	I_{sw} = 100 mA		200		mΩ
	M2 MOSFET on-resistance	I_{sw} = 100 mA		400		
	M3 MOSFET on-resistance	I_{sw} = 100 mA		900		
	M4 MOSFET on-resistance	I_{sw} = 100 mA		600		
I_{SW}	Switch current limit (M2)	V_{in} = 3.7 V	620	700	940	mA
		V_{in} = 2.5 V	720	830	1120	
P_{out}	Output power	$V_{pos} – V_{neg} \le 10$ V; V_{in} = 2.9 V	750			mW
f_s	Switching frequency	I_{out} neg = I_{out} pos = 30 mA		1		MHz
		I_{out} neg = I_{out} pos = 0 mA		40		kHz
Vo_{low}	Output pulldown voltage(1)	EN = GND, I_{out} neg = I_{out} pos = 1 mA		1		V
	Line regulation positive output OUTP	I_{out} neg = I_{out} pos = 5 mA		0		%/V
	Line regulation negative output OUTN	I_{out} neg = I_{out} pos = 5 mA		0.008		%/V
	Load regulation positive output OUTP	V_{in} = 3.7 V		0.27		%/A
	Load regulation negative output OUTN	V_{in} = 3.7 V		0.25		%/A

(1) The device actively pulls down the outputs during shutdown. The value specifies the output voltage as a current is forced into the outputs during shutdown.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency	vs load current (2.2 µH)	Figure 1
Efficiency	vs load current (4.7 µH)	Figure 2
Operation at light load current	DCM operation	Figure 3
Operation at high load current	CCM operation	Figure 4
Line transient response	I_{out} = 30 mA	Figure 5
Line transient response	I_{out} = 50 mA	Figure 6
Start-up		Figure 7
Switching frequency	vs load current	Figure 8
Quiescent current	vs input voltage	Figure 9
Maximum output current	2.2 µH, LPS3008-222	Figure 10
Maximum output current	2.2 µH, LPF3010-2R2	Figure 11
Maximum output current	4.7 µH, LPS3008-472	Figure 12
Maximum output current	4.7 µH, LPF3010-4R7	Figure 13

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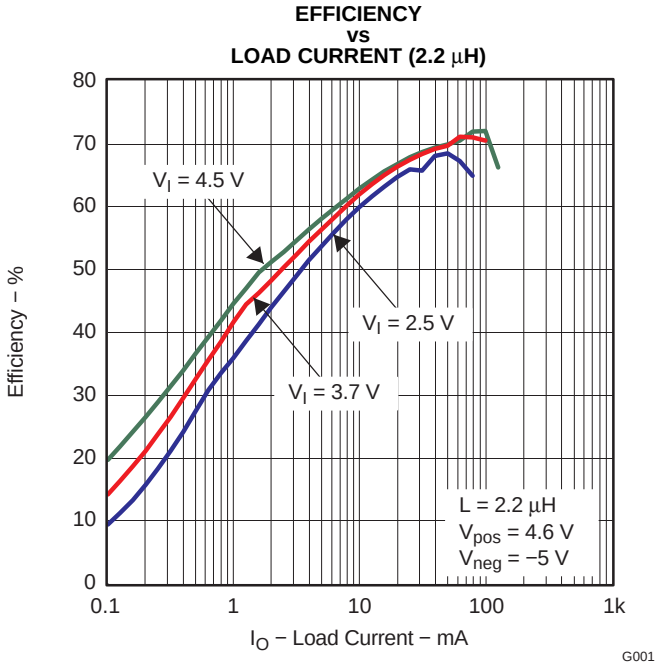

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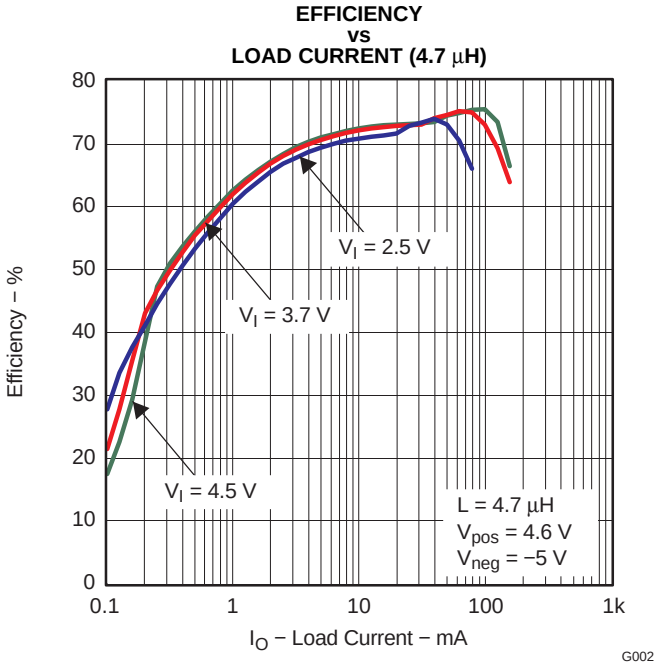

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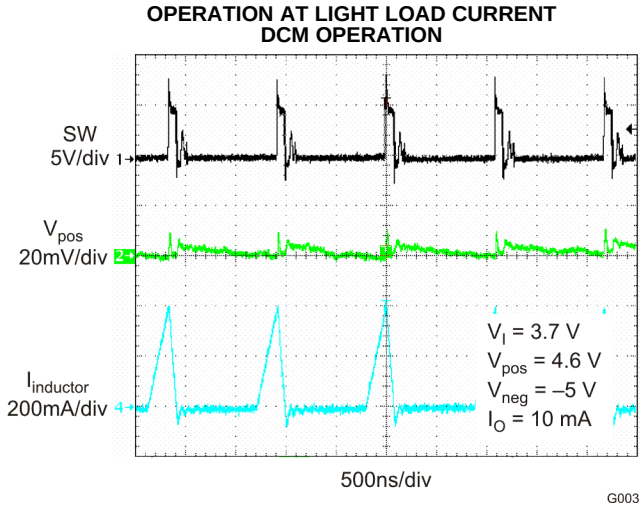

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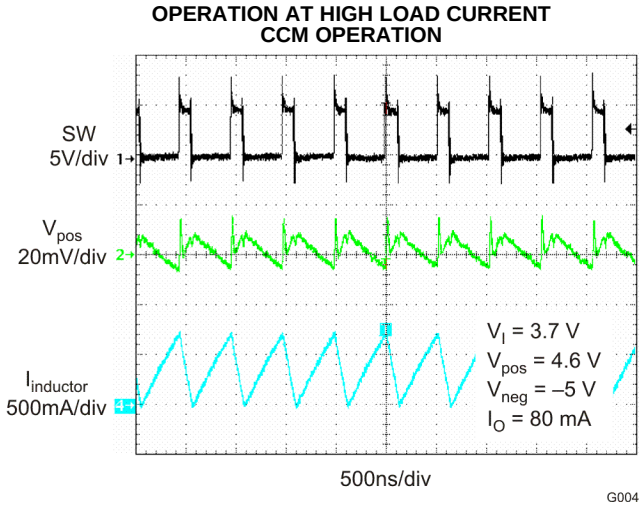

Figure 4.

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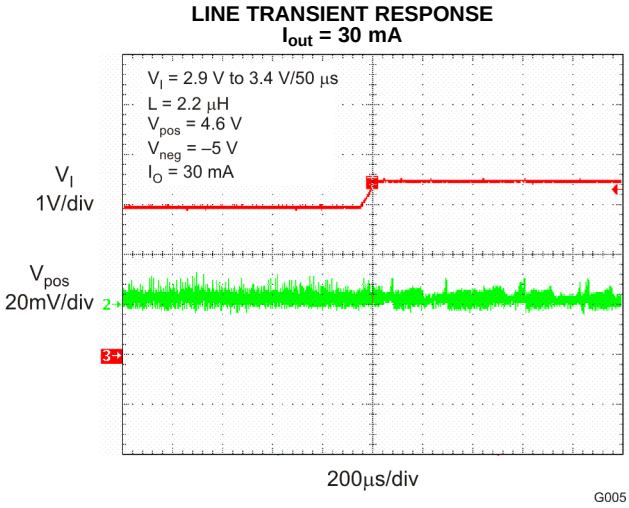

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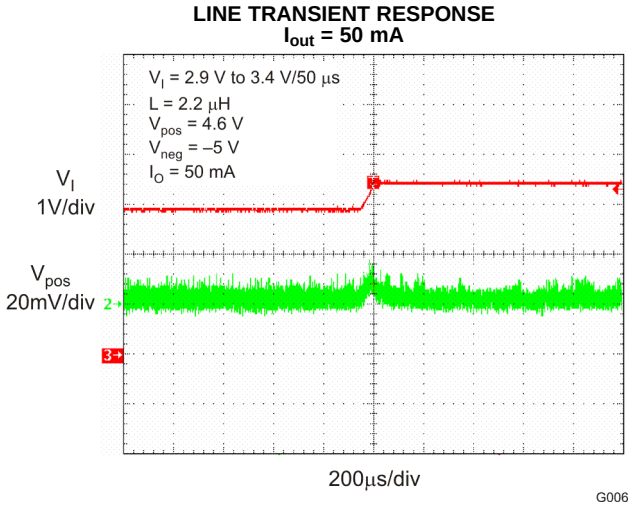

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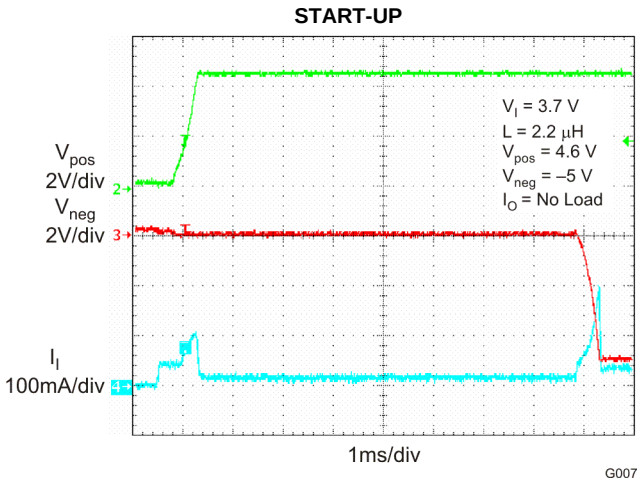

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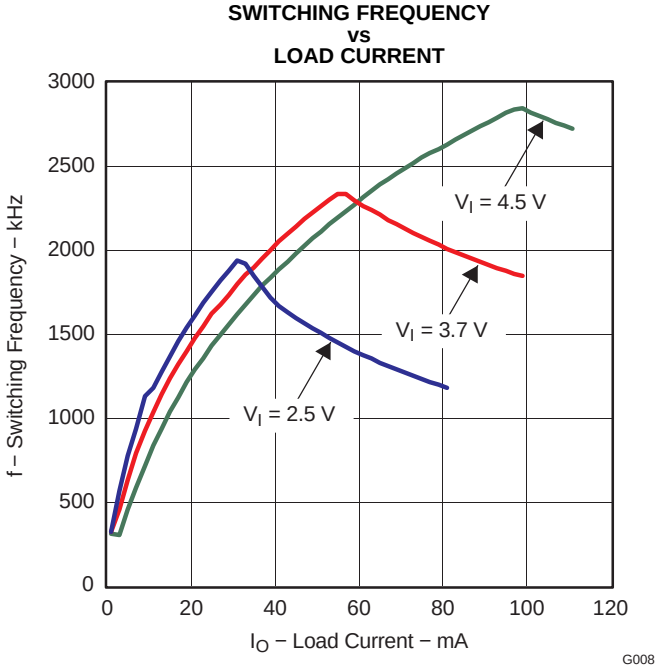

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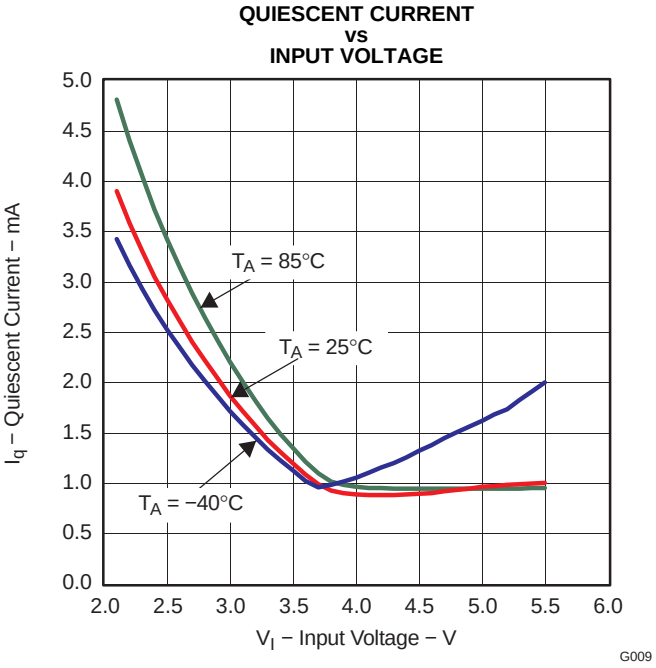

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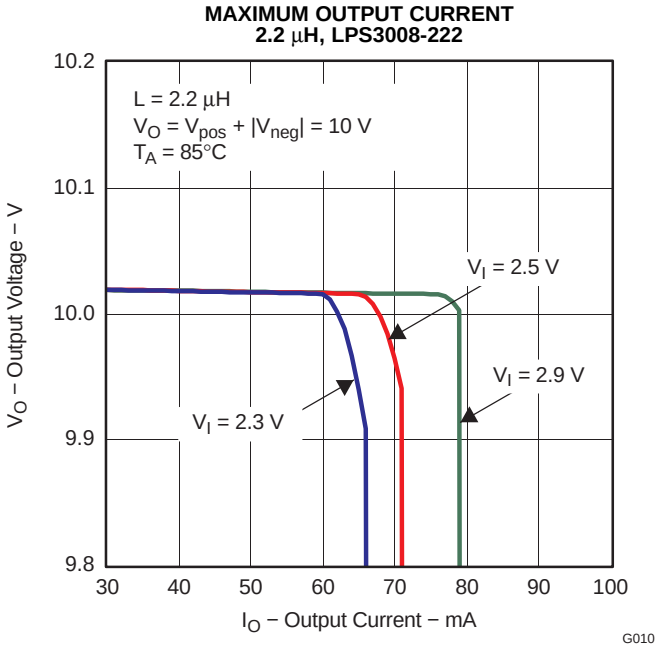

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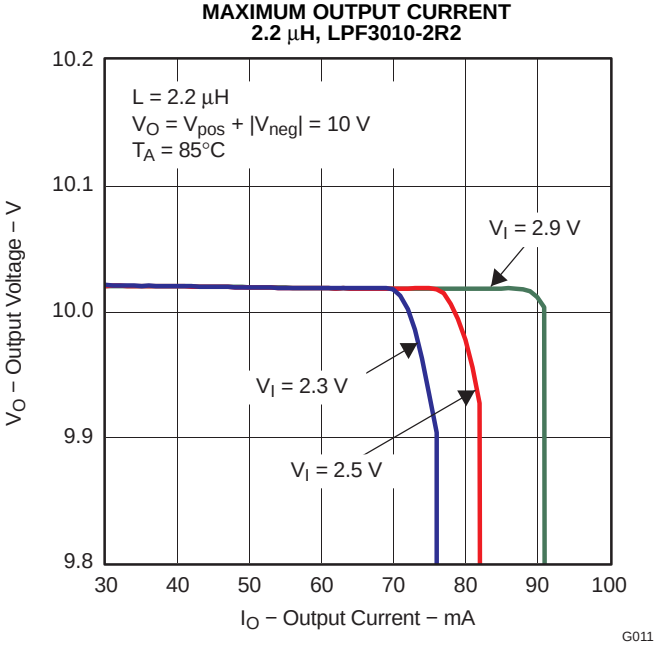

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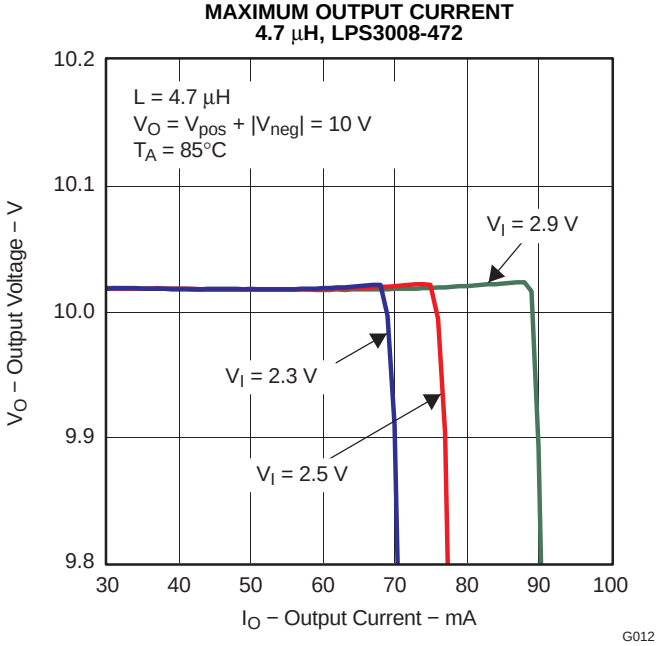

Figure 12.

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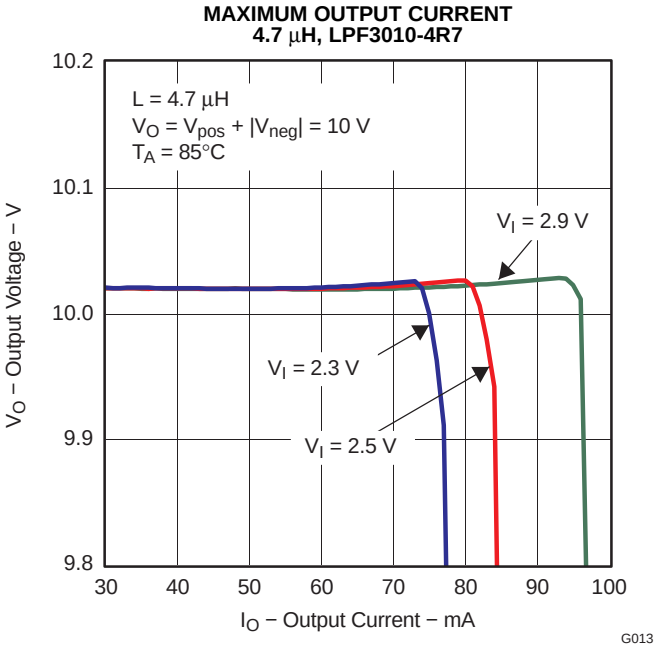

Figure 13.

DETAILED DESCRIPTION

The TPS65136 operates with a four-switch buck-boost converter topology, generating a negative and a positive output voltage with a single inductor. The device uses the SIMO regulator technology featuring best-in-class line-transient regulation, buck-boost mode for the positive and negative outputs, and highest efficiency over the entire load-current range. High efficiency over the entire load-current range is implemented by reducing the converter switching frequency. Out-of-audio mode avoids the switching frequency going below 20 kHz.

As illustrated in the functional block diagram, the converter operates with two control loops. One error amplifier sets the output voltage for the positive output, OUTP. The ground error amplifier regulates FBG to typically 0 V. Using the external feedback divider allows setting the output voltage of the negative output, OUTN. In principle, the converter topology operates just like any other buck-boost converter topology with the difference that the output voltage across the inductor is the sum of the positive and negative output voltages. With this consideration, all calculations of the buck-boost converter apply for this topology as well. During the first switch cycle, M1 and M2 are closed, connecting the inductor from VIN to GND. During the second switch cycle, the inductor discharges to the positive and negative outputs by closing switches M4 and M3. Because the inductor is discharged to both of the outputs simultaneously, the output voltages can be higher or lower than the input voltage. In addition to that, the converter operates best when the current out of OUTP is equal to the current flowing into OUTN. This is usually the case when driving an AMOLED panel. Any asymmetries in load current can be canceled out by the ground error amplifier connected to FBG. However, this is only possible for current asymmetries of typically 30%. During light load current in discontinuous conduction mode, the converter operates in peak-current-mode control with the switching cycle given by the internal voltage-controlled oscillator (VCO). As the load current increases, the converter operates in continuous-conduction mode. In this mode, the converter moves to peak-current control with the switch cycle given by the fixed off-time. The SIMO regulator topology has excellent line transient regulation when operating in discontinuous conduction mode. As the load current increases, entering continuous conduction mode, the line transient performance is linearly decreased.

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Advanced Power-Save Mode for Light-Load Efficiency

In order to maintain high efficiency over the entire load-current range, the converter reduces its switching frequency as the load current decreases. The advanced power-save mode controls the switching frequency using a voltage-controlled oscillator (VCO). The VCO frequency is proportional to the inductor peak current, with a lower frequency limit of 20 kHz. This avoids disturbance of the audio band and minimizes audible noise coming from the ceramic input and output capacitors. By maintaining a controlled switching frequency, possible EMI is minimized. This is especially important when using the device in mobile phones. See Figure 8 for typical switching frequency versus load current.

Buck-Boost Mode Operation

Buck-boost mode operation allows the input voltage to be higher than the output voltage. This mode allows the use of batteries and supply voltages that are above the fixed 4.6-V output voltage of OUTP.

Inherent Excellent Line-Transient Regulation

The SIMO regulator achieves inherent superior line-transient regulation when operating in discontinuous conduction mode, shown in Figure 5 and Figure 6. In discontinuous conduction mode, the current delivered to the output is given by the inductor peak current and falling slope of the inductor current. This is shown in Figure 14, where the output current, given by the area *A*, is the same for different input voltages. Because the converter uses peak-current-mode control, the peak current is fixed as long as the load current is fixed. The falling slope of the inductor current is given by the sum of the output voltage and inductor value. This is also a fixed value and independent of the input voltage. Because of this, any change in input voltage changes the converter duty cycle but does not change the inductor peak current or the falling slope of the inductor current. Therefore, the output current, given by the area *A* (Figure 14), remains constant over any input voltage variation. Because the area *A* is constant, the converter has an inherently perfect line regulation when operating in discontinuous conduction mode. Entering continuous conduction mode (CCM) linearly decreases the line-transient performance. However, the line-transient response in CCM is still as good as for any standard current-mode-controlled switching converter. The following formulas detail the relations of the TPS65136 converter topology operating in CCM.

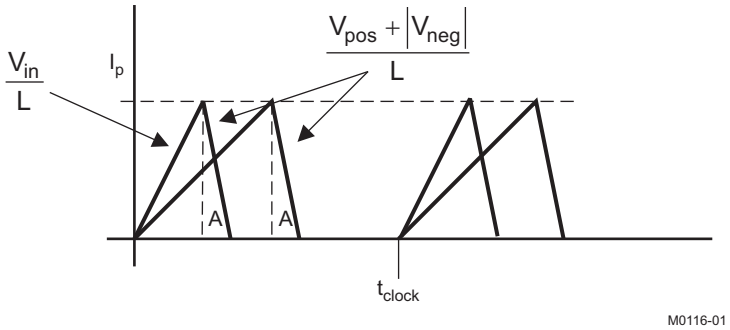

Figure 14. Inherently Perfect Line-Transient Regulation

The converter always sees the sum of the negative and positive output voltage, which is calculated as:

$$V_o = V_{outp} + |V_{outn}|$$

The converter duty cycle is calculated using the efficiency estimation from the data sheet curves or from real application measurements. A 70% efficiency value is a good value to go through the calculations.

$$D = \frac{V_o}{V_{in} \bullet \eta + V_o}$$

The output current for entering continuous conduction mode can be calculated. The switching frequency can be obtained from the data sheet graphs. A frequency of 1.5 MHz is usually sufficient for these types of calculations.

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$$I_c = \frac{V_o \cdot (1-D)^2}{f_S \cdot 2 \cdot L} \quad (1)$$

The inductor ripple current when operating in CCM can also be calculated.

$$\Delta i_L = \frac{V_{in} \cdot D}{L \cdot f_S}$$

Last but not least, the converter switch peak current is calculated.

$$I_{sw} = \frac{V_{in} \cdot D}{2 \cdot f \cdot L} + \frac{I_{out}}{1-D} \quad (2)$$

Overvoltage Protection

The device monitors both the positive and negative output voltages. The positive regulator monitors the positive output and reduces the current limit when the output voltage exceeds the overvoltage protection limit. The negative output is clamped using a zener diode, typically to –7.6 V.

Short-Circuit Protection

Both outputs are protected against short circuits either to GND or against the other output. For the positive output, the device switching frequency and the current limit are reduced in case of a short circuit.

Soft-Start Operation

The device increases the current limit during soft-start operation to avoid high inrush currents during start-up. The current limit typically ramps up to its full-current limit within 100 µs.

Start-Up Sequencing

The TPS65136 includes an internal, fixed start-up sequence, where the negative output voltage rail comes up after the positive output voltage rail. The device starts the positive rail first, and an internal counter delays the start-up of the negative rail, typically by 8.7 ms. The negative rail is clamped, typically to –0.4 V, until the internal timer commands the negative rail to start up.

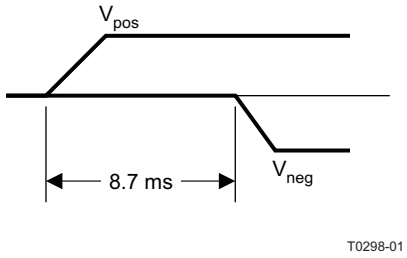

Figure 15. Start-Up Sequencing

Output-Current Mismatch

The device operates best when the current of the positive output is similar to the current of the negative output. However, the device is able to regulate an output-current mismatch between the outputs of up to 30%. If the output-current mismatch becomes much larger, then one of the outputs goes out of regulation.

Input Capacitor Selection

The device typically requires a 10-µF ceramic input capacitor. Larger values can be used to lower the input voltage ripple. Table 1 lists capacitors suitable for use on the TPS65136 input.

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Table 1. Input Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	SIZE
10 µF/10 V	Taiyo Yuden LMK212BJ106	0805
10 µF/6.3 V	Taiyo Yuden JMK107BJ106	0603

Inductor Selection/Efficiency/Line-Transient Response

The device is internally compensated and provides stable operation with either a 4.7-µH or 2.2-µH inductor. For this type of converter, the inductor selection is a key element in the design process, because it has an impact on several application parameters. The inductor selection influences the converter efficiency, line transient response, and maximum output current. Because the inductor ripple current is fairly large in this type of application, the inductor has a major impact on the overall converter efficiency. Having large inductor ripple current causes the inductor core and magnetizing losses to become dominant. Due to this, an inductor with a larger dc winding resistance can possibly achieve higher converter efficiencies when having lower core and magnetizing losses. Therefore, minimizing inductor ripple current also increases the overall converter efficiency. A 4.7-µH inductor achieves a higher efficiency compared to a 2.2-µH inductor, due to lower inductor ripple current. The inductor value also influences the line transient regulation. This is because the inductor value influences the current range entering continuous conduction mode (CCM). As discussed, the line transient performance decreases when entering CCM. The larger the inductor value, the lower the load current when entering CCM. The formula to calculate the current entering CCM is shown in Equation 1. The inductors listed in Table 2 achieve a good overall converter efficiency while having a low device profile of just 0,8 mm. The inductor saturation current should be 900 mA, depending on the maximum output current of the application. See Equation 2, where the converter switch current limit is calculated. The converter switch current is equal to the peak inductor current.

Table 2. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS in mm	I_{sat}/DCR
2.2 µH	Coilcraft LPS3008-222	2,95 × 2,95 × 0,8	1.1 A/175 mΩ
2.2 µH	TOKO FDSE0312-2R2	3,3 × 3,3 × 1,2	1.2 A/160 mΩ
2.2 µH	ABCO LPF3010T-2R2	2,8 × 2,8 × 1	1.0A/100 mΩ
2.2 µH	Maruwa CXFU0208-2R2	2,65 × 2,65 × 0,8	0.85A/185 mΩ
4.7 µH	Maruwa CXFU0208-4R7	2,65 × 2,65 × 0,8	0.51A/440 mΩ
4.7 µH	Coilcraft LPS3008-472	2,95 × 2,95 × 0,8	0.8 A/350 mΩ
4.7 µH	ABCO LPF3010T-4R7	2,8 × 2,8 × 1	0.7A/280 mΩ

Output Capacitor Selection

A 4.7-µF output capacitor is generally sufficient for most applications, but larger values can be used as well for improved line-transient response at higher load currents. The capacitor of Table 3 is recommended for use with the TPS65136.

Table 3. Output Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	SIZE
4.7 µF/10V	Taiyo Yuden LMK107BJ475	0603

Setting the Negative Output Voltage OUTN

For highest output-voltage accuracy, the TPS65136 has an internally fixed output voltage for the positive output. The negative output voltage is adjustable. Because the feedback FBG is regulated to ground, the voltage across R1 is equal to the positive output voltage of 4.6 V. R1 is selected to have at least 10 µA through the feedback divider.

$$R1 = \frac{4.6\ V}{10\ \mu A} \approx 464\ k\Omega$$

R2 is then calculated as:

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$$R2 = \frac{|V_{neg}|}{4.6\ V} \times R1$$

PCB Layout Guidelines

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the TPS65136, the following PCB layout guidelines are recommended.

Place the power components first. The inductor and the input and output capacitors must be as close as possible to the IC pins. Place the bypass capacitor for the reference output voltage VAUX as close as possible to pin 4. Use bold and wide traces for power traces connecting the inductor and input and output capacitors. Use a common ground plane or a start ground connection.

See the TPS65136EVM-063 user's guide (SLVU244) and evaluation module for a PCB layout example.

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TYPICAL APPLICATION

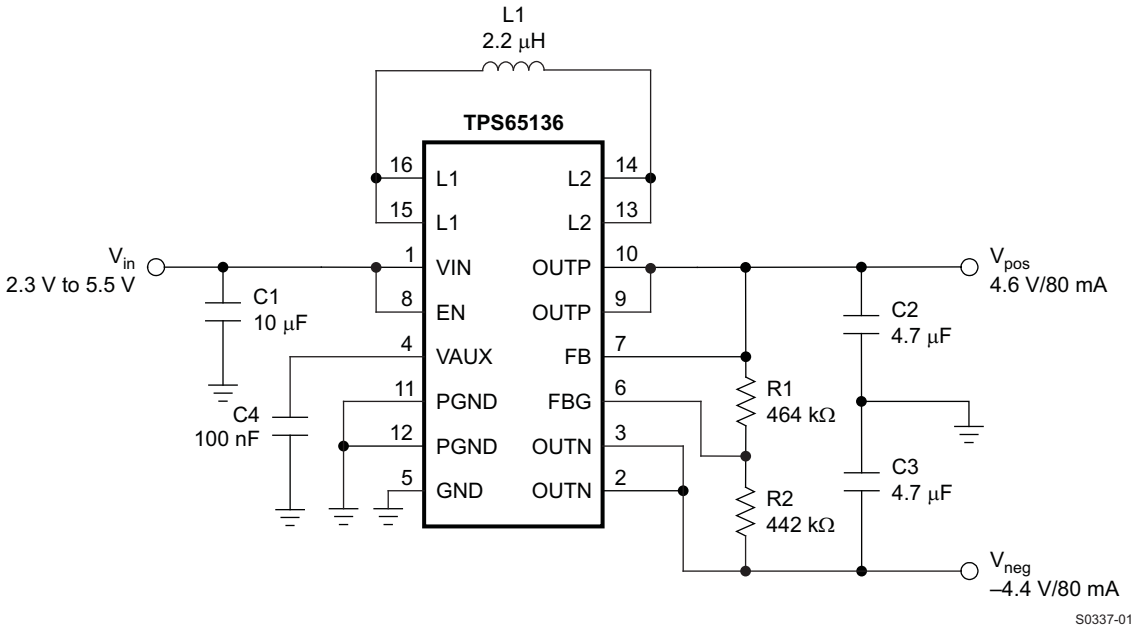

Figure 16. Standard Application AMOLED Supply

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65136RTER	ACTIVE	QFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65136RTERG4	ACTIVE	QFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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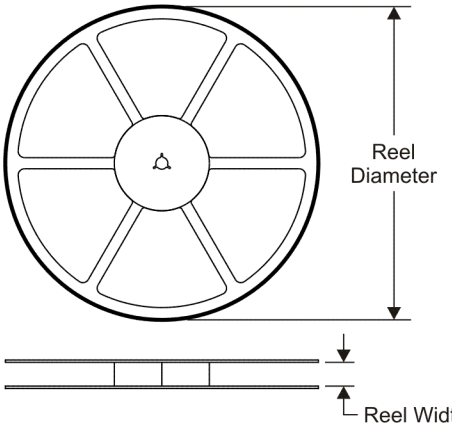
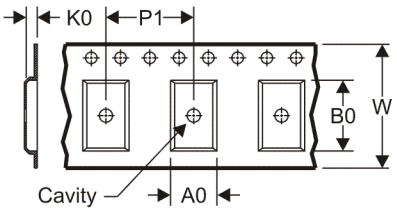
TAPE AND REEL INFORMATION

REEL DIMENSIONS

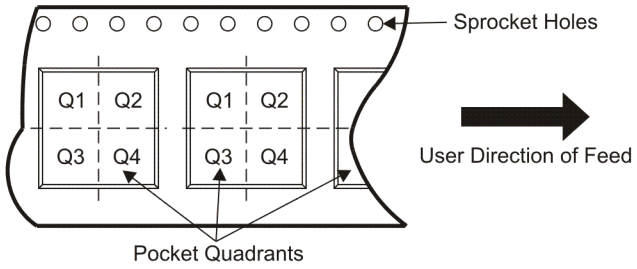


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

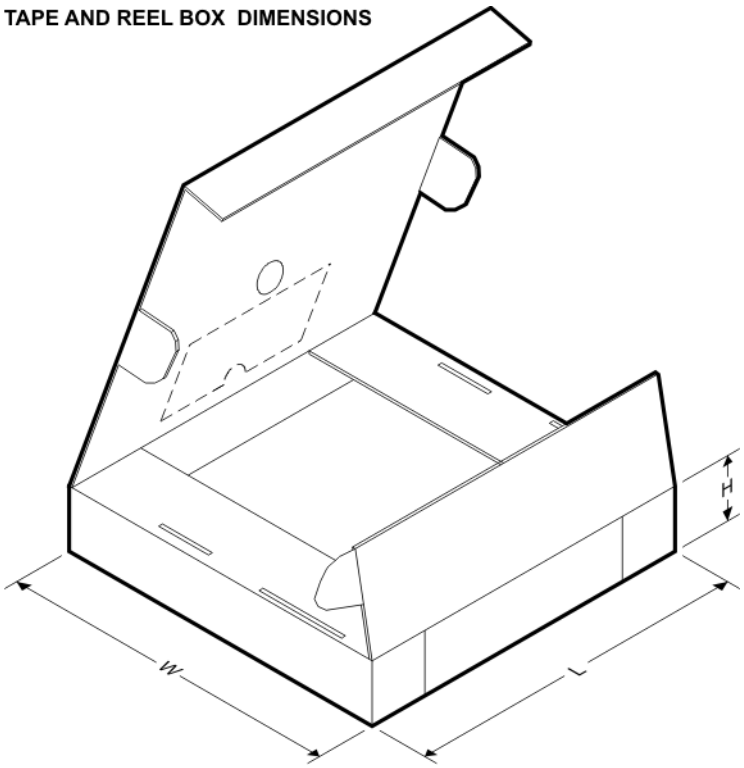
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65136RTER	QFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

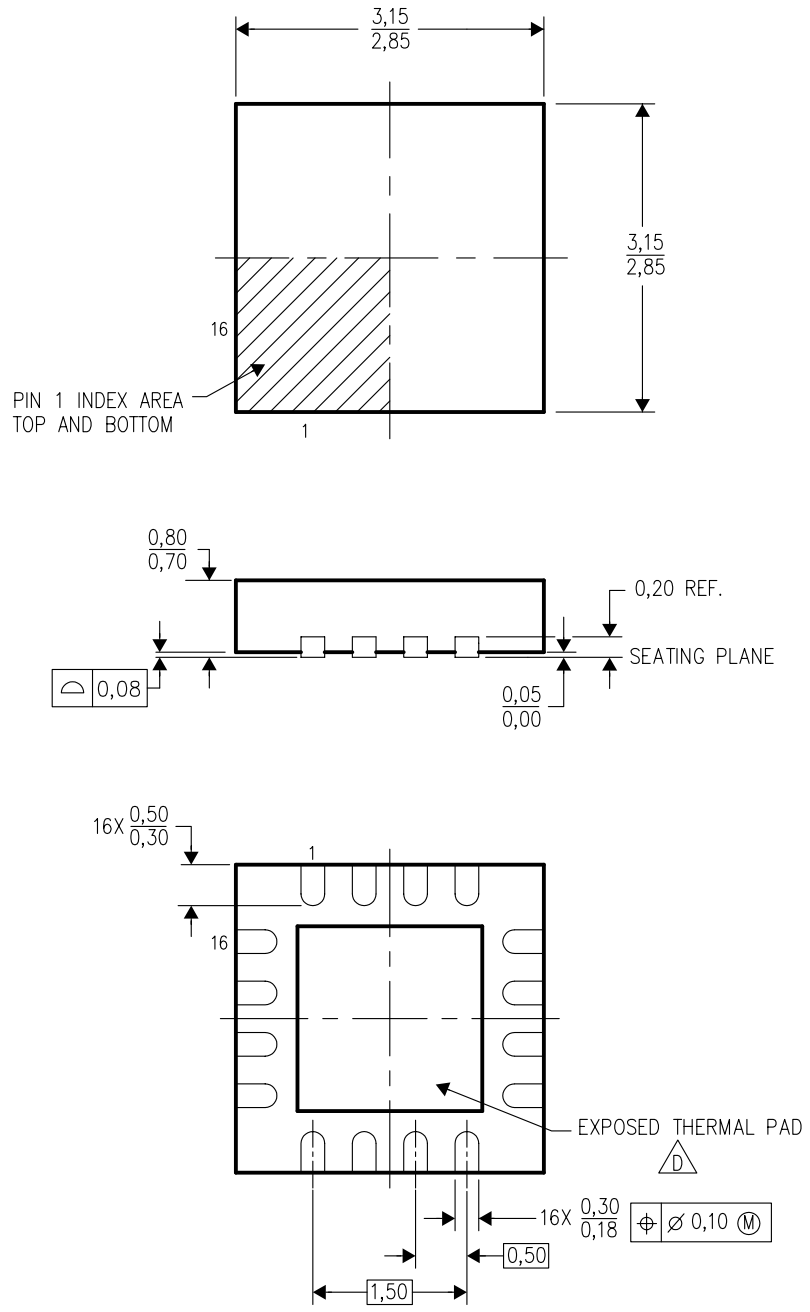
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65136RTER	QFN	RTE	16	3000	346.0	346.0	29.0

RTE (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

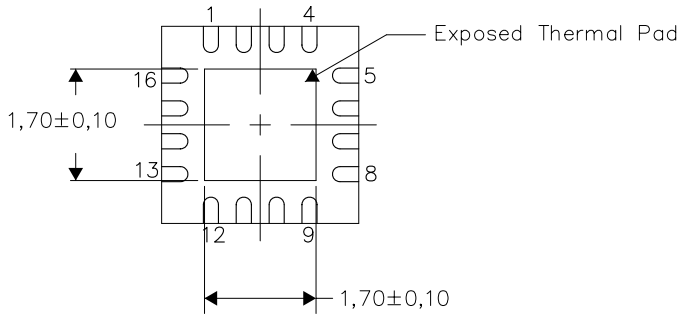
RTE (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

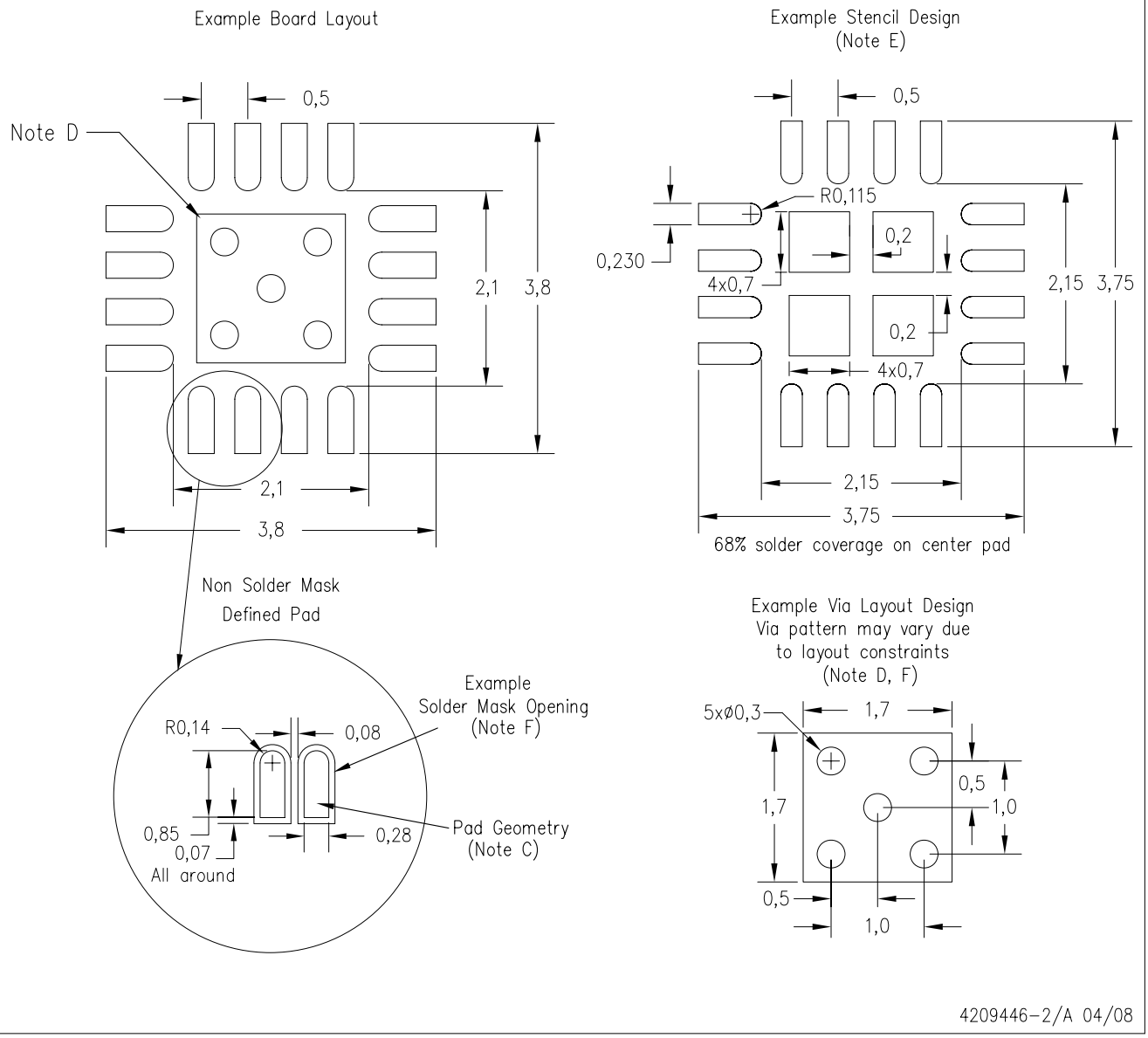


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RTE (S–PWQFN–N16)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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