

Compal Confidential

BCL50 Schematics Document Banias uFCBGA/uFCPGA Package with Odem Core Logic

2003-03-14

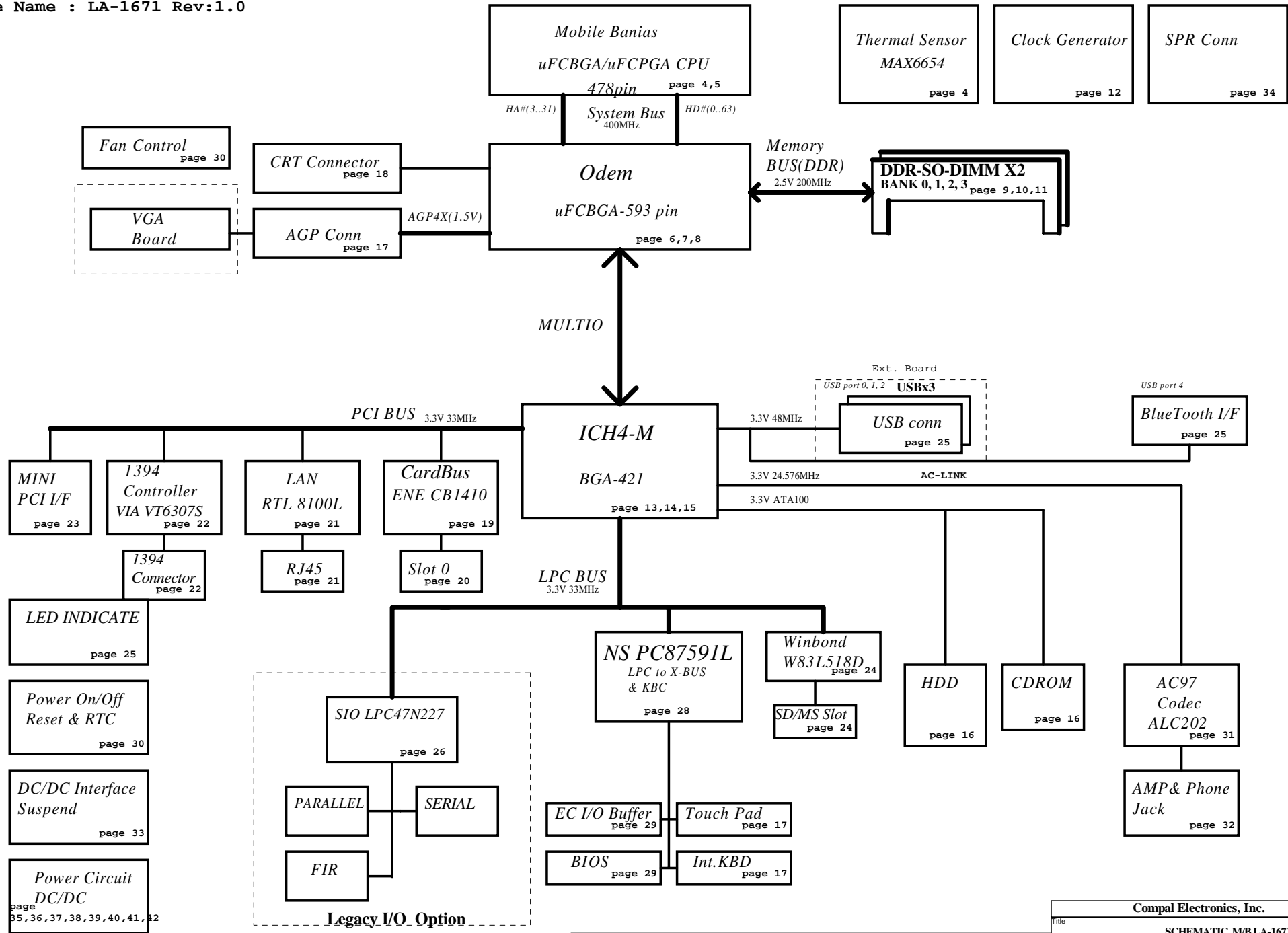
REV: 1.0

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SCHEMATIC, M/B LA-1671		
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Model Name :BCL50

File Name : LA-1671 Rev:1.0



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for MCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table

BID2	BID1	BID0	PCB Revision
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0	0	1	0.2
0	1	0	0.3
0	1	1	0.4
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1	0	1	
1	1	0	
1	1	1	

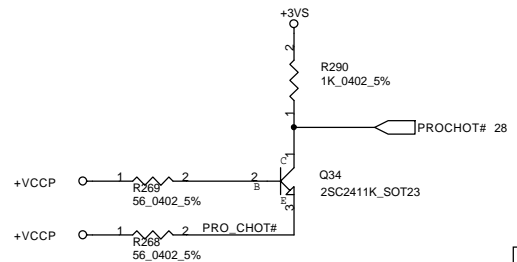
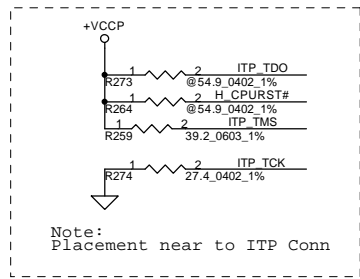
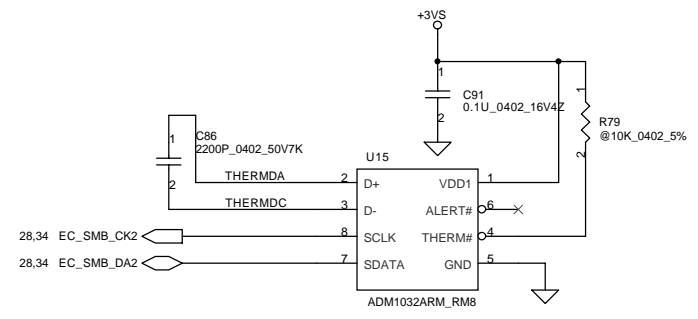
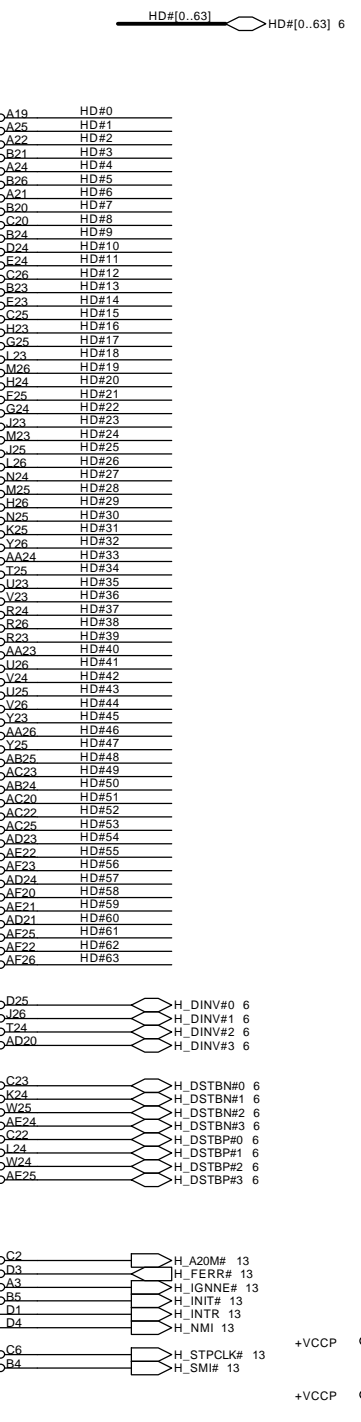
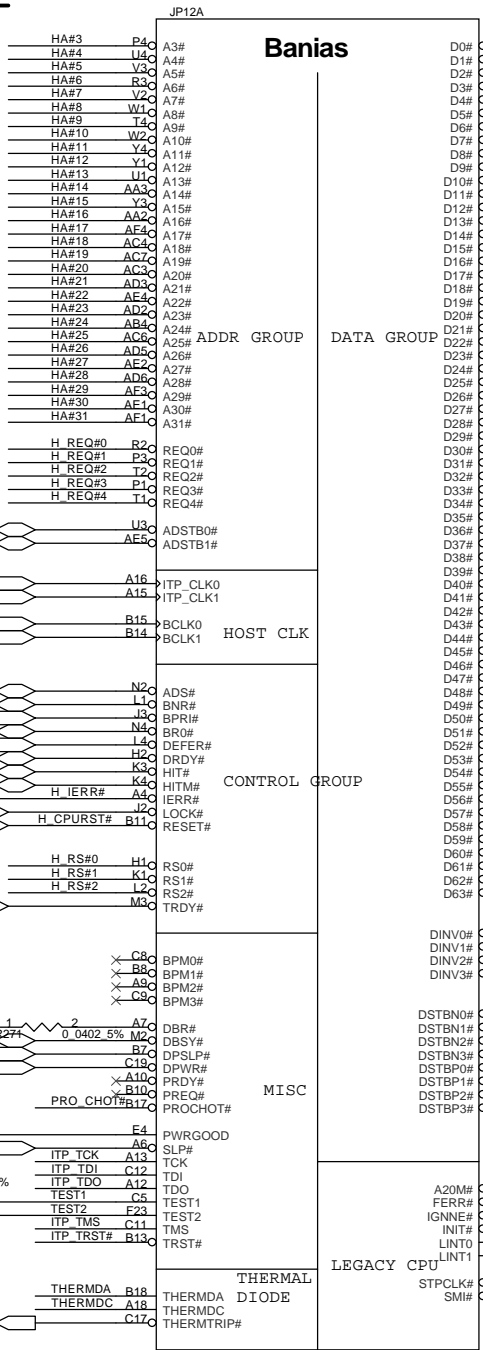
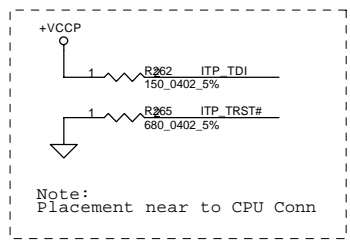
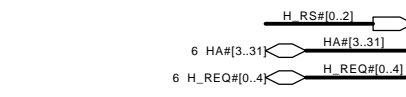
External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD19	2	PIRQC
LAN	AD17	3	PIRQD
Mini-PCI	AD18,AD22	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQB

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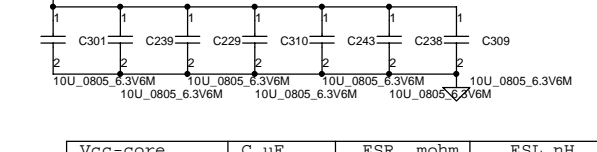
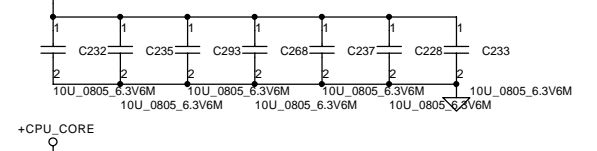
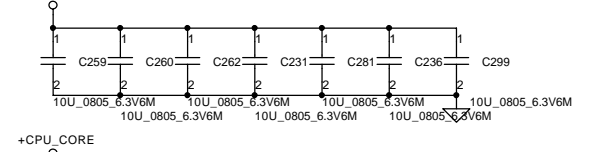
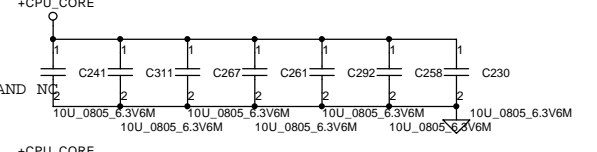
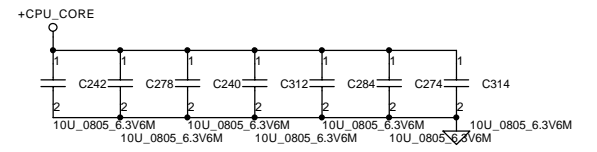
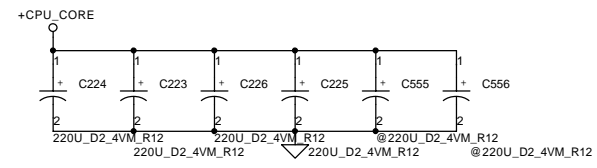
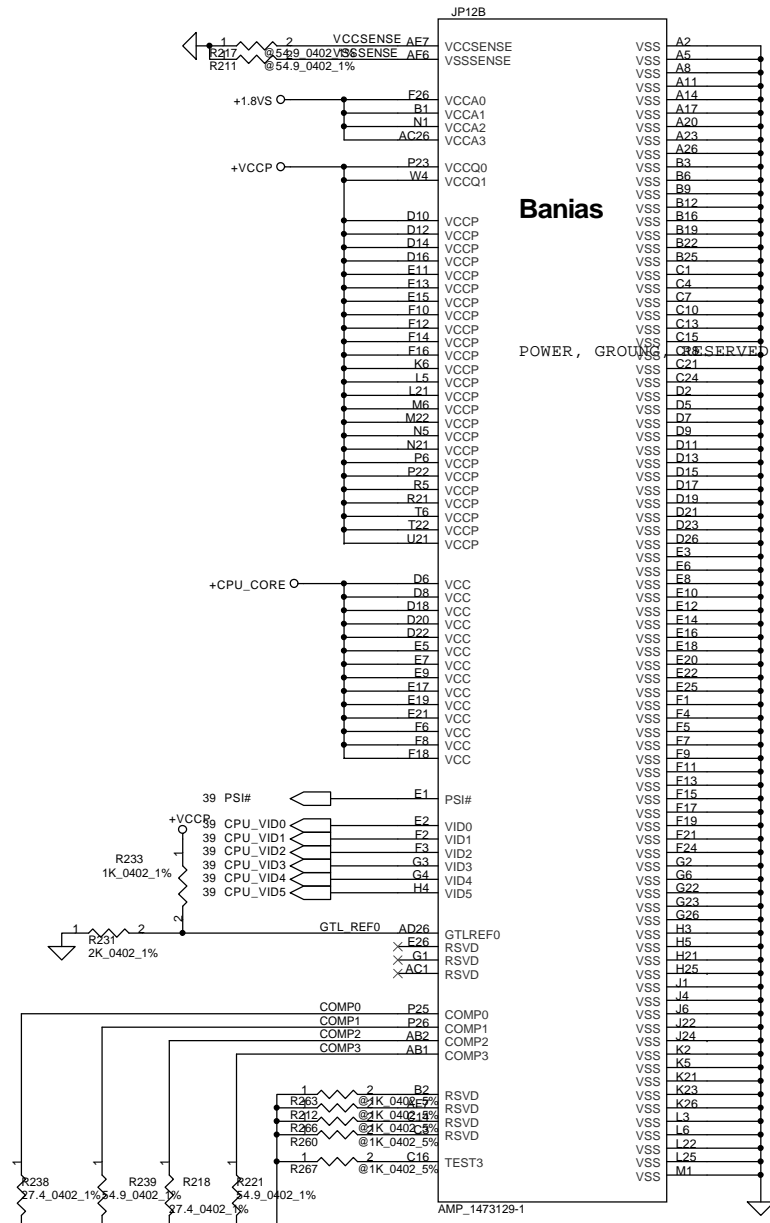
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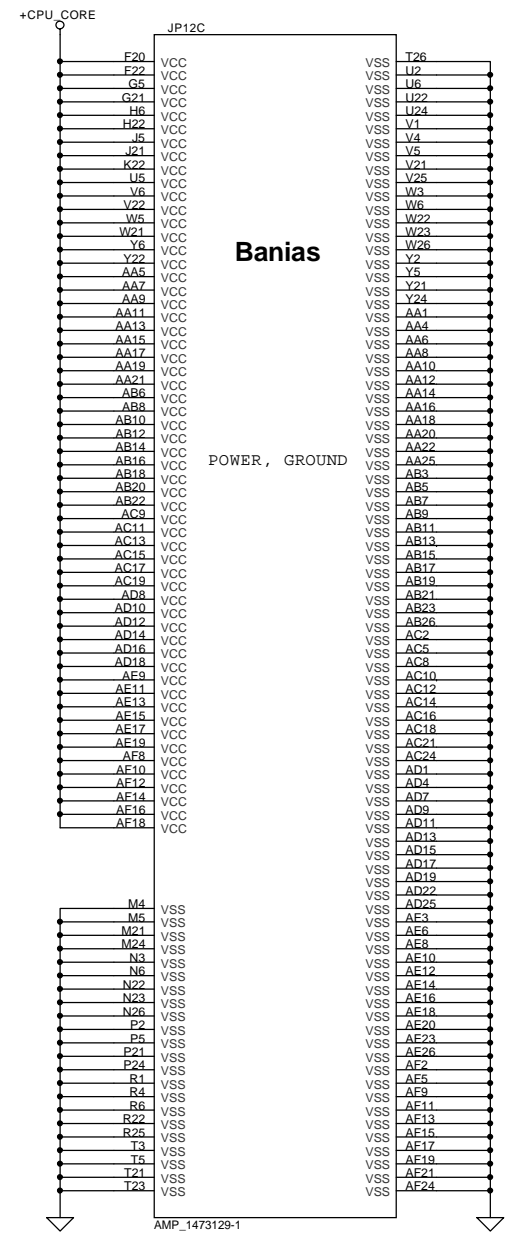
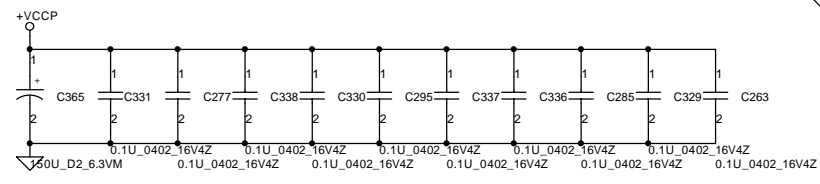
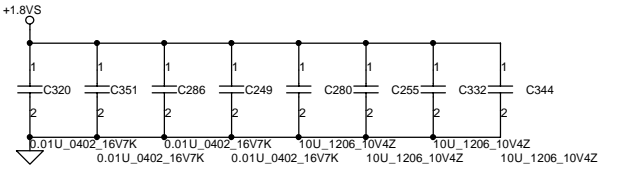
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AMP_1473129-1



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



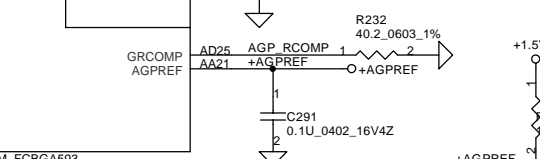
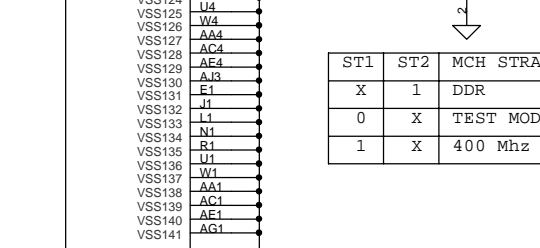
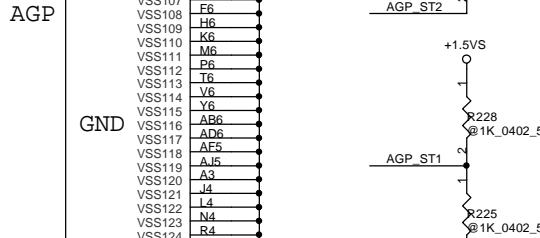
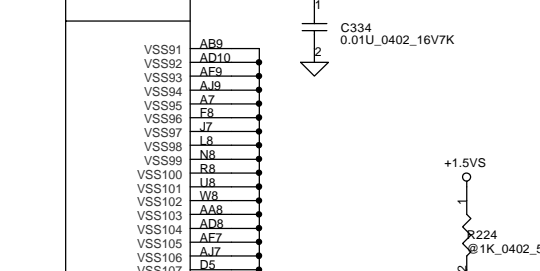
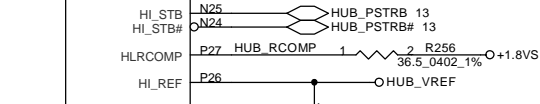
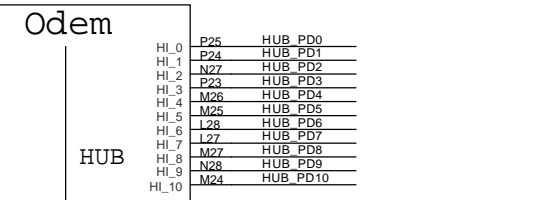
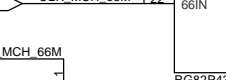
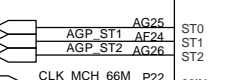
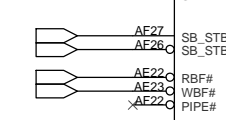
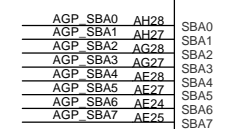
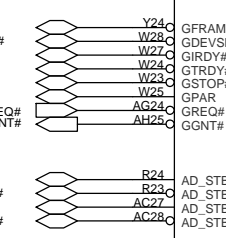
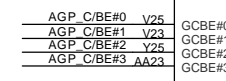
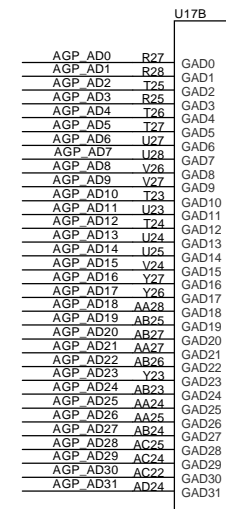
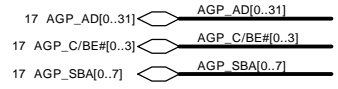
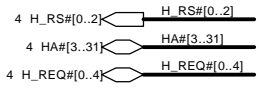
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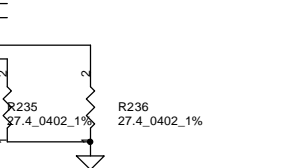
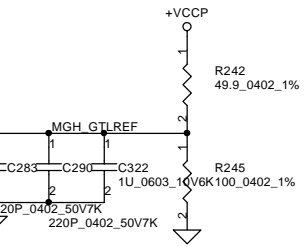
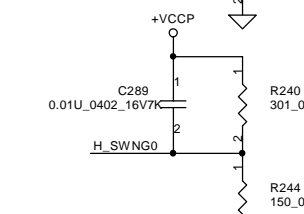
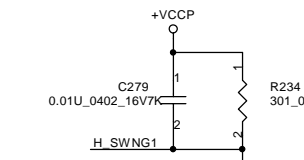
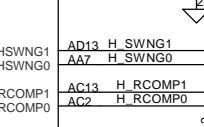
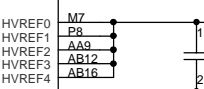
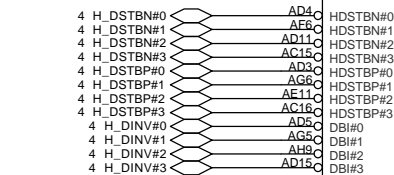
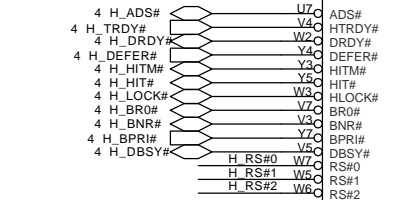
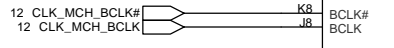
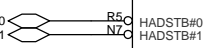
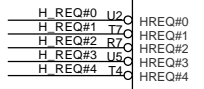
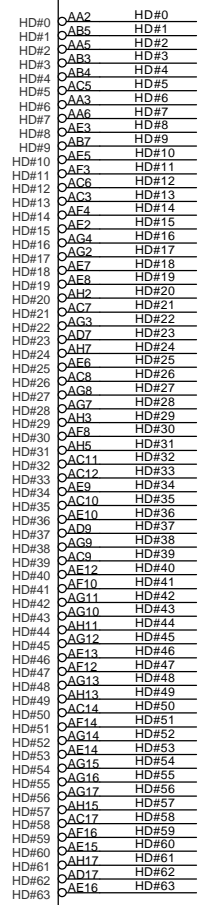
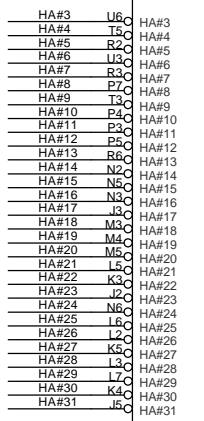
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Odem

HOST



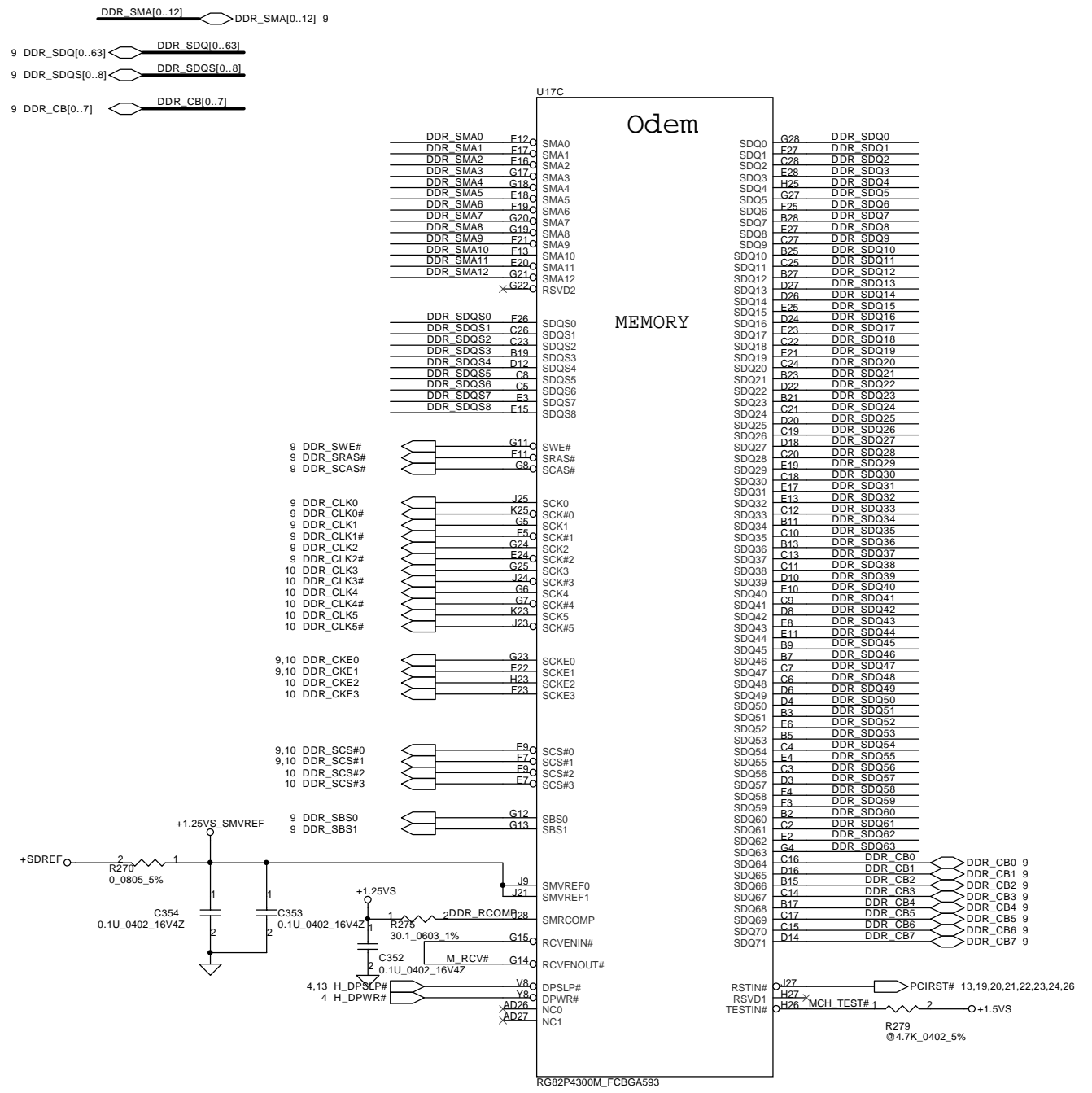
ST1	ST2	MCH STRAP
X	1	DDR
0	X	TEST MODE
1	X	400 Mhz PSB

Note:
 R203, R204 placement
 center of MCH and AGP

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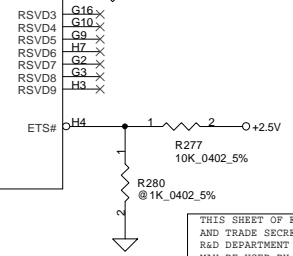
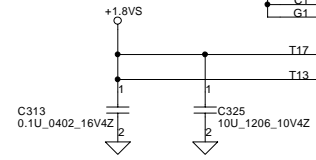
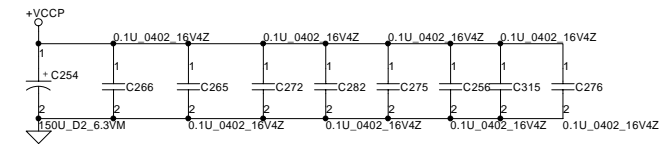
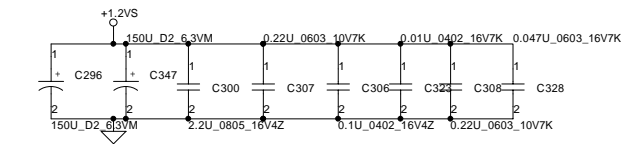
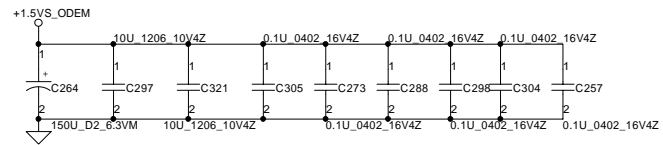
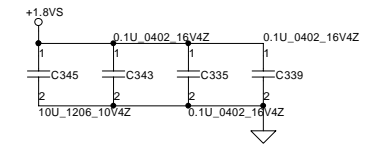
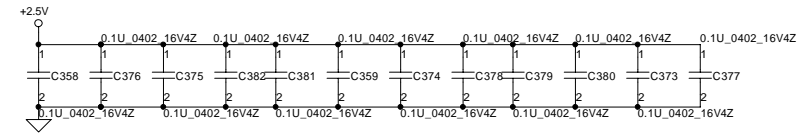
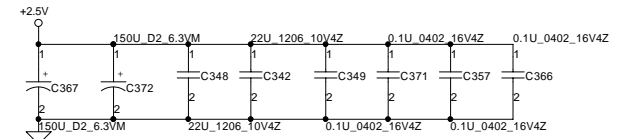
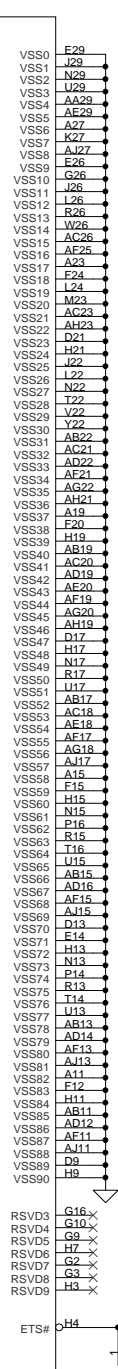
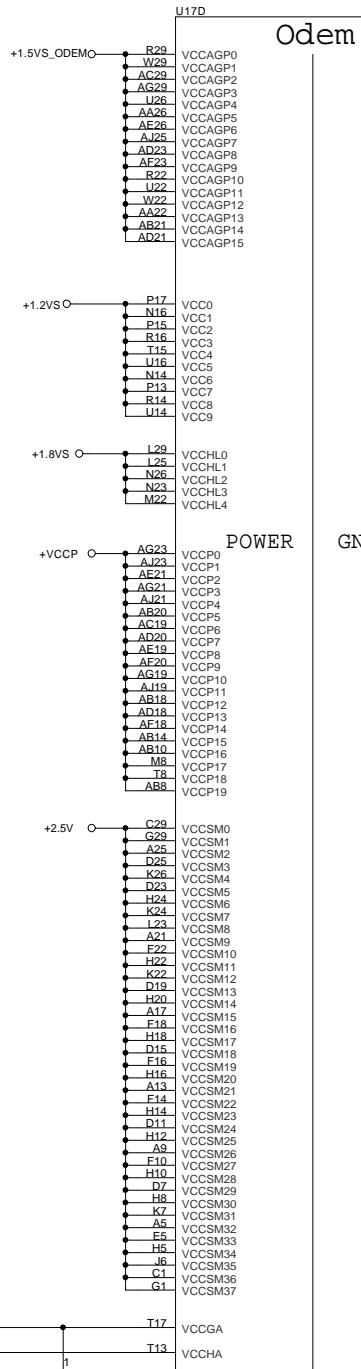


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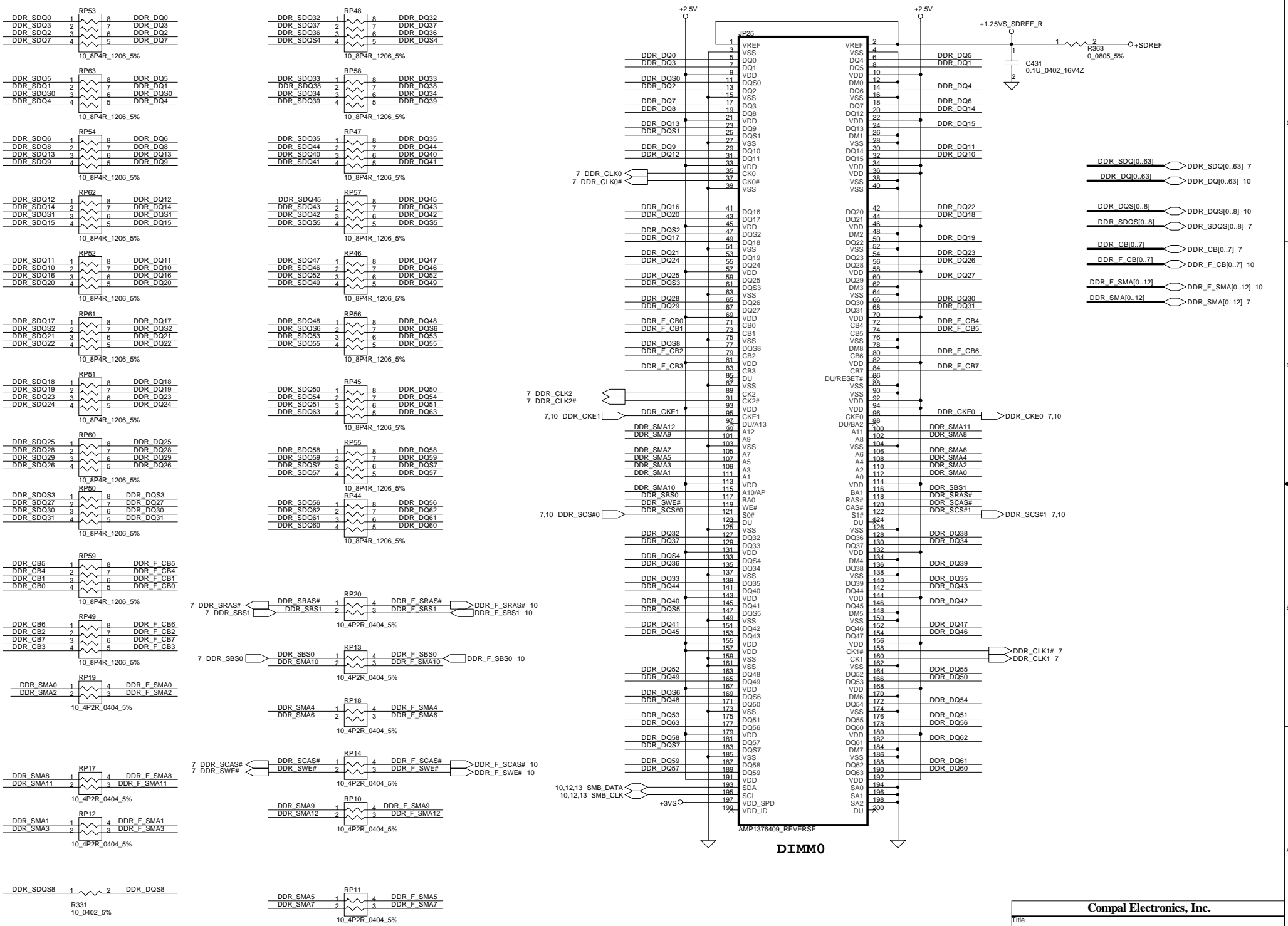
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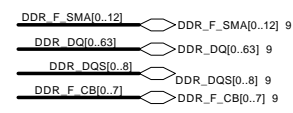
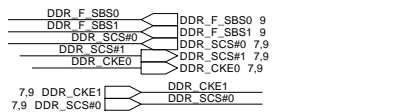
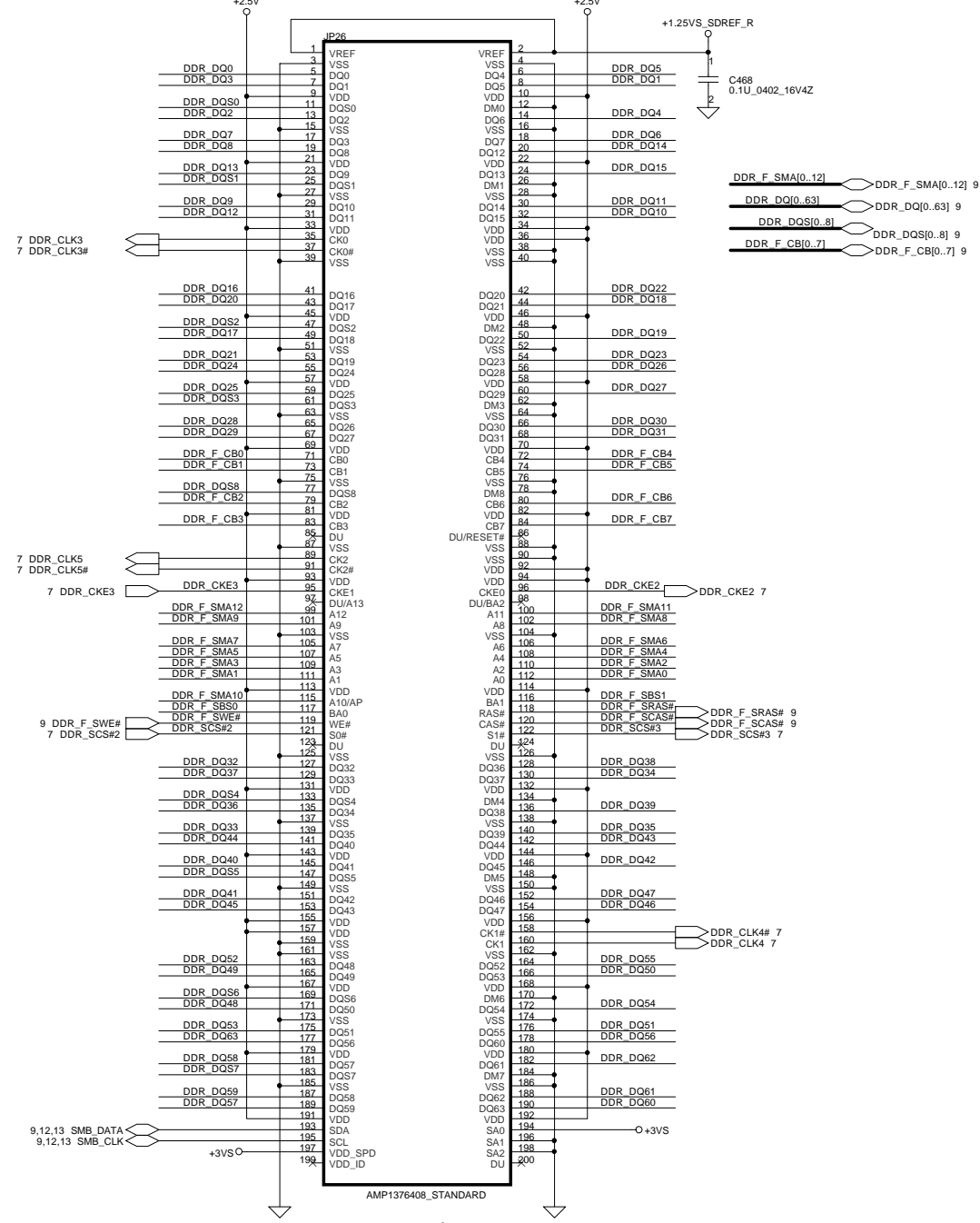
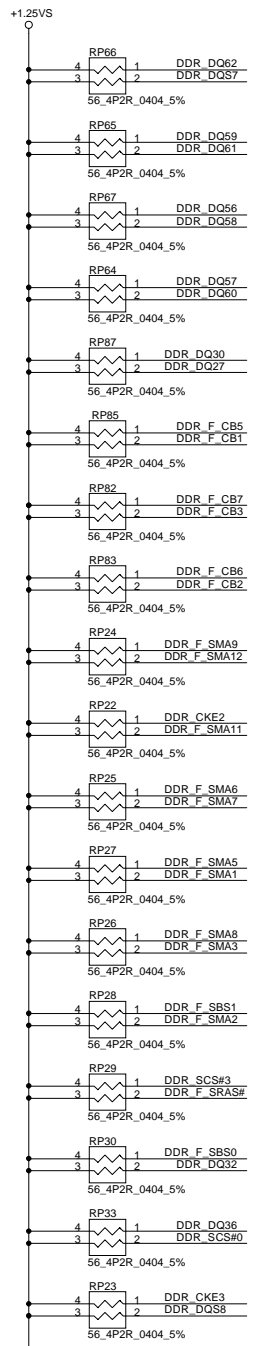
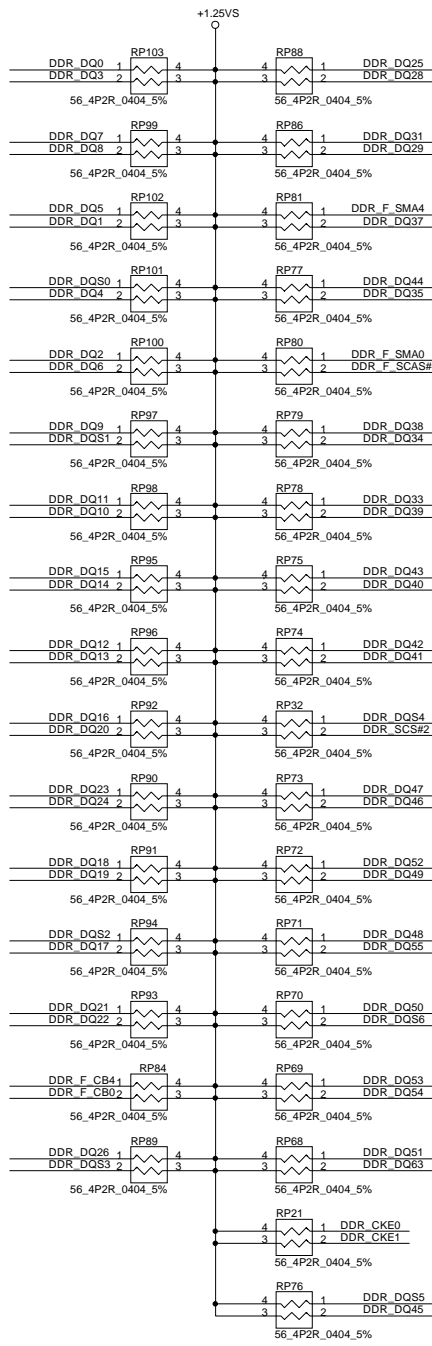
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- DDR_SDQ[0..63] ↔ DDR_SDQ[0..63] 7
- DDR_DQ[0..63] ↔ DDR_DQ[0..63] 10
- DDR_DQS[0..8] ↔ DDR_DQS[0..8] 10
- DDR_SDQS[0..8] ↔ DDR_SDQS[0..8] 7
- DDR_CB[0..7] ↔ DDR_CB[0..7] 7
- DDR_F_CB[0..7] ↔ DDR_F_CB[0..7] 10
- DDR_F_SMA[0..12] ↔ DDR_F_SMA[0..12] 10
- DDR_SMA[0..12] ↔ DDR_SMA[0..12] 7

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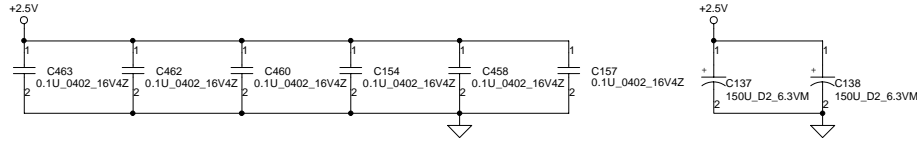
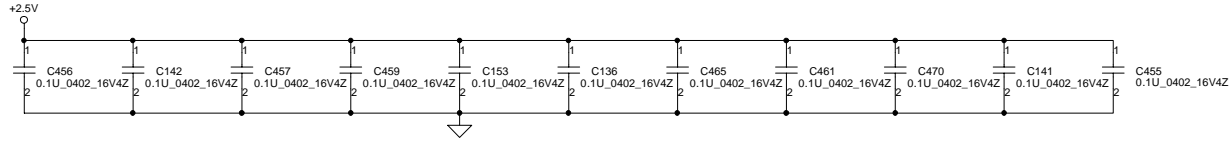


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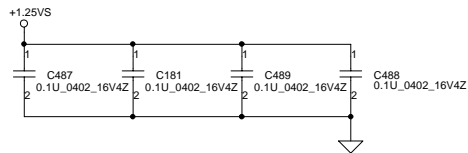
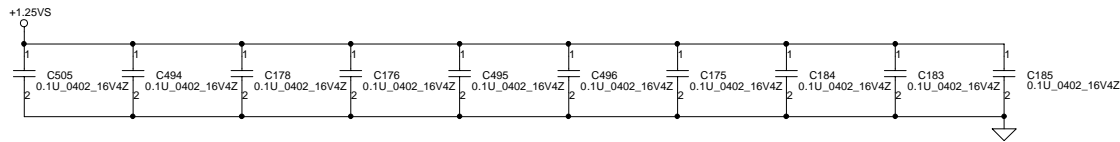
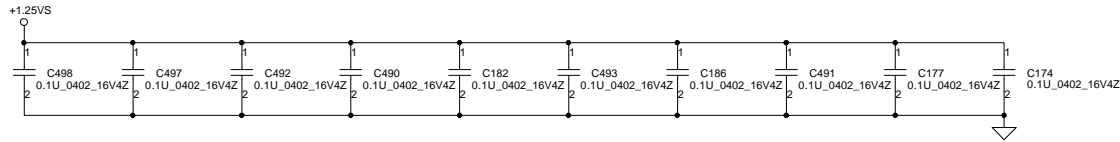
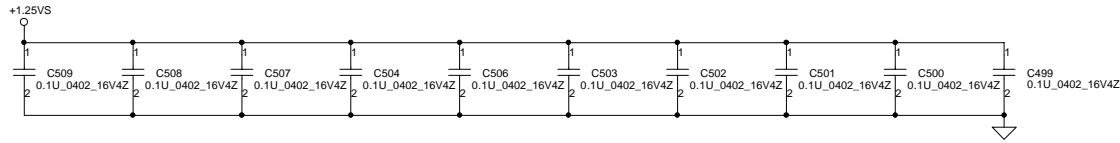
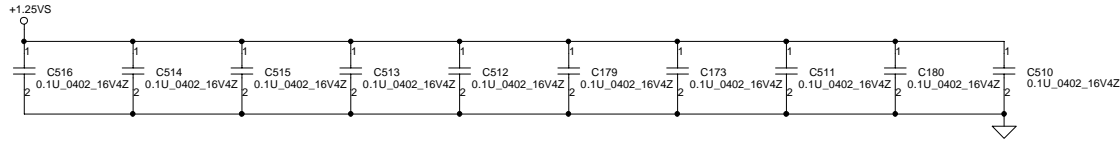
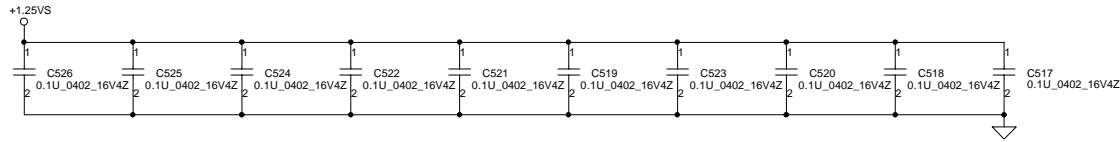
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

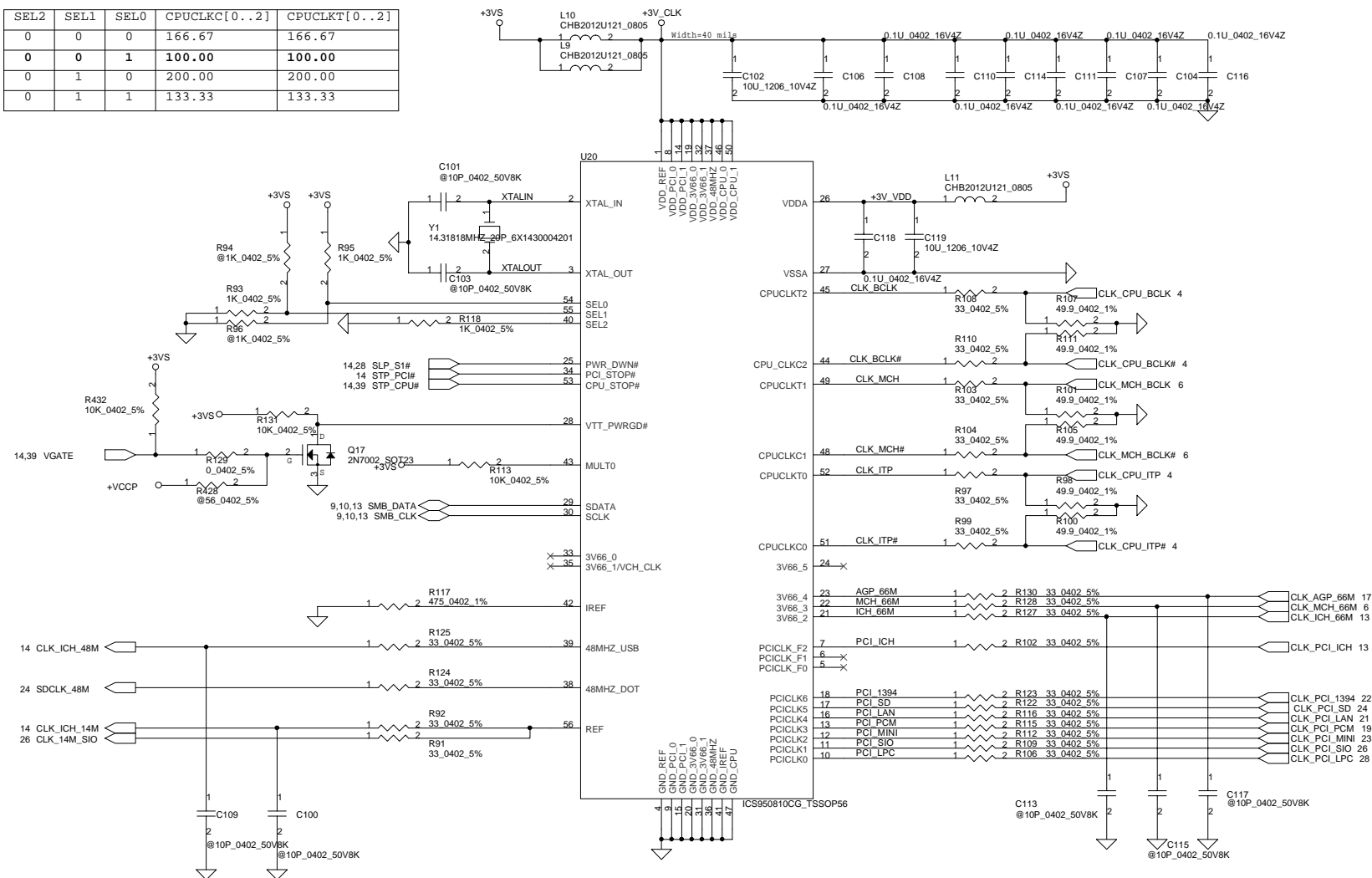
Place one cap close to every 2 pull up resistors termination to +1.25V



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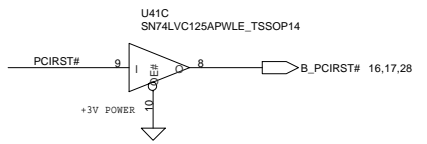
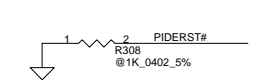
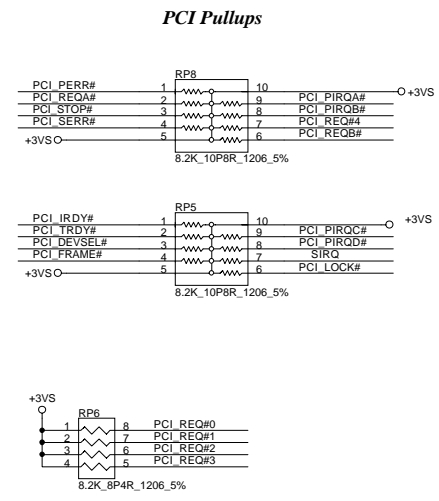
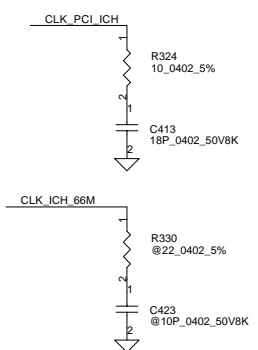
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SEL2	SEL1	SEL0	CPUCLK[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



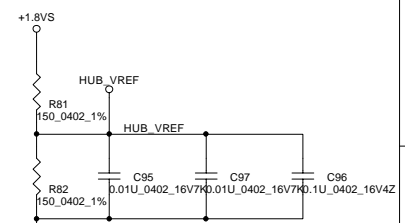
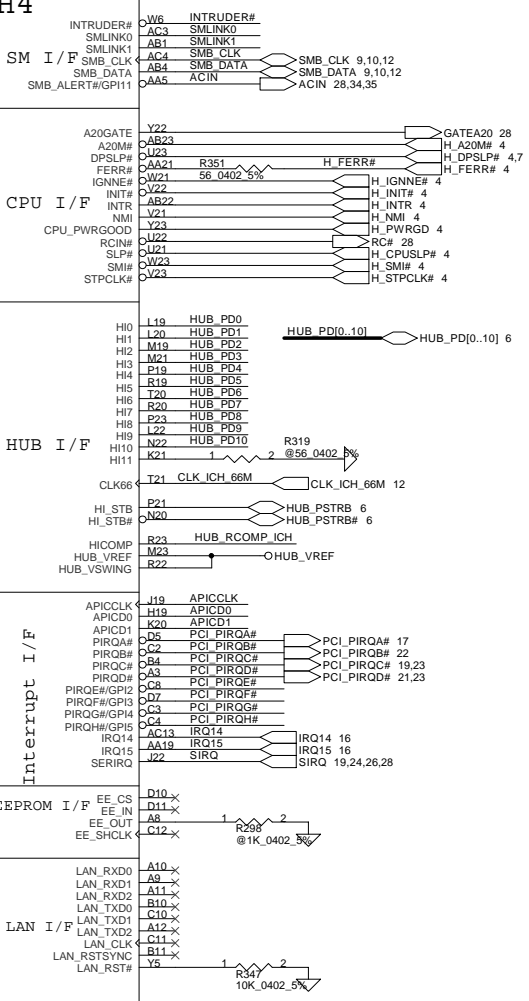
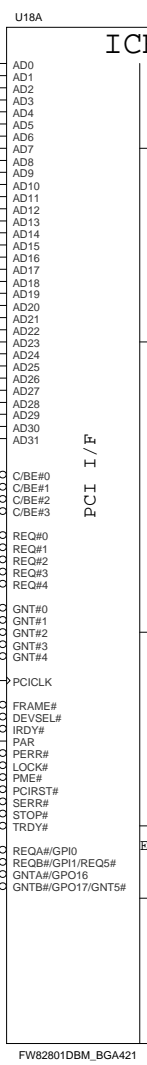
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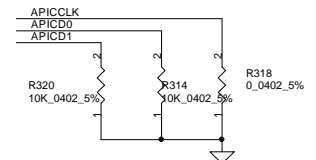
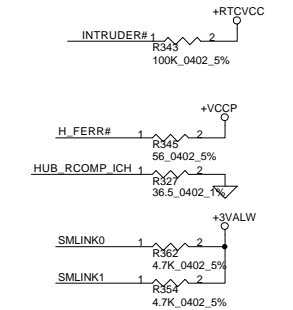
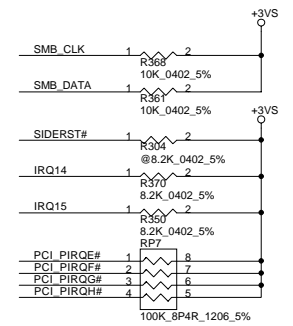


PCI_A00	H5	AD0
PCI_A01	J3	AD1
PCI_A02	H3	AD2
PCI_A03	K1	AD3
PCI_A04	G5	AD4
PCI_A05	J4	AD5
PCI_A06	H4	AD6
PCI_A07	J5	AD7
PCI_A08	K2	AD8
PCI_A09	G2	AD9
PCI_A10	L4	AD10
PCI_A11	G4	AD11
PCI_A12	L2	AD12
PCI_A13	H2	AD13
PCI_A14	L3	AD14
PCI_A15	F5	AD15
PCI_A16	F4	AD16
PCI_A17	F5	AD17
PCI_A18	N1	AD18
PCI_A19	N2	AD19
PCI_A20	E3	AD20
PCI_A21	N3	AD21
PCI_A22	F4	AD22
PCI_A23	M5	AD23
PCI_A24	E2	AD24
PCI_A25	E1	AD25
PCI_A26	P2	AD26
PCI_A27	P2	AD27
PCI_A28	D3	AD28
PCI_A29	R1	AD29
PCI_A30	D2	AD30
PCI_A31	P4	AD31

19,21,22,23	PCI_C/BE#0	J2	C/BE#0
19,21,22,23	PCI_C/BE#1	L4	C/BE#1
19,21,22,23	PCI_C/BE#2	M4	C/BE#2
19,21,22,23	PCI_C/BE#3	N4	C/BE#3
22	PCI_REQ#0	B1	REQ#0
23	PCI_REQ#1	A2	REQ#1
19	PCI_REQ#2	B3	REQ#2
21	PCI_REQ#3	C7	REQ#3
23	PCI_REQ#4	B6	REQ#4
22	PCI_GNT#0	C1	GNT#0
23	PCI_GNT#1	E6	GNT#1
19	PCI_GNT#2	A7	GNT#2
21	PCI_GNT#3	B7	GNT#3
23	PCI_GNT#4	D6	GNT#4
12	CLK_PCI_ICH	P5	PCICLK
19,21,22,23	PCI_FRAME#	F1	FRAME#
19,21,22,23	PCI_DEVSEL#	M3	DEVSEL#
19,21,22,23	PCI_IRDY#	L5	IRDY#
19,21,22,23	PCI_PAR#	G1	PAR#
19,21,22,23	PCI_PERR#	L4	PERR#
19,21,22,23	PCI_LOCK#	M2	LOCK#
7,19,20,21,22,23,24,26	PCIRST#	W2	PME#
19,21,23	PCI_SERR#	K5	PCIRST#
19,21,22,23	PCI_STOP#	F3	STOP#
19,21,22,23	PCI_TRDY#	E2	TRDY#
16	PCIRST#	B5	REQA#/GPIO
16	PCIRST#	A6	REQB#/GPIO5#
16	PCIRST#	E8	GNTA#/GPIO16
16	PCIRST#	C5	GNTB#/GPIO17/GNT5#

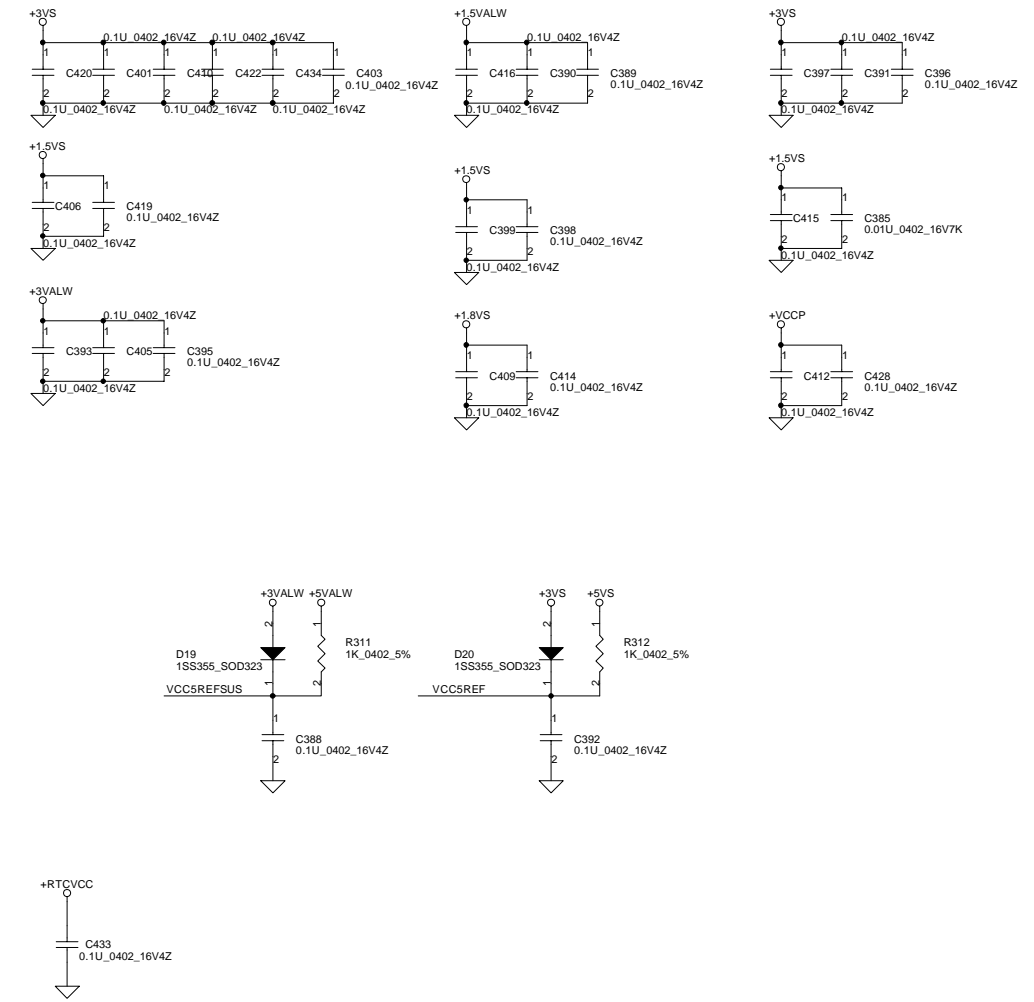
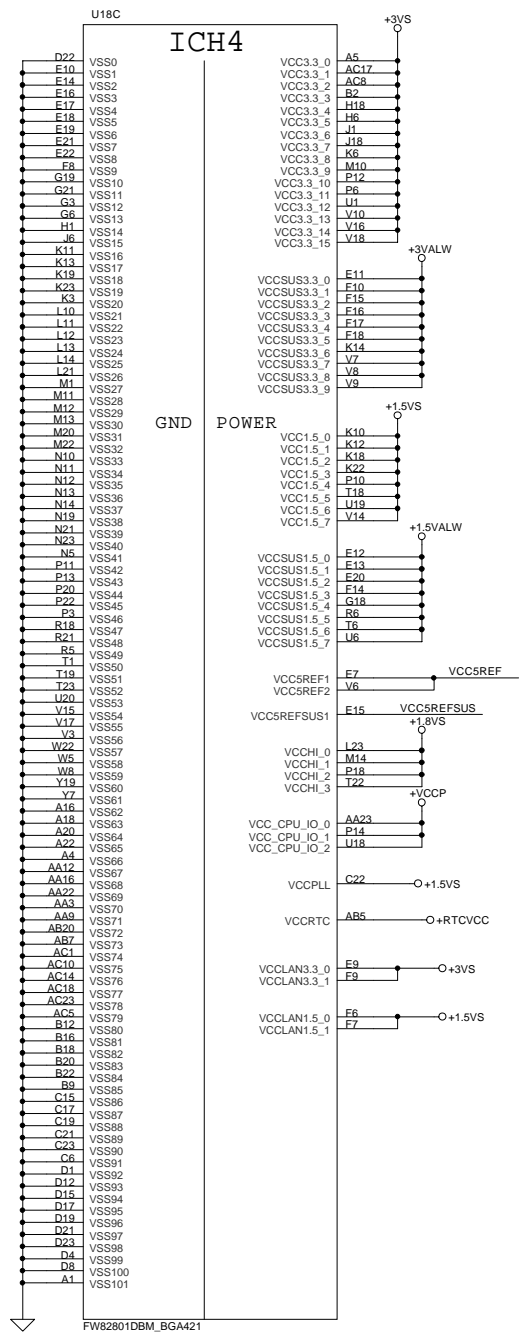


Note:
R272, R273 placement
center of MCH and
ICH4M



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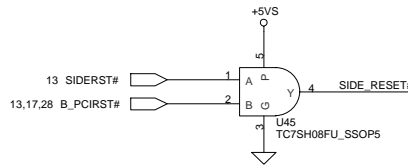
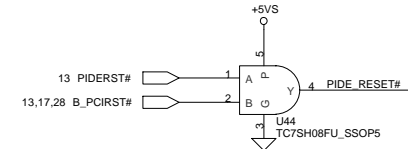
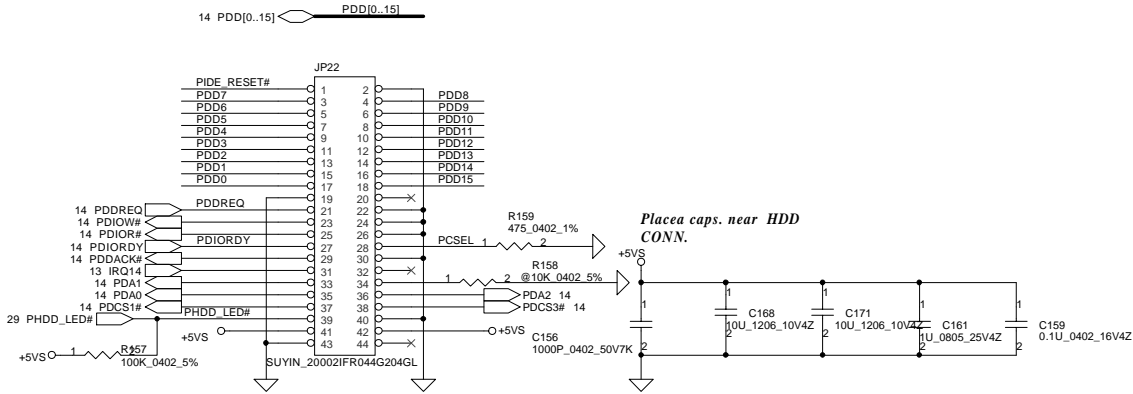
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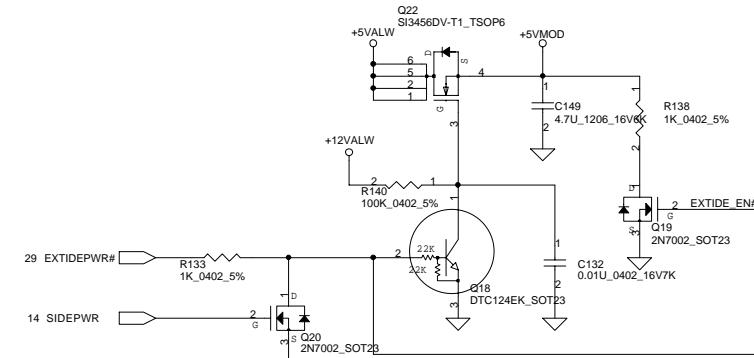
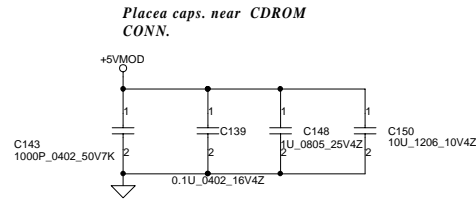
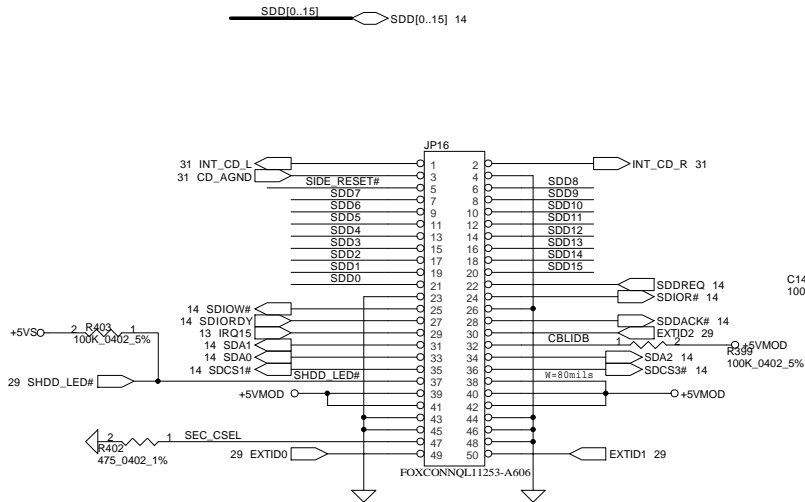
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HDD Connector



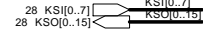
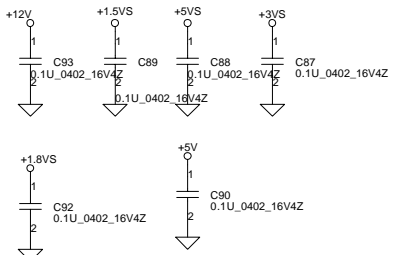
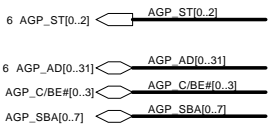
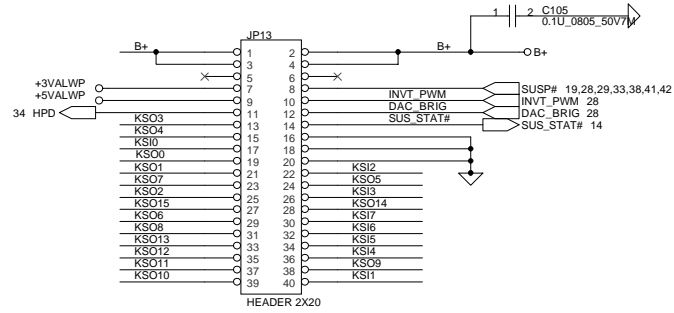
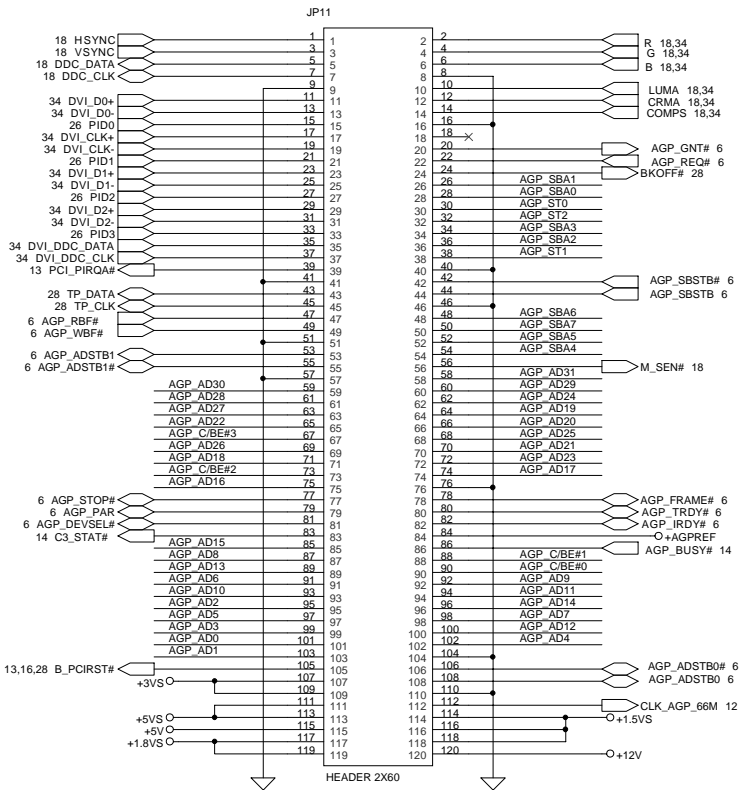
CD-ROM Connector



SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

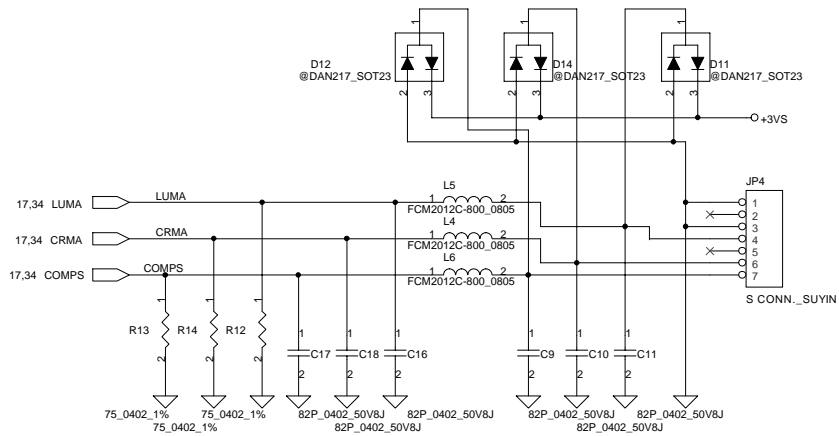
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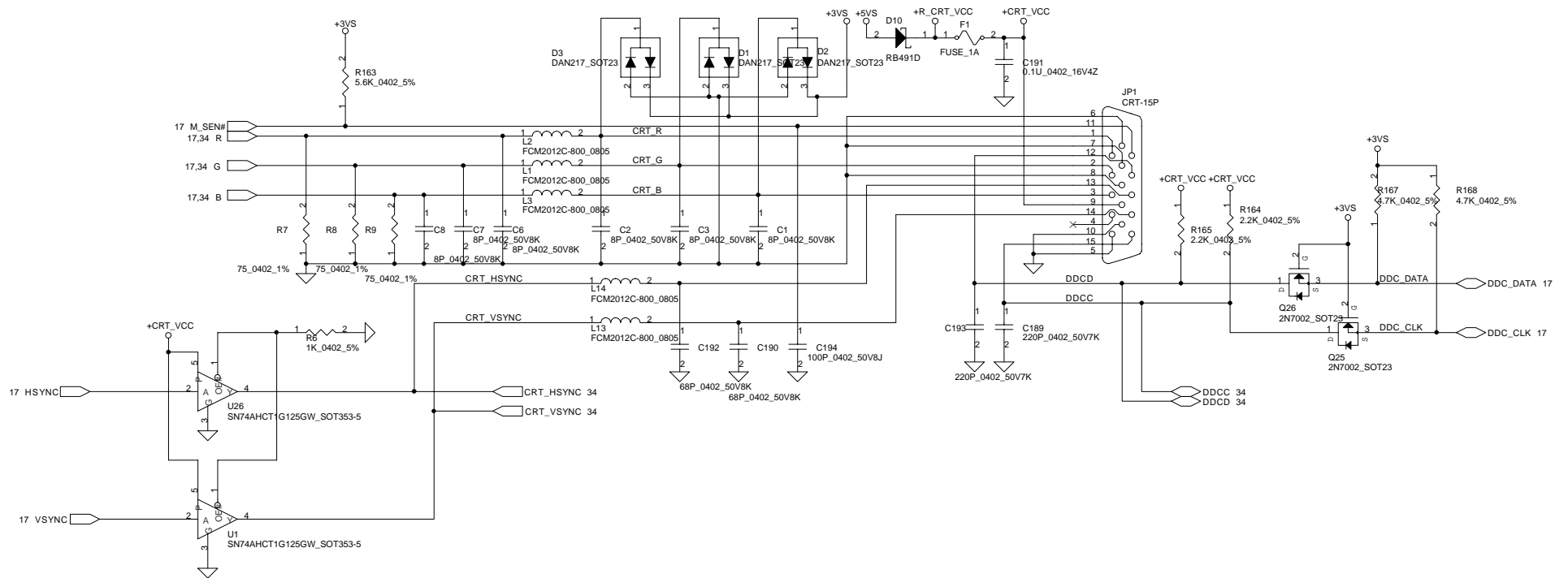


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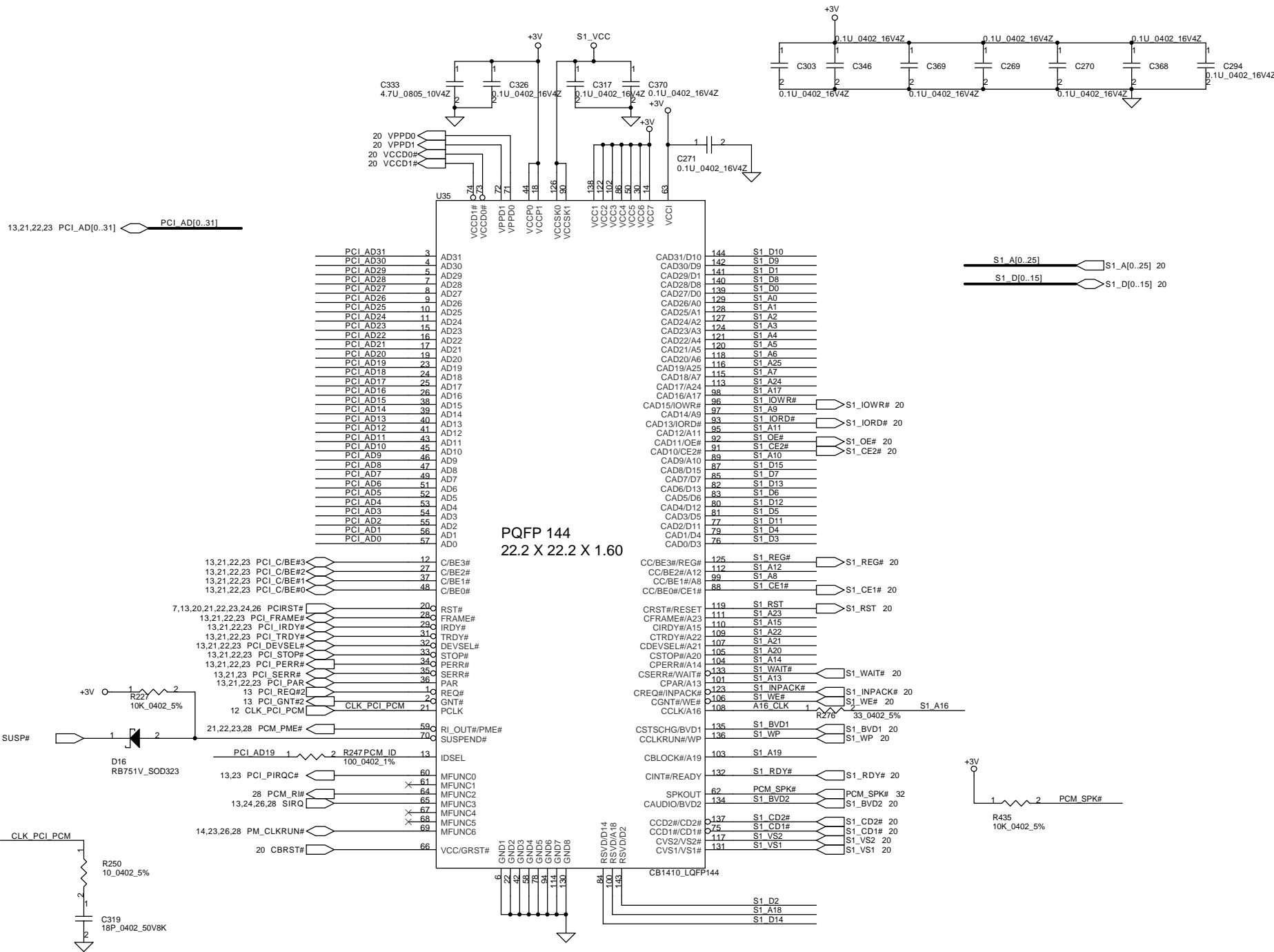


CRT Connector



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PQFP 144
22.2 X 22.2 X 1.60

PCI_AD31	3	AD31	CAD31/D10	144	S1 D10
PCI_AD30	4	AD30	CAD30/D9	142	S1 D9
PCI_AD29	5	AD29	CAD29/D1	141	S1 D1
PCI_AD28	7	AD28	CAD28/D8	140	S1 D8
PCI_AD27	8	AD27	CAD27/D0	139	S1 D0
PCI_AD26	9	AD26	CAD26/A0	129	S1 A0
PCI_AD25	11	AD25	CAD25/A1	128	S1 A1
PCI_AD24	10	AD24	CAD24/A2	127	S1 A2
PCI_AD23	15	AD23	CAD24/A2	124	S1 A3
PCI_AD22	16	AD22	CAD23/A3	121	S1 A4
PCI_AD21	17	AD21	CAD22/A4	120	S1 A5
PCI_AD20	19	AD20	CAD21/A5	120	S1 A6
PCI_AD19	23	AD19	CAD20/A6	118	S1 A6
PCI_AD18	24	AD18	CAD19/A25	116	S1 A25
PCI_AD17	25	AD17	CAD18/A7	115	S1 A7
PCI_AD16	26	AD16	CAD17/A24	113	S1 A24
PCI_AD15	38	AD15	CAD17/A24	98	S1 A17
PCI_AD14	39	AD14	CAD16/A17	96	S1 IOWR#
PCI_AD13	40	AD13	CAD15/IOVR#	97	S1 A9
PCI_AD12	41	AD12	CAD14/A9	93	S1 IORD#
PCI_AD11	42	AD11	CAD13/IORD#	93	S1 IORD#
PCI_AD10	43	AD10	CAD12/A11	95	S1 A11
PCI_AD9	46	AD9	CAD11/OE#	92	S1 OE#
PCI_AD8	47	AD8	CAD11/OE#	94	S1 CE2#
PCI_AD7	49	AD7	CAD10/CE2#	89	S1 A10
PCI_AD6	51	AD6	CAD9/A10	87	S1 D15
PCI_AD5	52	AD5	CAD8/D15	87	S1 D15
PCI_AD4	53	AD4	CAD7/D7	85	S1 D7
PCI_AD3	54	AD3	CAD6/D13	82	S1 D13
PCI_AD2	55	AD2	CAD5/D6	83	S1 D6
PCI_AD1	56	AD1	CAD5/D6	80	S1 D12
PCI_AD0	57	AD0	CAD4/D12	81	S1 D5
			CAD3/D5	77	S1 D11
			CAD2/D11	79	S1 D4
			CAD1/D4	76	S1 D3
			CAD0/D3		
			CC/BE3#/REG#	125	S1 REG#
			CC/BE2#/A12	112	S1 A12
			CC/BE1#/A8	99	S1 A8
			CC/BE0#/CE1#	88	S1 CE1#
			CRST#/RESET	119	S1 RST
			CFRAME#/A23	111	S1 A23
			CIRDY#/A15	110	S1 A15
			CTRDY#/A22	109	S1 A22
			CDEVSEL#/A21	107	S1 A21
			CSTOP#/A20	105	S1 A20
			CPERR#/A14	104	S1 A14
			CSERR#/WAIT#	133	S1 WAIT#
			CPAR#/A13	101	S1 A13
			CREQ#/INPACK#	106	S1 INPACK#
			CGNT#/WE#	108	S1 WE#
			CCLK/A16	108	A16 CLK
			CSTSCHG#/BVD1	135	S1 BVD1
			CLKRUN#/WP	136	S1 WP
			CBLOCK#/A19	103	S1 A19
			CINT#/READY	132	S1 RDY#
			SPKOUT	62	PCM_SPK#
			CAUDIO/BVD2	134	S1 BVD2
			CCD2#/CD2#	137	S1 CD#
			CCD1#/CD1#	75	S1 CD1#
			CVS2/VS2#	117	S1 VS2
			CVS1/VS1#	131	S1 VS1

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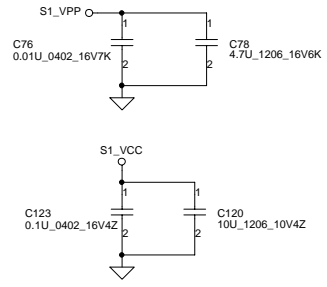
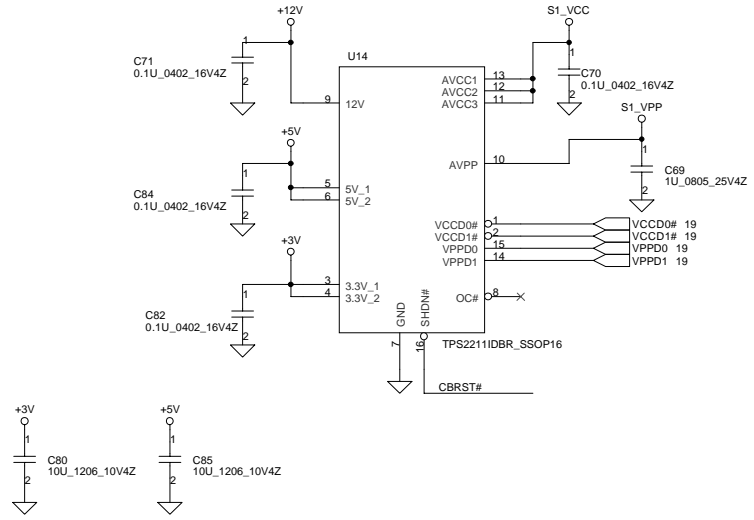
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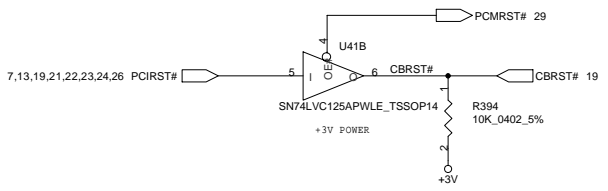
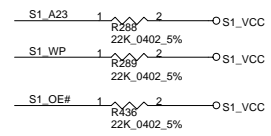
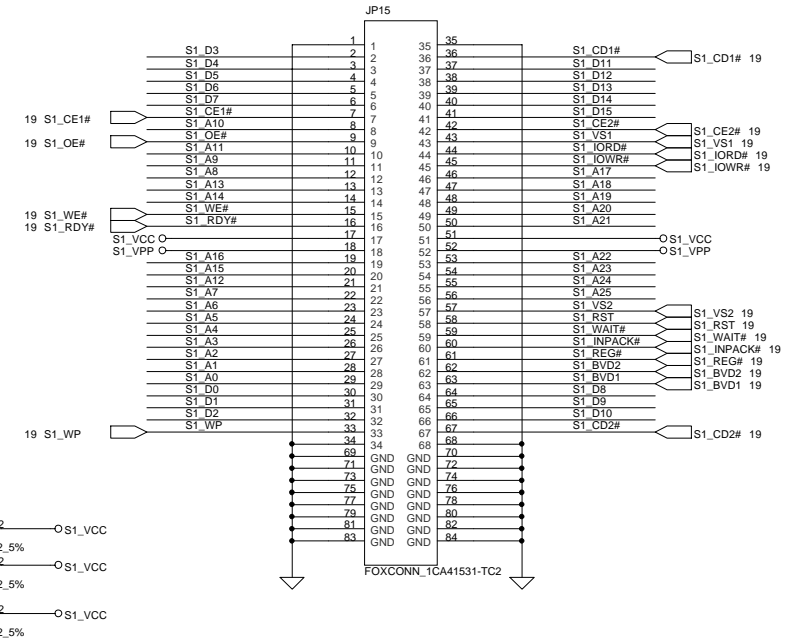
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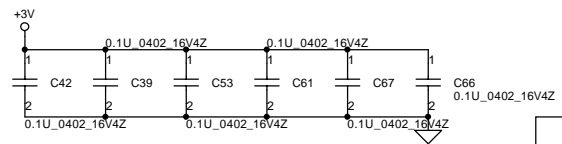
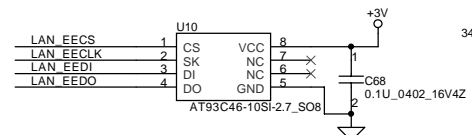
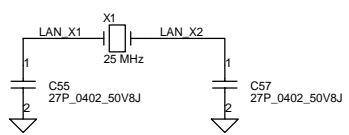
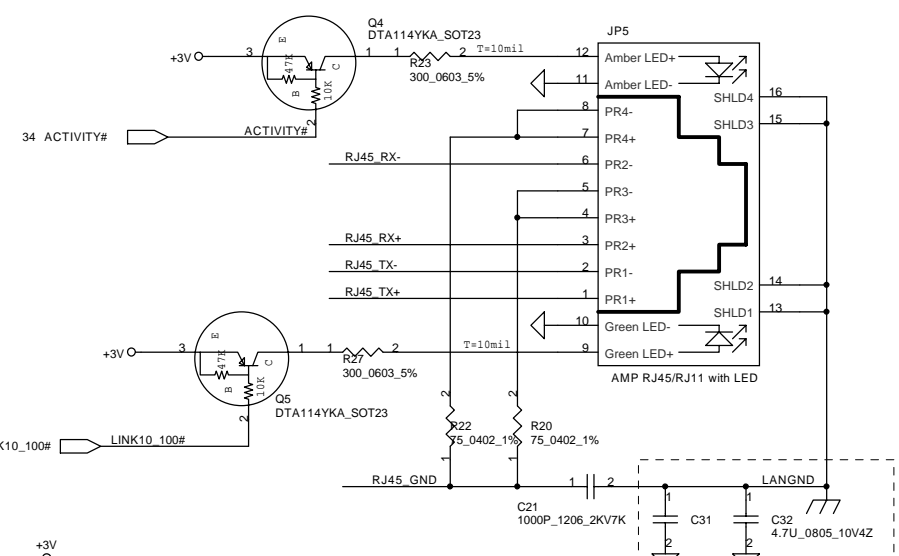
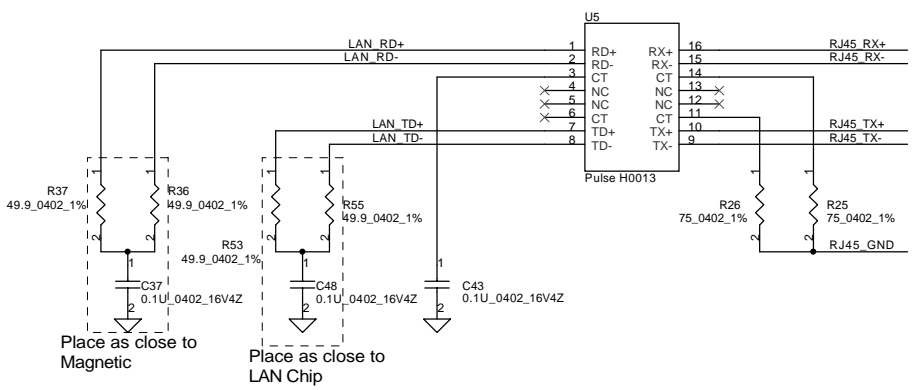
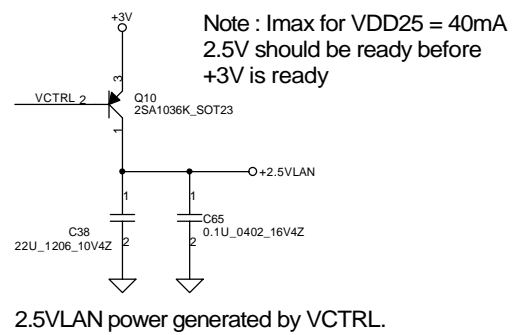
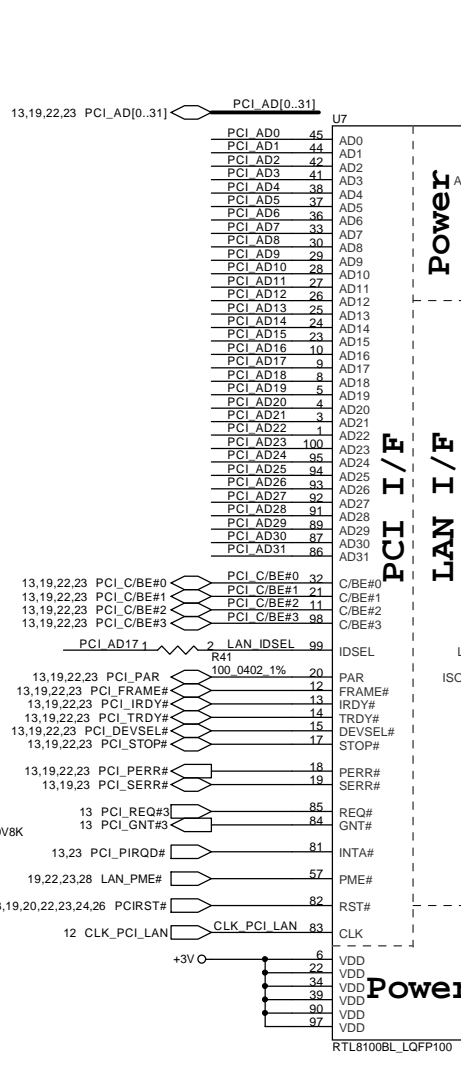
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PCMCIA Power Controller



CardBus Socket





Termination plane should be copied to chassis ground and also depends on safety concern

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13,19,21,23 PCI_AD[0..31] PCI_AD[0..31]

IEEE 1394 VT6307S

PCI AD0	25	AD0
PCI AD1	24	AD1
PCI AD2	20	AD2
PCI AD3	18	AD3
PCI AD4	18	AD4
PCI AD5	16	AD5
PCI AD6	15	AD6
PCI AD7	14	AD7
PCI AD8	11	AD8
PCI AD9	10	AD9
PCI AD10	9	AD9
PCI AD11	8	AD10
PCI AD12	7	AD11
PCI AD13	4	AD12
PCI AD14	2	AD13
PCI AD15	2	AD14
PCI AD16	117	AD15
PCI AD17	116	AD16
PCI AD18	115	AD17
PCI AD19	114	AD18
PCI AD20	113	AD19
PCI AD21	107	AD20
PCI AD22	109	AD21
PCI AD23	106	AD22
PCI AD24	103	AD23
PCI AD25	102	AD24
PCI AD26	101	AD25
PCI AD27	98	AD26
PCI AD28	97	AD27
PCI AD29	96	AD28
PCI AD30	95	AD29
PCI AD31	94	AD30

13,19,21,23 PCI_C/BE#0 12 CBE0#
 13,19,21,23 PCI_C/BE#1 1 CBE1#
 13,19,21,23 PCI_C/BE#2 119 CBE2#
 13,19,21,23 PCI_C/BE#3 104 CBE3#

PCI_AD16 1 R191 105 IDSEL
 100 0402 1% 120 FRAME#
 13,19,21,23 PCI_FRAME# 121 IRDY#
 13,19,21,23 PCI_IRDY# 123 TRDY#
 13,19,21,23 PCI_TRDY# 124 DEVSEL#
 13,19,21,23 PCI_DEVSEL# 125 PERR#
 13,19,21,23 PCI_PERR# 127 PAR#
 13,19,21,23 PCI_PAR# 128 REQ#
 13 PCI_REQ#0 93
 13 PCI_GNT#0 92
 13 PCI_GNT#1 91
 13 PCI_PIRQ#0 89
 13 PCI_PIRQ#1 88
 7,13,19,20,21,23,24,26 PCIRST# 90
 12 CLK_PCI_1394 PCI_CLK

VSSC2 22
 VSSC1 112
 VSS0 33
 VSS9 39
 VSS8 38
 VSS7 23
 VSS6 13
 VSS5 8
 VSS4 6
 VSS3 108
 VSS2 100
 VSS1 100
 VSS0 91
 RAMVSS 31

NC21 64
 NC19 54
 NC18 53
 NC17 52
 NC16 51
 NC15 49
 NC14 48
 NC13 45
 NC12 44
 NC11 43
 NC10 41
 NC9 37
 NC8 35
 NC7 55

I2CEENA 43
 XI 57
 XO 58
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EECS 26
 EEEO 27
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 SCL/EECK 29

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 NC1 39
 NC2 40

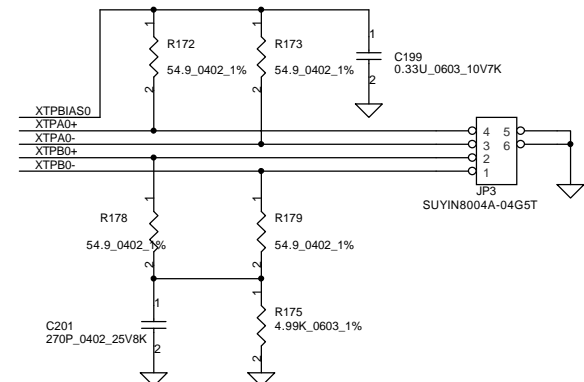
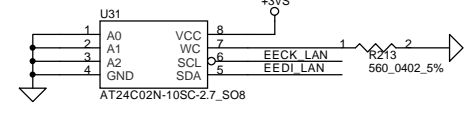
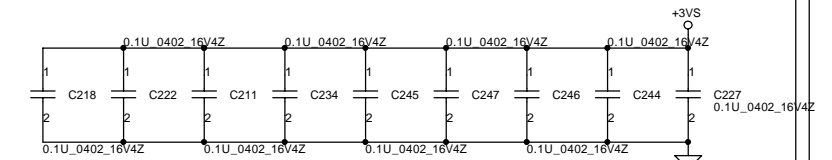
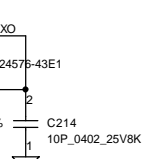
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XREXT 63

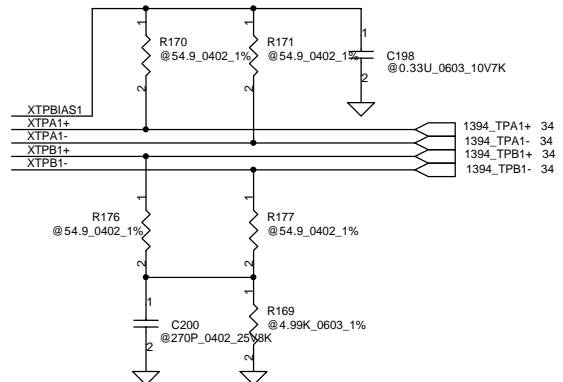
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 XTPB0P 68
 XTPA0M 69
 XTPA0P 70
 XTPBIAS0 71

XTPB1M 74
 XTPB1P 75
 XTPA1M 76
 XTPA1P 77
 XTPBIAS1 78

NC3 81
 NC4 82
 NC5 83
 NC6 84
 NC7 85
 NC8 55

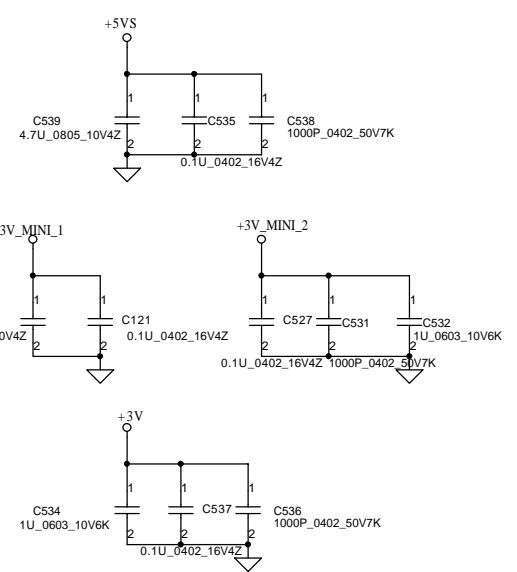
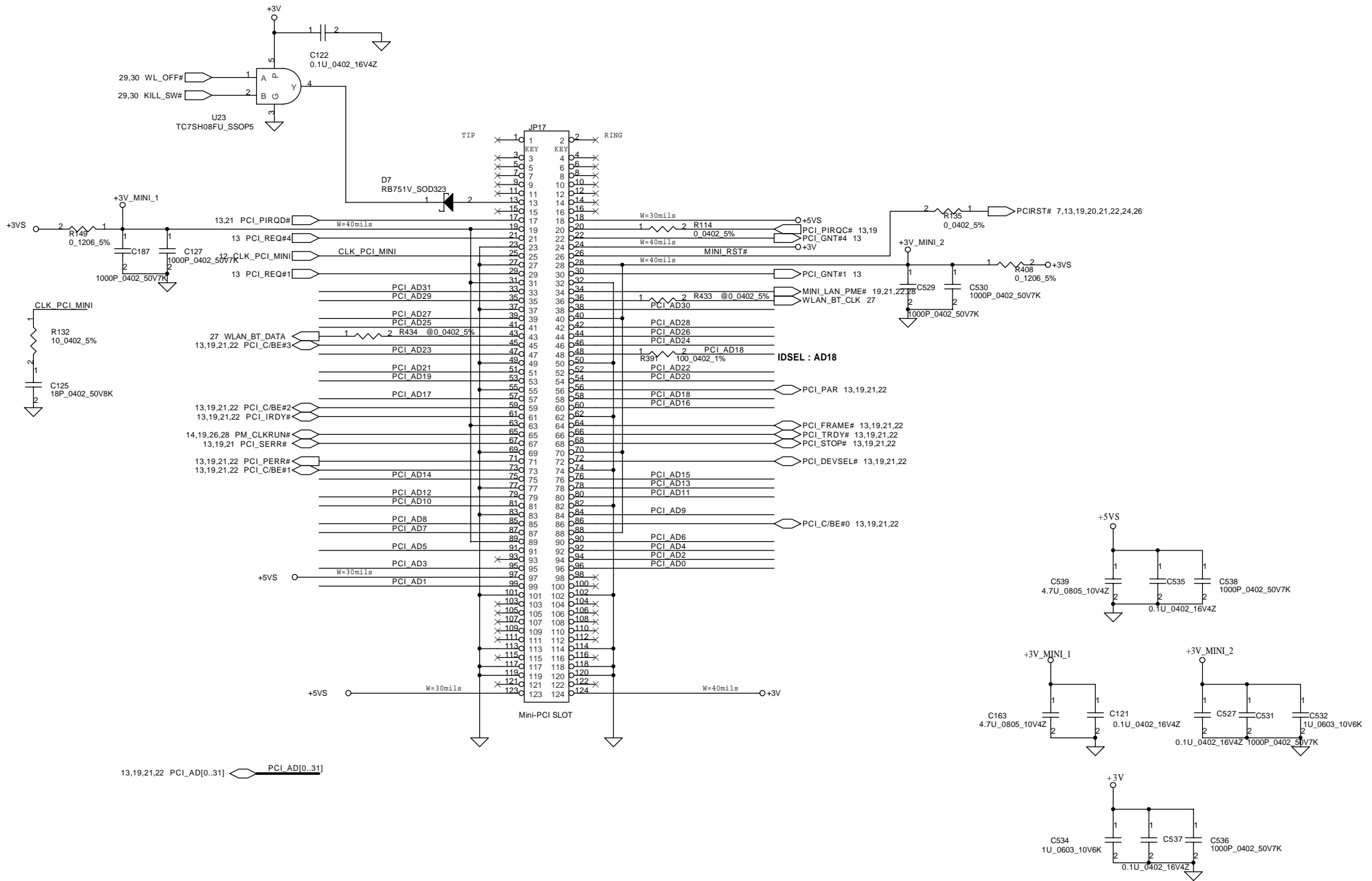


Note: These components need to close to chip pins.



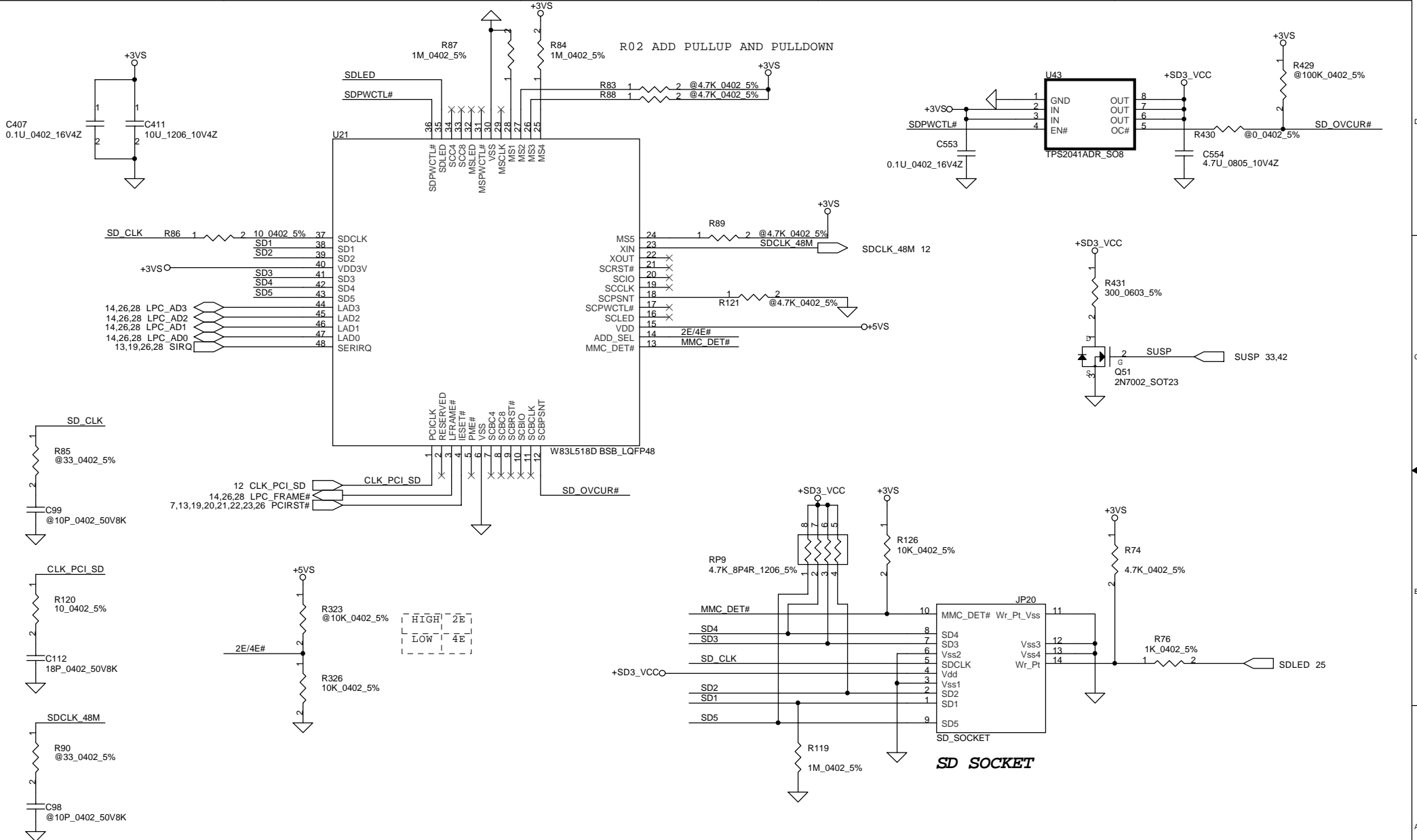
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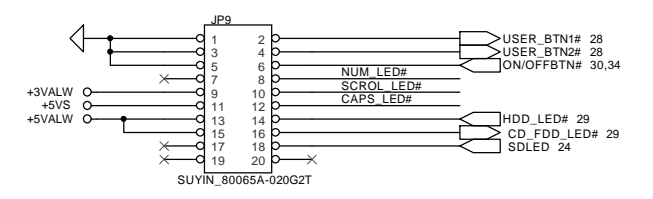
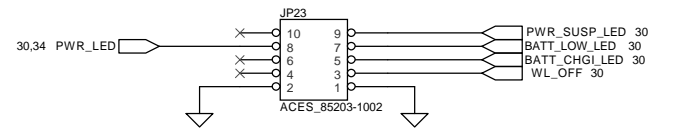
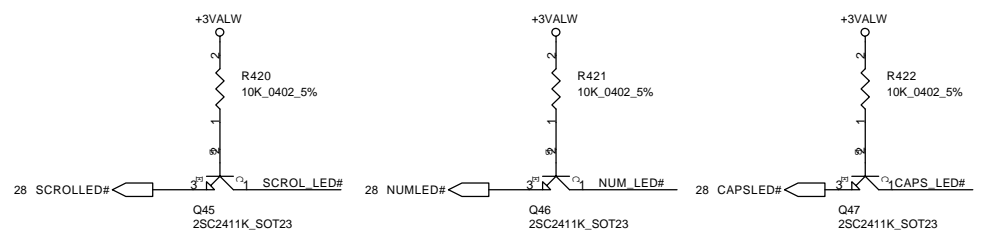
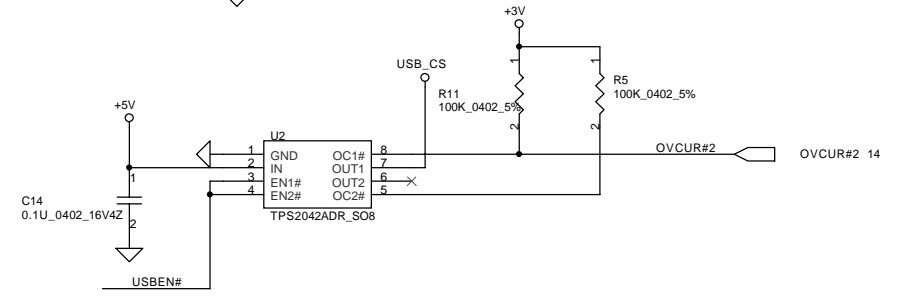
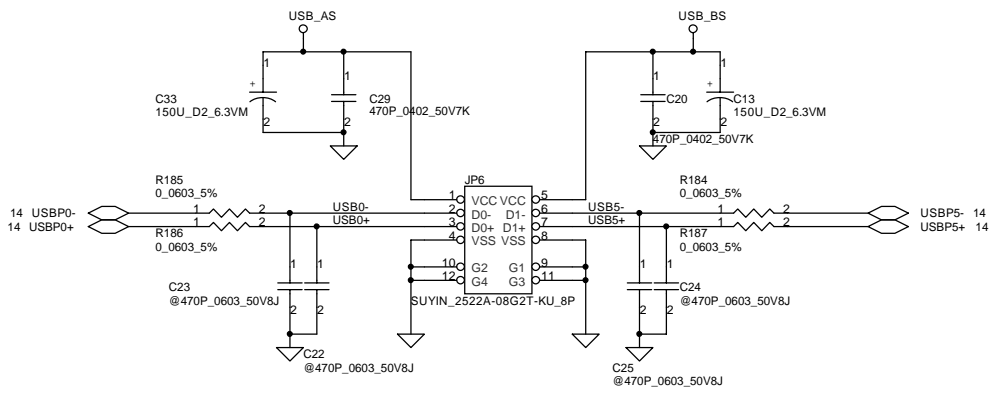
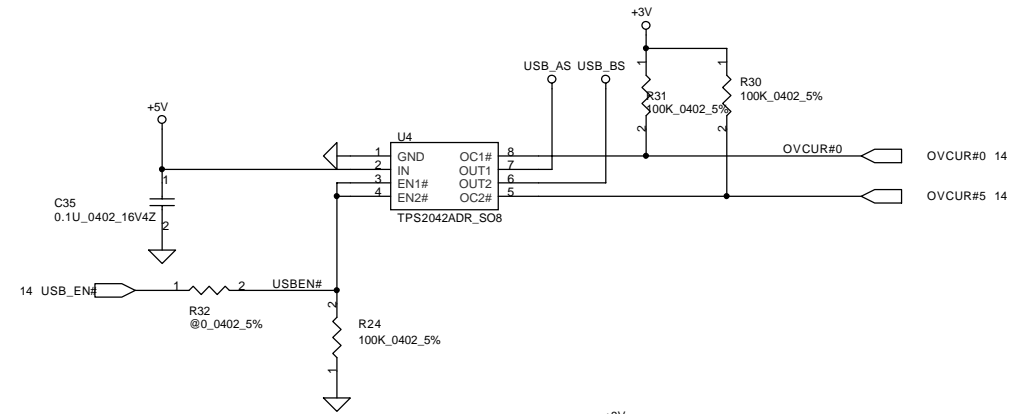
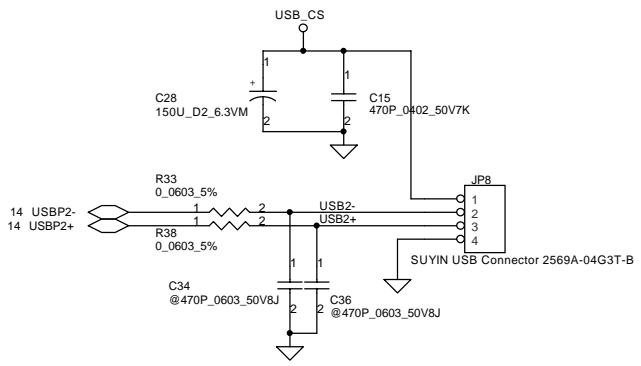
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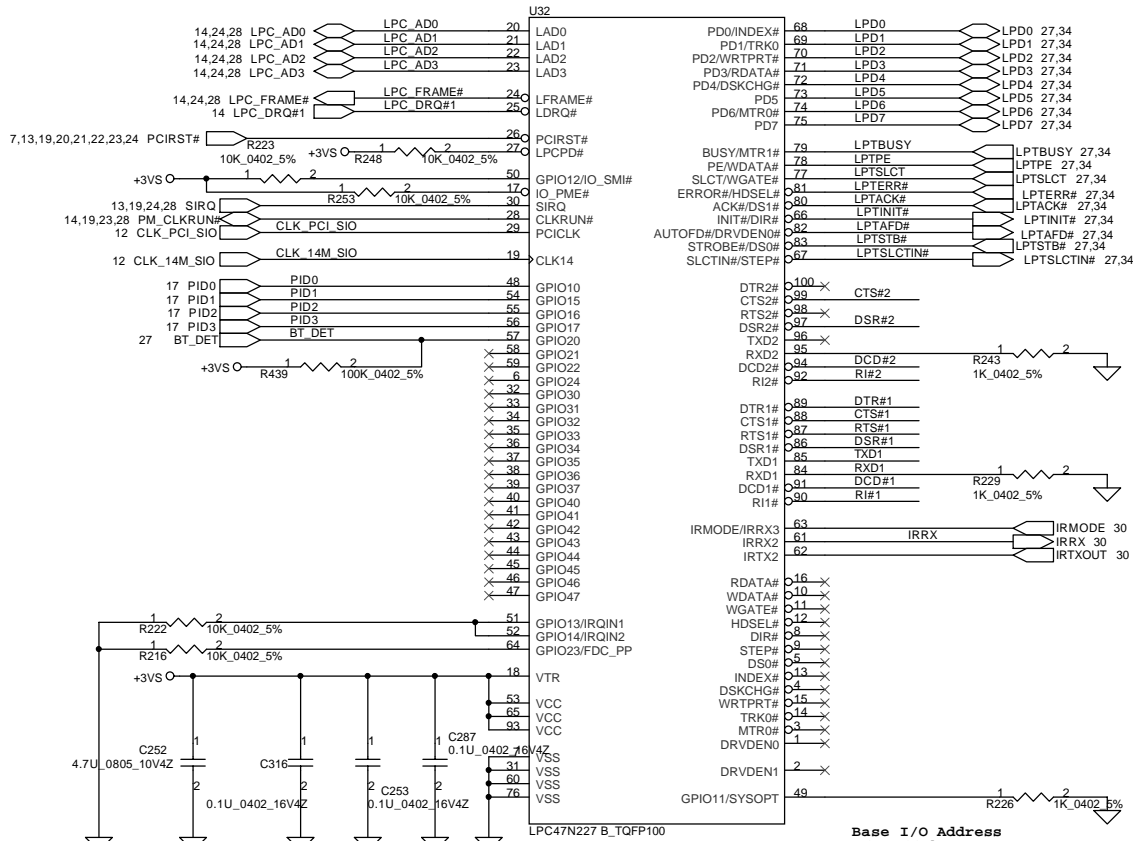
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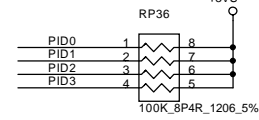
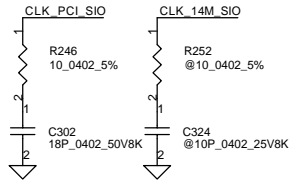
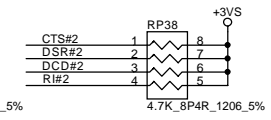
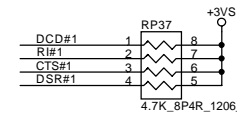
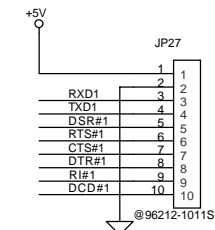
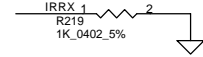
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SUPER I/O SMC FDC47N227



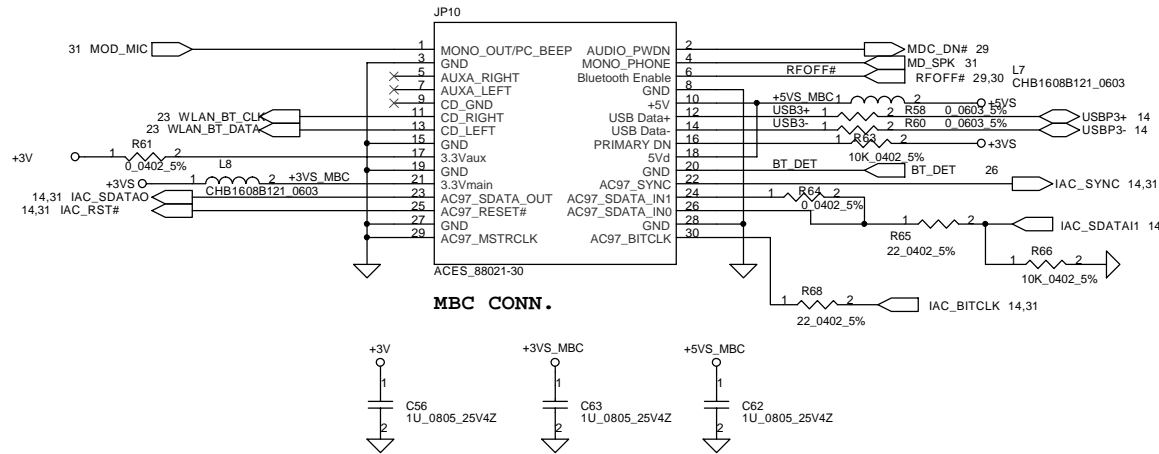
Base I/O Address
 * 0 = 02Eh
 1 = 04Eh



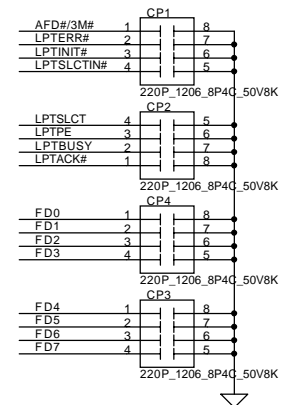
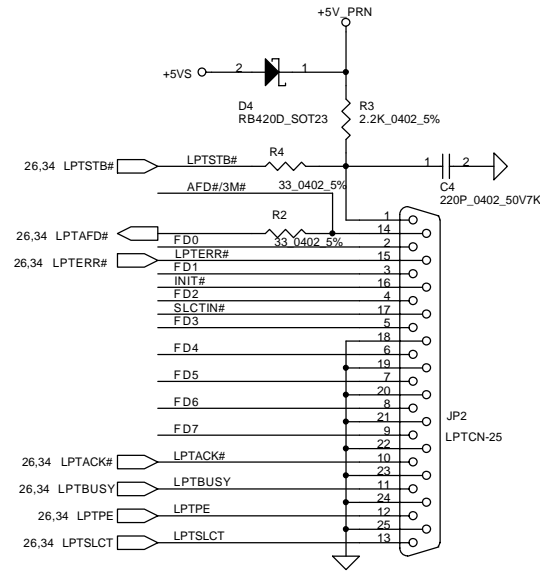
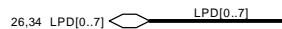
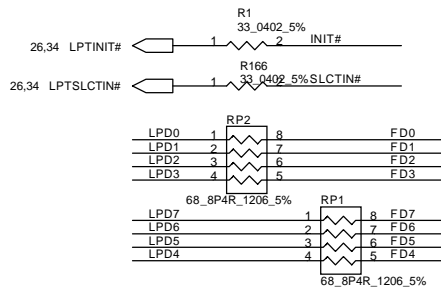
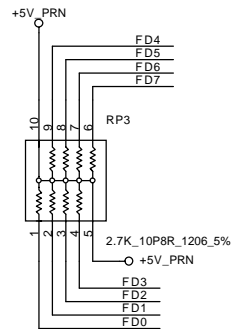
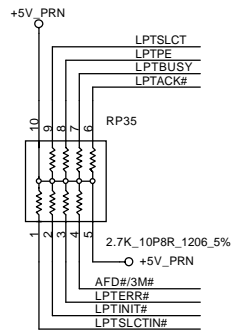
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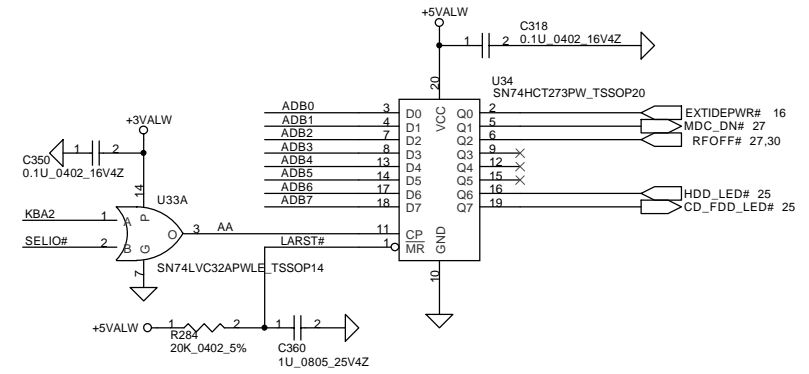
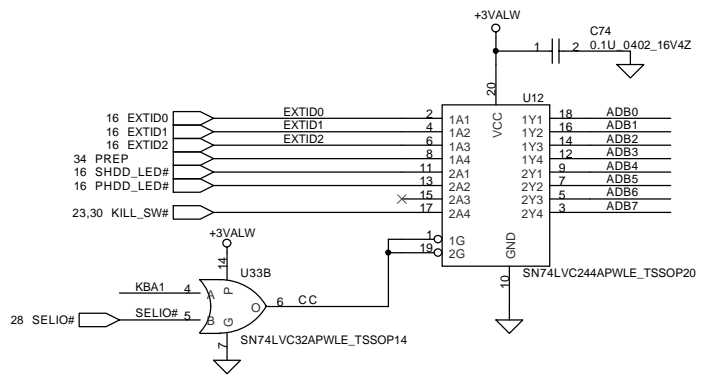
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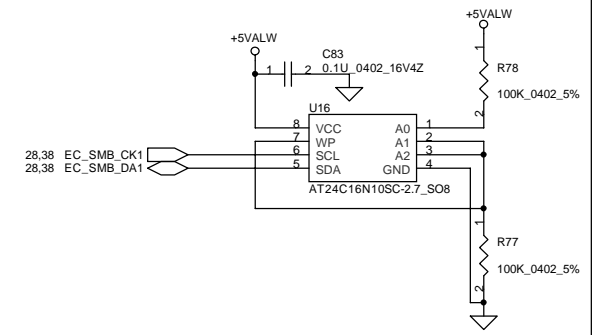
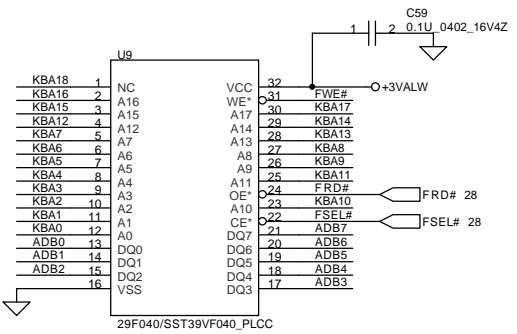
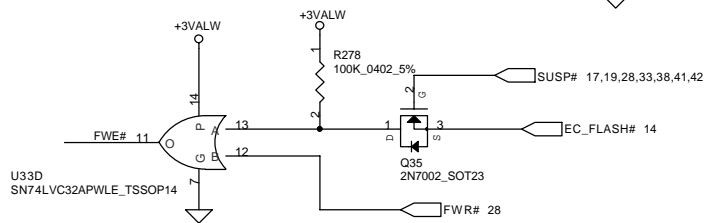
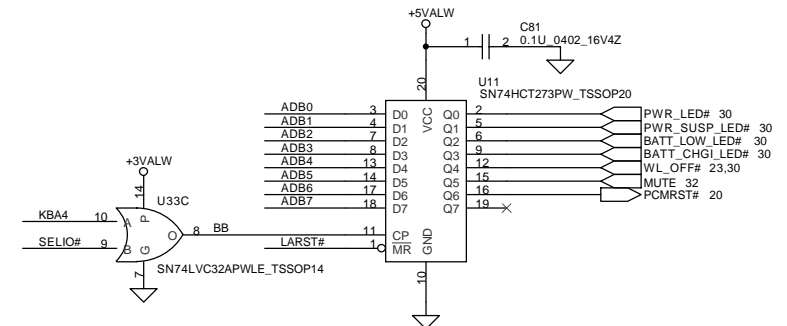
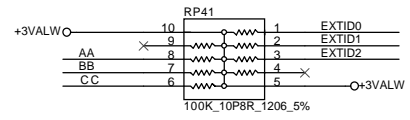
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EXTID2	EXTID1	EXTID0	Module
0	0	0	FDD
0	0	1	CDROM
0	1	1	2ndHDD
1	1	1	NO Module



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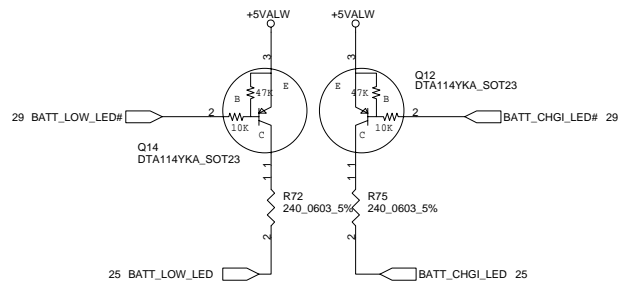
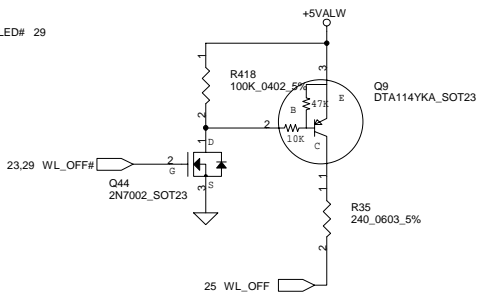
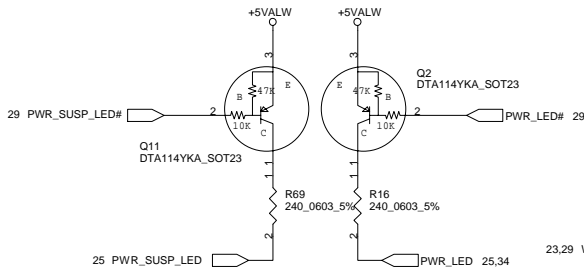
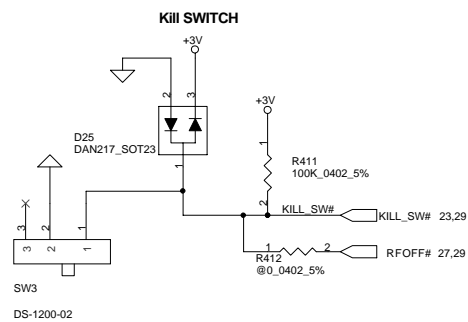
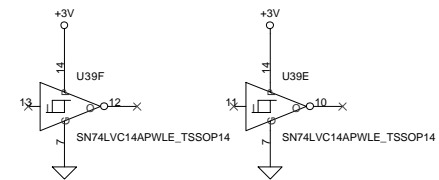
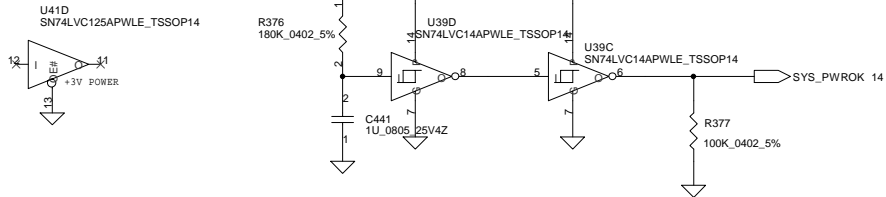
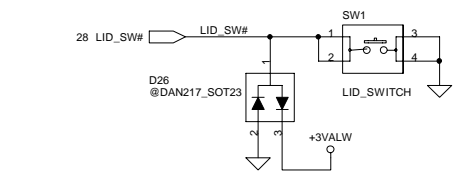
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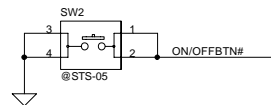
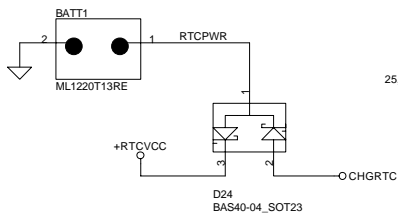
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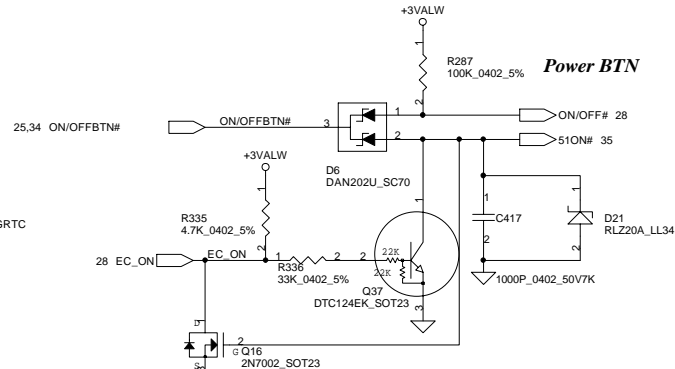
Power ON Circuit



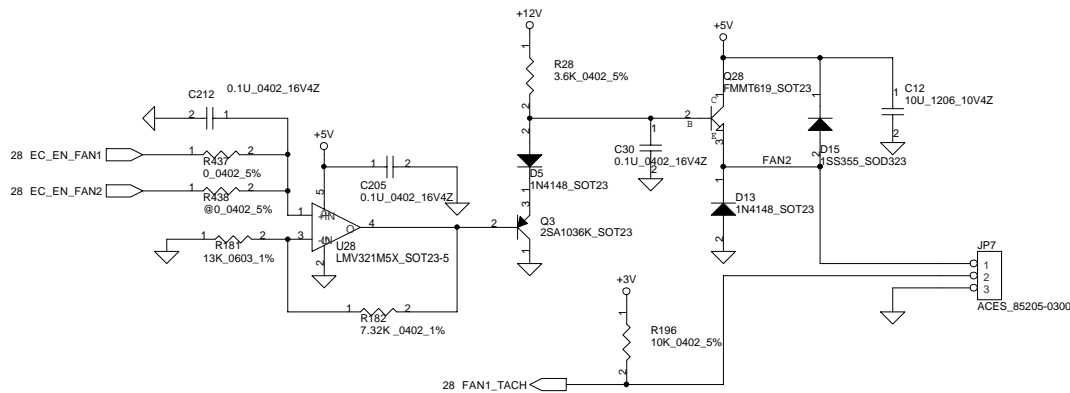
RTC Battery



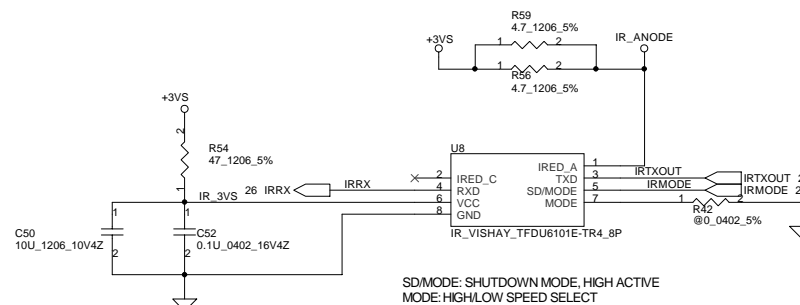
Power BTN



Fan Control circuit



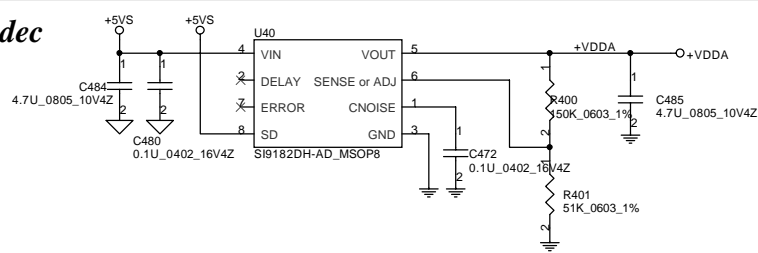
FIR Module



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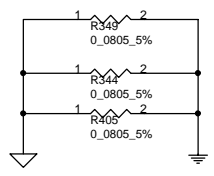
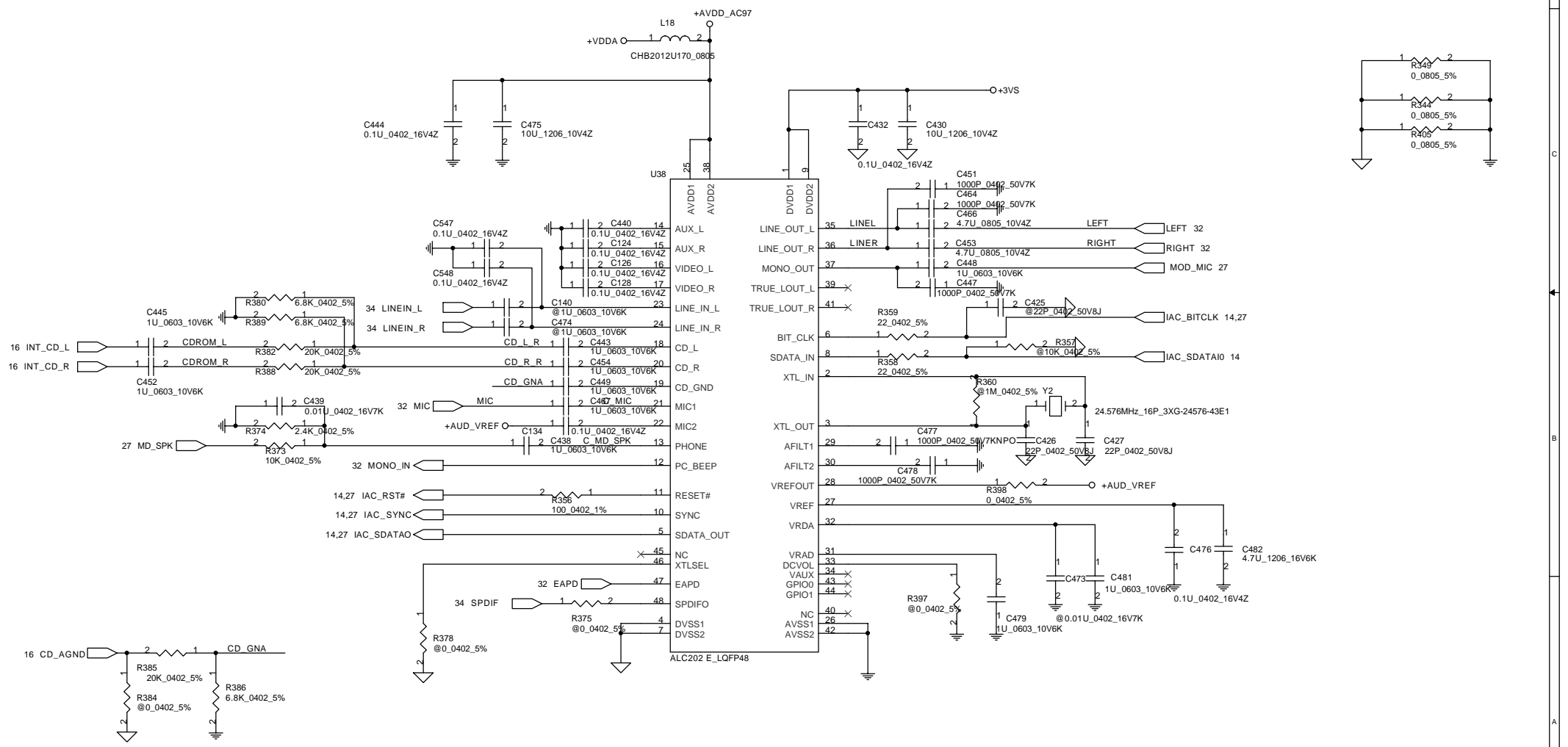
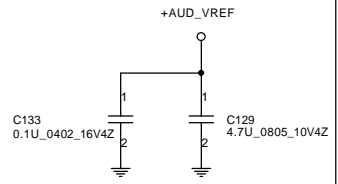
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AC97 Codec



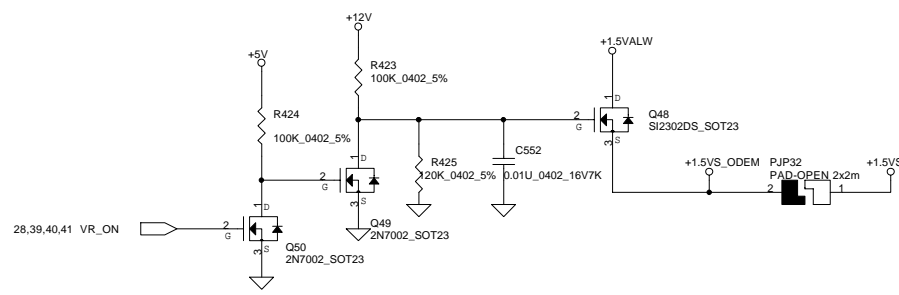
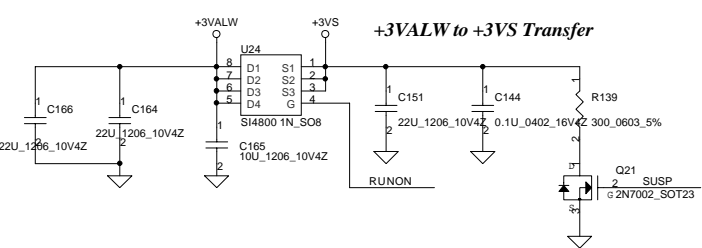
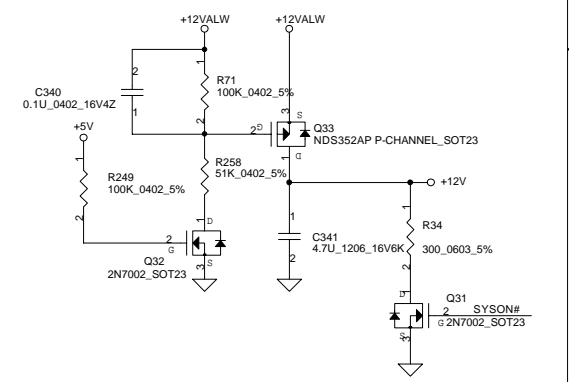
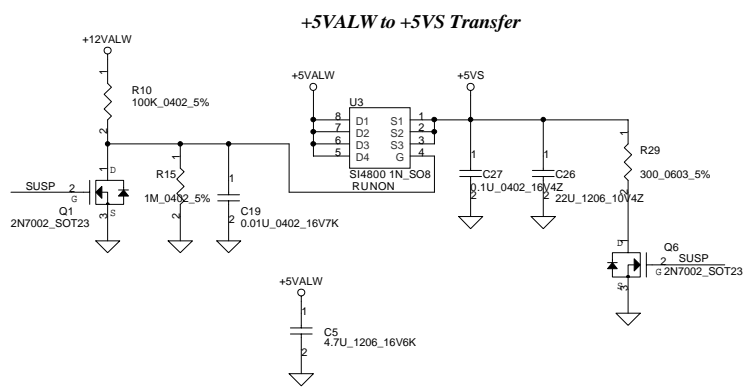
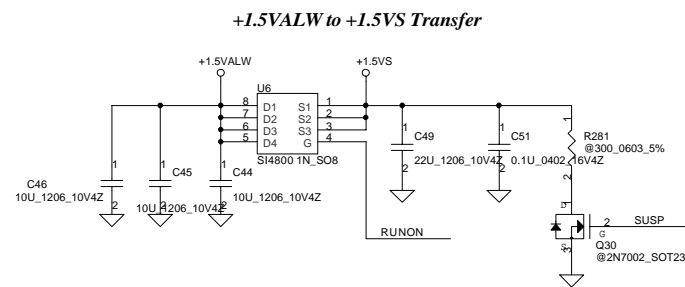
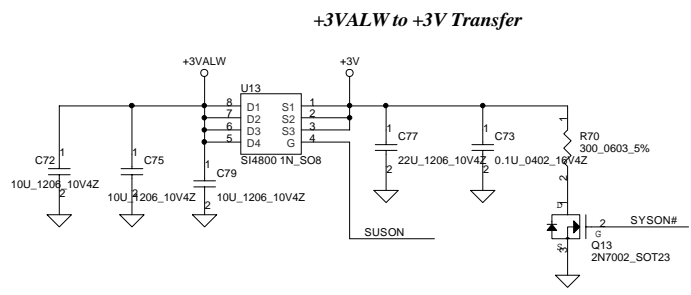
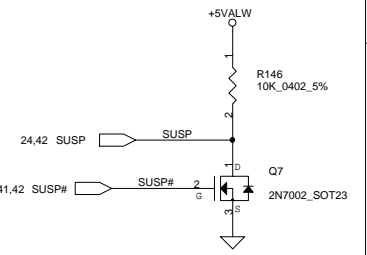
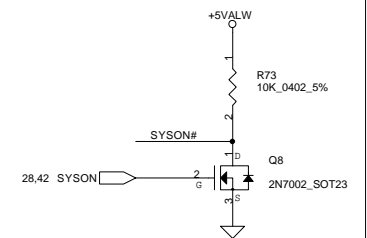
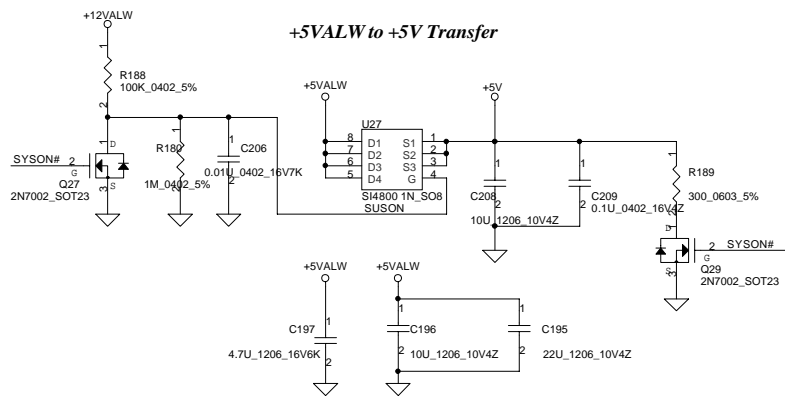
R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

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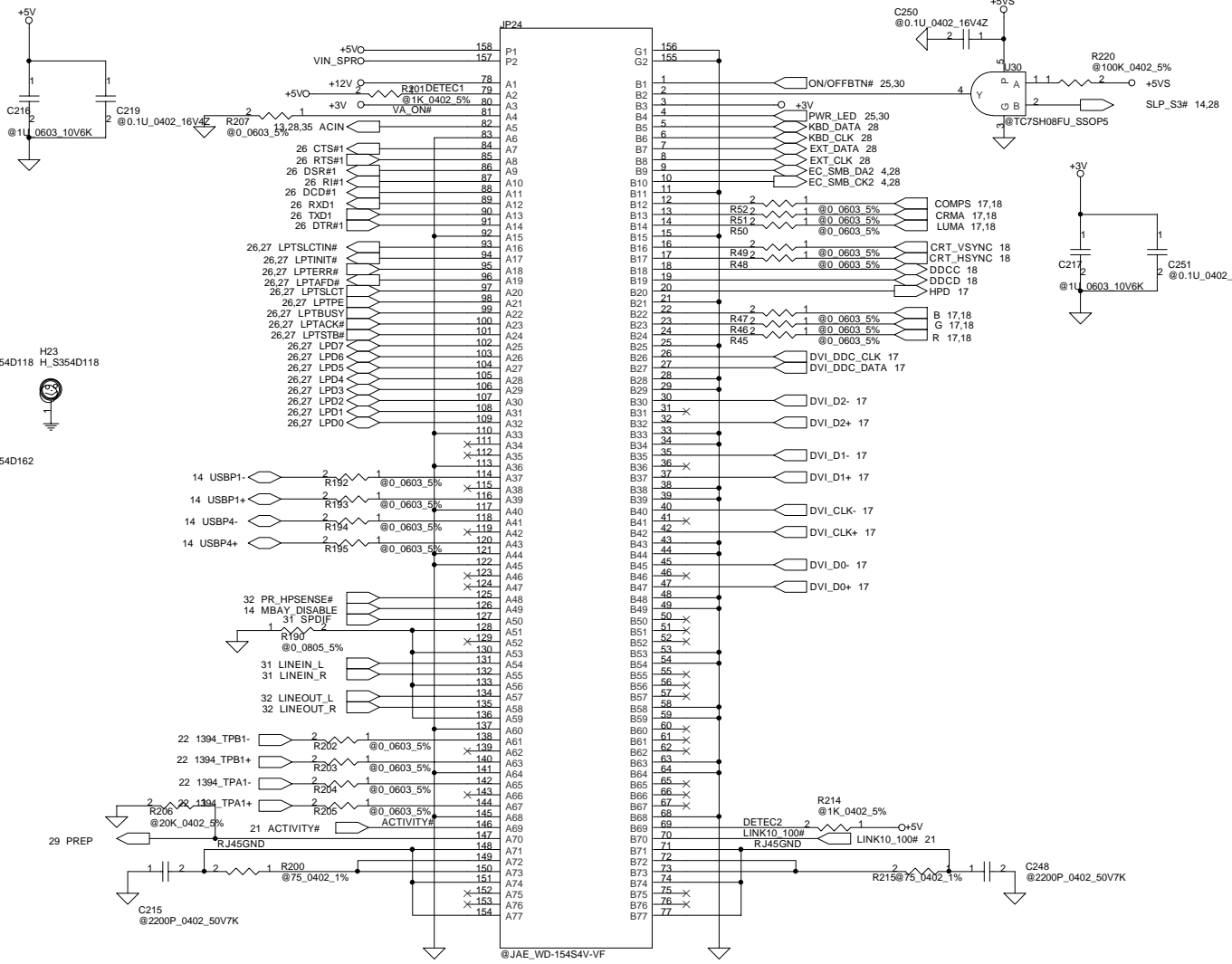
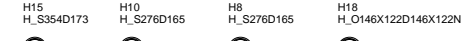
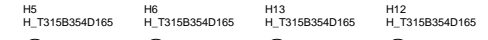
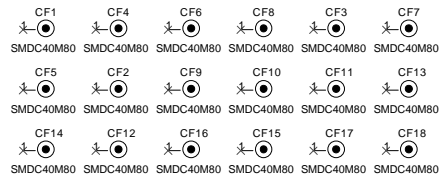
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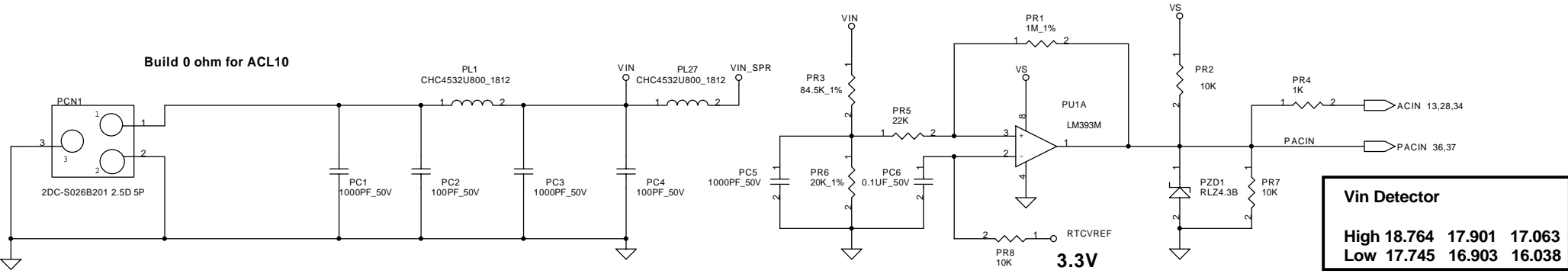
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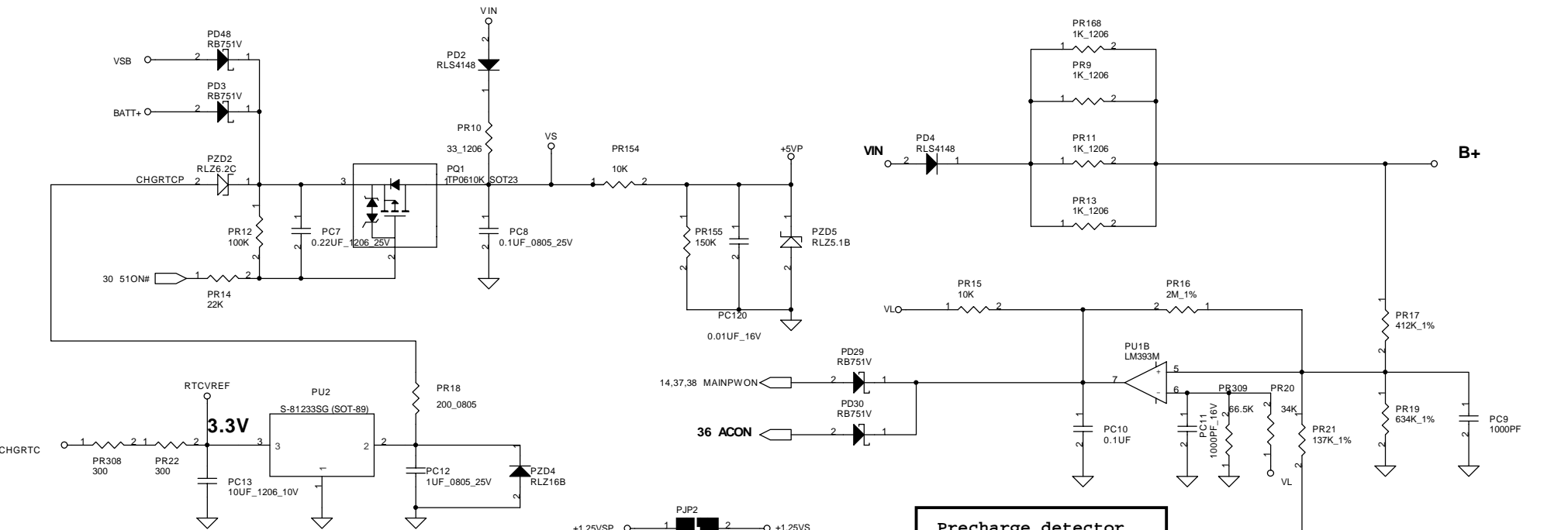
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Build 0 ohm for ACL10

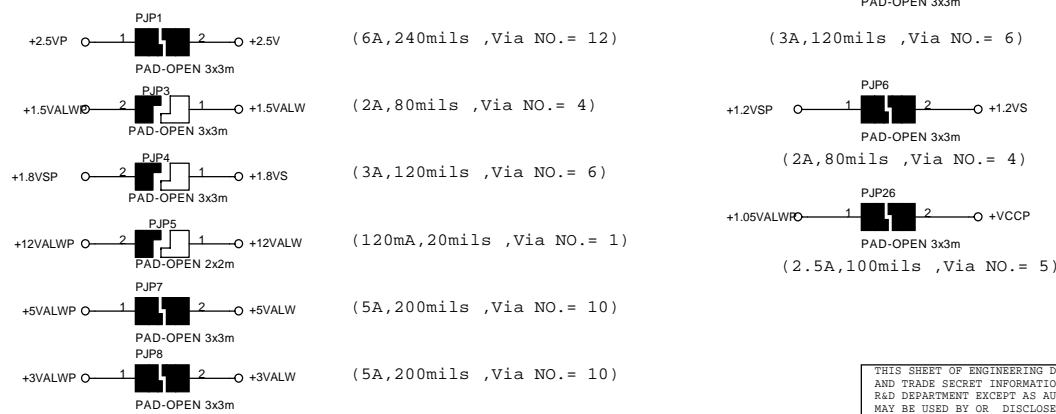


Vin Detector		
High	18.764	17.901 17.063
Low	17.745	16.903 16.038



Precharge detector AC ADAPTOR		
16.69	16.05	15.42
15.6	15.02	14.35

Precharge detector AC ADAPTOR		
6.33	6.12	5.92
5.227	5.09	4.85



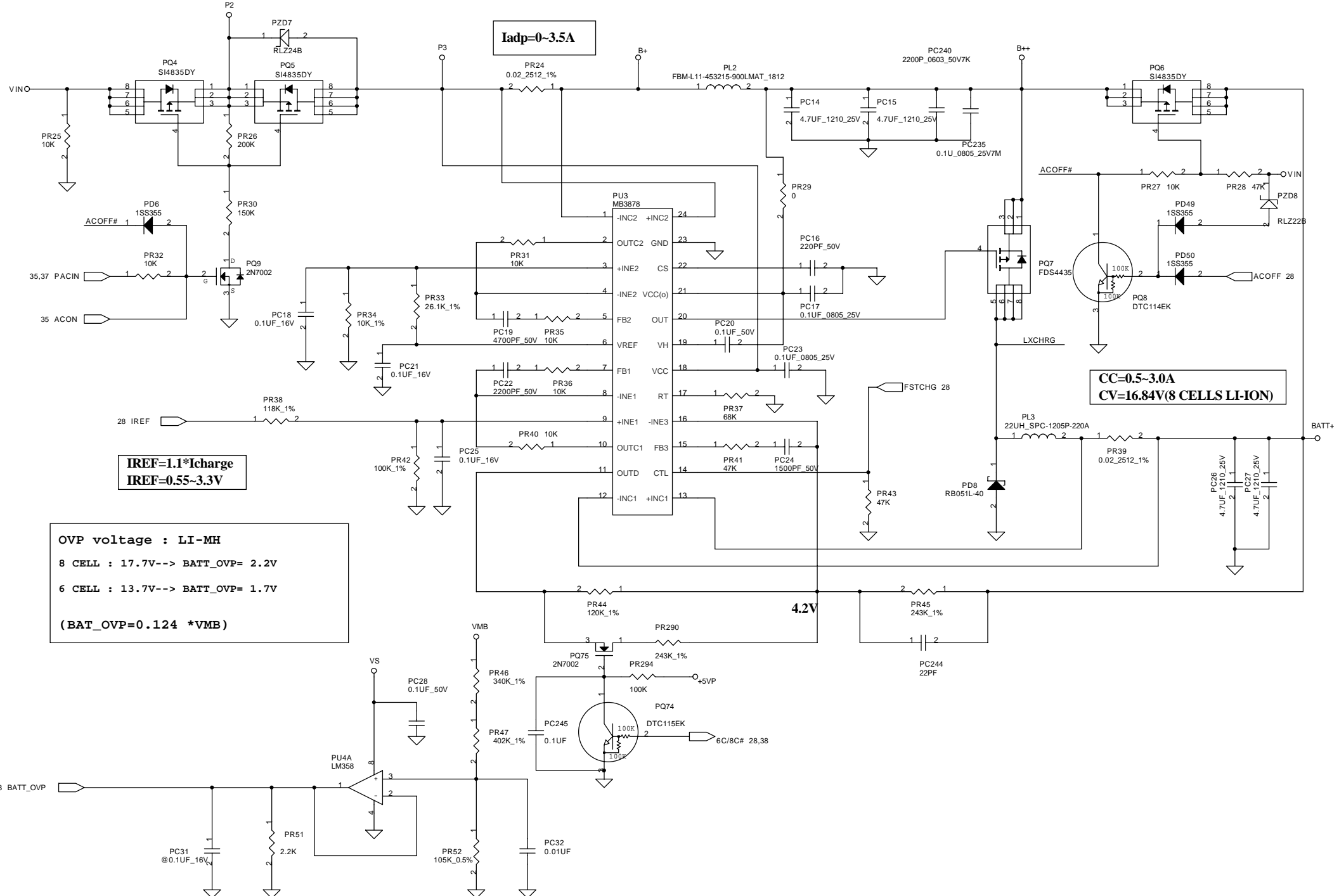
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Iadp=0-3.5A

IREF=1.1*Icharge
IREF=0.55~3.3V

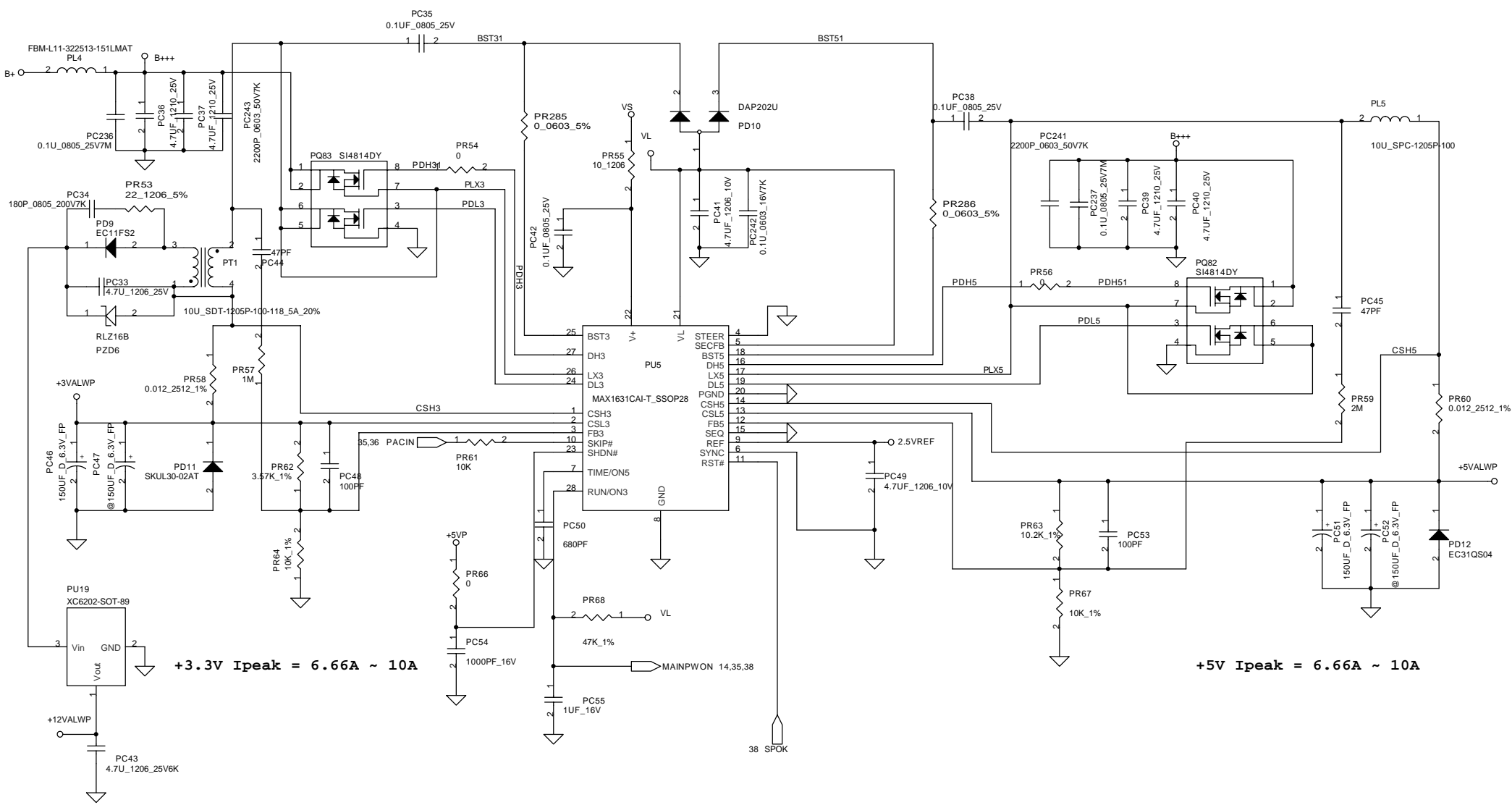
OVP voltage : LI-MH
8 CELL : 17.7V--> BATT_OVP= 2.2V
6 CELL : 13.7V--> BATT_OVP= 1.7V
(BAT_OVP=0.124 *VMB)

CC=0.5-3.0A
CV=16.84V(8 CELLS LI-ION)

4.2V

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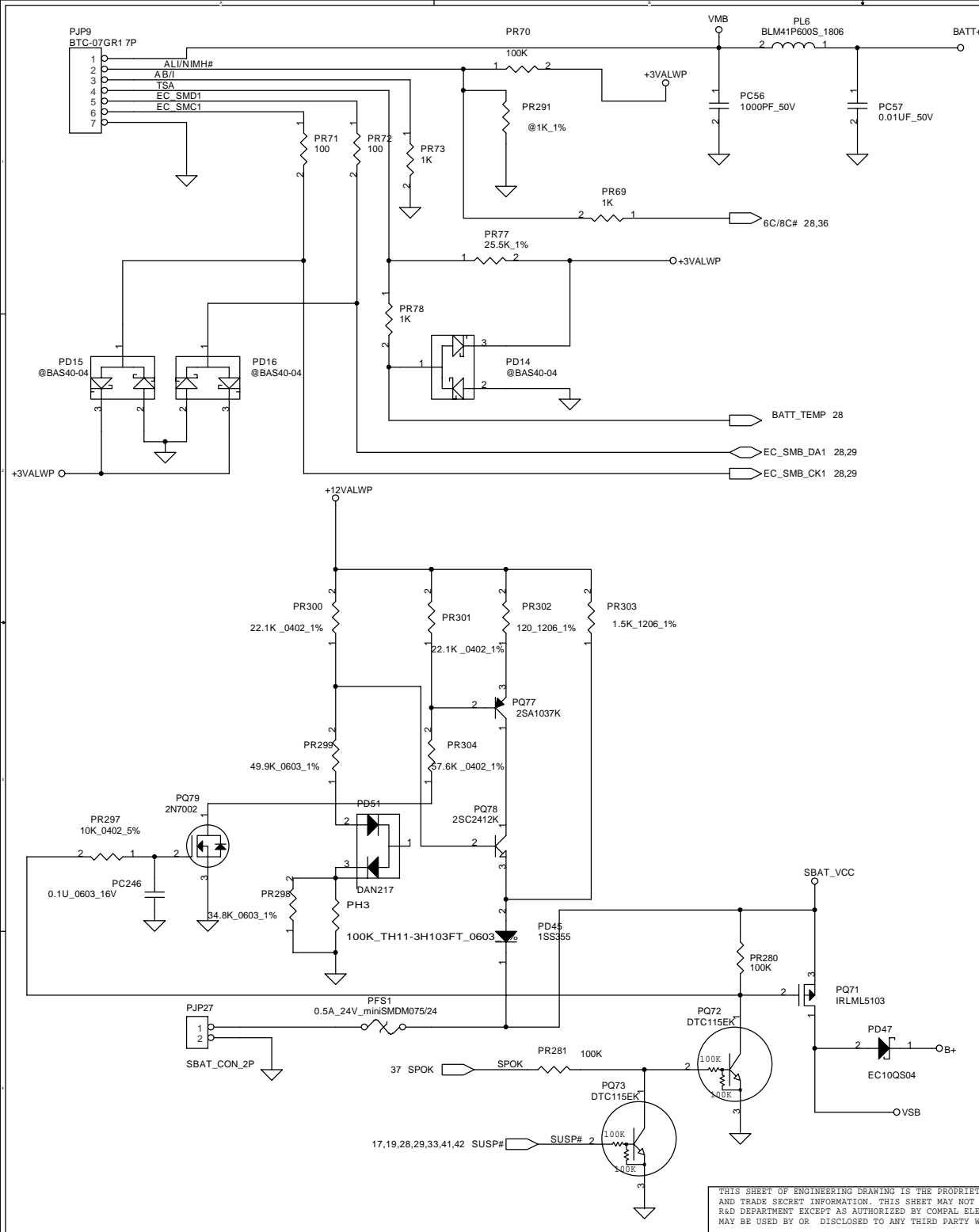


+3.3V I_{peak} = 6.66A ~ 10A

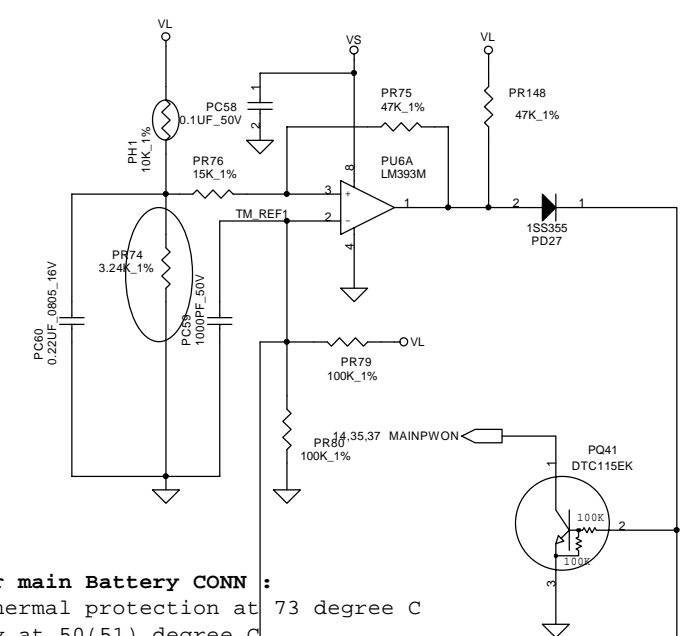
+5V I_{peak} = 6.66A ~ 10A

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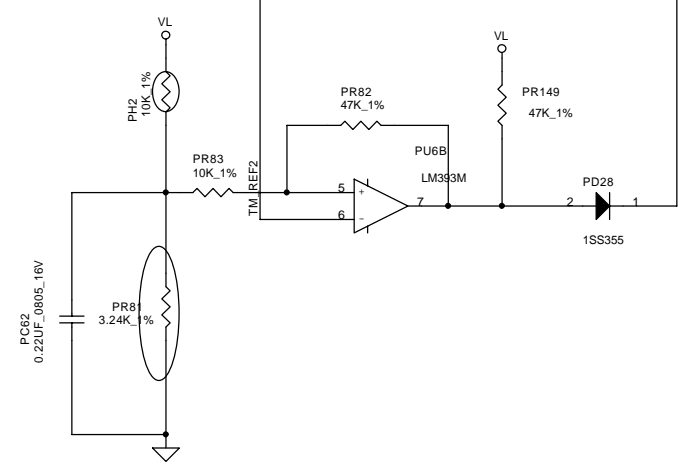
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PH1 under CPU bottom side :
 CPU thermal protection at 82 degree C
 Recovery at 48 degree C



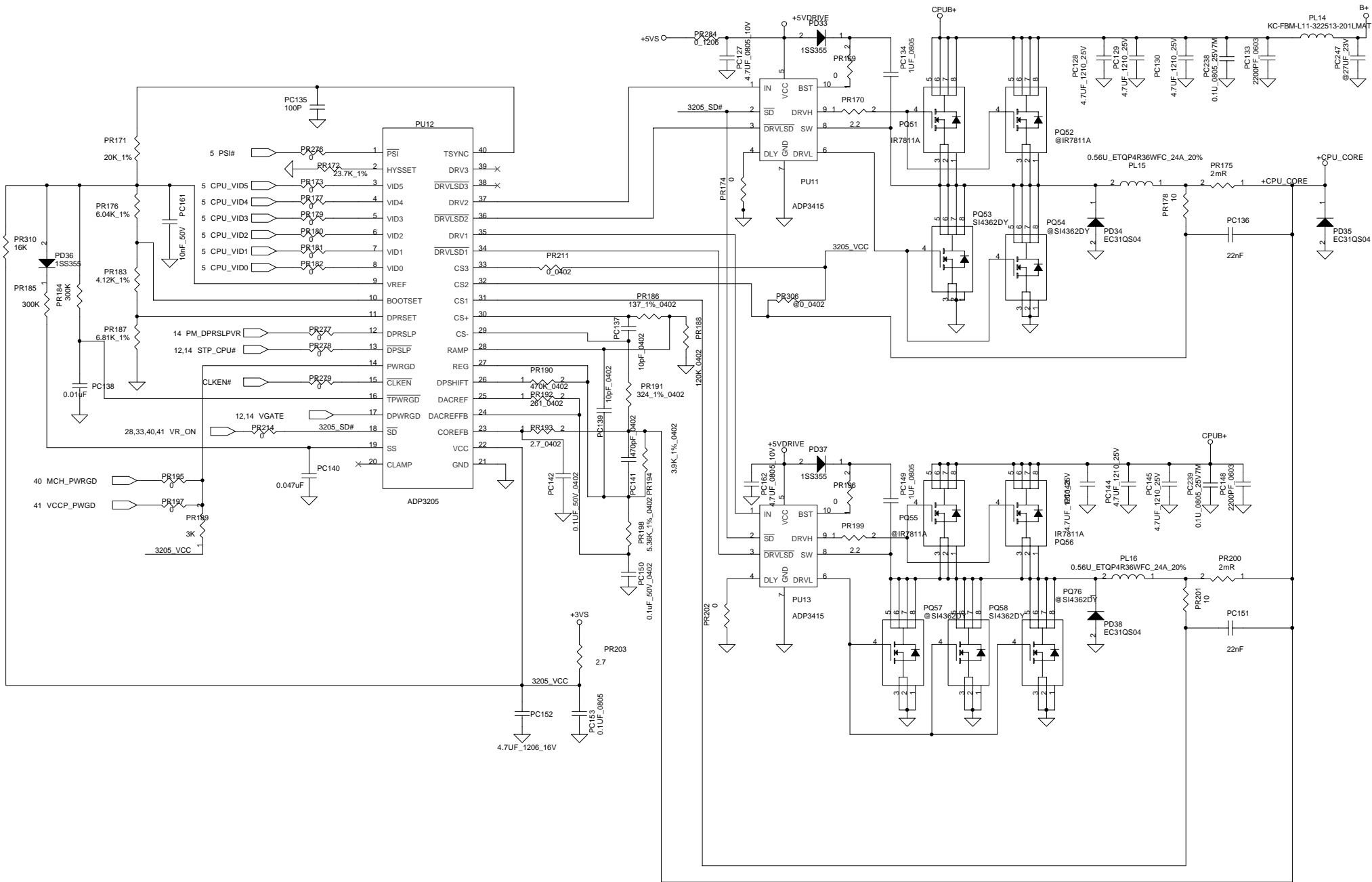
PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50(51) degree C



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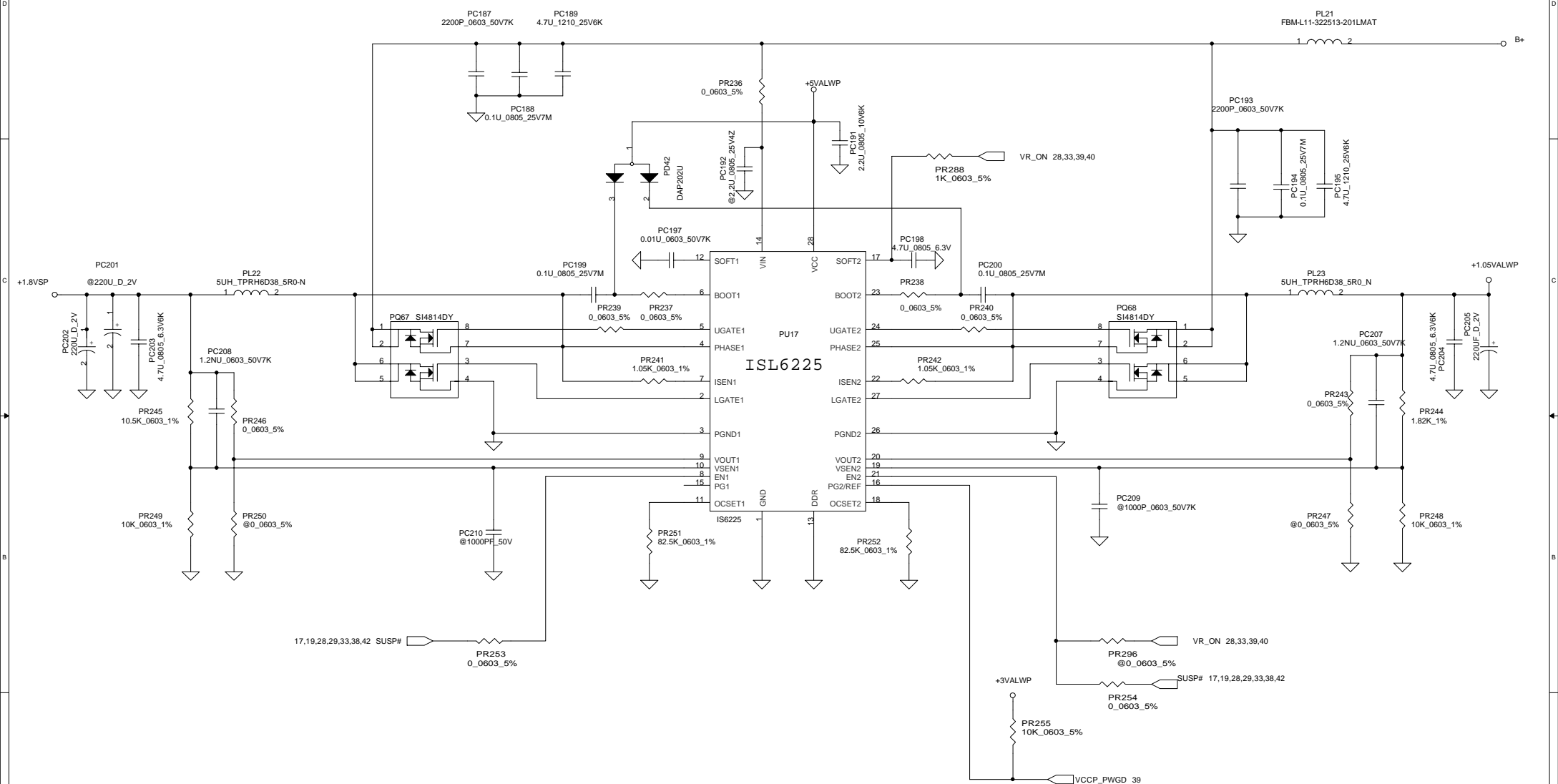
CPU-CORE



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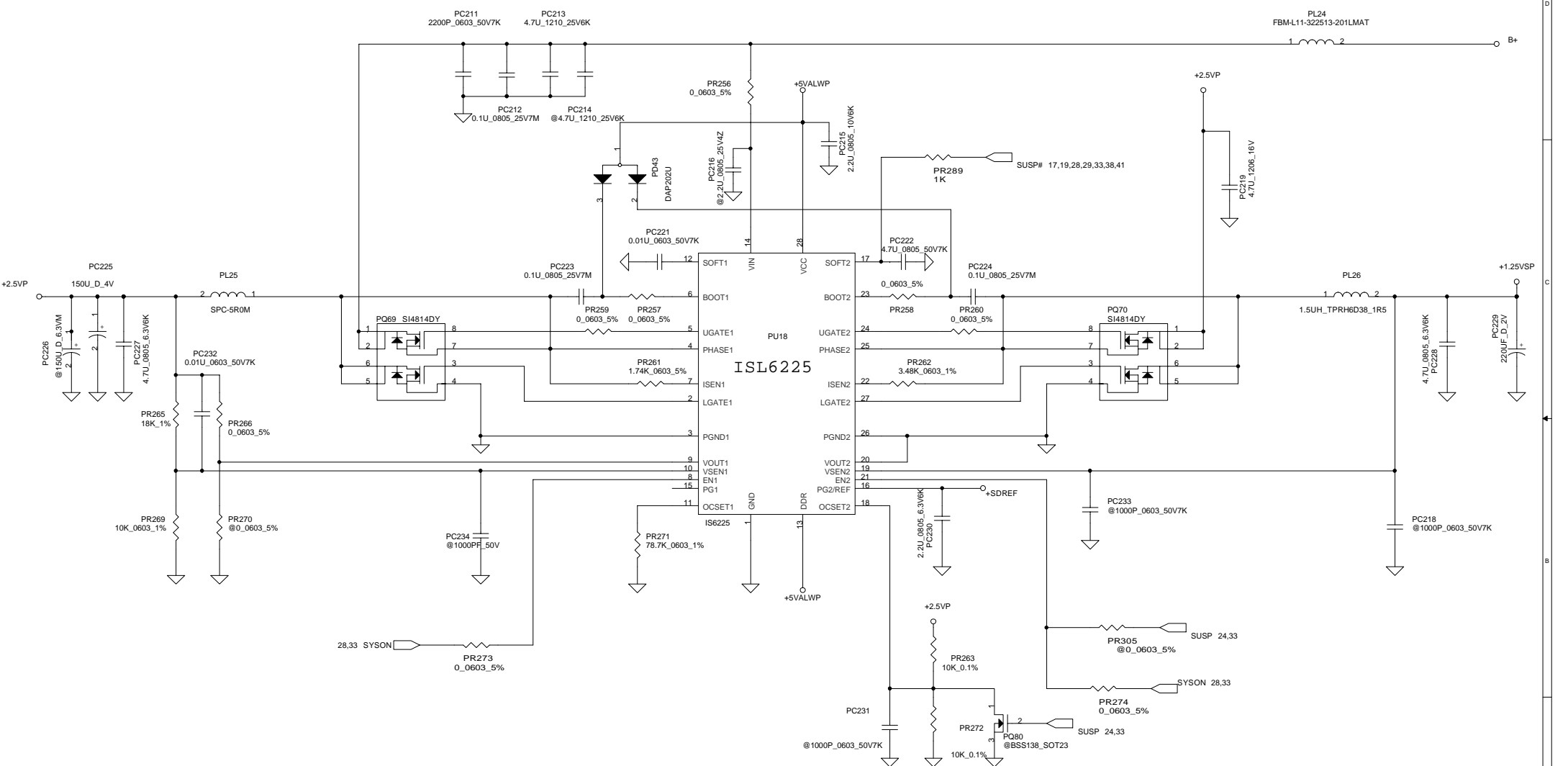
+1.8VALWP/+1.05VALWP



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+2.5VP/+1.25VSP



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1.	IDE reset signal level error	Change signal level from 3V to 5V		P16	Delete D8,D9,R144,R147 Add U44,U45		DVT
2.	LED light not enough	Change VCC from +3VALW to +5VALW		P25	Add Q45,Q46,Q47 Add R420,R421,R422		DVT
3.	Change flash ROM size	Change from 4Mb to 8Mb		P29	Delete U9 Add U42		DVT
4.	Change flash ROM size	Change from 8Mb to 4Mb		P29	Delete U42, C549, R419, JP28 Add U9, C59		PVT
5.	Change USB Power	Change USB Power from +5VALW to +5V		P25	Change U2.2, U4.2 form +5VALW to +5V		PVT
6.	Noise when system boot	Change PCM_SPK# sequence		P19	Add R435 on PCM_SPK# and pull up to +3V		PVT
7.	Some CF card can't read	Pull up S1_OE#		P20	Add R436 on S1_OE# to pull up to S1_VCC		PVT
8.	Change FAN Connector	Change FAN Connector		P30	Change FAN Connector JP7 from 4-Pin to 3-Pin		PVT
9.	Add Bluetooth Detect Pin	Add Bluetooth Detect Pin		P30	Add Bluetooth Detect Pin form Super I/O GPIO20 to JP10 Pin20		PVT

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Title		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		change cpu core from two phase to one phase		39	1.delete PC127,PU11,PD33,PR169,PR170, PC134,PR174,PQ51,PQ52,PQ53, PQ54,PC128,PC129,PC130,PC238, PC133,PD34,PR175,PC136,PR178 2.add PR306:0, PQ76:SI4362, PL28:0.6U 3.Change PR200 from 2m(CYNTEC) to 1m (DALE) PC51 from 22nF to 33nF PR190 from 620K to 910K PR188 from 240k to 390k PC143,PC144,PC145 from 4.7U from 10U		DVT
2		For new version FAN5236 & ISL6225, modify enable function		40,41,42	1. delete PR287, PR234, PR288, PR254, PR289, PR274 2. add PR295: 0, PR296: 0, PR297 3. change PC143,PC144,PC 145 from 4.7U to 10u		DVT
3		modify for 3.3v to reduce power loss		37	Change PC34 from 470PF to 180PF		DVT
4		modify 5V reference		37	change PR63 from 10k to 10.2k		DVT
5		modify charging current		35	Change PR22 from 200 to 300 Add PR308 from 300		DVT
6		modify bridge battery charging current		38	1. Add PR300:22.1K, PR301: 22.1K, PR302:442, PR303:6.8K, PQ77:2SA1037K, PQ78: 2SC2412K, PH3:100K ,PD51:DAN217, PQ79: 2N7002,PR299:49.9K, PR304 :57.6K, PC246: 0.1U, PR297:10K 2. Delete PD46		DVT
7		modify and to reduce 5VALWPS,3VALWPS output recover edge voltage		37	1.Change PD12 from EP10QY03 to EC10QS04 PD11 from EP10QY03 to EC10QS04 PU13(ADP3415 driver) VCC from +5VALWP to +5VS PU12(ADP3205 controller) VCC from +3VALWP to +3VS 2.Delete PQ10,PQ11:SI4800DY, PQ12,PQ13:SI4810DY, PC46,PC56 Add PQ82,PQ83:SI4814DY		DVT
8		modify precharge circuit		35	1.Change PR17 from 150k to 412k PR19 from 2.4M to 634K PR20 from 10K to 34K PR21 from 75K to 137K 2 Add PR309 :66.5K		DVT
		modify battery OVP:8 cell:2.2V cell 1.8V	6	36	1 change PR47 from 174k to 402k		
9		TP0610C will be phase out		35	change TP0610C to TP0610K		

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		change cpu core from two phase to one phase		39	1.ADD PC127,PU11,PD33,PR169,PR170, PC134,PR174,PQ51,PQ52,PQ53, PQ54,PC128,PC129,PC130,PC238, PC133,PD34,PR175,PC136,PR178 2.DELETE PR306:0, PQ76:SI4362, PL28:0.6U 3.Change PR175,PR200 from 1m (DALE) TO 2m(CYNTEC), PC151,PC136 from 33nF to 22nF, PR188 from 240k to 120k , ADD PC128,PC129,PC130 : 4.7U 4.Change PR186 from 56 TO 137(Frequency from 300k to 250KHZ), 5. ChangePR188 from 240k to 120k(Vcore from 1.46 to 1.466v,vid code=1.468v when Io=0A), PR187 change from 3.4k to 3.48k(Vboot=1.2v,and Vc4from0.741 to 0.752v)		PVT
2		Change new version FAN5236d & ISL6225b to ISL6225CA&FAN5236, modify enable function		40,41,42	1. ADD PR287, PR234, PR288, PR254, PR289, PR274 2. DELETE PR295: 0, PR296: 0, PR297 3.ADD PR287,PR288,PR289 4.Change PC174,PC198,PC222 FROM 0.01U TO 4.7U 16V		PVT
3		modify FAN5236 RC feed back compasation		40,41,42	PC183,PC184,PC207,PC208:FROM 0.01UF TO 1.2NF		PVT
4		change cpu core cap to 6*4.7uF 1210 not 3*10uF due to 10uF cap height >2mm		39	PC128,PC129,PC130,PC143,PC144,PC145FROM 10UF TO 4.7UNF		PVT
5		modify bridge battery charging current:		38	change PR302 be120 1206,PR303 be1.5k 1206		PVT
6		modify PU17,PU18 max current,OCP		40,41	change PR221,PR222,PR241,PR242 fom 1.27k(0603) to 1.05k(1206)		PVT
7		modify charger CP point :from from 61.5W to 54W		36	change PR332 fom 21K(0603) to 26.1K(0603)		PVT
8		modify and confirm PU12 Vref build time		39	INCREASE PR310 10KB between PU12Vref(PIN9) to PU12 VCC		
9		FOR bridge battery safety, add PTC as protection		38	add PFS1 0.75A/24V		

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