

LA-2251

Compal confidential

Schematics Document

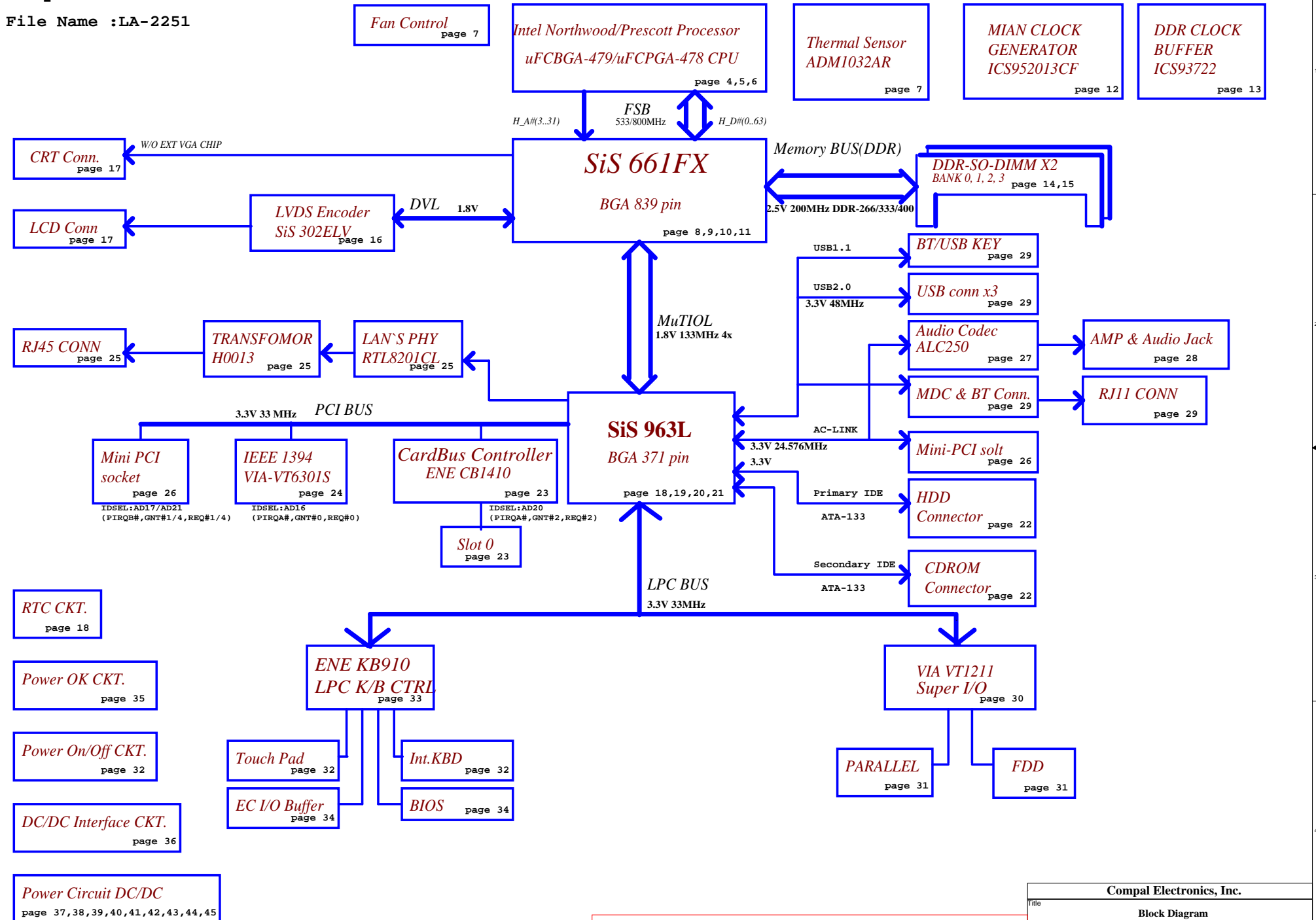
**DT TRANSPORT or Prescott uFCPGA
with Sis661FX+Sis963L core logic**

2004-05-17

REV:1.0

Compal Electronics, Inc.		
Title	Cover Sheet	
Document Number	LA-2251	Rev 1.0
Date	Monday, May 17, 2004	Sheet 1 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	The voltage(1.2V) for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON*	ON*
+1.8VS	1.8V switched power rail for SIS M661FX NB.	ON	OFF	OFF
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail for DDR Clock Buffer	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

FIR@ : means just build when FIR Module build in .

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD13 (INT.)	N/A	N/A
USB	AD14 (INT.)	N/A	E/F/H
AC97	AD13 (INT.)	N/A	C
ATA 100	AD13 (INT.)	N/A	A
ETHERNET	AD15 (INT.)	N/A	D
1394	AD16	0	A
LAN	AD19	3	D
CARD BUS	AD20	2	A
Wireless LAN(MINI PCI)	AD17/AD21	1/4	B

 Note: PLACE CLOSE TO M661FX, USE 10/10 WIDTH/SPACE

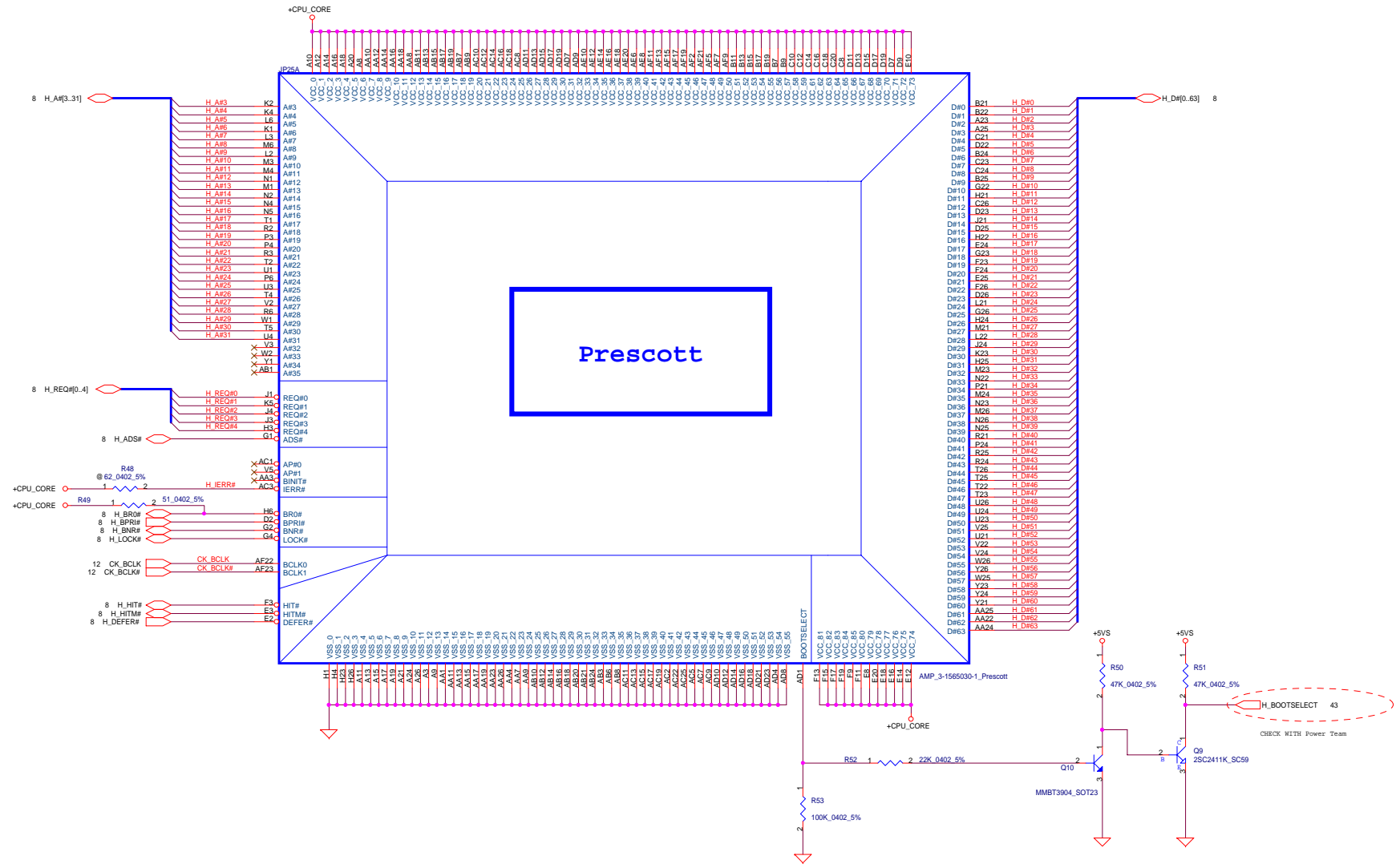
Board ID Table for AD channel

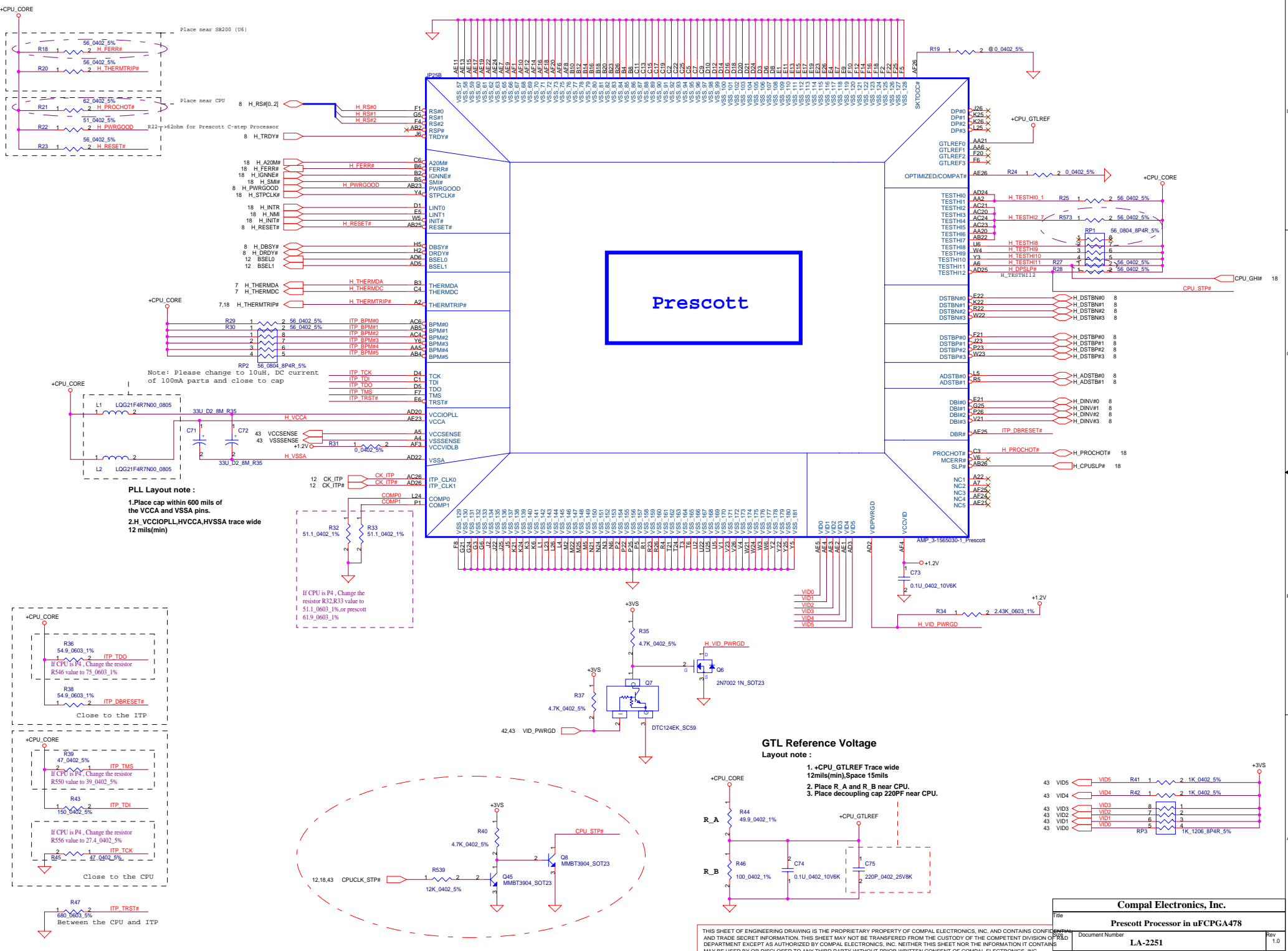
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

Compal Electronics, Inc.

Notes List





Prescott

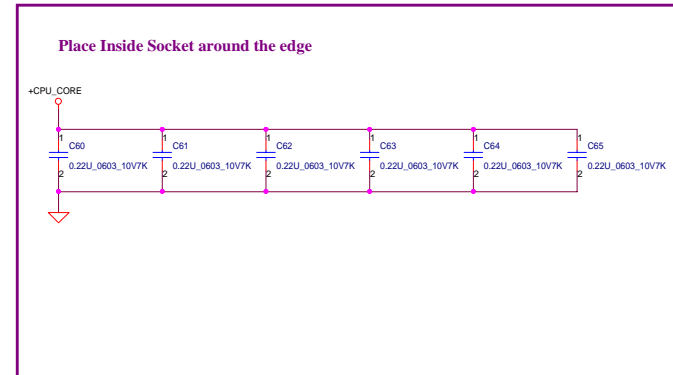
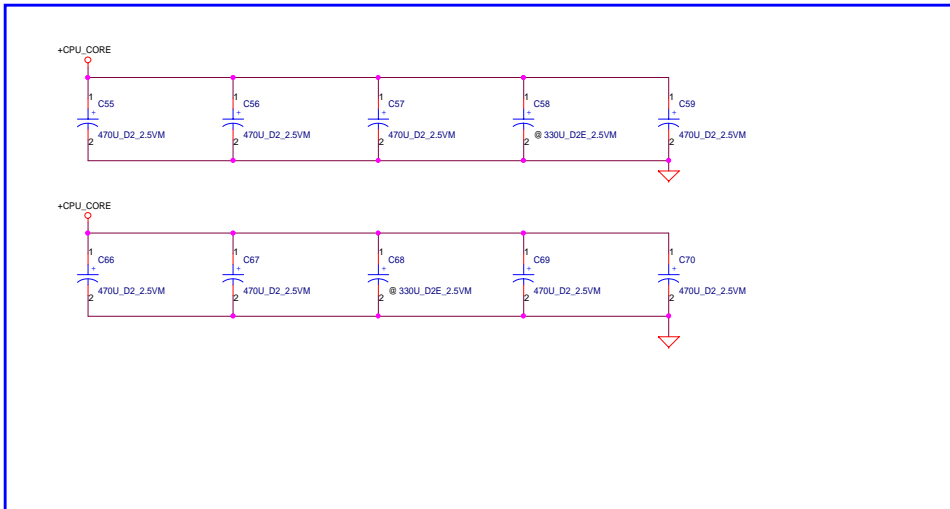
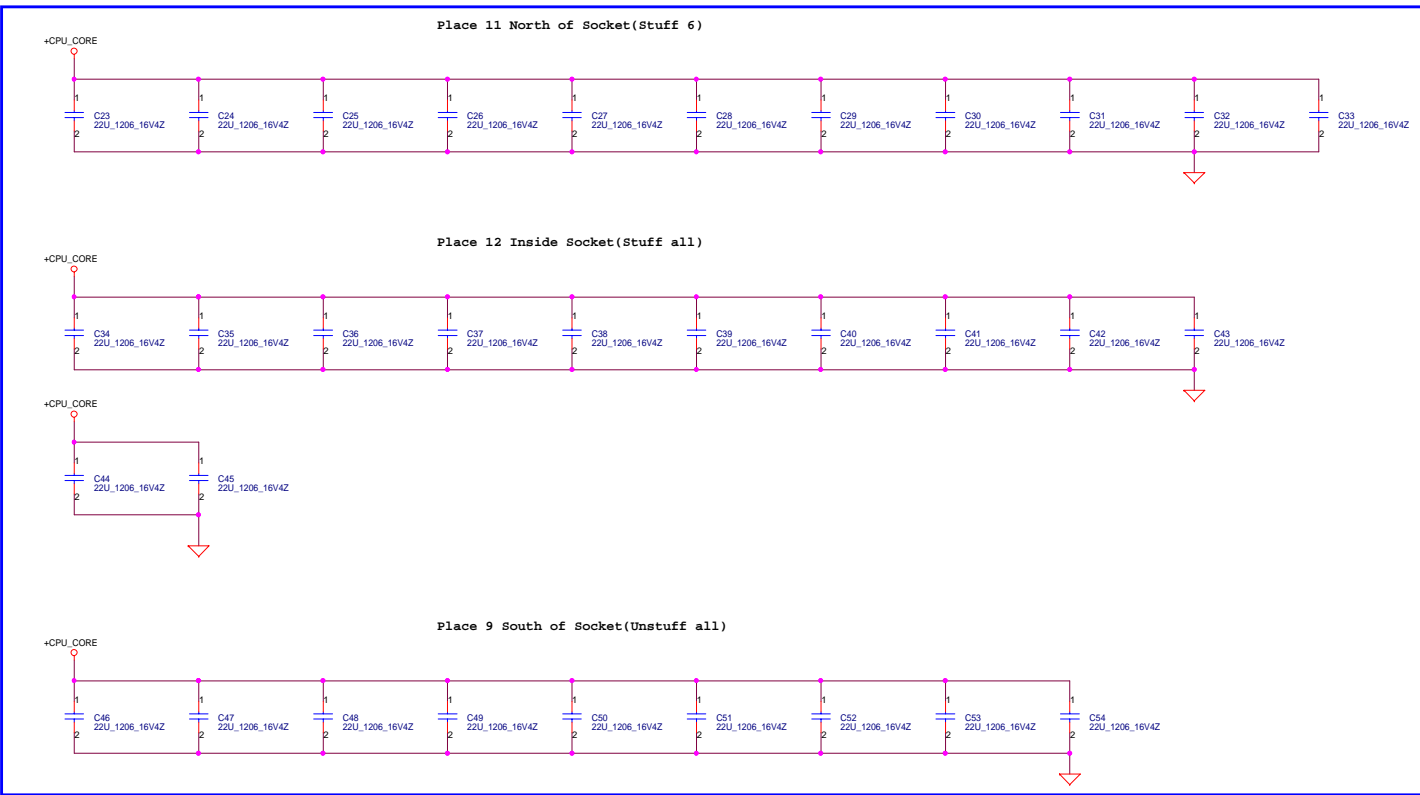
Note: Please change to 10uH, DC current of 100mA parts and close to cap

PLL Layout note :
 1. Place cap within 600 mils of the VCCA and VSSA pins.
 2. H_VCCIOPLL, HVCCA, HVSSA trace wide 12 mils(min)

GTL Reference Voltage Layout note :
 1. +CPU_GTLREF Trace wide 12mils(min), Space 15mils
 2. Place R_A and R_B near CPU.
 3. Place decoupling cap 220PF near CPU.

Compal Electronics, Inc.	
Prescott Processor in uPCPGA478	
Title	Rev 1.0
Document Number	LA-2251
Date	Monday, May 17, 2004
Sheet	5 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

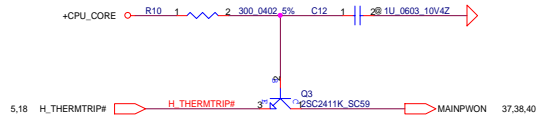
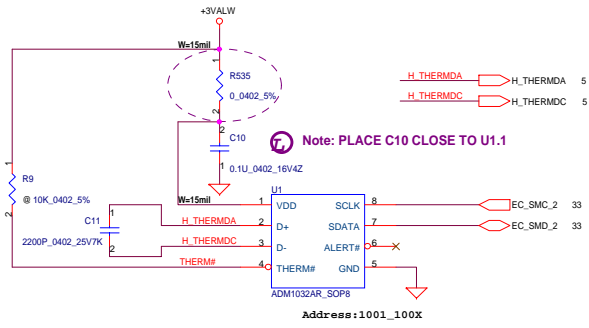


Compal Electronics, Inc.	
File	CPU Decoupling
Part No.	Document Number
Rev	LA-2251
Date	Monday, May 17, 2004
Sheet	6 of 47

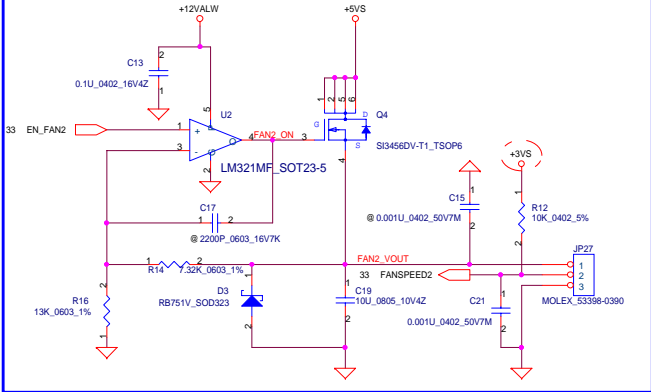
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Rev 1.0

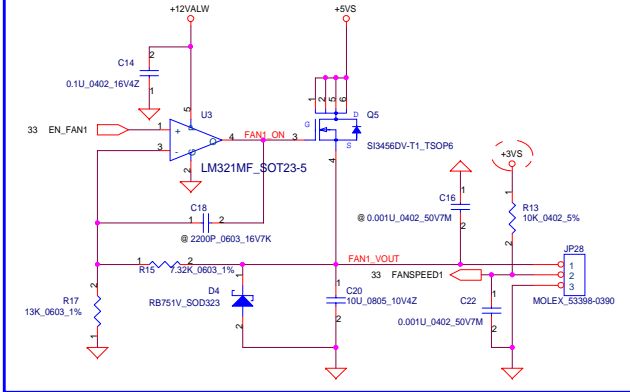
Thermal Sensor ADM1032AR



FAN CONN. 2 Fan Control circuit

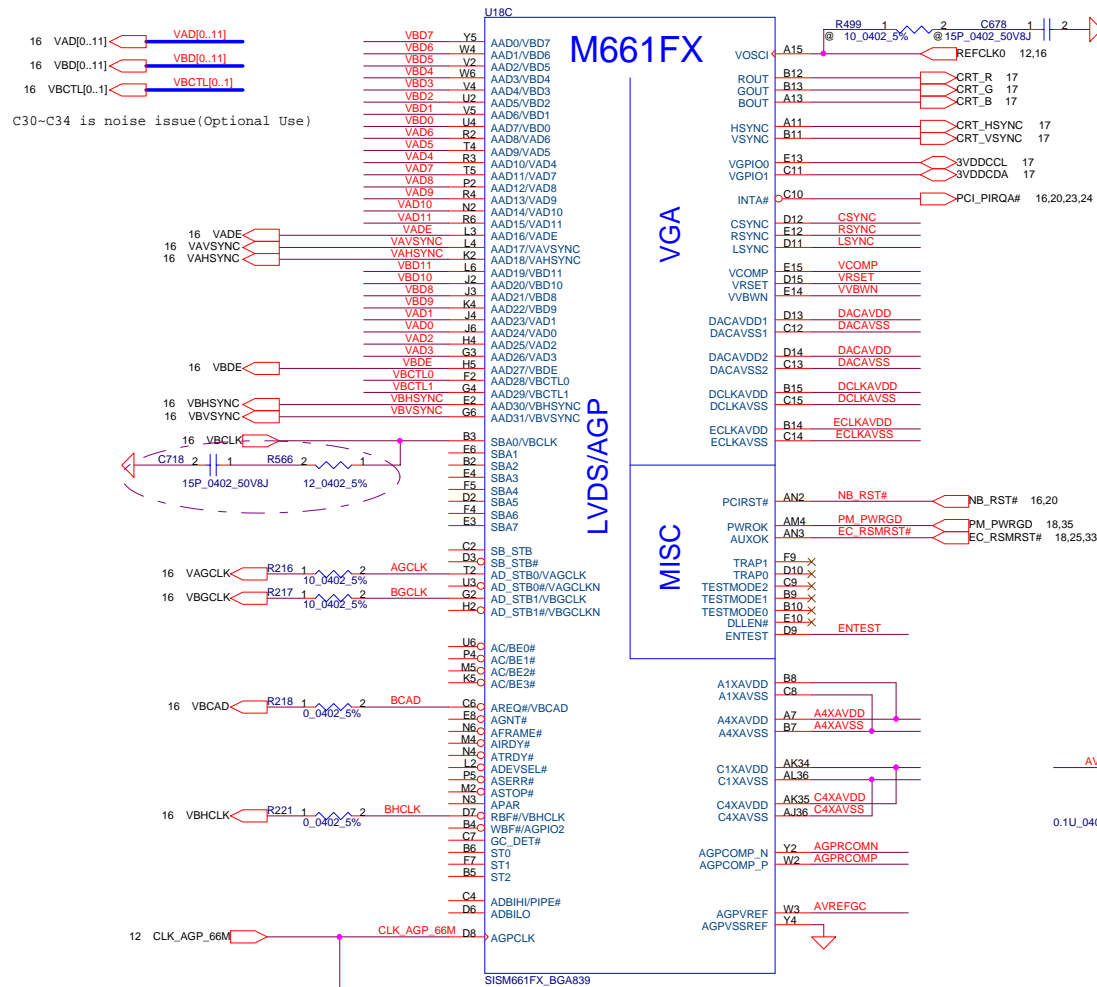


FAN CONN.1 Fan Control circuit



Compal Electronics, Inc.	
CPU Thermal Sensor&FAN CTRL	
Document Number	Rev 1.0
LA-2251	
Date: Monday, May 17, 2004	Sheet 7 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



C30-C34 is noise issue(Optional Use)

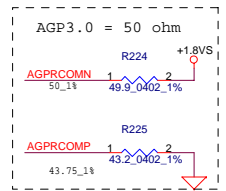
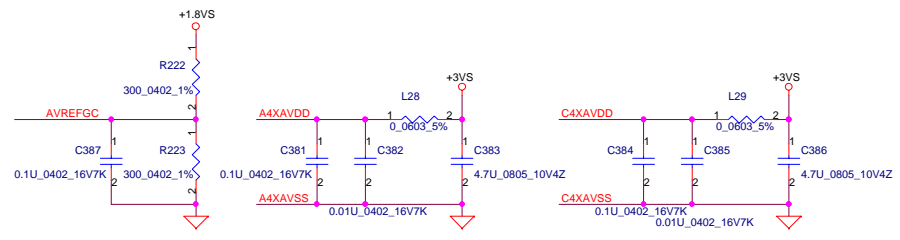
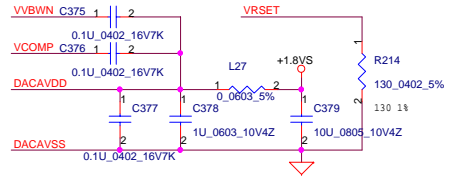
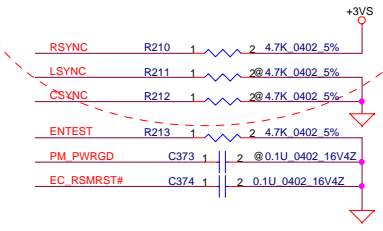
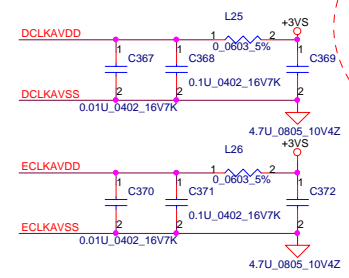
M661FX

VGA

LVDS/AGP

MISC

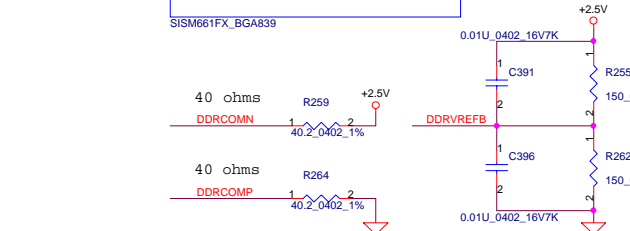
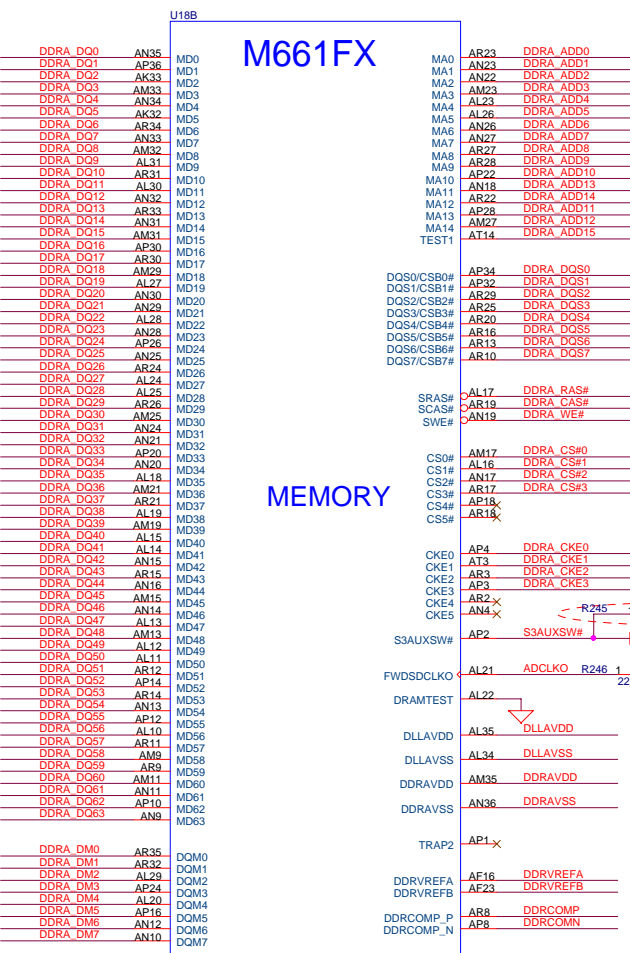
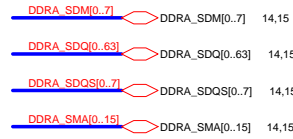
	VGA	Enable	Disable
RSYNC		1	0
LSYNC	panel link	1	0
CSYNC	VB	1	0



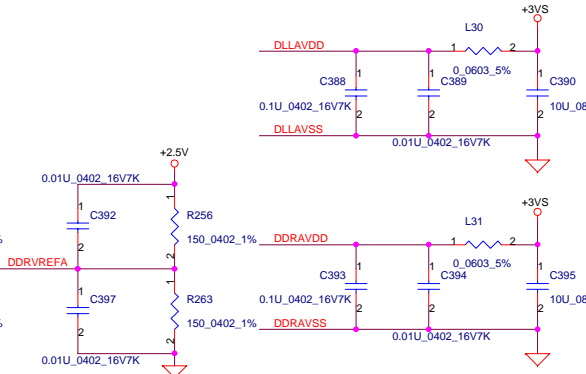
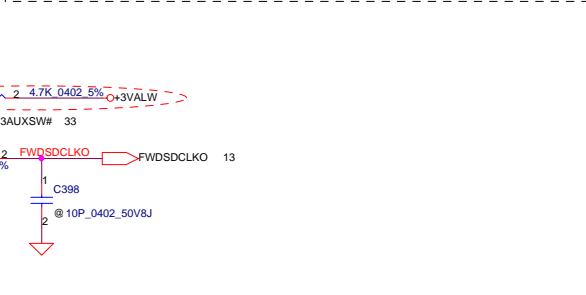
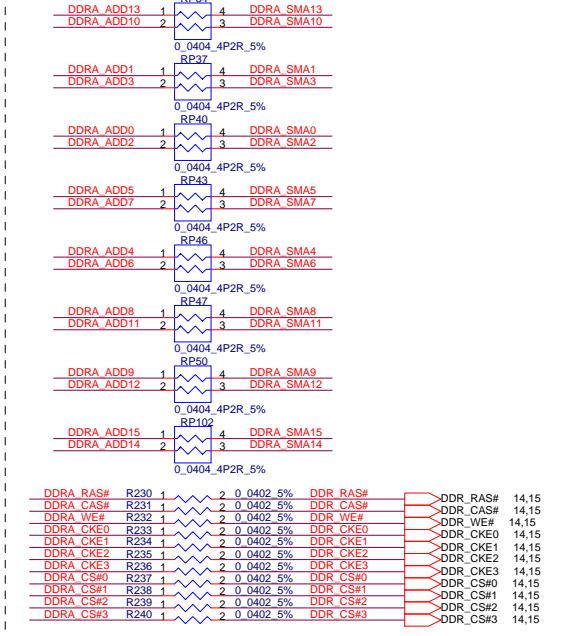
Compal Electronics, Inc.			
Title: M661FX-1 (LVDS/AGP/VGA/MISC)			
Size	Document Number	Rev	
	LA-2251	1.0	
Date:	Monday, May 17, 2004	Sheet	9 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Note: PLACE CLOSE TO DIMM0, and between NB chip and DIMM0

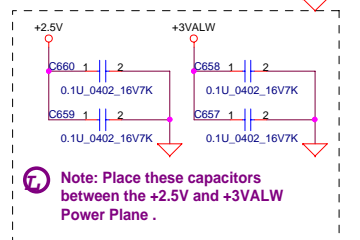
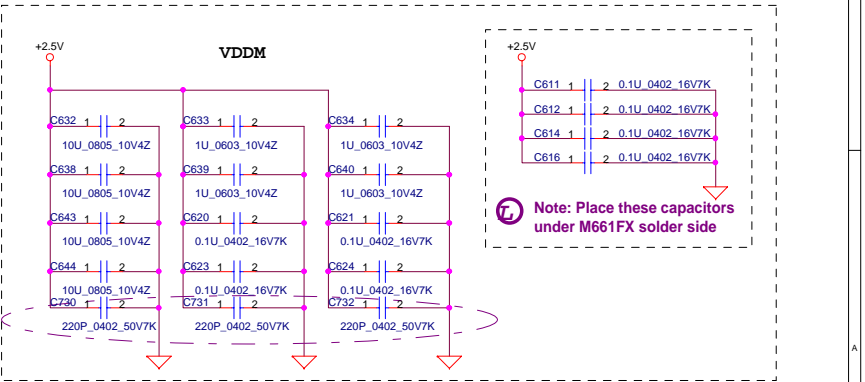
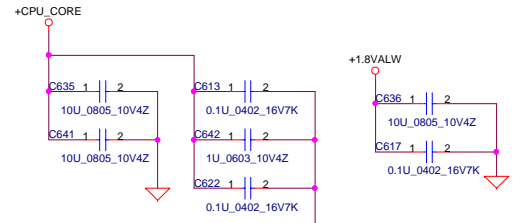
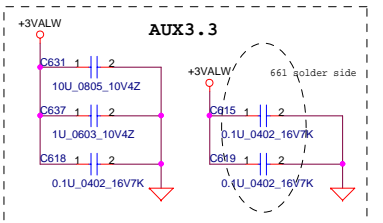
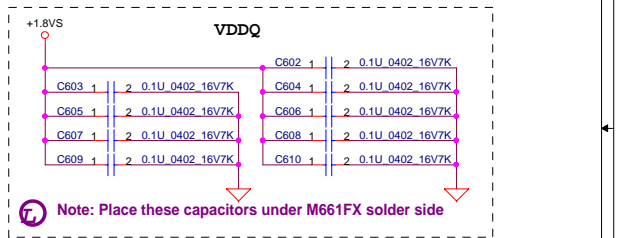
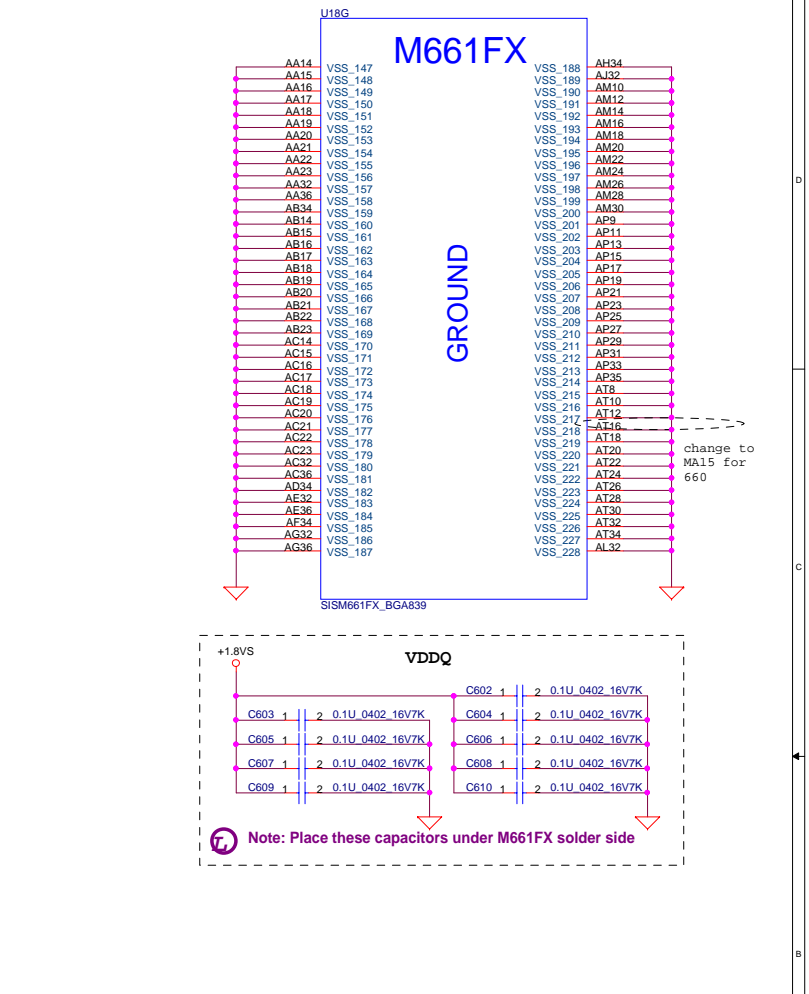
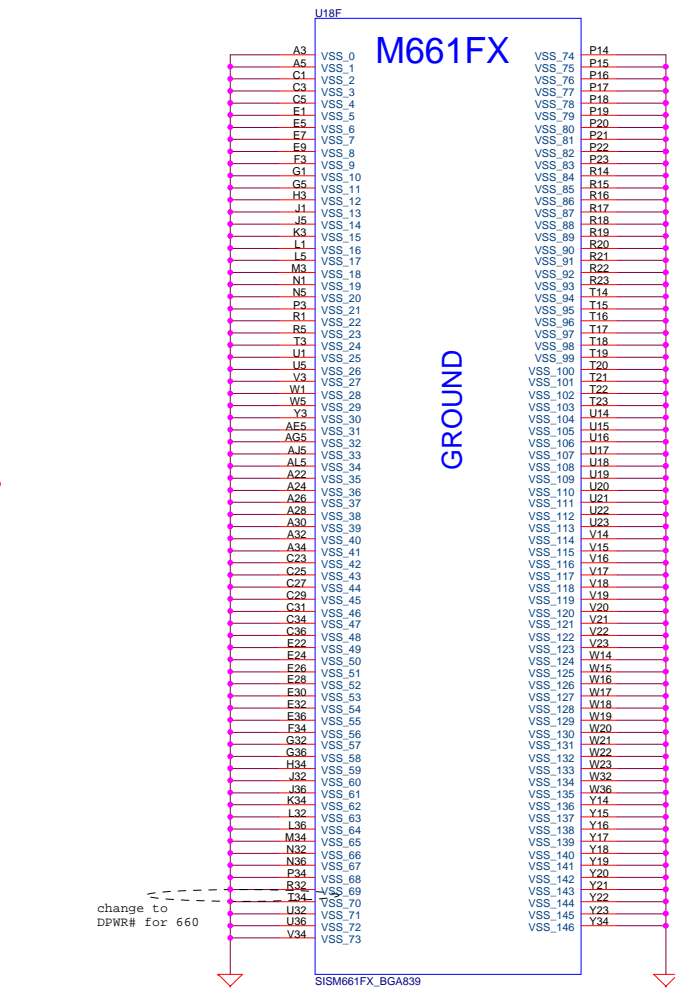
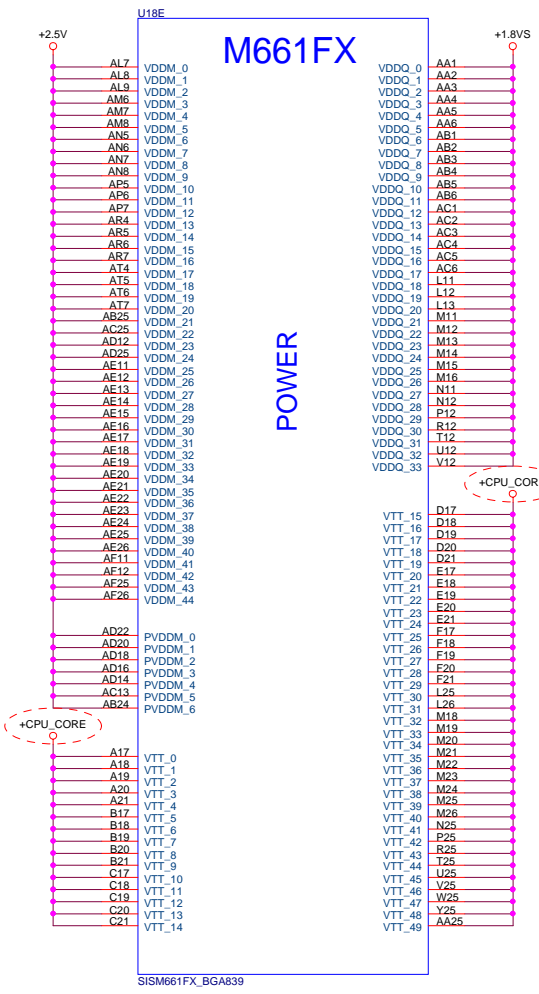


Note: PLACE CLOSE TO DIMM0, and between NB chip and DIMM0



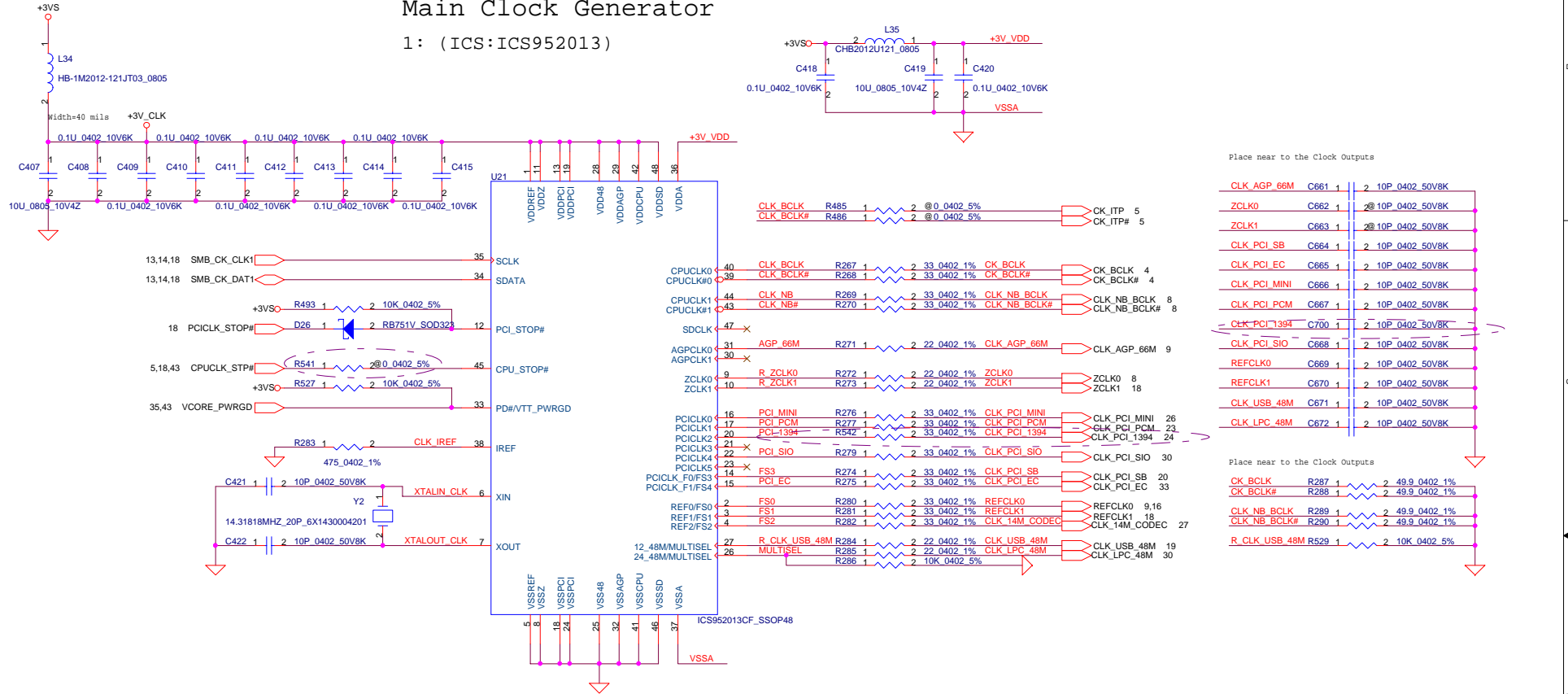
Compal Electronics, Inc.
M661FX-2 (MEMORY for DDR)
 Title: _____
 Part Number: _____
 Revision: _____
 Date: Monday, May 17, 2004
 Sheet 10 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

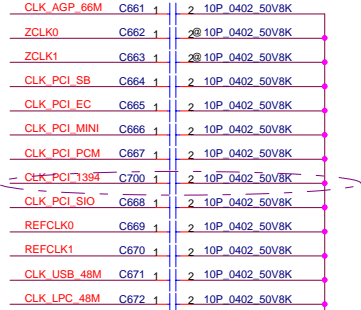


Main Clock Generator

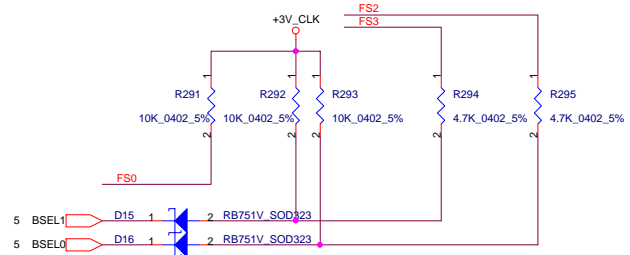
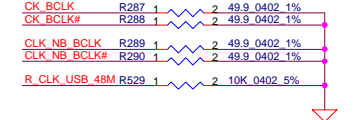
1: (ICS:ICS952013)



Place near to the Clock Outputs



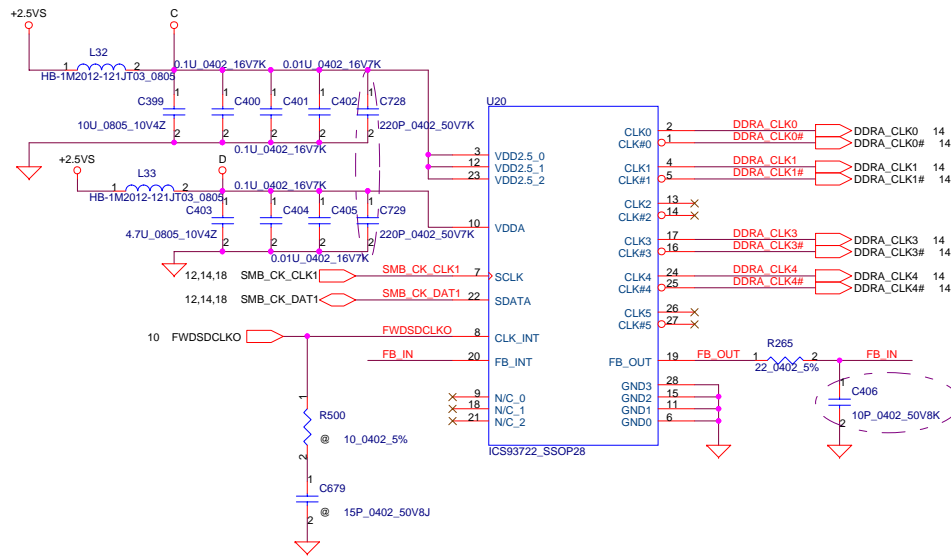
Place near to the Clock Outputs



FS3	FS2	CPU	ZCLK	AGP	PCI
0	0	100	133	66	33
0	1	133	133	66	33
1	0	200	133	66	33

Clock Buffer (DDR)

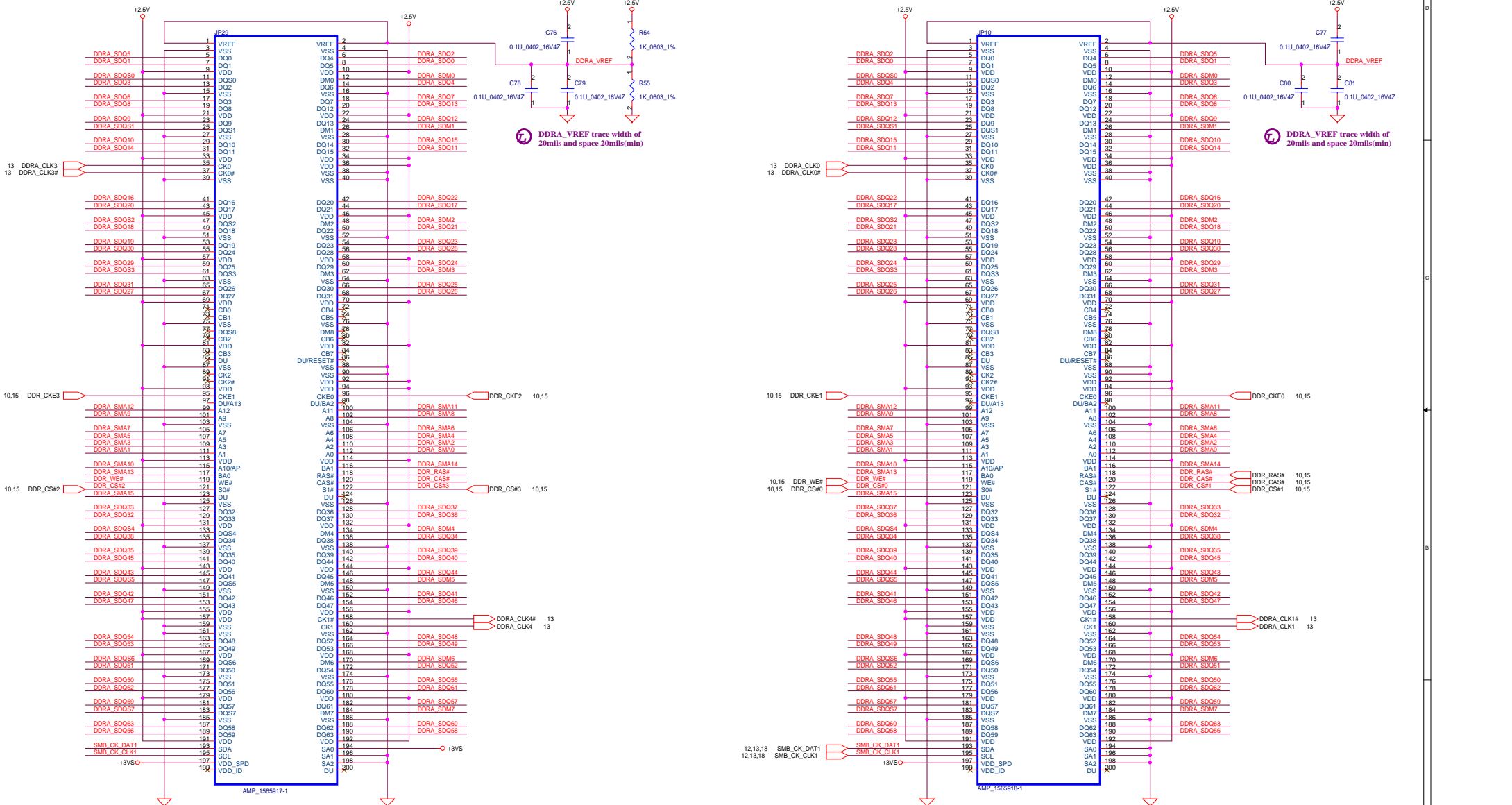
1:(ICS:ICS93722)



Compal Electronics, Inc.		
DDR Clock Buffer		
Title	Product Number	Rev
	LA-2251	1.0
Date	Monday, May 17, 2004	Sheet 13 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

- 10.15 DDRA_SDQ[0..63] DDR_A_SDQ0_63I
- 10.15 DDRA_SDQS[0..7] DDR_A_SDQS0_7I
- 10.15 DDRA_SMA[0..15] DDR_A_SMA0_15I
- 10.15 DDRA_SDM[0..7] DDR_A_SDM0_7I



**DIMM1
STANDARD**

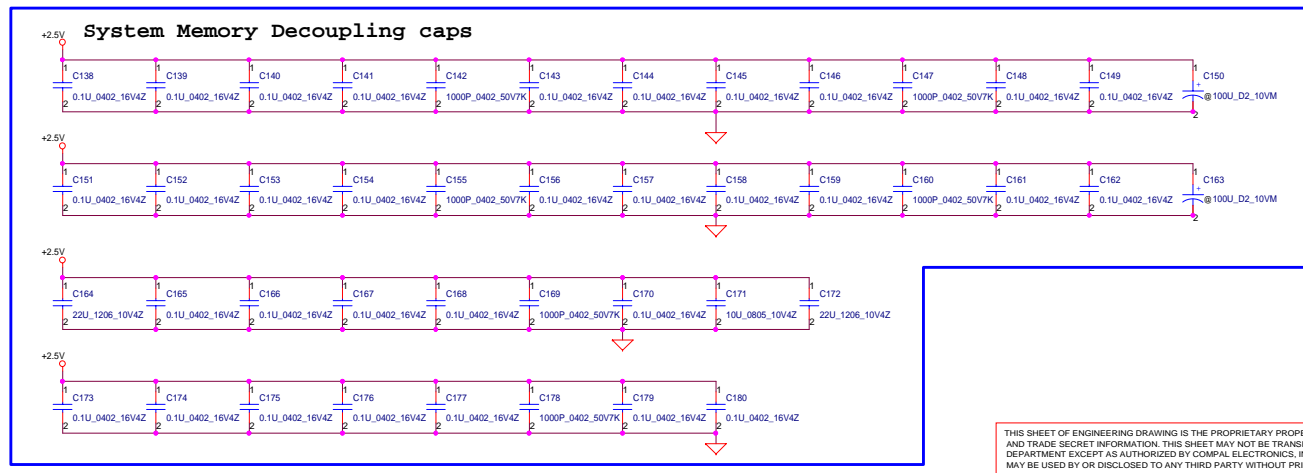
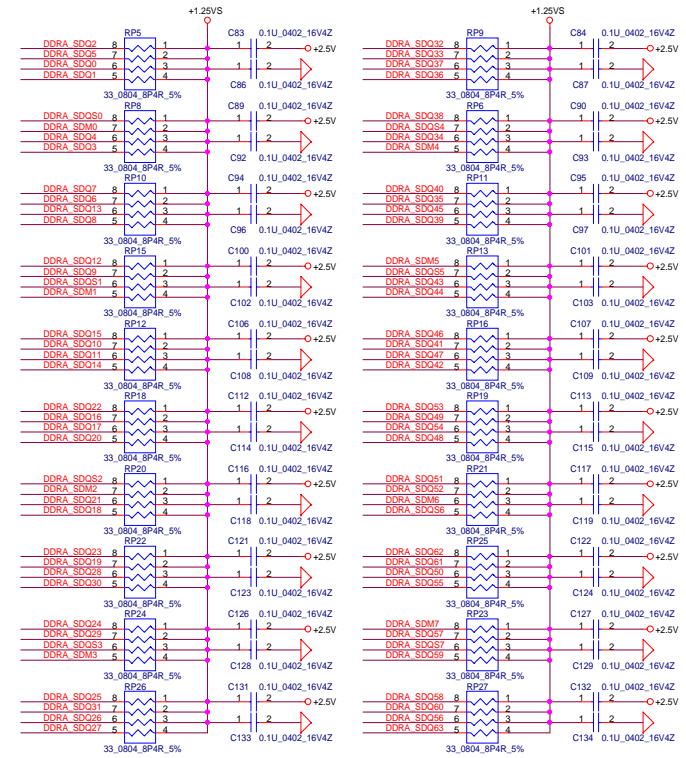
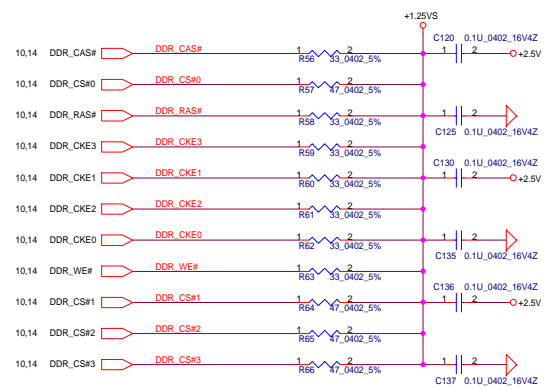
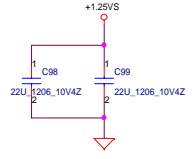
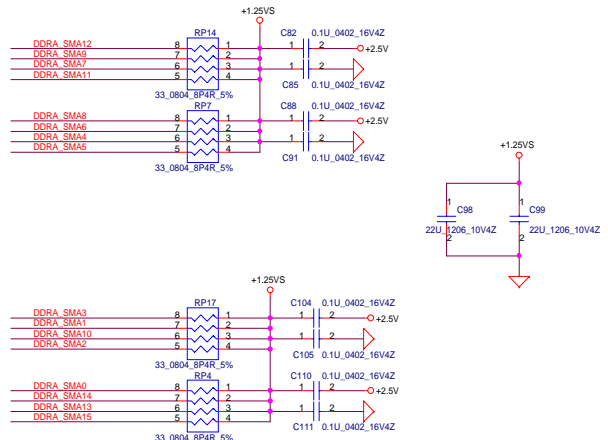
**DIMM0
REVERSE**

Compal Electronics, Inc.			
File	DDR-SODIMM SLOT1		
Document Number	LA-2251		
Date	Monday, May 17, 2004	Sheet	14 of 47
Rev	1.0		

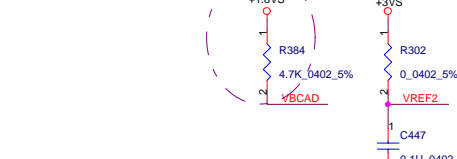
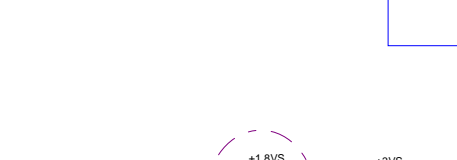
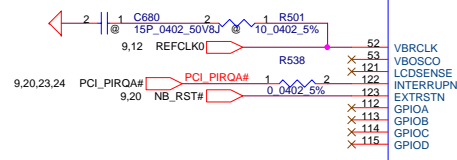
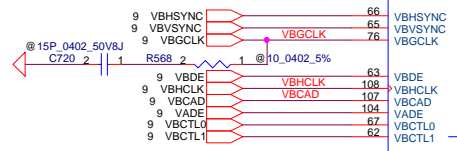
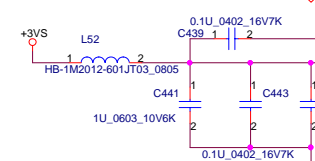
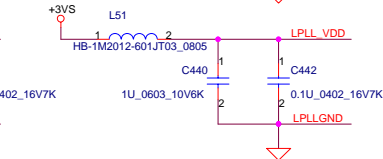
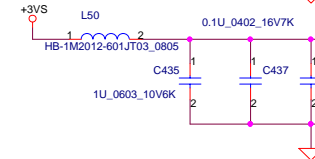
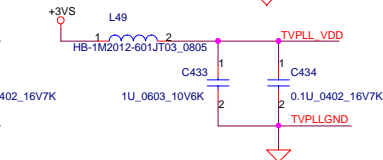
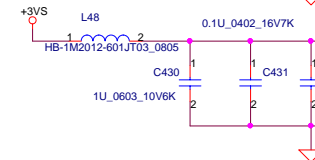
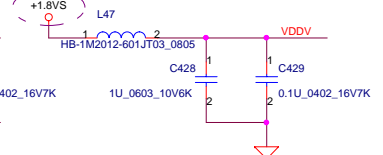
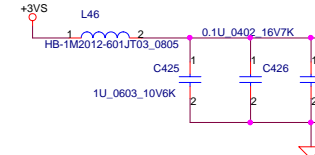
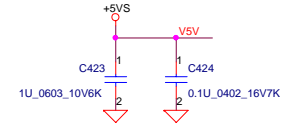
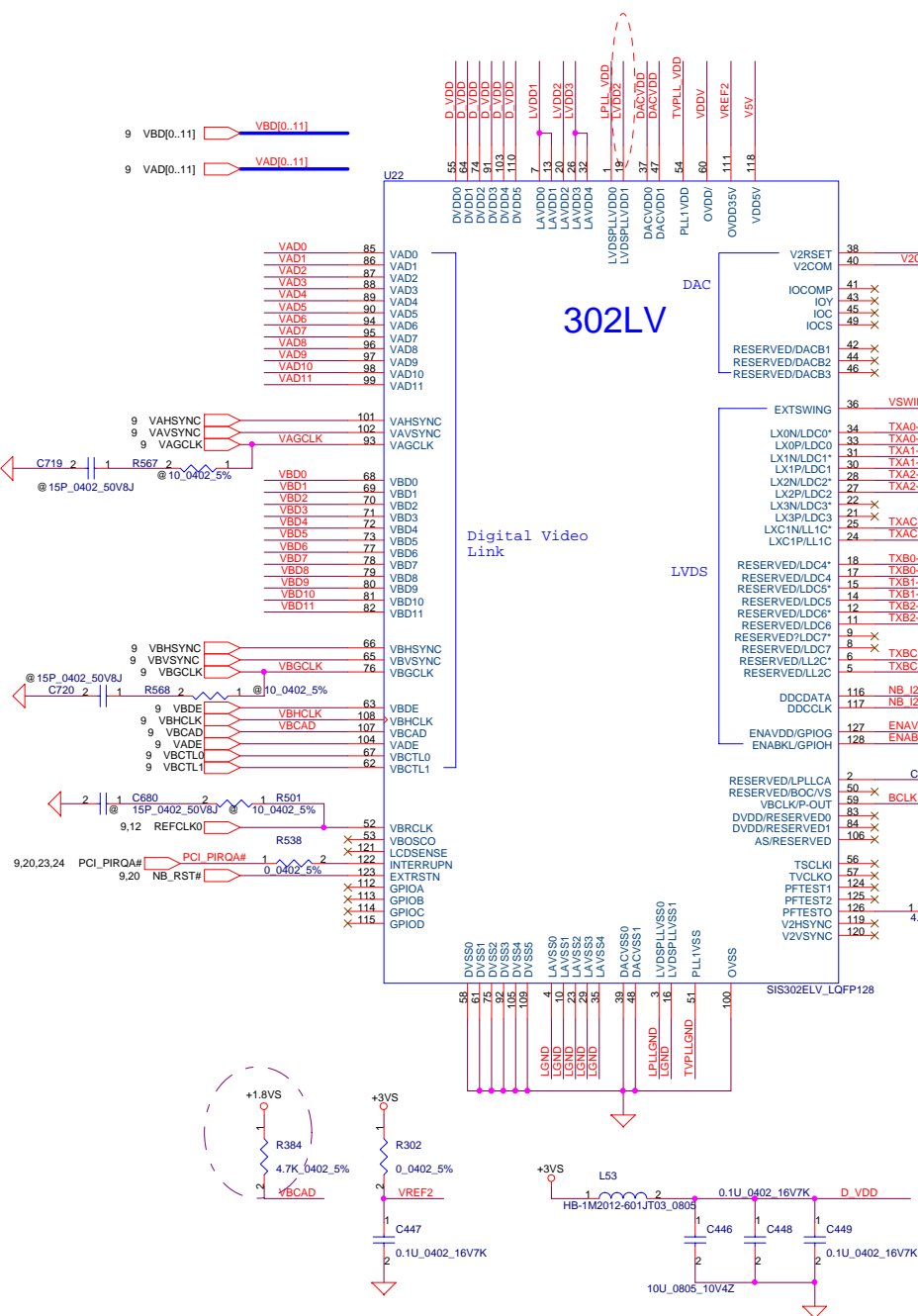
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

DDR Termination resistors & Decoupling caps

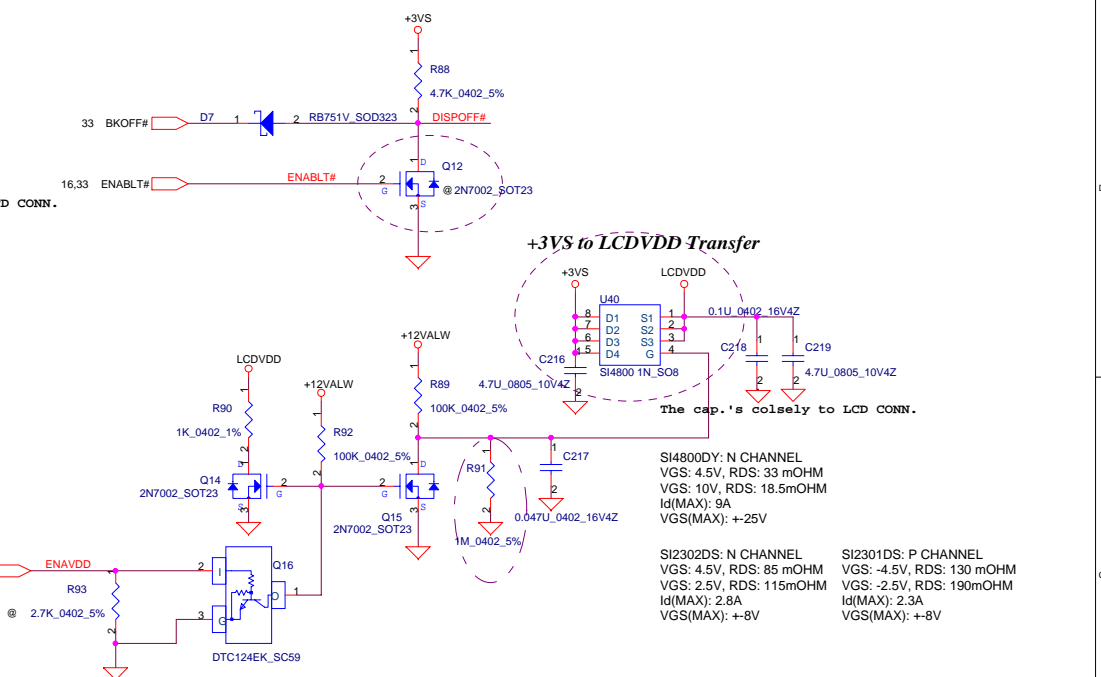
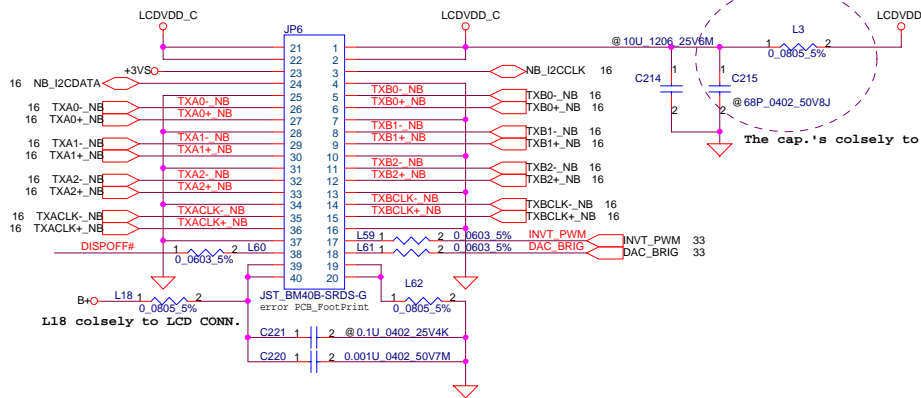
- 10.14 DDR_A_SDO[0..63] DDR_A_SDO[0..63]
- 10.14 DDR_A_SDS[0..7] DDR_A_SDS[0..7]
- 10.14 DDR_A_SMA[0..15] DDR_A_SMA[0..15]
- 10.14 DDR_A_SDM[0..7] DDR_A_SDM[0..7]



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

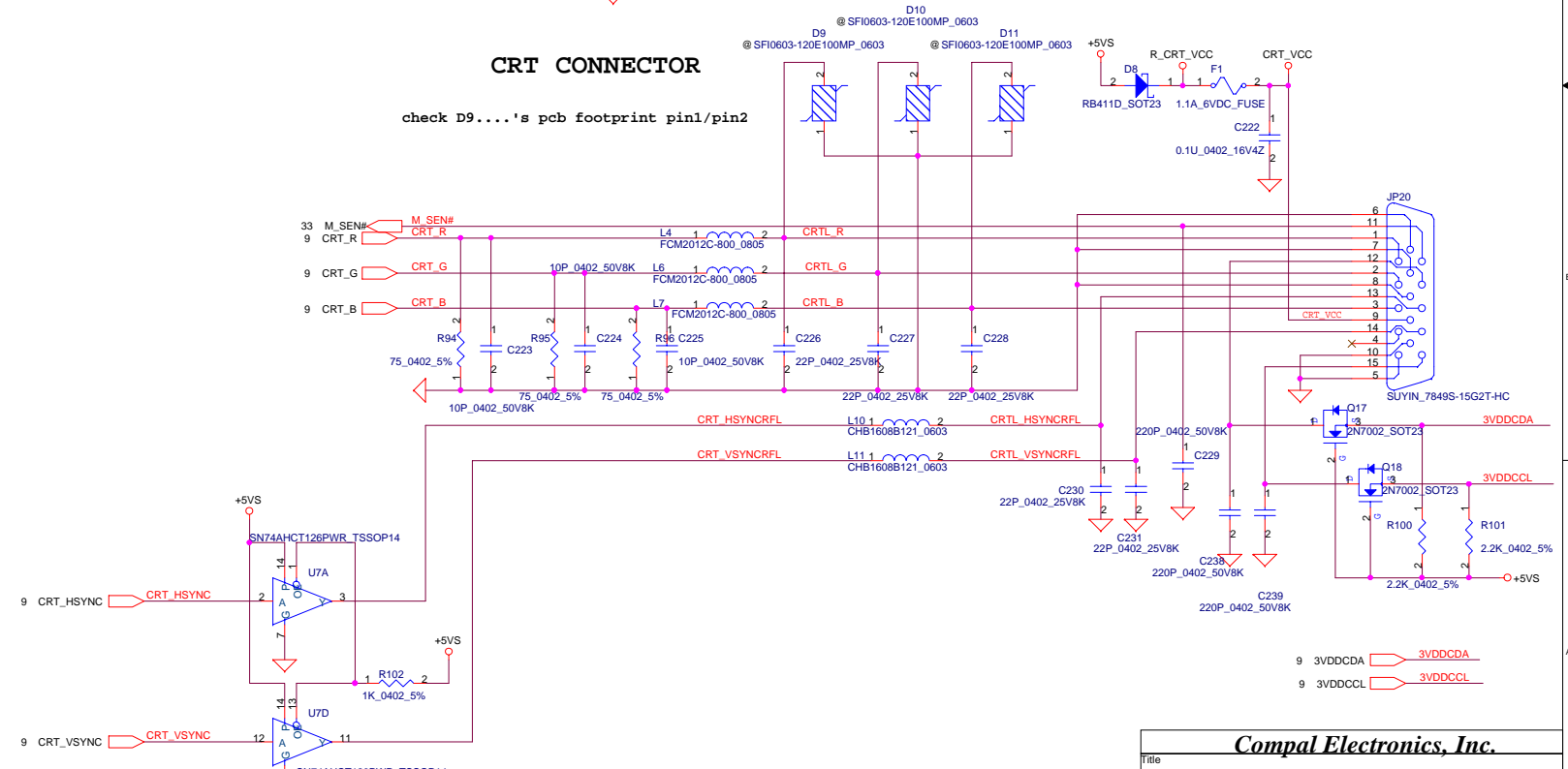


LCD CONN



CRT CONNECTOR

check D9....'s pcb footprint pin1/pin2

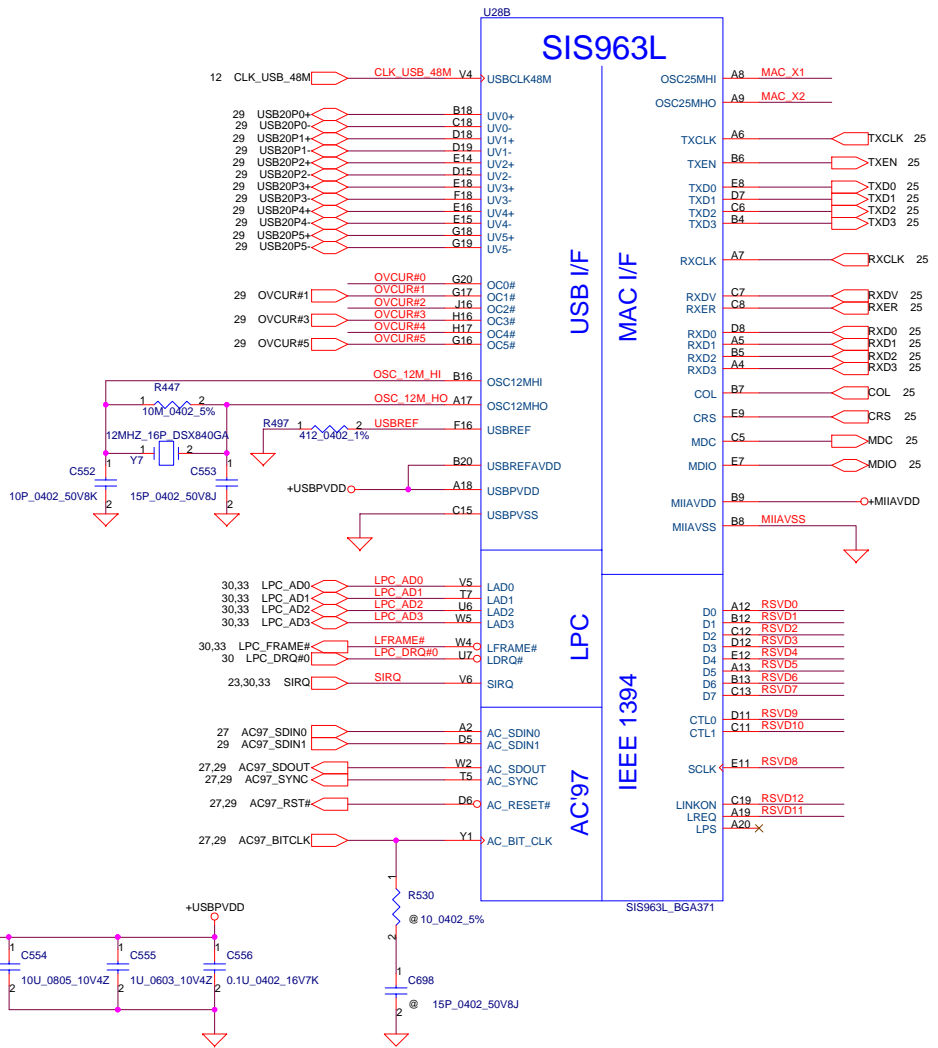
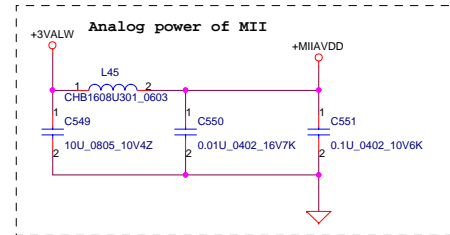
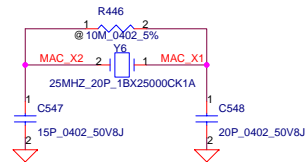
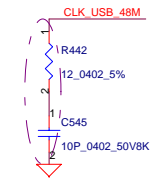
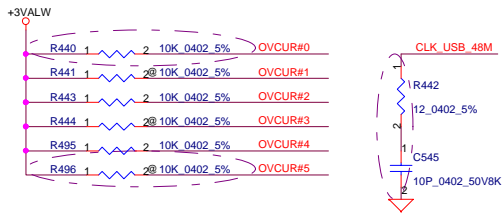


Compal Electronics, Inc.

LCD/Inverter BD & CRT CONN.

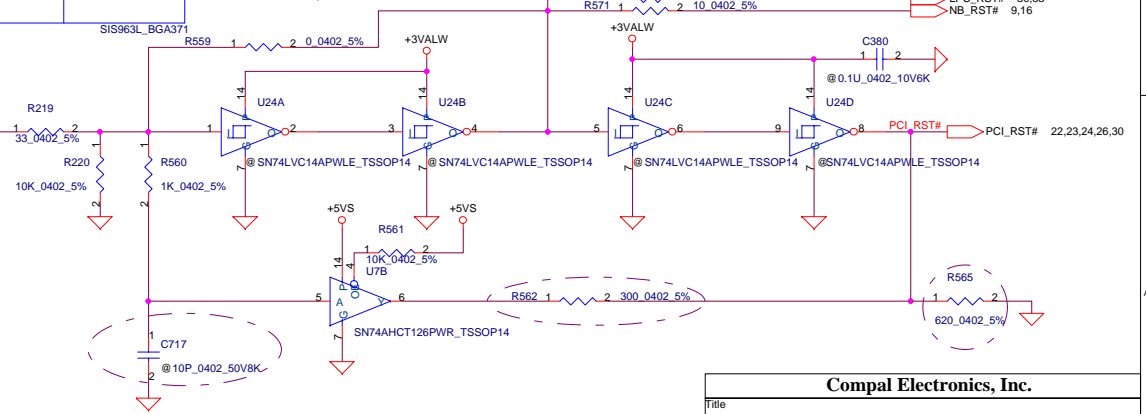
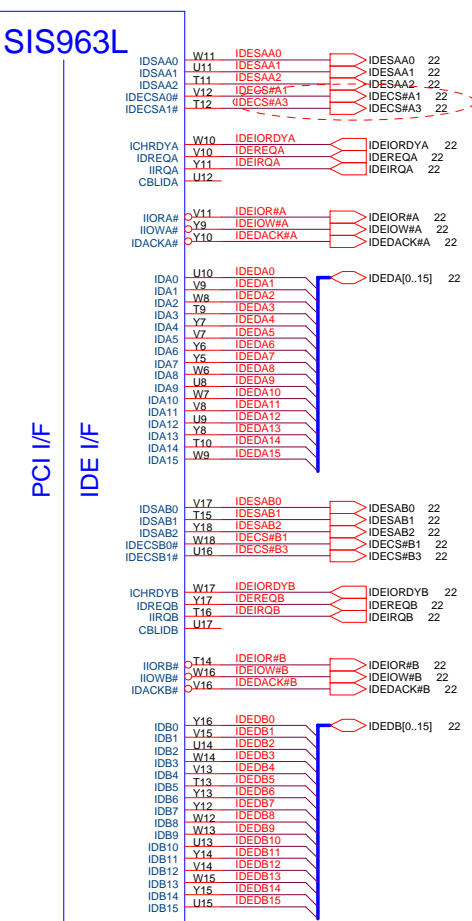
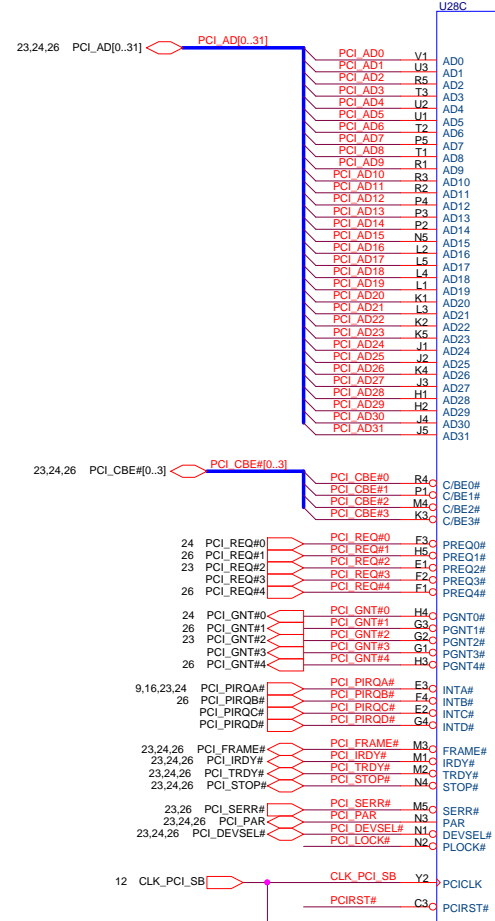
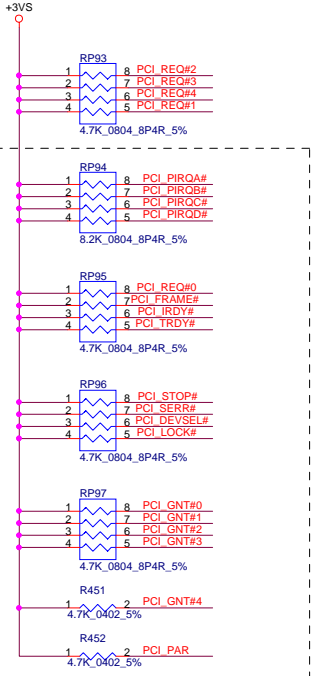
Title: _____
 Revision: _____
 Date: Monday, May 17, 2004
 Sheet 17 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Compal Electronics, Inc.	
Title	963L-2 (USB/LPC/AC97/1394/MAC)
Revision	1.0
Date	Monday, May 17, 2004
Sheet	19 of 47

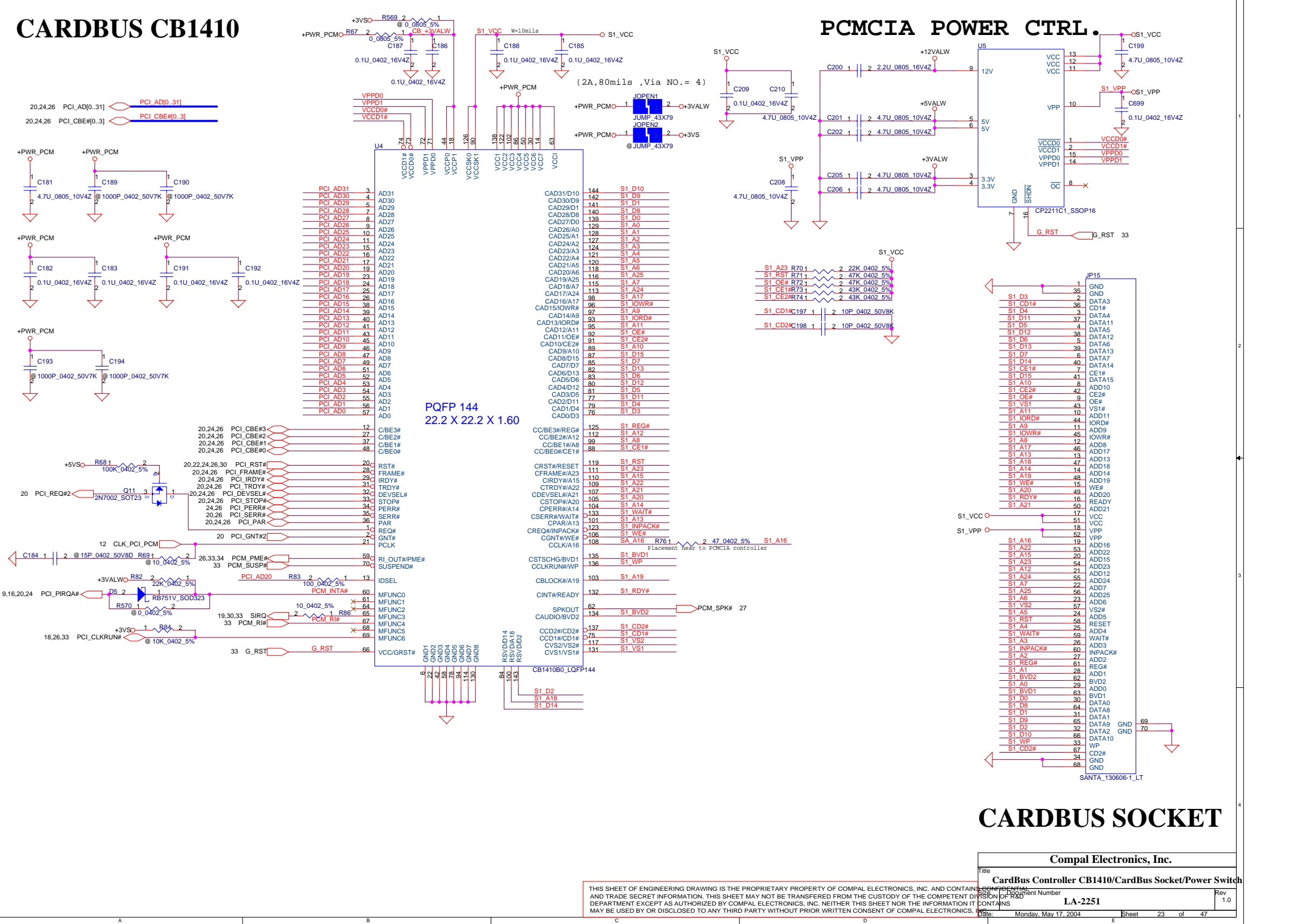
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

CARDBUS CB1410

PCMCIA POWER CTRL.



(2A, 80mils, Via NO. = 4)

PCI AD31	3	AD31	CAD31/D10	144	S1 D10
PCI AD30	4	AD30	CAD30/D9	142	S1 D9
PCI AD29	5	AD29	CAD29/D8	141	S1 D8
PCI AD28	7	AD28	CAD28/D8	140	S1 D8
PCI AD27	8	AD27	CAD27/D0	139	S1 D0
PCI AD26	8	AD26	CAD27/D0	129	S1 A0
PCI AD25	10	AD25	CAD26/A0	128	S1 A1
PCI AD24	11	AD24	CAD25/A1	127	S1 A2
PCI AD23	18	AD23	CAD24/A2	124	S1 A3
PCI AD22	16	AD23	CAD23/A3	121	S1 A4
PCI AD21	17	AD22	CAD22/A4	120	S1 A5
PCI AD20	19	AD20	CAD21/A5	118	S1 A6
PCI AD19	23	AD19	CAD20/A6	116	S1 A25
PCI AD18	24	AD18	CAD19/A25	115	S1 A7
PCI AD17	25	AD18	CAD18/A7	113	S1 A24
PCI AD16	26	AD17	CAD17/A24	98	S1 A17
PCI AD15	38	AD17	CAD16/A17	97	S1 IOWR#
PCI AD14	39	AD15	CAD15/IOWR#	96	S1 IOWR#
PCI AD13	40	AD14	CAD14/A9	93	S1 IORD#
PCI AD12	41	AD13	CAD13/IORD#	95	S1 A11
PCI AD11	43	AD12	CAD12/A11	91	S1 CE#
PCI AD10	46	AD11	CAD11/OE#	92	S1 OE#
PCI AD9	46	AD10	CAD10/CE2#	89	S1 CE2#
PCI AD8	47	AD9	CAD9/A10	88	S1 A10
PCI AD7	49	AD8	CAD8/A10	87	S1 D15
PCI AD6	51	AD7	CAD7/D7	85	S1 D7
PCI AD5	52	AD6	CAD6/D13	82	S1 D6
PCI AD4	53	AD5	CAD5/D6	80	S1 D12
PCI AD3	54	AD4	CAD4/D12	81	S1 D5
PCI AD2	58	AD3	CAD3/D5	77	S1 D11
PCI AD1	58	AD2	CAD2/D11	79	S1 D4
PCI AD0	57	AD1	CAD1/D4	76	S1 D3
		AD0	CAD0/D3		

PQFP 144
22.2 X 22.2 X 1.60

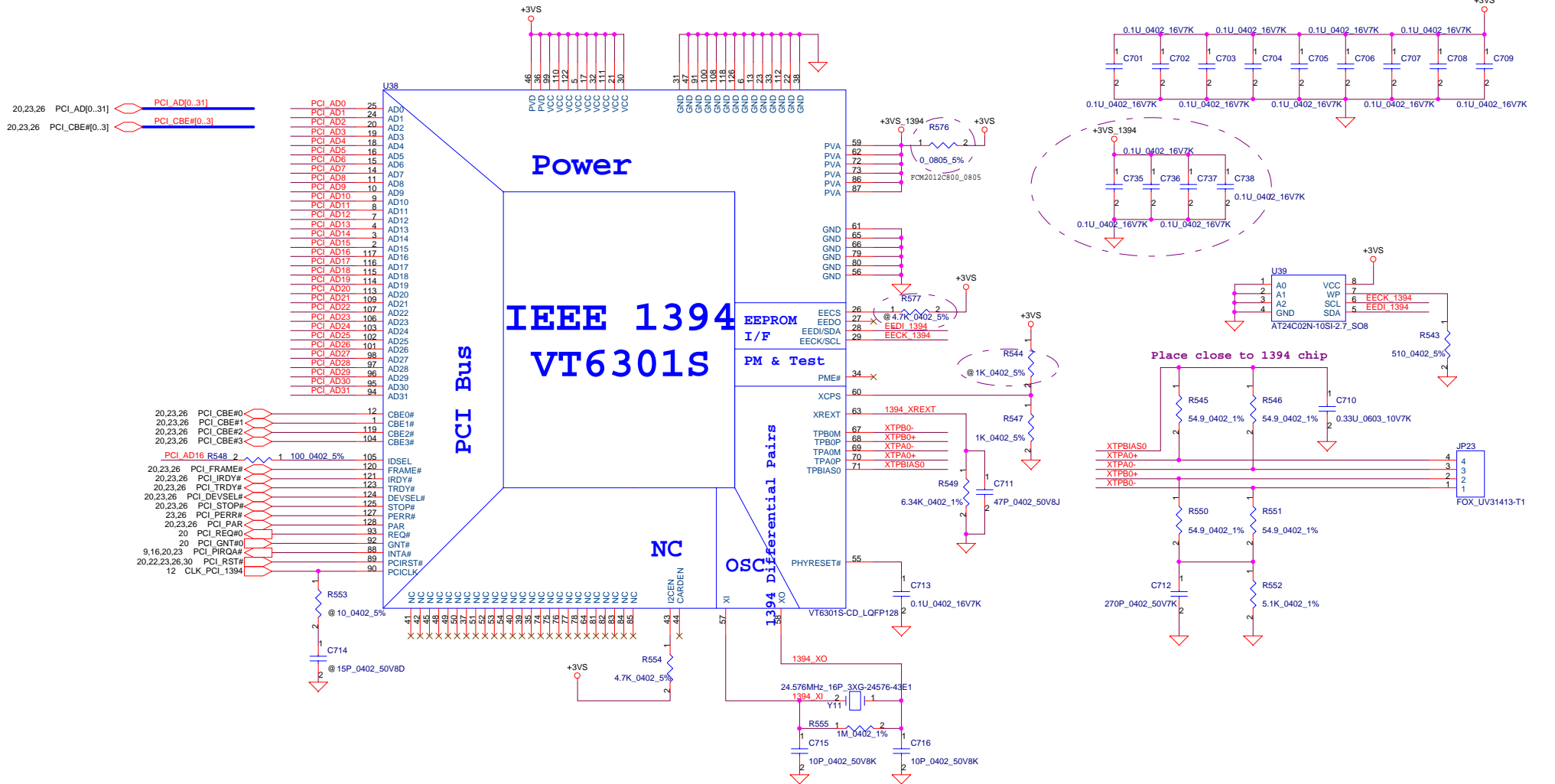
CARDBUS SOCKET

Compal Electronics, Inc.

CardBus Controller CB1410/CardBus Socket/Power Switch

Rev 1.0	Monday, May 17, 2004	Sheet 23 of 47
---------	----------------------	----------------

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



20,23,26 PCI_AD[0..31] \Rightarrow PCI_AD[0..31]
 20,23,26 PCI_CBE[0..3] \Rightarrow PCI_CBE[0..3]

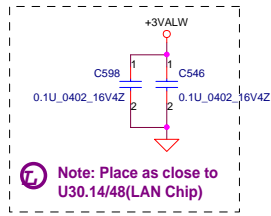
20,23,26 PCI_CBE#0 \Rightarrow CBE#0
 20,23,26 PCI_CBE#1 \Rightarrow CBE#1
 20,23,26 PCI_CBE#2 \Rightarrow CBE#2
 20,23,26 PCI_CBE#3 \Rightarrow CBE#3
 PCI_AD16 R548 2 \Rightarrow 1 100_0402_5%
 20,23,26 PCI_FRAME# \Rightarrow 120 IDSEL
 20,23,26 PCI_IRDY# \Rightarrow 121 FRAME#
 20,23,26 PCI_TRDY# \Rightarrow 123 TRDY#
 20,23,26 PCI_DEVSEL# \Rightarrow 124 DEVSEL#
 20,23,26 PCI_STOP# \Rightarrow 125 STOP#
 23,26 PCI_PERR# \Rightarrow 127 PERR#
 20,23,26 PCI_PAR \Rightarrow 128 PAR
 20 PCI_REQ# \Rightarrow 33 REQ#
 20 PCI_GNT#0 \Rightarrow 92 GNT#
 9,16,20,23 PCI_PIR0# \Rightarrow 88 INT#
 20,22,23,26,30 PCI_RST# \Rightarrow 89 PCIRST#
 12 CLK_PCI_1394 \Rightarrow 90 PCICLK

U38
 PCI_AD0 25 AD0
 PCI_AD1 24 AD1
 PCI_AD2 20 AD2
 PCI_AD3 19 AD3
 PCI_AD4 18 AD4
 PCI_AD5 15 AD5
 PCI_AD6 14 AD6
 PCI_AD7 11 AD7
 PCI_AD8 10 AD8
 PCI_AD9 9 AD9
 PCI_AD10 8 AD10
 PCI_AD11 7 AD11
 PCI_AD12 6 AD12
 PCI_AD13 4 AD13
 PCI_AD14 3 AD14
 PCI_AD15 2 AD15
 PCI_AD16 117 AD16
 PCI_AD17 116 AD17
 PCI_AD18 115 AD18
 PCI_AD19 114 AD19
 PCI_AD20 113 AD20
 PCI_AD21 109 AD21
 PCI_AD22 107 AD22
 PCI_AD23 106 AD23
 PCI_AD24 103 AD24
 PCI_AD25 102 AD25
 PCI_AD26 101 AD26
 PCI_AD27 98 AD27
 PCI_AD28 97 AD28
 PCI_AD29 96 AD29
 PCI_AD30 95 AD30
 PCI_AD31 94 AD31

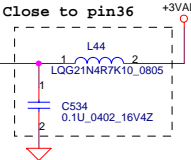
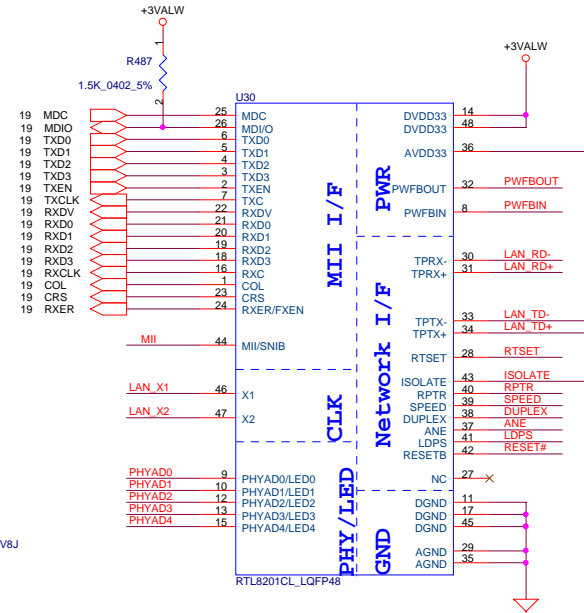
NC
 41 NC
 42 NC
 45 NC
 46 NC
 48 NC
 49 NC
 50 NC
 51 NC
 52 NC
 53 NC
 54 NC
 55 NC
 56 NC
 57 NC
 58 NC
 59 NC
 60 NC
 61 NC
 62 NC
 63 NC
 64 NC
 65 NC
 66 NC
 67 NC
 68 NC
 69 NC
 70 NC
 71 NC
 72 NC
 73 NC
 74 NC
 75 NC
 76 NC
 77 NC
 78 NC
 79 NC
 80 NC
 81 NC
 82 NC
 83 NC
 84 NC
 85 NC
 86 NC
 87 NC

Compal Electronics, Inc.	
IEEE1394 Controller & PHY-VIA VT6301S	
Revision 1.0	
Date: Monday, May 17, 2004	
Sheet	24 of 47

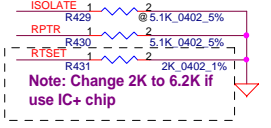
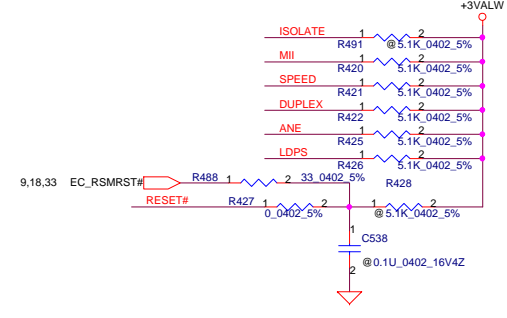
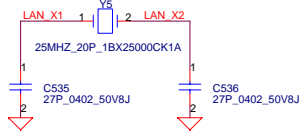
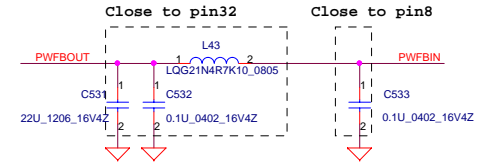
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



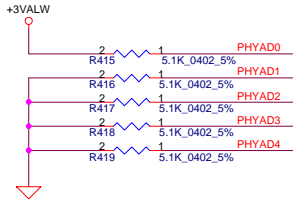
Note: Place as close to U30.14/48(LAN Chip)



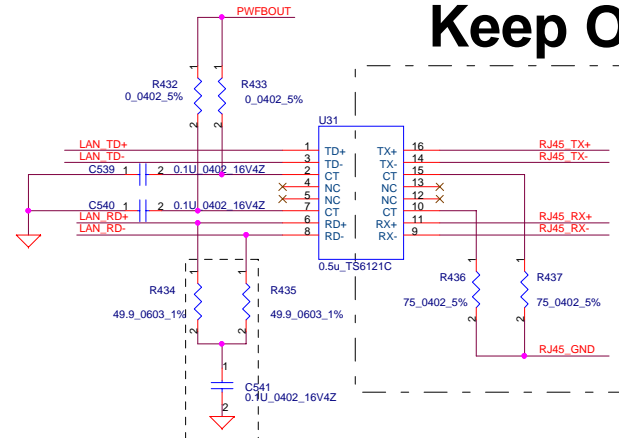
Note: Place as close to U30(LAN Chip)



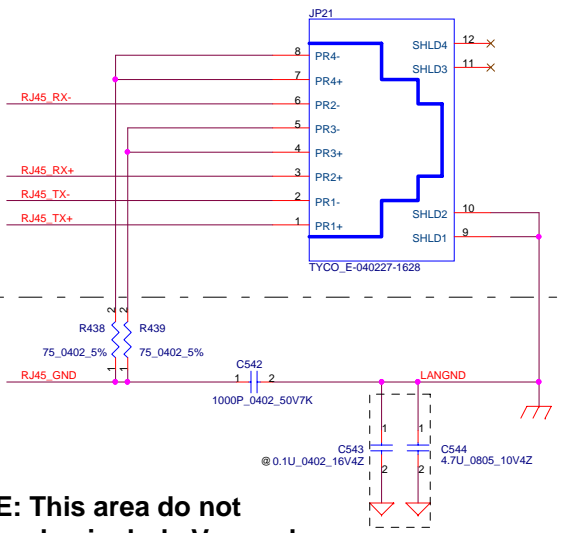
Note: Change 2K to 6.2K if use IC+ chip



Keep Out 40mil



Note: Place as close to U30(LAN Chip)

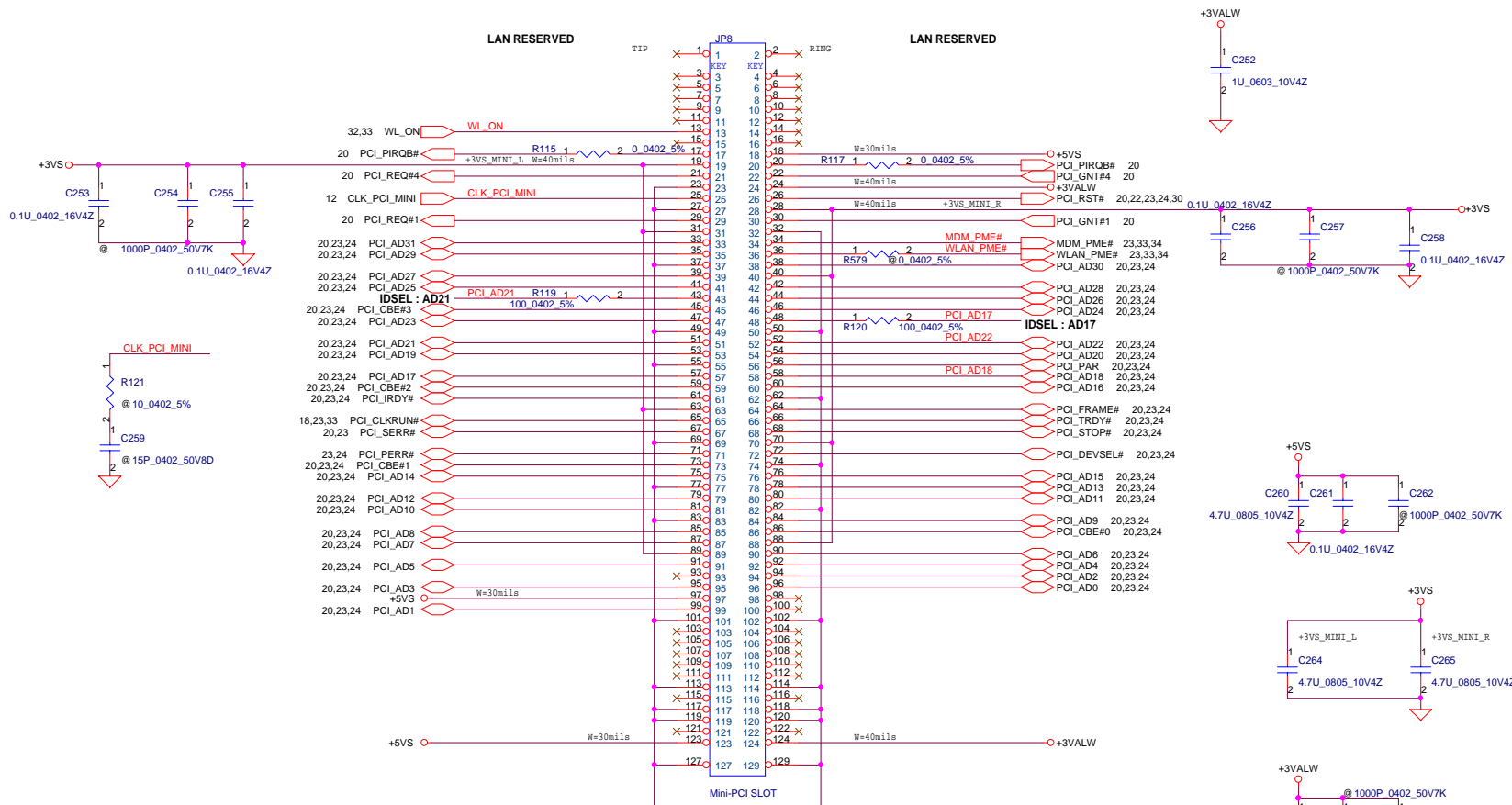


Termination plane should be copied to chassis ground and also depends on safety concern

LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer

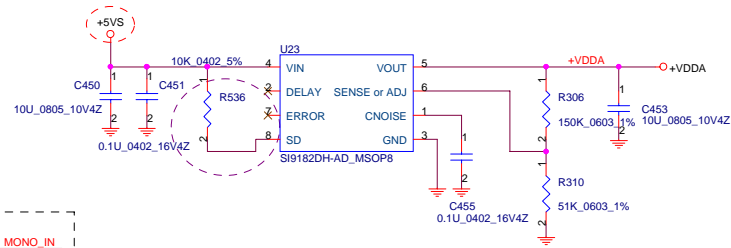
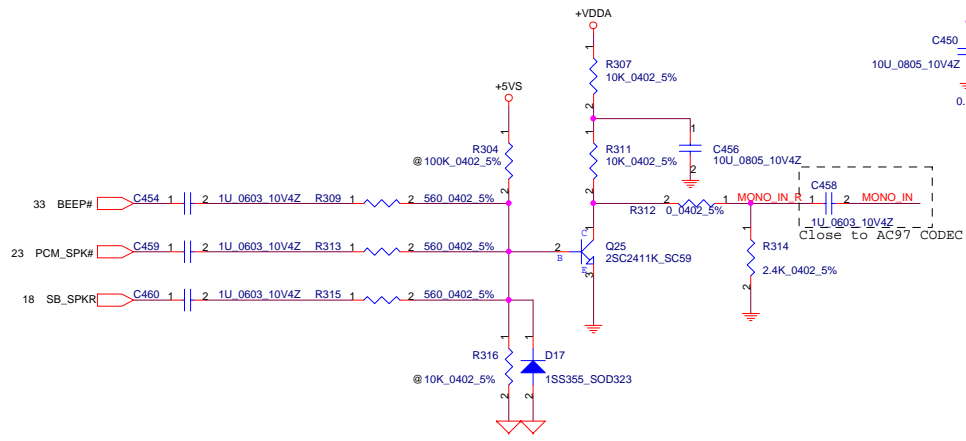
Compal Electronics, Inc.		
Title	LAN-PHY RTL8201CL	
Revision	Document Number	Rev
1.0	LA-2251	1.0
Date	Monday, May 17, 2004	Sheet 25 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

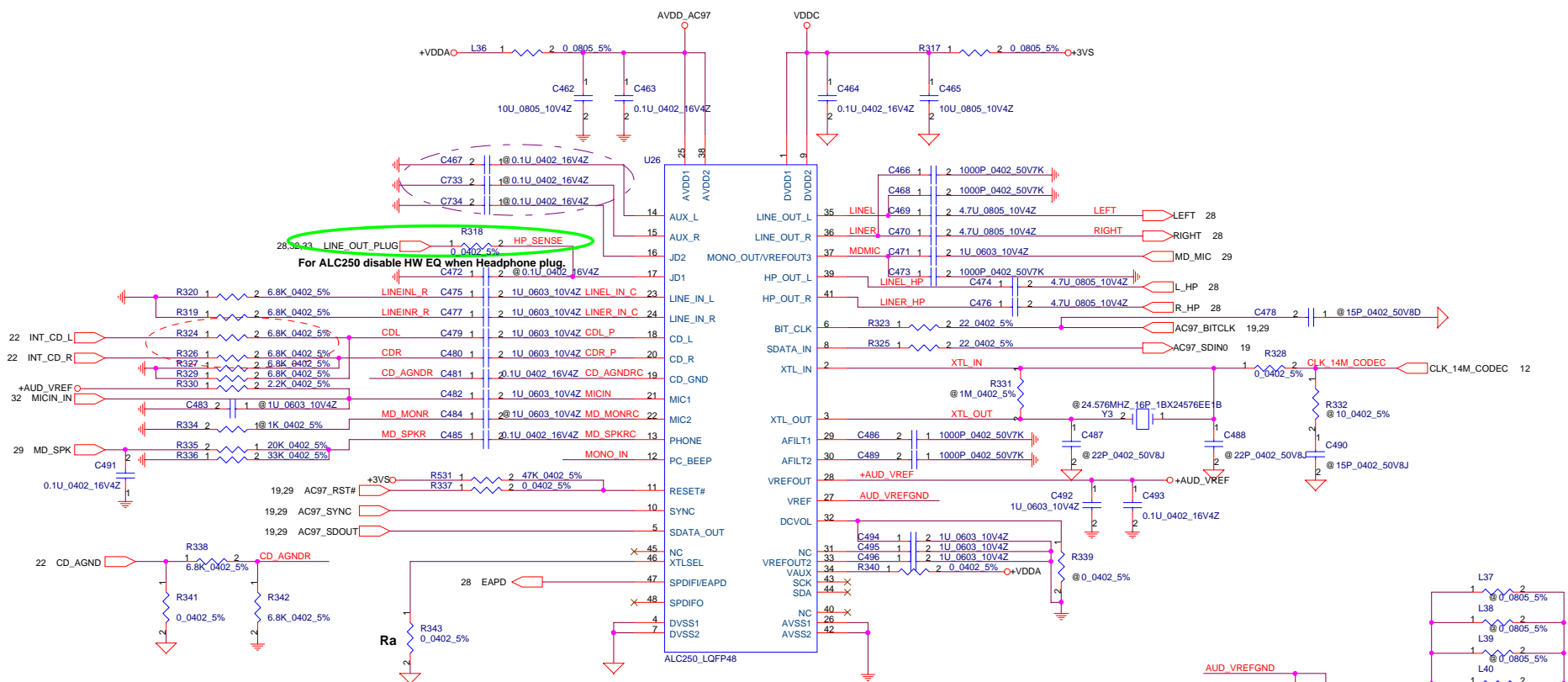


Note: Pin127,129 need be connected to GND

Compal Electronics, Inc.	
Title Mini PCI Slot	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.	Document Number LA-2251 Date: Monday, May 17, 2004
Rev 1.0	Sheet 26 of 47



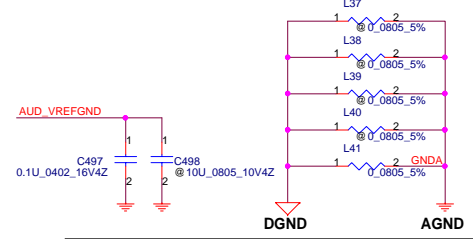
AC97 Codec



For ALC250 disable HW EQ when Headphone plug.

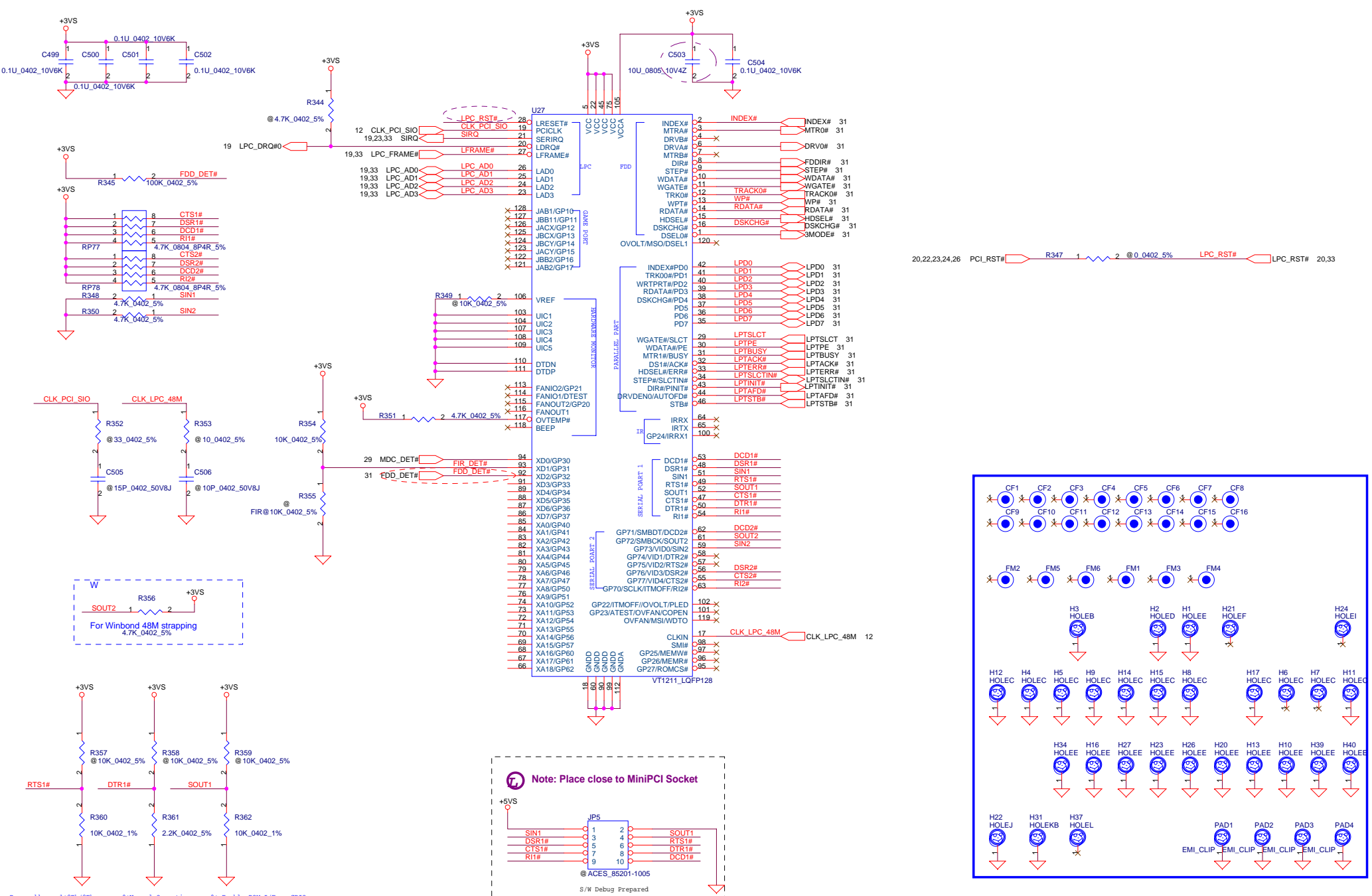
Ra	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

R345	Pin45	FREQ. SEL
X	X	24.576MHZ
ON	X	14.318MHZ
X	ON	48MHZ



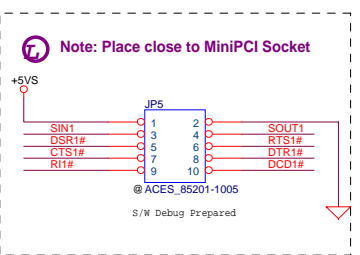
Compal Electronics, Inc.

AC97 CODEC-ALC250

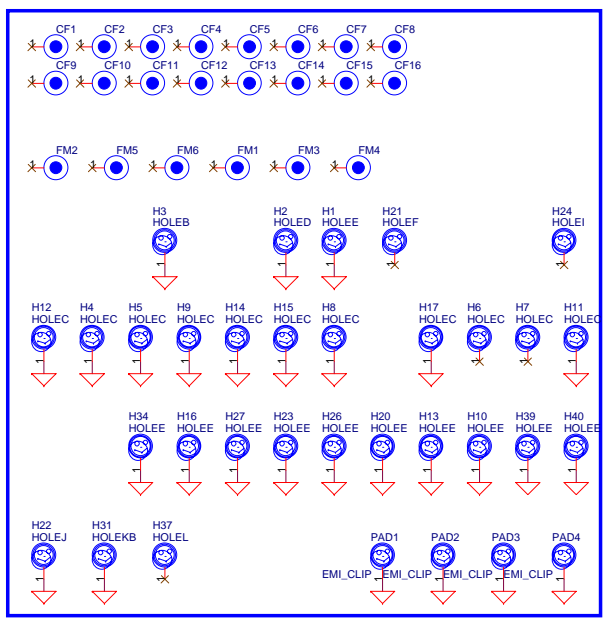


Base address 1:2Bh/2Fh 0:Normal Operation 0: Enable ROM I/F as GP10
 Base address 0:4Bh/4Fh 1:Test Mode 1:Enable Flash Rom

Super I/O strapping for VT1211



Note: Place close to MiniPCI Socket



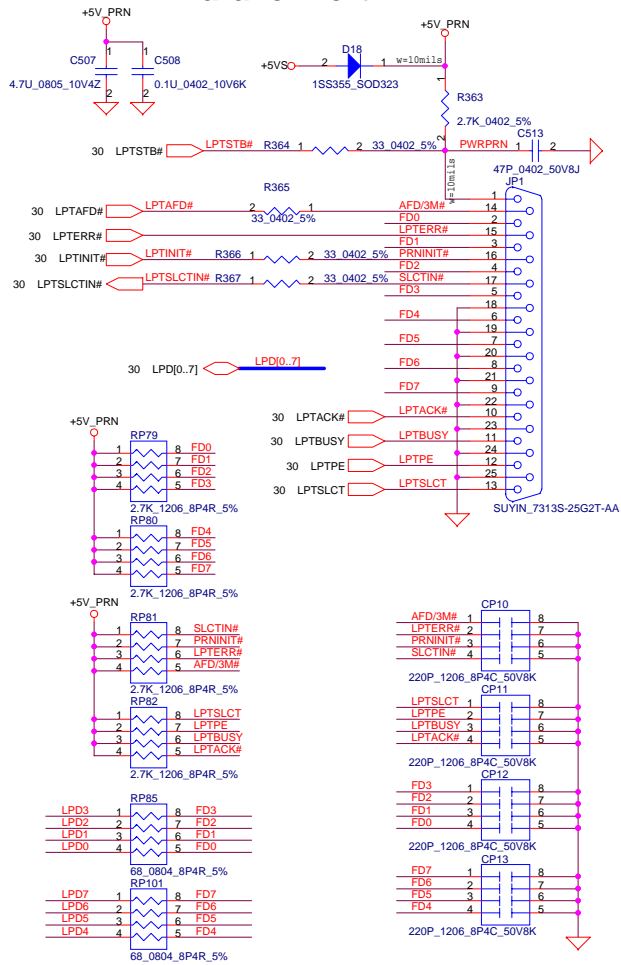
Compal Electronics, Inc.

LPC SUPER I/O VIA VT1211

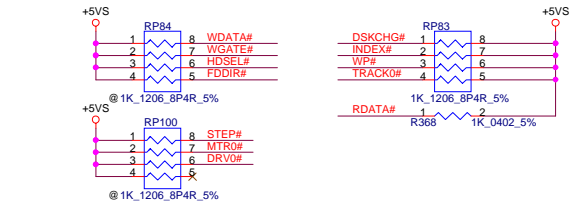
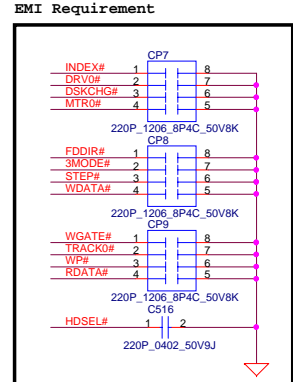
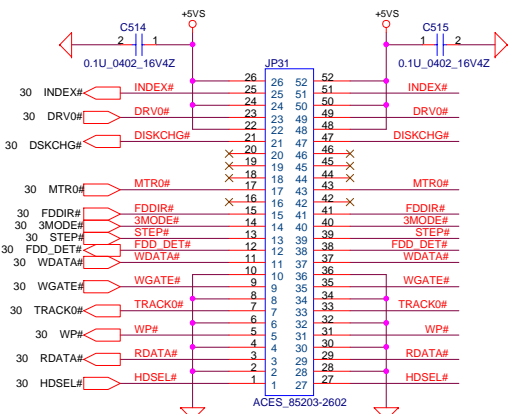
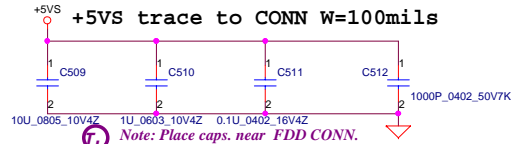
Title: _____
 Revision: _____
 Date: Monday, May 17, 2004 Sheet 30 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Parallel Port



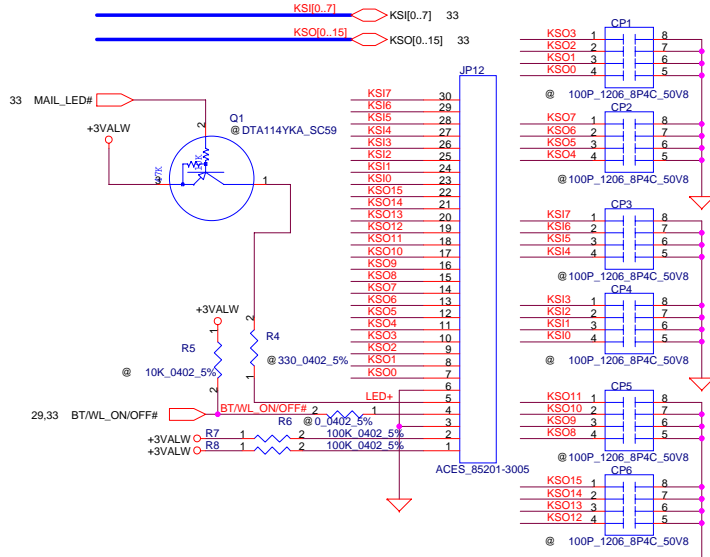
FDD CONN.



Compal Electronics, Inc.

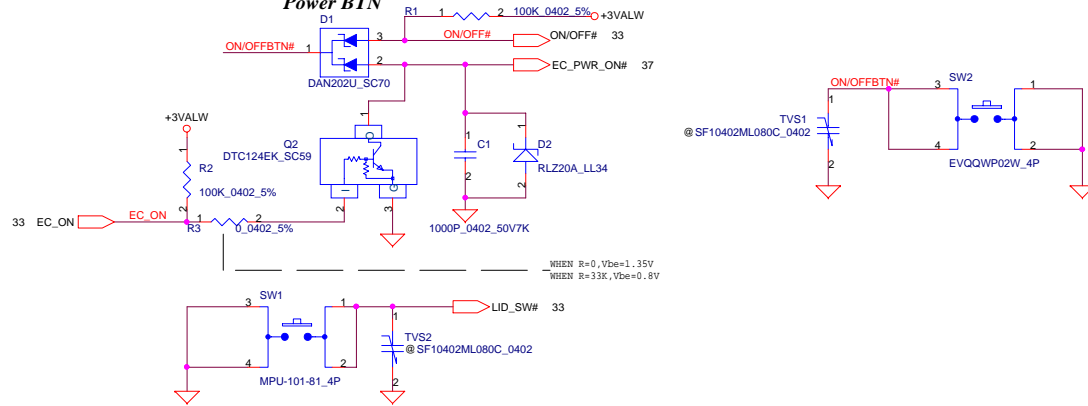
Parallel port and FDD Conn.

INT_KBD CONN.

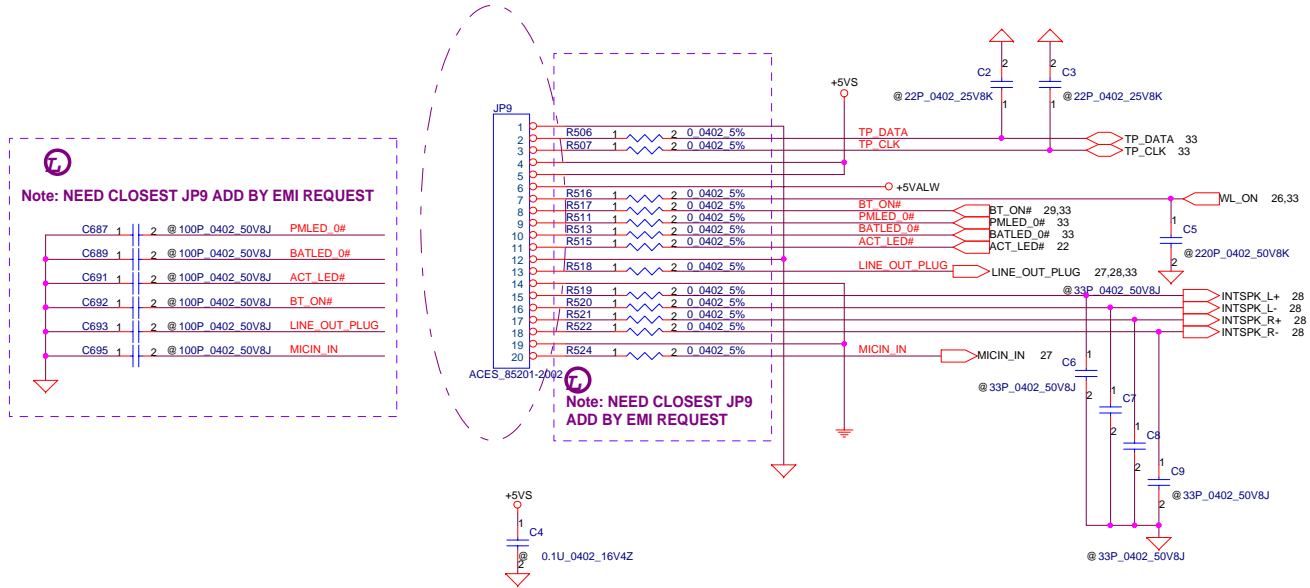


Note: NEED CLOSEST JP18 ADD BY EMI REQUEST

Power BTN



Touch Pad & Status LED Conn.





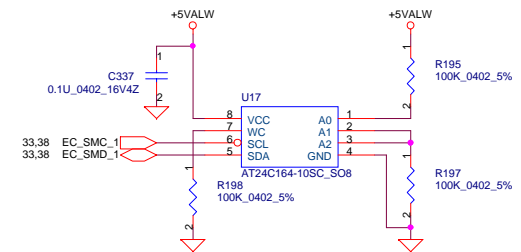
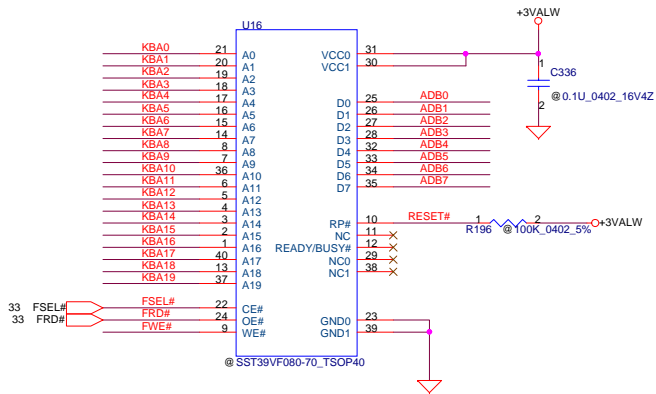
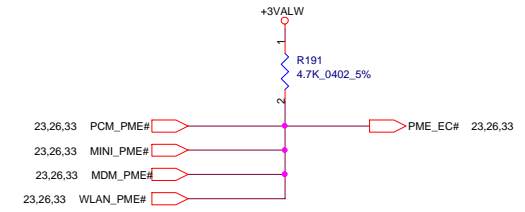
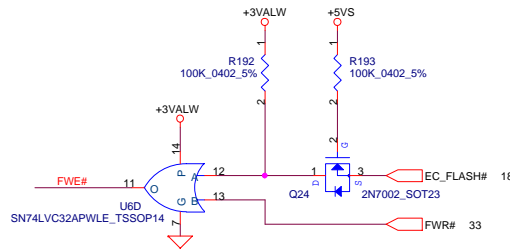
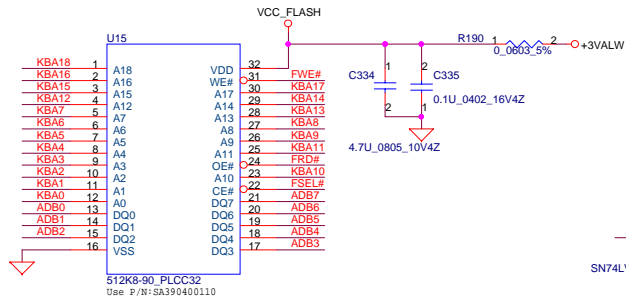
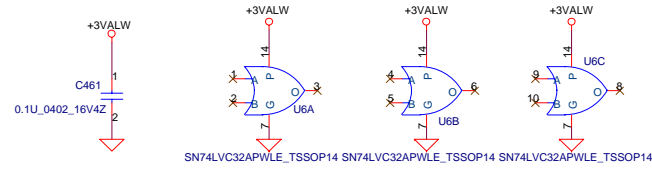
Note: NEED CLOSEST JP9 ADD BY EMI REQUEST

Note: NEED CLOSEST JP9 ADD BY EMI REQUEST

Compal Electronics, Inc.	
KBD,ON/OFF,T/P & LED	
Title KBD,ON/OFF,T/P & LED Department Number DIVISION OF R&D CONTAINING DATE:	Rev 1.0 Monday, May 17, 2004 Sheet 32 of 47

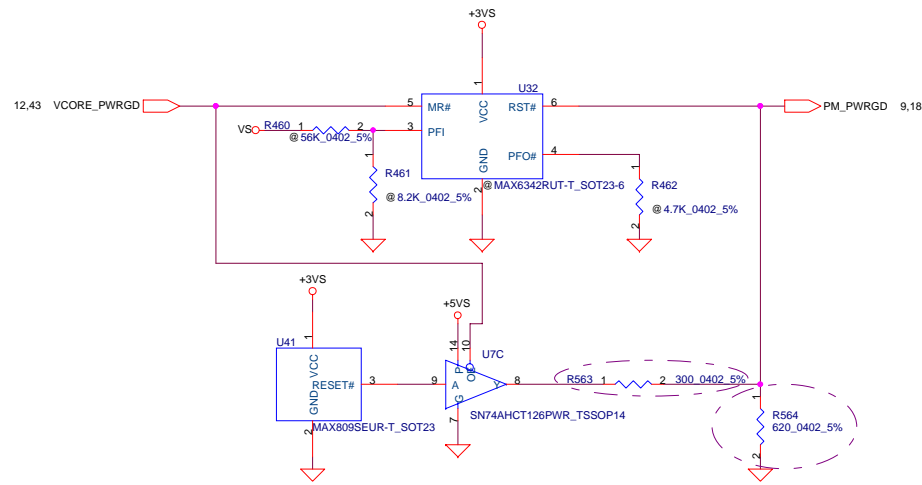
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

33 ADB[0..7]  ADB[0..7]
 33 KBA[0..19]  KBA[0..19]



Compal Electronics, Inc.

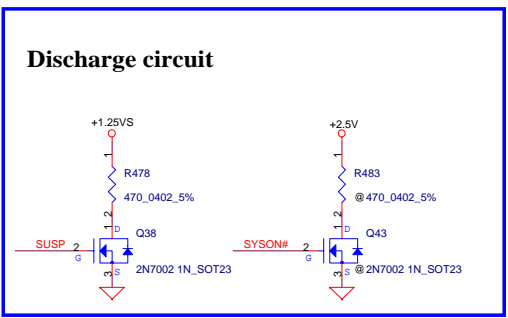
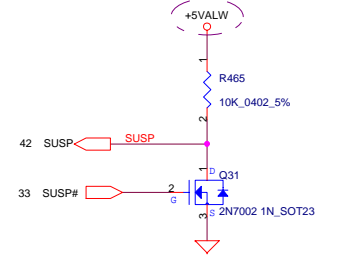
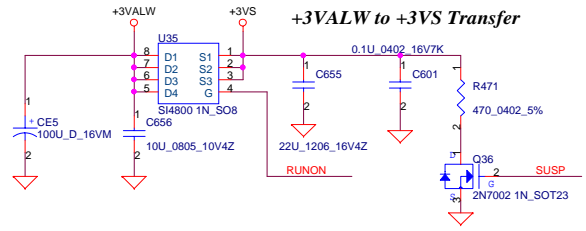
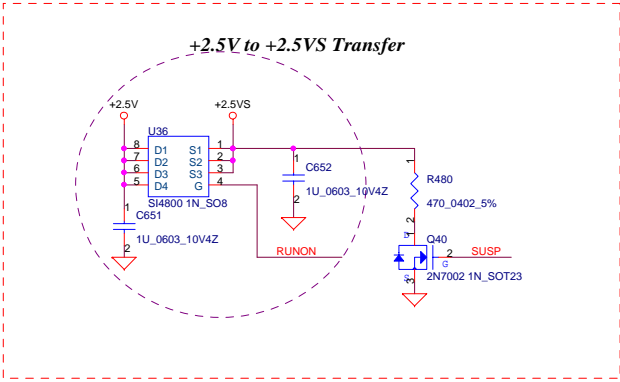
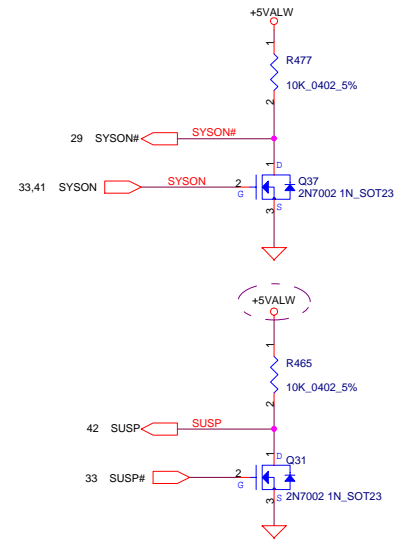
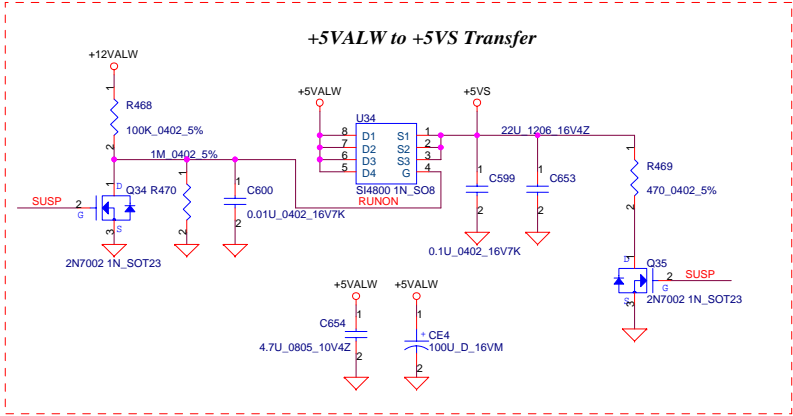
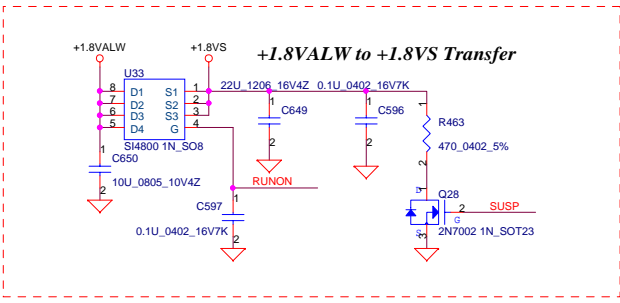
BIOS & EC I/O Port



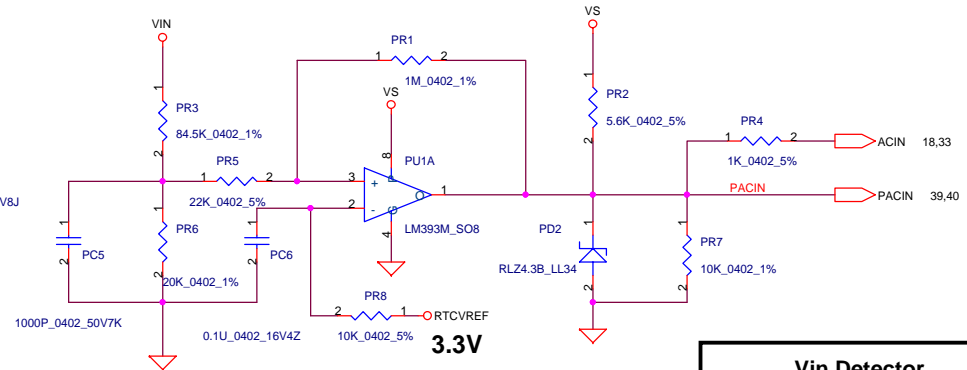
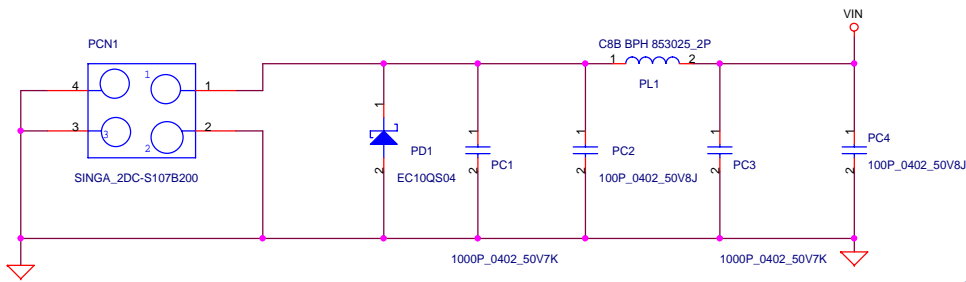
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.	
RESET & PS2 Connector	
Document Number LA-2251	Rev 1.0
Date: Monday, May 17, 2004	Sheet 35 of 47

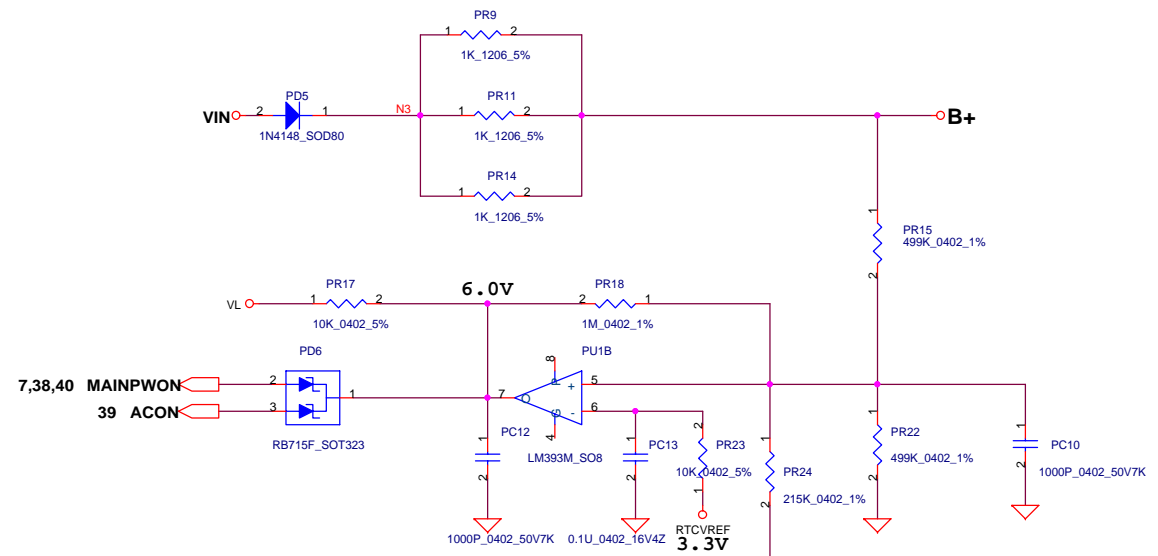
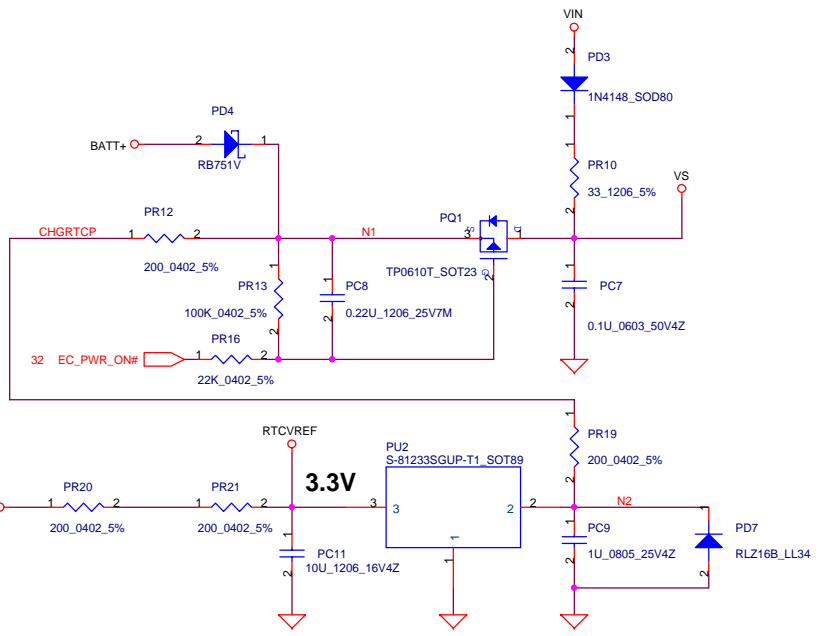
1.8VALW/+1.5VS Power direct provide



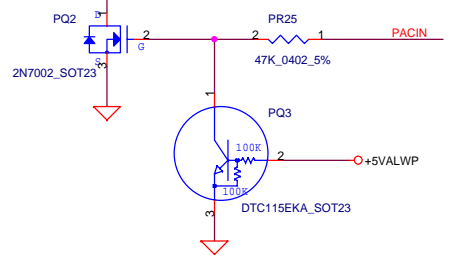
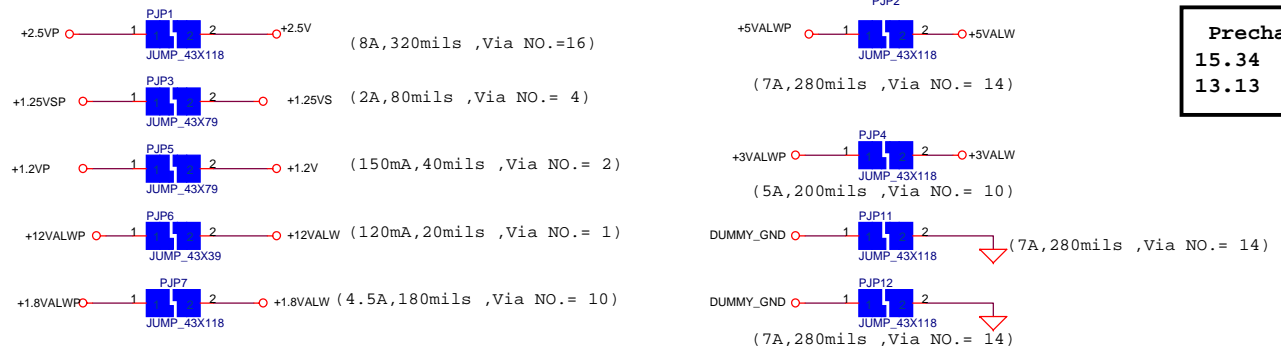
+1.8VS	C727	1	2	@ 0.1U 0402 16V7K	+2.5V
+1.8VS	C721	1	2	@ 0.1U 0402 16V7K	+2.5V
+1.8VS	C722	1	2	@ 0.1U 0402 16V7K	+3VS
+1.8VS	C723	1	2	@ 0.1U 0402 16V7K	+5VS
+2.5V	C724	1	2	@ 0.1U 0402 16V7K	+3VS
+2.5V	C725	1	2	@ 0.1U 0402 16V7K	+5VS
+3VS	C726	1	2	@ 0.1U 0402 16V7K	+5VS
+3VALW	C673	1	2	0.1U 0603 50V4Z	+5VS
+2.5V	C674	1	2	0.1U 0603 50V4Z	+5VS
+2.5V	C675	1	2	0.1U 0603 50V4Z	+3VALW
+1.8VS	C676	1	2	0.1U 0603 50V4Z	+3VS



Vin Detector
High 17.58
Low 14.11

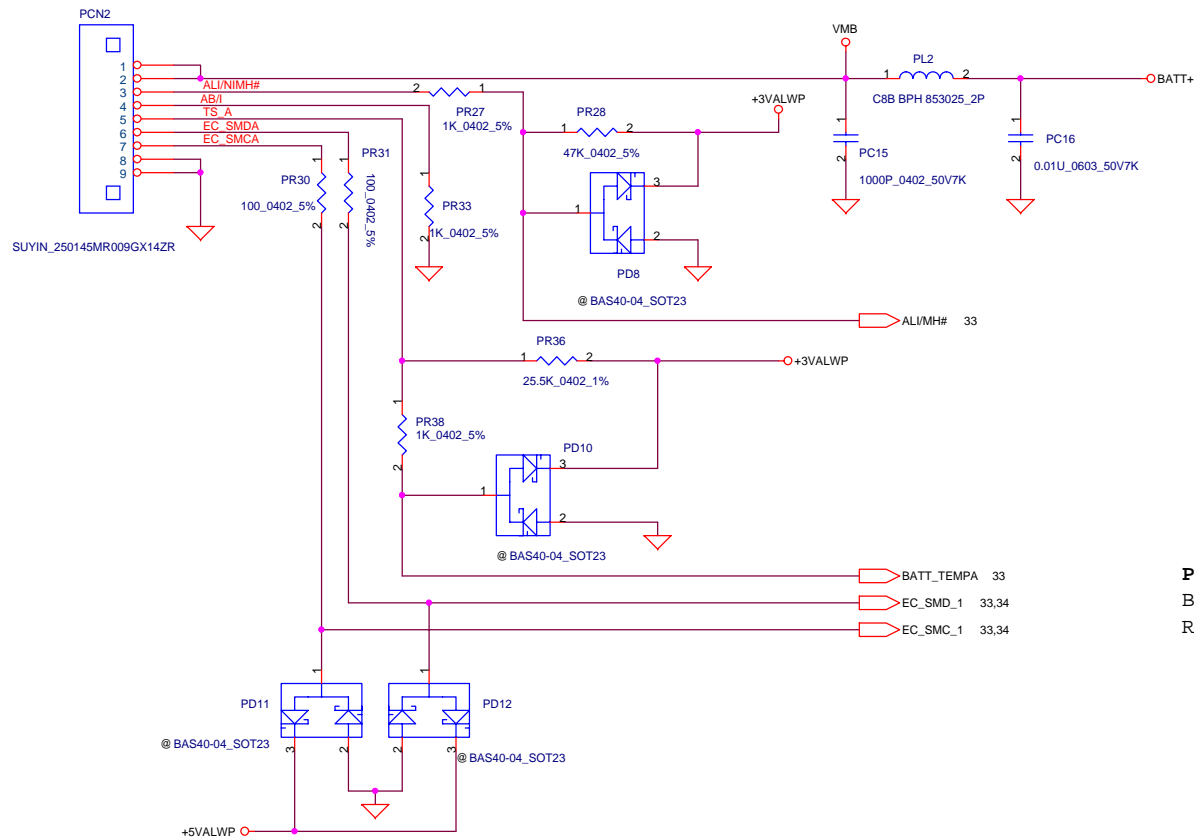


Precharge detector
15.34 15.90 16.48
13.13 13.71 14.20

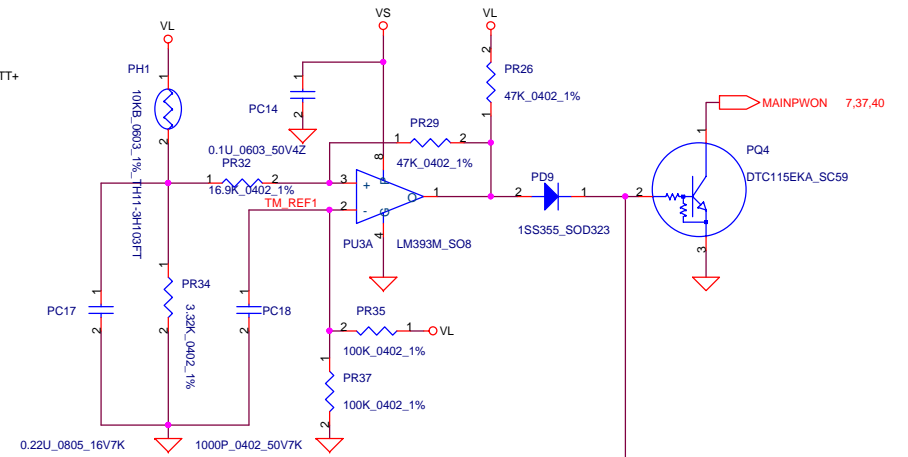


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

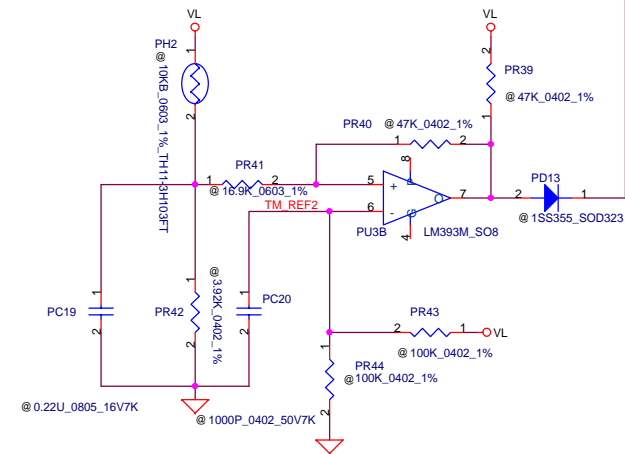
CHANGE CONNECTER



PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



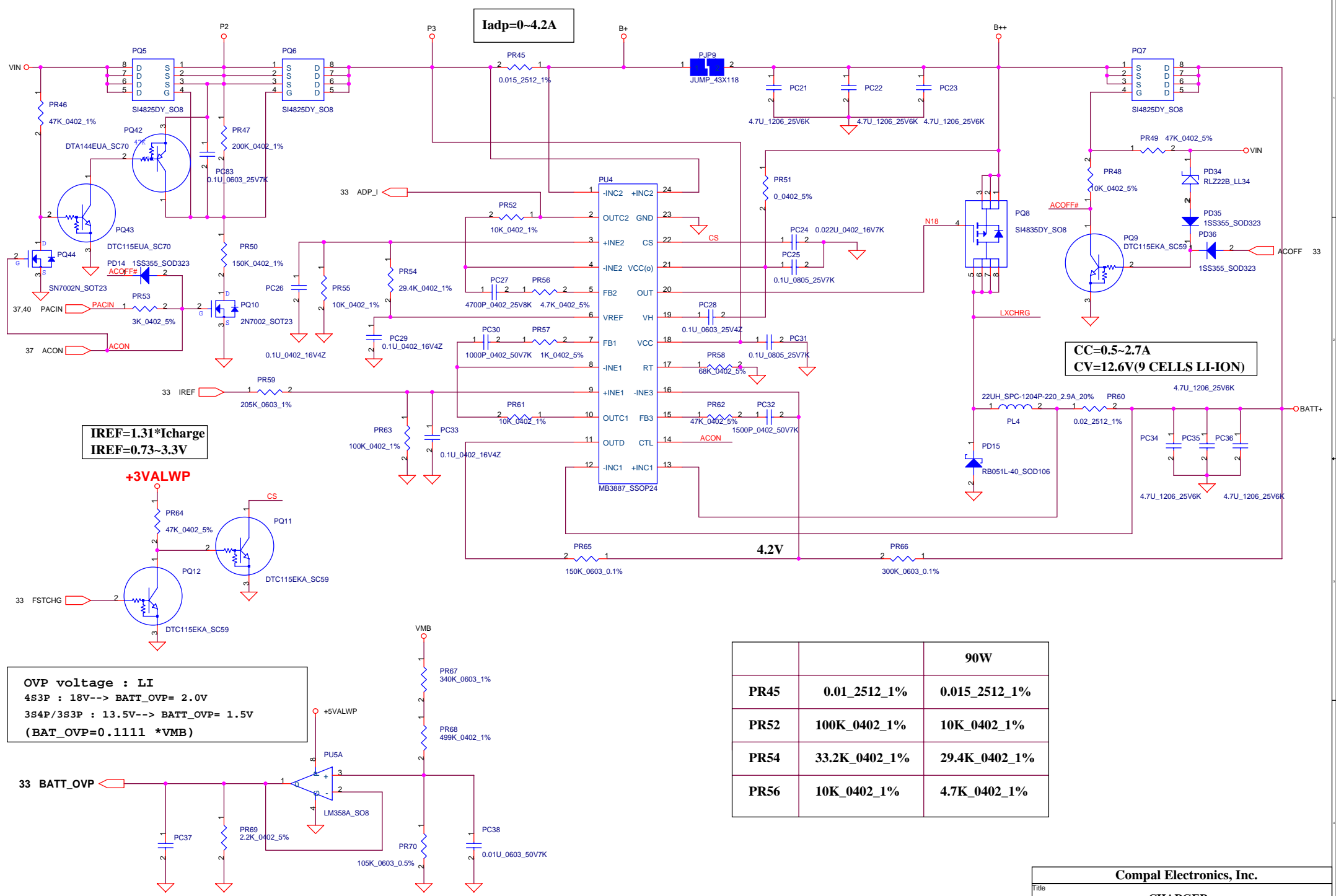
PH2 near main Battery CONN :
 BAT. thermal protection at 78 degree C
 Recovery at 45 degree C



Compal Electronics, Inc.

Title	BATTERY CONN / OTP	
Document Number	LA-2251	
Rev	1.0	
Date:	Monday, May 17, 2004	Sheet 38 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



I_{adp}=0~4.2A

CC=0.5~2.7A
CV=12.6V(9 CELLS LI-ION)

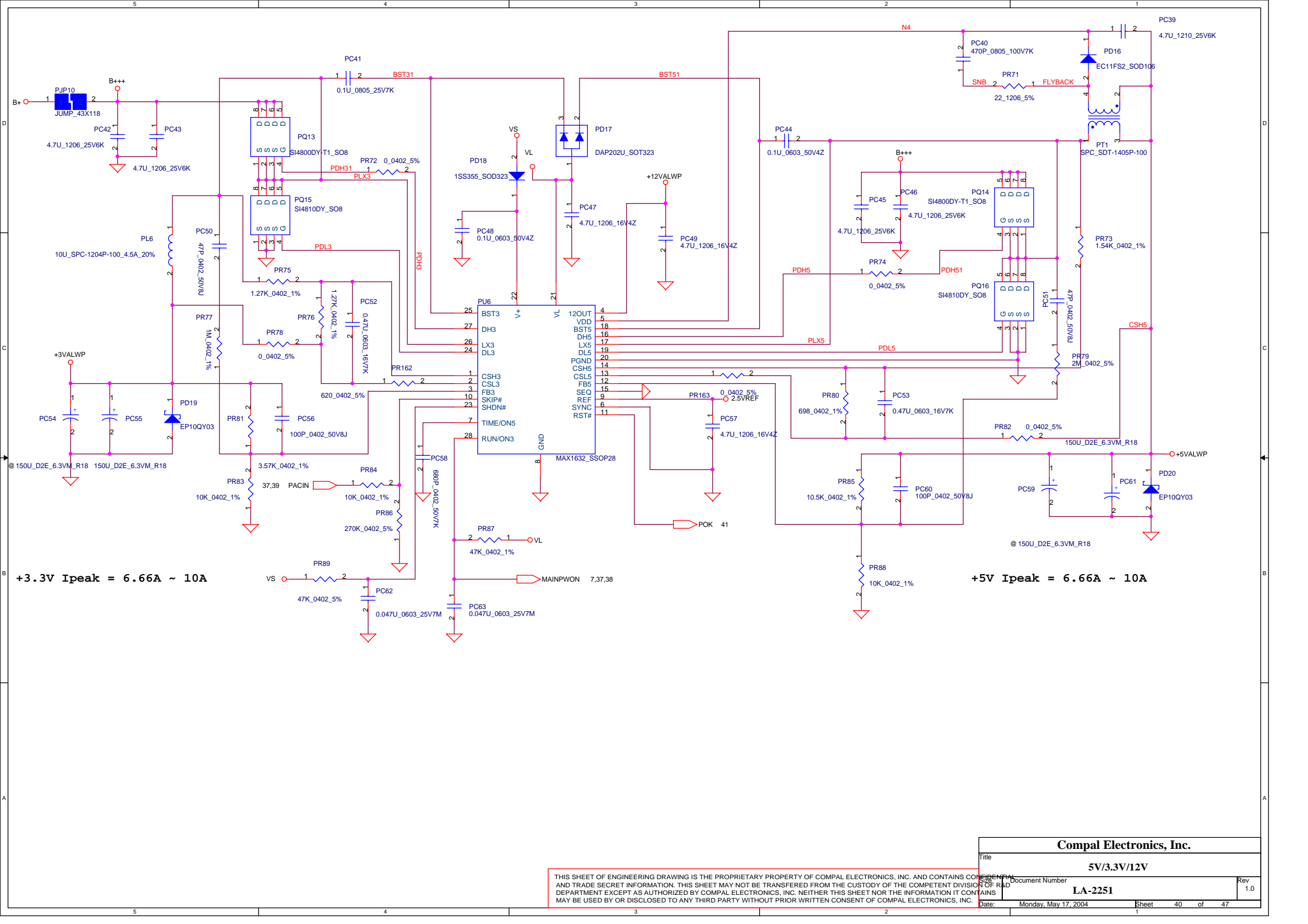
I_{REF}=1.31*I_{charge}
I_{REF}=0.73~3.3V

+3VALWP

OVP voltage : LI
4S3P : 18V--> BATT_OVP= 2.0V
3S4P/3S3P : 13.5V--> BATT_OVP= 1.5V
(BATT_OVP=0.1111 *VMB)

		90W
PR45	0.01_2512_1%	0.015_2512_1%
PR52	100K_0402_1%	10K_0402_1%
PR54	33.2K_0402_1%	29.4K_0402_1%
PR56	10K_0402_1%	4.7K_0402_1%

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

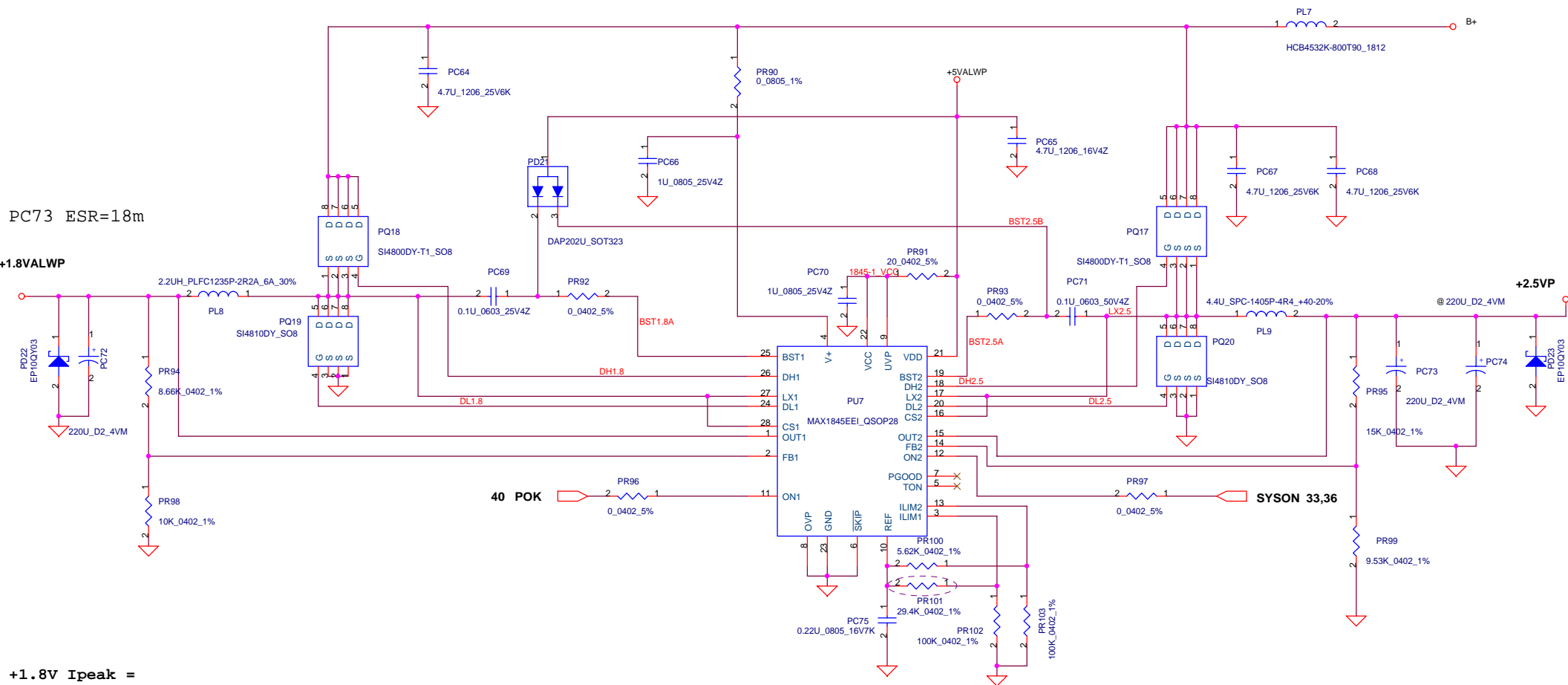


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

Compal Electronics, Inc.	
Title	5V/3.3V/12V
Document Number	LA-2251
Date	Monday, May 17, 2004
Sheet	40 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

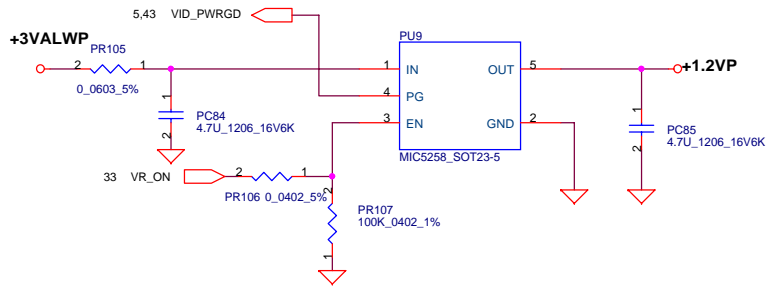
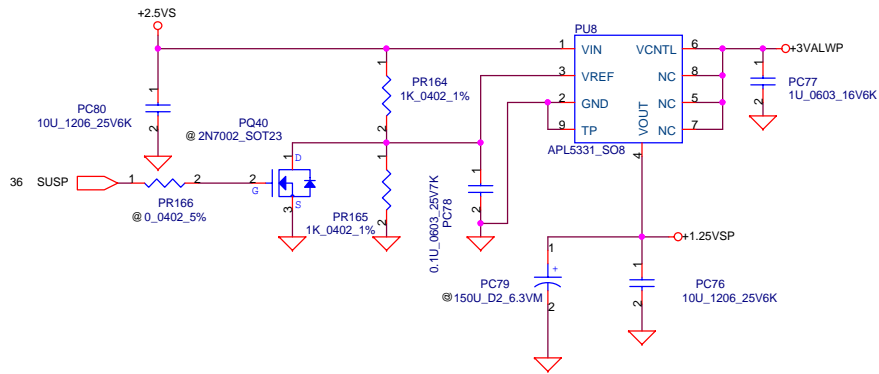


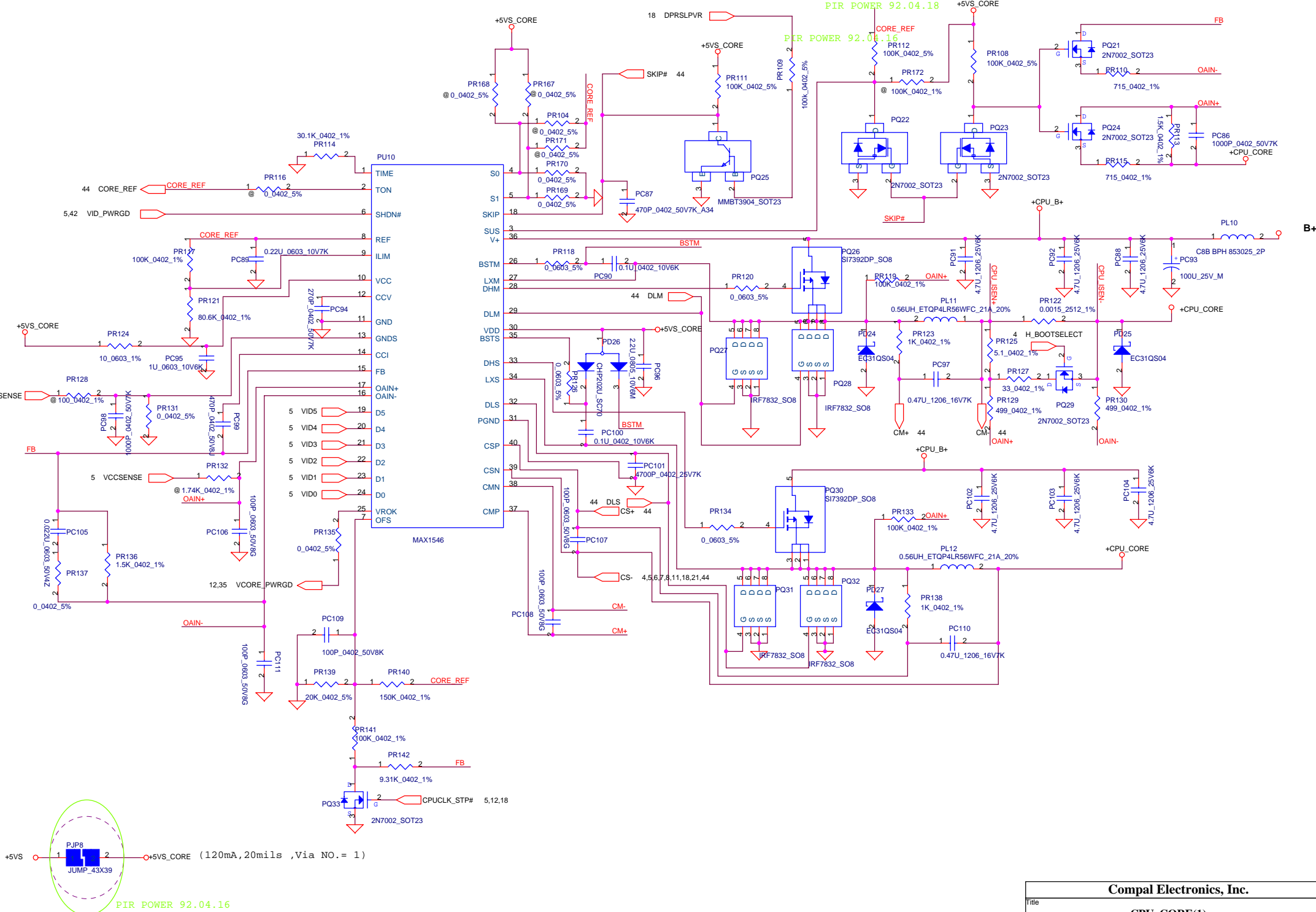
PC73 ESR=18m

+1.8VALWP

+1.8V Ipeak =

+2.5V Ipeak = 12.06A ~ 22.41A

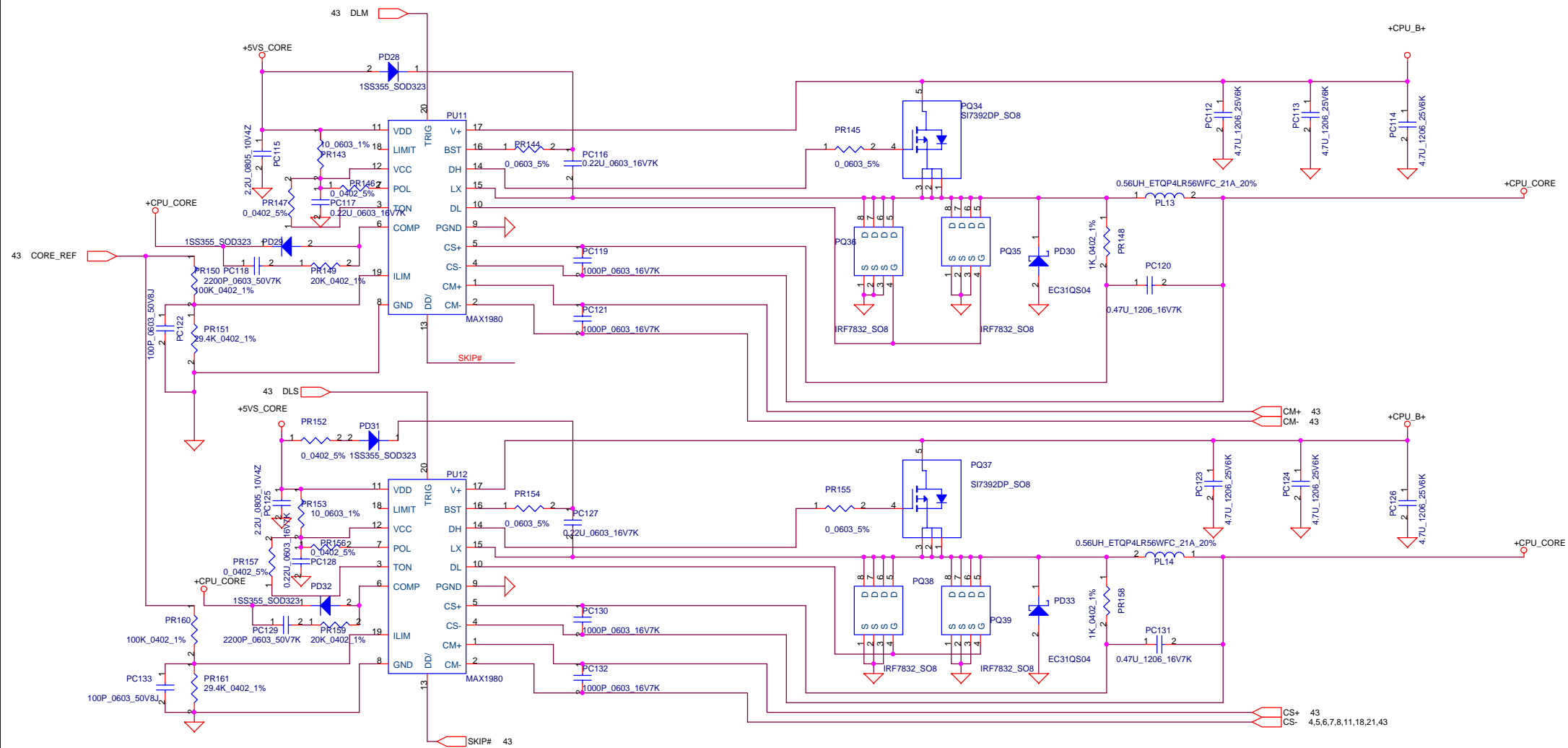




PIR POWER 92.04.16

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
CPU_CORE(1)		
Sheet	Document Number	Rev
LA-2251		1.0
Date:	Monday, May 17, 2004	Sheet 43 of 47



120W	POP	PD28, PC115, PR143, PR144, PC116, PR146, PR147, PC117, PD29, PR149, PC118 PR150, PR151, PC122, PU11, PC119, PC121, PQ34, PQ36, PQ35, PD30, PL13, PR148, PC120
90W	UNPOP	PD28, PC115, PR143, PR144, PC116, PR146, PR147, PC117, PD29, PR149, PC118 PR150, PR151, PC122, PU11, PC119, PC121, PQ34, PQ36, PQ35, PD30, PL13, PR148, PC120

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Description	Rev.
1	41	Wrong net	12/23/2003	Compal	Modify control signal for 2.5VSP & 1.8VALWP	0.2
2	43	For C3,C4 function	12/23/2003	Compal	Add 0 0402 5% Location is PR104,PR167,PR168,PR169,PR170,PR171.Add 100k 0402 5% Location PR172	0.2
3	43	Power	12/25/2003	Compal	Add PU13,PR173,PR174,PR175,PC81,PR176,PR177,PR179,PQ41,PR178,PC82 for monitor CPU POWER	0.2
4	39,40 41,43	For EMI cost down	02/13/2004	Compal	Del PL3,PL5,PL7,PL10 and add jump on it's location	0.2
5	39	Power	02/26/2004	Compal	Add component for charger 使背對背快速TURN OFF	0.2
6	41	Power	04/12/2004	Compal	Add PL7 avoid B+ noise interference	0.2
7	43	Power	04/12/2004	Compal	Add PL10 avoid B+ noise interference	0.2
8	43	Power	04/12/2004	Compal	Delete PU13,PR174,PR173,PR175,PC81,PR176,PR177,PQ41,PR178,PR179,PC82 for EC measure V_CORE power function	0.2
9	43	Power	04/12/2004	Compal	Change PR110,PR115 from 1K to 715 and change PR113,PR136 from 2.7k to 1.5k for modify load line from 2.5m to 1.5m	0.2

Compal Electronics, Inc.			
Changed-List History-1			
Size	Document Number	Rev	
	LA-2251	1.0	
Date:	Monday, May 17, 2004	Sheet	45 of 47

DFY30 from Pre-DB Step to DB-Step LA-2251 REV:0.0 -> 0.1 Modify <92.12.08.~93.02.05. >

1. Pull High 2.2Kohm_0402 from NB_I2CDATA/NB_I2CCLK to +3VS for panel I2C sense function . <Page 16> 92.12.25.
-Add R525,R526(2.2Kohm_0402) and related net . (Modify CKT,BOM&Layout)
2. Add Prescott C-step Processor reserve schematic . <Page 8,18> 92.12.30.
-Reserve R532(@470ohm_0402),R533(@1Kohm_0402),Q44(@2N7002),add R534(0ohm_0402) and related net . (Modify CKT,BOM&Layout)
3. Update ICS952013 CLK GEN. U21 CIS library . <Page 12> 92.12.31.
-Update U21(ICS952013) . (Modify CKT&Layout)
4. Remove ISOLATE function selection resistors for cost down . <Page 25> 92.12.31.
-Remove R49,R429(from 5.1K_0402_5% to @5.1K_0402_5%) . (Modify CKT&BOM)
5. Modify Prescott C-step Processor reserve schematic . <Page 18> 92.12.31.
-Modify net (H_PWRGOOD_SB and EC_ACIN) connection with U28 . (Modify CKT&Layout)
6. Add Pull High schematic for KBC ENE-KB910 . <Page 33> 92.12.31.
-Reserve R202(@10K_0402) for KBA1 . (Modify CKT&Layout)
-Add R194(10K_0402) for KBA4 . (Modify CKT,BOM&Layout)
7. Modify Material for CIS/BOM match . <Page 12> 92.12.31.
-Change C407.C419(from SE077106M00(1206) to SE053106Z00(0805)) . (Modify CKT&BOM)
8. Modify SB GPIO connection and PH/PL states . <Page 18> 93.01.02.
-Add R387,R388,R389(10Kohm_0402);Del R375(51Kohm_0402),R376,R382,R383(10Kohm_0402) . (Modify CKT,BOM&Layout)
9. Add RC termination for Thermal IC ADM1032 recommend . <Page 7> 93.01.05.
-Add R535(0ohm_0402) between +3VALW and U1.1 . (Modify CKT,BOM&Layout)
10. Change AAT14610's enable pin from SYSON to SYSON# . <Page 29> 93.01.05.
-Change U10.4 and U11.4's net from SYSON to SYSON# . (Modify CKT&Layout)
11. Change BIOS IC's P/N and wait CIS updated . <Page 34> 93.01.05.
-Change U15's P/N from SA390400100 to SA390400110 . (Modify CKT&BOM)
12. Remove Modem related EMI/Safety reserve material for cost down . <Page 29> 93.01.05.
-Remove VH1(@DSSA-P3100SB),C294,C295(@220P_1808_3KV8K) . (Modify CKT&BOM)
13. Change SI2306 to SI4800 for Cost Down . <Page 36> 93.01.07. **BOM Release.**
-Del Q30(SI2306DS),Add U36(SI4800) and modify related net connection . (Modify CKT,BOM&Layout)
14. Change U25F to U24F for Cost Down . <Page 27> 93.01.07.
-Del U25 , Change U25F to U24F(74LVC14) and modify related net connection . (Modify CKT,BOM&Layout)
15. Correct LCDVDD/B+ EMI solution . <Page 17> 93.01.08. **Net-In 8nd .**
-Change L3(from FBM-L11-*_0805 to 0ohm_0805),Add L18(FBM-L11-*_0805) between B+ and JP2.1,remove C215(@68P_0402),Remove Q12(@2N7002) . (Modify CKT,BOM&Layout)
16. Change the CPU related schematic for Cost Down . <Page 5> 93.01.08.
-Del R26(56ohm_0402) and change the net(H_TESTHI2_7) to RP1.1 PH . (Modify CKT,BOM&Layout)
17. Correct the NET Name for EC define clear . <Page 10,12,18,33> 93.01.08.
-Change the NET from SLP_S3# to S3AUXSW# . (Modify CKT&Layout)
-Change the D26.1&U28.F5's NET from PCI_STOP# to PCICLK_STOP# . (Modify CKT&Layout)
-Change the NET from SLP_S5# to PSON# . (Modify CKT&Layout)
18. Change PCIPIRQ connection . <Page 26> 93.01.08.
-Change R115.1 from PCI_PIRQC# to PCI_PIRQB,R117.2 from PCI_PIRQD# to PCI_PIRQB . (Modify CKT&Layout)
19. Modify AC97_Codec related schematic . <Page 27> 93.01.08.
-Add R537(0ohm_0402) between U24.12 and C454.1,add R536(10Kohm_0402) between U23.4 and U23.8 . (Modify CKT,BOM&Layout)
20. Short all Jopen Pad Named JSH? for GerberOut Prepared . <Page 8,9,18> 93.01.08.
-Short JSH1~9(JOPEN) . (Modify CKT&Layout)
21. Remove some parts about EMI related for cost down . <Page 23,26,27,29,> 93.01.12.
-Remove R69,R121,R153(@10ohm_0402),C184,C259,C478(@15P_0402),C296(@22P_0402) . (Modify CKT&BOM)
22. Remove some parts about EE related for cost down . <Page 29,> 93.01.12.
-Remove C299,C307,C311(@1000P_0402_50V) . (Modify CKT&BOM)
23. Remove some parts about USB related for Function Trial . <Page 19> 93.01.12.
-Remove R440,R441,R444(@10K_0402) . (Modify CKT&BOM)
24. Modify Material P/N for BOM correction . <Page 8,9,10,18,19,21> 93.01.12.
-Modify C356,C357,C360,C361,C363,C366,C367,C370,C382,C385,C389,C391,C392,C394,C396,C397,C402,C405,C526,C528,C530,C550,C557,C600(from P/N:SE076103Z00 to SE076103K00) . (Modify CKT&BOM)

25. Modify Material P/N for Purchase Dept. Recommend . <Page 25> 93.01.12.
-Modify C542(from P/N:SE068102K00 to SE074102K00) . (Modify CKT&BOM)
26. Remove some material EMI related for Cost Down . <Page 7,17,23,26,27,32,> 93.01.13.
-Remove C15,C16(@0.001U_0402_50V),C189,C190,C193,C194,C254,C257,C262,C267,C270(@1000P_0402_50V),C2,C3(@22P_0402_25V),C4(@0.1U_0402_16V),C5(@220P_0402_50V),C6,C7,C8,C9(@33P_0402_50V),CP1-CP6(@100P_1206_8P4C_50V8K) . (Modify CKT&BOM)
-Change L18(from KC FBM-L11-201209-221LMAT_0805 to 0ohm_0805),L36(from HB-1M2012-121JT03_0805 to 0ohm_0805) . (Modify CKT,BOM&Layout)
27. Modify Material P/N for BOM items simplify (Cost is the same) . <Page 25> 93.01.14.
-Modify C531(22U_1206_16V from P/N:SE021226Z10 to SE021226Z00) . (Modify CKT&BOM)

A-TEST SMT BUILT

DFY30 from DB-Step to Pre SI-Step LA-2251 REV:0.1 -> 0.2 Modify <93.02.06.~93.03.08. >

28. Modify "CPUCLK_STP#" related schematic for Risk fixed and Cost Down . <Page 5,12,18> 93.02.16.
-Add Q45(SB339040100) , R539(SD028120200) , R540(SD028100100) and R541(SD028000000);del D27(SC1B751V005) & R278(SD028100200) and modify the related schematic . (Modify CKT,BOM&Layout)
29. Modify "PWRBTN_OUT#" related schematic for Cost Down . <Page 18> 93.02.16.
-Modify "PWRBTN_OUT#" related schematic and del R381(SD028100200) . (Modify CKT,BOM&Layout)
30. Change "FANSPEED1" and "FANSPEED2" pull high power source from +5VS to +3VS for power saving . <Page 7> 93.02.16.
-Change R12.1 and R13.1's connection from +5VS to +3VS . (Modify CKT&Layout)
31. LCD Connector combined with Inverter Connector for cost down . <Page 17> 93.02.16.
-Modify the related schematic and del JP2 . (Modify CKT,BOM&Layout)
32. Remove TV-OUT function . <Page 17> 93.02.16.
-Modify the related schematic and del D12,D13,D14,L5,L8,L9,C232C233,C234,C235,C236,C237,R97,R98,R99,JP19 . (Modify CKT,BOM&Layout)
33. Modify PCMCIA spec from 2 slots to 1 slot . <Page 23> 93.02.16.
-Change U4 CB1420 to CB1410 and U5 CP2216 to CP2211 , del R85,D6,R75,C195,C196,R77~R81,C211,C212,C213,C204,C203,C207,R87 , add C699 . (Modify CKT,BOM&Layout)
34. Change SI2302 to SI4800 for Cost Down . <Page 17> 93.02.16.
-Change Q13(P/N: SB523020005) to U40(P/N: SB548000100) and modify the related schematic (Modify CKT,BOM&Layout)
35. Add IEEE1394 function and related schematic/material . <Page 24> 93.02.16.
-Add C701,C702,C703,C704,C705,C706,C707,C708,C709,C713,C710,C711,C712,C714,C715,C716,JP23,R543,R547,R544,R545,R546,R550,R551,R548,R549,R552,R553,R554,R555,U38,U39,X1 and modify the related schematic . (Modify CKT,BOM&Layout)
36. Change JP9 from P/N: SP010019210 to SP010009910 for cost down . <Page 32> 93.02.16.
-Change JP9 from P/N: SP010019210 to SP010009910 , del R508,R509,R510,R523,C684,C685,C686,C694 and modify the related schematic . (Modify CKT,BOM&Layout)
37. Modify BIOS pin definition and remove BIOS beffer IC for cost down plan . <Page 33,34> 93.02.16.
-Del U13,U14,RP33,C331,RP32,R186,R189,C333,C332,R188 and modify the related schematic . (Modify CKT,BOM&Layout)
38. LED function re-defined for cost down plan . <Page 32,33> 93.02.20.
-Del C688,C690,R512,R514, and modify the related schematic . (Modify CKT,BOM&Layout)
39. Issue BEEP# from EC pin directly for cost down plan . <Page 27> 93.02.22.
-Move U6,U24 location ; Del R305,R308,R303(@),R537,C457 and modify the related schematic . (Modify CKT,BOM&Layout)
40. Add EMI request schematic for Inverter related reserved . <Page 17> 93.02.22.
-Add L59,L60,L61,L62(close to JP6) and modify the related schematic . (Modify CKT,BOM&Layout)
41. Add pull down design for "SYSON","SUSP#","EC_RSMRST#" floating risk . <Page 33> 93.02.22.
-Add R556,R557,R558(close to U12) and modify the related schematic . (Modify CKT,BOM&Layout)
42. Modify the "PCI_RST#" related schematic for Cost Down verified and prepared . <Page 20> 93.02.23.
-Add R559,R560,C717,R561,R562,R565; (Remove U24,C380,C452(@)) and modify the related schematic . (Modify CKT,BOM&Layout)
43. Change Reset IC from MAX6342RUT to MAX809SEUR for Cost Down . <Page 35> 93.02.23.
-Add U41,R563,R564 ; (Remove U32,R460,R461,R462(@)) and modify the related schematic . (Modify CKT,BOM&Layout)

----PLEASE SEE NEXT PAGE

Compal Electronics, Inc.		
HW2 EE Dept. PIR SHEET(1)		
Rev	1.0	
Date	Monday, May 17, 2004	Sheet 46 of 47

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

DFY30 from DB-Step to Pre SI-Step LA-2251 REV:0.1 -> 0.2 Modify <93.02.06.~93.03.09. >

- 44. Reserve EMI request design for LVDS clock related signal . <Page 9,16> 93.02.23.
-Add R566(@),C718(@),R567(@),R568(@),C719(@),C720(@),move R215 (close to U22) and modify the related schematic . (Modify CKT&Layout)
- 45. Create +PWR_PCM for U4(CB1410) core power +3VALW and +3VS power source option . <Page 23> 93.02.25.
-Modify the related schematic to change +3VALW to +PWR_PCM . (Modify CKT&Layout)
- 46. Reserve +3VS power source option for U4(CB1410) pin18&44 . <Page 23> 93.02.25.
-Add R569(@),R570(@)(close to U4) and modify the related schematic . (Modify CKT&Layout)
- 47. Reserve some CAPs for Power Plane through mode risk improved . <Page 36> 93.02.25.
-Add C721~C726(@) and modify the related schematic . (Modify CKT&Layout)
- 48. Cancel VGA_GND for EMI request . <Page 16,17> 93.03.02.
-Del L54,L55,L56,L57 and modify the related schematic . (Modify CKT,BOM&Layout)
- 49. Remove MiniPCI Modem function . <Page 26> 93.03.02.
-Del R123 , C266(@),C267(@),R122(@),C263(@) and modify the related schematic . (Modify CKT,BOM&Layout)
- 50. Remove MiniPCI Modem function . <Page 27> 93.03.03.
-Del R333, Remove R334,C484(Close to Pin22) and modify the related schematic . (Modify CKT,BOM&Layout)
- 51. Modify Pull High Resistor Value from 100K to 10K for standard design . <Page 12> 93.03.03.
-Modify R527 from 100Kohm to 10Kohm . (Modify CKT&BOM)
- 52. Remove some parts because remove ACER keyboard function . <Page 32> 93.03.03.
-Remove Q1,R4,R5,R6 . (Modify CKT&BOM)
- 53. Add the Pull High Resistor to enable the VGA tuned function for SIS request . <Page 09> 93.03.03.
-Add R210 (P/N: SD028470100/ S RES 1/16W 4.7K +-5% 0402) . (Modify CKT&BOM)
- 54. Modify the resistor's value to 1Mohm for SI4800 design . <Page 17> 93.03.03.
-Change R91(P/N: SD028150300 to SD028100400) . (Modify CKT&BOM)
- 55. Modify NB_RST# related and change LPC_RST# resistor value for signal quality improved . <Page 20> 93.03.09.
-Change R346(0ohm->10ohm) ; Add R571(10ohm) . (Modify CKT,BOM&Layout)
- 56. Change SIS302ELV pin60 level latch power source from +3VS to +1.8VS(same as SIS661FX U18.W3 power source) for SIS Design Change . <Page 16> 93.03.09.
-Change L47.1's power source from +3VS to +1.8VS . (Modify CKT&Layout)
- 57. Modify PCI_RST# related and change PCI_RST# resistor value for signal rising time risk fixed . <Page 20> 93.03.18.
-Change R562(1Kohm->300ohm);R565(2Kohm->620ohm);Remove C717(10PF_0402).(Modify CKT&BOM)
- 58. Modify PM_PWRGD related and change PM_PWRGD resistor value for signal rising time risk fixed . <Page 35> 93.03.18.
-Change R563(1Kohm->300ohm) ; R564(2Kohm->620ohm) . (Modify CKT&BOM)
- 59. Pull Down BT_WAKE_UP signal . <Page 33> 93.03.19.
~~Add C330(100K_0603ohm,SD0131003T4) . (Modify CKT&BOM)~~
- 60. Change Material to meet Layout Size . <Page 30> 93.03.19.
-Change C503(10U_1206->10U_0805)(SE054106Z10->SE054106Z10) . (Modify CKT&BOM)
- 61. Disconnect CPUCLK_STP# to CLK_GEN . <Page 12> 93.03.19.
-Remove R541(@0ohm) . (Modify CKT&BOM)
- 62. Update PCMCIA SOCKET JP15 Library . <Page 23> 93.03.22.
-Update JP15 CIS library . (Modify CKT&Layout)
- 63. Correct H_FERR# have double Pull High problem . <Page 05> 93.04.05.
~~Remove R18(56ohm) . (Modify CKT&BOM)~~
- 64. Modify JP26 pin4 connection for Pioneer ODD(DVD Dual DVR-K12TBC/DVR-K13TBC) used . <Page 22> 93.04.08.
-Reserve R572(@0ohm_0402) . (Modify CKT,BOM&Layout)
- 65. Add Decoupling Capacitor 220PF close to DDR Clock Buffer for EMI request . <Page 13> 93.04.10.
-Add C728,C729(220PF_0402) close to U20 . (Modify CKT,BOM&Layout)
- 66. Add Decoupling Capacitor 220PF close to NB M661FX VDDM for EMI request . <Page 11> 93.04.10.
-Add C730,C731,C732(220PF_0402) close to U18 . (Modify CKT,BOM&Layout)
- 67. Modify H_TESTHI2_7 Pull-High Resistor connection for Layout placement issue . <Page 05> 93.04.10.
-Add R573(56ohm_0402) close to JP25 . (Modify CKT,BOM&Layout)
- 68. Del H19 for PCB space free . <Page 30> 93.04.10.
-Del H19 . (Modify CKT&Layout)

- 69. Modify Audio Codec pins connection related to fix the noise issue . <Page 27> 93.04.12.
-Remove C467(@0.1UF_0402) . (Modify CKT&BOM)
-Reserve C733,C734(@0.1UF_0402) . (Modify CKT&Layout)
- 70. Modify JP32 power source pins connection for new CardReader Board cost down and SB chip power issue fixed . <Page 29> 93.04.12.
~~Change JP32.1&JP32.7 from +5VS to +3VALW ; JP32.2&JP32.8 from +5VS to +3VS . (Modify CKT&Layout)~~
- 71. Modify the USB ports definition and related connection for SB USB power source issue improved . <Page 19,29> 93.04.12.
-Change USB ports from P0 to P3 ; P3 to P5 ; P5 to P4 ; P4 to P0 . (Modify CKT&Layout)
-Remove OVCUR#5 R496(@10K_0402) , Add OVCUR#0 R440(10K_0402) . (Modify CKT&BOM)
- 72. Add BT_WAKE_UP Pull Down resistor . <Page 33>93.04.12.
-Add R574(100Kohm_0402) . (Modify CKT,BOM&Layout)
- 73. Add some material to BOM for EMI request . <Page 9,13,19>93.04.15.
-Add C406,C545(10PF_0402) . (Modify CKT&BOM)
-Add R566,R442(12ohm_0402) . (Modify CKT&BOM)
-Add C718(15PF_0402) . (Modify CKT&BOM)
- 74. Modify H_PROCHOT# connection and add EC_PROCHOT# pin for Throttling function control by EC . <Page 5,18,33>93.04.19.
-Add R21 (62ohm_0402)(Because SB Int. PH disconnection) . (Modify CKT&BOM)
-Remove R378(0_0402) ; Add R578(0_0402) to connect CPU and EC CTRL(U12.92) . (Modify CKT,BOM&Layout)
- 75. Correct H_FERR# have double Pull High problem . <Page 18> 93.04.19.
-Del RP87.6(H_FERR# connection) . (Modify CKT&Layout)
- 76. Modify IEEE1394 related schematic for the Vendor VIA recommend . <Page 24> 93.04.19.
-Add R576(0ohm_0805) . (Modify CKT,BOM&Layout)
-Add C735,C736,C737,C738(0.1UF_0402) . (Modify CKT,BOM&Layout)
-Remove R544(1Kohm_0402) . (Modify CKT&BOM)
-Connect R550.2,R551.2,R552.1&C712.1 . (Modify CKT&Layout)
- 77. Disconnect JP8.36(WLAN_PME#) for normal design . <Page 26> 93.04.19.
-Reserve R579(@0ohm_0402) . (Modify CKT&Layout)
- 78. Change VBCAD's Pull-High Power Source from +3VS to +1.8VS for the vendor SIS recommend . <Page 16> 93.04.19.
-Change R384.1's connection from +3VS to +1.8VS . (Modify CKT&Layout)
- 79. Modify JP32 power source pins connection for new CardReader Board cost down and SB chip power issue fixed option . <Page 29> 93.04.19.
-Change JP32.1/2/7/8 from +5VS only to+5VS(JOPEN3)/+3VALW(JOPEN4) option . (Modify CKT,BOM&Layout)
- 80. Disconnect MDC Connector JP14.29 for power consumption save . <Page 29> 93.04.19.
-Reserve R575(@0_0402) between JP14.29 and GND . (Modify CKT&Layout)
- 81. Modify LPC_RST# and NB_RST# related resistor value to fix signal quality issue . <Page 20> 93.03.18.
-Change R346(0ohm_0402->10ohm_0402) ; Add R571(10ohm_0402) . (Modify CKT,BOM&Layout)

DFY30 from PV-Step to Pre MV-Step LA-2251 REV:0.3 -> 1.0 Modify <93.04.19.~93.05.27. >

- 82. Modify Audio AMP LIN/RIN CAPS' value to improve audio noise issue . <Page 28> 93.04.29.
-Change C283,C284 from 0.47UF_0603 to 22PF_0603 . (Modify CKT&BOM)
- 83. Modify Audio AMP FADE# pin define to improve audio noise issue . <Page 28> 93.04.29.
-Change U9.16(FADE#)'s connection from AGND to +5VAMP by 10Kohm resistor(R580_0402) . (Modify CKT,BOM&Layout)
- 84. Change EC_SMD_2/EC_SMC_2's pull high power source from +3VALW to +5VALW because ENE_KB910 SMBUS1/2 use the same power level . <Page 33> 93.05.05.
-Change RP31.7/RP31.8 from +3VALW to +5VALW . (Modify CKT&Layout)
- 85. Modify SI102221K05 to SI102221K10 for material shortage issue . <Page 31> 93.05.13.
-Change CP7,CP8,CP9 from SI102221K05 to SI102221K10 . (Modify CKT&BOM)

----PLEASE SEE NEXT PAGE

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.		
H/W2 EE Dept. PIR SHEET(2)		
Title	Document Number	Rev
	LA-2251	1.0
Date	Monday, May 17, 2004	Sheet 47 of 47