Project name: Bandera(EAX00)

PCB Serial Number: LA-2581

Bandera Schematics Document

Intel Dothan ULV1.1G/1.2G (Celeron-M ULV1.1G/1.2G) +Alviso GMS+ICH6-M

2005-06-17

REV: X5.0

Compal Electronics, Inc.(KunShan)

Title: Cover Sheet

Size: Custom | Document Number: *Bandera-EAX00-LA2581* | Rev: X5.0

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Power Sequence
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uFCBGA CPU
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Processor Thermal sensor ADM1032
page 5

Panel Thermal sensor TC74A1-5.0VCT
page 14

VCCP&CPU_CORE
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P.I.R List
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DDR2 Thermal sensor ADM1032
page 5

HDD Thermal sensor conn TC74A1-5.0VCT
page 20

HA#(3..31)
System Bus
400MHz
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Clock Generator
IDT CV140
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ALS

AU 8.4" SVGA TFT LCD Module
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LVDS

Intel Alviso GMS
FC-BGA840
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Memory BUS (DDR2)
Channel A 1.8V 400MHz

SO-DIMM X 1
BANK 0 page 12

CRT CONN
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DMI X2
1.5V
100MHz

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USBPORT 1 — JUSBP1 page 27
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PCI Express x2

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USB 2.0
48MHz / 480Mb

AC-LINK
3.3V 24.576MHz

3.3V 33MHz
PCI BUS

ATA100
IDE Bus

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page 20

AC97 CODEC
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page 25

AMP & Phone MIC
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SD Controller
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LPC BUS
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Ambient Light Sensor

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ROM DAUGHTER/BOARD
MXLV008BTC
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Digitizer

FIR

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Title: Block diagram

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External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
RTL8101L	AD17	3	F,B
Mini-PCI	AD18	1	G,H
W83L528D	AD20	2	A

ICH6M SM Bus Address

DEVICE	Address
Clock Generator	1101 001Xb
DDR2 DIMM0	1010 001Xb
DOCK NEW CARD	TBDXb

EC SM Bus1 Address

DEVICE	Address
Smart Battery 1	0001 011Xb
ALS TSL2550T	0111 0010b
CPU ADM1032	1001 100Xb
HDD TC74A1-5.0VCT	1001 0010b

EC SM Bus 2 Address

DEVICE	Address
DDR2 ADM1032	1001 100Xb
Panel TC74A1-5.0VCT	1001 0010b

Signal / State	+12VALW +5VALW +3VALW +1.5VALW	+3V +1.8V	+3VS +5VS +1.5VS +0.9VS +2.5VS +VCCP +CPU_CORE
FULL ON	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Power Management table

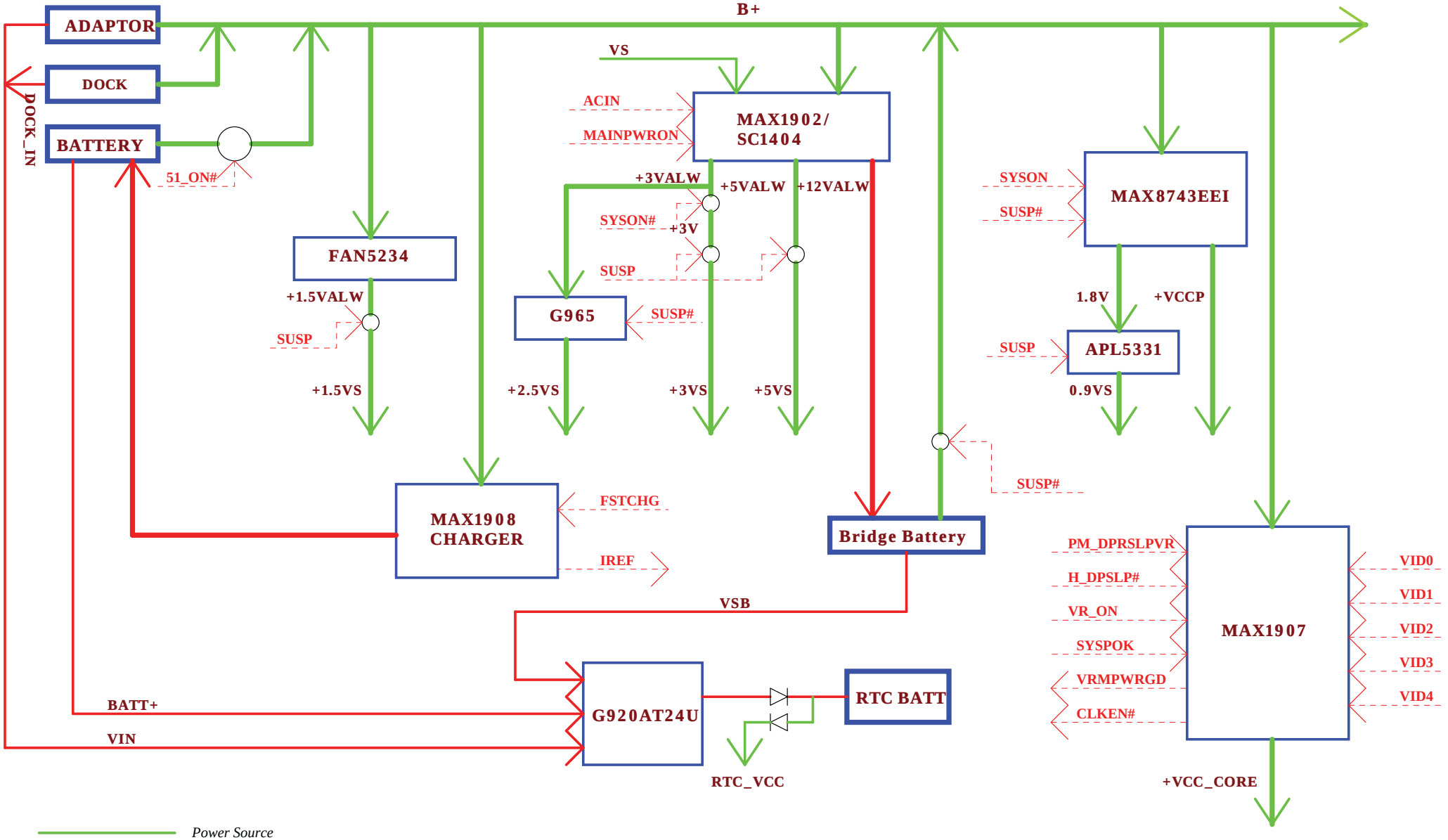
Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

PORT	FUNCTION
PORT 0	MB port
PORT 1	MB port
PORT 2	FPR
PORT 3	BT
PORT 4	Docking
PORT 5	reserved
PORT 6	Docking
PORT 7	Docking

USB PORT TABLE



Compal Electronics, Inc.(KunShan)
Title: Power rail
Size: Custom
Document Number: Bandera-EAX00-LA2581
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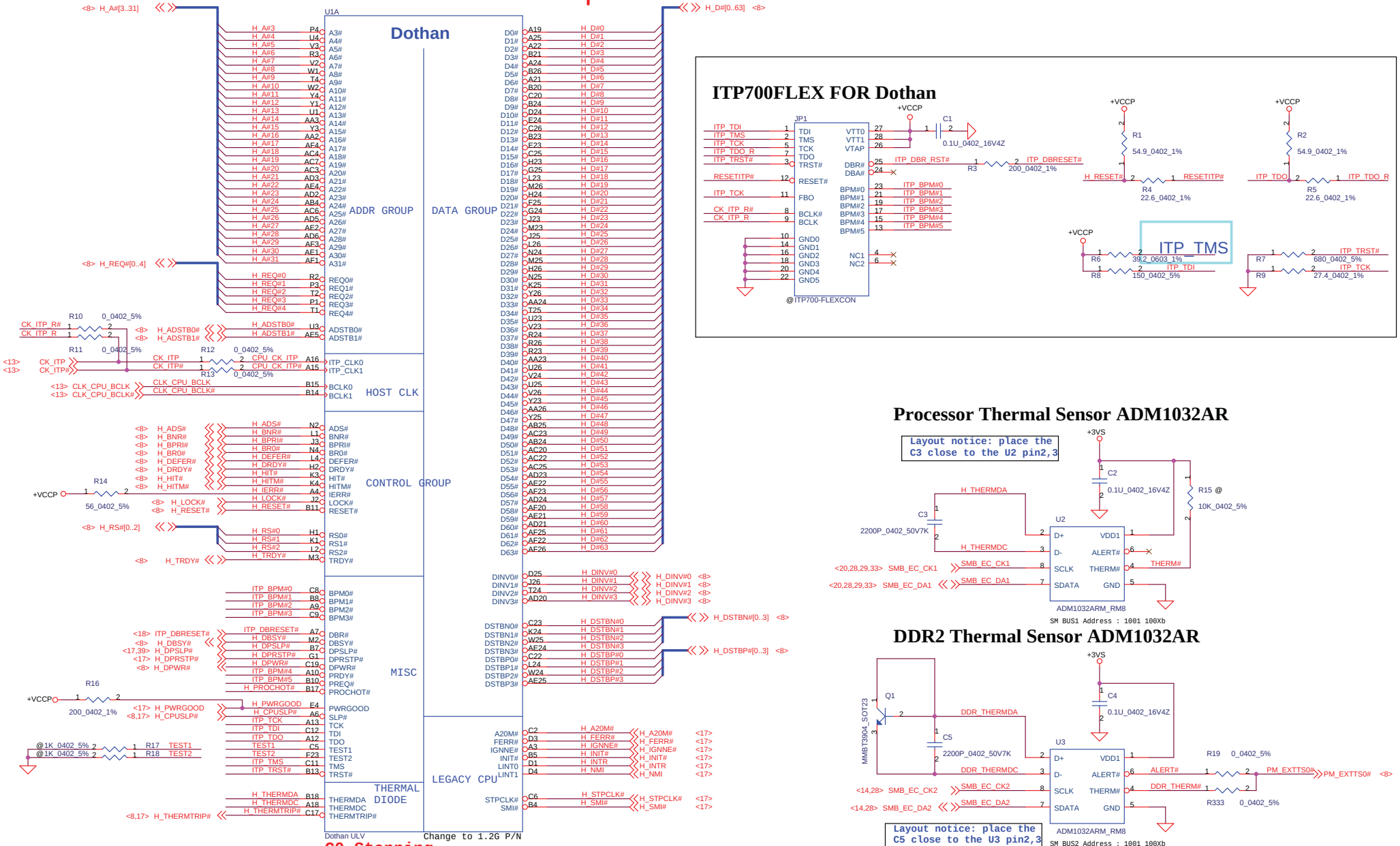
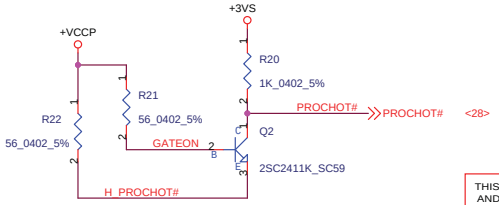


C0 Stepping



ITP700FLEX FOR Dothan

Processor Thermal Sensor ADM1032AR

Layout notice: place the C3 close to the U2 pin2,3

DDR2 Thermal Sensor ADM1032AR

Layout notice: place the C5 close to the U3 pin2,3

Compal Electronics, Inc.(KunShan)
Title: Dothan host interface
Size: Custom
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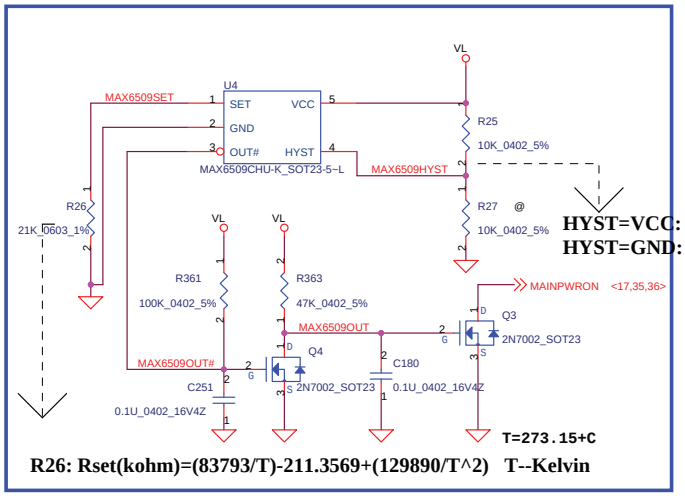
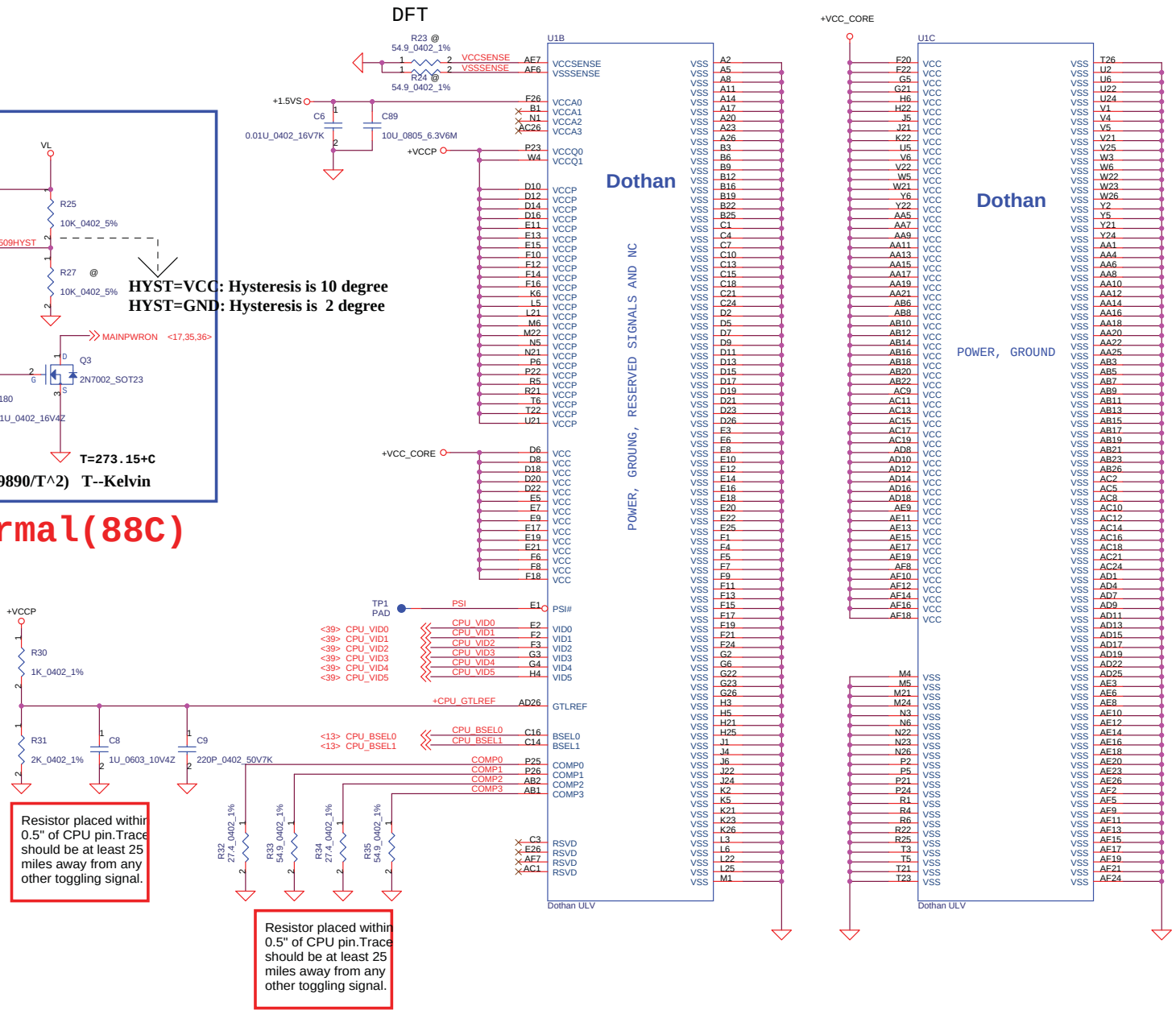
DFT



Check with thermal(88C)



Compal Electronics, Inc.(KunShan)
Title: Dothan power and ground
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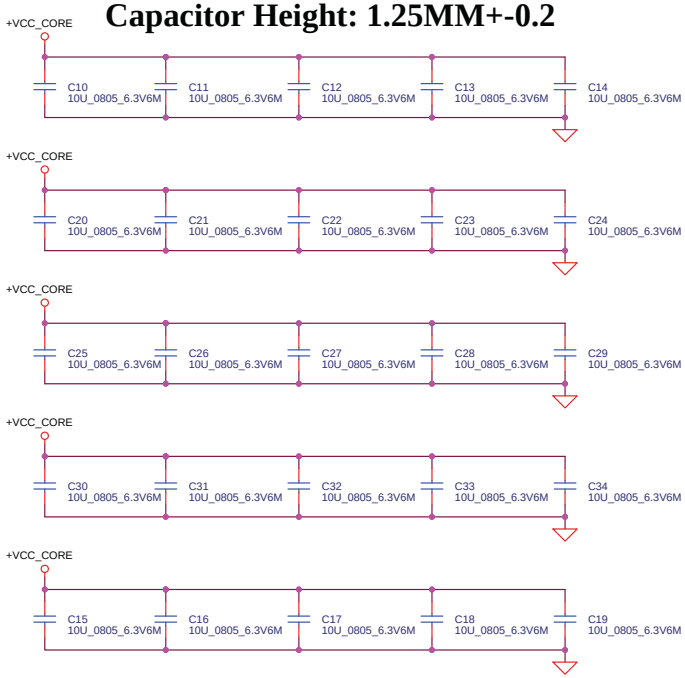
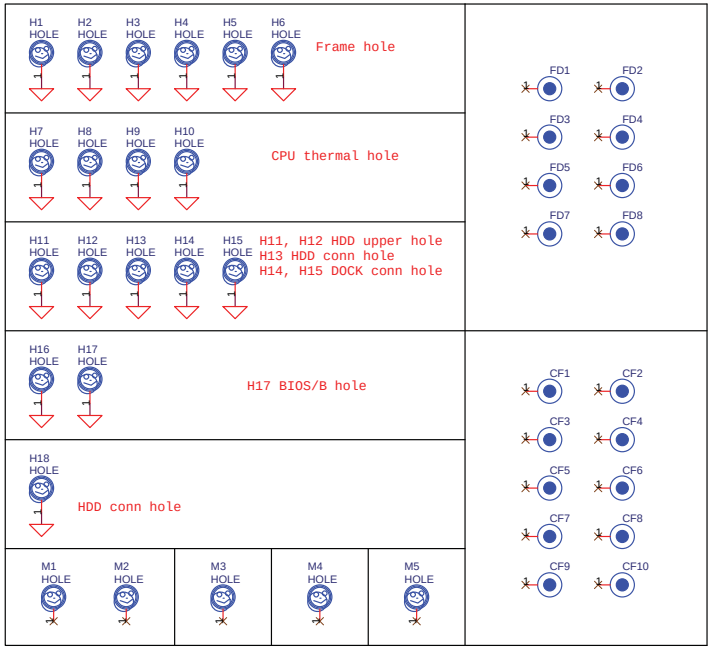
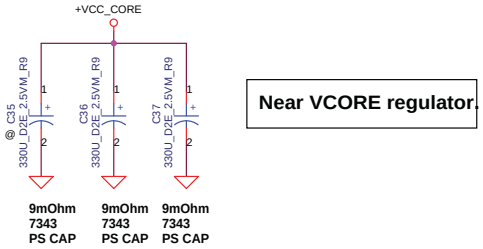
Intel:Mid-Frequency Decoupling (0805 MLCC>= X5R) 5m ohm (typ) /25, 0.6 nH / 25.

Capacitor Height: 1.25MM+-0.2



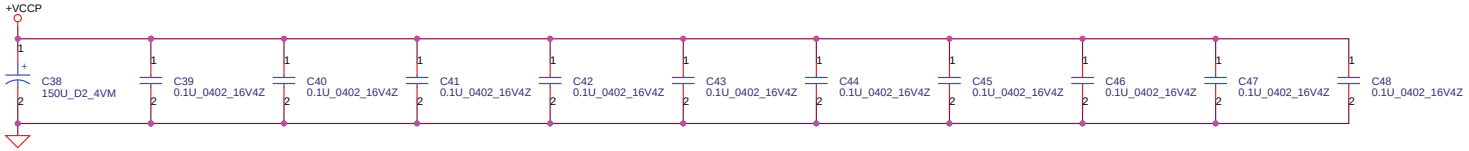


Intel: Low-Frequency Decoupling : 9 m ohm (max)/3, 1.8 nH / 3



Near VCORE regulator.

Intel: High Frequency Decoupling (0603 MLCC, >= X7R) 16 m ohm (typ) / 10, 0.6 nH / 10



Compal Electronics, Inc.(KunShan)
Title: Dothan decoupling cap
Size: Custom
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Rev: X5.0
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CFG[2:0]	101(400MHz FSB)
CFG5	Low = DMI x 2 * High = DMI x 4
CFG6	Low = DDR-II * High = DDR-I

U5A — Alviso — HOST — ALVISO_BGA840

Change to C0 version

Layout Note: Route as short as possible

10/20 Mil width/space , Length1.5''

U5B — DMI / DDR MUXING / CFG/RSVD / PM / CLK — ALVISO_BGA840

Close Alviso

R56 0_0402_5%
<5,17> H_CPUSLP# → H_CPUSLP# — H_R_CPUSLP#

Reserved this Resistor for CPU sleep drive by Alviso or ICH6, This resistor can be delete after intel ensure don't change this Enhance C3 function

Compal Electronics, Inc.(KunShan)
Title: Alviso GMS host/DMI/DDR/PM/CLK
Size: Custom
Document Number: Bandera-EAX00-LA2581
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Intel demand in Soloma Platform design guide P428

+2.5VS

R57

10K_0402_5%

U5C

ALVISO_BGA840

U5F

ALVISO_BGA840

U5G

ALVISO_BGA840

VSS

VSSALVDS

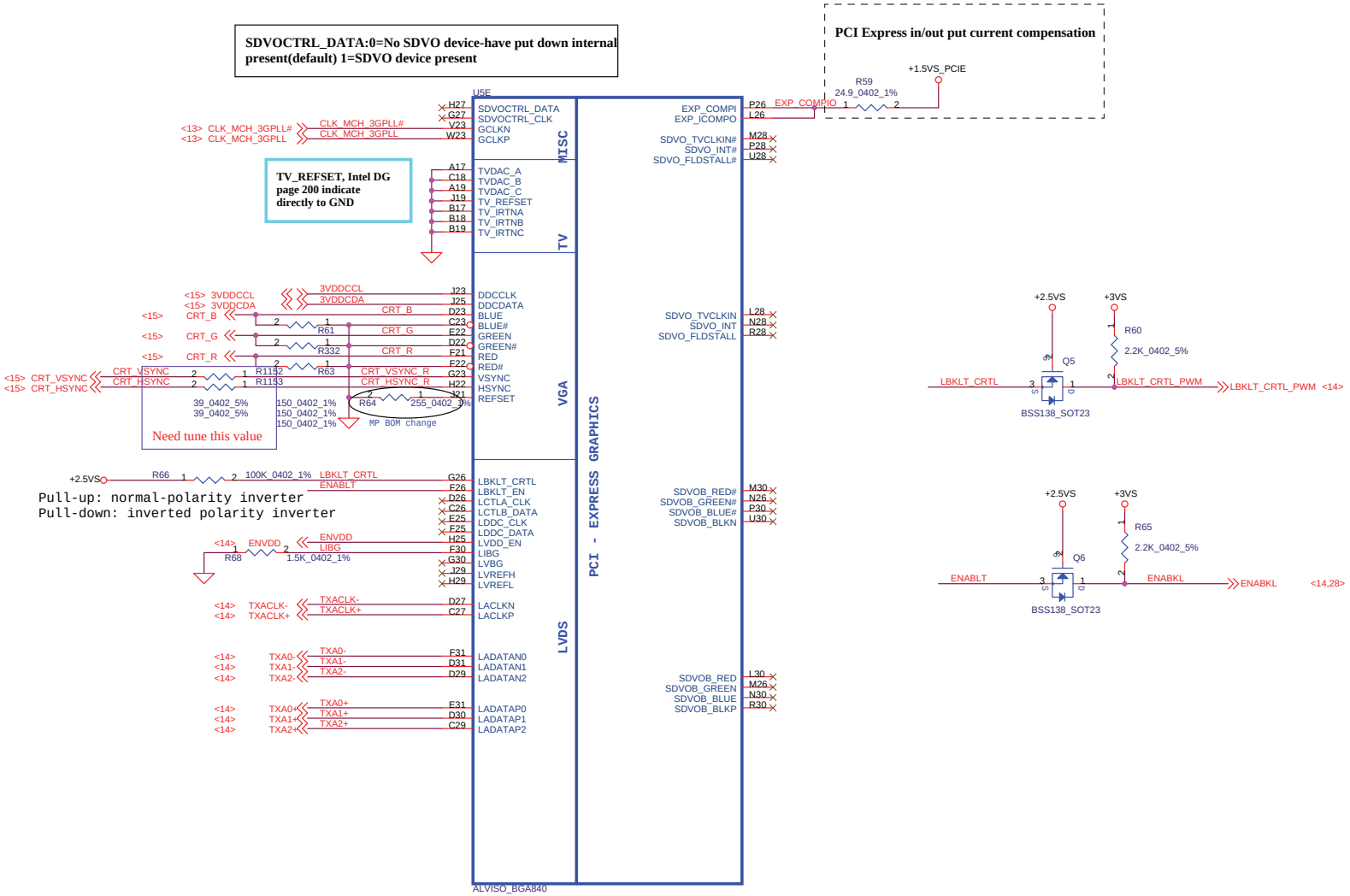
Use for emulating source synchronous clocking for reads. these signal are routed internally on the GMCH package and can be NC.

Compal Electronics, Inc.(KunShan)

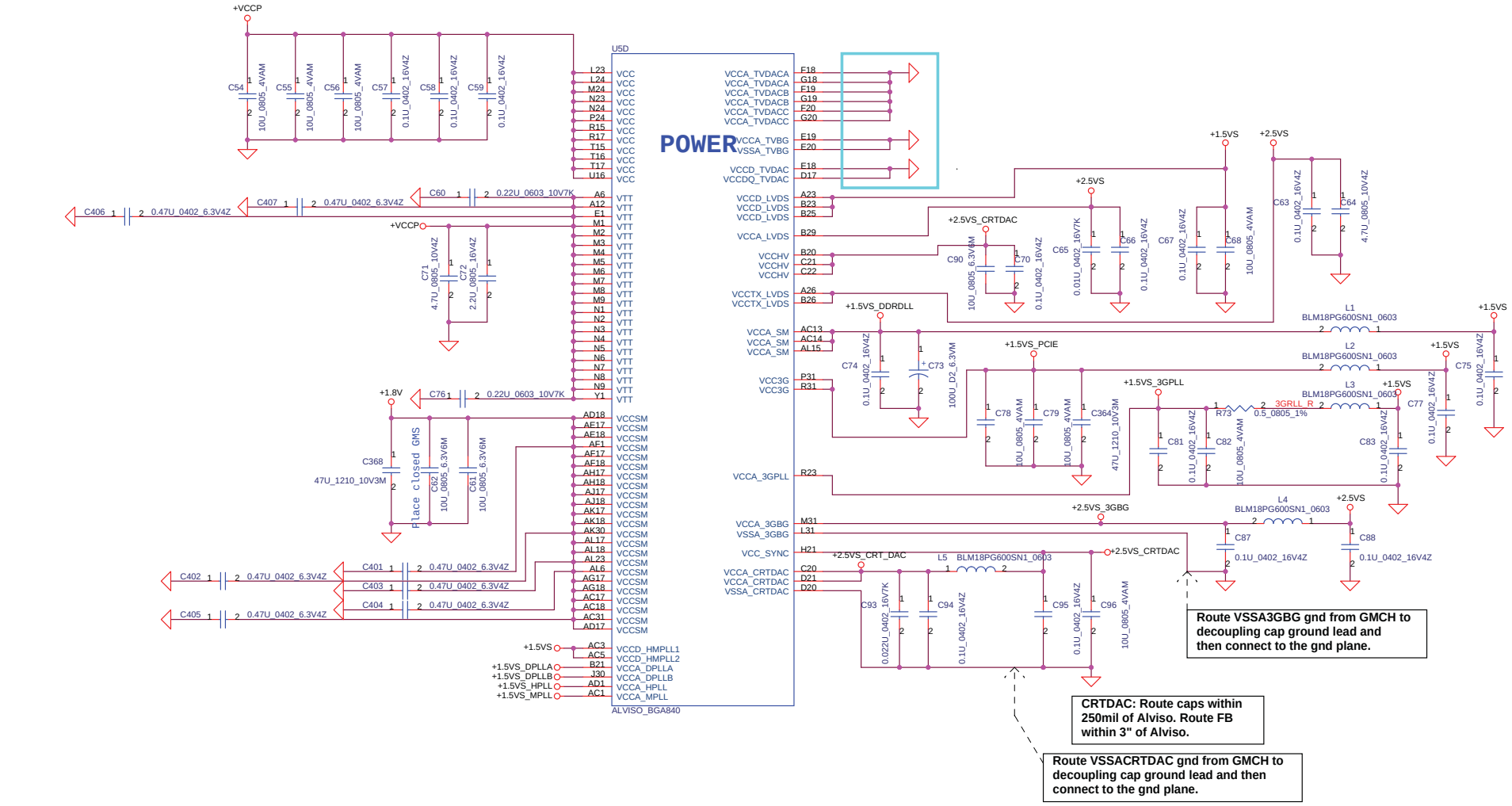
Title: Alviso GMS DDR2/VSS

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

Date: Friday, June 17, 2005 | Sheet 9 of 48



Compal Electronics, Inc.(KunShan)	
Title	Alviso GMS Display interface
Size: Custom	Document Number: Bandera-EAX00-LA2581
Rev	X5.0
Date: Friday, June 17, 2005	Sheet 10 of 48

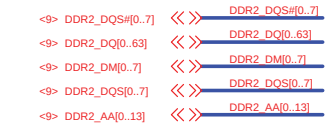


Compal Electronics, Inc.(KunShan)

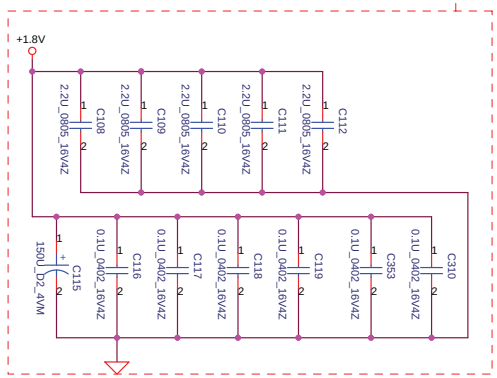
Title: Alviso GMS power interface

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

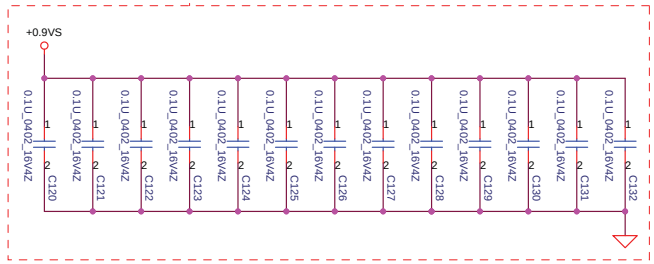
Date: Friday, June 17, 2005 | Sheet 11 of 48

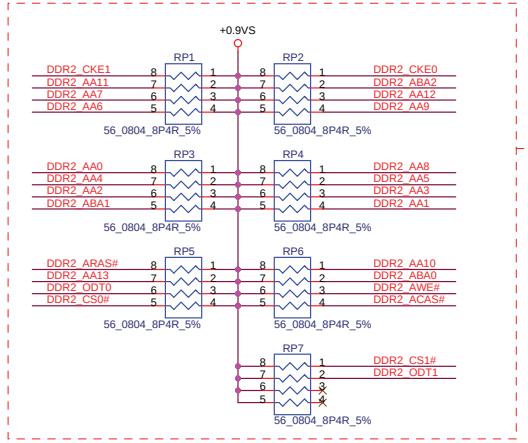


Layout Note:
Place near JP2



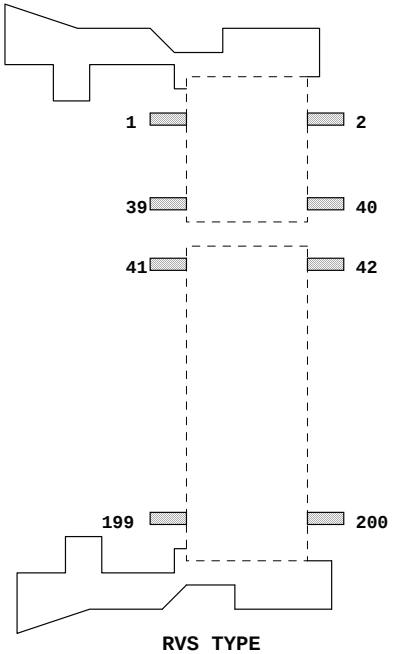
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



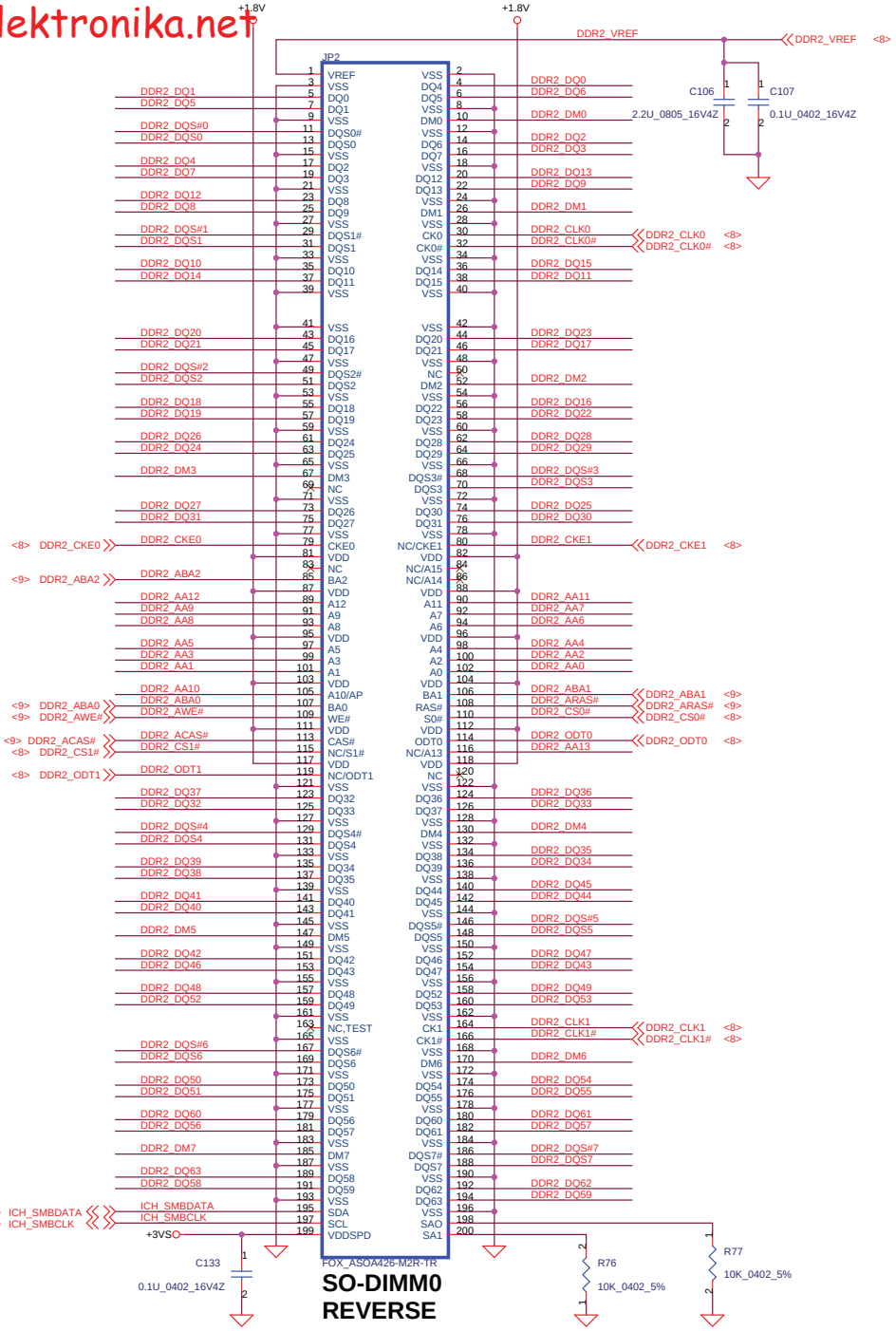


Layout Note:
Place these resistor closely JP2,all trace length<750 mil

Top view



RVS TYPE



Compal Electronics, Inc.(KunShan)	
Title	DDR2-SODIMM0
Size: Custom	Document Number: Bandera-EAX00-LA2581
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Date: Friday, June 17, 2005	Sheet 12 of 48

CLKSEL0	CLKSEL1	+3VS	BCLK
FS_C	FS_B	FS_A	100X4=400
1	0	1	

Signal / Model	CLKREQB#	CLKREQA#	SRC4/4# NewCard	SRC5/5# GigaLAN
IDT CV140	✕	0	✓	✓
	✕	1	✕	✕
SLG84443	0	0	✓	✓
	0	1	✓	✕
	1	0	✕	✓
	1	1	✕	✕
Comments	Main source IDT CV140 SRC1~7/1~7# can control by CLKREQA# or CLKREQB#, in MP use CLKREQA# control; 2nd source Silego SLG84443 SRC1,3,4/1#,3#,4# can control by CLKREQB# and SRC2,5/2#,5# can control by CLKREQA#			

Use 12.1ohm+/- 1% series resistor if the clock signal is shared bewteen two devices.

Place crystal within 500 mils of CK410M

SS frequency selection

96*_100MSEL	96_100MSST/C
LOW	96 MHZ
HIGH	100 MHZ

U40 IDTCV140PAG_TSSOP56

Compal Electronics, Inc.(KunShan)

Title: Clock generator-CV140

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

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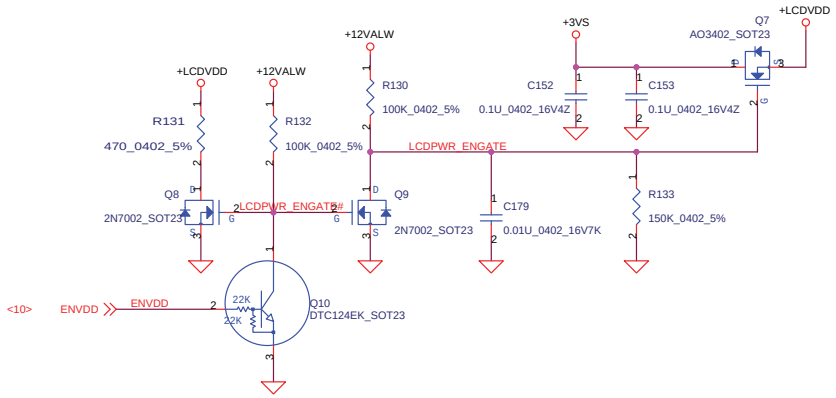
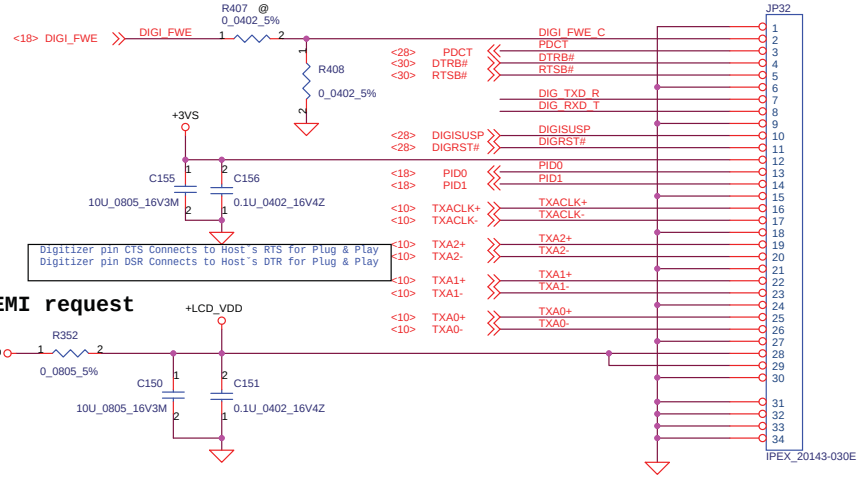
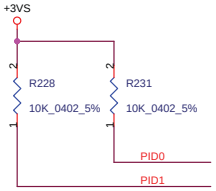
PID1	PID0	Vendor
0	0	AU-B084SN02
0	1	
1	0	
1	1	

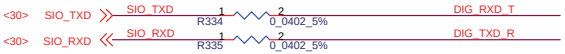




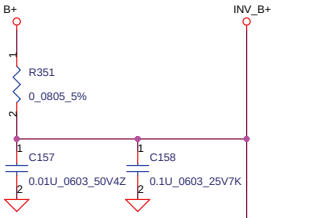
Top view

EMI request

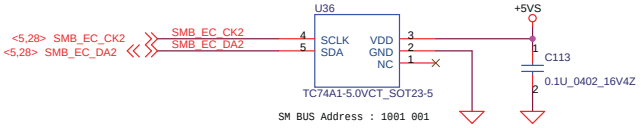




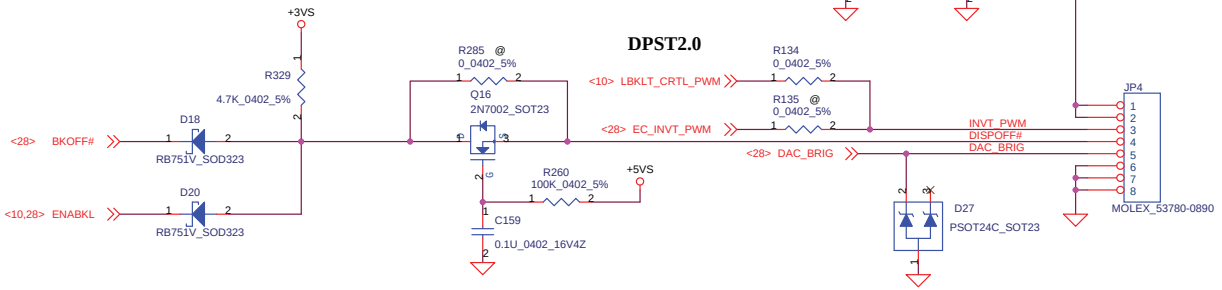
EMI request



LCD/Inverter temperature monitor



DPST2.0



Compal Electronics, Inc.(KunShan)
Title: LCD Conn/Inverter Conn
Size: Custom
Document Number: Bandera-EAX00-LA2581
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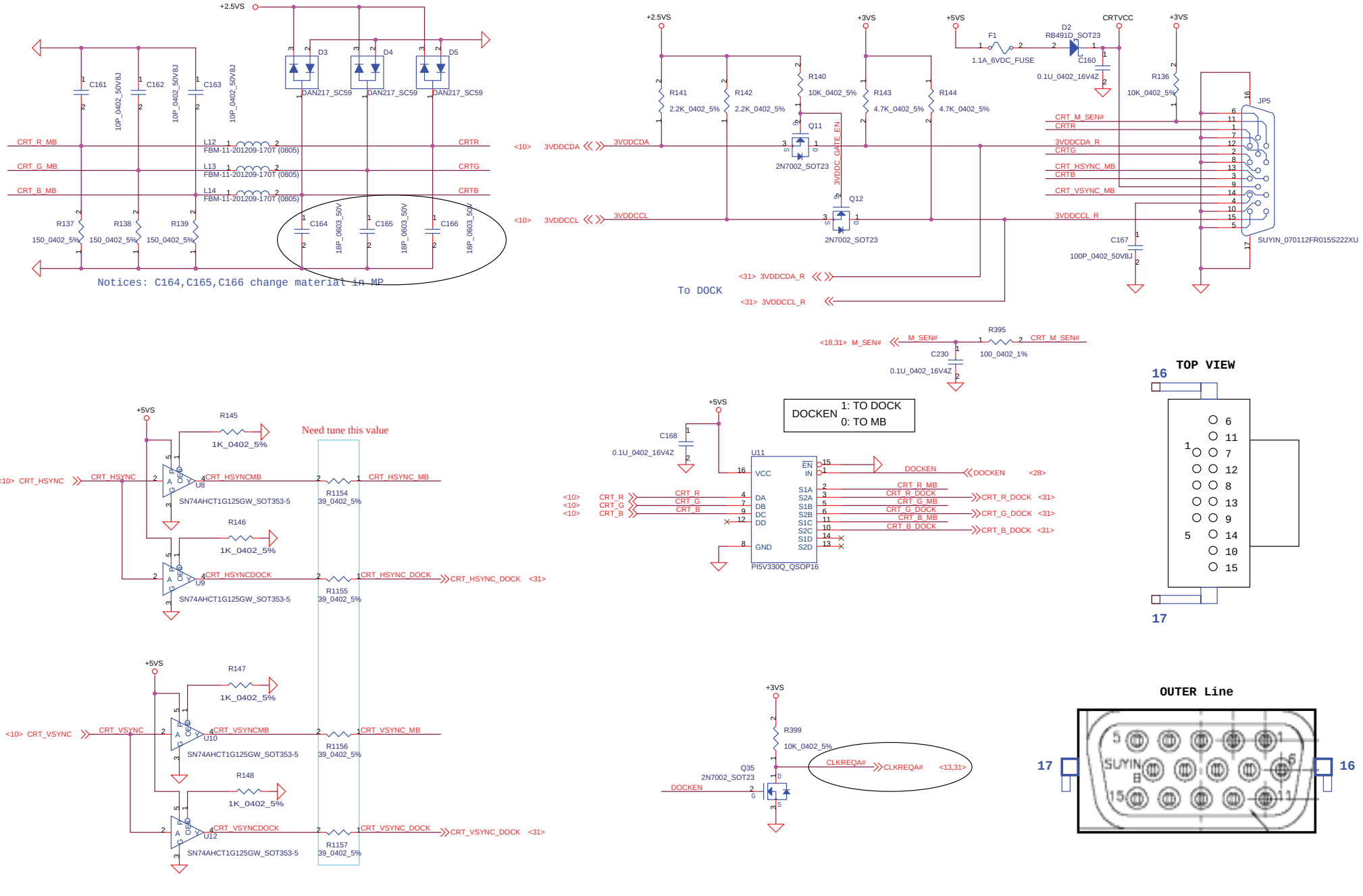

Compal Electronics, Inc.(KunShan)

Title: CRT interface

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

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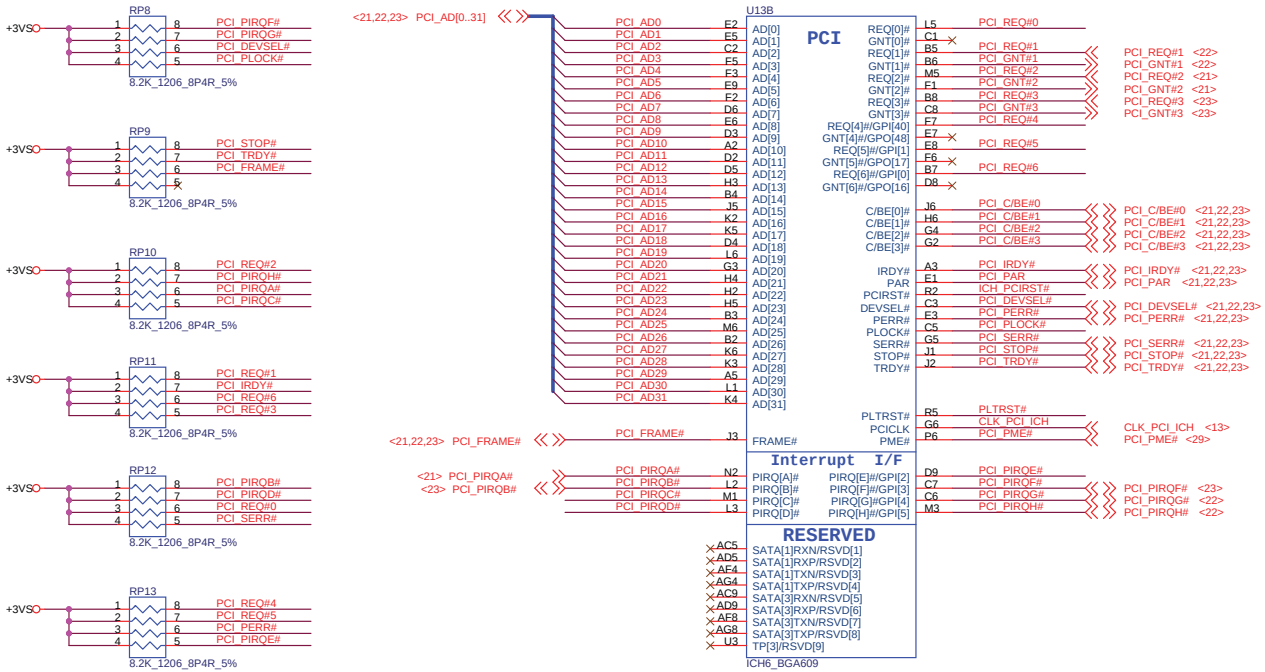
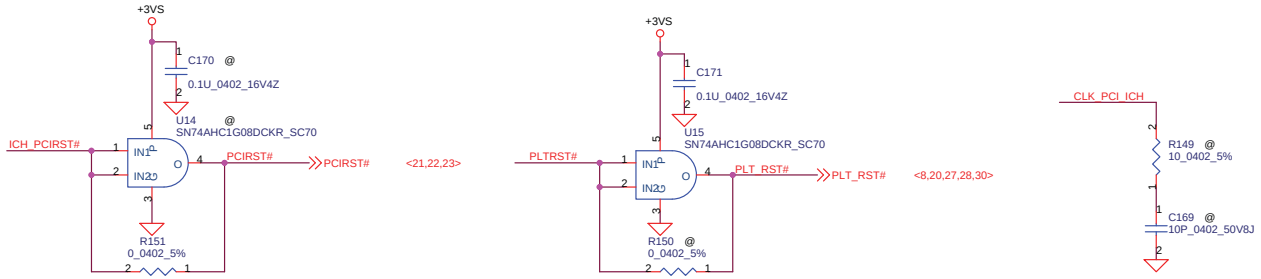


B2 Stepping



Compal Electronics, Inc.(KunShan)
Title: PCI/SATA interface
Size: Custom
Document Number: Bandera-EAX00-LA2581
Rev: X5.0
Date: Friday, June 17, 2005
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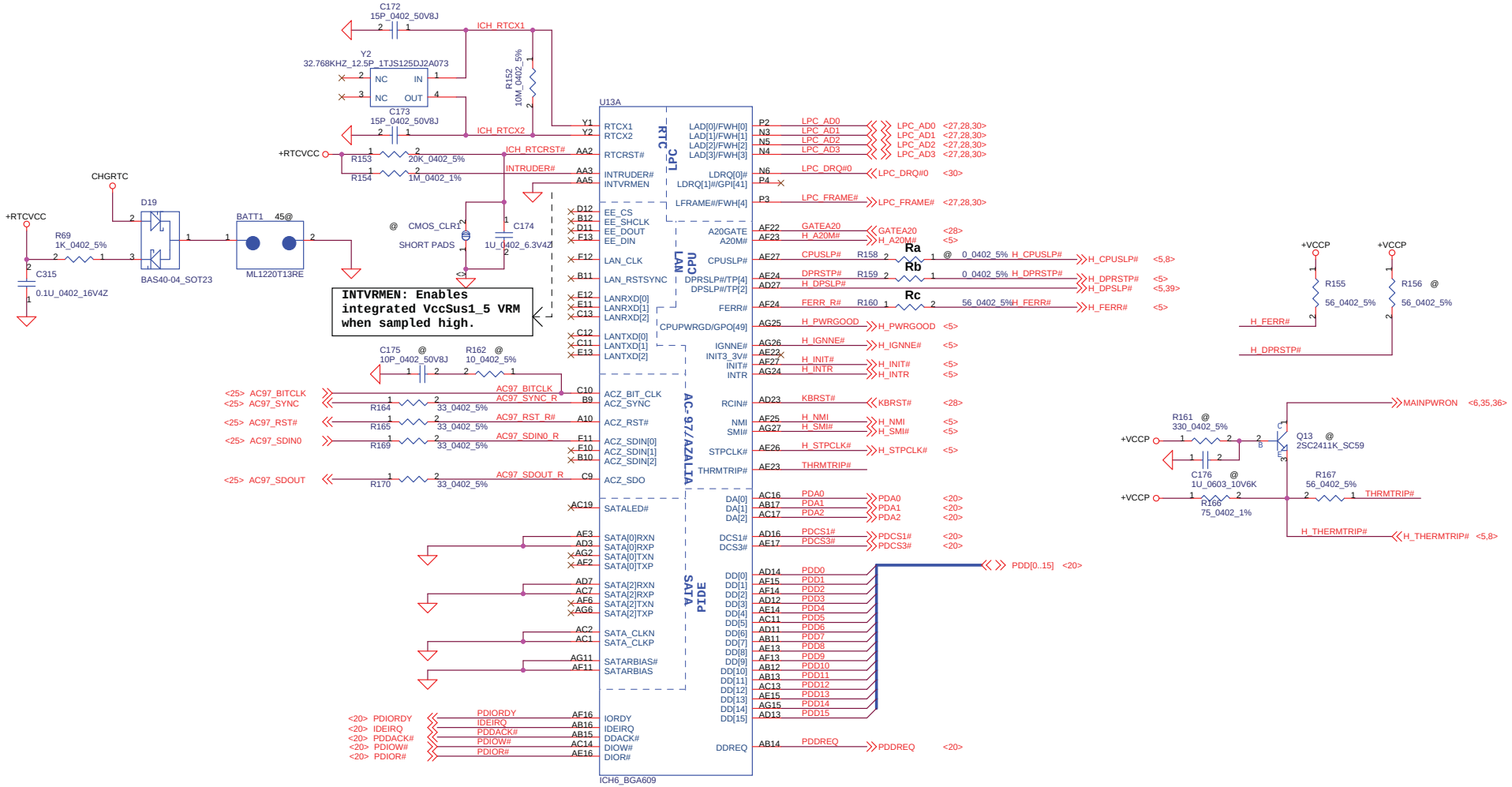

Compal Electronics, Inc.(KunShan)

Title: ICH6-RTC/AC97/SATA/PIDE/CPU Sideband

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

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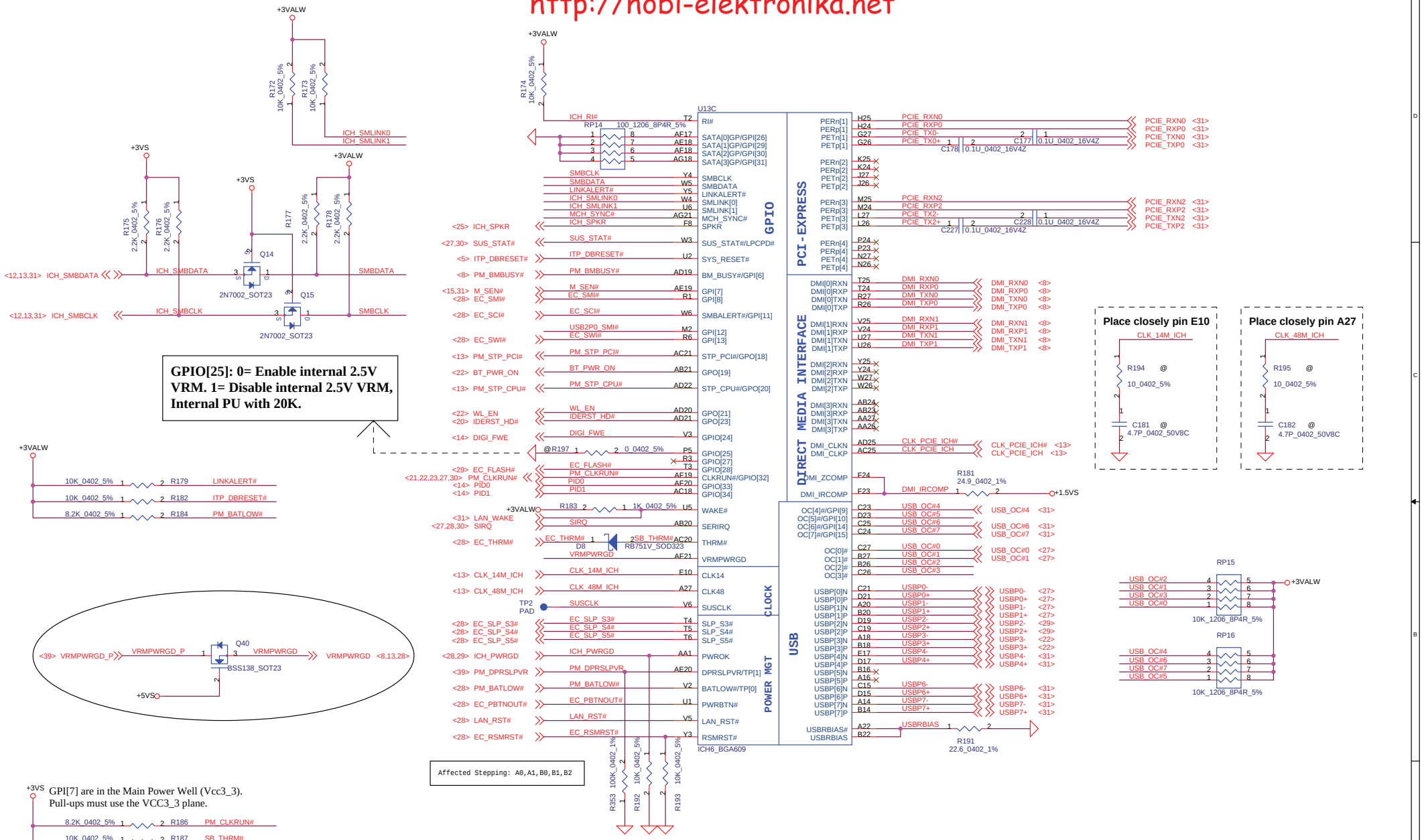
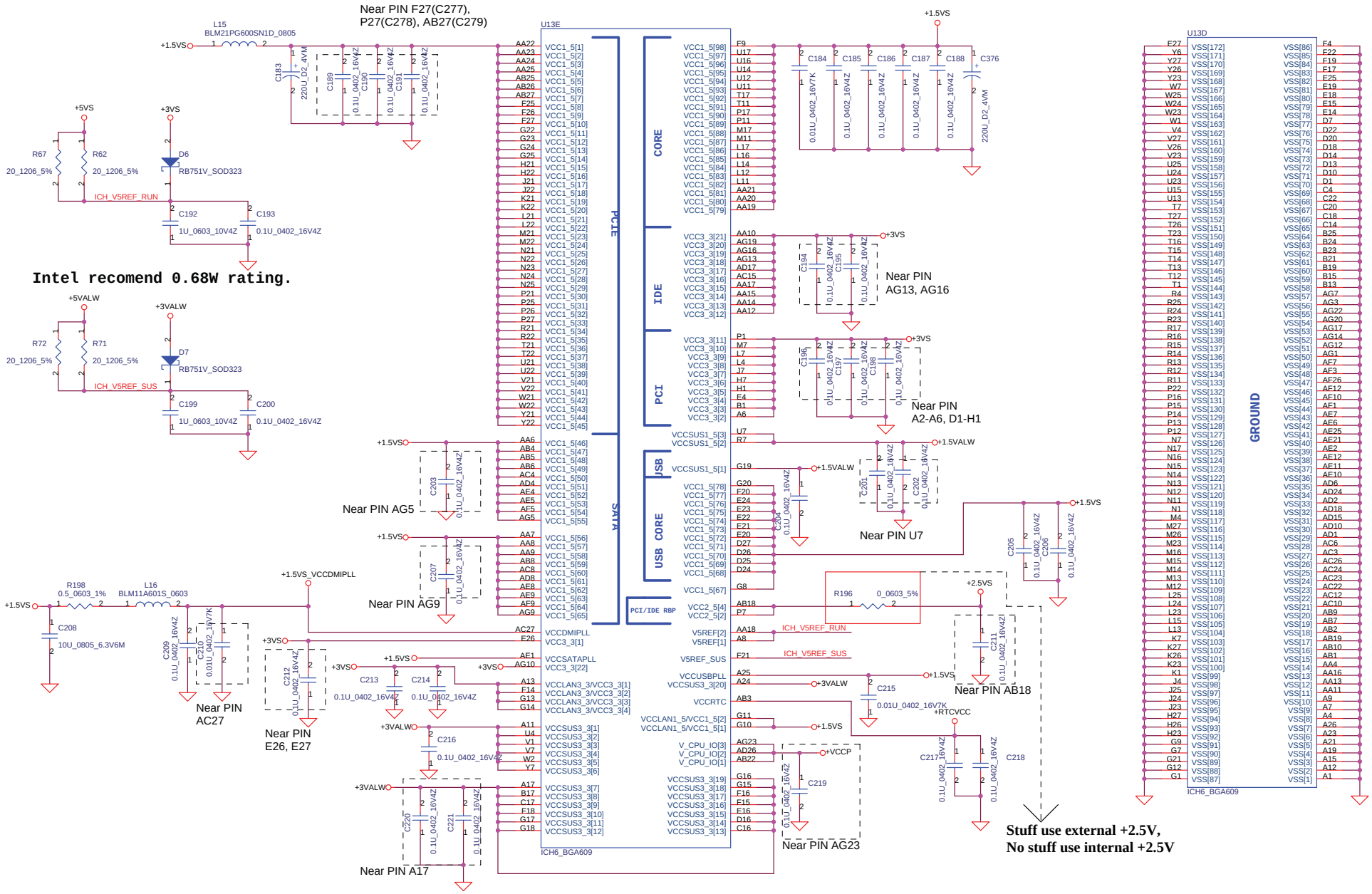
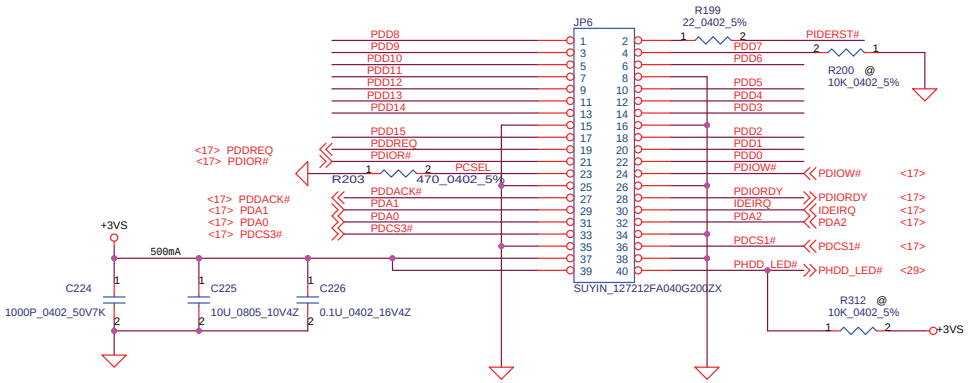
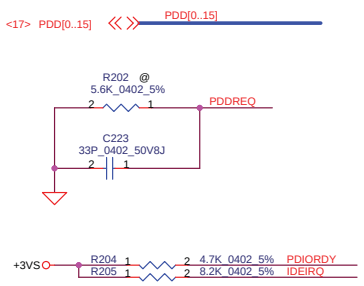


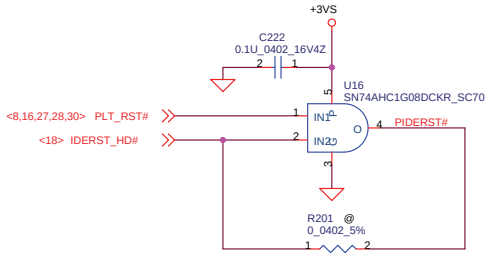
Compal Electronics, Inc.(KunShan)		
Title: ICH6-DMI/PCIE/USB/PM/CLK/GPIO		
Size: Custom	Document Number: Bandera-EAX00-LA2581	Rev: X5.0
Date: Friday, June 17, 2005	Sheet 18 of 48	



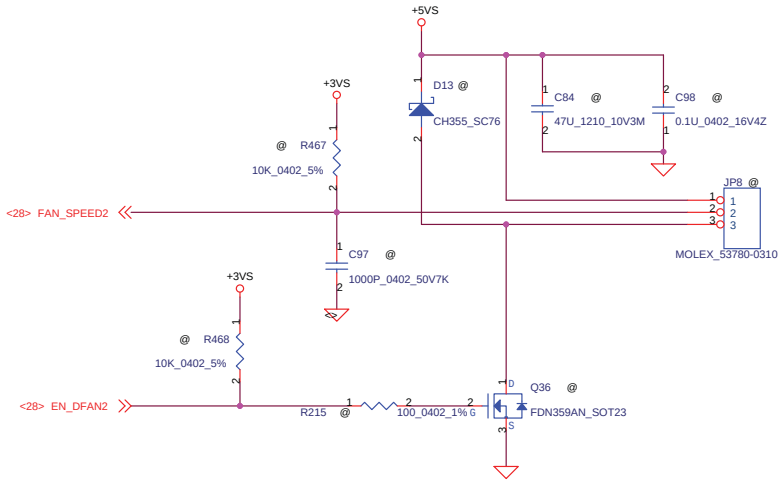
Compal Electronics, Inc.(KunShan)		
Title: ICH6-Power		
Size: Custom	Document Number: Bandera-EAX00-LA2581	Rev: X5.0
Date: Friday, June 17, 2005	Sheet 19 of 48	

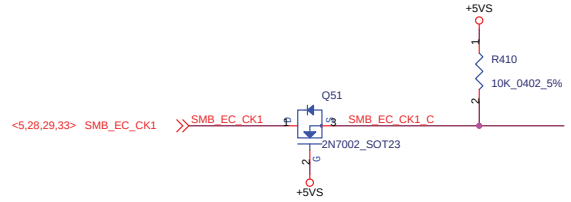


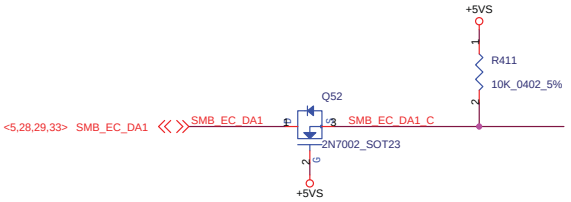


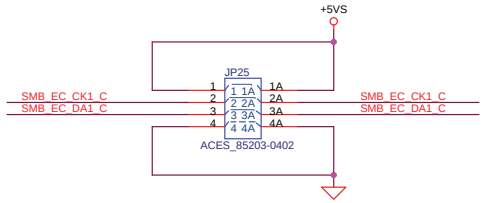


Fan Control Circuit







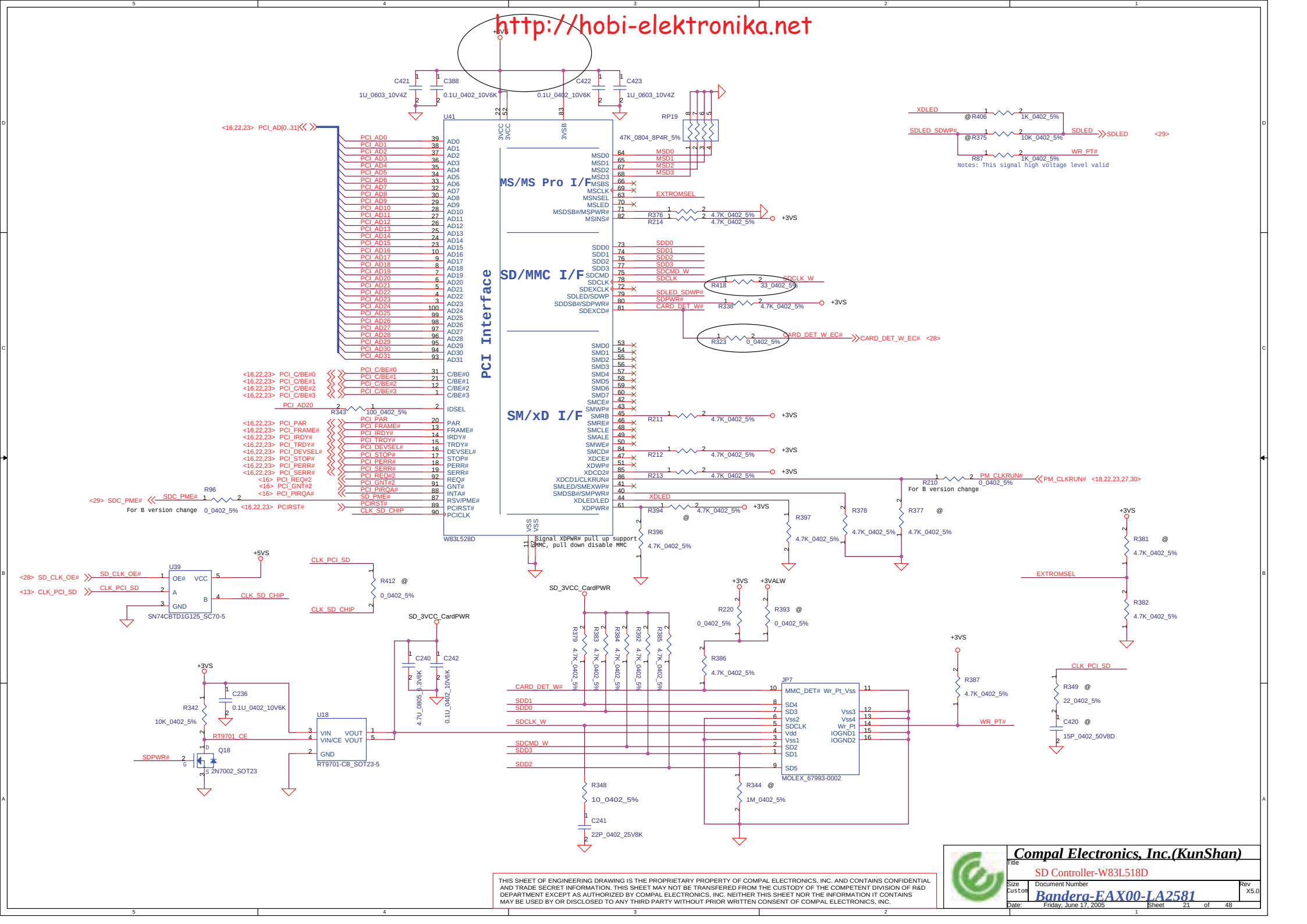


Compal Electronics, Inc.(KunShan)

Title: PIDE/FAN Control Interface

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

Date: Friday, June 17, 2005 | Sheet 20 of 48

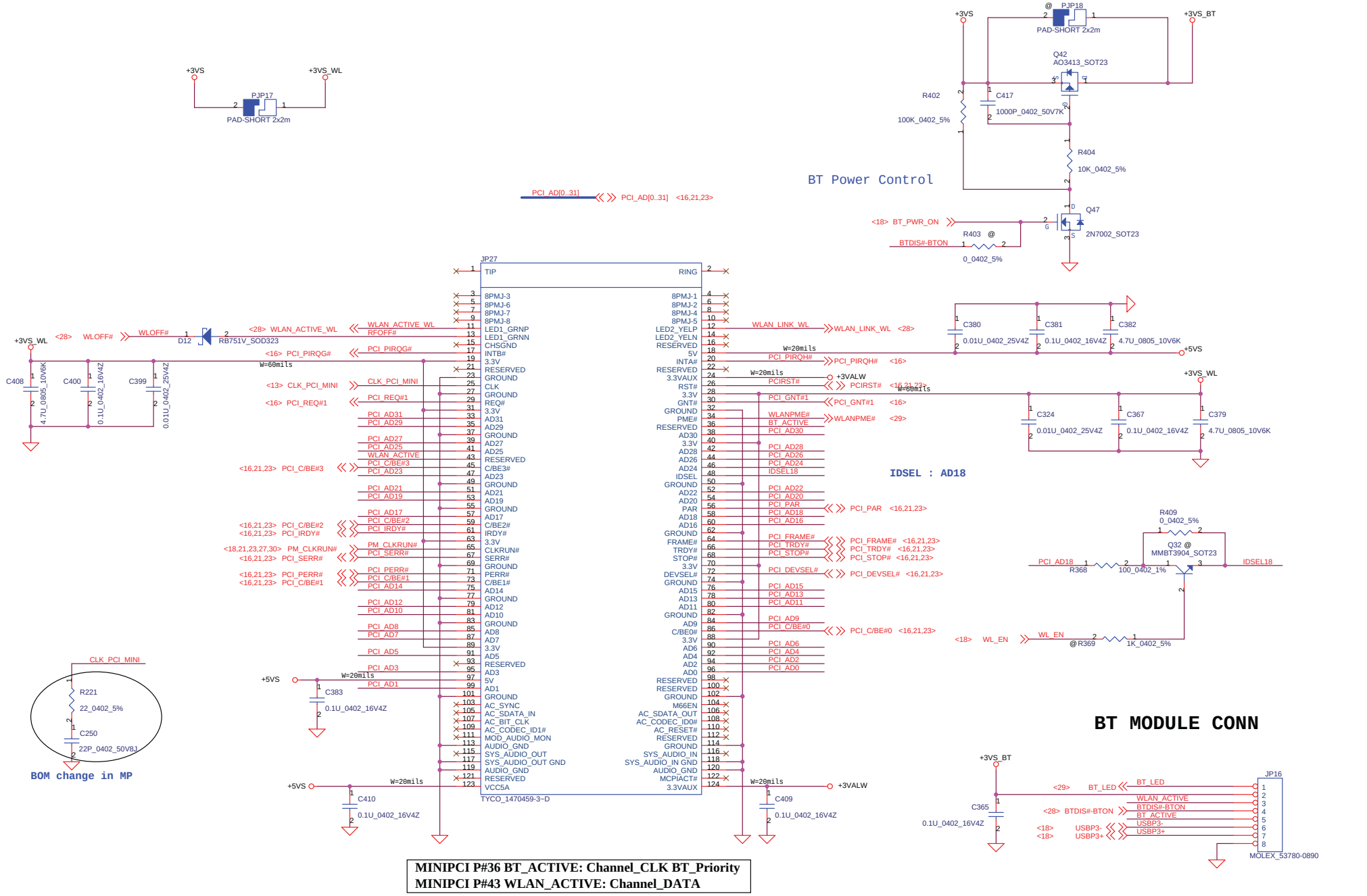


Compal Electronics, Inc.(KunShan)

Title: SD Controller-W83L518D

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

Date: Friday, June 17, 2005 | Sheet 21 of 48



MINIPCI P#36 BT_ACTIVE: Channel_CLK BT_Priority
MINIPCI P#43 WLAN_ACTIVE: Channel_DATA

Compal Electronics, Inc.(KunShan)
Title: MINIPCL Slot/BT
Size: Custom
Document Number: Bandera-EAX00-LA2581
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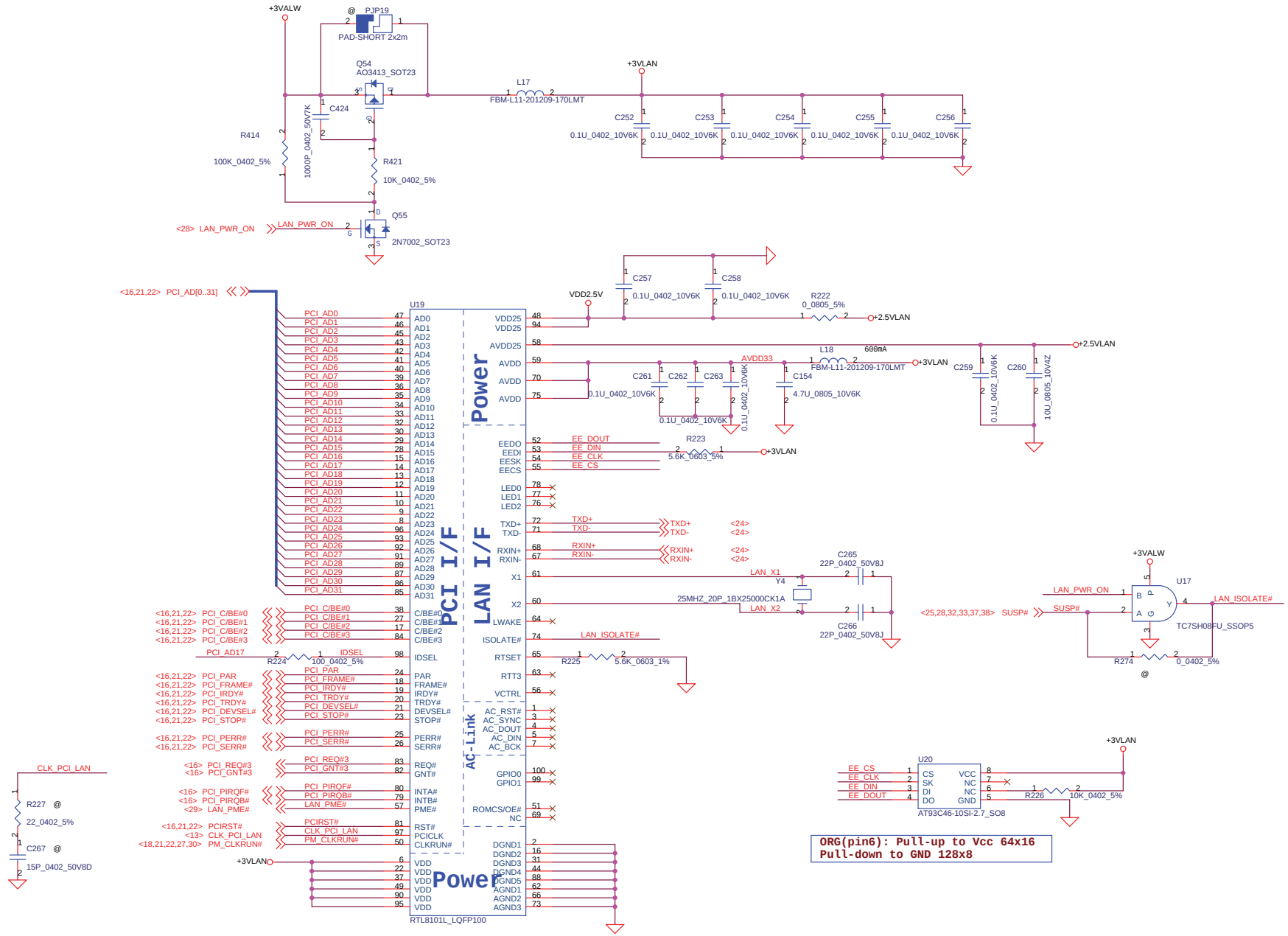
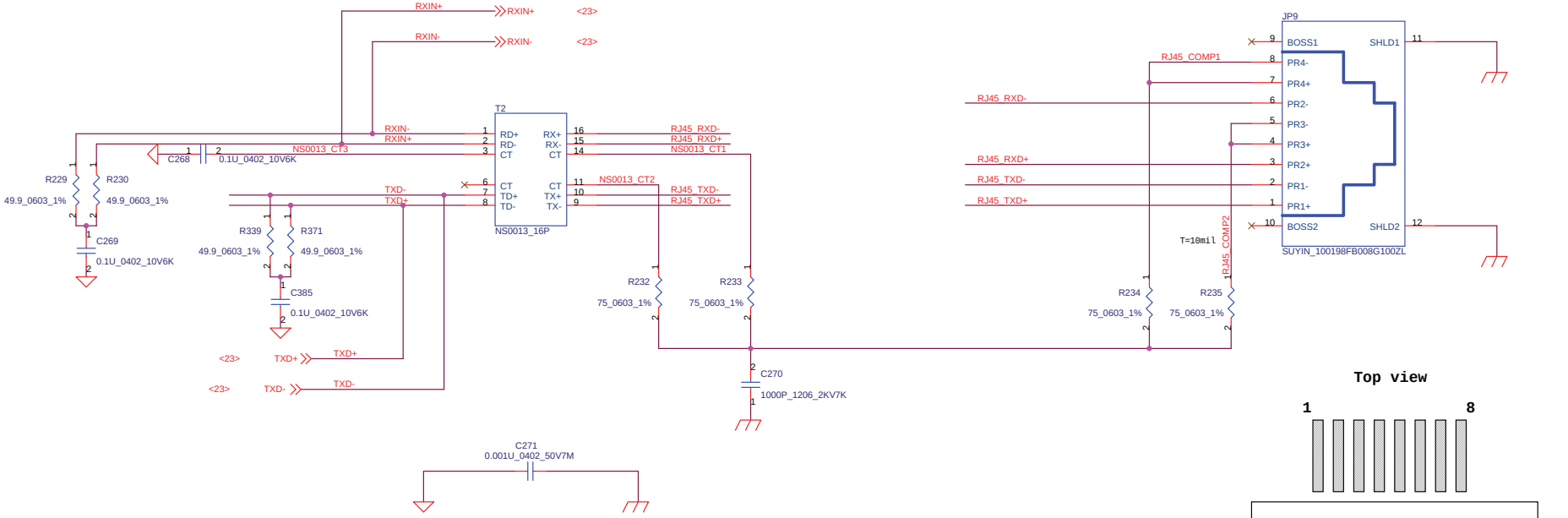


Compal Electronics, Inc.(KunShan)

Title: RTL8101L

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

Date: Friday, June 17, 2005 | Sheet 23 of 48



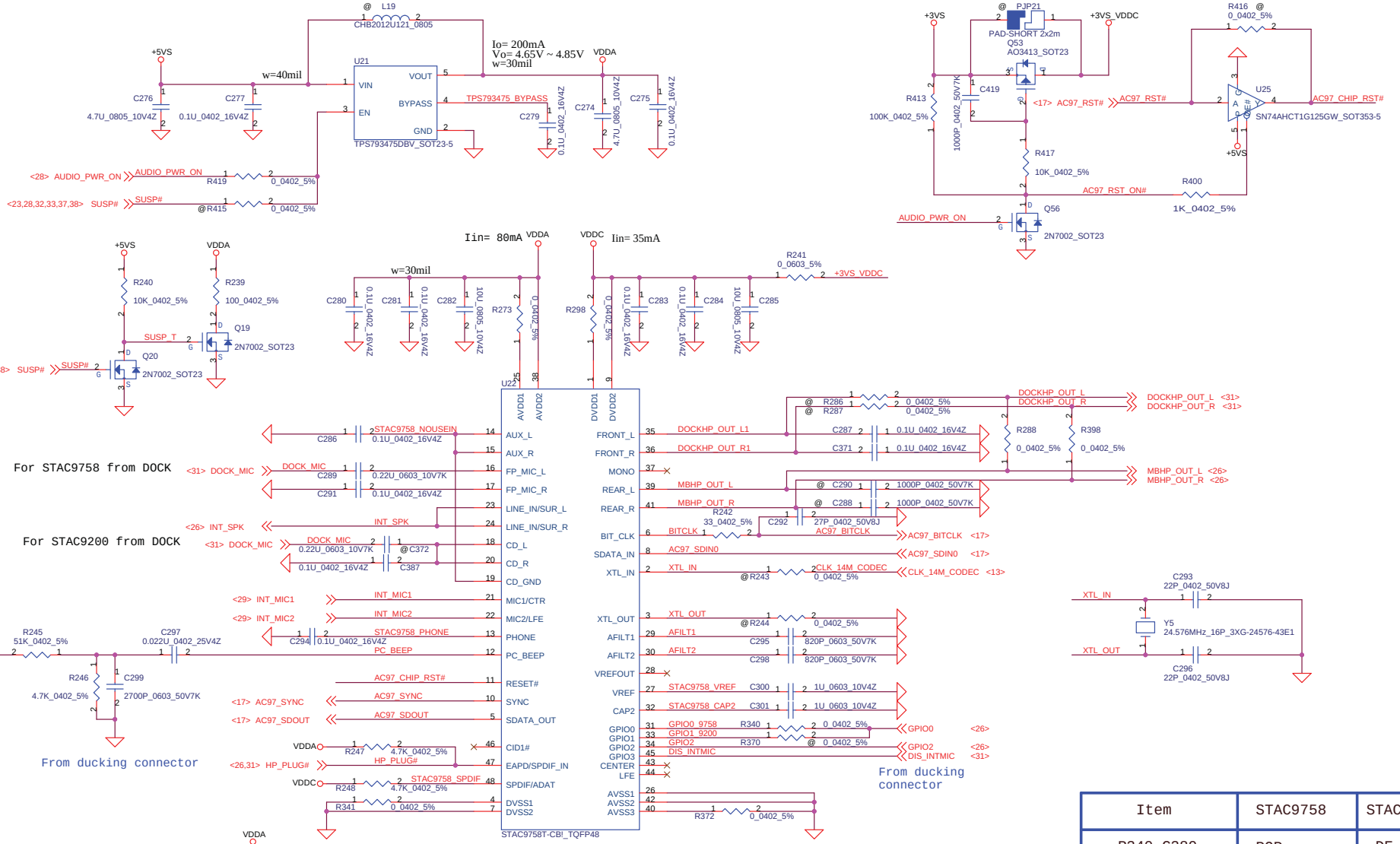
Top view

Compal Electronics, Inc.(KunShan)

Title: Magnetics/RJ45

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

Date: Friday, June 17, 2005 | Sheet 24 of 48



Item	STAC9758	STAC9200
R340,C289	POP	DE_POP
R370,C372	DE_POP	POP
R341,R372	Connect to GND	NC
R273	Connect to VDDA	NC
R298	Connect to VDDC	NC

EAPD PIN47	LINE_IN_L PIN23 LINE_IN_R PIN24
H	ENABLE
L	DISABLE

DIS_INTMIC (PIN 45)	INT_MIC1 INT_MIC2	DOCK_MIC (PIN 16)
H	DISABLE	ENABLE
L	ENABLE	DISABLE

XTL_OUT pin config	CID1 pin config	clock source input	Codec mode	codec ID
xtal	float	24.576MHz xtal	P	0
short to ground	float	14.31818MHz source	P	0
short to ground	pulldown	48MHz source	P	0
XTAL or open	pulldown	12.288MHz bit clk	S	2

Compal Electronics, Inc.(KunShan)
Title: STAC9758T
Size: Custom
Document Number: Bandera-EAX00-LA2581
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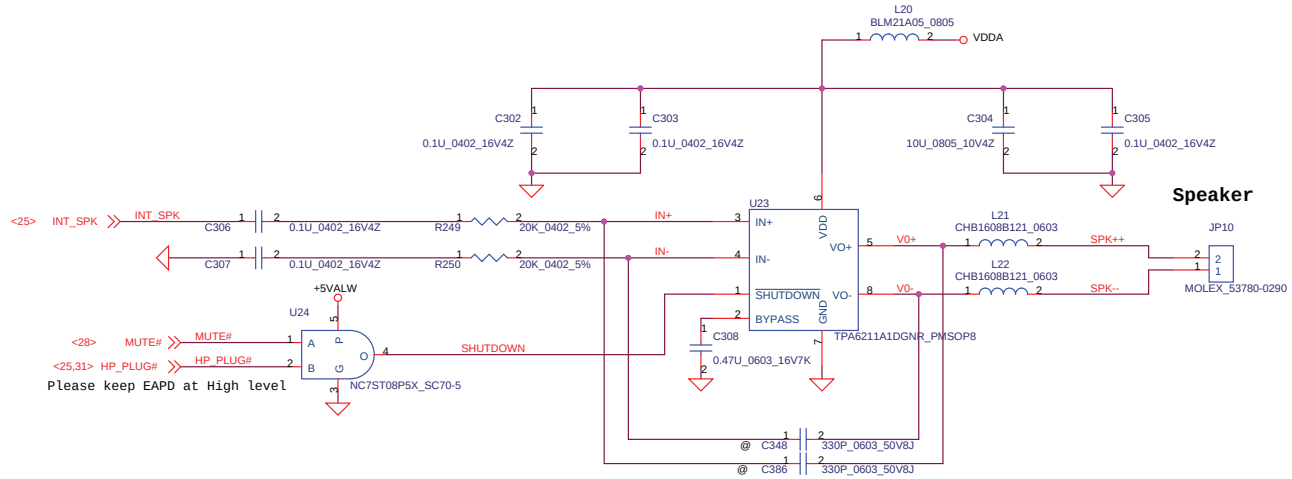
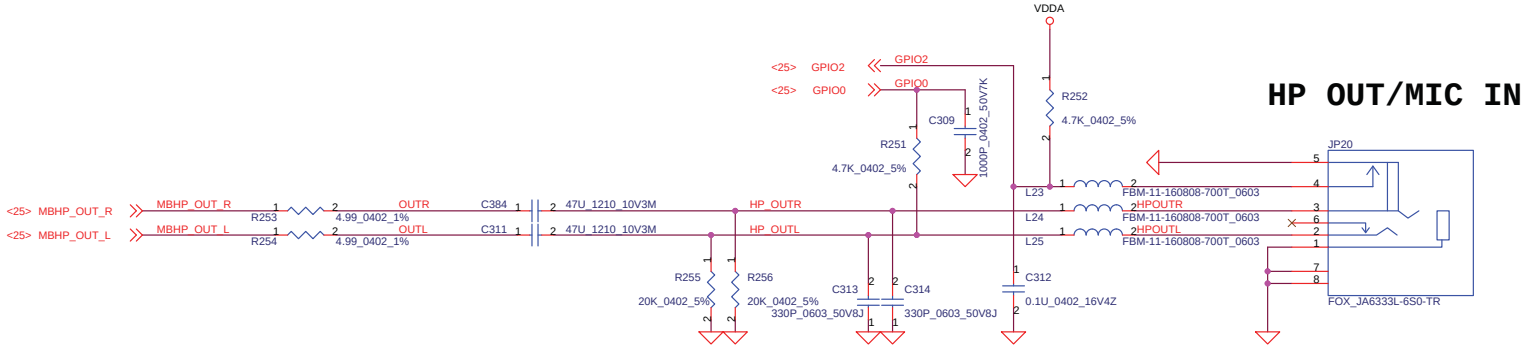
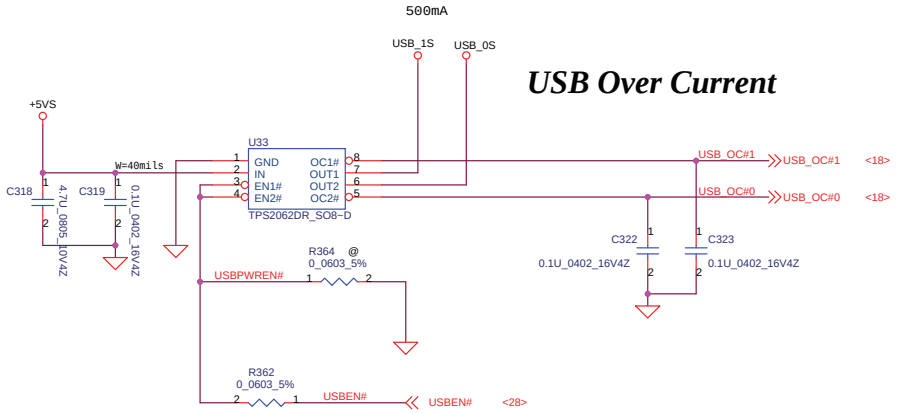
AMP. FOR INTERNAL SPEAKER



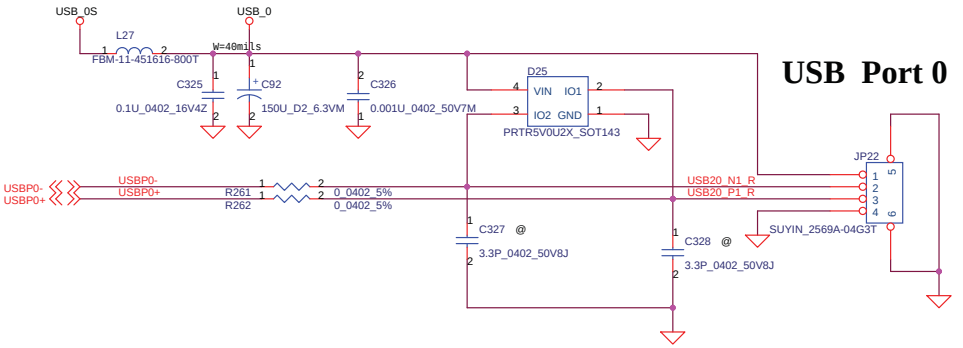
HP OUT/MIC IN



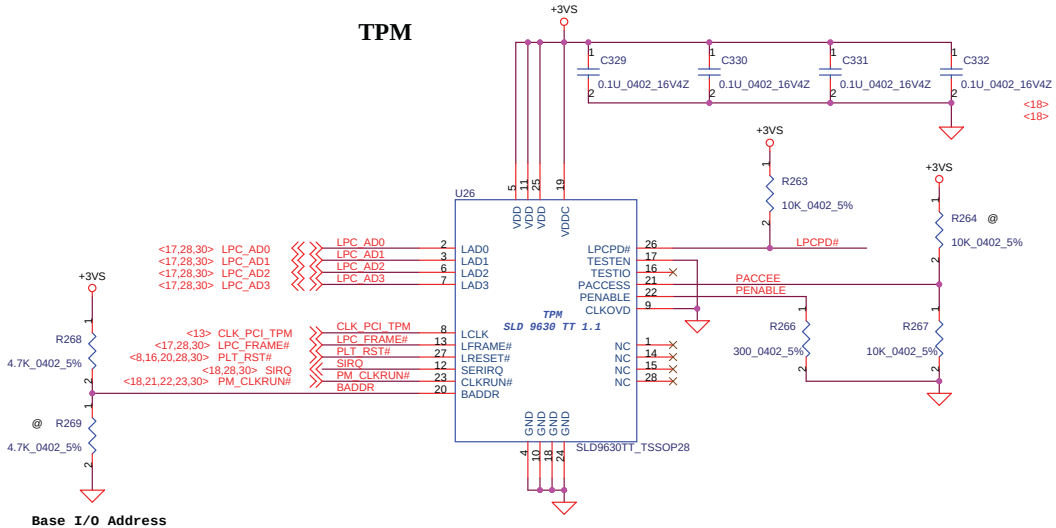
USB Over Current



USB Port 0



TPM

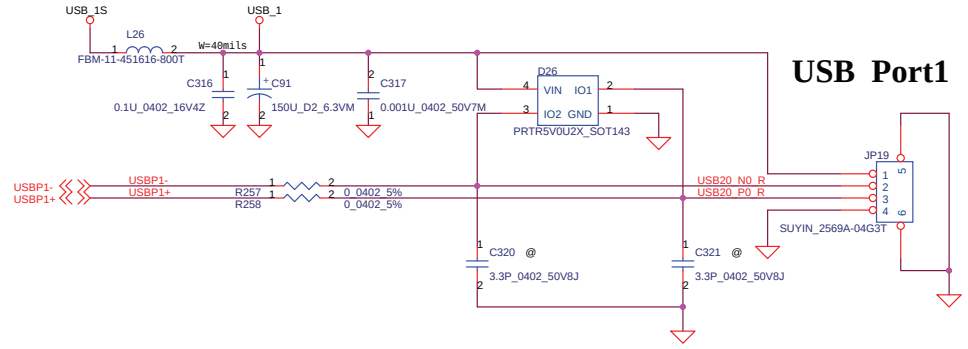


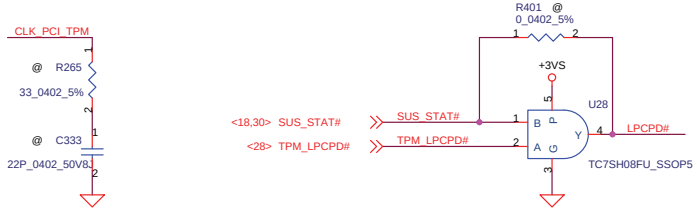
Base I/O Address
0 = 02Eh
* 1 = 04Eh

PACCESS: The standard should connect to GND, if the pin is connected to VDD, the Force_Clear command is enable. and also used for other features, fefer to the TCG.

9/22 is reserved pin. connect to GND

USB Port1





Compal Electronics, Inc.(KunShan)
Title: USB PORT/TPM
Size: Custom
Document Number: Bandera-EAX00-LA2581
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L28 FBM-L11-160808-601LMT_200mA_10%
L29 FBM-L11-160808-601LMT_200mA_10%

HW STRAP PIN(910L only 2 pin)
pin47: TP_TEST, Low active
pin48: TP_PLL, low active
For normal application, no application component is requried to select the normal mode because kb910L has an internally build-in pull up resistor that automatically selects the suitable operation mode.

TP_TEST: Clock Test Mode/ Low: Test Mode/ High: 32KHz clock in normal running
TP_PLL: DPLL Test Mode/ Low: Test Mode/ High: Normal operation
R272 and R323 is unnecessary, because KB910L pin 47 and 48 are pull-up internally04/11/30

U27 KB910L_LQFP144

Version5 is MP Board ID

BDID2	BDID1	BDID0	Version	Phase
0	0	0	0	EVT1
0	0	1	1	EVT2
0	1	0	2	DVT1
0	1	1	3	DVT2
1	0	0	4	PVT
1	0	1	5	MP
1	1	0	6	
1	1	1	7	

Project ID	Bandera	Pecos
0	△	
1		△

Compal Electronics, Inc.(KunShan)
Title: ENEKB910L
Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0
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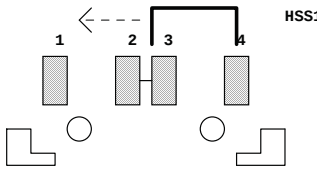
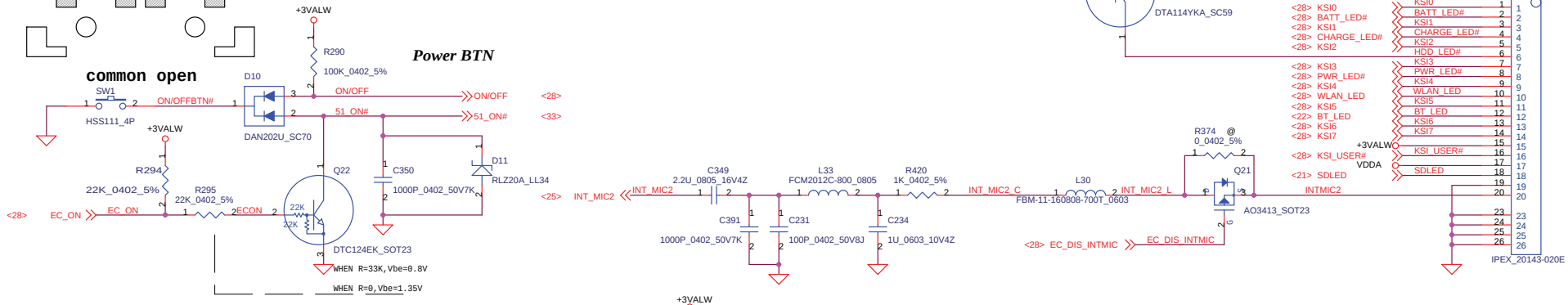
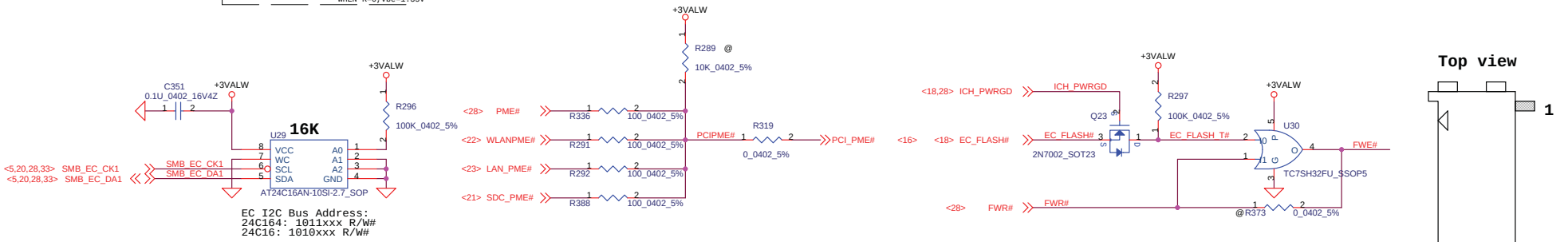
TOP VIEW(HSS111)



HSS110 reverse with HSS111

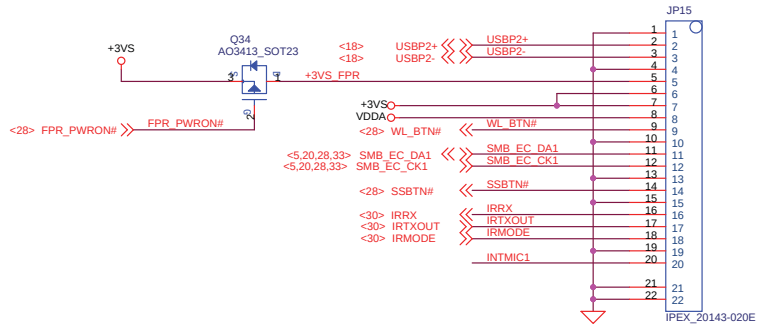
SW/LED/MIC2



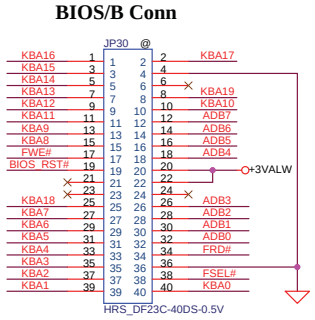


Top view

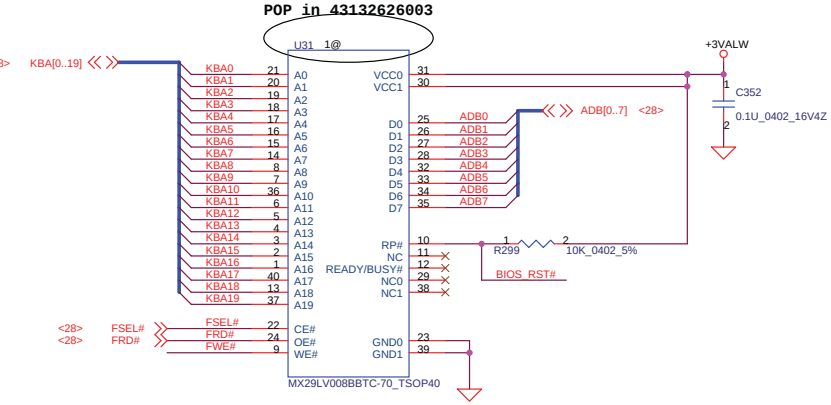
ALS/MIC1/FPR/irDA/WLBTN/SSBTN CONN.

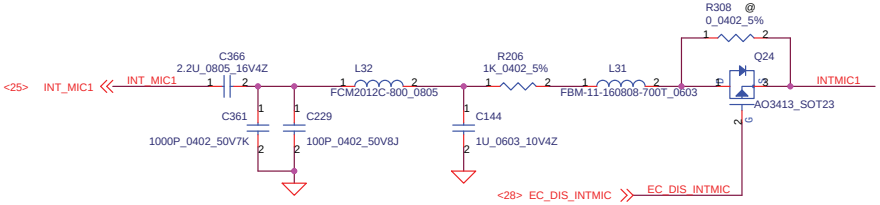


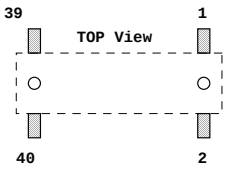
BIOS/B Conn



POP in 43132626003





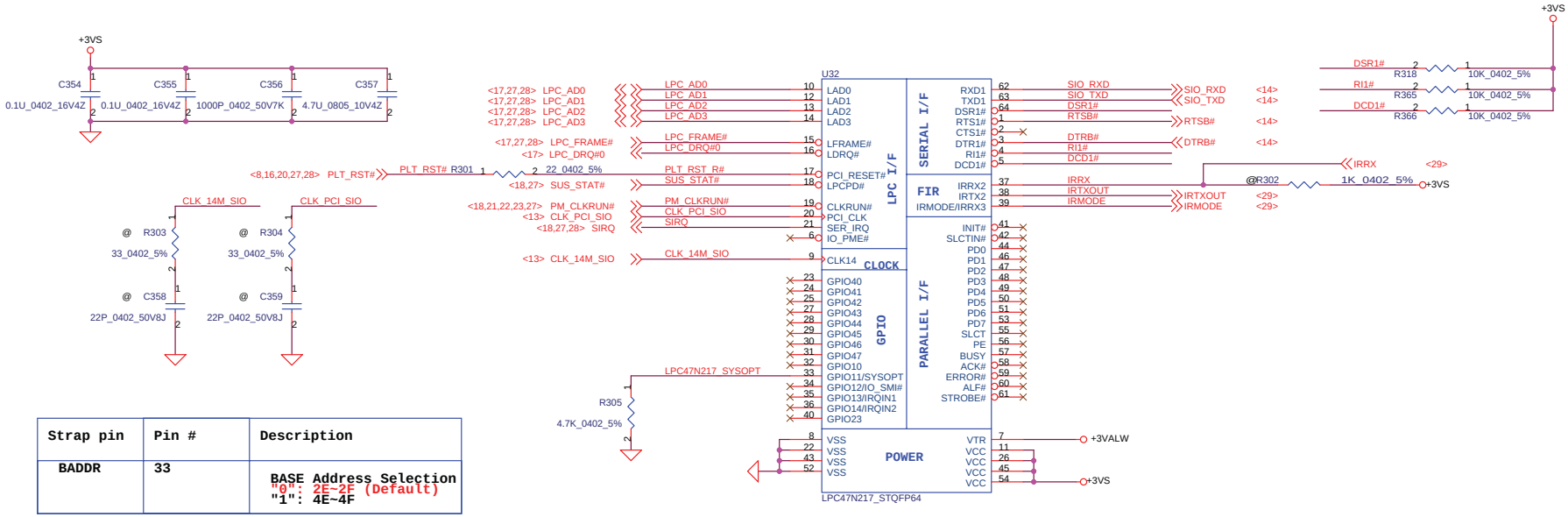


Compal Electronics, Inc.(KunShan)

Title: BIOS ROM/IO PORT

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

Date: Friday, June 17, 2005 | Sheet 29 of 48



Strap pin	Pin #	Description
BADDR	33	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F

Compal Electronics, Inc.(KunShan)
Title: LPC47N217/FIR
Size: Custom
Document Number: Bandera-EAX00-LA2581
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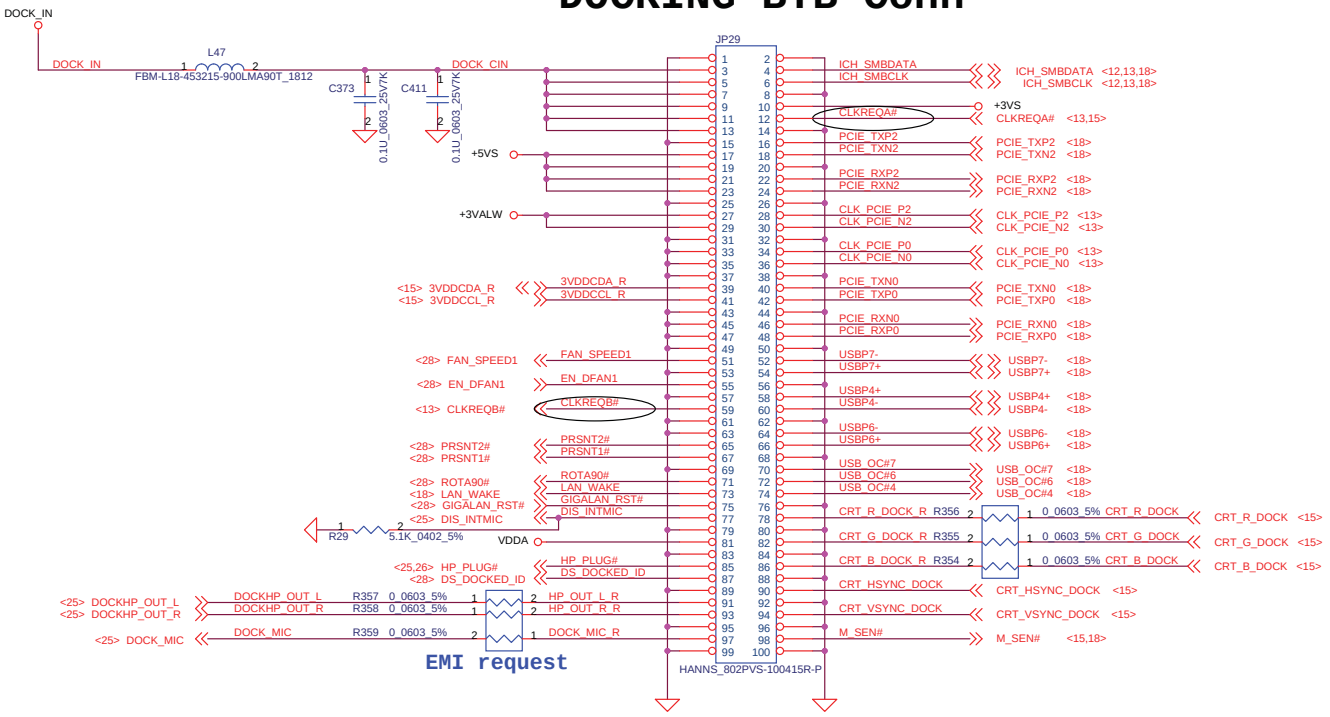
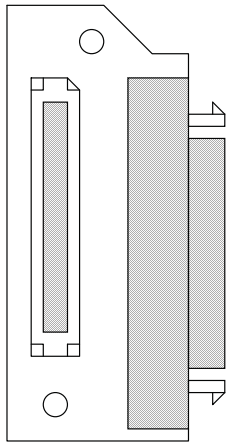
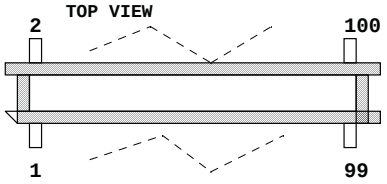
DOCKING BTB Conn

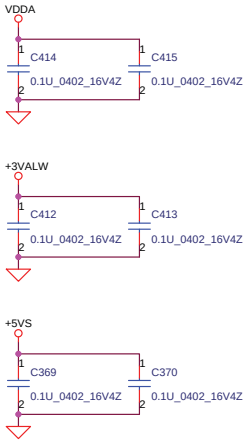


Dock covert board



Dock BTB conn(MB side)





Compal Electronics, Inc.(KunShan)
Title: Docking conn/other conn
Size: Custom
Document Number: Bandera-EAX00-LA2581
Rev: X5.0
Date: Friday, June 17, 2005
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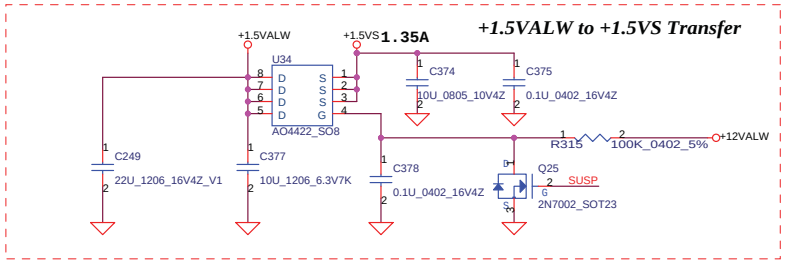

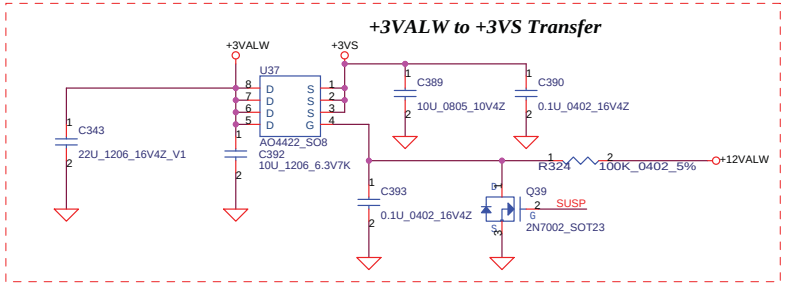

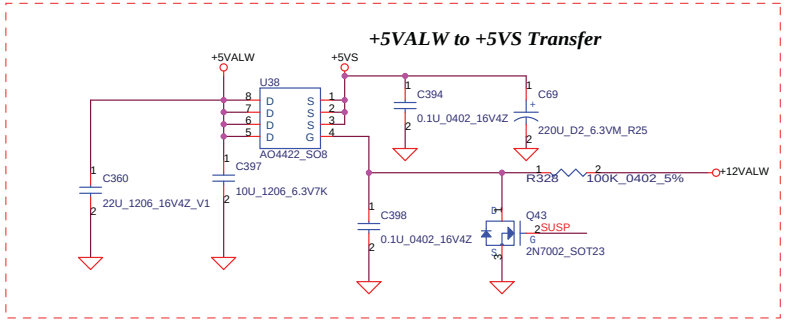

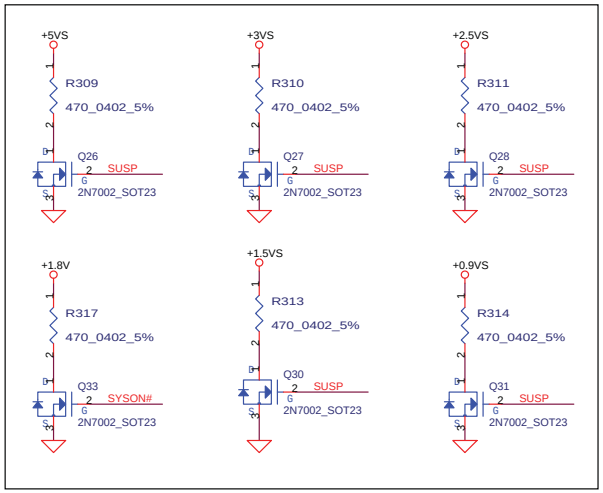

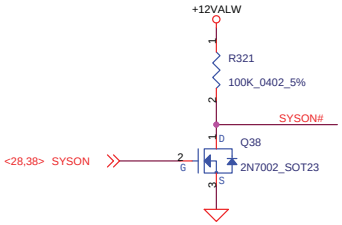

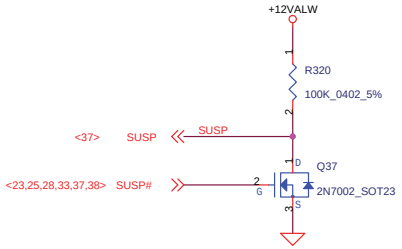

Compal Electronics, Inc.(KunShan)

Title: DC-DC

Size: Custom | Document Number: Bandera-EAX00-LA2581 | Rev: X5.0

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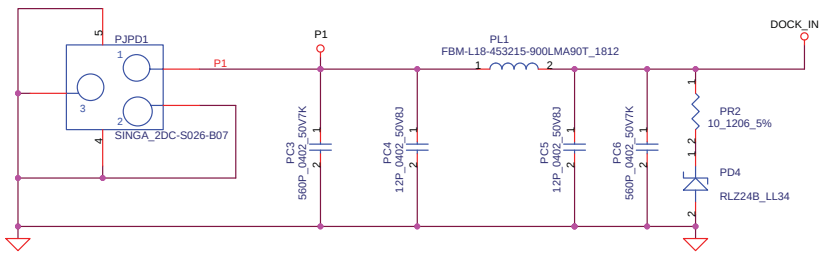
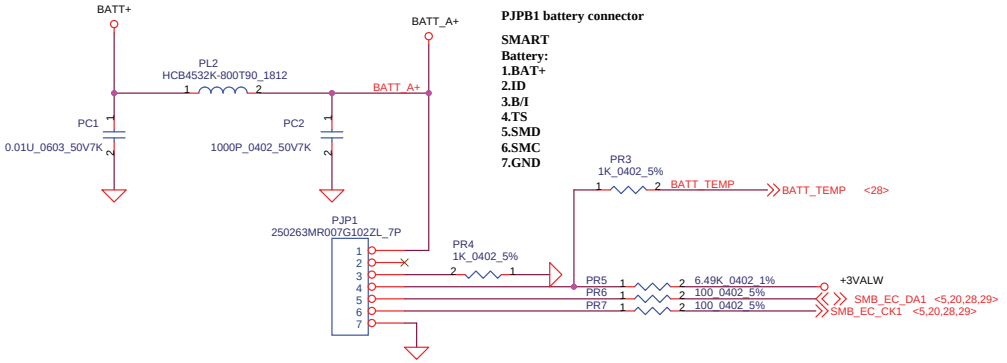
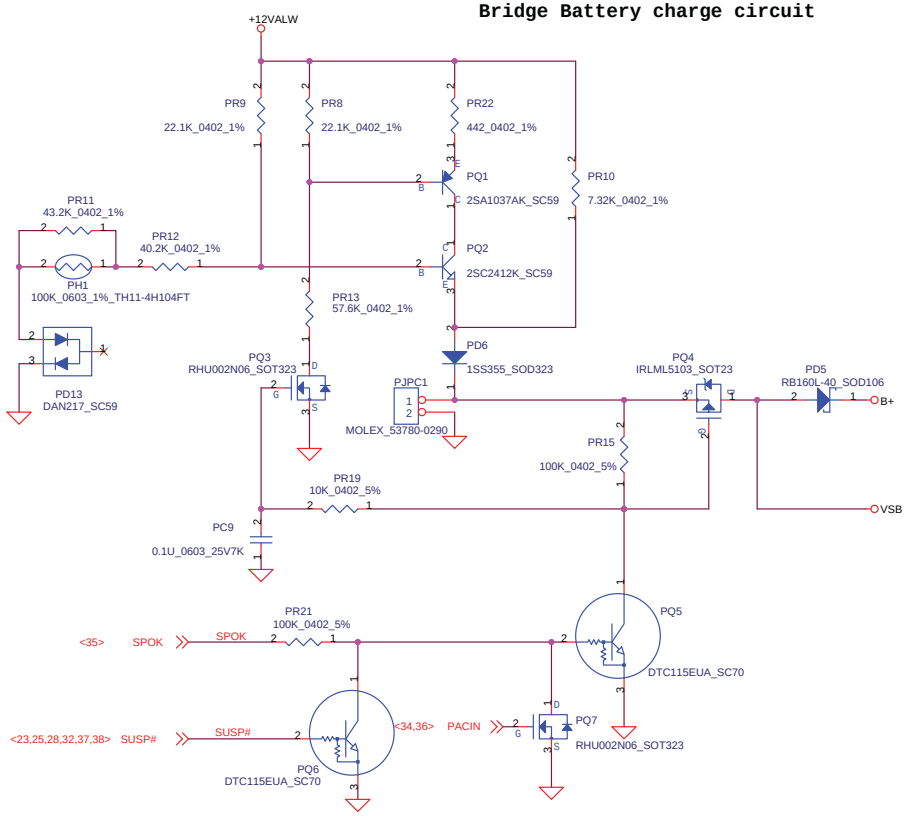
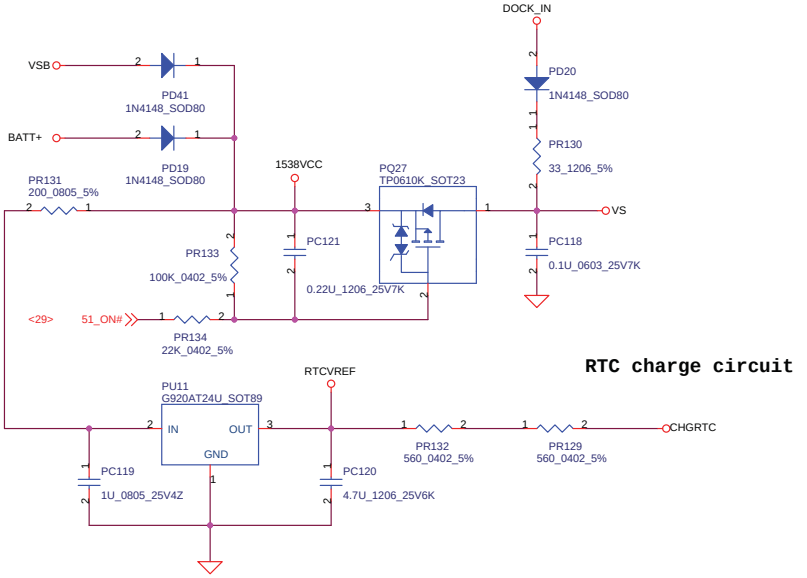




Bridge Battery charge circuit





RTC charge circuit

Compal Electronics, Inc.(KunShan)	
Title	Vin detec and bridge BATT
Size: Custom	Document Number: Bandera-EAX00-LA2581
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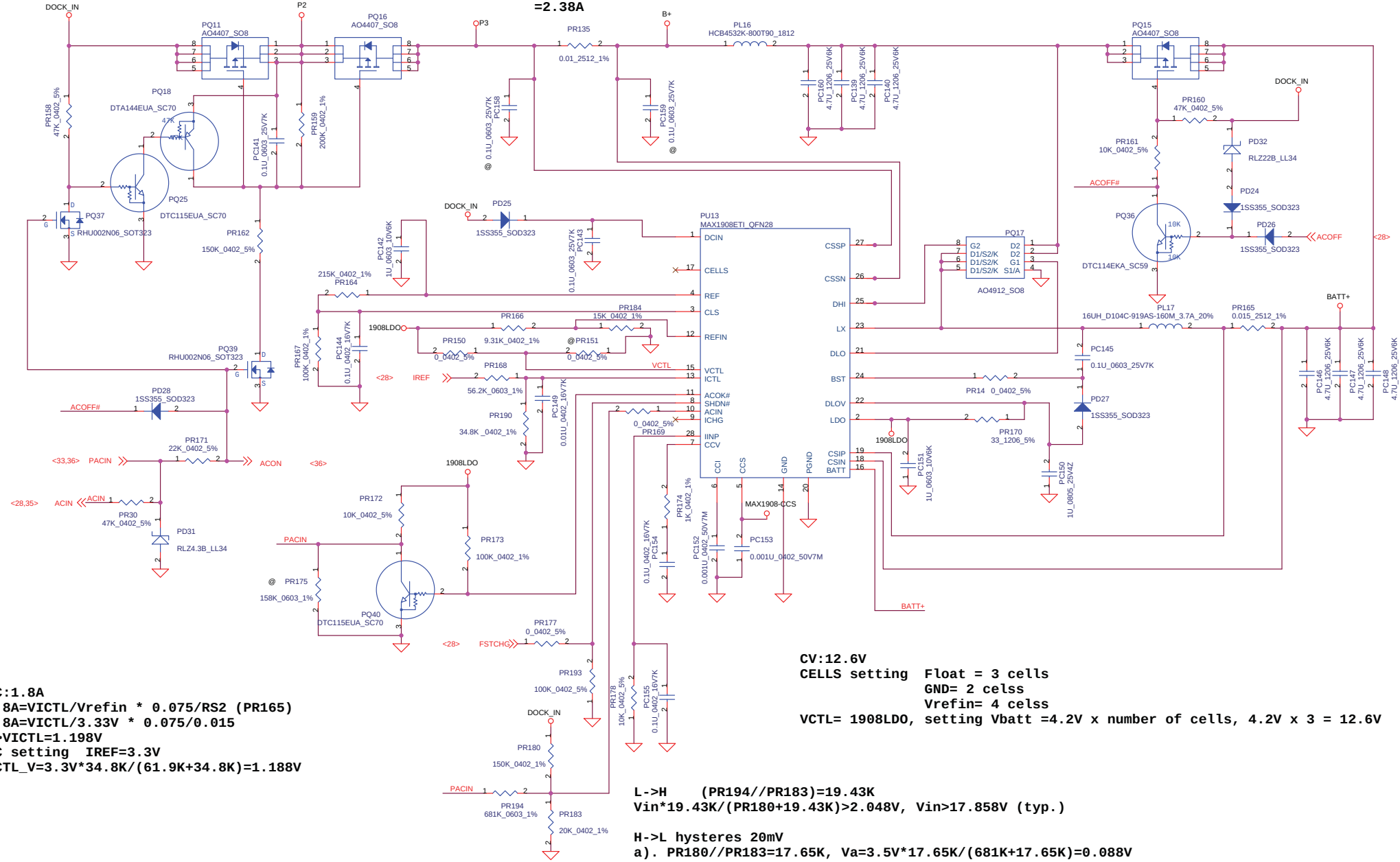
Date: Friday, June 17, 2005	Sheet 33 of 48

Charger

19V/2.63A(50W)
Iadp=2.63A*0.9 = 2.37A

Vcls=Vref*(PR167//(PR164+PR163))=4.096V*100K/150K=2.73V
Iadp=(Vcls/Vref)*0.075/R_sense
= 1.3V/4.096V * 0.075/0.01ohm
=2.38A



CC:1.8A
1.8A=VICTL/Vrefin * 0.075/RS2 (PR165)
1.8A=VICTL/3.33V * 0.075/0.015
->VICTL=1.198V
EC setting IREF=3.3V
ICTL_V=3.3V*34.8K/(61.9K+34.8K)=1.188V

CV:12.6V
CELLS setting Float = 3 cells
GND= 2 celss
Vrefin= 4 celss
VCTL= 1908LDO, setting Vbatt =4.2V x number of cells, 4.2V x 3 = 12.6V

L->H (PR194//PR183)=19.43K
Vin*19.43K/(PR180+19.43K)>2.048V, Vin>17.858V (typ.)

H->L hysteres 20mV
a). PR180//PR183=17.65K, Va=3.5V*17.65K/(681K+17.65K)=0.088V
b).PR194//PR183=19.43K, Vin*19.43K/(150K+19.43K)<4.096V/2-20mV-0.088V (ACOK# L->H)
Vin< 16.92V (tpy.)

L->H 17.858V(typ.)
H->L 16.92V(typ.)

Compal Electronics, Inc.(KunShan)
Title: Charger
Size: Custom
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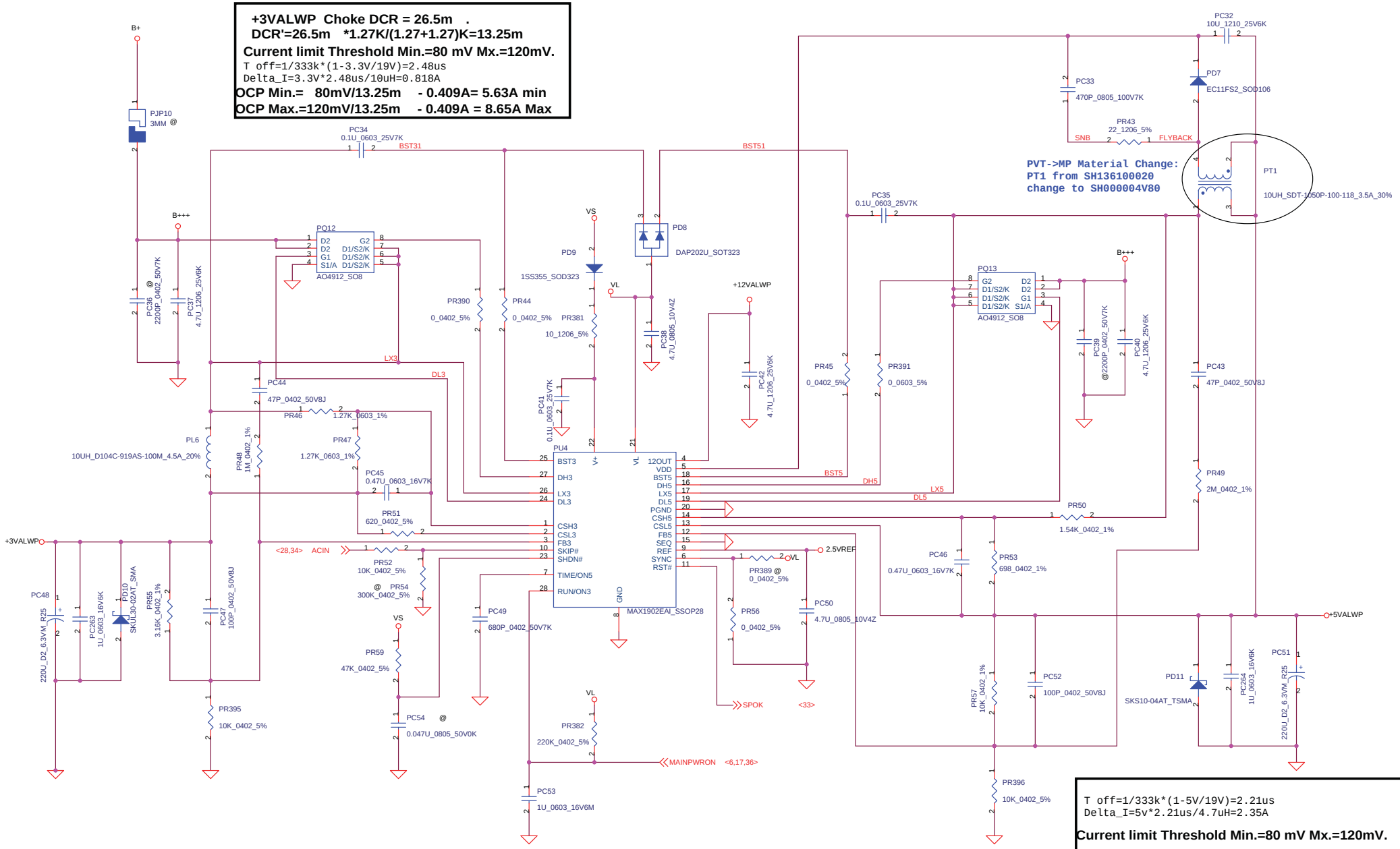
+3.3V/+5V/+12V

+3VALWP Choke DCR = 26.5m .
DCR'=26.5m *1.27K/(1.27+1.27)K=13.25m
Current limit Threshold Min.=80 mV Mx.=120mV.
T off=1/333k*(1-3.3V/19V)=2.48us
Delta_I=3.3V*2.48us/10uH=0.818A
OCP Min.= 80mV/13.25m - 0.409A= 5.63A min
OCP Max.=120mV/13.25m - 0.409A = 8.65A Max



T off=1/333k*(1-5V/19V)=2.21us
Delta_I=5v*2.21us/4.7uH=2.35A

Current limit Threshold Min.=80 mV Mx.=120mV.

OCP Min.= 80mV/11.12m-2.35A/2=6.02A min

OCP Max.=120mV/11.12m-2.35A/2= 9.62A Max

Compal Electronics, Inc.(KunShan)
Title: +3V/+5V/+12VALW
Size: Custom
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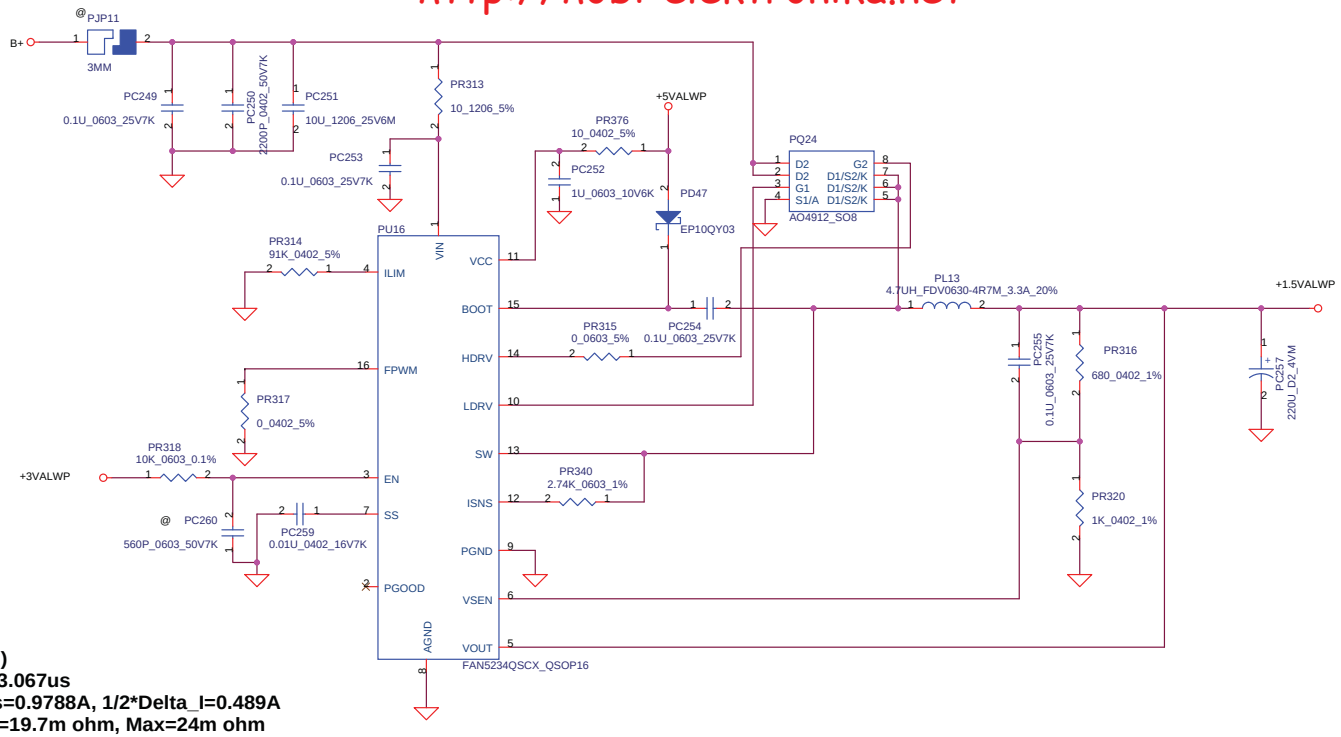
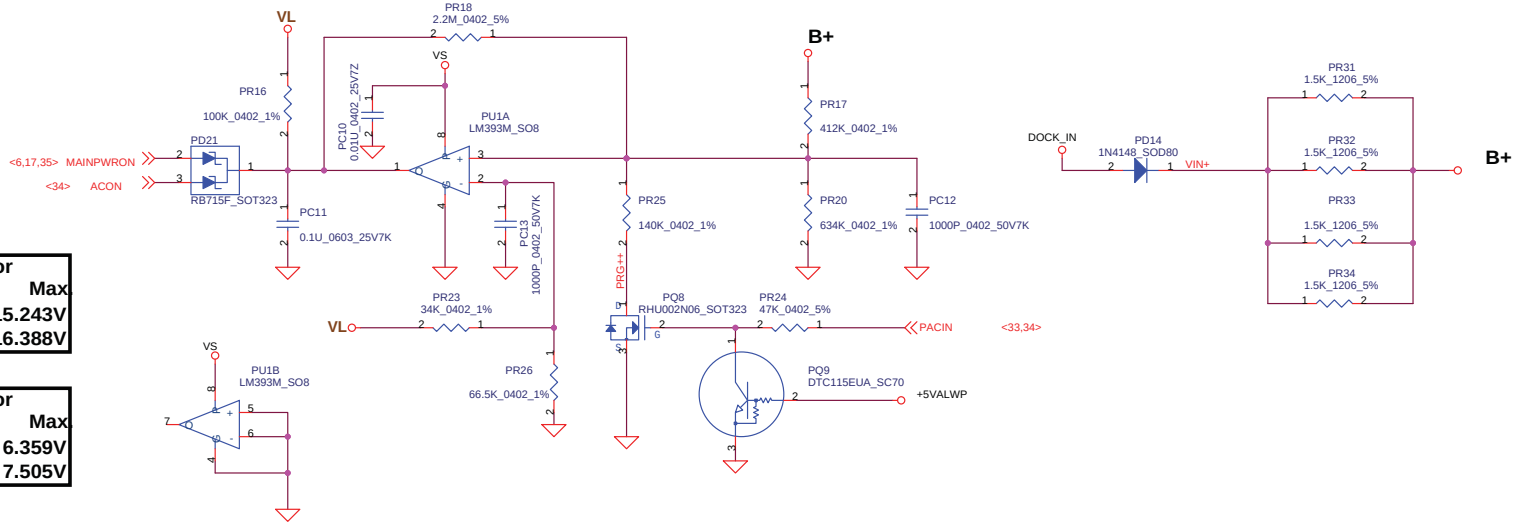


Iimit=9.6/RILIM*(100+Rsense)/Rds (on)
Toff=T(1-Vo/Vin)=3.33us(1-1.5V/19V)=3.067us
Delta_I=Vo/L*Toff=1.5V/4.7uH*3.067us=0.9788A, 1/2*Delta_I=0.489A
Rsense=2k, RILM=100k, Rds (on) typ.=19.7m ohm, Max=24m ohm
Iimit min = 9.6/100k*(100+24m ohm * 1.3)-1/2 Delta_I=5.97A
Iimit Max = 9.6/100k*(100+19.7m ohm)-1/2 Delta_I=9.74A



ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Compal Electronics, Inc.(KunShan)
Title: +1.5VALWP
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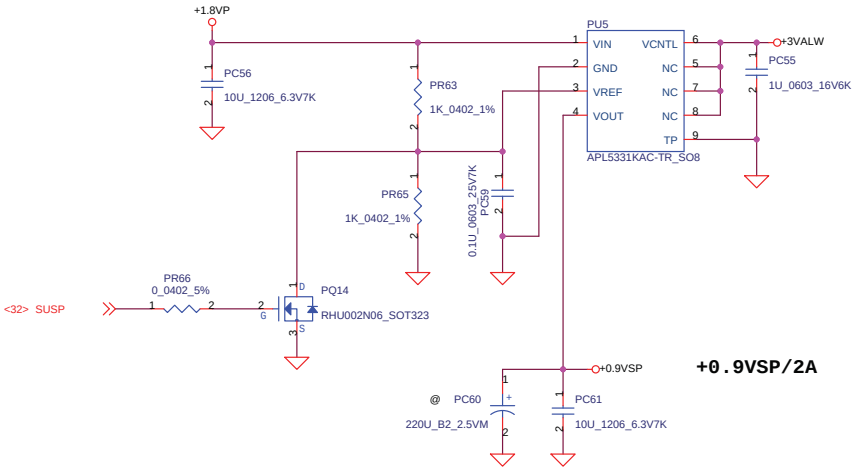
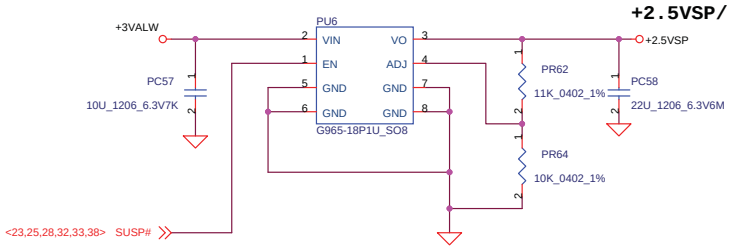
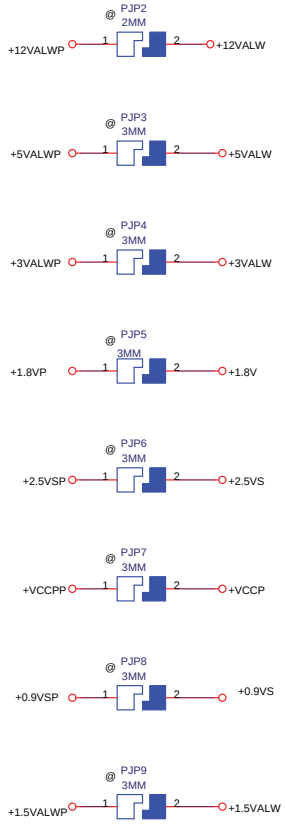
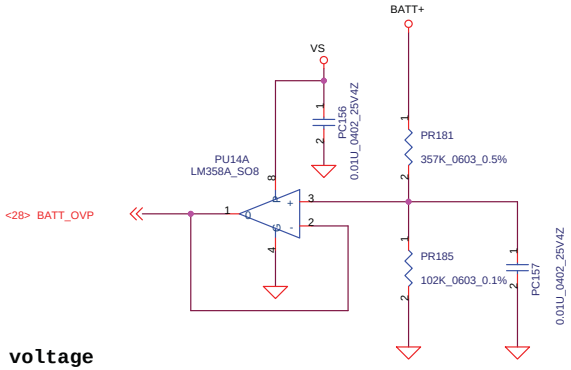


+0.9VSP/2A

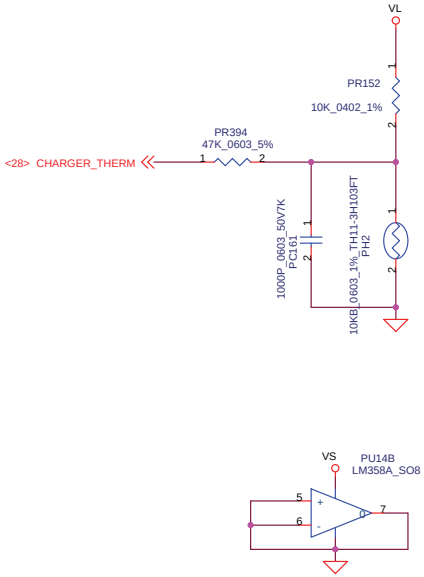


+2.5VSP/ 1A





OVP voltage
Li-3S : 13.5V
Batt-OVP=13.5v* 102K/(102K+357K)=3V



Del CPU OTP circuit , cause H/W implement this function
Del PR377,PR378,PR379, PQ41,PR380

Compal Electronics, Inc.(KunShan)
Title: 0.9VSP/1.5ALW/2.5V
Size: Custom
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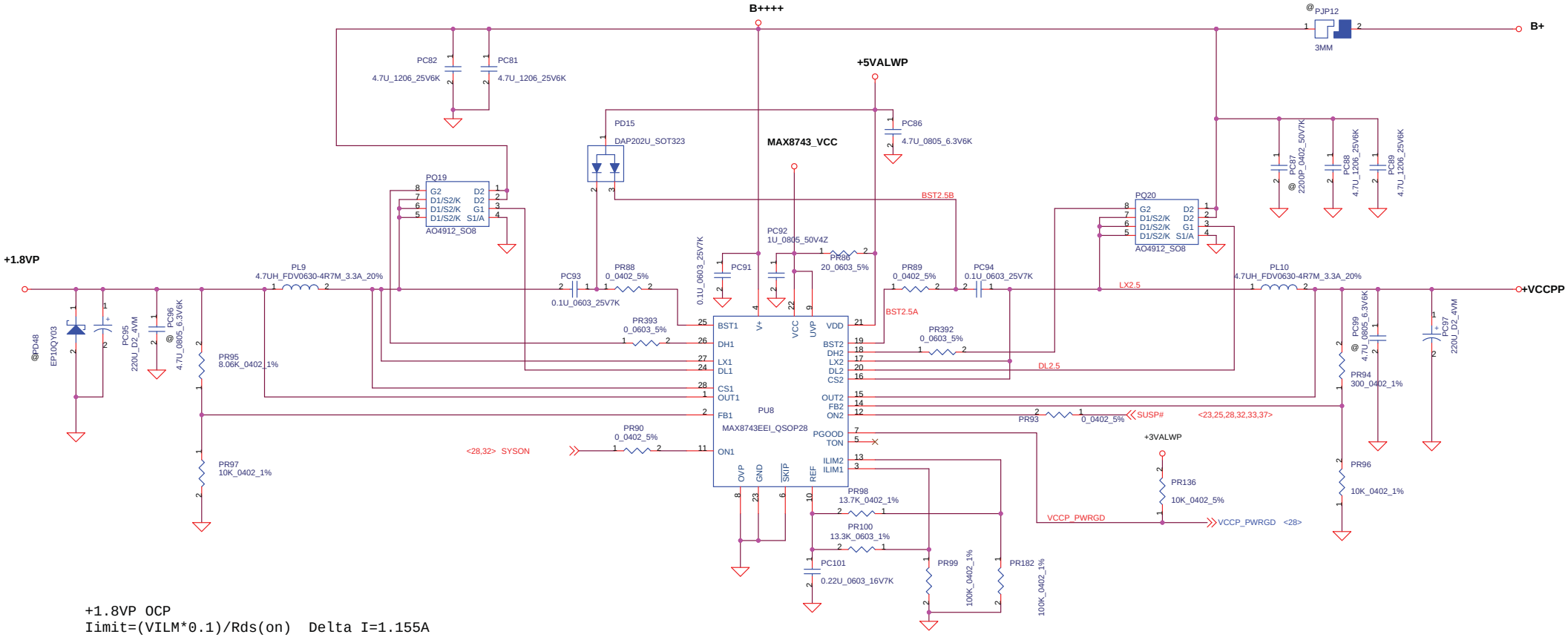

+1.8VP OCP
Iimit=(VILM*0.1)/Rds(on) Delta I=1.155A
VILM=1.765V Rds(on) typ=19.7mOhm, max=24mOhm
Iimit Min=(1.765*0.1)*0.9/(24mOhm*1.3)+1/2 Delta I=5.66A
Iimit Max=(1.765*0.1)*1.1/(19.7mOhm*1.3)+1/2 Delta I=8.15A

VCCP OCP
Delta I= Vo/L*Toff, Toff=T*(1-Vo/Vin), T=1/255Khz
Toff= 1/255Khz * (1-1.05V/19V)=3.7uS
Delta I= 1.05V/4.7uH * 3.7uS =0.826A
Iimit=(VILM*0.1)/Rds(on)
VILM=2V Rds(on) typ=15.5mOhm, max=20mOhm
Iimit Min=(1.76*0.1)*0.85/(20mOhm*1.3)+1/2 Delta I=6.16A
Iimit Max=(1.76*0.1)*1.15/(19.7mOhm*1.3)+1/2 Delta I=8.31A

Compal Electronics, Inc.(KunShan)
Title: VCCP/1.8VP
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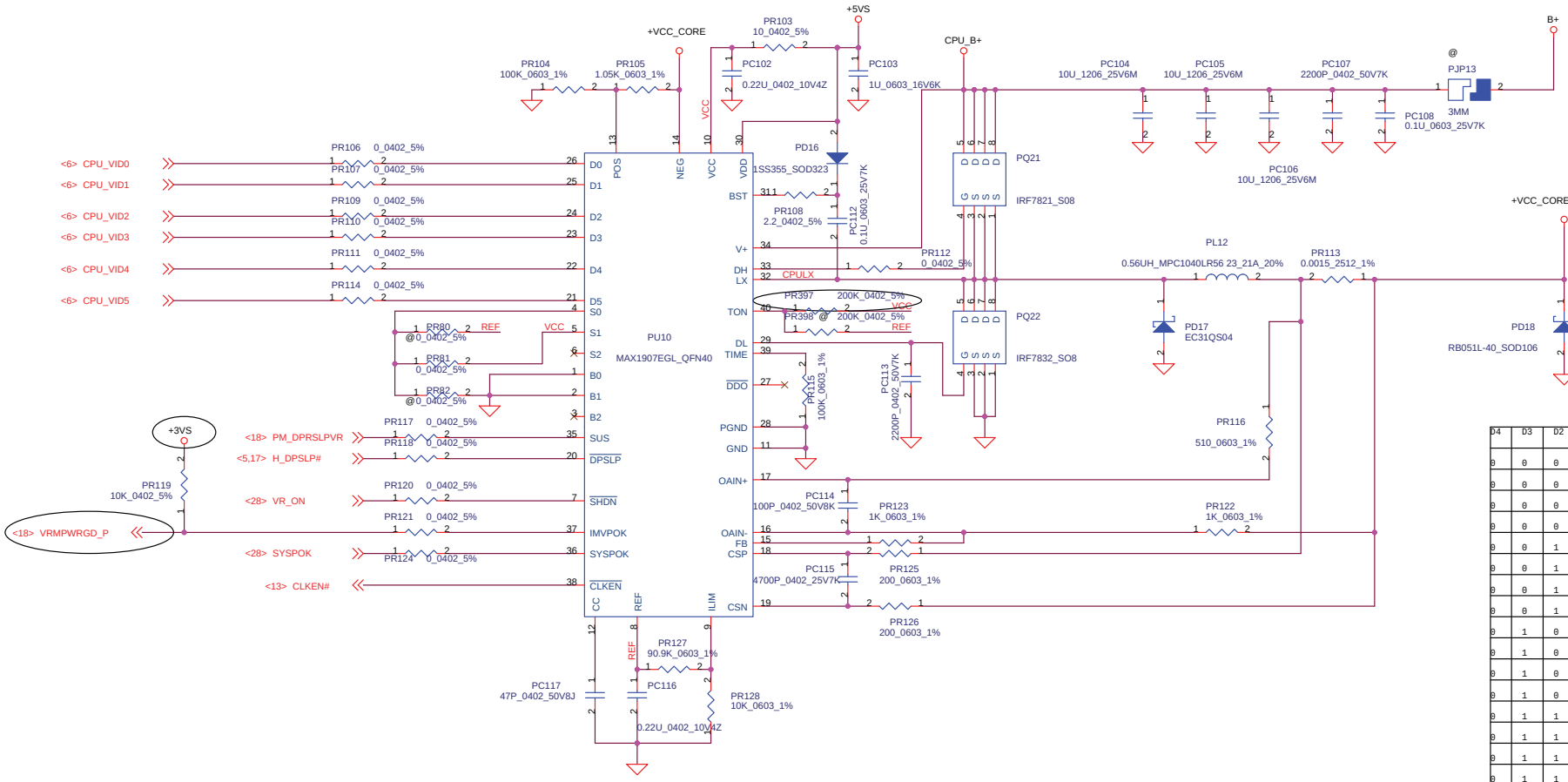
CPU-CORE



D4	D3	D2	D1	D0	D5 = 1	D5 = 0
0	0	0	0	0	1.196	1.708
0	0	0	0	1	1.180	1.692
0	0	0	1	0	1.164	1.676
0	0	0	1	1	1.148	1.660
0	0	1	0	0	1.132	1.644
0	0	1	0	1	1.116	1.628
0	0	1	1	0	1.100	1.612
0	0	1	1	1	1.084	1.596
0	1	0	0	0	1.068	1.580
0	1	0	0	1	1.052	1.564
0	1	0	1	0	1.036	1.548
0	1	0	1	1	1.020	1.532
0	1	1	0	0	1.004	1.516
0	1	1	0	1	0.988	1.500
0	1	1	1	0	0.972	1.484
0	1	1	1	1	0.956	1.468
1	0	0	0	0	0.940	1.452
1	0	0	0	1	0.924	1.436
1	0	0	1	0	0.908	1.420
1	0	0	1	1	0.892	1.404
1	0	1	0	0	0.876	1.388
1	0	1	0	1	0.860	1.372
1	0	1	1	0	0.844	1.356
1	0	1	1	1	0.828	1.340
1	1	0	0	0	0.812	1.324
1	1	0	0	1	0.796	1.308
1	1	0	1	0	0.780	1.292
1	1	0	1	1	0.764	1.276
1	1	1	0	0	0.748	1.260
1	1	1	0	1	0.732	1.244
1	1	1	1	0	0.716	1.228
1	1	1	1	1	0.700	1.212

```
Delta I=0.0528A  REF MAX=2.01V*10K/(10K+90.2K)=0.2005V
REF Min=1.99V*10K/(10K+90.2K)=0.1986V
Iimit Max=0.2005V*10/1.485m  +1/2
Iimit Min=0.1986V*10/1.515m  +1/2
Delta=13.135
```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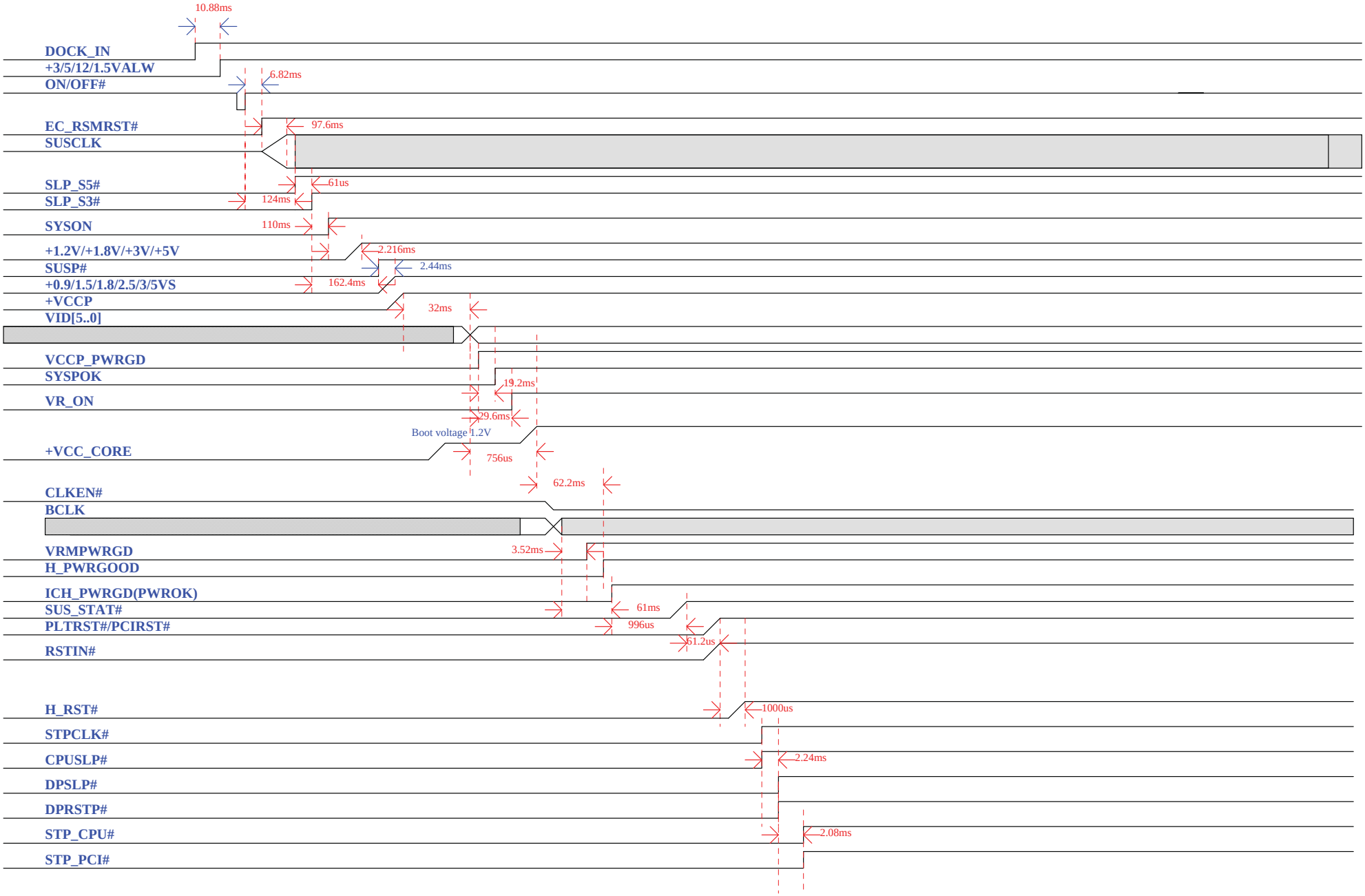
Bandera Platform power up sequence with AC



Compal Electronics, Inc.(KunShan)
Title: Power Sequence
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HW P.I.R LIST---EVT2

Change item	Change reason	Page#	Date	Revision
1. ADD C113 C114 R29 Q29 U6	Motion asked add thermal sensor to monitor Panel and inverter temperature	P14	9/30/04	X09D->X1.0
2. Route SMB_EC_CK2, SMB_EC_DA2 to dock	Motion asked to reading dock temperature	P32	9/30/04	X09D->X1.0
3. Route EN_DFAN1 and FAN_SPEED1 to dock	Motion asked to add this function to control dock fan	P32	9/30/04	X09D->X1.0
4. Swap dock pin	To layout as easily and well as enough	P32	9/30/04	X09D->X1.0
5. Add R319	Per EC team asked reserve ICH6M PME# funtion	P30	9/30/04	X09D->X1.0
6. Connect U5D.Y1 to VCCP	Net connect error	P11	9/30/04	X09D->X1.0
7. Delete SMB_EC_CK2, SMB_EC_DA2 from dock connector	Per Motion asking no need to read dock temperature.	P32	10/12/04	X1.0->X1.1
7. Swap PRSNT1# and PRSNT2# on dock connector	For layout trace to route.	P32	10/12/04	X1.0->X1.1
8. Delete USB port 5 over current signal from dock	Route USB port 4 over current signal to dock	P32	10/12/04	X1.0->X1.1
9. Swap BATT1 PIN	RTC BATT PIN error	P17	10/12/04	X1.0->X1.1
10. Add put down resister R353	Solve the DPRSLPVR signal may not be properly initialized until ICH6-M's core well power rails(Vcc1_5, Vcc3_3) became stable and ICH6-M receives PCI clock issue	P18	11/01/04	X1.0->X1.1
11. Add signal EC_SLP_S4#	Add the EC_SLP_S4# function	P18,P28,P29	11/01/04	X1.0->X1.1
12. Change PCI_PIRQA# to PCI_PIRF#	Sync up with Pecos	P16, P23	11/01/04	X1.0->X1.1
13. Change USBEN# connect point from GPO21 to GPO23	Meet customer specification	P18	11/01/04	X1.0->X1.1
14. Add R368,R369,Q32; Delete R340; connect WL_EN# control signal to GPO21	Meet customer specification	P18, P22	11/01/04	X1.0->X1.1
15. Delete C251,C264,C80,C99,C84,C98,C103,C372,C101,C371, R1158,R1159,Q54,Q55	Meet customer specification	P10,P32	11/01/04	X1.0->X1.1
16. Add U36; delete Q29, C114, R29, U6	Motion asked add thermal sensor to monitor Panel and inverter temperature	P14	11/01/04	X1.0->X1.1
17. Change PHDD_LED# control signal from SW/LED board to M/B and add Q29	SW/LED board do not have +3VS power plane and the signal PHDD_LED# need +3VS as power supplier	P30	11/08/04	X1.0->X1.1
18. Change U4 Power plane from +3VALW/+3VS to VL power plane	EE change request	P6	11/08/04	X1.0->X1.1
19. Change U36 power from +5VS to +3.3VS and will change the U36 to 3.3VCT	Layout need change the power +5VS plane to +3VS plane	P14	11/08/04	X1.0->X1.1
20. Change R216 from 4.7ohm to 4.7Kohm	EE change request, change material but reserve locatioin	P21	11/09/04	X1.0->X1.1
21. Change R242 from 22ohm to 33ohm	EE change request, for impedance matching. Change material but reserve locatioin	P25	11/09/04	X1.0->X1.1
22. Add R240 to GPIO0	EE change request	P25	11/09/04	X1.0->X1.1
23. Add R370 to GPIO1	EE change request for STAC9200 select	P25	11/09/04	X1.0->X1.1
23. Add C371 to FRONT_R	EE change request	P25	11/09/04	X1.0->X1.1
24. Add C372 to FRONT_L	EE change request	P25	11/09/04	X1.0->X1.1
25. Change net name	EE change request	P14/P31	11/10/04	X1.0->X1.1
26. Delete signal WRBT_ICH	EE change request	P18	11/10/04	X1.0->X1.1
27. Delete R185	It is the signal WRBT_ICH pull up resister, it should delete together with WRBT_ICH	P18	11/10/04	X1.0->X1.1
28. Move signal	Move signal M_SEN# from U13.R3(GPIO27) to U13.AE19(GPI7)	P18	11/10/04	X1.0->X1.1
29. Delete R163	Signal KBRST# pull up resister have reduplicate	P17	11/10/04	X1.0->X1.1
30. Delete R180	Signal EC_SMI# pull up resister have reduplicate	P18	11/10/04	X1.0->X1.1

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HW P.I.R LIST---EVT2

Change item	Change reason	Page#	Date	Revision
31. Delete R168	Signal AC97_RST_R# pull up resister have reduplicate	P17	11/10/04	X1.0->X1.1
32. Move control signal	Sync up with Pecos, move USBEN# signal from ICH6 to EC	P18/P28/P29	11/10/04	X1.0->X1.1
33. Add control signal	Add signal DIGI_FWE to U13.V3(GPIO24) and connect to JP32.9	P14/P18	11/10/04	X1.0->X1.1
34. Change material P/N	Change U33 P/N from SA02026000L to SA020620000	P27	11/10/04	X1.0->X1.1
35. Add FPR power control MOS	Add FPR power control MOS Q34 and FPR_PWRON control signal connect to EC	P28/P29/P30	11/10/04	X1.0->X1.1
36. Move control signal	Move control signal SSBTN from U28.98 to U28.90	P29	11/10/04	X1.0->X1.1
37. Add C251	Add C251 to net MAX6509OUT#	P6	11/11/04	X1.0->X1.1
38. Change R54,R55 resistance from 10K ohm to 1K ohm	Change R54,R55 resistance from 10K ohm to 1K ohm but do not change they location	P8	11/11/04	X1.0->X1.1
39. Delete R44, R45	EE change request	P8	11/13/04	X1.0->X1.1
40.Change signal WL_EN# to WL_EN	WL_EN signal valid should active high	P18/P22	11/13/04	X1.0->X1.1
41. Delete signal EC_RXD	EE change request	P28	11/13/04	X1.0->X1.1
42. Move signal EC_TXD	EE change request	P28	11/13/04	X1.0->X1.1
43. Move signal PRST1#	Move signal PRST1# from U27.34 to U27.89	P28	11/13/04	X1.0->X1.1
44. Move signal PRST2#	Move signal PRST2# from U27.35 to U27.90	P28	11/13/04	X1.0->X1.1
45. Add control signal	Add control signal EC_DIS_INTMIC	P28	11/13/04	X1.0->X1.1
46. Update Power Sequence	Update power sequence	P42	11/13/04	X1.0->X1.1
47. Add GigaLAN_RST# to Dock board	EE change request	P32/P28/P29	11/16/04	X1.0->X1.1
48. Add R339, R371, C385	Signal TXD+- EA test fail and Realtech suggest add these components	P24	11/17/04	X1.0->X1.1
49. Delete C228,C230,C229,C231,R213,R341,R214, C235,U17,R209,R212,Q18,U18,C236	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
50. Change R28: 1K_0402_5%--->1M_0402_5%	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
51. Change R216: 4.7K_0402_5%--->100K_0402_5%	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
52. Change R219: 1M_0402_5%--->10K_0402_5%~D	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
53. Change RP17: 4.7K_0804_8P4R_5%--->10K_1206_8P4R_5%	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
54. Add R180,Y3,C80,C84,L32,L33,U6,Q35,C391,C396,C416,C417C361, C386,C387,C418,R372,R341,R168,Q16,C264,R163	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
55. Delete SD Clock signal: CLK_48M_SD&CLK_PCI_SD and its serial resistor: R87,R96	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P21	11/19/04	X1.0->X1.1
56. Connect USB5+- to SD controller	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P18/P21	11/19/04	X1.0->X1.1
57. Delete SD signal SDC_PME#	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P30	11/19/04	X1.0->X1.1
58. Delete SD control signal: LPC_DRQ1#	Change the SD controller from W83L518D to Alcor 6369 and circuit need change	P17	11/19/04	X1.0->X1.1
59. Add PQ26,PQ23,PC162,PR187,PR163	Add DOCK_IN power control fucction	P32	11/19/04	X1.0->X1.1
60. Add SD controller W83L528D circuit	Add the W83L528D as the SD card controller	P22	11/23/04	X1.0->X1.1
61.Delete the Touch Screen function, please refer the attached Word file	For the following reason:1. PCB do not have enough space to placement and layout; 2. not use this function	P22	11/23/04	X1.0->X1.1
62.Change LCD_Digitizer_cable;BlueTooth_Cable; FPR_Mic_Cable pin define	For the cable wire can be more tidiness and some signal define change	P14/P23/P31	11/23/04	X1.0->X1.1

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HW P.I.R LIST---DVT1

Change item	Change reason	Page#	Date	Revision
1. Change R89 Resistance from 12ohm to 33ohm but location do not change	According to the Intel Design Guide the clock USB_48MHz should serial a 33ohm resistor	P13	04-12-13	X1.1A->X02
2. Add pull up resistor R293 to KSI_USER	This signal is high level voltage valid and should pull up so that the EC do not submit miss order	P28	04-12-13	X1.1A->X02
3. ADD R374	For cost down concern (after test verify try to remove Q21)	P30	04-12-13	X1.1A->X02
4. Change R373 net connect	EC Team suggest change the schematic for cost down (after test verify try to remove U30)	P30	04-12-13	X1.1A->X02
5. Delete:U6,Q16,Q35,R219,R28,R168,R341,R372,R29,R163,C391,C396,C416, C417,C361,C386,C264,C387,C80,C84,C418	After verify the AU6369 function and delete this USB SD controller interface	The page have been deleted	04-12-13	X1.1A->X02
6. Change USB5+_ net to NC	Due to the USB5+_ net connect to AU6369 and should delete together with AU6369	P18	04-12-13	X1.1A->X02
7.Delete: R180,R207,R389,R391,R393,R395,R397,R399,R401	Due to these select resistor only connect SD controller AU6369 to SD card socket and should delete together with AU6369	P21	04-12-13	X1.1A->X02
8.Add R298,R341,R273,R372	1.Add R298 to pin1:STAC9758 need connect to GND but STAC9200 NC; 2.Add R341to pin4:STAC9758 need connect to GND but STAC9200 NC; 3.Add R273 to pin25:STAC9758 need connect to GND but STAC9200 NC. 4. Add R372 to pin40:STAC9758 need connect to GND but STAC9200 NC;	P25	04-12-13	X1.1A->X02
9.Delete R206,R208,R390,R392,R394,R396,R398	Because only use W83L528D as SD card controller and do not need this select resistor	P21	04-12-13	X1.1A->X02
10.Change U11 PCB Footprint from TPS2043A_SO16 to PI5V330Q_QSOP16	Because the material have change but the PCB Footprint error and need change	P15	04-12-13	X1.1A->X02
11.Add Bridge Battery Power net: Bridge_PWR	Layout request	P33	04-12-13	X1.1A->X02
12.Change JP32 pin31,pin32,pin33,pin34 from DUMMY to GND and add these pin define to the schematic	Layout request	P14	04-12-15	X1.1A->X02
13.Change JP15 pin21,pin22 from DUMMY to GND and add these pin define to the schematic	Layout request	P30	04-12-15	X1.1A->X02
14.Change JP14 pin23,pin24,pin25,pin26 from DUMMY to GND and add these pin define to the schematic	Layout request	P30	04-12-15	X1.1A->X02
15.Add CLK_PCIE_P2/N2 signal from U40 toDock; add the clock serial resistor R168, R163 and pull high resistor R180,R207	The new added pair PCIE need clock signal	P13/P32	04-12-15	X1.1A->X02
16.Add PCIE_RXN2,PCIE_RXP2; PCIE_TXN2,PCIE_TXP2 from ICH6 to DOCK	DOCK board need add one pair PCIE signal for transmit and receive	P18/P32	04-12-15	X1.1A->X02
17.Change the H2,H6 PCB footprint from H_S315D110 to H_S354B315D110	Layout request	P7	04-12-15	X1.1A->X02
18.Change the H7,H8,H9,H10 PCB footprint from H_S315D154 to H_S315B184D154	Layout request	P7	04-12-15	X1.1A->X02
19.Change the H11 PCB footprint from H_S276D98 to H_T138B275D98	Layout request	P7	04-12-15	X1.1A->X02
20.Change the H16 PCB footprint from H_S276D150 to H_S276D98	Layout request	P7	04-12-15	X1.1A->X02
21.Add H18	Layout request	P7	04-12-15	X1.1A->X02
22.Change SRCCLKT5/SRCCLKT5# net name from SRC6/SRC6# to SRC5/SRC5#	Net name not match and need change	P13	04-12-15	X1.1A->X02
23.Change SRCCLKT6/SRCCLKT6# net name from SRC5/SRC5# to SRC6/SRC6#	Net name not match and need change	P13	04-12-15	X1.1A->X02
24.Add FD1,FD2,FD3,FD4,FD5,FD6,FD7,FD8	Per DFX and SMT engineer request	P7	04-12-15	X1.1A->X02
25.Change JP5 pin16,pin17 from DUMMY to GND and add these pin define to the schematic	Layout request	P15	04-12-16	X1.1A->X02
26.Change PJPD1 pin4,pin5 from DUMMY to GND and add these pin define to the schematic	Layout request	P34	04-12-16	X1.1A->X02
27.Change PCIE_TXP2 from JP29.22 to JP29.16	Layout request	P31	04-12-16	X1.1A->X02
28.Change PCIE_TXN2 from JP29.24 to JP29.18	Layout request	P31	04-12-16	X1.1A->X02
29.Change PCIE_RXP2 from JP29.28 to JP29.22	Layout request	P31	04-12-16	X1.1A->X02
30.Change PCIE_RXN2 from JP29.30 to JP29.24	Layout request	P31	04-12-16	X1.1A->X02
31.Change CLK_PCIE_P2 from JP29.22 to JP29.28	Layout request	P31	04-12-16	X1.1A->X02
32.Change CLK_PCIE_N2 from JP29.22 to JP29.30	Layout request	P31	04-12-16	X1.1A->X02

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HW P.I.R LIST DVT1

Change item	Change reason	Page#	Date	Revision
33.Change JP15 P/N fom SP010002100 to SP010002800	Material P/N error according to EVT2 BOM	P30	04-12-18	X1.1A->X02
34.Add WL_BTN pull high resistor R380 to +3VS	Because the WL_BTN signal is low voltage valid and need pull high to prevent the signal misact	P28	04-12-18	X1.1A->X02
35.Change R329 pull up power plane from +3VS to +3VALW	After verify this action can solve the LCD flash when the AC adaptor plug in issue	P14	04-12-18	X1.1A->X02
36.Change LAN_WAKE pull up resistor R183 value from 5.1Kohm to 1Kohm and do not change the location	Meet Intel specification	P18	04-12-18	X1.1A->X02
37.Add Q35 to control the PQ23, PQ26 gate through PRSNT2# control Q35's gate	Solve the DOCK_IN power work abnormal issue	P32	04-12-18	X1.1A->X02
38.Change the C366 value from 0.22U to 2.2U and the location do not change	To improve the INT_MIC1 tone quality	P30	04-12-20	X1.1A->X02
39.Add R206,C144	To improve the INT_MIC1 tone quality	P30	04-12-20	X1.1A->X02
40.Add ICH_SMBDATA and ICH_SMBCLK to DOCK	DOCK test board new design need add this signal	P32	04-12-20	X1.1A->X02
41.Add ,R215R467,R468,C84,C97,C98,JP8,Q36,D13	To solve the EAX00 thermal issue	P20	04-12-22	X1.1A->X02
42.Change PM_BATLOW# signal connection from KB910L pin80 KB910L pin44	Need KB910L pin80 to control FAN circuit	P28	04-12-22	X1.1A->X02
43.Change WL_BTN# signal connection from KB910L pin33 to pin102	Need these KB910L pin33 to control FAN circuit	P28	04-12-22	X1.1A->X02
44.Add FAN_SPEED2 signal to 910L pin33/910Q pin176	The FAN need speed feedback signal to let EC know the FAN speed	P28/P29	04-12-22	X1.1A->X02
45.Add EN_DFAN2 signal to 910L pin80/910Q pin102	The EC need a FAN enable signal to control FAN speed	P28/P29	04-12-22	X1.1A->X02
46.Change U4 P/N from SA06509000L to SA065090000	The material need change from for Dell only to normal material	P6	04-12-22	X1.1A->X02
47.Change U1 P/N from SA805360220(1.1G) to SA000008800(1.2G)	New material try run	P5/P6/P7	04-12-22	X1.1A->X02
48.Change WL_BTN#,KSI_USER#,GATEA20,KBRST# pull high power plane from +3VS to +3VALW	Meet the EC specification	P28	04-12-22	X1.1A->X02
49.Change DOCK CRT net name from 3VDDCDA/3VDDCCL to 3VDDCDA_R/3VDDCCL_R	DOCK test board new circuit design need change these signals net name to match the circuit	P15/P32	04-12-22	X1.1A->X02
50.Add CLKREQ# signal from DOCK new card to U40 pin33 (SRCCLKT6/CLKREQA#) and add this signal serial resistor R208 and pull high resistor R216	The DOCK new card need this signal to request clock generator submit clock signal to new card	P13/P32	04-12-22	X1.1A->X02
51.Change the SD connector from SP07M001500(14pin) to SP070005P00(16pin)	Old SD connector do not support SDIO and need change to new connector to support SDIO	P21	04-12-22	X1.1A->X02
52.Delete Q35;add Q40,Q41,R389,C99	Solve the DOCK power control MOS Q35 no control function issue	P32	04-12-22	X1.1A->X02
53.Delete the R400	It is used to select W83L528D signal WR_PT# in EVT2, should delete because the AU6369 is removed	P21	04-12-22	X1.1A->X02
54.Add U40 pin56 PCICLK2/SEL_CLKREQ pull high select resistor R217 or pull down select resistor R209	The PCICLK2/SEL_CLKREQsignal need double check and we keep this two selection	P13	04-12-22	X1.1A->X02
55.Delete the HOT_PLUG control signal	The signal HOT_PLUG do not use and the GPIO pin can be used for other function	P28/P29	04-12-22	X1.1A->X02
56.Move signal EC_DIS_INTMIC from KB910L pin35 to pin49	KB910L pin35 need reserver for other function	P28	04-12-22	X1.1A->X02
57.Move signal EC_DIS_INTMIC from KB910Q pin43 to pin4	Match the KB910L and KB910Q pin definition	P29	04-12-22	X1.1A->X02
58.Add signal EC_RXD to KB910L pin35 and KB910Q pin106	Add this signal for EC test	P28/P29	04-12-22	X1.1A->X02
59.Move DREF_SSCLK/SSCLK# from U40 pin17/18 to pin22/23	Layout requestion	P13	04-12-22	X1.1A->X02
60.Move CLK_MCH_3GPLL/3GPLL# from U40 pin19/20 to pin17/18	Layout requestion	P13	04-12-22	X1.1A->X02
61.Move CLK_PCIE_ICH/ICH# from U40 pin33/32 to pin19/20	Layout requestion	P13	04-12-22	X1.1A->X02
62.Move CLK_PCIE_P2/N2 from U40 pin24/25 to pin26/27	Layout requestion	P13	04-12-22	X1.1A->X02
63.Add L32,C361,C229	To improve the INT_MIC1 tone quality	P30	04-12-23	X1.1A->X02
64.SD card controller signal SDD3 need pull up to +3VS	According to the W83L528D new version design guide need add this pull high resistor connect to +3VS	P21	04-12-23	X1.1A->X02
65.Change R376,R378 resistance from 47Kohm to 4.7Kohm	According to the W83L528D new version design guide need change R376 and R378 resistance	P21	04-12-23	X1.1A->X02
66.Add R218,R219 to control W83L528D power plane select	Use these two resistor to control W83L528D power plane select and will verify the SD card function in DVT1	P21	04-12-23	X1.1A->X02
67.Add R220,R293 to control CARD_DET_W# pull up power plane selection	Use these two resistor to control CARD_DET_W# pull up power plane select and will verify the SD card function in DVT1	P21	04-12-23	X1.1A->X02
68.Add pull up resistor R394 to U41 pin61	According to the W83L528D new version design guide need add this resistor to pull high U41 pin61	P21	04-12-23	X1.1A->X02

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HW P.I.R LIST DVT2

Change item	Change reason	Page#	Date	Revision
1. Delete C35	According to Power consideration that how many bulk caps of bulk caps needed depend on the measurement of load-line and power team suggest to delete C35 after test verify.	P7	05-01-04 DVT1 MEMO CHANGE	X02->X3.0
2. Change net DREF_SSCLK connect from R118.2 to R113.2; Change net DREF_SSCLK# connect from R120.2 to R115.2; Change net CLK_MCH_3GPLL connect from R113.2 to R118.2; Change net CLK_MCH_3GPLL# connect from R115.2 to R120.2	According to Intel Datasheet 915g_gv_gl_p the clock signal CLK_MCH_3GPLL/3GPLL# should sync with SRCCLK and CV140 pin17/18 is LVDS signal and not sync with SRCCLK, so need change the relative signal connection.	P13	05-01-07	X02->X3.0
3. Change GATE20 and KBRST# pull up power plane from +3VALW to +3VS	According to Intel ICH6 datasheet the ICH6 signal A20GATE and RCIN should connect to +3VS so that S3cold and S4/S5 can work normally	P28	05-01-07	X02->X3.0
4. Change L12,L13,L14 value from 80 Ohm@100MHz to 11 Ohm@100MHz; Change C164,C165,C166 value from 10pF to 6.8pF	After test verify the VGA RGB filter component value change can improve the VGA signal quality	P15	05-01-18	X02->X3.0
5. Change R389 resistance from 100Kohm to 300Kohm and the location not change; Add R395 to add another control selection and this resistor can keep DEPOP; Add PR176 to load voltage for the Q42 gate open or close	This design change can solve the DOCK power control circuit can not work normally issue after test verify.	P32	05-01-20	X02->X3.0
6. Change SRC3/SRC3# net name to SRC4/SRC4#	Net name not match the clock generator pin name and need change	P13	05-01-20	X02->X3.0
7. Change board ID from version2(for DVT1) to version3(for DVT2)	New version build need change new board ID control	P29	05-01-20	X02->X3.0
8. EC part: Change signal PSCLK1 net name to WLAN_LINK_WL, Change signal PSDAT1 net name to WLAN_ACTIVE_WL, Change signal PSCLK2 net name to WLAN_LED; MiniPCI conn JP27 part: pin11 net name change from WL_LED to WL_ACTIVE_WL; pin12 connect to WL_LINK_WL; SW/LED conn JP14: pin10 net name change from WL_LED to WLAN_LED.	Solve the Wireless LAN LED does not operate properly issue	P28/P29/ P30	05-01-24	X02->X3.0
9. U41pin61 signal XDPWR# add pull down resistor R396	Add MMC select solution: signal XDPWR# pull up support MMC; signal XDPWR# pull down disable MMC	P21	05-01-24	X02->X3.0
10. Change signal EXTROMSEL# pull up (R381) or pull down (R382) select resistor resistance from 100K to 4.7K ohm and the location do not change	According to the W83L528D B version design guide need change these resistor resistance (signal EXTROMSEL# pull up select EEPROM;signal EXTROMSEL# pull down do not select EEPROM)	P21	05-01-24	X02->X3.0
11. Change R377 resistance value from 47K to 4.7Kohm	According to the W83L528D B version design guide need change these resistor resistance	P21	05-01-24	X02->X3.0
12. Add D14,D15,D16,D17 as USB port0 and port1 signal Switching diode	USB signal need add Switching diode to keep it in a stable voltage range when the USB device plug or evulse.	P27	05-01-26	X02->X3.0
13. Delete KB910Q	After confirm with customer delete the KB910Q and only use KB910L in DVT2	The page have been deleted	05-02-04	X02->X3.0
14. Add +3VS power to DOCK conn(JP29 PIN10)	LS2584 quick switch need +3VS power supply	P31	05-02-04	X02->X3.0
15. Add Q16,R260,R285,C159; change DISPOFF# pull up power plan from +3VALW to +3VS	Solve the LCD flash when plug in AC addaptor issue	P14	05-02-19	X02->X3.0
16. Add L19 and this location not populate	For save power consumption and cost down concern	P25	05-02-20	X02->X3.0
17. 1. Change C161, C162, C163 value from 22PF to 10PF 2. Change C164, C165, C166 value from 6PF to 10PF 3. Change L12, L13. L14 value from 11ohm@100MHz to 40ohm@100MHz 4. Change REFSET pull down resistor from 255ohm to 232ohm	According to Customer test this change can improve the VGA signal quality	P15/P10	05-03-08	X02->X3.0
18. 1. Change C306/C307 value from 1uF to 0.1uF 2. Change R249 value from 34.8Kohm to 20Kohm 3. Change R250 value from 1Kohm to 20Kohm 4. Add C348&C386 and do not populate in DVT2	After test verify the circuit change can improve the speaker volume	P26	05-03-08	X02->X3.0
19. Add Q35, R399 to switch DOCKEN signal to CLKREQB# used as quick switch control and Giga LAN clock request signal	Add quick switch to solve the USB show over current message when plug DOCK test board issue, need add thissignal to control quick switch; BIOS asked add clock request function for Giga LAN.	P13/P15/ P28/P31	05-03-08	X02->X3.0
20. Add 5.1Kohm pull down resister on MB,1Kohm pull up to VDDA on Dock	Sync with Pecos design change	P31	05-03-09	X02->X3.0
21. Add JP25 on MB	Add thermal sensor to monitor the HDD temperature and connect the sensor signal through FFC to MB connector	P20	05-03-10	X02->X3.0
22. Dispart MB/DOCK co-use signal HP_OUT_L/R 1. U22 pin39/41 as MBHP_OUT_L/R connect to MB HP OUT/MIC IN 2. U22 pin35/36 as DOCKHP_OUT_L/R connect to DOCK HP OUT/MIC IN and add 0ohm resister R286,R287,R288,R398 3. Signal DOCK_MIC connect to U22 pin18/19 and add C387	Reserve FRONT_L/FRONT_R for Dock Headphone.	P25	05-03-12	X02->X3.0
23. Add PJP14 and not populate in DVT2	Reserve for cost down	P31	05-03-12	X02->X3.0
24. Add F1	Compal safty engineer request	P15	05-03-15	X02->X3.0
25. Add Q44, Q48, R400, C264, PJP19	Control LAN power gate to reduce power consumption	P23	05-03-15	X02->X3.0
26. Add Q45, Q46, R401, C416, PJP17	Control Wirelesse LAN power gate to reduce power consumption	P22	05-03-25	X02->X3.0

HW P.I.R LIST DVT2

Change item	Change reason	Page#	Date	Revision
27. Add Q42, Q47, R402, R403, R404, C417, PJP18	Control BT power gate to reduce power consumption	P22	05-03-15	X02->X3.0
28. Add Q49. Q50, R405, C418, PJP20	Control SD chip power gate to reduce power consumption	P21	05-03-16	X02->X3.0
29. Chang C172, C173 value from 12pF to 15pF	After verify this action can solve the RTC time issue	P17	05-03-17	X02->X3.0
30. +5VS power plane add C69 (220uF); delete C395(10uF)	Solve trinity cold dock re-booting issue	P32	05-03-17	X02->X3.0
31. Add C406	According to the W83L528D B version design guide need use XDLED as SD LED signal	P21	05-03-17	X02->X3.0

HW P.I.R LIST PVT

Change item	Change reason	Page#	Date	Revision
1. Delete D14, D15, D16, D17; Add D25, D26 (Change material)	To improve USB ESD protect	P27	05-04-25	X3.0->X4.0
2. Add R407, R408	Solve the signal Digi_FWE leak power issue	P14	05-04-25	X3.0->X4.0
3. Add Q51, Q52, R410, R411	Solve battery can not charge normally when system is shut down issue. (Because the HDD thermal monitor used SMBus is same as battery SMBus --> SMB_EC_CK1/DA1, when the system is shut down the HDD thermal monitor cause the battery SMBus error)"	P20	05-04-25	X3.0->X4.0
4. Add R409 connect PCI_AD18 to IDSEL16	BIOS team can control this signal directly	P22	05-05-25	X3.0->X4.0
5. Change Q16 power from +LCDVDD (3V) to +5VS	Solve Q16 can not fully turn on issue	P14	05-04-29	X3.0->X4.0
6. Add U39, R412	For save SD controller power consumption concern (when do not use SD card to cut off the signal CLK_PCI_SD to SD controller chip can save much SD controller power consumption)	P21	05-05-06	X3.0->X4.0
7. Delete Q48, R400, C264, Q44;Add Q54, R414, R421, C424, Q55; U17, R274	To improve LAN power consumption function	P23	05-05-06	X3.0->X4.0
8. Add R419, R415 to control VDDA power; Add PJP21, Q53, Q56, R413, R417, C419 to control +3VS_VDDC power; Add U25, R416 to control signal AC97_RST#	For save Audio power consumption concern	P25	05-05-06	X3.0->X4.0
9. Change U24 power from VDDA to +5VALW	Solve signal MUTE#/HP_PLUG# leak power to VDDA issue	P26	05-05-06	X3.0->X4.0
10. Add Q44, R418, C101, PR179	Solve gain chager can not chager issue	P31	05-05-09	X3.0->X4.0
11. Add R395, C230	To improve this signal quality	P15	05-05-09	X3.0->X4.0
12. Add C391, C231, C234, C33, R420 and change C349 value from 0.22U to 2.2U	To improve this signal quality and balance it with INT_MIC1	P29	05-05-09	X3.0->X4.0
13. Add D27	Add ESD protect diode to prevent ESD damage EC	P14	05-05-09	X3.0->X4.0
14. Connect signal CARD_DET_W# from SD controller to EC (U27.48)	EC can use signal CARD_DET_W# to control SD controller	P21/P28	05-05-09	X3.0->X4.0
15. Delete Q45, Q46, R401, C416	Do not need this control circuit to control W/L power because cut off the W/L power can cause system hang up	P22	05-05-09	X3.0->X4.0
16. Add U28	To save power when system do not use TPM function	P28	05-05-09	X3.0->X4.0

HW P.I.R LIST MP

1. Delete: PJP20,Q50,Q49,R405,C418;Change all +3VS_SD to +3VS power plan	SD controller power save can be controlled by enable/disable SD clock and do not need this power control circuits	P21	05-05-27	X4.0->X5.0
2. Add R323	Reserver the 0ohm resistor for debug	P21	05-05-27	X4.0->X5.0
3. Swap CARD_DET_W_EC# from EC pin48 to EC PIN96	910L pin48 is HW strap pin, low active, SD card detect signal pull low this pin while boot so that make EC go into test mode.	P28	05-05-27	X4.0->X5.0
4. Connect JP29 un-connect pin to GND	Connect JP29 un-connect pin to GND can improve DOCK EMI.	P31	05-05-27	X4.0->X5.0
5. Delete: PJP14,PQ26,PQ23,PC162,PR187,PR163,R389,Q41,C99,PR176, Q40,Q44,C101,R418,PR179	After verify found these circuits no need.	P31	05-05-31	X4.0->X5.0
6. Change SRC5/5# control signal from CLKREQB# to CLKREQA#; Add R389, R405, R218; Swap JP29 CLKREQA# and CLKREQB# signal name for these two signal control function change.	Main source IDT CV140 SRC1~7/1~7# can control by CLKREQA# or CLKREQB#, MP use CLKREQA# control; 2nd source Silego SLG84443 SRC1,3,4/1#,3#,4# can control by CLKREQB# and SRC2,5/2#,5# can control by CLKREQA#.Use CLKREQA# control SRC5/5# can meet CV140 and SLG84443 specification.	P13/P15/P31	05-06-10	X4.0->X5.0
7. Add Q40	Found glitch on VRMPWRGD, so add MOS gating this glitch.	P18	05-06-13	X4.0->X5.0
8. Delete R218, R219	Winbond B2 and up no support standby power, all power pins are connected inner the chip, so delete standby power. And large power trace in the same time.	P21	05-06-13	X4.0->X5.0
9. Add R418	To improve the signal SDCLK quality	P21	05-06-13	X4.0->X5.0

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Change item	Change reason	Date	Revision
1. PC262 from SE071101K10 change to SE071101K00	SE071101K10 is A34 part.		
2. PR98 from SD034715200(71.5K) change to SD034137200(13.7K) Add PR182 SD034100300(100K)	Improve Vccp O.C.P to 8.5A.		
3. PR46 from SD014113100(1.13K) change to SD013820000(820) PR47 from SD014402000(402) change to SD014732000(732)	Improve +3VALW O.C.P to 6.2A		
4. PR50 from SD014113100(1.13K) change to SD034124100(1.24K) PR53 from SD014402000(402) change to SD014442000(442)	Improve +5VALW O.C.P to 7.2A		
5. PC53 from SE026474KT6(0.47uF)change to SE135105M00(1uF/16V) PR382 from SD028470200(47K) change to SD028220300(220K) Del PC54 SE033105Z08	Improve +5VALW/+3VALW turn on timing.		
6. PR190 from SD034324200(32.4K) change to SD034348200(34.8k) PC161 from SE074102K00(1000P/50V) change to SE025102K04(1000P/50V)	Improve charge current to 1.68A.		
7. Del PR377 SD034169200(16.9K),PR378 SD034100300(100K), PR379 SD028200400(2M),PR380 SD02847020(47K),PQ41 SB301150000(DTC115EA) Add PR394 SD0134702T5(47K)	Del Power CPU O.T.P circuit that H/W has built by U4 Max6509		
8. PC48 from SGA20151320(150U/18mOhm) change to SGA20221210(220U/25mOhm) PC51 from SGA20151320(150U/18mOhm) change to SGA20221210(220U/25mOhm)	SGA20221210 (220U/6V 25M OHM) cheaper than SGA20151320 (150u/6V 18m ohm)		
9. Del PR151 SD028000000	Improve charge voltage to 12.6V.		
10. PC61 from SE142475K00(4.7U/25V) change to SE114106K00(10U/6.3V) PC57 from SE142475K00(4.7U/25V) change to SE114106K00(10U/6.3V) PC58 from SE021226Z00(22U/16V) change to SE077226M10(22U/6.3V)	For cost down		
11. PR99 from SD034499000(449) change to SD034300000(300)	Improve VCCP voltage to 1.05V		
12. PU4 from SA000009700(SC1404) change to SA019020000(MAX1902) PR46 from SD013820000(820) change to SD014127100(1.27K) Add PC44 SE071470J00(47P/50V) Add PR48 SD034100400(1M) PR47 from SD014732000(732) change to SD014127100(1.27K) PC45 from SE135105M00(1U/16V) change to SE026474KT6(0.47U/16V) PR51 from SD028000000(0) change to SD028620000(620) Add PC47 SE071101J00(100P/50V) Add PR55 SD034332100(3.32K) Del PC261 SE068101K00(100P/25V) Add PR395 SD028100200(10K) PR59 from SD028100300(100K) change to SD028470200(47K) Del PR58 SD028200300(200K) Del PR67 SD028200400(2M) PC49 from SE074102K00(1000P/50V) change to SE074681K00(680P/50V) Del PR389 SD028000000(0) Add PR56 SD028000000(0) Add PC43 SE071470J00(47P/50V) Add PR49 SD034200400(2M) PR50 from SD034124100(1.24K) change to SD034154100(1.54K) PR53 from SD014442000(442) change to SD034698000(698) PC46 from SE135105M00(1U/16V) change to SE026474KT6(0.47U/16V) Add PC52 SE071101J00(100P/50V) Add PR57 SD028102200(10.2K) Del PC262 SE071101K00(100P/50V) Add PR396 SD028100200(10K) PC48, PC51 from SGA20221210(220U/25m) change to SG020151330(150U/45m) Add PR43 SD011220AT7(22) Add PC33 SE028471K01(470P/100V)	3V/5V/12V PWM IC from SC1404 change to MAX1902, need change these componemts	04-12-28	

PWR P.I.R LIST

Change item	Change reason	Date	Revision
13. PC48 from SG020151330(150uF/45mOhm) change to SGA20221210(220uF/25mOhm) PR55 from SD034332100(3.32K) change to SD000006500(3.16K)	To improve battery mode 3.3VALWP dynamic ripple voltage. (Cut in MAX1902 on DVT-1)	05-03-07	
14. PC51 from SG020151330(150uF/45mOhm) change to SGA20221210(220uF/25mOhm) PR57 from SD034105200(10.5K) change to SD034100200(10K)	To improve battery mode 5VALWP dynamic ripple voltage. (Cut in MAX1902 on DVT-1)	05-03-07	
15. PC32 from SE142475K00(4.7uF/1206) change to SE065106K00(10uF/1210)	To improve 12VALW boost ceramic capacitor PC32 4.7uf/25v 1206 resonance when battery light load.	05-03-07	
16. PR168 from SD014634200(63.4K) change to SD014562207(56.2K)	Battery cell capacity from 2400mAh change to 2600mAh that charge current need to modify from 1.68A to 1.8A.	05-03-10	
17. PR132 and PR129 from SD028300000(300/0603/5%) change to SD028560000(560/0603/5%)	For meet RTC battery charge current specification. (3.3V-0.2V-2V)/ 1.2K (560 ohm * 2) <=1mA	05-03-07	
18. PR17 from SD034499300(499K) change to SD034412300(412K) PR20 from SD034499300(499K) change to SD034634300(634K) PR25 from SD034191300(191K) change to SD034140300(140K)	To improve Bridge Battery turn off voltage from 6.5V to 5.5V	05-03-10	

PWR P.I.R LIST MP

1. PT1 from SH136100020 (N1:N2 =1:1.8) change to SH000004V80 (N1:N2 =1:2)	Reduce power consumption about 0.13W when battery only on S3 mode.	05-06-13	
2. PR119 pull high voltage source from +3VALW change to +3VS.	To solve VRMPWRGD 430mV of back drive with system off.	05-06-13	