

Desert Eagle  
LA-3161P

# Compal confidential

## HEL80/HEL81 Schematics Document

Mobile Yonah uFCPGA with Intel  
Calistoga\_GM/PM+ICH7-M

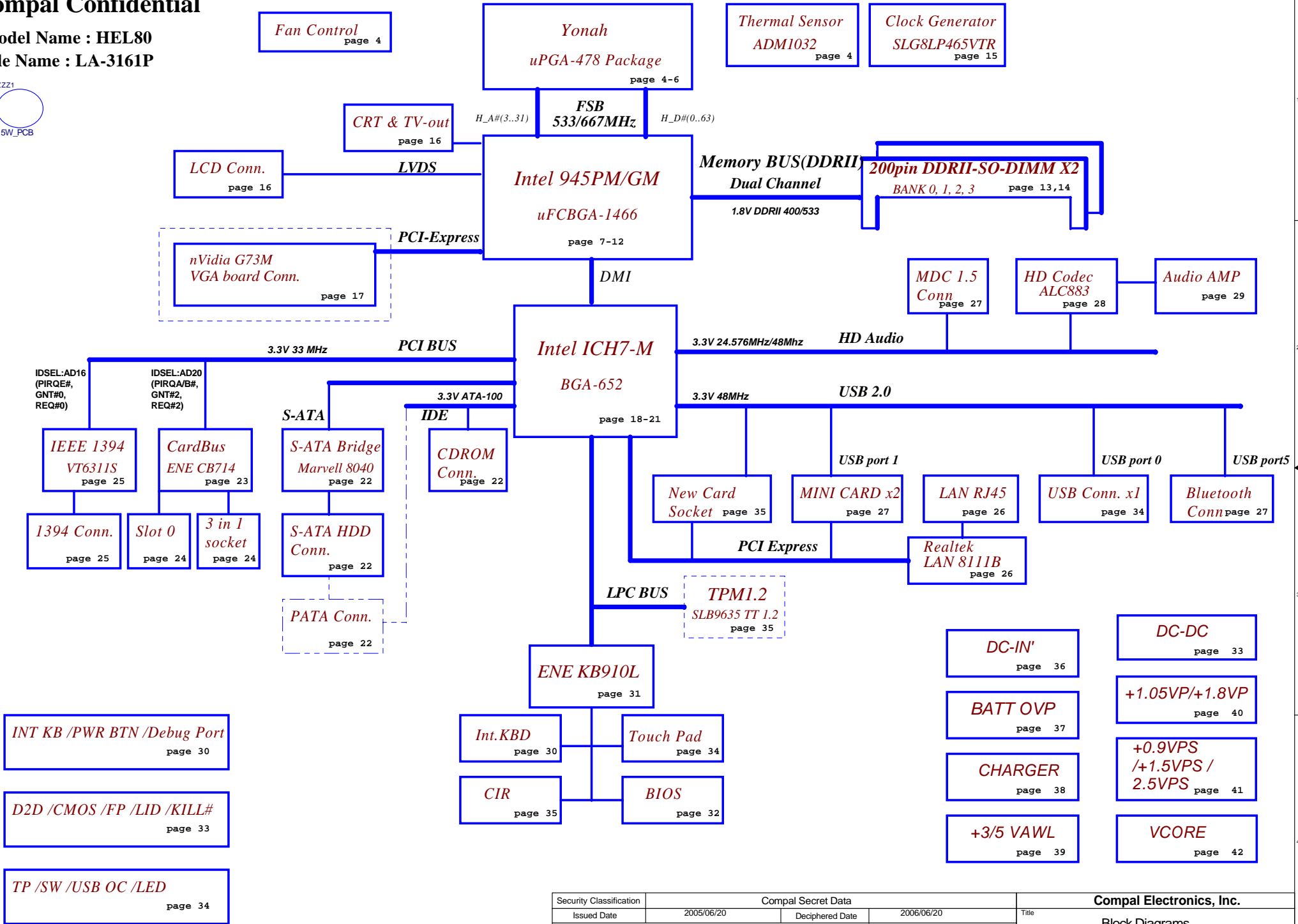
Thursday, February 23, 2006

REV:0.3

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Date:				Sheet 1 of 43		

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Model Name : HEL80  
File Name : LA-3161P



INT KB /PWR BTN /Debug Port  
page 30

D2D /CMOS /FP /LID /KILL#  
page 33

TP /SW /USB OC /LED  
page 34

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### Voltage Rails

power plane	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
state				
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

○ MEANS ON

✗ MEANS OFF

S3 : STR

S4 : STD

S5 : SOFT OFF

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/B
1394	AD16	0	PIRQE

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

### ICH7 SM Bus address

Device	Address
Clock Generator (SLG8LP465VTR)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

### SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	Vad_BID min	Vad_BID typ	Vad_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	HEL80/81 SKU
* 0	HEL80 SKU
1	HEL81 SKU
2	TEST MODE
3	
4	
5	
6	
7	

### BOM Structure

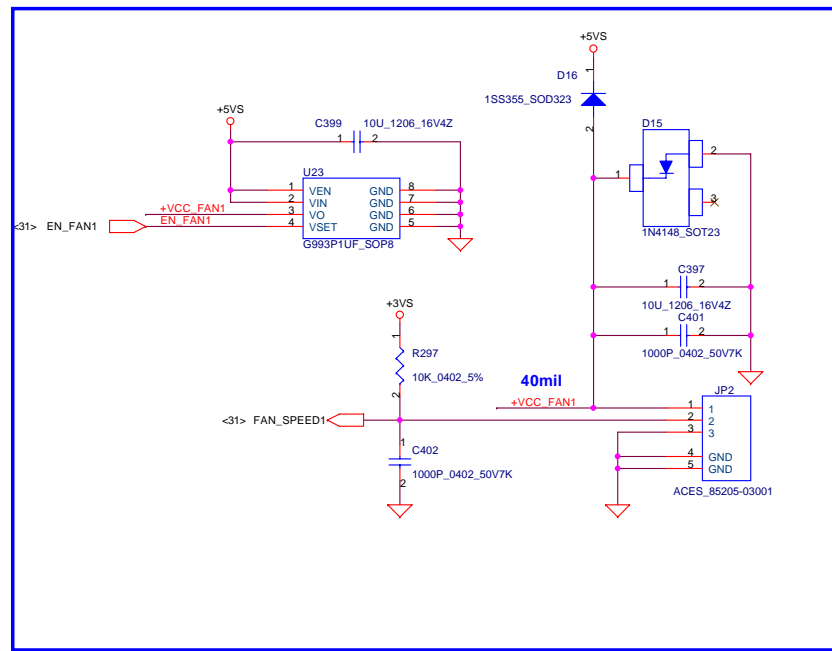
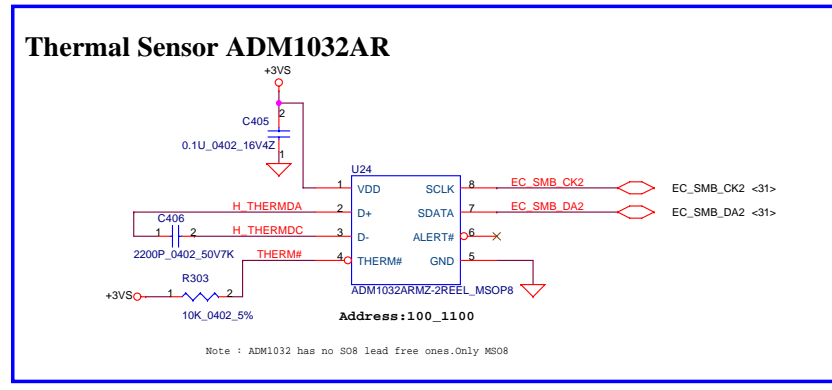
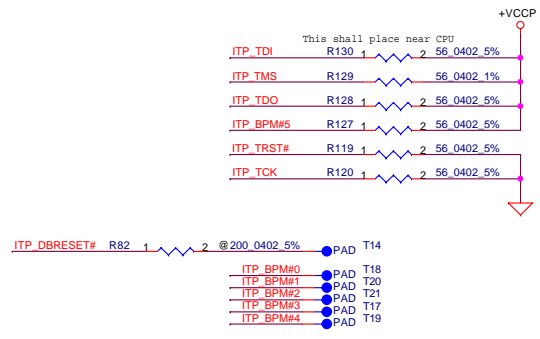
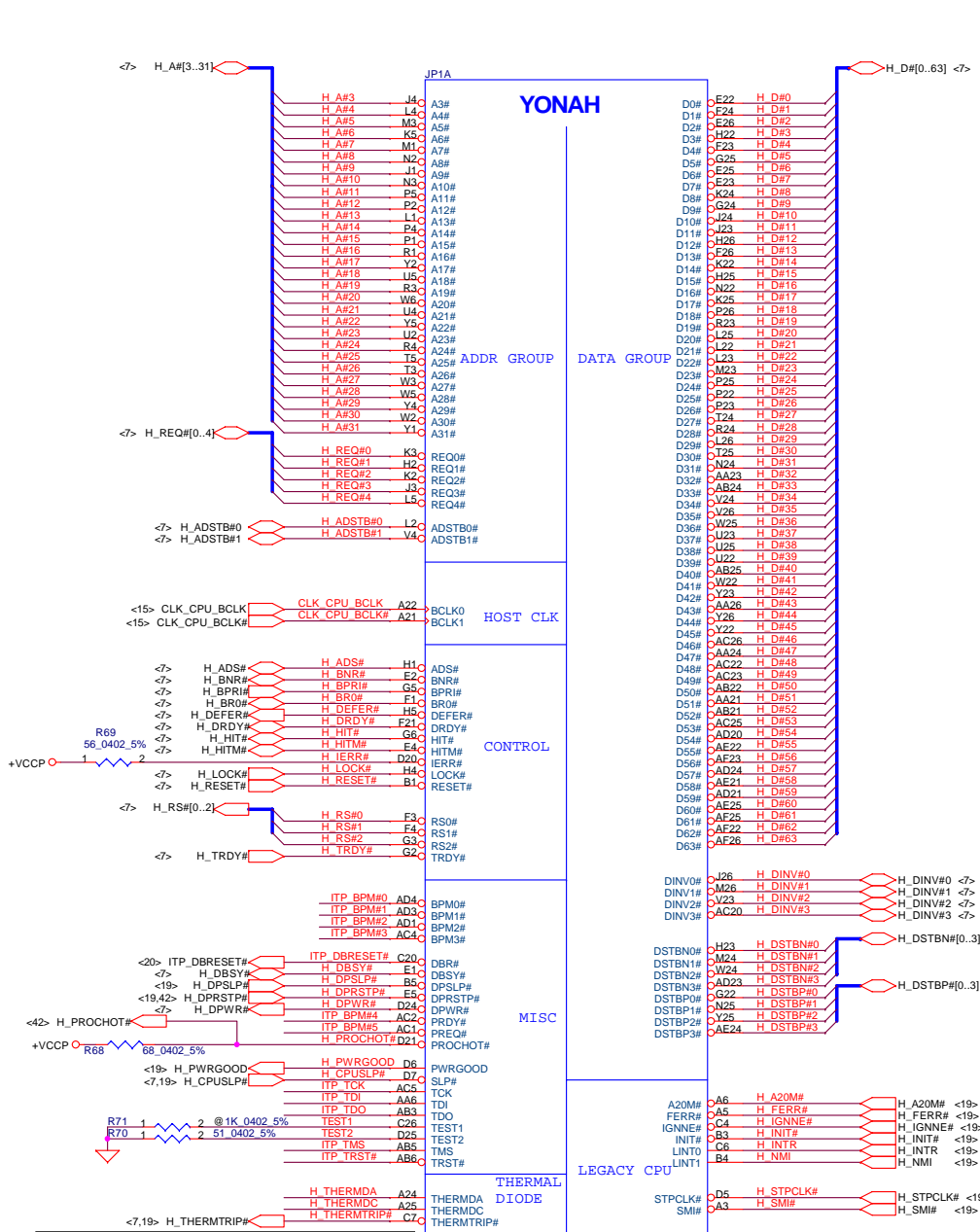
MARK	FUNCTION
@	NC FOR ALL
UMA@	Internal 945GM
VGA@	External G7xM
TPM@	TPM1.2
CIR@	CIR
1394@	1394
SATA@	SATA HDD
8040@	PATA HDD
IOMP@	IOMP
15W@	15W PANEL
APA@	HP out from AMP
HPA@	HP out from HP AMP
HP@	HP out from CODEC

### USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	NEW CARD
7	TV

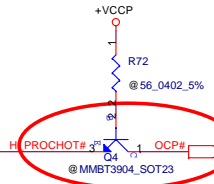
+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A(13.8A) 3.8A 1A 0.65A 2A

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**H\_THERMDA, H\_THERMDC routing together.**  
Trace width / Spacing = 10 / 10 mil

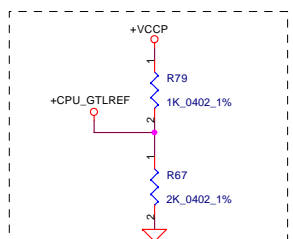
TYCO\_1-1674770-2\_Yonah-D  
ME@



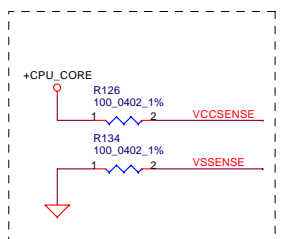
2005/1/07  
**Modified Q4 part number to SB03904000.**

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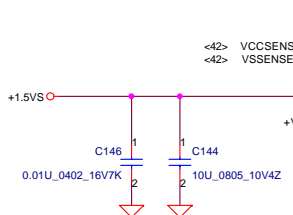
Compal Electronics, Inc.			
Title <b>Yonah CPU in mFCPGA479</b>			
Size	Document Number	Rev	
Custom	<b>HEL80 LA-3161P</b>	0.2	
Date:	Thursday, February 23, 2006	Sheet	4 of 43



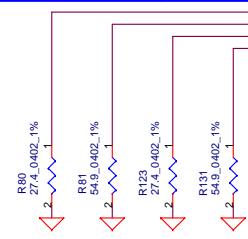
Close to CPU pin AD26 within 500mils.  
Trace / Width = 4 / 25 mils



Close to CPU pin within 500mils.  
Trace / Width = 18 / 50 mils

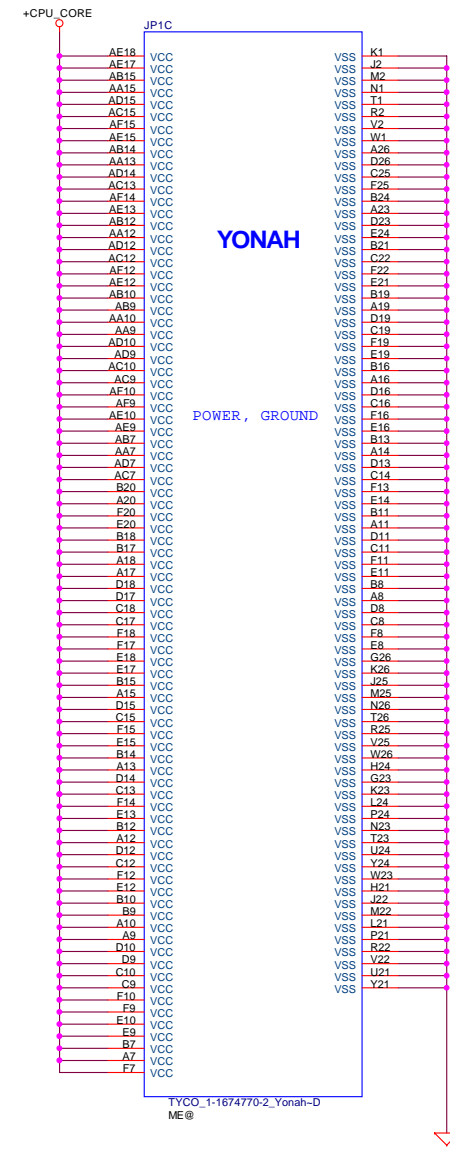
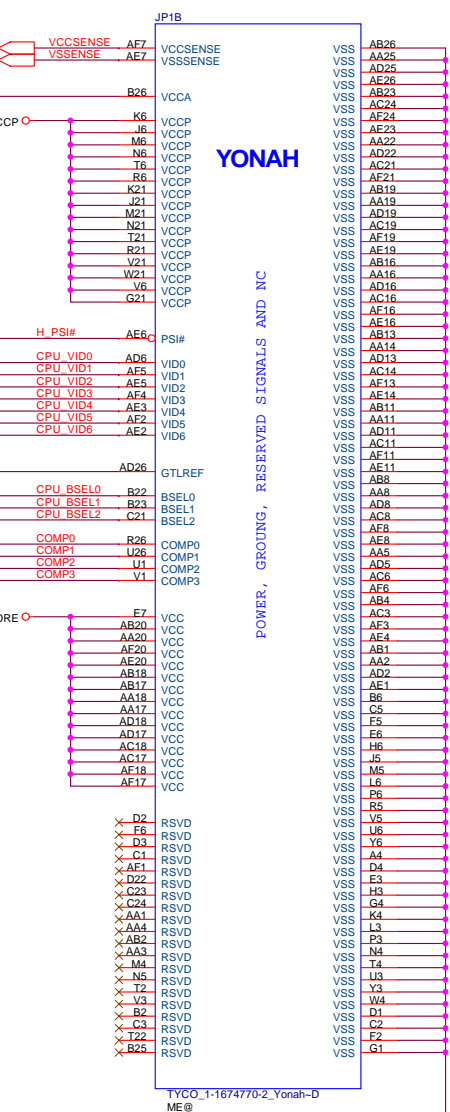


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

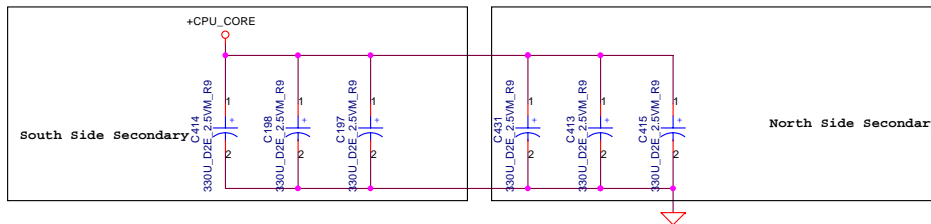
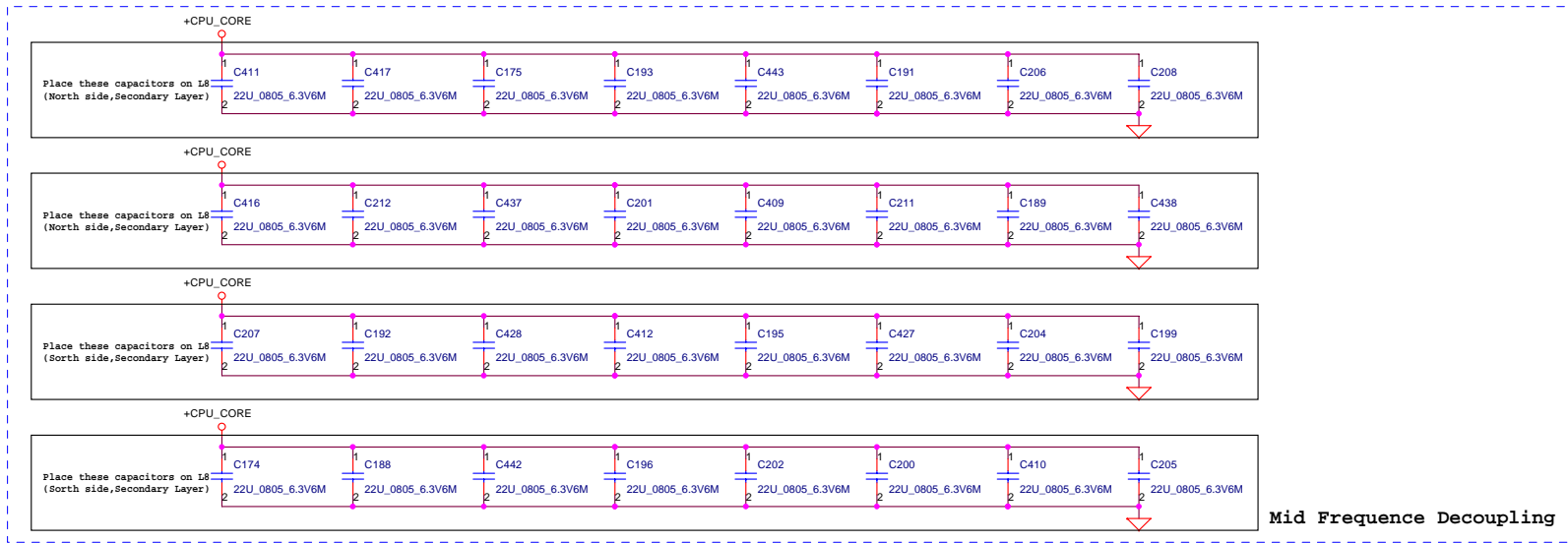
COMP 0/2 Trace / Width = 18 / 25 mils  
COMP 1/3 Trace / Width = 5 / 25 mils



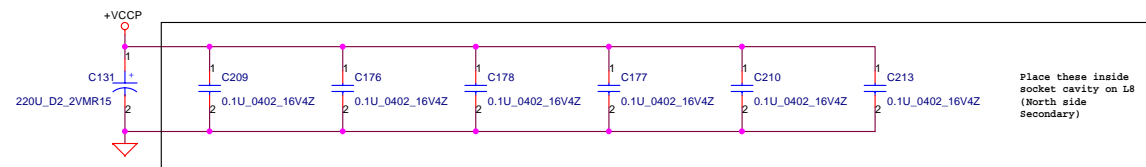
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Yonah CPU in mFCPGA479		
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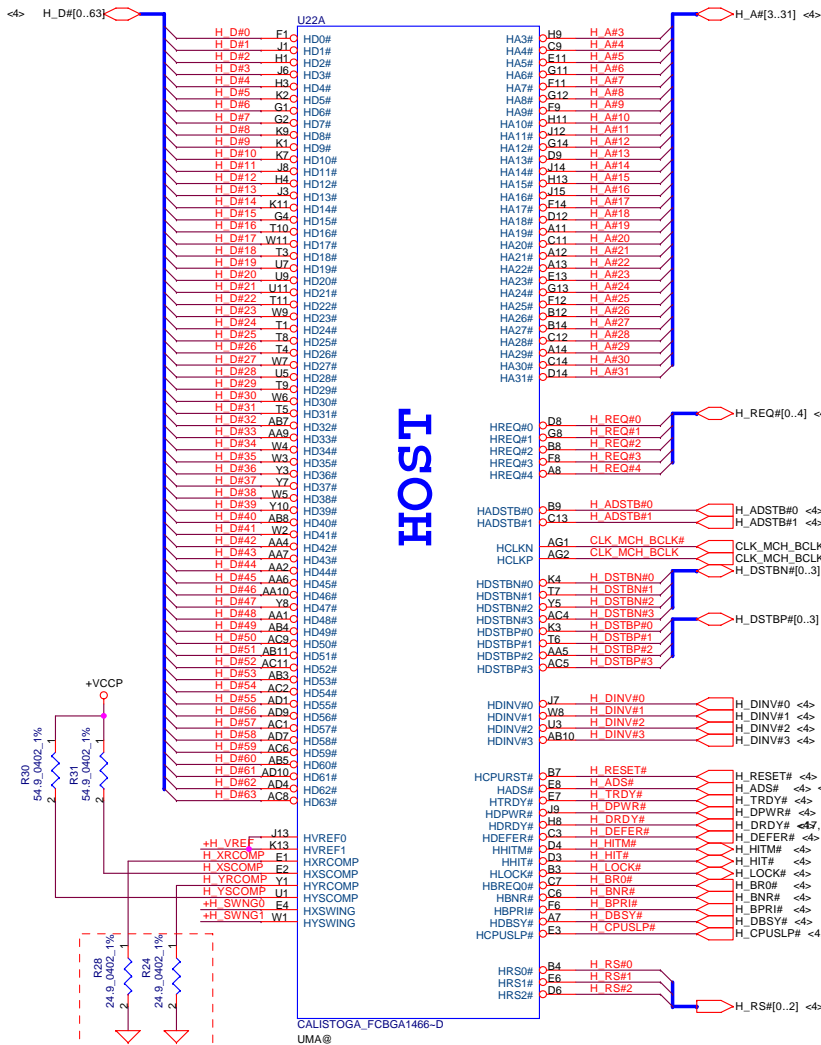
ESR <= 1.5m ohm  
Capacitor > 1980uF



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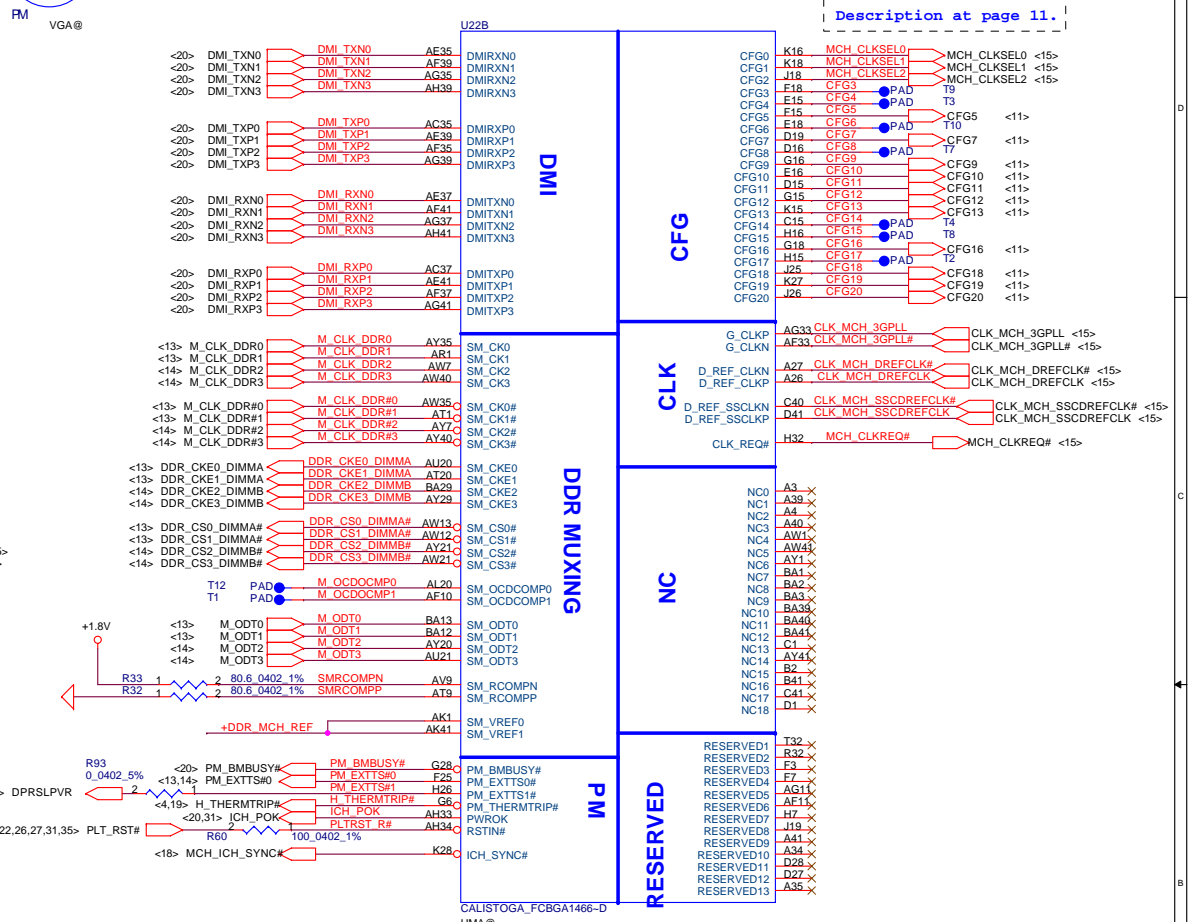
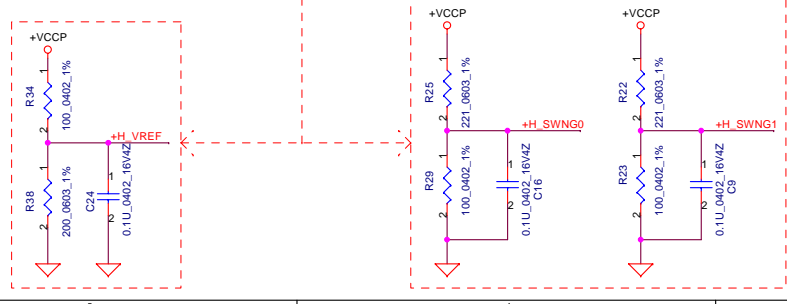
<b>Compal Electronics, Inc.</b>			
<b>CPU Bypass capacitors</b>			
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Note : 2005/12/26 modify pm  
 PM : SA00000KDC0  
 GM : SA0000059H0



HOST

Layout Note:  
 H\_XRCOMP / H\_YRCOMP / +H\_VREF / +H\_SWNG0 /  
 +H\_SWNG1 trace width and spacing is 10/20.

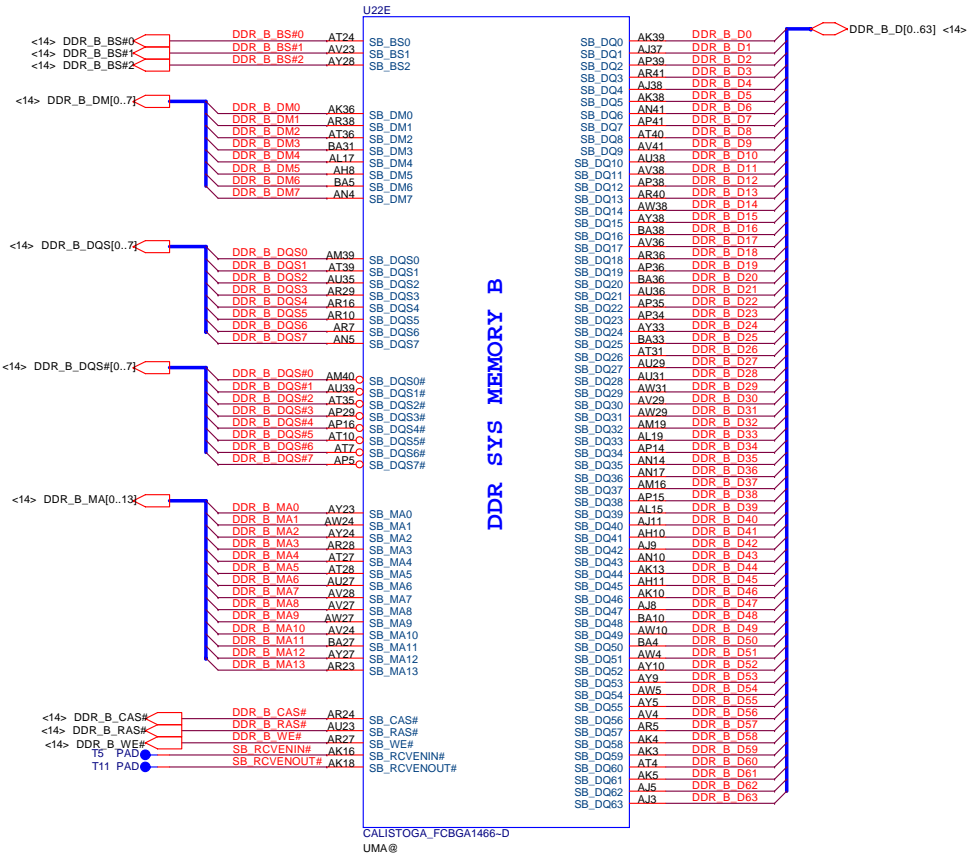
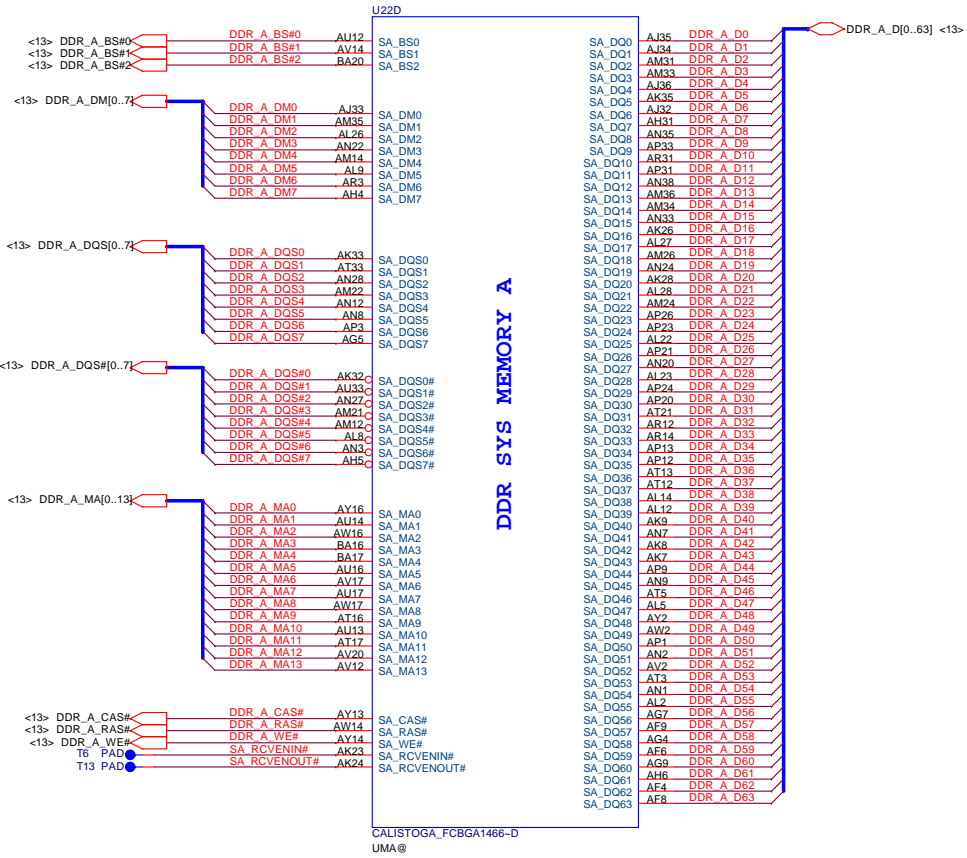


Layout Note:  
 +DDR\_MCH\_REF  
 trace width and  
 spacing is 20/20.



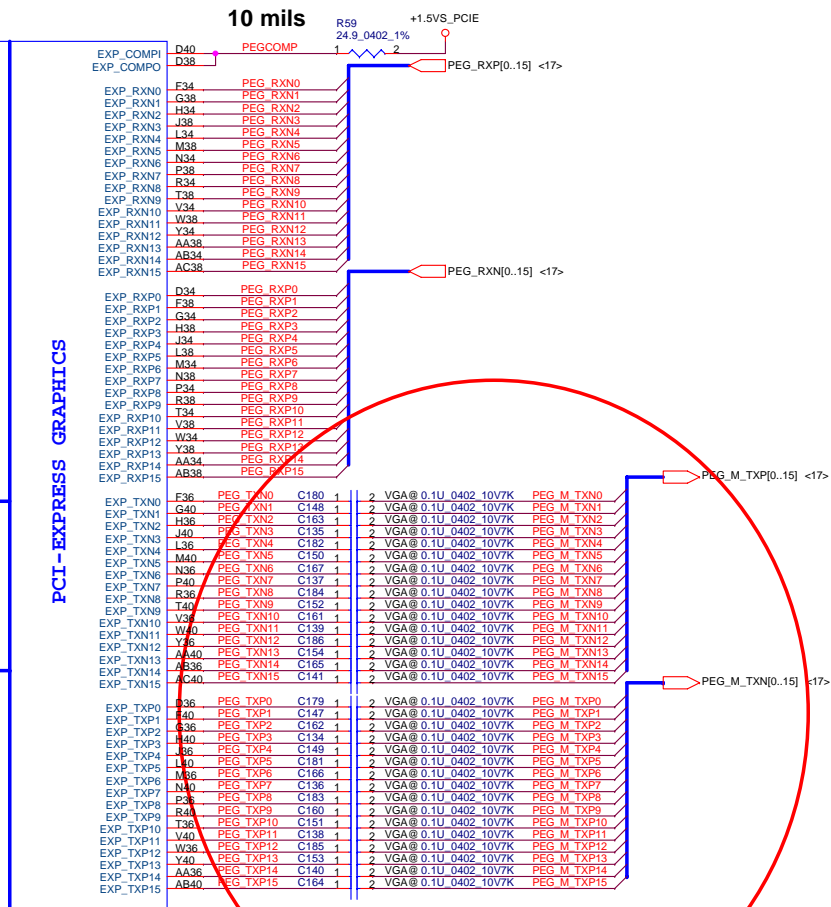
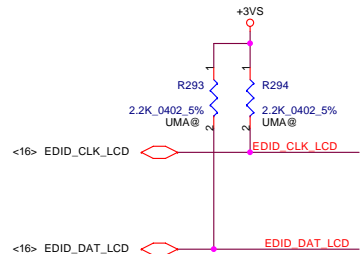
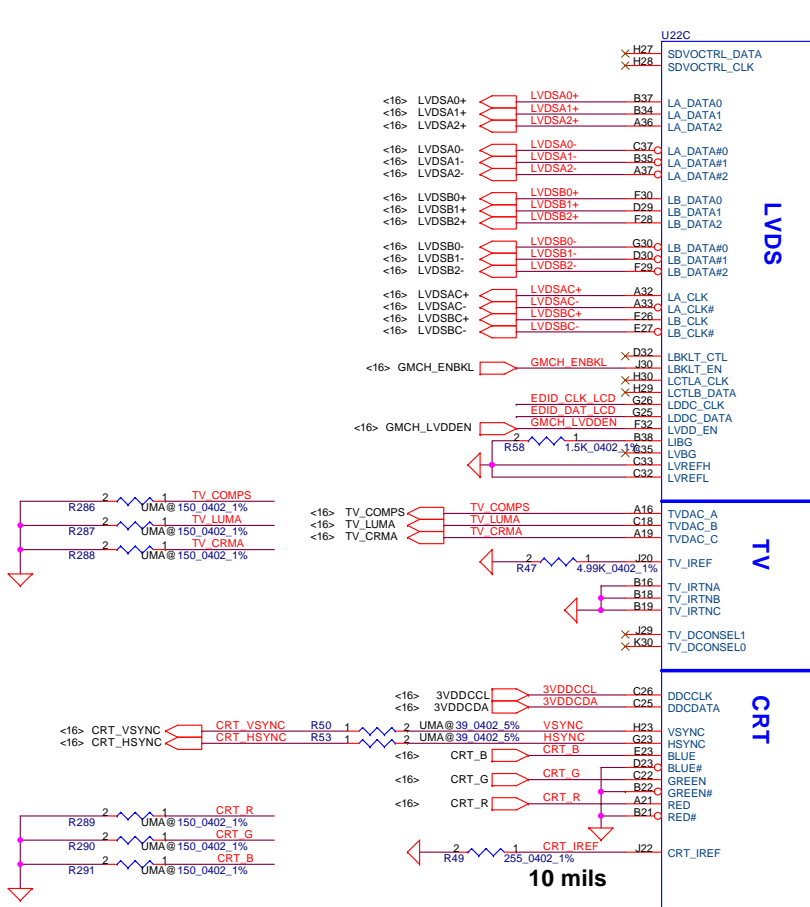
Description at page 11.

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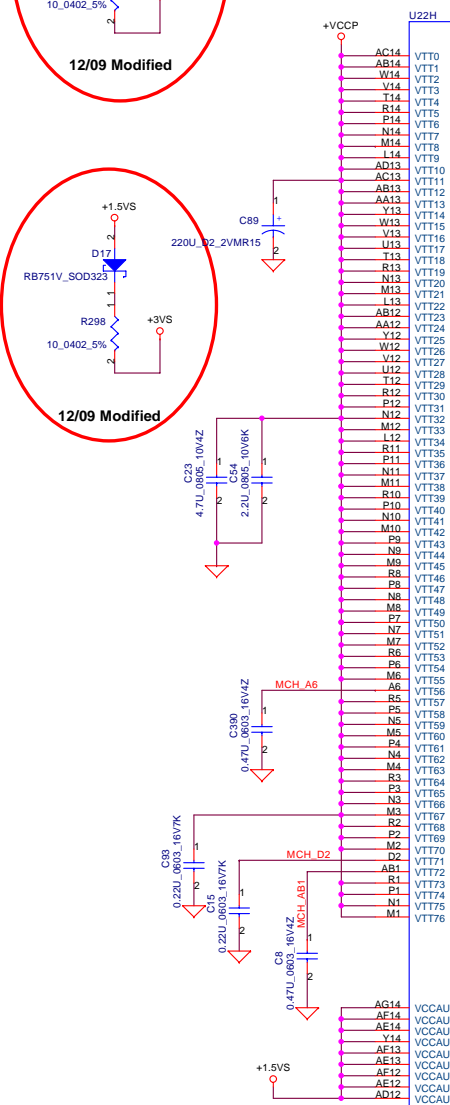
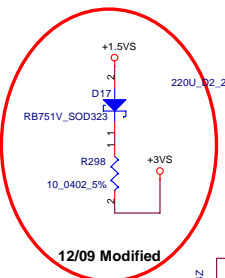
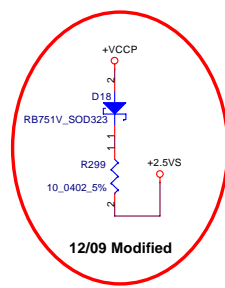




CALISTOGA\_FC8GA1466-D  
UMA@  
2/20 modified to 0402\_X7R

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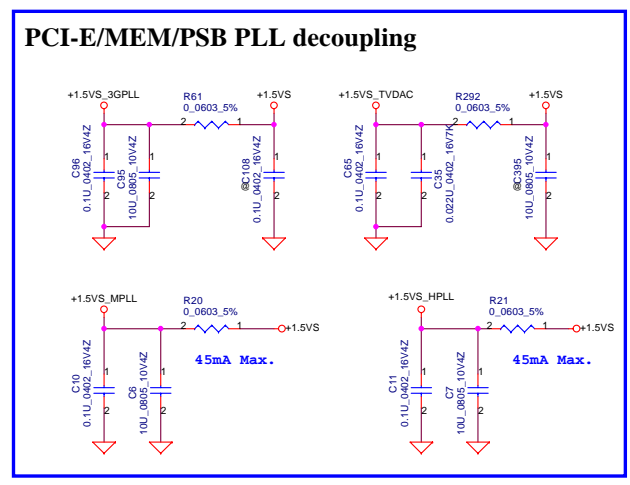
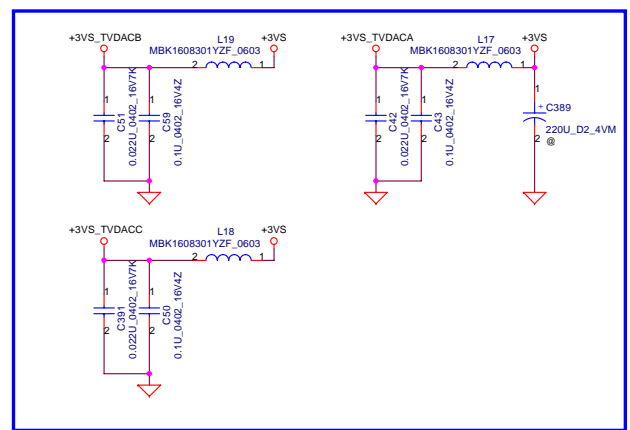
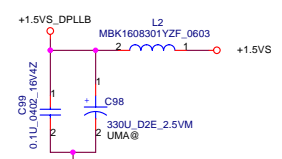
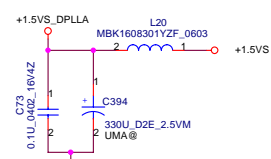
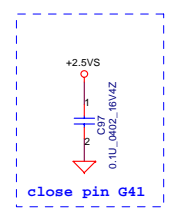
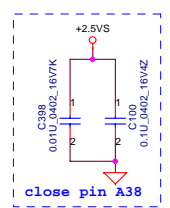
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**POWER**

W=60 mils

**CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga**



**PCI-E/MEM/PSB PLL decoupling**

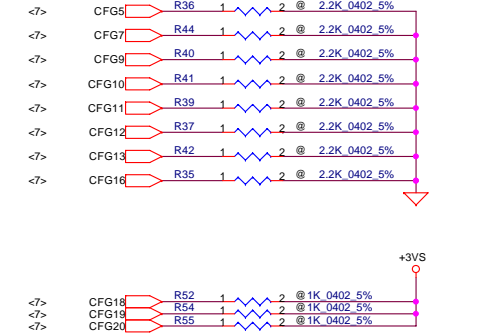
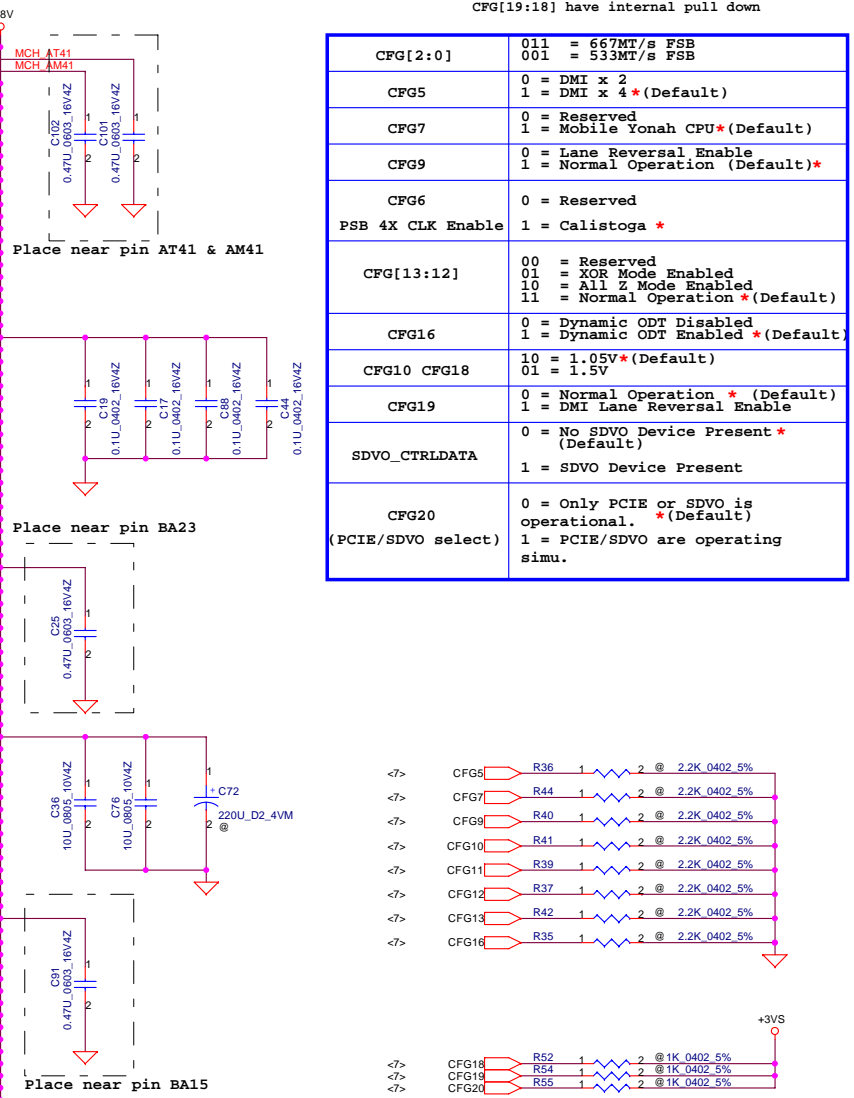
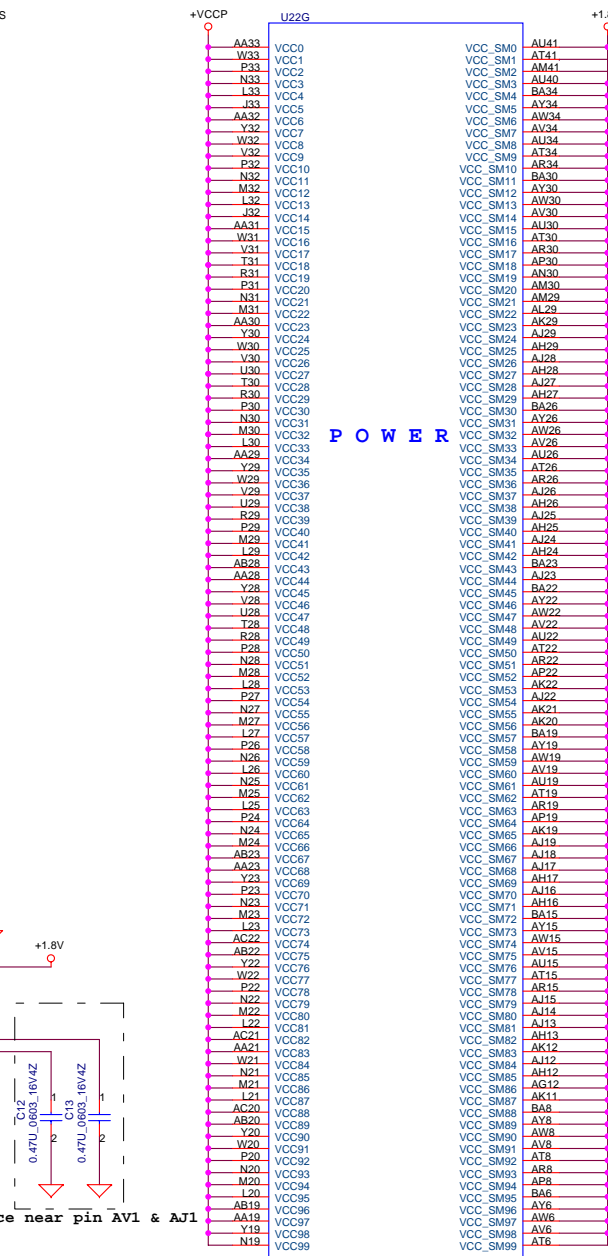
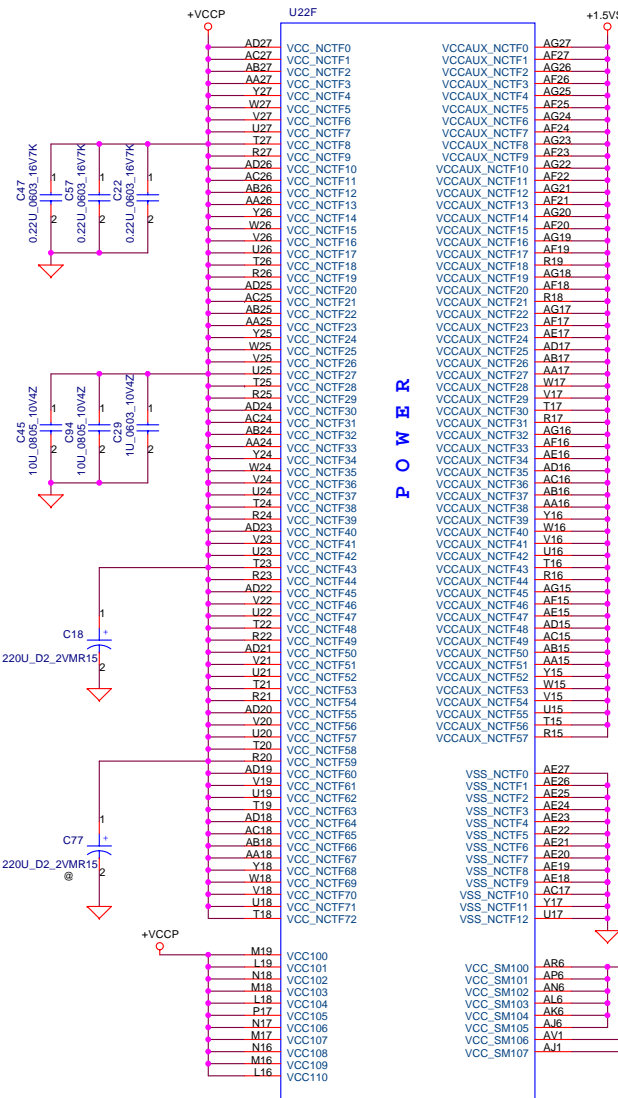
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<b>Calistoga (4/6)</b>		
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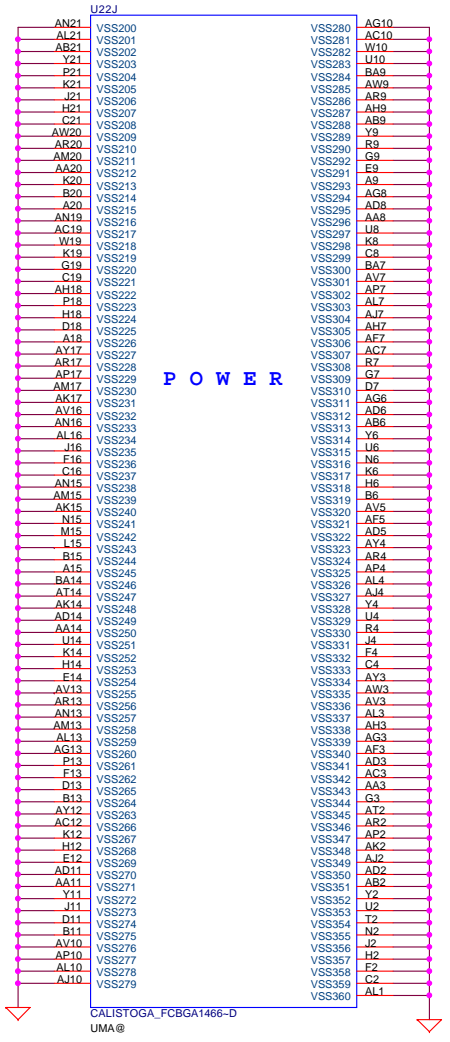
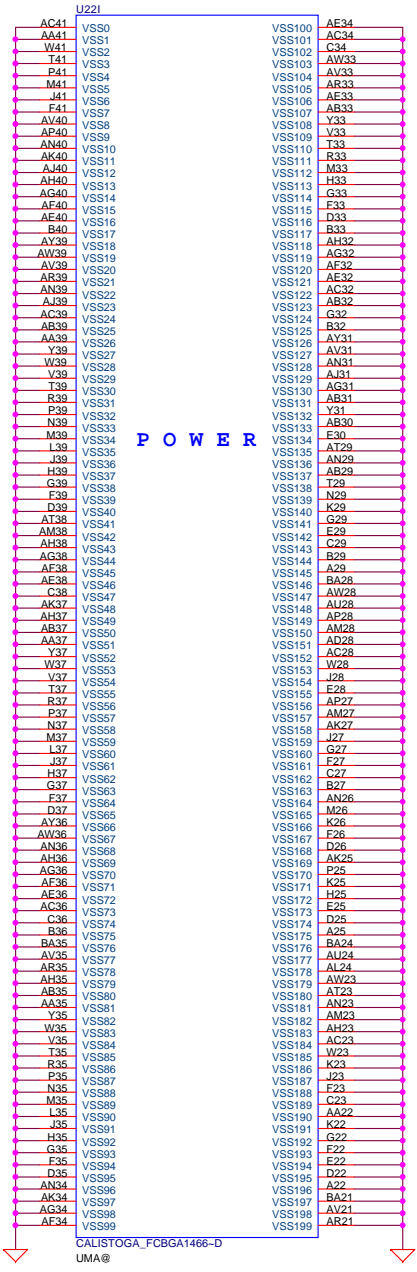
### Strap Pin Table

CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

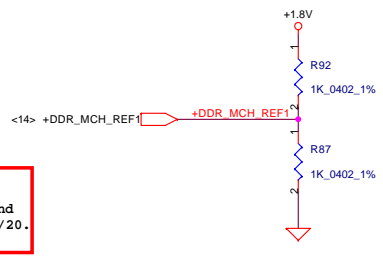
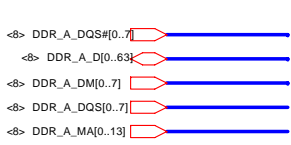
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved PSB 4X CLK Enable 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. *(Default) 1 = PCIe/SDVO are operating simu.



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Size	Document Number	Rev	Date: Thursday, February 23, 2006 Sheet 11 of 43		
Custom	HEL80/81 LA-3161P	0.2			

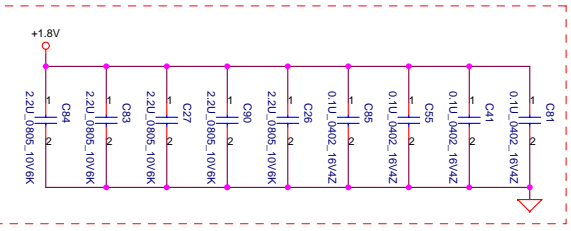


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				Rev: 0.2
				Sheet 12 of 43

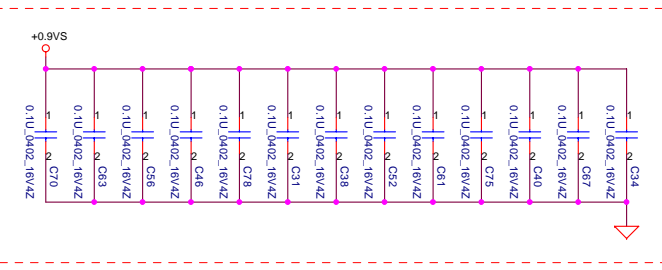


**Layout Note:**  
Place near JP41

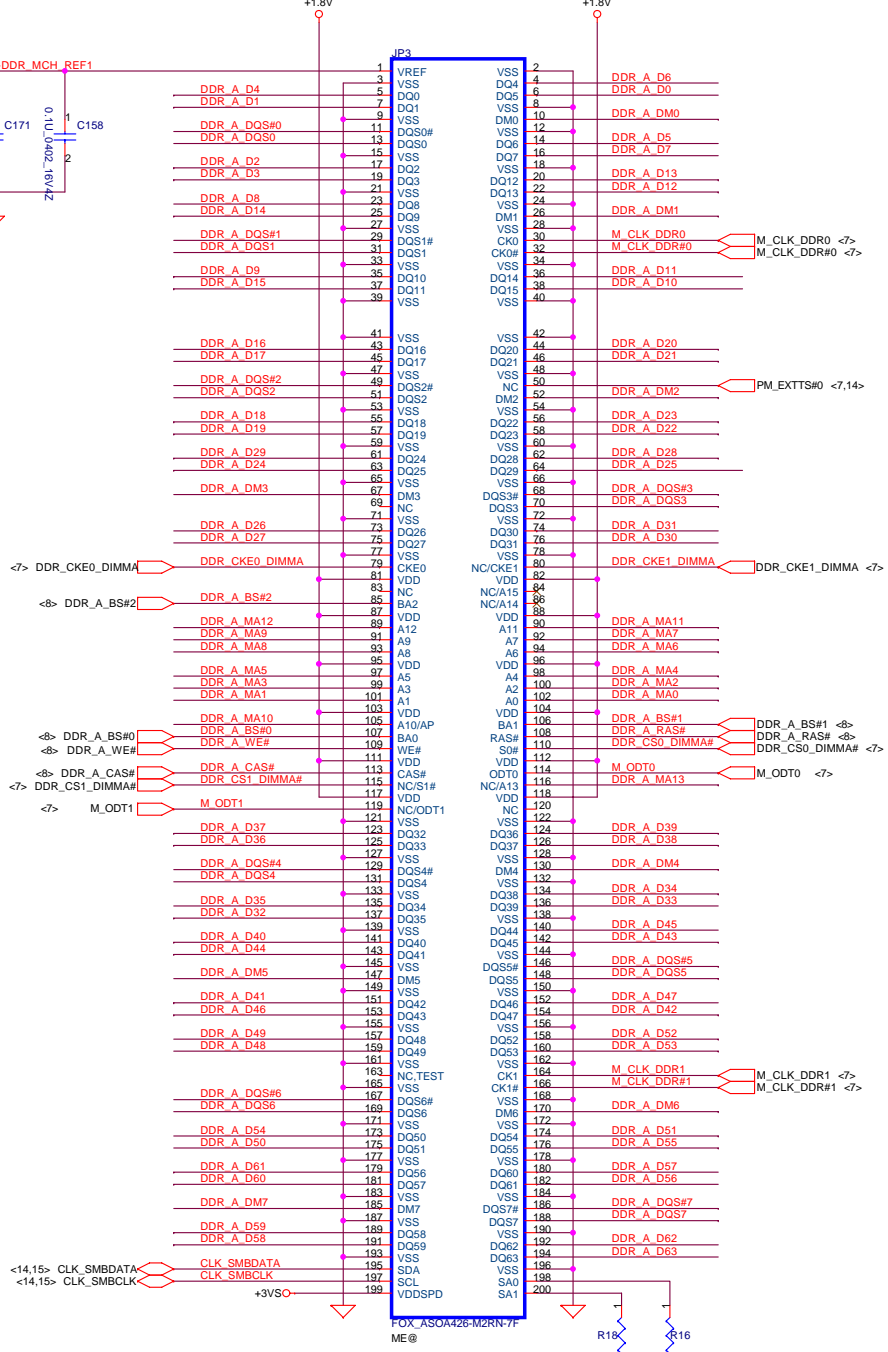
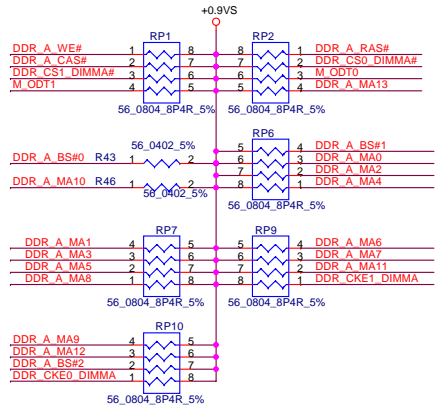
**Layout Note:**  
+DDR\_MCH\_REF  
trace width and  
spacing is 20/20.



**Layout Note:**  
Place one cap close to every 2 pullup  
resistors terminated to +0.9VS

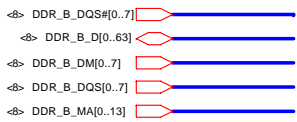


**Layout Note:**  
Place these resistor  
closely JP41,all  
trace length Max=1.5"

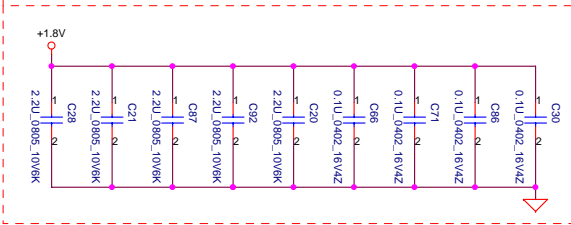


11/9 Modify pn to SP070006V00 SO-DIMM A  
Top side

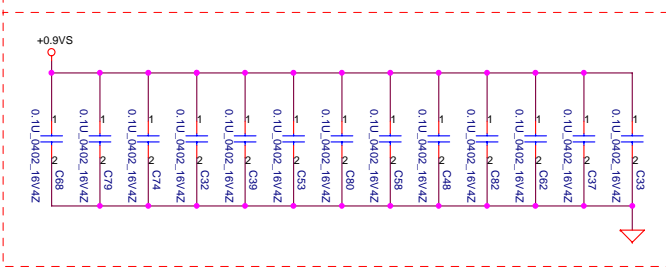
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	<b>DDRII-SODIMM SLOT1</b>	
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Size	Document Number	Rev	Date: Thursday, February 23, 2006 Sheet 13 of 43		
Custom	HEL80 LA-3161P	0.2			



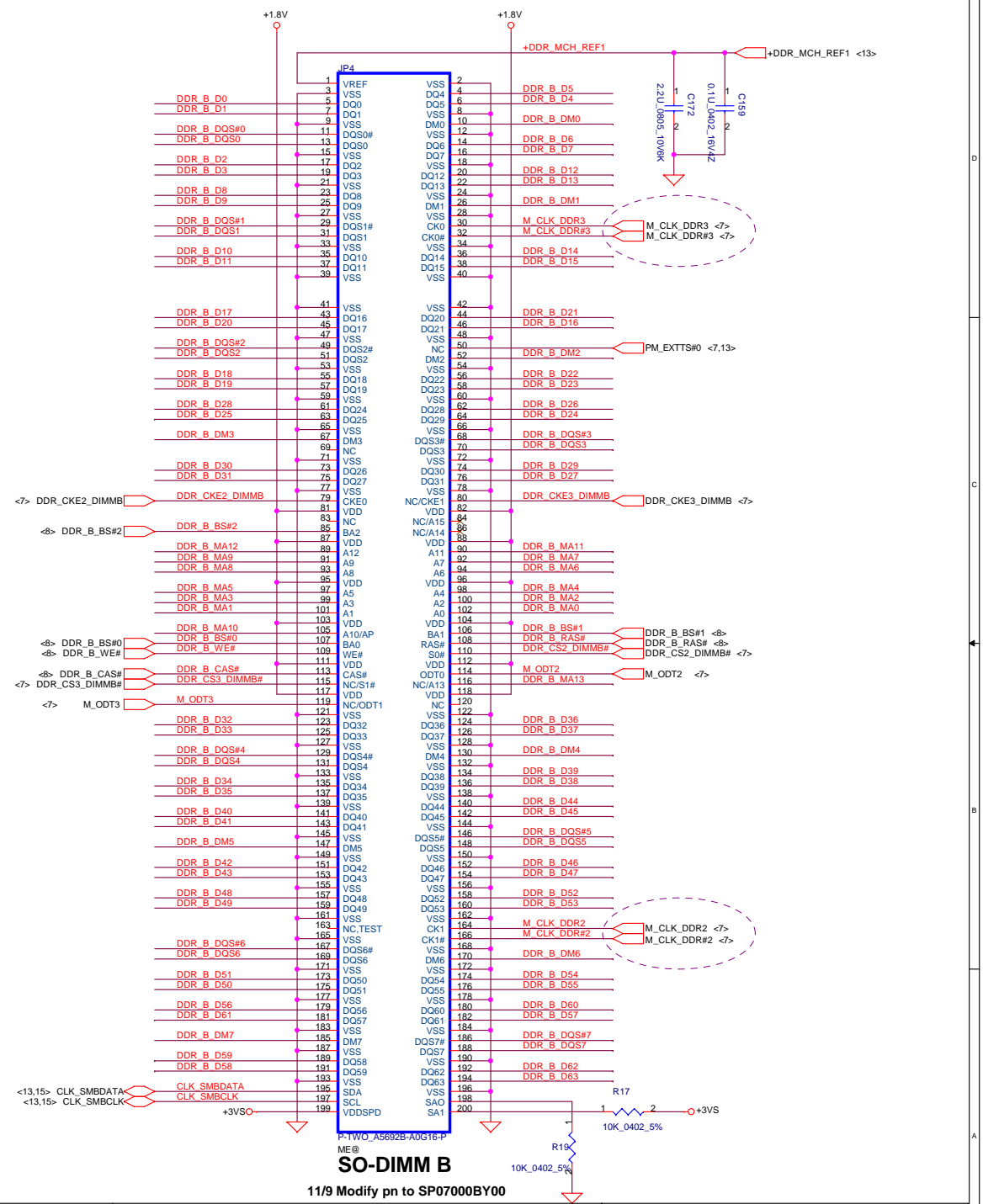
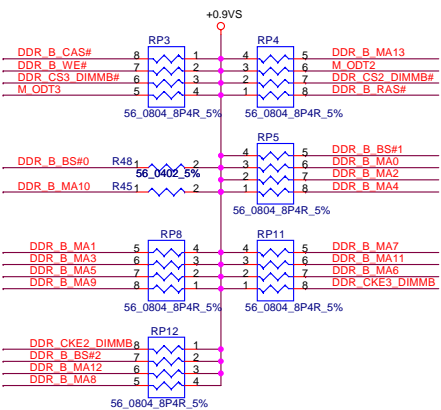
**Layout Note:**  
Place near JP42



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP42, all trace length Max=1.5"



**SO-DIMM B**  
11/9 Modify pn to SP07000BY00

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Issued Date	2005/10/06	Deciphered Date	2006/10/06	<b>DDRII-SODIMM SLOT2</b>	
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Size	Document Number	Rev	Date: Thursday, February 23, 2006 Sheet 14 of 43		
	HEL80 LA-3161P	0.2			

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

**FSB Frequency Selet:**

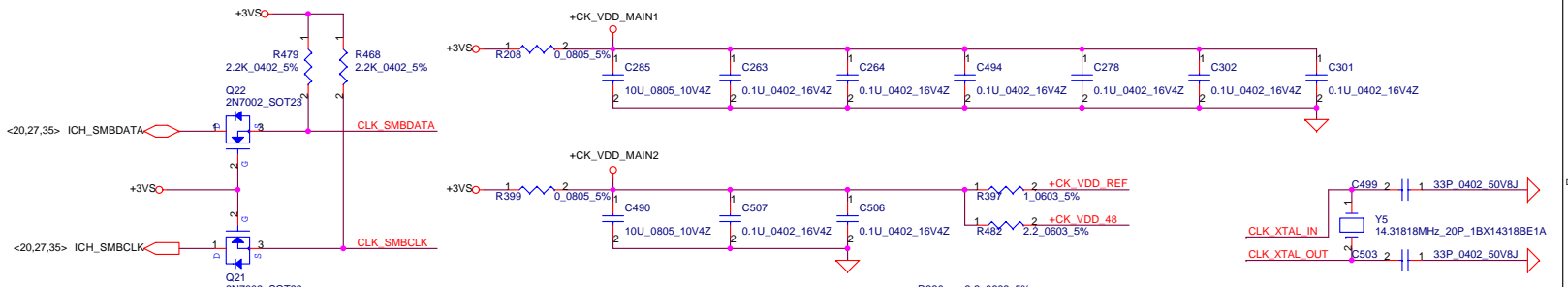
CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	* (Default)	No Stuff	CLK_Rd	CLK_Re

533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc

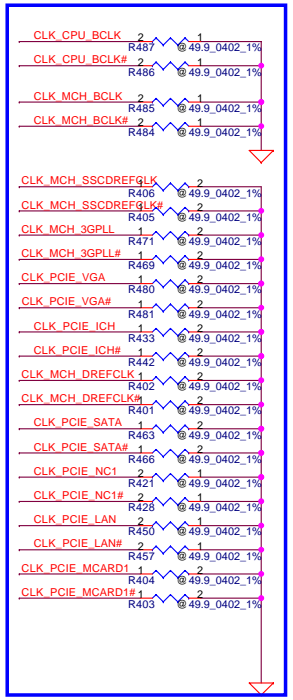
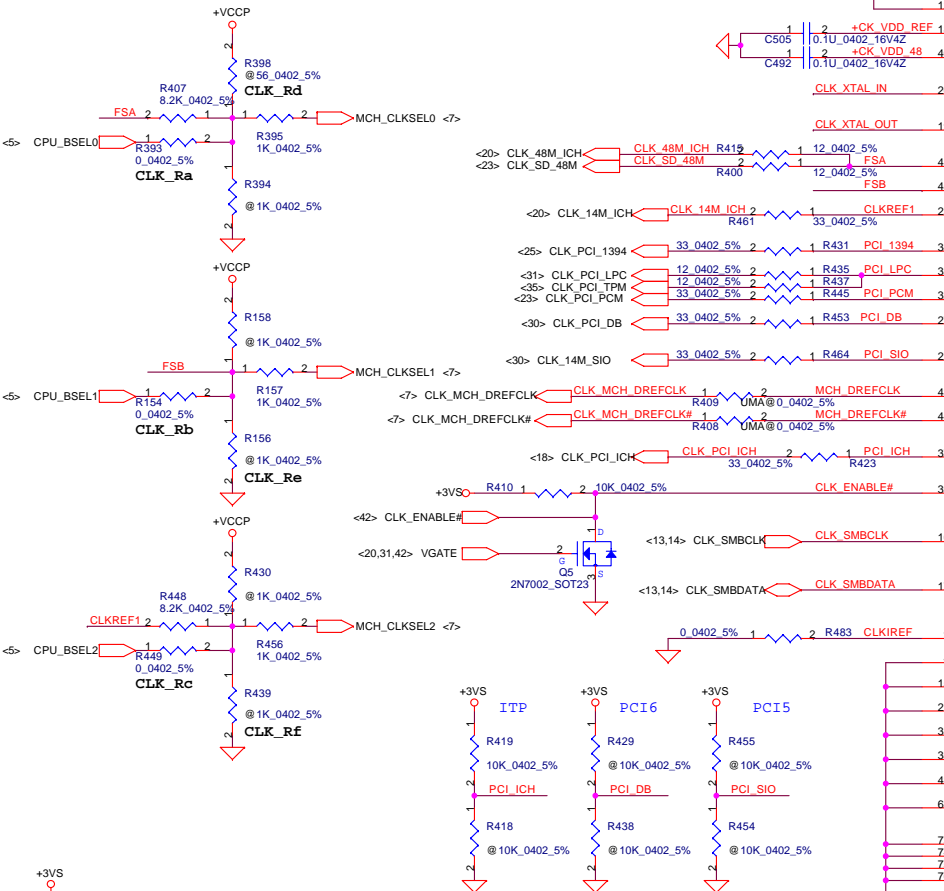
  

667MHz	Stuff	CLK_Rd	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb



Place crystal within 500 mils of CK410

Place near U4  
Place these components near each pin within 40 mils.



PCI\_1394 = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

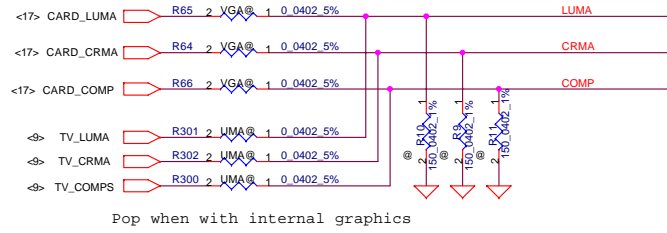
PCI\_DB=SEL\_PCI6

PCI_DB	PIN27
0	CLKREQ5
1	PCICLK6

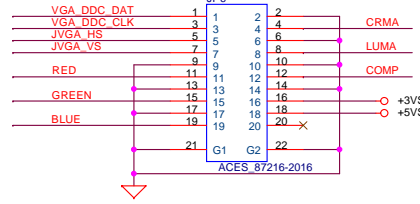
ICS9LPR325CKLFT\_MLF72: SA00000RE20  
 SLG8LP465VTR: SA00000TS00  
 2005/1/8 modify footprint to ICS954305DKLFT\_MLF72 for Thermal Pad use

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Date:	Thursday, February 23, 2006	Sheet	15 of 43	

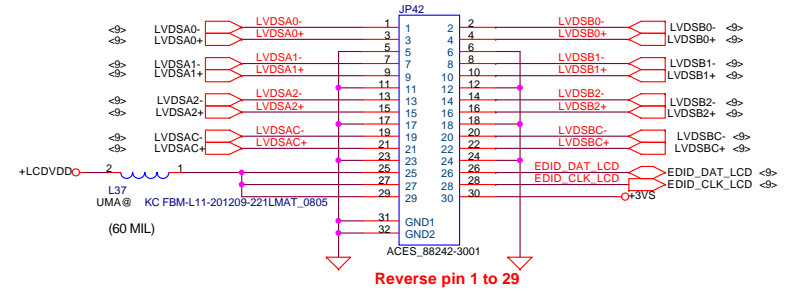
### TV-OUT Conn.



### VGA I/O PORT Conn.

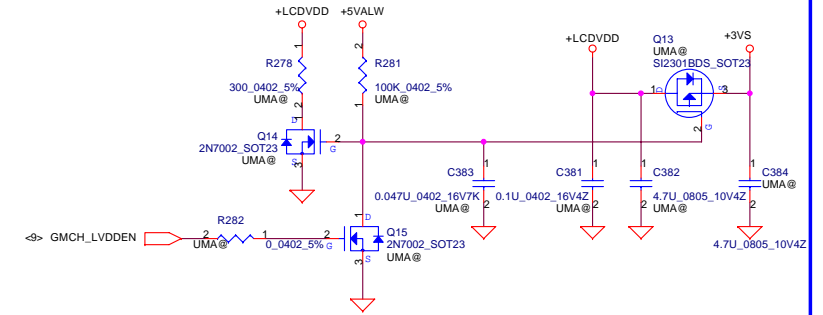
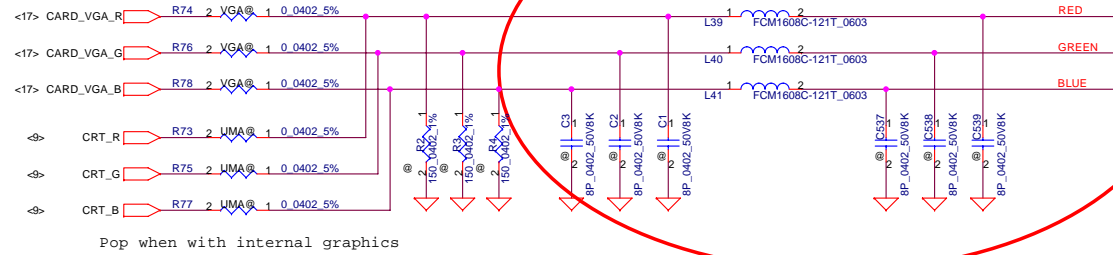


### UMA LCD / PANEL Conn.

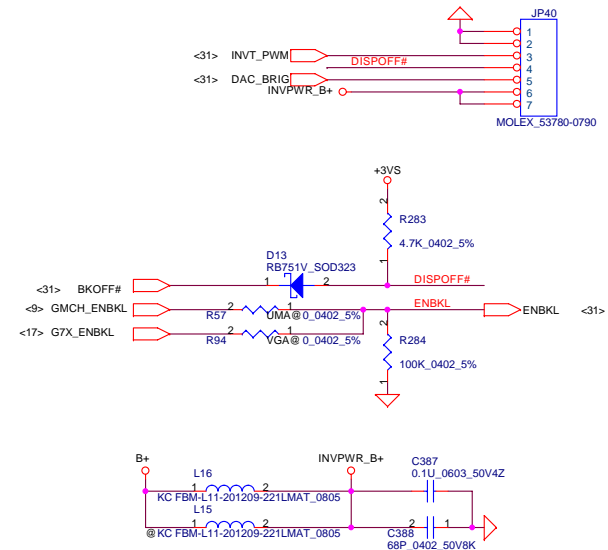


### CRT Conn.

2/09 Add for Compliance Engineering request



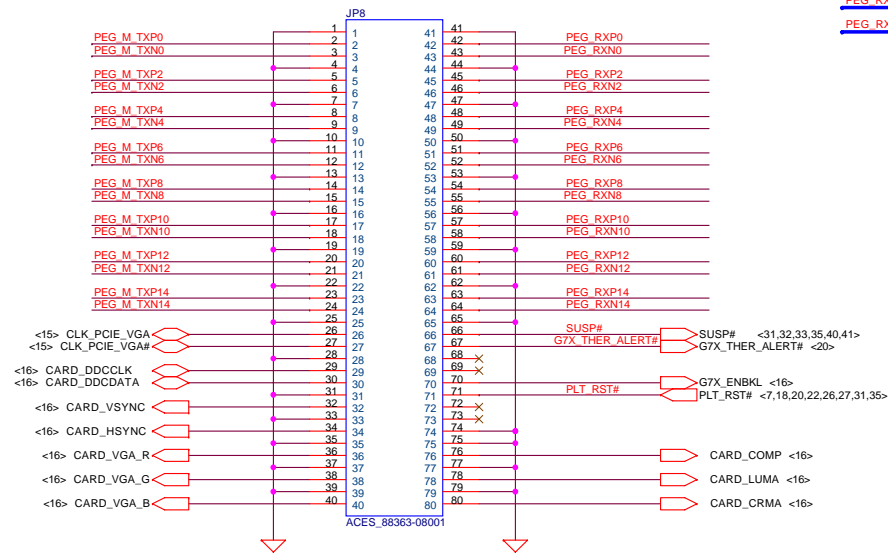
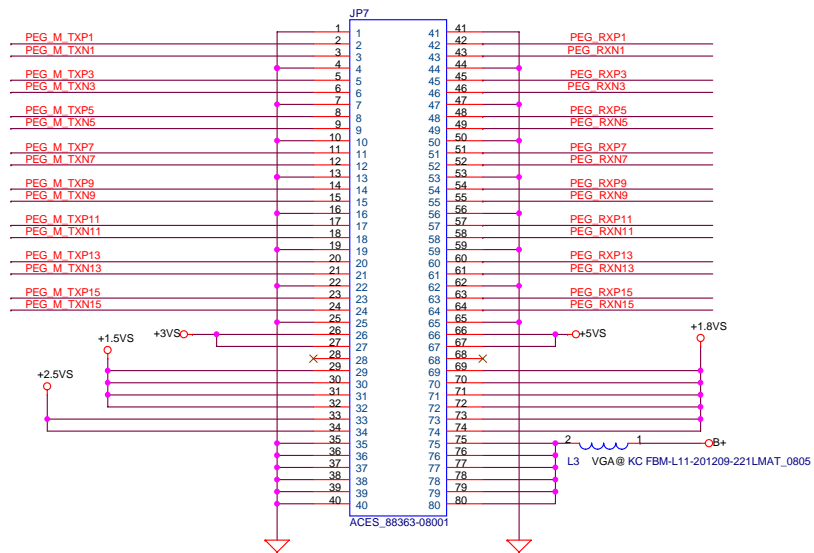
### INVERTER Conn.



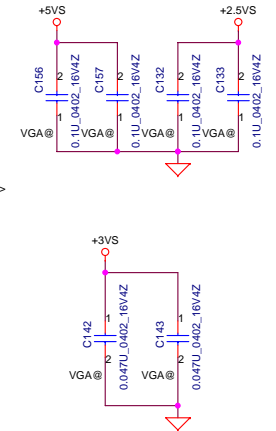
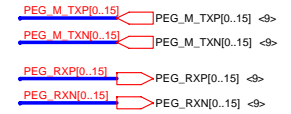
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Issued Date	2005/10/06	Deciphered Date
		2006/10/06
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Title	
Compal Electronics, Inc.	
CRT & TVout Connector	
Size	Document Number
Custom	HEL80 LA-3161P
Date:	Thursday, February 23, 2006
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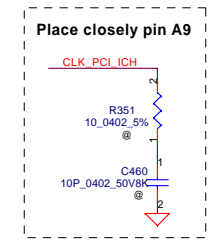
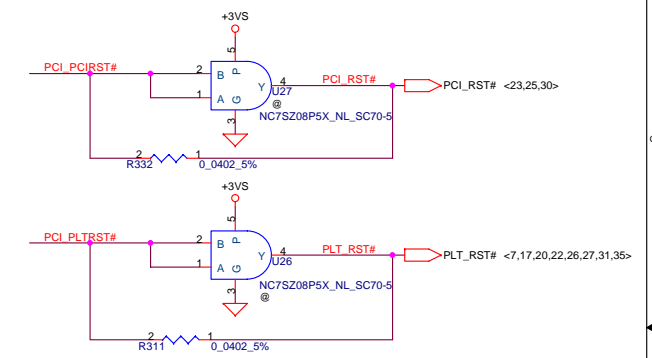
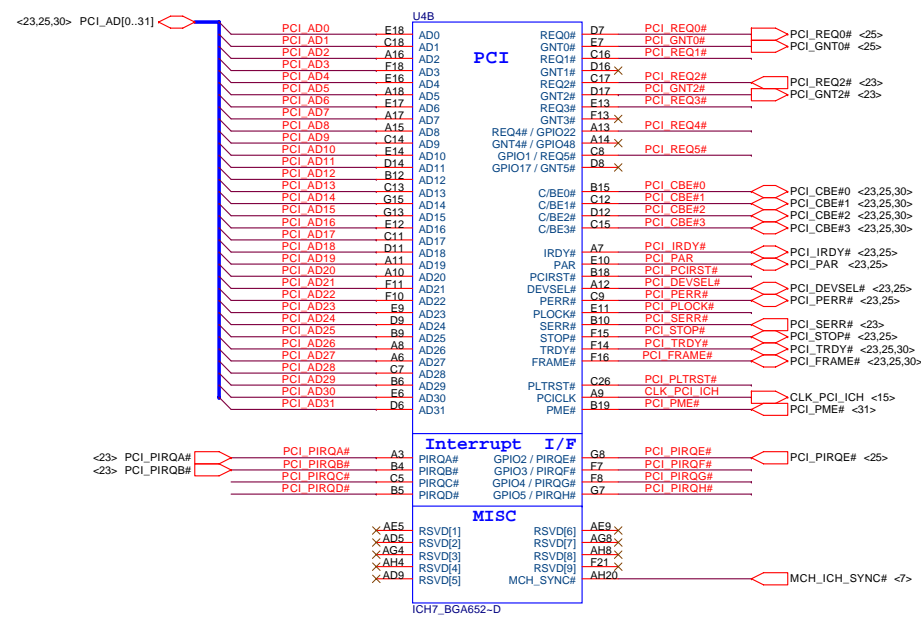
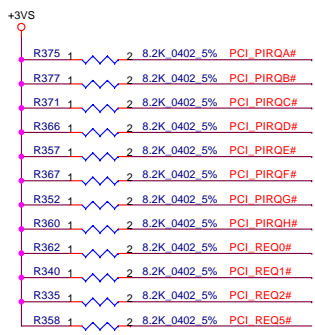
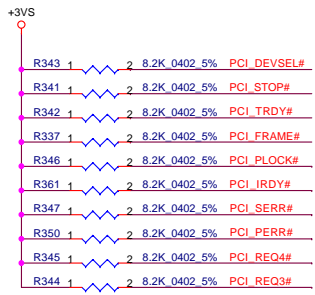




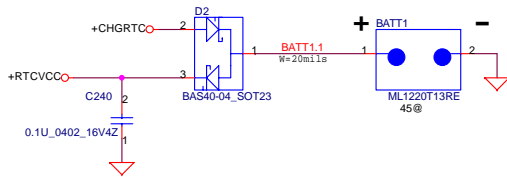
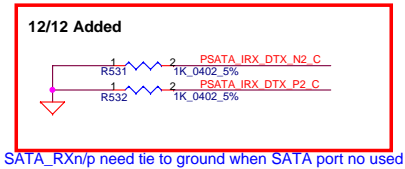
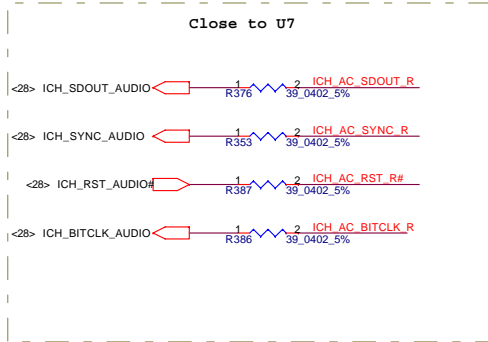
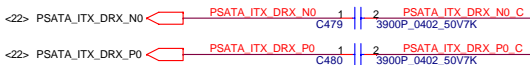
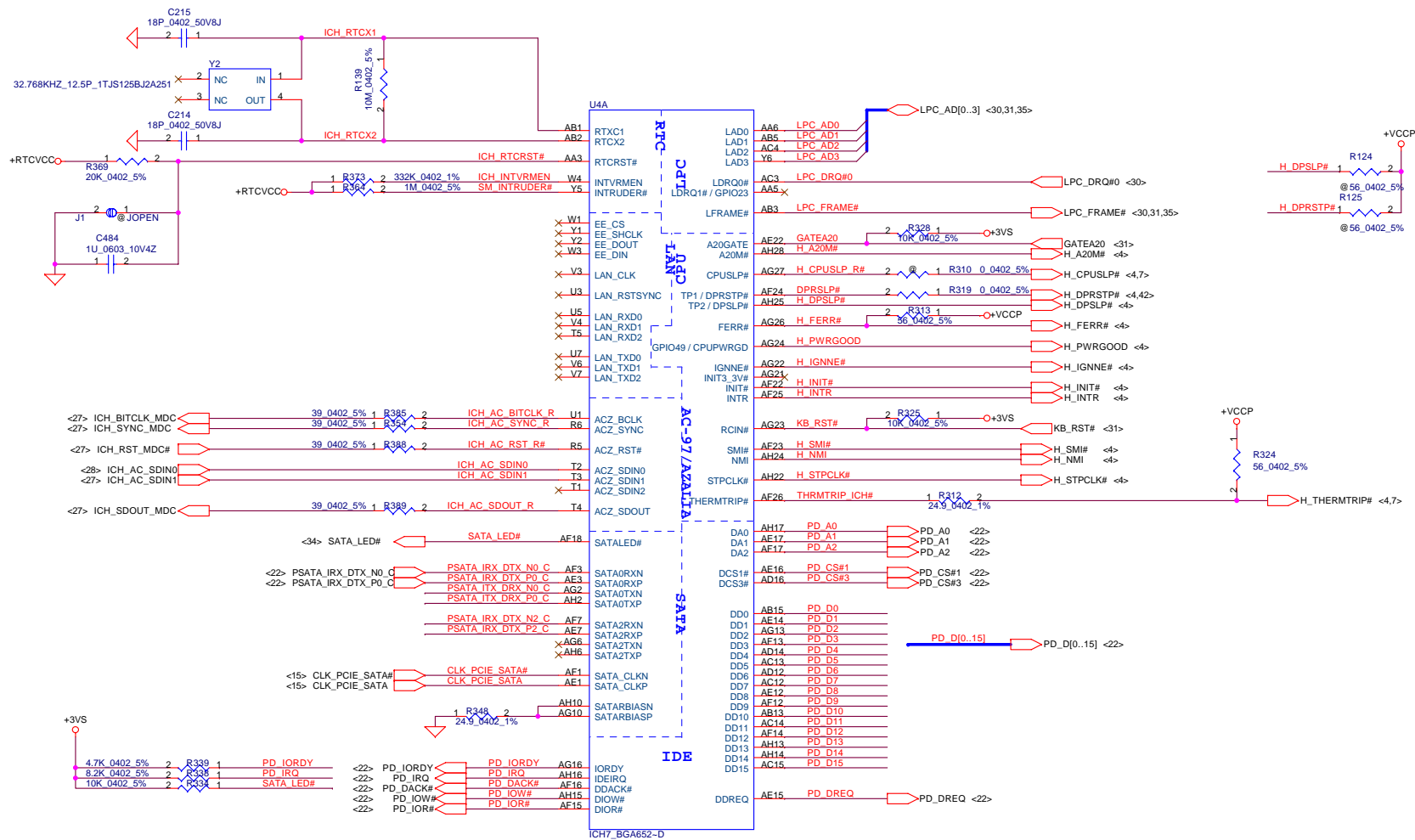
MAX. 4.06A @ 1.8V  
 MAX. 130mA @ 2.5V  
 MAX. 655mA @ 3.3V



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				HEL80 LA-3161P		0.2
Date: Thursday, February 23, 2006				Sheet 17 of 43		

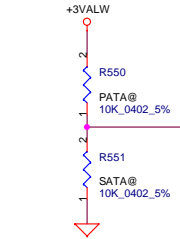
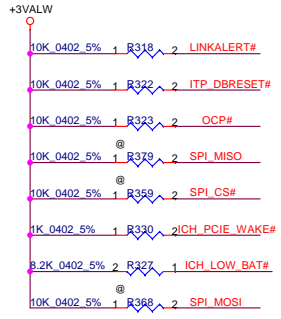
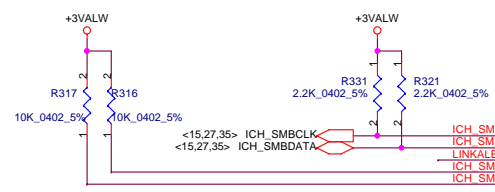
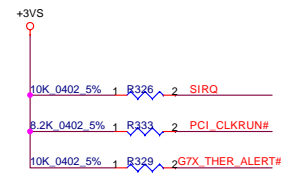


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				ICH7-M(1/4)		
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					HEL80 LA-316P	0.2
				Date:	Thursday, February 23, 2006	Sheet 18 of 43

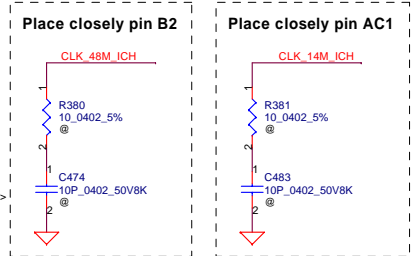
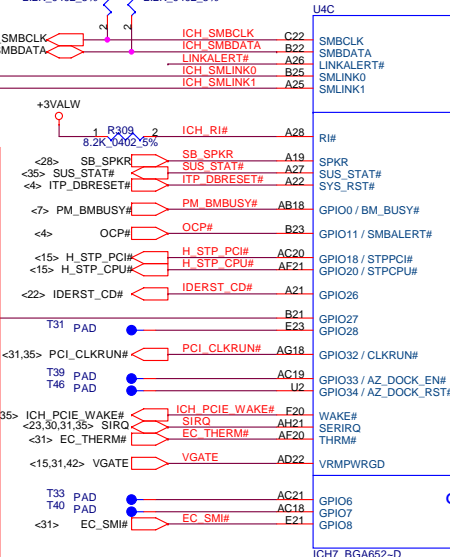


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Issued Date	2005/10/06	Deciphered Date
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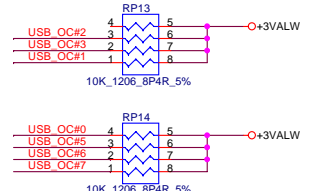
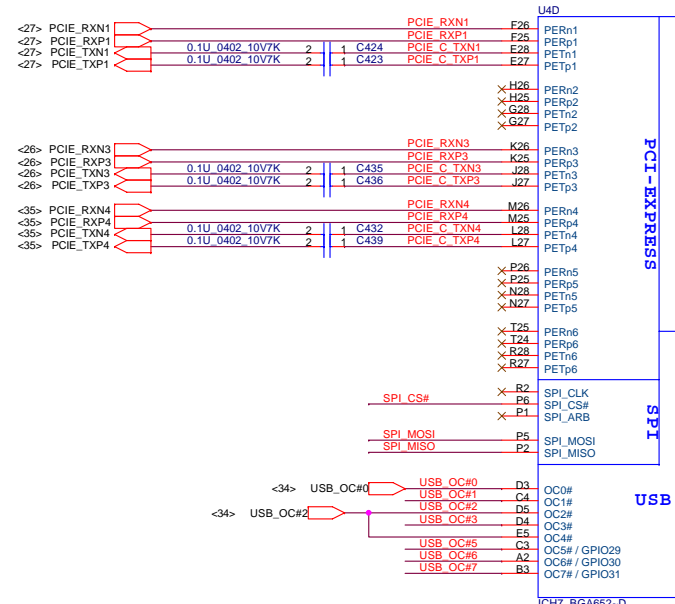
<b>Compal Electronics, Inc.</b>	
<b>ICH7-M(2/A)</b>	
Size	Document Number
Custom	<b>HEL80 LA-3161P</b>
Date	Thursday, February 23, 2006
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Rev	0.2



**2/13 Add feature:  
Pull high for pure IDE interface  
Pull low for SATA interface**



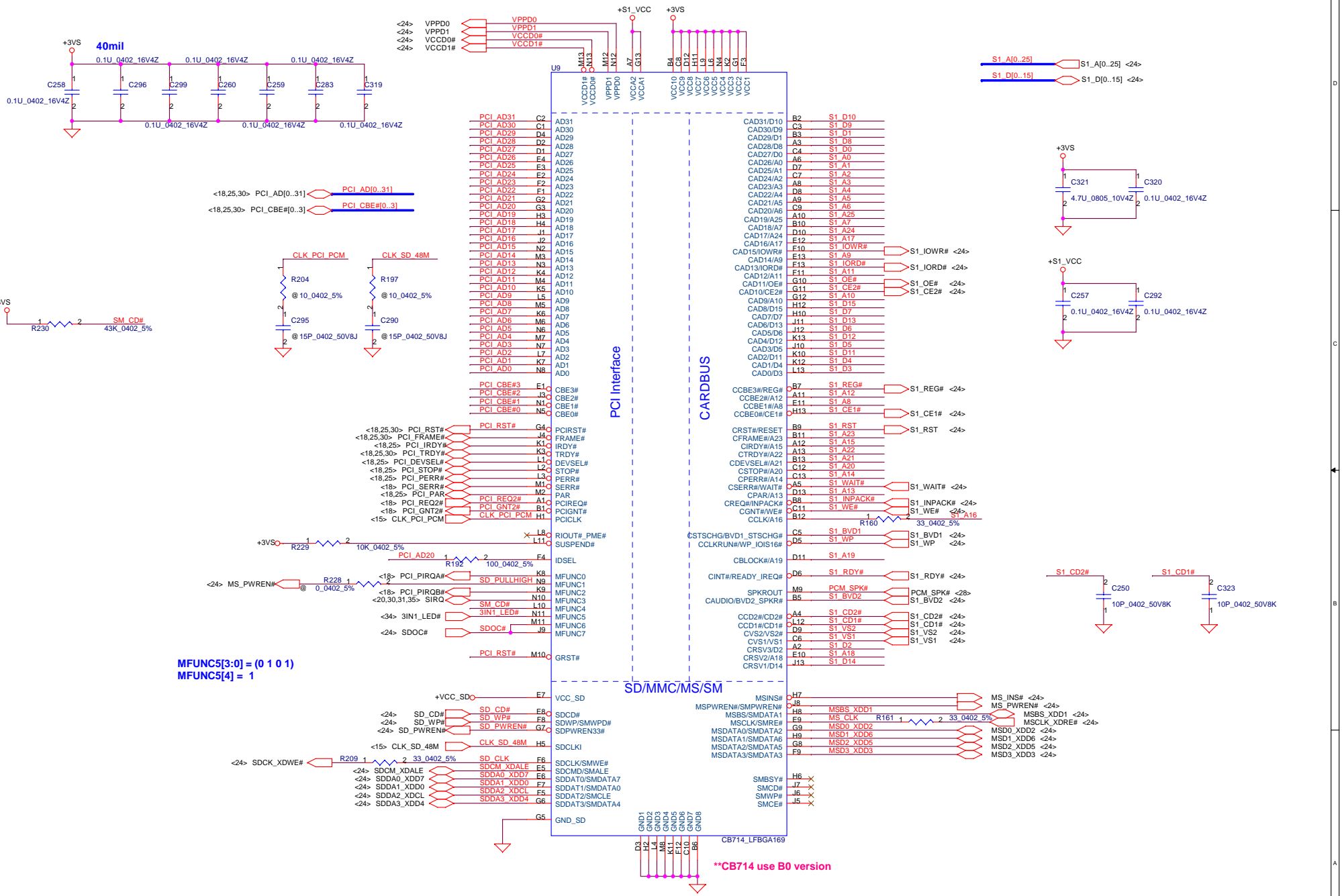
Need update symbol



Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	<b>IC7-M(3/4)</b>
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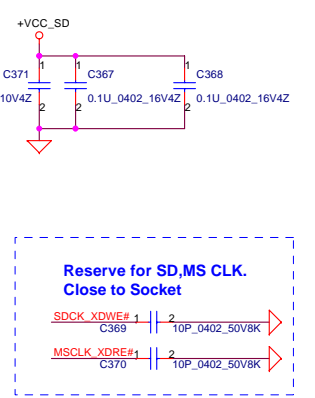
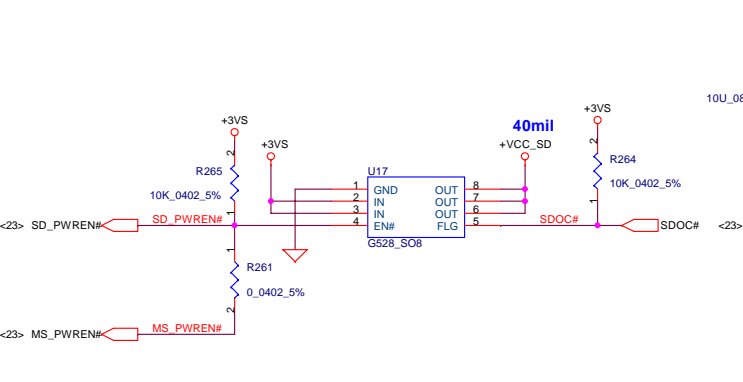
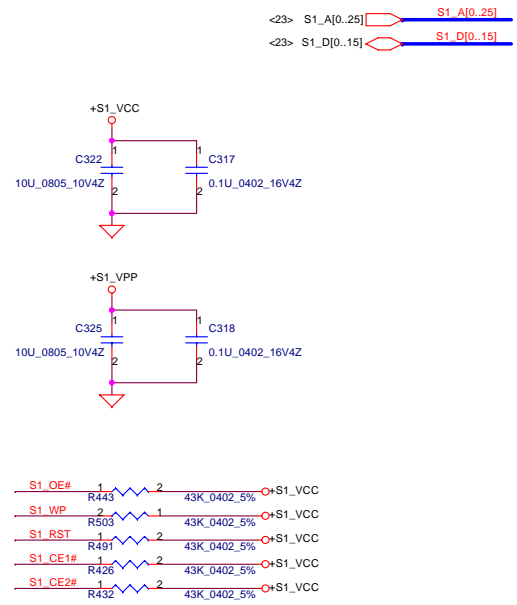
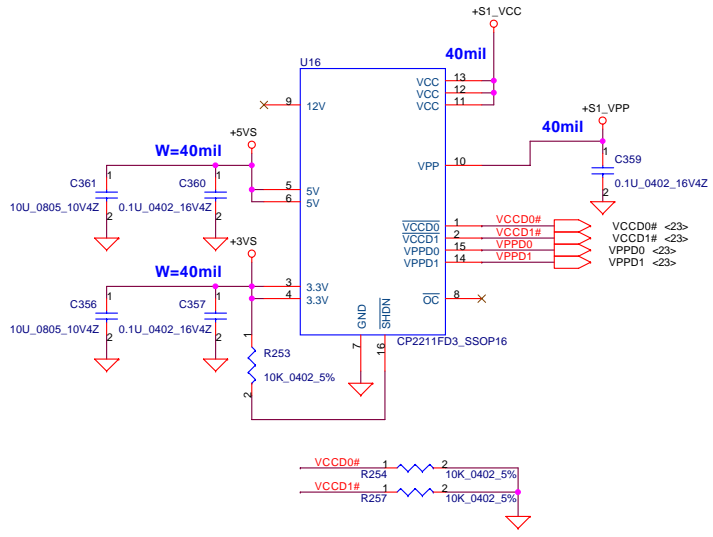
MFUNC5[3:0] = (0 1 0 1)  
MFUNC5[4] = 1

Security Classification	Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date
		2006/06/20

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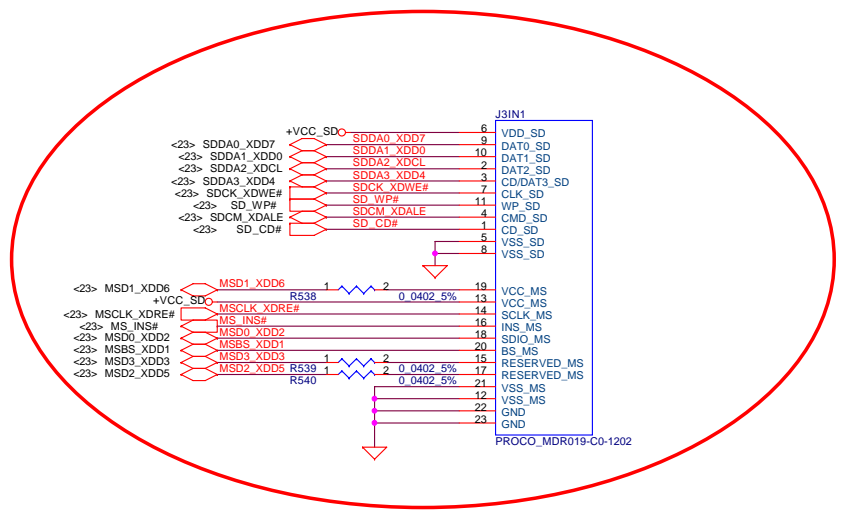
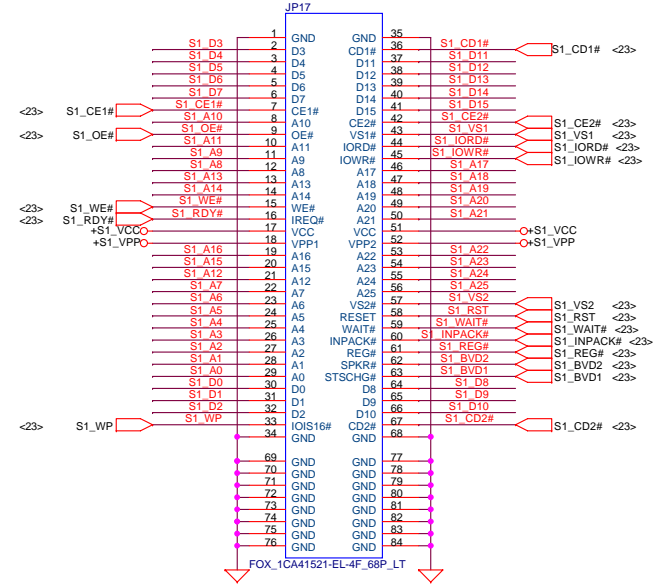
Compal Electronics, Inc.		
Title	Cardbus Controller CB714	
Size	Document Number	Rev
Custom	HEL80 LA-3161P	0.2
Date:	Thursday, February 23, 2006	Sheet 23 of 43

### PCMCIA Power Control



### PCMCIA Socket

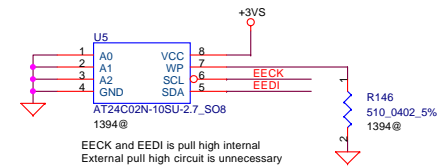
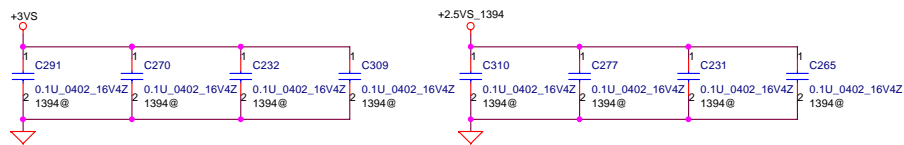
Note : 11/10 modify library to meet spec  
 pn: SP01000IC00  
 02/17 modify footprint to FOX\_1CA41521-EL-4F\_68P\_LT



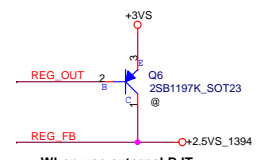
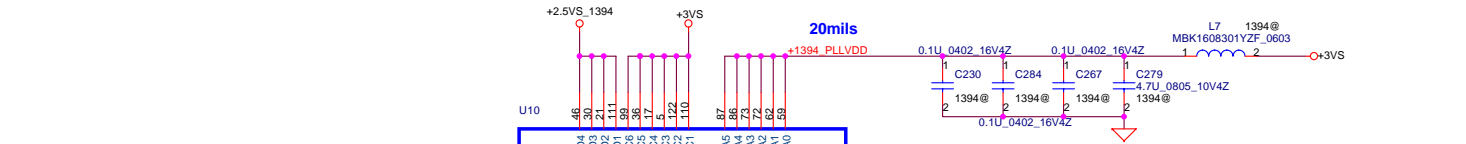
12/20 modified

Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	PCMCIA Socket		Size
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				Date: Thursday, February 23, 2006		Sheet 24 of 43

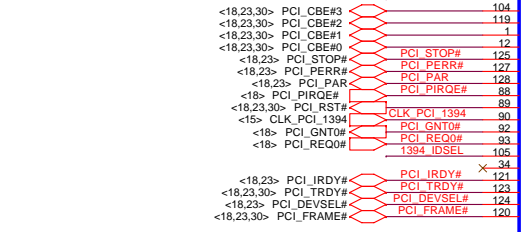
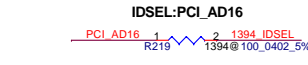
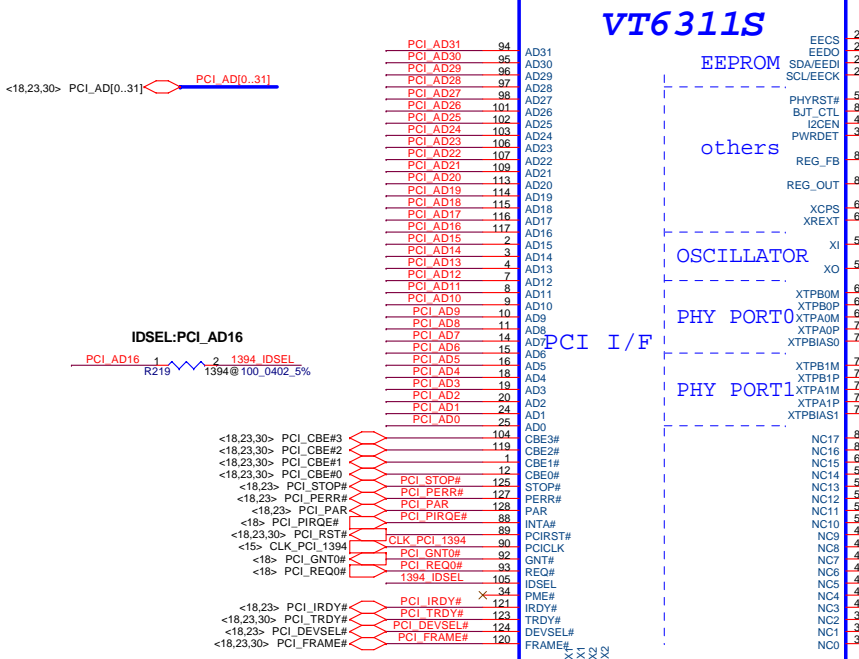




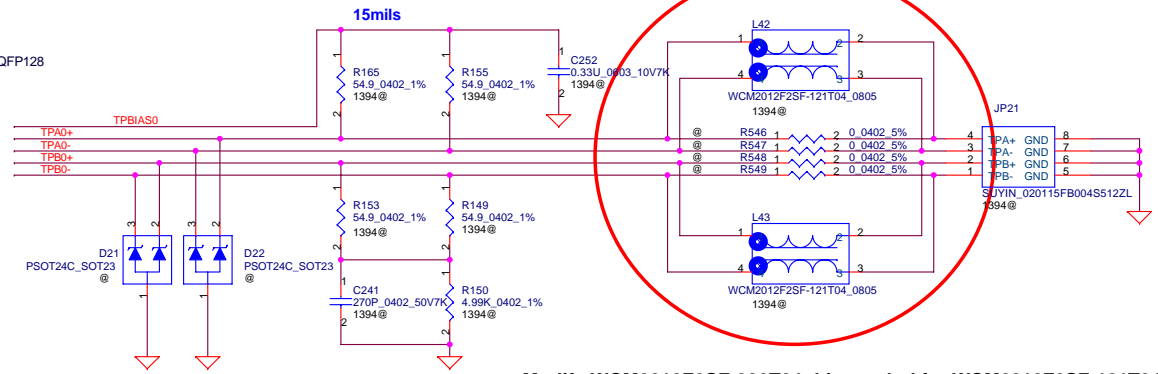
When use external EEPROM  
Populate U14, R246, R253  
Un-populate R261



When use external BJT  
Populate Q35, R279



2/21 Add for Compliance Engineering request

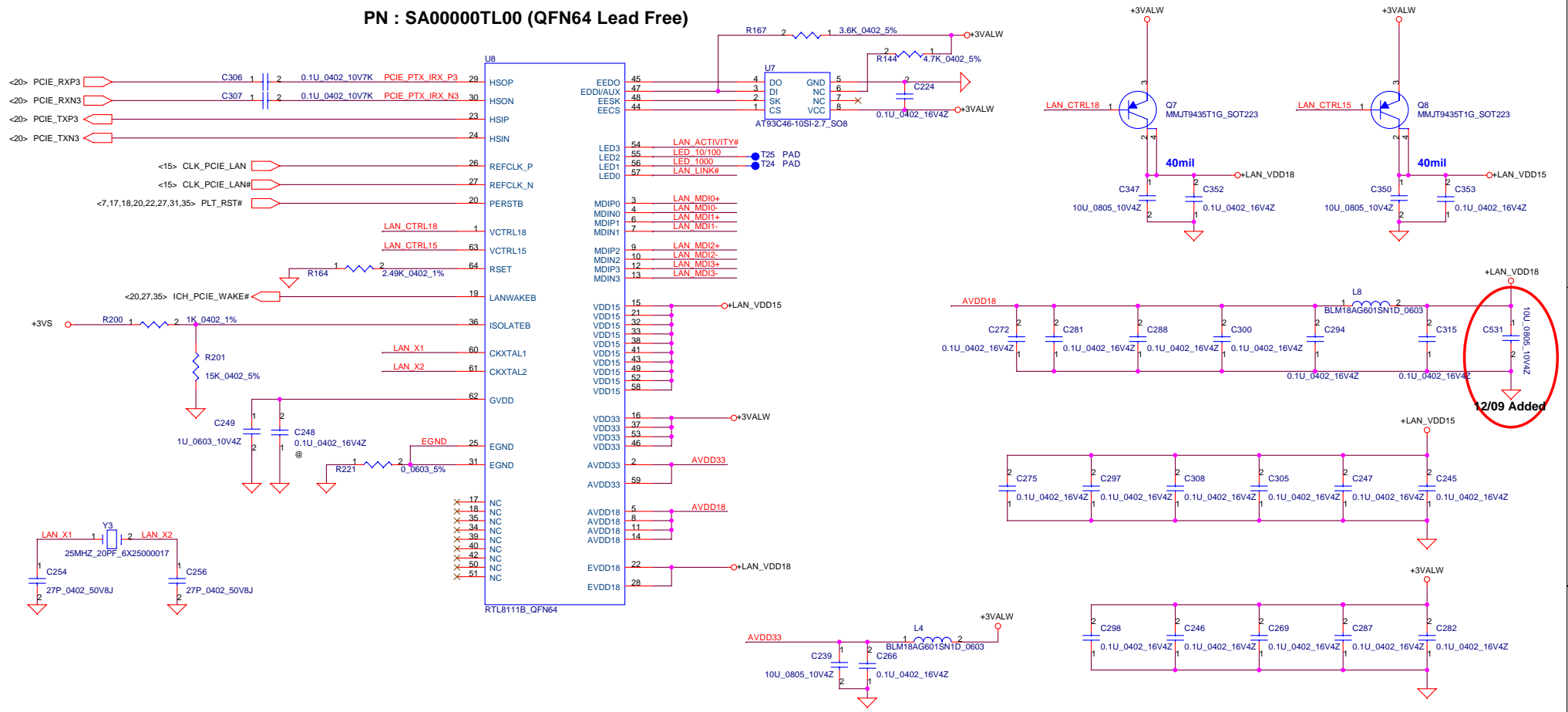


Modify WCM2012F2SF-900T04 this symbol for WCM2012F2SF-121T04

Note : This page copied from HBL50

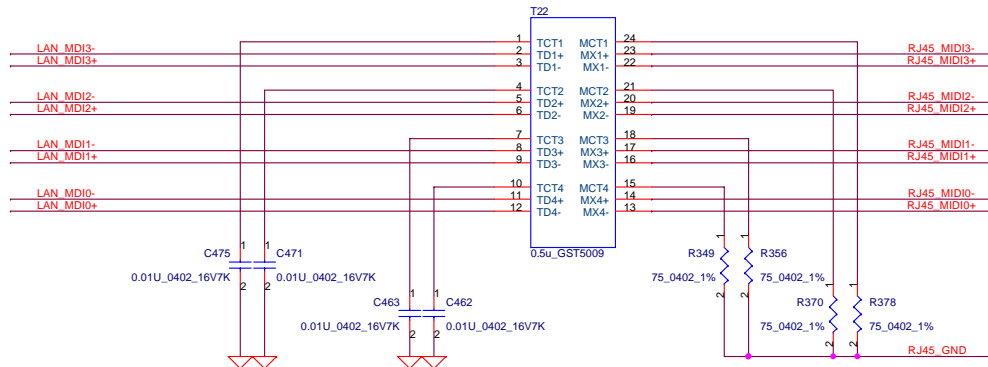
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	IEEE1394 VIA VT6311S
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				Document Number HEL80 LA-3161P
				Rev 0.2
				Date: Thursday, February 23, 2006 Sheet 25 of 43

PN : SA00000TL00 (QFN64 Lead Free)



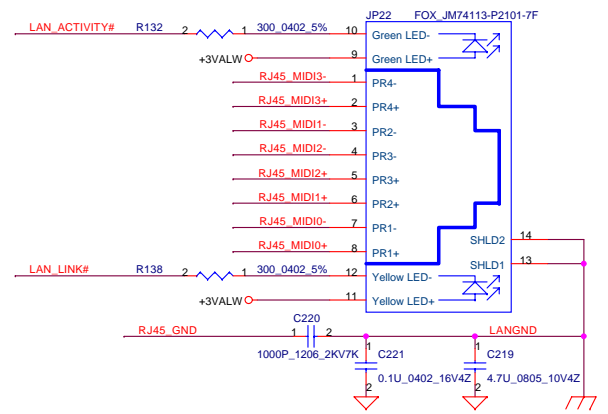
12/09 Added

GbE Transformer: GST5009 (SP050005610) MY



Place these components colsed to LAN chip

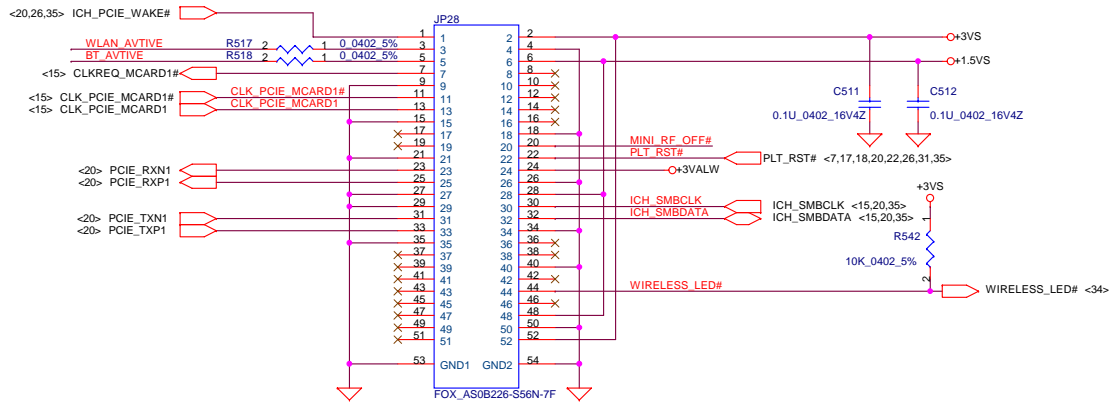
LAN Conn.



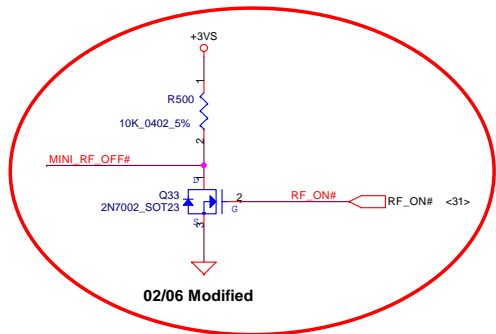
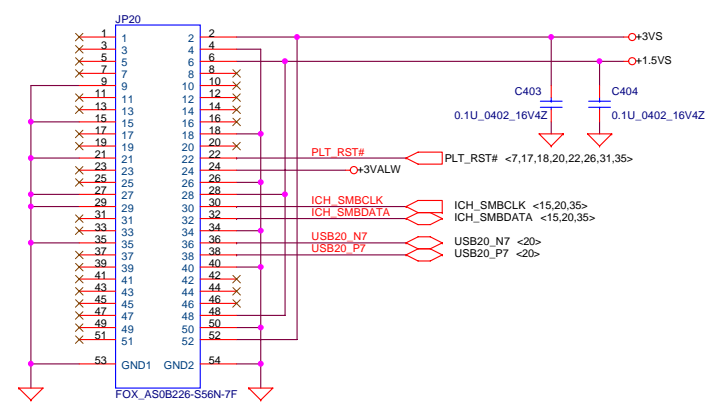
<p><b>Compal Electronics, Inc.</b></p> <p>Title: LAN REALTEK RTL8111B</p>			
Size	Document Number	Rev	
	HEL80 LA-3161P	0.2	
Date:	Thursday, February 23, 2006	Sheet	26 of 43

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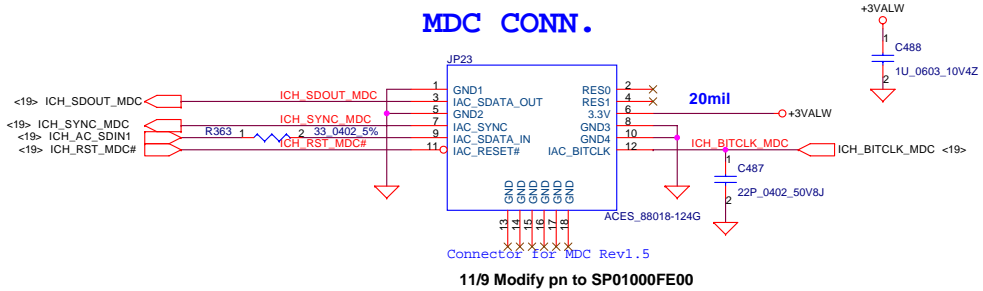
# Mini-Express Card(Slot 1-WLAN)



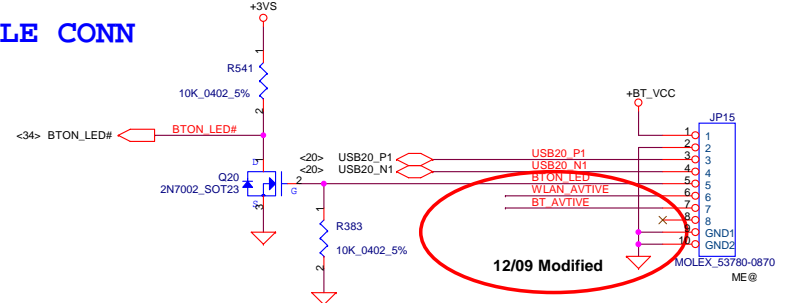
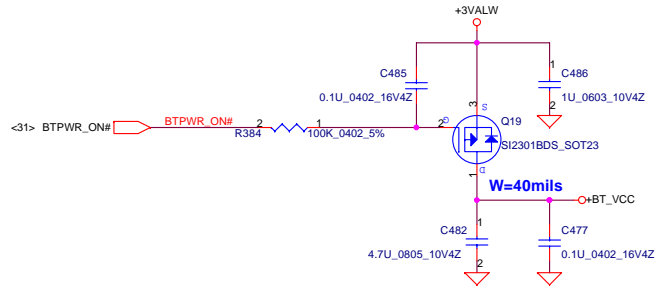
# Mini-Express Card(Slot 2-TV)



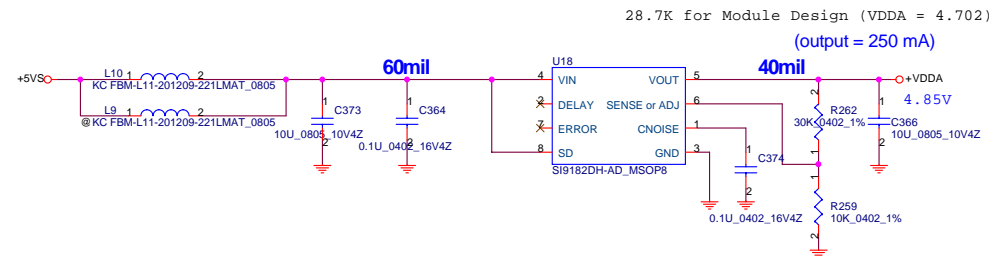
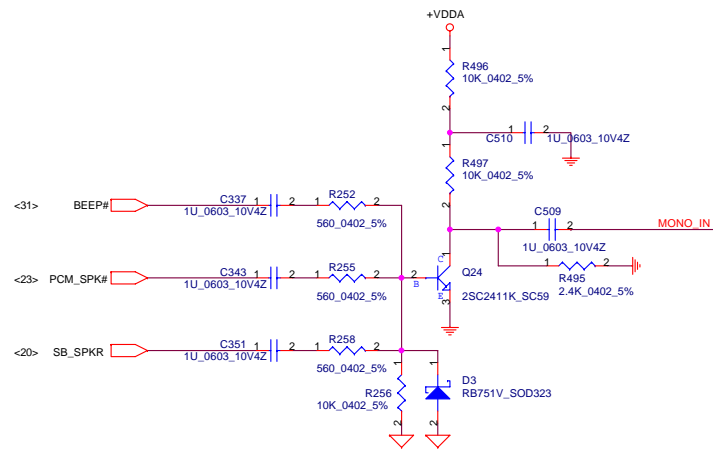
## MDC CONN.



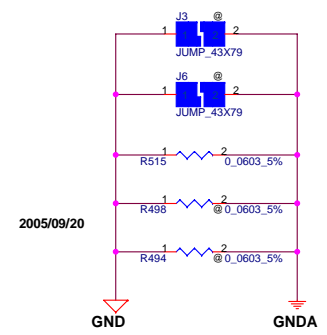
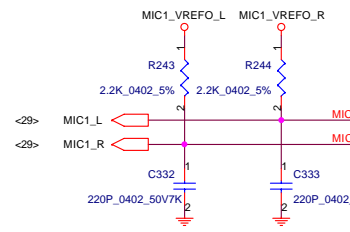
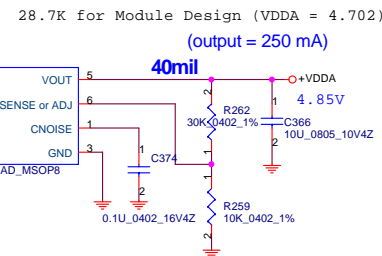
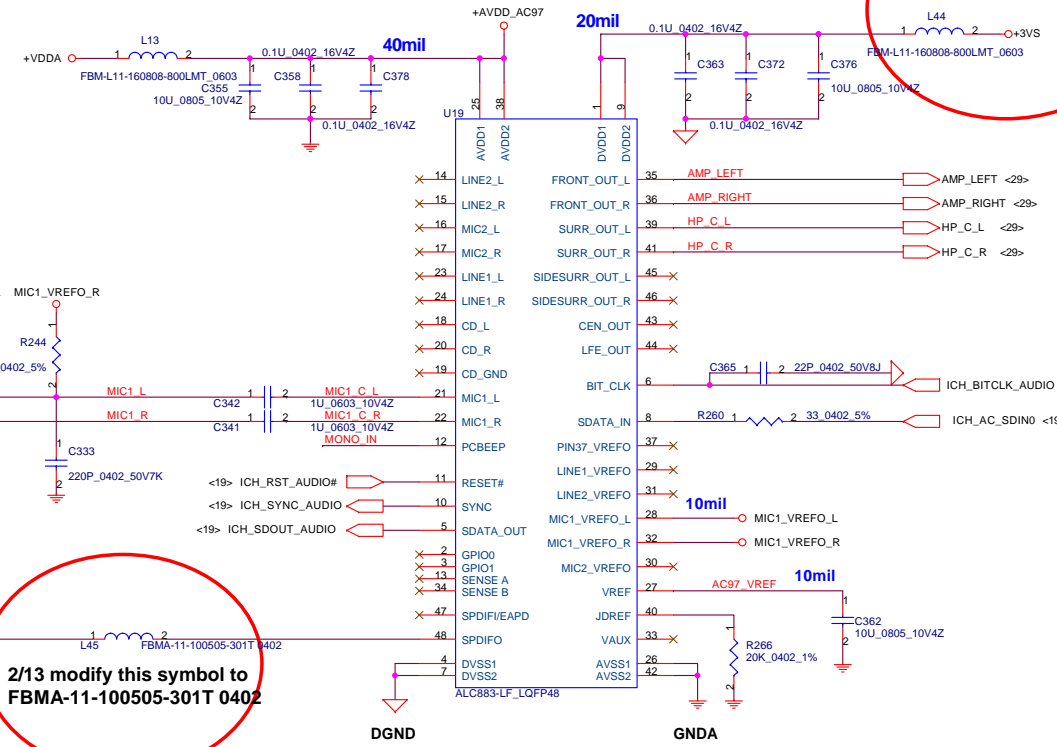
## BT MODULE CONN



Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Mini Card / MDC CONN	
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				Custom	HEL80/81 LA-3161P
				Date:	Thursday, February 23, 2006
				Sheet	27 of 43



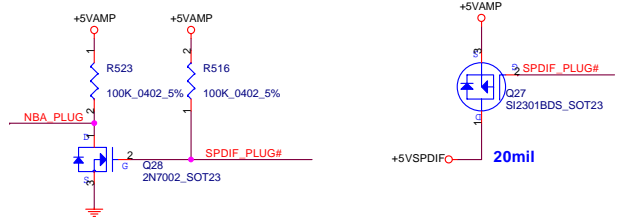
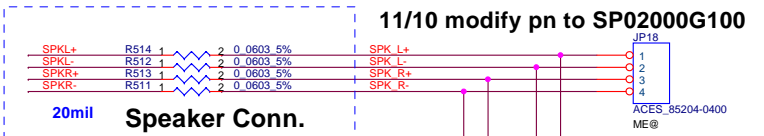
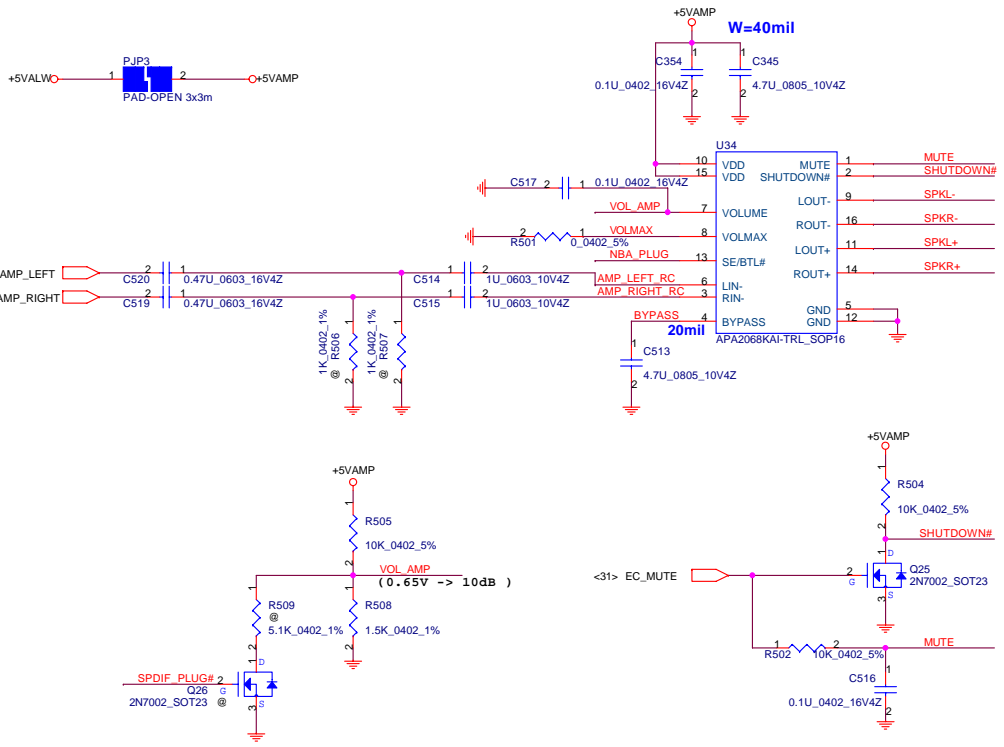
**HD Audio Codec**



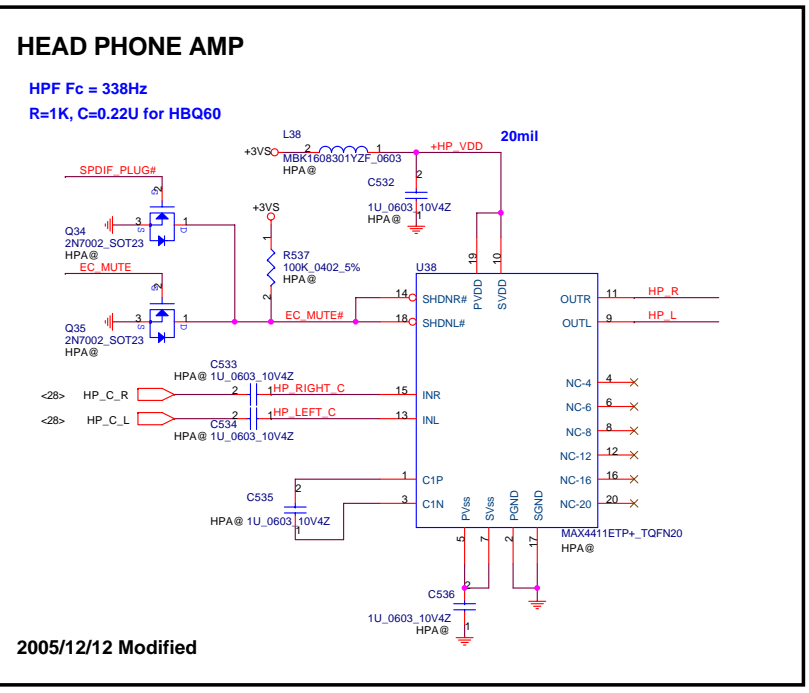
Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
		2006/10/06

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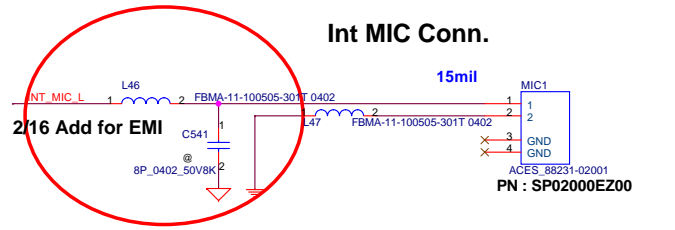
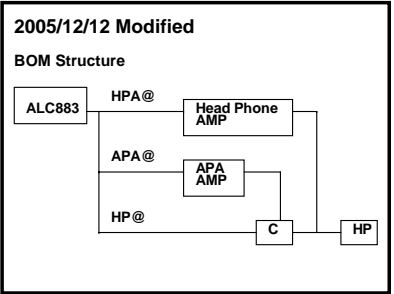
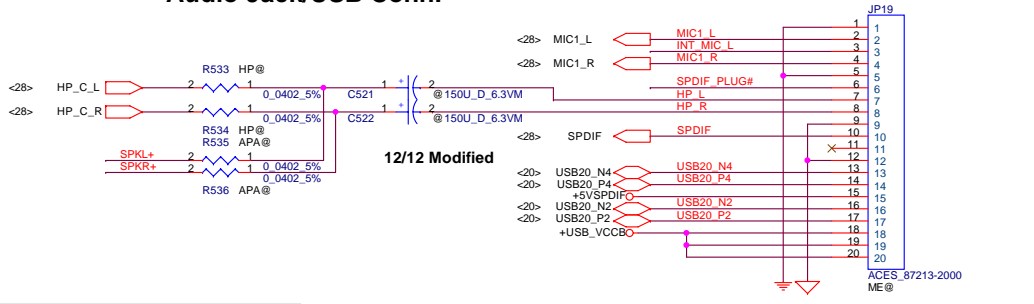
<b>Compal Electronics, Inc.</b>	
<b>HD CODEC ALC883</b>	
Size	Document Number
Custom	HEL80 LA-3161P
Date:	Thursday, February 23, 2006
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	SPDIF_PLUG#	NBA_PLUG
Un-Plug	H	L
HP_Plug_In	L	H
SPDIF_Plug_In	L	H

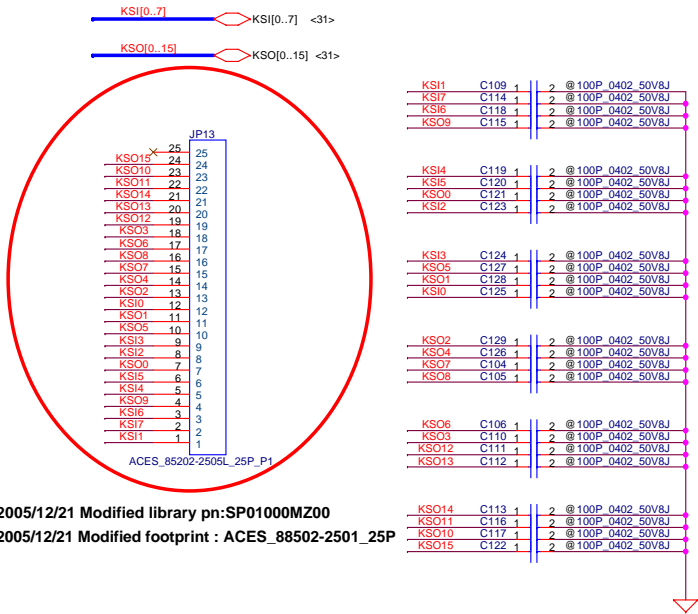


### Audio Jack/USB Conn.



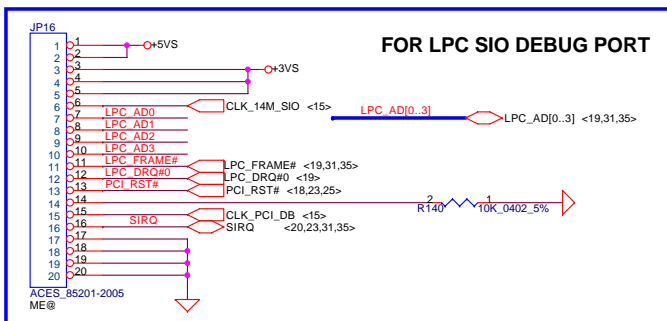
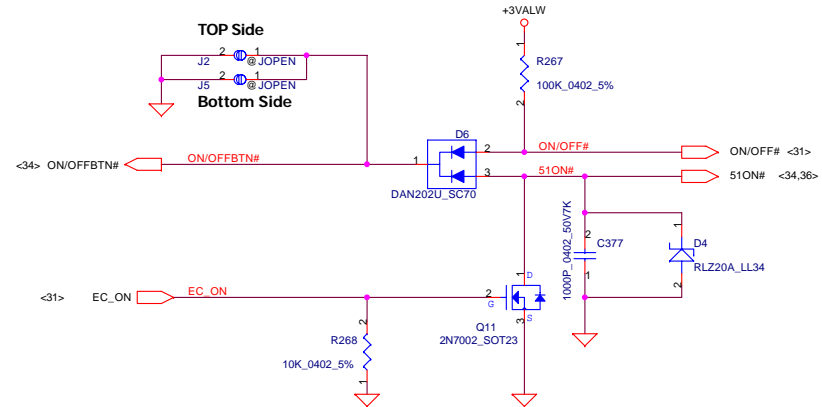
Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	AMP & Audio Jack
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Date: Thursday, February 23, 2006				Rev 0.2
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# INT\_KBD\_CONN.( TYPE "D" KB)

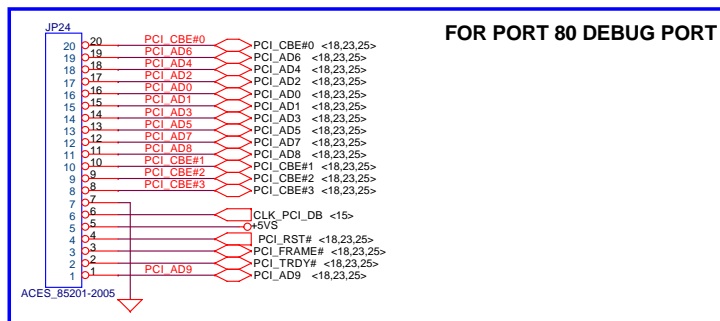


2005/12/21 Modified library pn:SP01000MZ00  
 2005/12/21 Modified footprint : ACES\_88502-2501\_25P

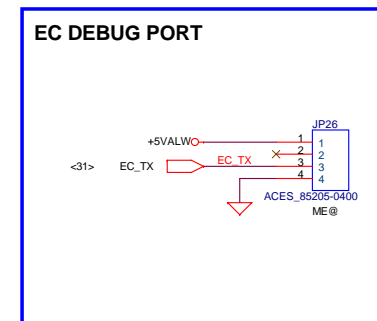
# Power BTN



Not lead free

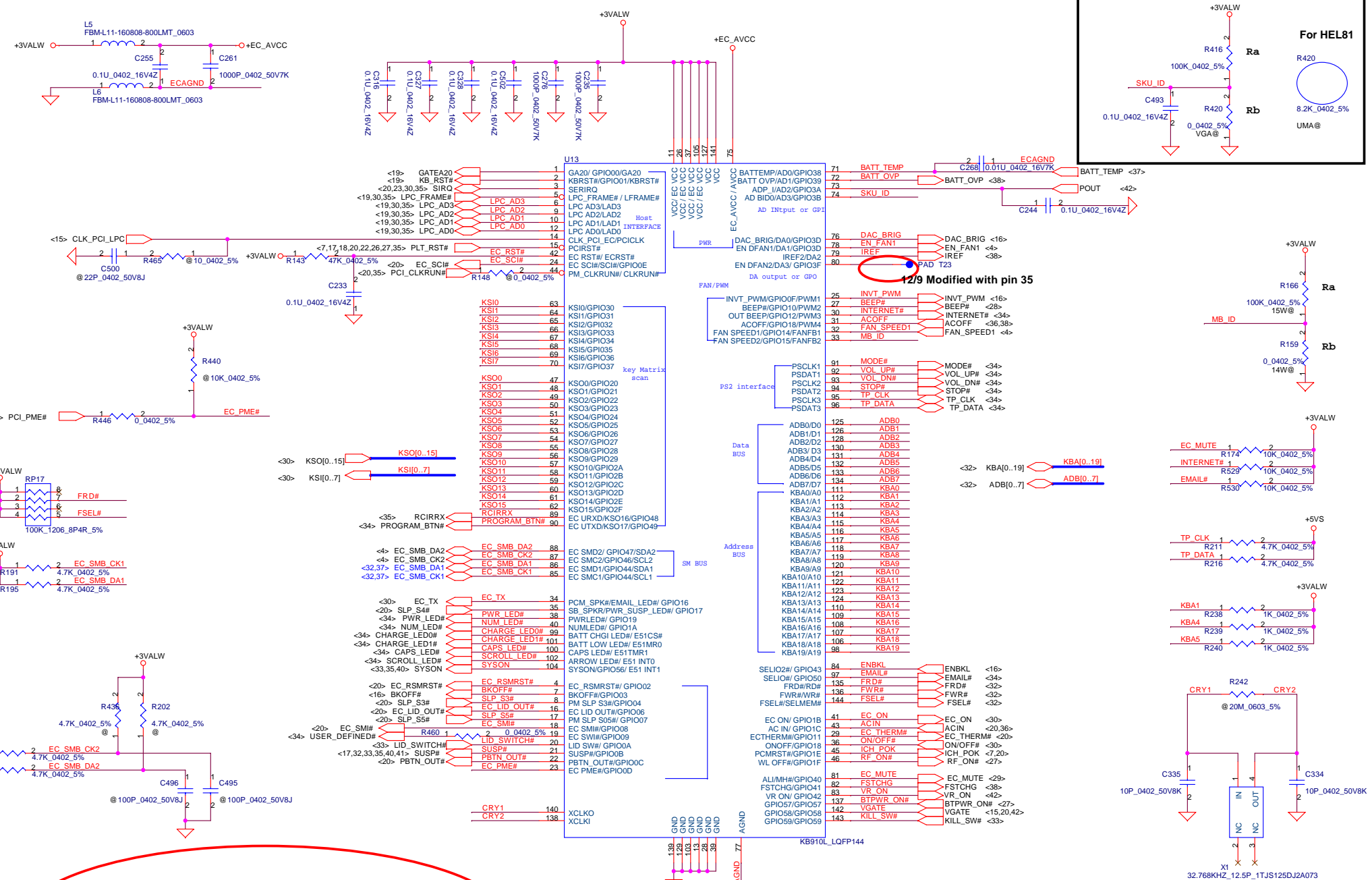
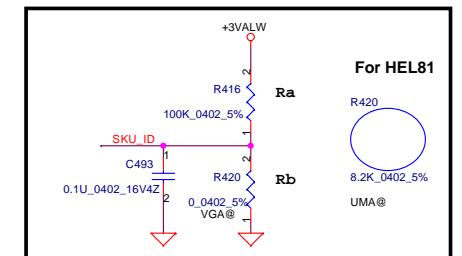


Not lead free



Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	<b>KBD,ON/OFF,TP,LED/B,DEBUG</b>
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Date:	Thursday, February 23, 2006	Sheet	30	of 43

Analog Board ID definition,  
Please see page 3.



Pin name	Pin number	2/20 New pin define
90	PROGRAM_BTN#	User-1
30	INTERNET#	User-2
97	EMAIL#	INTERNET
19	USER_DEFINED#	EMAIL

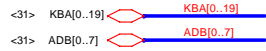
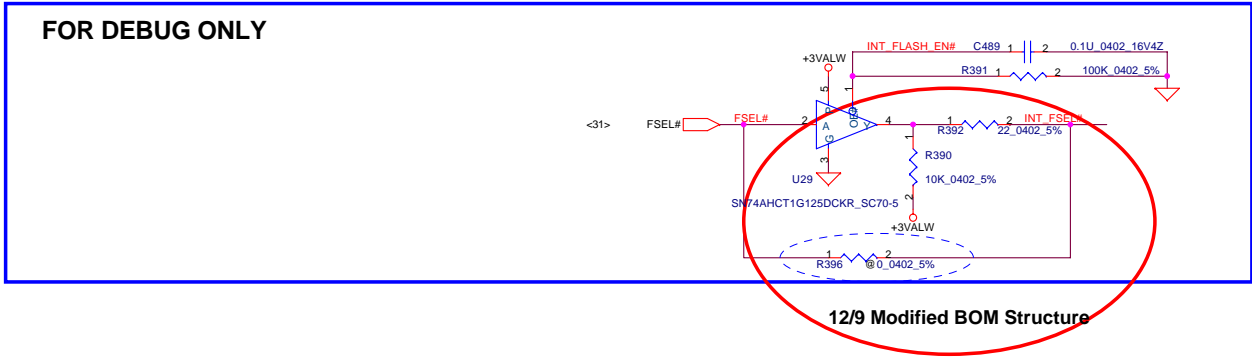
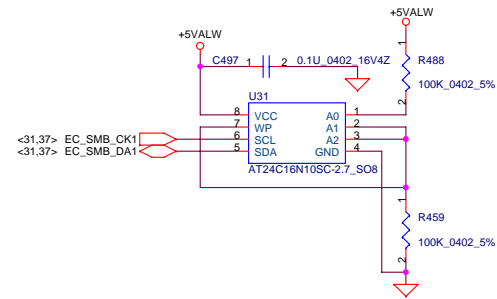
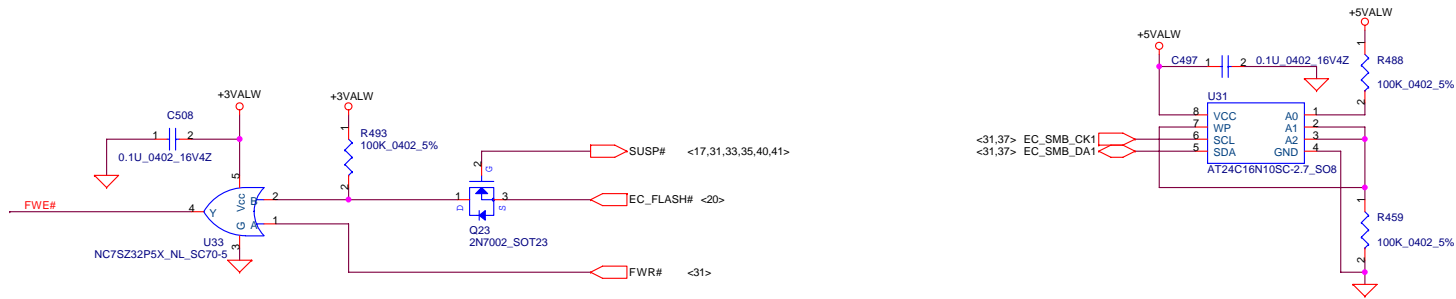
2/20 New added

Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
		2006/10/06

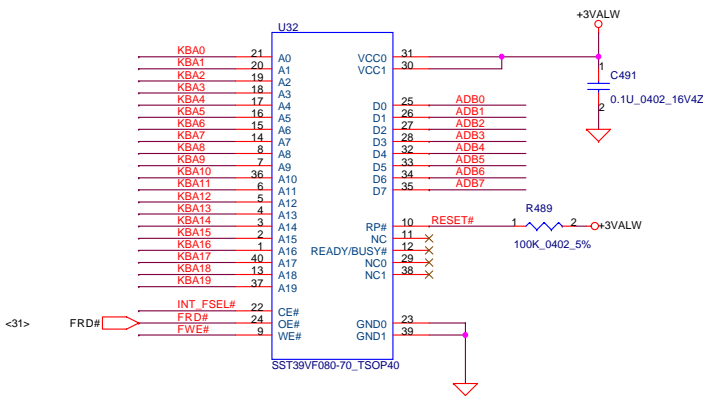
Title  
**Compal Electronics, Inc.**

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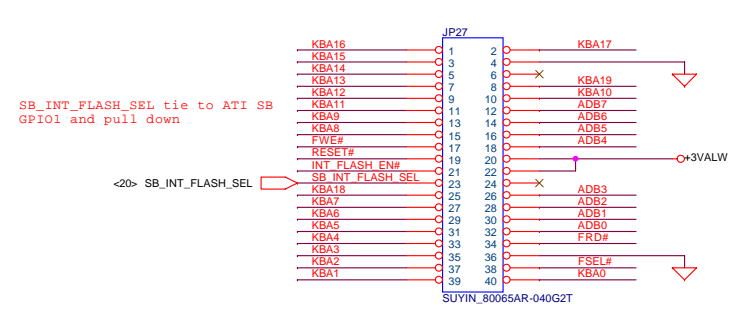
ENE-KB910L  
Size: Document Number  
Custom: HEL80 LA-3161P  
Date: Thursday, February 23, 2006  
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**1MB Flash ROM**



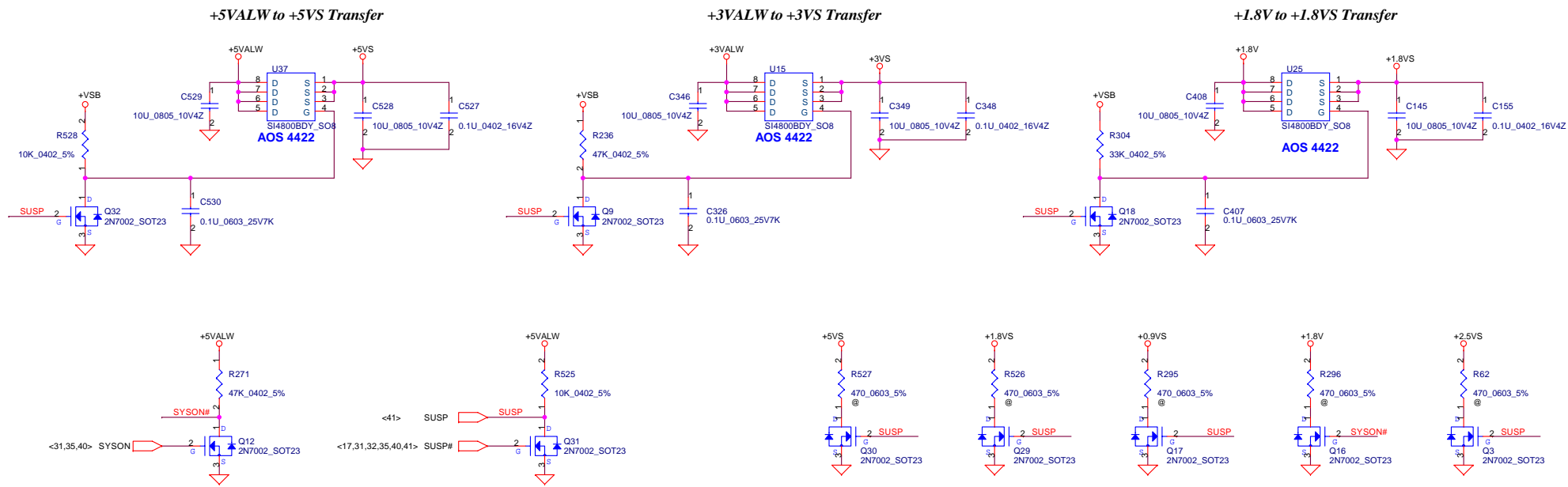
**1MB ROM Socket**



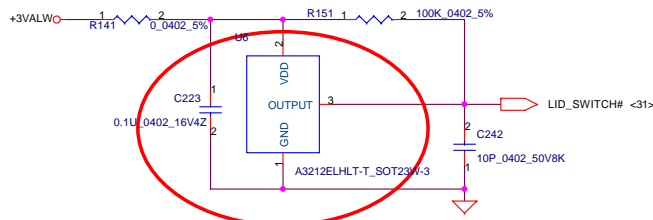
**Not Lead Free**

Security Classification	Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>BIOS &amp; EC I/O Port</b>	
Issued Date	2005/10/06	Deciphered Date		
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Title <b>BIOS &amp; EC I/O Port</b> Size Document Number <b>HEL80 LA-3161P</b> Date: Thursday, February 23, 2006
				Rev 0.2 Sheet 32 of 43

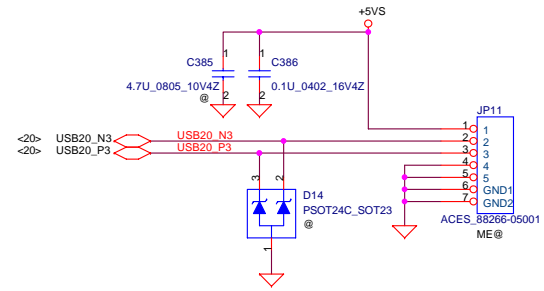




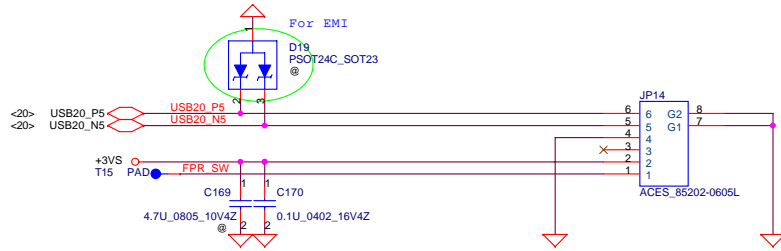
**LID Switch**



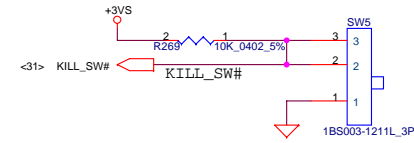
**CMOS Camera Conn**



**Finger Print board + MP3 Module CONN.**



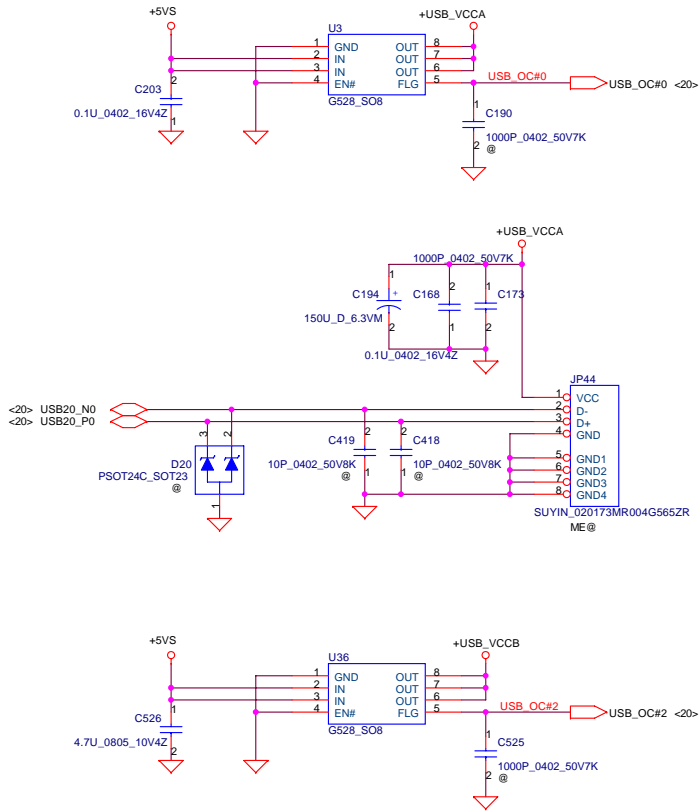
**Kill Switch**



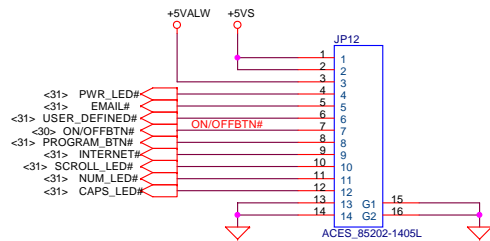
Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
		2006/10/06
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<b>Compal Electronics, Inc.</b>	
Title	<b>DC/DC Circuit</b>
Size	Document Number
Customer	<b>HEL80 LA-3161P</b>
Date:	Thursday, February 23, 2006
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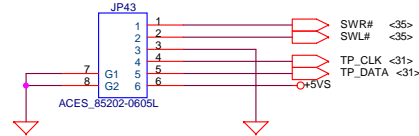
### USB Port



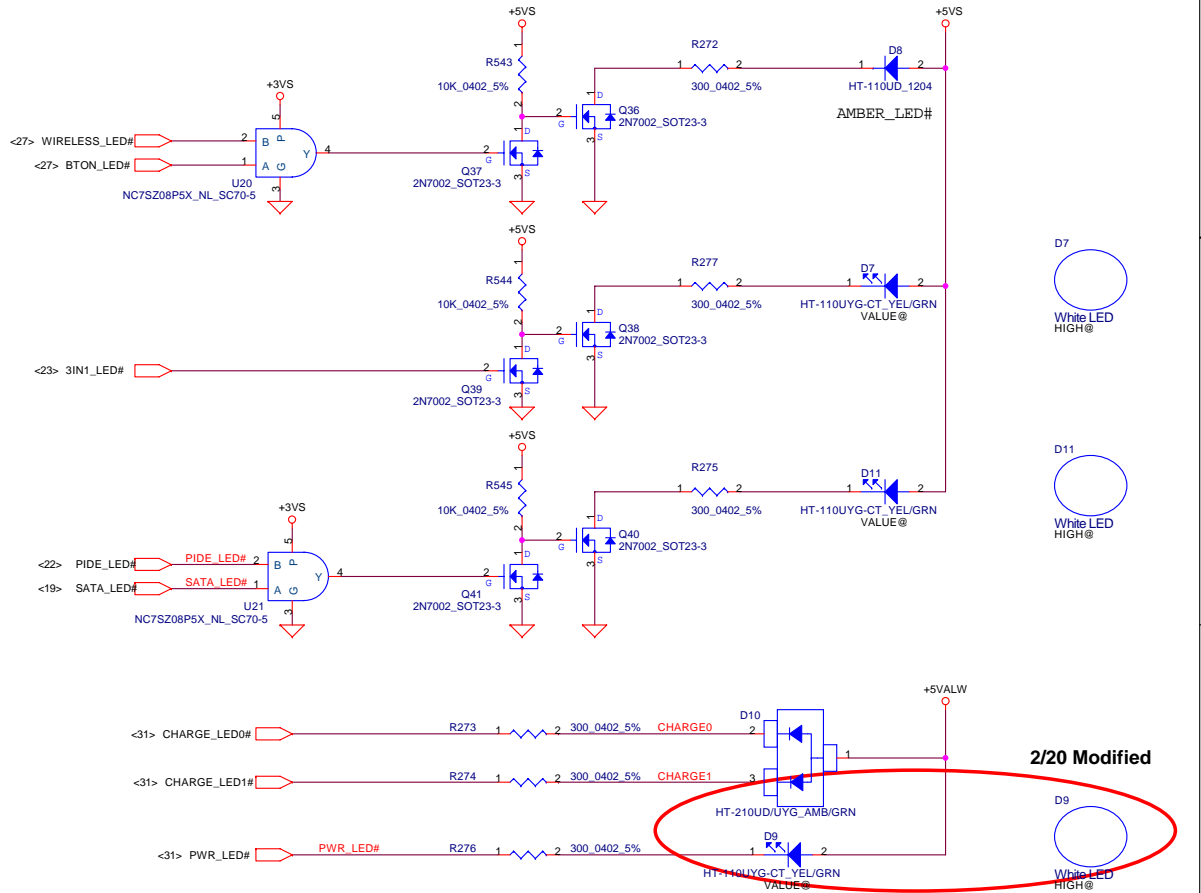
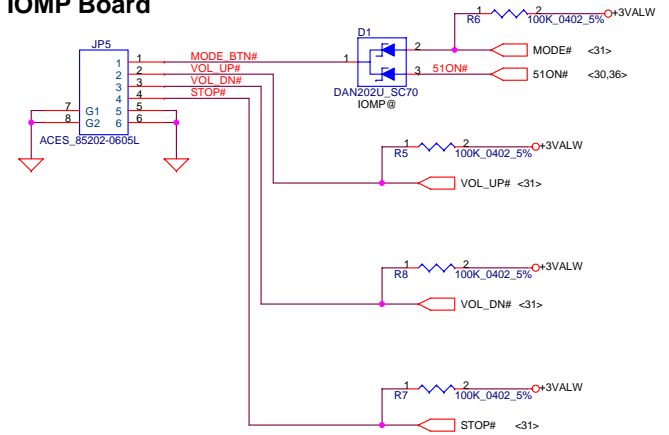
### Switch Board CONN.



### T/P Board

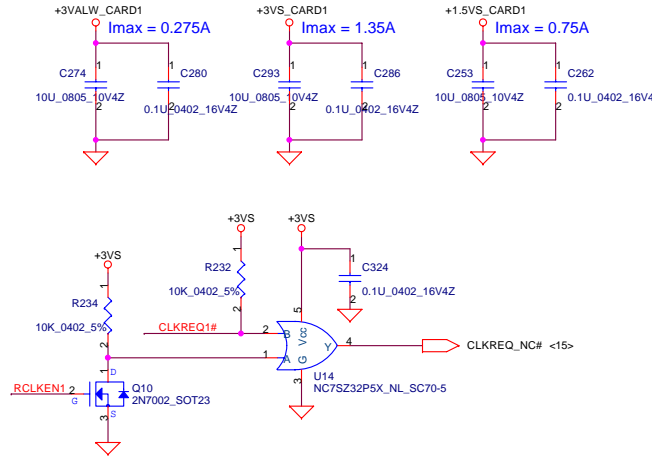
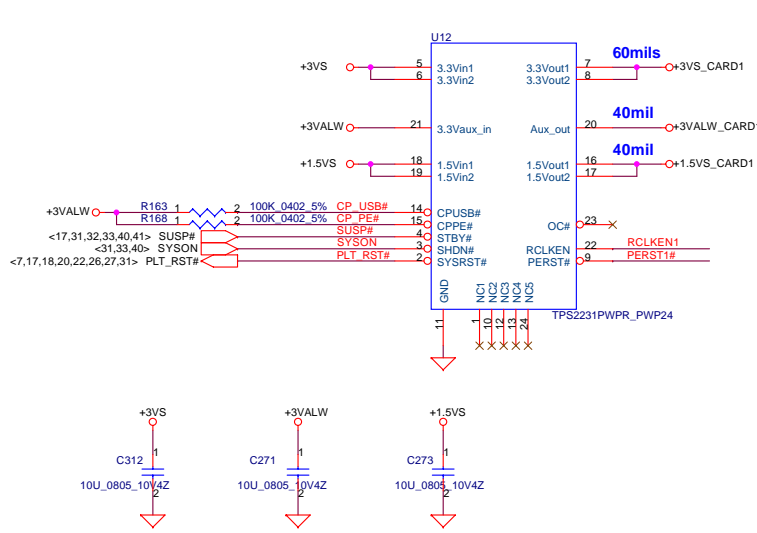


### IOMP Board

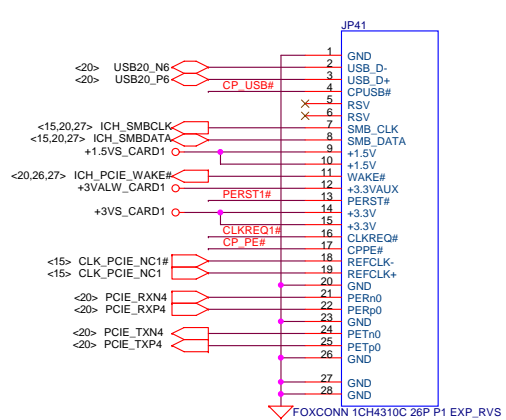


Security Classification		Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	INDICATE LED	
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				Custom	HEL80 LA-3161P
				Date:	Thursday, February 23, 2006
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				Rev	0.2

### New Card Power Switch

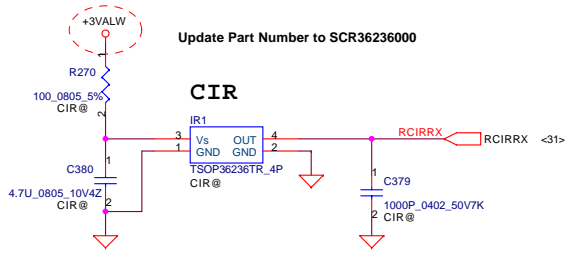


### New Card Socket (Left)



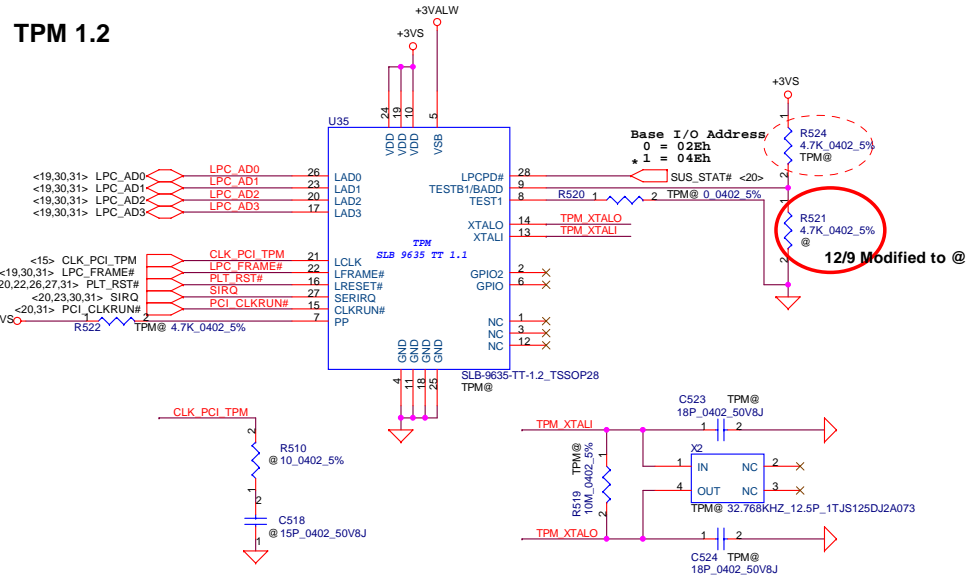
(NEW)  
 2005/11/4 Modified library pn:SP02000JC00  
 2005/12/9 Modified footprint to FOX\_1CX43201\_26P\_LB

### CIR

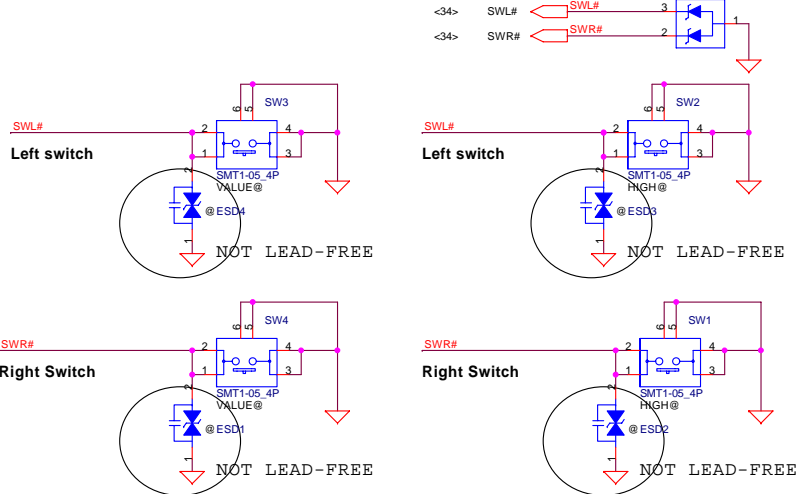


Update Part Number to SCR36236000

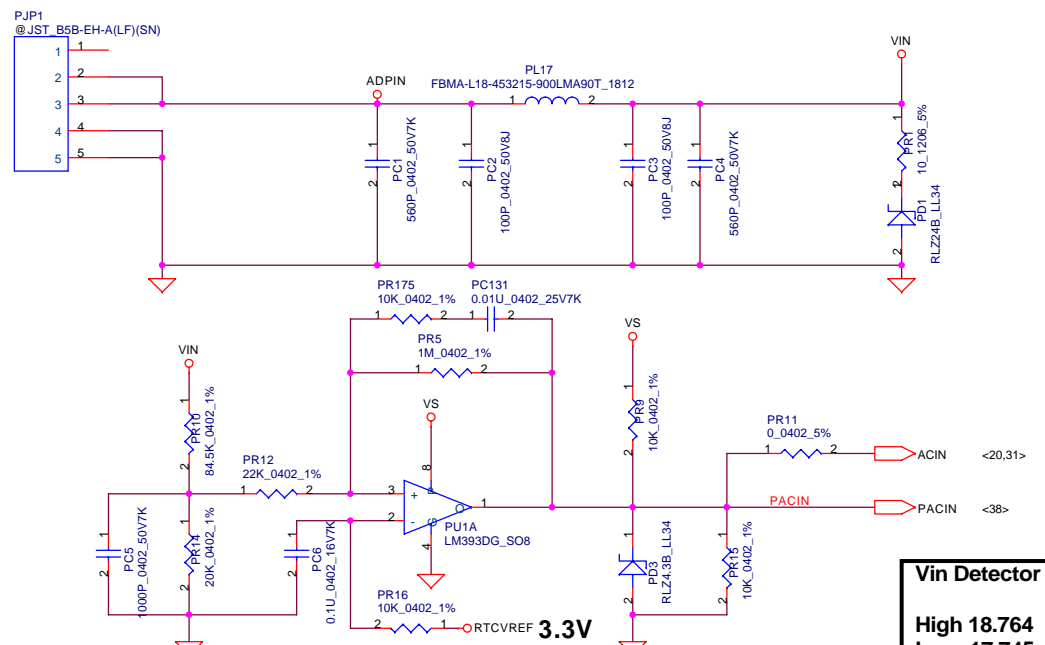
### TPM 1.2



Note : TPM IC Lead free status is MN



Security Classification		Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	New card	
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**Vin Detector**

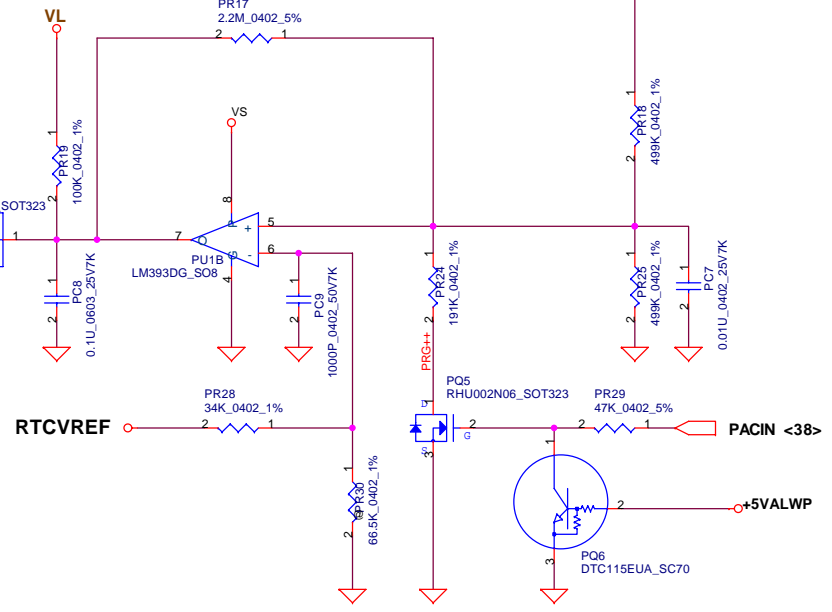
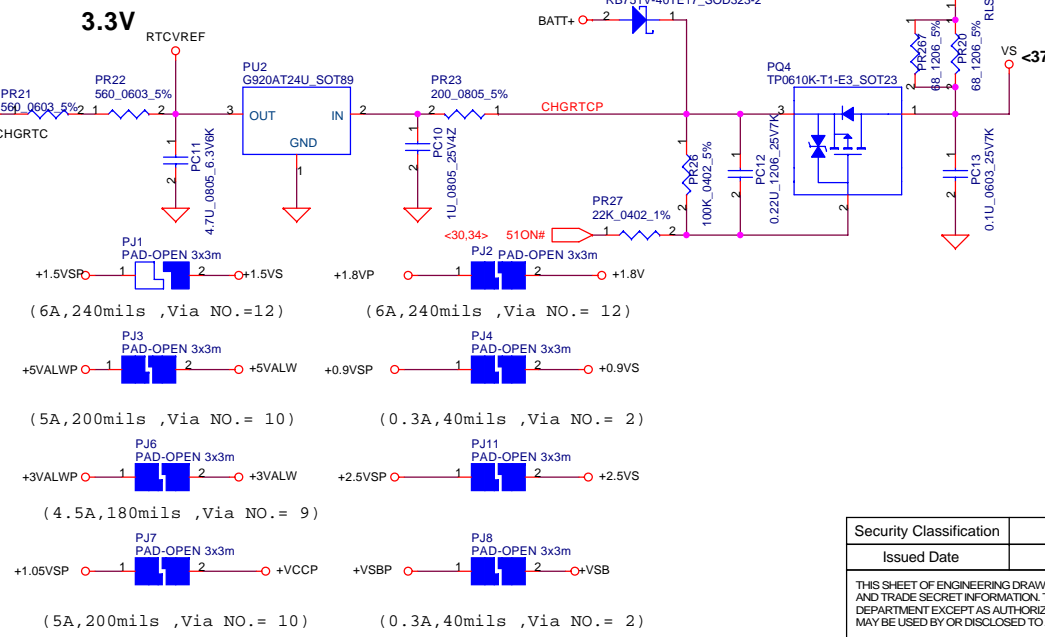
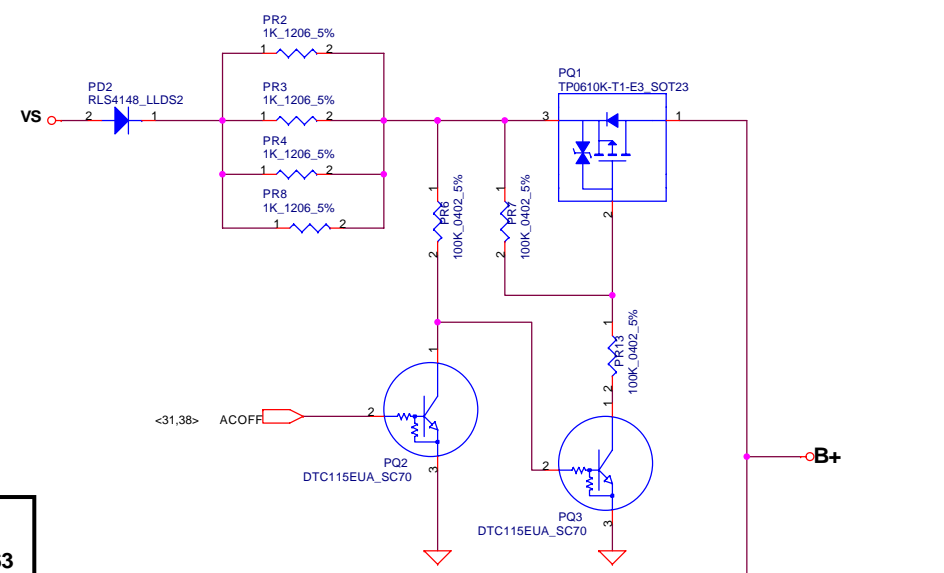
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

**ACIN**

	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

**BATT ONLY**

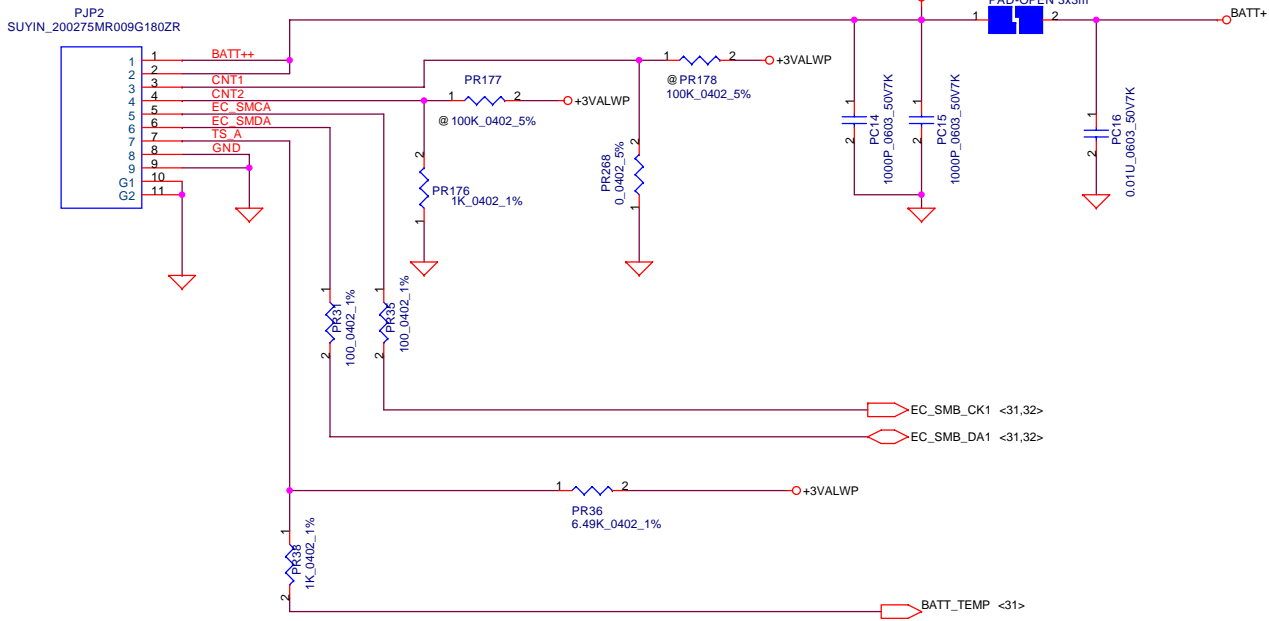
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



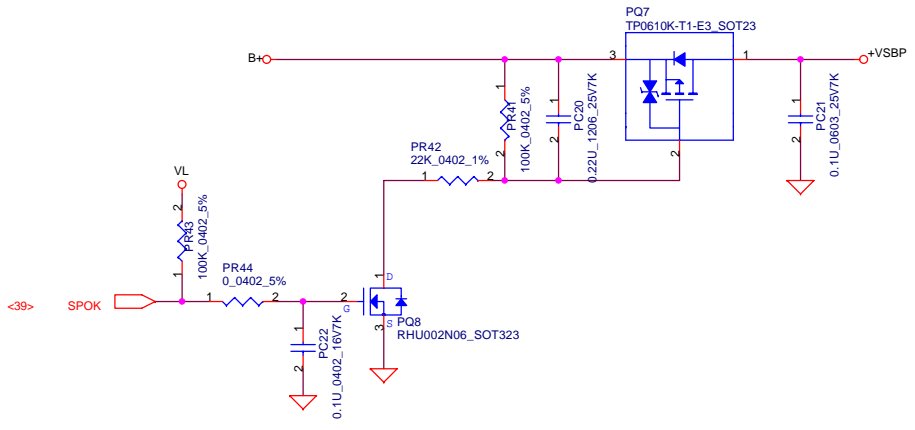
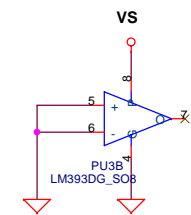
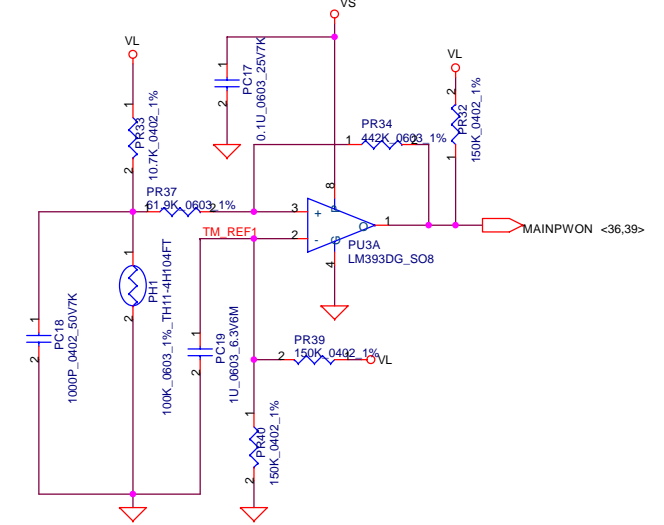
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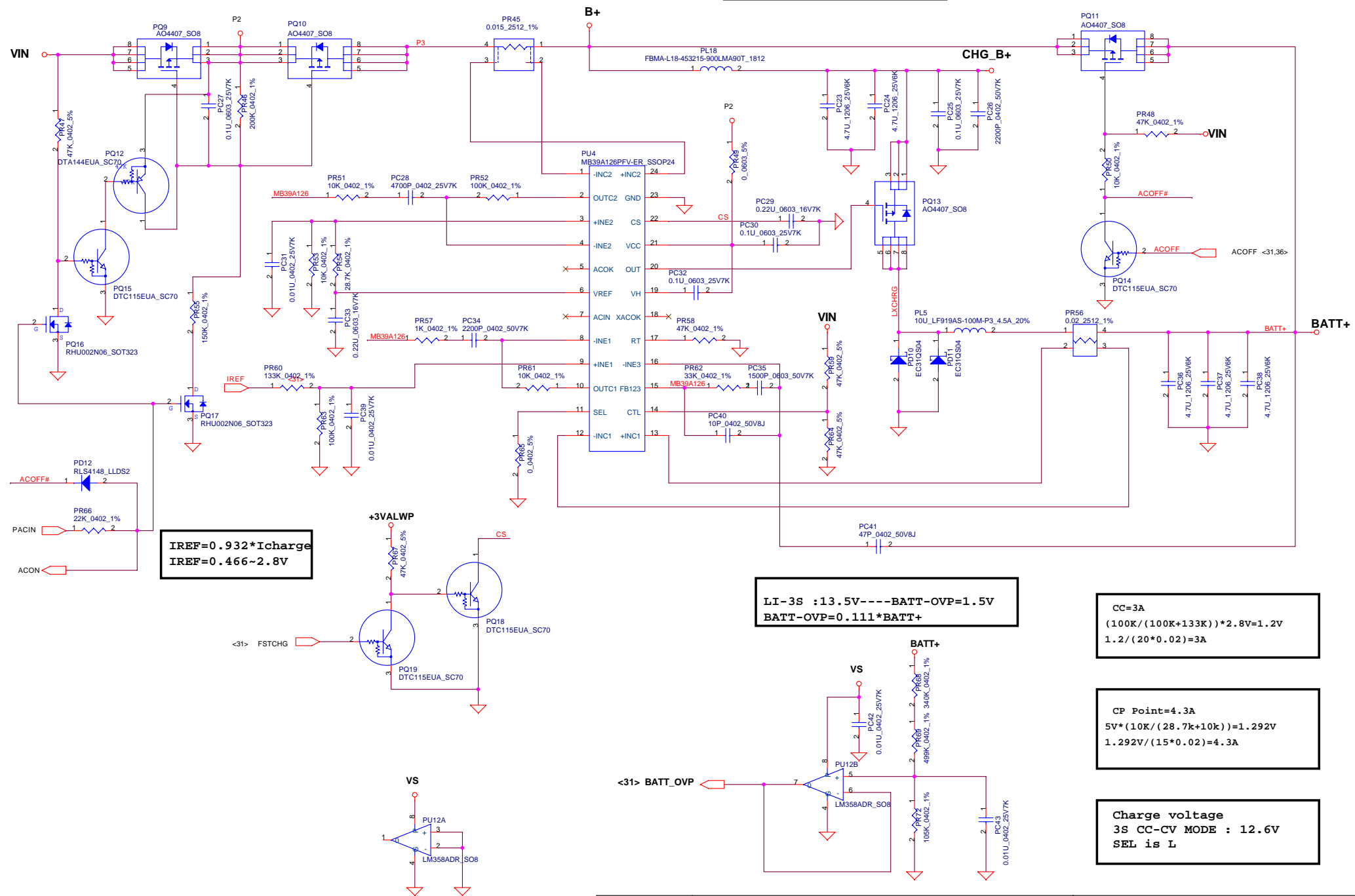
**PH1 under CPU bottom side :**  
 CPU thermal protection at 85 degree C  
 Recovery at 70 degree C



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75W PR45=0.02\_2512\_1% PR54=23.7K\_0402\_1% Iadp=0~3.71A  
 90W PR45=0.15\_2512\_1% PR54=28.7K\_0402\_1% Iadp=0~4.3A

Fosc=14100/Rt=14100/47=300KHz



$I_{REF} = 0.932 \cdot I_{charge}$   
 $I_{REF} = 0.466 \sim 2.8V$

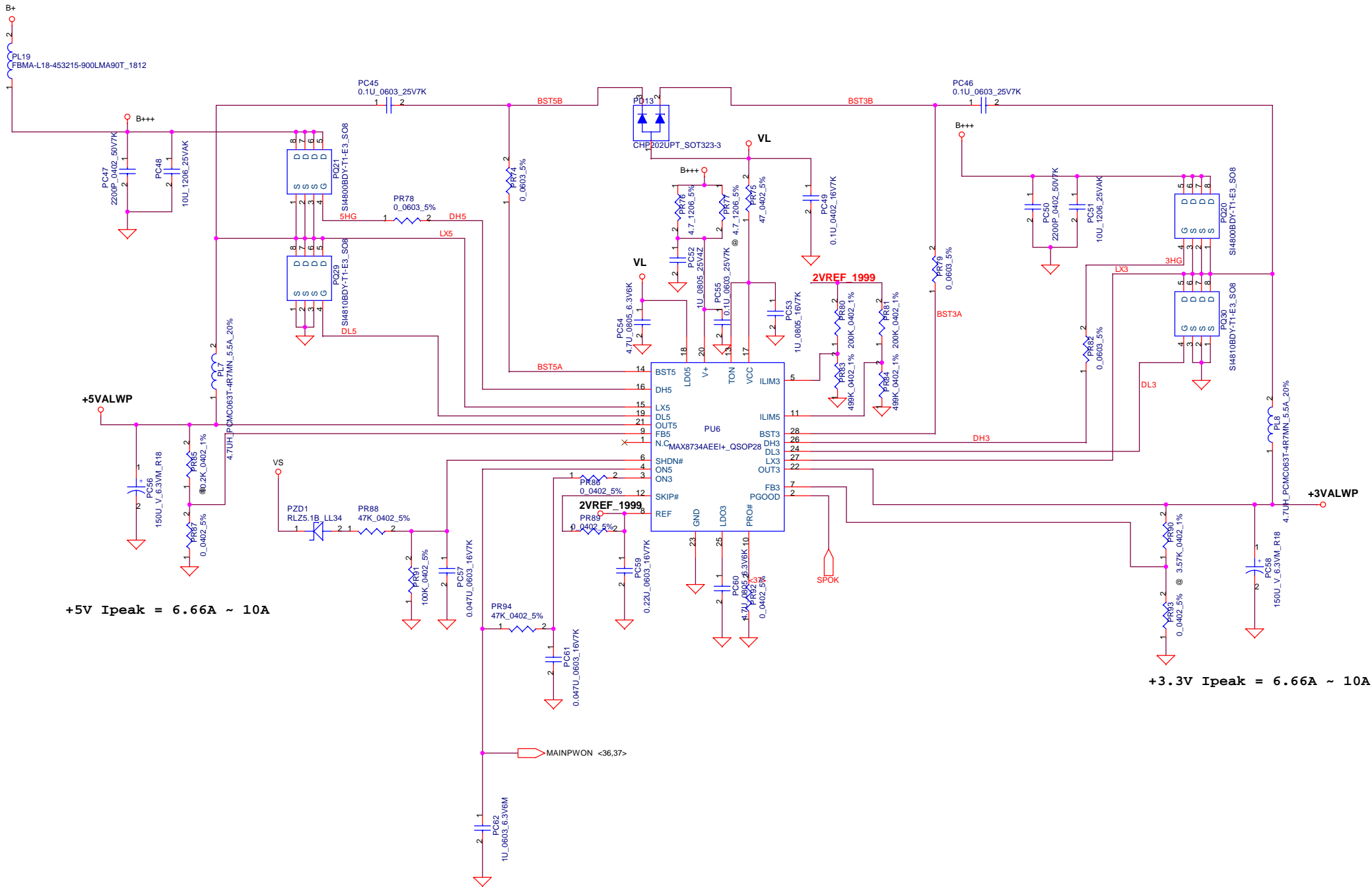
LI-3S : 13.5V --- BATT-OVP=1.5V  
 $BATT-OVP = 0.111 \cdot BATT+$

CC=3A  
 $(100K / (100K + 133K)) \cdot 2.8V = 1.2V$   
 $1.2 / (20 \cdot 0.02) = 3A$

CP Point=4.3A  
 $5V \cdot (10K / (28.7K + 10K)) = 1.292V$   
 $1.292V / (15 \cdot 0.02) = 4.3A$

Charge voltage  
 3S CC-CV MODE : 12.6V  
 SEL is L

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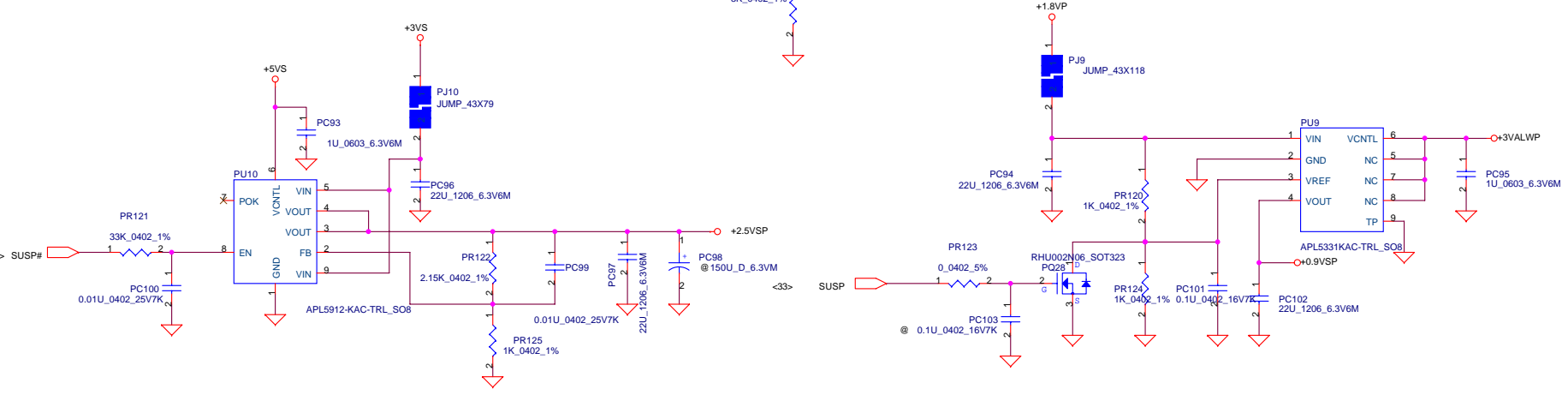
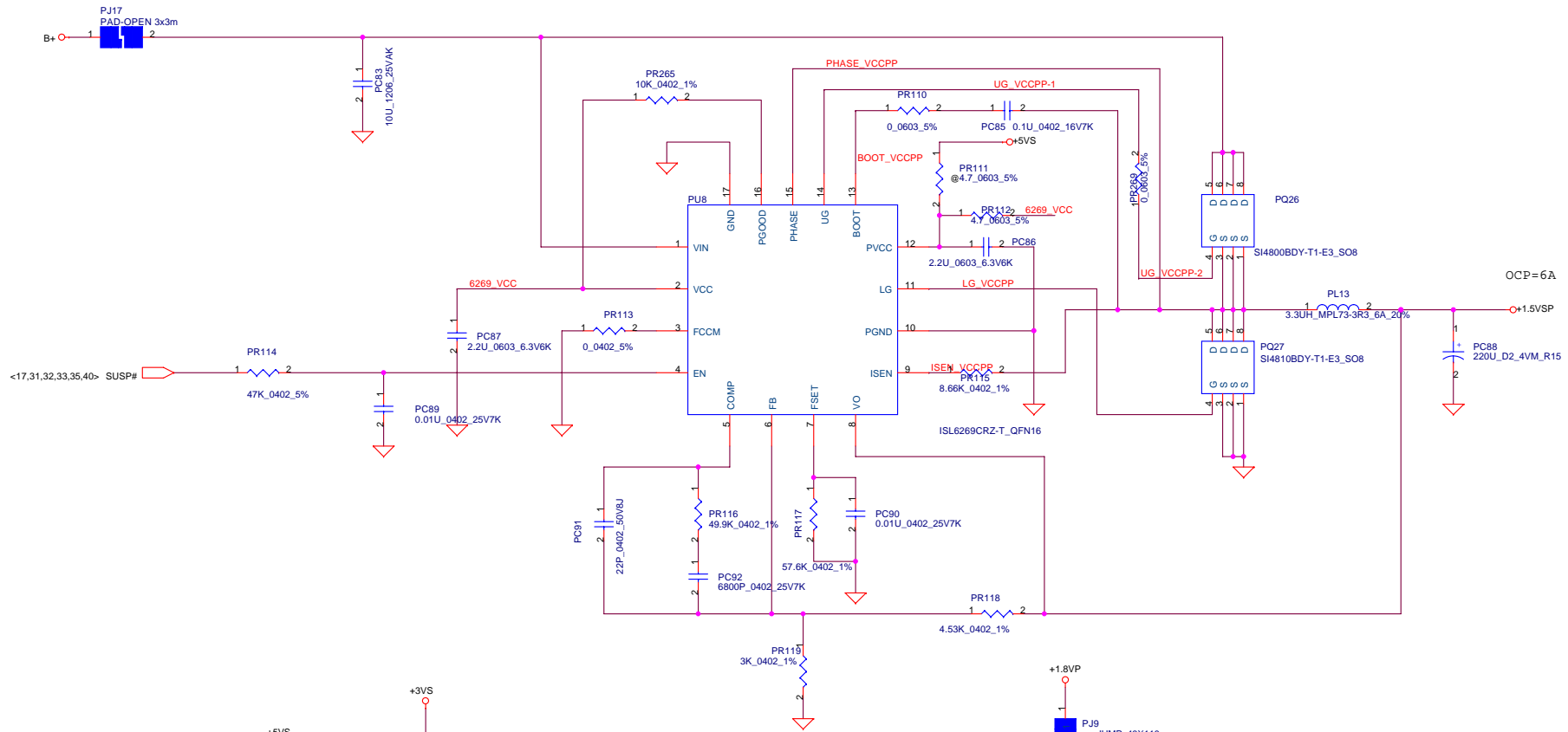
**+5V Ipeak = 6.66A ~ 10A**

**+3.3V Ipeak = 6.66A ~ 10A**

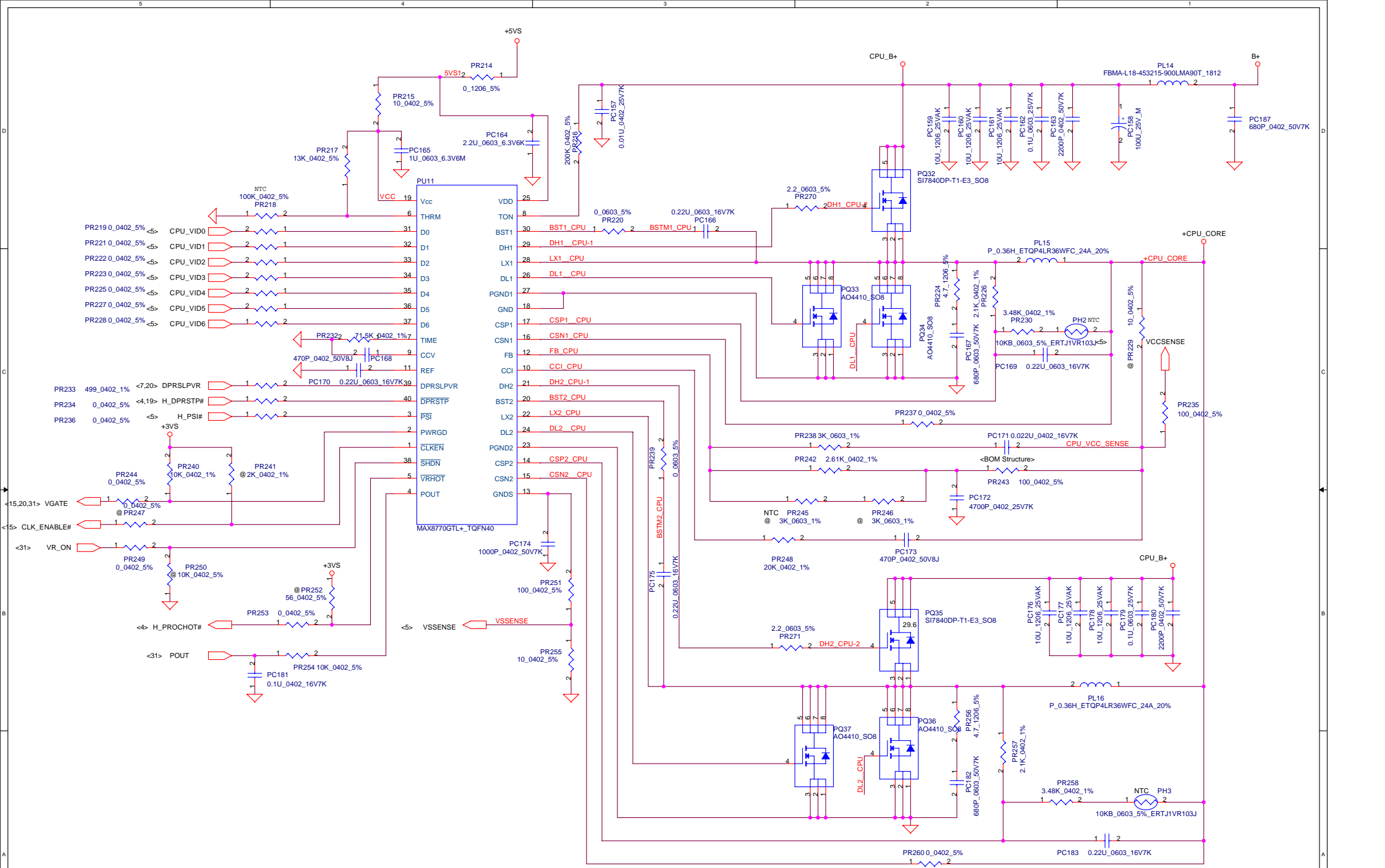
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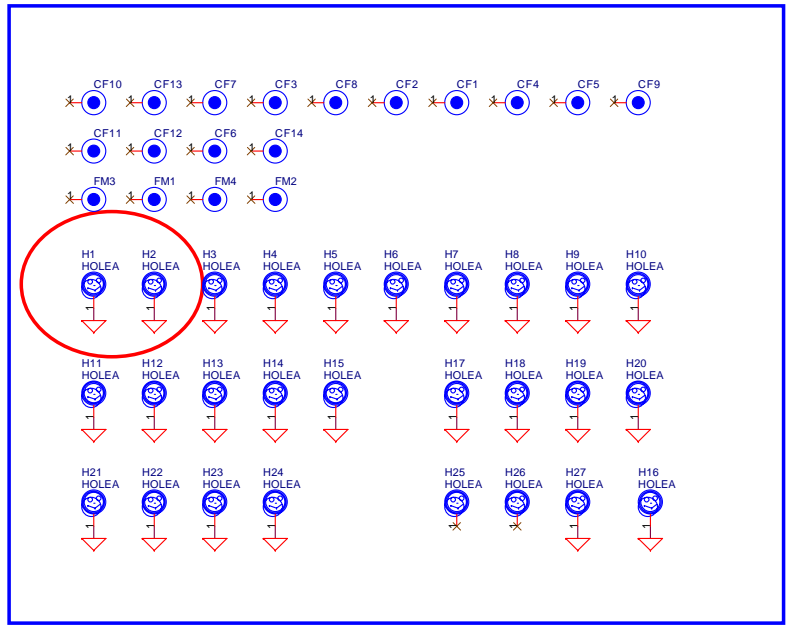




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