

# Compal Confidential

## Schematics Document

AMD Turion/Sempron + Nvidia MCP67-MV

2007-01-12

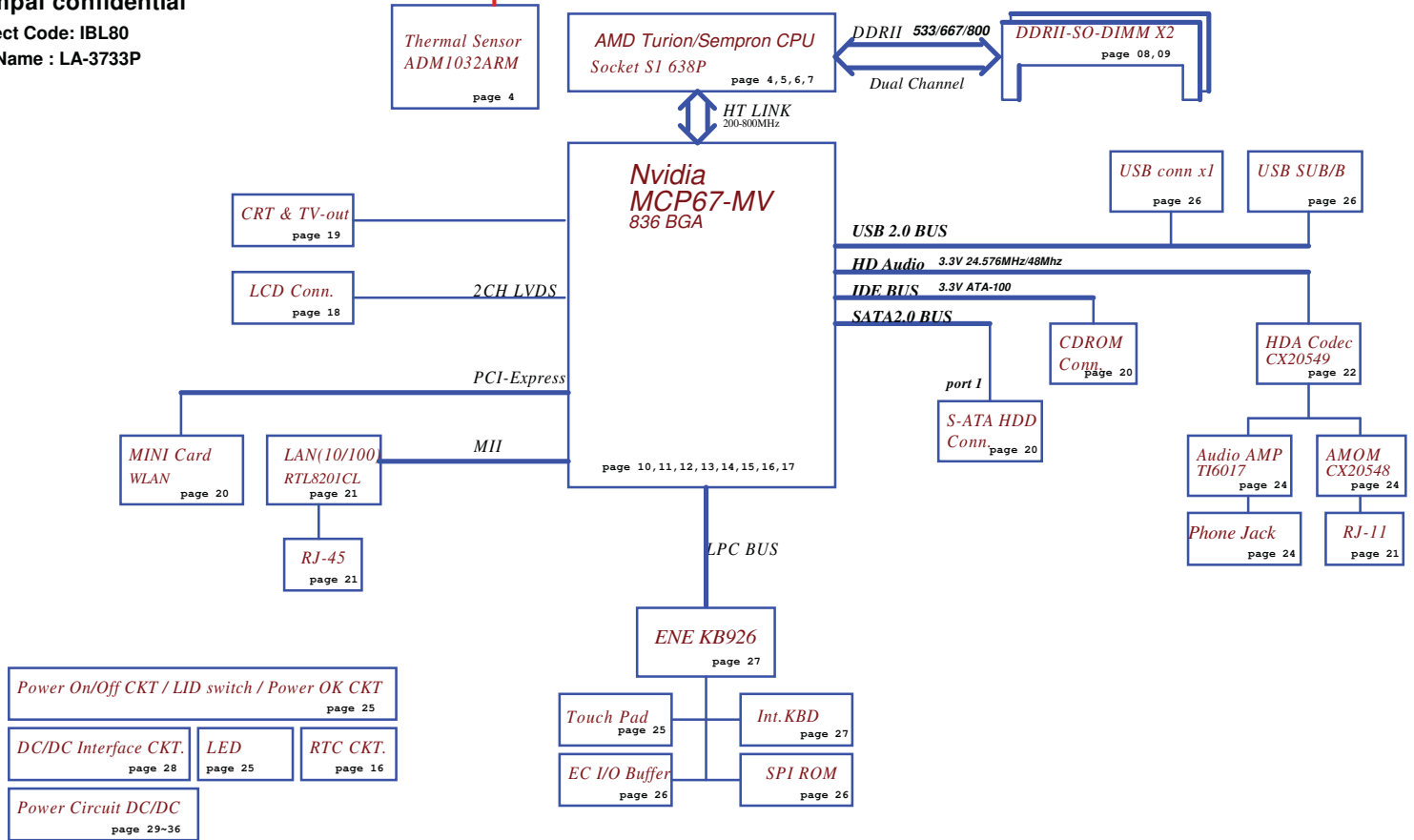
Rev: 0.1



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Issued Date	2007/01/07	Deciphered Date	2008/01/12	Title		
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Project Code: IBL80  
File Name : LA-3733P



Security Classification	Compal Secret Data		Title	BLOCK DIAGRAM
Issued Date	2007/01/07	Deciphered Date	2008/01/12	Size
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### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON*
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Rd	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

### External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts

### BTO Option Table

BTO Item	BOM Structure
DIP CAP & RTC	45@

### EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

### EC SM Bus2 address

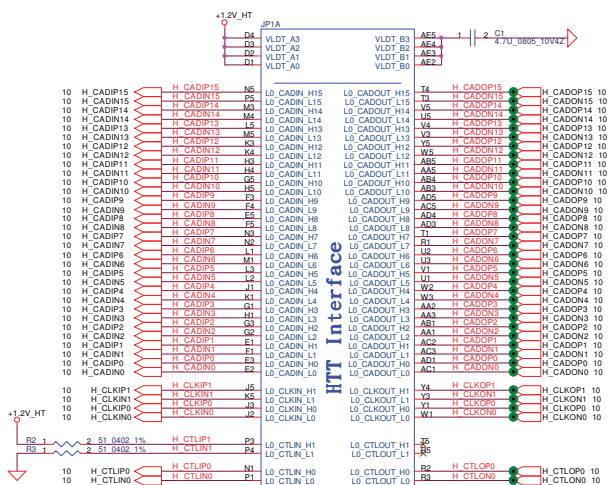
### MCP67 SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb
MINI CARD	

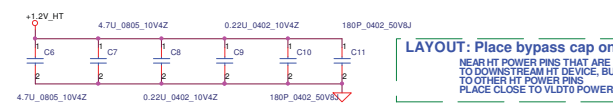
Security Classification	Compal Secret Data		Title	TABLE OF CONTENTS
Issued Date	2007/01/07	Deciphered Date	2008/01/12	Size
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PROCESSOR HYPERTRANSPORT INTERFACE

VLD1\_Ax AND VLD1\_Bx ARE CONNECTED TO THE LDT RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE BOARD. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

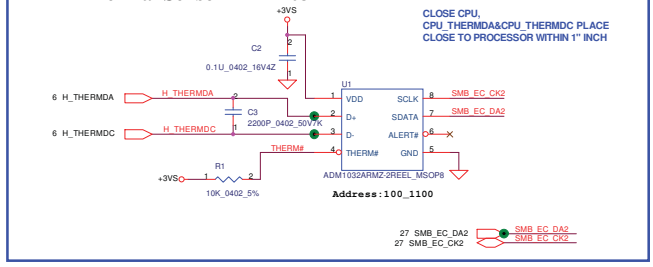


FIG\_P24 (REV. 2) 2410-1113  
Athlon 64-91  
Processor Socket



LAYOUT: Place bypass cap on top side of board NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS PLACE CLOSE TO VLD10 POWER PINS

Thermal Sensor ADM1032ARMZ



PWM Fan Control circuit

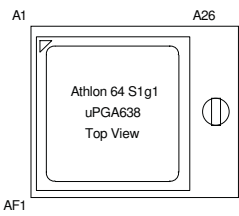
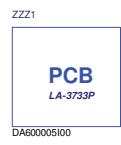
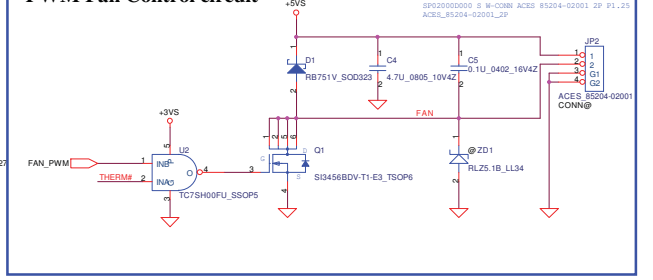
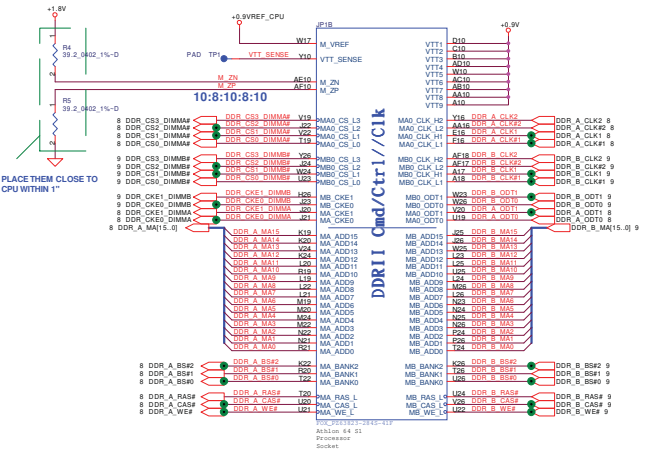


Table with columns for Security Classification, Issued Date, Deciphered Date, Title (AMD CPU HT I/F), and other metadata.

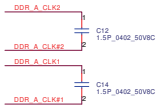
VDD\_VTT\_SUS\_CPU IS CONNECTED TO THE VDD\_VTT\_SUS\_POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE IT IS ONLY CONNECTED ON THE BOARD TO OCCURRY JUMP NEAR THE CPU PACKAGE



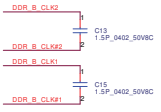
PLACE THEM CLOSE TO CPU WITHIN 1"

To reverse SODIMM socket

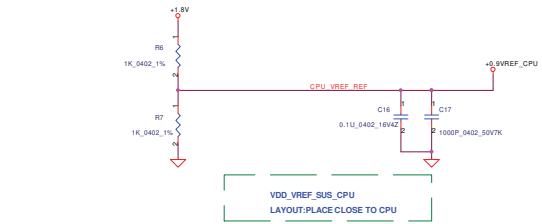
To normal SODIMM socket



PLACE CLOSE TO PROCESSOR WITHIN 1.2 INCH

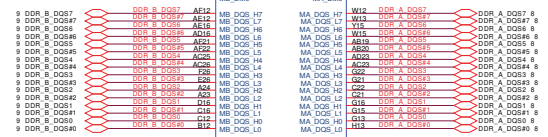


PLACE CLOSE TO PROCESSOR WITHIN 1.2 INCH



9 DDR\_B\_DM[7..0]

DDR\_A\_DM[7..0]

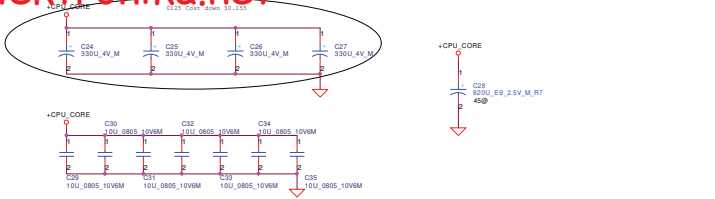
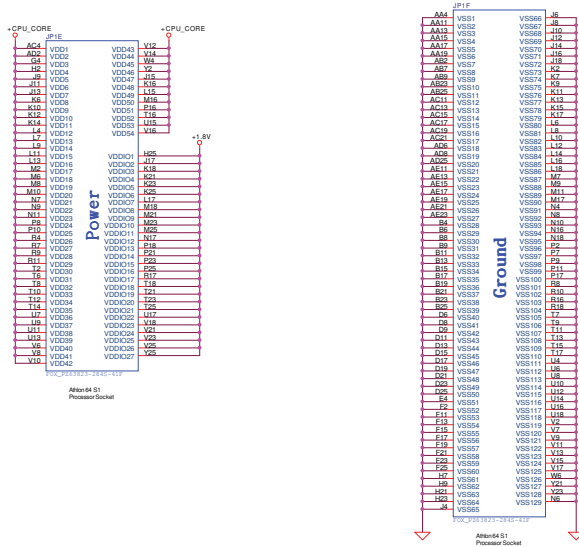


9 DDR\_B\_DM[7..0]

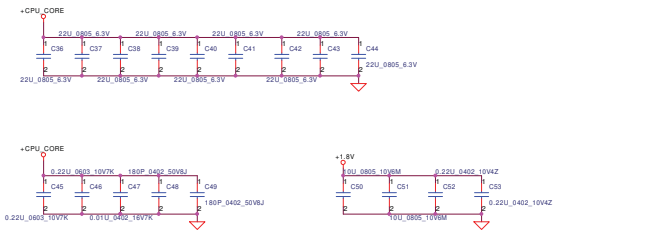
DDR\_A\_DM[7..0]



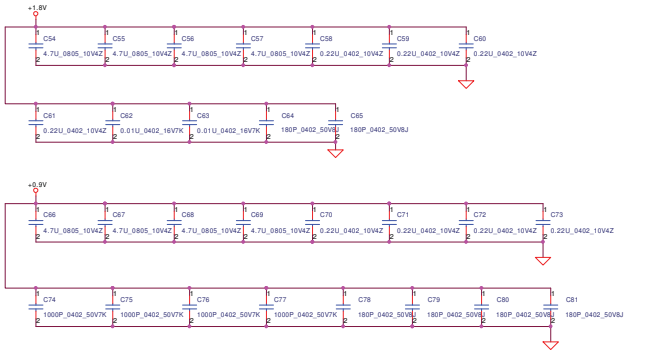
# PROCESSOR POWER AND GROUND



## CPU SOCKET S1 DECOUPLING



## DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE

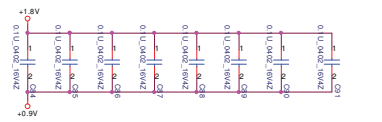


- 5 DDR\_A\_D0[63] (DDR A D0\_63)
- 5 DDR\_A\_DM0[7] (DDR A DM0\_7)
- 5 DDR\_A\_D0S0[7] (DDR A D0S0\_7)
- 5 DDR\_A\_MA0[15] (DDR A MA0\_15)
- 5 DDR\_A\_D0S0[0-7] (DDR A D0S0\_0-7)

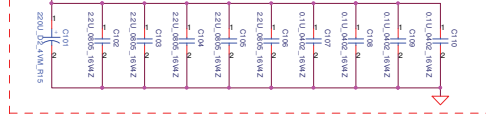
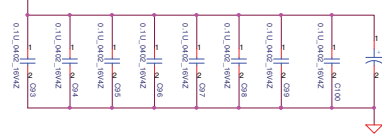


**DIMM1 REV H:4mm (BOT)**

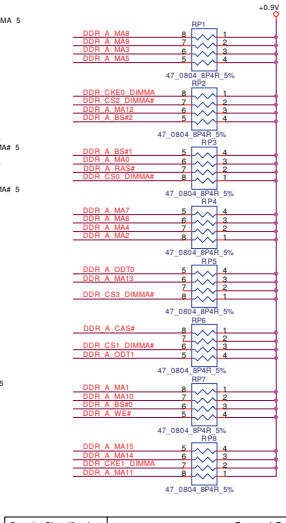
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



- 5 DDR\_CKE0\_DIMMA (DDR\_CKE0\_DIMMA)
- 5 DDR\_CS2\_DIMMA# (DDR\_CS2\_DIMMA#)
- 5 DDR\_A\_BS2# (DDR\_A\_BS2#)
- 5 DDR\_A\_MA1# (DDR A MA1#)
- 5 DDR\_A\_MA2# (DDR A MA2#)
- 5 DDR\_A\_MA3# (DDR A MA3#)
- 5 DDR\_A\_MA1 (DDR A MA1)
- 5 DDR\_A\_MA10 (DDR A MA10)
- 5 DDR\_A\_BS0# (DDR A BS0#)
- 5 DDR\_A\_WE# (DDR A WE#)
- 5 DDR\_A\_CAS# (DDR A CAS#)
- 5 DDR\_CS1\_DIMMA# (DDR\_CS1\_DIMMA#)
- 5 DDR\_A\_ODT1 (DDR A ODT1)

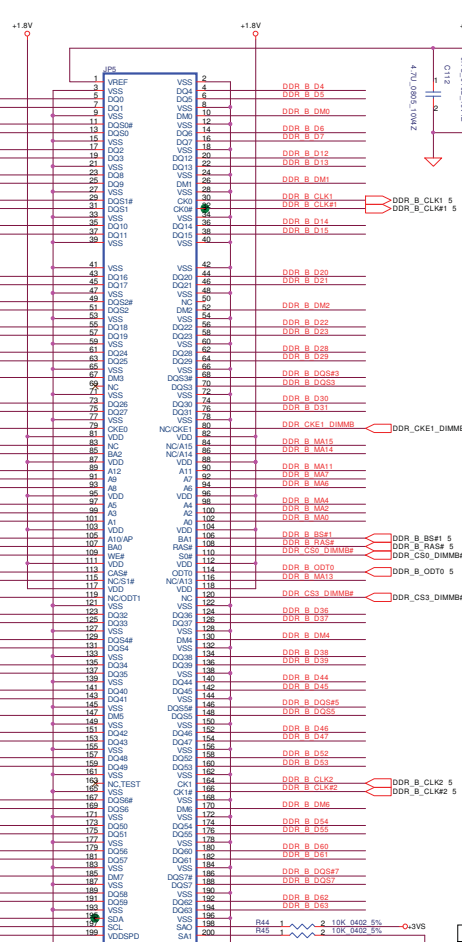


Security Classification		2007/01/07		Compal Secret Data	
Issued Date	Deciphered Date	2008/01/12			
Title: <b>DDR2 SO-DIMM I</b>					
Size	Document Number				
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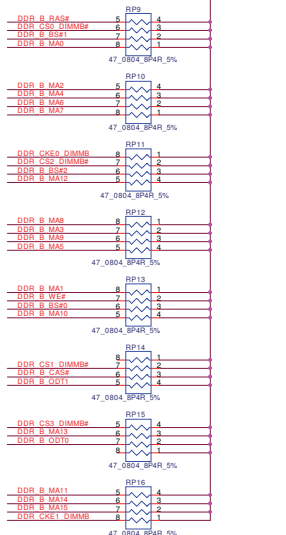
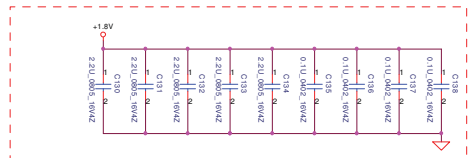
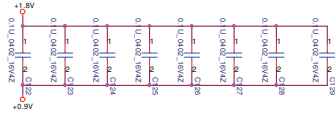
- 5 DDR\_B\_D0[0..63] **DDR B D0\_63I**
- 5 DDR\_B\_DM0[7] **DDR B DM0\_7I**
- 5 DDR\_B\_DOS0[7] **DDR B DOS0\_7I**
- 5 DDR\_B\_MA0[15] **DDR B MA0\_15I**
- 5 DDR\_B\_DOS0[0..7] **DDR B DOS0\_7I**



- 5 DDR\_CKE0\_DIMMB **DDR\_CKE0\_DIMMB**
- 5 DDR\_CS2\_DIMMB **DDR\_CS2\_DIMMB**
- 5 DDR\_B\_BS#2 **DDR B BS#2**
- 5 DDR\_B\_MA#2 **DDR B MA#2**
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- 5 DDR\_B\_MA#4 **DDR B MA#4**
- 5 DDR\_B\_MA#5 **DDR B MA#5**
- 5 DDR\_B\_MA#6 **DDR B MA#6**
- 5 DDR\_B\_MA#7 **DDR B MA#7**
- 5 DDR\_B\_MA#8 **DDR B MA#8**
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- 5 DDR\_B\_MA#18 **DDR B MA#18**
- 5 DDR\_B\_MA#19 **DDR B MA#19**
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- 5 DDR\_B\_MA#44 **DDR B MA#44**
- 5 DDR\_B\_MA#45 **DDR B MA#45**
- 5 DDR\_B\_MA#46 **DDR B MA#46**
- 5 DDR\_B\_MA#47 **DDR B MA#47**
- 5 DDR\_B\_MA#48 **DDR B MA#48**
- 5 DDR\_B\_MA#49 **DDR B MA#49**
- 5 DDR\_B\_MA#50 **DDR B MA#50**
- 5 DDR\_B\_MA#51 **DDR B MA#51**
- 5 DDR\_B\_MA#52 **DDR B MA#52**
- 5 DDR\_B\_MA#53 **DDR B MA#53**
- 5 DDR\_B\_MA#54 **DDR B MA#54**
- 5 DDR\_B\_MA#55 **DDR B MA#55**
- 5 DDR\_B\_MA#56 **DDR B MA#56**
- 5 DDR\_B\_MA#57 **DDR B MA#57**
- 5 DDR\_B\_MA#58 **DDR B MA#58**
- 5 DDR\_B\_MA#59 **DDR B MA#59**
- 5 DDR\_B\_MA#60 **DDR B MA#60**
- 5 DDR\_B\_MA#61 **DDR B MA#61**
- 5 DDR\_B\_MA#62 **DDR B MA#62**
- 5 DDR\_B\_MA#63 **DDR B MA#63**
- 5 DDR\_B\_MA#64 **DDR B MA#64**
- 5 DDR\_B\_MA#65 **DDR B MA#65**
- 5 DDR\_B\_MA#66 **DDR B MA#66**
- 5 DDR\_B\_MA#67 **DDR B MA#67**
- 5 DDR\_B\_MA#68 **DDR B MA#68**
- 5 DDR\_B\_MA#69 **DDR B MA#69**
- 5 DDR\_B\_MA#70 **DDR B MA#70**
- 5 DDR\_B\_MA#71 **DDR B MA#71**
- 5 DDR\_B\_MA#72 **DDR B MA#72**
- 5 DDR\_B\_MA#73 **DDR B MA#73**
- 5 DDR\_B\_MA#74 **DDR B MA#74**
- 5 DDR\_B\_MA#75 **DDR B MA#75**
- 5 DDR\_B\_MA#76 **DDR B MA#76**
- 5 DDR\_B\_MA#77 **DDR B MA#77**
- 5 DDR\_B\_MA#78 **DDR B MA#78**
- 5 DDR\_B\_MA#79 **DDR B MA#79**
- 5 DDR\_B\_MA#80 **DDR B MA#80**
- 5 DDR\_B\_MA#81 **DDR B MA#81**
- 5 DDR\_B\_MA#82 **DDR B MA#82**
- 5 DDR\_B\_MA#83 **DDR B MA#83**
- 5 DDR\_B\_MA#84 **DDR B MA#84**
- 5 DDR\_B\_MA#85 **DDR B MA#85**
- 5 DDR\_B\_MA#86 **DDR B MA#86**
- 5 DDR\_B\_MA#87 **DDR B MA#87**
- 5 DDR\_B\_MA#88 **DDR B MA#88**
- 5 DDR\_B\_MA#89 **DDR B MA#89**
- 5 DDR\_B\_MA#90 **DDR B MA#90**
- 5 DDR\_B\_MA#91 **DDR B MA#91**
- 5 DDR\_B\_MA#92 **DDR B MA#92**
- 5 DDR\_B\_MA#93 **DDR B MA#93**
- 5 DDR\_B\_MA#94 **DDR B MA#94**
- 5 DDR\_B\_MA#95 **DDR B MA#95**
- 5 DDR\_B\_MA#96 **DDR B MA#96**
- 5 DDR\_B\_MA#97 **DDR B MA#97**
- 5 DDR\_B\_MA#98 **DDR B MA#98**
- 5 DDR\_B\_MA#99 **DDR B MA#99**
- 5 DDR\_B\_MA#100 **DDR B MA#100**
- 5 DDR\_B\_MA#101 **DDR B MA#101**
- 5 DDR\_B\_MA#102 **DDR B MA#102**
- 5 DDR\_B\_MA#103 **DDR B MA#103**
- 5 DDR\_B\_MA#104 **DDR B MA#104**
- 5 DDR\_B\_MA#105 **DDR B MA#105**
- 5 DDR\_B\_MA#106 **DDR B MA#106**
- 5 DDR\_B\_MA#107 **DDR B MA#107**
- 5 DDR\_B\_MA#108 **DDR B MA#108**
- 5 DDR\_B\_MA#109 **DDR B MA#109**
- 5 DDR\_B\_MA#110 **DDR B MA#110**
- 5 DDR\_B\_MA#111 **DDR B MA#111**
- 5 DDR\_B\_MA#112 **DDR B MA#112**
- 5 DDR\_B\_MA#113 **DDR B MA#113**
- 5 DDR\_B\_MA#114 **DDR B MA#114**
- 5 DDR\_B\_MA#115 **DDR B MA#115**
- 5 DDR\_B\_MA#116 **DDR B MA#116**
- 5 DDR\_B\_MA#117 **DDR B MA#117**
- 5 DDR\_B\_MA#118 **DDR B MA#118**
- 5 DDR\_B\_MA#119 **DDR B MA#119**
- 5 DDR\_B\_MA#120 **DDR B MA#120**
- 5 DDR\_B\_MA#121 **DDR B MA#121**
- 5 DDR\_B\_MA#122 **DDR B MA#122**
- 5 DDR\_B\_MA#123 **DDR B MA#123**
- 5 DDR\_B\_MA#124 **DDR B MA#124**
- 5 DDR\_B\_MA#125 **DDR B MA#125**
- 5 DDR\_B\_MA#126 **DDR B MA#126**
- 5 DDR\_B\_MA#127 **DDR B MA#127**
- 5 DDR\_B\_MA#128 **DDR B MA#128**
- 5 DDR\_B\_MA#129 **DDR B MA#129**
- 5 DDR\_B\_MA#130 **DDR B MA#130**
- 5 DDR\_B\_MA#131 **DDR B MA#131**
- 5 DDR\_B\_MA#132 **DDR B MA#132**
- 5 DDR\_B\_MA#133 **DDR B MA#133**
- 5 DDR\_B\_MA#134 **DDR B MA#134**
- 5 DDR\_B\_MA#135 **DDR B MA#135**
- 5 DDR\_B\_MA#136 **DDR B MA#136**
- 5 DDR\_B\_MA#137 **DDR B MA#137**
- 5 DDR\_B\_MA#138 **DDR B MA#138**
- 5 DDR\_B\_MA#139 **DDR B MA#139**
- 5 DDR\_B\_MA#140 **DDR B MA#140**
- 5 DDR\_B\_MA#141 **DDR B MA#141**
- 5 DDR\_B\_MA#142 **DDR B MA#142**
- 5 DDR\_B\_MA#143 **DDR B MA#143**
- 5 DDR\_B\_MA#144 **DDR B MA#144**
- 5 DDR\_B\_MA#145 **DDR B MA#145**
- 5 DDR\_B\_MA#146 **DDR B MA#146**
- 5 DDR\_B\_MA#147 **DDR B MA#147**
- 5 DDR\_B\_MA#148 **DDR B MA#148**
- 5 DDR\_B\_MA#149 **DDR B MA#149**
- 5 DDR\_B\_MA#150 **DDR B MA#150**
- 5 DDR\_B\_MA#151 **DDR B MA#151**
- 5 DDR\_B\_MA#152 **DDR B MA#152**
- 5 DDR\_B\_MA#153 **DDR B MA#153**
- 5 DDR\_B\_MA#154 **DDR B MA#154**
- 5 DDR\_B\_MA#155 **DDR B MA#155**
- 5 DDR\_B\_MA#156 **DDR B MA#156**
- 5 DDR\_B\_MA#157 **DDR B MA#157**
- 5 DDR\_B\_MA#158 **DDR B MA#158**
- 5 DDR\_B\_MA#159 **DDR B MA#159**
- 5 DDR\_B\_MA#160 **DDR B MA#160**
- 5 DDR\_B\_MA#161 **DDR B MA#161**
- 5 DDR\_B\_MA#162 **DDR B MA#162**
- 5 DDR\_B\_MA#163 **DDR B MA#163**
- 5 DDR\_B\_MA#164 **DDR B MA#164**
- 5 DDR\_B\_MA#165 **DDR B MA#165**
- 5 DDR\_B\_MA#166 **DDR B MA#166**
- 5 DDR\_B\_MA#167 **DDR B MA#167**
- 5 DDR\_B\_MA#168 **DDR B MA#168**
- 5 DDR\_B\_MA#169 **DDR B MA#169**
- 5 DDR\_B\_MA#170 **DDR B MA#170**
- 5 DDR\_B\_MA#171 **DDR B MA#171**
- 5 DDR\_B\_MA#172 **DDR B MA#172**
- 5 DDR\_B\_MA#173 **DDR B MA#173**
- 5 DDR\_B\_MA#174 **DDR B MA#174**
- 5 DDR\_B\_MA#175 **DDR B MA#175**
- 5 DDR\_B\_MA#176 **DDR B MA#176**
- 5 DDR\_B\_MA#177 **DDR B MA#177**
- 5 DDR\_B\_MA#178 **DDR B MA#178**
- 5 DDR\_B\_MA#179 **DDR B MA#179**
- 5 DDR\_B\_MA#180 **DDR B MA#180**
- 5 DDR\_B\_MA#181 **DDR B MA#181**
- 5 DDR\_B\_MA#182 **DDR B MA#182**
- 5 DDR\_B\_MA#183 **DDR B MA#183**
- 5 DDR\_B\_MA#184 **DDR B MA#184**
- 5 DDR\_B\_MA#185 **DDR B MA#185**
- 5 DDR\_B\_MA#186 **DDR B MA#186**
- 5 DDR\_B\_MA#187 **DDR B MA#187**
- 5 DDR\_B\_MA#188 **DDR B MA#188**
- 5 DDR\_B\_MA#189 **DDR B MA#189**
- 5 DDR\_B\_MA#190 **DDR B MA#190**
- 5 DDR\_B\_MA#191 **DDR B MA#191**
- 5 DDR\_B\_MA#192 **DDR B MA#192**
- 5 DDR\_B\_MA#193 **DDR B MA#193**
- 5 DDR\_B\_MA#194 **DDR B MA#194**
- 5 DDR\_B\_MA#195 **DDR B MA#195**
- 5 DDR\_B\_MA#196 **DDR B MA#196**
- 5 DDR\_B\_MA#197 **DDR B MA#197**
- 5 DDR\_B\_MA#198 **DDR B MA#198**
- 5 DDR\_B\_MA#199 **DDR B MA#199**
- 5 DDR\_B\_MA#200 **DDR B MA#200**

Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V

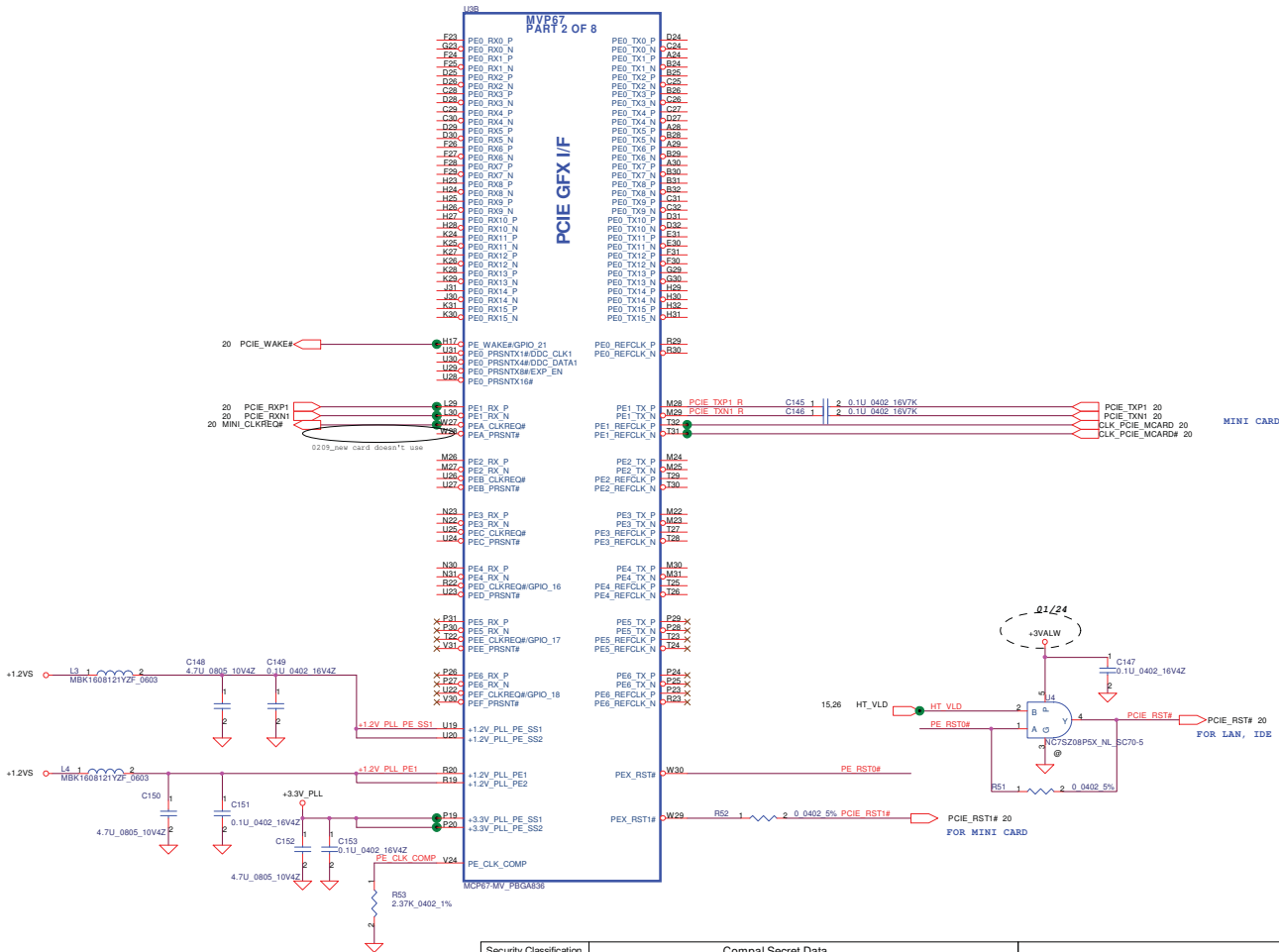
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V



Change PCB Footprint  
**DIMMO REV H:8mm (BOT)**

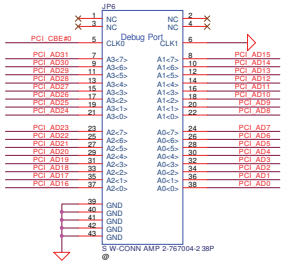
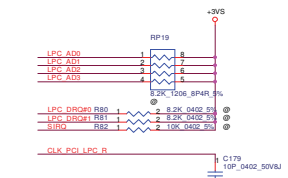
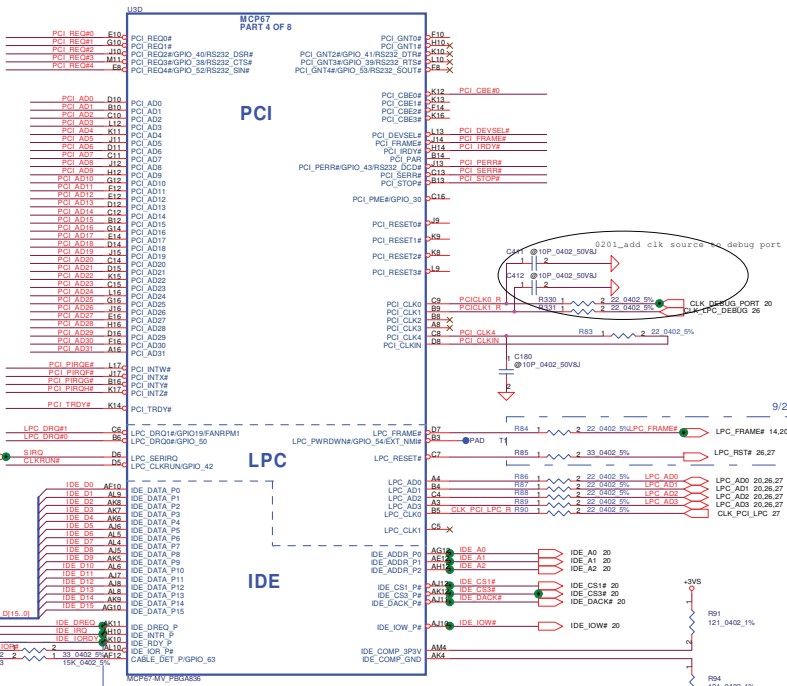
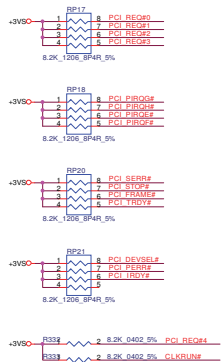
Security Classification		Compal Secret Data		Title
Issued Date	2007/01/07	Deciphered Date	2008/01/12	DDR2 SO-DIMM II
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Size	Customer	Number	Date	Sheet	Rev
	LA-3733P		Monday, March 05, 2007	13 of 36	0.1

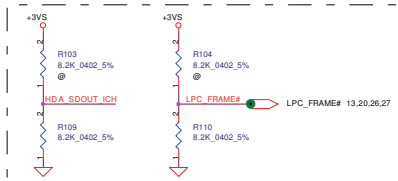
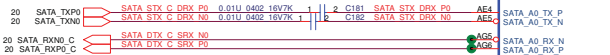




9/21 Add 33ohm for IDE\_IOR#

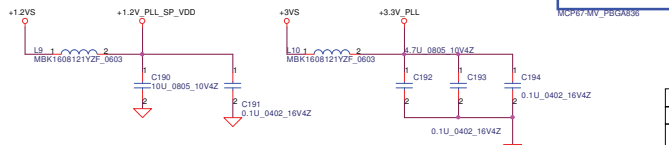
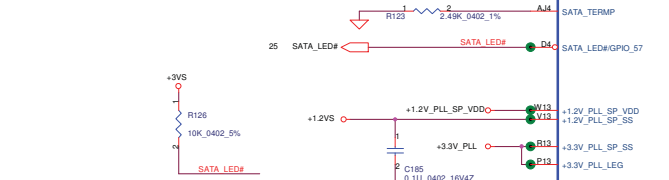
Security Classification	Compal Secret Data		File	MCP67 PCW/LPC/IDE
Issued Date	2007/01/07	Deciphered Date	2008/01/12	Rev
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LA-3733P				0.1
Issue	13	01	06	

PLACE SATA AC COUPLING CAPS CLOSE TO MCP67



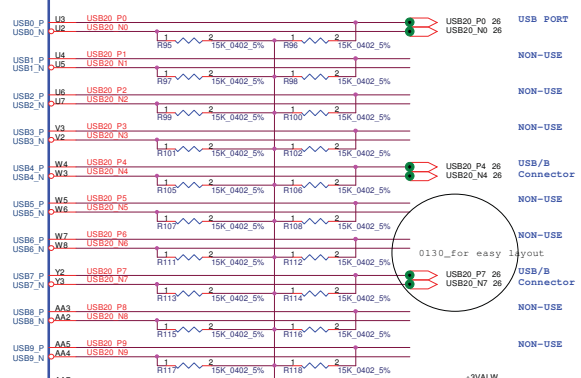
HDA_SDOUT	LPC_FRAME	FUNCTION
"0"	"0"	LPC BIOS*
"0"	"1"	PCI BIOS
"1"	"0"	SPI BIOS
"1"	"1"	RESERVED

\*DEFAULT

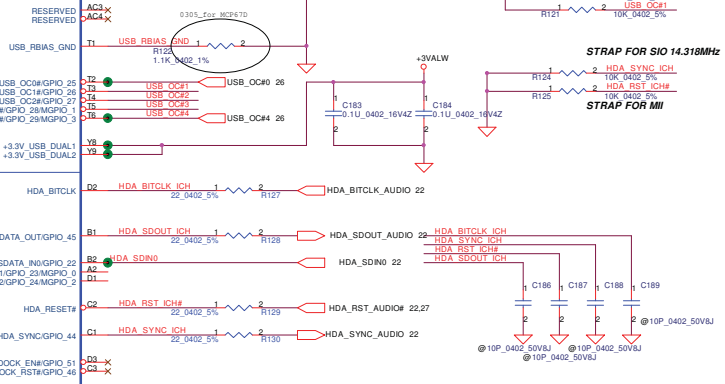


SATA USB

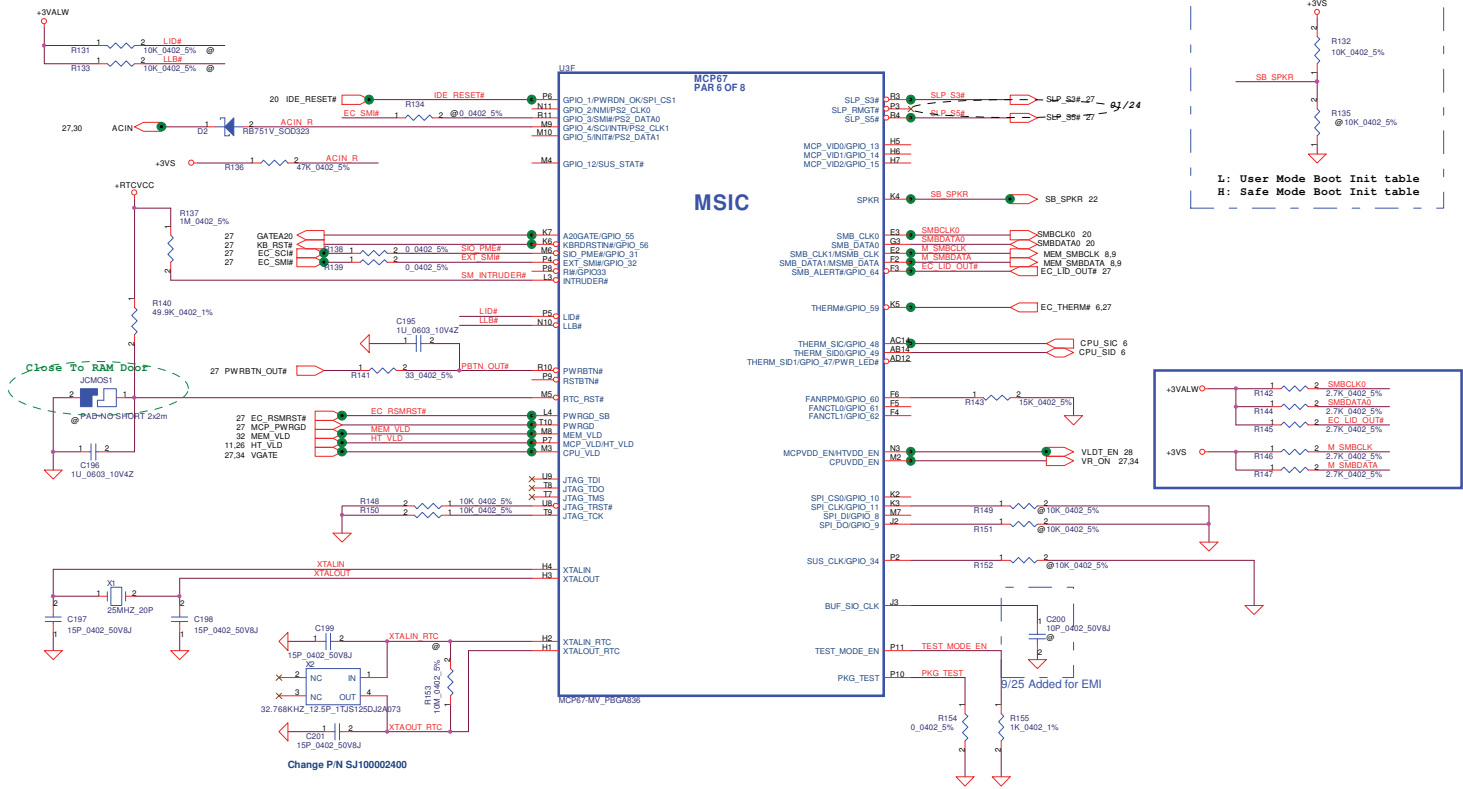
MCP67 PAR 5 OF 8



HDA



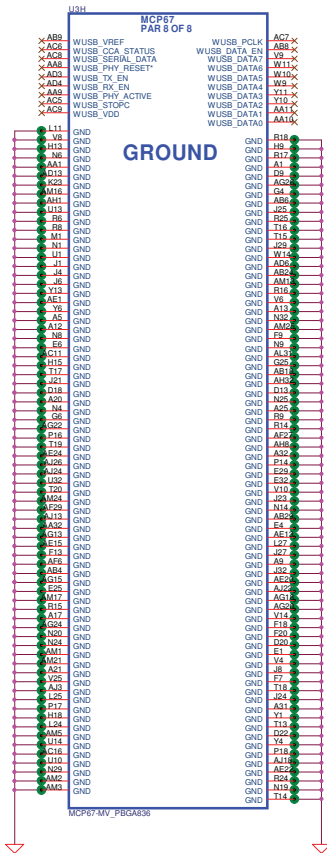
Security Classification	Compal Secret Data		Title
Issued Date	2007/01/07	Deciphered Date	2008/01/12
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Date	Monday, March 05, 2007	Sheet	14 of 36



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Date	Monday, March 05, 2007	Sheet	15	of 36

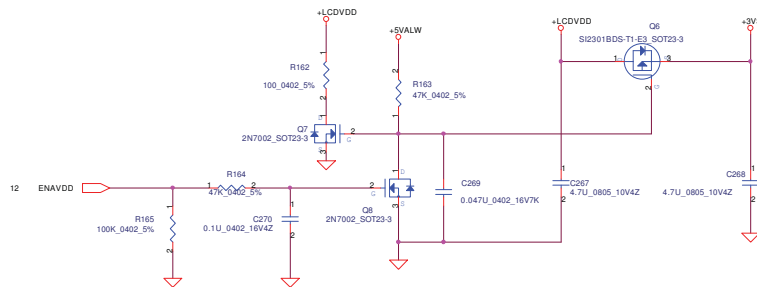
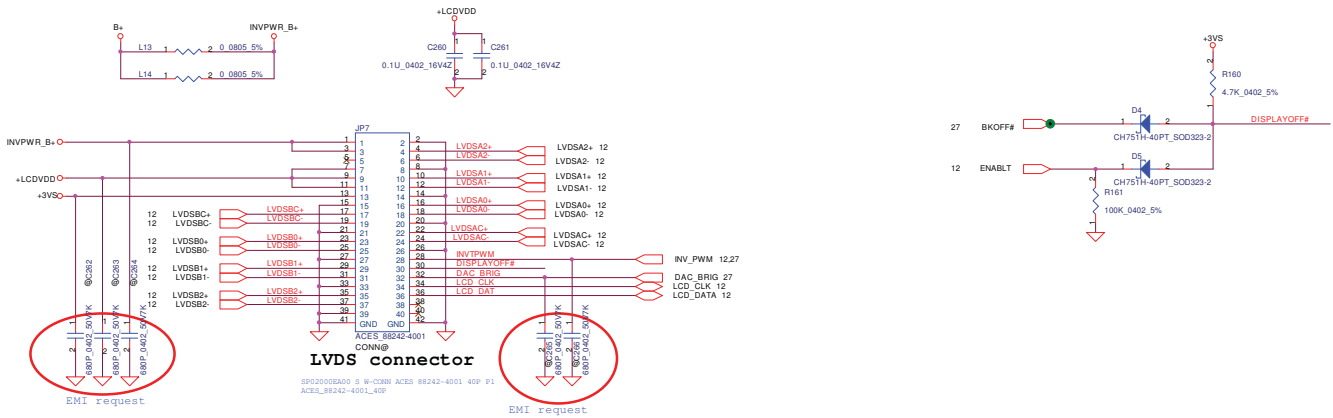






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LVDS CONN

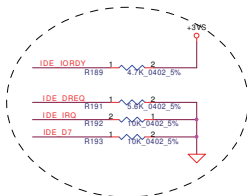
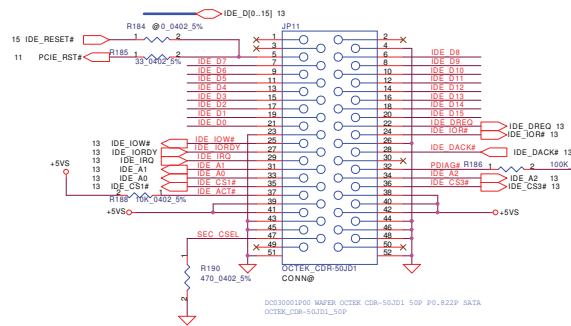
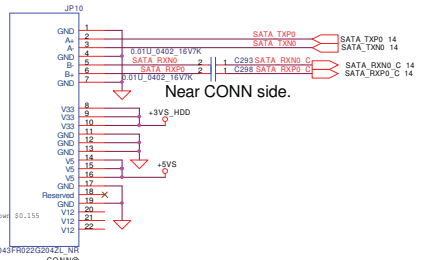
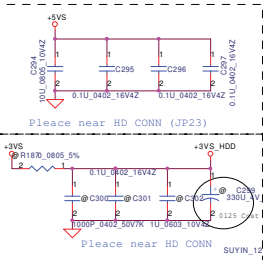
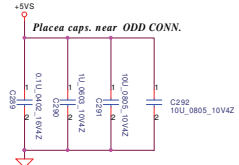


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Issued Date	2007/01/07	Deciphered Date	2008/01/12	Size
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				LA-3733P
				Rev
				0.1
Date: Monday, March 05, 2007				Sheet 18 of 36



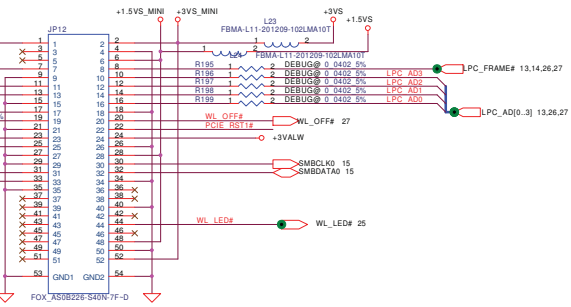
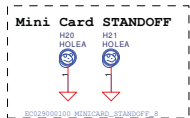
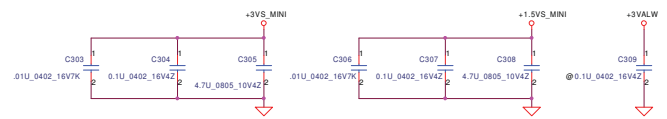
### HDD Connector

### CD-ROM Connector



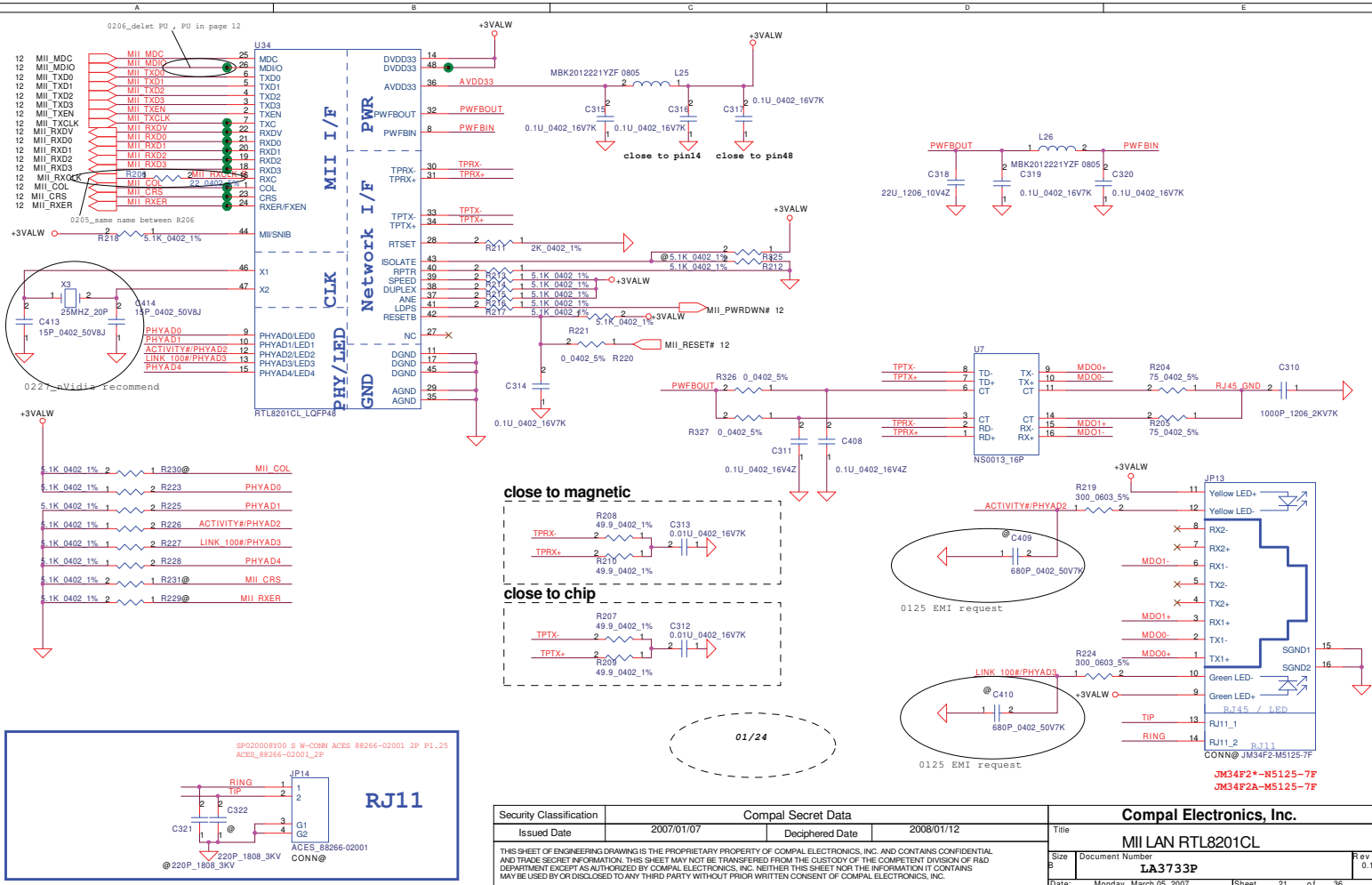
OC310053060 800518NC SUYIN 127043FR0220204E1 22P SATA SUYIN\_127043FR0220204E1\_22P\_NR

### Mini-Express Card---WLAN



SP01060P700 S-H-CONN ACES 88914-5204 52P P0.8

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				Rev 0.1	
				LA-3733P	
				Date: Monday, March 05, 2007 Sheet 20 of 38	



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Issued Date	2007/01/07	Deciphered Date
		2008/01/12

Title		MII LAN RTL8201CL	
Size	Document Number	Rev	0.1
Date		Monday, March 05, 2007	

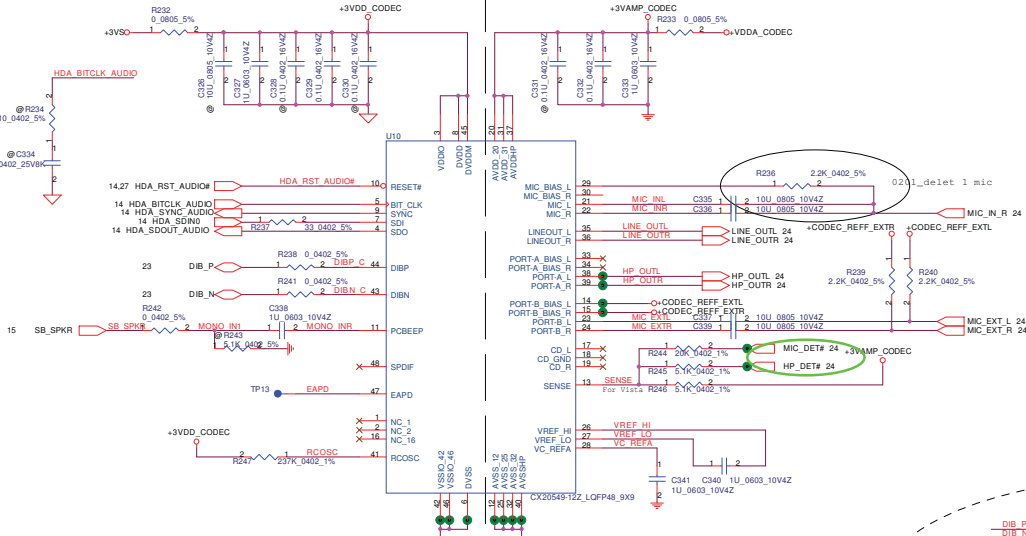
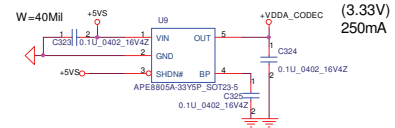
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**AUDIO CODEC**

**CODEC POWER**

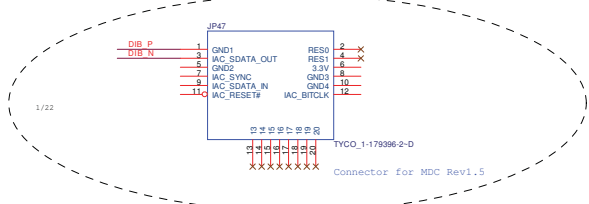
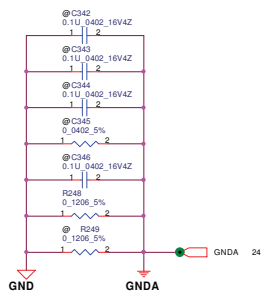
In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

**For Layout:**  
Place decoupling caps near the power pins of SmartAMC device.

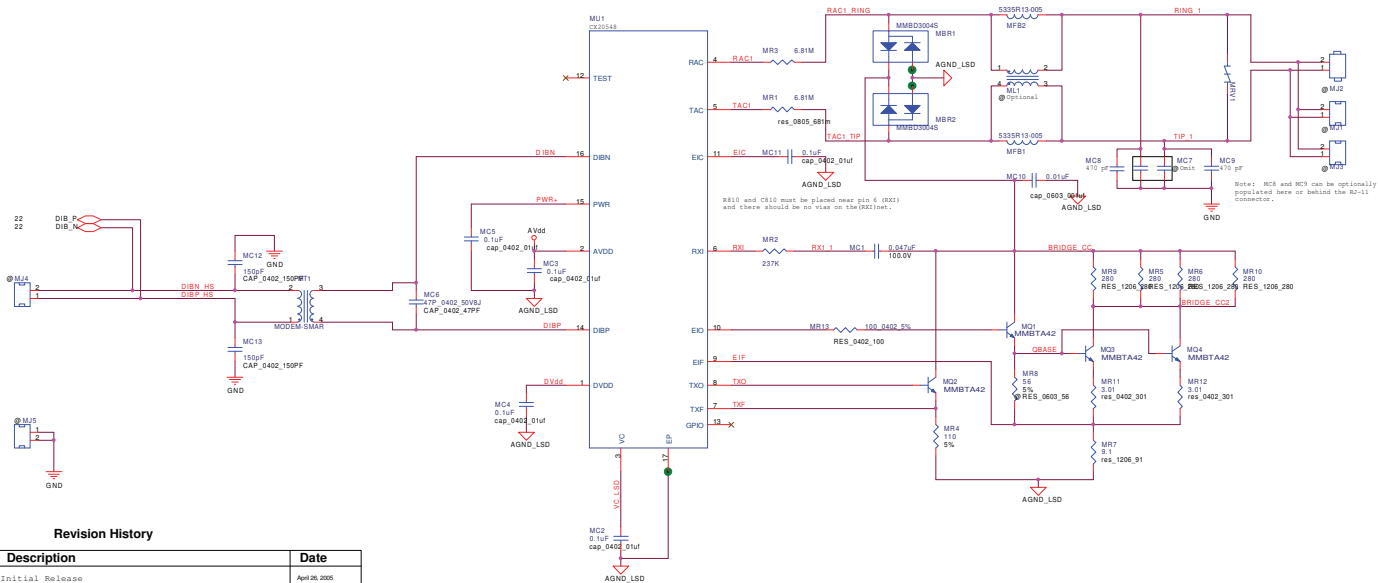


**DIGITAL**

**ANALOG**



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

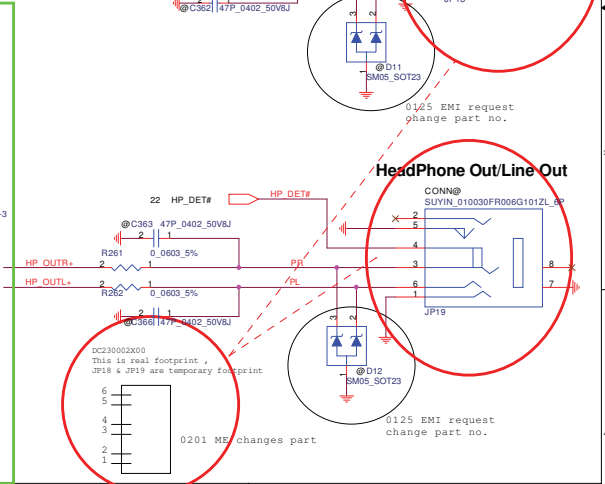
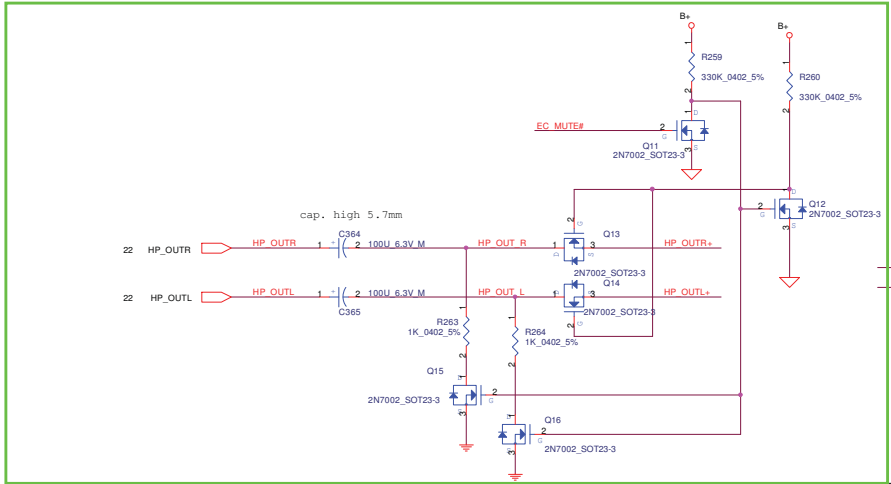
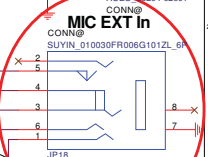
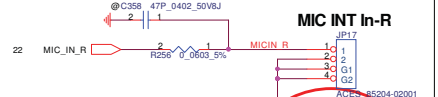
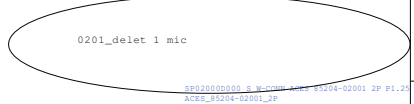
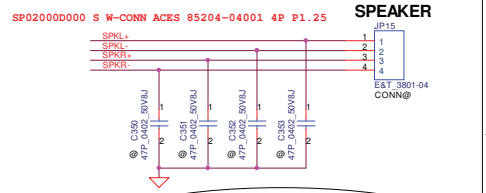
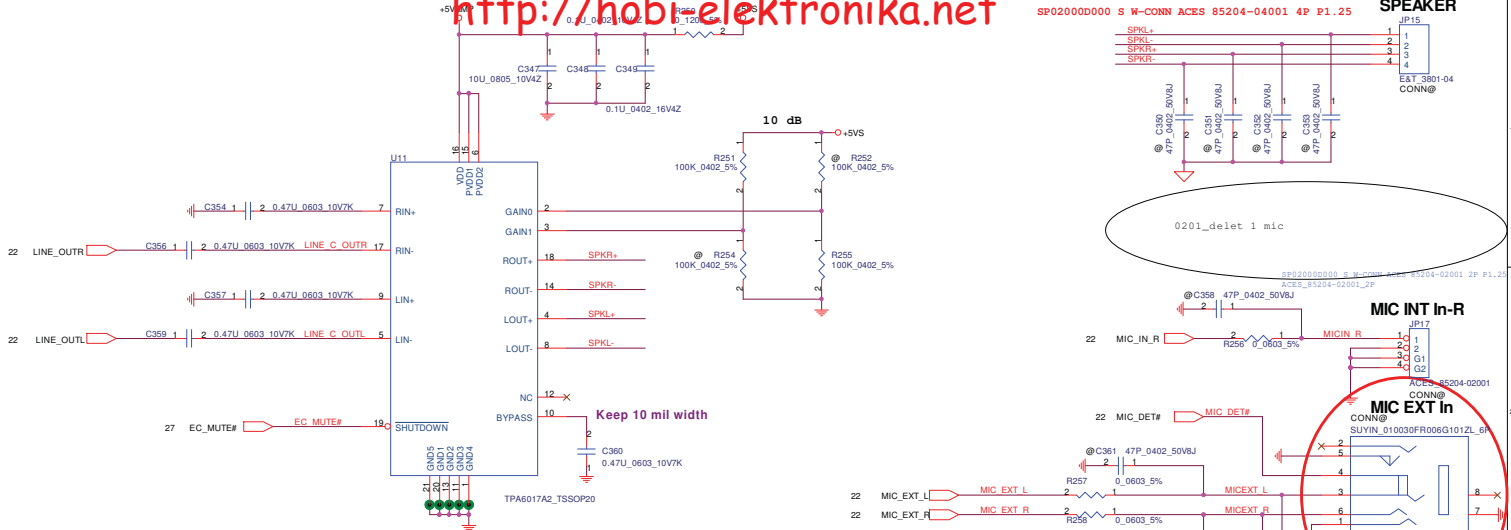


Note: MC8 and MC9 can be optionally populated here or behind the RJ-11 connector.

**Revision History**

REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 16, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

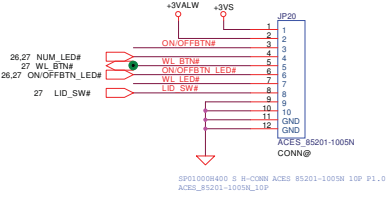
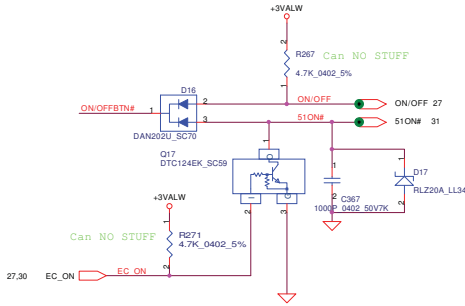
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Date	Monday, March 04, 2007	Sheet	23 of 36	Rev	8.1



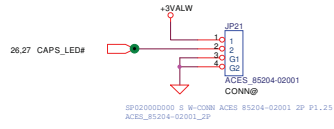
Security Classification	Compal Secret Data		Title	
Issued Date	2007/01/07	Deciphered Date	2008/01/12	AMP & Audio Jack
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**Power ON/OFF**



**M/B to SB (Caps Lock LED)**

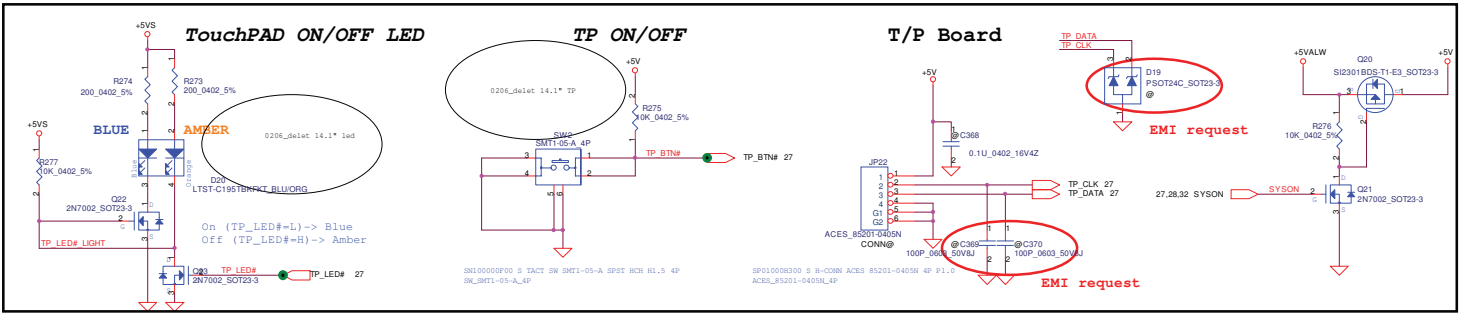


D21, D25, D23 Footprint can not match part number.

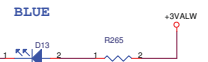
**TouchPAD ON/OFF LED**

**TP ON/OFF**

**T/P Board**



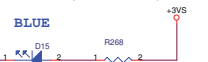
**POWER LED (Left 1)**



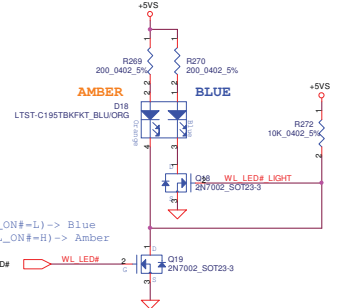
**Battery Charge LED (Left 2)**



**HDD LED (Left 3)**



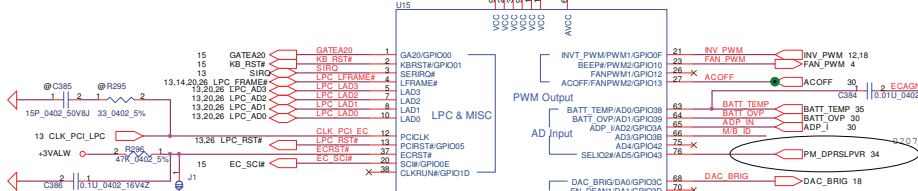
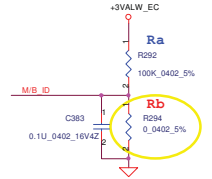
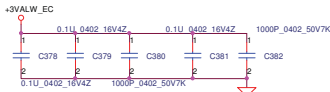
**Wireless ON/OFF LED (Left 4)**



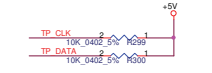
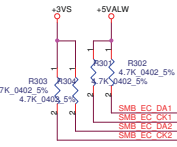
On (WL\_ON#-L) -> Blue  
Off (WL\_ON#-H) -> Amber

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Date: Monday, March 05, 2007				0.1
Sheet 25 of 38				

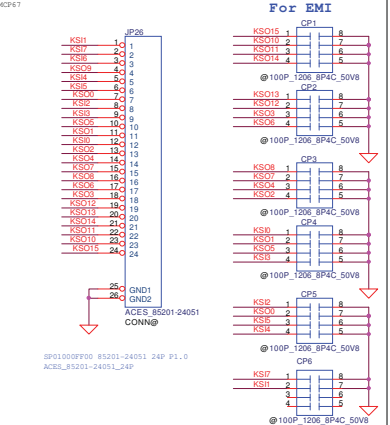
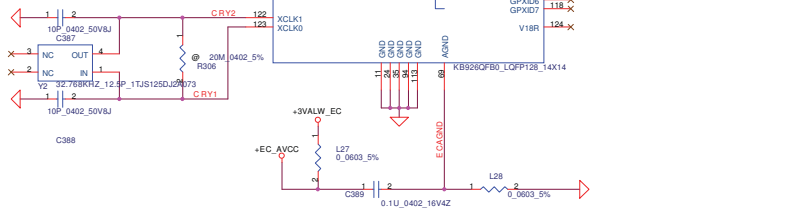
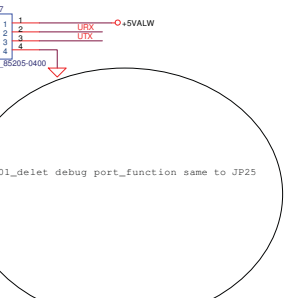


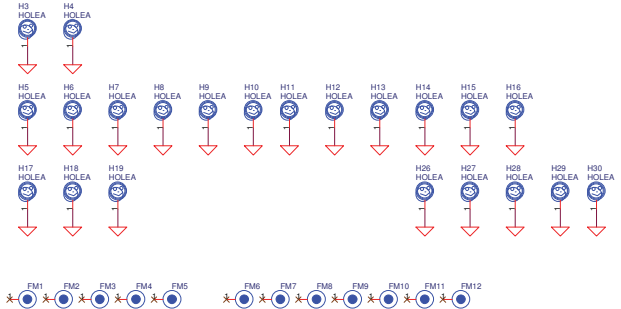
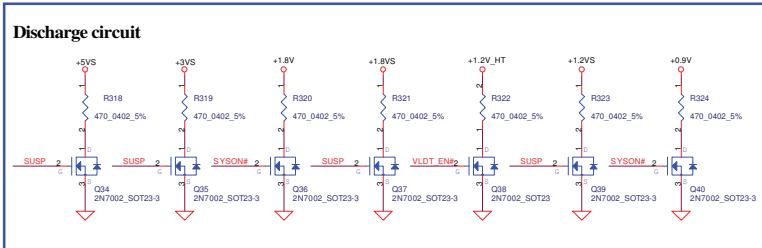
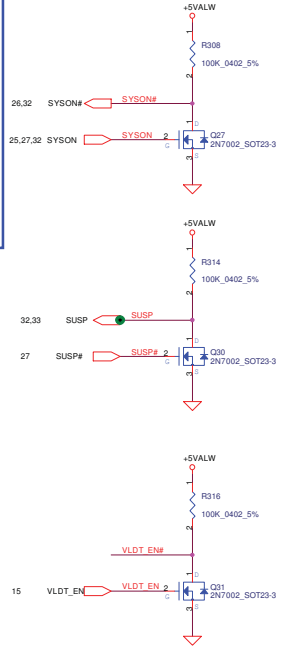
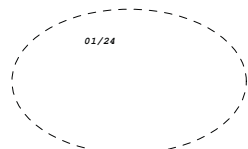
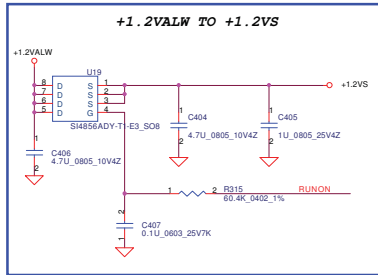
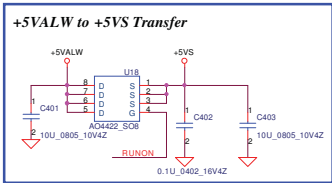
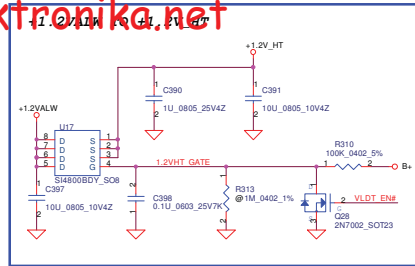
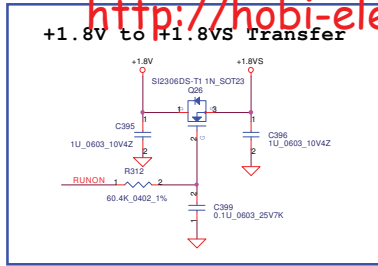
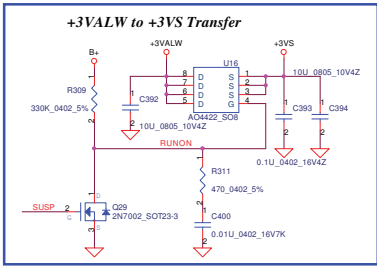


Board ID	Ra	Rb	V <sub>AD_MIN</sub>	V <sub>AD_MAX</sub>	V <sub>REG</sub>	V <sub>MIN</sub>	V <sub>MAX</sub>	I <sub>REG</sub>	I <sub>MAX</sub>
0	3.3V+/-5%	100K+/-5%	0V	0V	0V	0V	0V	0V	0V
1	8.2K+/-5%	100K+/-5%	0.216V	0.250V	0.289V				
2	18K+/-5%	100K+/-5%	0.436V	0.503V	0.538V				
3	33K+/-5%	100K+/-5%	0.712V	0.819V	0.875V				
4	56K+/-5%	100K+/-5%	1.036V	1.185V	1.264V				
5	100K+/-5%	100K+/-5%	1.453V	1.650V	1.759V				
6	200K+/-5%	100K+/-5%	1.935V	2.200V	2.341V				
7	NC	NC	2.500V	3.300V	3.300V				



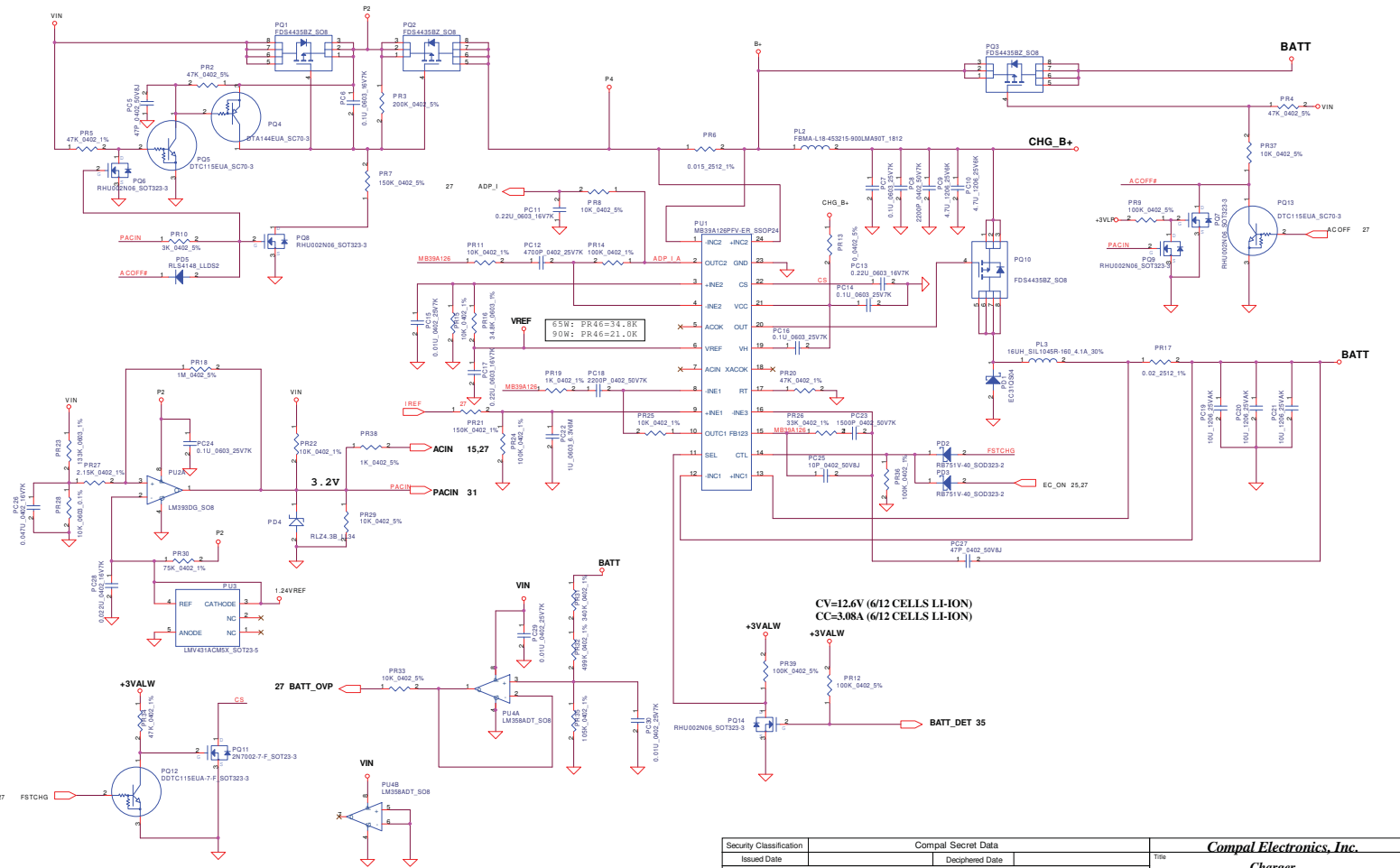
EC DEBUG port





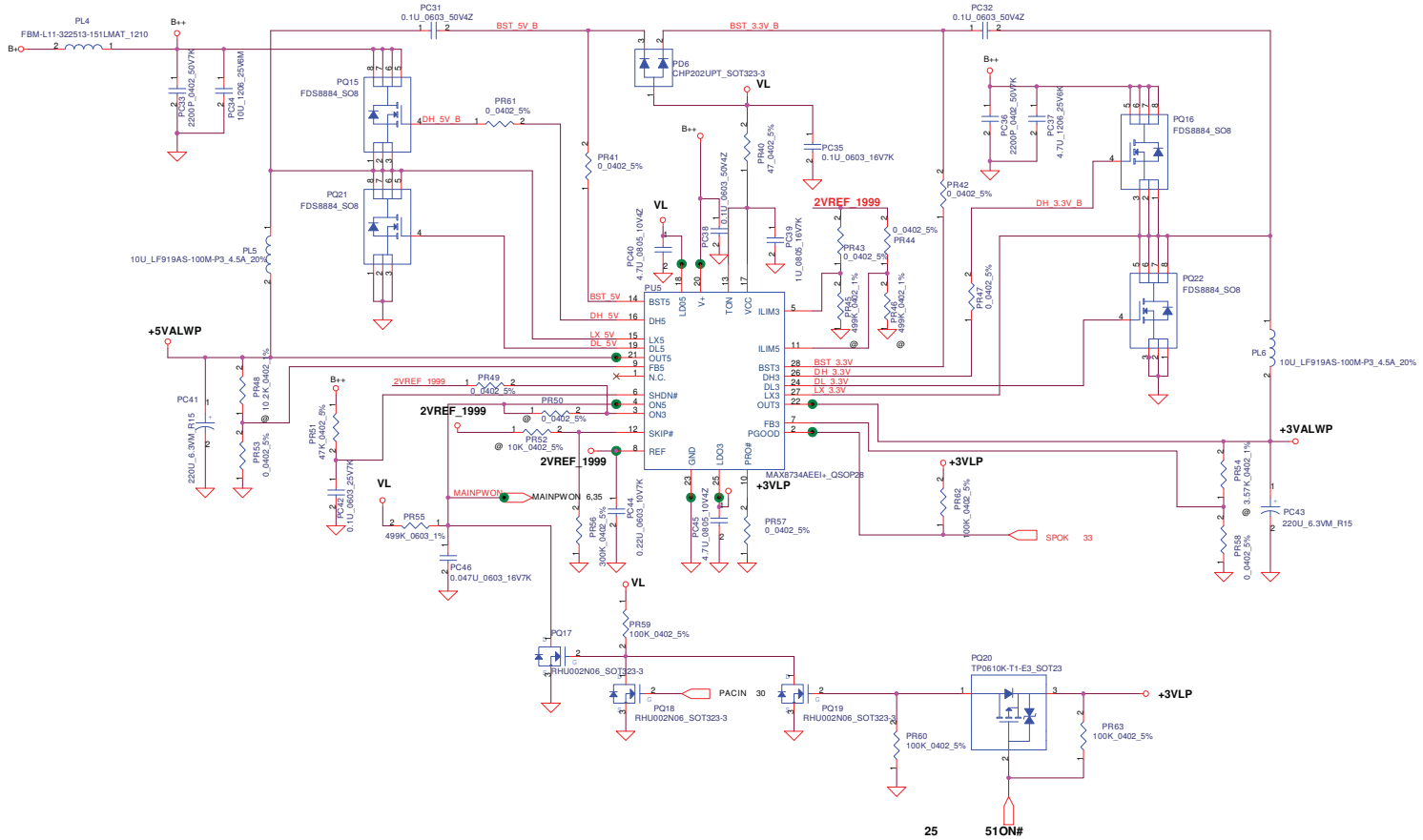
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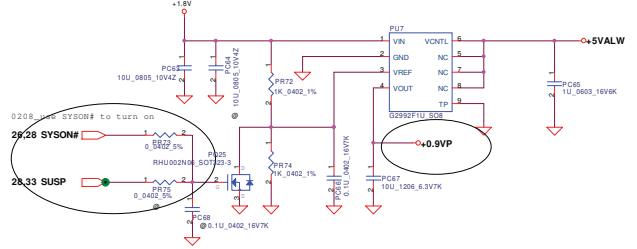
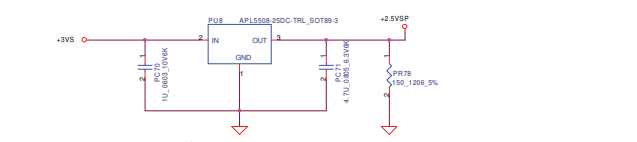
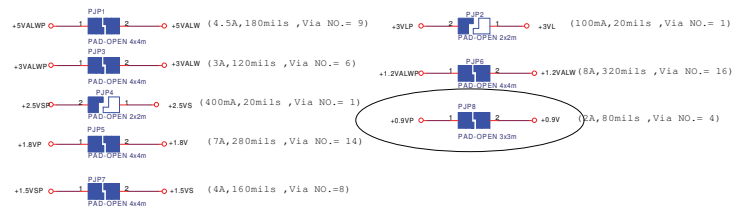
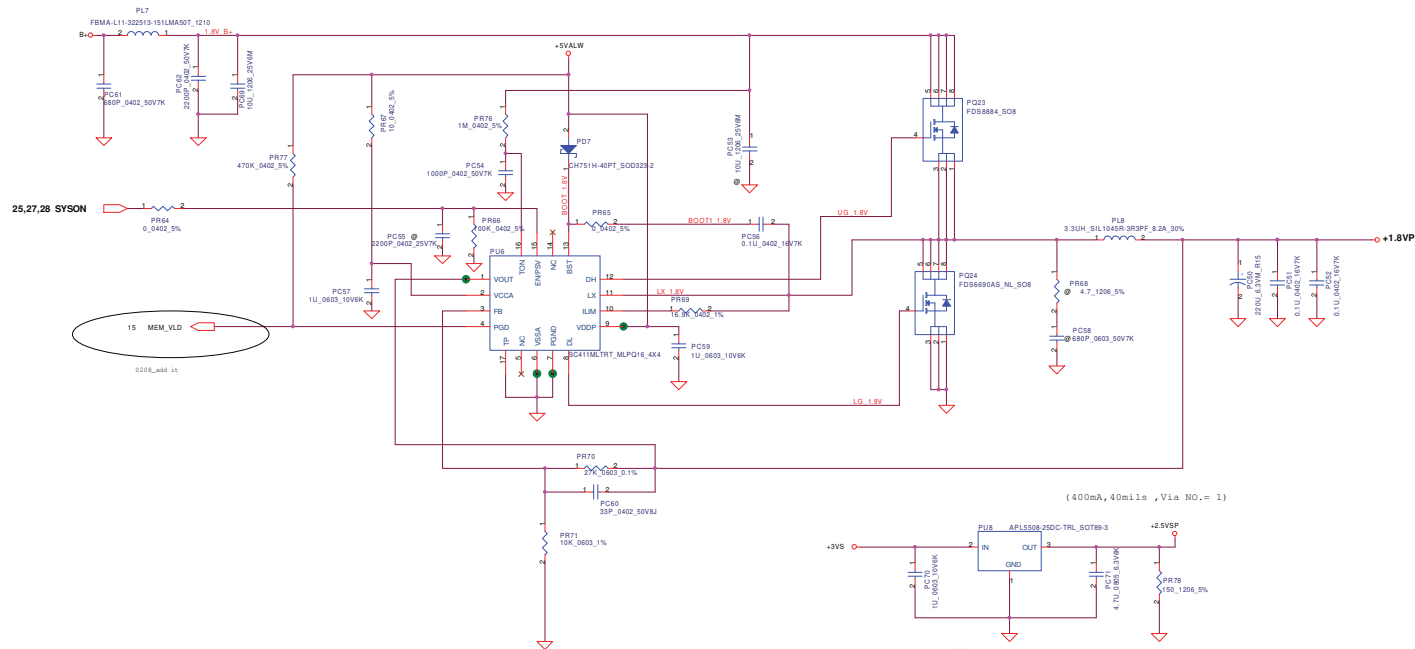
CV=12.6V (6/12 CELLS LI-ION)  
CC=3.08A (6/12 CELLS LI-ION)

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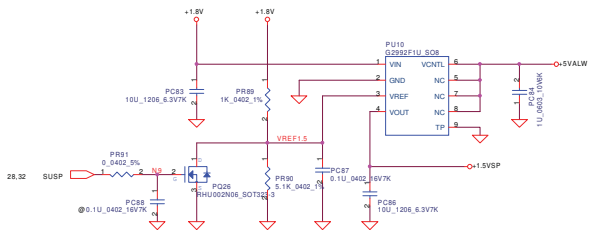
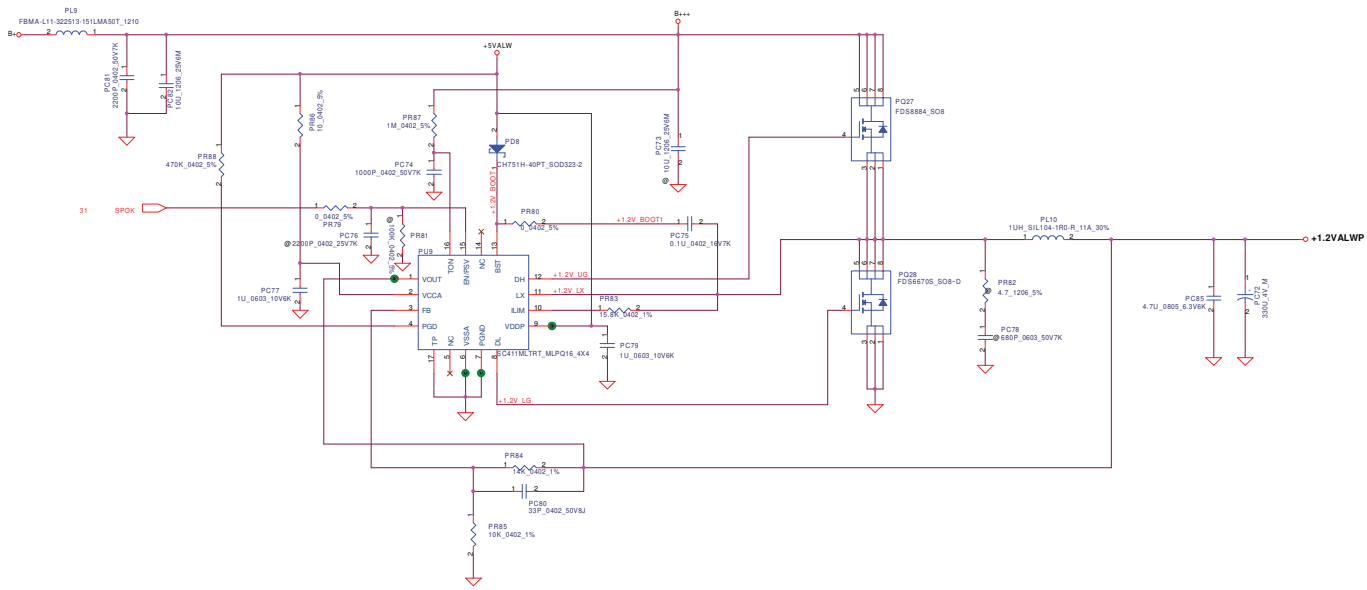
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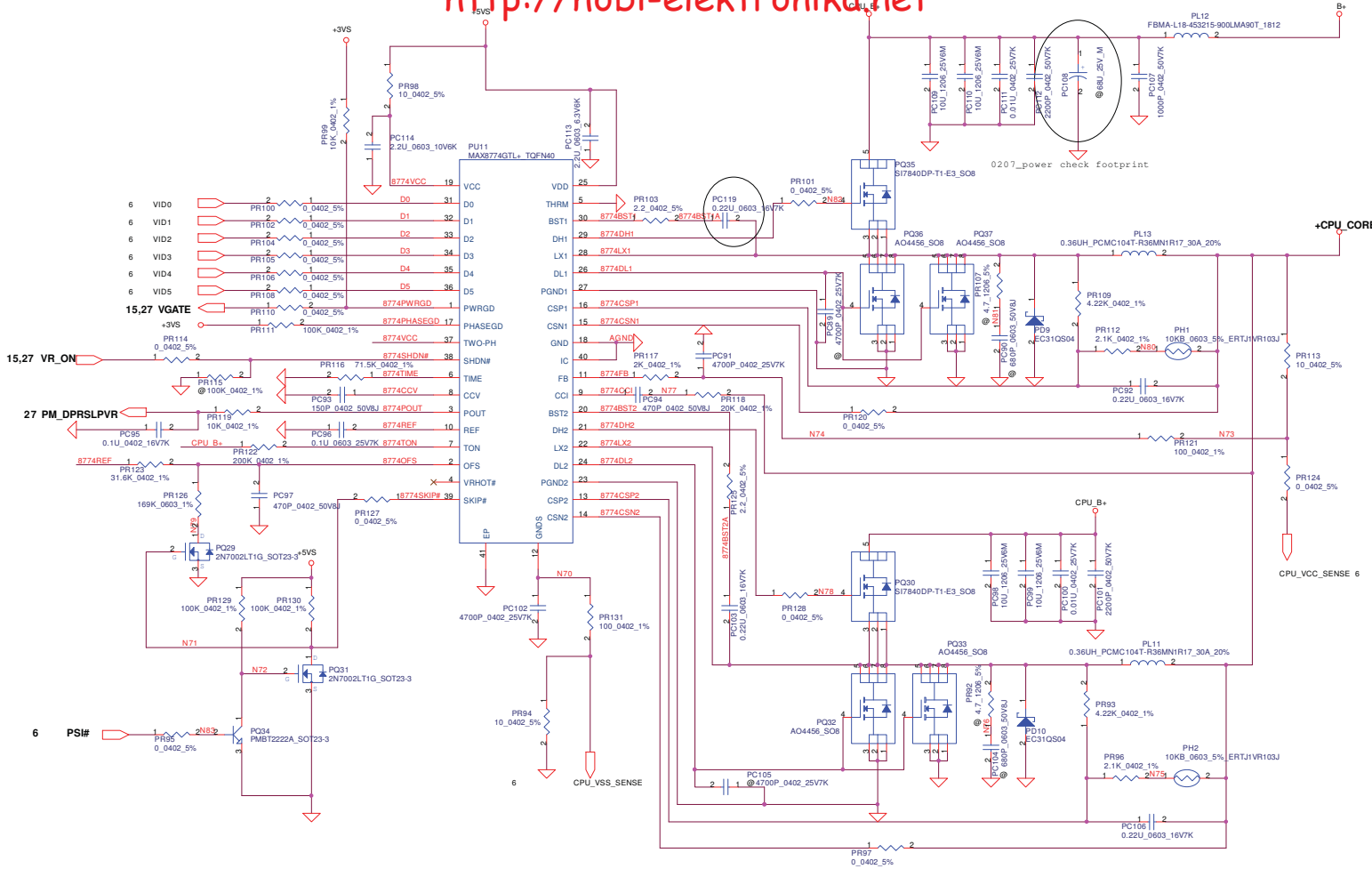


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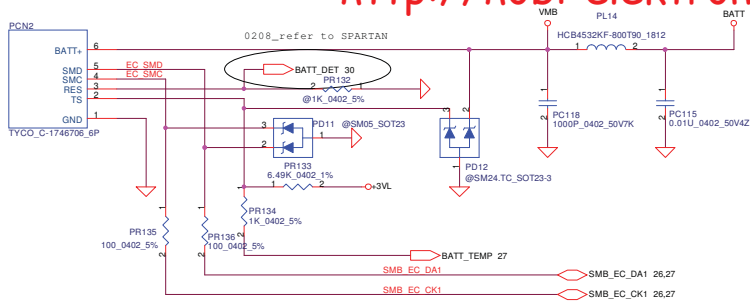




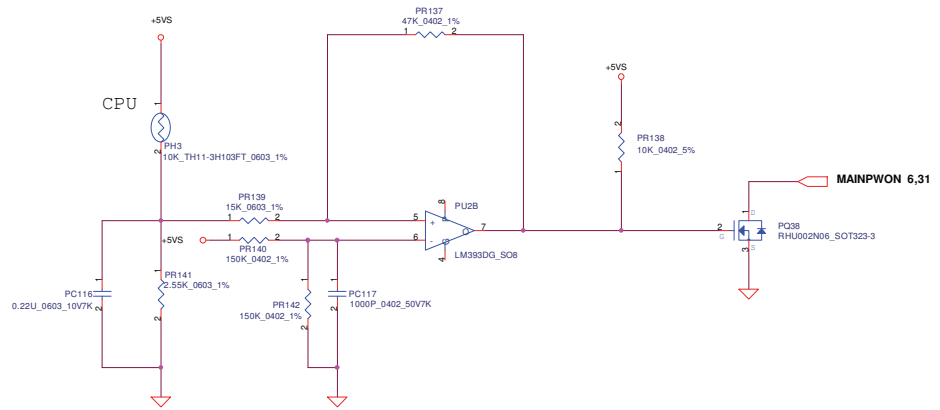
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Issued Date	2007/01/07	Deciphered Date	2008/01/12	1.2V VP/1.5VSP/1.05VP
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**PH1 under CPU bottom side :**  
 CPU thermal protection at 90  $\pm$ 3 degree C  
 Recovery at 47  $\pm$ 3 degree C



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Item	Reason for change	PG#	Modify List	Date	Phase
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	<b>PWR PIR</b>	
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Power On Sequence (AC IN mode)

