

COMPAL CONFIDENTIAL

N32NN6 LA736B/C DISCRETE MODEL

AMD MOBILE K7 + ALI M1647 & M1535+

VER1.0 (w/ LCL)

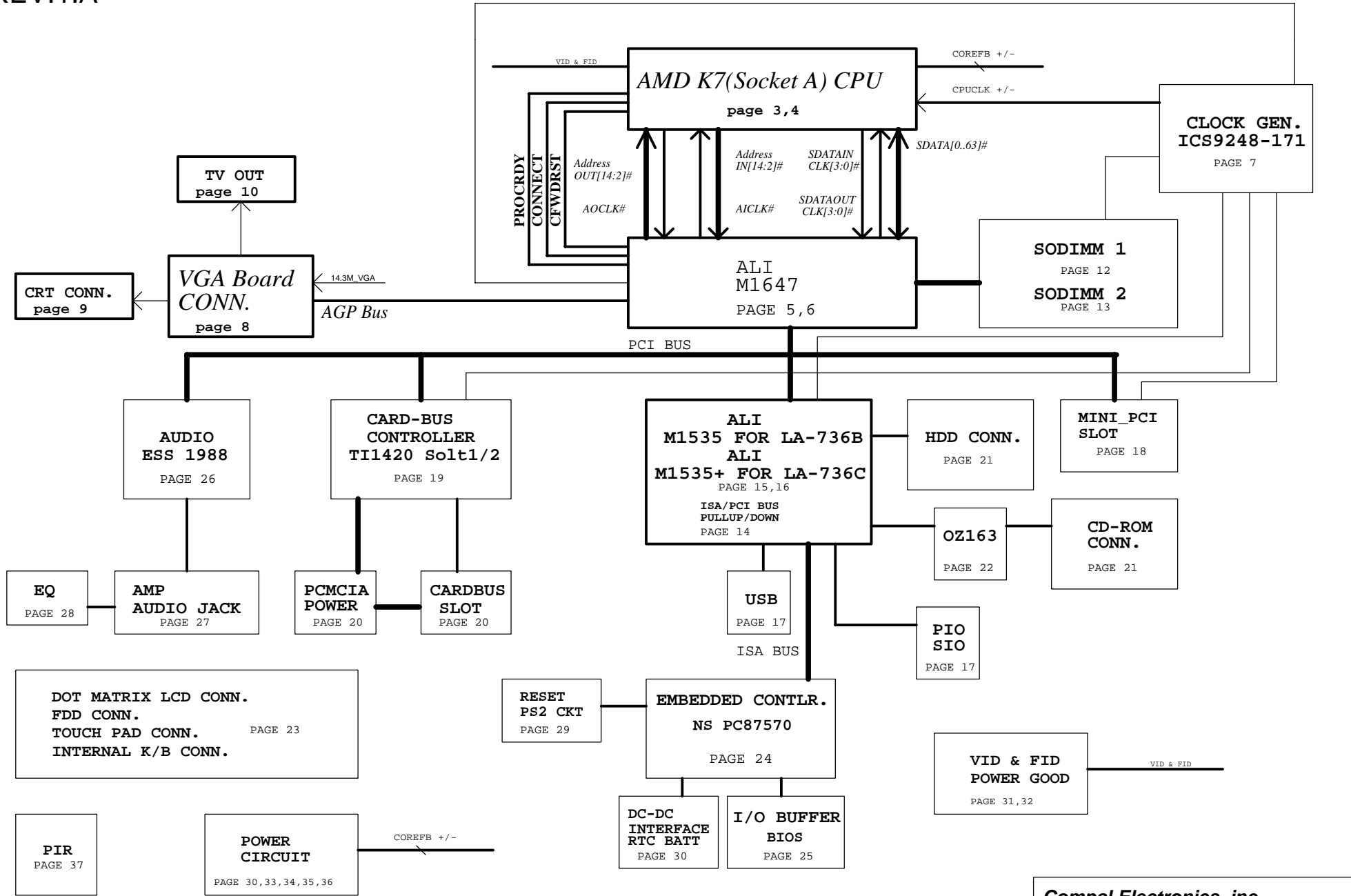
LA-736B AND LA-736C DIFFERENCE IN PAGE 41(P.I.R) FOR DETAIL!

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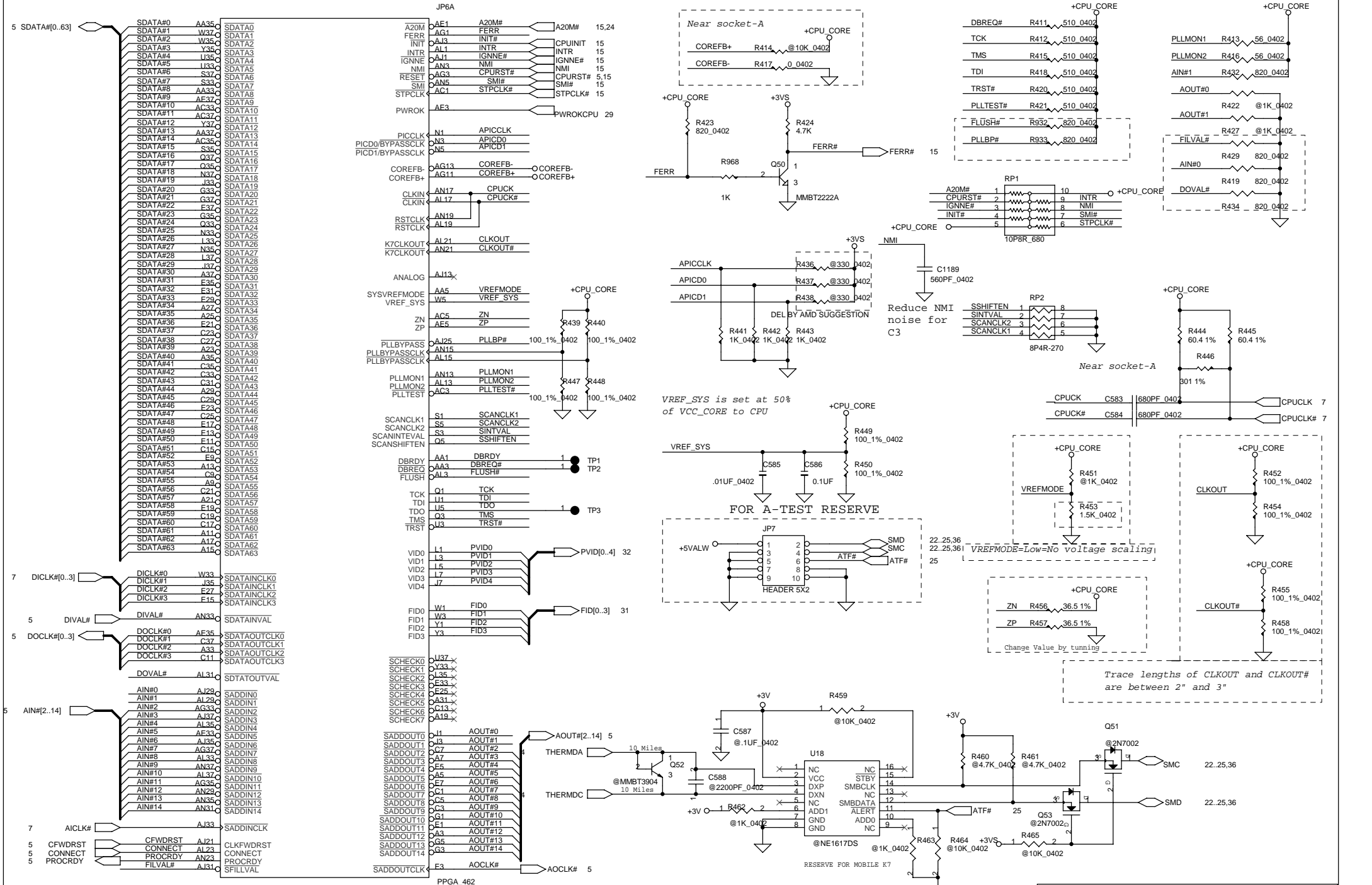
MODEL NAME : N32N AMD K7 M/B LA-736C

REV:1.A



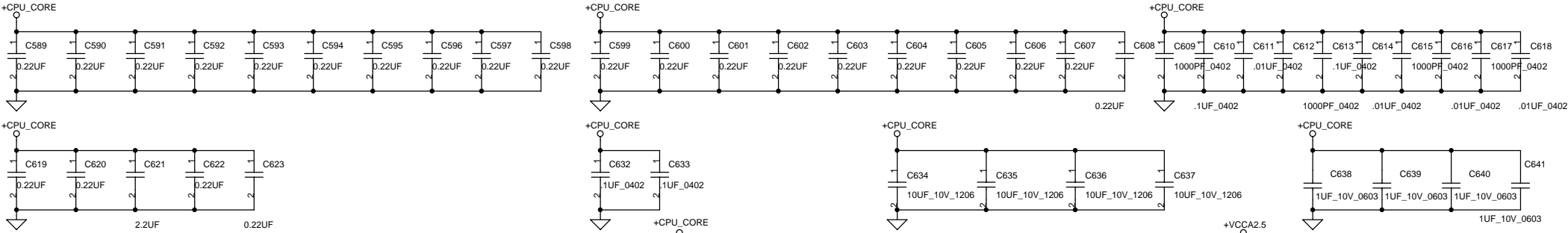
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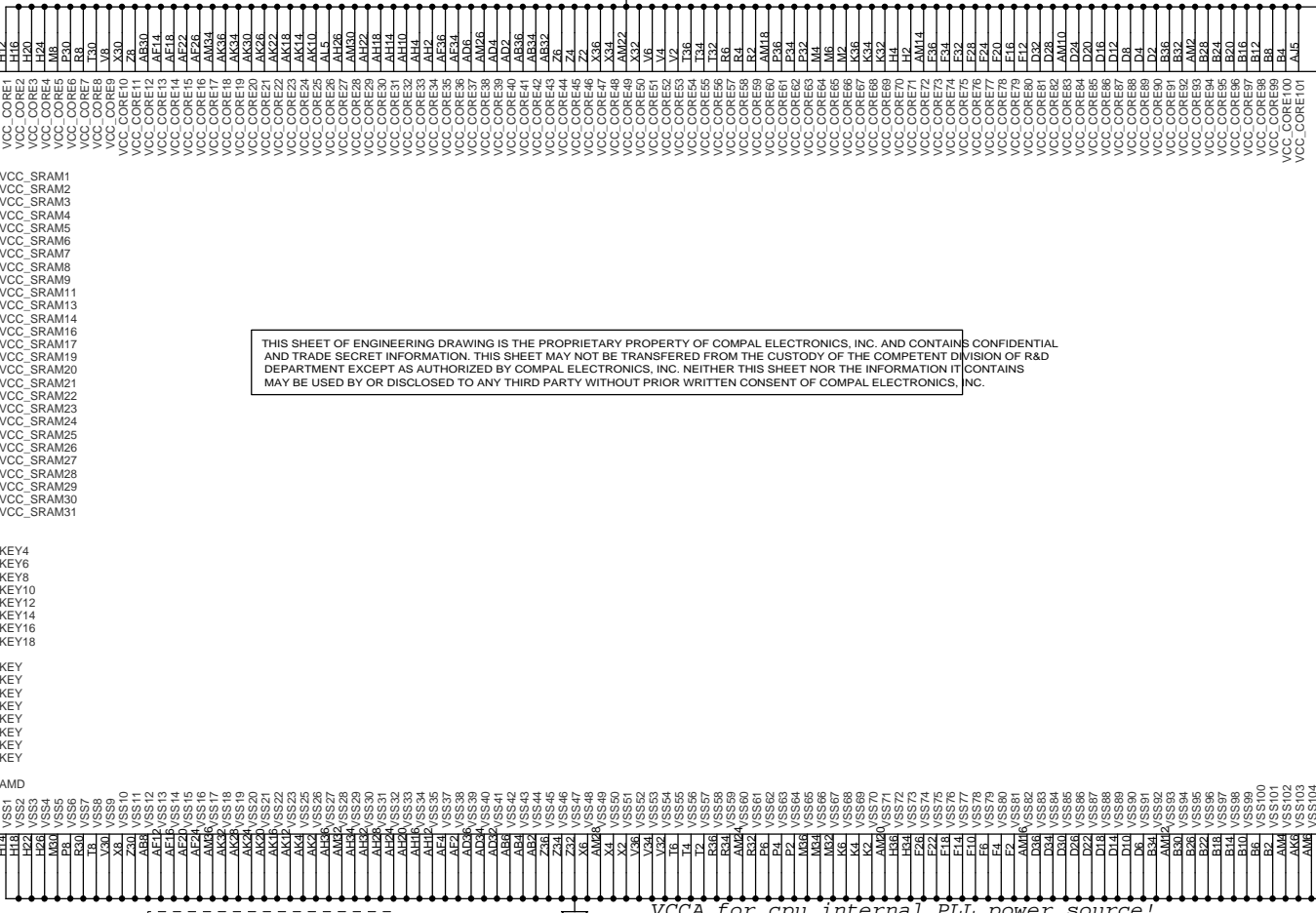
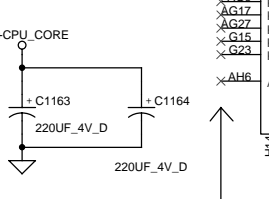
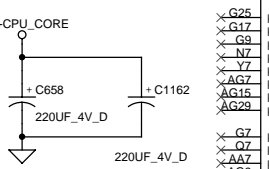
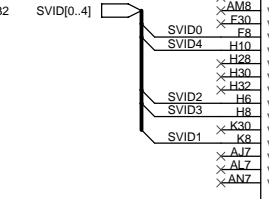
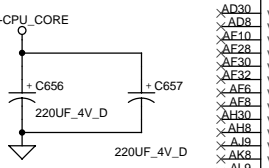
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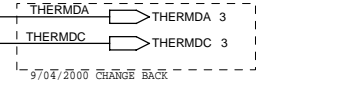
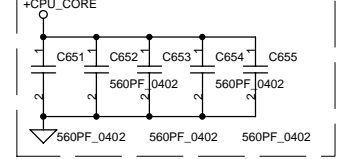
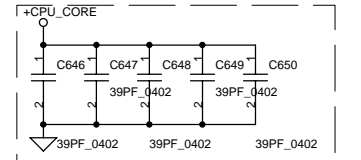
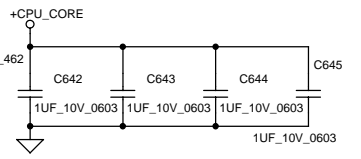


Located at Socket-A Cap

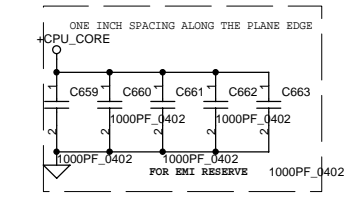
- 0.22uF(0603) X 22
 - 0.22uF(0603) X 3 FOR RESERVE
 - 0.1uF(0603) X 2
 - 0.01uF(0603) X 8
 - 1uF(0805) X 8
 - 10uF(1206) X 4
- AMD recommendation
220uF X10



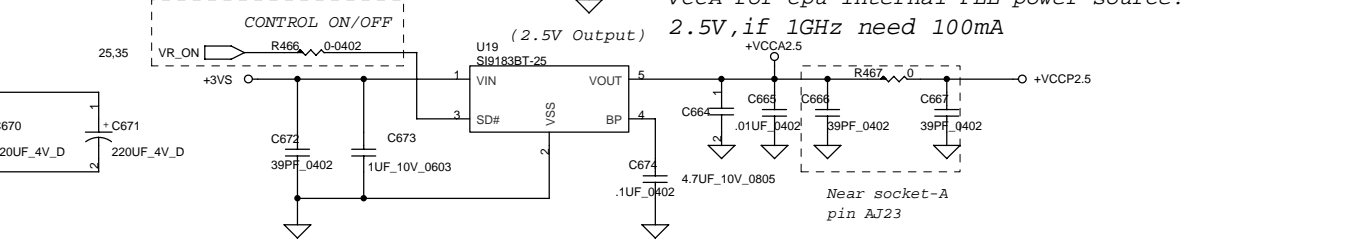
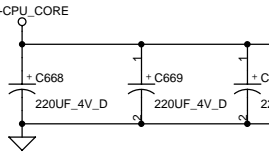
- VCC_A
- VCC_Z
- VSS_Z
- AA31
- AC31
- AC23
- AG24
- AG31
- AG5
- AI11
- AI15
- AI17
- AI18
- AI27
- AI11
- AN11
- ANS
- G11
- G13
- G27
- G29
- G31
- I31
- I5
- I31
- N31
- Q31
- NC29
- S31
- S7
- U31
- W31
- W37
- Y31
- Y5
- AG19
- G21
- AG21
- G19
- AN27
- AL27
- AN25
- AL25
- BP0_CUT
- BP1_CUT
- BP2_CUT
- BP3_CUT



9704/2000 CHANGE BACK



AMD Socket-A processors will not implement a pin at location AH6.



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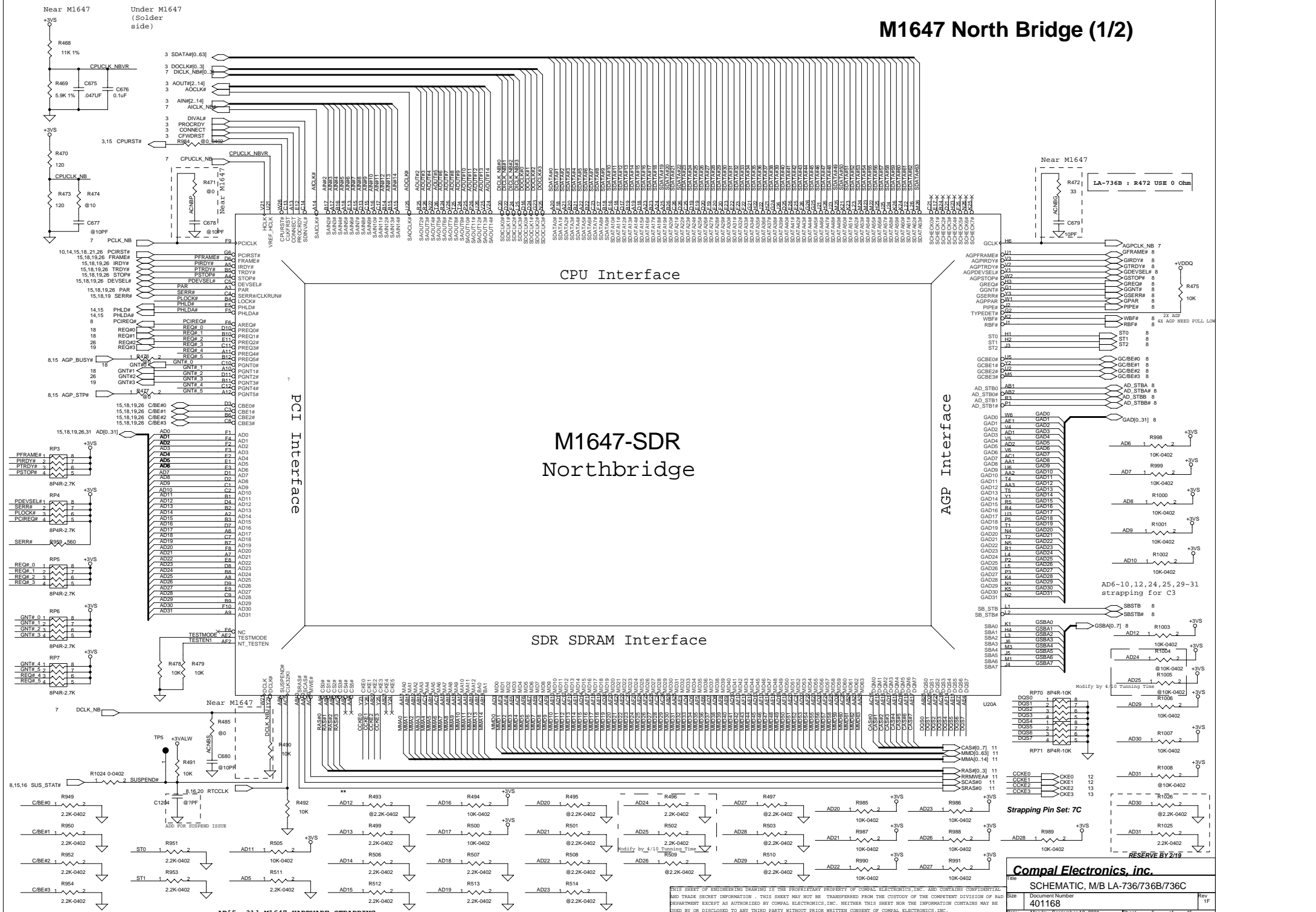
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M1647 North Bridge (1/2)



CPU Interface

M1647-SDR Northbridge

SDR SDRAM Interface

Strapping Pin Set: 7C

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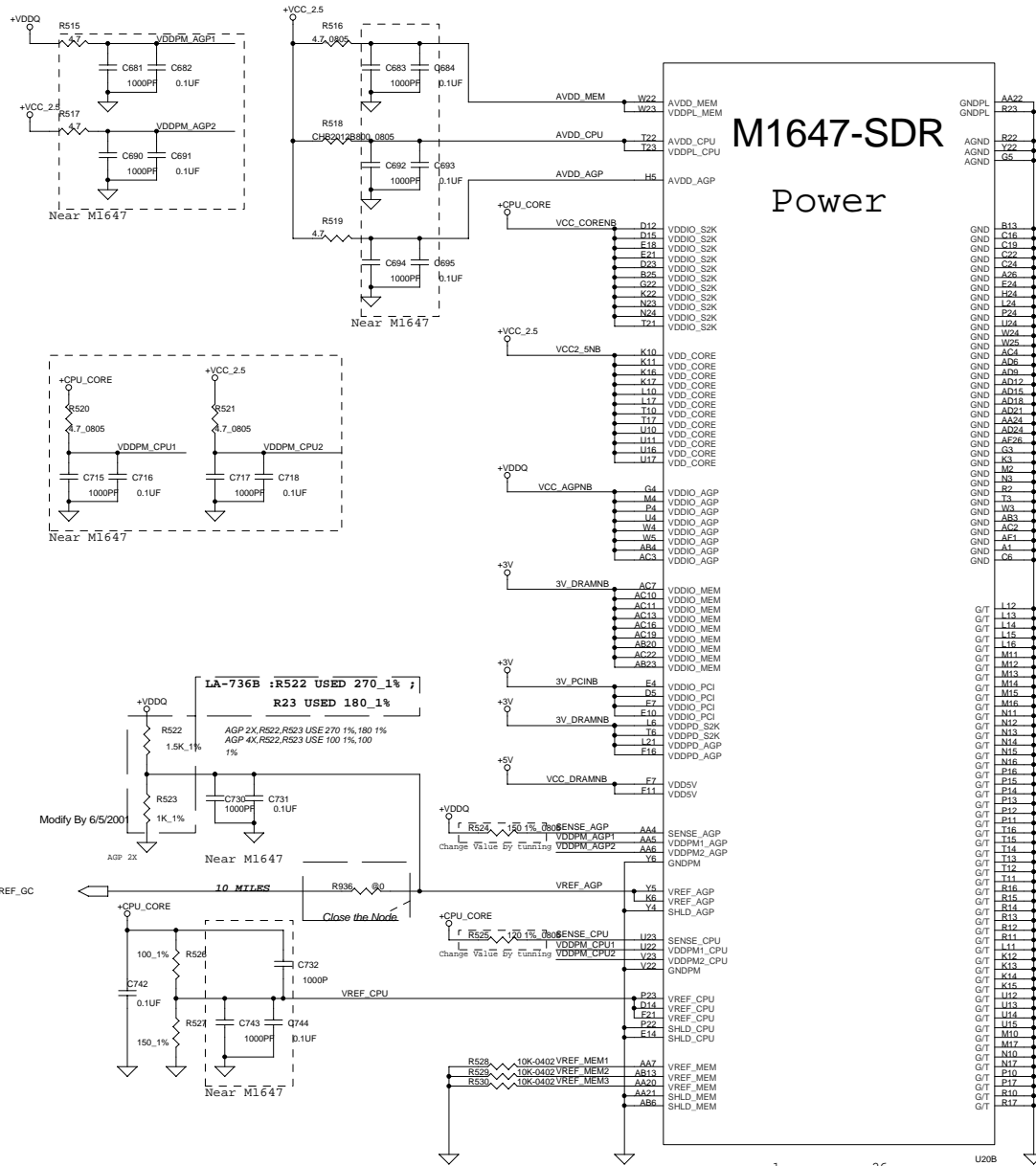
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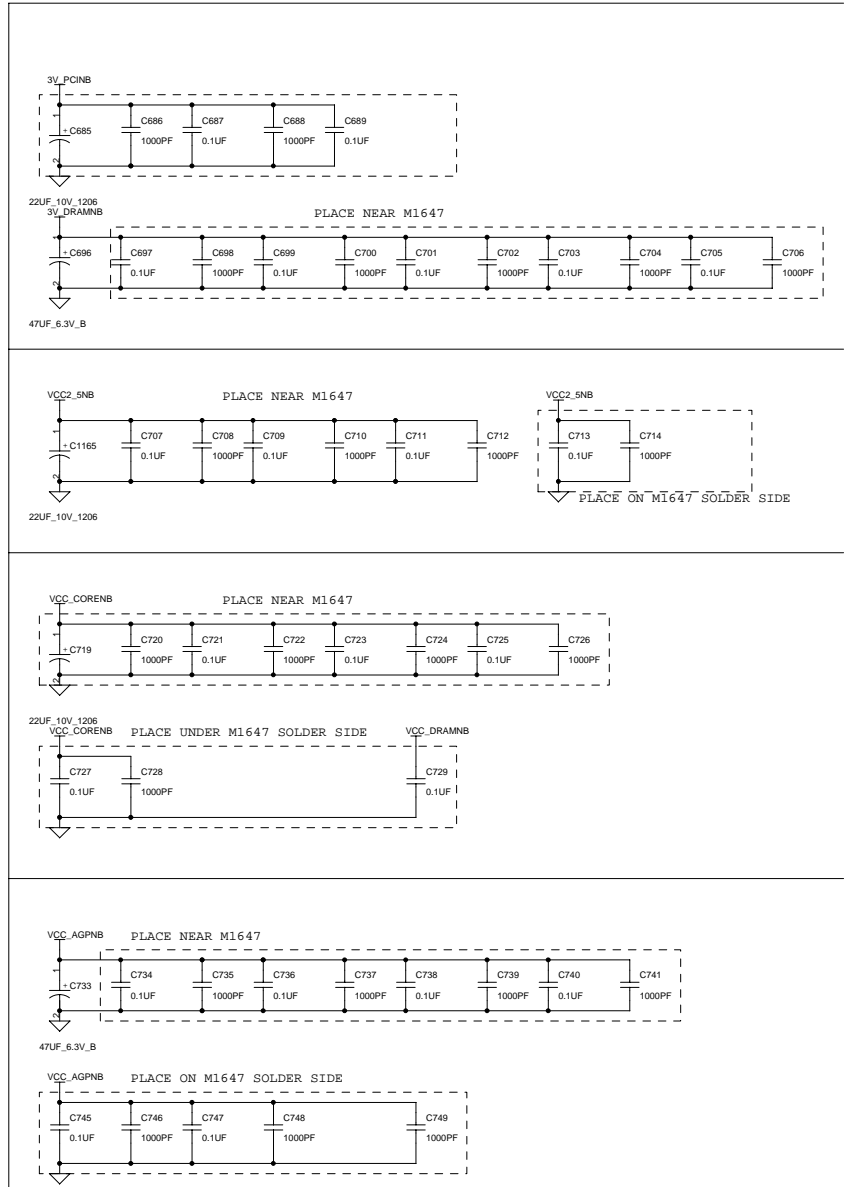
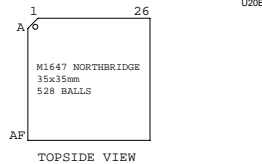
Monday, September 10, 2001

M1647 North Bridge (2/2)

M1647-SDR Power



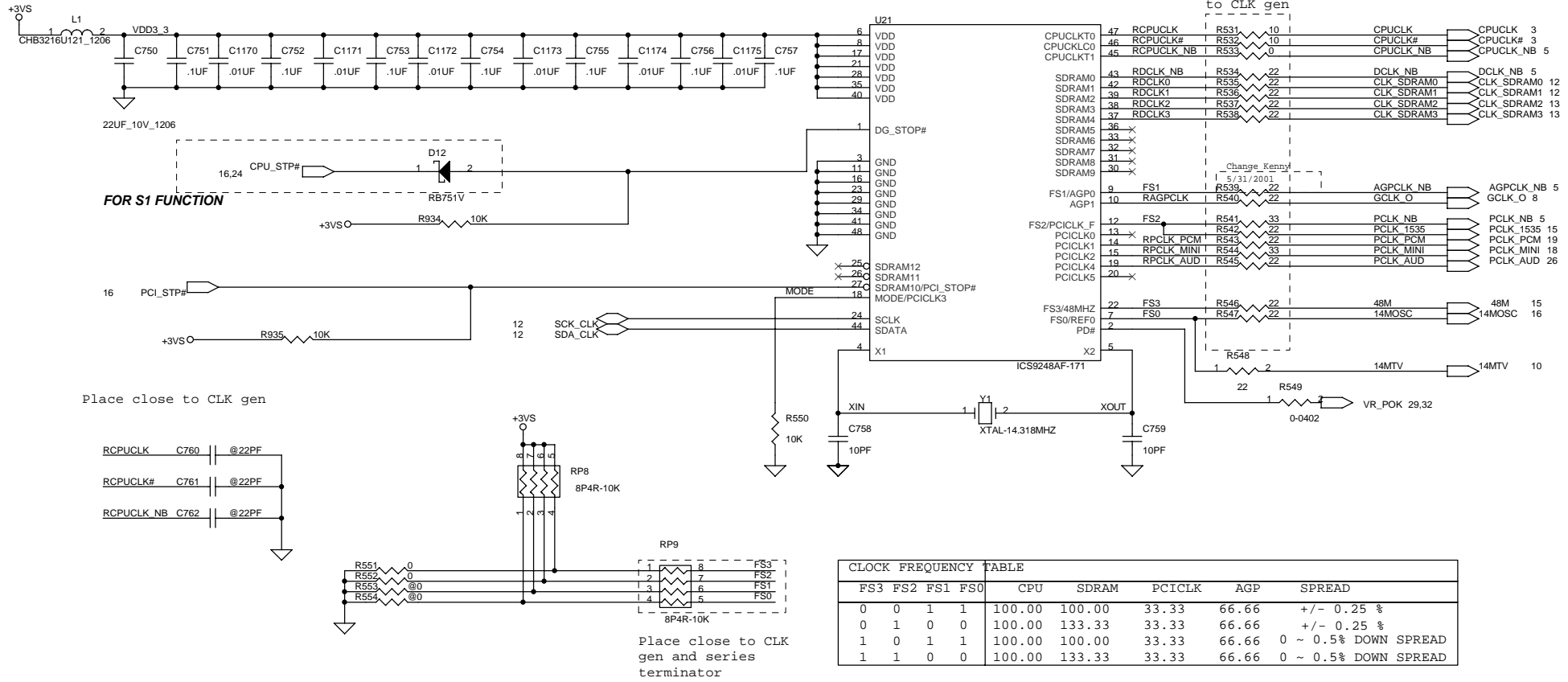
NOTE : R524,R525 Value depend on PCB impedance X 3



PLACE NEAR CLOCK GENERATOR

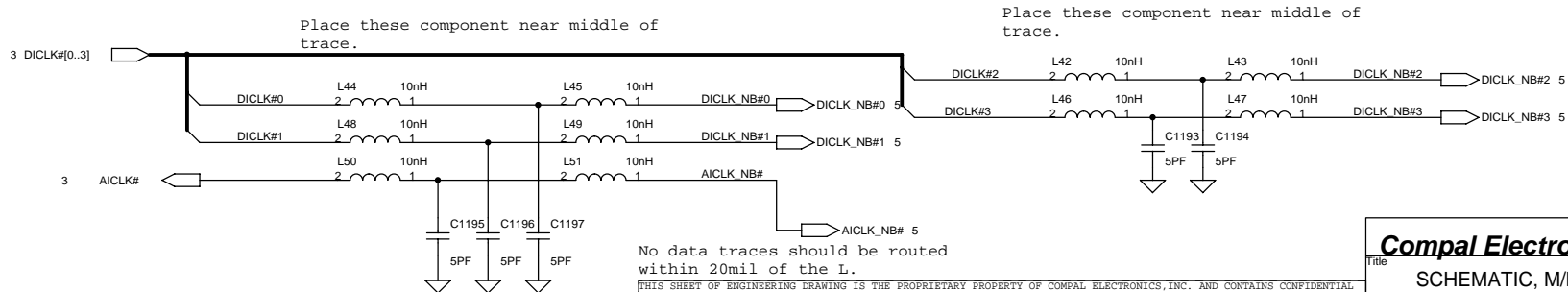
Clock Generator

Place close to CLK gen



Note : S0 - S1 & CPU ON C0-C3, THE CPU CLOCK CAN'T STOPPED

LCL



No data traces should be routed within 20mil of the L.

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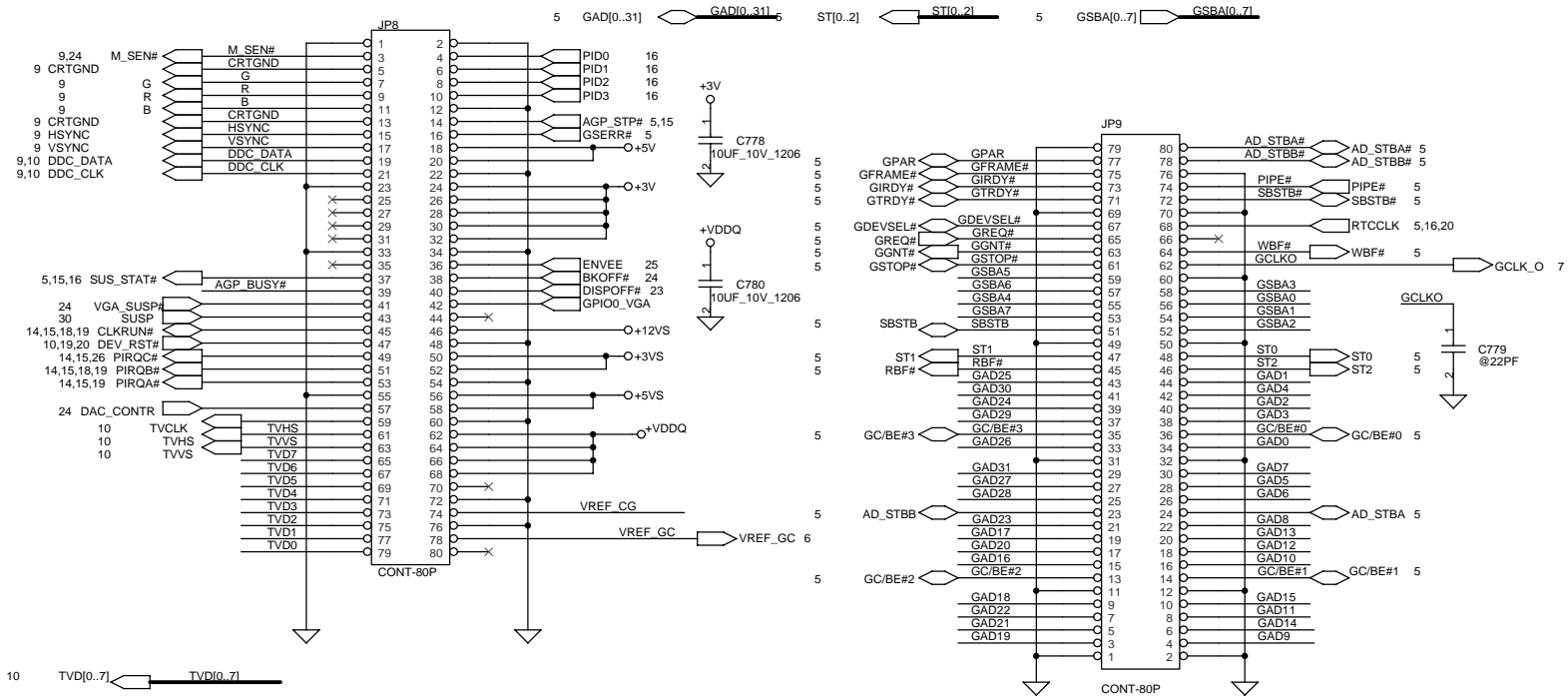
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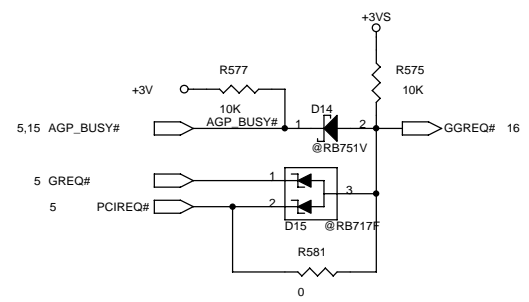
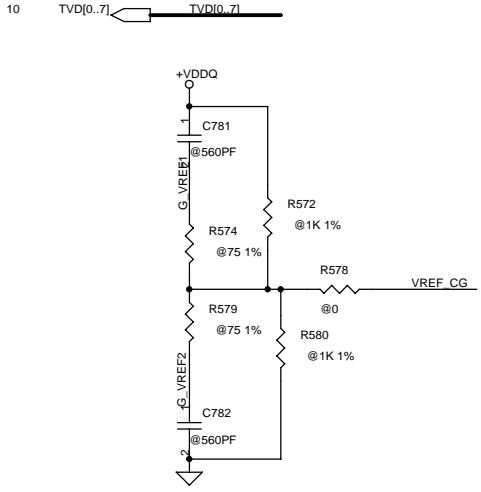
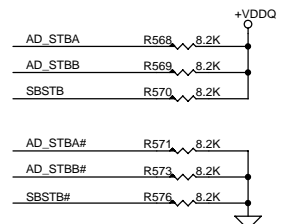
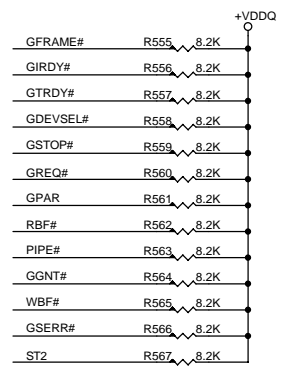
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AGP BUS PULL/DOWN RESISTER

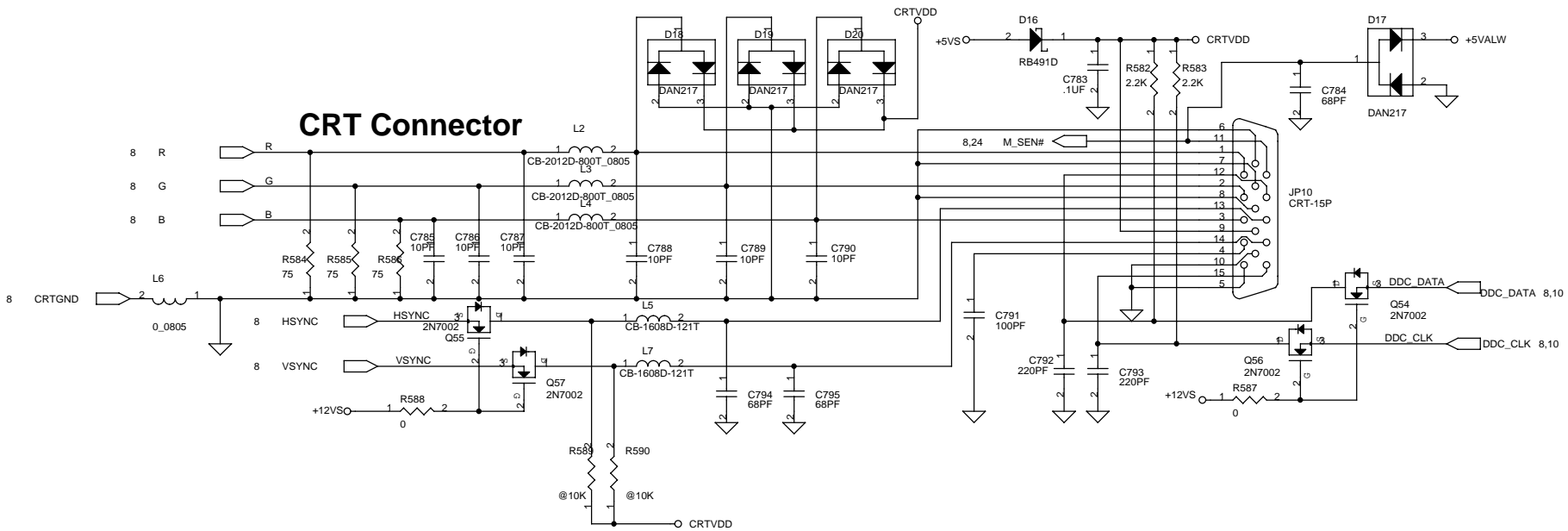


Change by 8/28/2000 ALI Suggest

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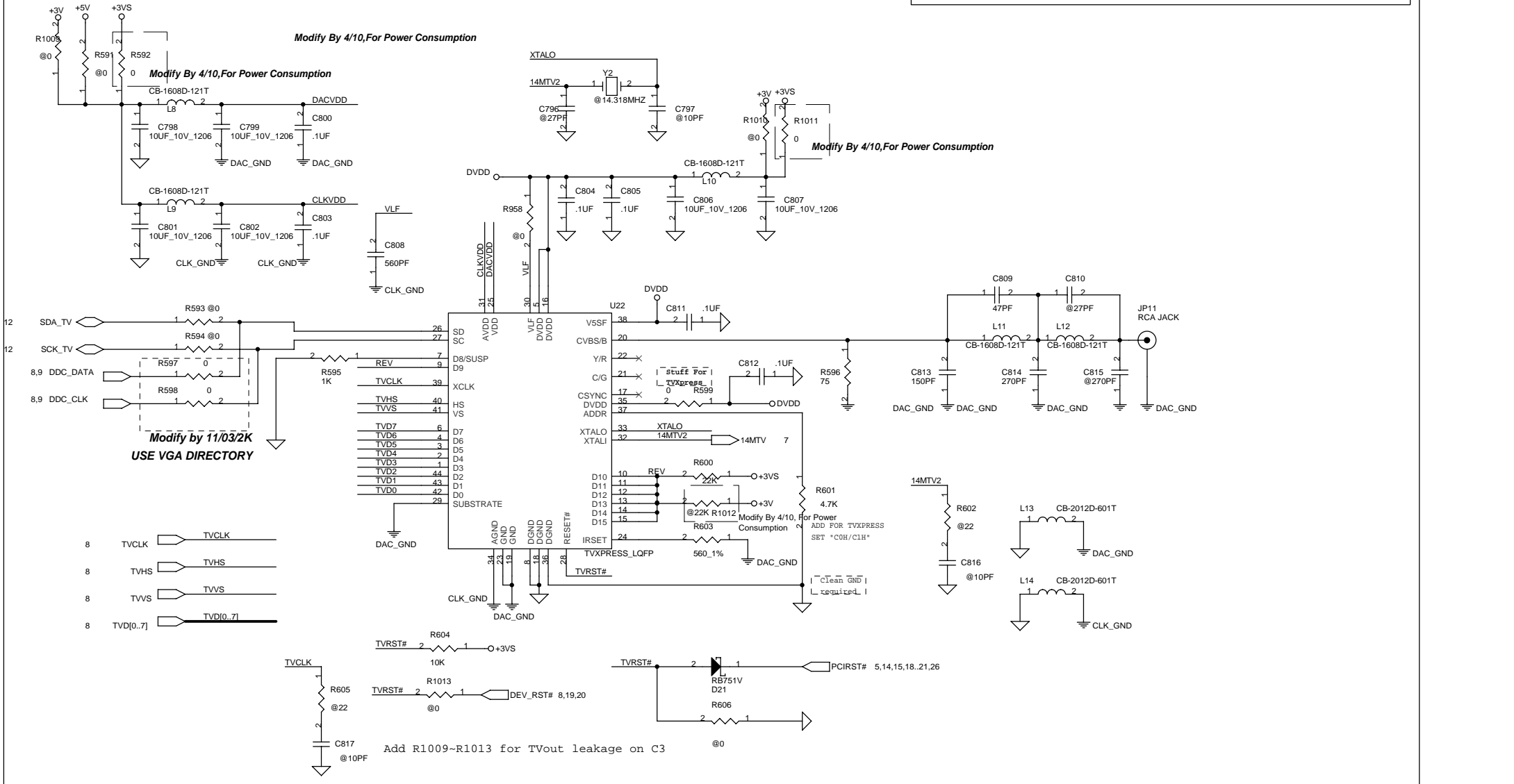
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CRT Connector



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CONFIGURATION

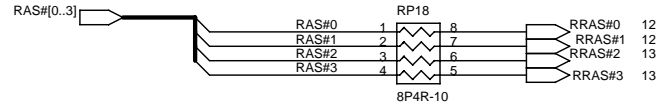
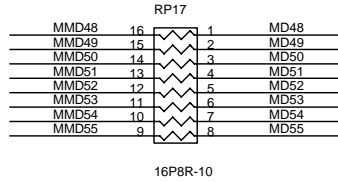
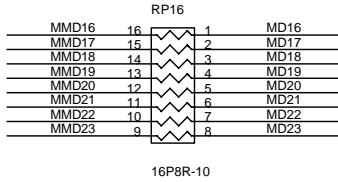
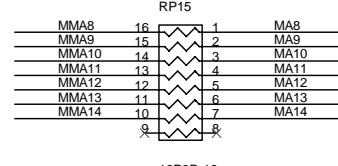
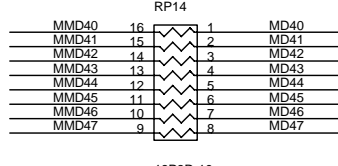
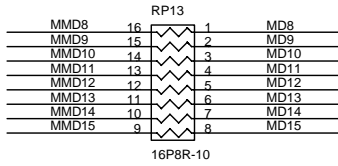
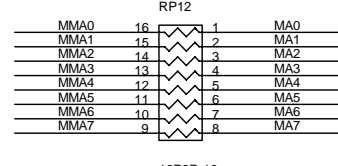
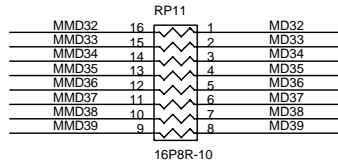
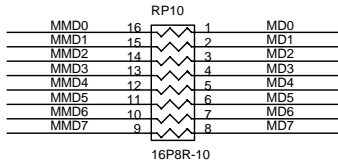
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R592	STUFF	OPEN	USE +3VS
R591	OPEN	STUFF	USE +5VS
R599	STUFF	OPEN	
R601	STUFF	OPEN	FOR TVXPRESS ADDR SET *C0H/C1H*
R603	560 1K	OPEN	
C808	560PF	OPEN	
D21	STUFF	OPEN	
R606	OPEN	STUFF	
R958	OPEN	STUFF	

NOTE :CH7004 ADDR SET 76H BY PIN 29 *LOW*

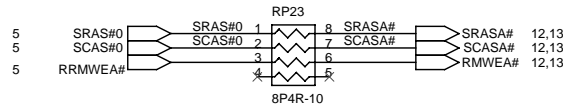
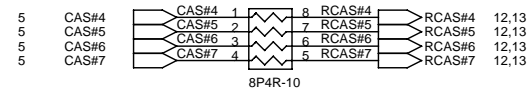
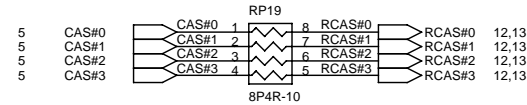
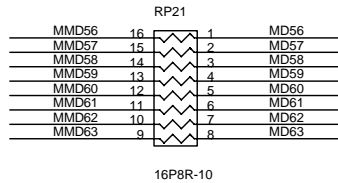
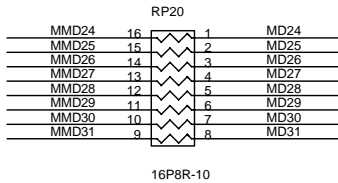
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LA-736B : RP18 ~ RP23 USED 22 Ohm



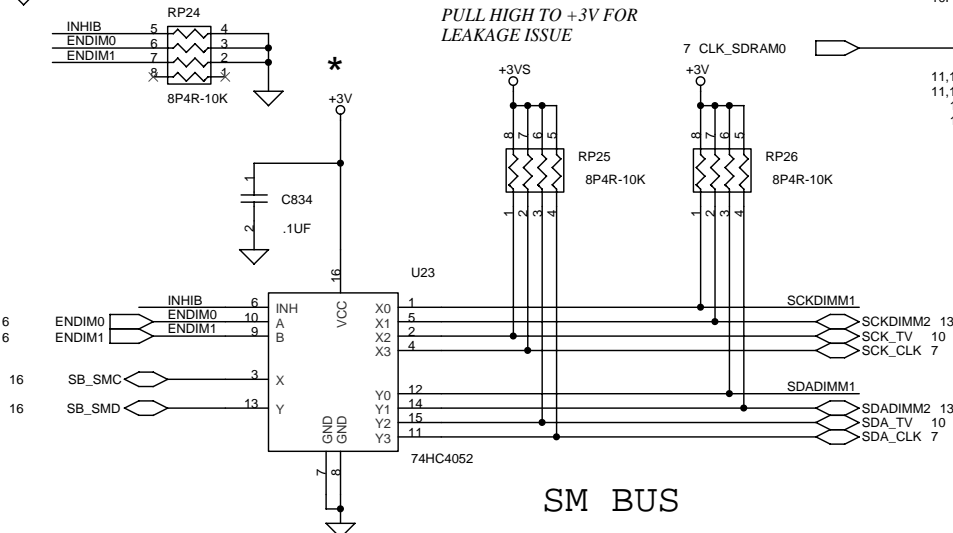
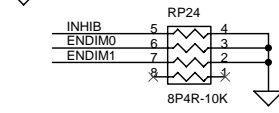
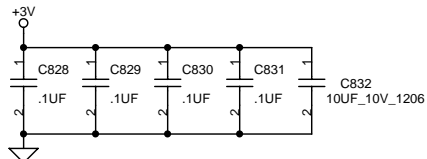
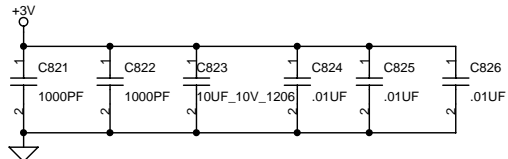
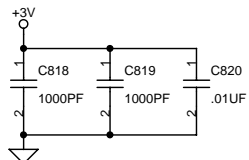
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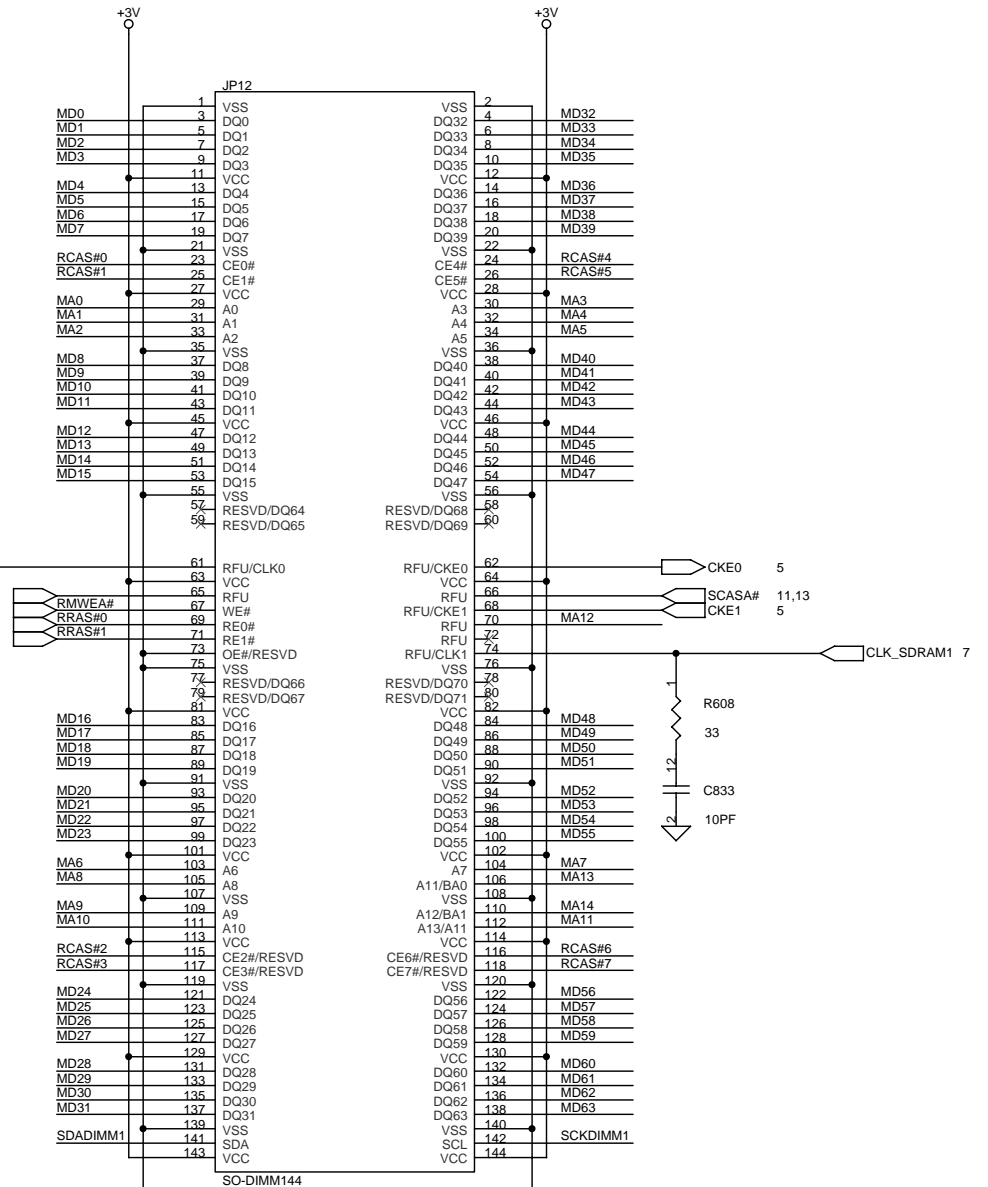
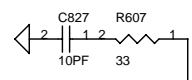
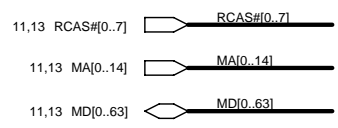
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INHIB	ENDIM1	ENDIM0	CHANNEL ON
0	0	0	SCKDIMM0/SDADIMM0
0	0	1	SCKDIMM1/SDADIMM1
0	1	0	SCK_TV/SDA_TV
0	1	1	SCK_CLK/SDA_CLK
1	X	X	NONE



DIMM1

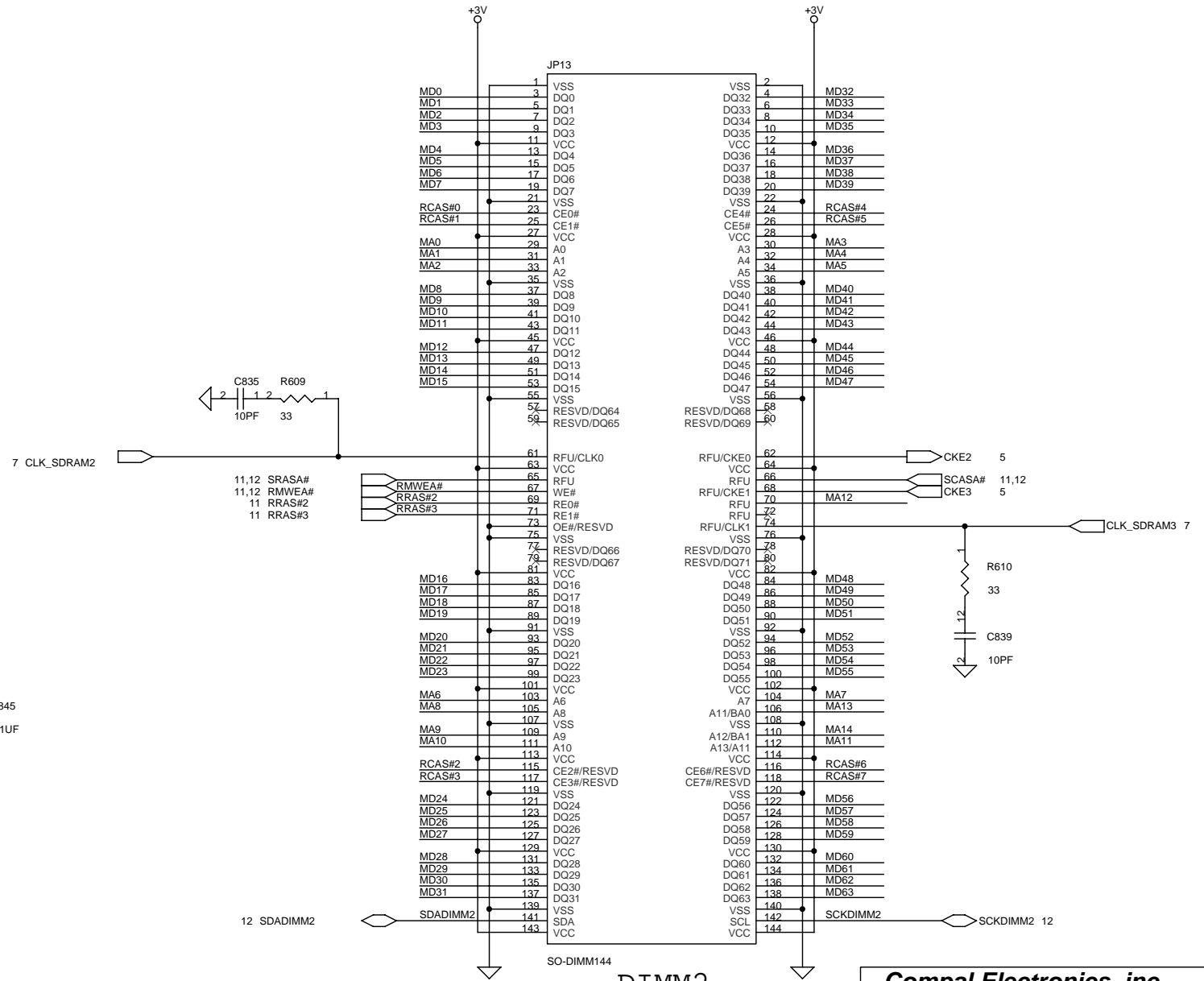
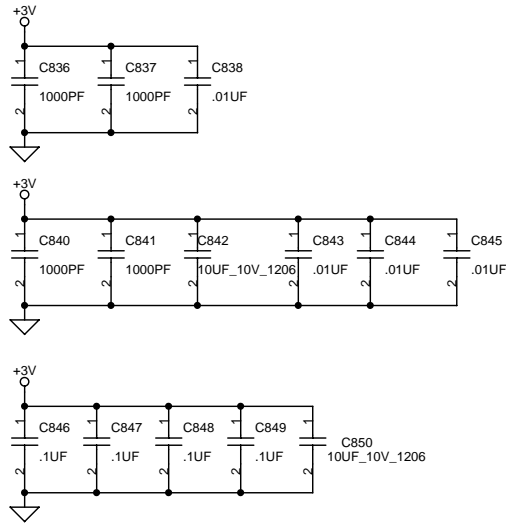
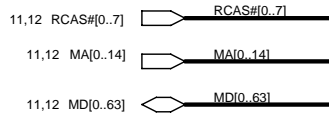
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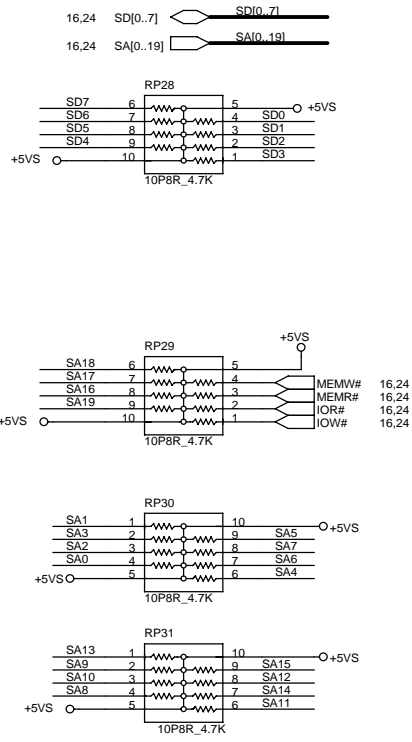


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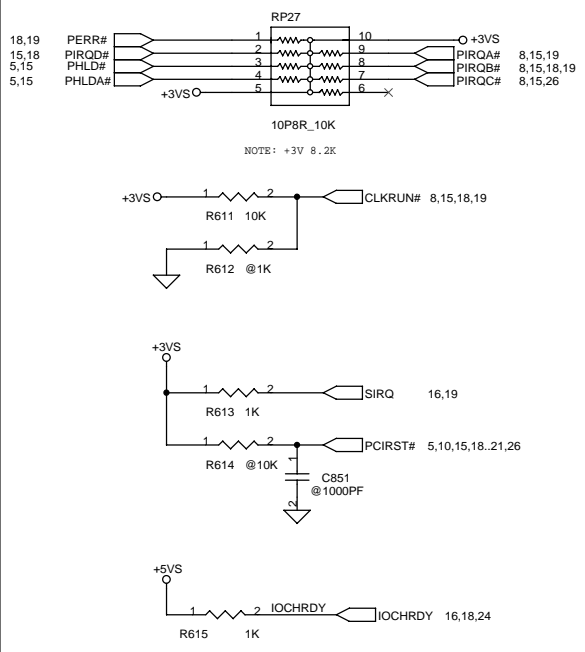
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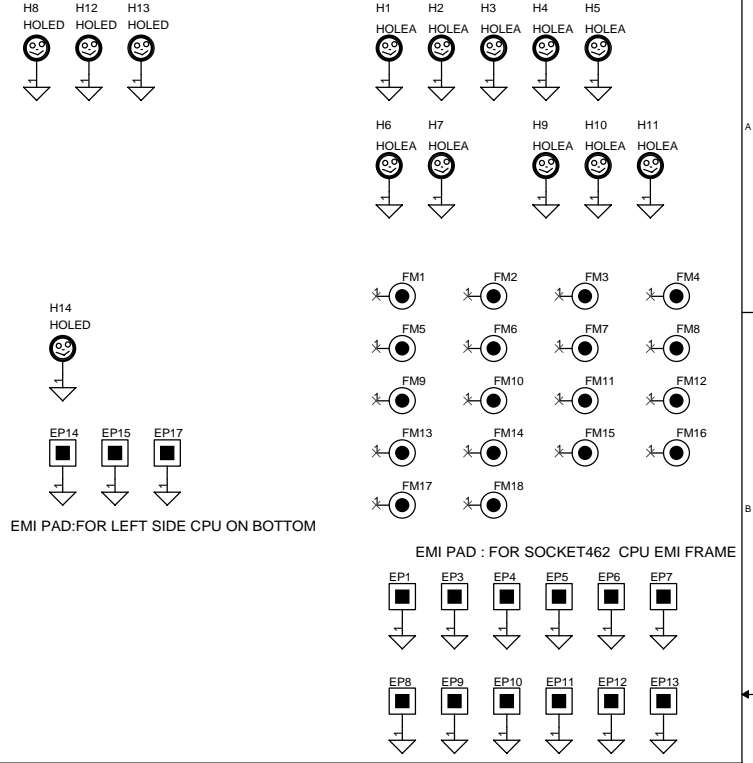
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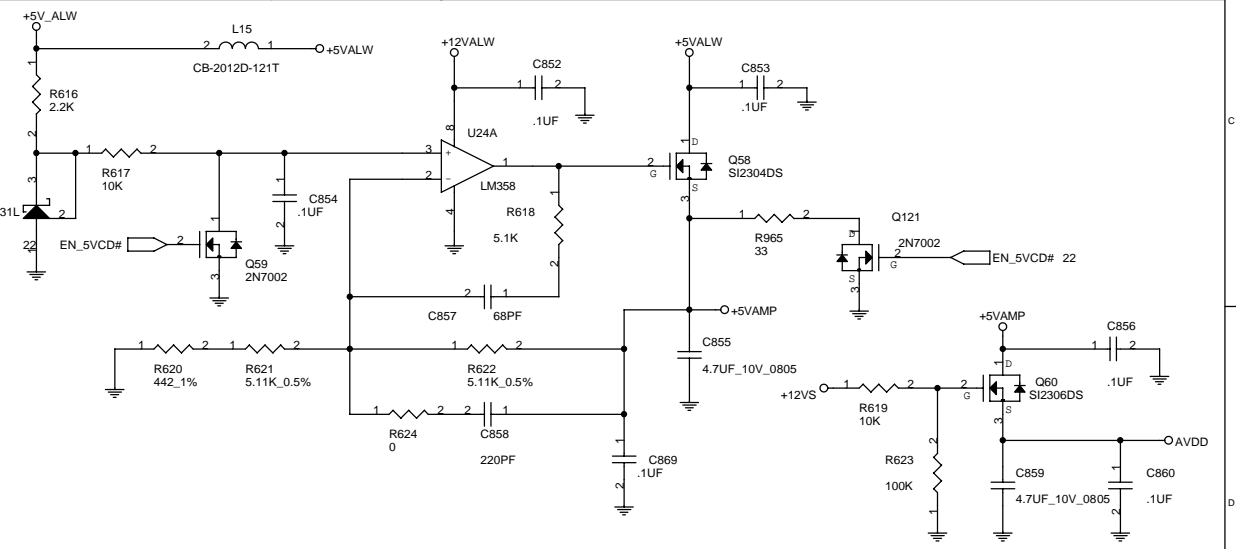
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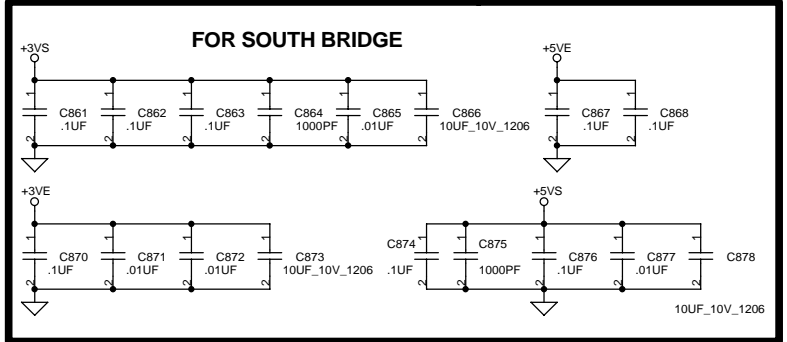
For VGA BROAD HOLE



AUDIO POWER SOURCE

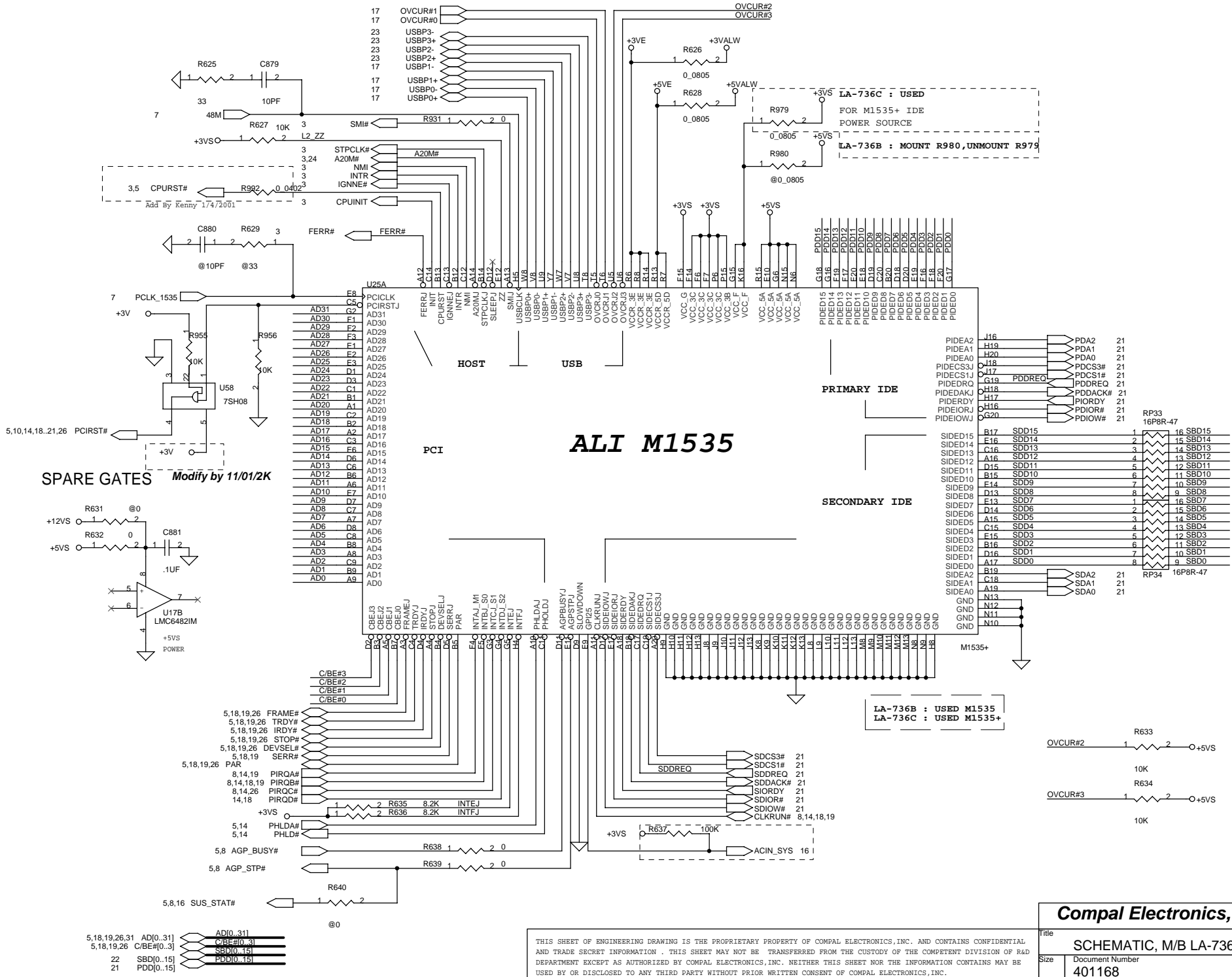


FOR SOUTH BRIDGE



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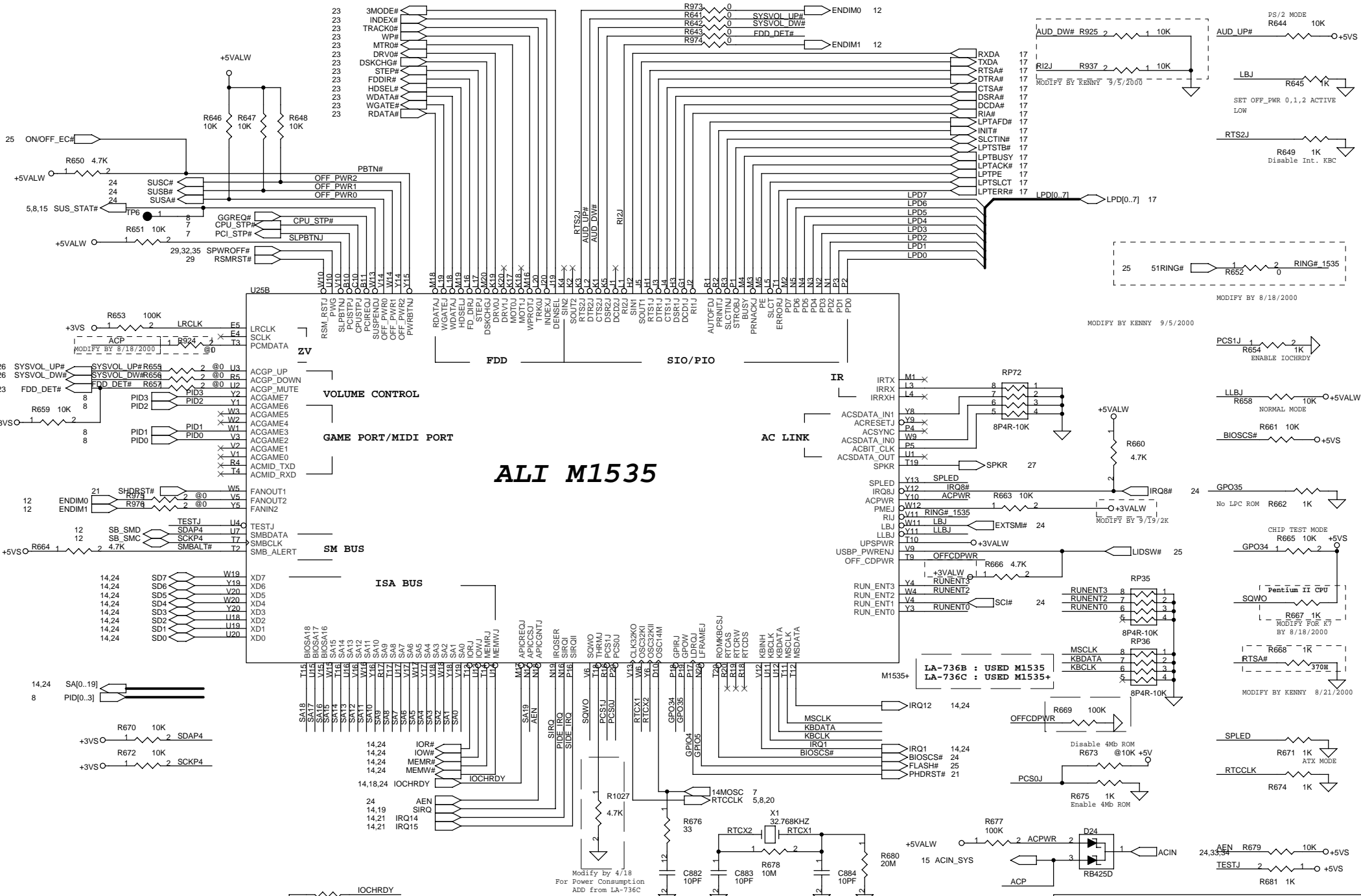


ALI M1535

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- SBD[0..15]
- 22 SBD[0..15]
- 21 PDD[0..15]



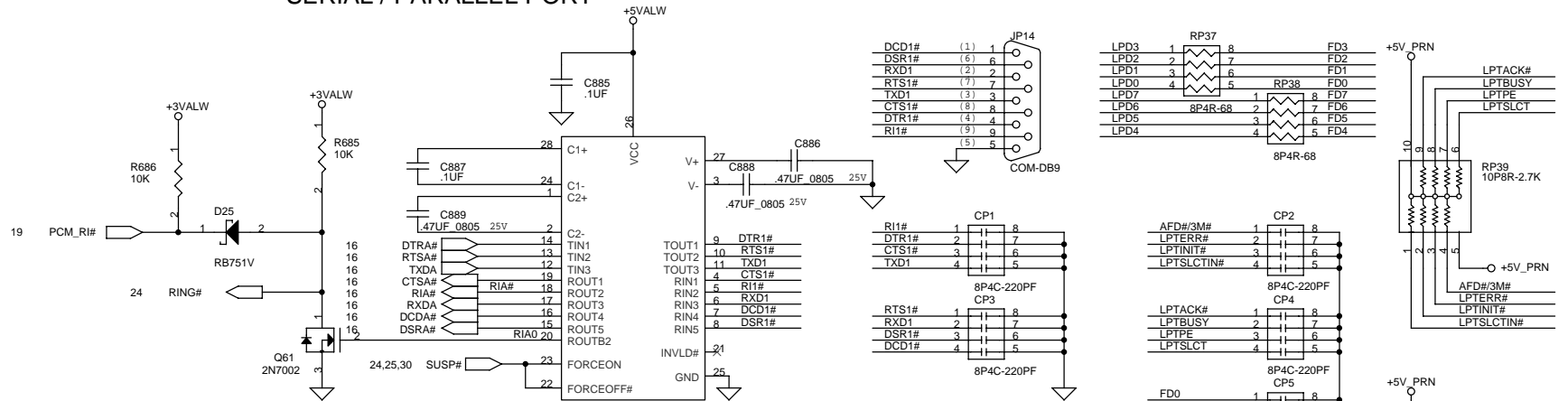
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Compal Electronics, inc.

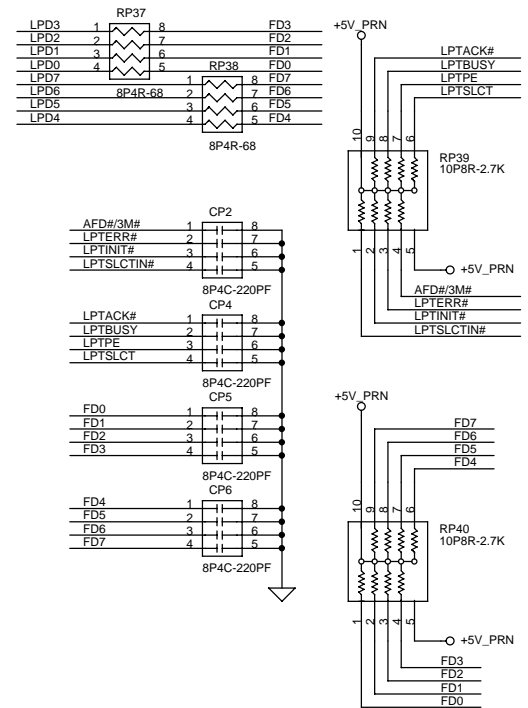
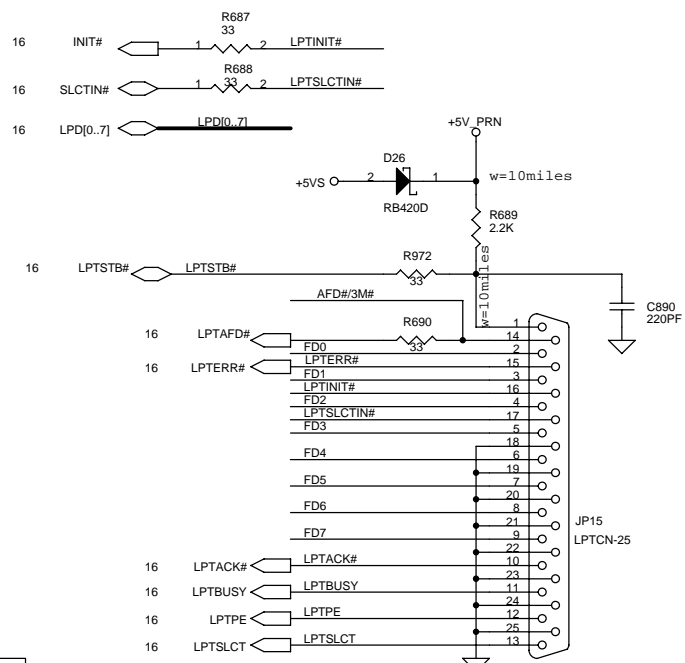
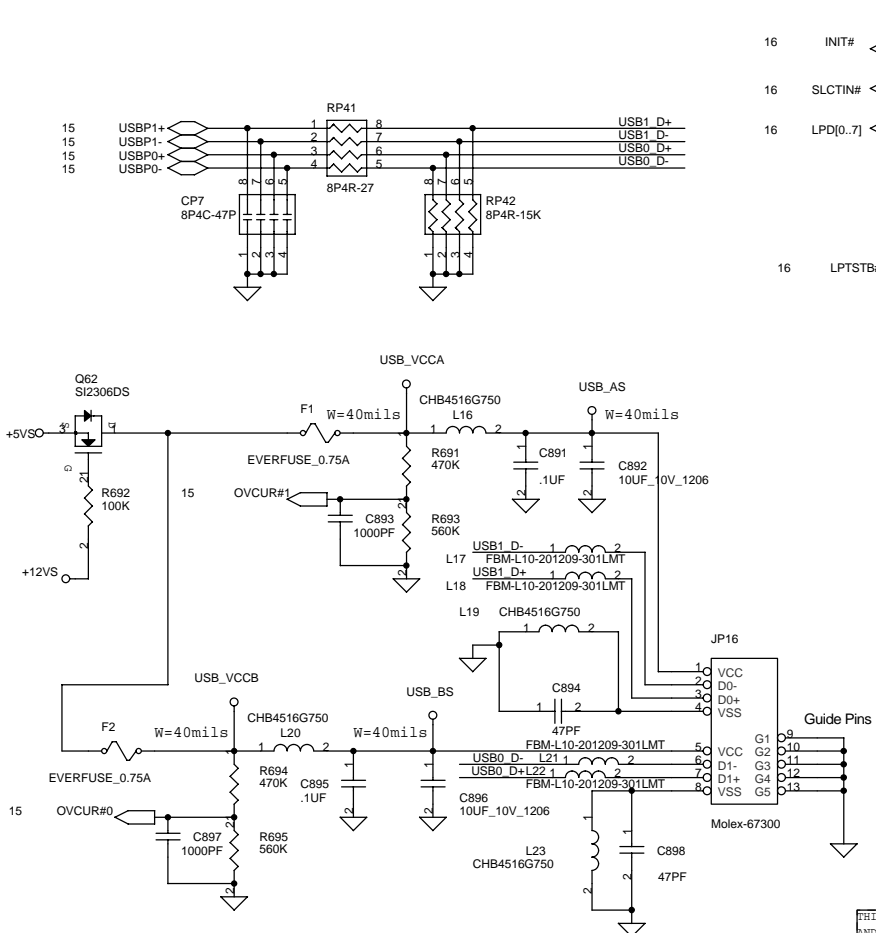
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SERIAL / PARALLEL PORT

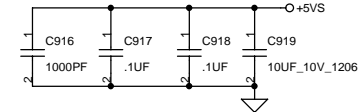
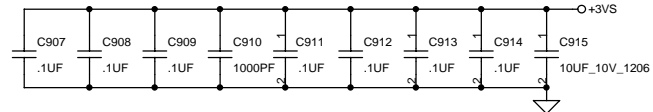
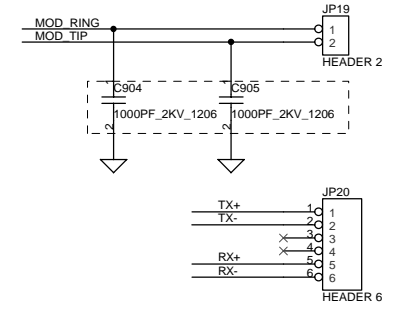
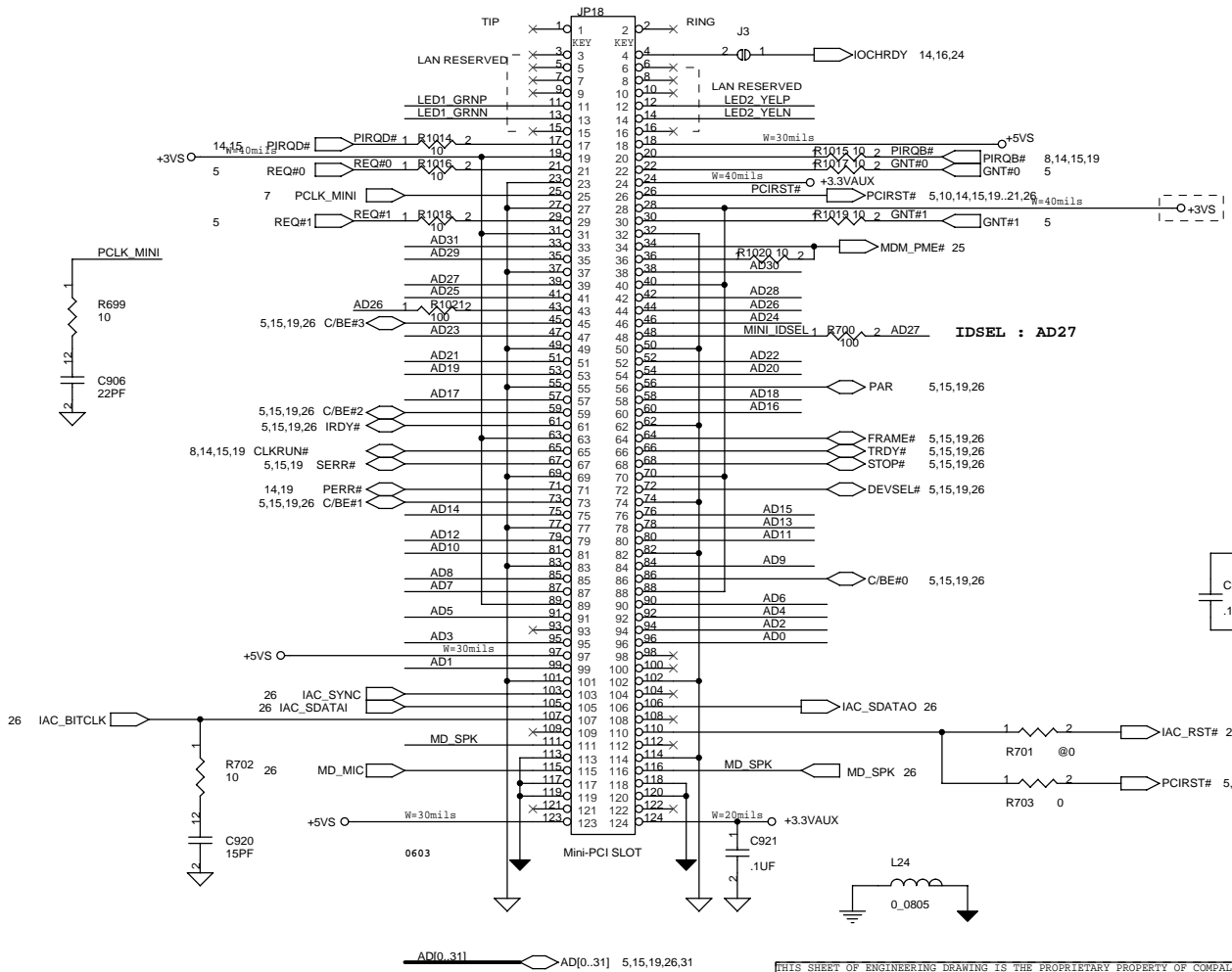
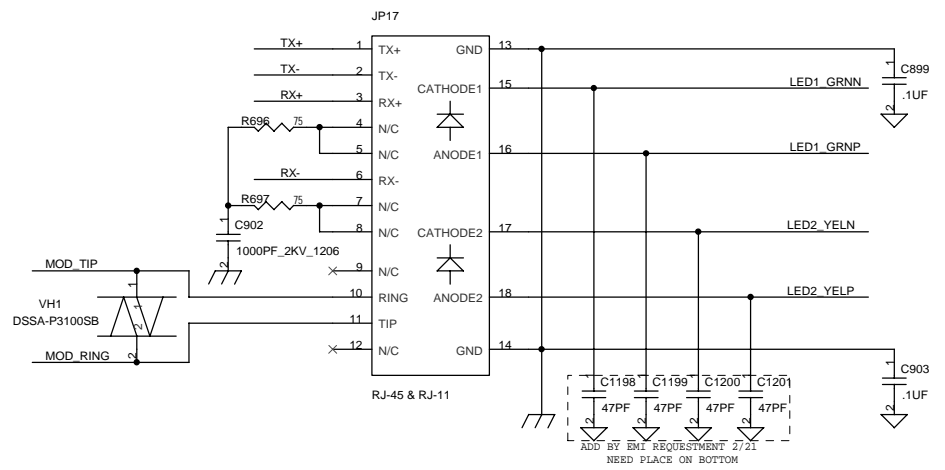
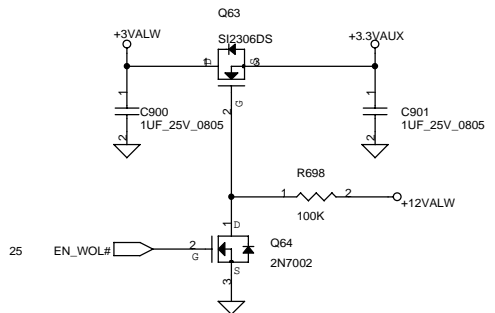


USB



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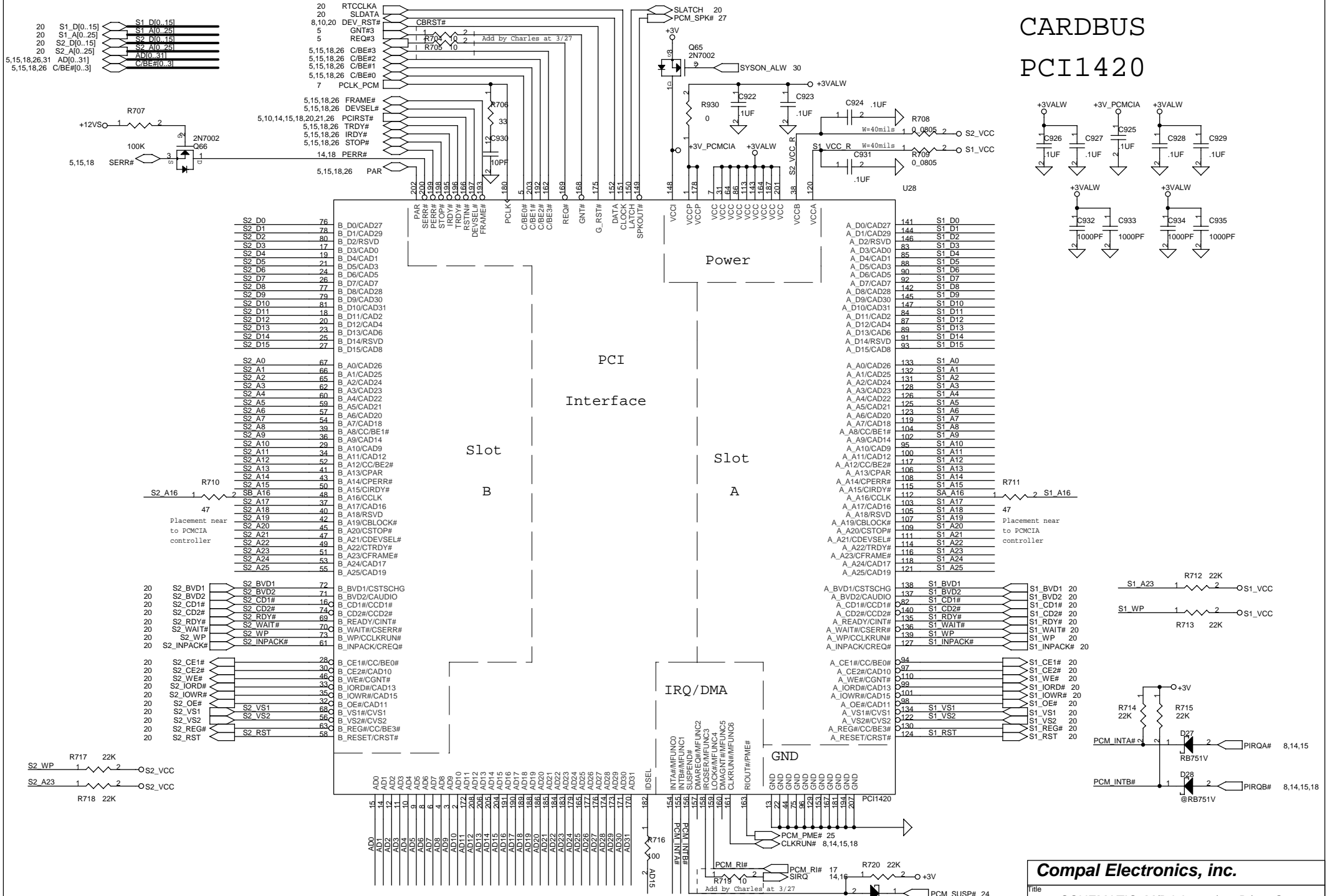
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CARDBUS PCI1420



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Compal Electronics, inc.

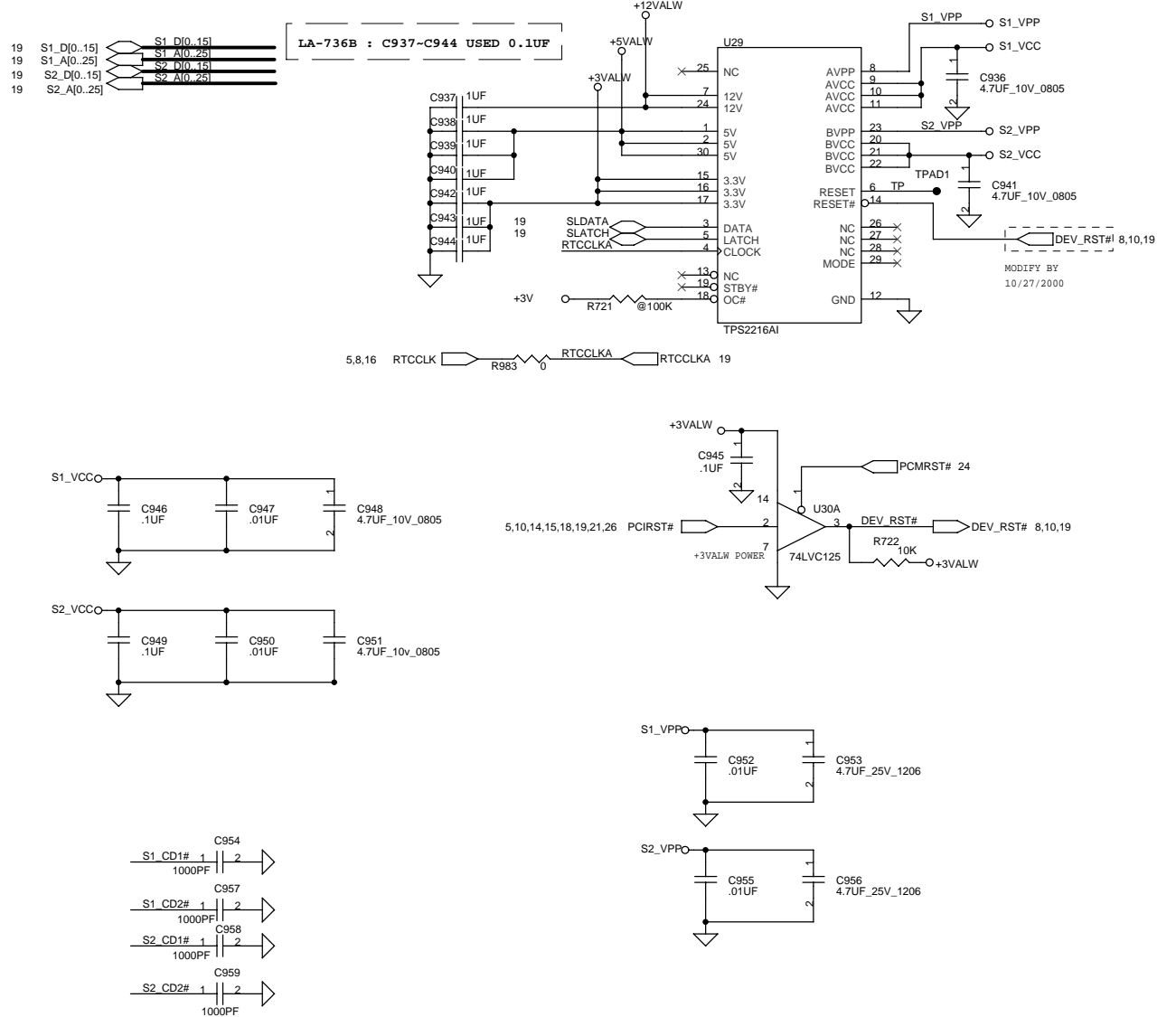
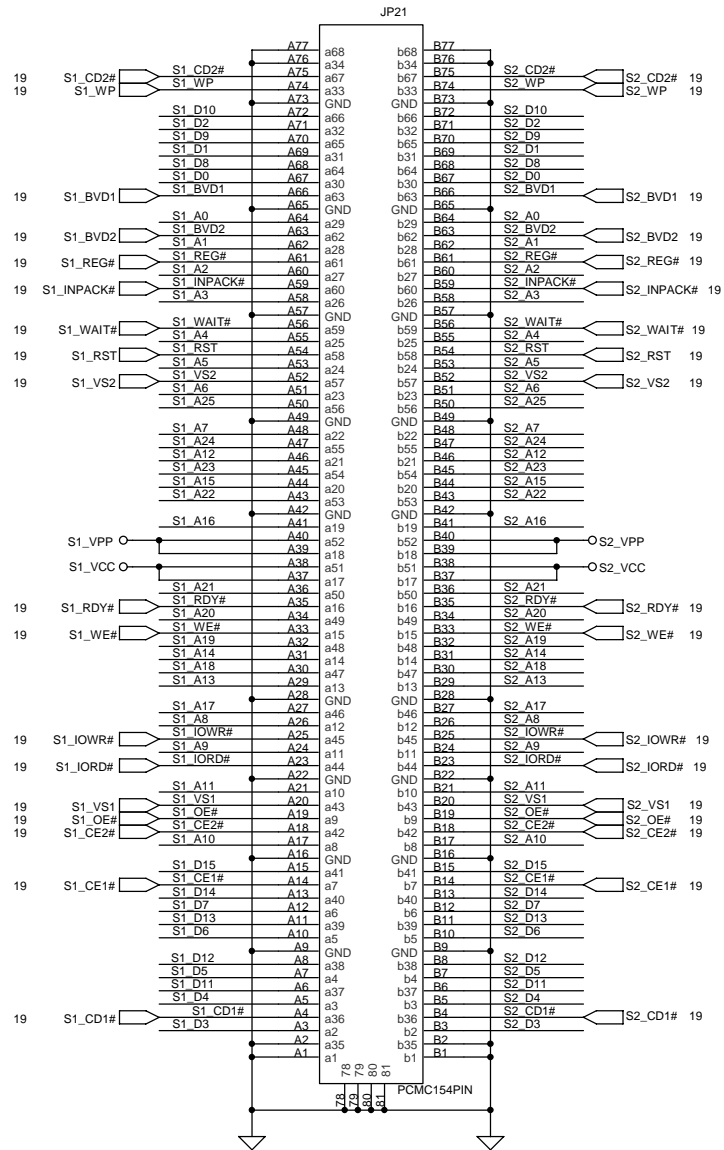
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Size: B Document Number: 401168 Rev: 1F

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PCMCIA POWER CTRL.

CARDBUS SOCKET



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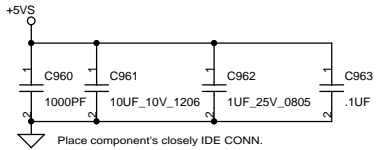
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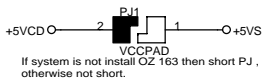
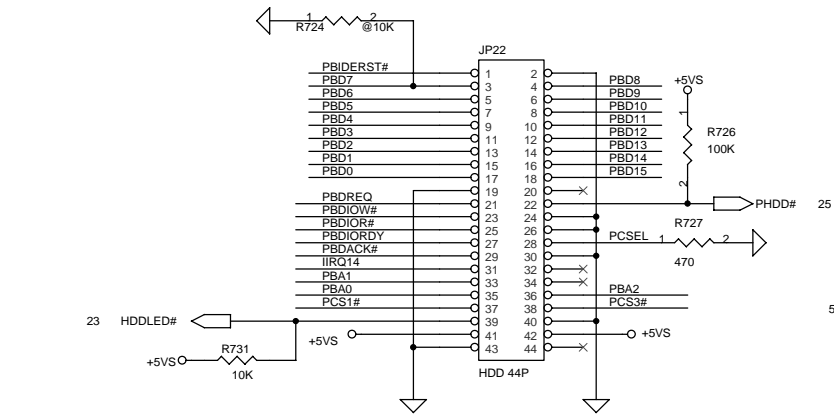
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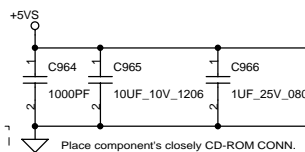
IDE & CD-ROM CONNECTORS



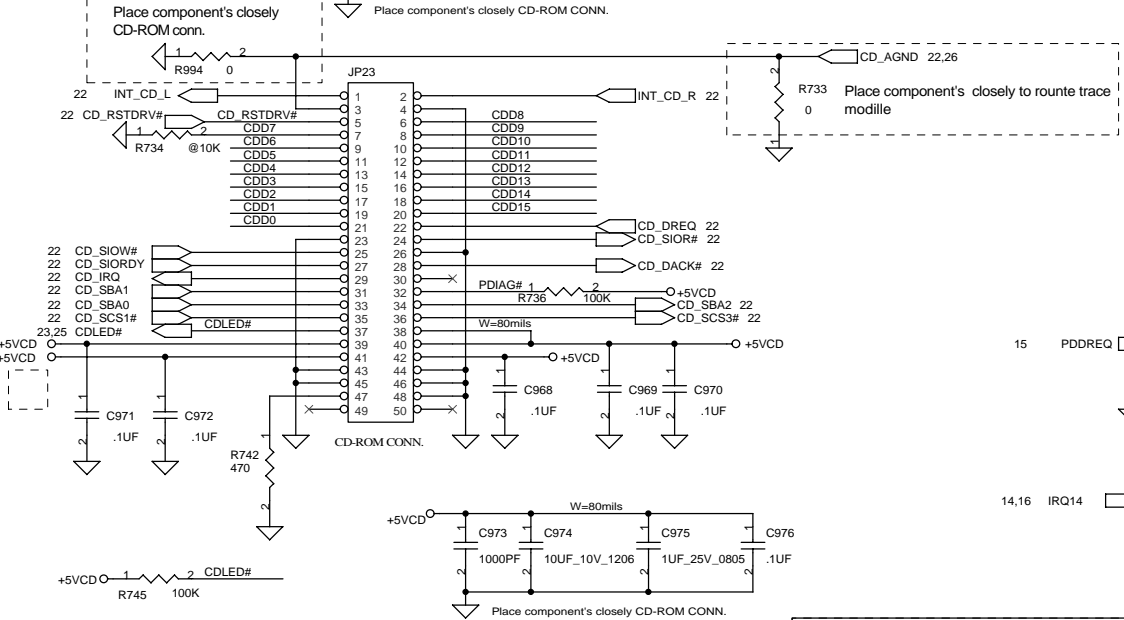
Place component's closely IDE CONN.



If system is not install OZ 163 then short PJ, otherwise not short.

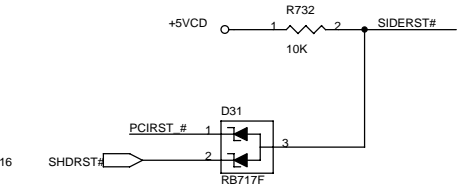
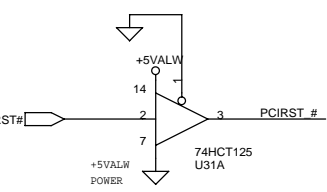
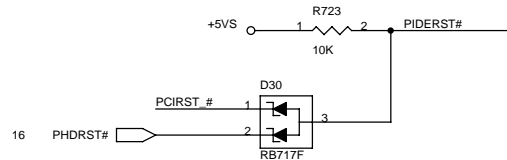
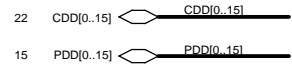


Place component's closely CD-ROM CONN.

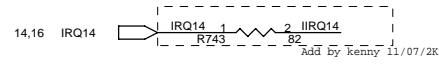
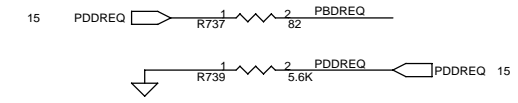
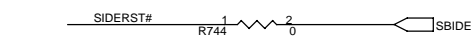
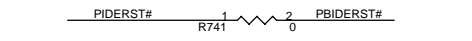
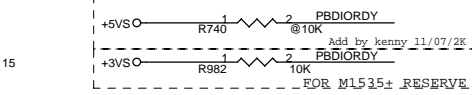
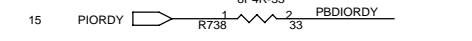
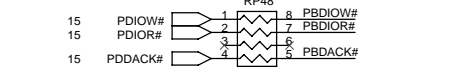
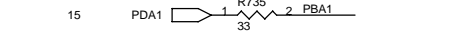
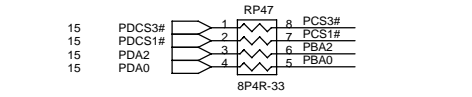
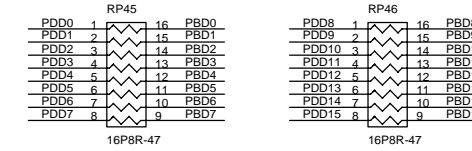
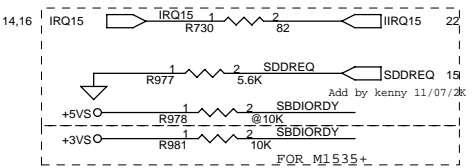
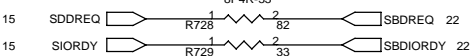
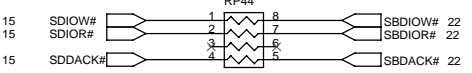
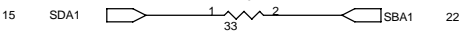
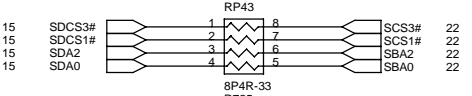


Place component's closely CD-ROM conn.

Place component's closely to route trace

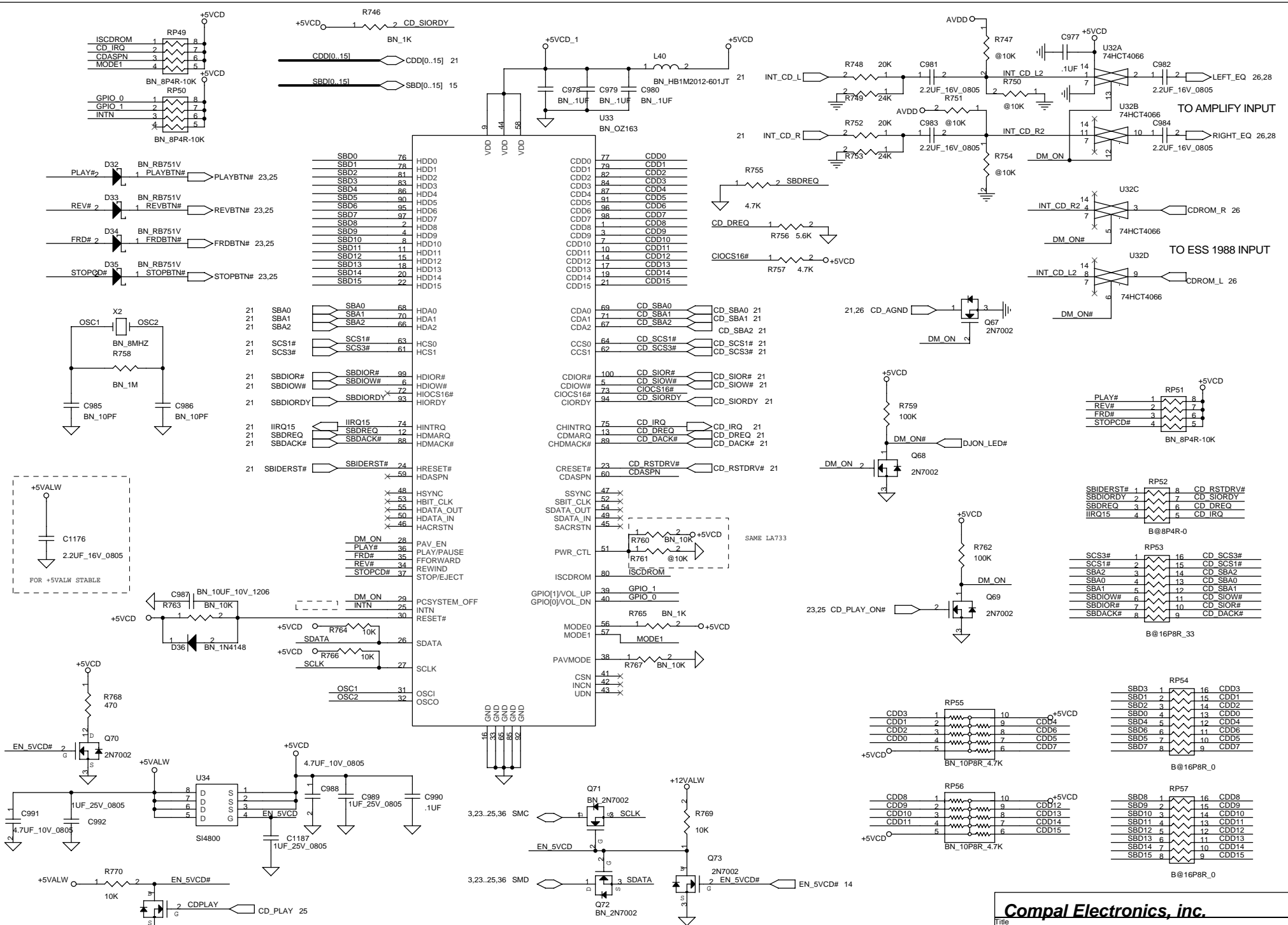


LA-736B : MOUNT R978,R740 UNMOUNT R981,R982



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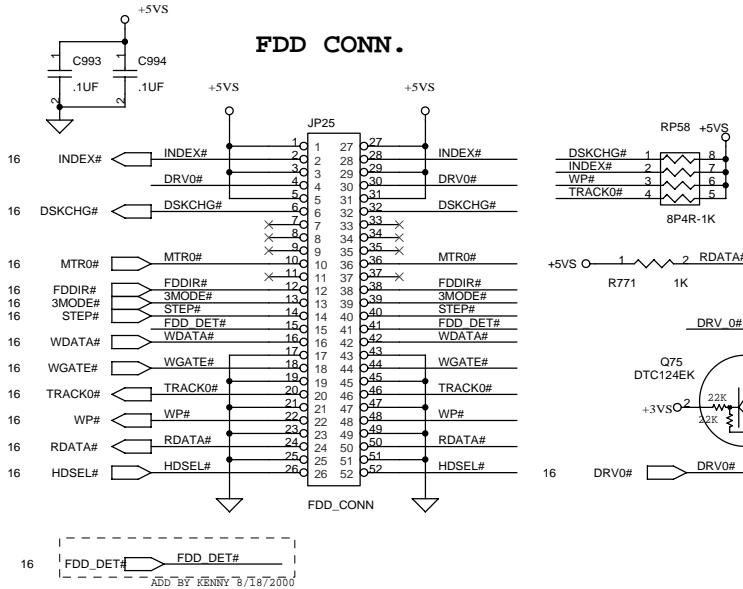
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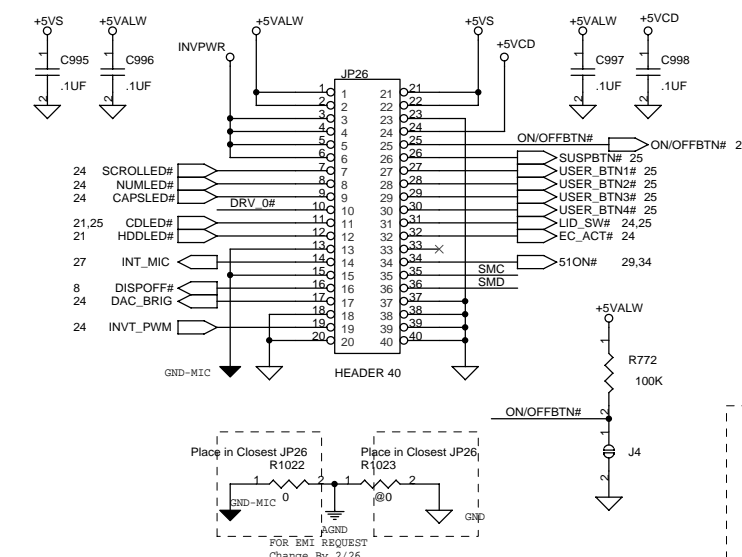
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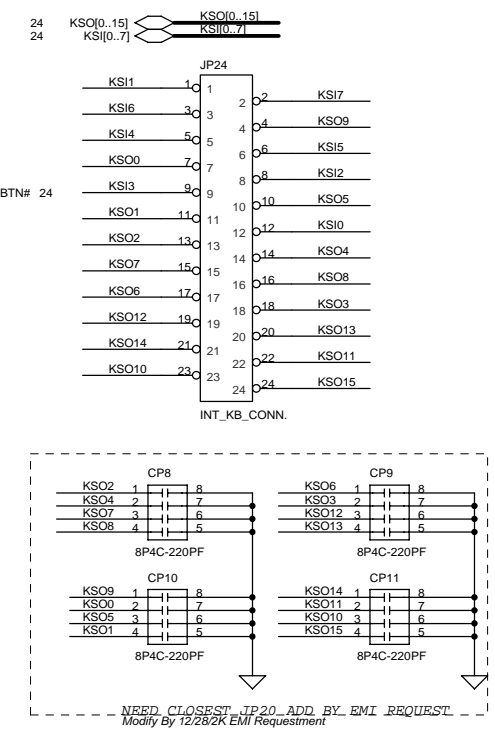
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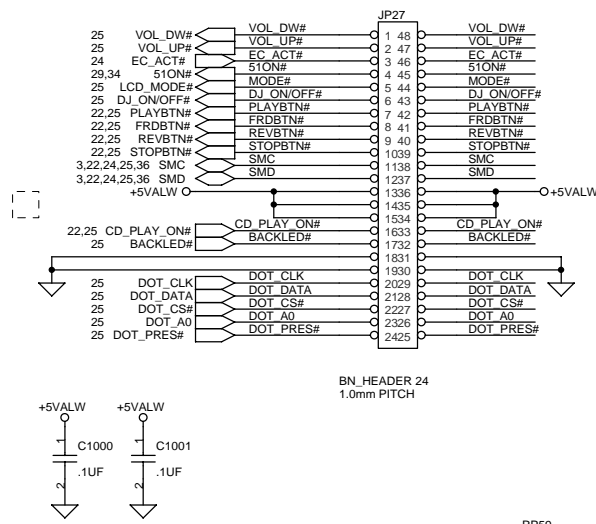
SWITCH BOARD CONN.



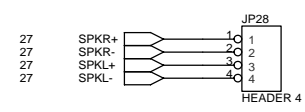
INT_KBD CONN.



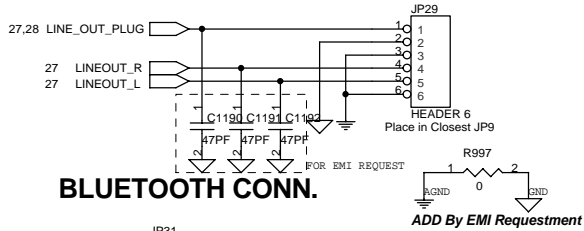
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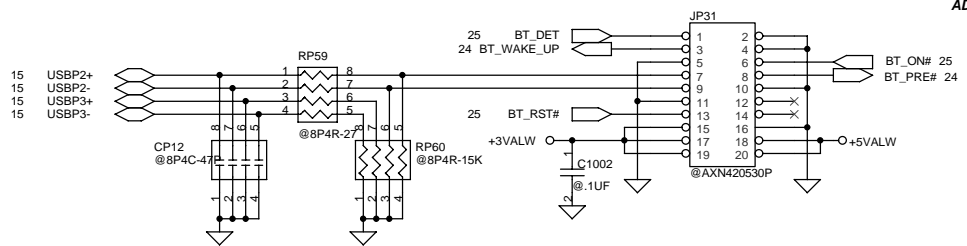
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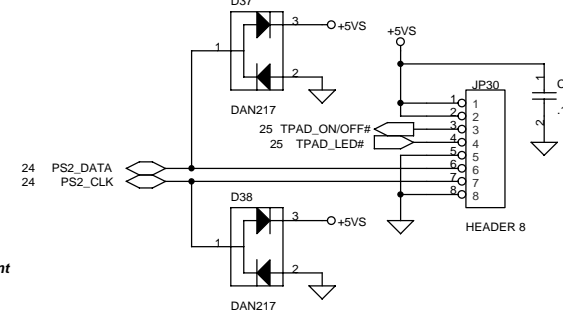
LINE OUT CONN.



BLUETOOTH CONN.

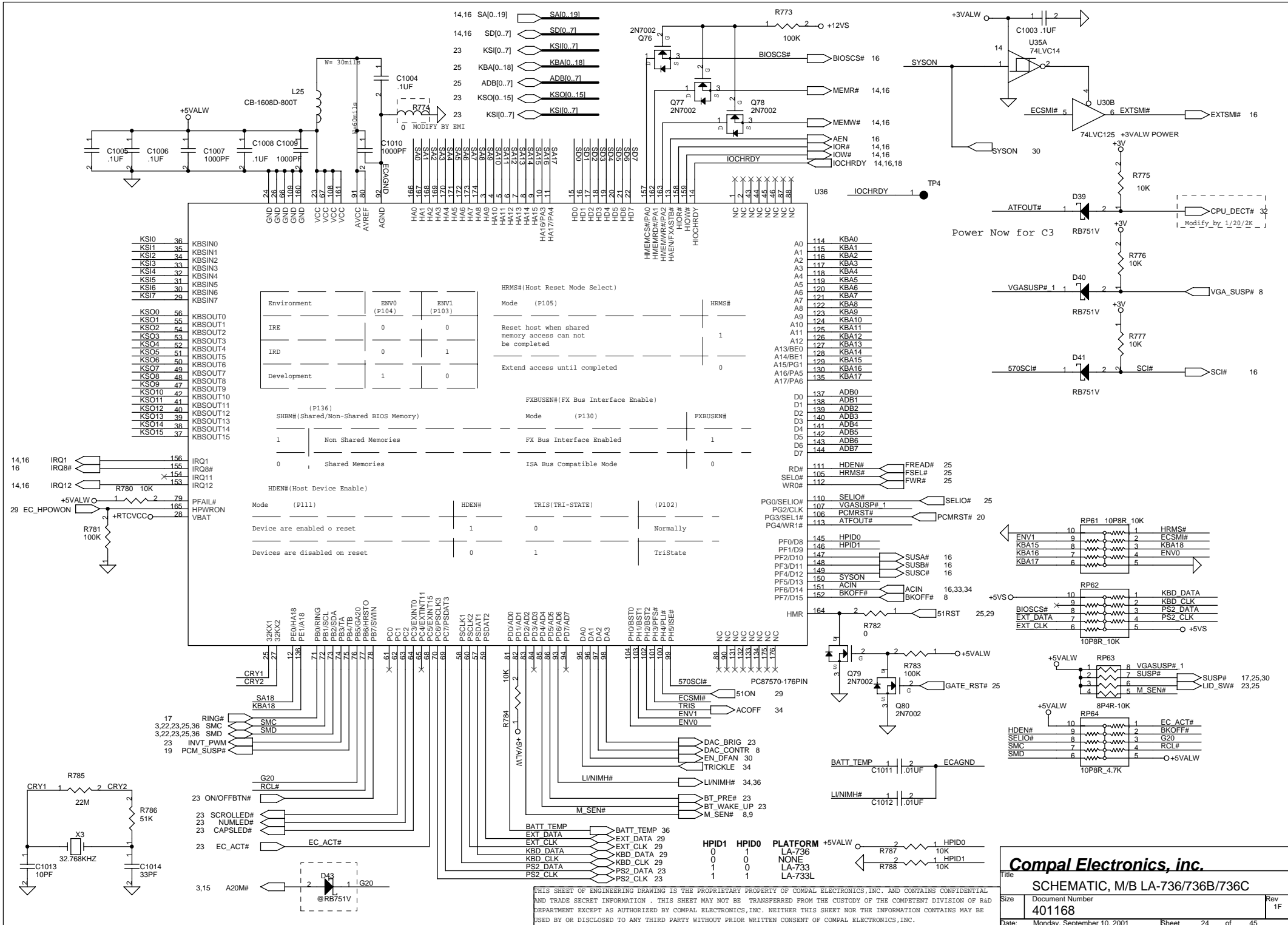


TOUCH PAD CONN.



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- KSI0 36
- KSI1 35
- KSI2 34
- KSI3 33
- KSI4 32
- KSI5 31
- KSI6 30
- KSI7 29
- KSI8 28
- KSI9 27
- KSI10 26
- KSI11 25
- KSI12 24
- KSI13 23
- KSI14 22
- KSI15 21
- KSI16 20
- KSI17 19
- KSI18 18
- KSI19 17
- KSI20 16
- KSI21 15
- KSI22 14
- KSI23 13
- KSI24 12
- KSI25 11
- KSI26 10
- KSI27 9
- KSI28 8
- KSI29 7
- KSI30 6
- KSI31 5
- KSI32 4
- KSI33 3
- KSI34 2
- KSI35 1

Environment	ENV0 (P104)	ENV1 (P103)	HRMS# (Host Reset Mode Select)	Mode (P105)	HRMS#
IRE	0	0	Reset host when shared memory access can not be completed		1
IRD	0	1	Extend access until completed		0
Development	1	0			

SHRM# (Shared/Non-Shared BIOS Memory) (P136)		Mode (P130)		FXBUSEN#
1	Non Shared Memories	FX Bus Interface Enabled		1
0	Shared Memories	ISA Bus Compatible Mode		0

HDEN# (Host Device Enable) (P111)		HDEN#	TRIS (TRI-STATE) (P102)
Device are enabled o reset		1	0 Normally
Devices are disabled on reset		0	1 TriState

- A0 114 KBA0
- A1 115 KBA1
- A2 116 KBA2
- A3 117 KBA3
- A4 118 KBA4
- A5 119 KBA5
- A6 120 KBA6
- A7 121 KBA7
- A8 122 KBA8
- A9 123 KBA9
- A10 124 KBA10
- A11 125 KBA11
- A12 126 KBA12
- A13 127 KBA13
- A13/BE0 128 KBA14
- A14/BE1 129 KBA15
- A15/PG1 130 KBA16
- A16/PA5 131 KBA17
- A17/PA6 132 KBA18

- D0 137 ADB0
- D1 138 ADB1
- D2 139 ADB2
- D3 140 ADB3
- D4 141 ADB4
- D5 142 ADB5
- D6 143 ADB6
- D7 144 ADB7

- RD# 111 HDEN#
- SEL# 105 HRMS#
- WR# 112 FWR#

- PG0/SELIO# 110 SELIO#
- PG2/CLK 107 VGASUSP# 1
- PG3/SEL1# 106 PCMRST# 20
- PG4/WR1# 113 ATFOU#

- PF0/D8 145 HPID0
- PF1/D9 146 HPID1
- PF2/D10 147 SUSAS#
- PF3/D11 148 SUSBS#
- PF4/D12 149 SYSON
- PF5/D13 150 ACIN
- PF6/D14 152 BKOFF#
- PF7/D15 151 BKOFF#

- HMR 164
- 570SCI#
- ECSMI#
- TRIS
- ENV1
- ENV0

- DAC BRIG 23
- DAC CONTR 8
- EN DFAN 30
- TRICKLE 34
- LI/NIMH#
- LI/NIMH# 34,36
- BT_PRE# 23
- BT_WAKE_UP 23
- M_SEN# 8,9

- BATT_TEMP
- EXT_DATA
- EXT_CLK
- KBD_DATA
- PS2_DATA
- PS2_CLK

- HPID1 0
- HPID0 1
- PLATFORM LA-736
- LA-733
- LA-733L

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File: SCHEMATIC, M/B LA-736/736B/736C

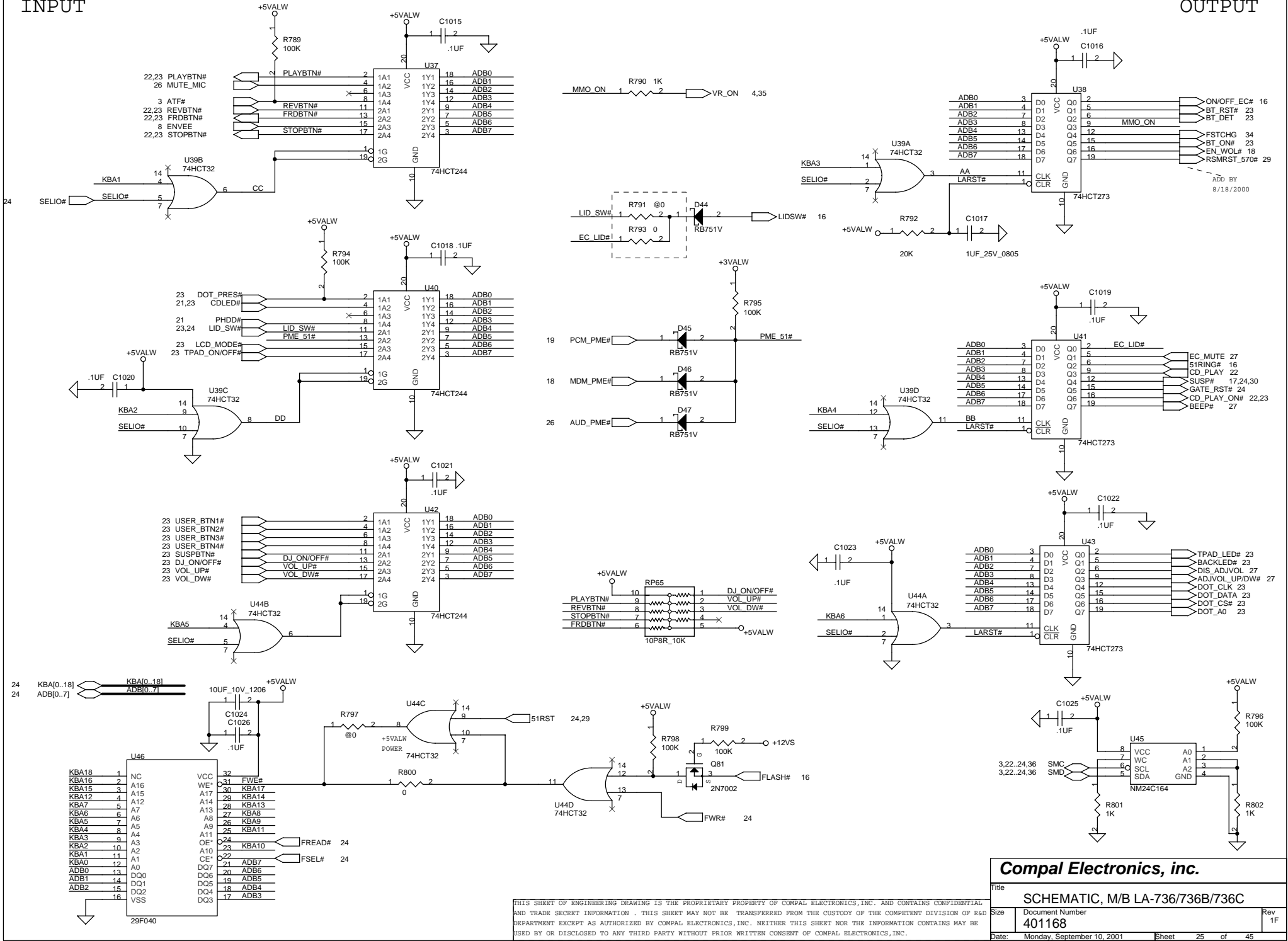
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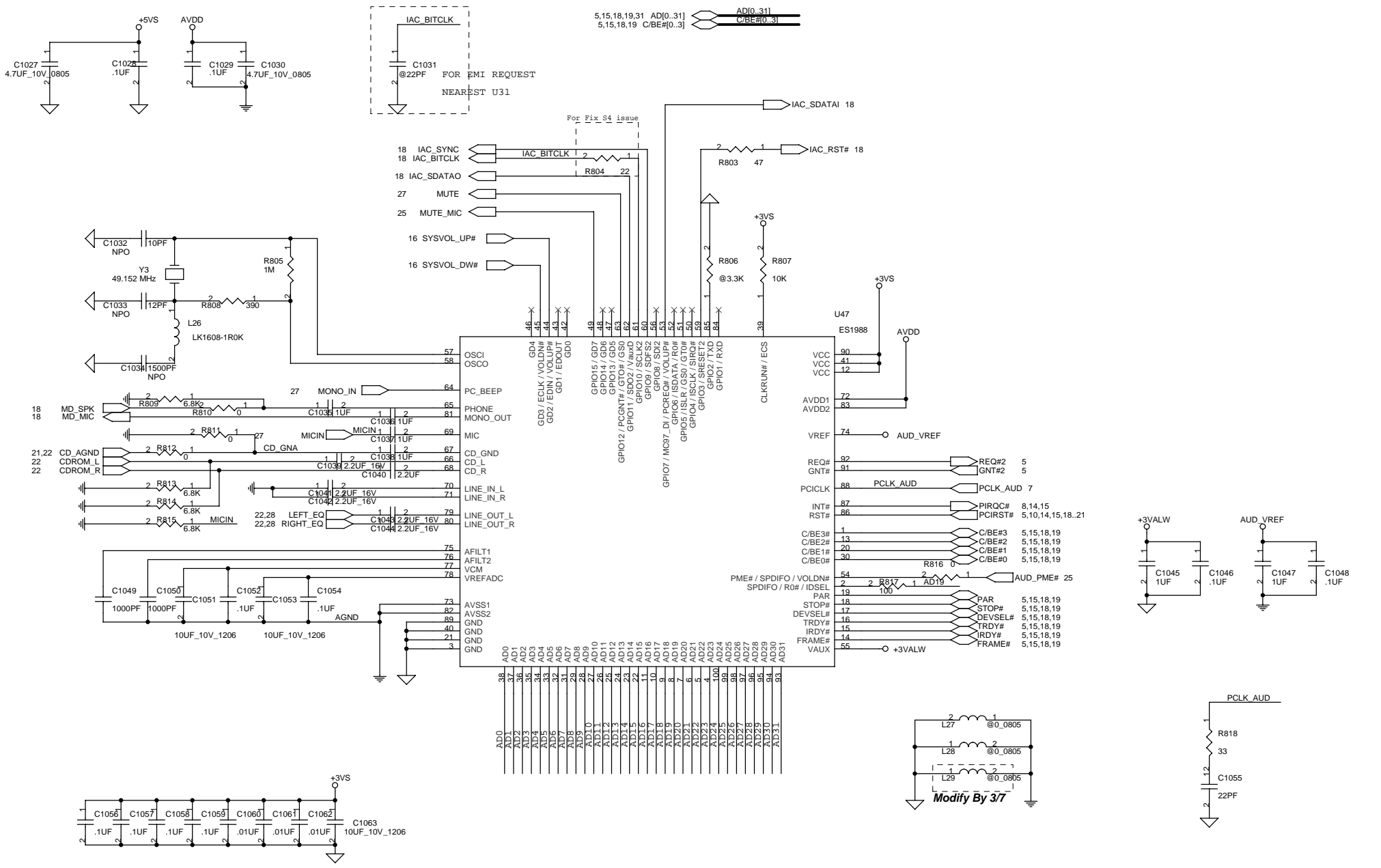
INPUT

OUTPUT



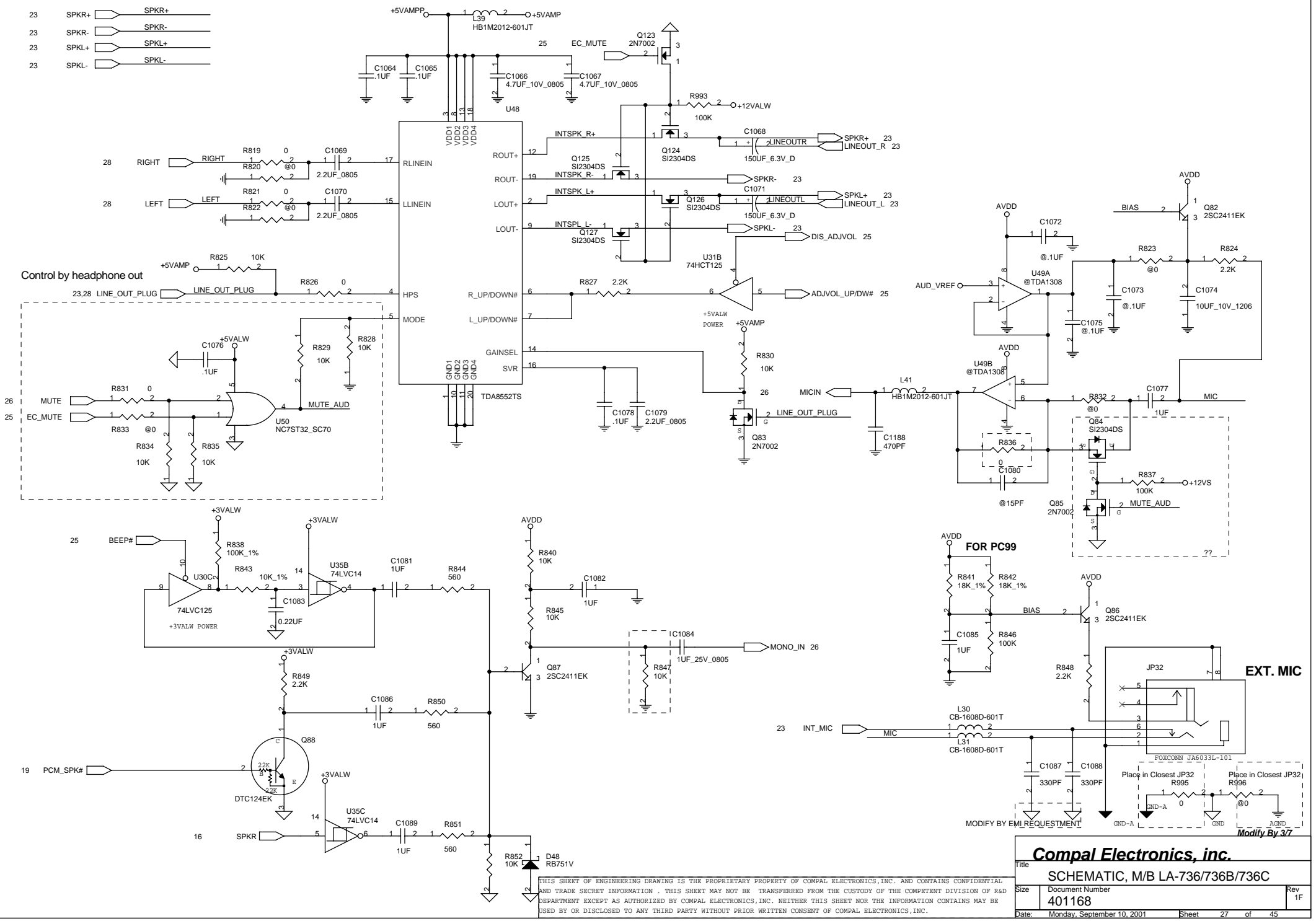
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- 23 SPKR+ SPKR+
- 23 SPKR- SPKR-
- 23 SPKL+ SPKL+
- 23 SPKL- SPKL-

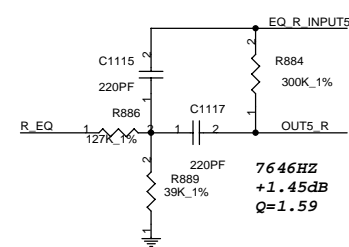
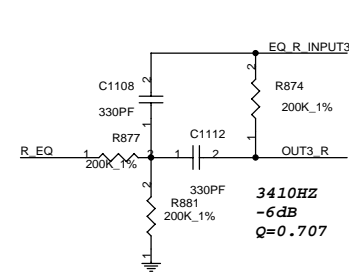
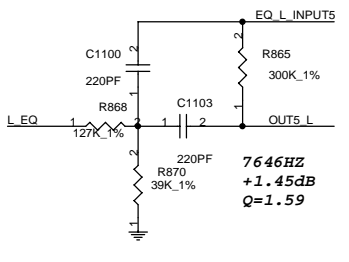
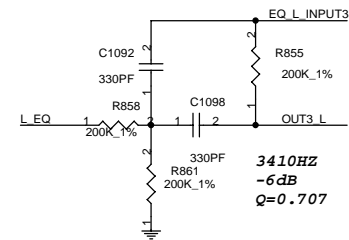
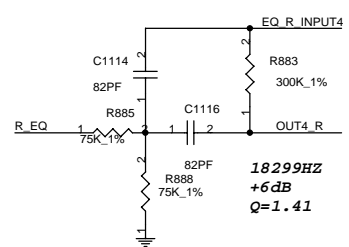
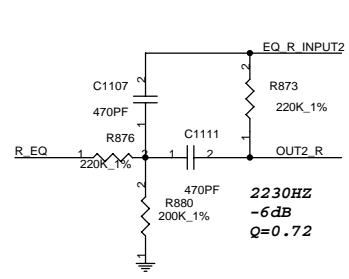
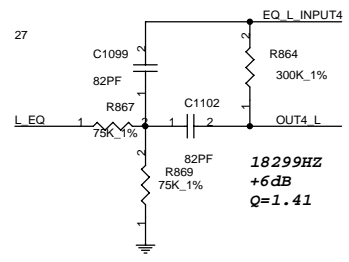
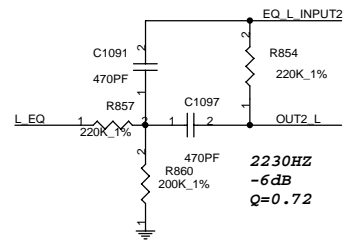
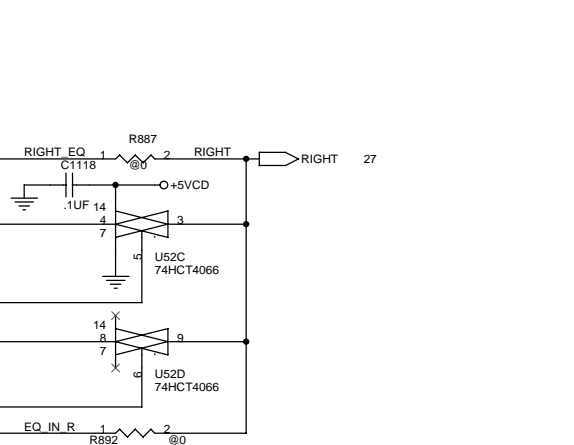
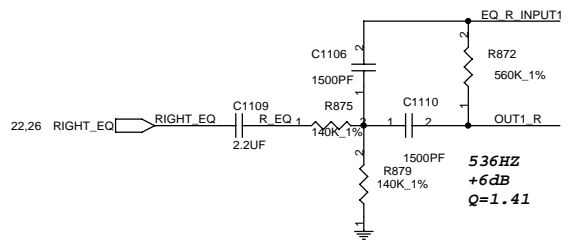
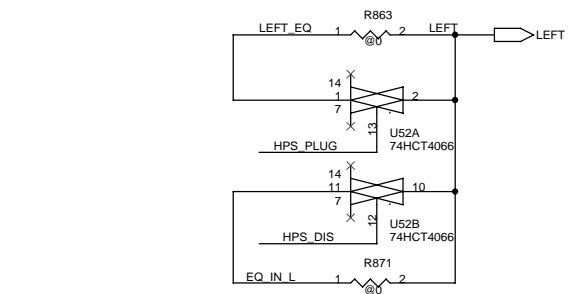
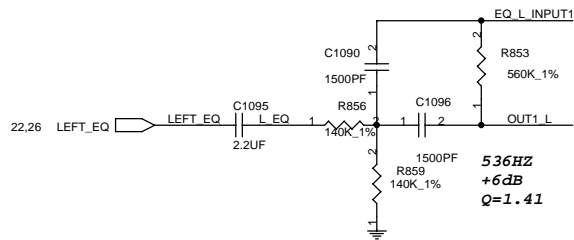
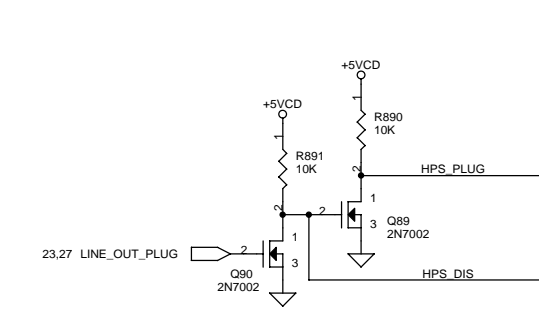
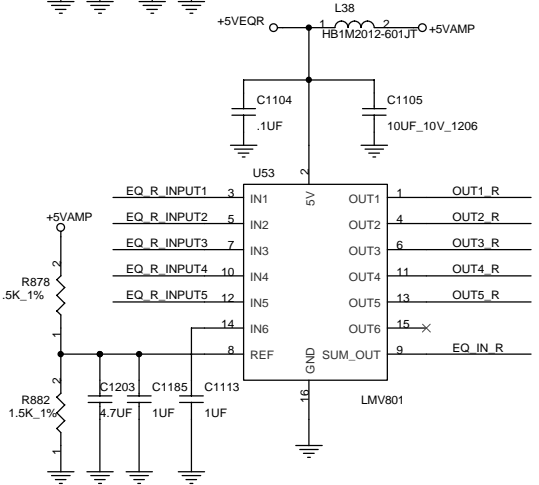
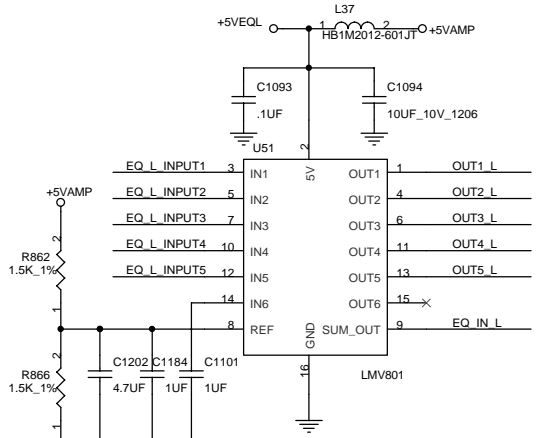


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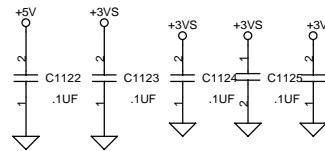
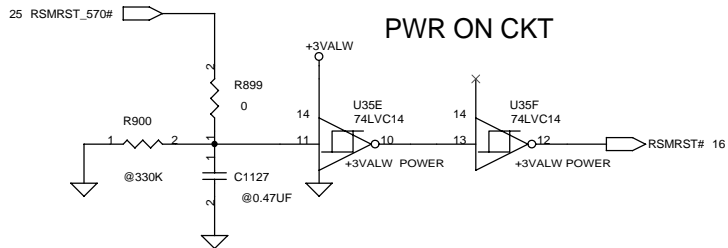
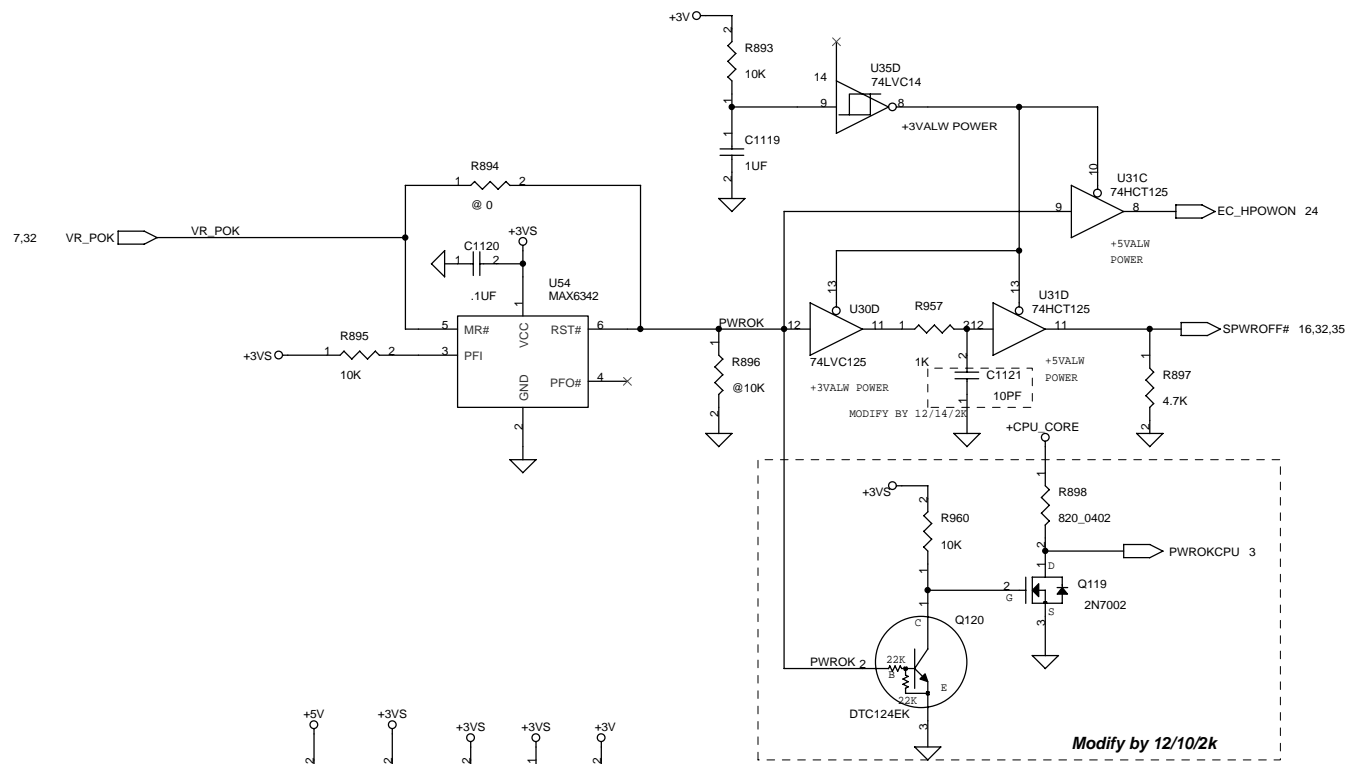
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Modify By 37

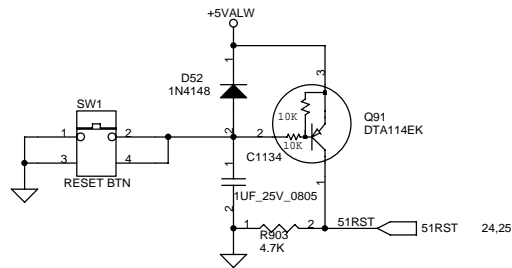


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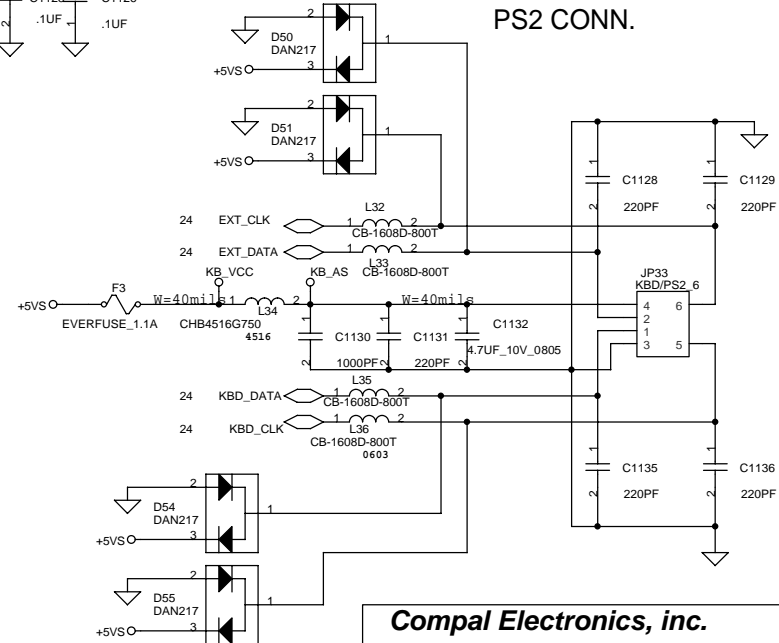
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Reset Button



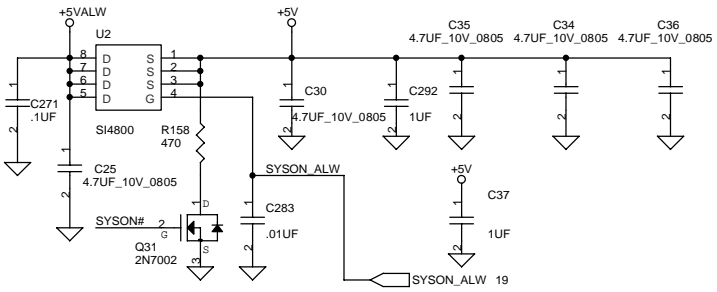
WHEN R=0, Vbe=1.35V
WHEN R=33K, Vbe=0.8V



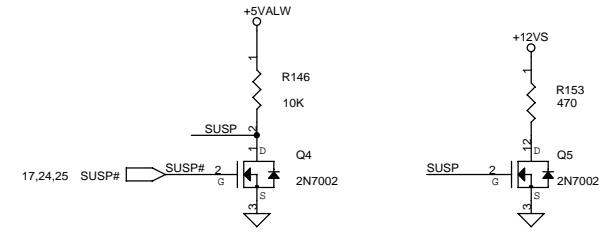
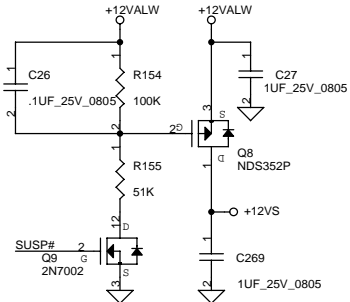
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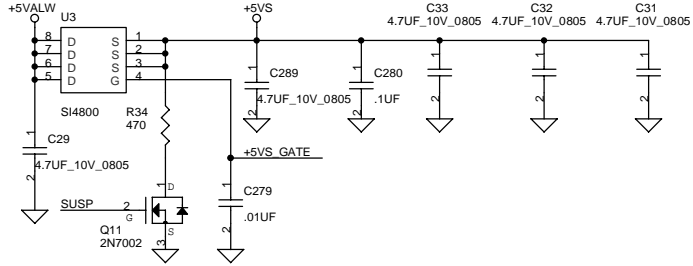
+5VALW Transfer to +5V



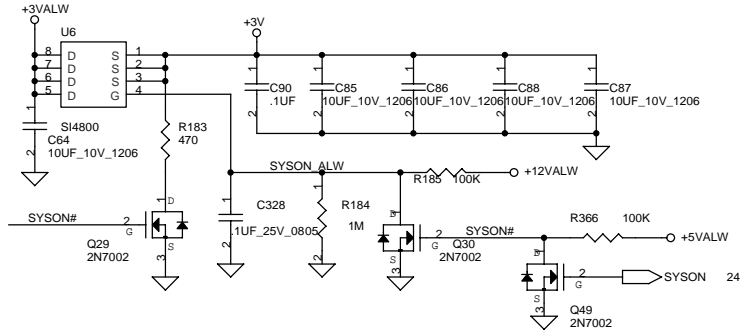
+12VALW TO +12VS Transfer



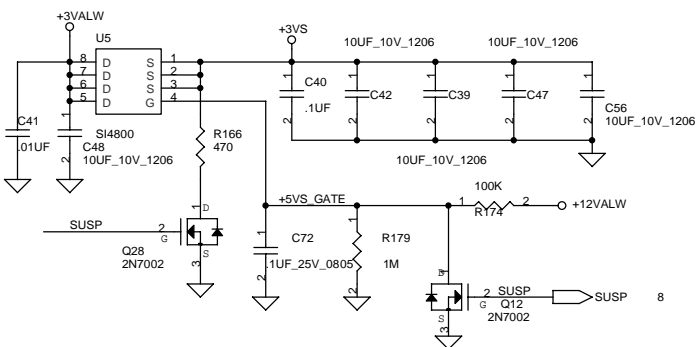
+5VALW Transfer to +5VS



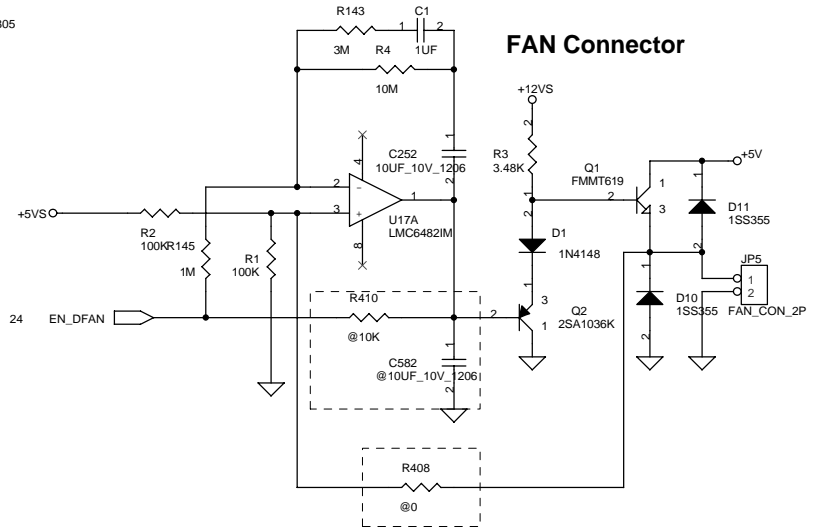
+3VALW Transfer to +3V



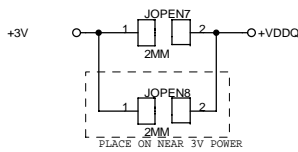
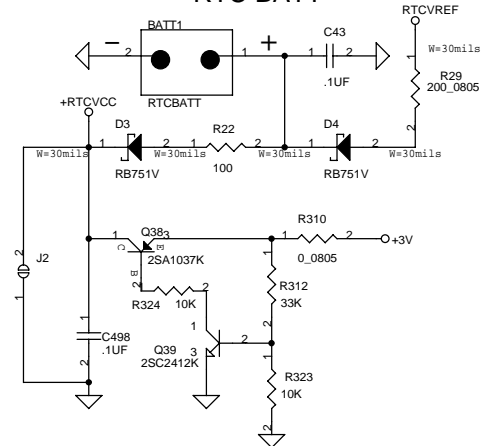
+3VALW Transfer to +3VS



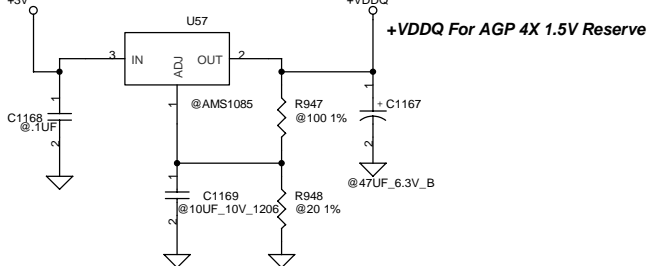
FAN Connector



RTC BATT



SHORT FOR +3V, OPEN FOR 1.5V

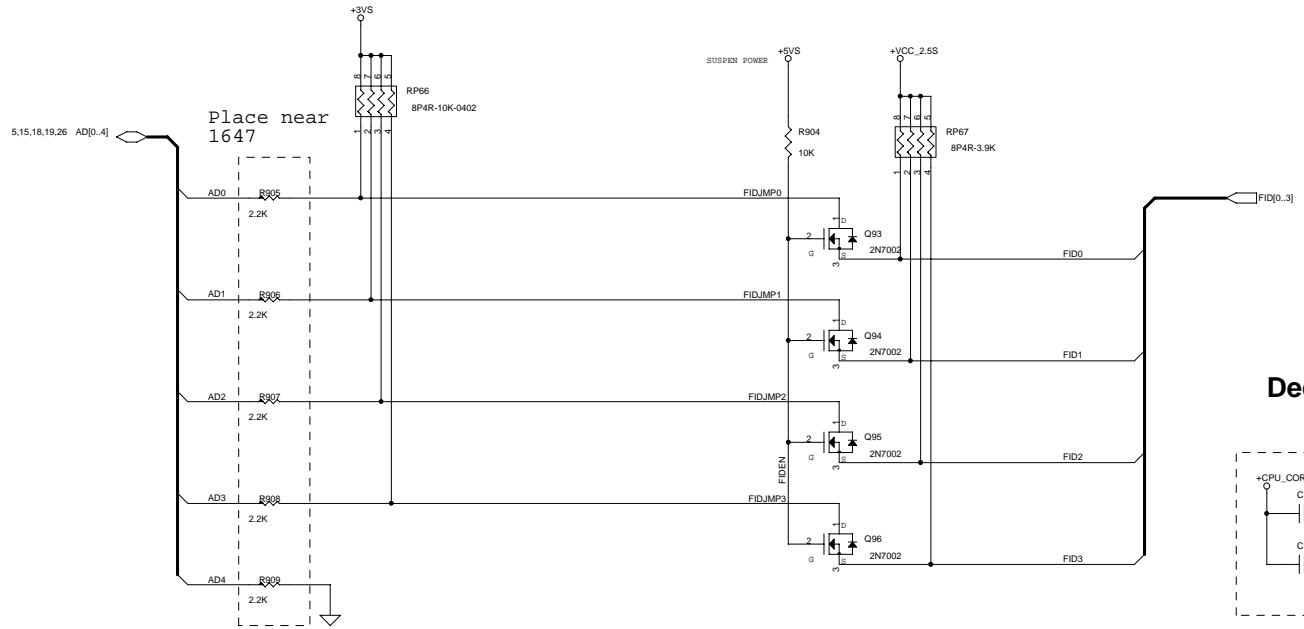


R32,R33 Use The 100 %,20 % for +1.5V

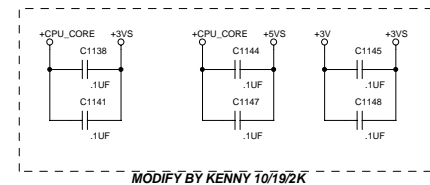
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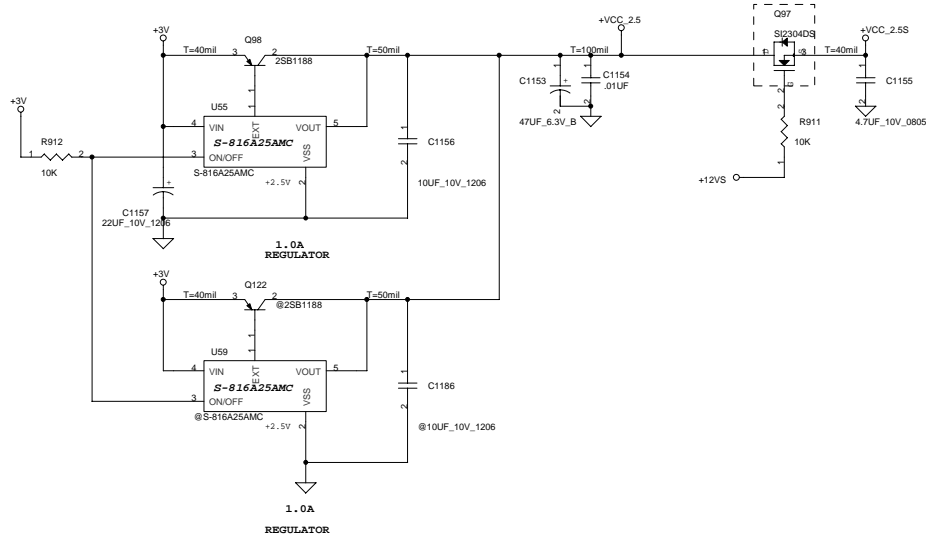
CPU FID ISOLATION



Decoupling Between Planes



ClkDiv[3] FID[3]	ClkDiv[2] FID[2]	ClkDiv[1] FID[1]	ClkDiv[0] FID[0]	Processor Clock and SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	12.5
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5



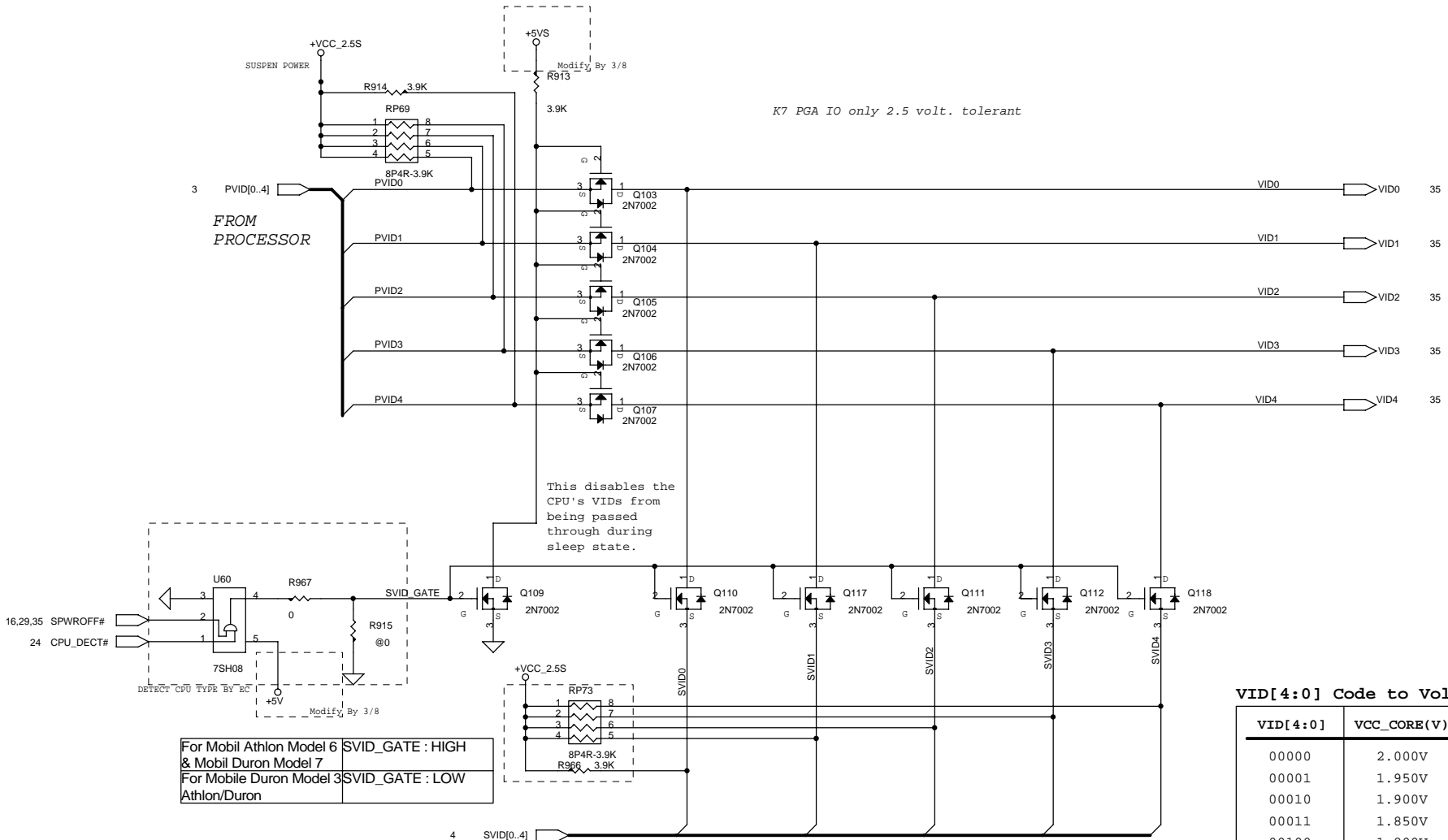
WARNING: PRELIMINARY SCHEMATICS. FOR REFERENCE PURPOSES ONLY. DESIGN HAS NOT BEEN BUILT OR VERIFIED.

NOTE: All resistors are 5% 0603, and all capacitors are 10% 0603 unless otherwise noted.

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K7 PGA IO only 2.5 volt. tolerant

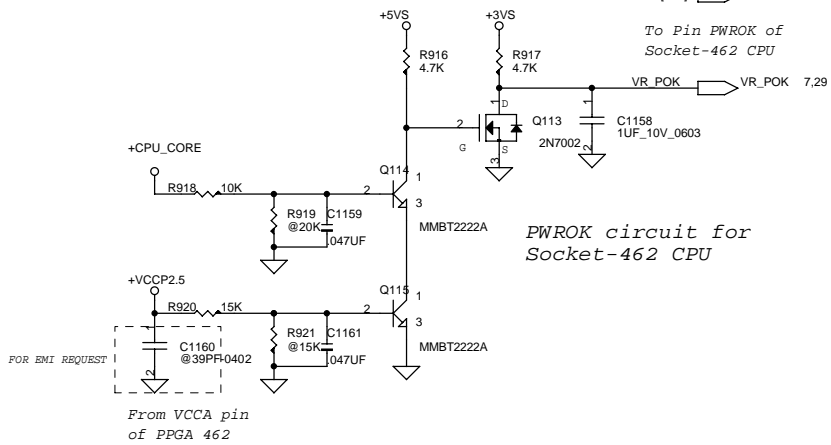


For Mobil Athlon Model 6 & Mobil Duron Model 7
SVID_GATE : HIGH

For Mobile Duron Model 3 Athlon/Duron
SVID_GATE : LOW

VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE(V)	VID[4:0]	VCC_CORE(V)
00000	2.000V	10000	1.275V
00001	1.950V	10001	1.250V
00010	1.900V	10010	1.225V
00011	1.850V	10011	1.200V
00100	1.800V	10100	1.175V
00101	1.750V	10101	1.150V
00110	1.700V	10110	1.125V
00111	1.650V	10111	1.100V
01000	1.600V	11000	1.075V
01001	1.550V	11001	1.050V
01010	1.500V	11010	1.025V
01011	1.450V	11011	1.000V
01100	1.400V	11100	0.975V
01101	1.350V	11101	0.950V
01110	1.300V	11110	0.925V
01111	NO CPU	11111	NO CPU



PWROK IS EQUAL TO CPUPOWEROK, THEN IT WILL BE DELAYED 20ms TO GENERATE PWDGD FOR SYSTEM

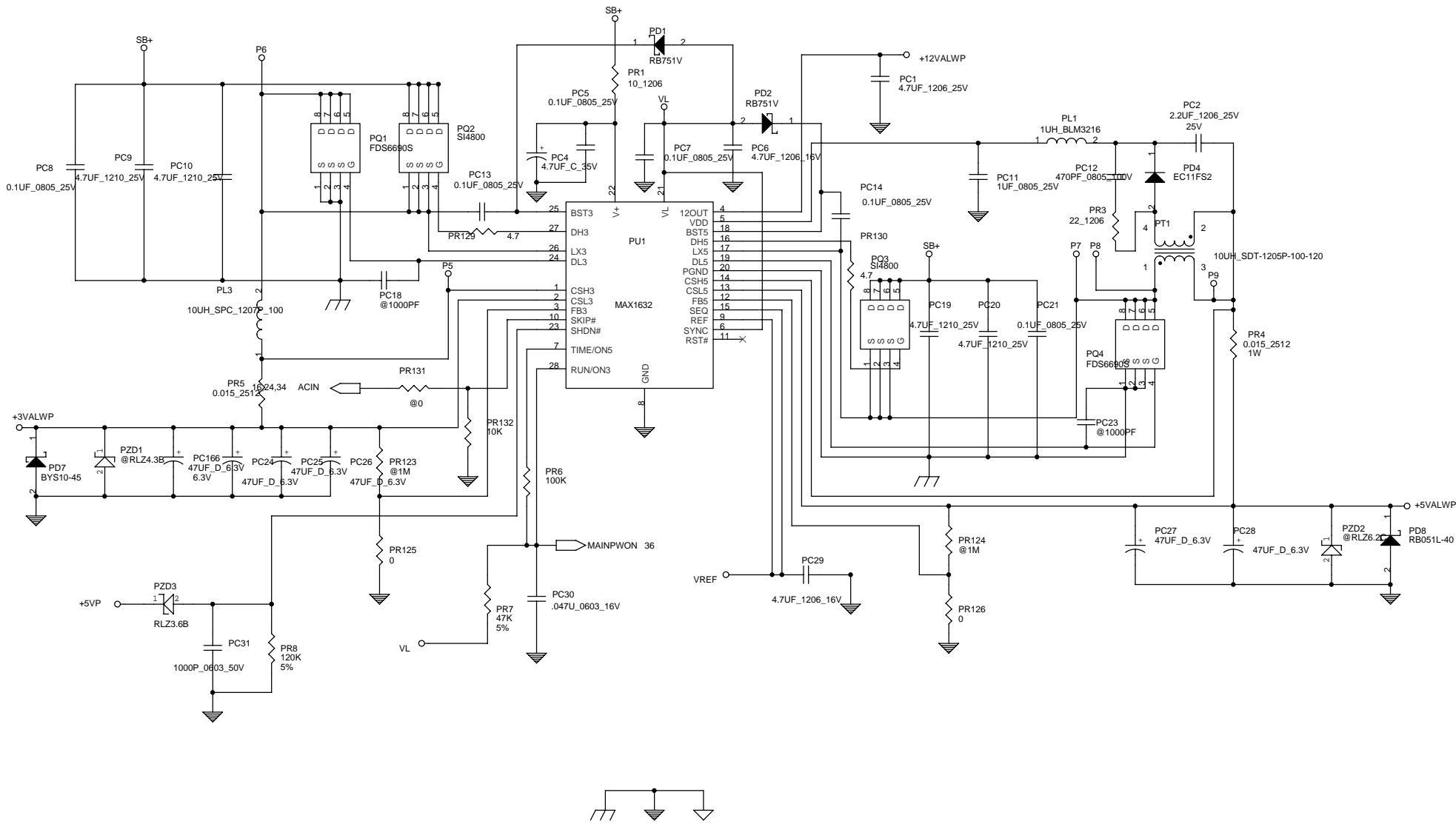
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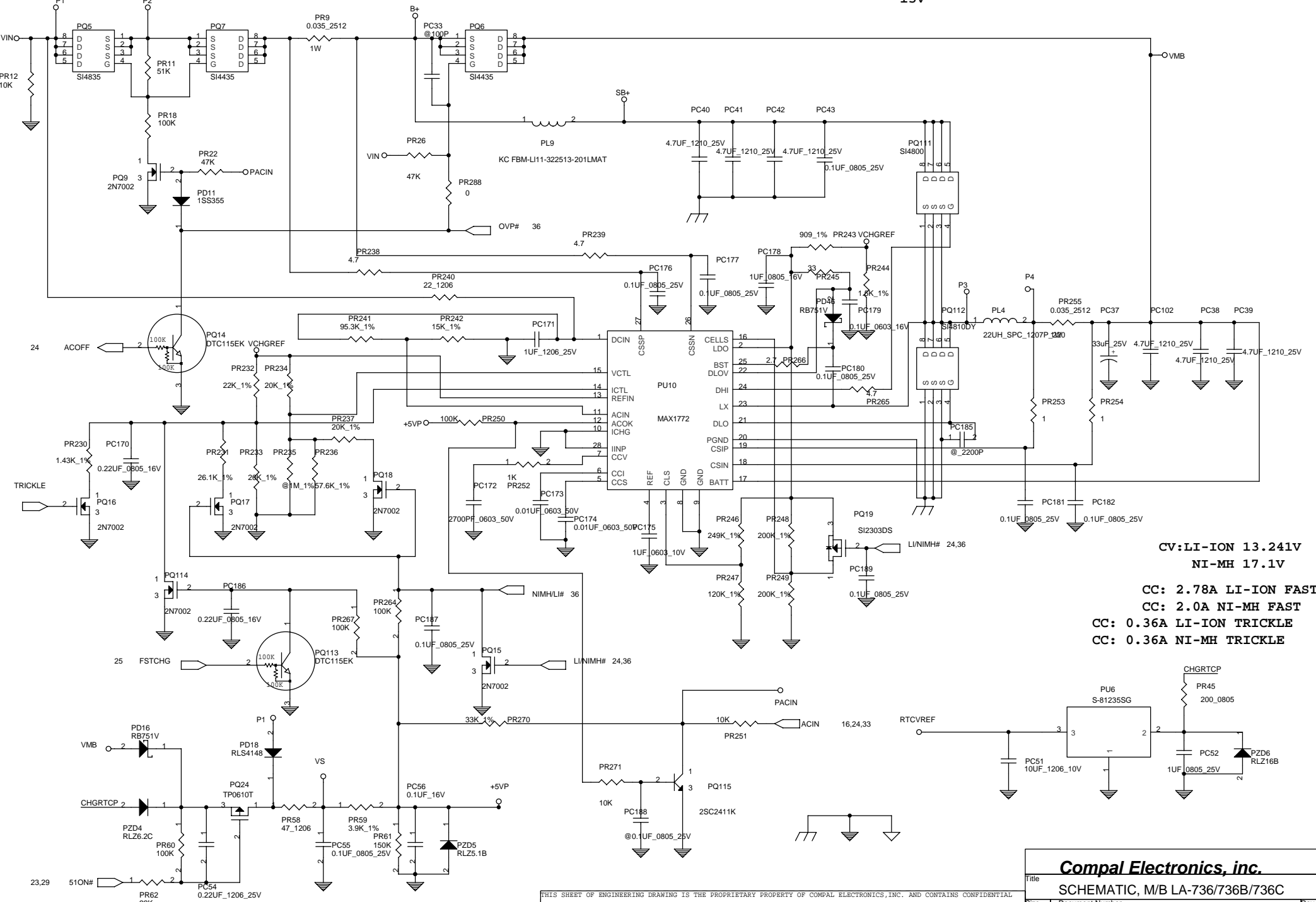
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ADAPTER CURRENT 2.5A

CP: 2.57A

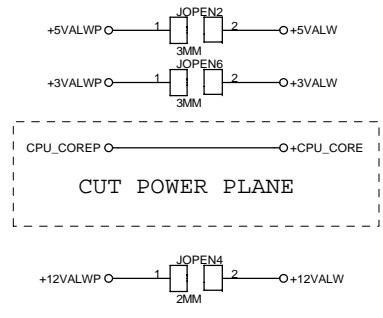
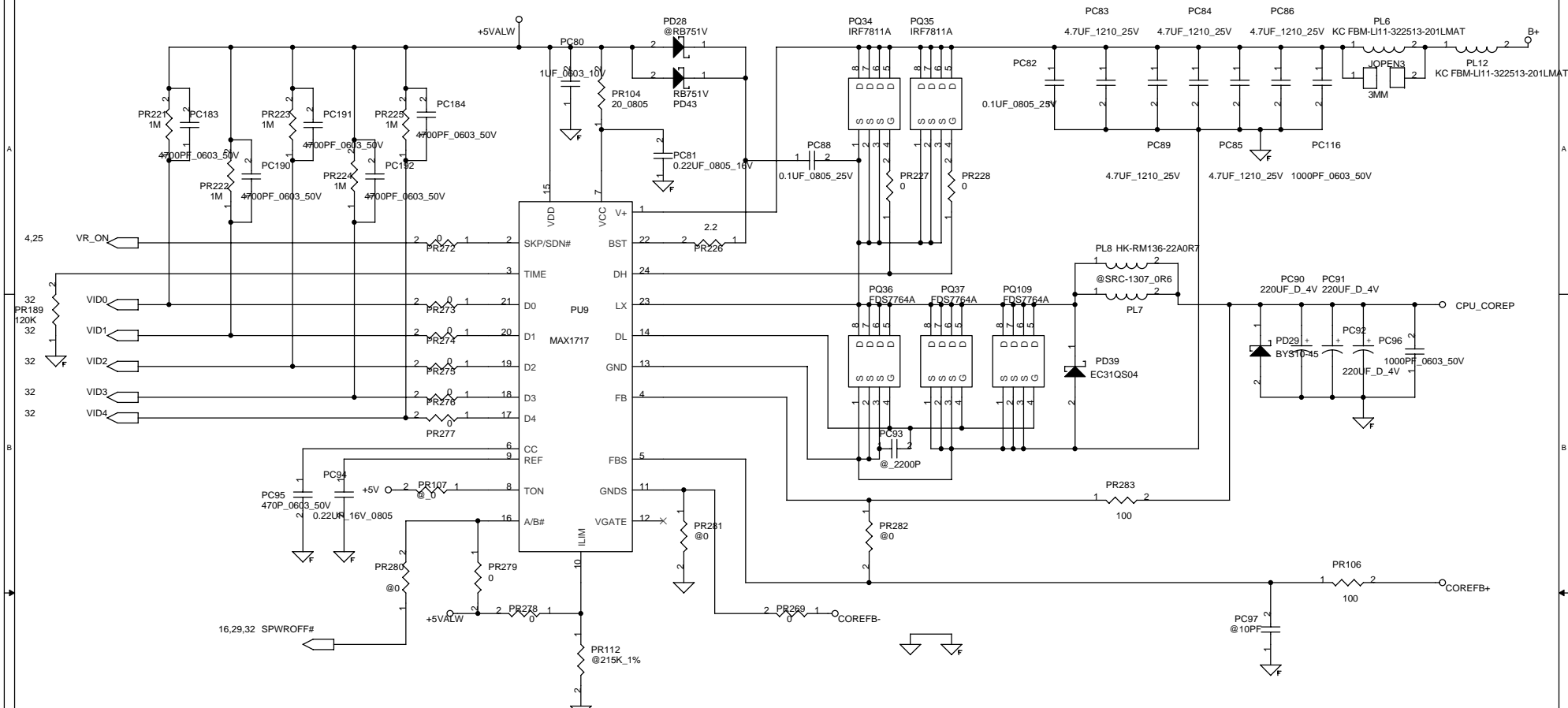
ACIN threshold 15V



CV: LI-ION 13.241V
 NI-MH 17.1V
 CC: 2.78A LI-ION FAST
 CC: 2.0A NI-MH FAST
 CC: 0.36A LI-ION TRICKLE
 CC: 0.36A NI-MH TRICKLE

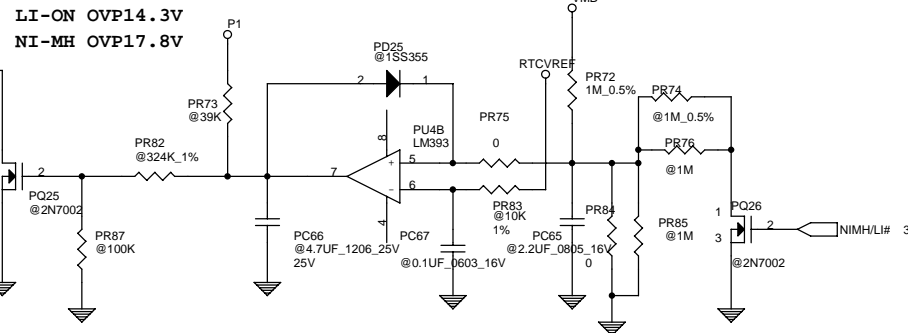
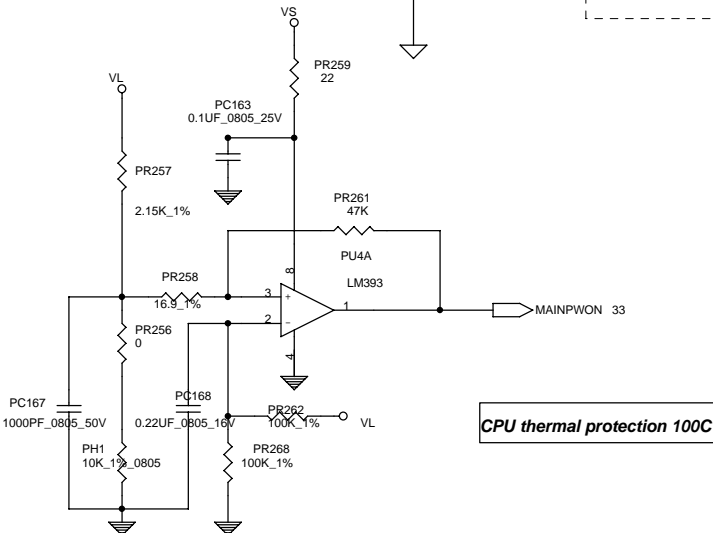
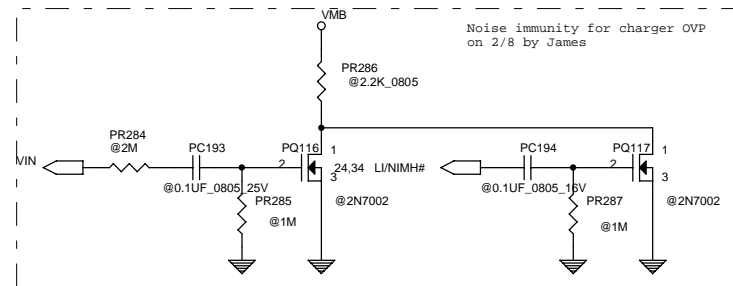
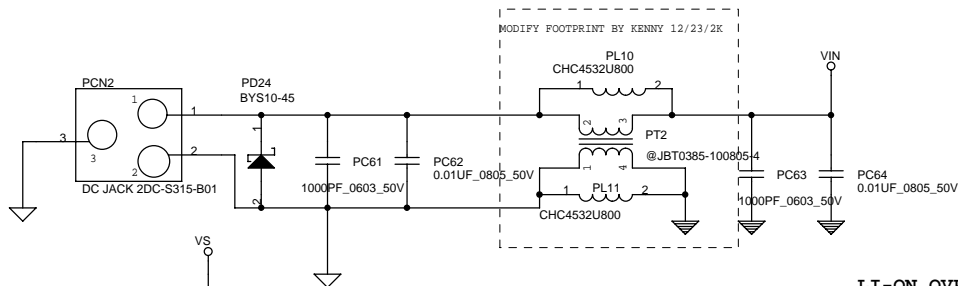
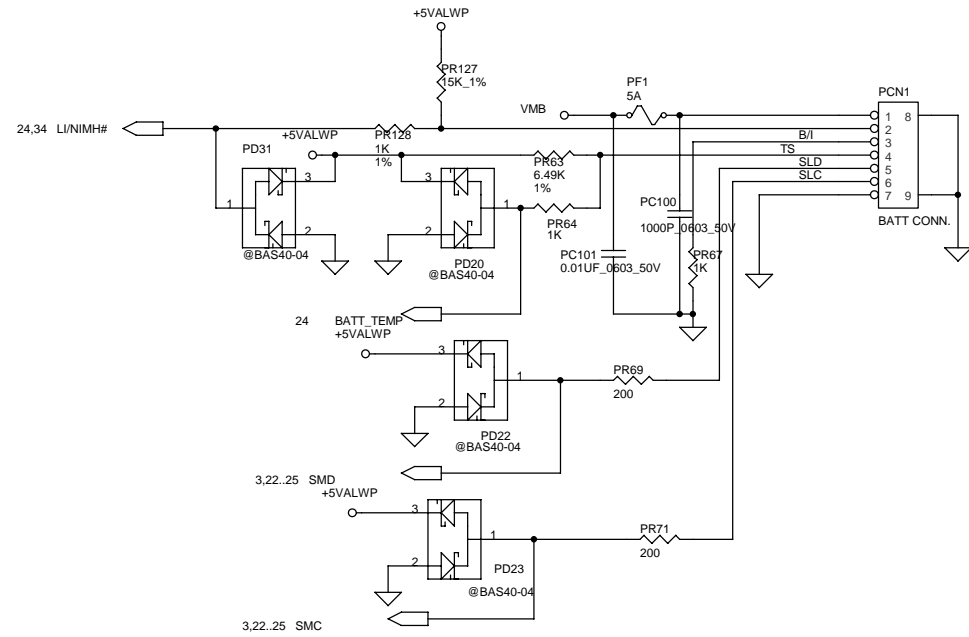
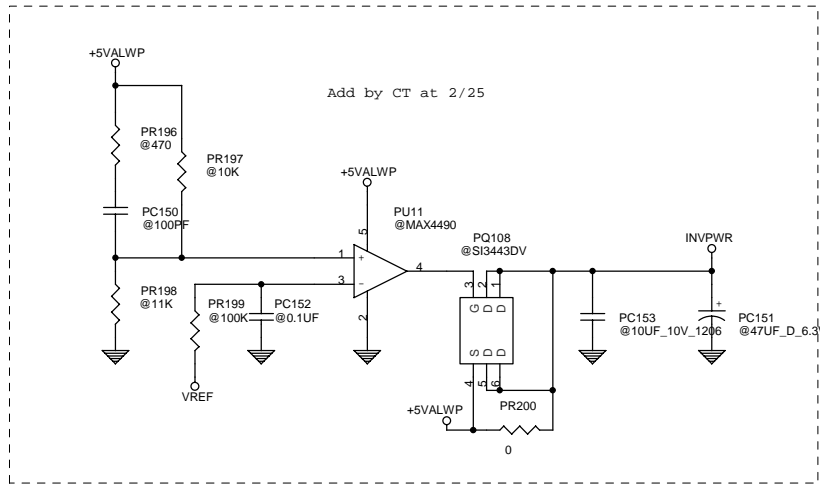
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N32NN061 / LA-736 Rev0.1 HISTORY LIST (PIR)

01. 21/AUG/2000

- *) PAGE 1: Correct R419 from 56 Ohm to 1K
- *) PAGE 3: Correct U20.E6 Pin Name from RATIO# to NC,DEL R480
- *) PAGE 3: Correct U20.Y3 Pin Name from GSERR#/CLKRUN# to GSERR#
- *) PAGE 4: CHANGE R493 FROM OPEN TO STUFF
- *) PAGE 4: Change all pull low strapping resister value from 10K to 2.2K
- *) PAGE 10: ADD TVXpress and CH7004 Configuration table
- *) PAGE 15 :Change U26A location to U17A
- *) PAGE 16: RTSA# Change pull up +5VS to GND,by BIOS Requested ,Set to 370H
- *) PAGE 16:U25.K1 Add Pull up resister to +5VS
- *) PAGE 16: U25.L3 , U25.Y8 , U25.W9 ,U25.P5 Add Pull up resister to +3VS
- *) PAGE 21: Add U31A pin 14 connect to +5VALW and pin 7 connect to GND
- *) PAGE 33~36 :Change all Location to the same LA-732,Power team requested

01. 22/AUG/2000

- *) PAGE 15:Correct RP33,RP34 from 33 to 47 Ohm
 - *) PAGE 21 :Correct RP44,R729,RP45,RP46,RP48,R738 From 33 to 47 Ohm
 - *) PAGE 21 :Correct R728,R737 Value from 22 to 82 Ohm
 - *) PAGE 21 :Correct R741,R744 Value from 33 to 0 Ohm
 - *) PAGE 21 :Correct R739 Value from 4.7K to 5.6K Ohm
 - *) PAGE 21 :Change R724,R734 to OPEN
 - *) PAGE 22:Correct R755 from 4.7K to 5.6K Ohm
- Alii Suggestion

01. 24/AUG/2000

- *)PAGE 4: ADD 3 CAP. C1162,C1163,C1164
- *)PAGE 16:Correct R654.,R668 from 10K to 1K

01. 25/AUG/2000

- *)PAGE 5:Change R502,R503 from OPEN to STUFF,set the S2K BUS read & write forward clock"5/16 T"
- *)PAGE 5:Correct R481,R482,R483,R484,R486,R487,R488,R489 to RP70,RP71
- *)PAGE 5:Change R927 pull up from +3VS TO +3VALW,Because it it resume power group
- *)PAGE 5:Change R491 from +3VS to +3VALW
- *)PAGE 14:Change IRQ1 pull up from +3VS TO +3VALW,Because it it resume power group,So add R929 pull up to +5VALW
- *)PAGE 16:Change R683,R684 from STUFF to OPEN
- *)PAGE 30:Del outport "+5VS_GATE",because don't used!
- *)PAGE 19:Add R930 for VCCP

01. 28/AUG/2000

- *)PAGE 3:Correct R419 Value from 1K to 270 Ohm and Change pull up to +CPU_CORE to GND
- *)PAGE 3:Correct R432 Value from 1K to 680 Ohm and Change pull up to GND to +CPU_CORE
- *)PAGE 3:Correct R429 Value from 0 to 270 Ohm
- *)PAGE 3:Correct R434 Value from 1K to 270 Ohm
- *)PAGE 3:Correct R425 ~ R433,RP1 Value from 560 to 680 Ohm
- *)PAGE 3:Correct R453 Value from 1K to 270 Ohm
- *)PAGE 3:DEL R435,No request
- *)PAGE 3:Correct R585 from STUFF to OPEN
- *)PAGE 3:Correct R586 Value from 0.1UF to 0.047UF
- *)PAGE 3,Add R931 on SMI#,AMD suggest no connect!
- *)PAGE 4 DEL C624 ~ C631,by AMD Suggestion.
- *)PAGE 4 &PAGE 31 : DEL BPFID[0:3] CIRCUIT
- *)PAGE 6:Correct Value R524,R525 from 210 to 180,depend on PCB impedance X 3,ALI recommend
- *)PAGE 6:Add R936 for AGPVREF,NEAR NODE
- *)PAGE 7:ADD R934,R935 Pull Up the U21Pin 1,27
- *)PAGE 8:Change R577,R575,D14,D15 from STUFF to OPEN,R581 from OPEN to STUFF
- *)PAGE 16:ADD R937 for U25.L1 PULL UP TO +5VS
- *)PAGE 16:ADD R938 for U25.P5 PULL UP TO +3VALW
- *)PAGE 17:Correct C894,C898 Value from 0.1UF to 47PF

01. 28/AUG/2000

- *)PAGE 31:Correct RP67 Value from 10K to 680 Ohm,R905 ~ R909 from 10K to 3.3K
- *)PAGE 32:Correct R913,R914,RP69 Value from 10K to 680 Ohm,By AMD Suggest
- *)PAGE 32:Correct VID Table

01. 29/AUG/2000

- *)PAGE 6:Correct C685,C719 from 0.1UF to 22UF_1206
- *)PAGE 7:Add R939, "6 inch" trace "GCLK_1",for AGP Clock tuning by ALI Suggest
- *)PAGE 14,ADD H12,H13 For VGA Broad HOLE!
- *)PAGE 35,ADD PR230 0 Ohm on COREFB-

01. 30/AUG/2000

- *)PAGE 35:DEL PR229,BY Power request
- *)PAGE 3:MOVE R931 TO PAGE 15 (North bridge side)

01. 1/SEP/2000

- *)PAGE 3:Change R414,R417 from STUFF to OPEN,By AMD suggestion
- *)PAGE 3,4:Correct Some Resister and Cap. to 0402 size
- *)PAGE 27:Correct C1083 to 0402 size
- *)PAGE 5:Change R475 from +3VS to +3V
- *)PAGE 3:Change R446 from OPEN to STUFF,BY AMD NEW SPEC.
- *)PAGE 3:Change R446 from OPEN to STUFF,BY AMD NEW SPEC.
- *)PAGE 6:ADD R940,C1166 FOR G_RST

01. 4/SEP/2000

- *)PAGE 4:Change Back THERMDA(S7),THERMDC(U7) By AMD Recommand
- *)PAGE 6,For VDDIO_AGP,ADDPIM_AGP Change Name From +3V to +VDDQ

- *)PAGE 8,JP8 Pin62 ~68 Change Name From +3V to +VDDQ
- *)PAGE 30,Add 1.5V Regulator,JOPEN7 for AGP 4X Reserve.
- *)PAGE 6,Del R922,R923,Because it can't suspend the PCI power,By ALI Recommand
- *)PAGE 5,Add pull low resister R949 ~ R954 For C/BE#0 ~ C/BE#3,ST0,ST1 By ALI Recommand
- *)PAGE 31,Correct R905~R909 Value From 3.3K to 2.2K

01. 5/SEP/2000

- *)PAGE 3,Correct Value R423 from 4.7K to 680 Ohm
- *)PAGE 3,Correct Value RP2 from 10K to 270 Ohm
- *)PAGE 5,Change R475 Pull up from +3V to +VDDQ
- *)PAGE 7,Change PCLK_1535 Connect with PCLK_NB,Before Damping
- *)PAGE 8,Change AGP PULL UP Resister From +3V to +VDDQ
- *)PAGE 15,ADD U58 ON PCIRST# For LEAKAGE
- *)PAGE 16,Correct R925 ~ R928 & R937,R938 Pull Down to GND
- *)PAGE 19,ADD OUTPORT ON CBRST#
- *)PAGE 20,CHANGE U29 RESET# FROM DEV_RST# TO CBRST#
- *)PAGE 32,ADD Q117,Q118 For Meet AMD NEW SPEC.

01. 6/SEP/2000

- *)PAGE 5,DELR498,R504,Because Repeat By R511,R909
- *)PAGE 29,ADD R957 For Time Tuning
- *)PAGE 8,Correct R599 Note(Stuff For TVXPRESS)
- *)PAGE 6,8 : Correct Net Name From AGPVREF To VREF_GC
- *)PAGE 10, ADD R958 ON U22 PIN 30 FOR CH7004 RESERVE

01. 7/SEP/2000

- *)PAGE 31,Correct RP67 From 0804 to 8P4R Size
- *)PAGE 3,Correct RP2 From 0804 to 8P4R Size
- *)PAGE 14,ADD H14~H18,EP13~EP17 FOR LAYOUT RESERVE

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N32NN061 / LA-736 Rev0.1 HISTORY LIST (PIR)

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01. 7/SEP/2000
*)PAGE 5,Correct Footprint R468,R469 From 0805 to 0603
*)PAGE 8,Correct R577 From OPEN to STUFF
*)PAGE 15,Change R955 and U58 From +3VS to +3V,By ALI Recommend
*)PAGE 31,Correct Value C1137 ~ C1152 From C0603 To C0402
*)PAGE 32,Correct R905~R909 Footprint From 0603 to 0402
02. 13/SEP/2000
*)PAGE 7,Correct L1 From CHB2012U170_0805 To CHB010012800_1206
*)PAGE 29,Correct R957 Value From 22 Ohm to 1K
*)PAGE 32,Change U56 PIN 2 From PWROKCPU to SPWROFF#
02. 14/SEP/2000
*)PAGE 33,34,35,36,Change From Power team Schematic by K9-DC-0914-1.DSN
*)PAGE 35,Add PR230 On COREFB-
*)PAGE 7,Del C763~C777
02. 15/SEP/2000
*)PAGE 4,Correct C589~C608,C619~C623 From C0402 To C0603,Because the material shortage
*)PAGE 14,Modify the EMI PAD Footprint to "EPIPAD_PS-4
02. 18/SEP/2000
*)PAGE 14,DEL RP27.6 Signal(PAR),Because M1535 Internal Pull Low
*)PAGE 16,Change R663 from 0 Ohm to 10K Pull Up +3VALW,By Bios Request
02. 21/SEP/2000
*)PAGE 18,Chaneg Q63 from 2N7002 to SI2306DS
02. 22/SEP/2000
*)PAGE 27,Change C1083 from C0402 to C0603
*)PAGE 7,MOVE R939 To PAGE 8 ,It Need Closest The JP9
*)PAGE 35,ADD RQ115,RP270,RP271 for ACIN
02. 26/SEP/2000
*)PAGE 33~36,Modify the Power Schematic By K7-DC-0925.DSN
It Modify Some Value
N32NN061 / LA-736 Rev0.2 HISTORY LIST (PIR)
FOR A-TEST
8/OCT/2000
*)PAGE 31,Change RP66 from 8P4R_0804 size to 8P4R
*)PAGE 29,Change C1121 from 0.1UF to 10PF,By Power Good Timing
*)PAGE 3,Change Q50 from 2CS2412K to 2N7002
*)PAGE 5,ADD R499,R506,R510,R496 & DEL R494,R500,R503 By ALI Strapping
12/OCT/2000
PAGE 24,Modify HPID 01 for LA-736
PAGE 7,ADD C1170 ~ C1175 0.01UF For Clock GN
PAGE 14,DEL EP2
PAGE 19,Mount R941 and DEL R940,C1166
13/OCT/2000
PAGE 8,DEL R939
17/OCT/2000
PAGE 3,Change value R460,R461 from 4.7K to 1K(SMB pull up)
PAGE 28,ADD L37,L38 & C1184,C1185(0.1UF For EQ REF Votage) to Solve the EQ Noise!
PAGE 14,ADD R965,Q121 For Fix Noise Sound When Plug-in headphone
PAGE 26,DEL L27,L28,L29 Fix T/P Noise
19/OCT/2000
PAGE 27,ADD L39 For U48(+5VAMP)
PAGE 31,DEL C1137,C1140,C1139,C1142,C1143,C1146,C1149,C1151,C1150,C1152
26/OCT/2000
*)PAGE 3,ADD R968,Change Q50 from 2N7002 to MMBT2222A
*)PAGE 32,DEL U56,R915,R919,R921 ADD Q111,Q112,Q117,RP73,R966,R967 For Power Now
27/OCT/2000

Fix Battery Only Boot Fail:
*)PAGE 29,Change R899 From 47K to 0 Ohm,Change C1127 from 0.47UF To OPEN
Fix Boot Beep Loudly :
*)PAGE 27,ADD R970(1K),Change R847 from 10K To 1K
1/DEC/2000
Power update schematic for B-TEST!
Fix suspen resume problem!
*)PAGE 15,Change U58 power source from +3VS TO +3V,
Fix VCC 2.5V drop,Change REGULATOR By AMS1085
*)PAGE 17,ADD R972 on LPTSTB#
3/DEC/2000
Change GPIO For VOLUME CONTROL and ENDIM0,1 (Because original group need enable UART3)
*)PAGE 16,unmount R655,R656,R657,and reserve R975,R976 for ENDIM0,1
*)PAGE 16,mount R641,R642,R643 and ADD R973,R974 for ENDIM0,1
TUNNING PCI CLK
*)PAGE 15,UNMOUNT R629,C880

7/DEC/2000
For meet ALI IDE interface design notice
1)PAGE 14 : Change RP32 value from 10K to 4.7K
Change IRQ14,15 pull down instead pull high to +5VS
*)PAGE 21 : ADD R977 For SDDREQ pull down 5.6K to GND
ADD R978 for SBDIORDY pull high 10K to +5VS
Change R740 value From 1K to 10K
Change R728 value From 33 to 82 Ohm(SBDREQ)
Change R743,R730 value From 22 to 82 Ohm(IRQ 14,15)

Add One +3V Jump For +VDDQ
*)PAGE 30,Add JOPEN8 For +VDDQ
14/DEC/2000
RESERVE RESISTER (+3VS) FOR M1535+
*)PAGE 15,Add R979,R980 For +3VS,+5VS Option
*)PAGE 21,Add R981,R982 FOR IDERDY Pull Up to +3VS
FIX System Unstable Tunning :
*)PAGE 3,Change R456,R457 Value from 40.2 Ohm 1% to 35 Ohm 1%
*)PAGE 6,Change R524 Value from 180 Ohm1% to 150 Ohm 1%
*)PAGE 6,Change R525 Value from 180 Ohm 1% to 120 Ohm 1%
*)PAGE 27,Correct R970 Value from 1K Ohm to 0 Ohm
15/DEC/2000
*)Power Modify Schematic!
Modify Some Value:
*)PAGE 3,R417 Mount 0 Ohm,Becaus need connect to gnd
CORRECT C586 From 0.1UF To 0.47UF
*)PAGE 5,Change RP3,RP4,RP5,RP7 Value From 8P4R-2.7K TO 8P4R-8.2K
*)PAGE 6,Correct R515,R517 Value From 4.7 Ohm to CB-1608D-800TT(0603)
Correct R516,R518,R519,R520,R521 Value From 4.7 Ohm to CB-2012D-800TT(0805)
For PC-133 Stable:
*)PAGE 11,Correct RP18,RP19,RP22,RP23 Value From 8P4R-10 to 8P4R-22
*)PAGE 12,Correct R607,R608,R609,R610 from 10 Ohm to 33 Ohm

*)PAGE 14,DEL R614,C851
*)PAGE 28,Correct C1184,C1185 Value From 0.1UF to 1UF
*)PAGE 32,Correct RP73 Value From 8P4R-680 to 8P4R-2.7K
Correct R966 Value From 680 to 2.7K

*)PAGE 20,ADD R986

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11/16/NEV

*)PAGE 26,Correct Some Value :

R804 From 22 to 47 Ohm,C1031 Mount 22 PF

L27,L28,L29 Need Mount

*)PAGE 32,Correct R913,R914,RP69 Value from 680 to 2.7K Ohm

*)PAGE 31,Correct RP67 Value From 680 Ohm to 2.7K Ohm,ADD One Regulator Circuit for +VCC_2.5

11/17/NEV

*)PAGE 6,Change R516,R518,R519,R520,R521 Value from 4.7_0805 to CHB2012B800_0805

*)PAGE 6,Change R515,R517 Value from 4.7 Ohm to CHB1608U800

11/22/NEV

FOR AGP 4X Function Reserve:

*)PAGE 6,Change R524 Pull Up From +3V To +VDDQ

*)PAGE 6,Change R936 Connect From VREF_GC to VREF.CG,UNMOUNT 936

*)PAGE 8,Change R578 Connect From VREF.CG To VREF_GC

11/24/NEV

FOR FIX SUSPEND / RESUME FAIL:

*)PAGE 24,Correct R775 Pull Up from +3V to +3VS

*)PAGE 24,Correct R776 Pull Up from +3VS to +3V

*)PAGE 24,DEL R778,R779,D42 Then Connect PCMRST# From U36.106 to U30.1

11/24/NEV

MODIFY POWER RB751V FOOTPRINT FROM RB751V TO CH71B

11/27/NEV

*)PAGE 23,ADD Q75 FOR FDD LED

B-TEST FOR VER0.3

For Fix Boot Need Twice,Change CPURST# From Northbridge to Sorthbridge::

*)Page 5,ADD R984,Page 15,ADD R992 For CPURST#

For SUSPEN Stable By ALI Requestment

*)Page 5,ADD Straping R985~R991

FOR DETECT CPU TYPE BY EC:

*)PAGE 24,35 ADD CPU_DETECT# From U36 pin 94,AND with SPWROFF# for SVID_GATE

FOR FIX BC018:

*)Modify the PCN2 footprint from DJ-305S to DJ-305S-NEW,it will include hole change size!

*)Modify Footprint For New Lib

FOR FIX MONO_IN NOISE::

*)PAGE 27:Correct R852 value from 33K to 10K

*)PAGE 27:DEL R839,Correct R847 from 4.7K to 10K

FOR Mic NOISE:

*)PAGE 27:Correct R836 Value From 0 to 6.8K

For EMI requestment Correct value:

*)PAGE 23:Correct CP8,CP9,C10,C11 Value From 33pf to 220 pf

*)PAGE 22,Add L40 For EMI request

For TV Out Resest Stable:

*)PAGE 10:ADD R604

FOR Layout Requestment:

*)Page 31,Q98,Q122 Change Footprint to 2SB1188

*)Page 7,PCLK_1535 Trace Modify From 9533 to 2977

*)Page 36,Change PCN2 Footprint From DJ-305S To DJ-305S-NEW

*)Page 14,Change EP13,EP14,EP15,EP16 Footprint From EMIPAD_PS-4 To EMIPAD_PS-3

*)Page 14,Del H15,H16,H17,H18

*)Page 3,Del TP5,TP6,TP7,TP8

For Fix +5VALW Drop:

*)Page 22,U34 Pin 4 ADD C1187 On "EN_5VCD"

Some Requestment:

*)PAGE 3,Correct 680 Ohm 820 Ohm (R432,R429,R419,R434,RP1)

*)PAGE 7:Change D12,1 From SUSAN# to CPU_STP#

Change R542 From 33 Ohm To 22 Ohm

DEL C1177 ~ C1183 By EMI Requestment

*)PAGE 9,Change JP10 PIN 1,6,8 From CRTGND to GND By EMI Requestment

(Change L6 Position)

*)PAGE 10:Umount C810 (27PF),mount C809 (47PF) For TV_OUT Quality And Meent EMI Requestment

*)PAGE 26,Correct C1039 From 1UF To 2.2UF,DEL L27,L28

*)PAGE 27:ADD Q123,Q124,Q125,Q126,Q127 For POWER ON PO-PO Sound

*)PAGE 29,C1119 Mount 1UF For EC_HPOWON Stable

FEB/14/2001

FOR MIC QUALITY:

ADD L41 : HB1M2012-601JT,C1188 : 470PF

Change SVID to FIX VID

*)PAGE 32,Change R967 to R915 (0_0603)

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N32NN061 / LA-736 Rev0.4 HISTORY LIST (PIR) FOR C3-TEST

1/20/JAN
 *)PAGE 3,Change C621 from 0.22UF(0603) to 2.2UF (0805) For Assembly.(Thermal Pad)
 Modify For Power Now Function:
 *)PAGE 24,Change R775 Pull Up From +3VS to +3V
 *)PAGE 24,Change R775 PIN1 & D39 PIN 2 From ATFIN# to CPU_DECT#
 FOR FIX AUDIO MONO_IN NOISE:
 *)PAGE 27,DEL R839

2/12/FEB
 FOR FIX STR ISSUE
 *)PAGE 5,UNMOUNT R493[AD12],THEN MOUNT R1003 USE OFFSET MODE
 RESERVE R998 - R1008 PULL UP TO +3VS,CPU READ/WRITE USE 8 STAGE
 FOR FIX S1 HALT ISSUE:
 *)PAGE 7,UNMOUNT D12 AND Change D12 PIN1 From CPU_STP# To SUSB#
 FOR FIX BLUE SCREEN CC005:
 *)PAGE 3,ADD C1189(560PF_0402) ON NMI(NEED NEAR AN3)
 For FIX TV_OUT Leagage
 *)PAGE 10:ADD R1010 FOR DVDD And Change From +3VS To +3V
 ADD R1012 FOR D10 ~ D15 FOR REV Change Pull +3VS To +3V
 ADD R1009 FOR DACVDD,CLKVDD Change From +3VS To +3V AND Reserve +5VS
 FOR FIX Play CD Audio Volume Too Small:
 *)PAGE 22,Change R749,R753 Value From 24K TO 33K
 RESERVE SOME PCI Signal On MINI-PCI:
 *)PAGE 18:ADD R1014 ~ R1021 FOR OPTION IN FEATURE
 FOR POWER NOW FUNCTION:
 *)PAGE 32,MOUNT R967,UNMOUNT R915 (MODIFY BOM)
 FOR EMI REQUESTMENT:
 *)PAGE 23,ADD C1190 ~ C1192
 *)PAGE 19:ADD PIN 7,8 ON JP24 AND CONNECT TO GND-A,C1087,C1088 CHANGE CONNECT FROM GNDA TO GND
 FOR MIC TUNNING:
 *)PAGE 23,ADD R1022,AND RESERVE R1023
 FOR LAYOUT MODIFY:
 *)Change FOOTPRINT 10P8R,16P8R,0402 TO 10P-8R-NEW,16P-8R-NEW,0402-U
 *)PAGE 36,Change PCN2 Footprint From DJ-305S-new to DJ-305S
 *)PAGE 29,Change R898 Footprint From R0603 to R0402
 *)MODIFY JP32,GND-A AND AGND

2/21/FEB
UPDATE FROM 736 A(2.0) VER 0.4(C3-TEST) TO 736B (A2.1) VER0.6
 FOR LCL TUNNING:
 *)PAGE 7: ADD LCL FILTER:
 ADD L42,L43,L45,L46,L47,L51 & C1193 ~ C1197 ON DICLK#0~3,AICLK#
 FOR EMI REQUESTMENT:
 ADD C1198 - C1201 ON JP17 PIN15 ~ 18

2/27/FEB
 *)PAGE 7,Change D12.1 FROM SUSB# TO CPU_STP#,AND MOUNT D12

3/1/MARCH
 *)PAGE 5,ADD R1024,TP5,TP6 ON SUS_STAT# FOR RESERVE
 *)PAGE 23,MODIFY MIC GND,R1022 CONNECT TO AGND,R1023 CONNECT TO GND

3/7/MARCH
 FIX EARPHONE NOISE:
 *)PAGE 26:DEL L29, PAGE 27:DEL R996;PAGE 23:DEL R997

3/14/MARCH
 *)Power Team Modify Circuit By Send New Schematic(Jone)

3/16/MARCH
 *)PAGE 3,DEL R436,R437,R438(330) By AMD Suggestion!

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4/10/APRIL

*)PAGE 5, Tunning S2K BUS Time:(Clock In Side) Use AD[31..24] "FC"

DEL R1004,R1005(10K_0402),ADD R496,R502(2.2_0402)

*)PAGE 5,Change RP3,RP4,RP5,RP6,RP7 From 8P4R-8.2K To 8P4R-2.7K

*)PAGE 6,Change R515,R517 From CHB1608U800 To 4.7 Ohm (By EMI Requestment)

*)PAGE 6,Change R516,R519,R520,R521 From CHB2012U800_0805 To 4.7_0805 Ohm (By EMI Requestment)

*)PAGE 10,Change TV_OUT Power Source From +3V to +3Vs

DEL R1009,R1010(0 Ohm),R1012 (22K),AND R592,R1011(0 Ohm),R600(22 K)

*)PAGE 28,For FIX Audio Quality:

Change R862,R866,R878,R882 From 22K to 1.5K_1%

4/16/APRIL

*)PAGE 5, Tunning S2K BUS Time:(Clock In Side & Clock Out Side) Use AD[31..24] : "75" (By ALI Suggestion)

DEL R1008,R991,R496(10K_0402),then ADD R1025,R497,R1004 (By ALI Suggestion)

For Fix S4 Resume issue:

*)PAGE 26,DEL C1031(22 PF),Change R804 From 47 Ohm to 22 Ohm

4/20/APRIL

For Enable Save Power Consumption Function,Ali Suggest Need Pull Low "THERMJ":

*)PAGE 16,ADD R1027(4.7K)

For FIX MIC Phone Record Noise Issue:

*)PAGE 27,Change C1077 From 0 Ohm to 1UF,R836 From 1K to 0 Ohm

For Fix Wireless Noise Issue:

*)PAGE 23,Mount R997 0 Ohm

5/4/MAY

Update Power P.I.R

5/16/MAY

Update Power Circuit By Jones send(5/15)

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5/28/MAY

*)PAGE 16:ADD R1027(4.7K) For Enable Clock Trolter (Save Power Consumption.)

Layout:

Modify +5VALW,+3VALW Trace,Add Trace By Cut Power Plan.

Power Team Modify PCN2 Footprint

ME Team Modify OUTLET Drawing!

5/31/MAY

*)PAGE 5,Set Strapping Pin "7C"

Clock Tunning:

*)PAGE 7:Change R539,R540 From 33 to 22 Ohm.

*)PAGE 5:Change R472 From 0 to 33 Ohm.

For PC-133 Tunning:

*)PAGE 11,Change RP18 ~ RP23 From 22 to 10 Ohm

For Save Power Consumption While S3:

*)PAGE 6,Change R522 From 270_1% to 1.5K_1%; R523 From 180_1% to 1K_1%.

For PCMCIA Power Solution More Stable:

*)PAGE 20: Change C938 ~ C944 From 0.1UF to 1UF

For Change Sourth Bridge From M1535 to M1535+:

*)PAGE 15:DEL R980,Mount R979 (For IDE Power Solution)

*)PAGE 21:DEL R978,R740,Mount R981,R982 (FOR IDE IORDY)

8/28/2001 Modify BOM before MP

EMI Solution

*)PAGE 35: PR226 change from 0 to 2.2 ohm

*)PAGE 17: L17,L18,L21,L22 from 800 to 300 ohm

KDS crystal issue

*)PAGE 26: R808 change from 0 to 390 ohm

C1033 change from 33 PF to 12

Improve POP sound when CD player power on

*)PAGE 27: R833 delete

Improve pcmcia modem sound

*)PAGE 27: R849 change from 10K to 2.2K

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
P1		DCIN quiescent current too large while battery existed	0.1	34	Connect PR241 to PU10	0.2	EVT1
P2		Change Ni-MH charging current to 2A	0.1	34	Change PR231 to 26.1K	0.2	EVT1
P3		Improve overshoot voltage of charger start-up voltage	0.1	34	Change PC172 to 2700PF.	0.2	EVT1
P4		Setting OCP of CPU-Core at 30A	0.1	35	1. Remove PR112 2. Add +5VALW to PU9 Pin#10	0.2	EVT1
P5		Reduce noise on PU9	0.1	35	Change PC80 to 1UF/10V.	0.2	EVT1
P6		Trace between PF1 and PC1 too small	0.1	36	1. rework withg big wire 2. remove PL5 and enlarge trace in next ver.	0.2	EVT1
P7		Setting OVP point of Ni-MH charging voltage at 18.5V	0.1	36	Change PR74 to 768K.	0.2	EVT1
P8		Setting CPU thermal protection point to 100C	0.1	35	Change PR257 to 16.9K	0.2	EVT1
P9	AC018 With adapter connected, system will shut down by remove battery. AC019 Use R570.exe to check the charging status, battery cannot be charged	Function for selecting cell on PU10 didn't work well	0.1	36 34	1. Change PR127 to 15K. 2. Change PQ19 to SI2303DY.	0.2	EVT1
P10		Setting input of VID from system chip	0.1A	35	1. reserve PR280 2. Add +5VALW to PU9 pin#16	0.2	EVT1 DVT1
P11		Add PR272 for testing VR-ON	0.1A	35	Add PR272	0.2	DVT1
P12		Reverve resistors and capacitors for selecting B set of VID in PU9	0.2	35	1. Add PR273, PR274, PR275, PR276, PR277, PC190, PC191, PC192 2. set o to all resistor 3. set 4700PF to all capacitors	0.2	DVT1
P13		reserve resistor to adjust OCP setting point of PU9.	0.2	35	1. Add PR278. 2. set PR278 to 0	0.2	DVT1
P14		reserve resistor to have a option of A/B#	0.2	35	1. Add PR279. 2. set PR279 to 0	0.2	DVT1
P15		reserve resistor to have a option for monitoring feedback of CPU voltage	0.2	35	1. Add PR282, PR283 2. set PR282, PR283 to 0	0.2	DVT1
P16		reserve a resistor to ground PU9 pin11 for COREFB-	0.2	35	Add PR281	0.2	DVT1

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B. Ver#	Phase
P17		Reduce transition of control signal	0.2	34	1. Add PC187, PC188, PC189 2. set PC187, PC189 to .1UF	0.2	DVT1
P18		Cost down on common choke	0.2	36	1. reserve PL10, PL11 2. use KC FBM-LI11-322523-121AT at PL10, PL11 to replace PT2	0.2	DVT1
P19		Cost down on CPU thermal protection circuitry	0.2	36	1. delete PQ110, PC169, PD45, PR263, PD49 2. change the location of PH1 3. PR256 change to 5.11K 4. PR257 change to 7.32K 5. PR257 connect to VL	0.2	DVT1
P20		delete redundant resistor	0.2	34	delete PR163	0.2	DVT1
P21		Reduce leakage current of battery quiescent on system	0.2	34	Change PQ112 to SI4810DY		
P22		Improve EMI performance	0.1A & 0.2 0.2	35 33	add PL9 Change PR129, PR130 to 4.7	0.2	EVT1 DVT1 DVT1
P23		Improve voltage rating	0.2	35	Change PD39 from RB081L-20 to EC31QS04	0.2	DVT1
P24		Cost down on CPU_CORE	0.2	35	Delete PD28	0.2	DVT1
P25		Modify Thermal Protection to 85 degree C	0.3	36	1. Change PR256 to 0 2. Change PR258 to 16.9K 3. Change PR257 to 2.15K	0.2	PVT
P26		Improve current rating	0.3	36	Change PL11 and PL10 to CHENG-HANNCHC4532U800(1812)	0.2	PVT
P27		Change footprint	0.3	36	Change footprint of PR200 to R0805	0.2	PVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B. Ver#	Phase
P28		Enhance OVP function	0.2	34 36	1. change PQ15 from DTC115EK to 2N7002 (P34) 2. change PR83 from 100K to 10K (P36)	0.2	DVT1
P29		Increase charger OVP design margin for plugging out Ni_MH battery	0.3 0.4	36	1. change PC67 from 1000pF to 0.1uF 2. change PC66 from 1uF to 4.7uF 3. add PC194 0.1uF 0805 4. add PR287 1M 5. add PR286 2.2K 0805 6. add PQ117 2N7002	0.3	DVT3
P30		Fix OVP function	0.4	36	1. change pin#6 of PU4 connection from VREF to RTCVREF 2. change PR84 from 249K to 374K 3. change PR74 from 768K to 1.1M	0.3	DVT3
P31		Remove OVP function	0.4	36	1. Delete PQ25 and PQ26 2n7002 2. Delete PR87 100K +-5% 0603 3. Delete PR82 324K +-1% 0603 4. Delete PR73 39K +-5% 0603 5. Delete PR83 10K +-1% 0603 6. Delete PR72 and PR74 1M +-0.5% 0603 7. Delete PC66 4.7UF_1206_25V 8. Delete PC67 0.1UF_0603_16V 9. Delete PD25 1SS355 10. Delete PC65 2.2UF_16V 11. Change PR84 from 249K to 0	0.3	DVT3
P32							
P33							
P34		Increase design margin		34	1. Add PR288 10K 2. Change PR59 from 10K to 3.9K 3. Change PR11 from 150K to 51K 4. Change PR241 from 113K to 95.3K		DVT3
P35				36	5. Change PR270 from 100K to 33K 6. Change PC167 from 1U to 1000P		
P36		Reduce leakage current while plugging out Adapter		34	1. Change PQ15 from DTC115EK to 2SC2411K 2. Change PR288 from 10K to 0		DVT3
P37							
P38							

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