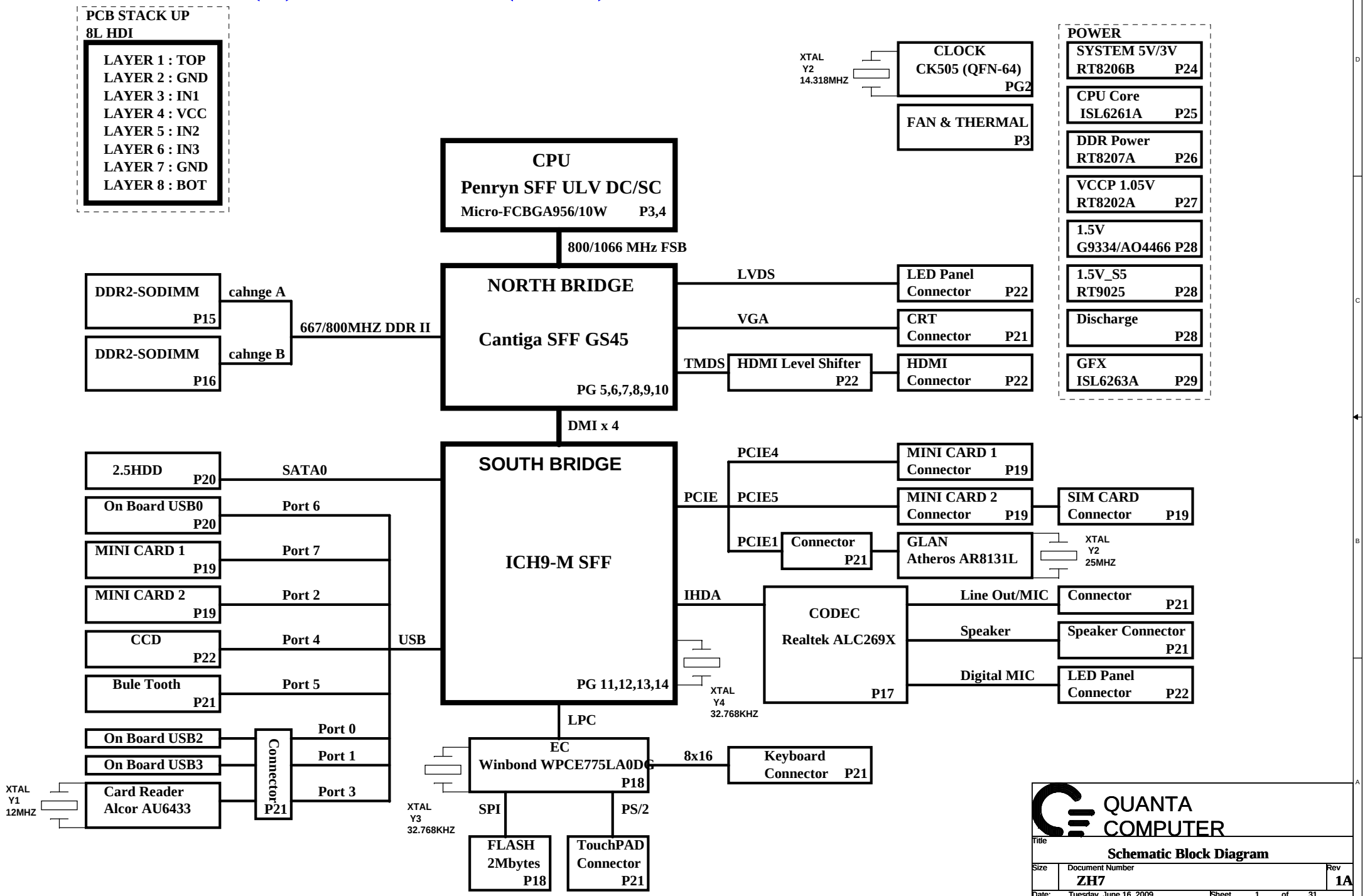
(S)JM11_MS (ZH7) BLOCK DIAGRAM



QUANTA COMPUTER

Title	Schematic Block Diagram	
Size	Document Number: ZH7	Rev: 1A
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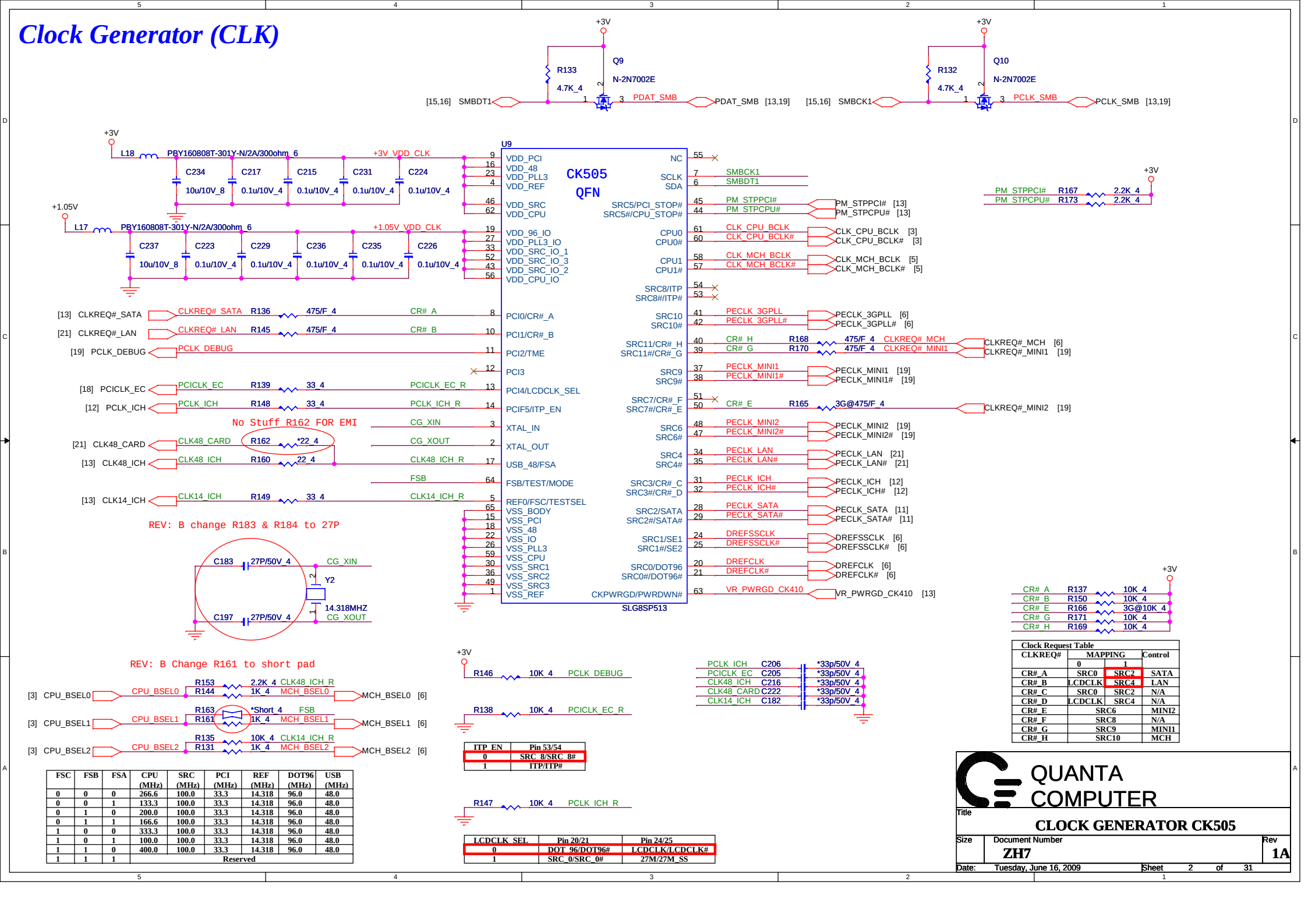
Clock Generator (CLK)



FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#

LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

Clock Request Table			
CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

QUANTA COMPUTER

Title: CLOCK GENERATOR CK505

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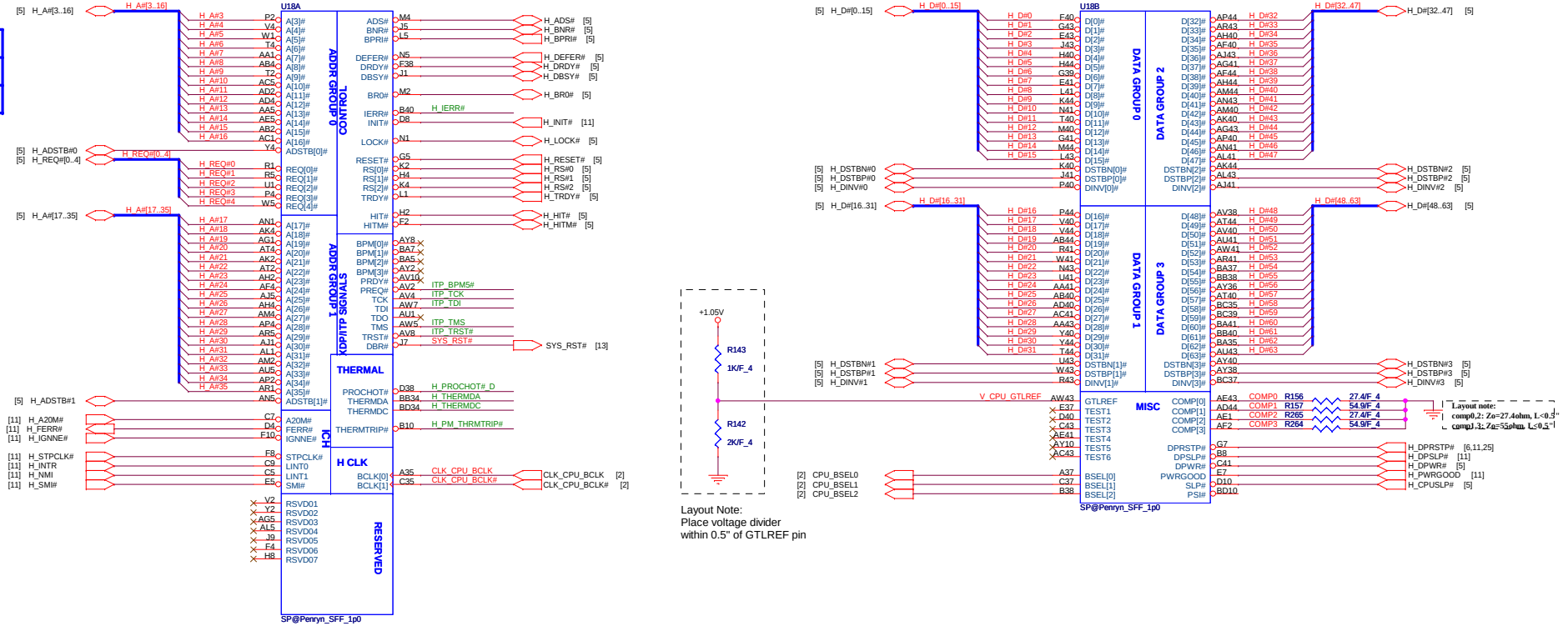
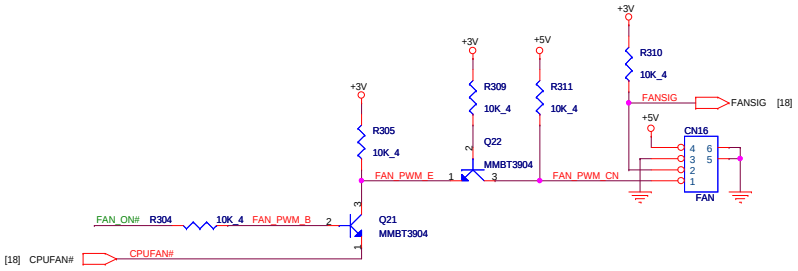
Penryn SFF - Host Bus (CPU)

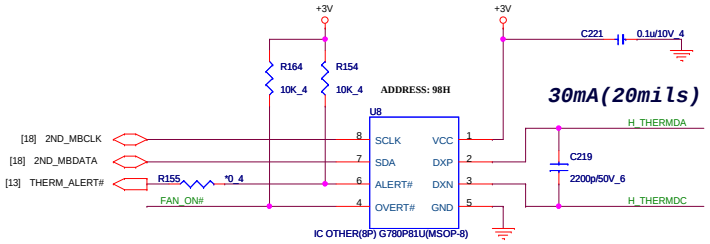
1.2G	AJSLGAMVT02
1.4G	AJSLGFMTT00



CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



QUANTA COMPUTER

Title	Penryn SFF (Host Bus)/FAN/Thermal	
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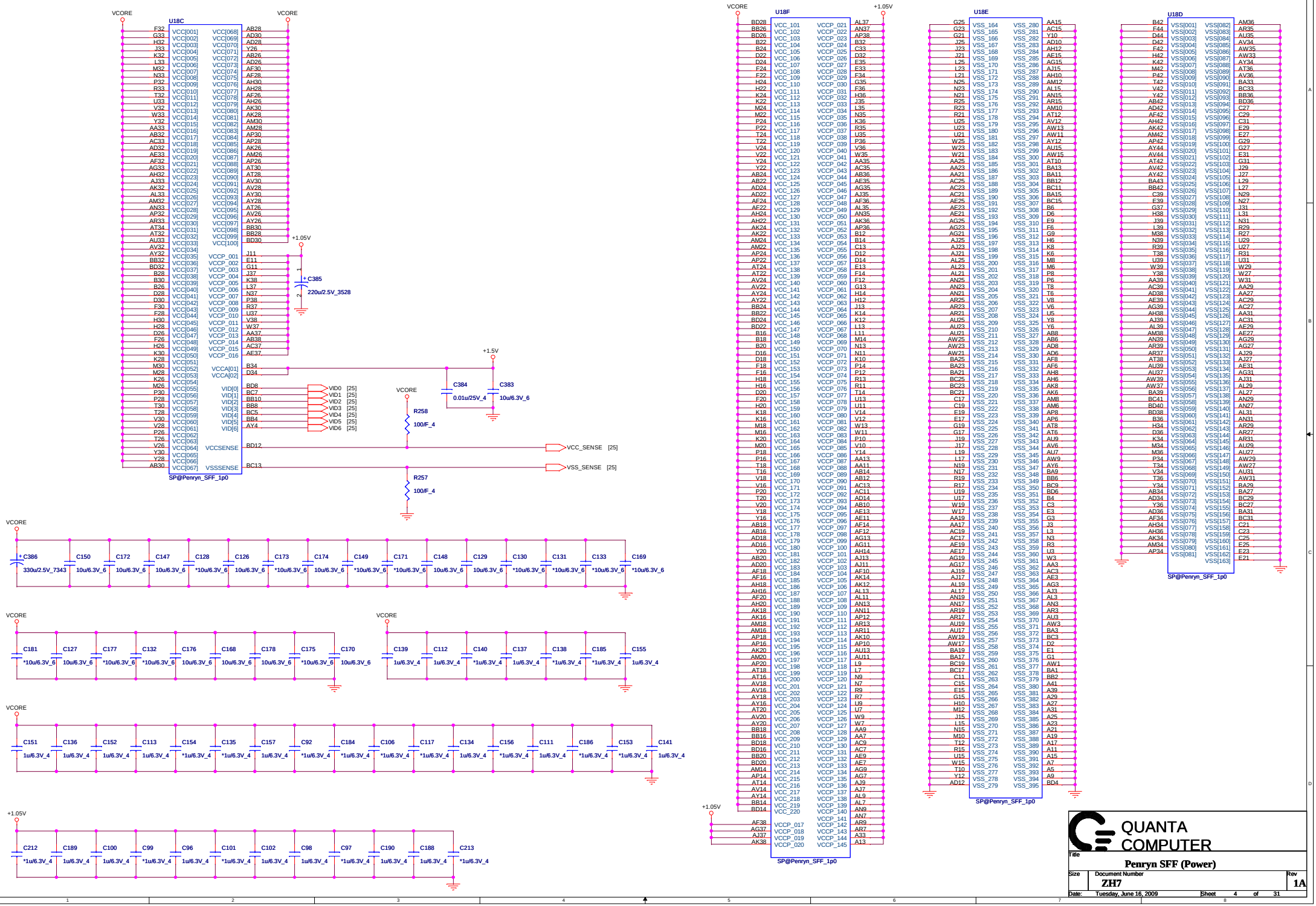
Penryn SFF - Power (CPU)



QUANTA COMPUTER

Title	Penryn SFF (Power)	
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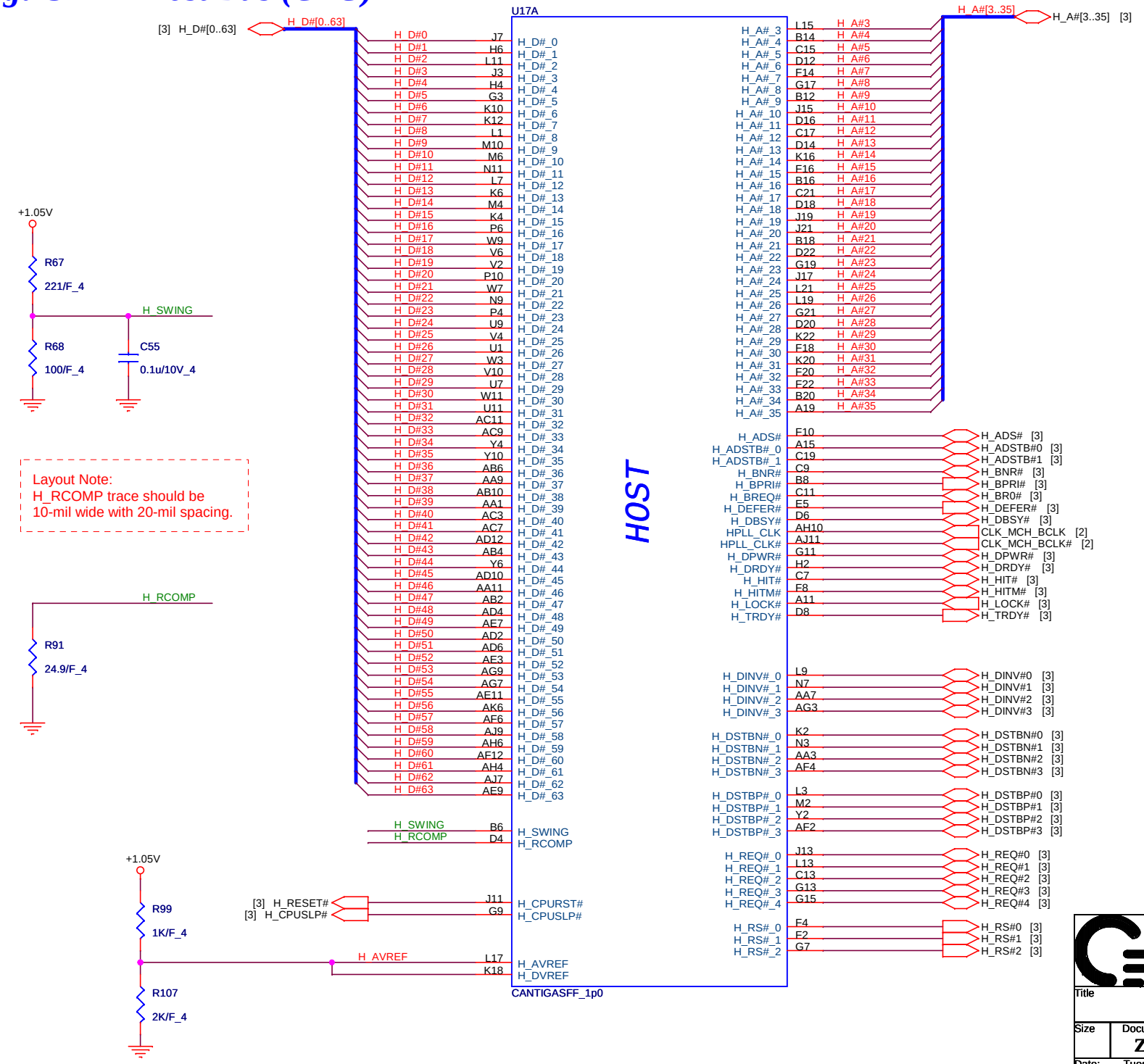
Cantiga SFF - Host Bus (CLG)



QUANTA COMPUTER

Title	Cantiga SFF (Host Bus)	
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Cantiga SFF - DMI/VGA (CLG)

Intel GS40/GS45 Strapping Signals and Configuration		
Pin Name	**Strap Description**	**Configuration**
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/HDMI/DP interface enabled 0 = No SDVO/HDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present; PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) devide present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 kΩ ±1%
- The recommended pull-down resistor value is 2.21 kΩ ±1%.

U17B

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
CFG
DMI
GRAPHICS VID
PM
GRAPHICS
ME
MISC
NC
HDA

CANTIGASFF_1p0

U17C

CLG
PCI-EXPRESS GRAPHICS
DMI
VGA

CANTIGASFF_1p0

HDMI Port B

CRT setting

LVDS setting

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

Check list note : CL_REF=0.35V

REV: B Change R254 to short pad

Title	Cantiga SFF (DMI/VGA)
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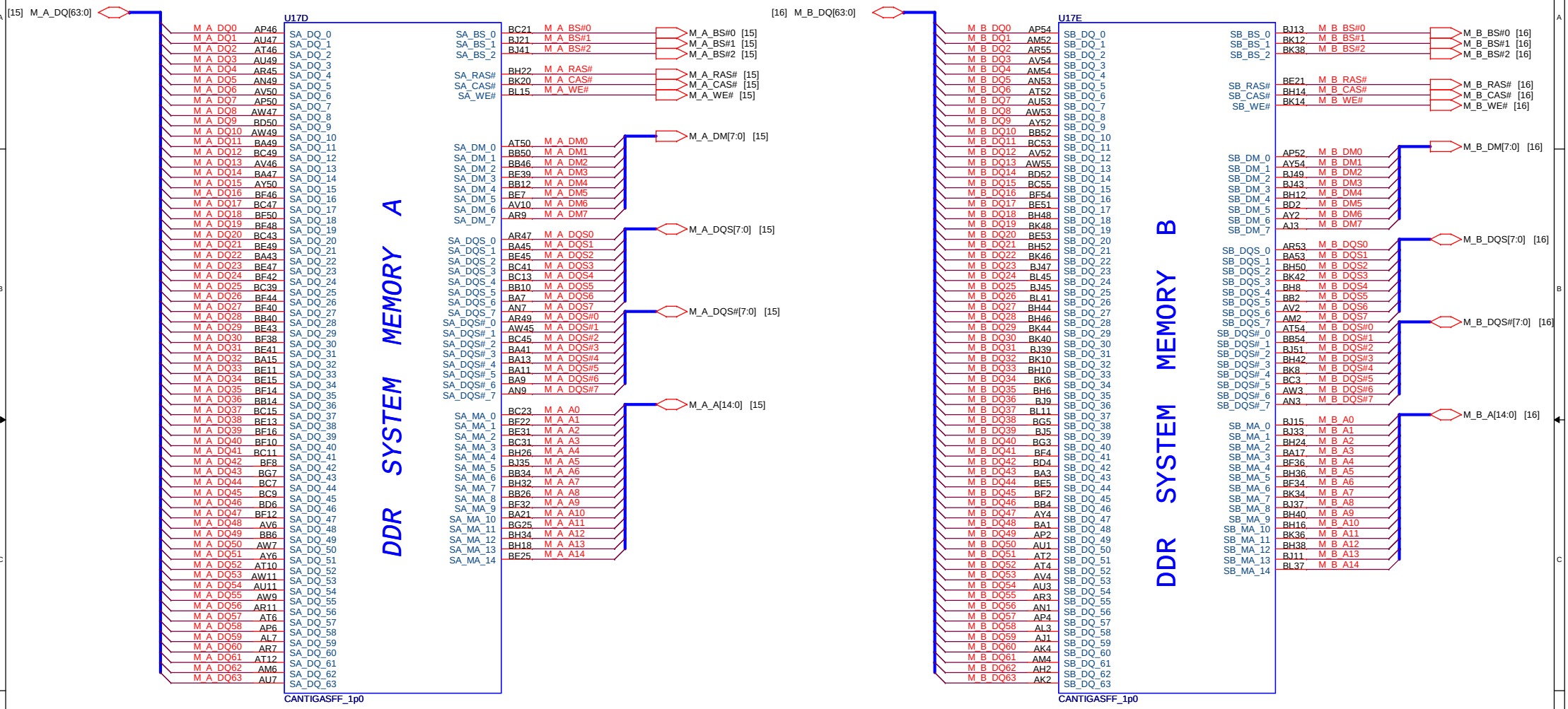
QUANTA COMPUTER

Cantiga SFF - DDRII (CLG)



Title	Cantiga SFF (DDRII)
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Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

DDR2-667 2.6A
DDR2-800 3A
(Shape or 140mils)

UMA 9.6A(GM45)
(Plane or shape)

VCC 2200mA

VCC_SM :3000mA

VCC_AXG 7700mA

U17F

U17G

CANTIGASFF_1p0

VCC CORE

POWER

VCC NCTF

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

Differential routing

[29] GFX_VCCSENSE
[29] GFX_VSSSENSE

Close to GMCH

Layout Note:
Inside GMCH cavity.

Layout Note:
370 mils from edge.

10mil

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

QUANTA COMPUTER

Title	Cantiga SFF (VCC/NCTF)	
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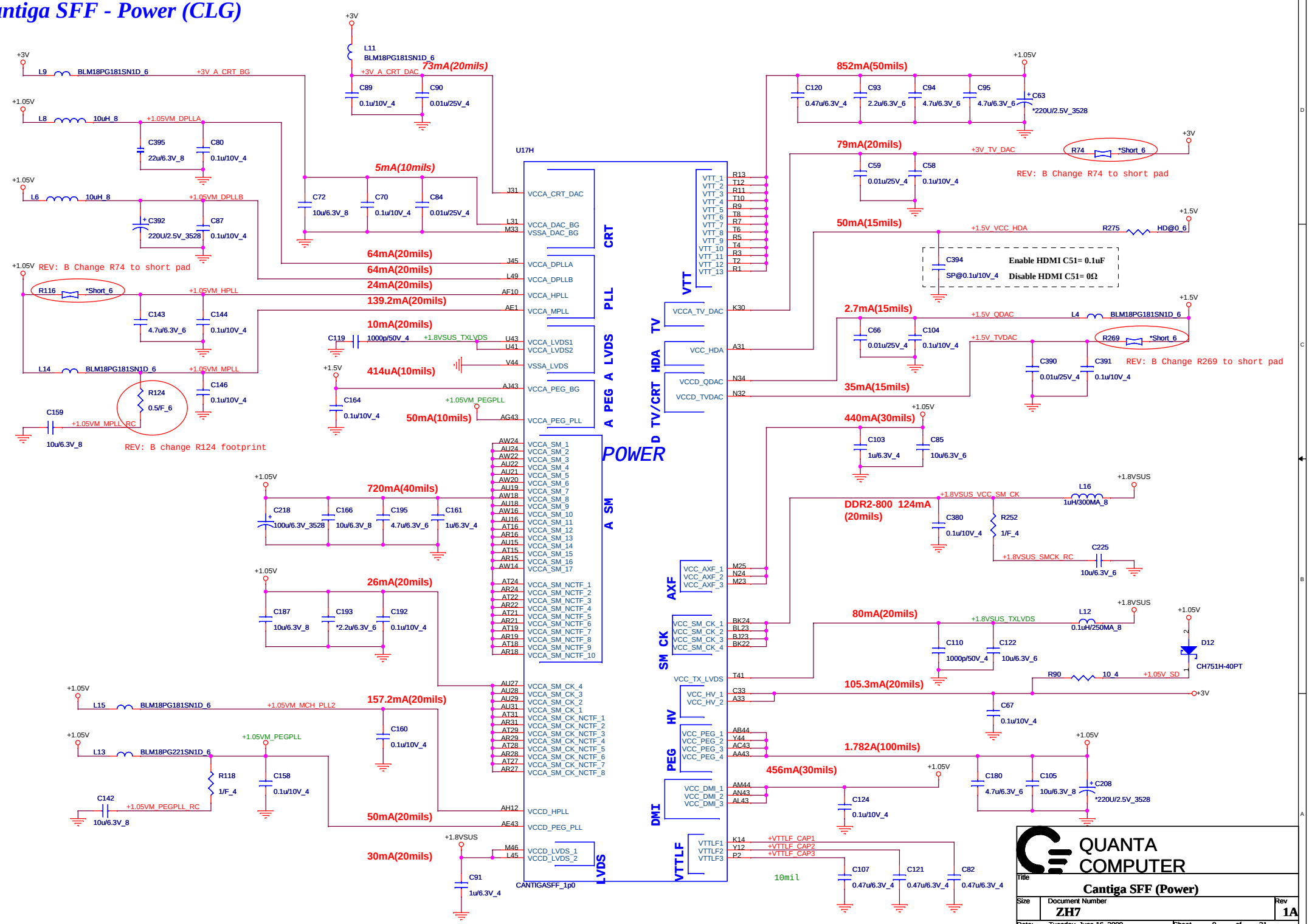
Cantiga SFF - Power (CLG)



Title	Cantiga SFF (Power)		
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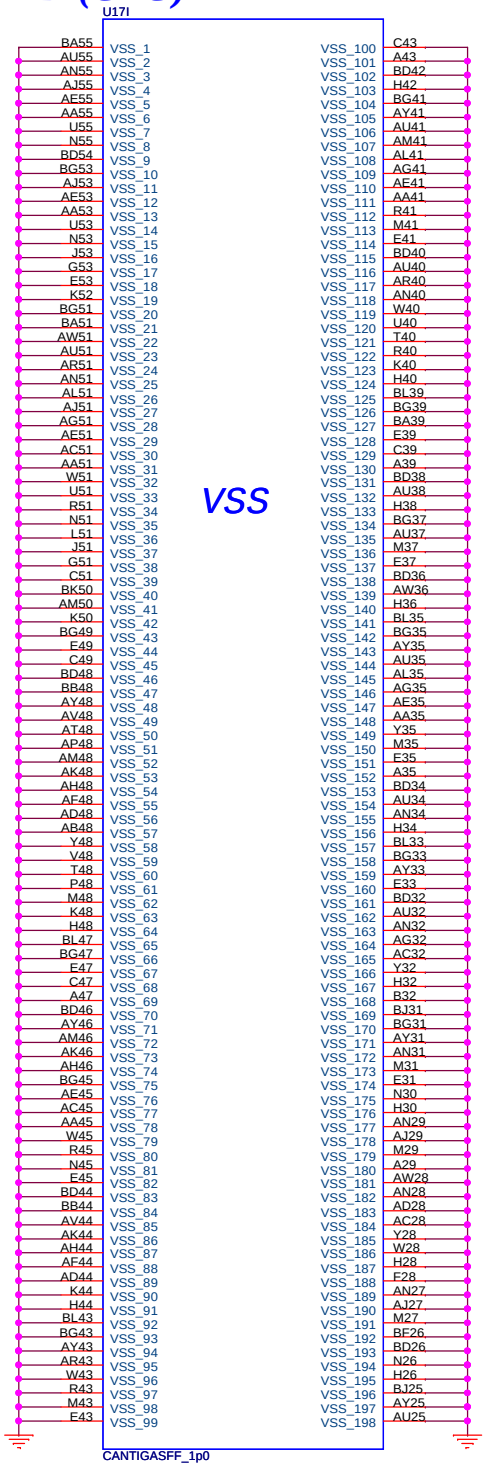
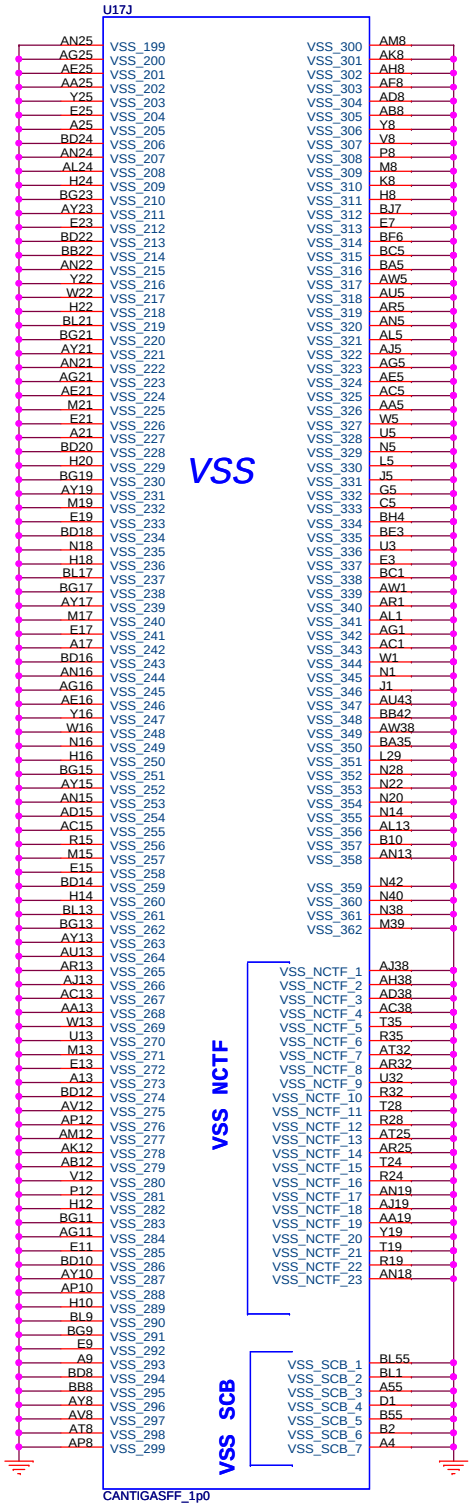
Cantiga SFF - GND (CLG)





QUANTA COMPUTER

Title	Cantiga SFF (GND)	
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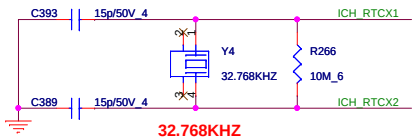
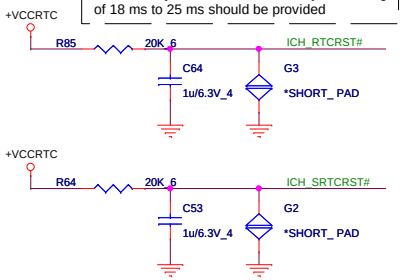
RTC CRYSTAL

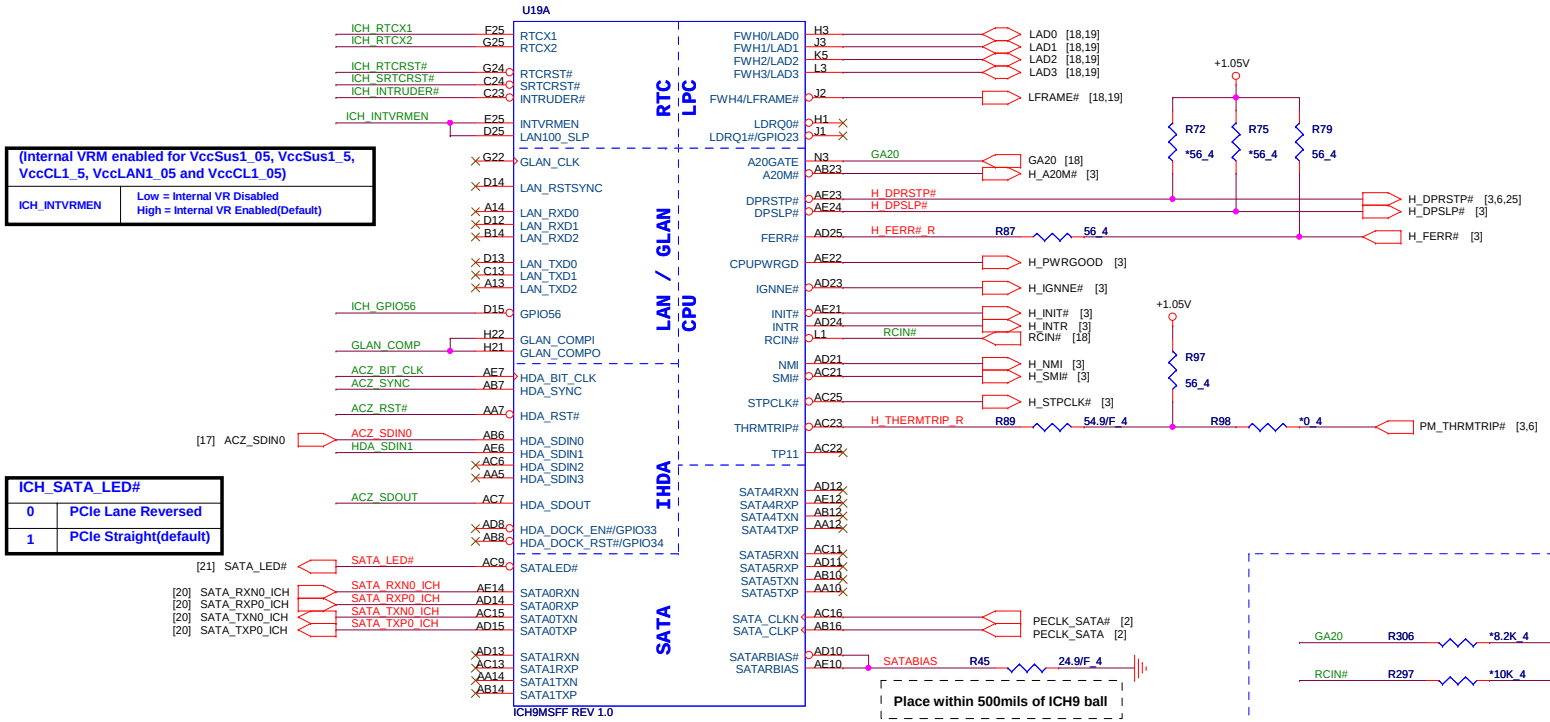


RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided

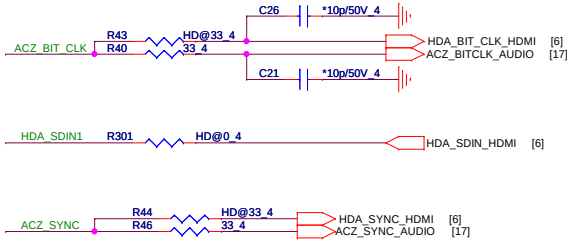


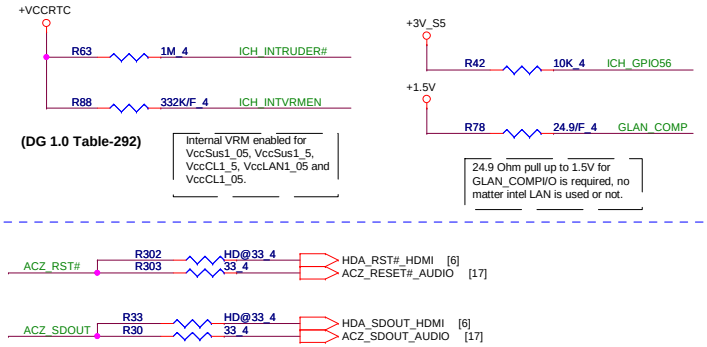
ICH9M SFF - Host,SATA,HDA (CLG)



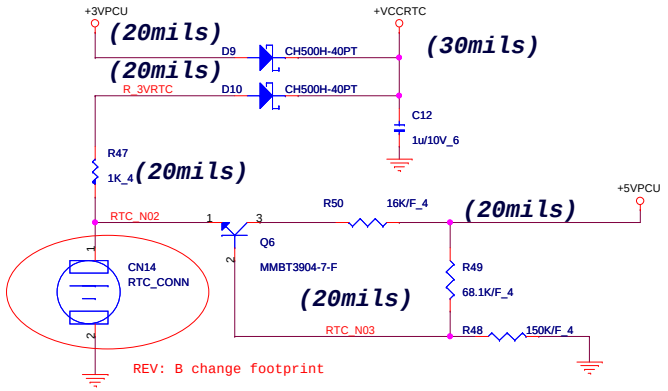
ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

HD Audio Interface





RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

REV: B del. R282 , add T23

ACZ_SDOUT T24
ACZ_SYNC T25
REV: B del R36 & R39 , add T24 & T25

QUANTA COMPUTER

Title	ICH9M SFF (Host/SATA/HDA)	
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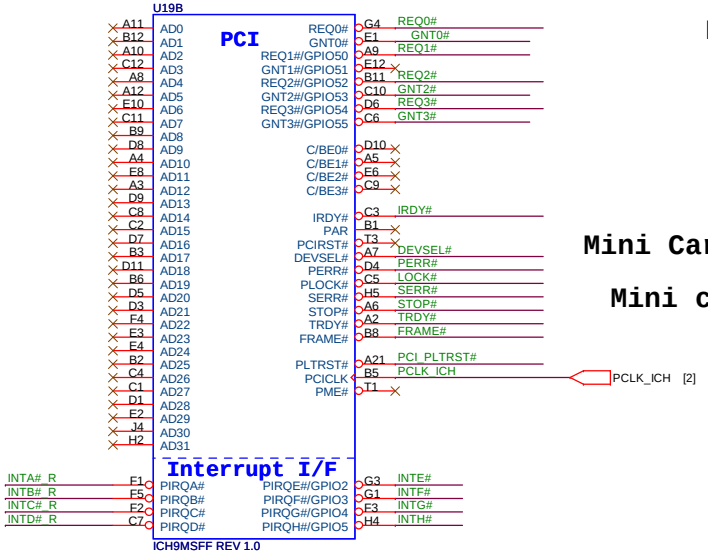
ICH9M SFF - USB/PCIE/DMI (CLG)

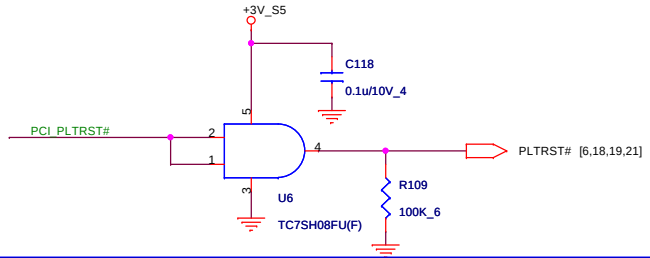
Place TX DC blocking caps close ICH9.

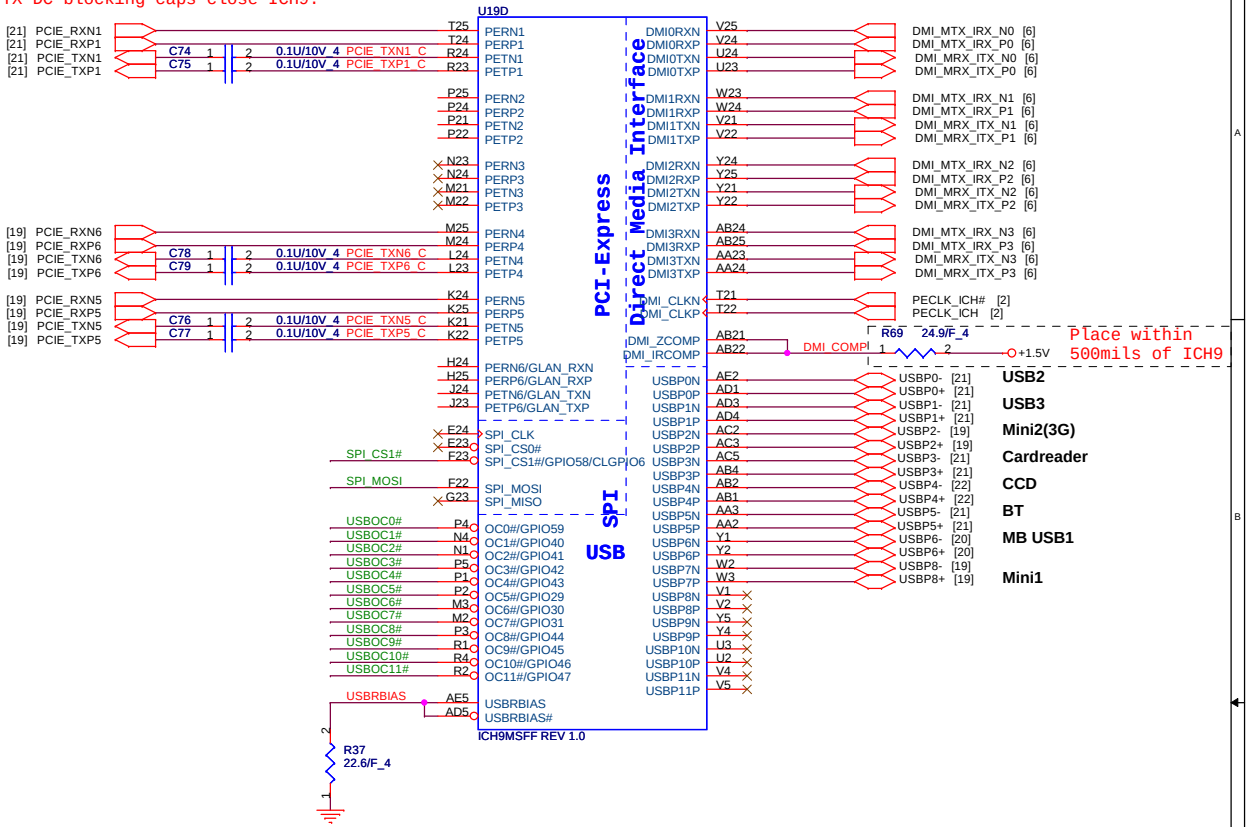
LAN

Mini Card (Wi-Fi)

Mini card (3G)



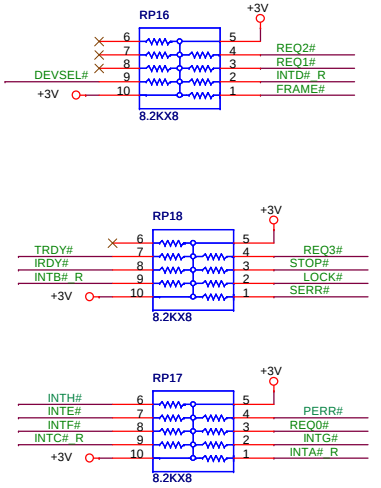




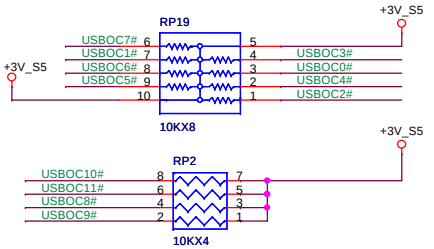
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T6
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# — T4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T11
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI	GNT0# — T2
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — T10

PCI PULL-UP



USBOC# PULL-UP



QUANTA COMPUTER

Title	ICH9M SFF (USB/PCIE/DMI)	
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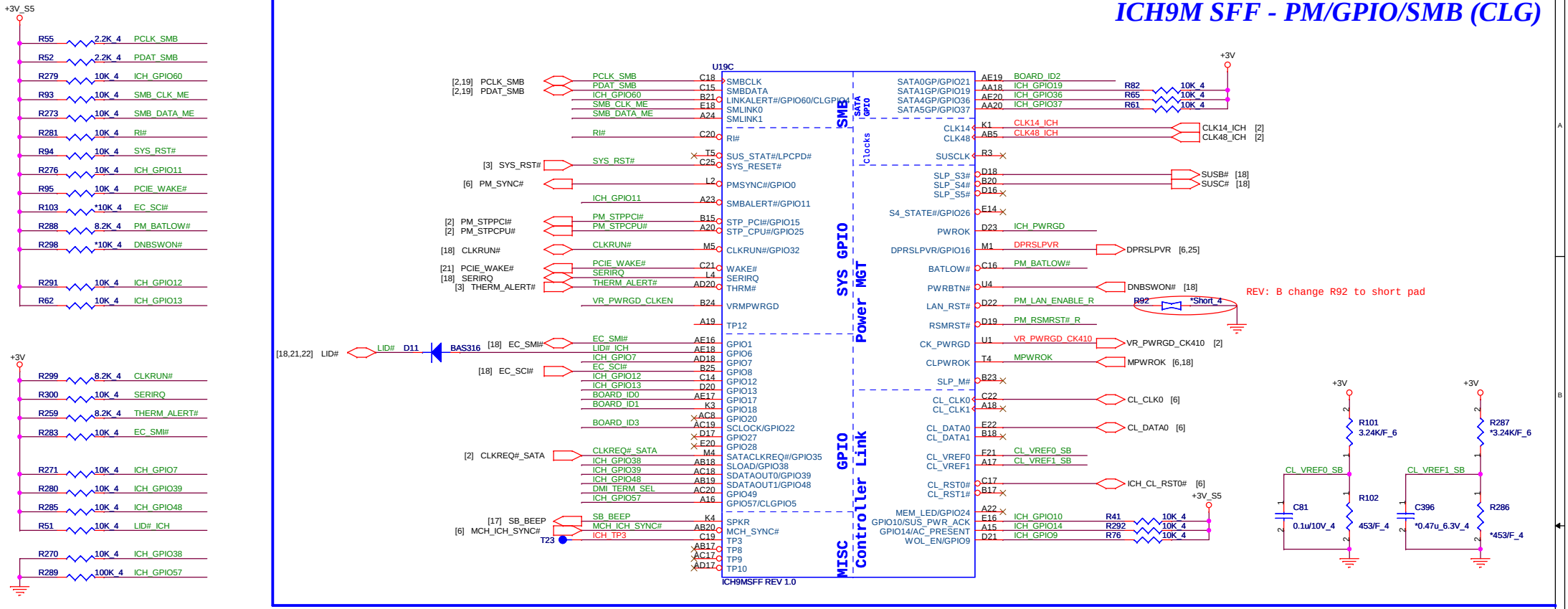
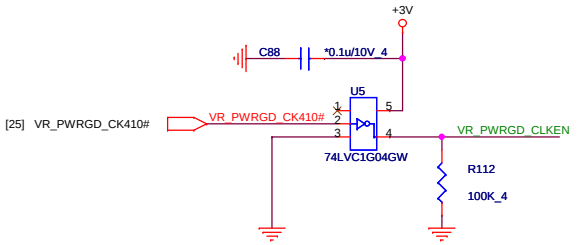
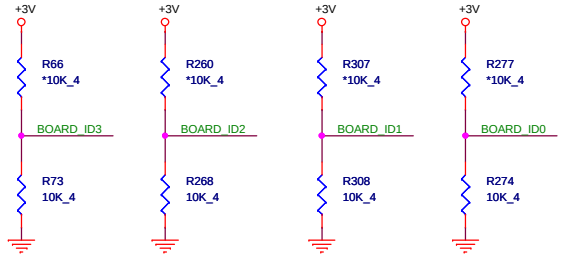
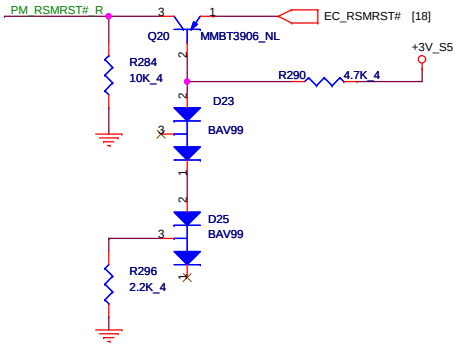
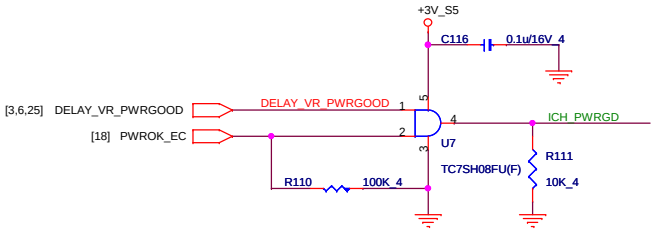
ICH9M SFF - PM/GPIO/SMB (CLG)











South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL — T12

QUANTA COMPUTER

Title	ICH9M SFF (PM/GPIO/SMB)	
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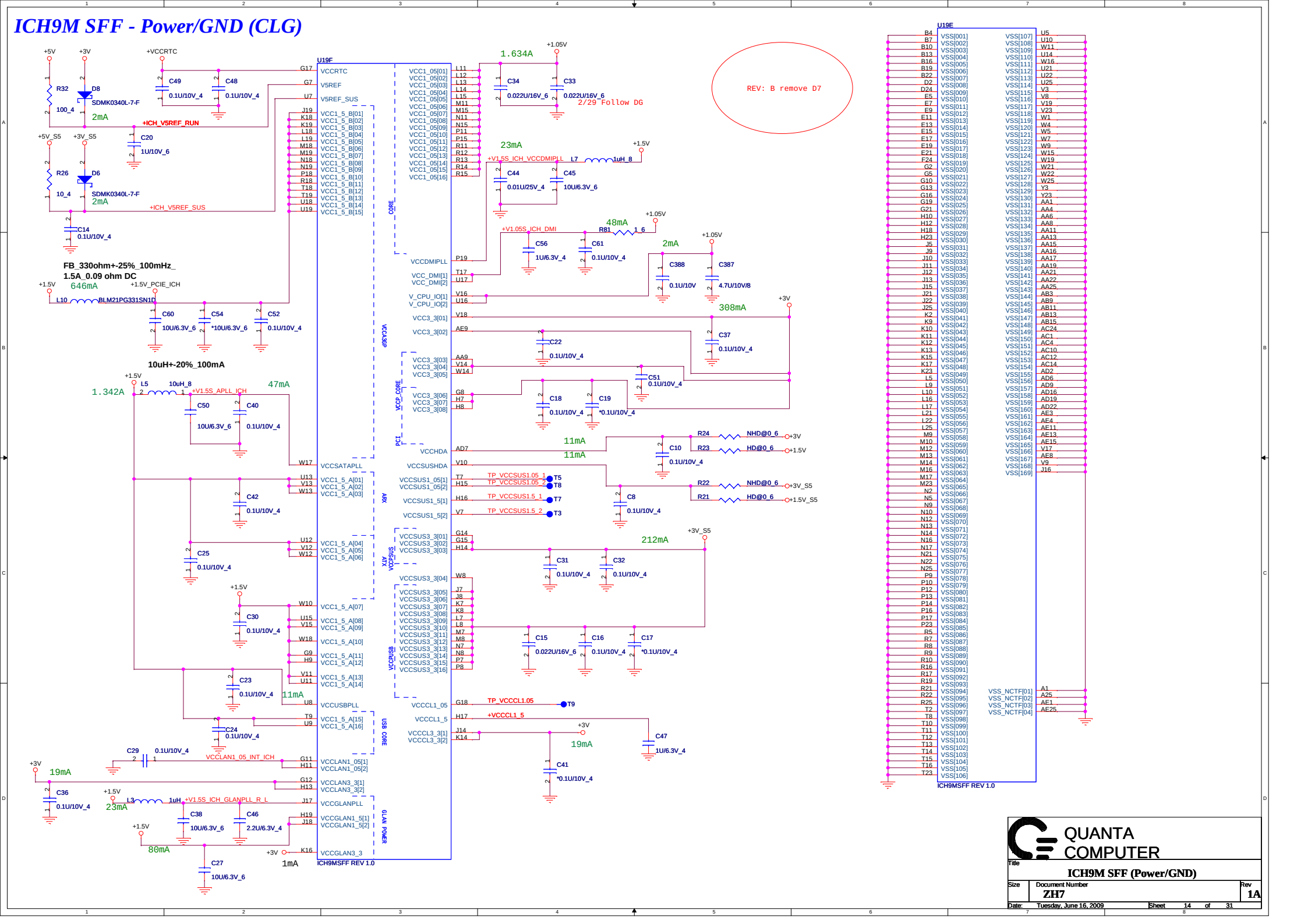
ICH9M SFF - Power/GND (CLG)



Title	ICH9M SFF (Power/GND)
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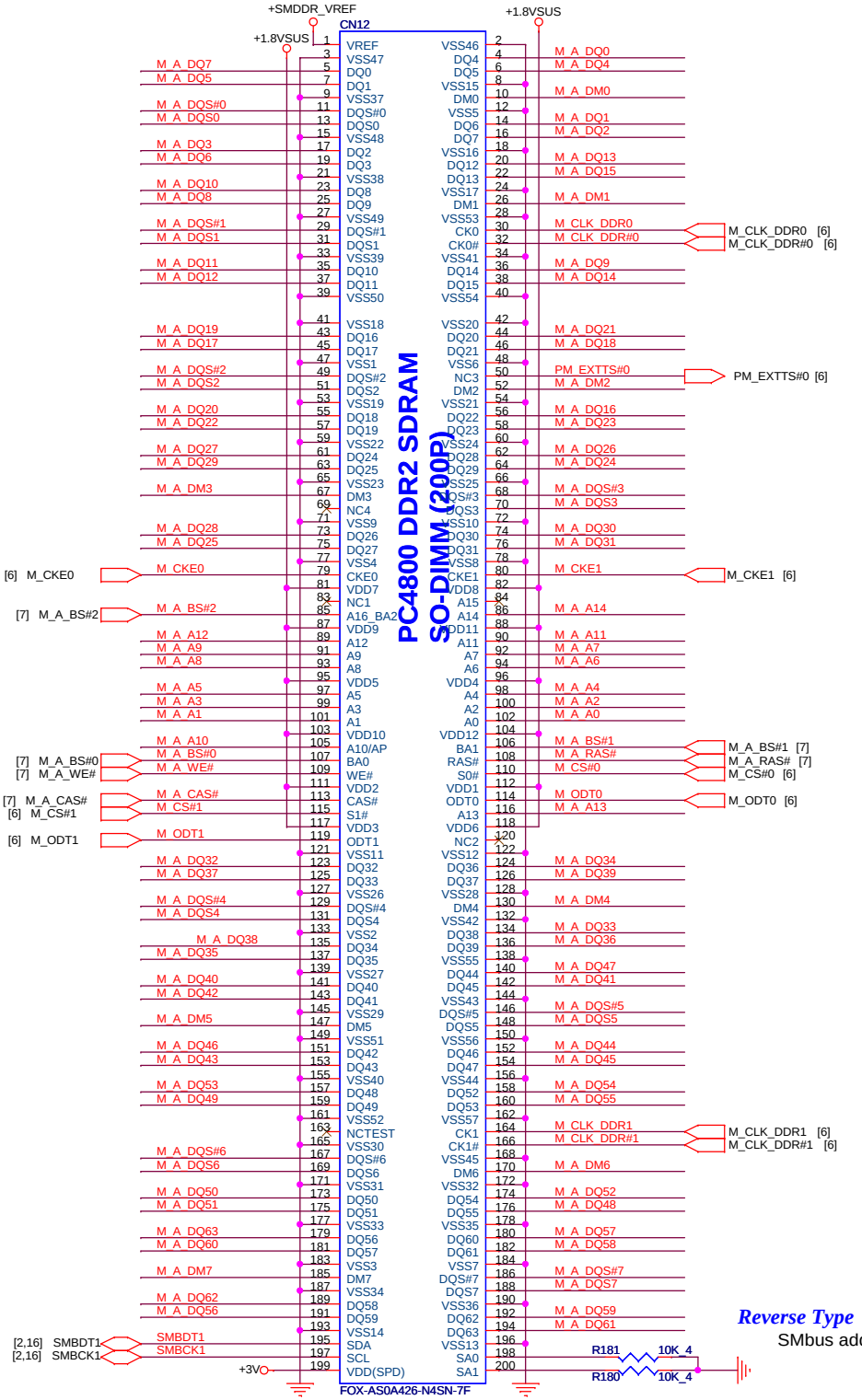
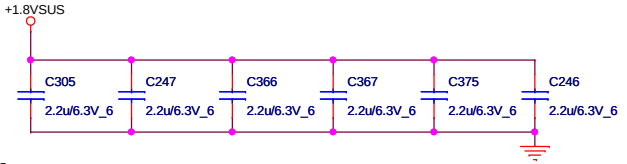
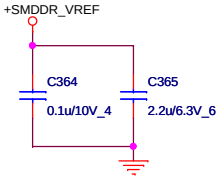
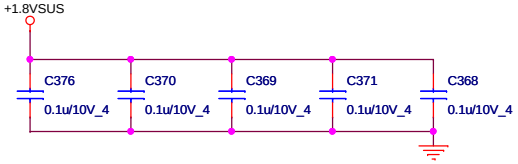
QUANTA COMPUTER

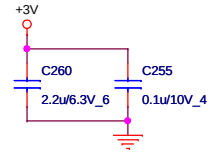
DDRII SO-DIMM (DDR)

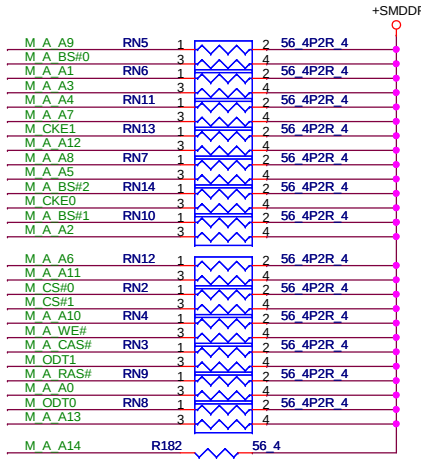


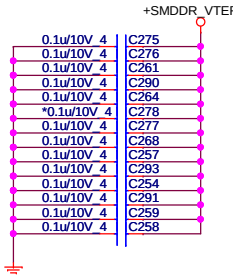


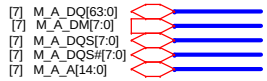












Reverse Type H: 5.2mm

SMbus address A0

QUANTA COMPUTER

Title: DDRII SO-DIMM		
Size	Document Number: ZH7	Rev: 1A
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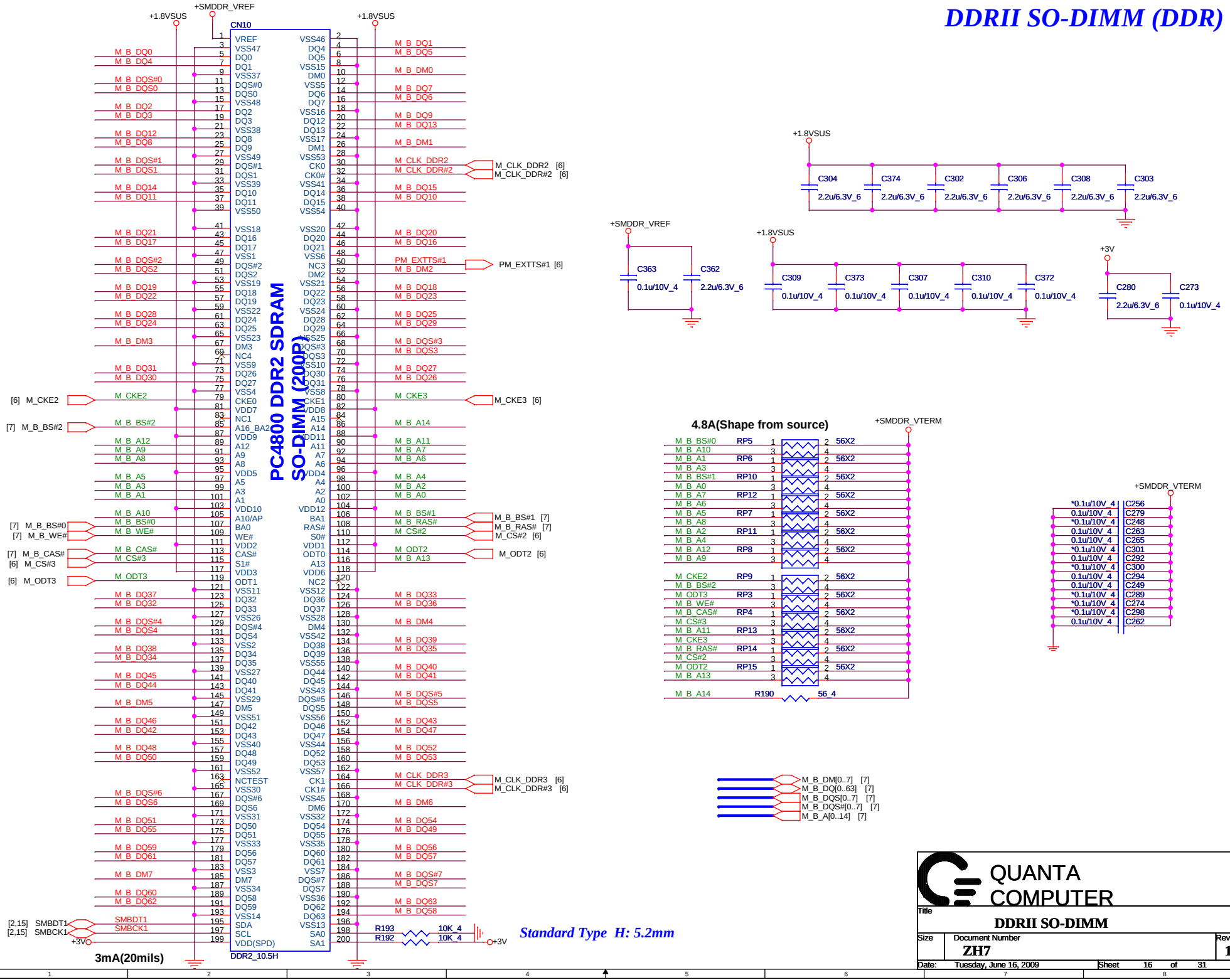
DDRII SO-DIMM (DDR)



Title	DDRII SO-DIMM		
Size	Document Number ZH7		Rev 1A
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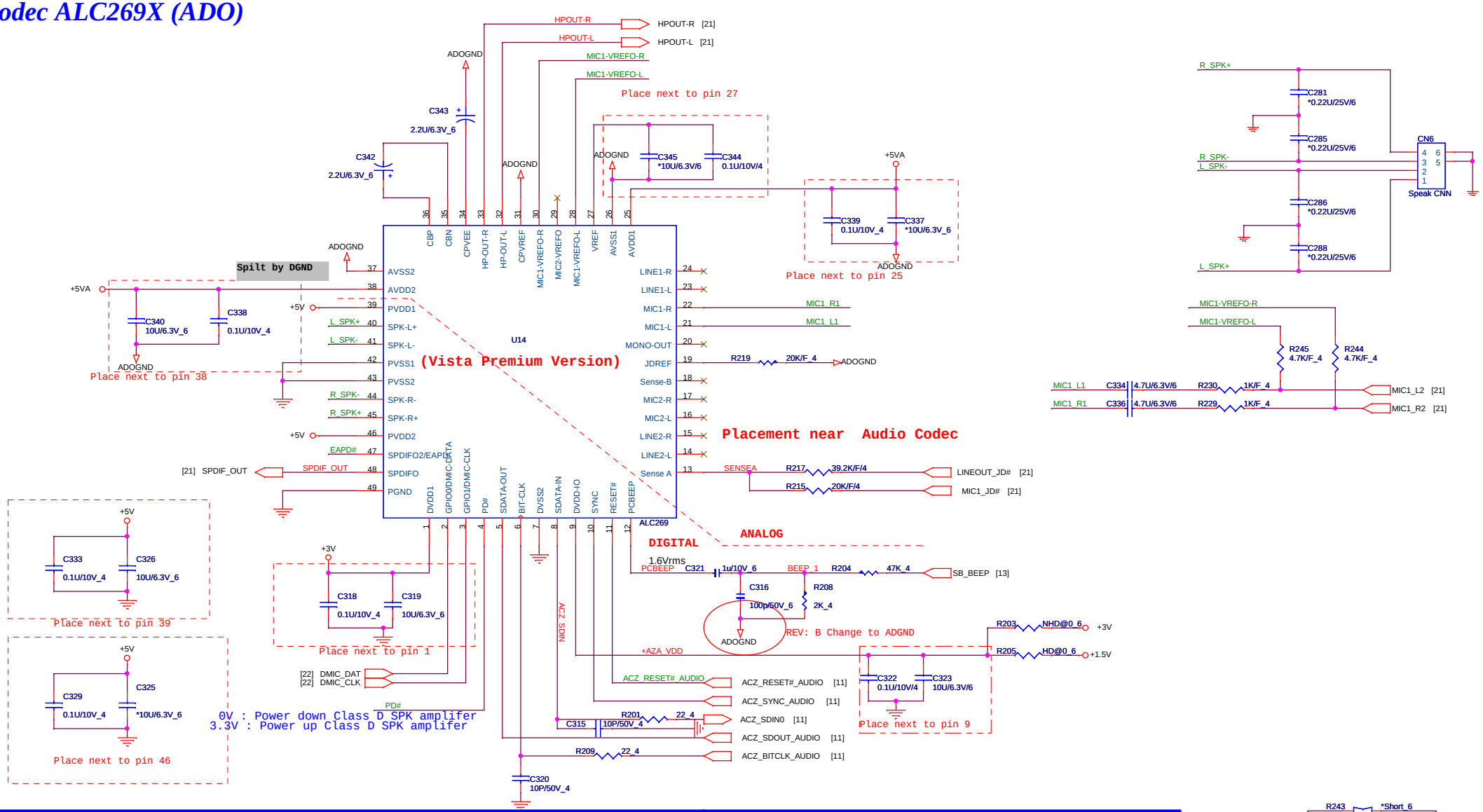
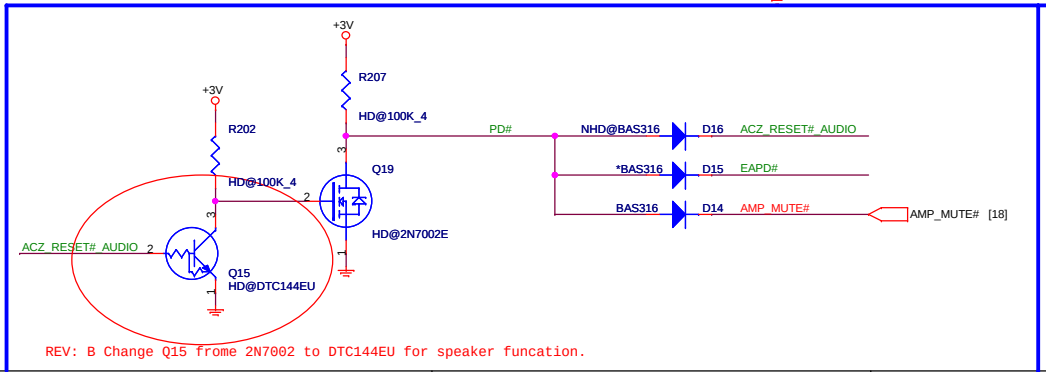
QUANTA COMPUTER

Codec ALC269X (ADO)

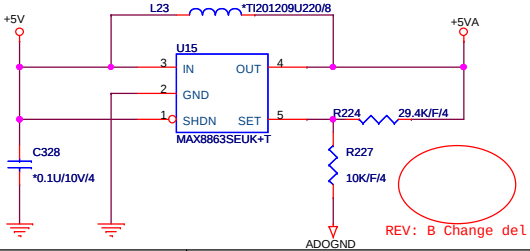




Power (ADO)

Demodulation Filter

Place close to Codec



QUANTA COMPUTER

Title	Codec ALC269X	
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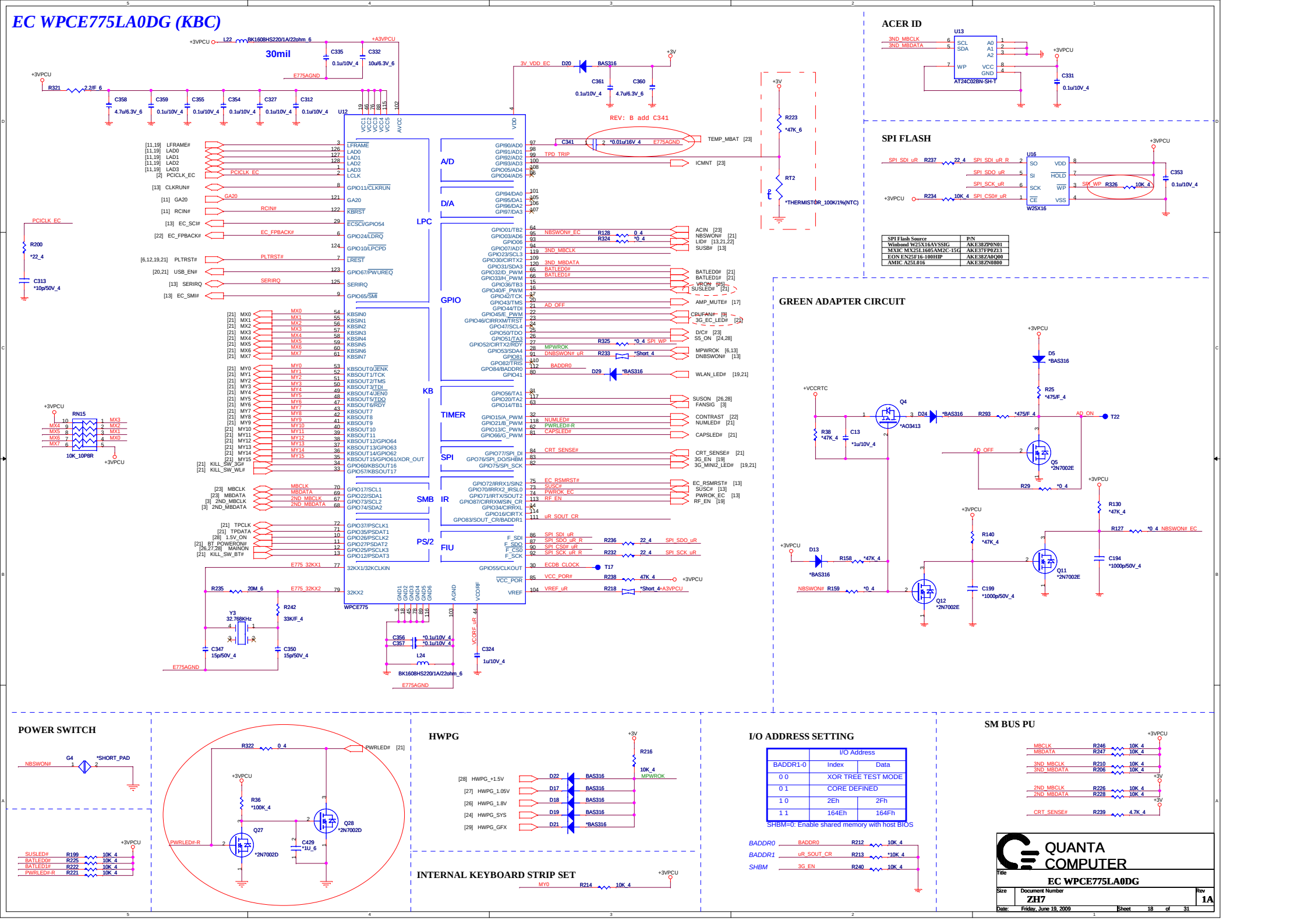
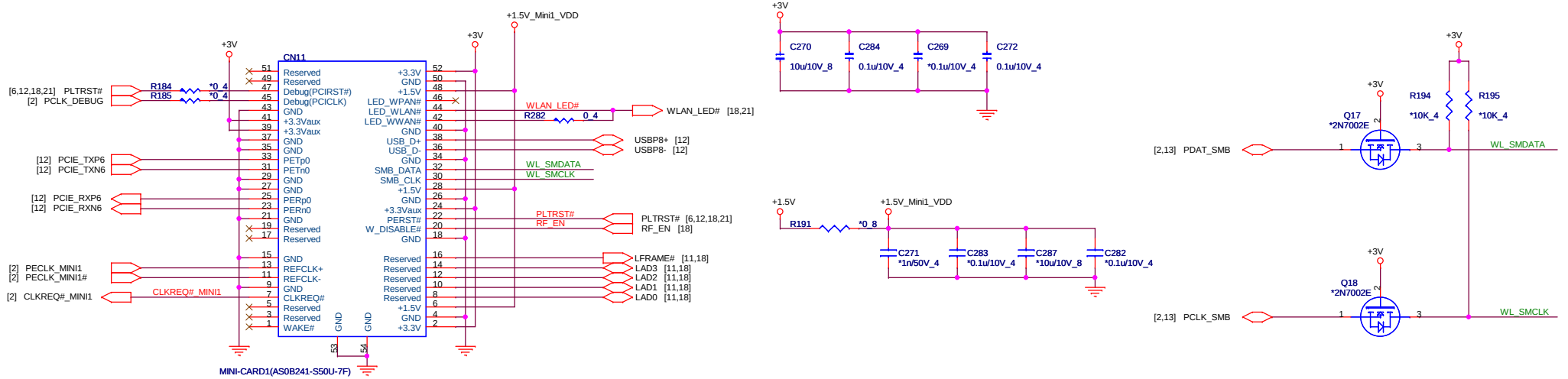
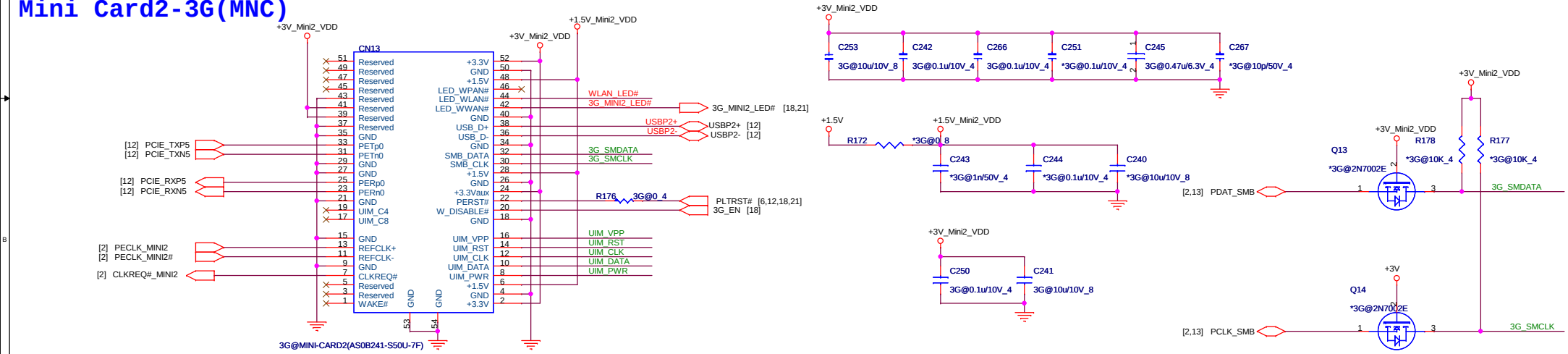
EC WPCE775LA0DG (KBC)

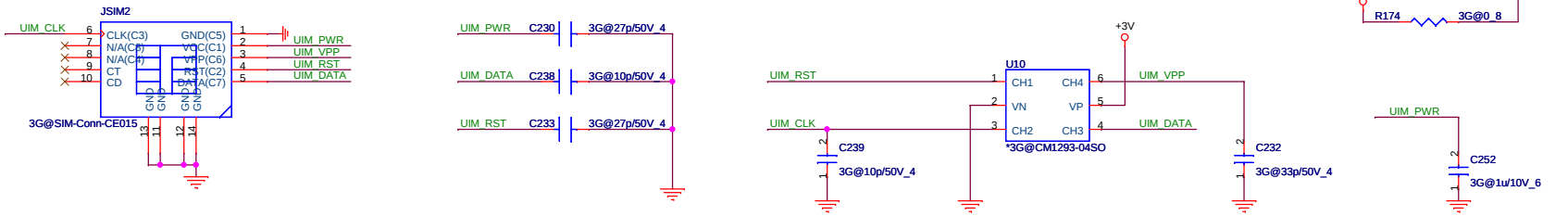


Mini Card1-WLAN/WMAX(MPC)



Mini Card2-3G(MNC)





Title	MINI PCIE (WLAN/WMAX/3G)	
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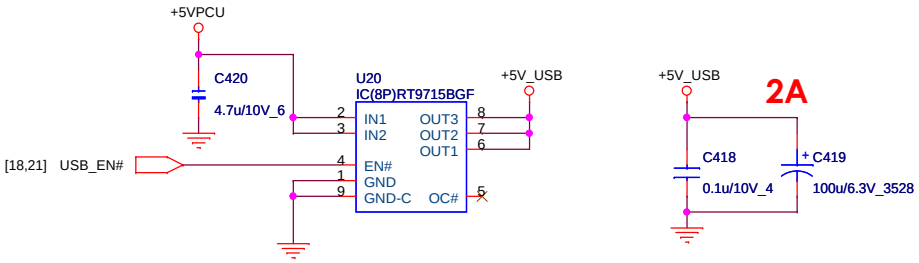
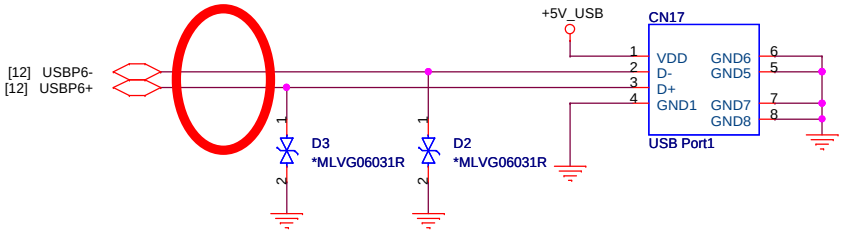
QUANTA COMPUTER

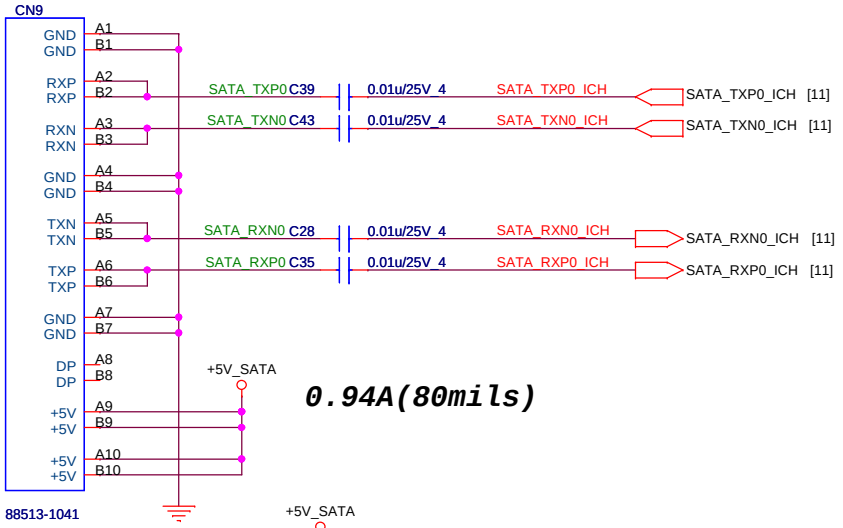
MB USB (USB)

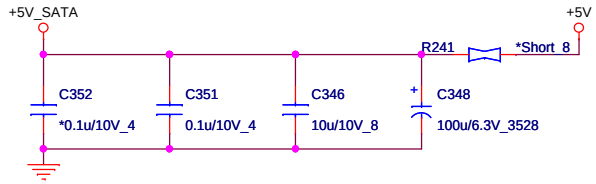


Remove R6、R7、L2

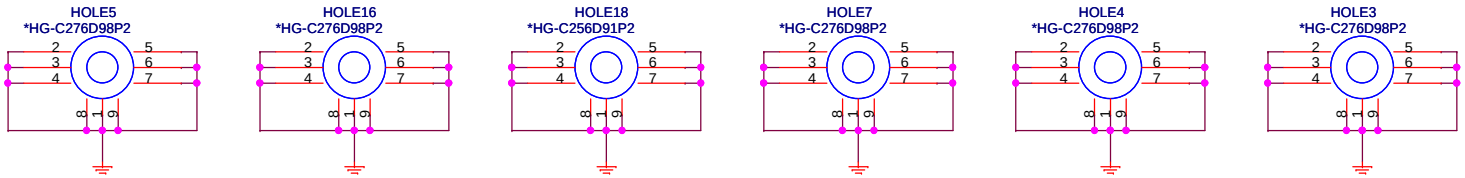


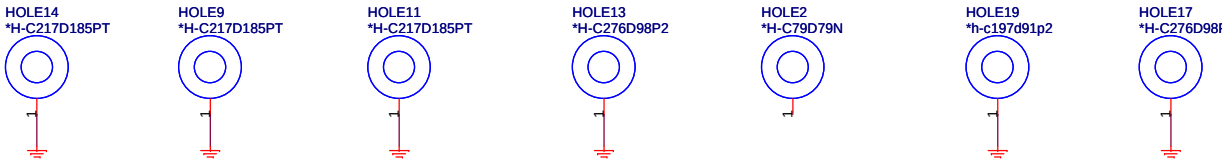
2.5" SATA HDD(HDD)

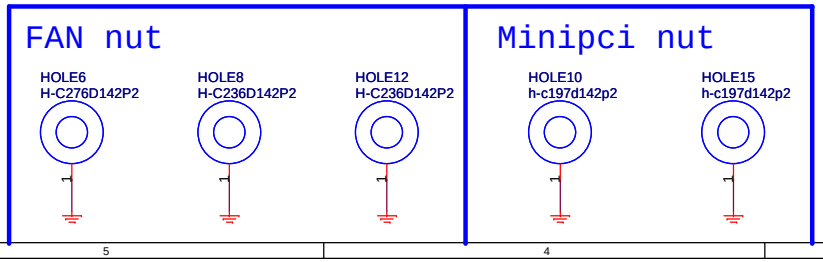


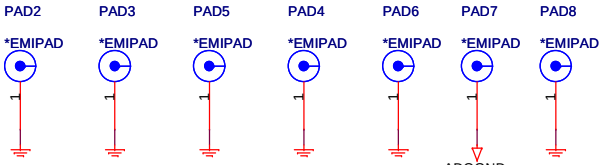


HOLE (EXC)









QUANTA COMPUTER

Title	USB/HDD/HOLE	
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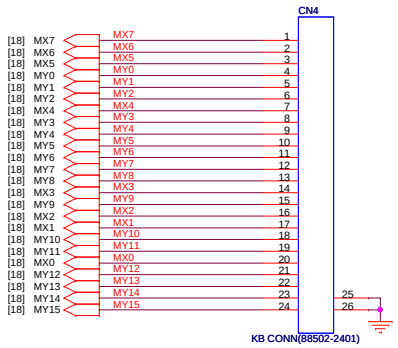
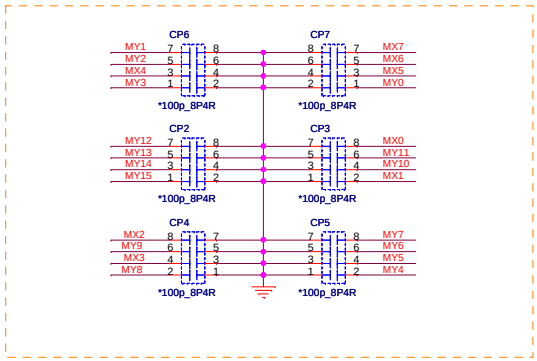
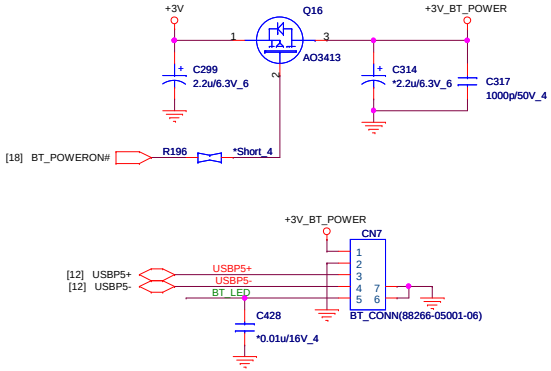
Keyboard(KBC)



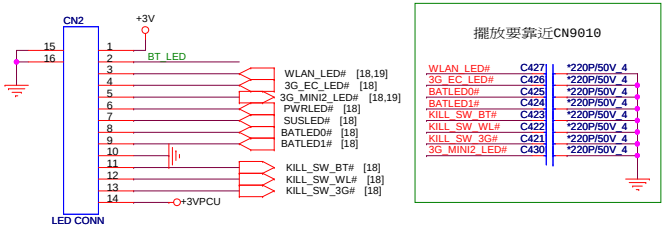
For EMI Reserve Caps for debug



BuleTooth (BTM)

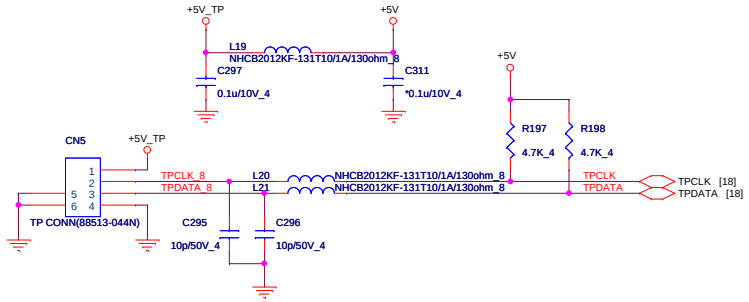


LED D/B (UIF)

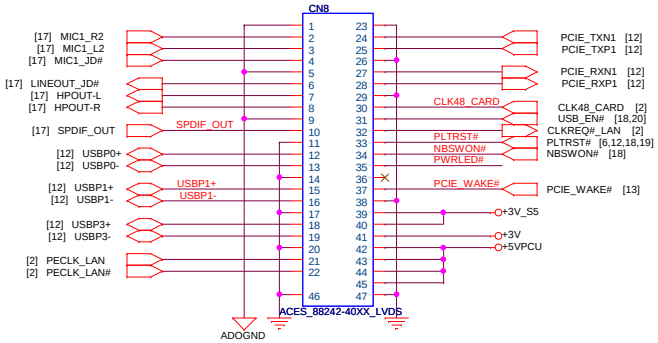


Check P/N footprint

Touch Pad D/B (TPD)

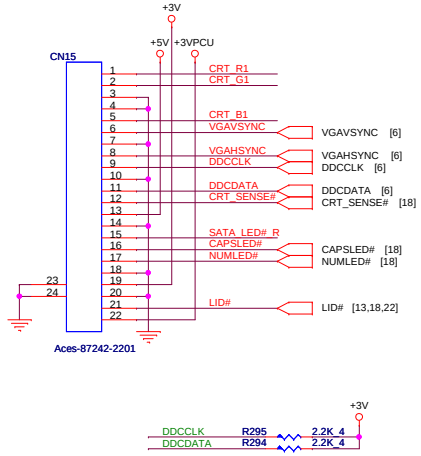


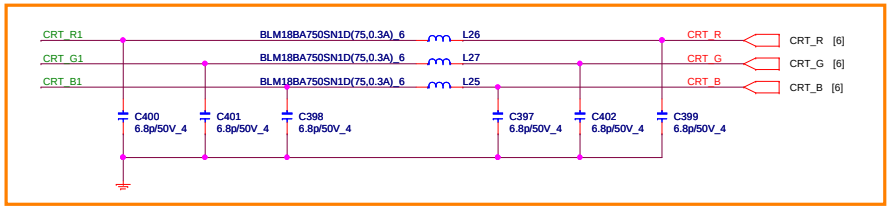
Card Reader/USB DB CONNECTER(MMC)/Power Connector



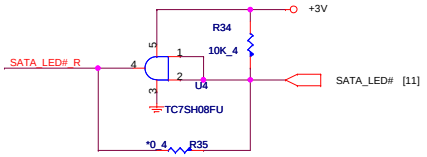
REV: B DEL CN8.36 SUSLED#

CRT D/B (UIF)





For EMI



QUANTA COMPUTER

Title	KB/BT/PR/TP/LAN/LED/CR Connects	
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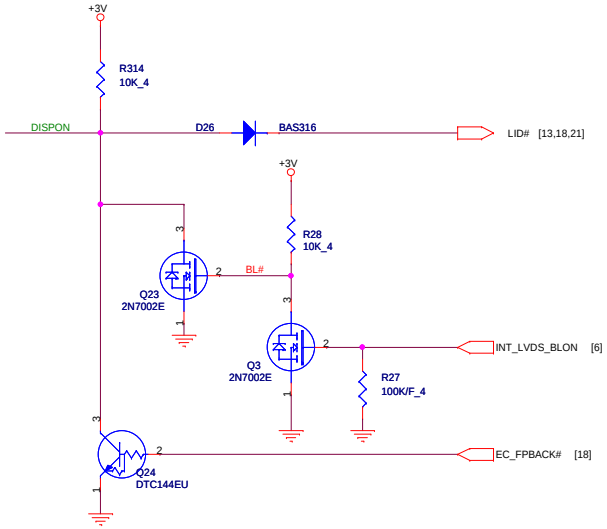
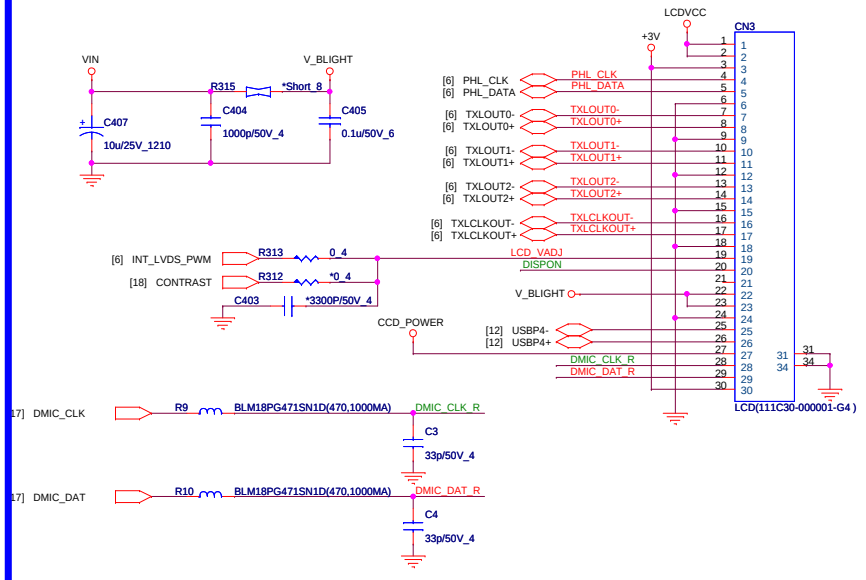
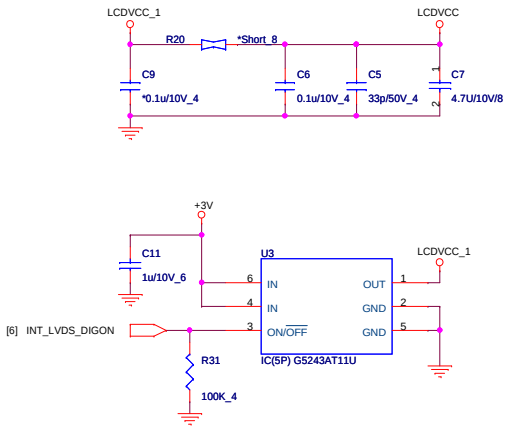
Backlight Control(LDS)



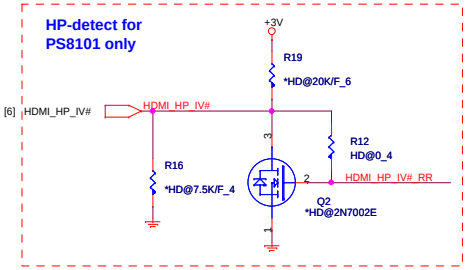
LED Panel(LDS)



LED Panel POWER SWITCH(LDS)

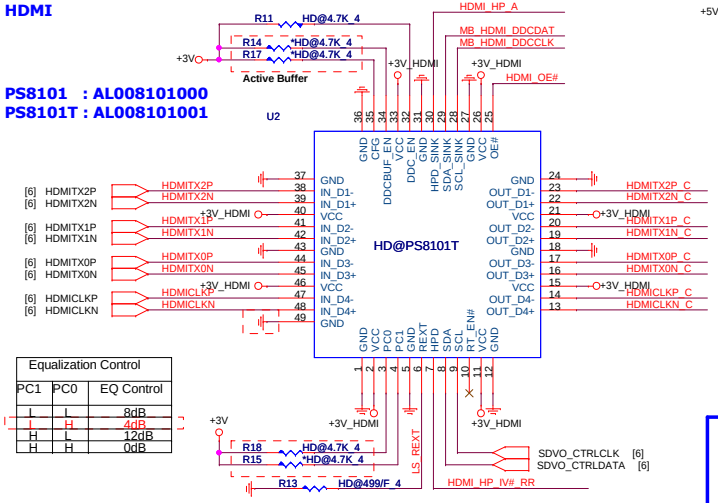


HDMI(HDM)

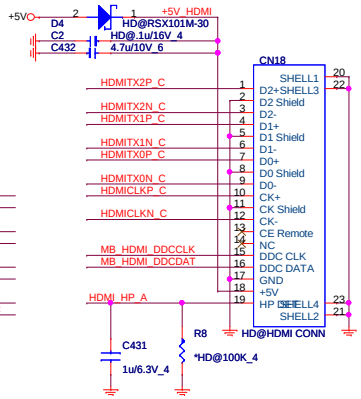


HDMI

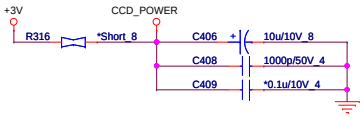
PS8101 : AL008101000
PS8101T : AL008101001



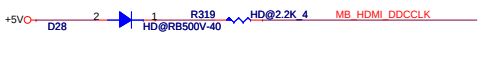
Equalization Control		
PC1	PC0	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

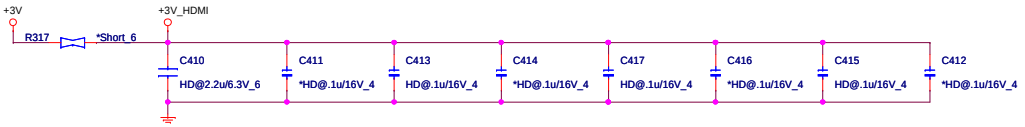


Camera(CCD)

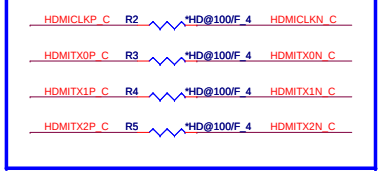


SDVO I2C Control

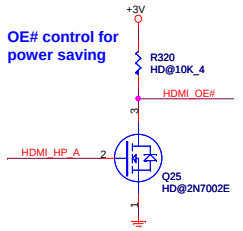




FOR EMI



OE# control for power saving



QUANTA COMPUTER

Title: LED Panel/CCD/HDMI

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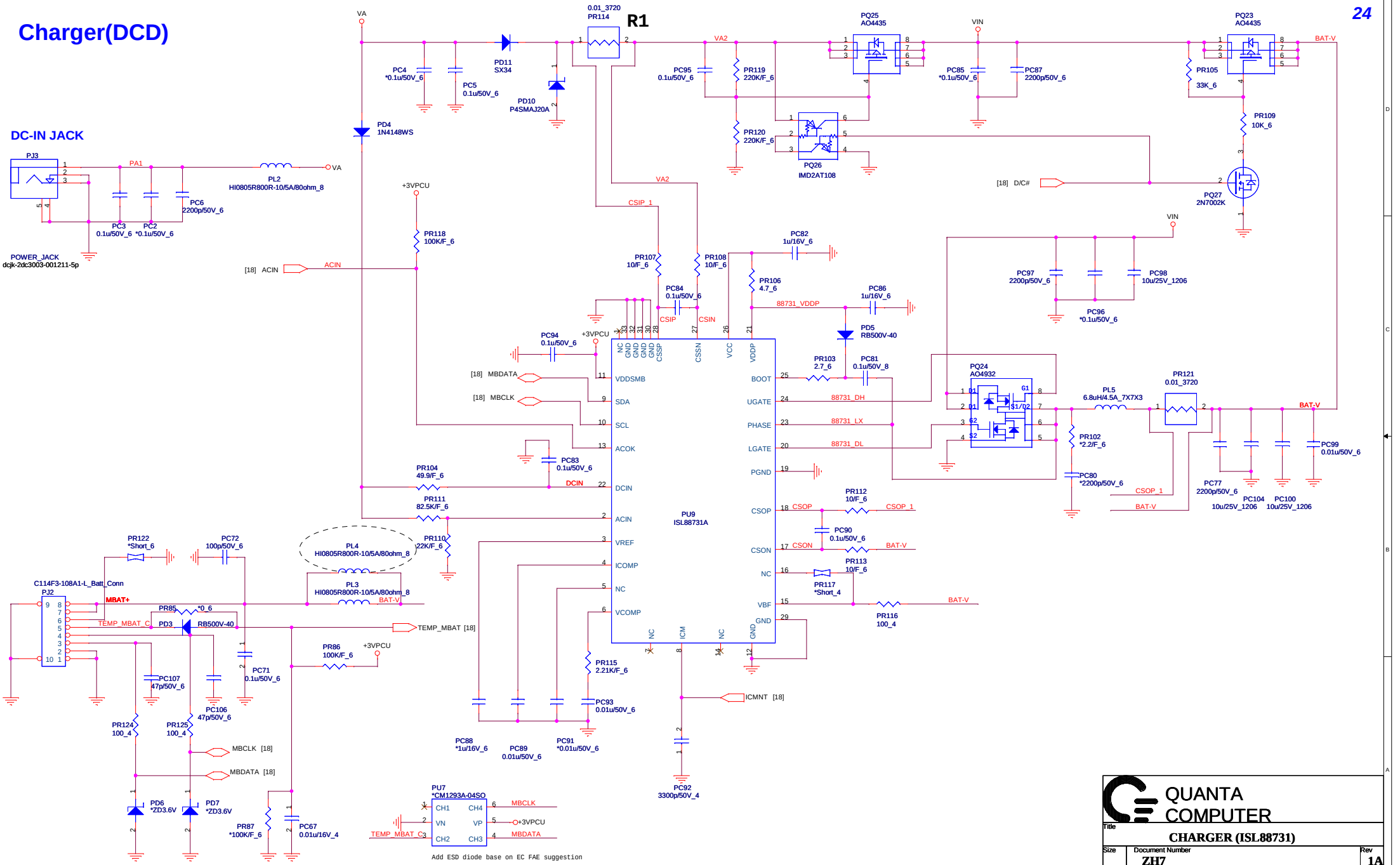
Charger(DCD)

DC-IN JACK



QUANTA COMPUTER

Title	CHARGER (ISL88731)	
Size	Document Number: ZH7	Rev: 1A
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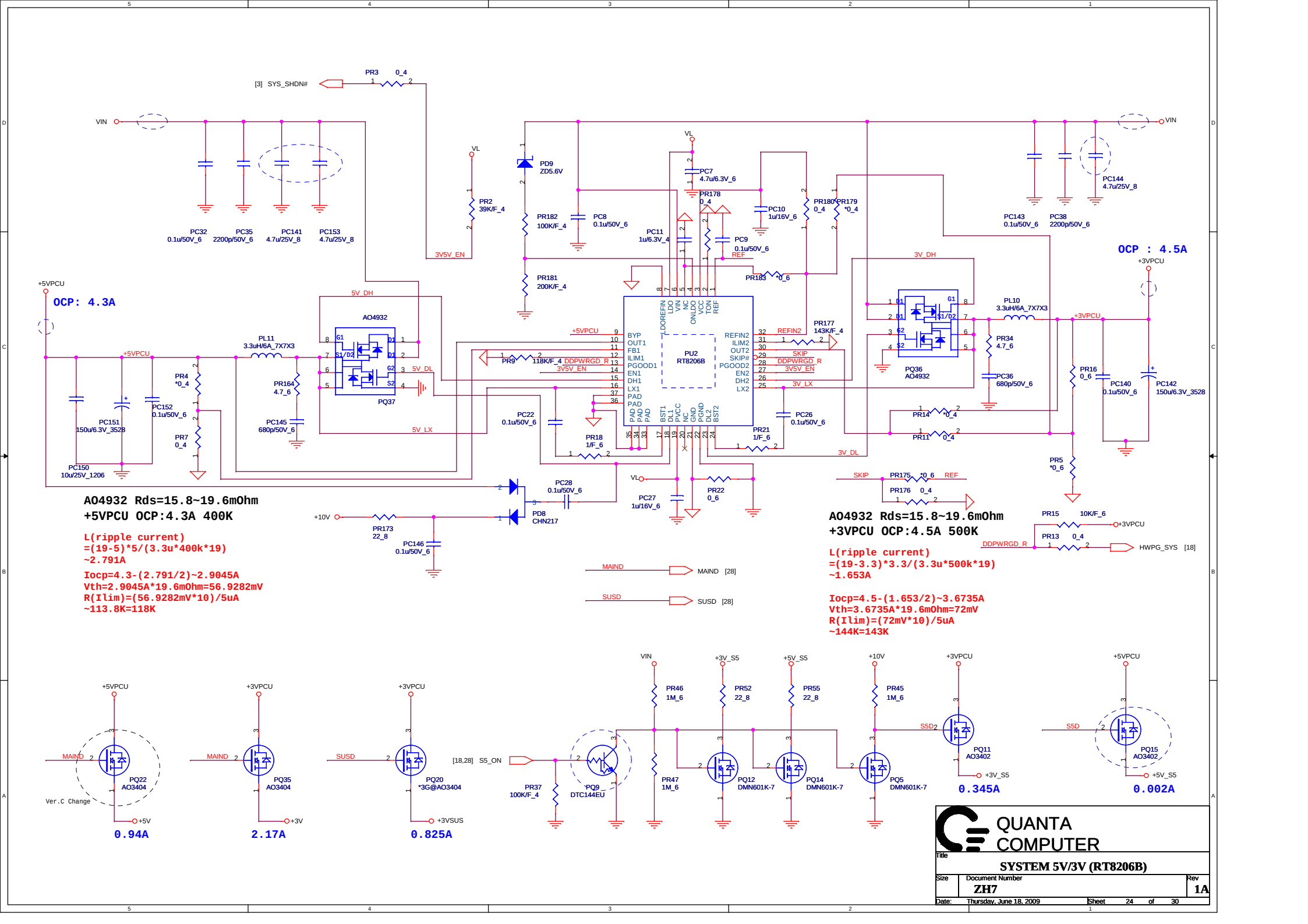

QUANTA COMPUTER

Title	SYSTEM 5V/3V (RT8206B)	
Size	Document Number: ZH7	Rev: 1A
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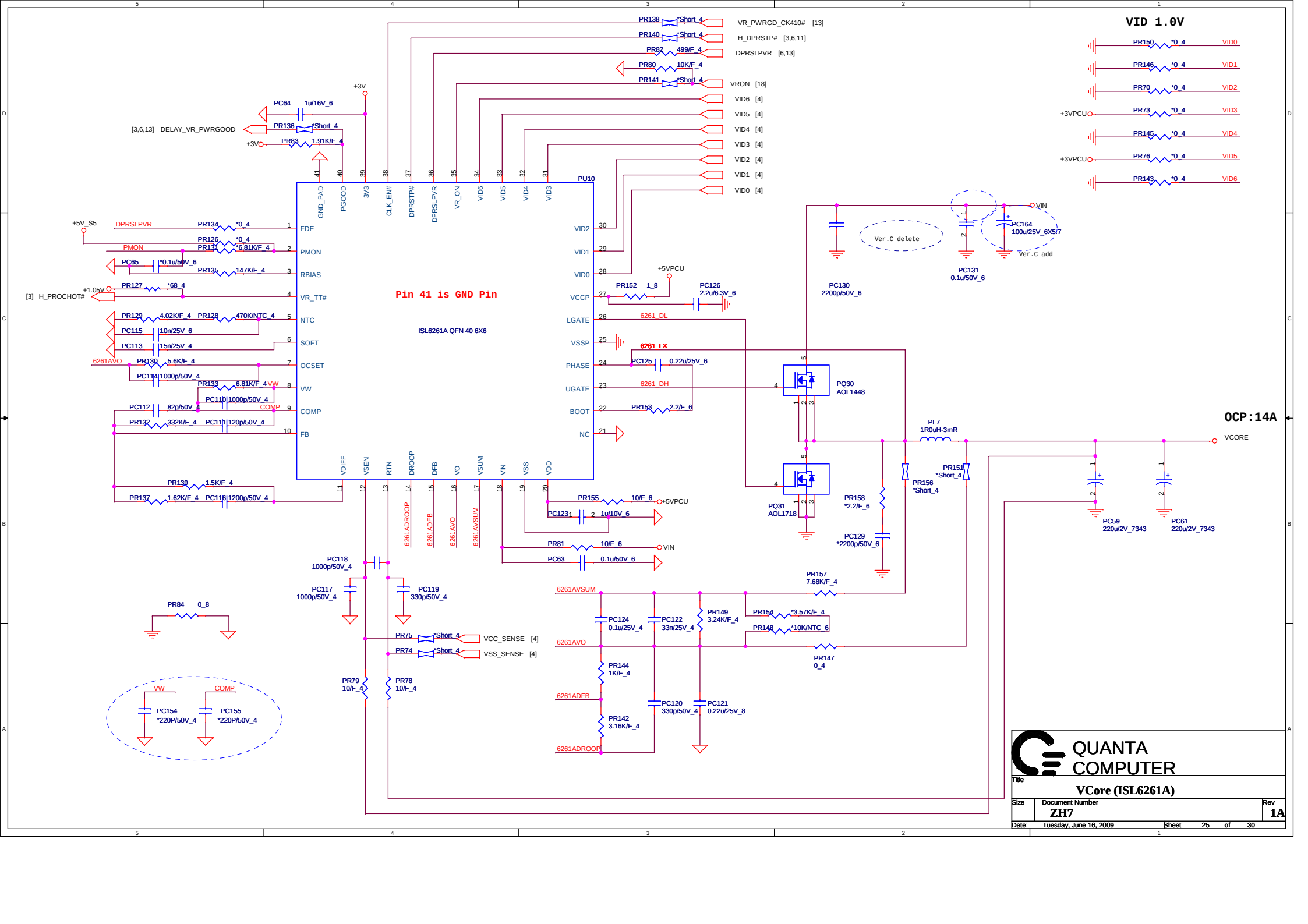
VID 1.0V
OCP:14A
Pin 41 is GND Pin
ISL6261A QFN 40 6X6
PU10
GND_PAD
PGOOD
3V3
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
FDE
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
VID2
VID1
VID0
VCCP
LGATE
VSSP
PHASE
UGATE
BOOT
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VSS
VDD
PQ30 AOL1448
PQ31 AOL1718
PL7 1R0uH-3mR
VCORE
VIN
+5VPCU
+3V
+5V_S5
+1.05V
6261AVO
6261ADROOP
6261ADFB
6261AVSUM
6261_DL
6261_DH
6261_LX
VCC_SENSE [4]
VSS_SENSE [4]
DELAY_VR_PWRGOOD [3,6,13]
H_PROCHOT# [3]
VR_PWRGD_CK410# [13]
H_DPRSTP# [3,6,11]
DPRSLPVR [6,13]
VRON [18]
Ver.C delete
Ver.C add
QUANTA COMPUTER
VCore (ISL6261A)
ZH7
1A
Tuesday, June 16, 2009
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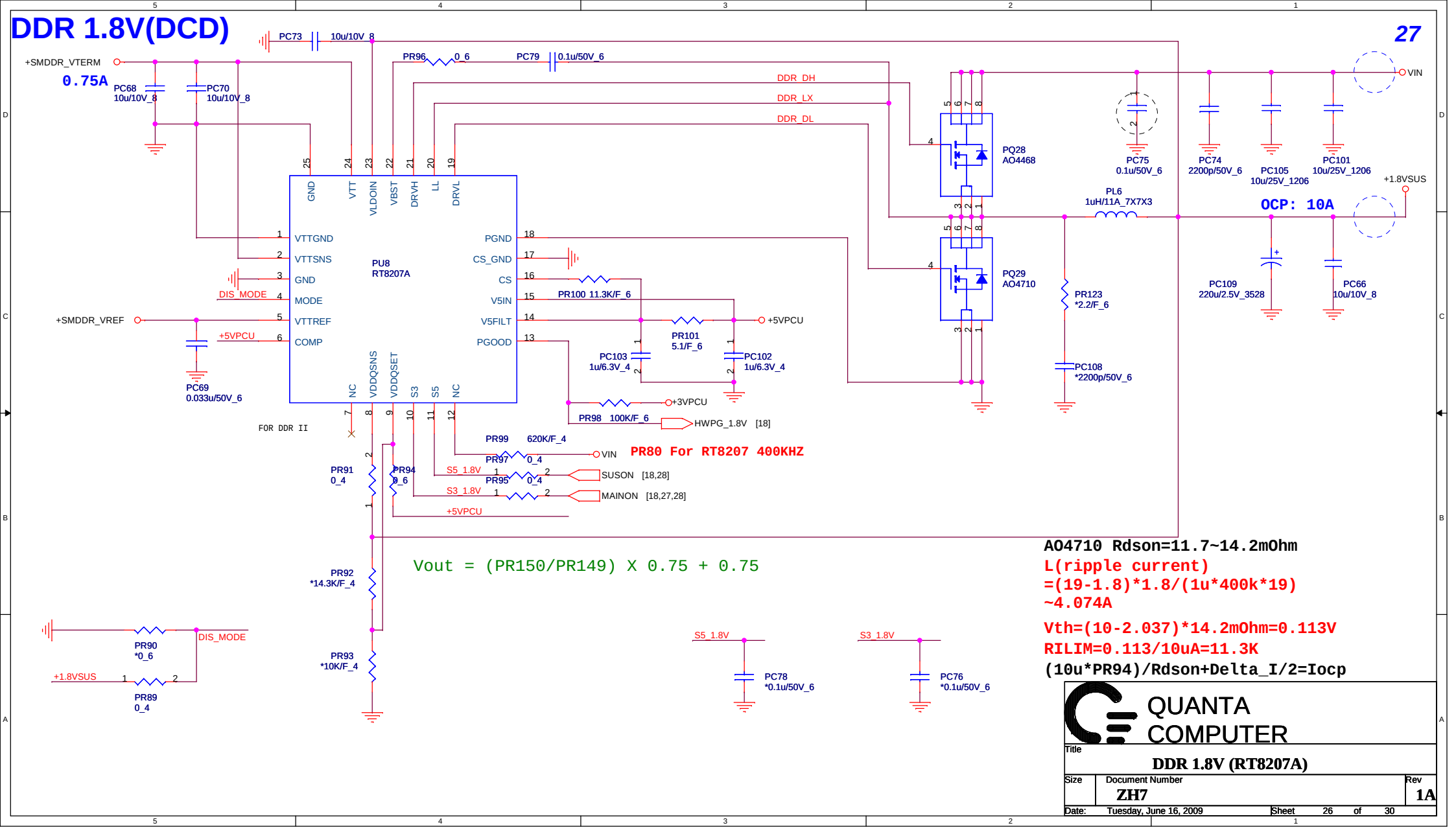
DDR 1.8V(DCD)



Vout = (PR150/PR149) X 0.75 + 0.75

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.8)*1.8/(1u*400k*19)
~4.074A

Vth=(10-2.037)*14.2mOhm=0.113V

RILIM=0.113/10uA=11.3K

(10u*PR94)/Rdson+Delta_I/2=Iocp

QUANTA COMPUTER

Title: DDR 1.8V (RT8207A)		
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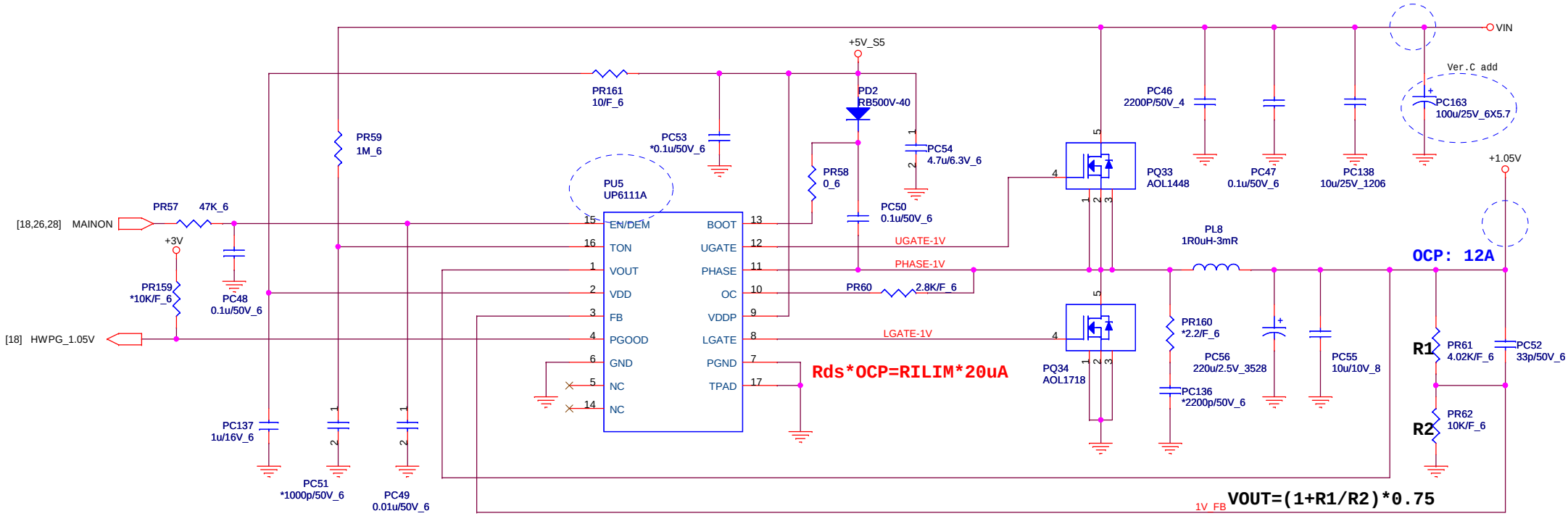


TON=3.85p*RTON*Vout/(Vin-0.5)

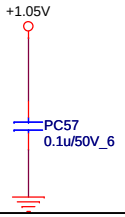
Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1412 Rdson=4.6mOhm
OCP=16-0.8A
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA
RILIM=2.76K--- 2.8K



QUANTA COMPUTER

Title: VCCP 1.05V (RT8202A)		
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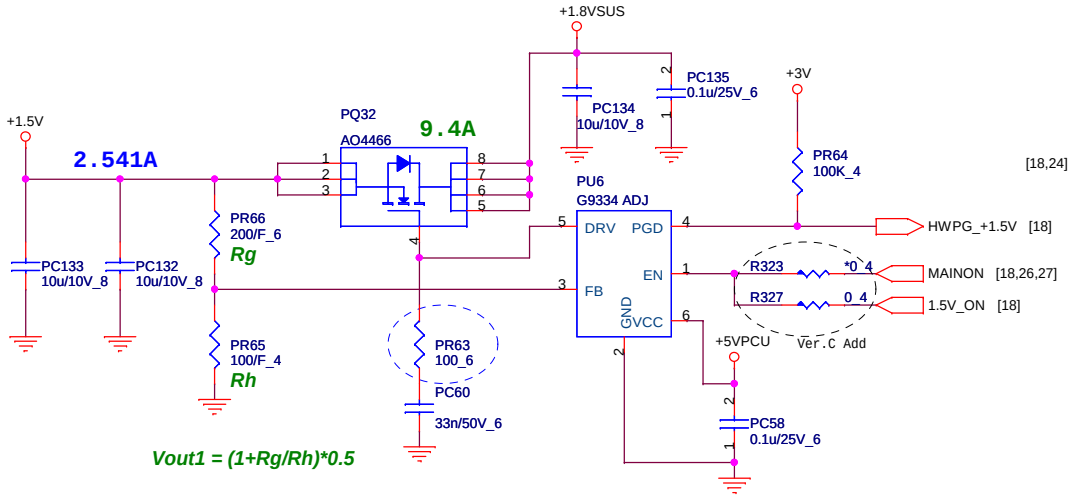
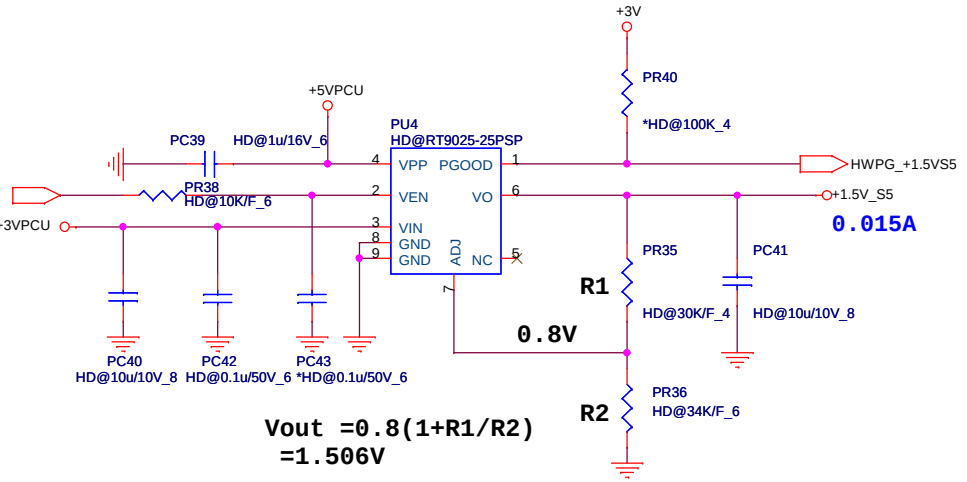
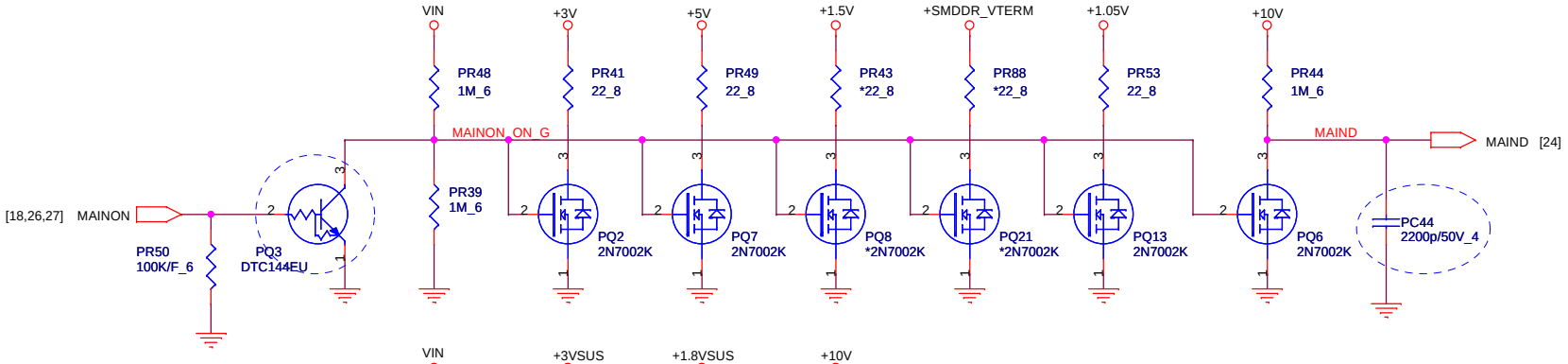
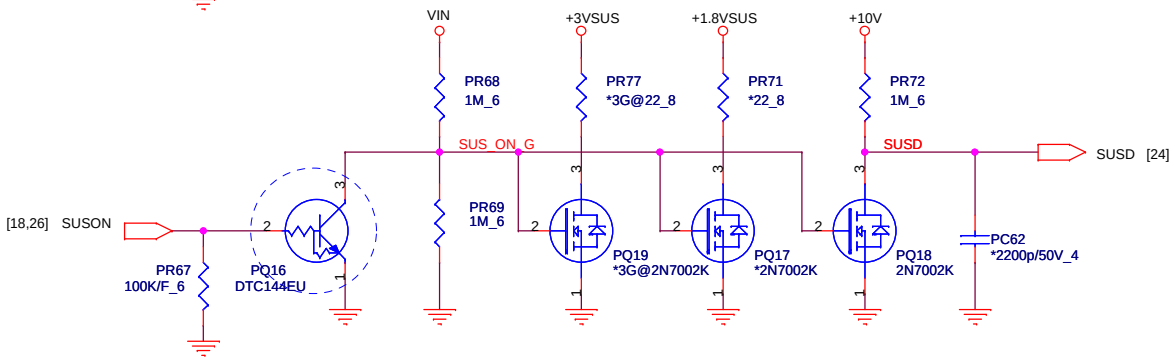
Discharger/1.5V(DCD)









QUANTA COMPUTER

Title: Discharge/1.5V		
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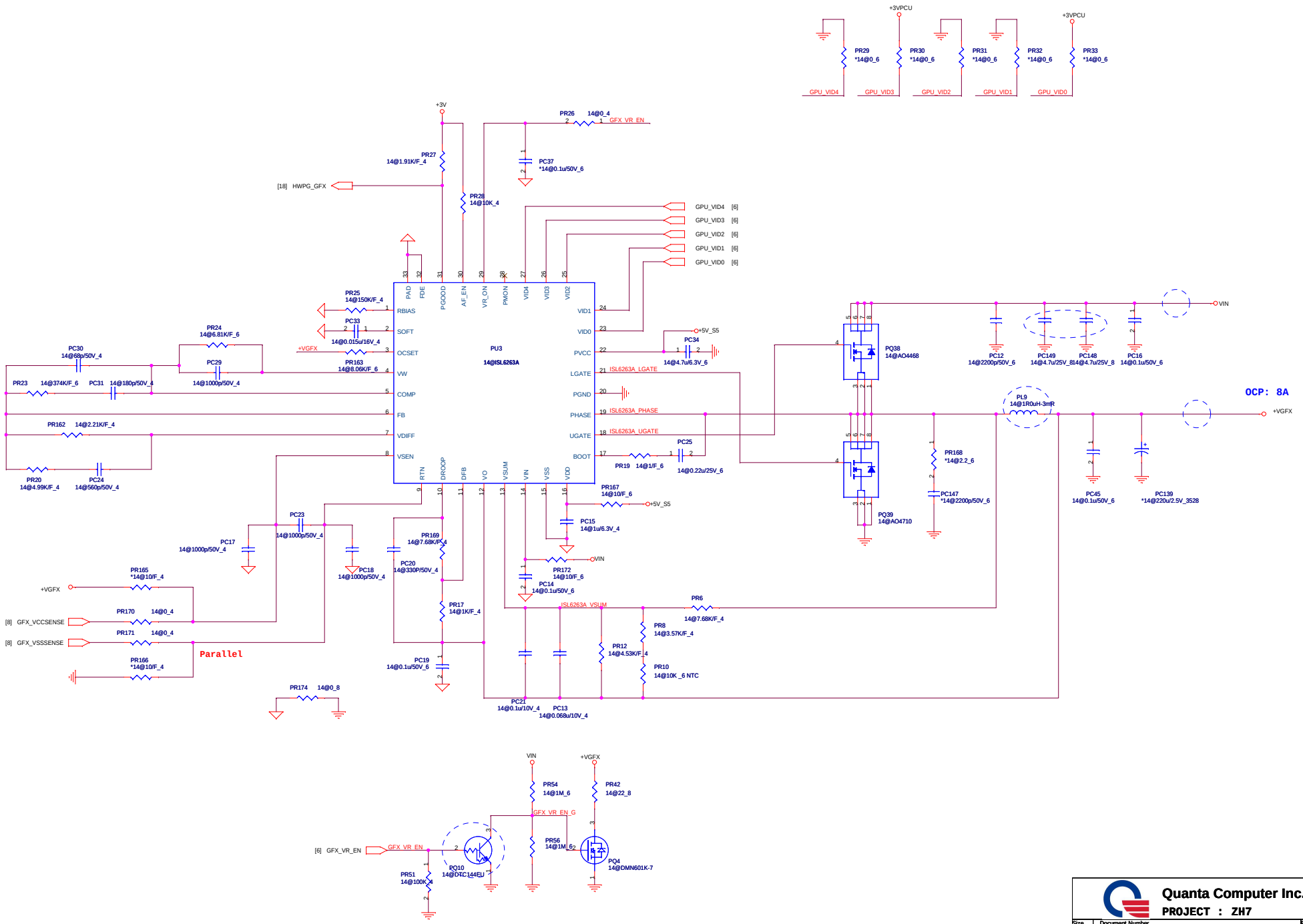

Quanta Computer Inc.

PROJECT : ZH7

Size	Document Number	Rev
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Model	REV	CHANGE LIST
ZH7 MB	1A	FIRST RELEASED: (PCB:A)
	2B	Page 2 : No Stuff R162 FOR EMI Page11 : Remove R282 ,R36 & R39 Page11 : Change CN14 footprint. Page14 : Remove D7 Page17 : Change Q15 frome 2N7002 to DTC144EU for speaker funcation. Page17 :Stuff U15, R244 & R227 , No stuff L23 for audio noisy. Page18 : Add R324 Page18 : Add R323 Page19 : Add R325 and short to CN11.44 for 3G LED function Page19 : Remove 3G wake up funcation ,Remove R179 , R183 & U11 Page20 : CN9 Change pin define.(CONN. reverse) Page 9 ,13 ,17 ,22 ,23 &25 : R116 ,R269 ,R74 ,R92 ,C330 ,C349 ,R211 ,R220 ,R231 ,R243 ,R248 &R317 Change to short pad Page 18 : D5 ,D20 & D13 Change footprint. Page 29 : PL9 Change footprint. Page 3 : R142 Change footprint. Page 25 : PU10 Change footprint. Page 11 : CN14 Change footprint. Page 21 : CN4 Change footprint.
	3C	Page 17 ,20 ,21 & 22 : R186 ,R187 ,R188 ,R189 ,R241 ,R196 ,R315 ,R20 & R316 Change to short pad Page 18 : Add R321 for ESD(Vedor suggest) Page 18 : D21 connect to HWPG_GFX Page 18 : D29 replace by R323. Page 20 : DEL R6 ,R7 & L2 Page 21 : CN2 connect to 3G_MINI2_LED meet customer request. and add C430 for EMI Page 22 : CN3.21 Change to floating Page 25 : page25 Delete PC127;PC128 10uf/25V_1206 and add PC164 100uF/25V 6x5.7 Page 27 : Add PC163 100uF/25V 6x5.7 Page 28 : Add R323 and R327
	1D	

MODEL	ZH7 FROM	ZH7 To
	X	1A
	X	1A
	1A	2A
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	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

Quanta Computer Inc.
PROJECT : ZH7

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	PART NUMBER:		DRAWING BY:		REVISON:	1A

EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwer switch in
GPIO4/AD5		GPI	No used
GPIO5/AD4		GPI	No used
GPIO6	LID#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#		GPI	No used
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDAT3	KILL_SW_BT#	GPI	Detect bule tooth enable/disable
GPIO13/C_PWM	PWRLED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX		GPI	No used
GPIO17/SCL1	MBCLK	O	SMBus Clock for M/B
GPIO20/TA2		GPI	No used
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SCL3	3ND_MBCLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBACK#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2		GPI	No used
GPIO27/PSDAT2	BT_POWERON#	GPO	Turn On/Off bule tooth power
GPIO30/CIRTX2		GPI	No used
GPIO31/SDA3	3ND_MBDATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED0#	GPO	Battery status LED drive
GPIO33/H_PWM	BATLED1#	GPO	Battery status LED drive
GPIO34/CIRRXL		GPI	No used
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO41	3G_WAKE_2	GPI	3G wake up
GPIO42/TCK		GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplier
GPIO44/TDI		GPI	No used
GPIO45/E_PWM	CPUFAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#	3G_WAKE_1	GPI	3G wake up
GPIO47/SCL4		GPI	No used
GPIO50/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	PCIE_WAKE#_EC	GPI	No used
GPIO53/SDA4	EC_SCI#	O	EC SCI
GPIO54/ECSCI#	ECDB_CLOCK	GPI	No used
GPIO55/CLKOUT	ECDB_CLOCK	GPI	No used
GPIO56/TA1		GPI	No used
GPIO57/KBSOUT17	KILL_SW_WL#	GPI	Detect mini card 1 (WLAN) enable/diable
GPIO60/KBSOUT16	KILL_SW_3G#	GPI	Detect mini card 2 (3G) enable/diable
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SMI#	EC_SMI#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USB_EN#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWROK_EC	GPO	System Power Good for PCI Reset
GPIO72/IRRX1/SIN2	EC_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SCL2	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SPI_SCK	PCI_RESET	GPO	PLTRST# enable/diable for mini card 2
GPIO76/SPI_DO/SHBM	3G_EN	GPO	Mini card 2 (3G) enable/disable
GPIO77/SPI_DI	CRT_SENSE#	GPI	To detect CRT
GPIO81	DNBSWON#	GPO	S.B Power button Event
GPIO82/TRIS#		GPI	No used
GPIO83/SOUT_CR/BADDR1	uR_SOUT_CR	GPI	No used (Address Setting)
GPIO84/BADDR0	BADDR0	GPI	No used (Address Setting)
GPIO87/CIRRRXM/SIN_CR	RF_EN	GPO	Mini card 1 (WLAN) enable/disable
GPIO90/AD0	TEMP_MBAT	I	EC detect battery state
GPIO91/AD1		GPI	No used
GPIO92/AD2	TPD_TRIP	GPI	No used
GPIO93/AD3	ICMNT	I	EC detect system current in AC mode
GPIO94/DA0		GPI	No used
GPIO95/DA1		GPI	No used
GPIO96/DA2		GPI	No used
GPIO97/DA3		GPI	No used

ICH9M GPIO Setting

Pin Name	Power	ICH9M Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0/PMSYNC#	Core	GPI	PM_SYNC#	Power Management Sync	O		
GPIO1	Core	GPI	EC_SMI#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2/PIRQE#	Core	GPI	INTE#	No used	GPI		PU 10KΩ to +3V
GPIO3/PIRQF#	Core	GPI	INTF#	No used	GPI		PU 10KΩ to +3V
GPIO4/PIRQG#	Core	GPI	INTG#	No used	GPI		PU 10KΩ to +3V
GPIO5/PIRQH#	Core	GPI	INTH#	No used	GPI		PU 10KΩ to +3V
GPIO6	Core	GPI	LID#_ICH	Lid function	GPI		PU 10KΩ to +3V
GPIO7	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO8	S5	GPI	EC_SCI#	EC SCI interrupt	GPI		PU 10KΩ to +3V_S5
GPIO9/WOL_EN	S5	Native	ICH_GPIO9	No used	GPI		PU 10KΩ to +3V_S5
GPIO10/SUS_PWR_ACK	S5	GPI	ICH_GPIO10	No used	GPI		PU 10KΩ to +3V_S5
GPIO11/SMBALERT#	S5	Native	ICH_GPIO11	No used	GPI		PU 10KΩ to +3V_S5
GPIO12/LAN_PHY_PWR_CTRL	S5	GPO	ICH_GPIO12	No used	GPI		PU 10KΩ to +3V_S5
GPIO13	S5	GPI	ICH_GPIO13	No used	GPI		PU 10KΩ to +3V_S5
GPIO14/AC_PRESENT	S5	GPI	ICH_GPIO14	No used	GPI		PU 10KΩ to +3V_S5
GPIO15/STP_PCI#	S5	Native	PM_STPPCI#	Stop PCI Clock	O		
GPIO16/DPRSLPVR	Core	Native	DPRSLPVR	Deeper Sleep-Voltage Regulator	O	PD 20KΩ	
GPIO17	Core	GPI	BORAD_ID0	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO18	Core	GPO	BORAD_ID1	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO19/SATA1GP	Core	GPI	ICH_GPIO19	No used	GPI		PU 10KΩ to +3V
GPIO20	Core	GPO		No used	GPO	PD 20KΩ	
GPIO21/SATA0GP	Core	GPI	BORAD_ID2	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO22/SCLOCK	Core	GPI	BORAD_ID3	M/B ID Setting	GPI		PU or PD 10KΩ
GPIO23/LDRQ1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO24/MEM/LED	S5	GPO		No used	GPO		
GPIO25/STP_CPU#	S5	Native	PM_STPCPU#	Stop CPU Clock	O		
GPIO26/S4_STATE#	S5	Native		No used	GPO		
GPIO27	S5	GPO		No used	GPO		
GPIO28	S5	GPO		No used	GPO		
GPIO29/OC5#	S5	Native	USBOC5#	No used	GPI		PU 10KΩ to +3V_S5
GPIO30/OC6#	S5	Native	USBOC6#	No used	GPI		PU 10KΩ to +3V_S5
GPIO31/OC7#	S5	Native	USBOC7#	No used	GPI		PU 10KΩ to +3V_S5
GPIO32/CLKRUN#	Core	GPO	CLKRUN#	PCI Clock Run	I		PU 8.2KΩ to +3V
GPIO33/HDA_DOCK_EN#	Core	GPO		No used	GPO	PU 20KΩ	
GPIO34/HDA_DOCK_RST#	Core	GPO		No used	GPO		
GPIO35/SATACLKREQ#	Core	GPO	CLKREQ#_SATA	SATA Clock Request	O		PU 10KΩ to +3V
GPIO36/SATA4GP	Core	GPI	ICH_GPIO36	No used	GPI		PU 10KΩ to +3V
GPIO37/SATA5GP	Core	GPI	ICH_GPIO37	No used	GPI		PU 10KΩ to +3V
GPIO38/SLOAD	Core	GPI	ICH_GPIO38	No used	GPI		PD 10KΩ to GND
GPIO39/SDATAOUT0	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO40/OC1#	S5	Native	USBOC1#	No used	GPI		PU 10KΩ to +3V_S5
GPIO41/OC2#	S5	Native	USBOC2#	No used	GPI		PU 10KΩ to +3V_S5
GPIO42/OC3#	S5	Native	USBOC3#	No used	GPI		PU 10KΩ to +3V_S5
GPIO43/OC4#	S5	Native	USBOC4#	No used	GPI		PU 10KΩ to +3V_S5
GPIO44/OC8#	S5	Native	USBOC8#	No used	GPI		PU 10KΩ to +3V_S5
GPIO45/OC9#	S5	Native	USBOC9#	No used	GPI		PU 10KΩ to +3V_S5
GPIO46/OC10#	S5	Native	USBOC10#	No used	GPI		PU 10KΩ to +3V_S5
GPIO47/OC11#	S5	Native	USBOC11#	No used	GPI		PU 10KΩ to +3V_S5
GPIO48/SDATAOUT1	Core	GPI		No used	GPI		PU 10KΩ to +3V
GPIO49	Core	GPO	DMI_TERM_SEL	No used	GPO	PU 20KΩ	
GPIO50/REQ1#	Core	Native	REQ1#	No used	GPI		PU 10KΩ to +3V
GPIO51/GNT1#	Core	Native		No used	GPI	PU 20KΩ	
GPIO52/REQ2#	Core	Native	REQ2#	No used	GPI		PU 10KΩ to +3V
GPIO53/GNT2#	Core	Native		No used	GPI	PU 20KΩ	
GPIO54/REQ3#	Core	Native	REQ3#	No used	GPI		PU 10KΩ to +3V
GPIO55/GNT3#	Core	Native		No used	GPI	PU 20KΩ	
GPIO56	S5	GPI	ICH_GPIO56	No used	GPI		PU 10KΩ to +3V_S5
GPIO57	S5	GPI	ICH_GPIO57	No used	GPI		PD 100KΩ to GND
GPIO58/SPI_CS1#	S5	GPI	SPI_CS1#	No used	GPI	PU 20KΩ	
GPIO59/OC0#	S5	Native	USBOC0#	No used	GPI		PU 10KΩ to +3V_S5
GPIO60/LINKALERT#	S5	Native	ICH_GPIO60	No used	GPI		PU 10KΩ to +3V_S5

CK505 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	
CPU_0#	60	CLK_CPU_BCLK#	Differential CPU clock
CPU_1	58	CLK_MCH_BCLK	
CPU_1#	57	CLK_MCH_BCLK#	Differential NB GS45 clock

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOT96	20	DREFCLK	
SRC0#/DOT96#	21	DREFCLK#	96MHz DOT clock for NB GS45
LCDCLK/27M	24	DREFSSCLK	
LCDCLK#/27M_SS	25	DREFSSCLK#	Clock output for NB GS45 graphic contoller
SRC2	28	PECLK_SATA	
SRC2#	29	PECLK_SATA#	Differential Serial Reference Clock for SB ICH9M SATA
SRC3/CR#_C	31	PECLK_ICH	
SRC3#/CR#_D	32	PECLK_ICH#	Differential Serial Reference Clock for SB ICH9M
SRC4	34	PECLK_LAN	
SRC4#	35	PECLK_LAN#	Differential Serial Reference Clock for on board LAN
SRC6	48	PECLK_MINI2	
SRC6#	47	PECLK_MINI2#	Differential Serial Reference Clock for Mini Card 2
SRC7/CR#_F	51		No use
SRC7#/CR#_E	50	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8/CPU_ITP	54		
SRC8#/CPU_ITP#	53		No use
SRC9	37	PECLK_MINI1	
SRC9#	38	PECLK_MINI1#	Differential Serial Reference Clock for MINI CARD 1
SRC10	41	PECLK_3GPLL	
SRC10#	42	PECLK_3GPLL#	Differential Serial Reference Clock for NB GS45
SRC11/CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#/CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0/CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1/CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_48	17	CLK48_ICH	48MHz for SB ICH9M
		CLK48_CARD	48MHz for USB Card Reader
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table

CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

QUANTA COMPUTER

Title: **Schematic Setting**

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