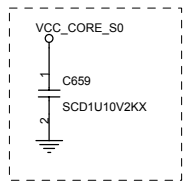
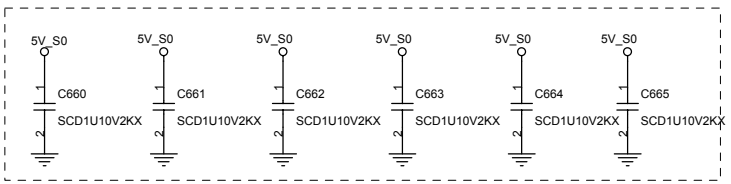
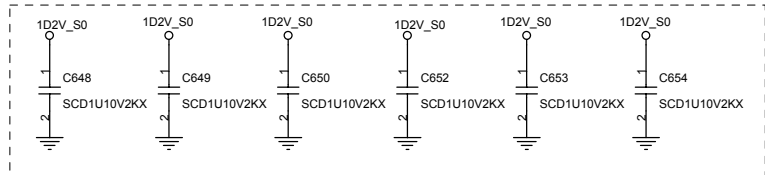
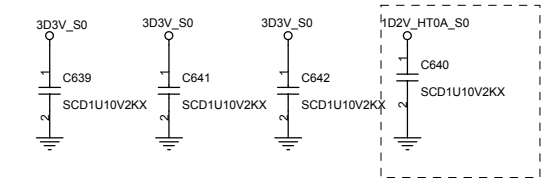
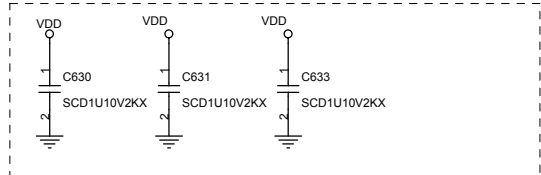
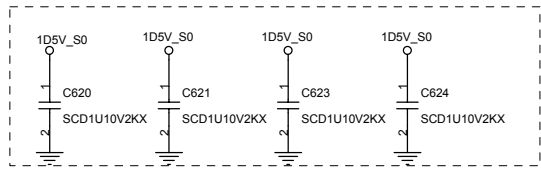
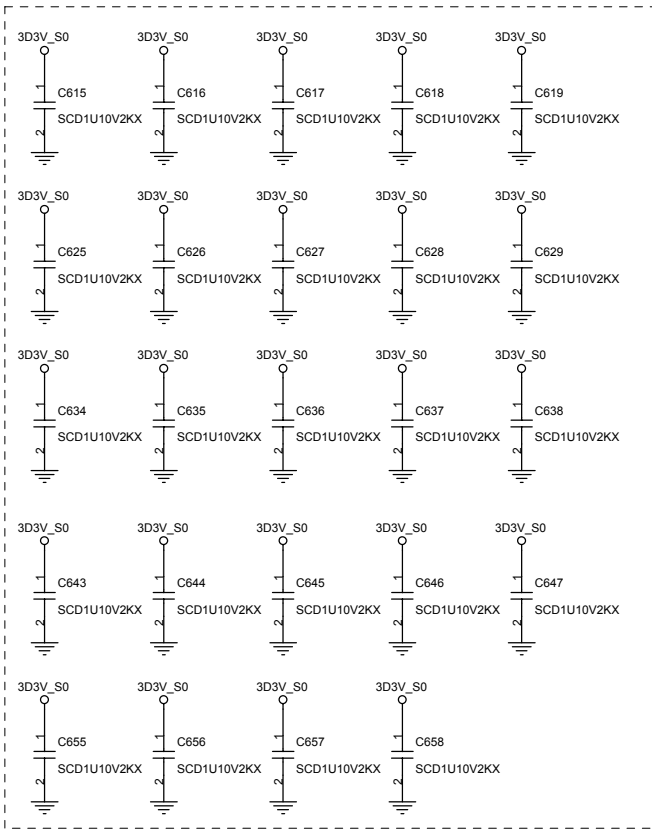


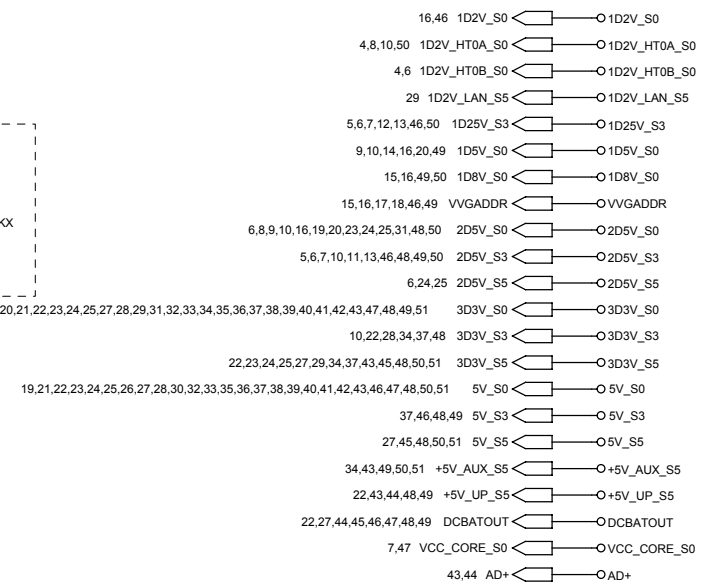
J8 REVISION HISTORY

6/12 EMI Bypass Cap.



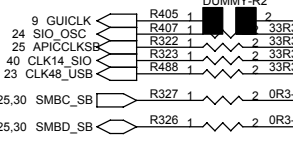
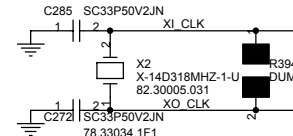
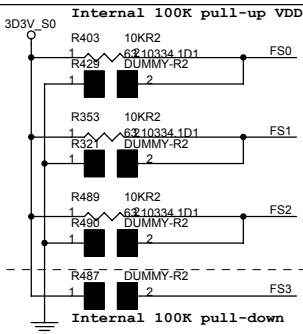
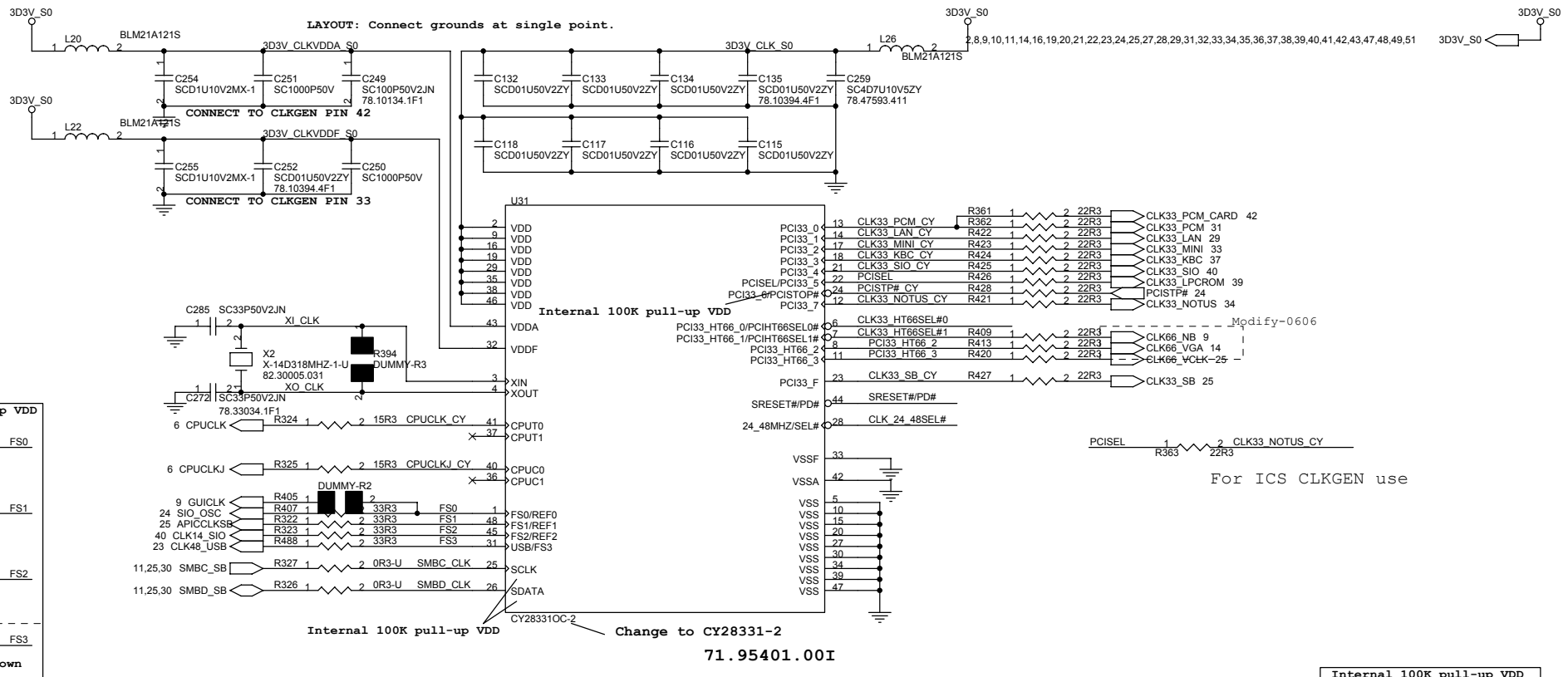
PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ#/GNT#
Mini-PCI	AD21	P_INTF#	P_REQ#0/P_GNT#0
R5C554-CardBus A	AD22	P_INTB#	P_REQ#1/P_GNT#1
R5C554-CardBus B	AD22	P_INTC#	P_REQ#1/P_GNT#1
R5C554-IEEE 1394	AD22	P_INTD#	P_REQ#1/P_GNT#1
VGA-ATI M10-P		P_INTA#	
BCM-5705M	AD23	P_INTE#	P_REQ#2/P_GNT#2



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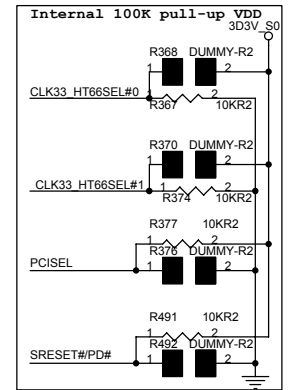
Title			REVISION HISTORY		
Size	Document Number				Rev
A3	GANNET				-1
Date:	Thursday, December 04, 2003	Sheet	2	of	51



Input Configuration				Clock Generator Output				
FS3	FS2	FS1	FS0	PCI_HT#	CPU (MHz)	PCI33_HT66 (MHz)	PCI33 (MHz)	
0	0	0	0	X	Hi-Z	Hi-Z	Hi-Z	All output Tri-state
0	0	0	1	X	133.9	33.5 or 67.0	33.5	
0	0	1	0	X	166.9	33.4 or 66.8	33.4	
0	0	1	1	X	200.9	33.5 or 67.0	33.5	
0	1	0	0	X	100	33.3 or 66.7	33.3	
0	1	0	1	X	133.33	33.3 or 66.7	33.3	
0	1	1	0	X	166.66	33.3 or 66.7	33.3	
* 0	1	1	1	X	200	33.3 or 66.7	33.3	Normal Hammer operation
1	0	0	0	X	105.0	35.0 or 70.0	35.0	
1	0	0	1	X	110.0	36.7 or 73.3	36.7	
1	0	1	0	X	210.0	35.0 or 70.0	35.0	
1	0	1	1	X	240.0	30.0 or 60.0	30.00	
1	1	0	0	X	270.0	33.8 or 67.5	33.8	
1	1	0	1	X	233.3	27.2 or 58.3	27.2	
1	1	1	0	X	266.7	33.3 or 66.7	33.3	
1	1	1	1	X	300.0	37.5 or 75.0	37.5	

PCISEL	PIN22	24_48 SEL#	24_48MHz
0	PCI33_6	0	48MHz
1	PCISTOP#	1	24MHz

PCIHT66 SEL[1:0]#PCI33_HT66[3:0]					
SEL1	SEL0	PIN6	PIN7	PIN8	PIN11
0	0	HT66	HT66	HT66	HT66
0	1	HT66	HT66	HT66	PCI33
1	0	HT66	HT66	PCI33	PCI33
1	1	HT66	PCI33	PCI33	PCI33



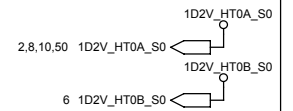
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Title: **CLKGEN_CY28331**

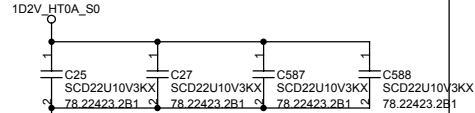
Size: A3 Document Number: **Gannet** Rev: -1

Date: Thursday, December 04, 2003 Sheet: 3 of 51

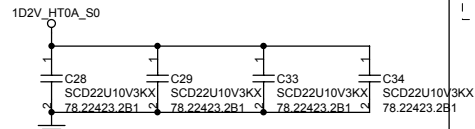
Clawhammer HT Interface



LAYOUT: Close to CPU within 1 inch
#24665 PG:135



Between CPU and NB

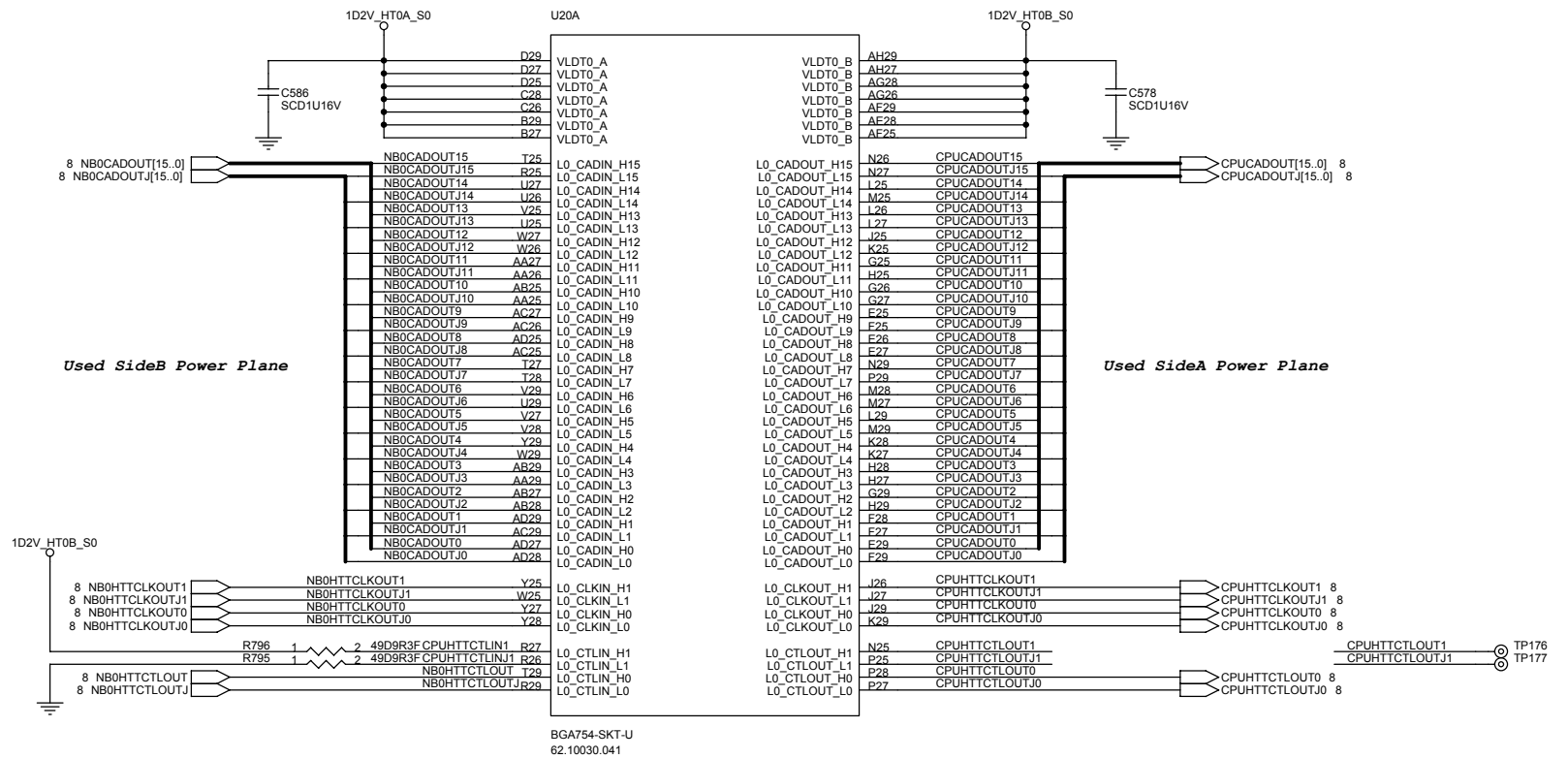
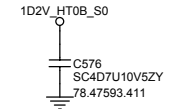


11/11 add SCD22U
For AMD suggest.

HTT for CPU sideA
Transmit power
and NB sideA Receive
power

HTT for CPU sideB
Receive power
and NB sideA
Transmit power

LAYOUT: Place bypass cap on topside of board near
HTT power pins that are not connected directly to
downstream HTT device, but connected internally to
other HTT power pins.



BGA754-SKT-U
62.10030.041

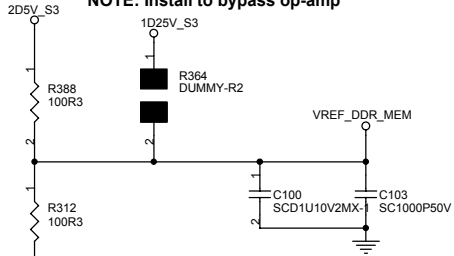
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Title			
CPU(1/4)_HyperTransport I/F			
Size	Document Number	Rev	
A3	Gannet	-1	
Date: Thursday, December 04, 2003			
Sheet		4	of
		51	

Clawhammer DDR Interface

VREF_DDR_MEM

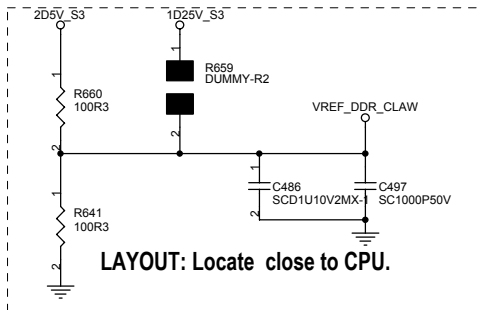
NOTE: Test with passive probes only.
NOTE: Install to bypass op-amp



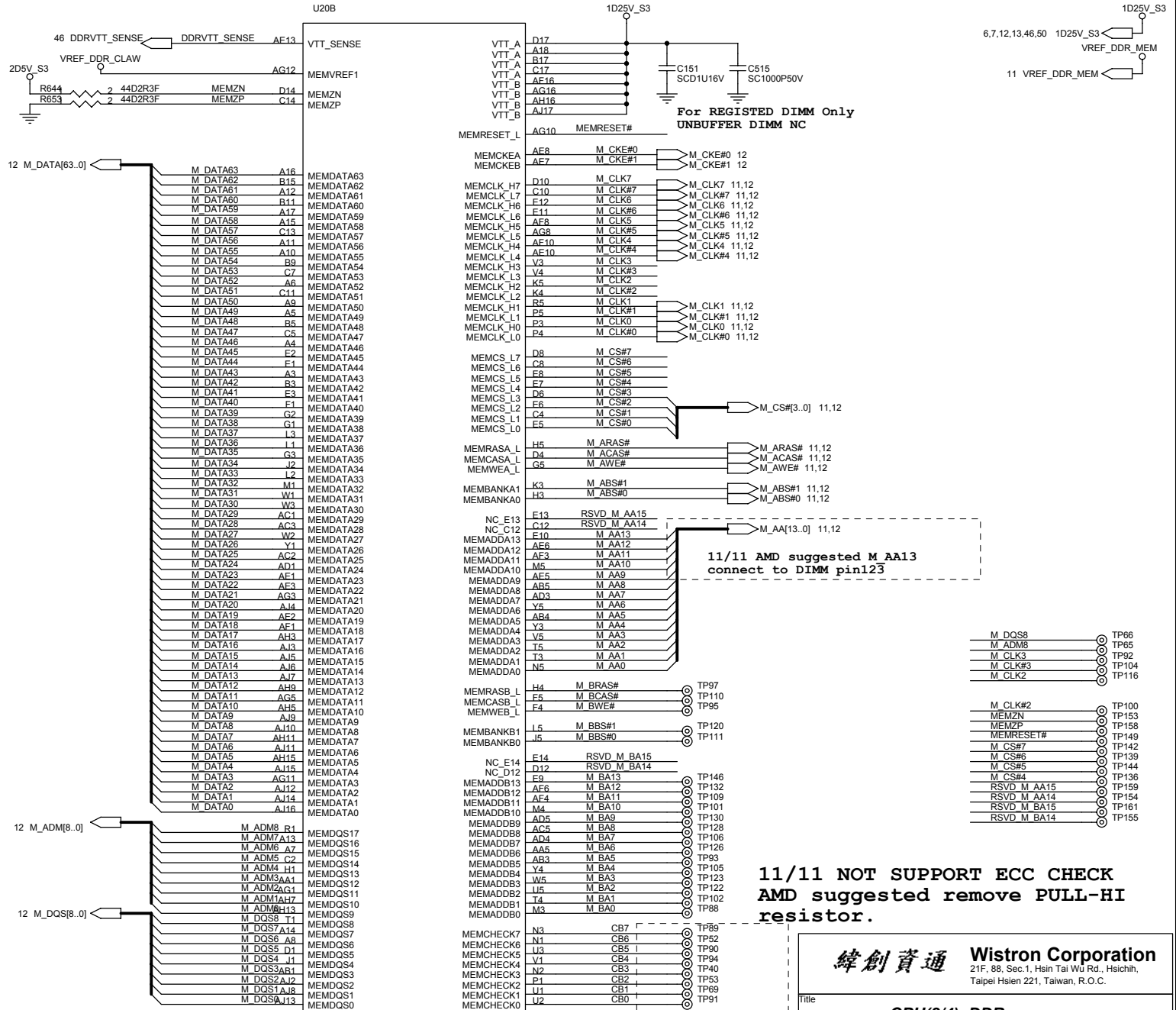
LAYOUT: Locate close to DIMMs.

NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



LAYOUT: Locate close to CPU.



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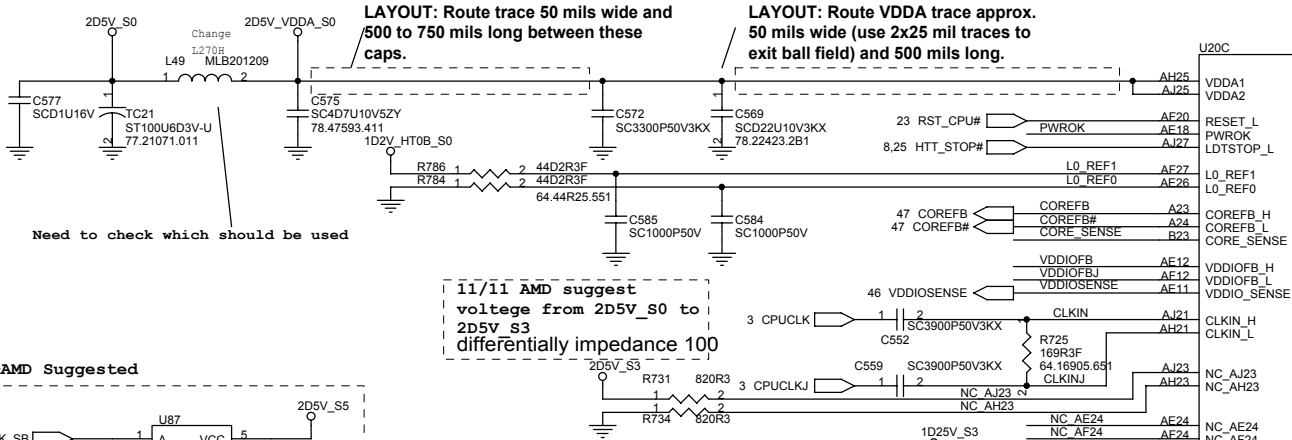
Title CPU(2/4)_DDR

Size A3 Document Number Gannet Rev -1

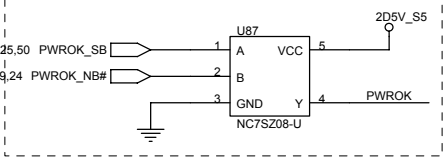
Date: Thursday, December 04, 2003 Sheet 5 of 51

Clawhammer Control and Debug

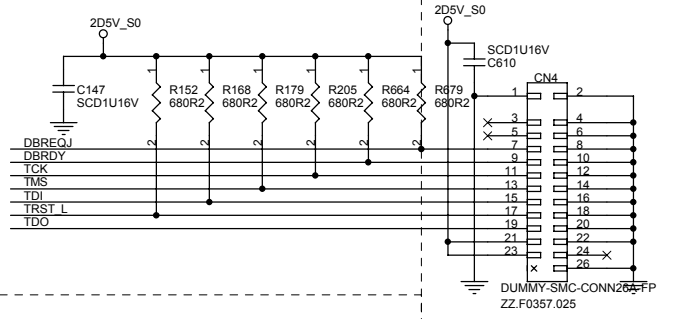
2D5V_VDDA_S0



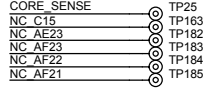
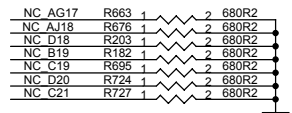
5/12-->AMD Suggested



HDT Connectors

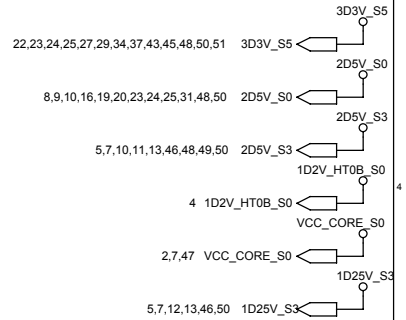
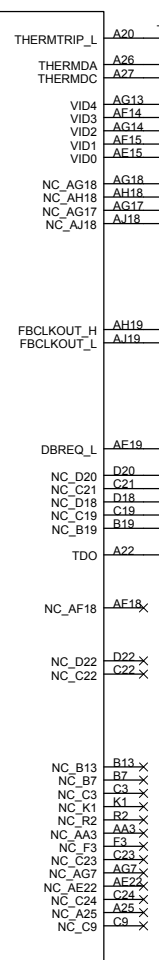
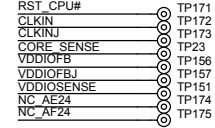


10/22 CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST

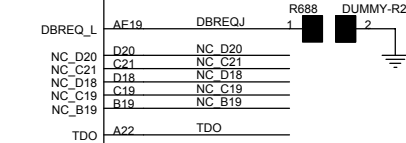
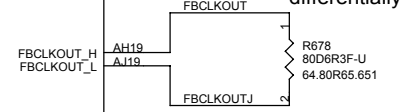


Validation Test Points

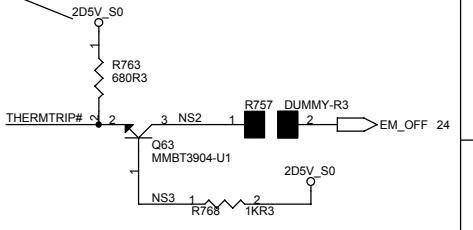
LAYOUT: Place close to the CPU.



LAYOUT: Route FBCLKOUT_H/L differentially impedance 80



10/22 CHANGE VCC FROM 2D5V_S3 TO 2D5V_S0



THERMTRIPJ Level shift to VT8235 EM_OFF PIN near VT8235

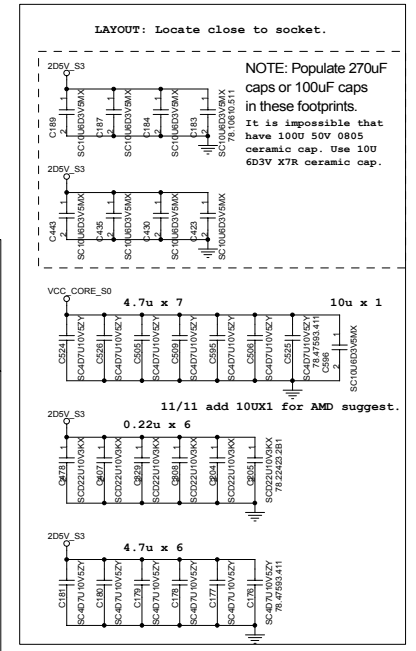
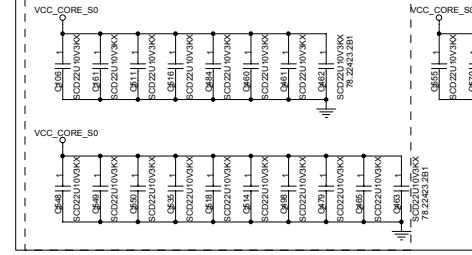
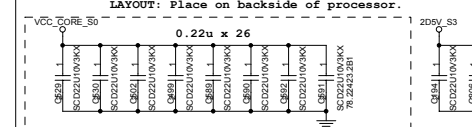
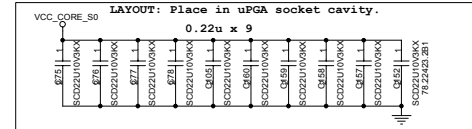
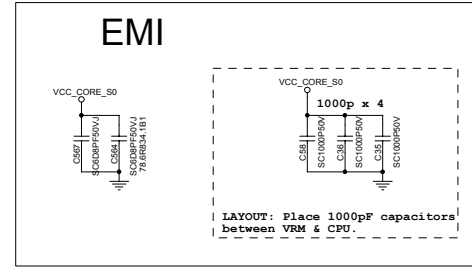
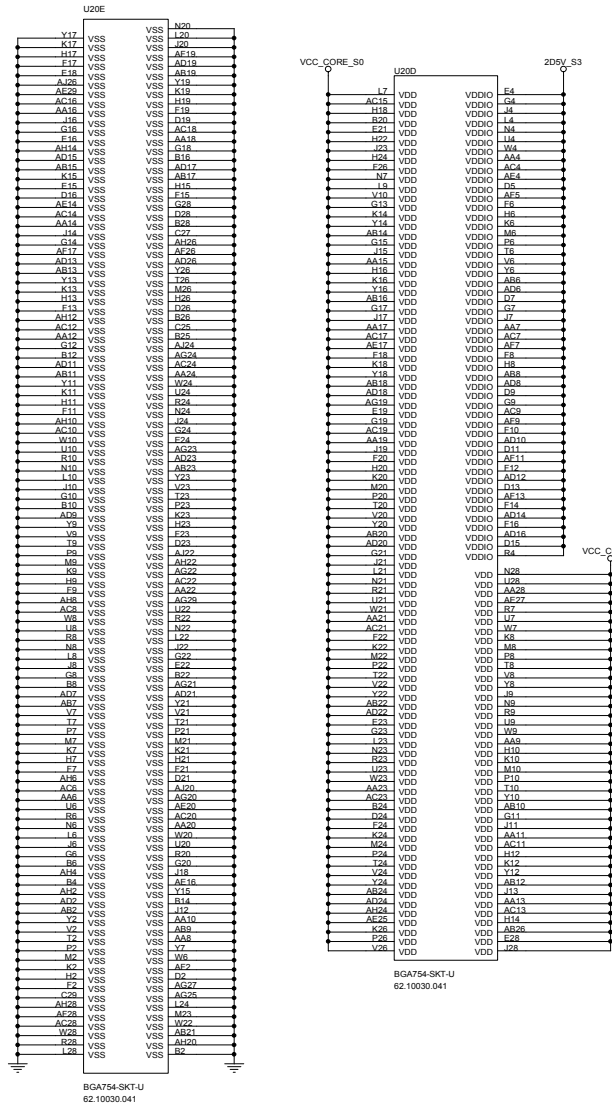
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Title: **CPU(3/4)_Control & Debug**

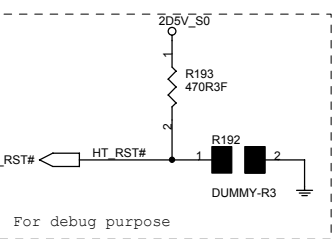
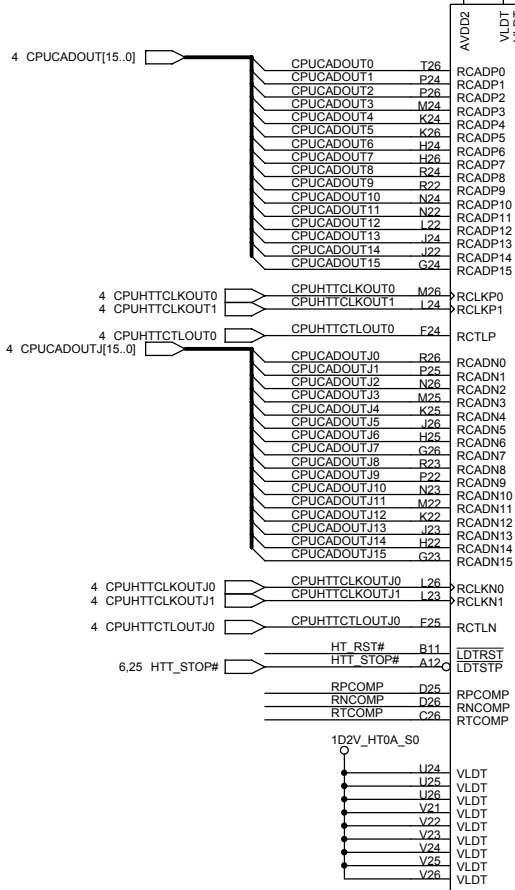
Size: A3 Document Number: **Gannet** Rev: -1

Date: Thursday, December 04, 2003 Sheet: 6 of 51

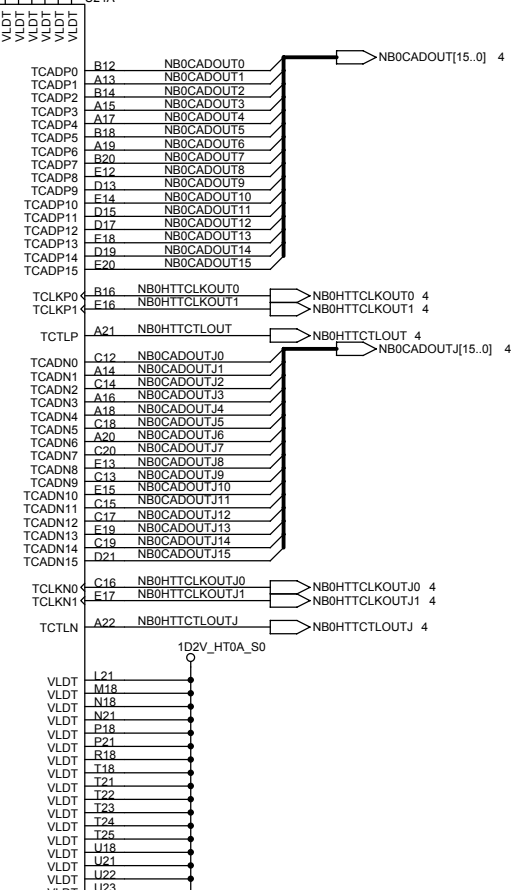
Clawhammer Power and Ground Connections



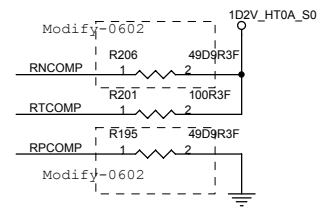
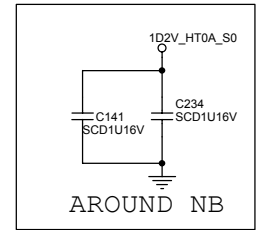
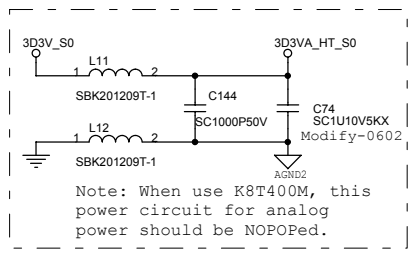
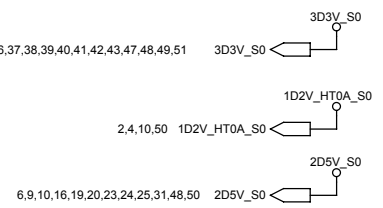
CLAW HAMMER TO NB



NB TO CLAW HAMMER



K8M400-VD7
71.K8T00.00U



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Title: **NB-K8T800M(1/3)_HT**

Size: A3	Document Number: Gannet	Rev: -1
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Date: Thursday, December 04, 2003 Sheet: 8 of 51

25 VLAD[7..0]

VLAD0 AD20
VLAD1 AD21
VLAD2 AD22
VLAD3 AF24
VLAD4 AE18
VLAD5 AF20
VLAD6 AD24
VLAD7 AF25

25 VBE# VBE# AE21
25 LPAR LPAR AF19

25 UPSTB UPSTB AF23
25 UPSTB# UPSTB# AF23

25 DNSTB DNSTB AF22
25 DNSTB# DNSTB# AD22

25 UPCMD UPCMD AF26
25 DNCMD DNCMD AD23

VL_VREF AF21
LVREF

6,24 PWROK_NB# AE26
PWRGD

23 RST_NB# AC25
PCIRST

14,24 PM_SUS_STAT# AC26
TESTIN

DEBUG AC17
SUSTAT

CRT_A/R B3
CRT_A/G A3
CRT_A/B A2

CRT_RSET C4
CRT_HSYNC A1
CRT_VSYNC B1

AR/NC
AG/NC
AB/NC

RSET/NC
HSYNC/NC
VSYNC/NC

XIN/NC
INTA/NC
BIST/NC

SPCLK1/NC P2
SPCLK2/NC C2
SPD1/NC P1
SPD2/NC C1

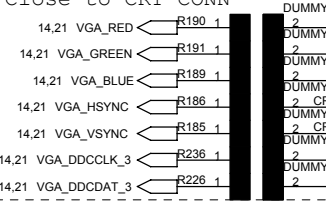
DPO_D0 J1
DPO_D1 K2
DPO_D2 K3
DPO_D3 L4
DPO_D4 K1
DPO_D5 L2
DPO_D6 L3
DPO_D7 M4
DPO_D8 L1
DPO_D9 M2
DPO_D10 M3
DPO_D11 M1

DPO_DET B4
DPO_HSYNC N1
DPO_VSYNC N4
TVCLK/DPVDET/NC N1
TVDE/DPVDE/NC N4
TVHS/DPVHS/NC N3
TVVS/DPVVS/NC N3

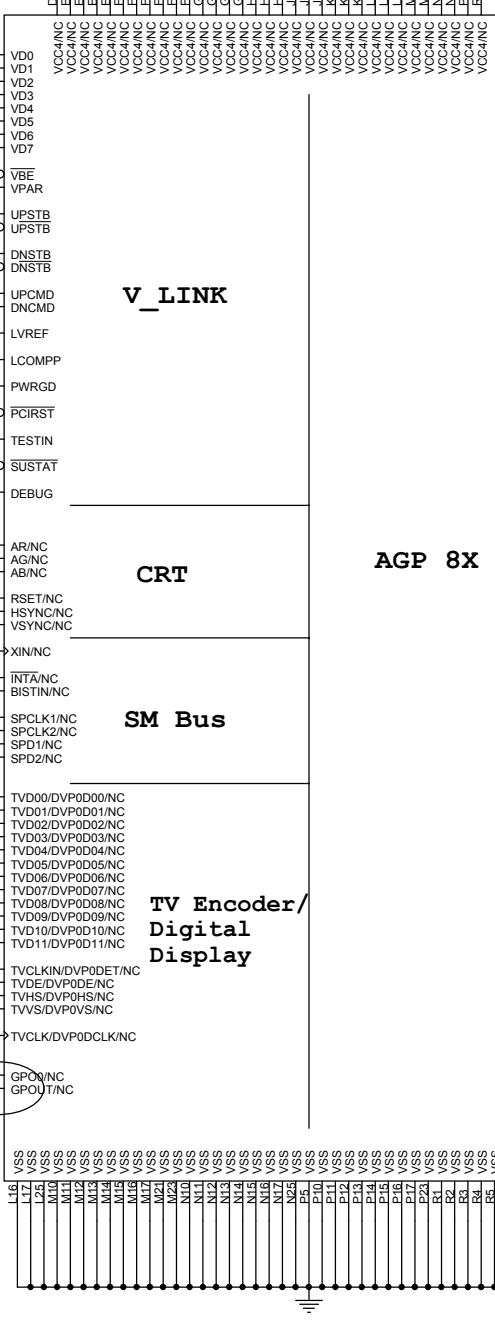
TVCLK/DPVDC/NC
TVCLK/DPVDC/NC

GPO0/NC
GPO1/NC

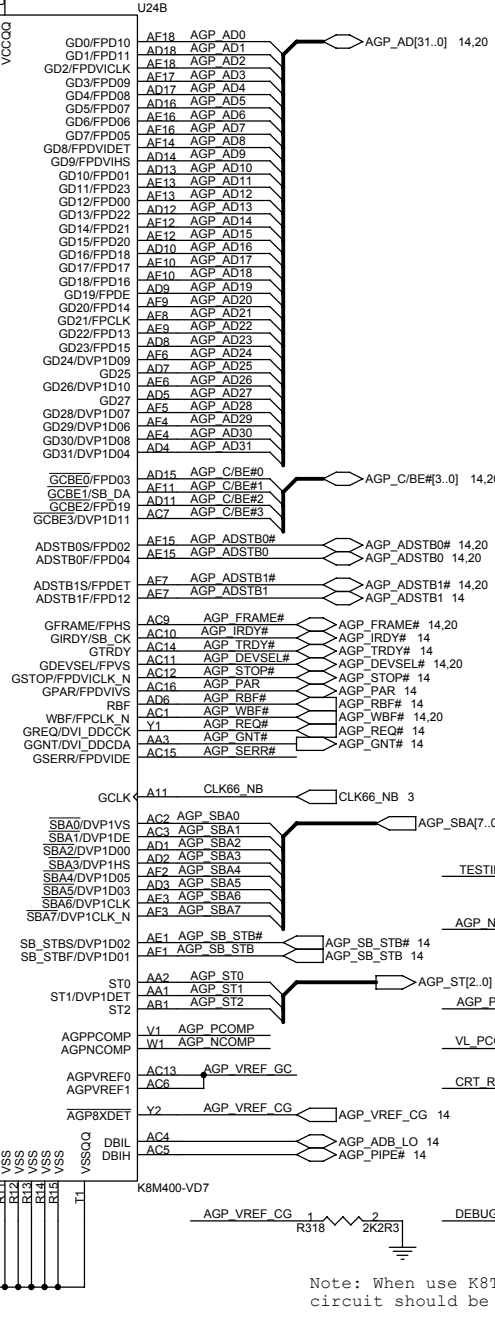
DUMMY-0R3-U Modify-0602



V_LINK

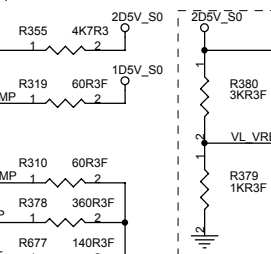
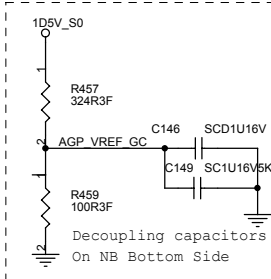
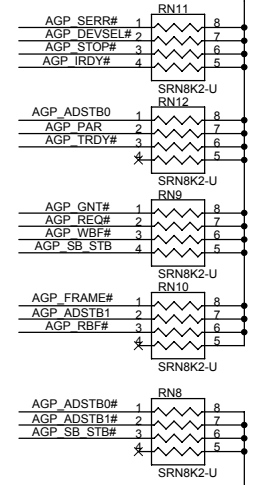


AGP 8X



SM Bus

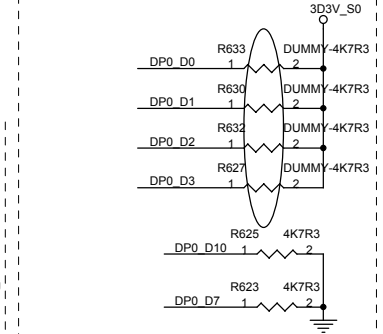
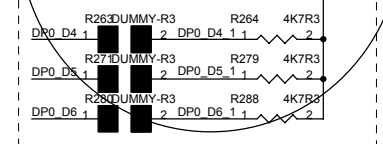
TV Encoder/ Digital Display



Layout trace 20 mil
The voltage level of
VL_VREF is 0.625V
Cross NB as short as possible

Use this function for K8M400

AGP power up strapping setting:
TV0/DPV0D[3:0] => Panel type selection
TV04/DPV0D4 => FP-port multiplexed on AGP interface selection
0: Two 12-bit DVI interface
1: One 24-bit panel interface
TV05/DPV0D5 => Dedicated DVI port configuration
0: DMS
1: TV Encoder
TV06/DPV0D6 => Dedicated DVI port selection
0: Disable
1: Enable



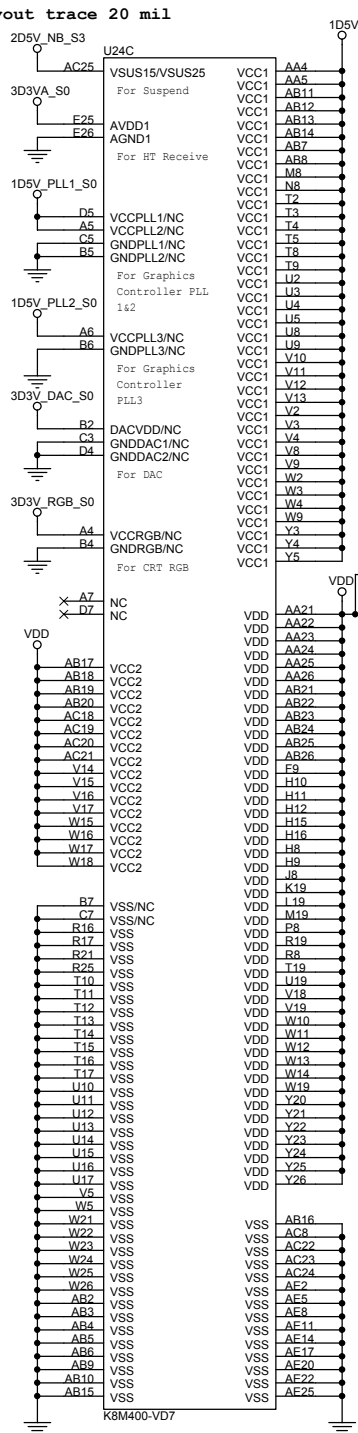
Note: All of these power up strapping pin have internal pull down. Put an external pull up resistor if want to set the default value to 1.

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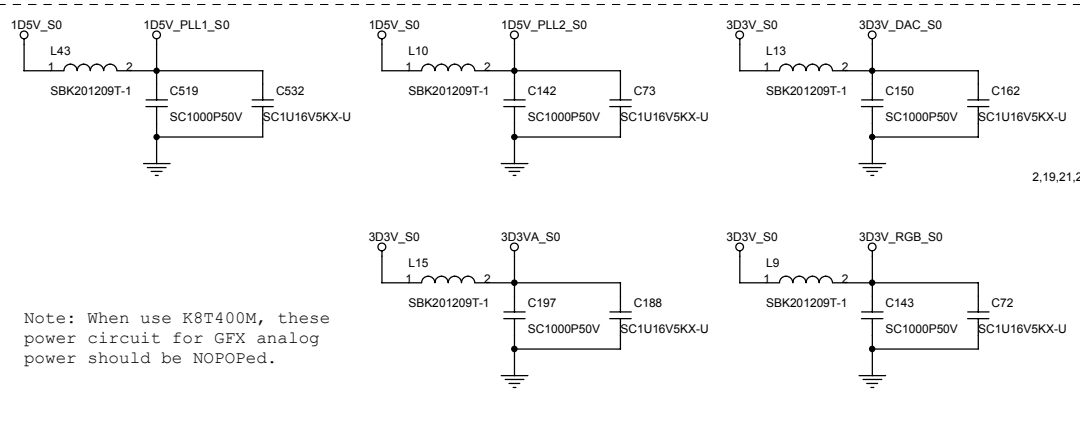
Title		NB-K8T800M(2/3) AGP VLINK	
Size	A3	Document Number	Gannet
Date:	Thursday, December 04, 2003	Sheet	9 of 51

Note: When use K8T400M, GFX relative circuit should be NOPOped.

Layout trace 20 mil

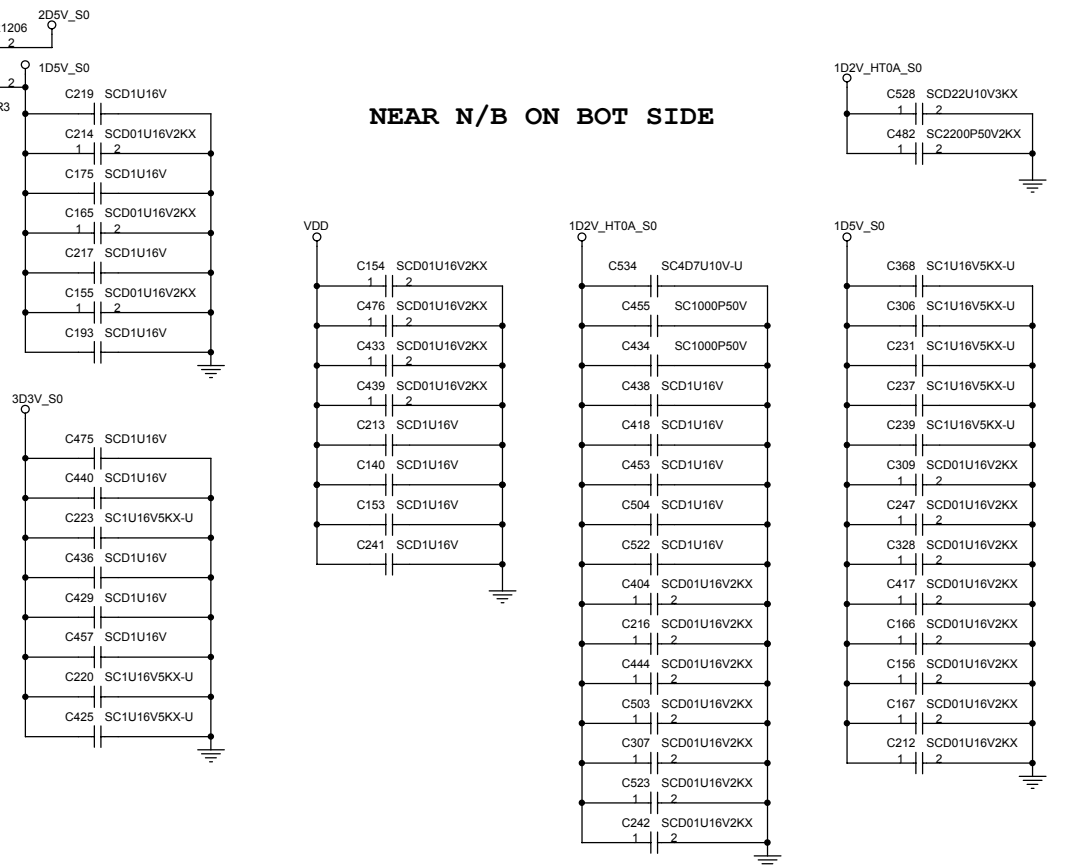


Layout trace 20 mil

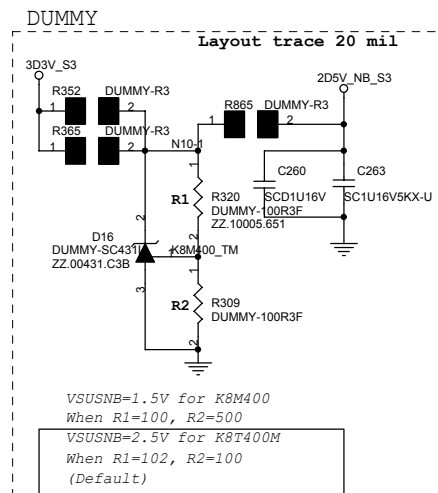
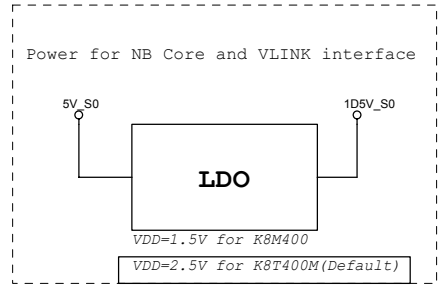
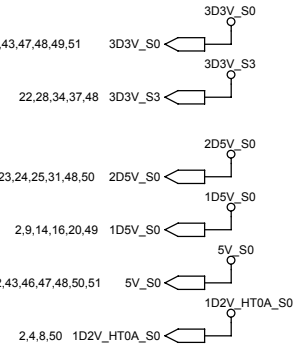


Note: When use K8T400M, these power circuit for GFX analog power should be NOPOPed.

NEAR N/B ON BOT SIDE



2,3,8,9,11,14,16,19,20,21,22,23,24,25,27,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,47,48,49,51

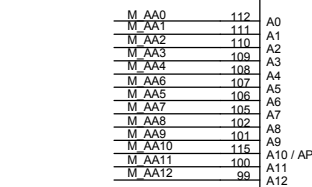


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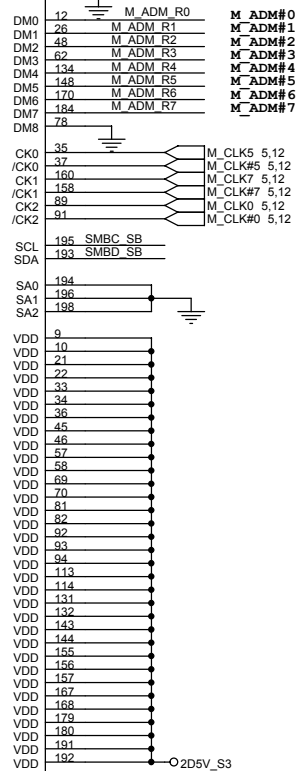
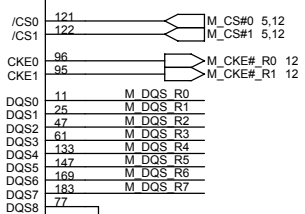
Title: **NB-K8T800M(3/3) POWER**

Size: A3 Document Number: **Gannet** Rev: -1

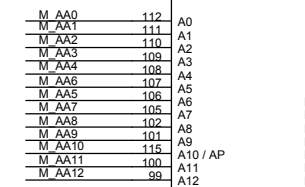
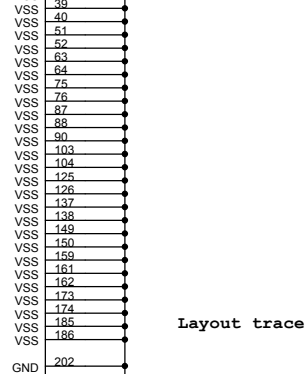
Date: Thursday, December 04, 2003 Sheet 10 of 51



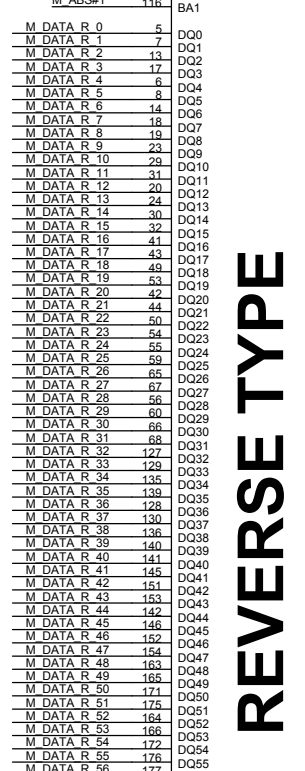
NORMAL TYPE



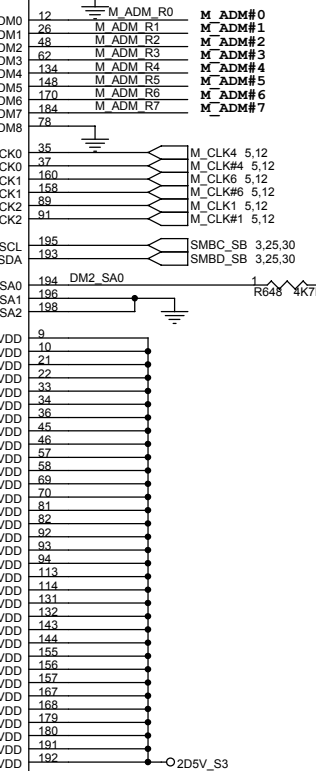
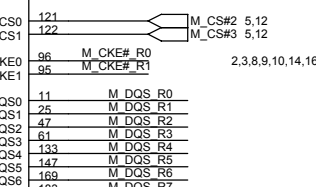
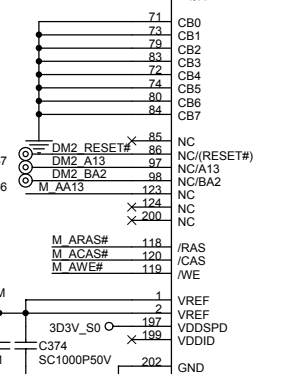
NOT SUPPORT ECC CHECK
Ali suggested pull-low



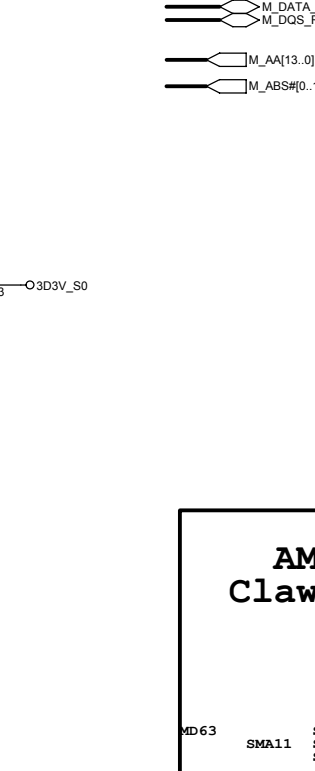
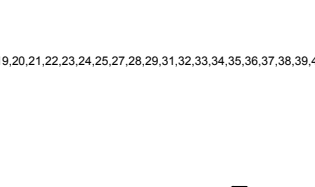
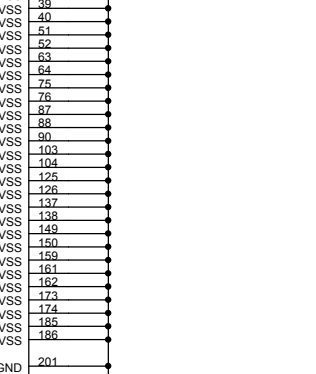
REVERSE TYPE



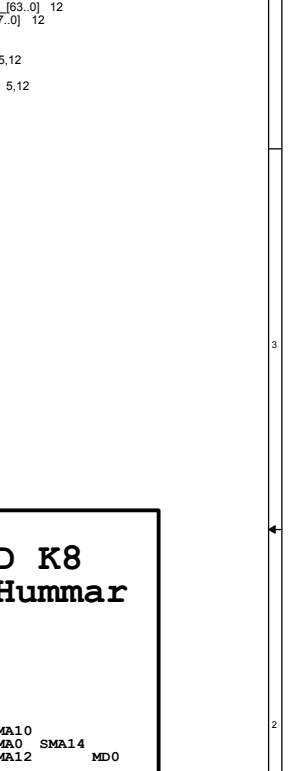
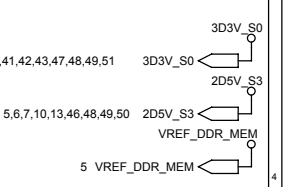
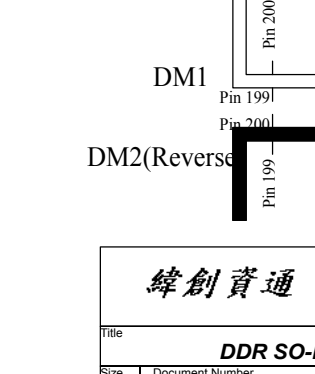
NOT SUPPORT ECC CHECK
Ali suggested pull-low



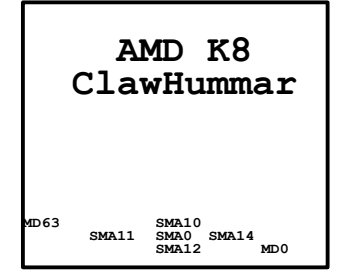
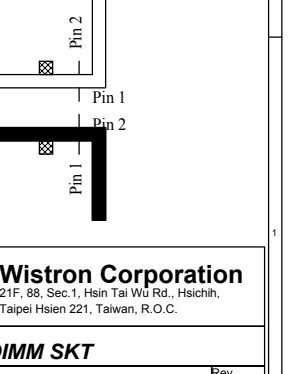
NOT SUPPORT ECC CHECK
Ali suggested pull-low



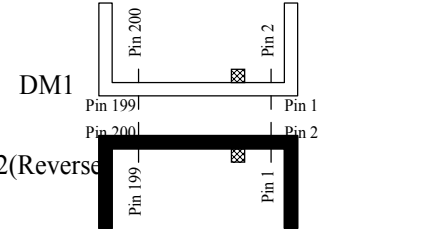
NOT SUPPORT ECC CHECK
Ali suggested pull-low



NOT SUPPORT ECC CHECK
Ali suggested pull-low



**DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING**



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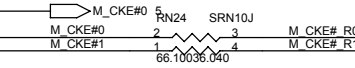
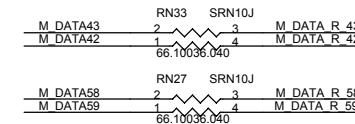
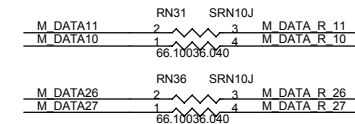
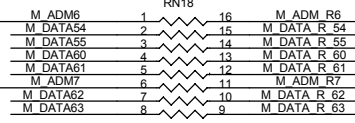
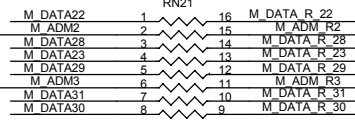
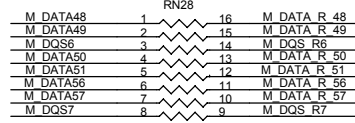
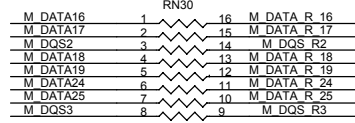
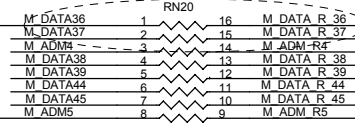
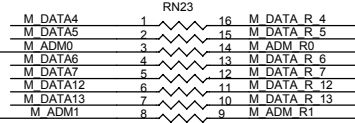
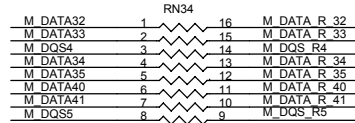
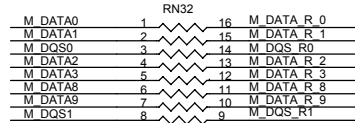
Title: **DDR SO-DIMM SKT**

Size A3	Document Number	Rev -1
Gannet		

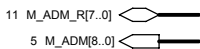
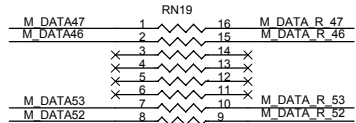
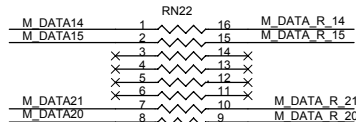
Date: Thursday, December 04, 2003 Sheet 11 of 51

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM2), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

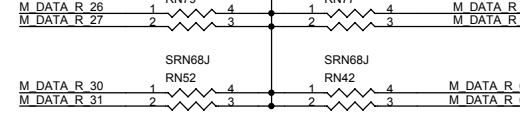
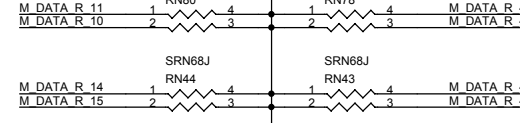
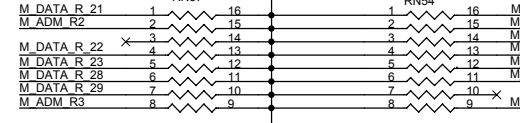
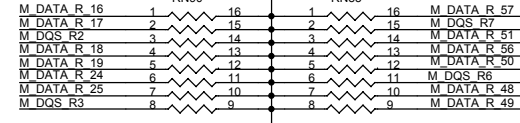
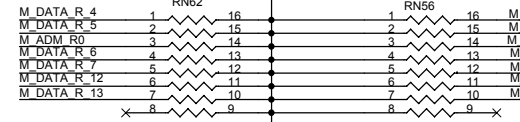
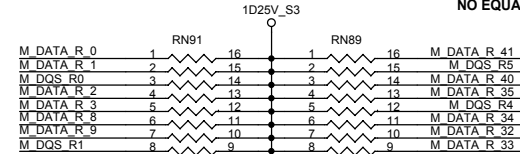


11/11 add RN30 for AMD suggest.

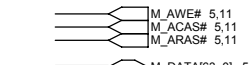
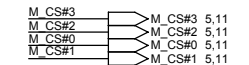
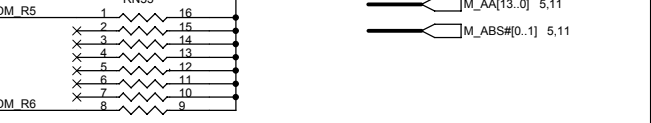
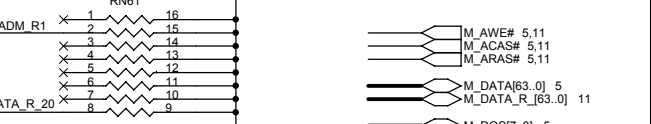
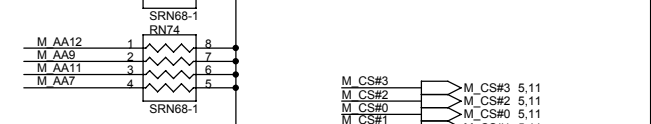
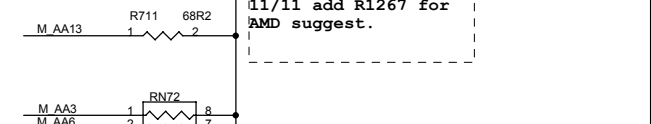
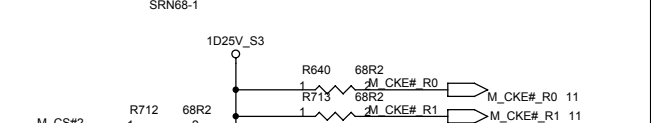
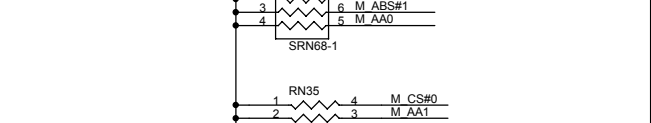
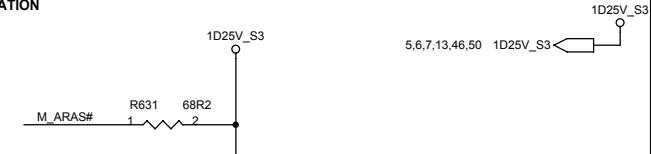
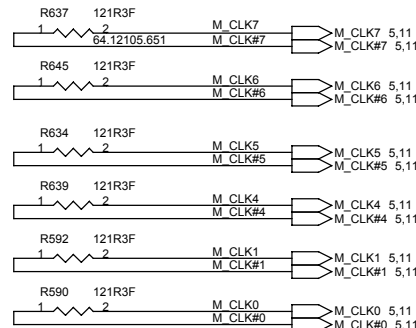


TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM1)
NO EQUAL LENGTH LIMITATION



PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM 2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#



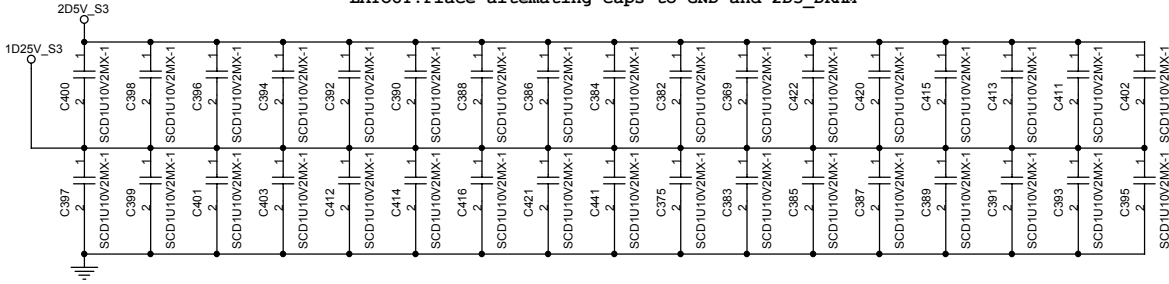
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1D25V_S3 TO GND	100u	10u	4.7u	0.22u	0.1u	1000p	100p
	2	2	10	10	34	4	4

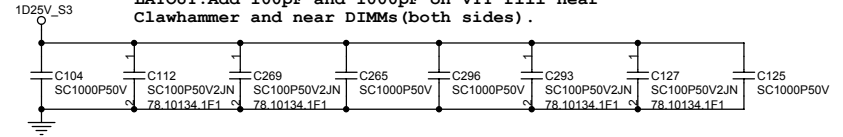
1D25V_S3 TO 2D5V_S3	220u	0.22u	0.1u
	1	10	34



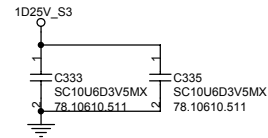
LAYOUT: Place alternating caps to GND and 2D5_DRAM



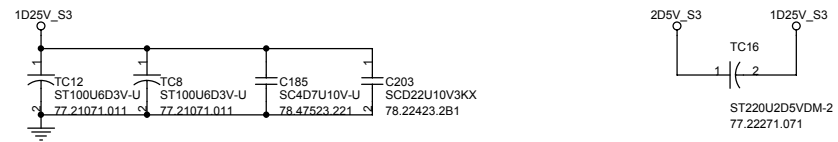
LAYOUT: Add 100pF and 1000pF on VTT fill near Clawhammer and near DIMMs (both sides).



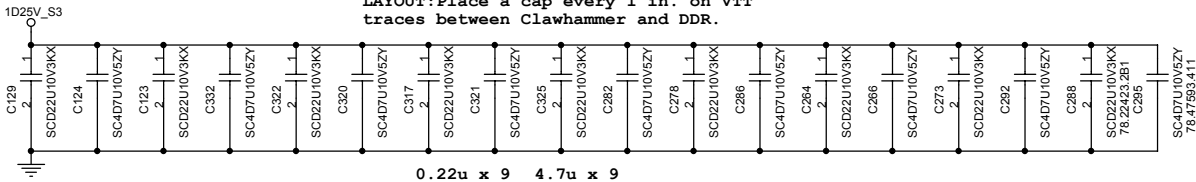
LAYOUT: Place one 10uF capacitor on each end of the VTT island.



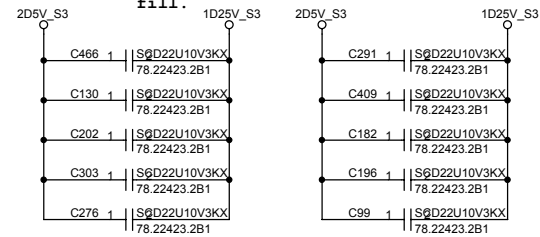
LAYOUT: Locate close to Clawhammer socket.



LAYOUT: Place a cap every 1 in. on VTT traces between Clawhammer and DDR.

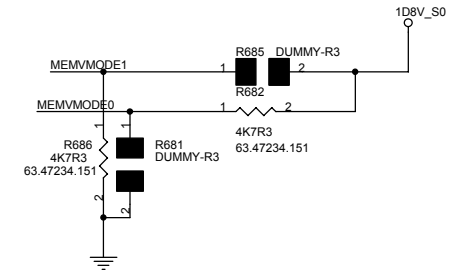
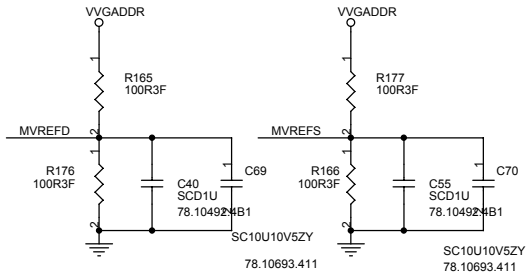
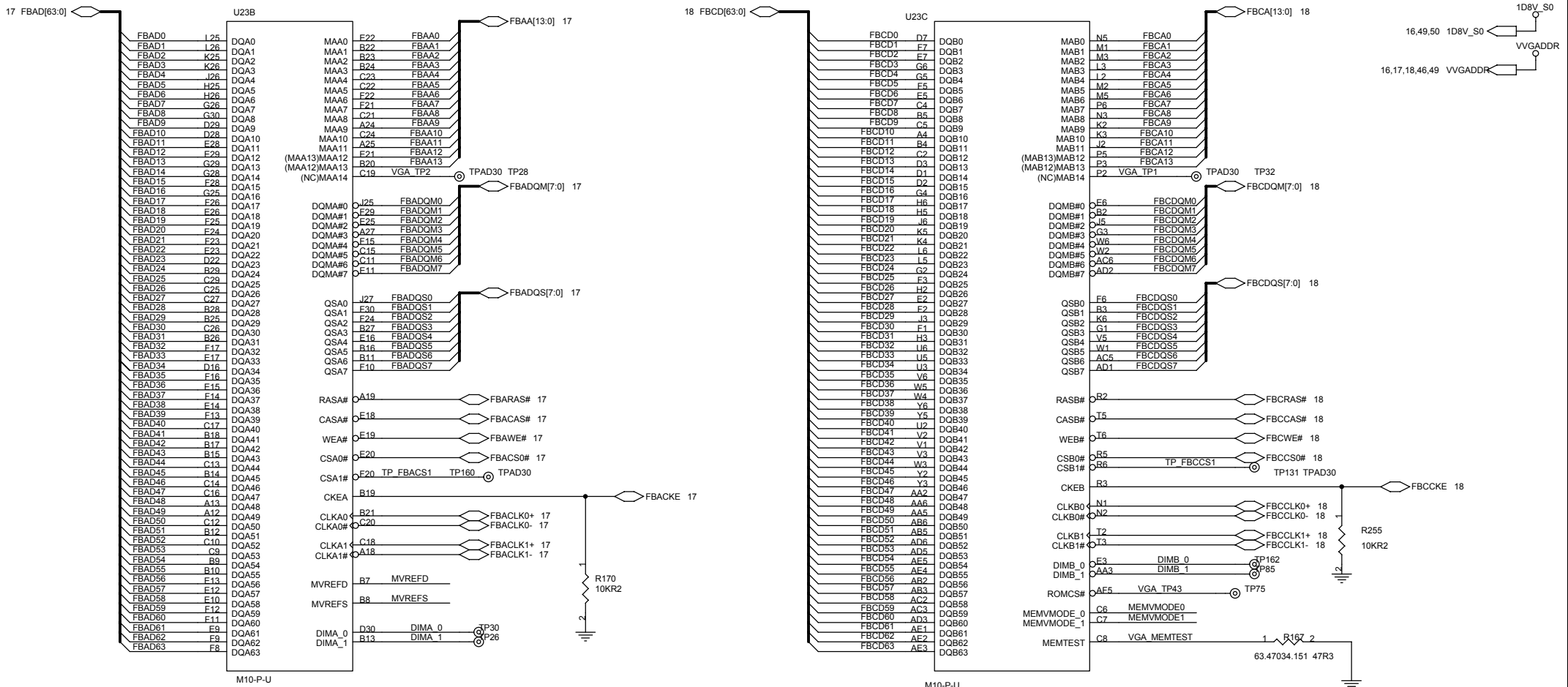


LAYOUT: Place on backside, evenly spaced around VTT fill.



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Title			DDR DECOUPLING		
Size	Document Number	Gannet		Rev	-1
A3					
Date: Thursday, December 04, 2003			Sheet	13	of 51



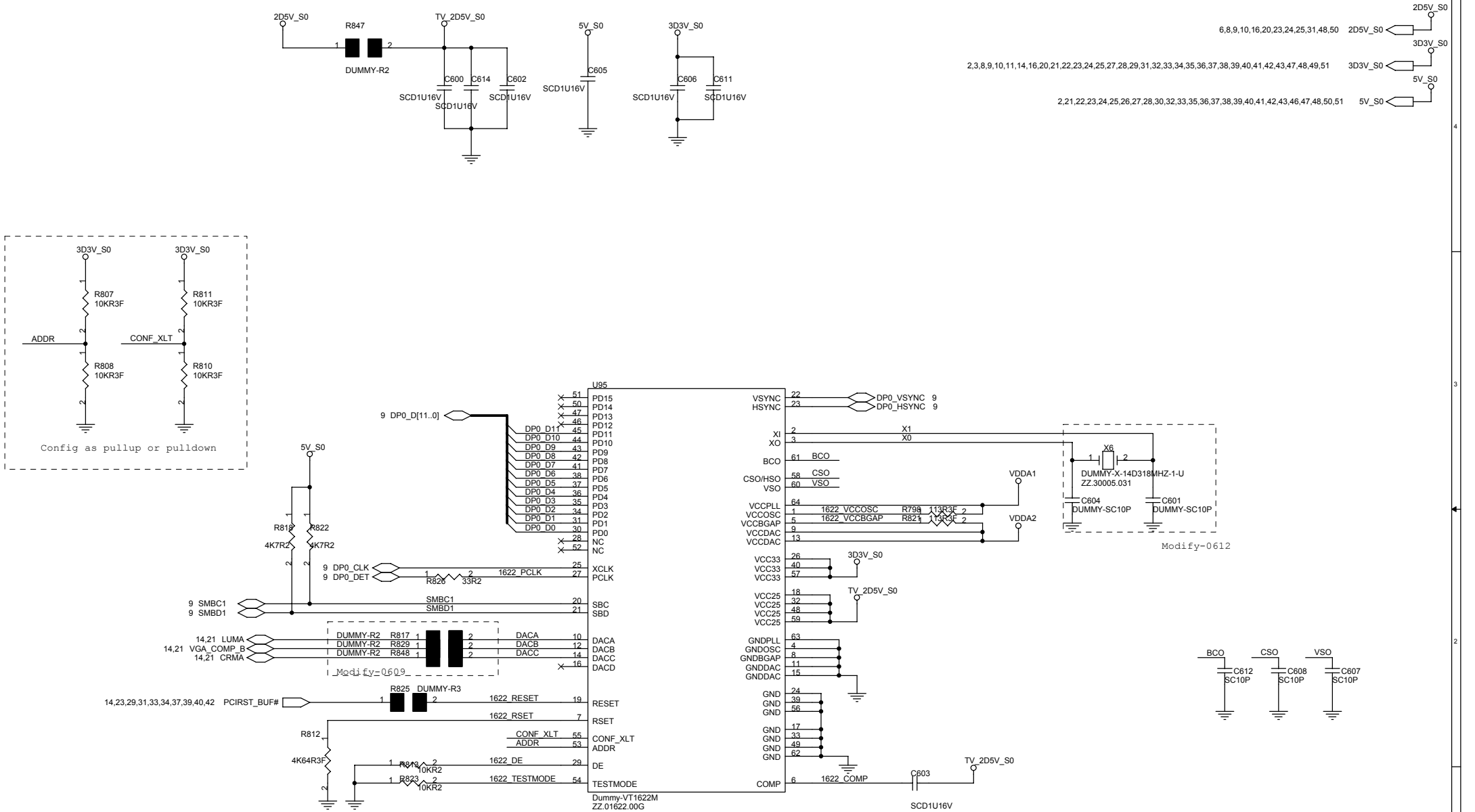
	MEMMODE0	MEMMODE1
2D5V VDDR1	1	0
1D8V VDDR1 (ELPIDA)	0	1

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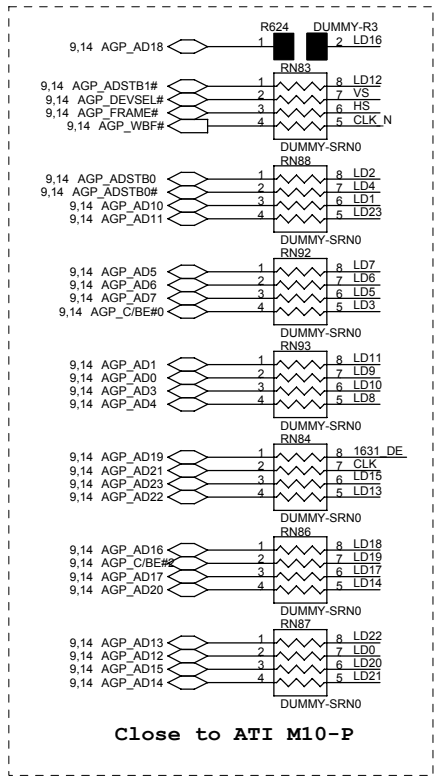
Title: **VGA(2/3) ATI M10-P MEM**

Size: A3 Document Number: Gannet Rev: -1

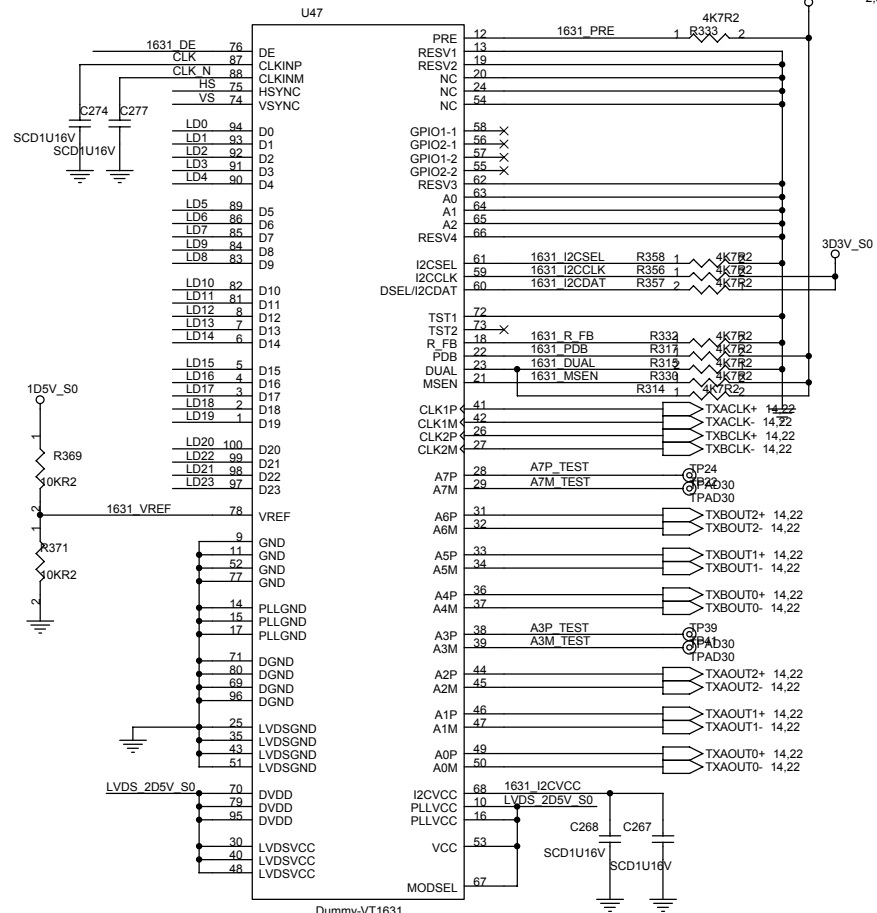
Date: Thursday, December 04, 2003 Sheet: 15 of 51



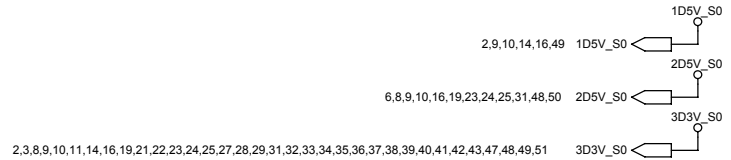
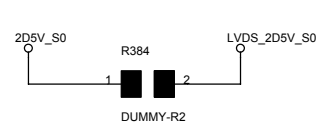
DUMMY-SRNO



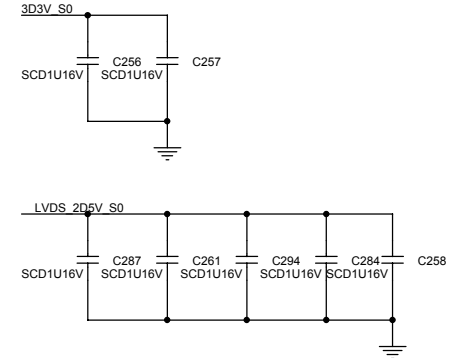
Close to ATI M10-P



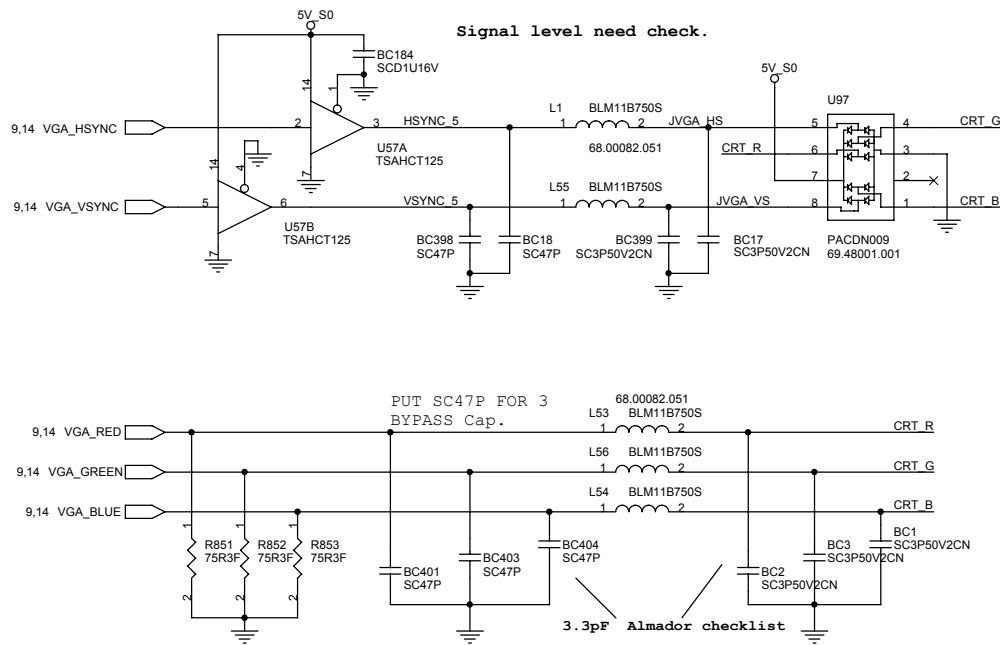
Dummy-VT1631
ZZ.V1631.00G



5/15
Remove the 5V_S0 C701-705
and 3D3V_S0 C693-C695

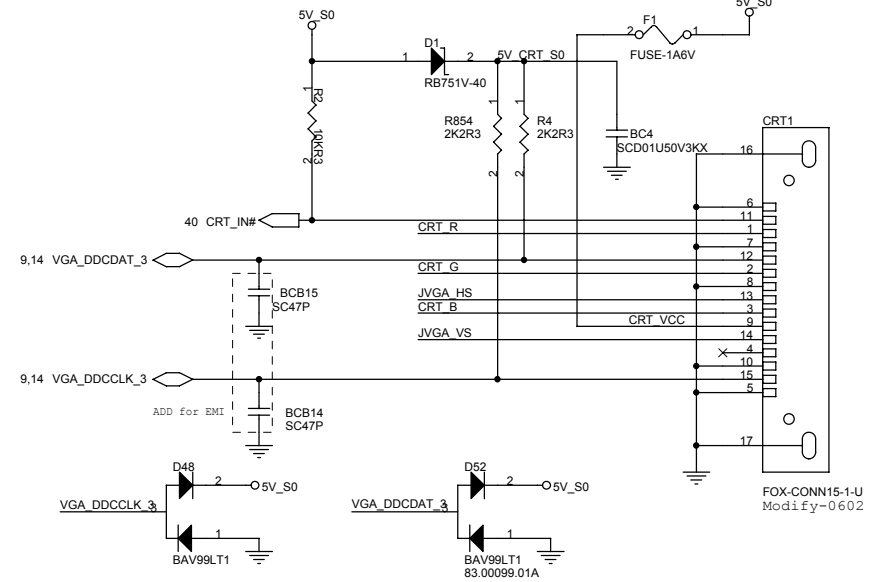


CRT



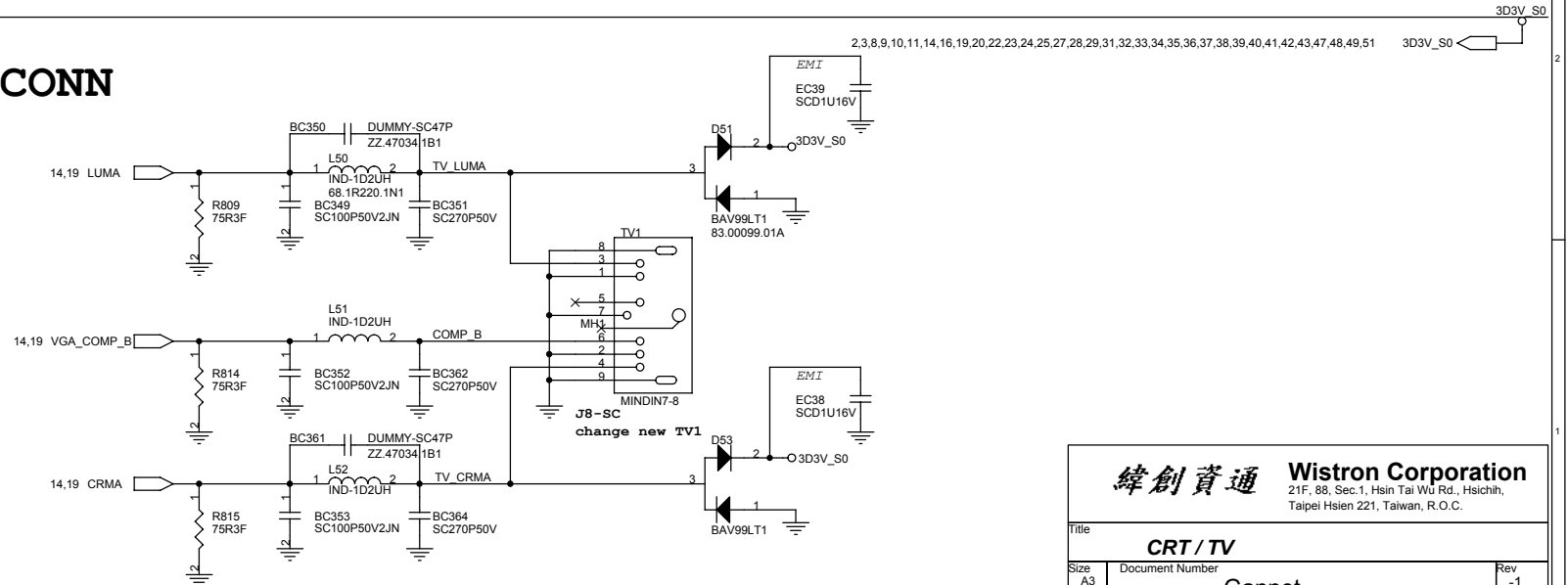
CRT CONN

200mA Rating/Spec 500mA



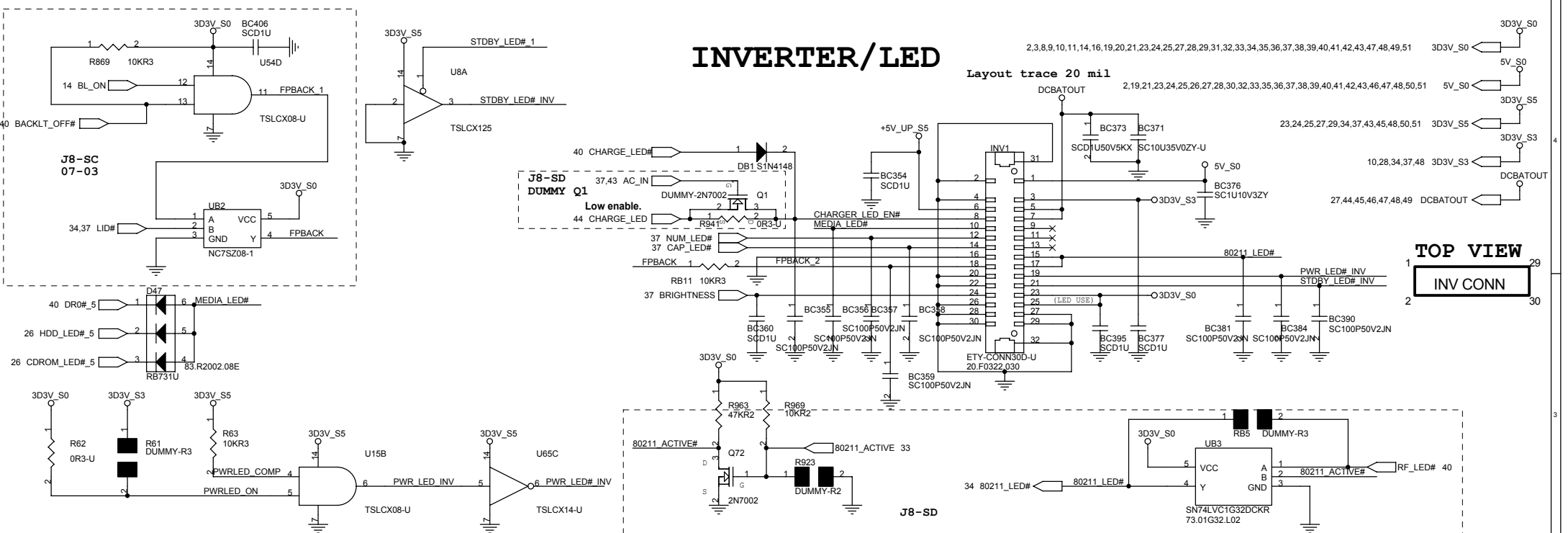
Layout Note:
Must be a ground return path between this ground and the ground on the VGA connector.
37.4 1% resistors must be placed after RGB pi filter ,near CRT connector.

TV CONN

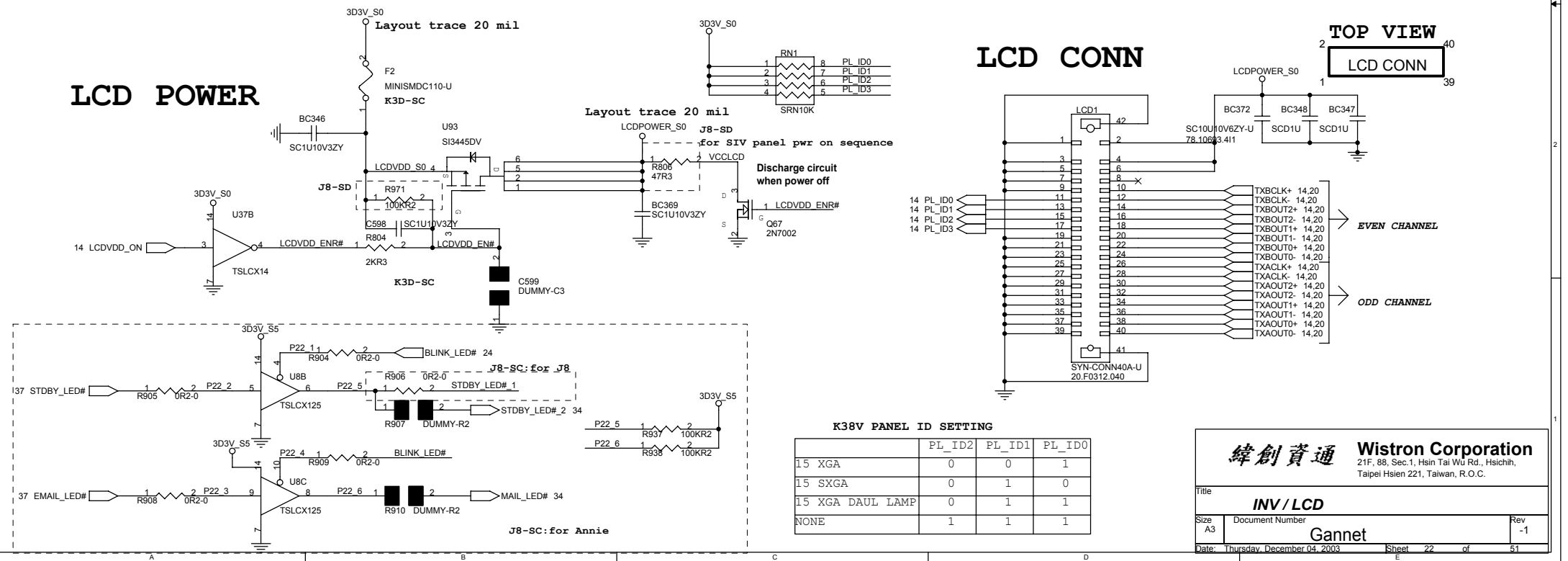


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Title: CRT / TV			
Size: A3	Document Number:	Gannet	
Date: Thursday, December 04, 2003		Sheet: 21	of: 51
		Rev: -1	

INVERTER/LED



LCD POWER



K38V PANEL ID SETTING

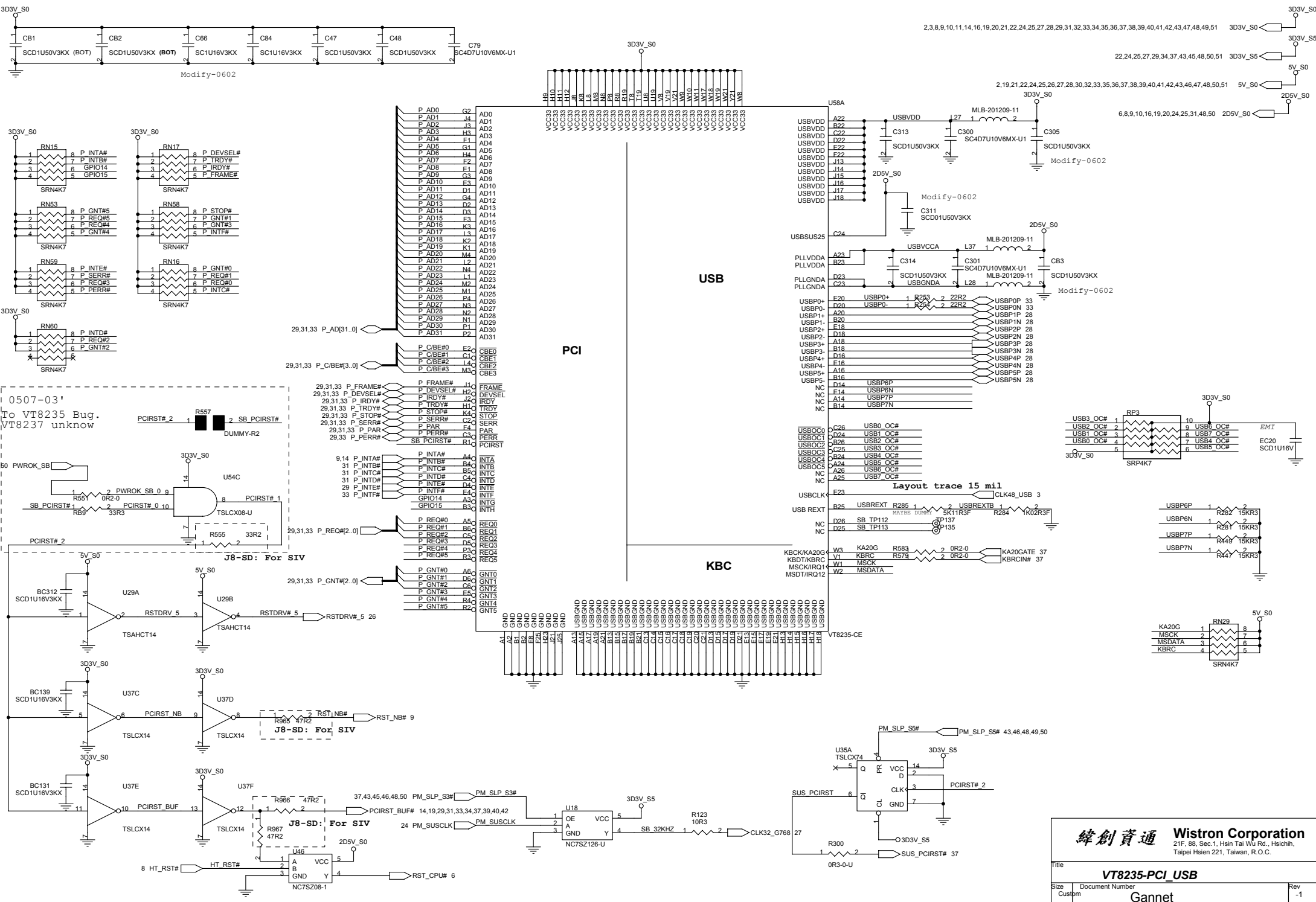
	PL_ID2	PL_ID1	PL_ID0
15 XGA	0	0	1
15 SXGA	0	1	0
15 XGA DAUL LAMP	0	1	1
NONE	1	1	1

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Title: **INV / LCD**

Size: A3 Document Number: **Gannet** Rev: -1

Date: Thursday, December 04, 2003 Sheet: 22 of 51



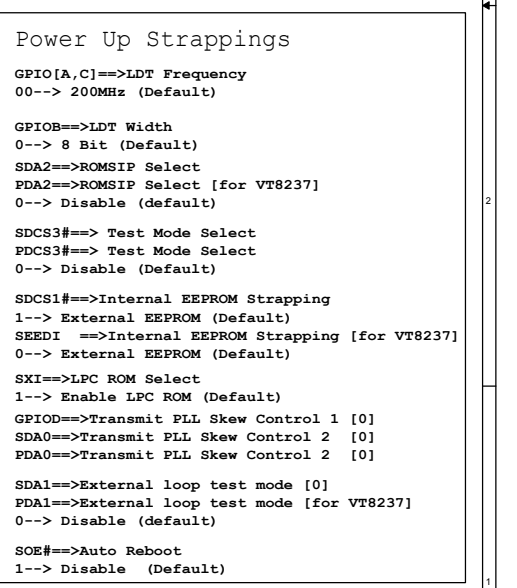
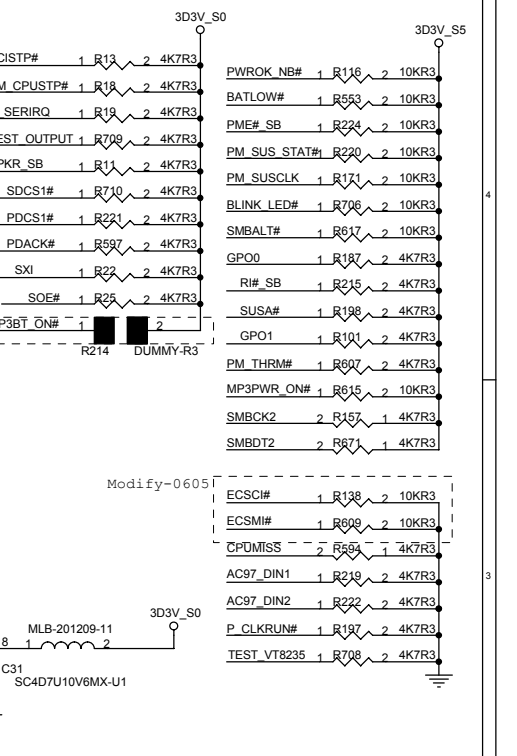
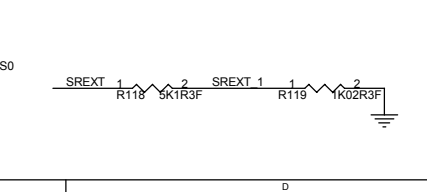
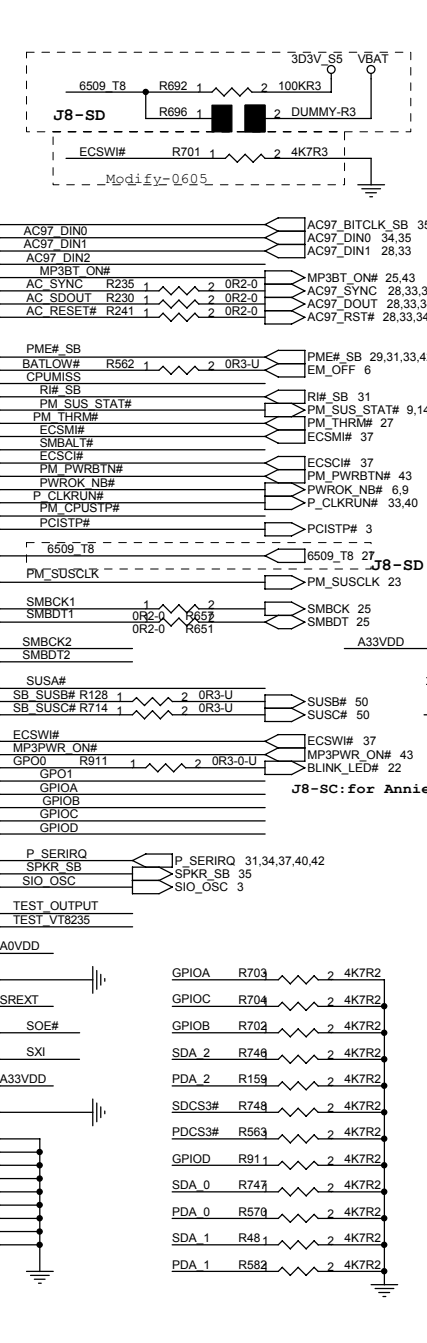
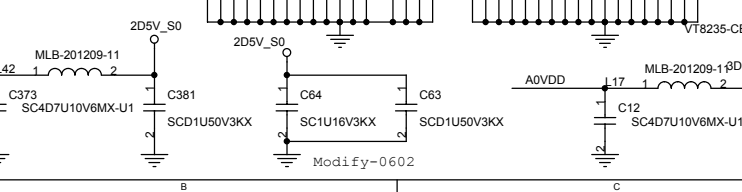
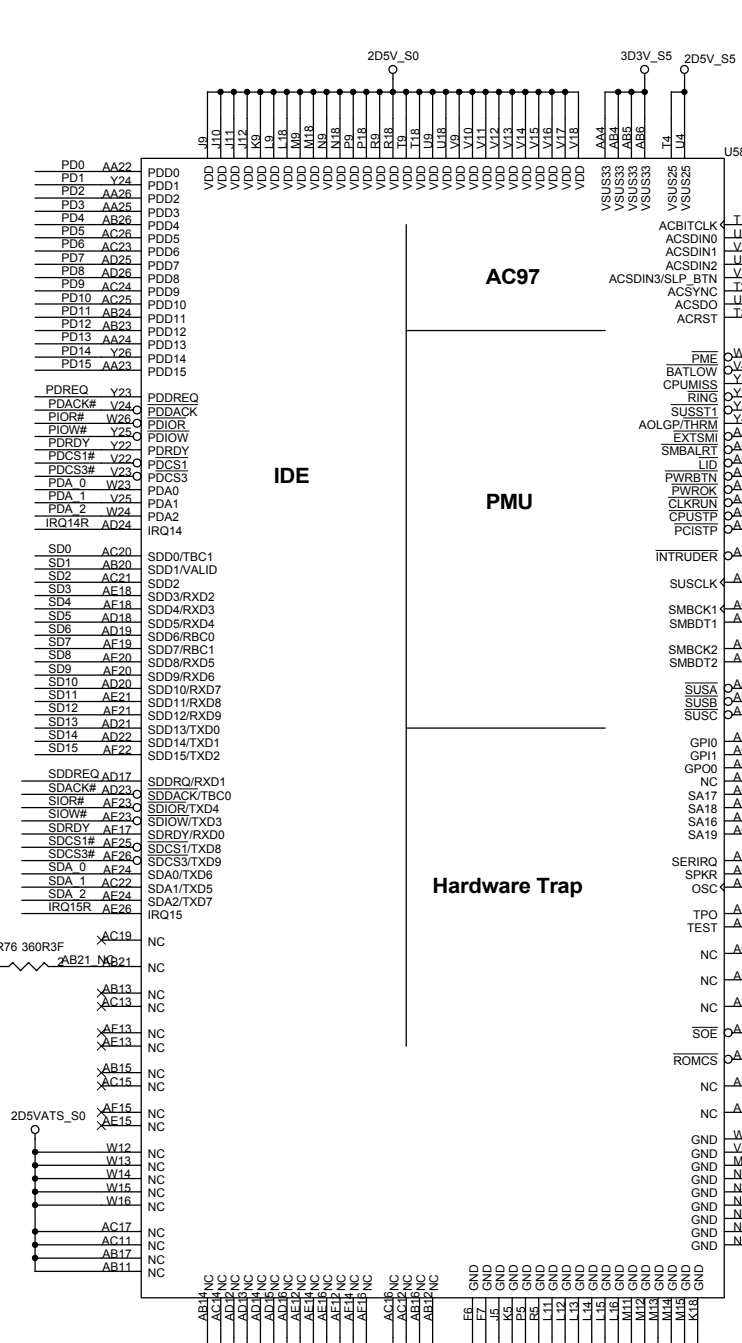
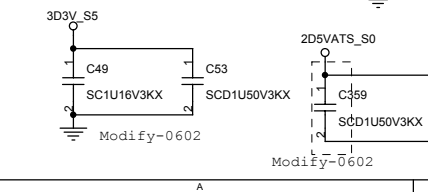
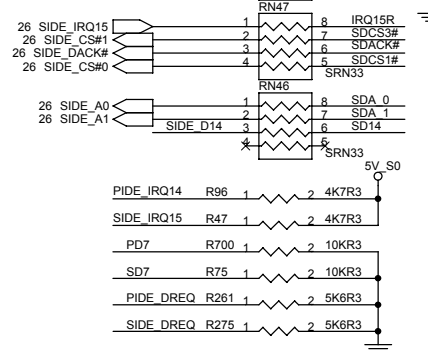
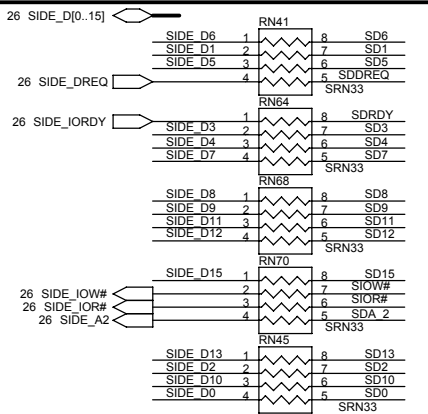
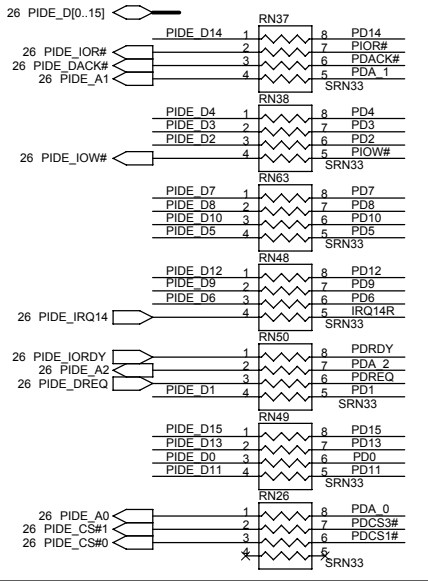
0507-03'
To VT8235 Bug.
VT8237 unknow

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File: **VT8235-PCI_USB**

Size	Document Number	Rev
Custom	Gannet	-1

Date: Thursday, December 04, 2003 Sheet 23 of 51



Power Up Strappings

GPIO[A,C]==>LDT Frequency
00--> 200MHz (Default)

GPIOB==>LDT Width
0--> 8 Bit (Default)

SDA2==>ROMSIP Select
FDA2==>ROMSIP Select [for VT8237]
0--> Disable (default)

SDCS3==> Test Mode Select
PDCS3==> Test Mode Select
0--> Disable (Default)

SDCS1==>Internal EEPROM Strapping
1--> External EEPROM (Default)
SEEDI ==>Internal EEPROM Strapping [for VT8237]
0--> External EEPROM (Default)

SXI==>LPC ROM Select
1--> Enable LPC ROM (Default)

GPIOD==>Transmit PLL Skew Control 1 [0]
SDA0==>Transmit PLL Skew Control 2 [0]
FDA0==>Transmit PLL Skew Control 2 [0]

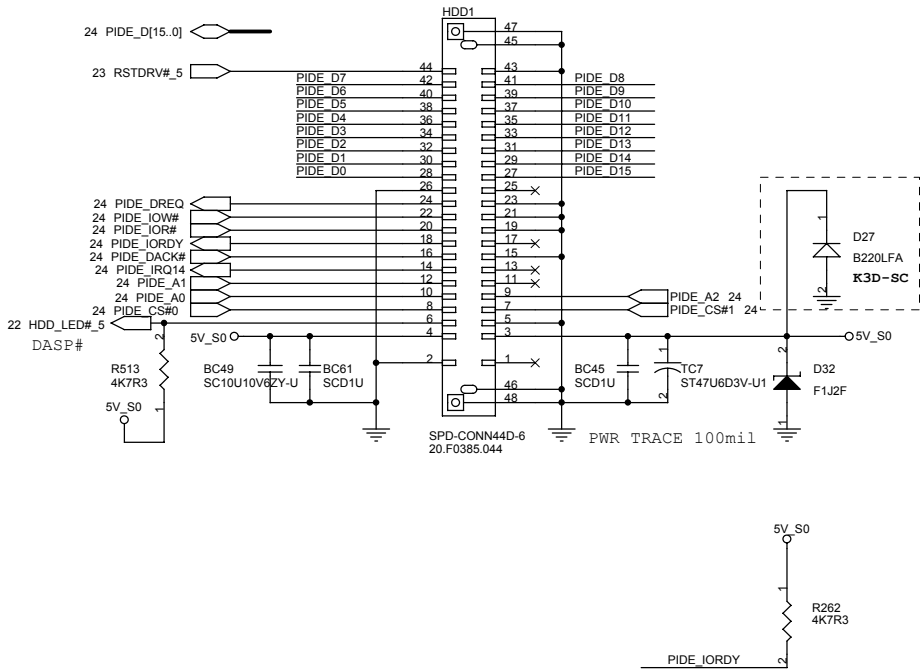
SDA1==>External loop test mode [0]
FDAl==>External loop test mode [for VT8237]
0--> Disable (default)

SOE==>Auto Reboot
1--> Disable (Default)

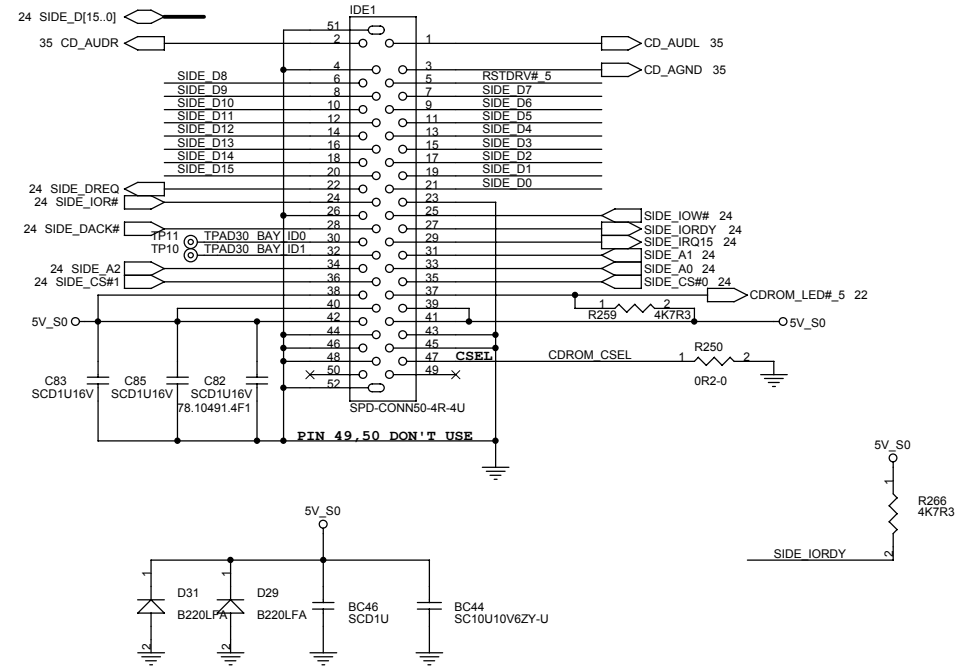
緯創資通 Wistron Corporation
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Title		VT8235-IDE_AC97_PMU	
Size	A3	Document Number	Gannet
Date:	Thursday, December 04, 2003	Sheet	24 of 51

HDD

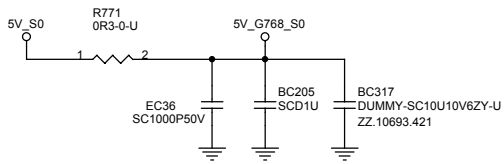


CDROM

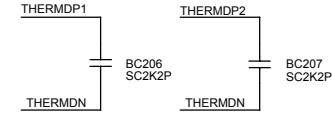
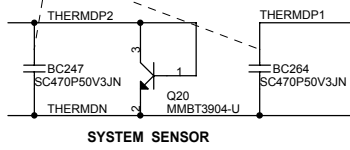


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 Taipei Hsien 221, Taiwan, R.O.C.

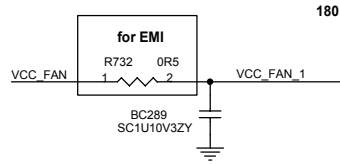
Title HDD / CDROM		
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003 Sheet 26 of 51		



Put these two Caps near the thermal diode.

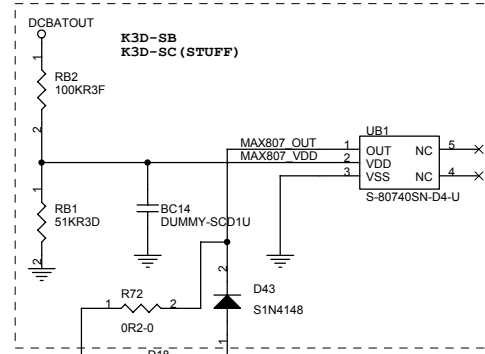


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

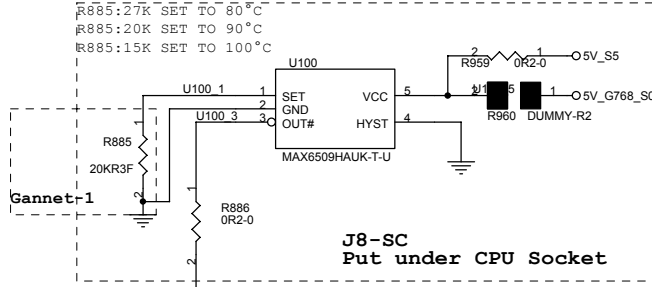
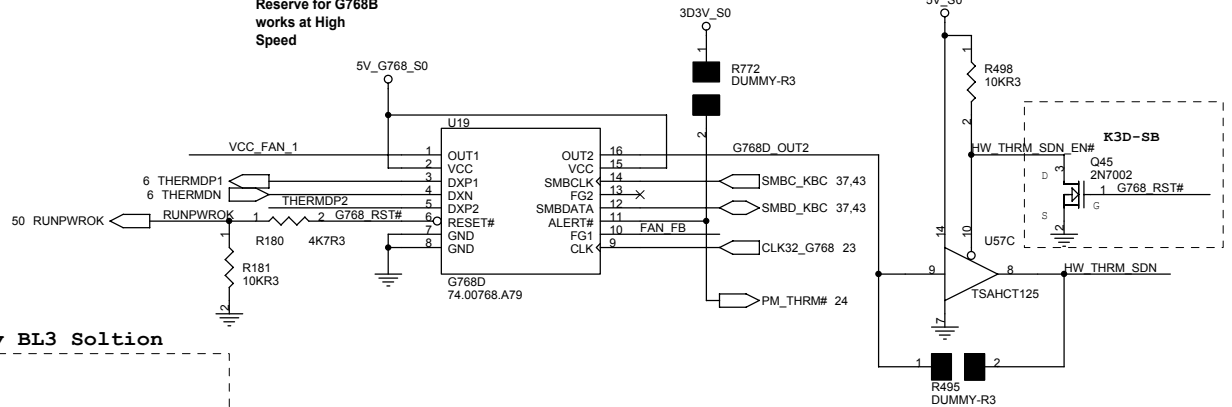


180 ms after VCC_G768 > 4.38v, p2, 7

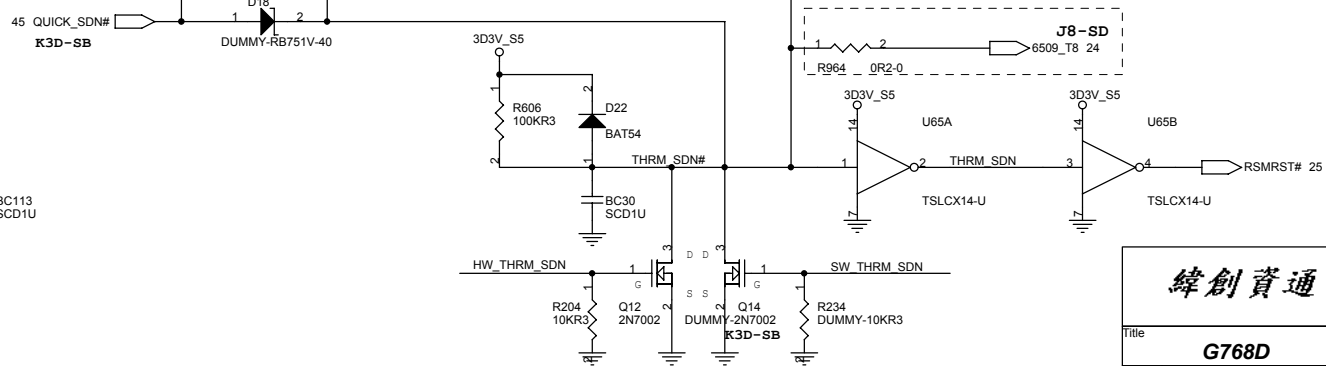
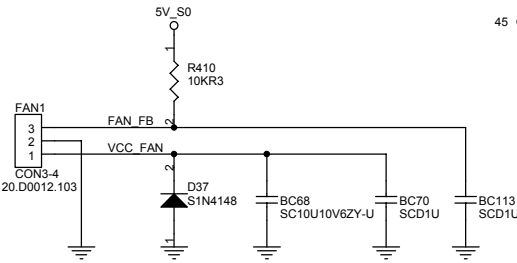
For Ni-MH Battery BL3 Soltion



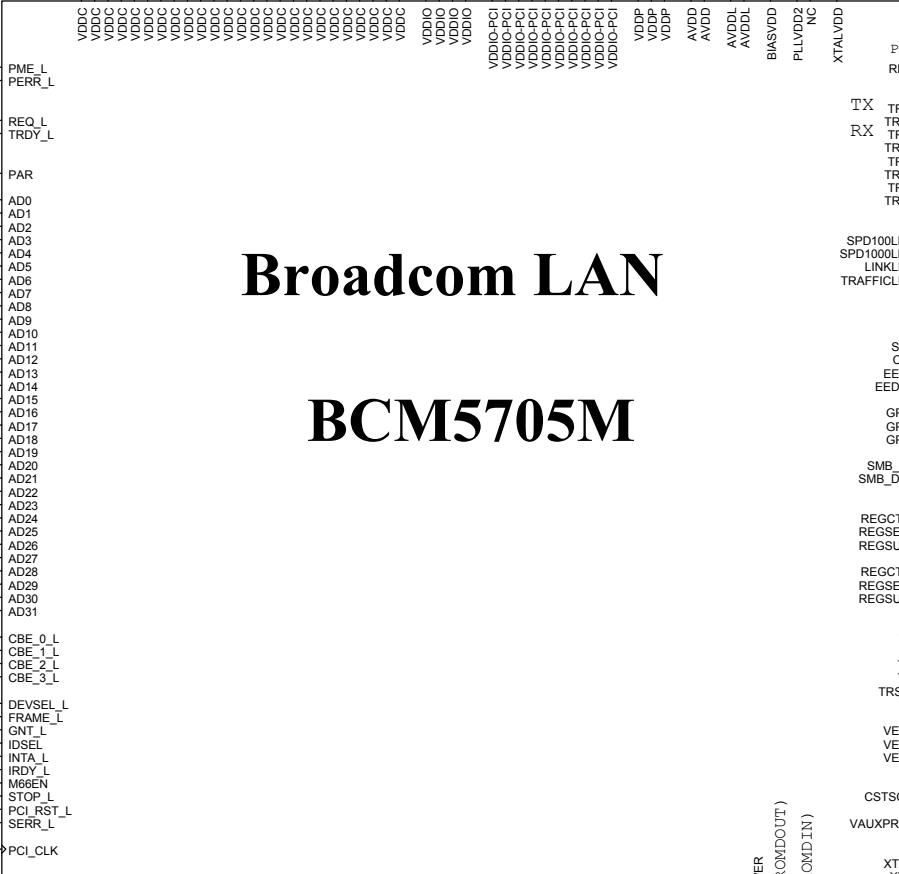
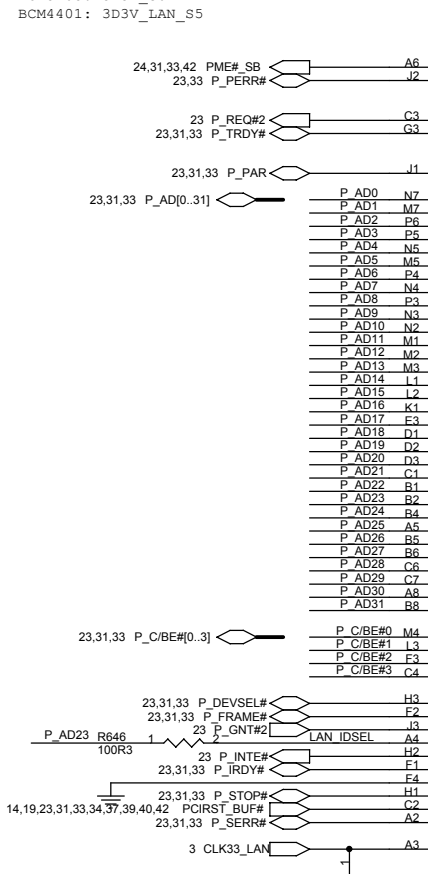
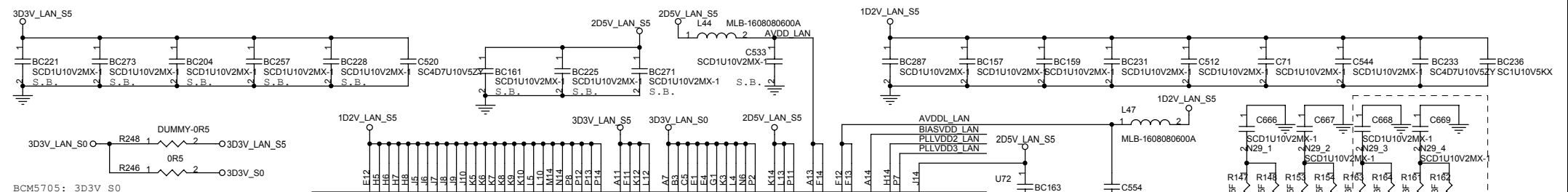
Reserve for G768B works at High Speed



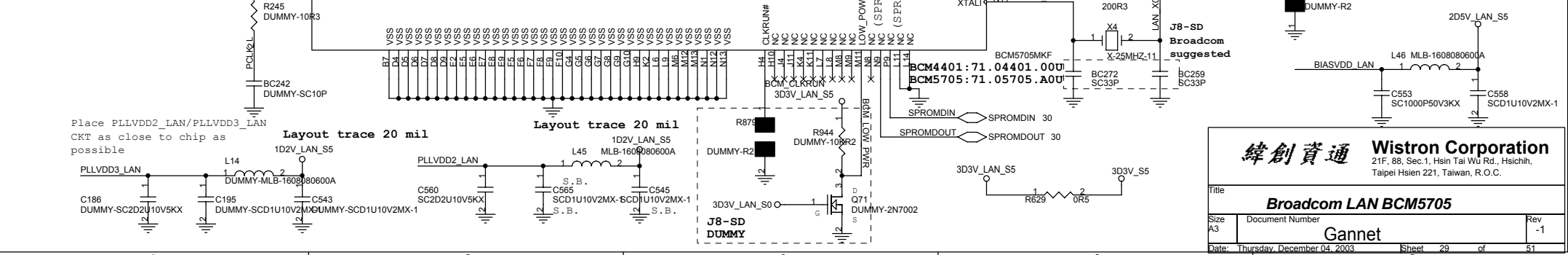
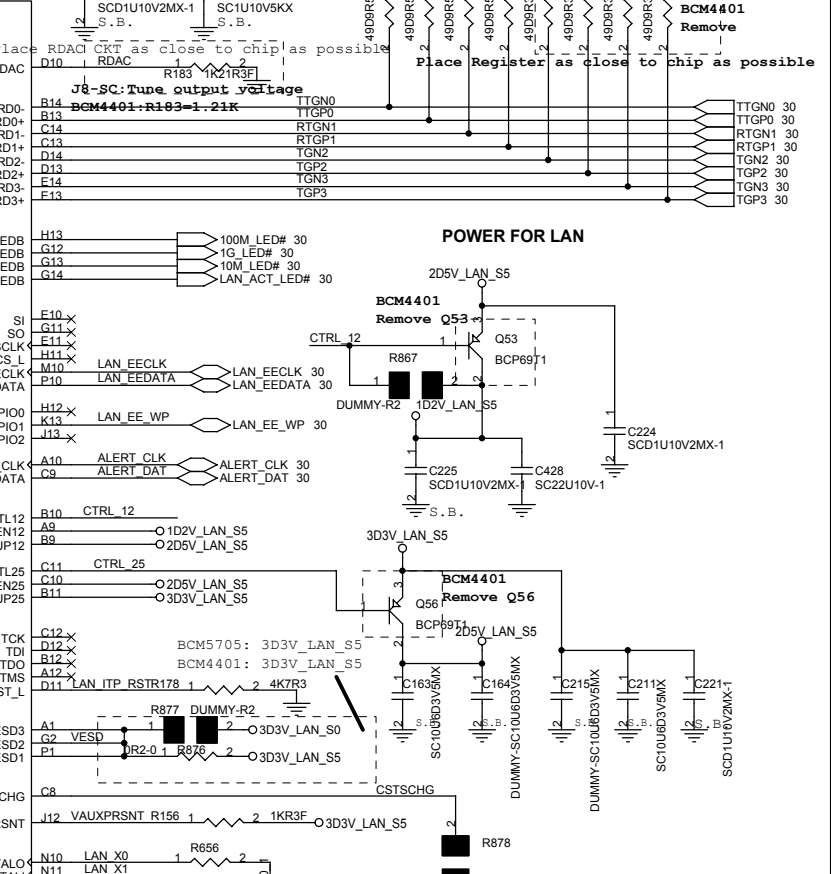
J8-SC Put under CPU Socket



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Title G768D	
Size A3	Document Number
Gannet	
Date: Thursday, December 04, 2003	Sheet 27 of 51

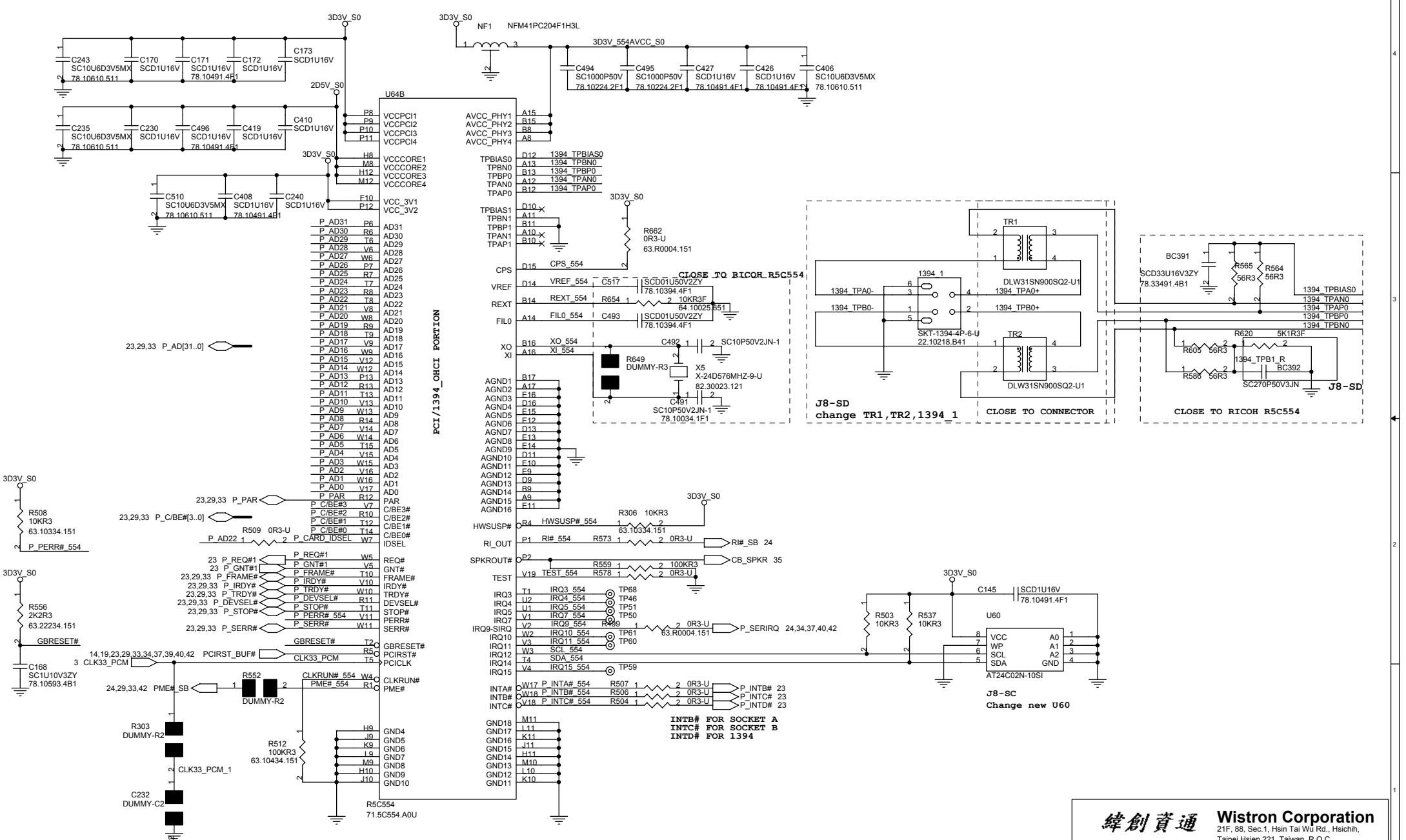


Broadcom LAN BCM5705M



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Broadcom LAN BCM5705	
File	Rev
Size A3	Document Number
Gannet	
Date: Thursday, December 04, 2003 Sheet 29 of 51	

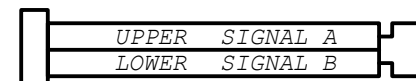


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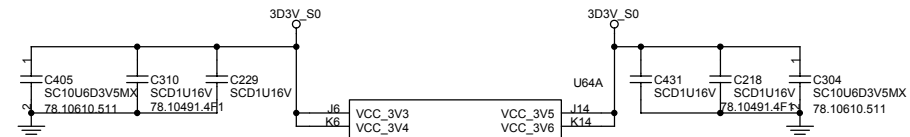
Title: **RICOH_R5C554(1/2)_1394**

Size: A3	Document Number: Gannet	Rev: -1
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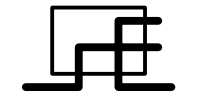
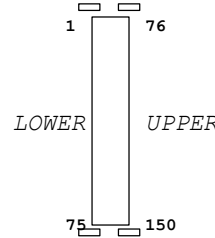
Date: Thursday, December 04, 2003 Sheet 31 of 51



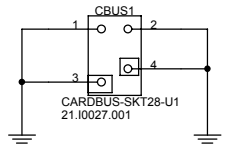
SIGNAL B SIGNAL A



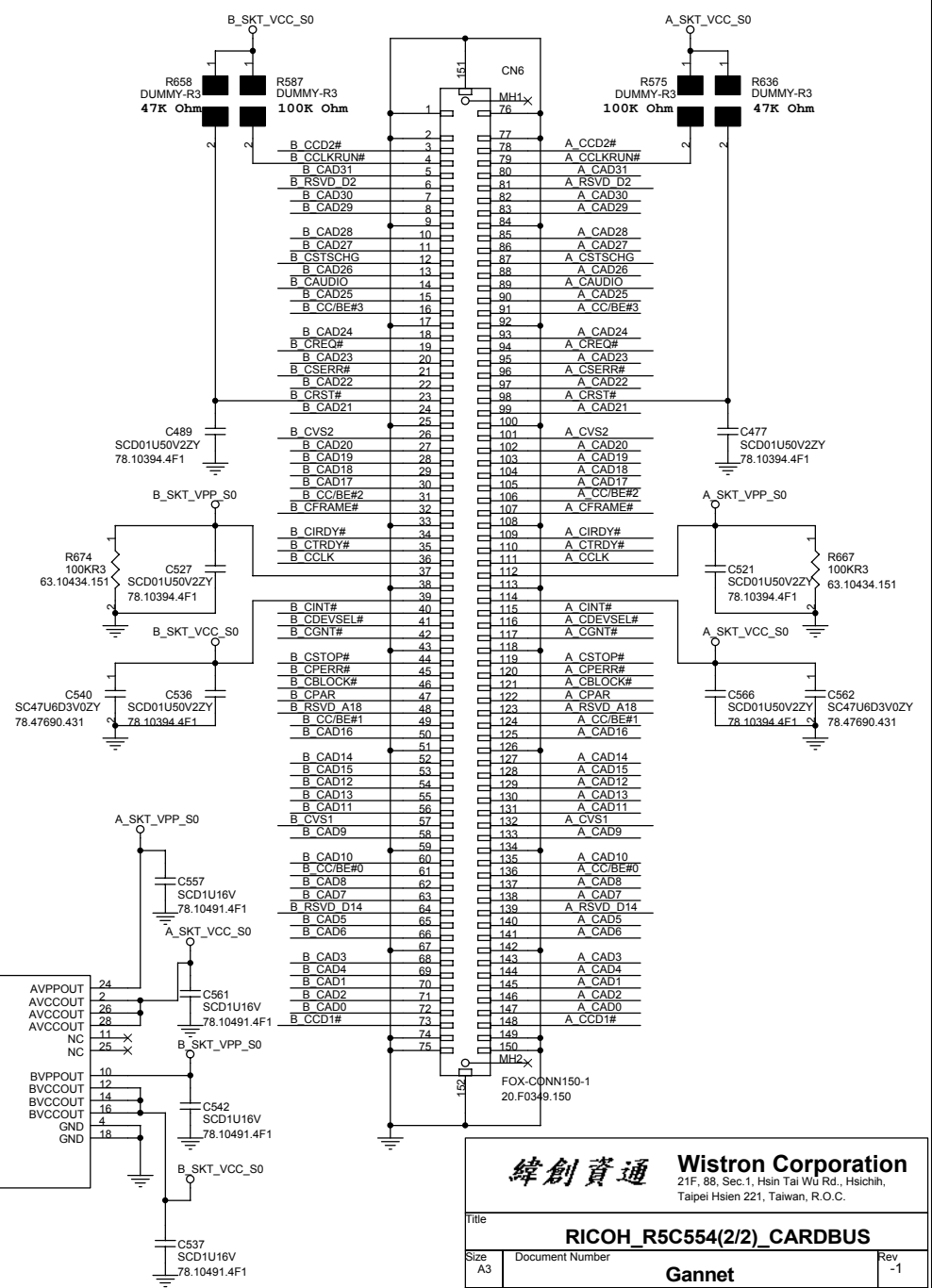
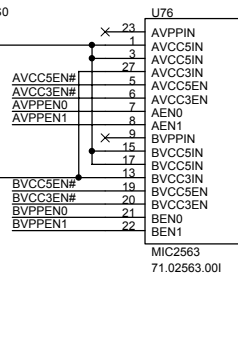
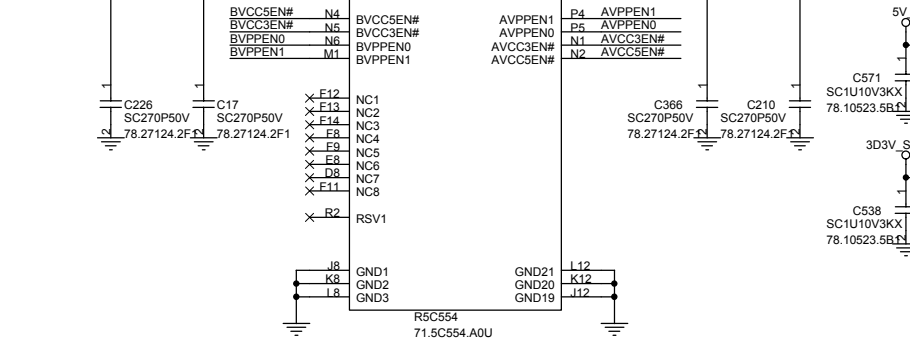
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B_CAD17	G4	BCADR24	CAD17	ACADR24	H15	A_CAD17
B_CFRAME#	G6	BCADR23	CFRAME#	ACADR23	K18	A_CFRAME#
B_CTRDY#	F2	BCADR22	CTRDY#	ACADR22	K15	A_CTRDY#
B_CDEVSEL#	F5	BCADR21	CDEVSEL#	ACADR21	L18	A_CDEVSEL#
B_CSTOP#	F1	BCADR20	CSTOP#	ACADR20	L15	A_CSTOP#
B_CBLOCK#	F4	BCADR19	CBLOCK#	ACADR19	M16	A_CBLOCK#
B_RSVD_A18	D1	BCADR18	RSVD_A18	ACADR18	M19	A_RSVD_A18
B_CAD16	D4	BCADR17	CAD16	ACADR17	K16	A_CAD16
B_CCLK	F4	BCADR16	CCLK	ACADR16	K19	A_CCLK
B_CIRDY#	F1	BCADR15	CIRDY#	ACADR15	L14	A_CIRDY#
B_CPERR#	F5	BCADR14	CPERR#	ACADR14	M18	A_CPERR#
B_CPAR	D2	BCADR13	CPAR	ACADR13	N16	A_CPAR
B_CC/BE#2	G5	BCADR12	CC/BE#2	ACADR12	P18	A_CC/BE#2
B_CAD12	A2	BCADR11	CAD12	ACADR11	N16	A_CAD12
B_CAD9	B4	BCADR10	CAD9	ACADR10	P18	A_CAD9
B_CAD14	B1	BCADR9	CAD14	ACADR9	N19	A_CAD14
B_CC/BE#1	C1	BCADR8	CC/BE#1	ACADR8	M15	A_CC/BE#1
B_CAD18	G2	BCADR7	CAD18	ACADR7	J19	A_CAD18
B_CAD20	H6	BCADR6	CAD20	ACADR6	H15	A_CAD20
B_CAD21	H4	BCADR5	CAD21	ACADR5	L12	A_CAD21
B_CAD22	H1	BCADR4	CAD22	ACADR4	G14	A_CAD22
B_CAD23	J4	BCADR3	CAD23	ACADR3	G16	A_CAD23
B_CAD24	J1	BCADR2	CAD24	ACADR2	G19	A_CAD24
B_CAD25	K4	BCADR1	CAD25	ACADR1	F16	A_CAD25
B_CAD26	K1	BCADR0	CAD26	ACADR0	F19	A_CAD26



SIGNALB SIGNALA
Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A



B_CAD8	A5	BCDATA15	CAD8	ACDATA15	P16	A_CAD8
B_RSVD_D14	D5	BCDATA14	RSVD_D14	ACDATA14	P14	A_RSVD_D14
B_CAD6	B6	BCDATA13	CAD6	ACDATA13	R18	A_CAD6
B_CAD4	F6	BCDATA12	CAD4	ACDATA12	R15	A_CAD4
B_CAD2	B7	BCDATA11	CAD2	ACDATA11	T18	A_CAD2
B_CAD30	M5	BCDATA10	CAD30	ACDATA10	C18	A_CAD30
B_CAD28	L4	BCDATA9	CAD28	ACDATA9	D18	A_CAD28
B_CAD7	A6	BCDATA7	CAD7	ACDATA7	R19	A_CAD7
B_CAD5	D6	BCDATA6	CAD5	ACDATA6	R16	A_CAD5
B_CAD3	A7	BCDATA5	CAD3	ACDATA5	T19	A_CAD3
B_CAD1	D7	BCDATA4	CAD1	ACDATA4	T18	A_CAD1
B_CAD0	E7	BCDATA3	CAD0	ACDATA3	U18	A_CAD0
B_RSVD_D2	M6	BCDATA2	RSVD_D2	ACDATA2	C19	A_RSVD_D2
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B_CAD27	L5	BCDATA0	CAD27	ACDATA0	F19	A_CAD27

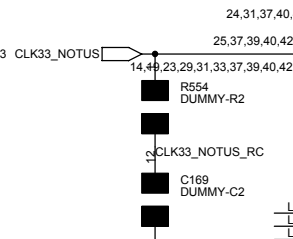


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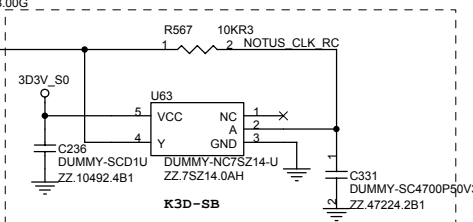
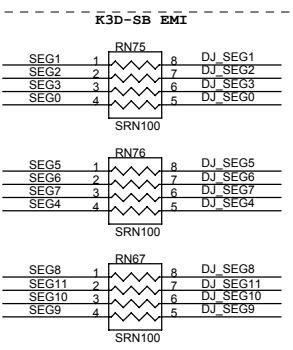
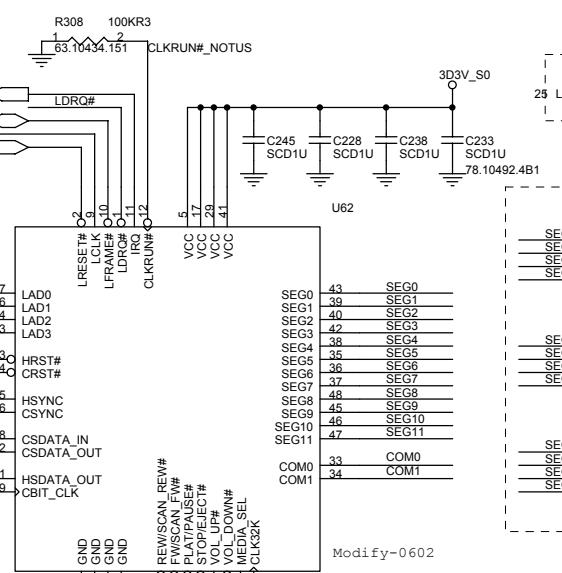
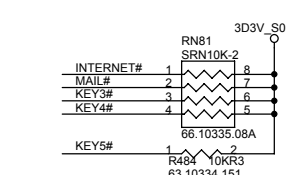
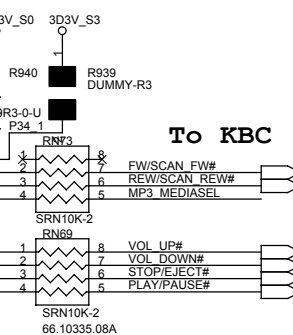
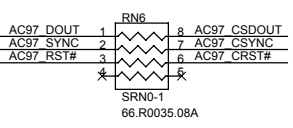
RICOH_R5C554(2/2)_CARBUS

Title: _____
Size: A3 Document Number: _____ Rev: -1
Date: Thursday, December 04, 2003 Sheet: 32 of 51

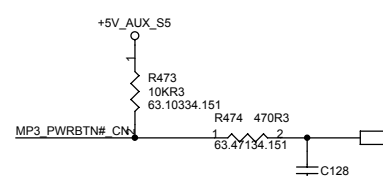
25.37.39.40.42 LPC_LAD[3..0]



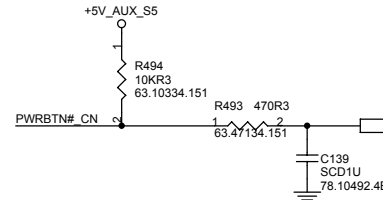
**For Non-MP3 Model
PUT INSIDE OZ263**



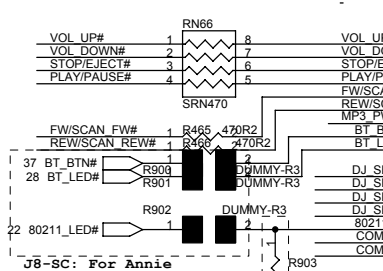
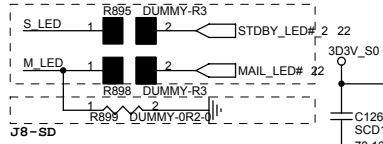
MP3 POWER BUTTON



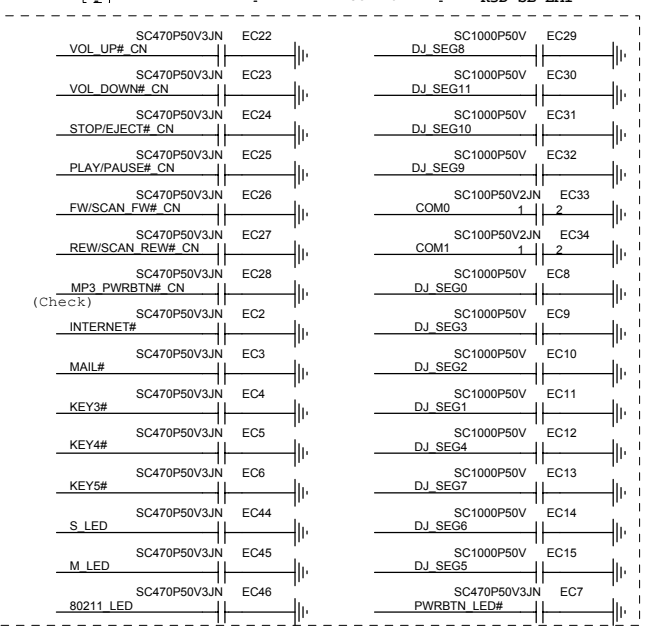
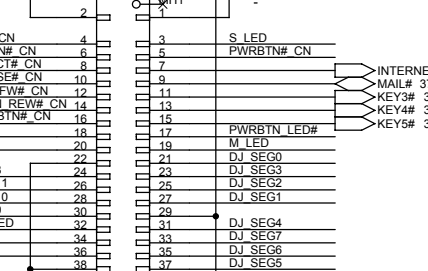
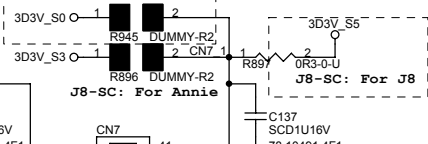
POWER BUTTON



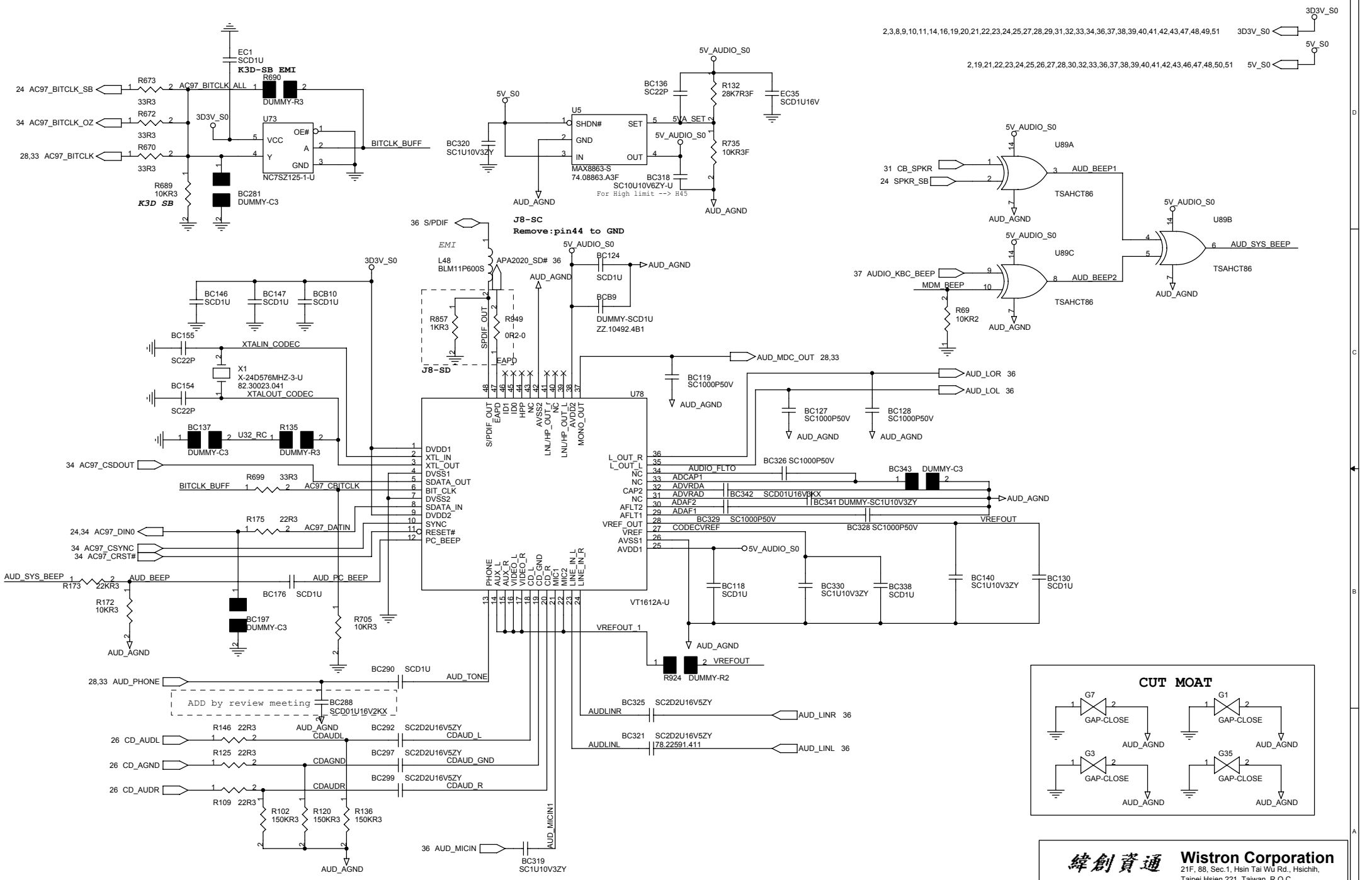
J8-SC: For Annie



J8-SC: For Annie



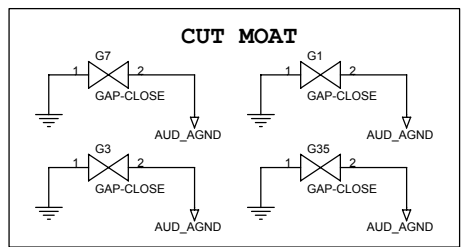
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2,3,8,9,10,11,14,16,19,20,21,22,23,24,25,27,28,29,31,32,33,34,36,37,38,39,40,41,42,43,47,48,49,51 3D3V_S0

2,19,21,22,23,24,25,26,27,28,30,32,33,36,37,38,39,40,41,42,43,46,47,48,50,51 5V_S0

J8-SC
Remove:pin44 to GND



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Title: **AUDIO (1/2) -- CODEC VT1612A**

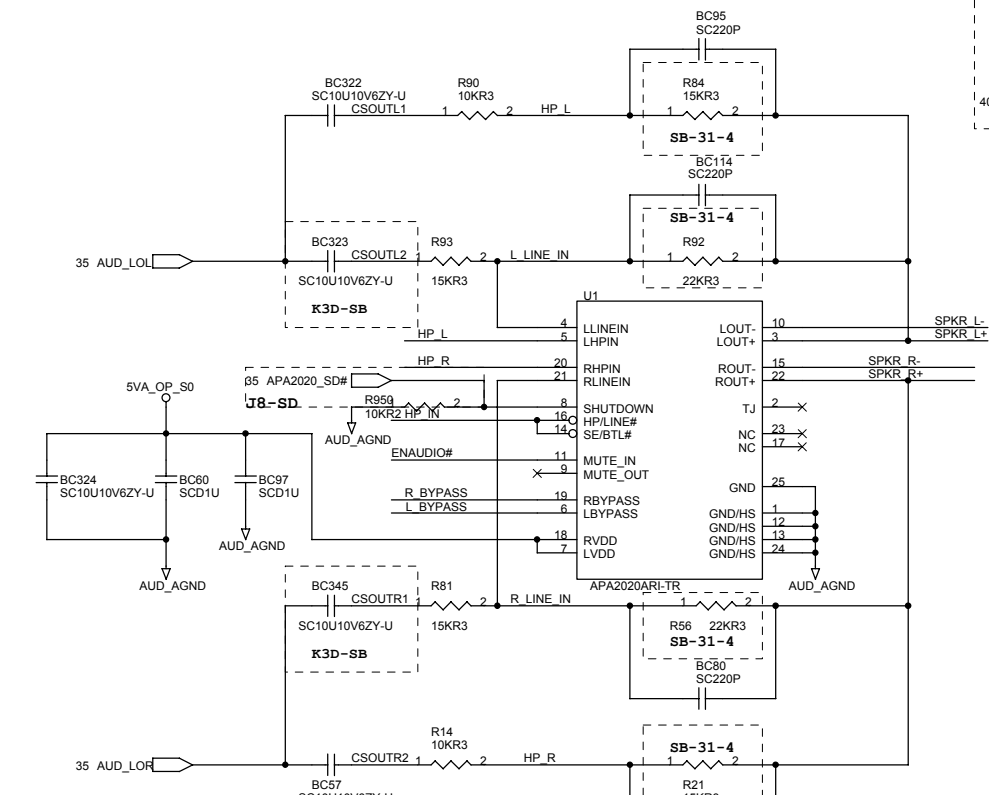
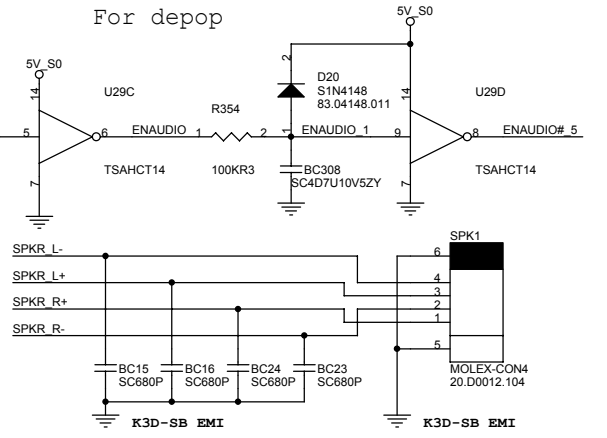
Size: A3	Document Number: Gannet	Rev: -1
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Date: Thursday, December 04, 2003 Sheet 35 of 51

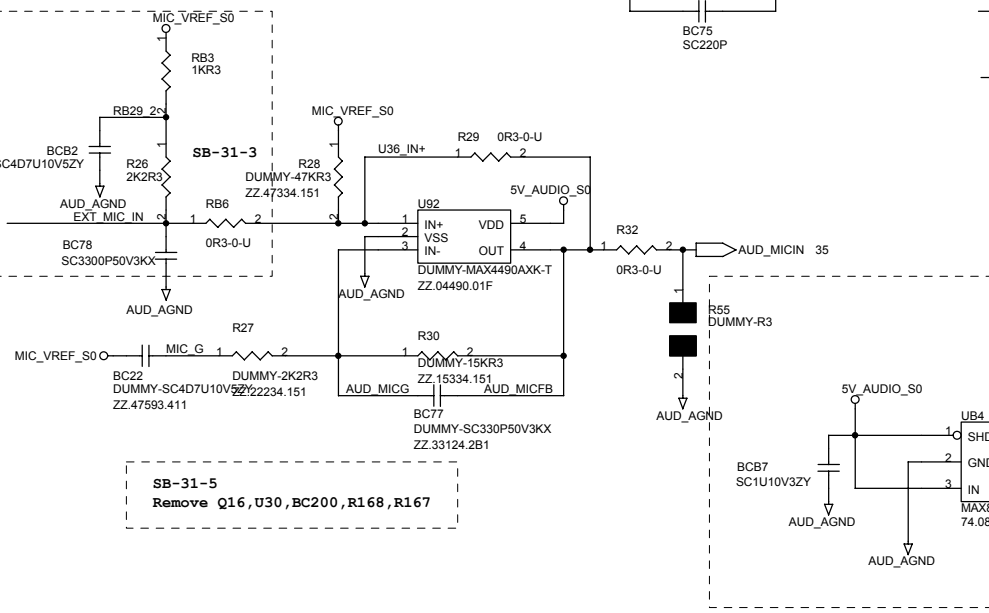
J8-SC
Delete "Bo" sound

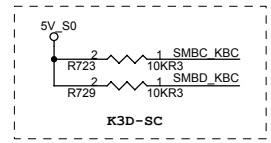
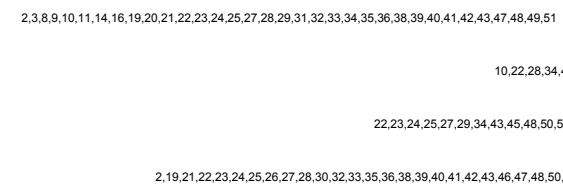


For depop

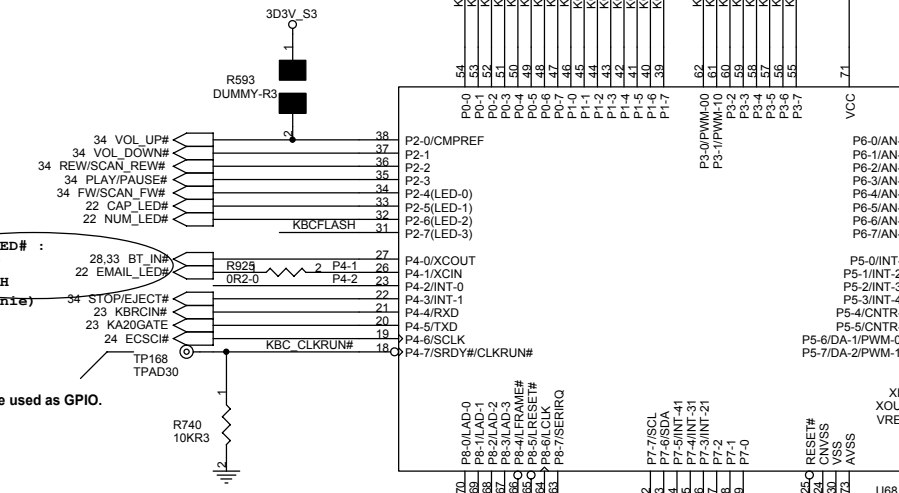
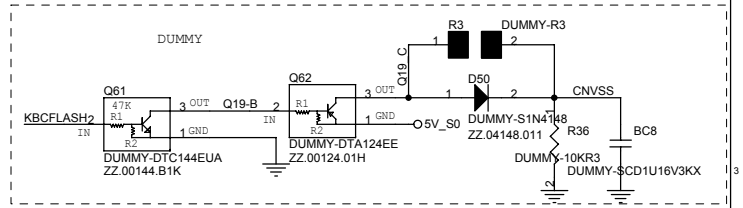
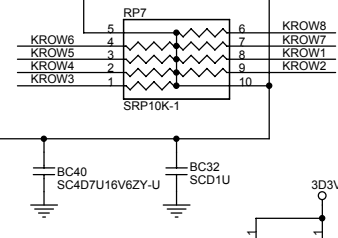


MIC PREAMP

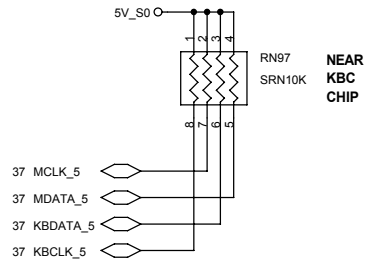




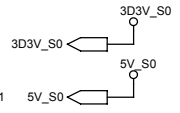
NEAR M38859



PS/2 CONN

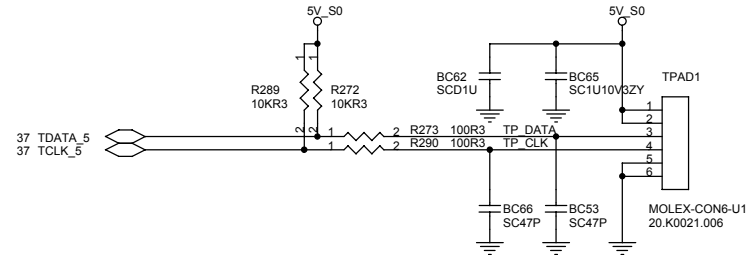


2,3,8,9,10,11,14,16,19,20,21,22,23,24,25,27,28,29,31,32,33,34,35,36,37,39,40,41,42,43,47,48,49,51

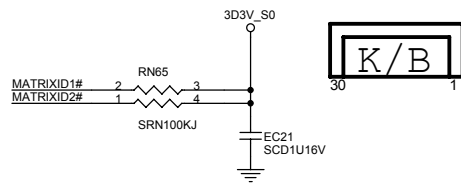


2,19,21,22,23,24,25,26,27,28,30,32,33,35,36,37,39,40,41,42,43,46,47,48,50,51

TOUCH PAD



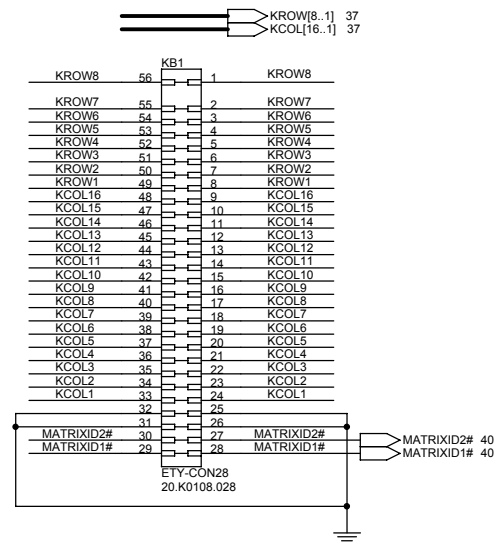
Internal Keyboard CONN



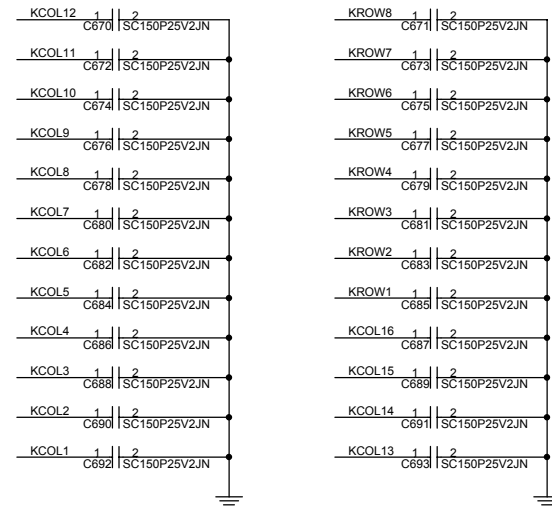
SB

Keyboard matrix (from vendor)

	US	Jap	Eur	Other	
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

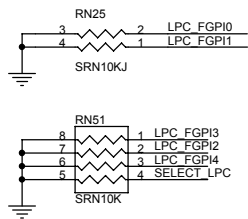


7/09 EMI Bypass cap.

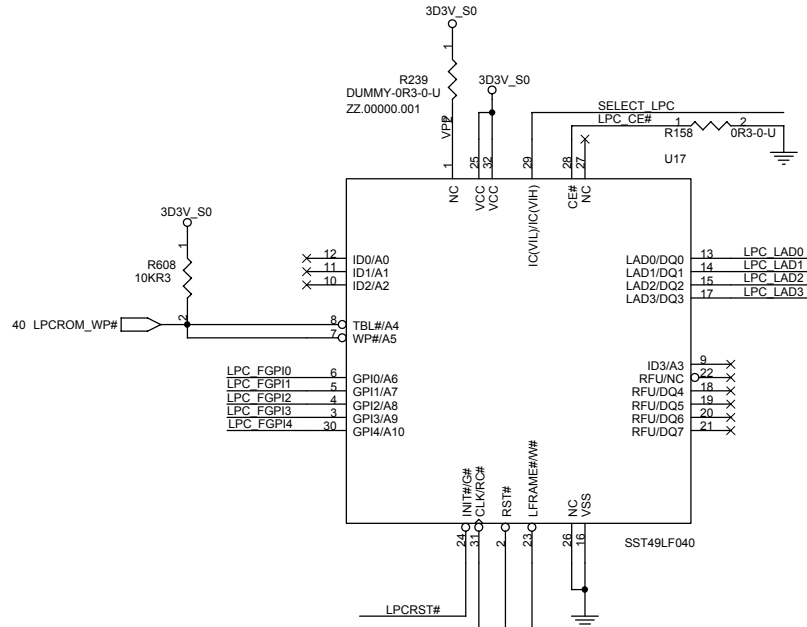
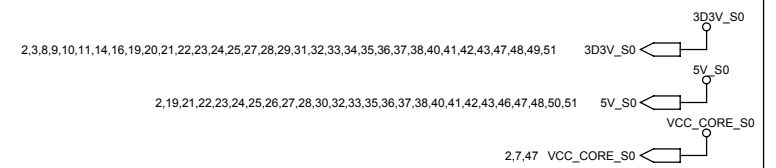
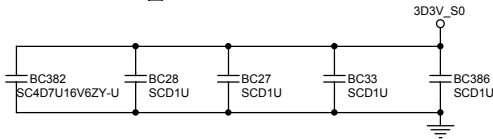


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Title			PS2 / TOUCHPAD / KB CONN	
Size	Document Number		Rev	
A3	Gannet		-1	
Date: Thursday, December 04, 2003			Sheet	38 of 51



25,34,37,40,42 LPC_LAD[3..0]

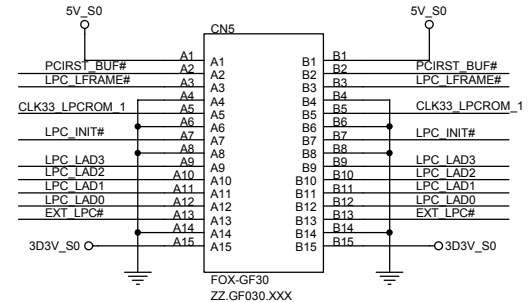


TOP VIEW

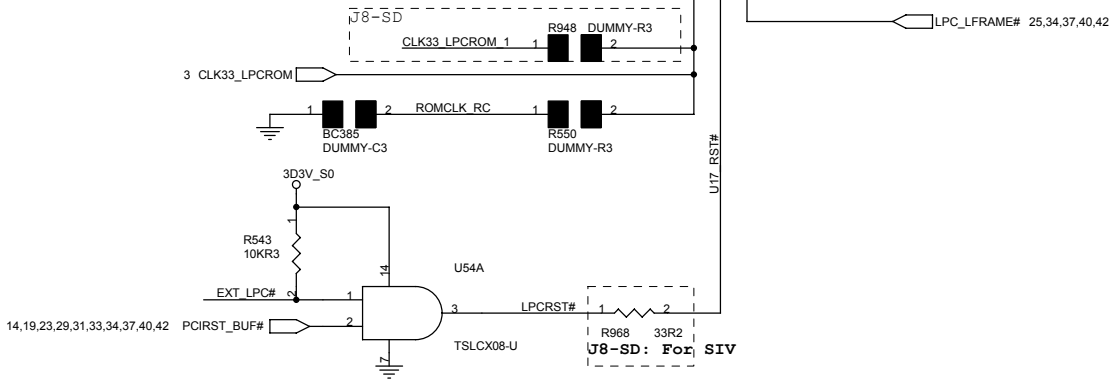
- A15 (B1)
- A14 (B2)
- ...
- A2 (B14)
- A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

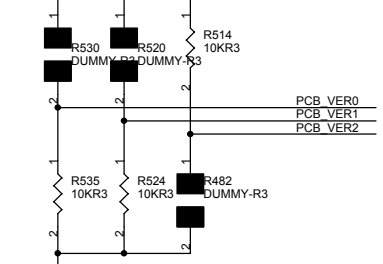
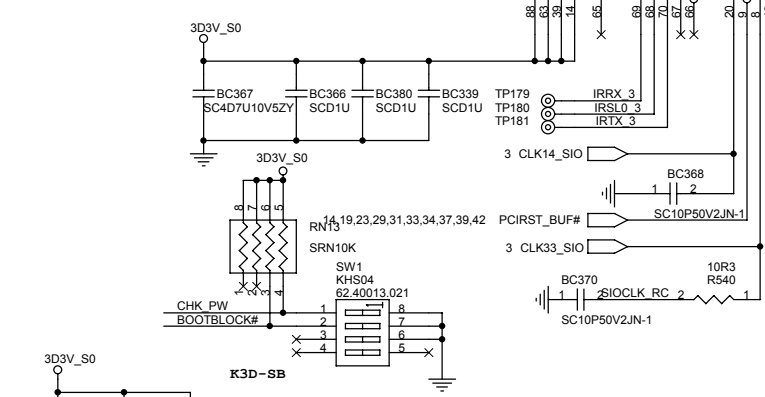
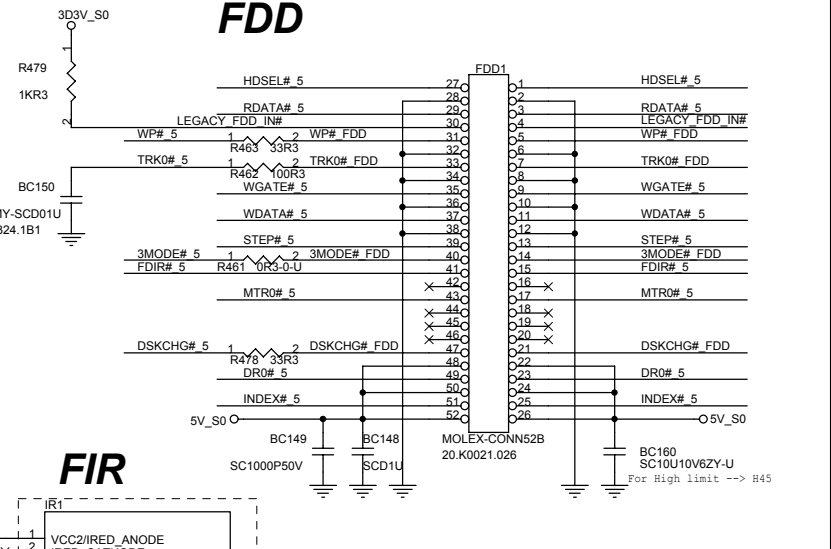
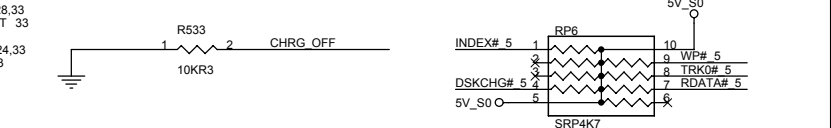
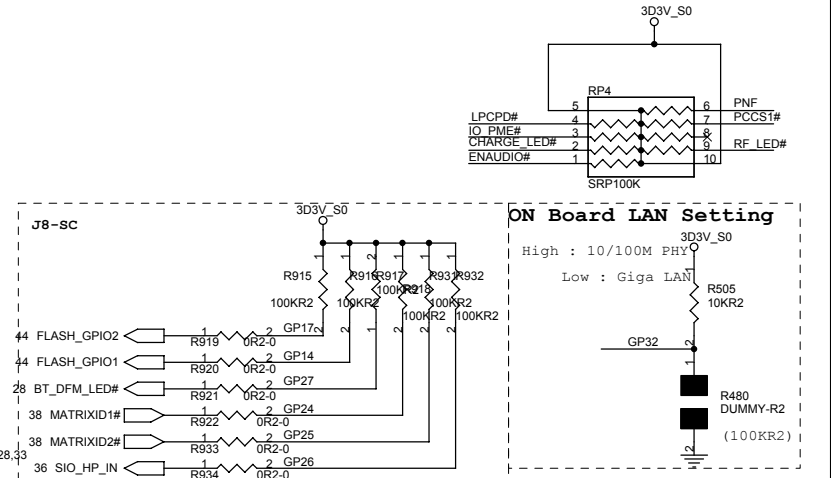
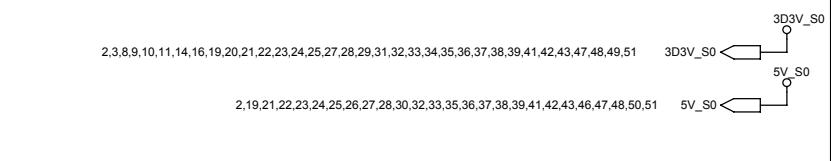
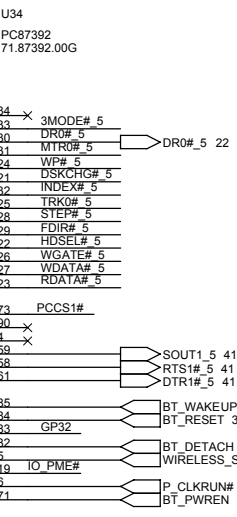
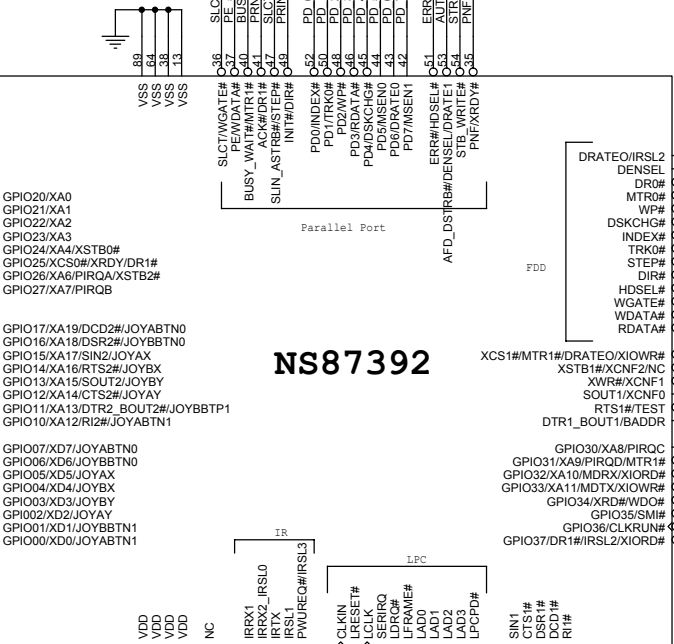
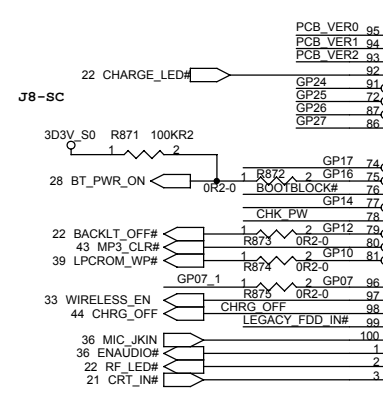
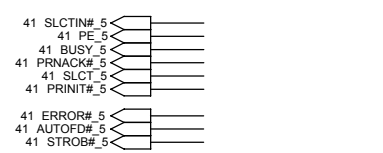
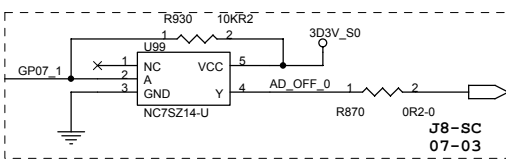


PLCC 32pin ST: 72.50040.003
 PLCC 32pin SST:
 72.49004.B03



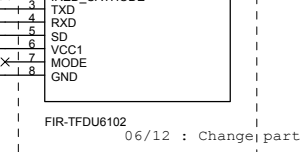
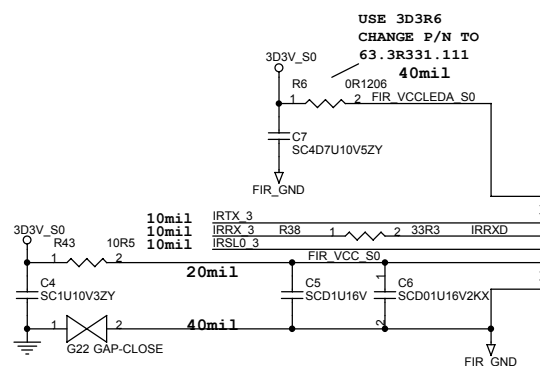
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 Taipei Hsien 221, Taiwan, R.O.C.

Title LPCROM / DEBUG PORT		
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003 Sheet 39 of 51		



K3D Board Ver. Setting

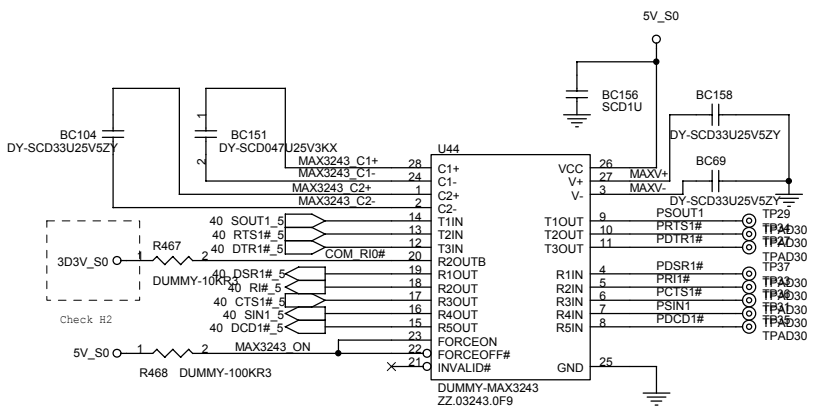
Ver.	PCB_VER0	PCB_VER1	PCB_VER2
SA	0	1	1
SB	0	1	0
SC	1	1	0
SD	0	0	1
-1	1	0	1
-2	1	1	1



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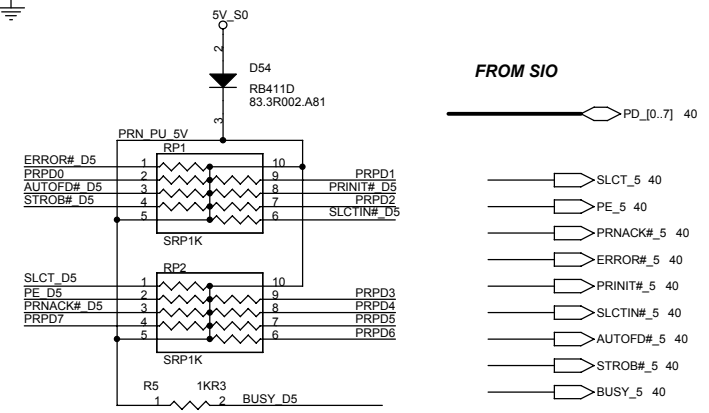
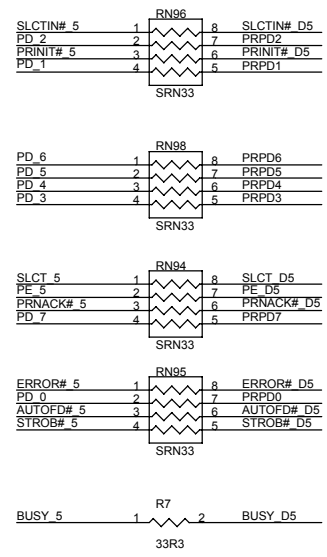
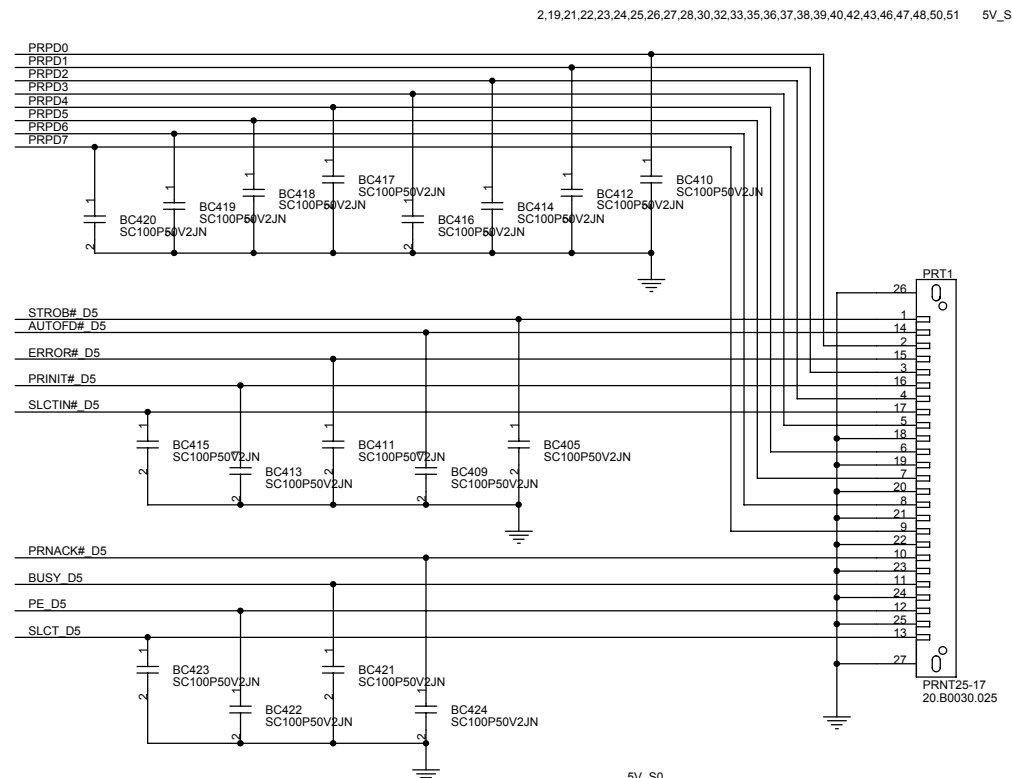
SUPER IO
 Document Number: Gannet
 Date: Thursday, December 04, 2003 Sheet 40 of 51

SERIAL PORT



SA DV-3 Change MAX3243CDB TI to MAX3243 MAXIM

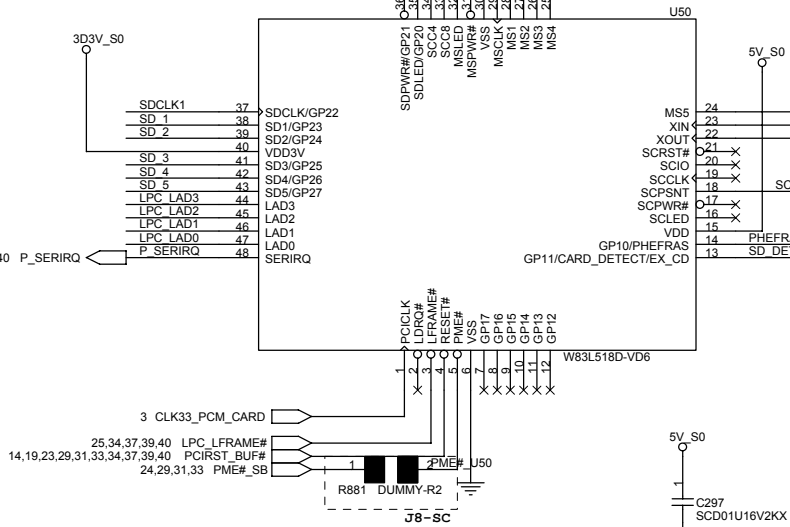
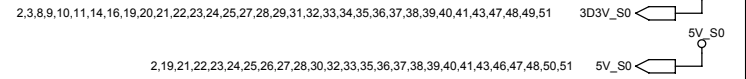
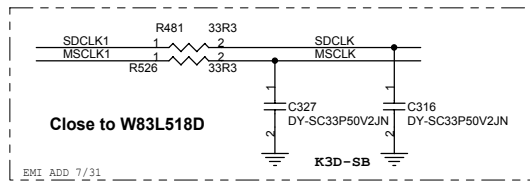
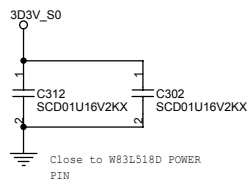
PRINTER PORT



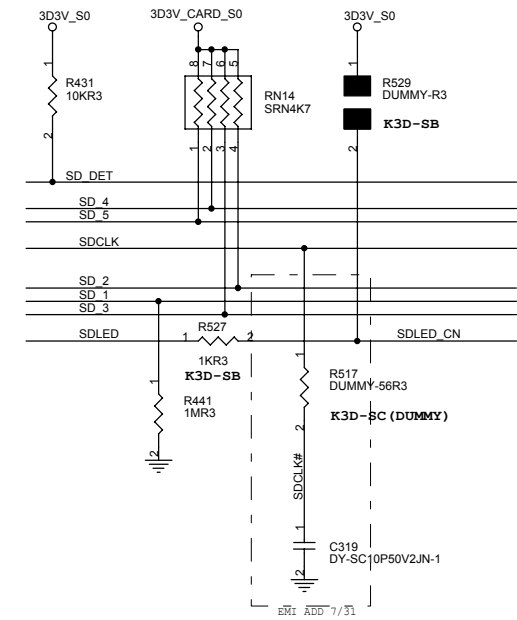
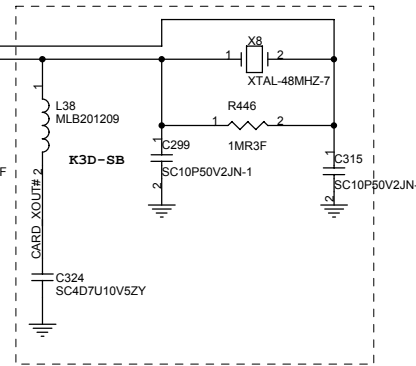
CHECK PULL HIGH

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Title		PORTS	
Size	A3	Document Number	Gannet
Date:	Thursday, December 04, 2003	Sheet	41 of 51
Rev	-1		



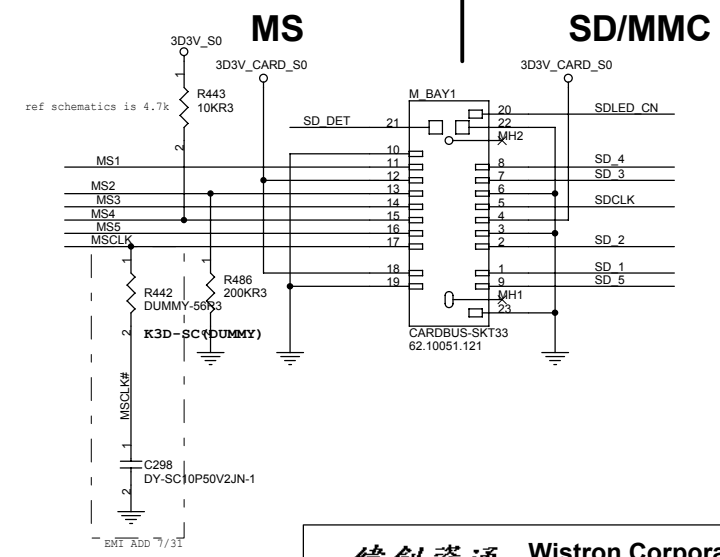
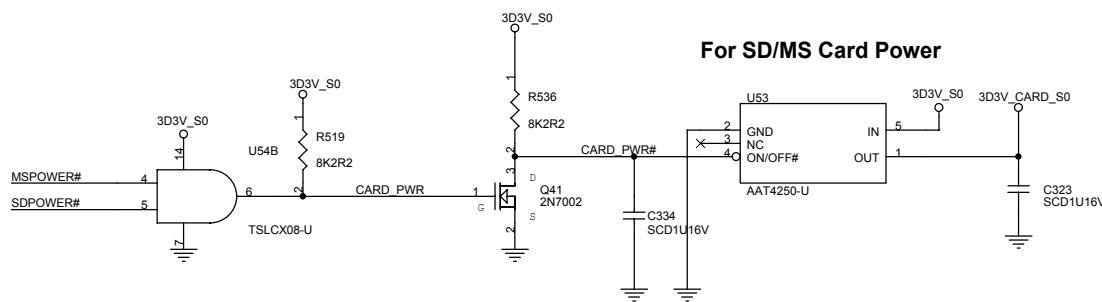
Close to W83L518D



25,34,37,39,40 LPC_LAD[0..3]

Pull-low : Addr - 4E h
PHEFRAS
ref schematics is 4.7k
R432 10KR3

For SD/MS Card Power

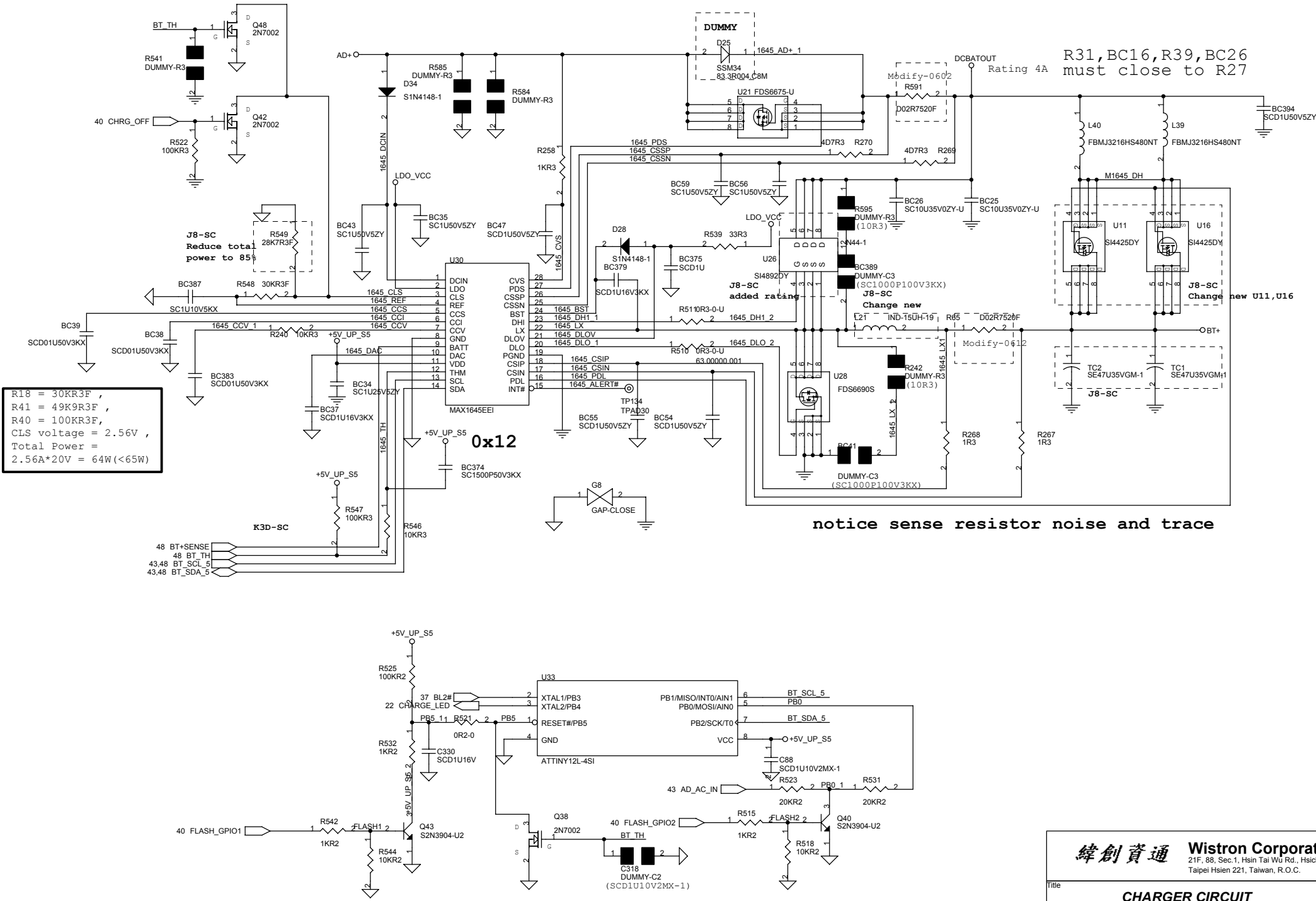


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Title: **CARD READER/MS/SD**

Size: A3	Document Number: Gannet	Rev: -1
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Date: Thursday, December 04, 2003 Sheet 42 of 51



R18 = 30KR3F ,
 R41 = 49K9R3F ,
 R40 = 100KR3F ,
 CLS voltage = 2.56V ,
 Total Power =
 2.56A*20V = 64W (<65W)

0x12

notice sense resistor noise and trace

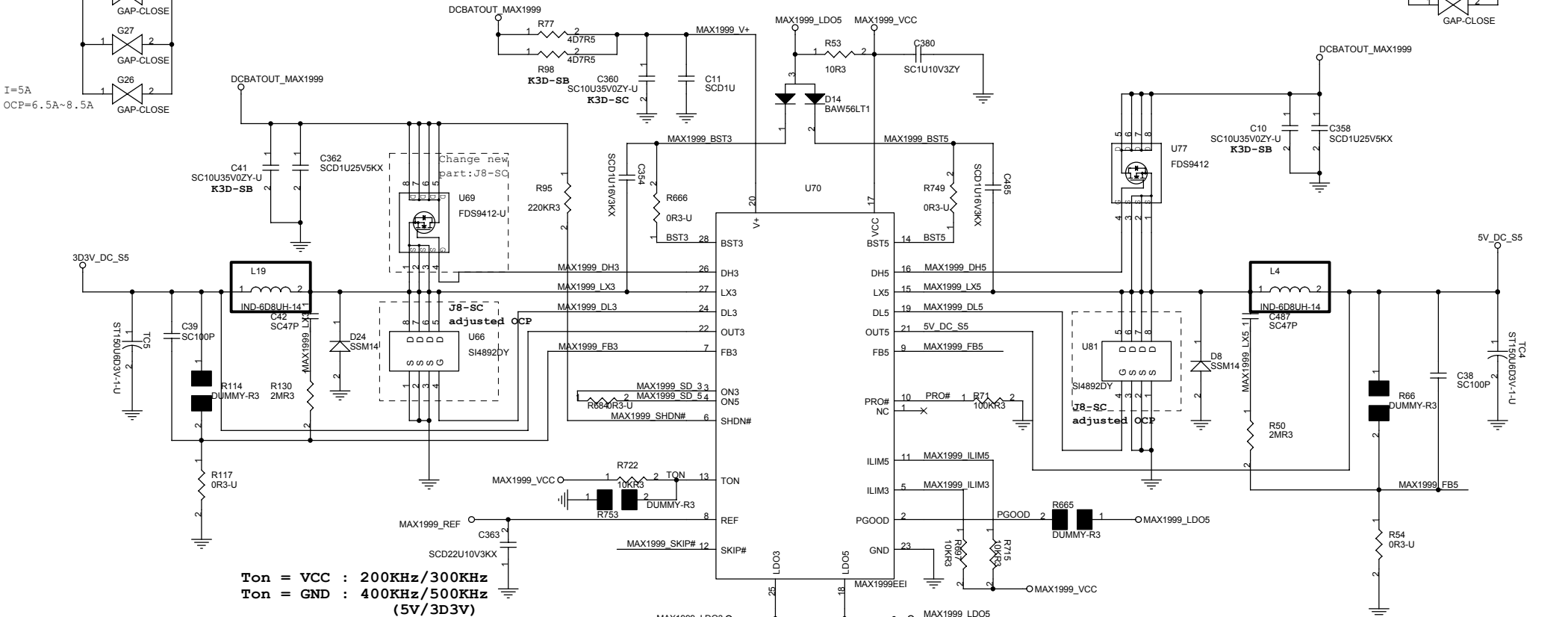
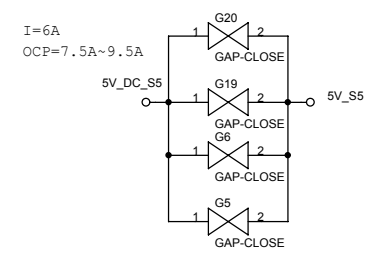
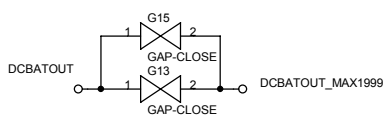
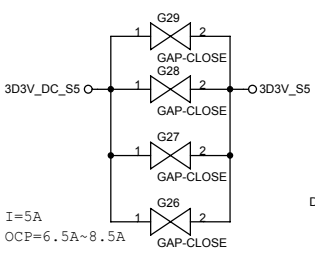
R31, BC16, R39, BC26 must close to R27

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Title		
CHARGER CIRCUIT		
Size	Document Number	Rev
A3	Gannet	-1
Date: Thursday, December 04, 2003		
Sheet 44		of 51

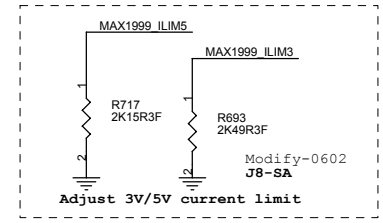
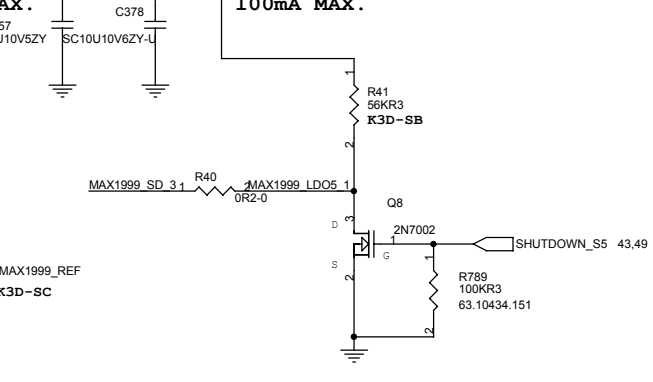
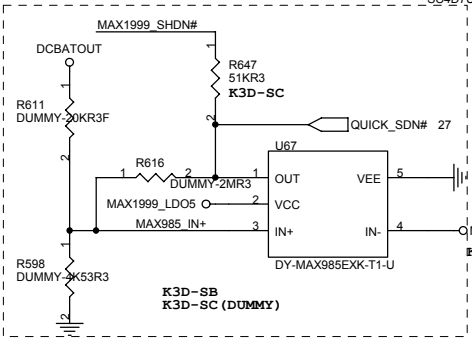
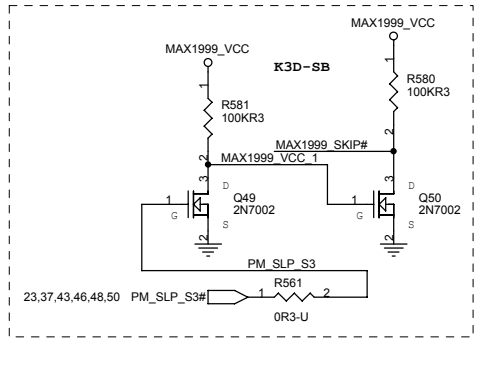
SYSTEM DC/DC

3D3V_S5/5V_S5/1D5V_S5/UP+5V



Ton = VCC : 200KHz/300KHz
Ton = GND : 400KHz/500KHz
(5V/3D3V)

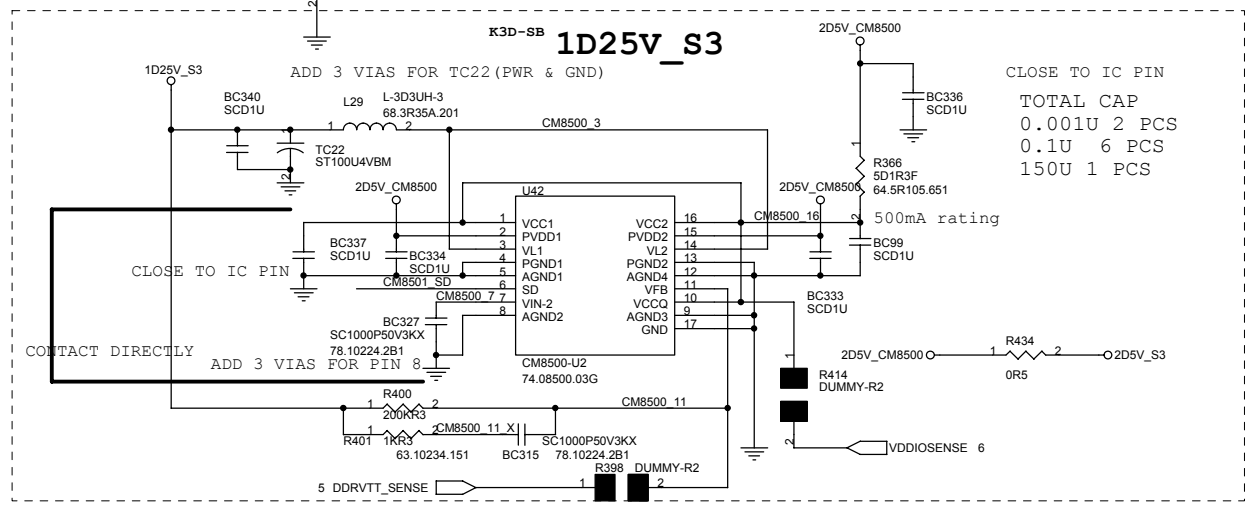
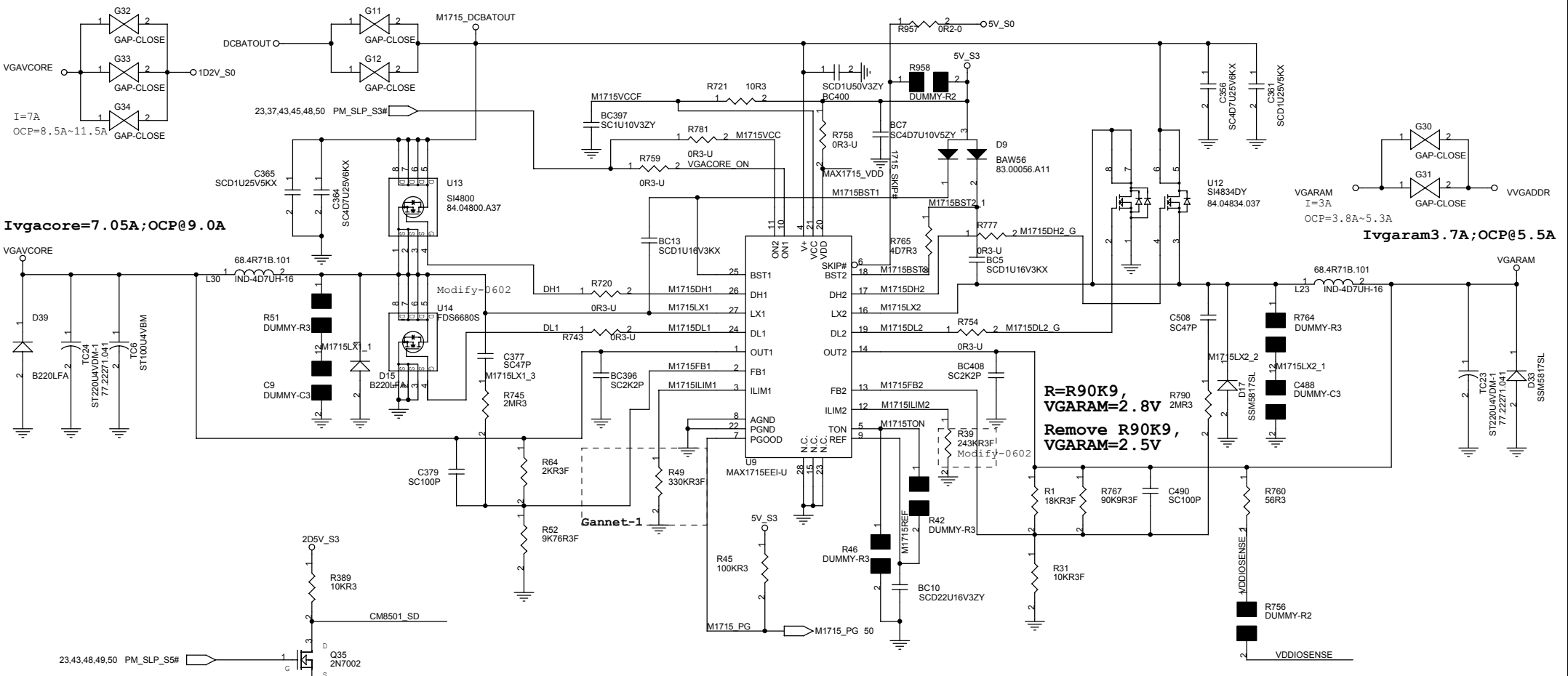
100mA MAX.
100mA MAX.



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Title		
MAX1999/3D3V_S5/5V_S5		
Size	Document Number	Rev
A3		-1
Gannet		
Date: Thursday, December 04, 2003	Sheet 45	of 51

VGAPOWER / 1D25V_S0 / Charger Connector



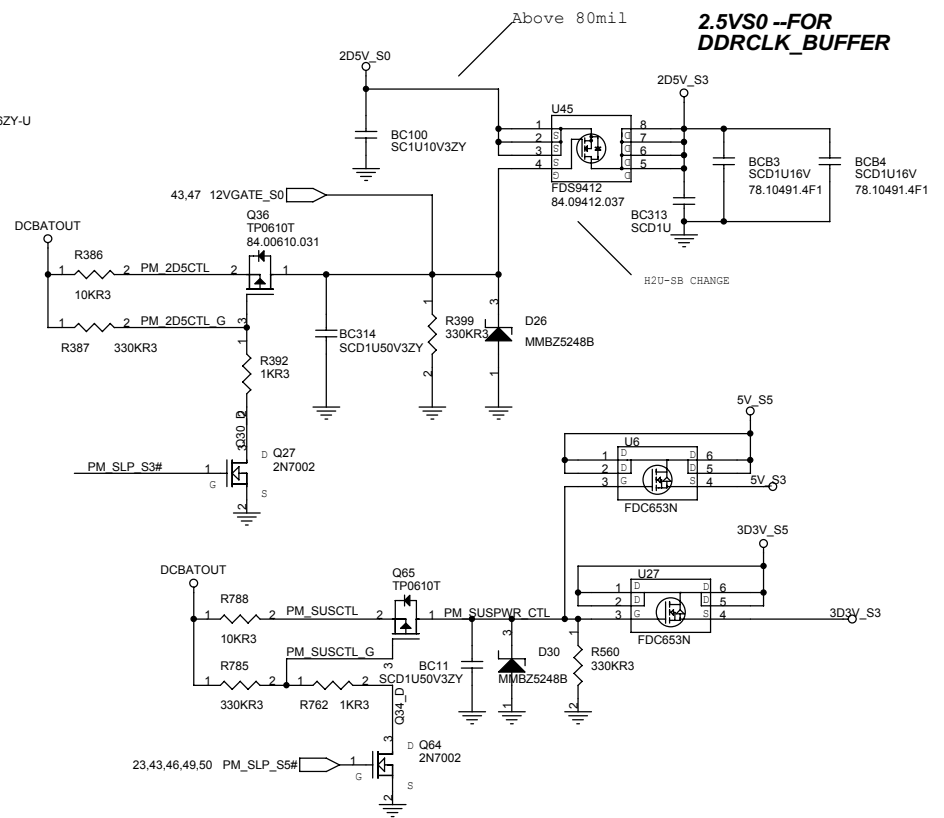
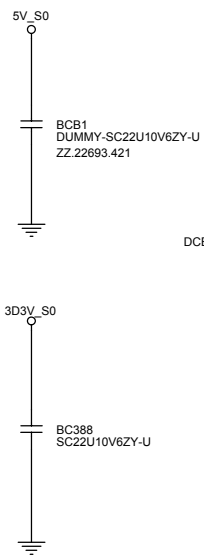
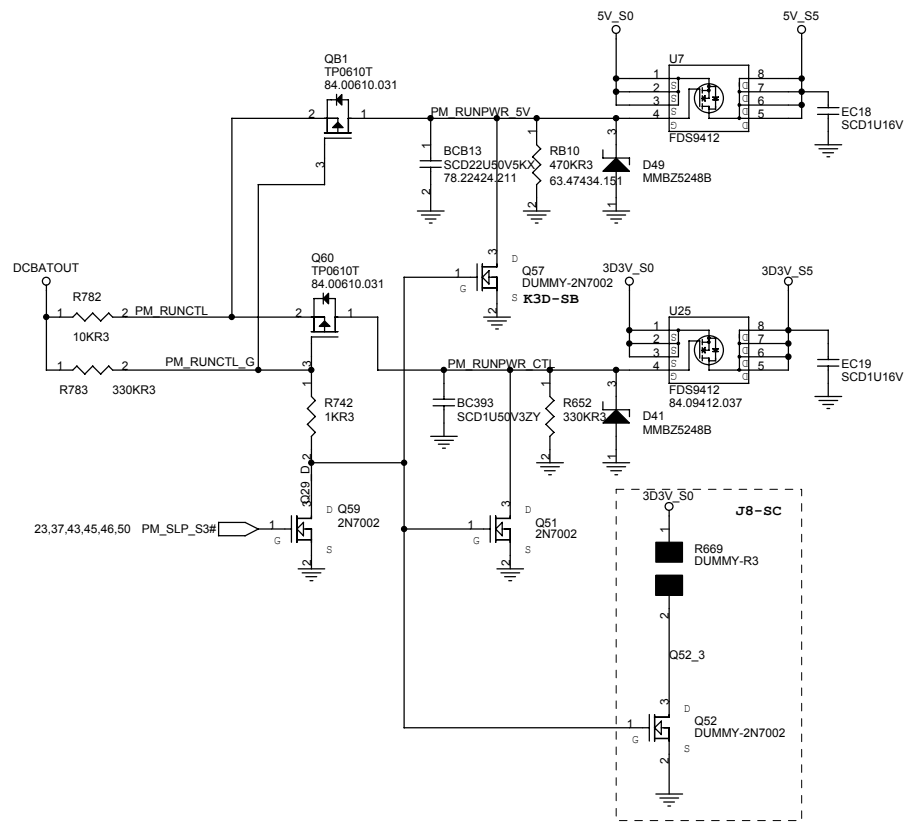
CLOSE TO IC PIN
TOTAL CAP
0.001U 2 PCS
0.1U 6 PCS
150U 1 PCS

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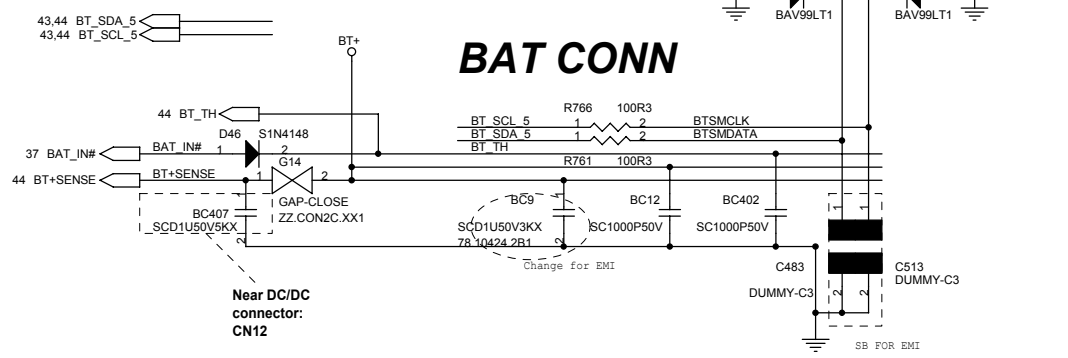
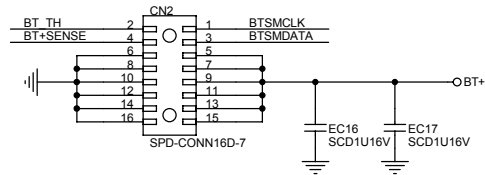
Title: **VGAPOWER / 1D25V_S3**

Size: A3 Document Number: **Gannet** Rev: -1

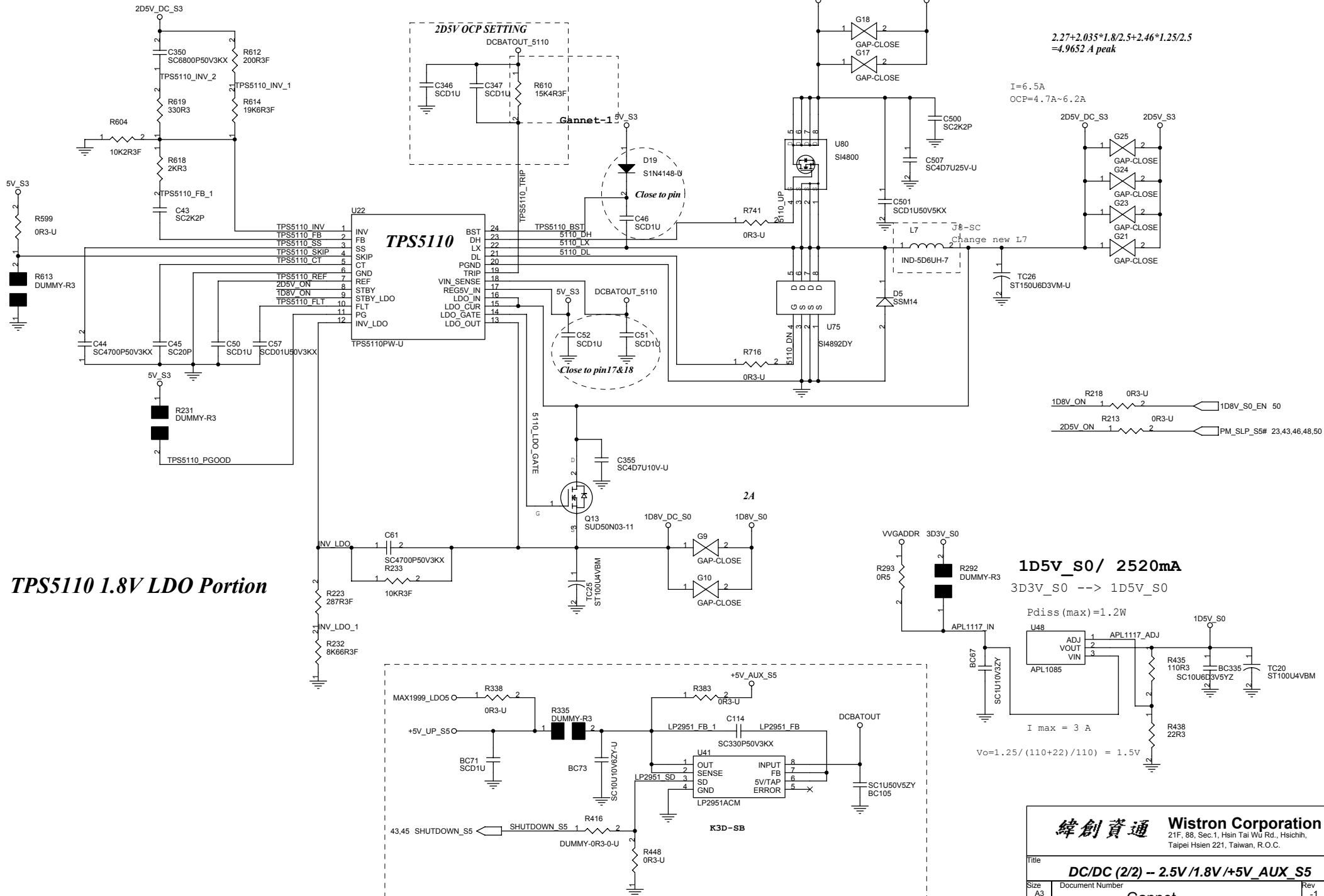
Date: Thursday, December 04, 2003 Sheet: 46 of 51



Charger CONN



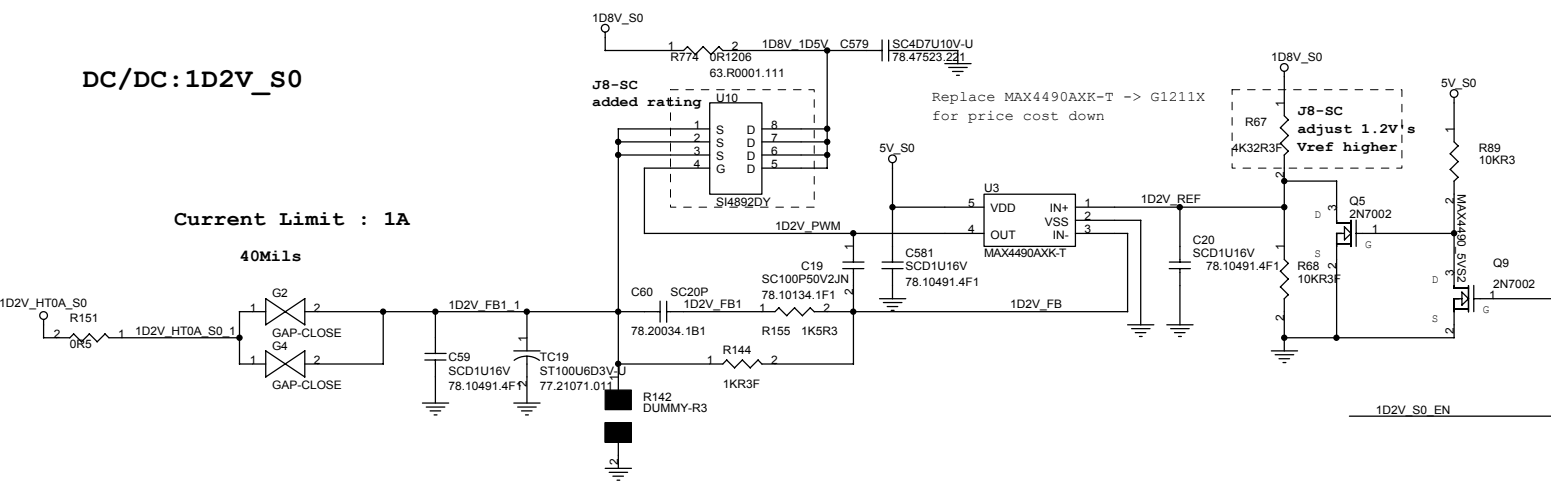
DC/DC (2/3) -- 2.5V /1.8V



DC/DC:1D2V_S0

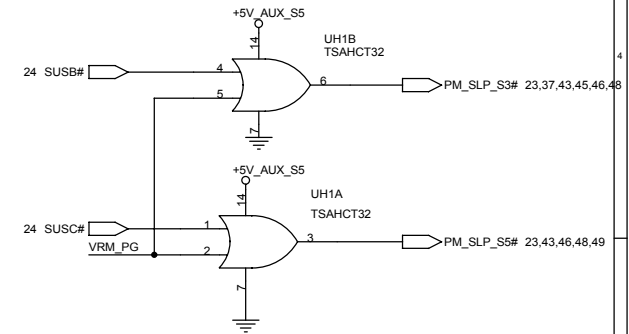
Current Limit : 1A

40Mils

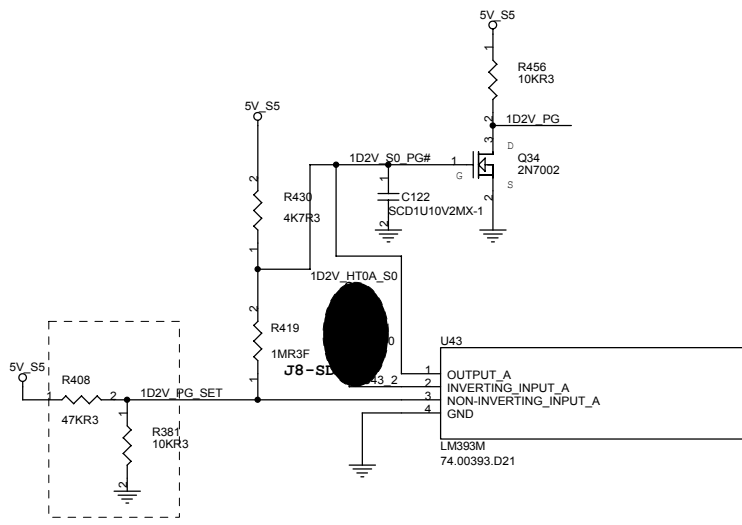
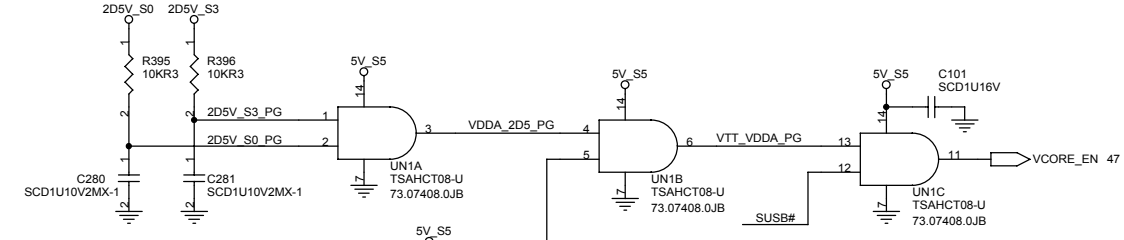


Replace MAX4490AXK-T -> G1211X for price cost down

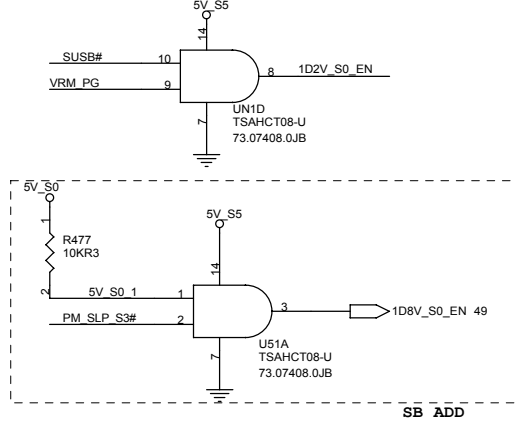
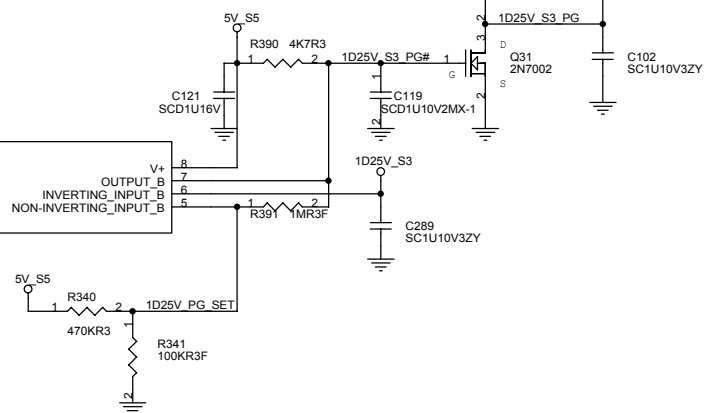
J8-SC
adjust 1.2V₁s
Vref higher



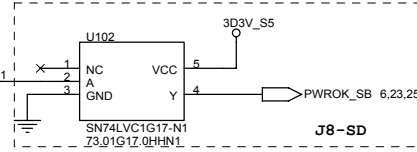
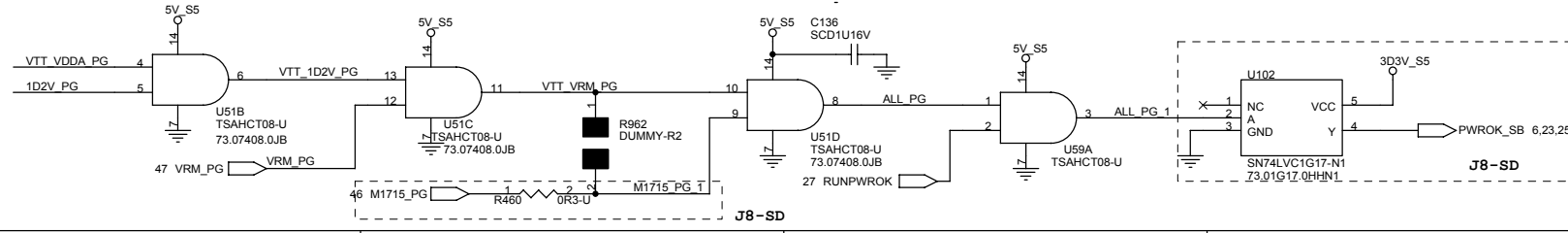
For CPU power off sequence



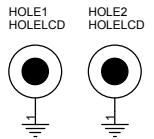
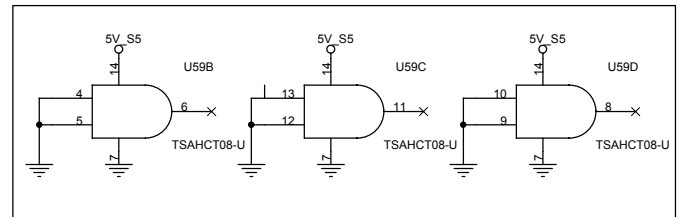
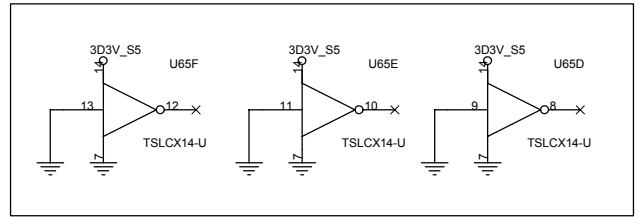
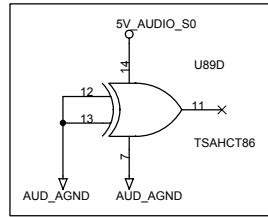
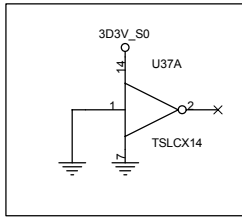
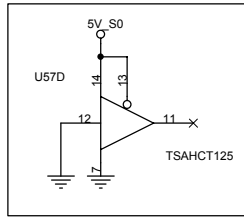
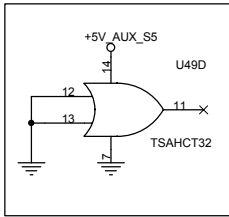
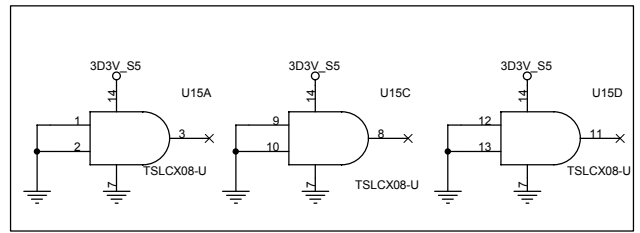
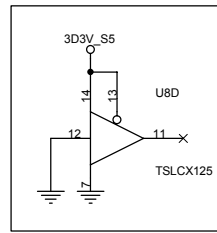
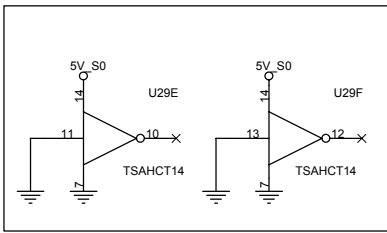
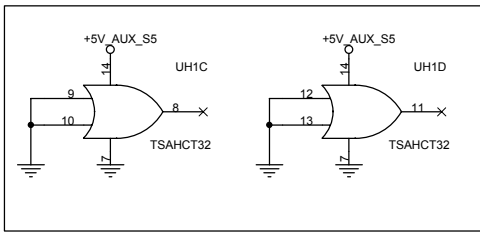
SB change R583 from 470KR3 to 47KR3, R584 from 100KR3 to 10KR3



SB ADD



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POWERGOOD&ENABLES	
Size	Document Number
Custom	Gannet
Date: Thursday, December 04, 2003	Sheet 50 of 51



MDC Stand Off
P/N:
34.41Q08.001

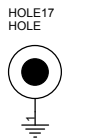


LCD Stand Off
P/N:
34.41T01.001



DC/DC Stand Off
P/N:
34.41T02.001

SPARE GATES



S3:34.42P26.001



S1:34.39S03.001



34.42P26.001

J8-SD
MODIFY
BY EMI.



34.42P26.001



ZZ_NDPAD.XXX

J8-SD
MODIFY BY EMI



ZZ_NDPAD.XXX

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Taippei Hsien 221, Taiwan, R.O.C.

Title MISC		
Size A3	Document Number Gannet	Rev -1
Date: Thursday, December 04, 2003 Sheet 51 of 51		