Compal Confidential

NEWX5 / PEW56 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

2010-06-17

LA5912P REV: 1.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/10/06	Deciphered Date 2010/03/12	Title: SCHEMATICS, MB A5912
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Model Name : NEWX5 / PEW56
File Name : LA-5912P
P/N : DA60000FZ10

Danube

AMD S1G4 Processor
uPGA-638 Package
Champlain page 6,7,8,9

Memory BUS(DDR3)
Dual Channel
1.5V DDRIII 1066~1333MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3 page 10,11

Hyper Transport Link
16 x 16

ATI RS880M
uFCBGA-528
page 12,13,14

LVDS page 16
CRT page 18
HDMI Conn. page 17

Thermal Sensor ADM1032 page 8
Clock Generator ICS9LPRS488 page 15

A link Express2
Gen1

ATI SB820M
uFCBGA-605
page 19,20,21,22,23

page 28	page 16	page 28	page 27	page 28	page 28
USB conn X 3	CMOS Camera	Bluetooth Conn <Option>	Mini card (WL)X1	3G/GPS WWAN <Option>	Card Reader
USB port 0,1,2	USB port 5	USB port 12	USB port 8	USB port 9	USB port 6

3.3V 48MHz
USB
3.3V 24.576MHz/48Mhz
HD Audio

S-ATA Gen2

MINI Card 1
WLAN page 36
GPP1

LAN(GbE)
Broadcom BCM57780 page 25
GPP0

RJ45 page 26

LPC BUS

SATA HDD Conn. page 24
port 0

SATA ODD Conn. page 24
port 1

HDA Codec ALC272X page 31

Audio AMP page 32

Phone Jack x2 page 32

ENE KB926 page 29

Touch Pad page 30
Int.KBD page 30
EC I/O Buffer page 30
BIOS page 30

LED page 30
RTC CKT. page 19
LID SW / MEDIA/B page 30
Power On/Off CKT. page 33
DC/DC Interface CKT. page 34
Power Circuit page 35,36,37,38,39,40,41,42,43

Fan Control page 33

Extend Card/B
1. USB X2
2. Cardreader RTS5160
w/ 5IN1 Conn.
w/ 2IN1 Conn.

PCB

ZZZ
NEWX5
LA-5912P MB Rev1: DA60000FZ10
LA-5912P MB DAZ0C600100
LA-5912P REV1 M/B
NEWX5@

ZZZ1
PEW56
LA-5912P MB Rev1: DA60000FZ10
LA-5912P MB DAZ0GJ00100
LA-5912P REV1 M/B
PEW56@

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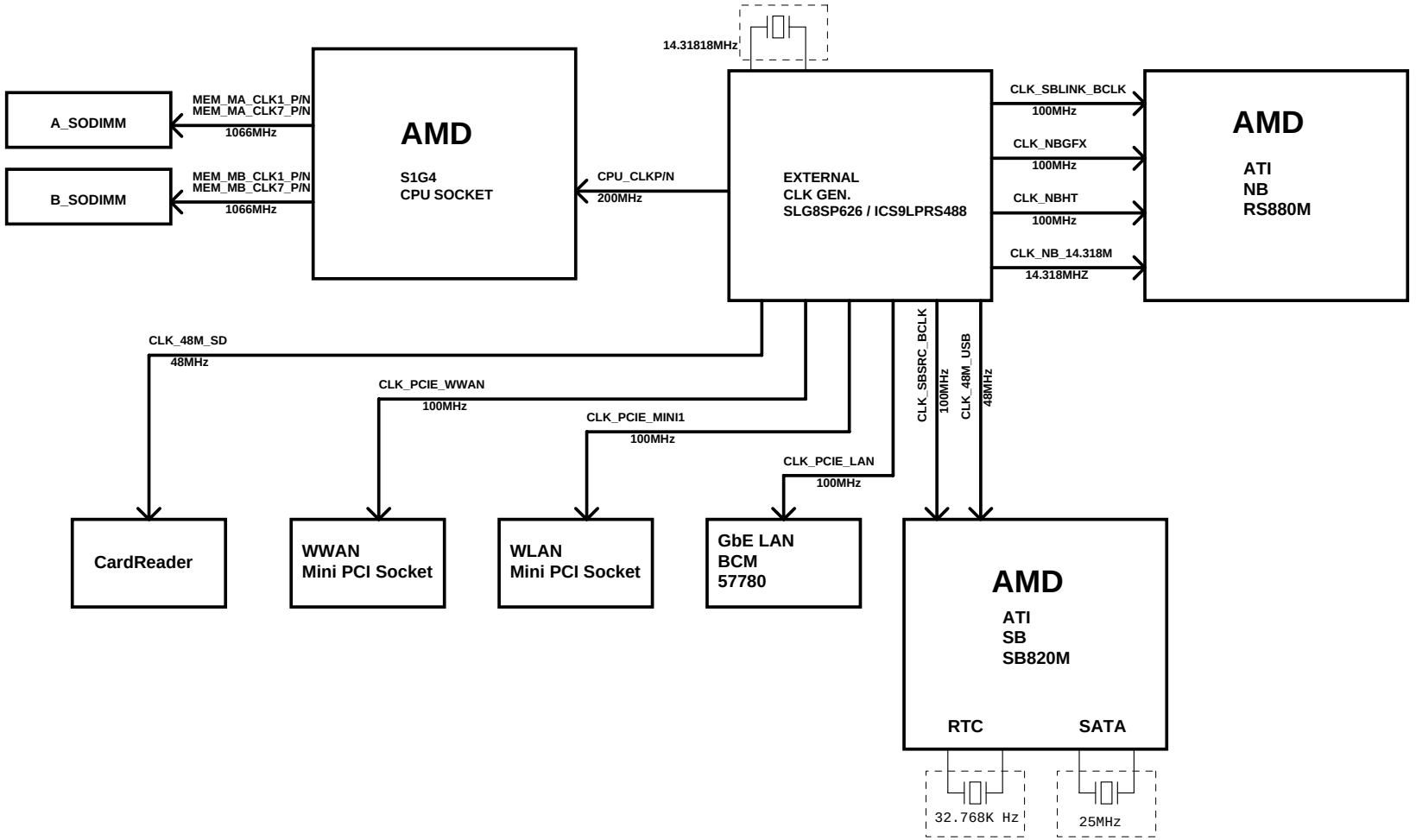

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (1.375-1.5V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+CPU_VDDR	1.05V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V power rail for MINI Card	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
SB-Temp Sensor		98H

SB820 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB820 SM Bus 1 address

Device	Address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	*NEWX5 / PEW56 PVT stage (w/ pach code)*
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	*NEWX5*
1	*PEW56*
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Internal CLK	INT@
External CLK	EXT@
Vari-Bright	VB@
No Vari-Bright	UNVB@
HDMI	HDMI@
NEWX5	NEWX5@
PEW56	PEW56@
NEW75/85 LED	7585@
NEW95/PEW56 LED	9556@
Bluetooth	BT@
3G	3G@

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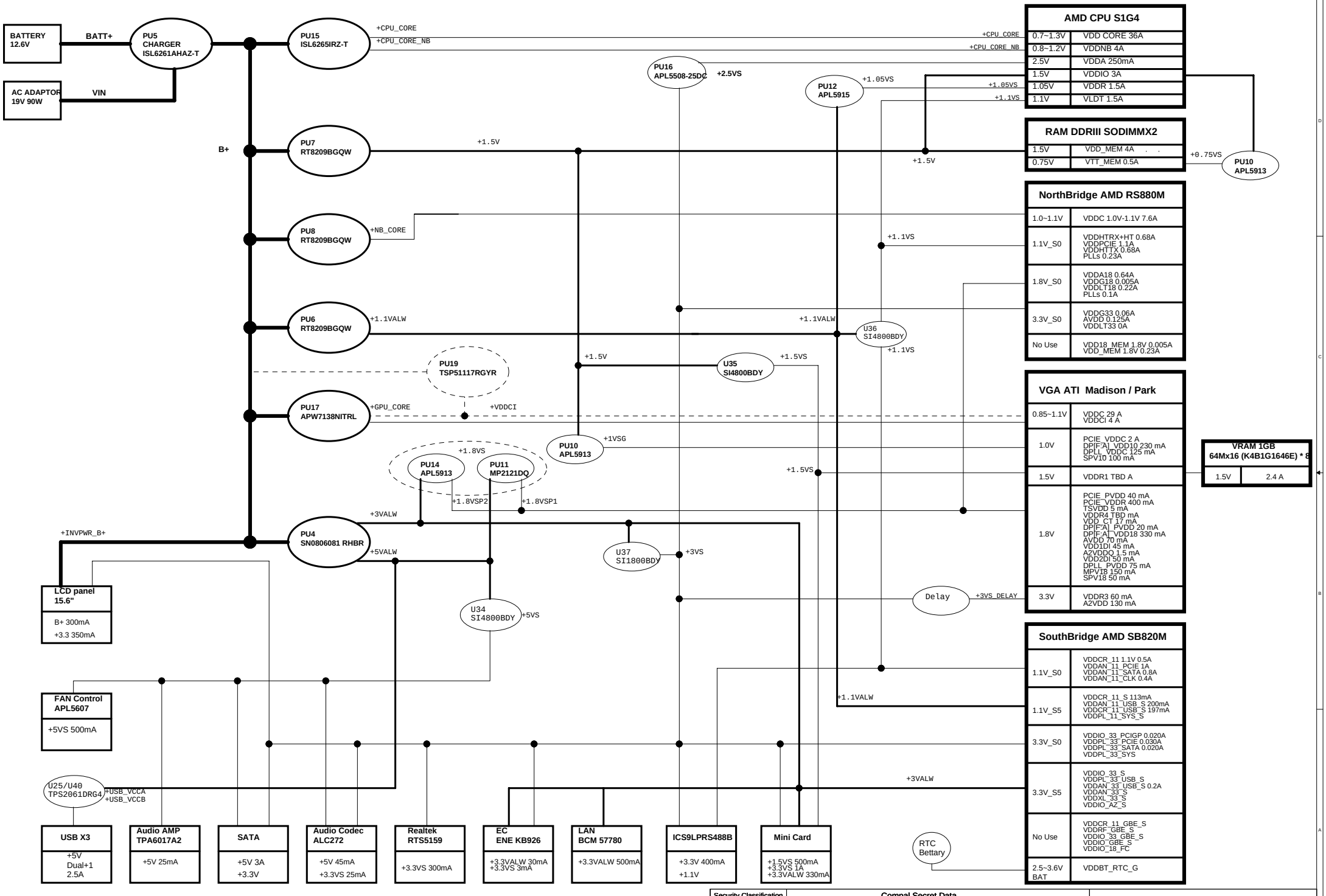

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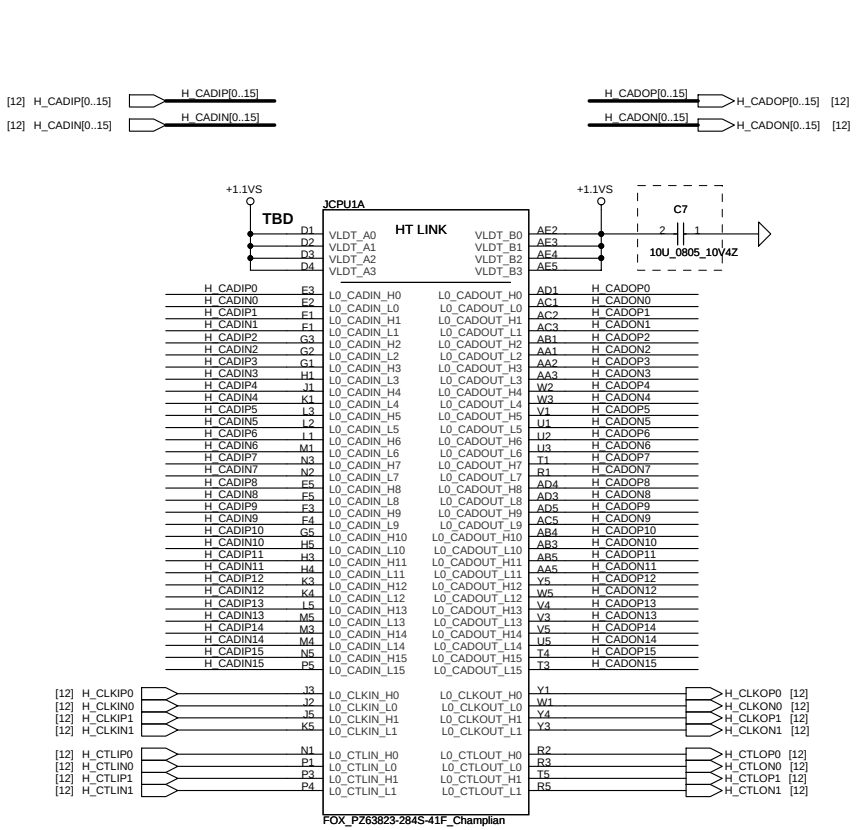
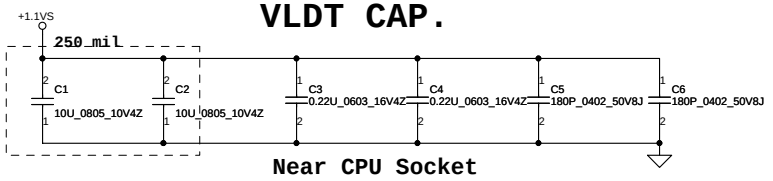


VLDT CAP.



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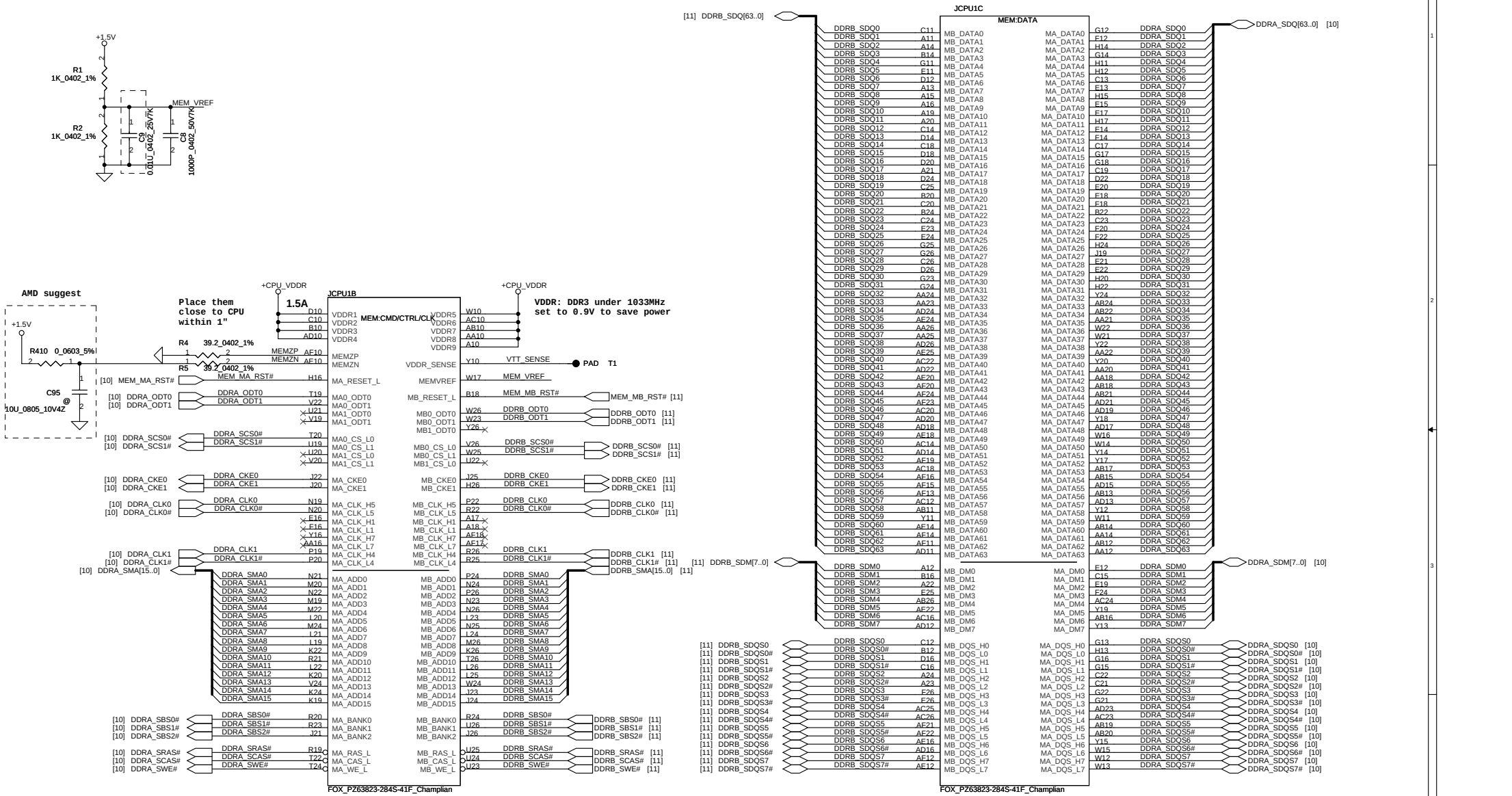
Processor DDR3 Memory Interface



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Champlain: C1E
C1E: LDT_REQ# no connect
CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
no support in S1g4

VDDA=0.25A

+2.5VS — L1 FBMA-L11-201209-221LMA30T_0805 — +2.5VDDA
C11 220U_6.3V_M
C12 4.7U_0805_10V4Z
C13 3300P_0402_50V7K
C14 0.22U_0603_16V4Z

JCPU1D
FOX_PZ63823-284S-41F_Champlian

[15] CLK_CPU_BCLK — C16 3900P_0402_50V7K — CPU_CLKIN_SC_P / CPU_CLKIN_SC_N
[15] CLK_CPU_BCLK# — C15 3900P_0402_50V7K — R10 169_0402_1%

LDT_RST# / H_PWRGD / LDT_STOP# — T2 PAD

+1.5VS — R12 1K_0402_5% — CPU_SIC / CPU_SID
+1.5VS — R14 1K_0402_5%

+1.1VS — R15 44.2_0402_1% — CPU_HTREF0
+1.1VS — R16 44.2_0402_1% — CPU_HTREF1

[43] CPU_VDD0_FB_H / CPU_VDD0_FB_L
[43] CPU_VDD1_FB_H / CPU_VDD1_FB_L

CPU_DBRDY / CPU_TMS / CPU_TCK / CPU_TRST# / CPU_TDI

CPU_TEST23 / CPU_TEST18 / CPU_TEST19 / CPU_TEST25H / CPU_TEST25L / CPU_TEST21 / CPU_TEST20 / CPU_TEST24 / CPU_TEST22 / CPU_TEST12 / CPU_TEST27

R24 0_0402_5% — CPU_TEST29_H_FBCLKOUT_P / CPU_TEST29_L_FBCLKOUT_N — R25 80.6_0402_1%

CPU_SVC [43] / CPU_SVD [43]
CPU_THERMTRIP#_R — H_PROCHOT# — PAD T3
THERMDC_CPU / THERMDA_CPU
CPU_VDDNB_FB_H [43] / CPU_VDDNB_FB_L [43]
CPU_DBREQ# — CPU_TDO

PAD T4 — PAD T11 — PAD T5 — PAD T6 — PAD T7 — PAD T8

+1.5V — R6 10K_0402_5% <BOM Structure>
R7 1K_0402_5%
Q1 MMBT3904_NL_SOT23-3
CPU_THERMTRIP#_R — R8 0_0402_5% — H_THERMTRIP# [20]
R9 @ 0_0402_5% — MAINPWON [36,37,41]

+1.5V — R11 300_0402_5%
H_PROCHOT# — R13 0_0402_5% — H_PROCHOT_R# [19]

PROCHOT:
Input: For HTC Function
Output: Over Temperature Condition

+1.5VS — R17 300_0402_5% — [19] LDT_RST# — C17 0.01U_0402_25V4Z @
+1.5VS — R18 300_0402_5% — [13,19] LDT_STOP# — C18 0.01U_0402_25V4Z @
+1.5VS — R21 300_0402_5% — [19] H_PWRGD — C19 0.01U_0402_25V4Z @

+3VS — NEWX5@ C20 0.1U_0402_16V4Z
NEWX5@ U1 ADM1032ARMZ_MSOP8
THERMDA_CPU / THERMDC_CPU
C21 @ 100P_0402_50V8J
EC_SMB_CK2 — EC_SMB_CK2 [29]
EC_SMB_DA2 — EC_SMB_DA2 [29]

For MP

Address 1001 100X b

+1.5V — CPU_SVC — R19 1K_0402_5%
CPU_SVD — R20 1K_0402_5%

+1.5V — CPU_TEST25H — R22 510_0402_5% — R23 @ 510_0402_5%
+1.5V — CPU_TEST25L — R26 @ 510_0402_5% — R27 510_0402_5%

+1.5V — CPU_TEST27 — R28 1K_0402_5%

For SCAN connect use

CPU_TEST12 — R29 1K_0402_5%
CPU_TEST18 — R30 1K_0402_5%
CPU_TEST19 — R31 1K_0402_5%
CPU_TEST20 — R32 1K_0402_5%
CPU_TEST21 — R33 1K_0402_5%
CPU_TEST22 — R34 1K_0402_5%
CPU_TEST24 — R35 1K_0402_5%
CPU_TEST23 — R265 1K_0402_5%

+1.5V — R36 @ 220_0402_5% / R37 @ 220_0402_5% / R38 @ 220_0402_5% / R39 @ 300_0402_5% / R40 300_0402_5%

JP2 CONN@ SAMTEC_ASP-68200-07
CPU_DBREQ# / CPU_DBRDY / CPU_TCK / CPU_TMS / CPU_TDI / CPU_TRST# / CPU_TDO / HDT_RST#

R43 @ 0_0402_5%
+3VS — @ U2 NC7SZ08P5X_NL_SC70-5
LDT_RST# — SB_PWRGD [13,20,29]

CPU internal thermal sensor

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

+3VS — R41 PEW56@ 31.6K_0402_1% — R42 PEW56@ 30K_0402_5%
C22 PEW56@ 0.1U_0402_16V4Z

2.09V for Gate

CPU_SID — Q2 PEW56@ FDV301N_NL_SOT23-3 — EC_SMB_DA — R44 @ 0_0402_5% — SB_SID — SB_SID [20] — T0 SB
EC_SMB_DA2 — R45 PEW56@ 0_0402_5% — T0 EC

CPU_SIC — Q3 PEW56@ FDV301N_NL_SOT23-3 — EC_SMB_CK — R46 @ 0_0402_5% — SB_SIC — SB_SIC [20] — T0 SB
EC_SMB_CK2 — R47 PEW56@ 0_0402_5% — T0 EC

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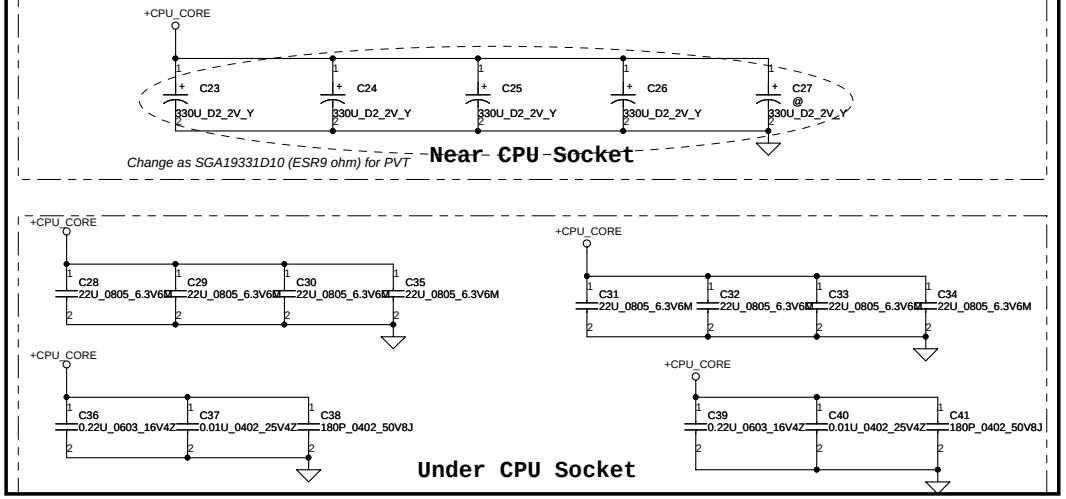
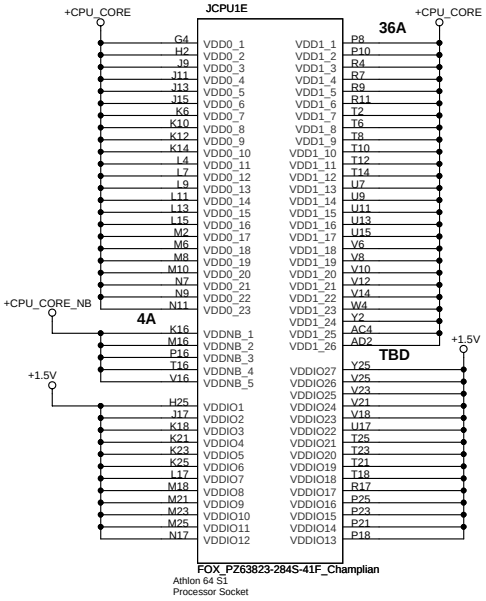
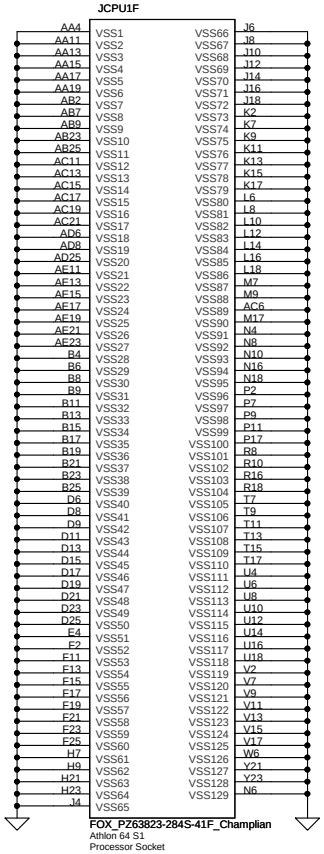
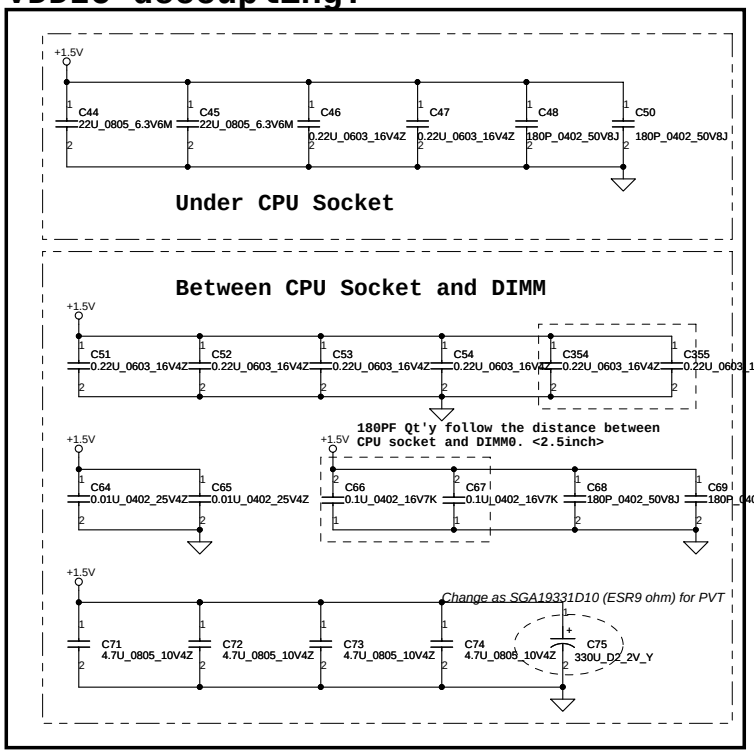
VDD(+CPU_CORE) decoupling.



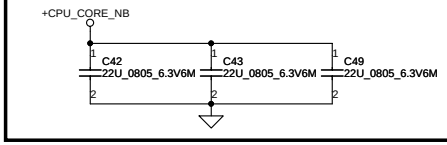




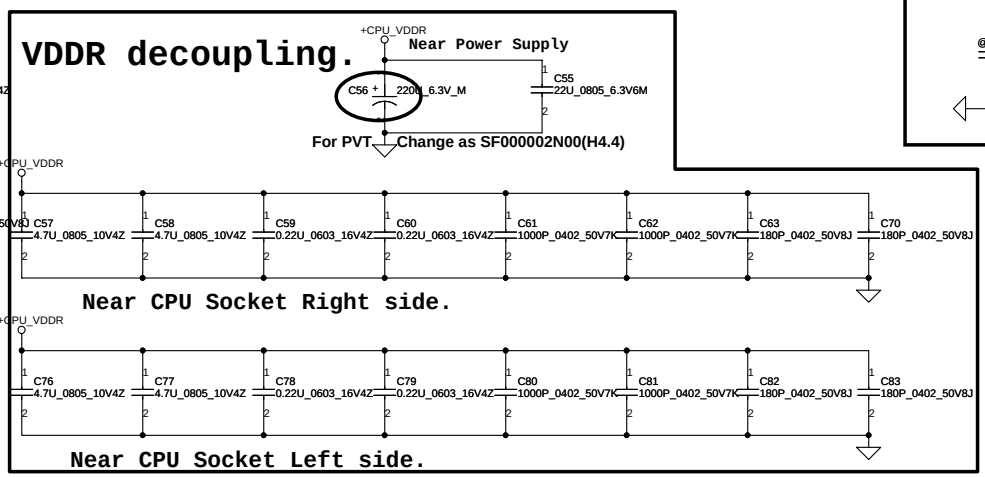
VDDIO decoupling.

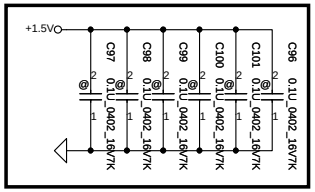


+CPU_CORE_NB decoupling.



VDDR decoupling.





Reserve for EMI

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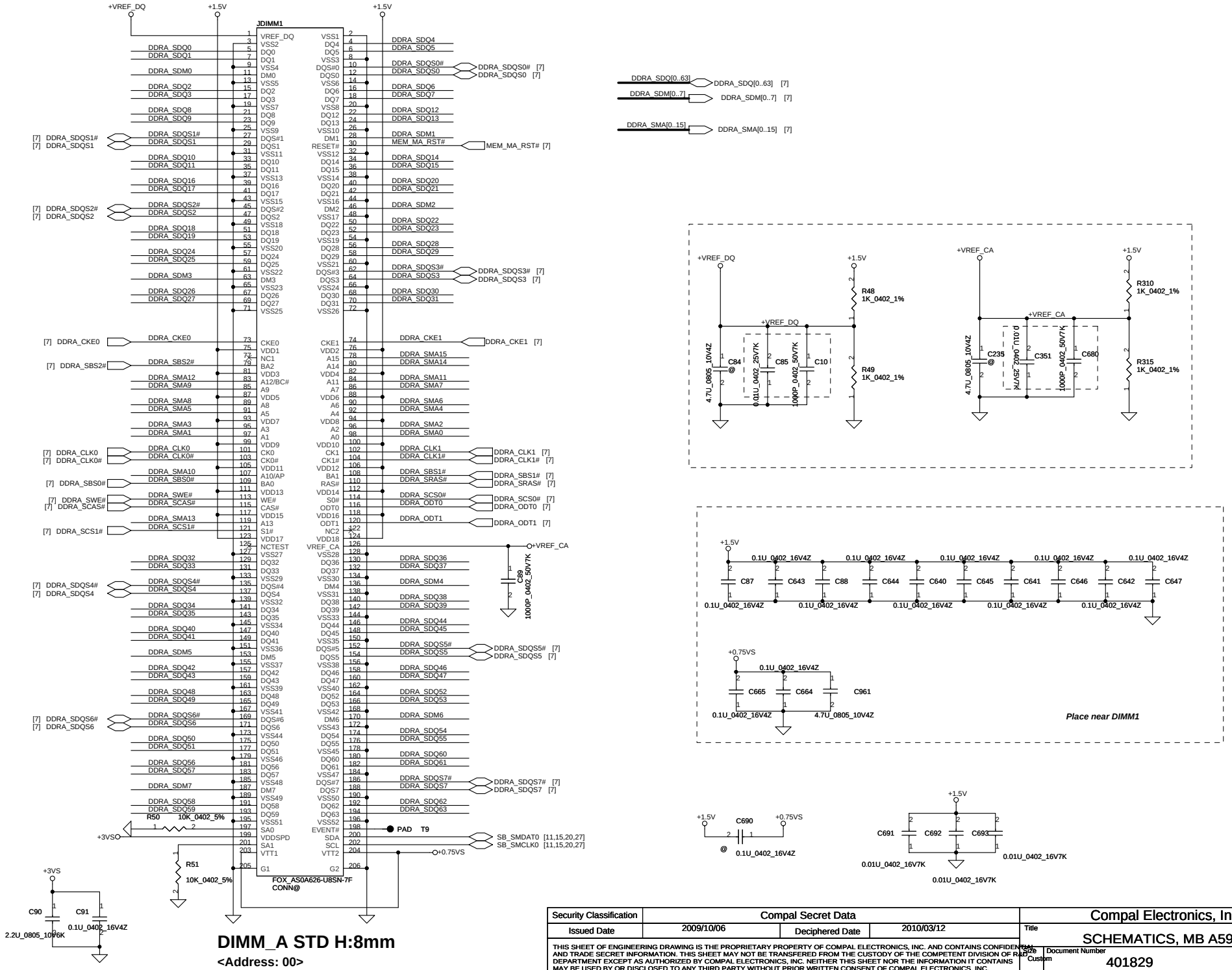

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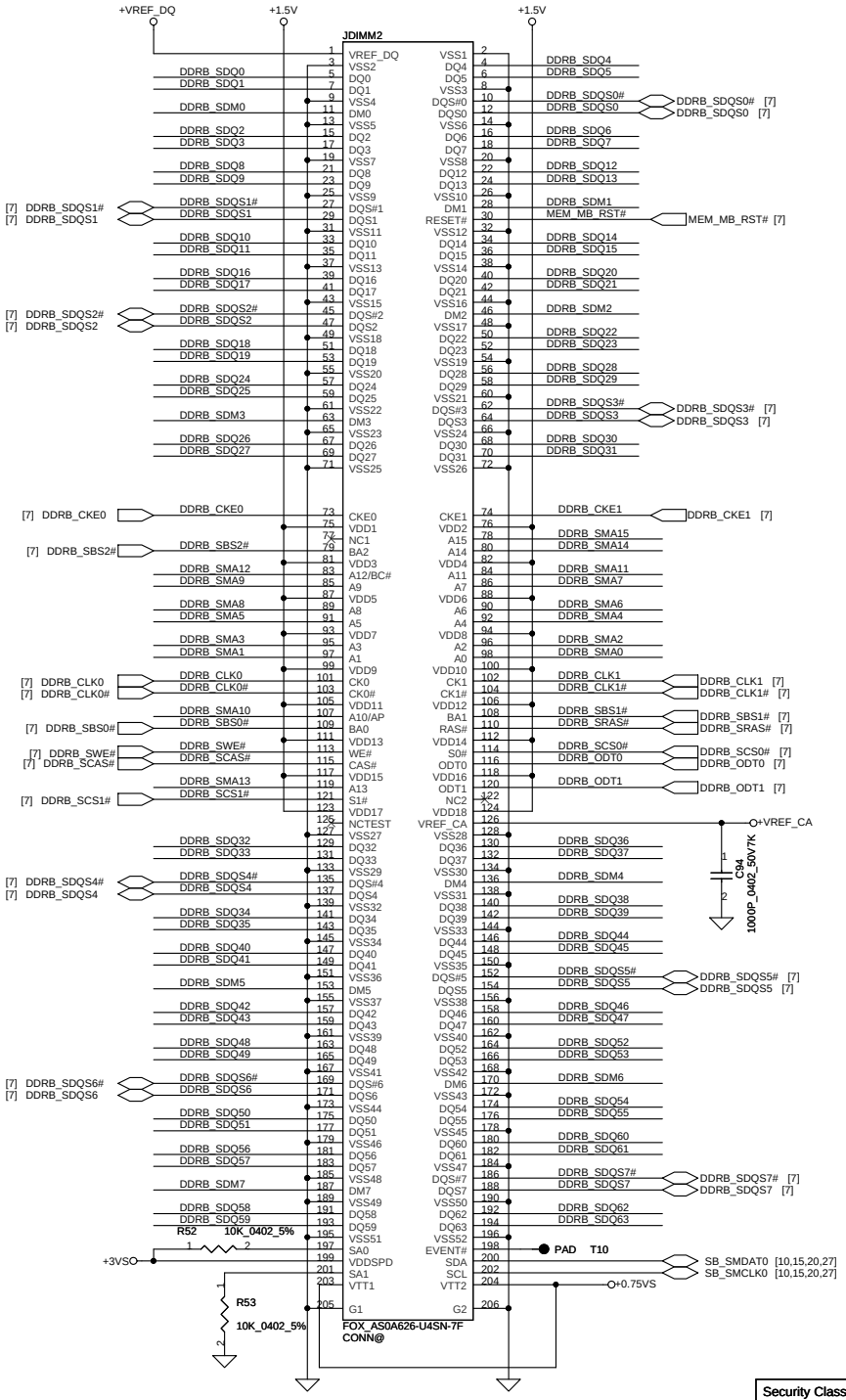

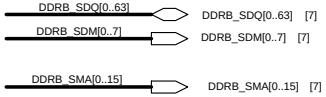

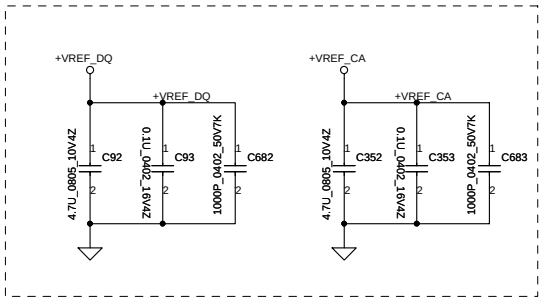

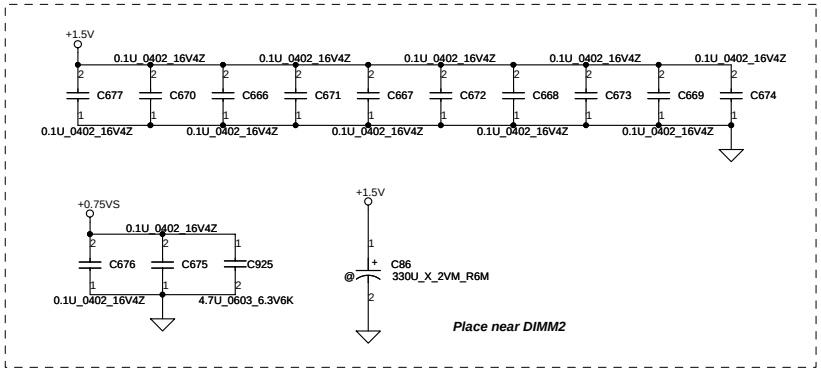

DIMM_B STD H:4mm

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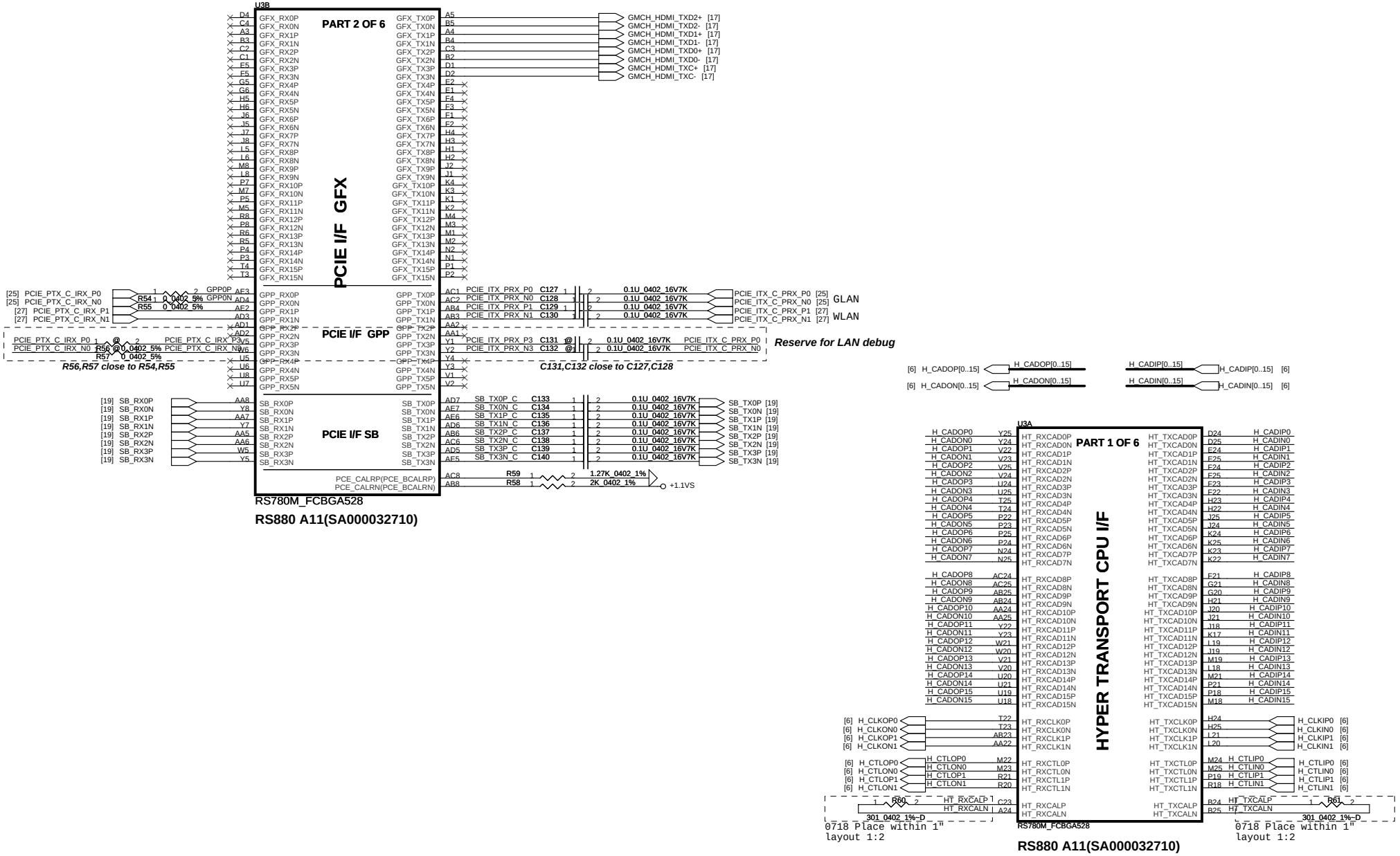

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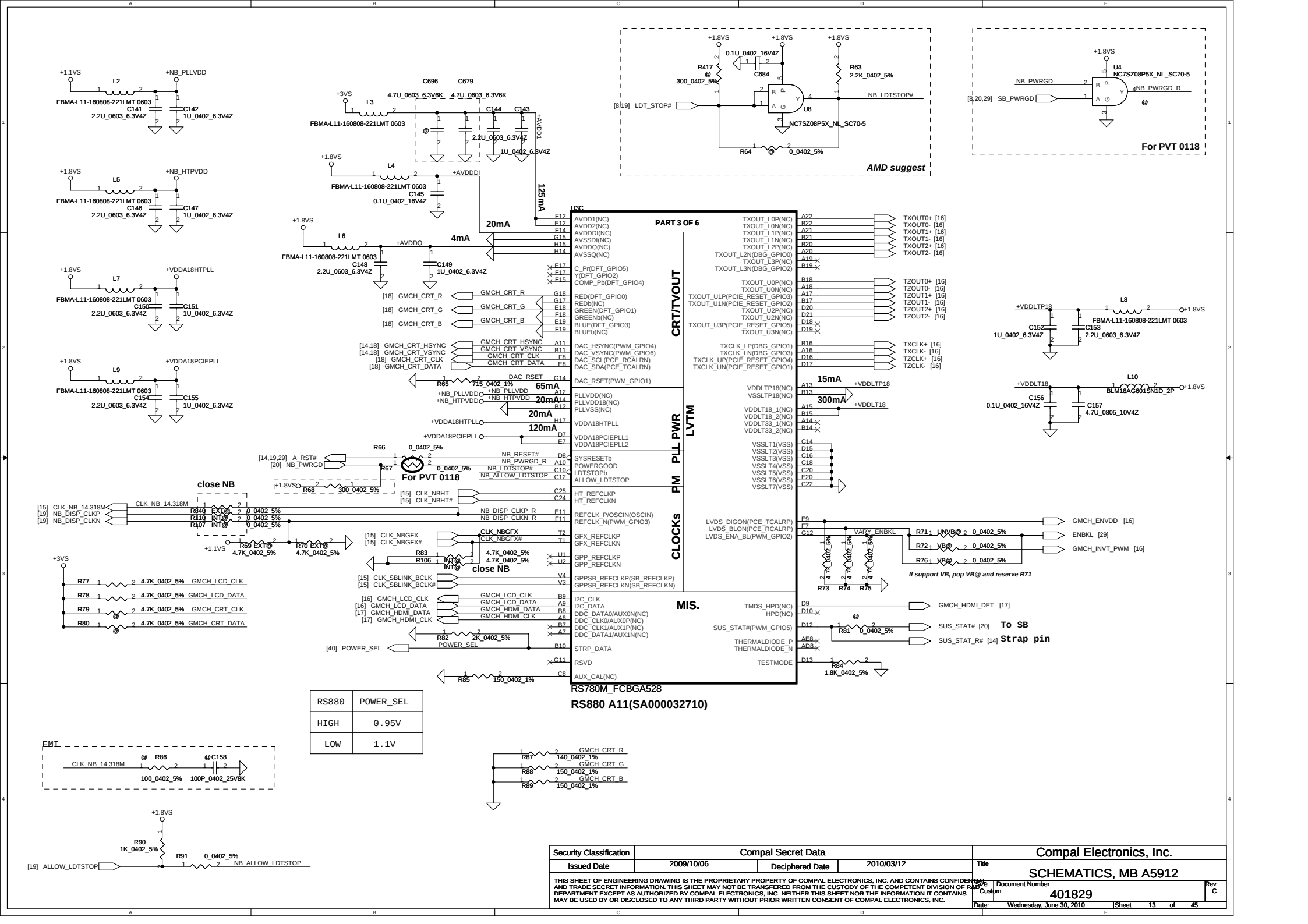

RS880	POWER_SEL
HIGH	0.95V
LOW	1.1V

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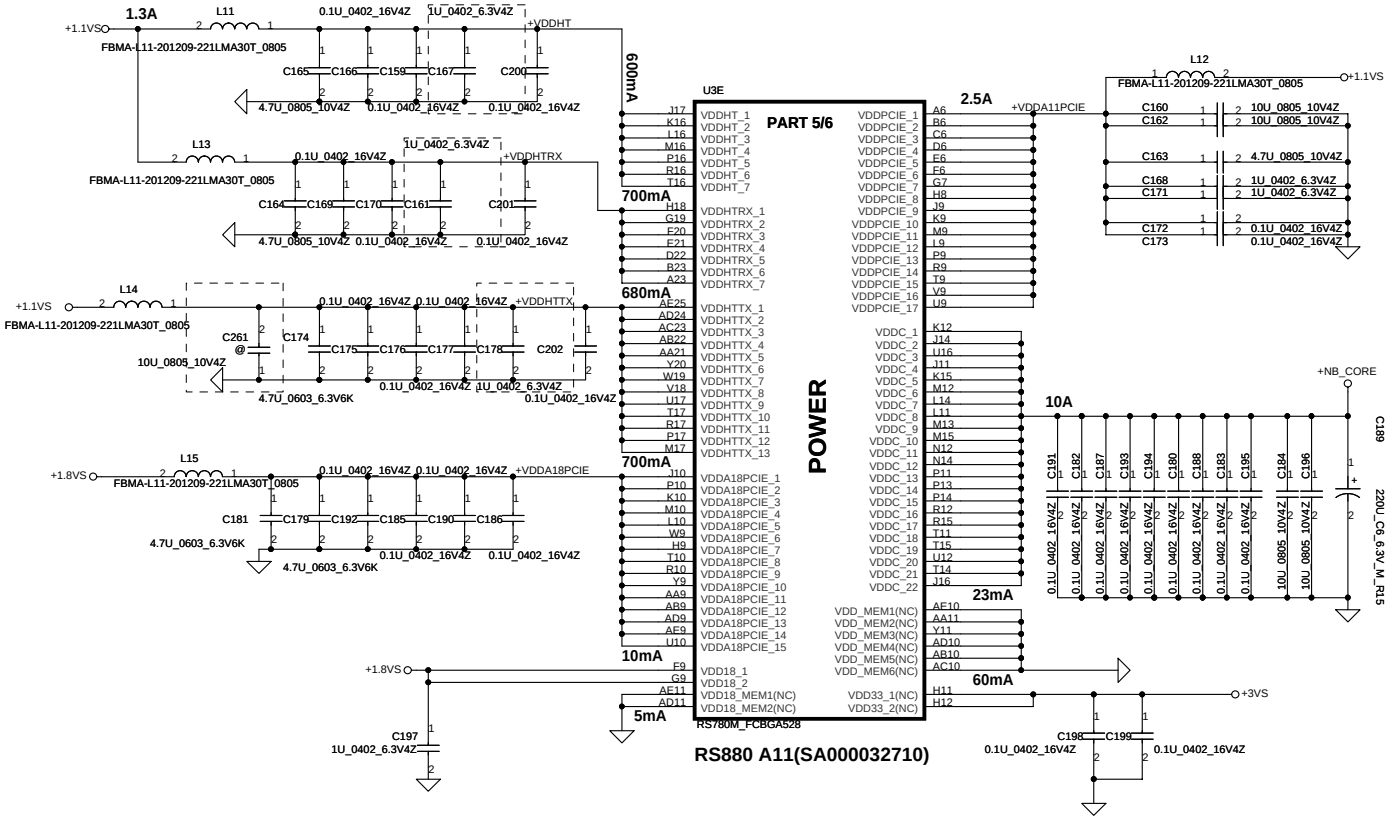
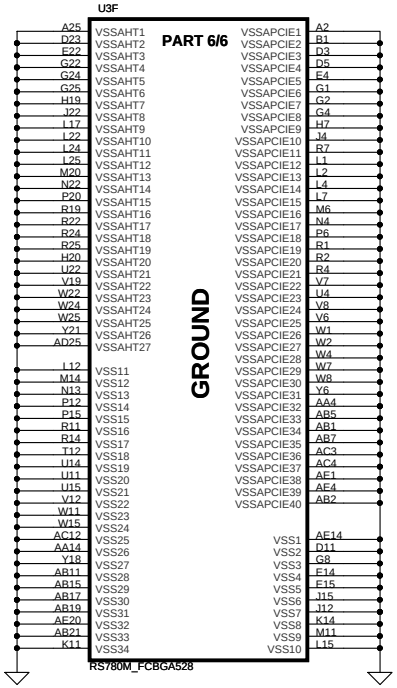


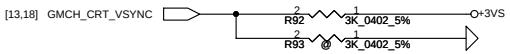
RS880 A11(SA000032710)



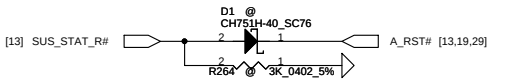
RS880 A11(SA000032710)

Side port and Strap setting

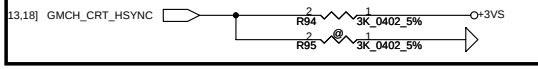
Debug Mode



Load EEPROM Strap



Enable Side Port Memory



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

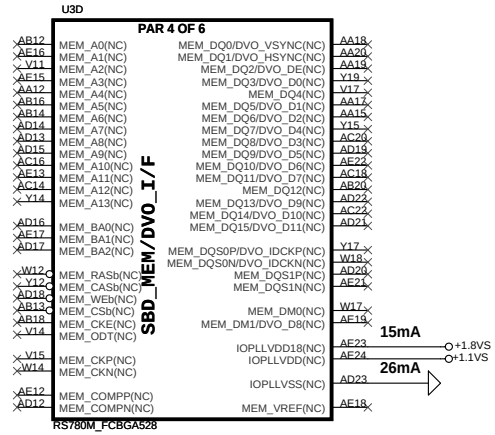
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

Enable Side Port Memory

```
RS880: HSYNC#
0:   Enable        Register Readback of strap:
1 :  Disable       NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



RS880 A11(SA000032710)

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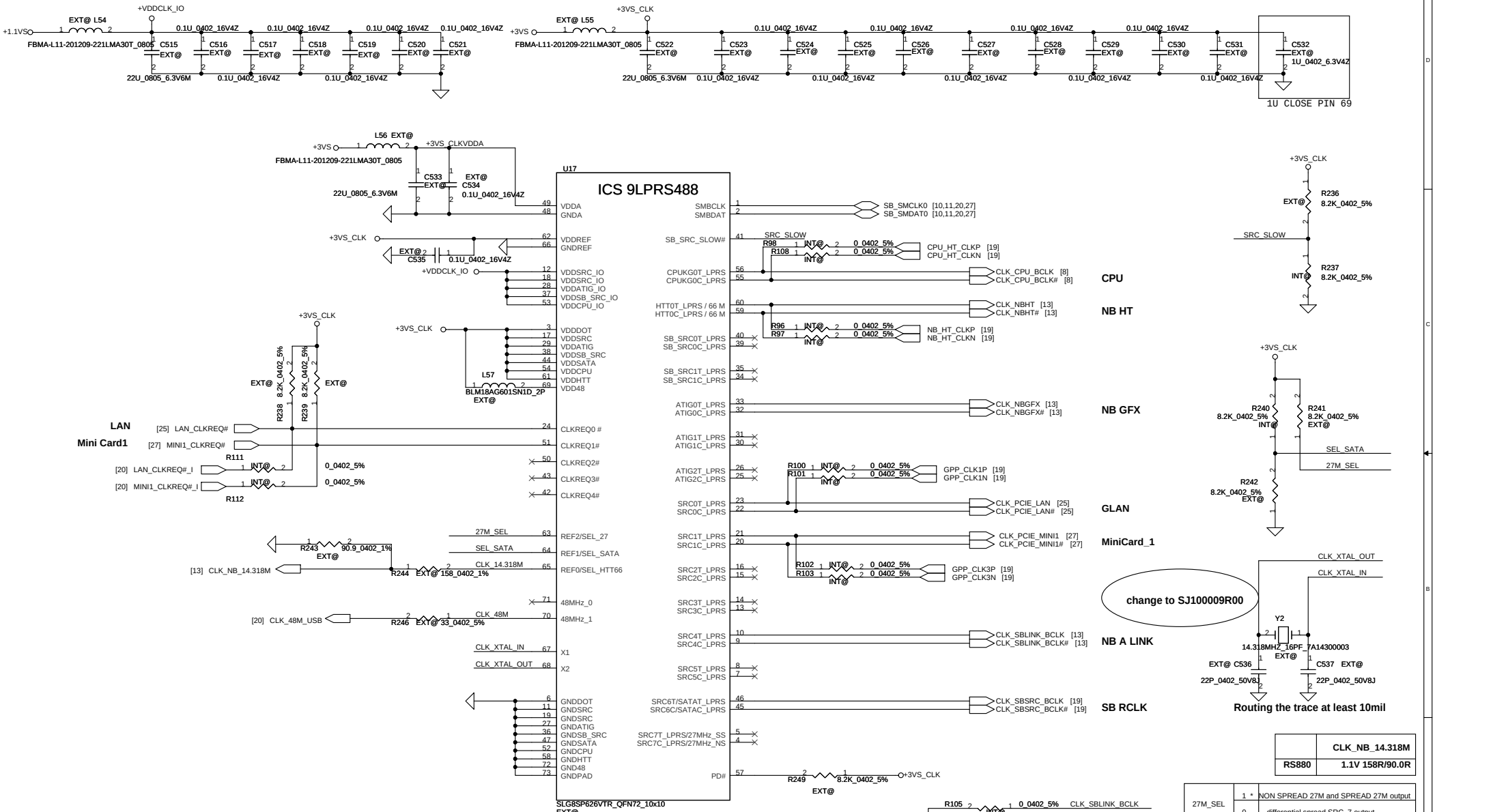

1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN

2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

	CLK_NB_14.318M
RS880	1.1V 158R/90.0R

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

* default

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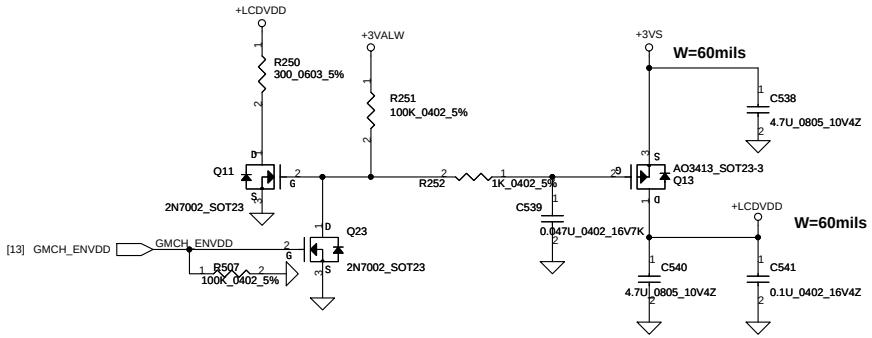
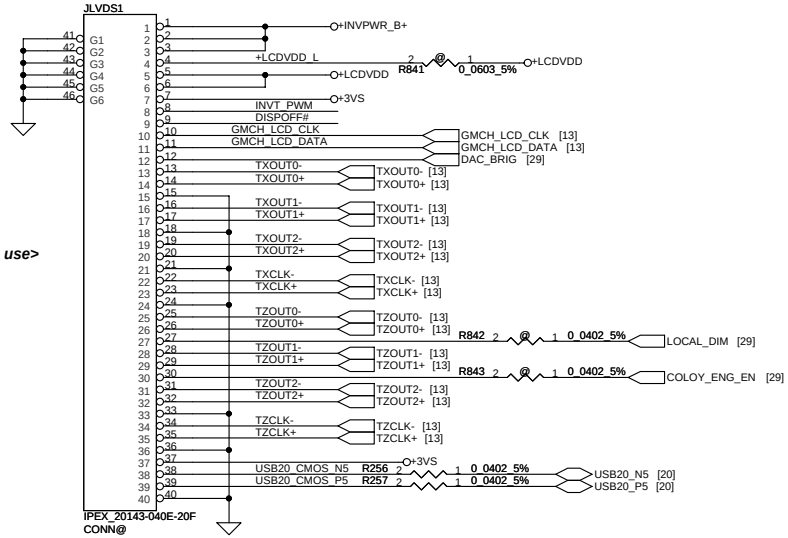
LCD POWER CIRCUIT



LCD/LED PANEL Conn.



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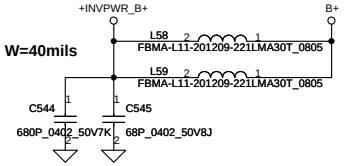

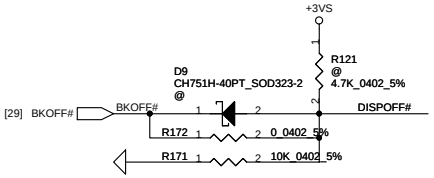

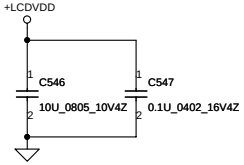

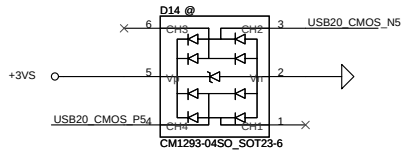

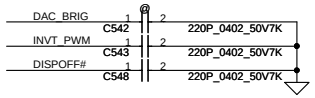

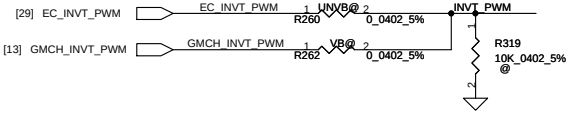

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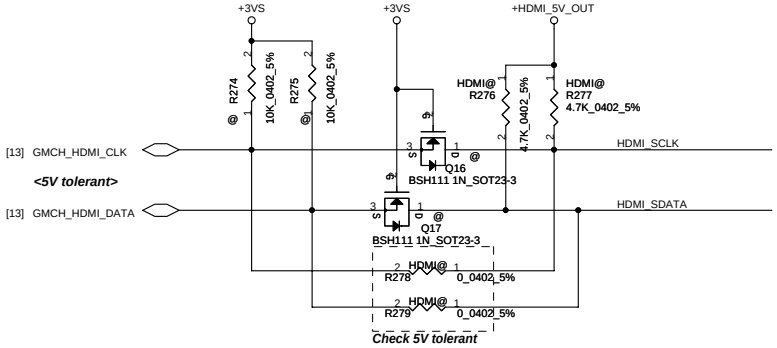
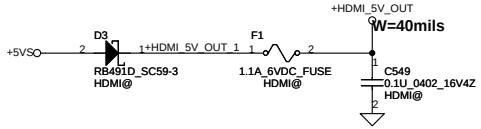
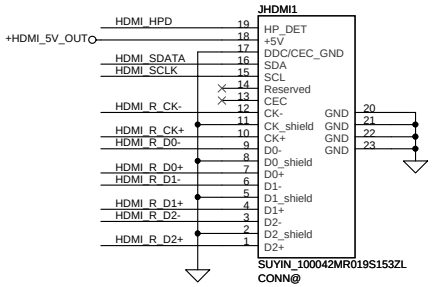
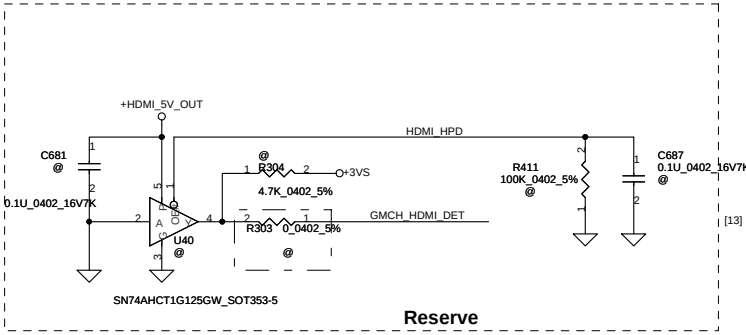
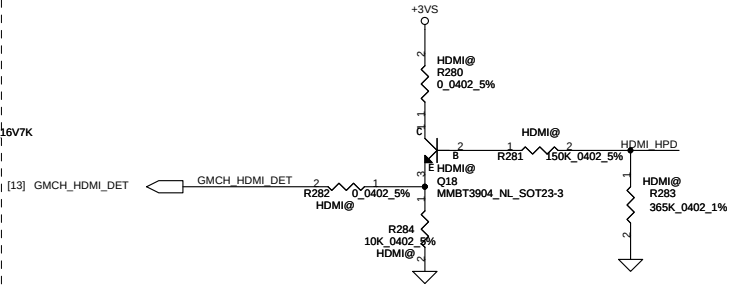


Place closed to JHDMI1

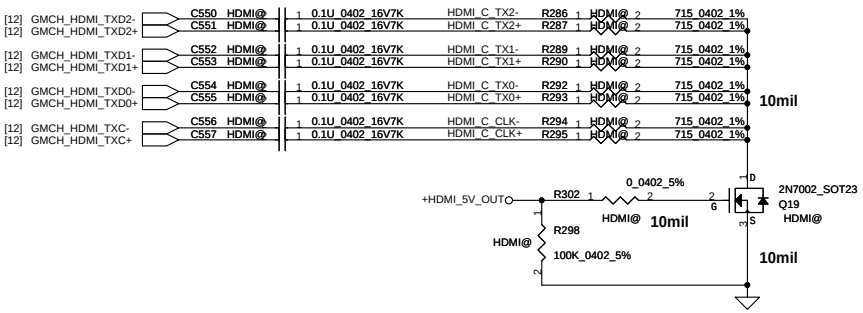




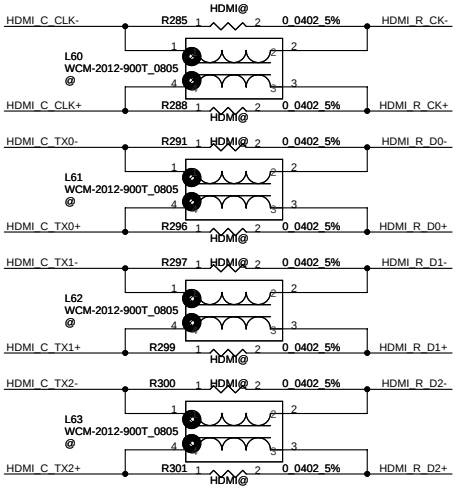




UMA 715 ohm



Place closed to JHDMI1



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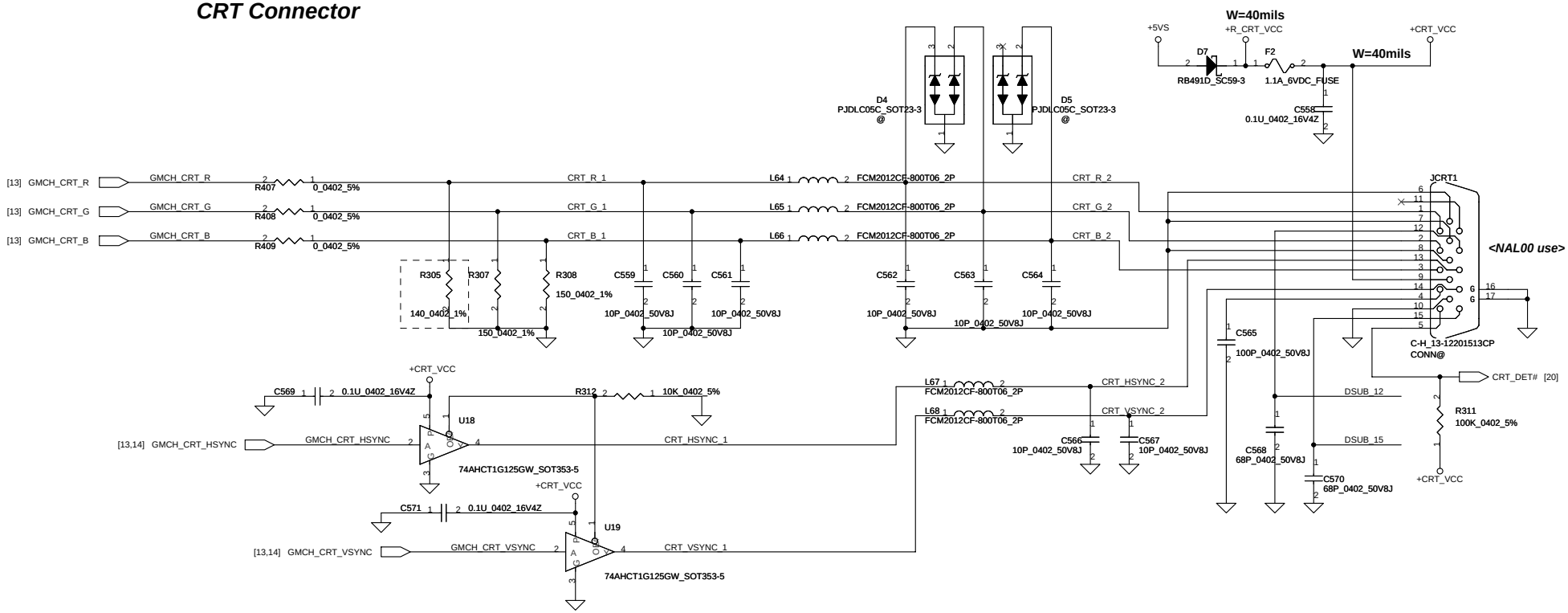
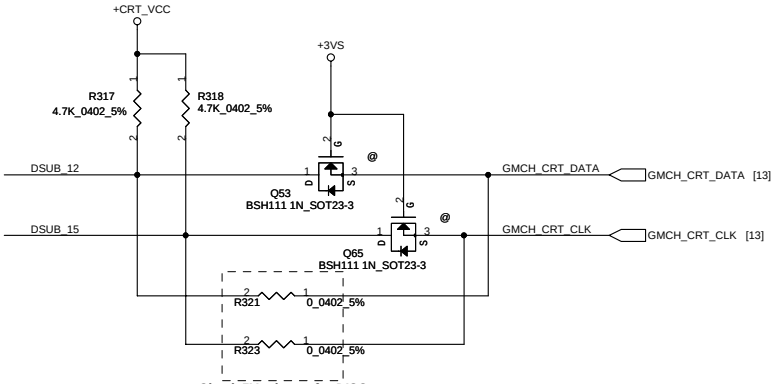
CRT Connector



Close to Conn side



Check 5V tolerant for DISO state

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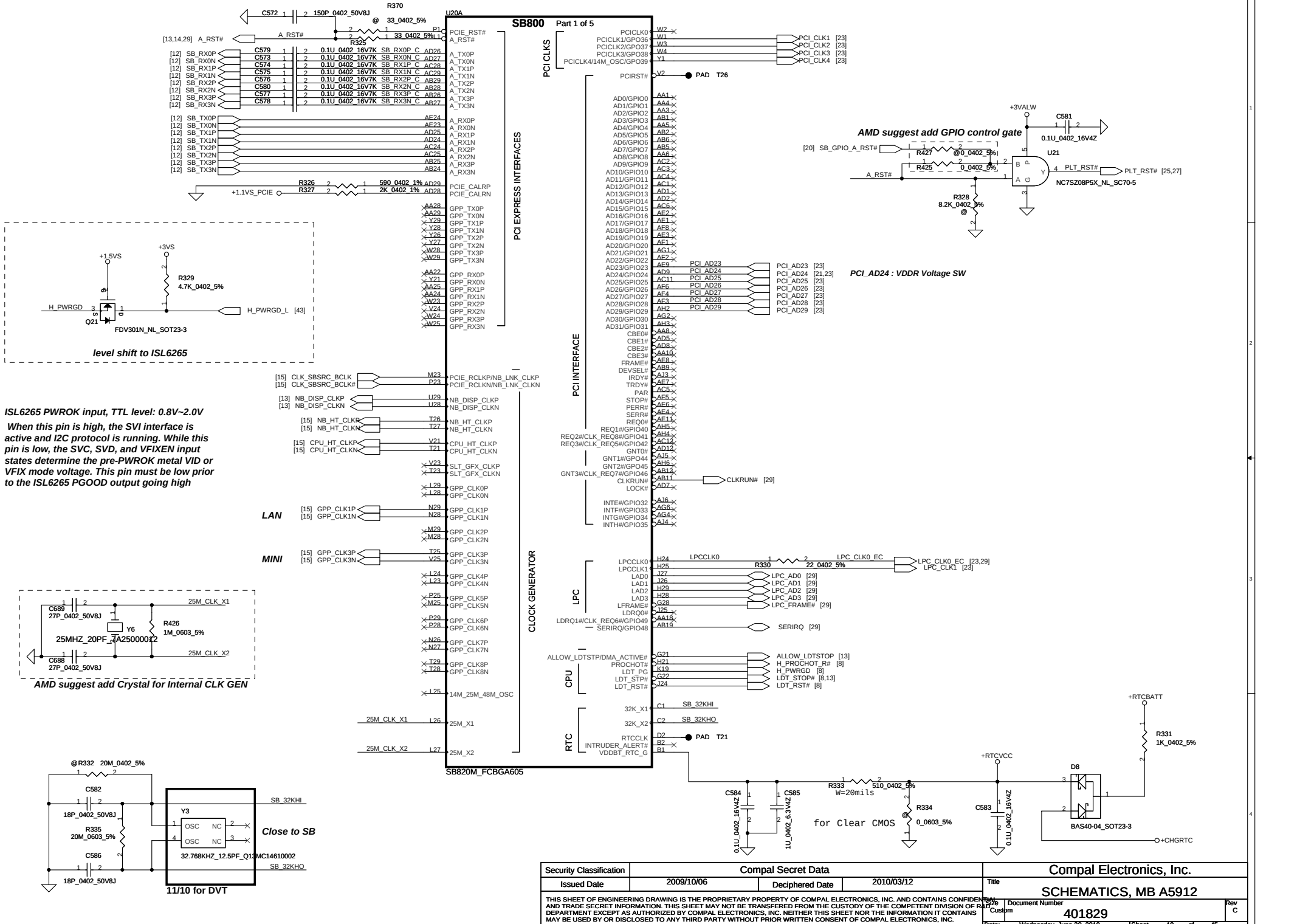

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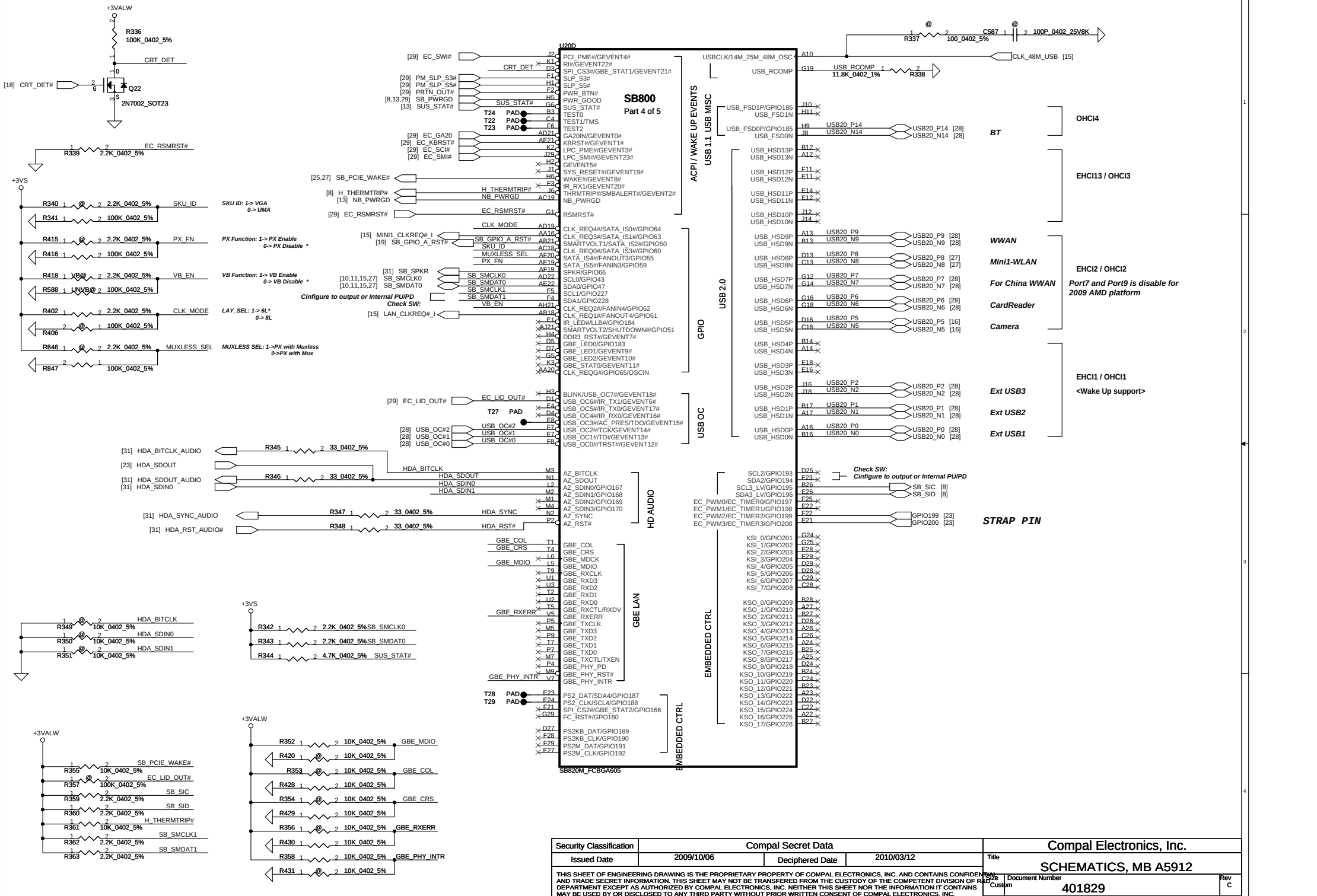

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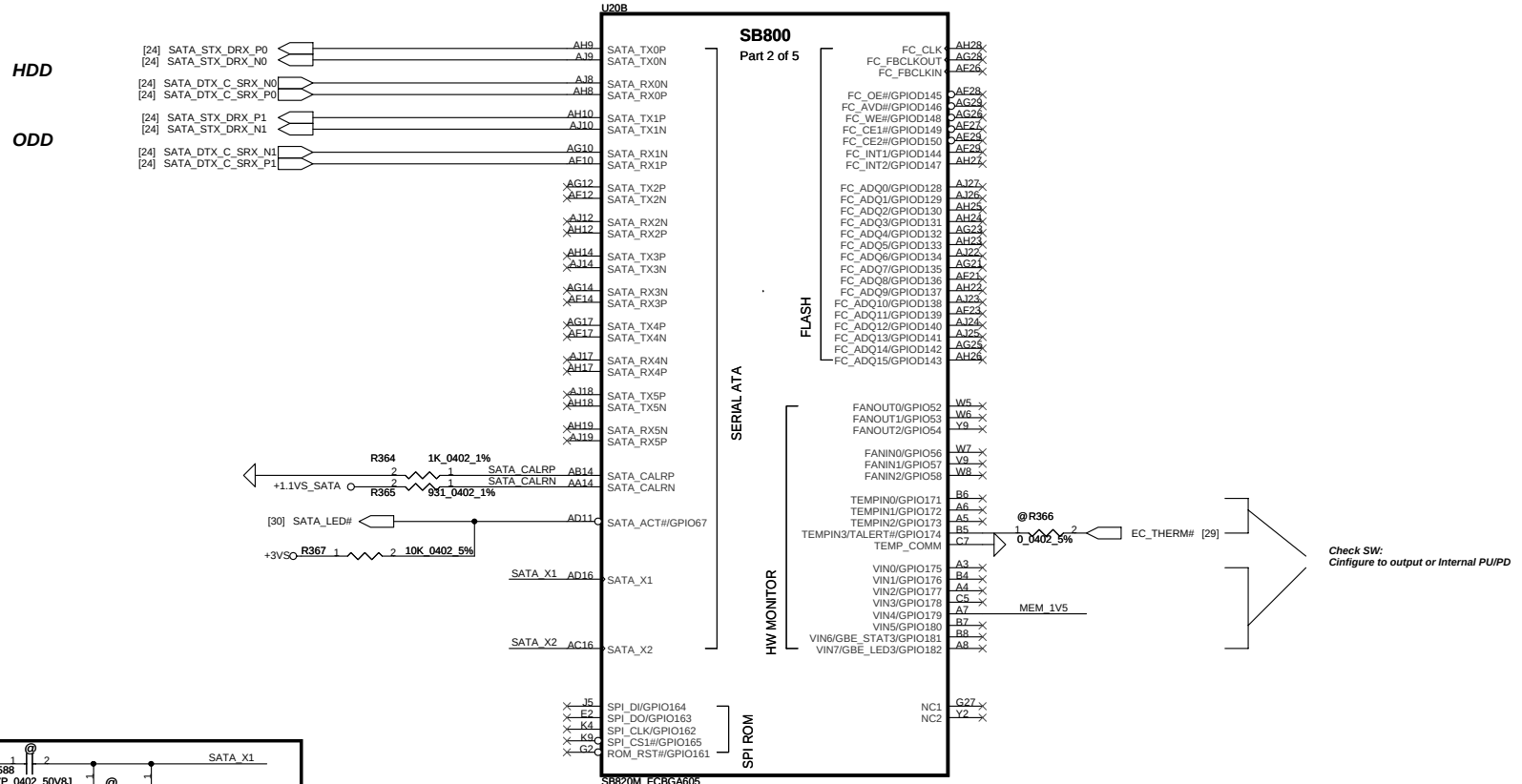
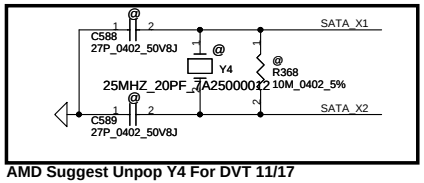
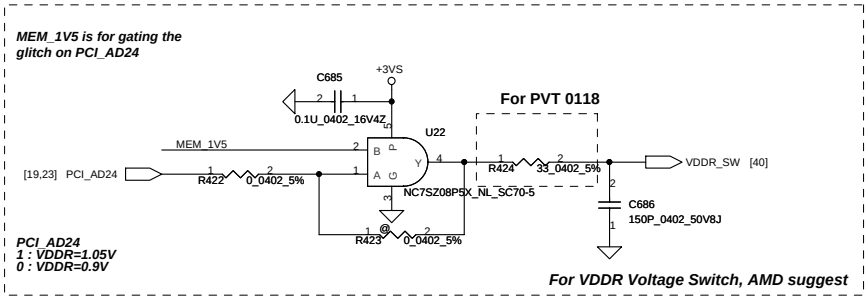


SB820 A12(SA00003IW10)



AMD Suggest Unpop Y4 For DVT 11/17



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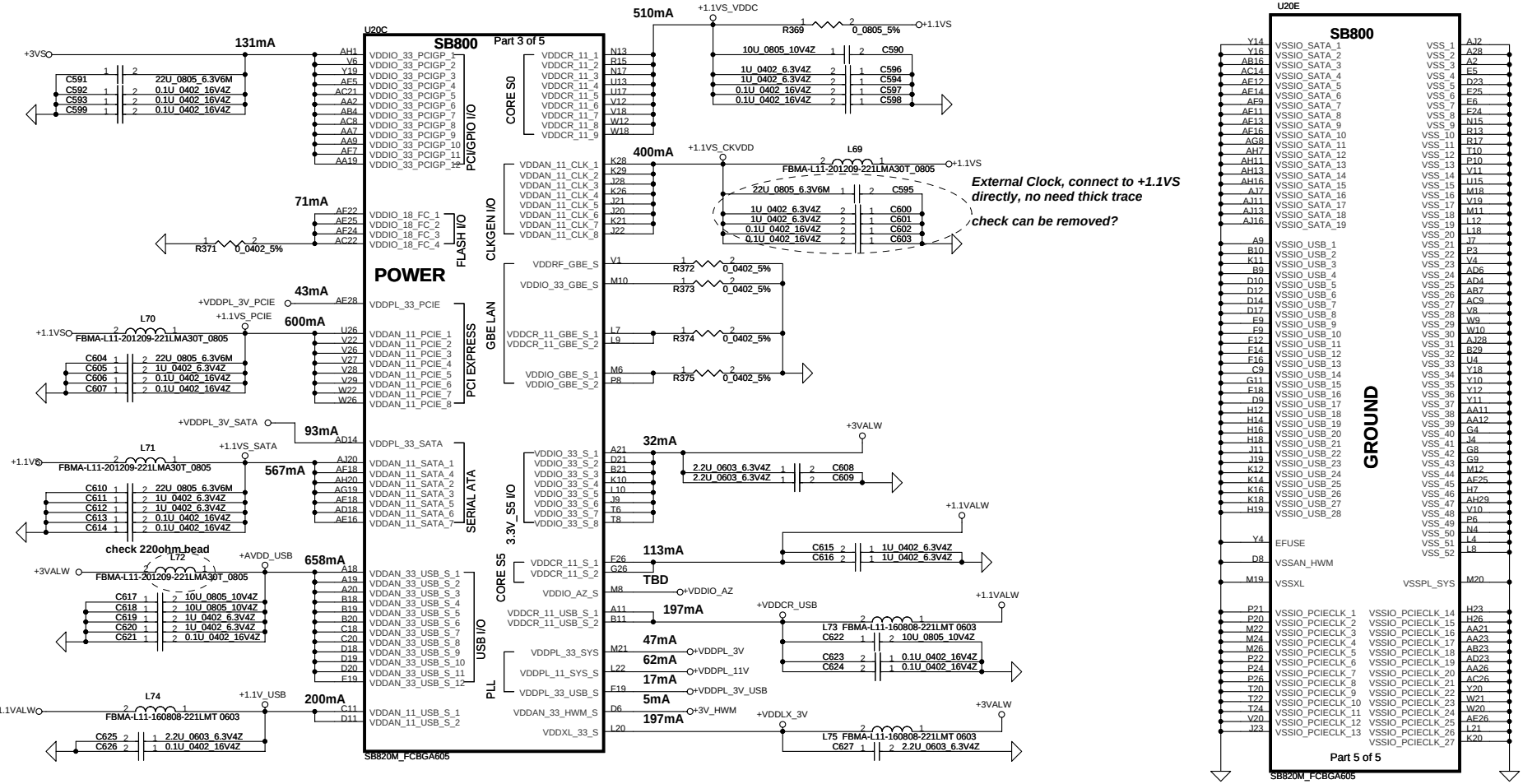

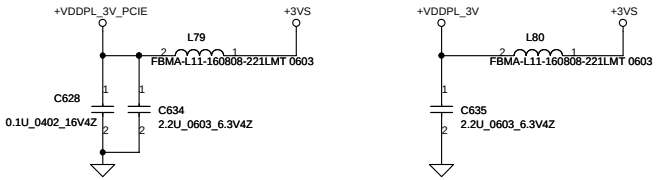

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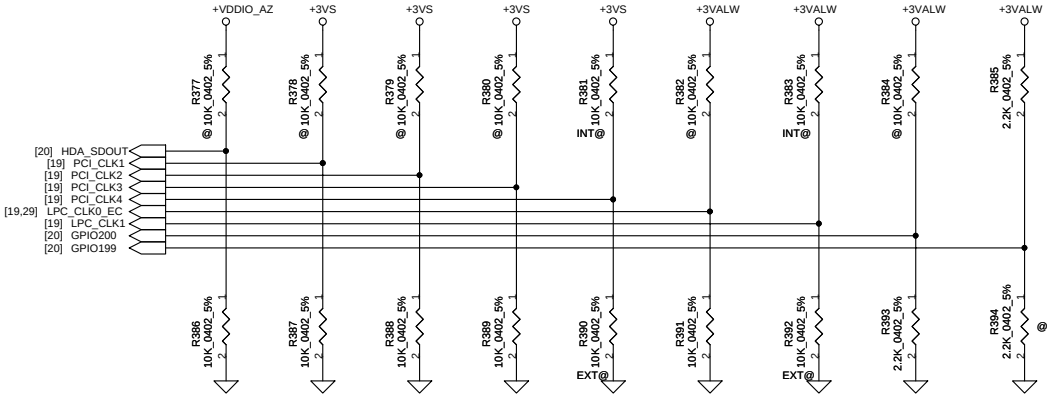
REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable DEFAULT	EC DISABLE DEFAULT	CLOCKGEN DISABLE DEFAULT		



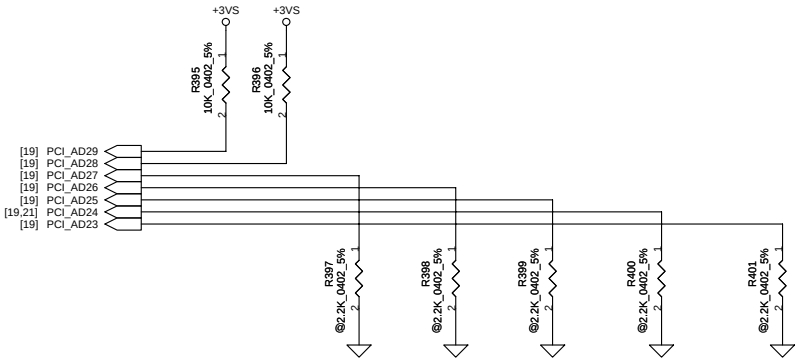
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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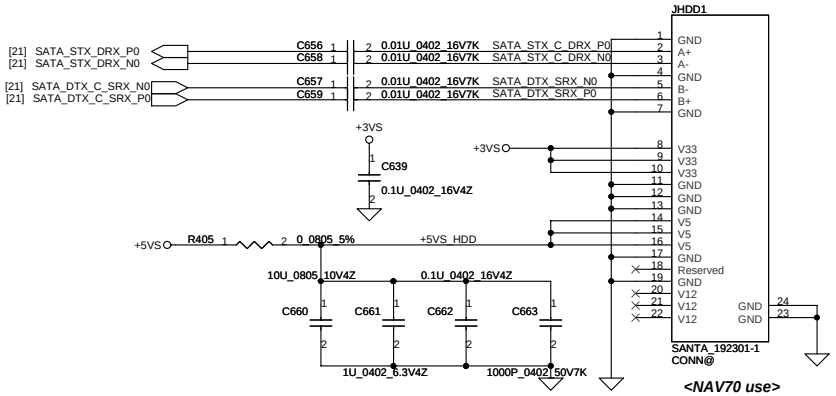
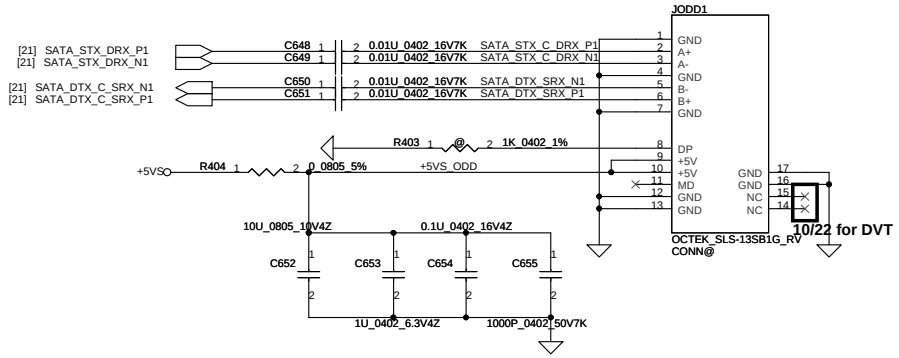
SATA HDD Conn.



SATA ODD Conn.



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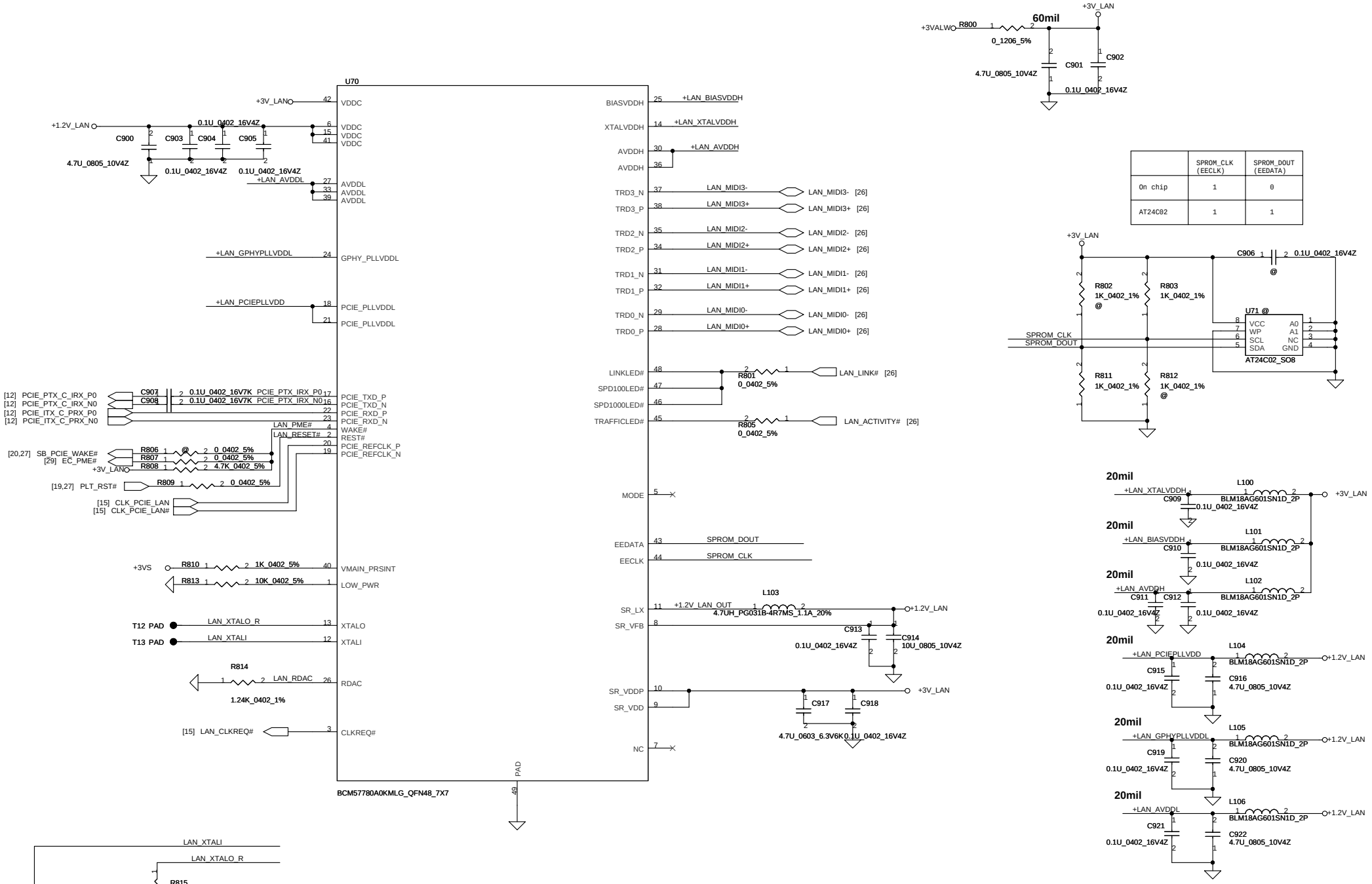

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

TXC suggest change SE071330J80 For DVT

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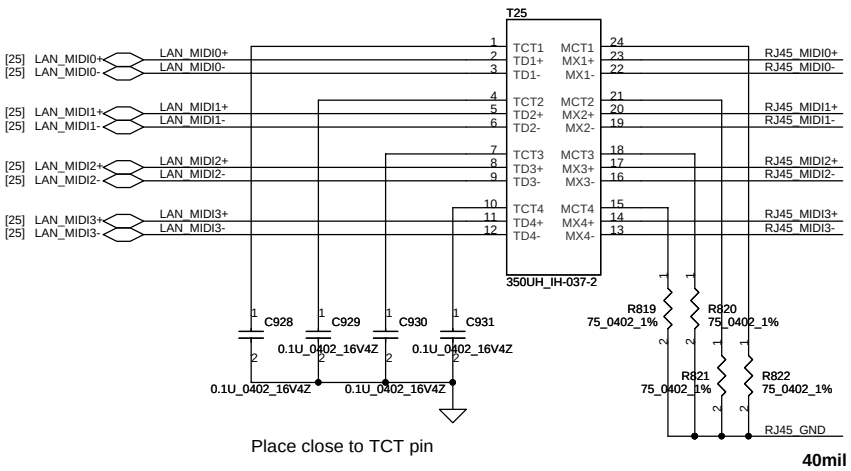
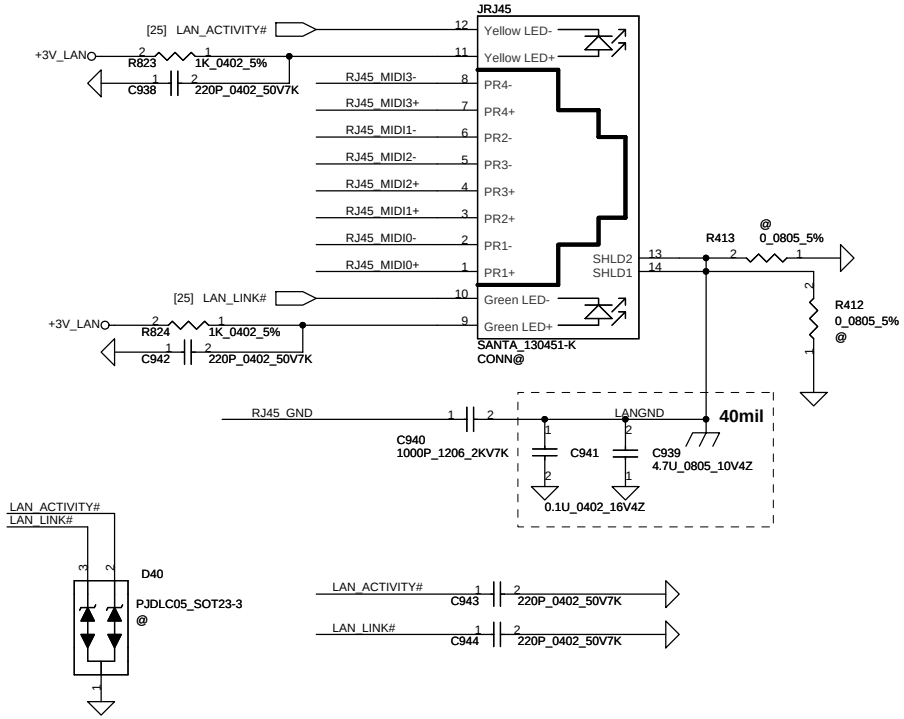
LAN Connector

BH GS5009-D <SP050006B00>



Place close to TCT pin



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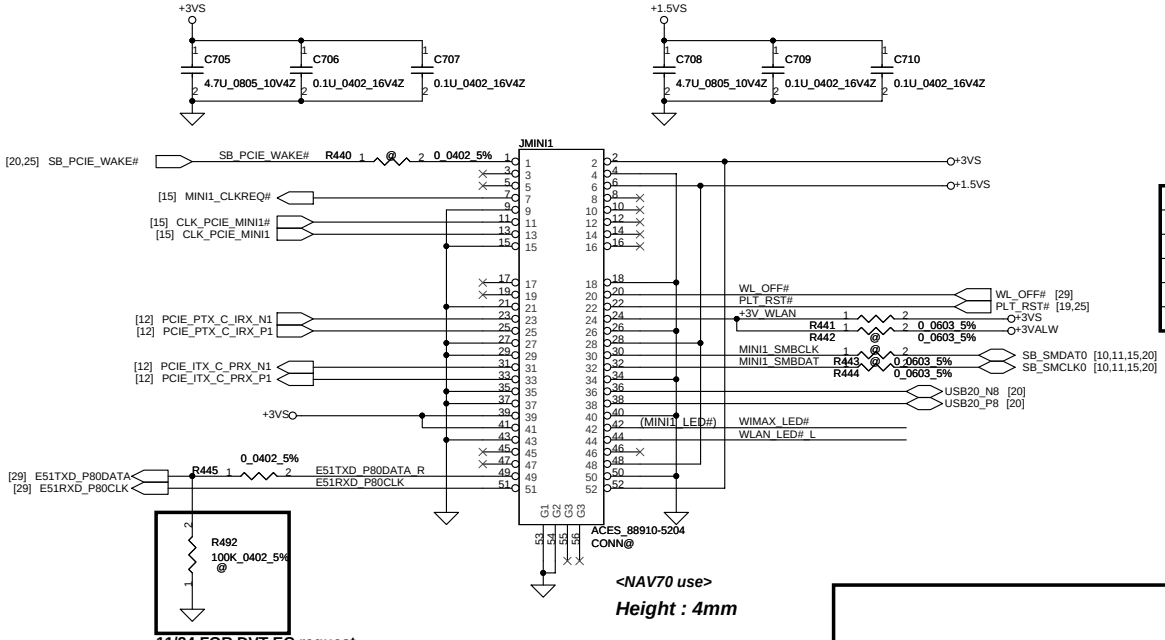
Mini-Express Card for WLAN

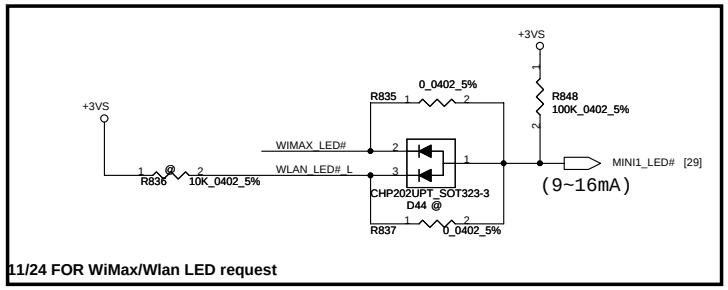


<NAV70 use>

Height : 4mm

11/24 FOR DVT EC request

Mini Card Power Rating			
Power	**Primary Power (mA)**		**Auxiliary Power (mA)**
	Peak	**Normal**	**Normal**
+3VS	**1000**	**750**	
+3V	**330**	**250**	**250 (wake enable)**
+1.5VS	**500**	**375**	**5 (Not wake enable)**



11/24 FOR WiMax/Wlan LED request

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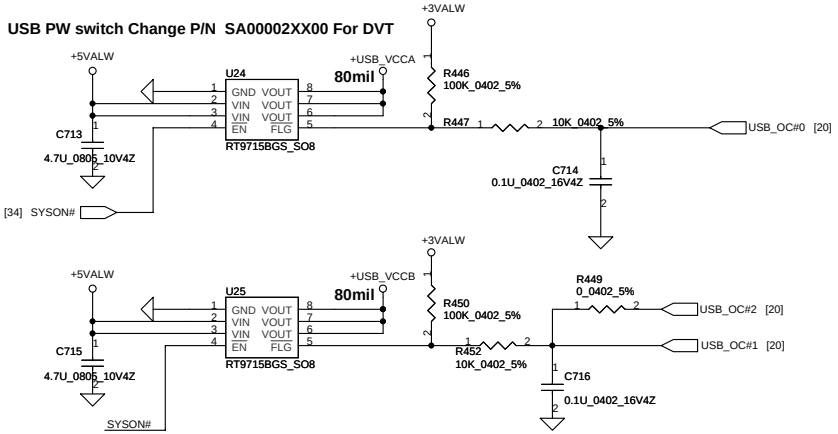
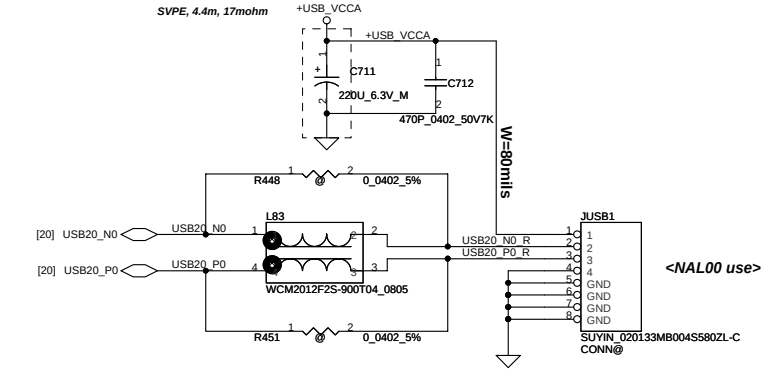
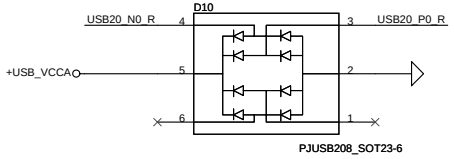
USB PW switch Change P/N SA00002XX00 For DVT

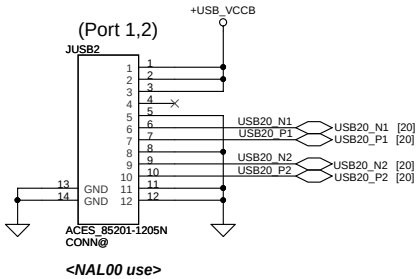






ESD Change P/N SC300000B00 For DVT

To USB/B Connector



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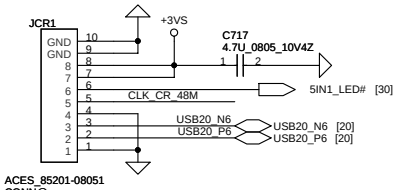
To CardReader/B Connector



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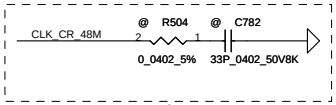
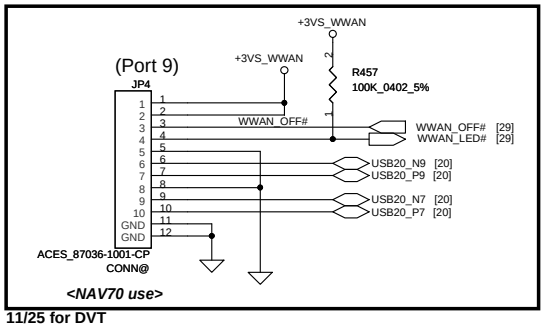


Reserve for EMI

To 3G Module Connect



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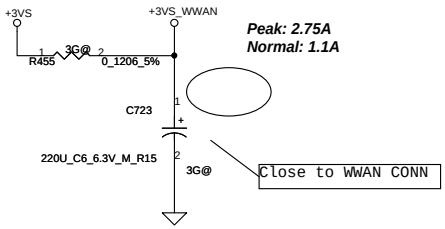
11/25 for DVT



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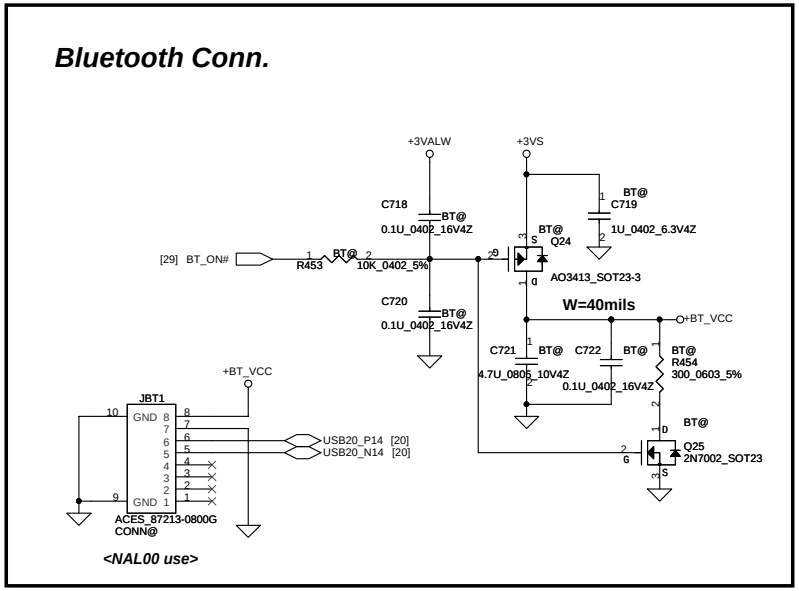

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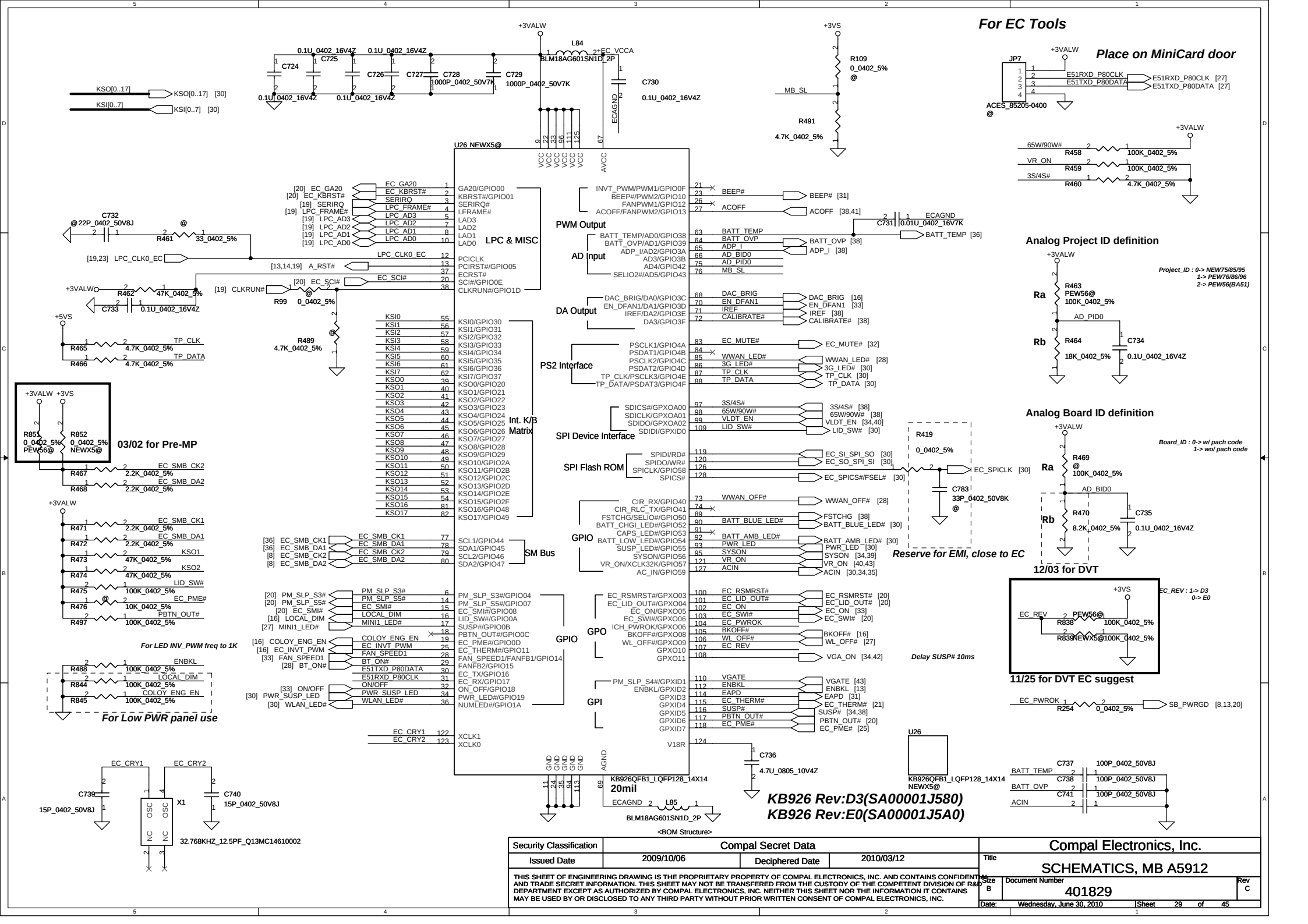
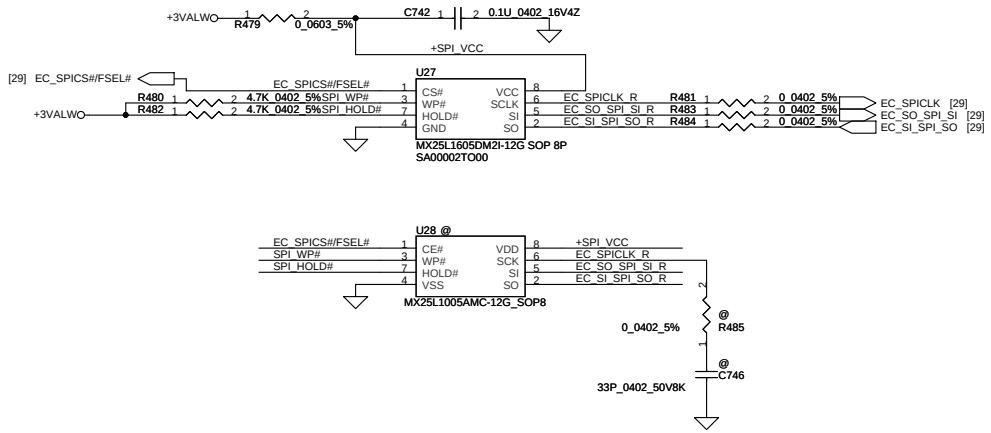
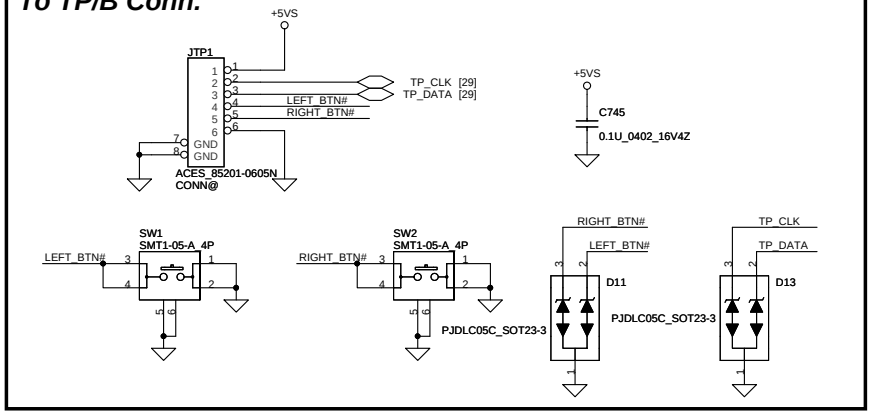
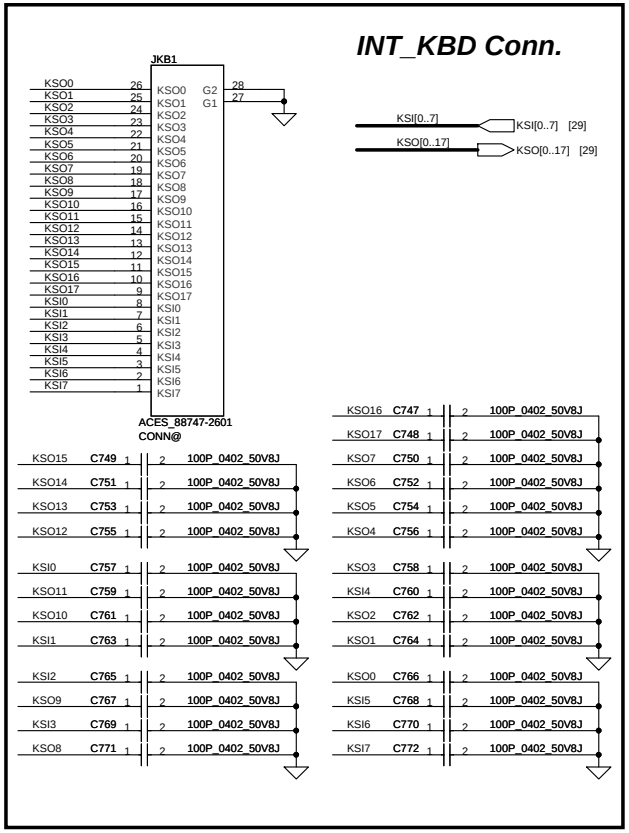

For EC Tools
Place on MiniCard door
U26 NEWX5@
KB926QFB1_LQFP128_14X14
20mil
KB926 Rev:D3(SA00001J580)
KB926 Rev:E0(SA00001J5A0)
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
Int. K/B Matrix
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
03/02 for Pre-MP
For LED INV_PWM freq to 1K
For Low PWR panel use
Analog Project ID definition
Analog Board ID definition
Reserve for EMI, close to EC
12/03 for DVT
11/25 for DVT EC suggest
Delay SUSP# 10ms
32.768KHZ_12.5PF_Q13MC14610002
<BOM Structure>
Compal Secret Data
2009/10/06
2010/03/12
Compal Electronics, Inc.
SCHEMATICS, MB A5912
401829
Wednesday, June 30, 2010



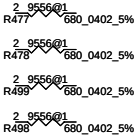
To TP/B Conn.



INT_KBD Conn.

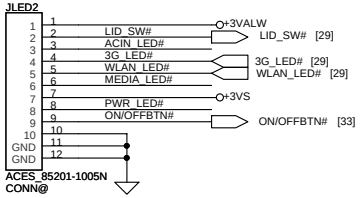


NEW95 / PEW56 LED Option

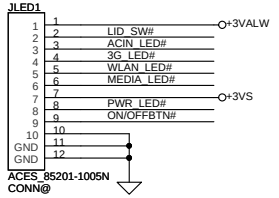


Left side / Right side

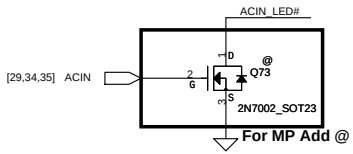
For NEW75 NEW85

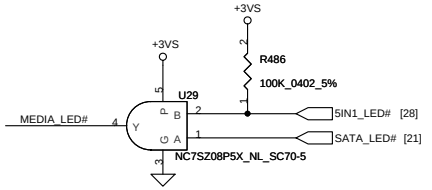


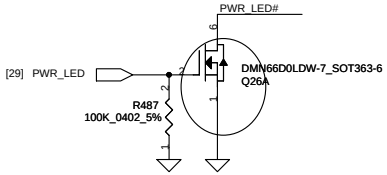
For NEW95



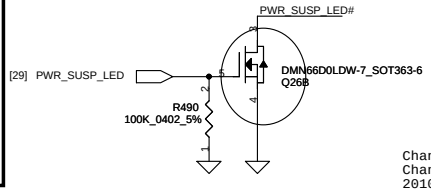
PIN define modify for 01/22

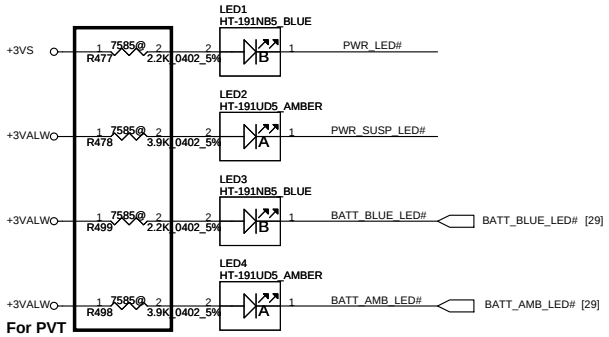






Change Q26 as SB00000DH00
20100120





For PVT

Change R477/R499 to 2.2kohm
Change R478/R498 to 3.9kohm
20100118

Follow Intel Setting
Change LED1, LED3 as SC591NB5A30
20100118

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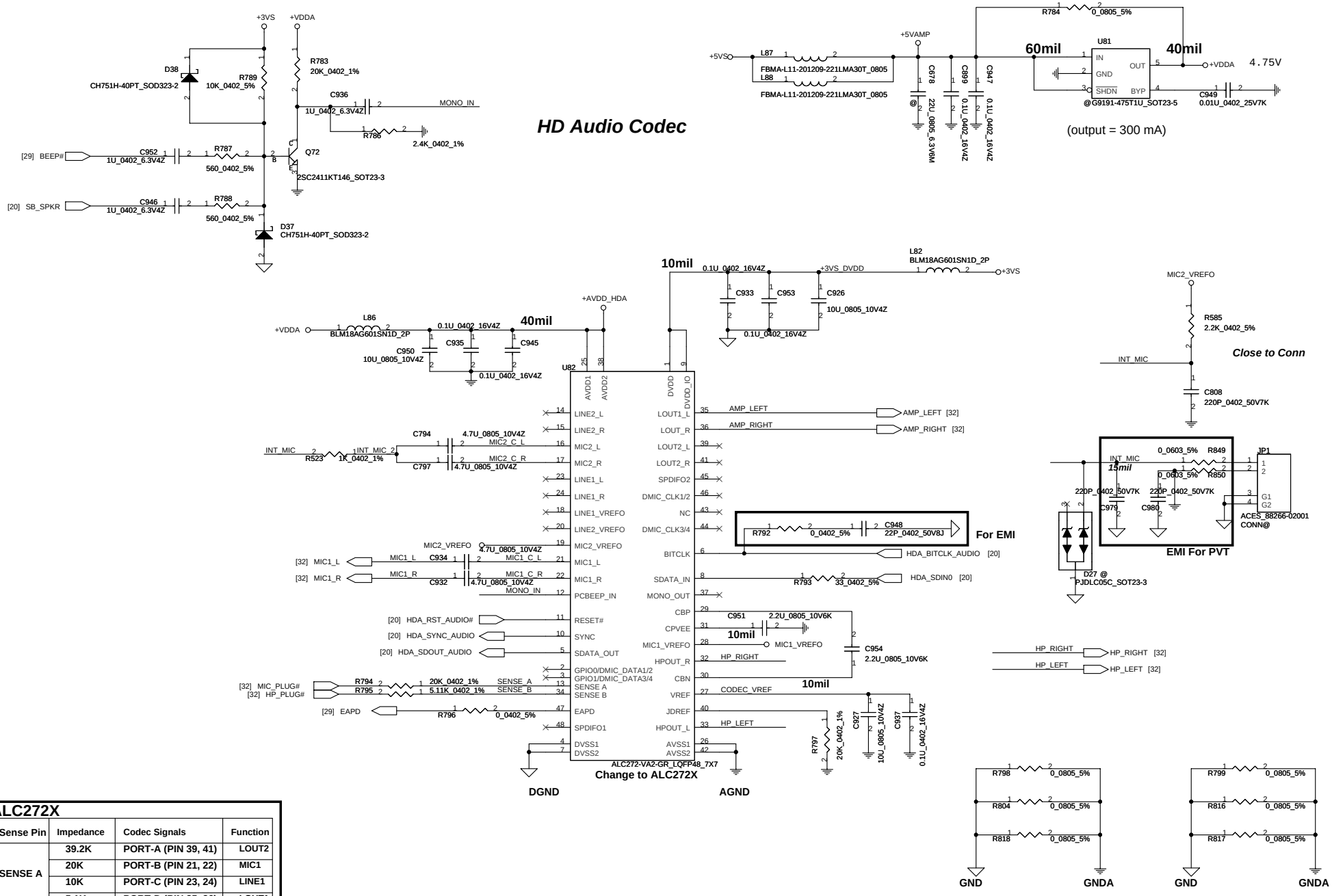

ALC272X

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K		
	5.1K	PORT-I (PIN 32, 33)	HP

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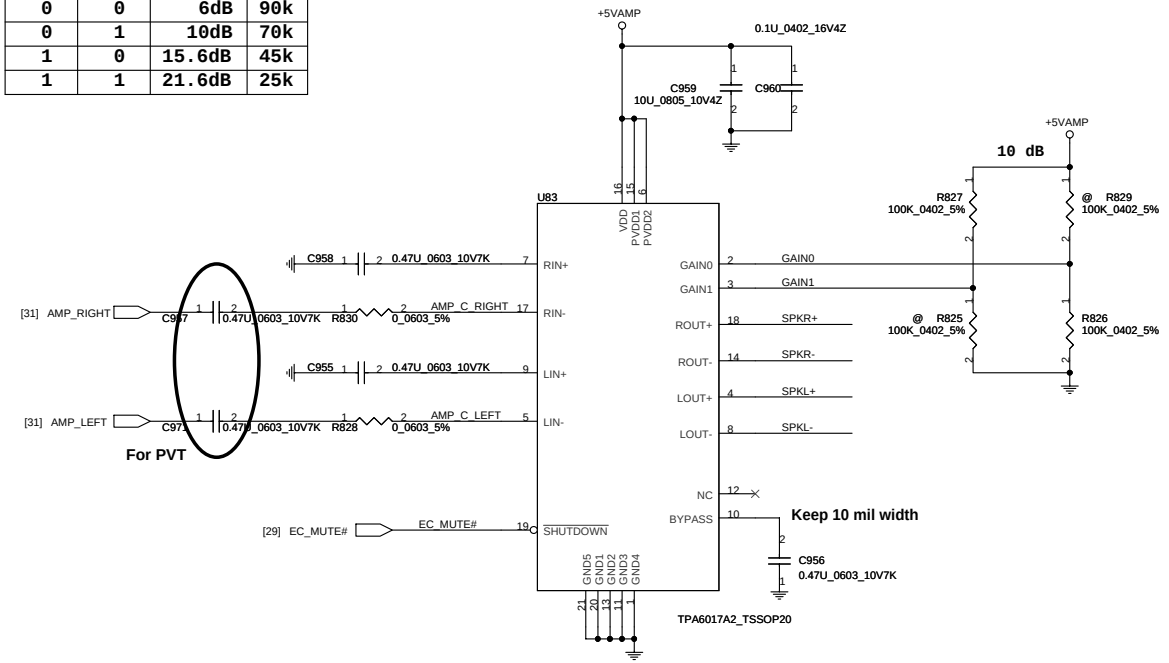
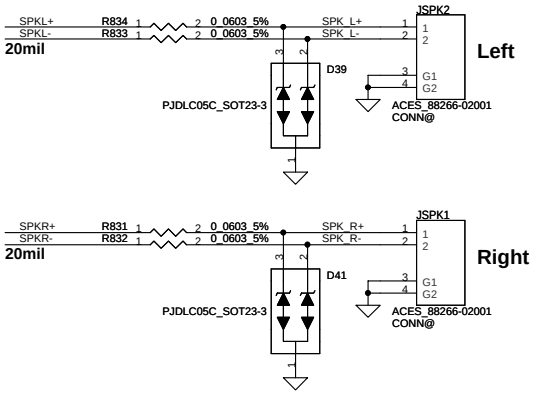
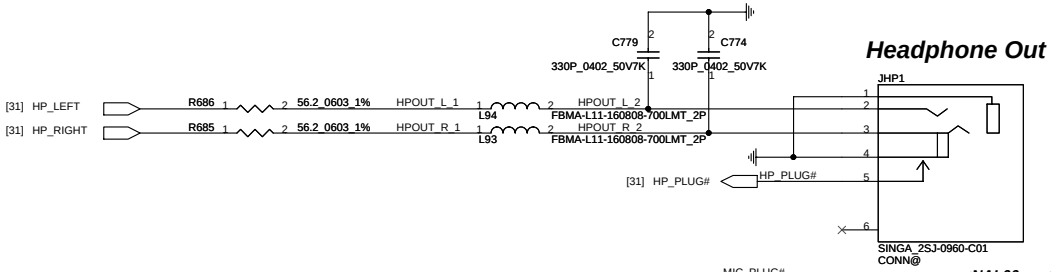
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



Int. Speaker Conn.



Headphone Out



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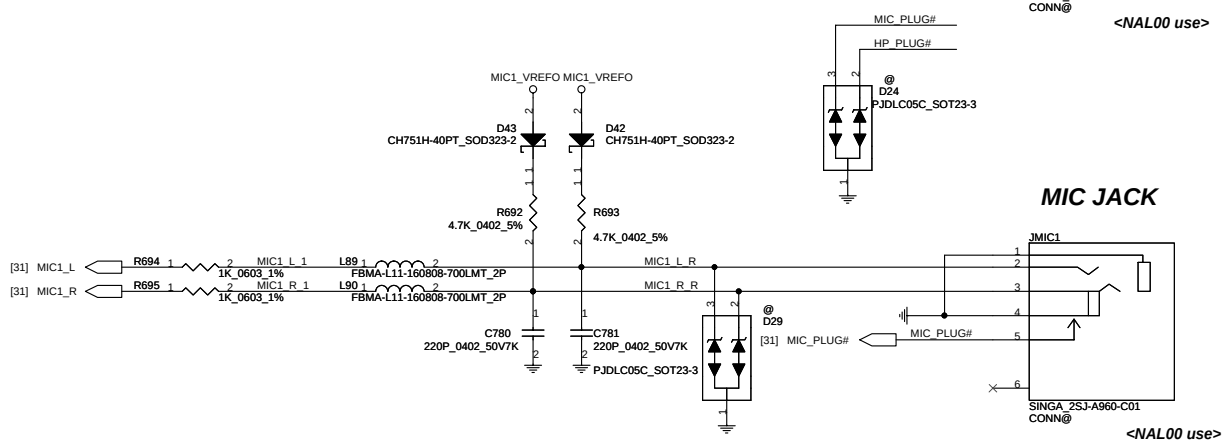

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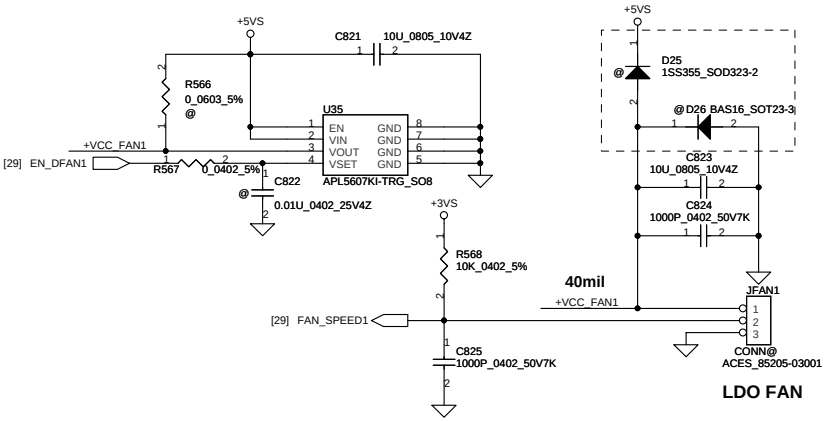
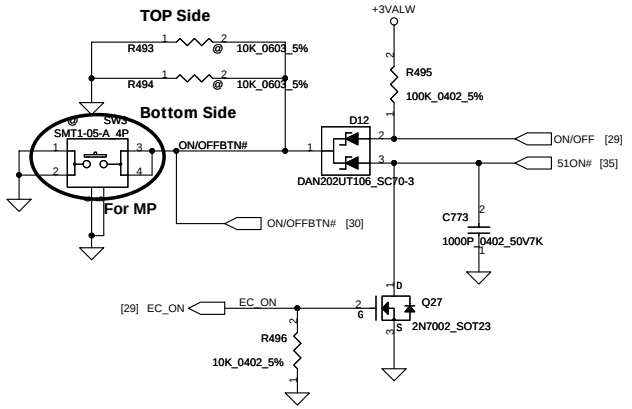
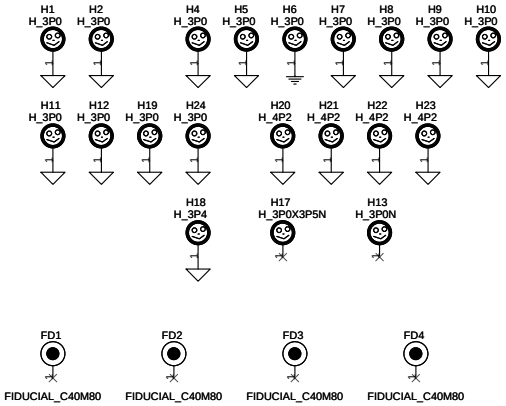
FAN1 Conn



LDO FAN

ON/OFF switch ***Power Button***





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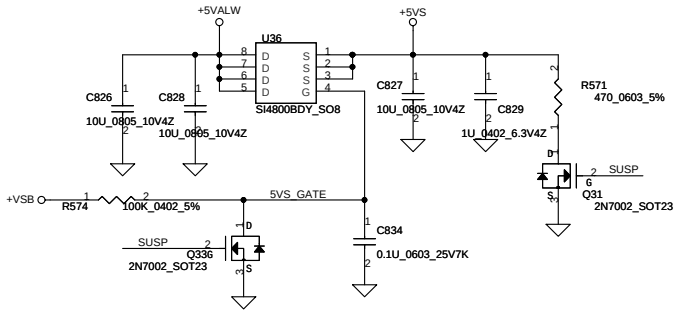
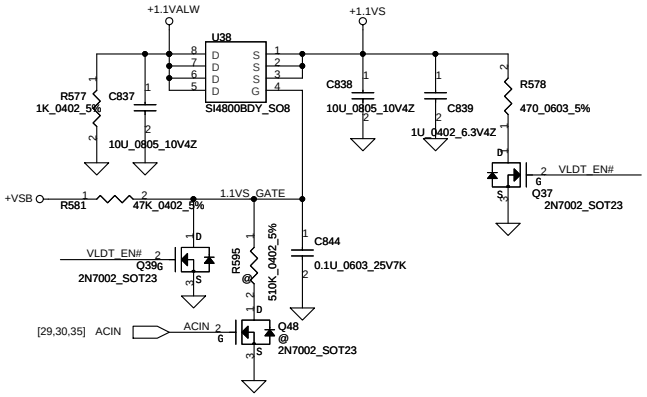
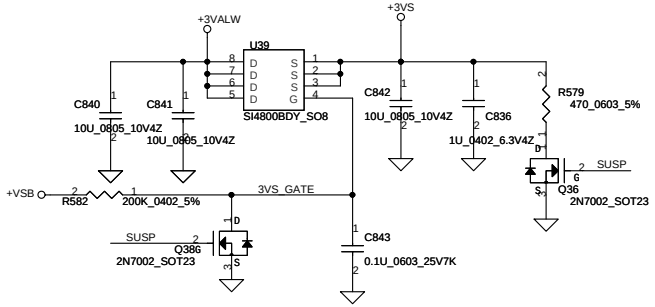
+5VALW TO +5VS



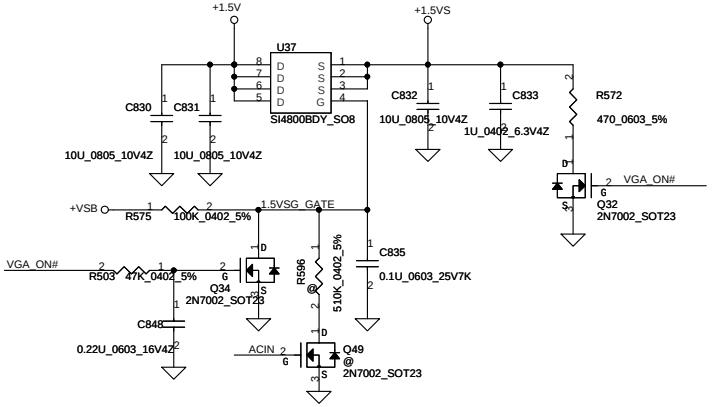
+1.1VALW TO +1.1VS

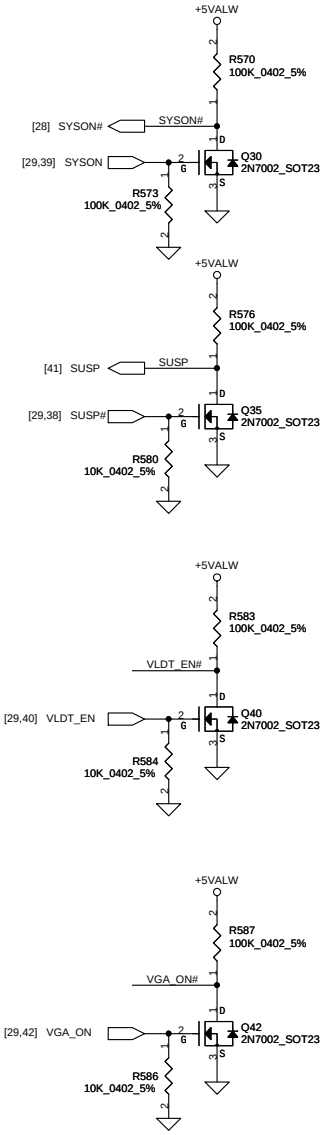


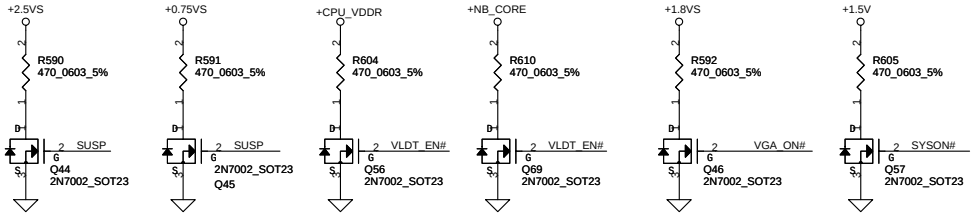
+3VALW TO +3VS

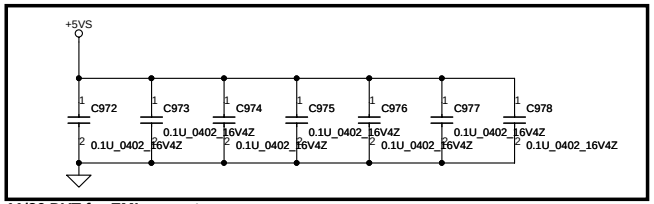


+1.5V to +1.5VS









11/26 DVT for EMI request

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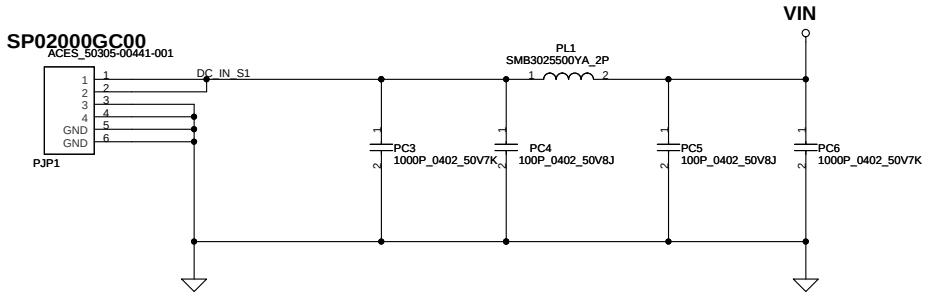
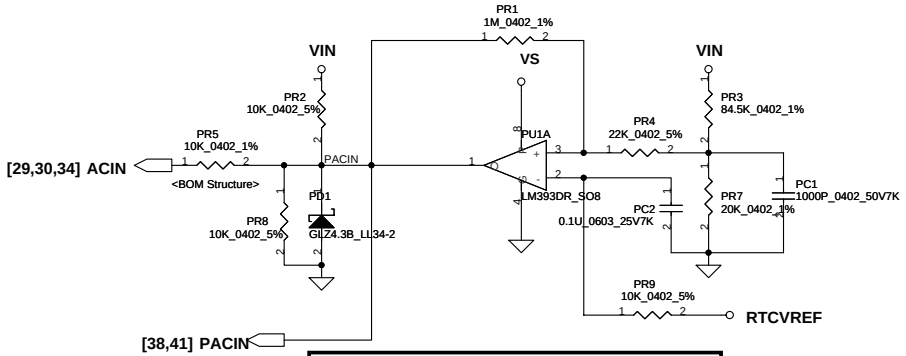
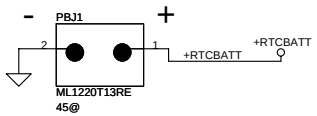
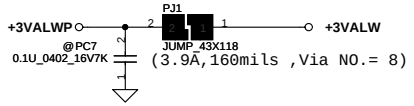


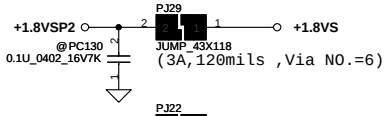


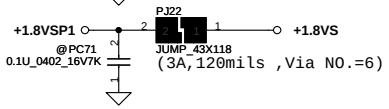
Vin Dectector

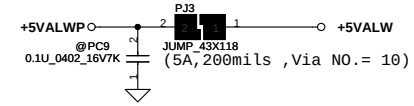
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

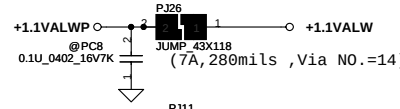


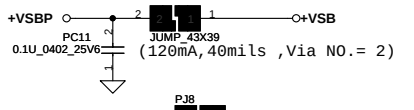


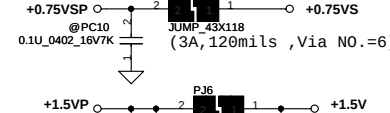


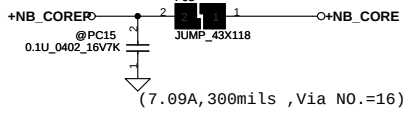


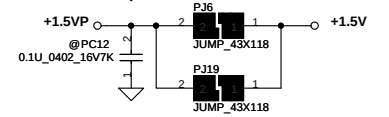


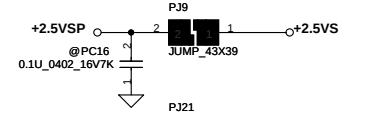


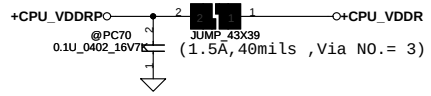


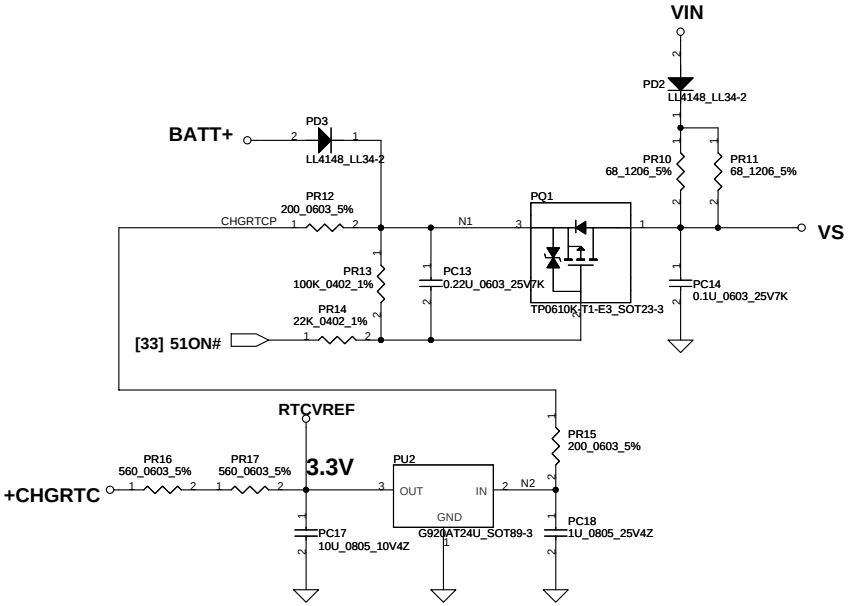












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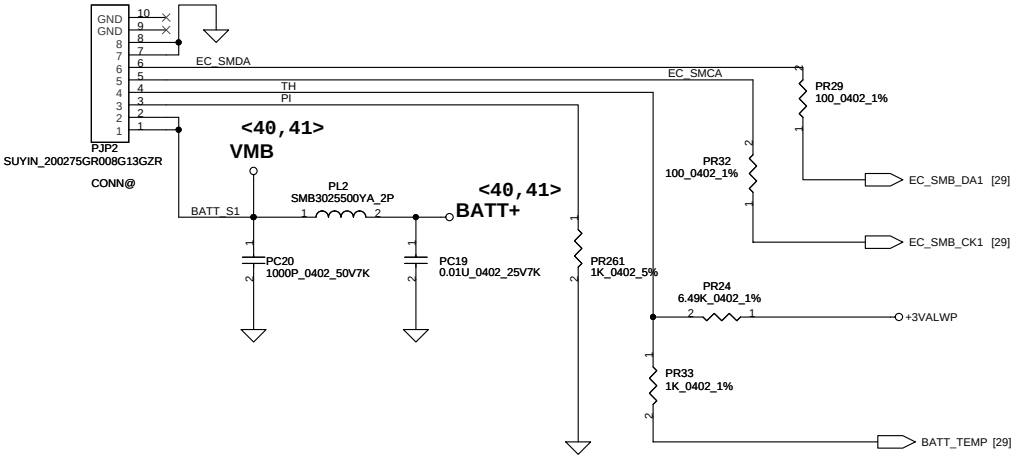
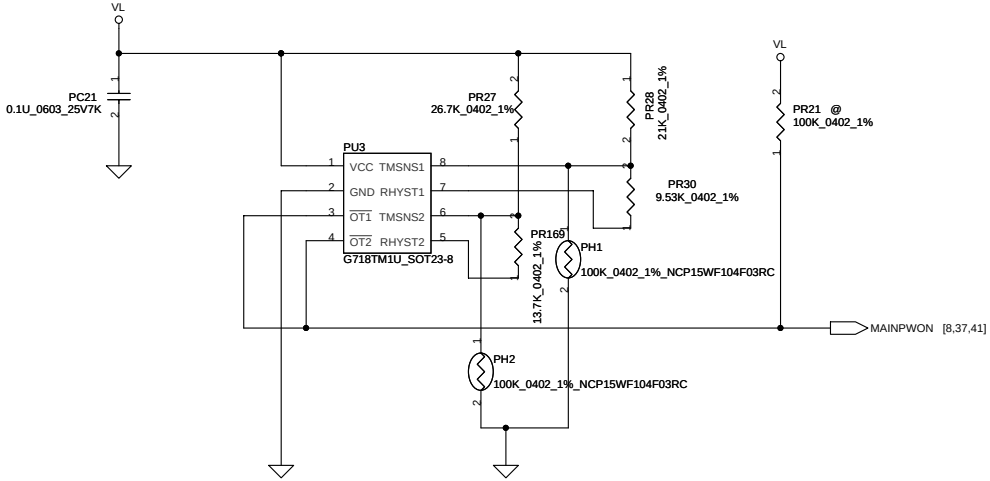
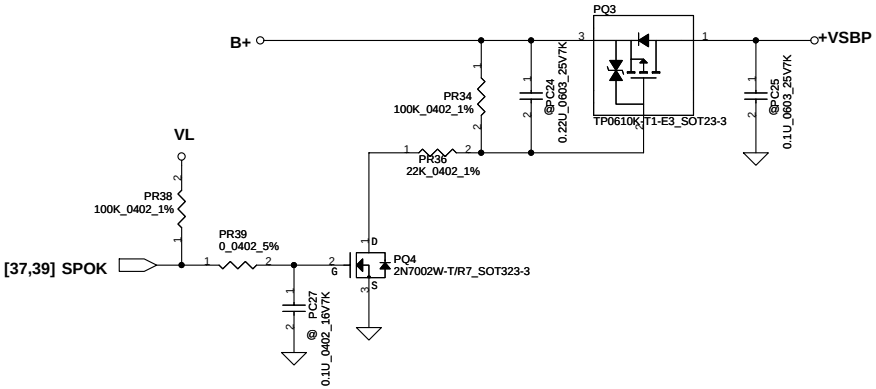
PH1 thermal protection at 92 degree C Recovery at 56 degree C
PH2 thermal protection at 85 degree C Recovery at 56 degree C







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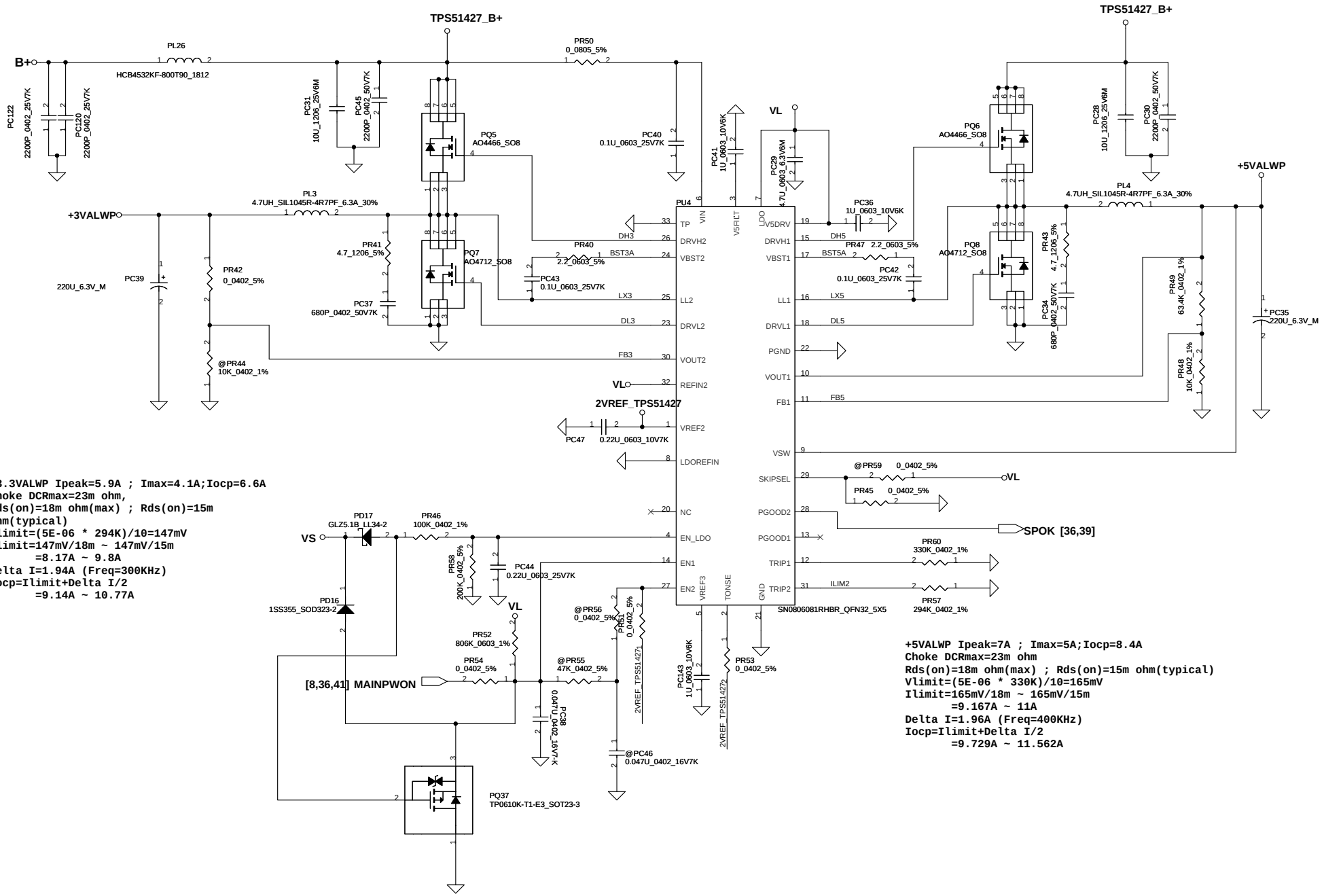

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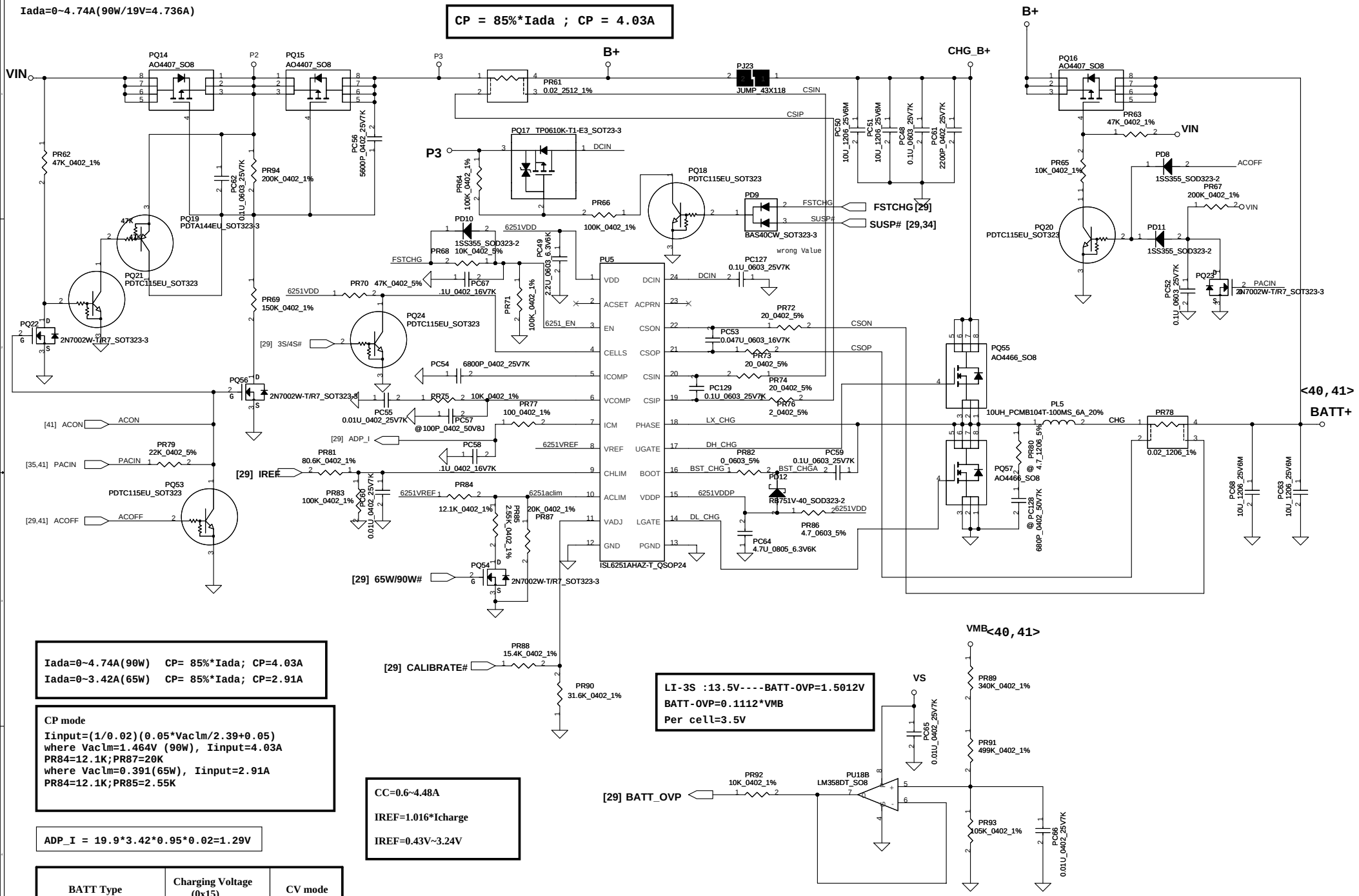
Iada=0~4.74A(90W/19V=4.736A)

CP = 85%*Iada ; CP = 4.03A



Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.03A
Iada=0~3.42A(65W) CP= 85%*Iada; CP=2.91A

CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vaclm=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K

ADP_I = 19.9*3.42*0.95*0.02=1.29V

CC=0.6~4.48A

IREF=1.016*Icharge

IREF=0.43V~3.24V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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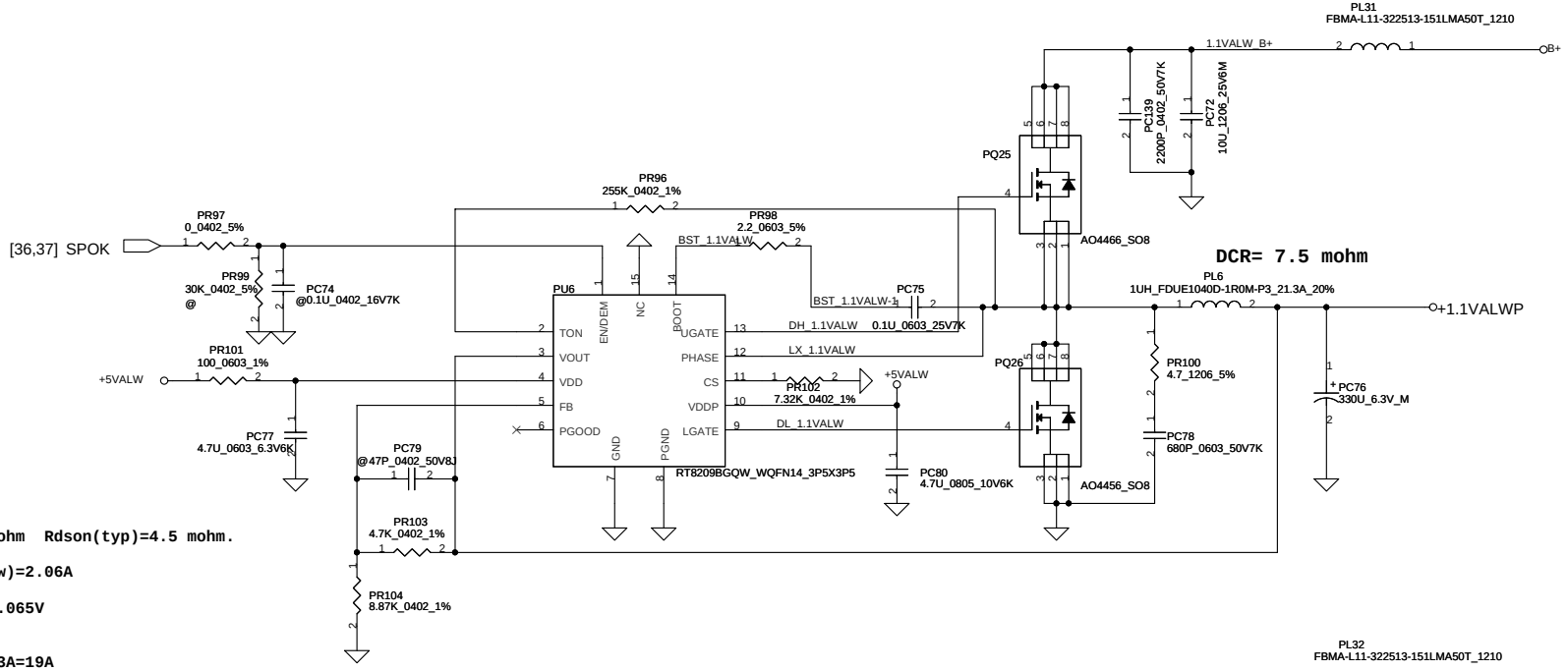
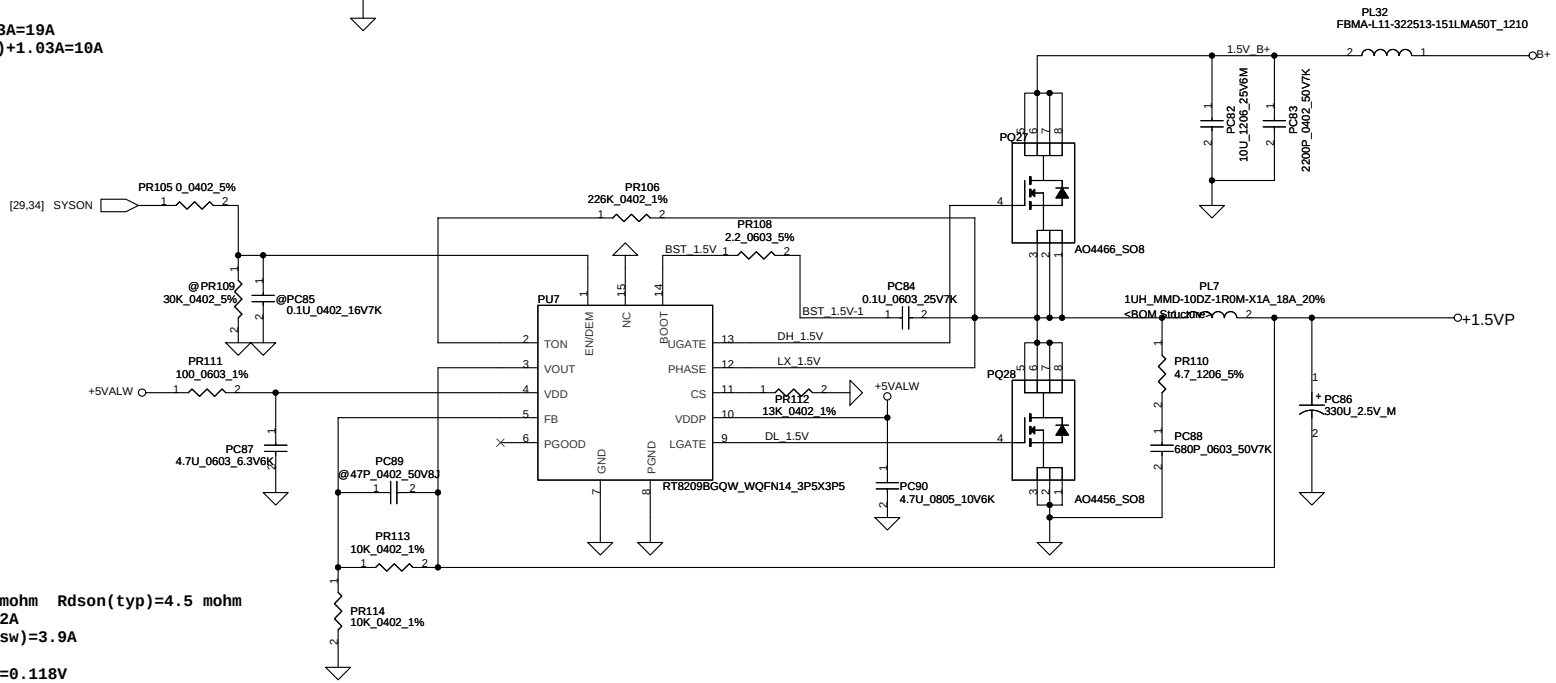


<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=7.42A, Imax=5.2A, Iocp=8.9A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
=>1/2Delta I=1.03A
Vtripmax=Iocp*Rdson=8.9*5.6*1.3=0.065V
Rcs=Vtrip/9uA=0.065V/9uA=7.2K
choose Rcs=7.32K
Iocpmax=((7.32K*11uA)/0.0045)+1.03A=19A
Iocpmin=((7.32K*9uA)/(0.0056*1.3))+1.03A=10A
Iocp=10A~19A



<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=335KHz

Cout ESR=17 mohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm
Ipeak=13.5A, Imax=9.5A, Iocp=16.2A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
=>1/2Delta I=1.95A
Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
Rcs=Vtrip/9uA=0.118V/9uA=13.1K
choose Rcs=13K
Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
Iocp=18A~32A

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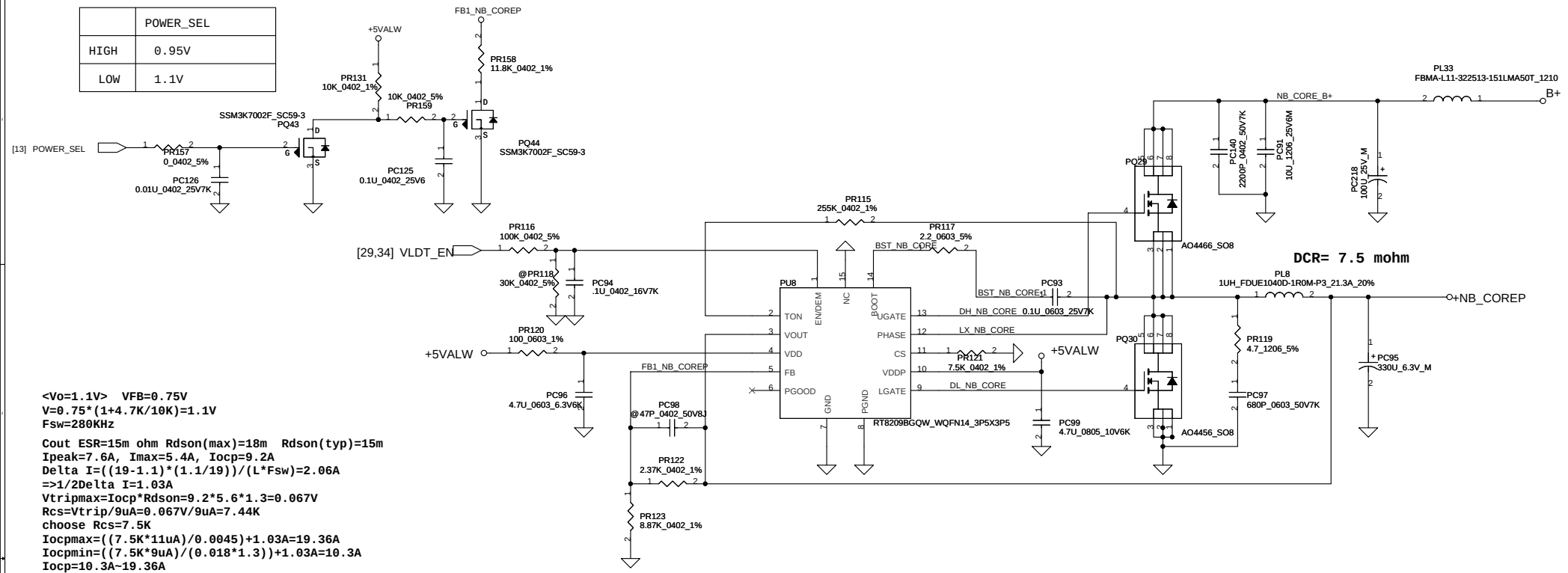
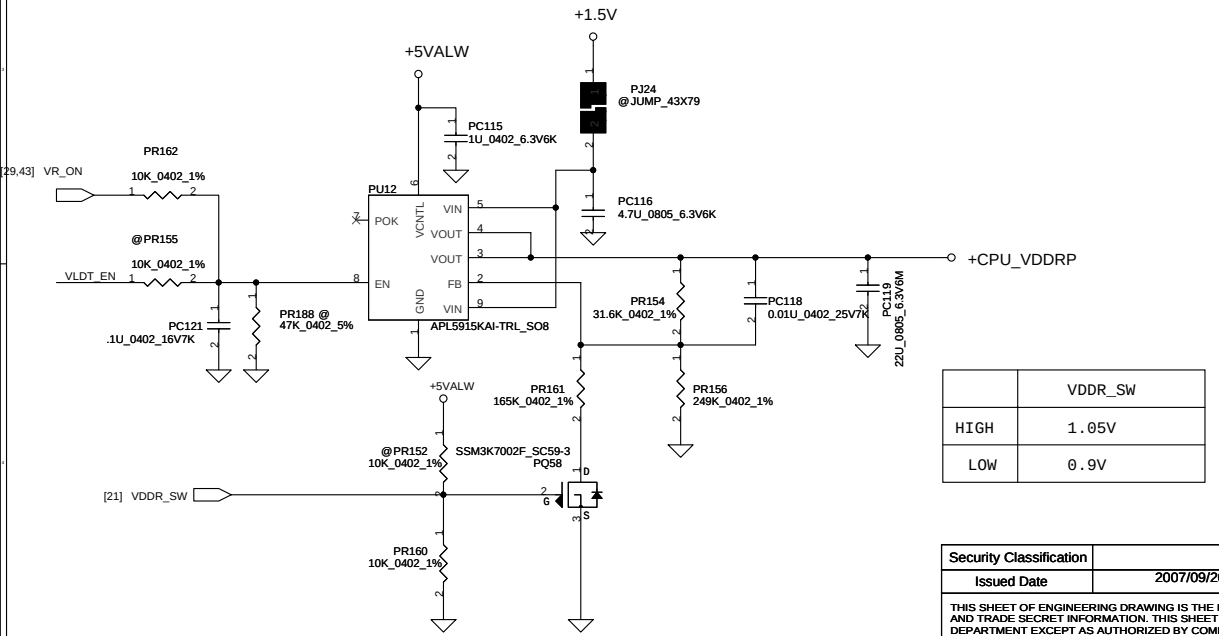
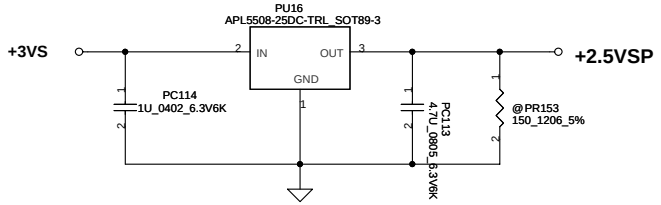
	POWER_SEL
HIGH	0.95V
LOW	1.1V



<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=18m Rdson(typ)=15m
Ipeak=7.6A, Imax=5.4A, Iocp=9.2A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
=>1/2Delta I=1.03A
Vtripmax=Iocp*Rdson=9.2*5.6*1.3=0.067V
Rcs=Vtrip/9uA=0.067V/9uA=7.44K
choose Rcs=7.5K
Iocpmax=((7.5K*11uA)/0.0045)+1.03A=19.36A
Iocpmin=((7.5K*9uA)/(0.018*1.3))+1.03A=10.3A
Iocp=10.3A~19.36A





	VDDR_SW
HIGH	1.05V
LOW	0.9V

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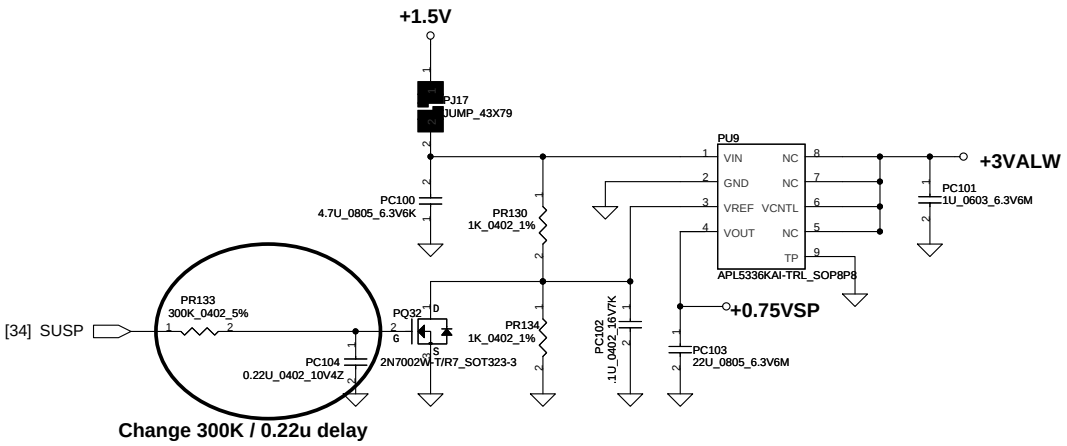
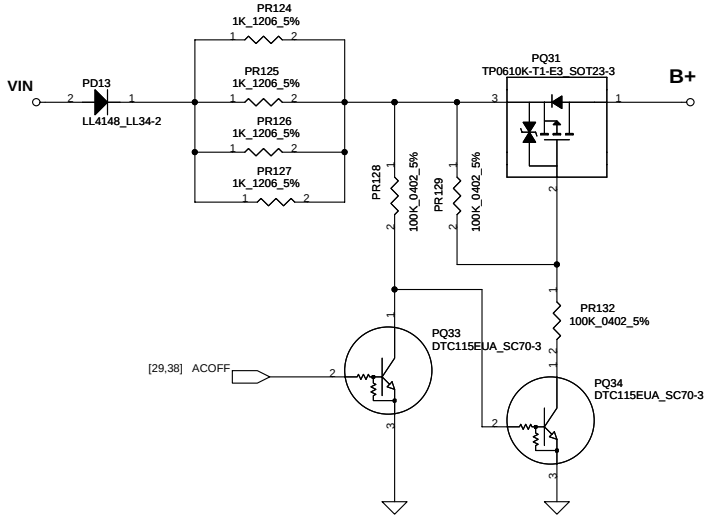
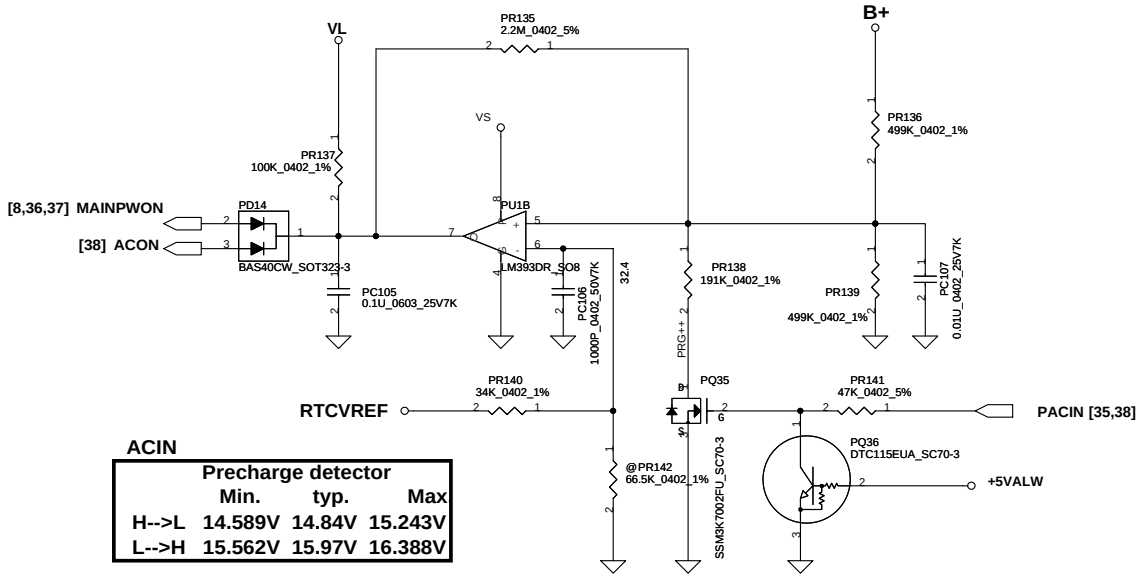


Ipeak=1A, Imax=0.7A





ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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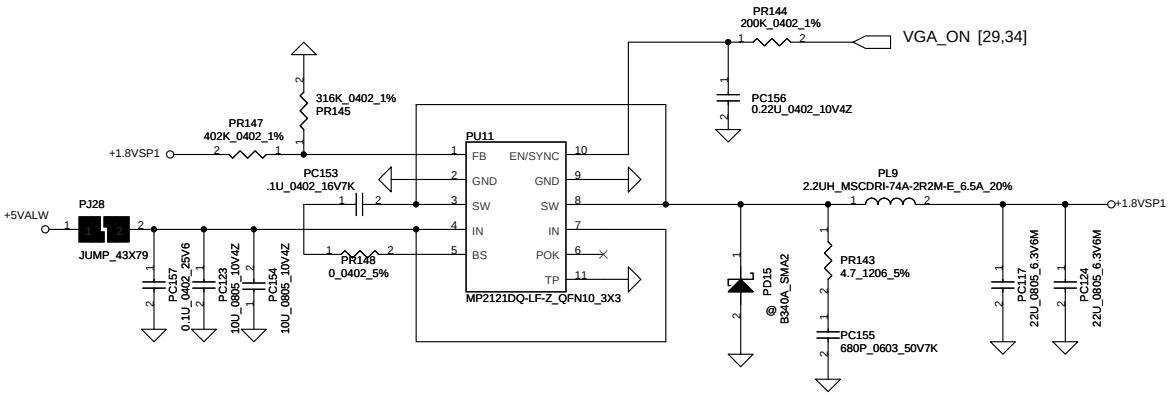

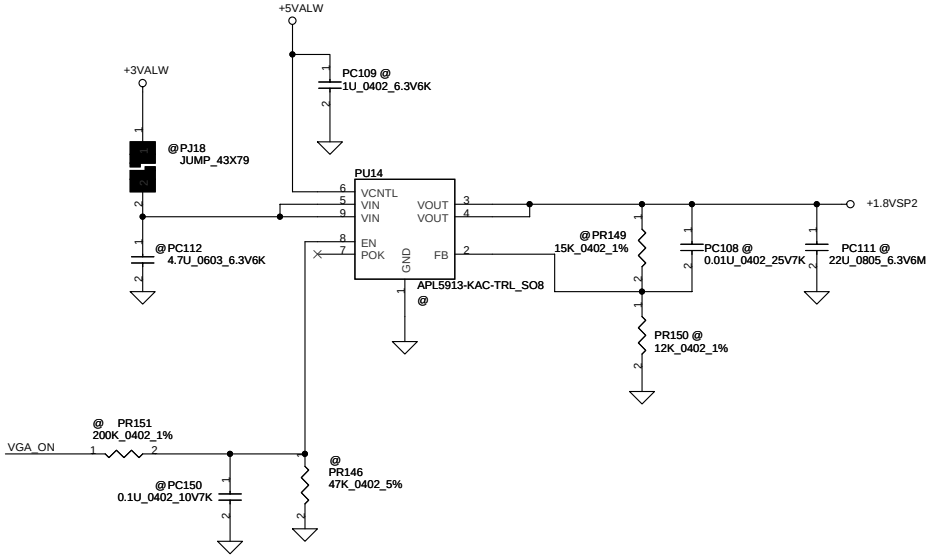

Security Classification	Compal Secret Data		
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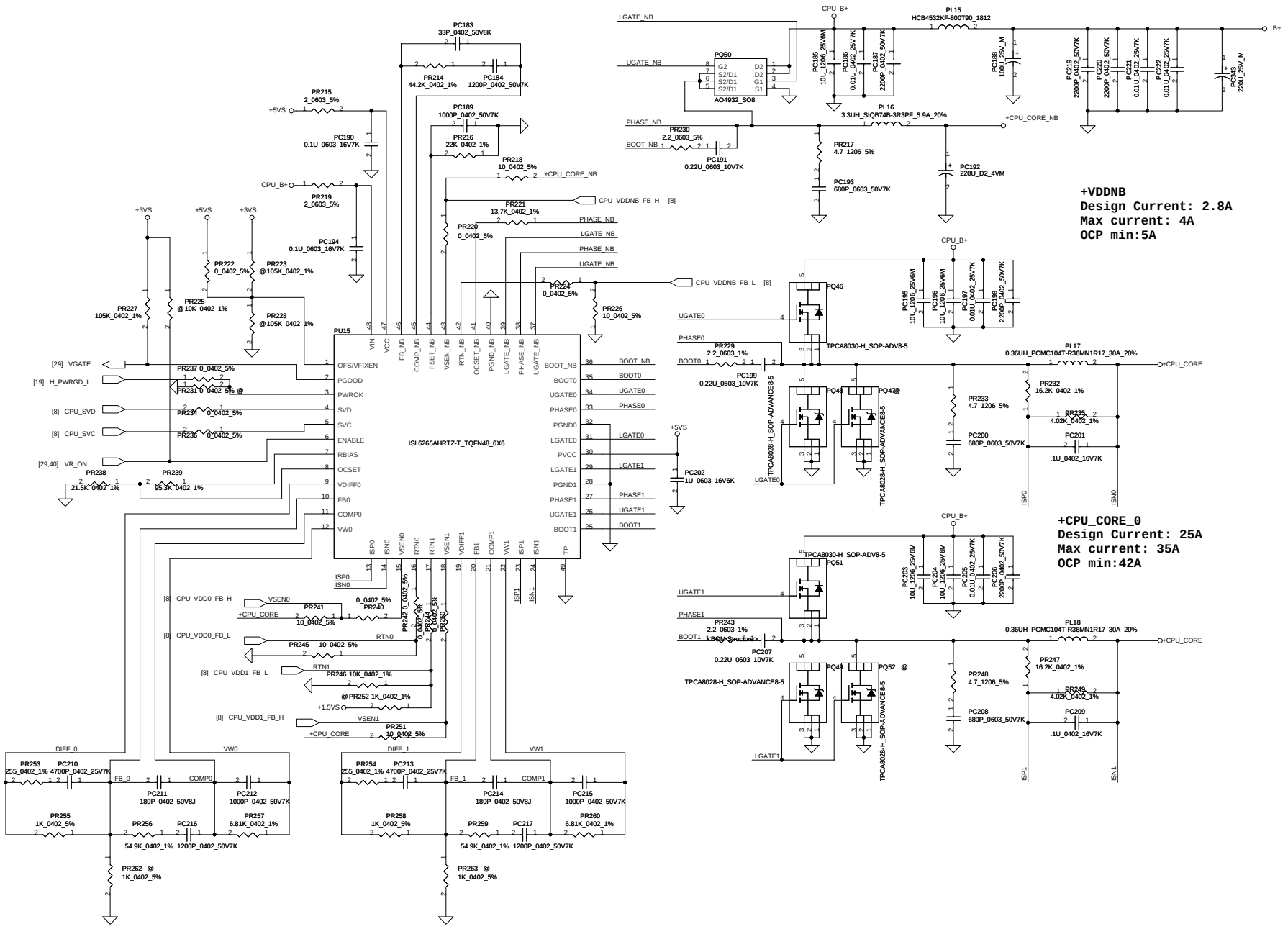

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD 2 switch mos and remove 2 pull high resistance to modify VGA_CORE switch level	Before modify to fault, we recognize that VGAPWRSEL pin is open drain state. But after check with AMD AE regoer to clear the foul that VGAPWRSEL pin has driviing ability.so i take away 2 pull high resistance and add 2 switch mos to modify the switch level.	0.1	52	ADD PQ60 and PQ61 remove PR212(10K,0402) and PR213(10K.0402)	2009/08/21	EVT_NAV71
2	change thermister , tune PH1 protection and recovery set point	change thermister from 150K to 100K	0.1	44	thermister part number SL200000V00 and PR28 change to 21K, PR30 change to 9.53K	2009/08/27	EVT_NEW75
3	Add GPU voltagr sence net	Cause GPU have GCORE_SEN and FB_GND pin so power add receive net.	0.1	51	ADD GCORE_SEN and FB_GND net, also add PR296(0_0402_1%), PR297(10_0402_5%) and PR298(0_0402_5%)	2009/09/04	EVT_NEW75
4	change DC-IN connector part number	to meet pin definition	0.1	43	change part number is SP020908120	2009/09/10	EVT_NEW75
5	change reistance PR81 value	Cause meet battery Ki value setting from 1.106 to 0.7224. change PR81 from 154K(0402_1%) to 80.6K(0402_1%)	0.1	46	change resistance PR81 value from 154K to 80.6K	2009/09/22	EVT_NEW75
6	ADD switch circuit for 1.05V	Cause follow AMD electrcial sheet, VDDIO/ VDDR voltage setting procedure. AMD processor will switch between 1.05V and 0.9V by VDDIO and VDDR	0.1	48	ADD PR161 (165K_0402_1%), PQ58,PR152(10K_0402_5%),PR160(10K_0402_5%), PC131(0.1U_25V6) , change PR161 value from 100K to 249K, and ADD enable net name -VDDR_SW	2009/09/22	EVT_NEW75
7	Change enable signal of +CPU_VDDRP	Cause follow HW demand	0.1	41	change +CPU_VDDR enable signal from VLDT_EN to VR_ON	2009/10/02	EVT_NEW75_6L
8	change resistance size	cause for component de-rating . Prevent the component break down when inrush current happen.	0.1	39	change PR61 from (0.02_1206_1%) to (0.02_2512_1%)	2009/10/06	EVT_NEW75
9	change capacitor value for 0.75VSP request	Cause follow HW request	0.1	41	Change PC103 value from 10u to 22u	2009/10/15	EVT_NEW75_6L
10	Add snubber and boost resistance of 1.1Valw and 1.5V	Cause follow EMI request	0.2	39	Add 4.7 ohm to PR100, add cap. 680p to PC78 and add 2.2 ohm toPR98. Add 4.7 ohm to PR110, add cap. 680p to PC88 and add 2.2 ohm toPR108	2009/11/23	EVT_NEW75_6L
11	Add bead	For reduce B+ noise	0.2	37,39,40	Add PL31,PL32,PL33(SM010020720) and PL26(SM010018210)	2009/11/23	EVT_NEW75_6L
12	Change chock	Cause A phase put wrong chock	0.2	37,39,40	Change PL9 from SH00000FK00 to SH000009Q00	2009/11/23	EVT_NEW75_6L
13	Change resistance value	Cause Hw request 1.1Valw need to set to 1.15V, so change divider resistance PR104	0.2	39	Change PR104 from SD000000680 (S RES 1/16W 8.45K +-1% 0402) to SD034887180 (S RES 1/16W 8.87K +-1% 0402)	2009/12/01	EVT_NEW75_6L
14	ADD capacitance	Cause EMI request	0.2	43	ADD PC219 PC220 SE074222K80 (S CER CAP 2200P 50V K X7R 0402) and PC221 PC222 SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402)	2009/12/01	EVT_NEW75_6L
15	change resistance value	Cause NB_CORE need to switch	0.2	40	change PR158 from SD034232280 (S RES 1/16W 23.2K +-1% 0402) to SD034118280 (S RES 1/16W 11.8K +-1% 0402)	2009/12/01	EVT_NEW75_6L
16	ADD Boost resistance	Cause EMI request	0.2	37-43	ADD PR40, PR47,PR117 and PR230 from SD013000080 (S RES 1/10W 0 +-5% 0603) to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	2009/12/01	EVT_NEW75_6L

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11/20

1. P.21 unstuff Y4, C588, C589, R368 for AMD suggest
2. P.19 Modify Y3 net connect
3. P.25 Change C923, C924 as 33pF for Y5

11/24

1. P.13, P.15, P.20, P.23 Add Ext@ & Int@ option ; Modify CLK_SBLINK_BCLK net connect
2. P.13, P.16, P.20 Add VB@ & UNVB@ option
3. P.34 Change U38 as 4430(SB000007O10)
4. P.27 Add R835, R837 unstuff D44, R836 for WiMax/Wlan LED request ; change R492 as 100Komh for EC request
5. P.30 Change R477, R499 as 680ohm ; R478, R498 as 3.9kohm for LED brightness

11/25

1. P.19, P20 update SB GPIO PIN
2. P.29 Add R838, R839 for EC RevD3, E0
3. P.34 Add C972, C973, C974, C975, C976, C977, C978 for EMI Request
4. P.15 Remove R245, R247 for unSD CLK
5. P.13 Add R840 for CLK_NB_14.318

11/28

1. P.30 JLED1, JLED2 Pin define modify; Add Q73
2. P.23 Add R841, R842, R843 ; P.29 Add R844, R845 for Panel Low Power
3. P.28 Change D10 P/N as SC300000B00 ; Stuff D41, D27, D39, D11, D13, D29, D24 For ESD Request

PVT

01/18

1. P.17 Add HDMI@
2. P.19 Change C56 as SF000002N00(H4.4)
3. P.13 stuff R67, unstuff U4 for NB_PWRGD
4. P.21 stuff R424 for +CPU_VDDR
5. P.30 Change LED1, LED3 as SC591NB5A30 ; Change Resistance value for NEW75/85/95
6. P.32 Change C957, C971 as 0.47UF
7. P.20 Unstuff R359, R360 for SB_SIC, SB_SID

01/25

1. P.30 Change Q26 as SB00000DH00
2. P.29 Define U26 Pin 36, Pin 17, Pin 85, Pin86 for WWAN & WLAN
3. P.31 Reserve C979, C980, R849, R850 for EMI solution
4. P.9 Change C23, C24, C25, C26, C75 as SGA19331D10 (ESR 9 ohm)

03/02

1. P.29 Add R851, unstuff R852

03/30 For MP

1. P.8, P33 unstuff C21, SW3 for MP

05/18 For Cost down

1. P.8, P.29, P.31, P.32 unstuff Q73, D24, D27, D29, U2, U40, C681, R304 ,C687, R411 stuff R283

05/18 For PEW56

1. Modify SB GPIO64, B_ID, P_ID, LED, TSI BOM option

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