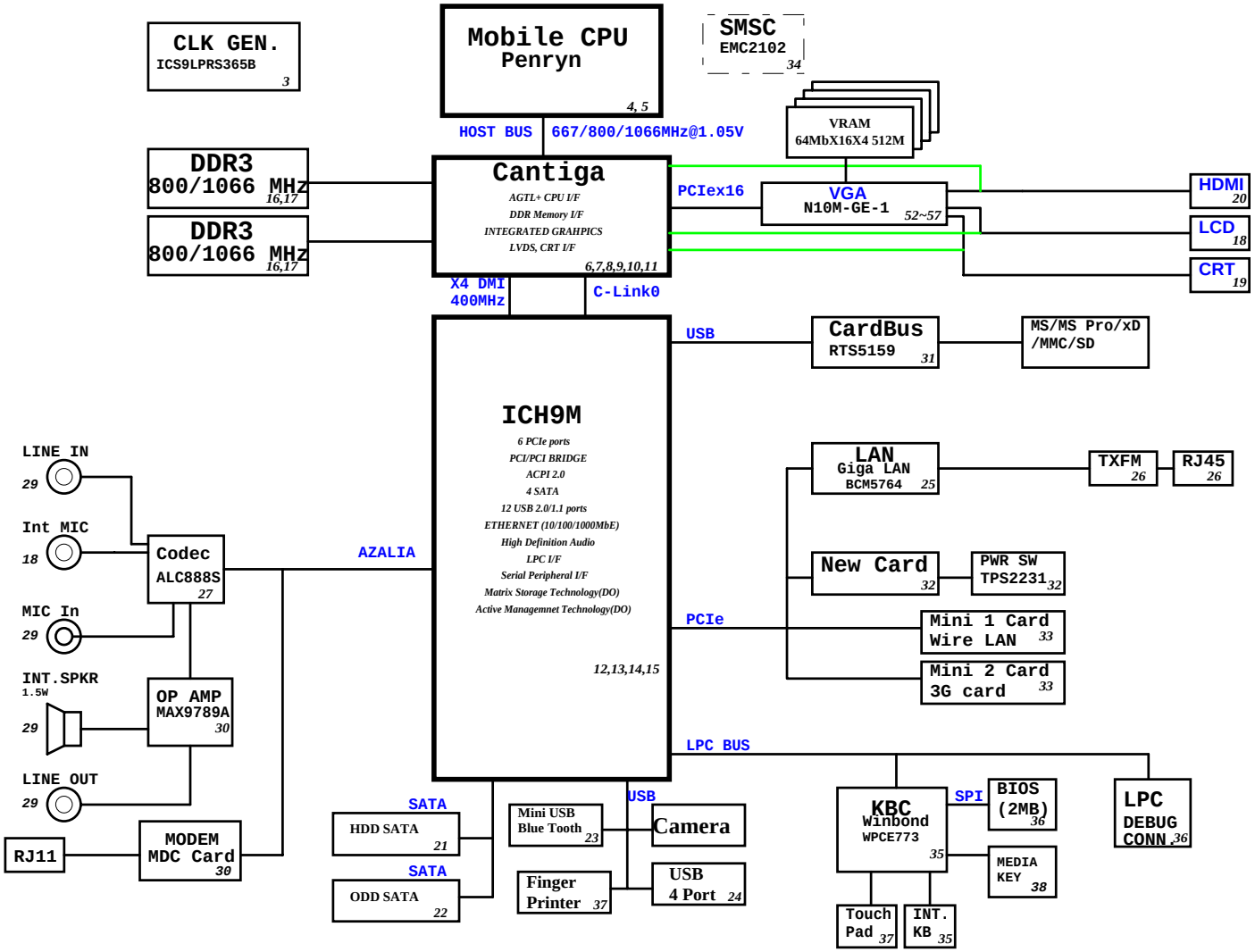
JV50 Block Diagram

Project code: 91.4CG01.001
PCB P/N : 48.4CG01.0SA
REVISION : 08245-SA



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SYSTEM DC/DC ISL62392 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44	
1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44	
1D5V_S3	1D1V_S0(2A)

TPS51117 45	
DCBATOUT	FBVDD(4A)

CHARGER ISL88731A 47	
INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202A 47	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

JV50

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Title: BLOCK DIAGRAM

Size: A2 | Document Number: JV50 | Rev: SB

Date: Tuesday, December 16, 2008 | Sheet 1 of 60

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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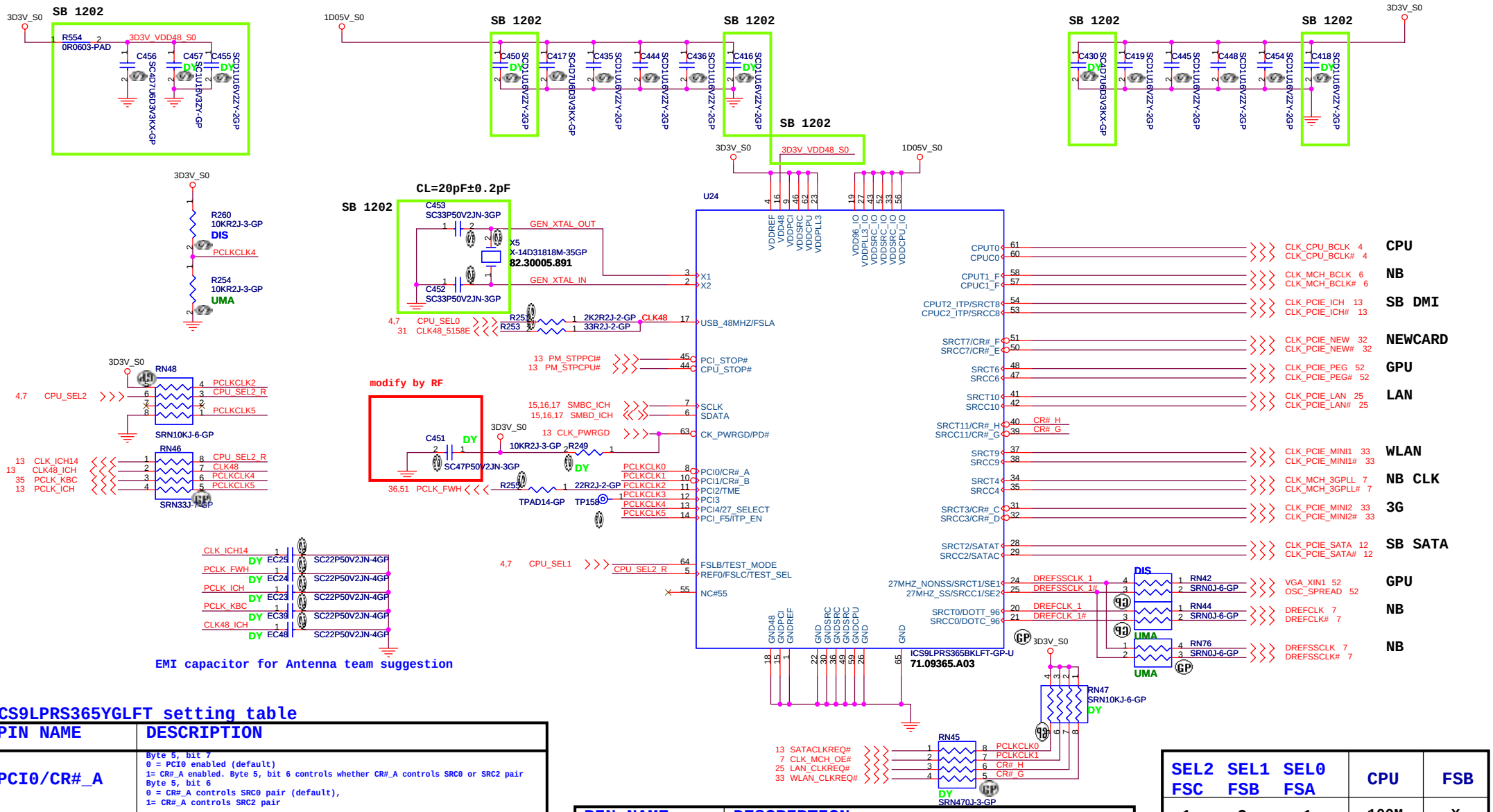
Title: ***Reference***

Size: A3 | Document Number: JV50 | Rev: SB

Date: Tuesday, December 16, 2008 | Sheet 2 of 60



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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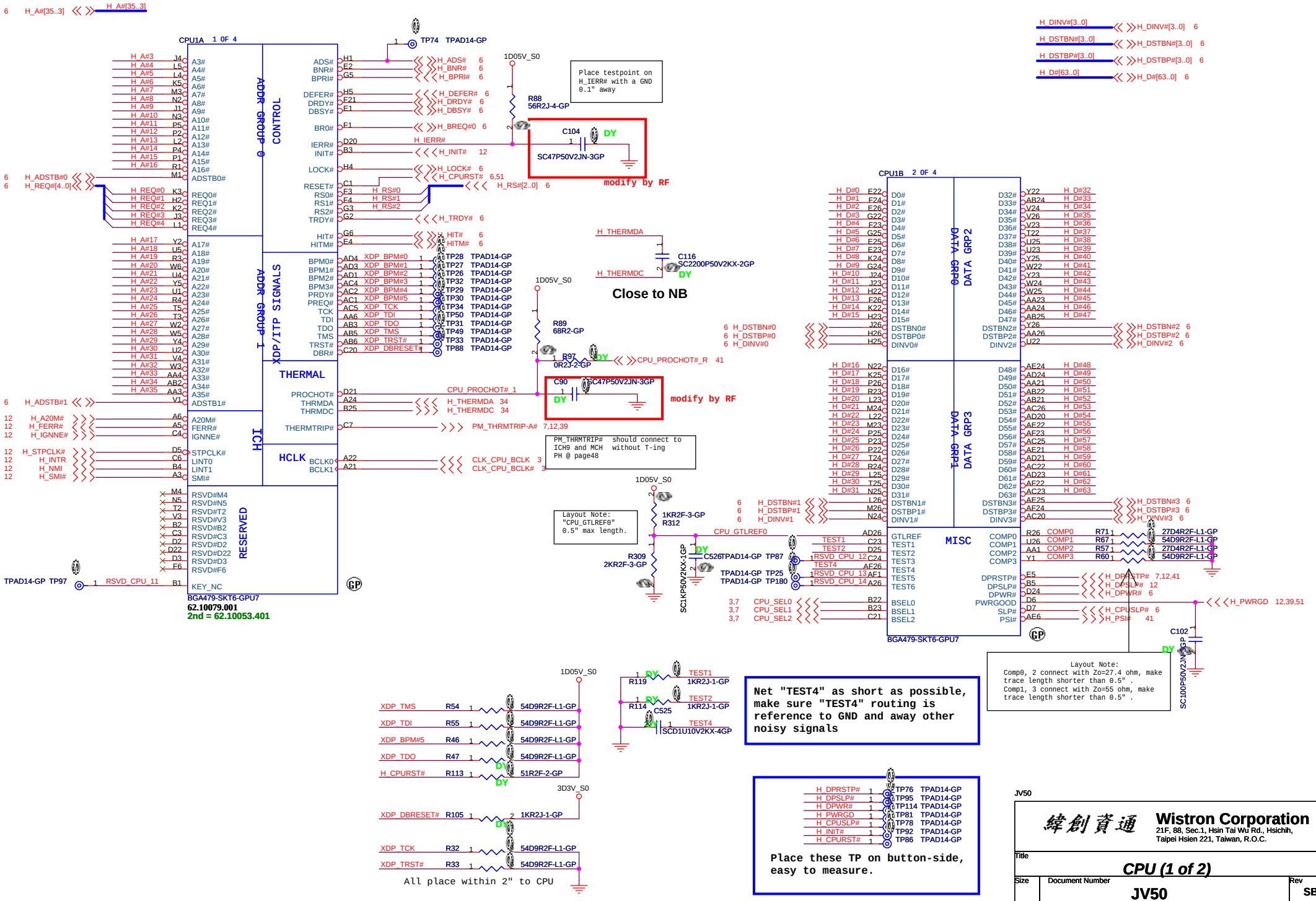
Title: Clock Generator

Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 3 of 60


CPU1A 1 0F 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
CPU1B 2 0F 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU7
Place testpoint on H_IERR# with a GND 0.1" away
modify by RF
Close to NB
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
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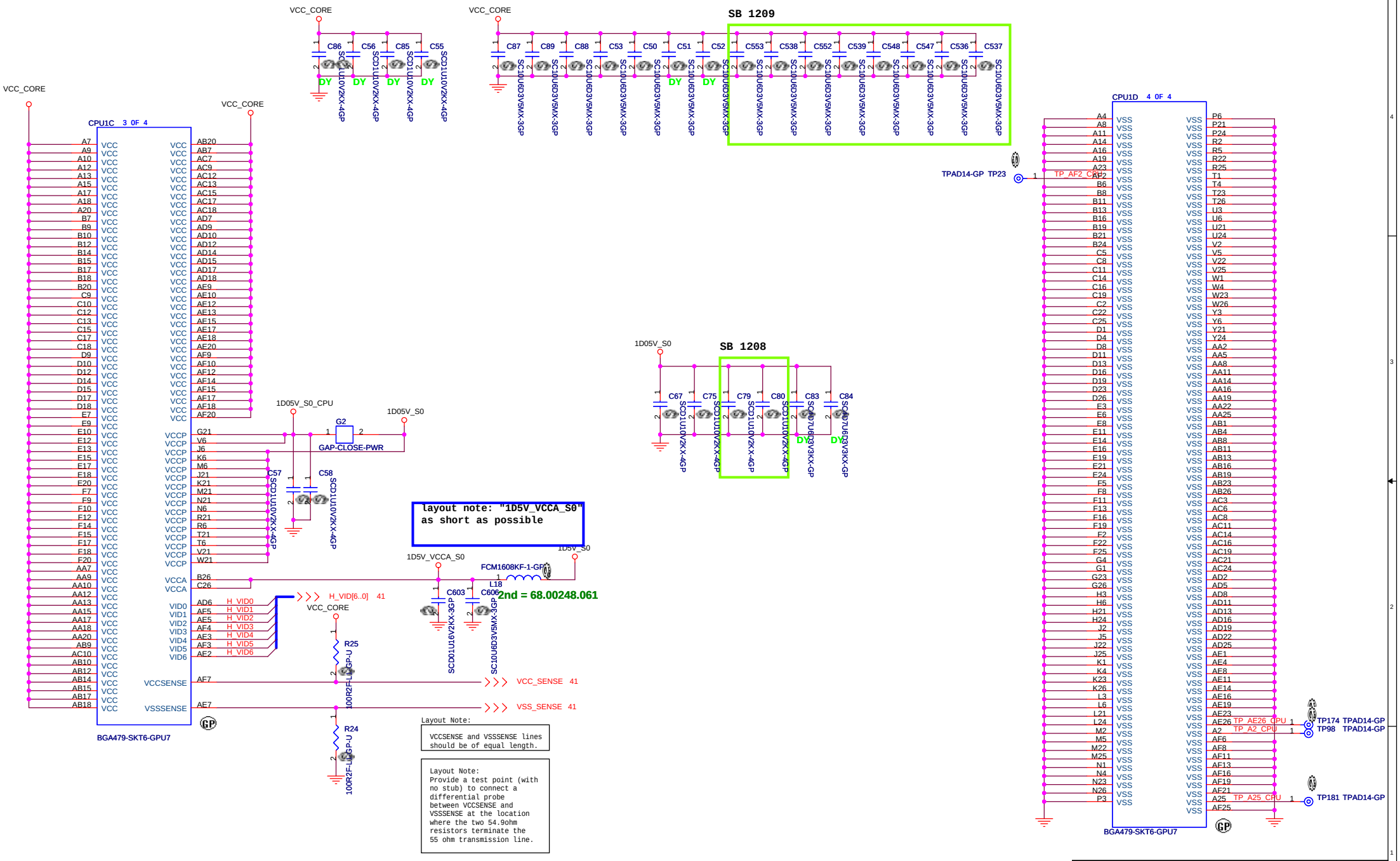
CPU (1 of 2)
JV50
Rev SB
Tuesday, December 16, 2008
Sheet 4 of 60



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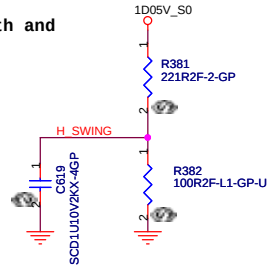
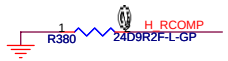
Title	***CPU (2 of 2)***	
Size	Document Number: **JV50**	Rev: **SB**
Date: Tuesday, December 16, 2008	Sheet 5 of 60	

H_SWING routing Trace width and Spacing use 10 / 20 mil

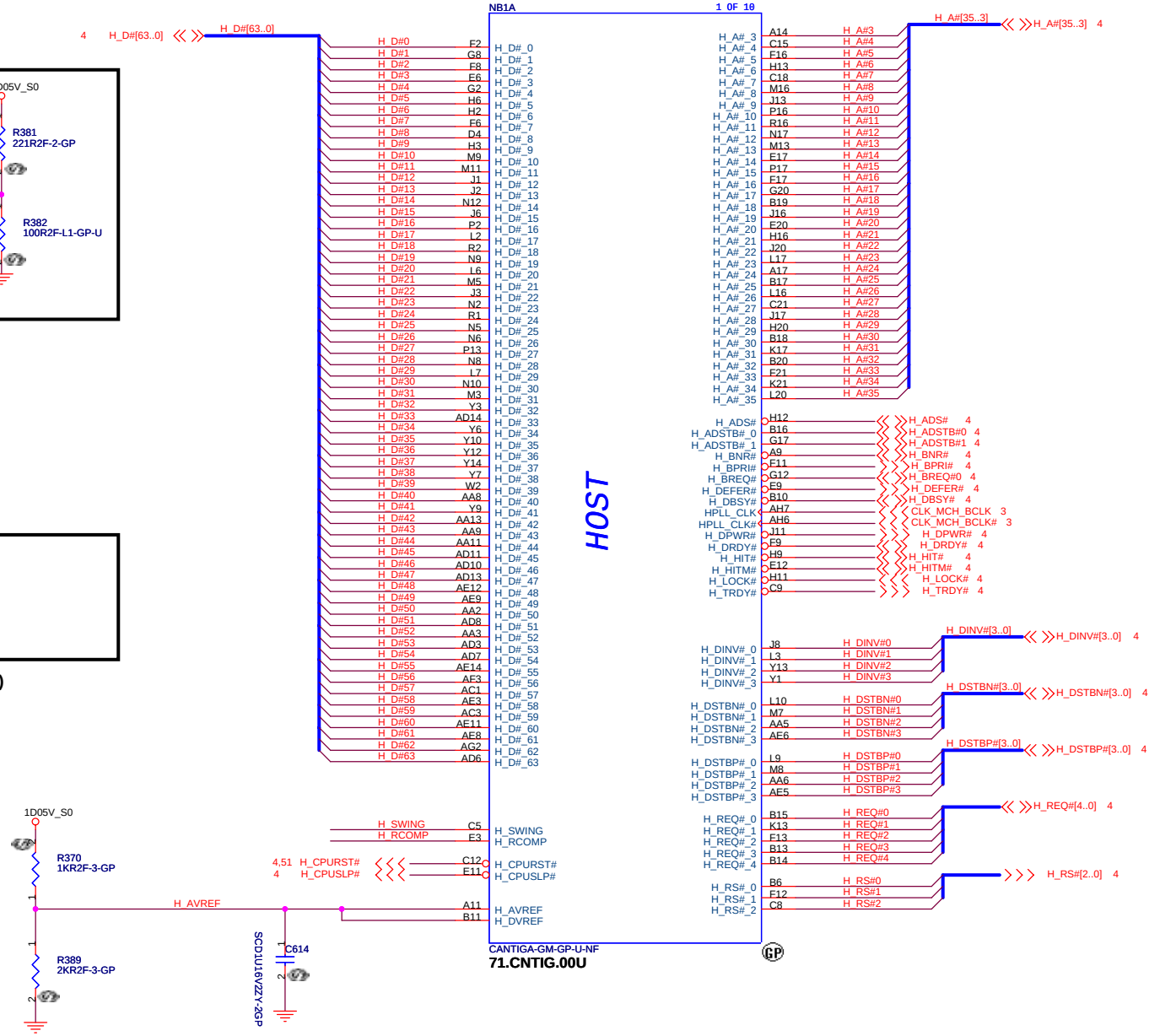
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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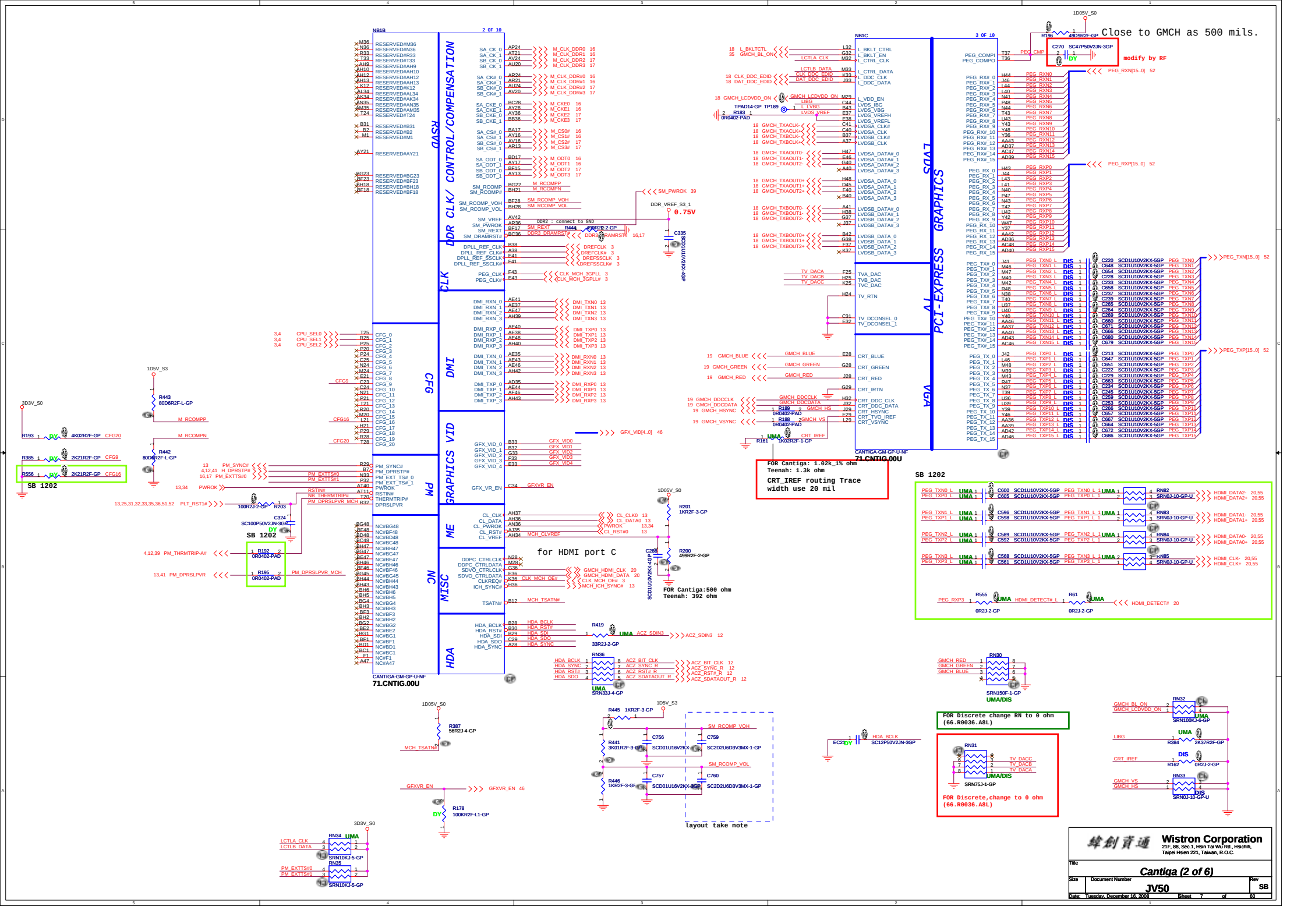
Title	*Cantiga (1 of 6)*	
Size	Document Number: JV50	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 6 of 60	


Close to GMCH as 500 mils.
modify by RF
SB 1202
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
layout take note
DDR_VREF_S3_1 0.75V
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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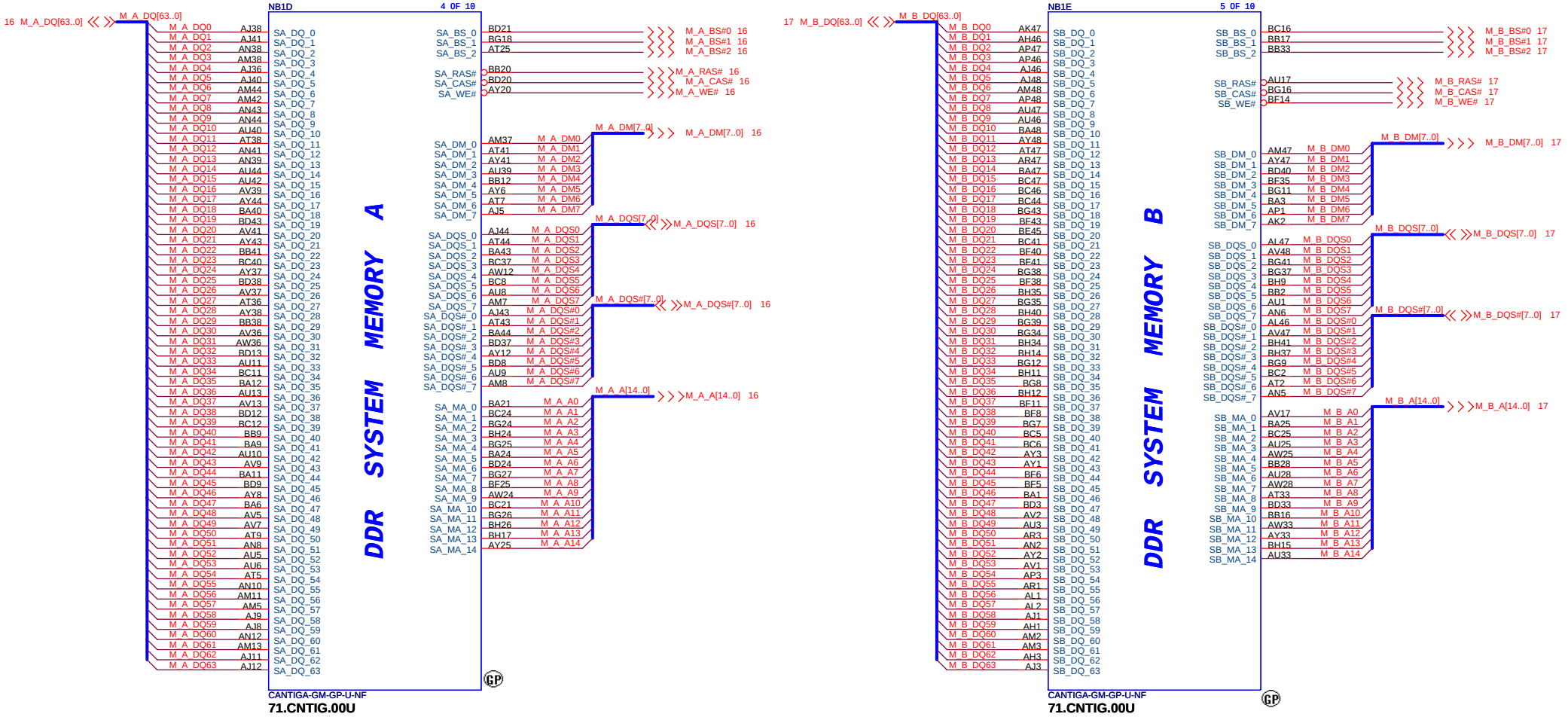
Cantiga (2 of 6)
JV50
Tuesday, December 16, 2008



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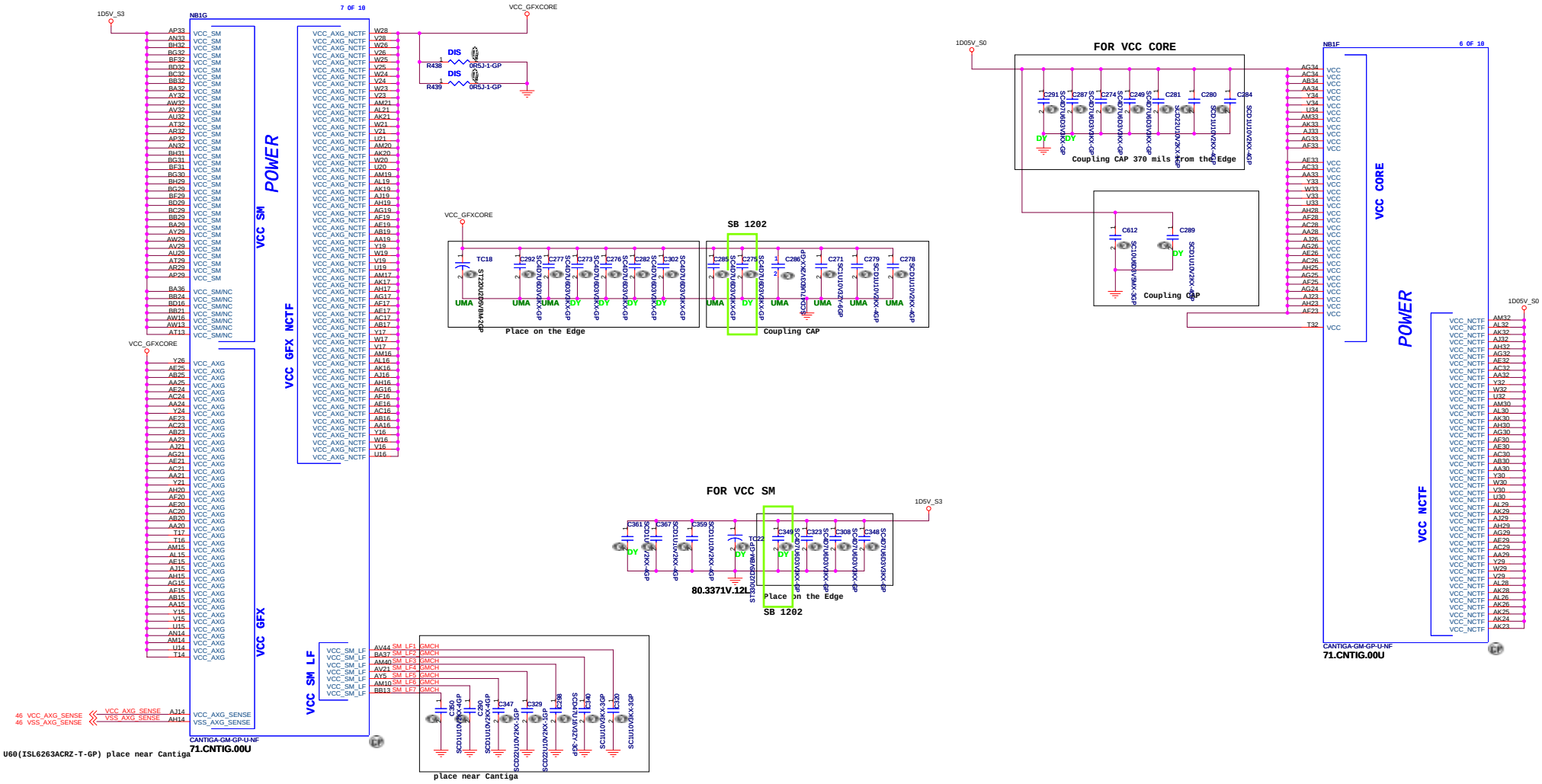
Title: Cantiga (3 of 6)

Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 8 of 60



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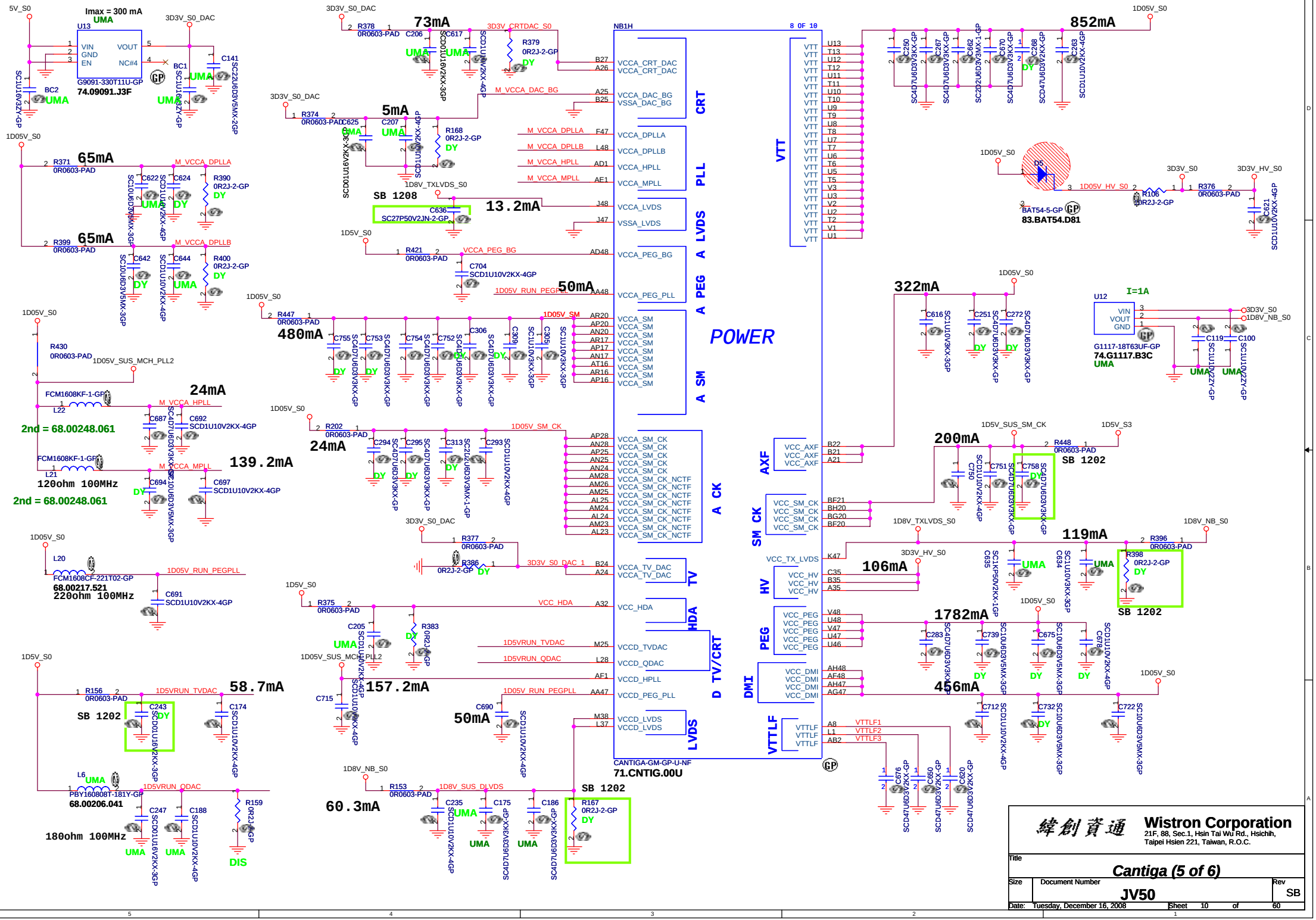
Title: Cantiga (4 of 6)

Size: | Document Number: JV50 | Rev: SB

Date: Tuesday, December 16, 2008 | Sheet 9 of 60


POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
UMA
G9091-330T11U-GP
74.09091.J3F
73mA
5mA
65mA
65mA
SB 1208
13.2mA
50mA
480mA
24mA
139.2mA
2nd = 68.00248.061
120ohm 100MHz
2nd = 68.00248.061
68.00217.521
220ohm 100MHz
157.2mA
58.7mA
SB 1202
68.00206.041
180ohm 100MHz
50mA
60.3mA
SB 1202
852mA
322mA
I=1A
G1117-18T63UF-GP
74.G1117.B3C
200mA
SB 1202
119mA
SB 1202
106mA
1782mA
456mA
BAT54-5-GP
83.BAT54.D81
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
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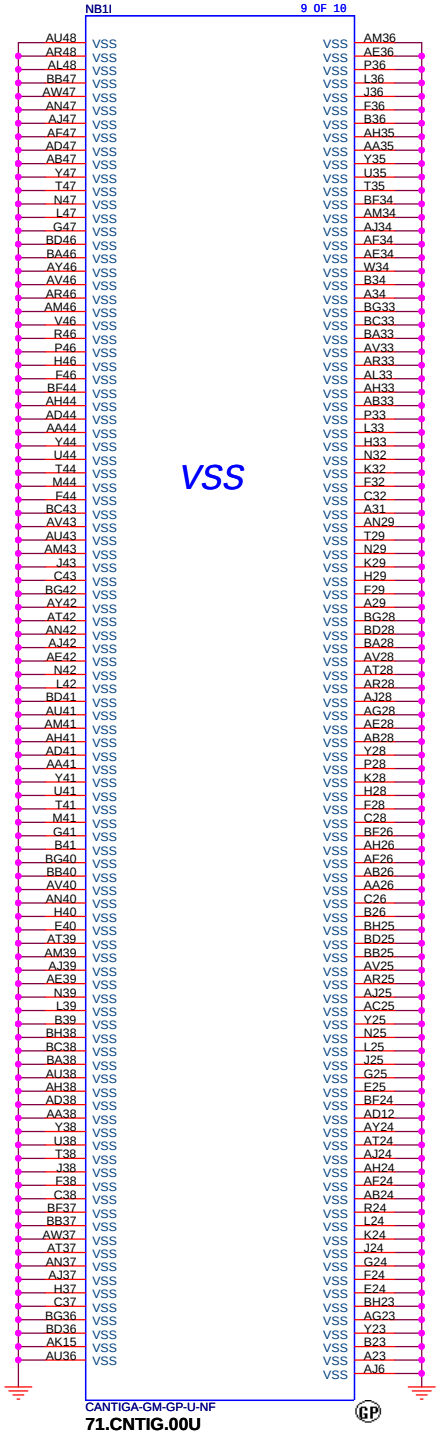
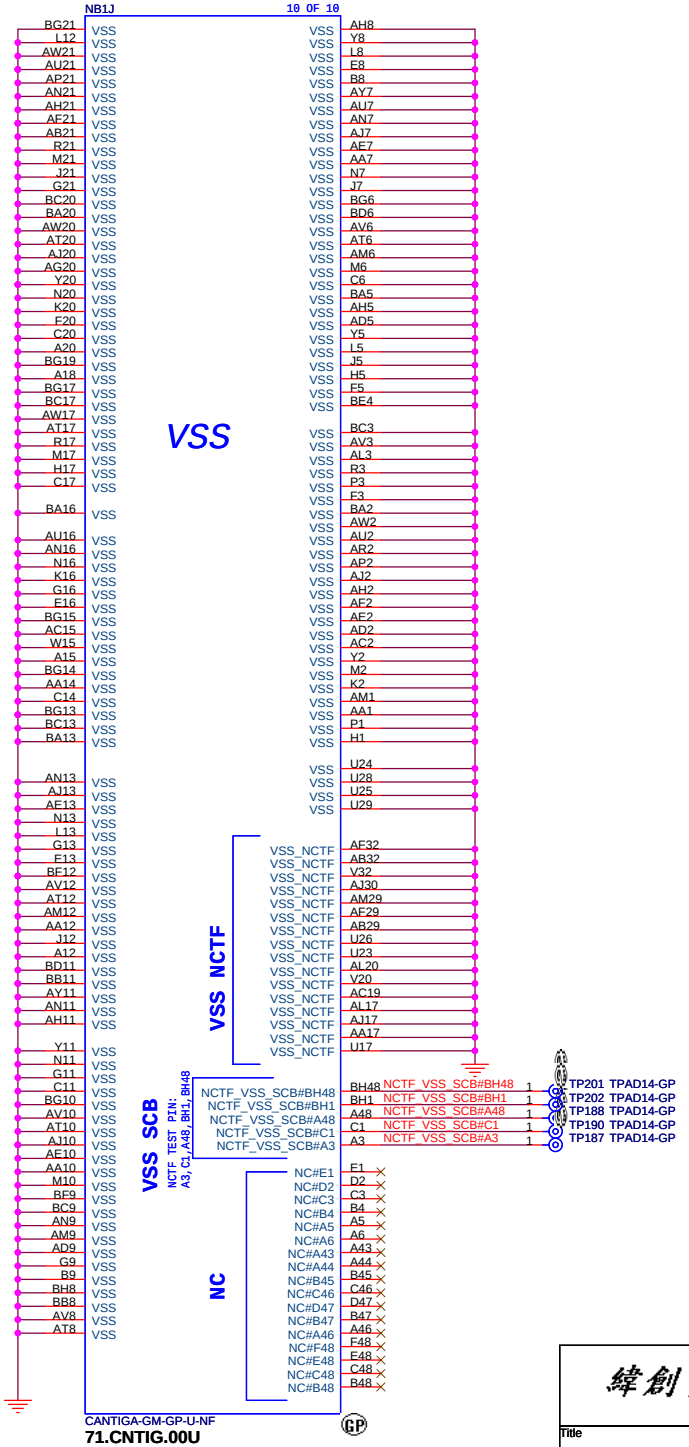
Cantiga (5 of 6)
JV50
Rev SB
Tuesday, December 16, 2008
Sheet 10 of 60





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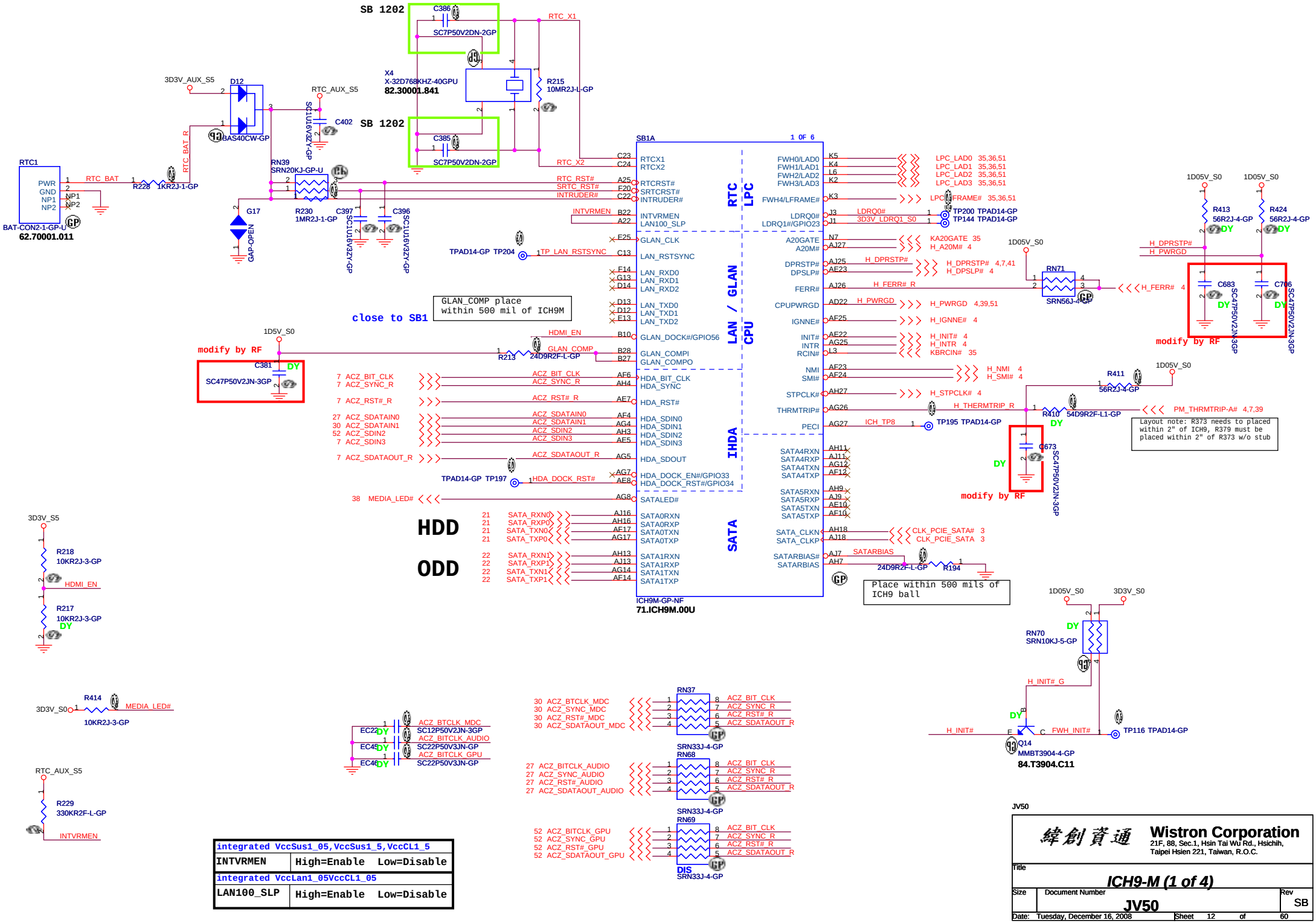
Title: ***Cantiga (6 of 6)***

Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 11 of 60


SB 1202
C386
SC7P50V2DN-2GP
RTC_X1
X4
X-32D768KHZ-40GPU
82.30001.841
R215
10MR2J-L-GP
SB 1202
C385
SC7P50V2DN-2GP
RTC_X2
3D3V_AUX_S5
D12
BAS40CW-GP
RTC_AUX_S5
SC1U16V2ZX-GP
C402
RTC_BAT_R
RTC1
PWR
GND
NP1
NP2
RTC_BAT
R228
1KR2J-1-GP
BAT-CON2-1-GP-U
62.70001.011
RN39
SRN20KJ-GP-U
G17
GAP-OPEN
R230
1MR2J-1-GP
C397
SC1U16V3ZY-GP
C396
SC1U16V3ZY-GP
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
GLAN
LAN / CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
GLAN_COMP place within 500 mil of ICH9M
close to SB1
HDMI_EN
GLAN_COMP
R213
24D9R2F-L-GP
1D05V_S0
modify by RF
C381
SC47P50V2JN-3GP
DY
TPAD14-GP TP204
TP_LAN_RSTSYNC
TPAD14-GP TP197
HDA_DOCK_RST#
HDD
ODD
LPC_LAD0 35,36,51
LPC_LAD1 35,36,51
LPC_LAD2 35,36,51
LPC_LAD3 35,36,51
LPC_FRAME# 35,36,51
LDRQ0#
3D3V_LDRQ1_S0
TP200 TPAD14-GP
TP144 TPAD14-GP
KA20GATE 35
H_A20M# 4
H_DPRSTP# 4,7,41
H_DPSLP# 4
H_FERR# R
H_PWRGD 4,39,51
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 35
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
TP195 TPAD14-GP
ICH_TP8
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
24D9R2F-L-GP
R194
Place within 500 mils of ICH9 ball
RN71
SRN56J-4-GP
H_FERR# 4
R413
56R2J-4-GP
R424
56R2J-4-GP
C683
C706
SC47P50V2JN-3GP
modify by RF
R411
56R2J-4-GP
R410
54D9R2F-L1-GP
PM_THRMTRIP-A# 4,7,39
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
C673
SC47P50V2JN-3GP
modify by RF
RN70
SRN10KJ-5-GP
H_INIT# G
H_INIT#
FWH_INIT#
TP116 TPAD14-GP
Q14
MMBT3904-4-GP
84.T3904.C11
3D3V_S5
R218
10KR2J-3-GP
HDMI_EN
R217
10KR2J-3-GP
R414
10KR2J-3-GP
MEDIA_LED#
RTC_AUX_S5
R229
330KR2F-L-GP
INTVRMEN
EC22
EC45
EC46
SC12P50V2JN-3GP
SC22P50V3JN-GP
SC22P50V3JN-GP
ACZ_BTCLK_MDC
ACZ_BITCLK_AUDIO
ACZ_BITCLK_GPU
RN37
SRN33J-4-GP
RN68
SRN33J-4-GP
RN69
SRN33J-4-GP
DIS
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
JV50
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
JV50
Rev
SB
Date: Tuesday, December 16, 2008
Sheet 12 of 60

PCI_GNT#0 and SPI_CS1# have weak internal Pull up

SB1B 2 OF 6

PCI

Interrupt I/F

ICH9M-GP-NF
71.ICH9M.00U

SB1C 3 OF 6

SMB

SYS GPIO

Power MGT

GPIO

Controller Link

MISC

ICH9M-GP-NF
71.ICH9M.00U

GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

SB1D 4 OF 6

PCI-Express

Direct Media Interface

SPI

USB

ICH9M-GP-NF
71.ICH9M.00U

LAN

MINICARD1

MINICARD2

NEW CARD

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1
4	CCD
5	New Card
6	Finger Print
7	Blue Tooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

These R need close SB within 600 mils

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

JV50

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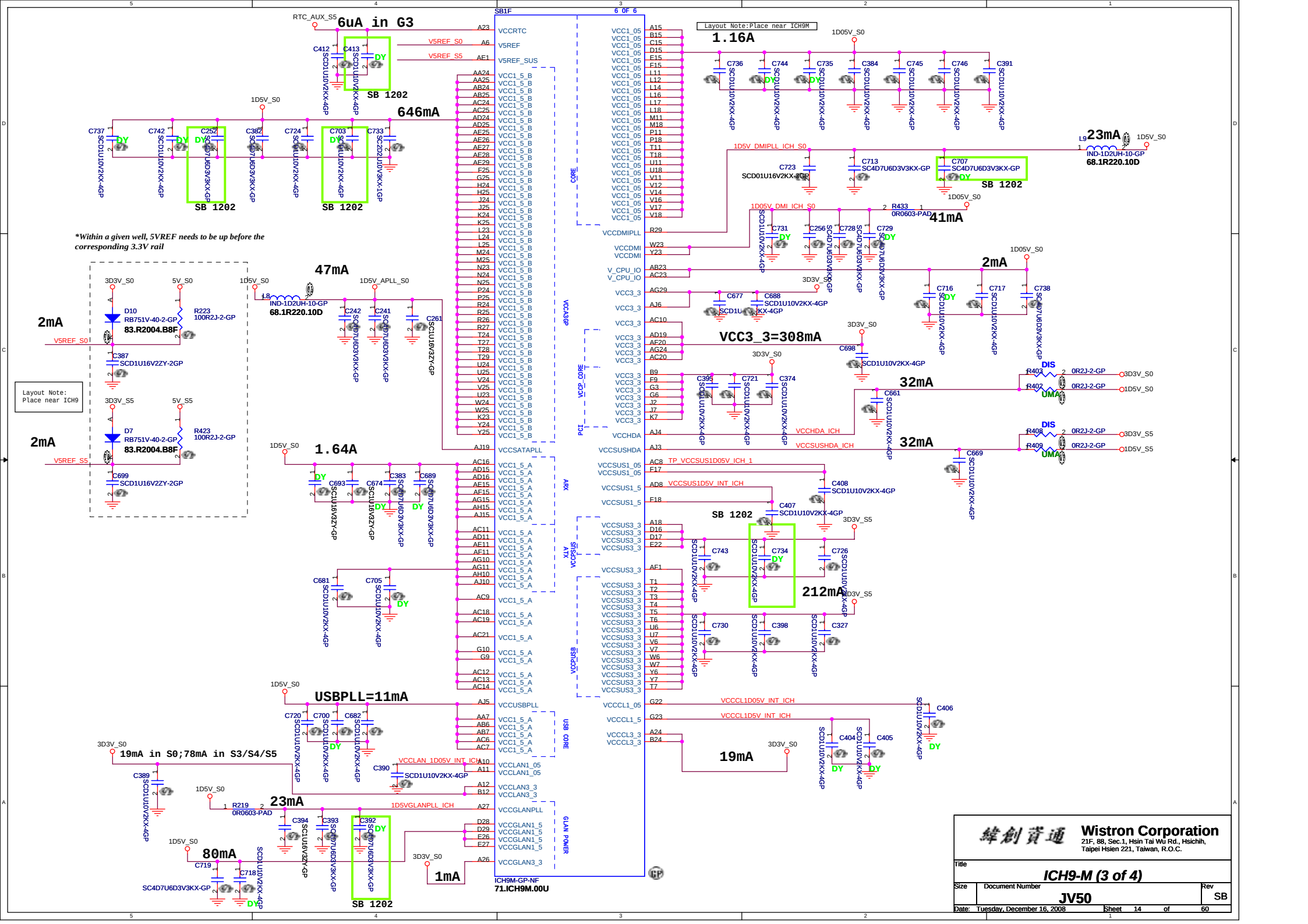
Title: ICH9-M (2 of 4)

Size: | Document Number: JV50 | Rev: SB

Date: Tuesday, December 16, 2008 Sheet 13 of 60



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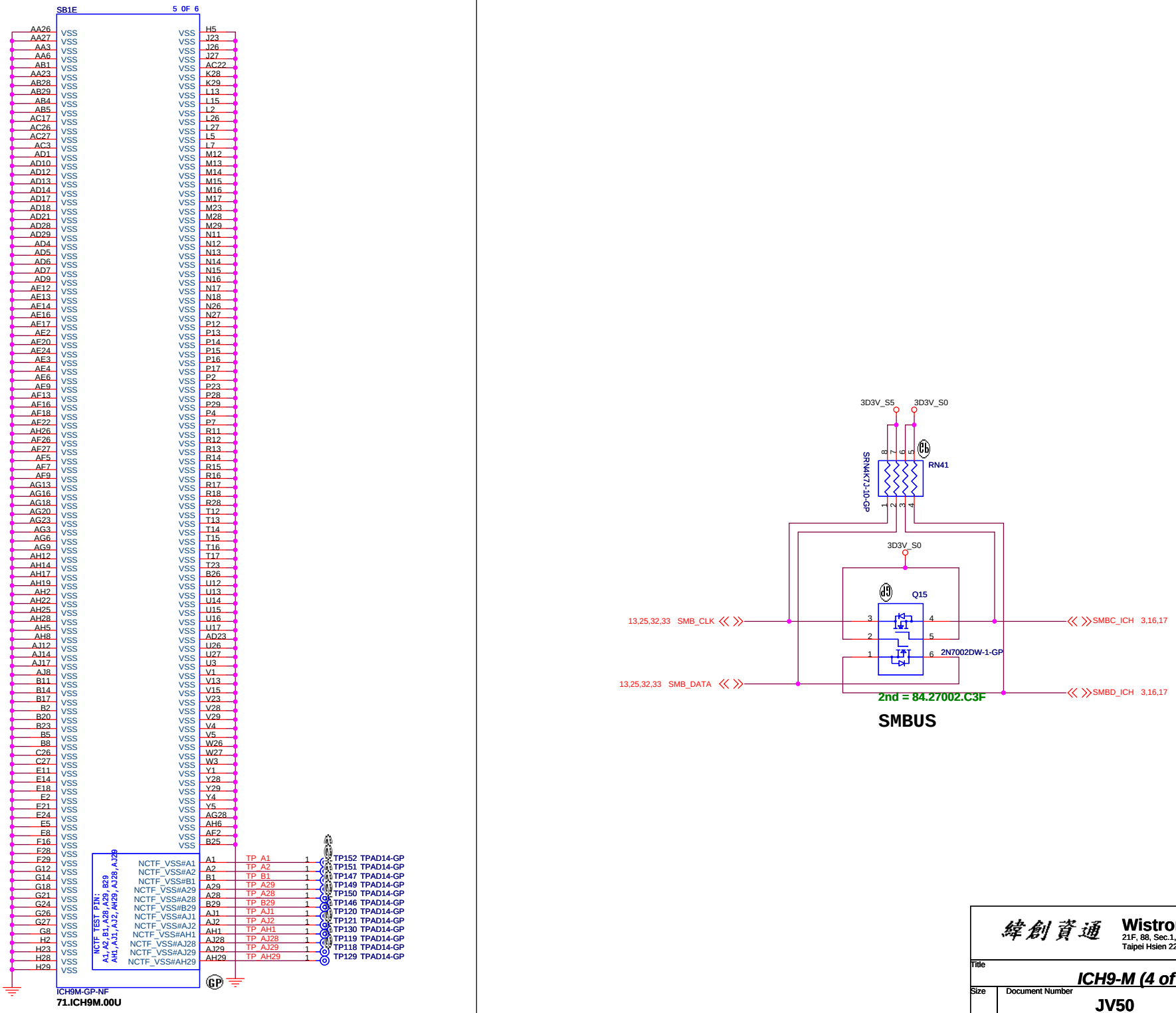
Title: ICH9-M (3 of 4)

Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 14 of 60



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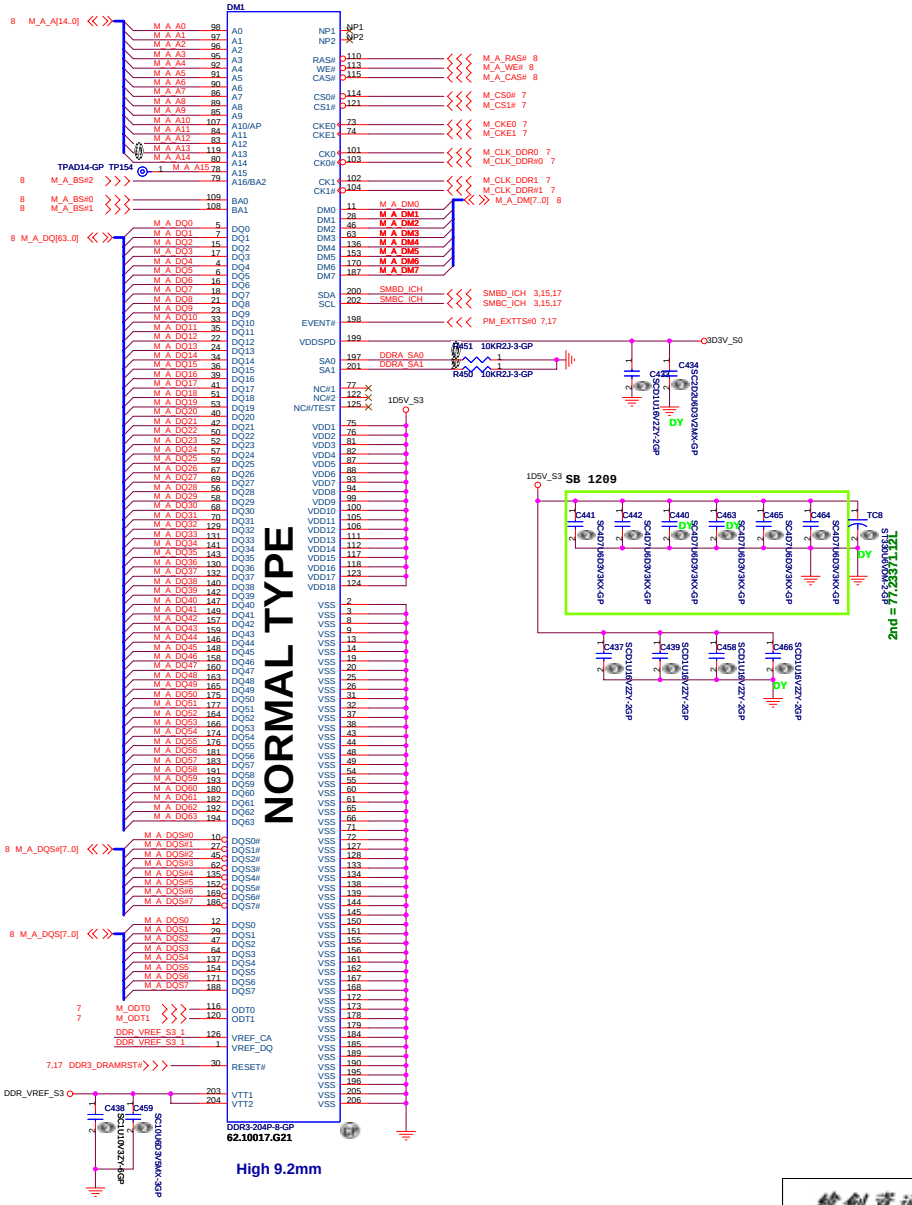
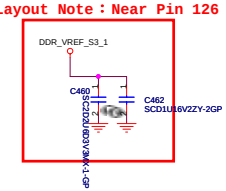
Title	*ICH9-M (4 of 4)*	
Size	Document Number JV50	Rev SB
Date: Tuesday, December 16, 2008	Sheet 15 of 60	

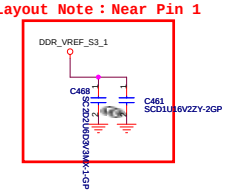
DDR3 SOCKET_1



Layout Note : Near Pin 126

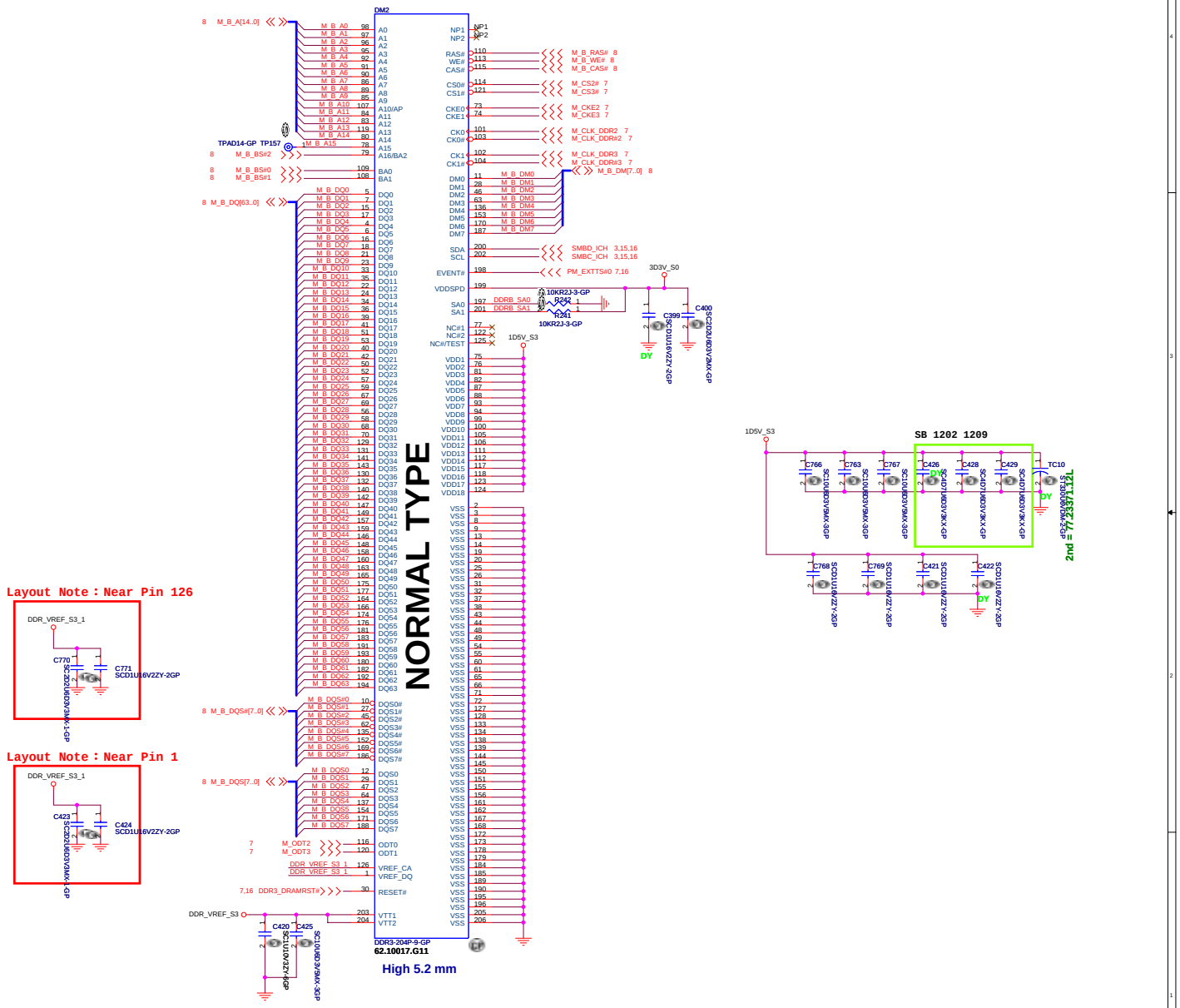


Layout Note : Near Pin 1



蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR3 Socket***	
Size	Document Number **JV50**	Rev SB
Date: Tuesday, December 16, 2008	Sheet 16 of 60	

DDR3 SOCKET_2



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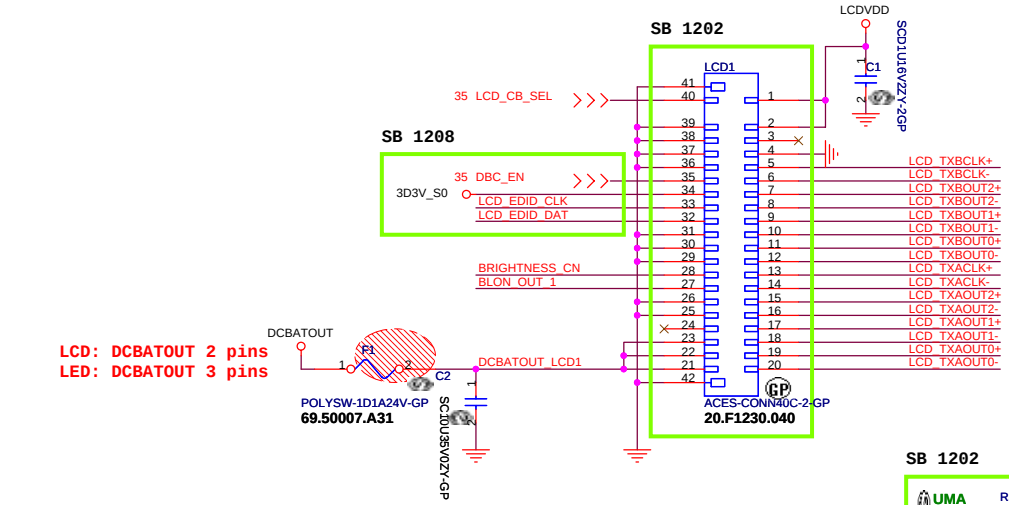
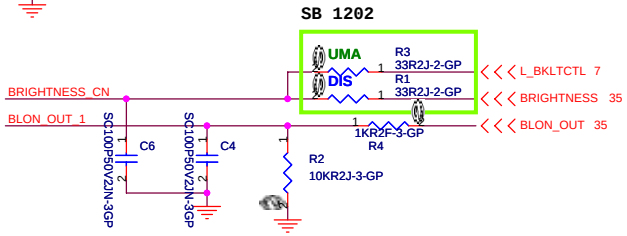
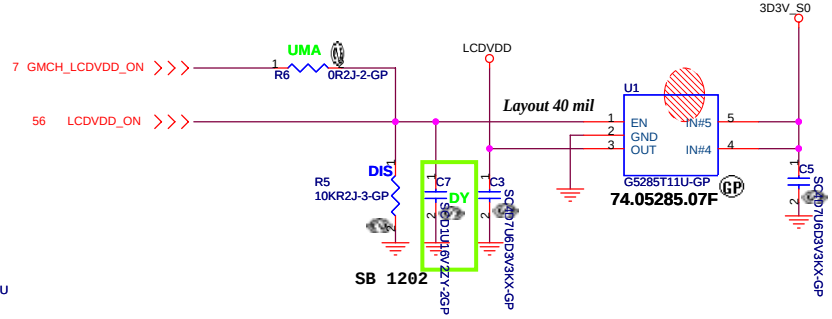
Title		
DDR3 Socket2		
Size	Document Number	Rev
	JV50	SB
Date: Tuesday, December 16, 2008	Sheet 17 of 60	

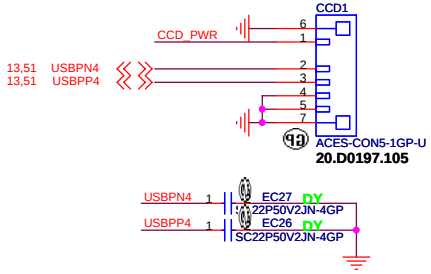
LCD/INVERTER/CCD CONN

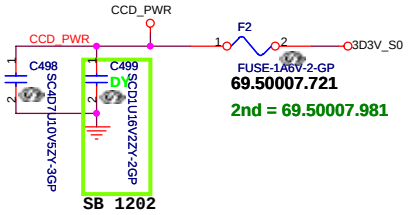




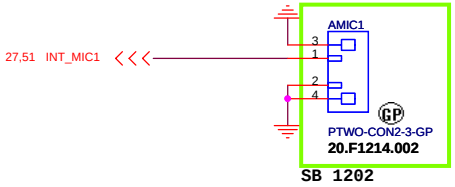


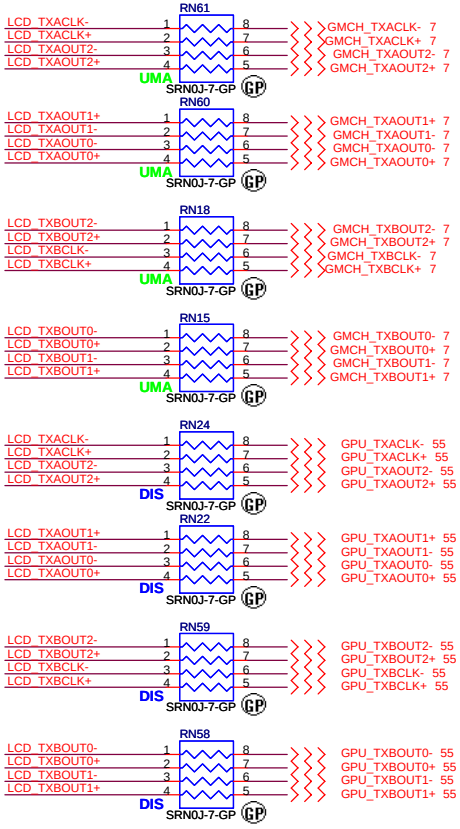
CCD

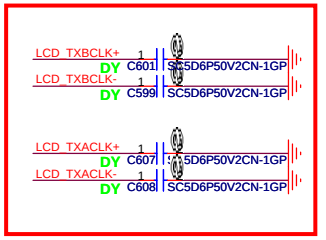




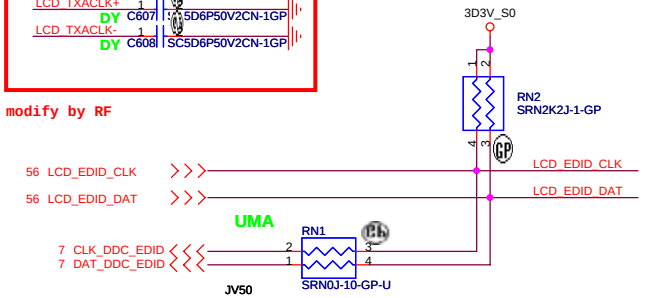
Internal Mic







modify by RF



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: JV50	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 18 of 60	

Layout Note:
Place these resistors close to the CRT-out connector

UMA RN26 SRN0J-7-GP

Close to MXM card

GMCH_BLUE 7
GMCH_GREEN 7
GMCH_RED 7

Ferrite bead impedance: 10 ohm@100MHz

54 CRT_RED — L5 FCB1608CF-GP 68.00230.021 — CRT_R
54 CRT_GREEN — L4 FCB1608CF-GP 68.00230.021 — CRT_G
54 CRT_BLUE — L3 FCB1608CF-GP 68.00230.021 — CRT_B

RN25 SRN150F-1-GP

C158 SC3P50V2CN-1-GP DY
C137 SC3P50V2CN-1-GP DY
C109 SC3P50V2CN-1-GP DY
C165 SC6D8P50V2DN-GP
C151 SC6D8P50V2DN-GP
C108 SC6D8P50V2DN-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_S0

C107 SCD1U16V2ZY-2GP

SB

DIS
54 CRT_HSYNC
54 CRT_VSYNC
RN63 SRN0J-10-GP-U
HSYNC_1
VSYNC_1

U18A TSAHCT125PW-GP
U18B TSAHCT125PW-GP

CRT_HSYNC1
CRT_VSYNC1

UMA
7 GMCH_HSYNC
7 GMCH_VSYNC
RN62 SRN0J-10-GP-U

C632 SC47P50V2JN-3GP DY
C633 SC47P50V2JN-3GP DY

U18C TSAHCT125PW-GP
U18D TSAHCT125PW-GP

DDC_CLK & DATA level shift

5V_CRT_S0
F3 FUSE-1D1A6V-4GP-U 69.50007.691
5V_S0
3D3V_S0
D4 CH551H-30PT-GP 83.R5003.C8F 500mA
5V_CRT_DDC
RN20 SRN10KJ-6-GP
CRT_IN# R

RN66 SRN2K2J-1-GP

DIS
54 CRT_DDCDATA
54 CRT_DDCCLK
RN57 SRN0J-10-GP-U
DAT_DDC1_5_Q

UMA
7 GMCH_DDCDATA
7 GMCH_DDCCLK
RN53 SRN0J-10-GP-U
CLK_DDC1_5_Q

U42 2N7002EDW-GP 84.27002.F3F

DAT_DDC1_5
CLK_DDC1_5

CRT I/F & CONNECTOR

D24 D23 D22 BAV99PT-GP-U DY

CRT_R 3
CRT_G 3
CRT_B 3

SC100P50V2JN-3GP C128 DY
C115
C105
C93 DY
SC18P50V2JN-1-GP
SC18P50V2JN-1-GP
SC100P50V2JN-3GP

DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5

CRT1
CRT_R
CRT_G
CRT_B
CRT_IN# R
VIDEO-15-42-GP-U
20.20378.015

5V_CRT_S0
C602 SCD01U16V2KX-3GP

35 CRT_DEC# — R93 470R2J-2-GP — CRT_IN# R
C98 SC100P50V2JN-3GP

D21 BAV99PT-GP-U DY
CRT_IN# R 3

6 1 7 2 8 3 9 4 10 5

JV50

緯創資通 **Wistron Corporation**
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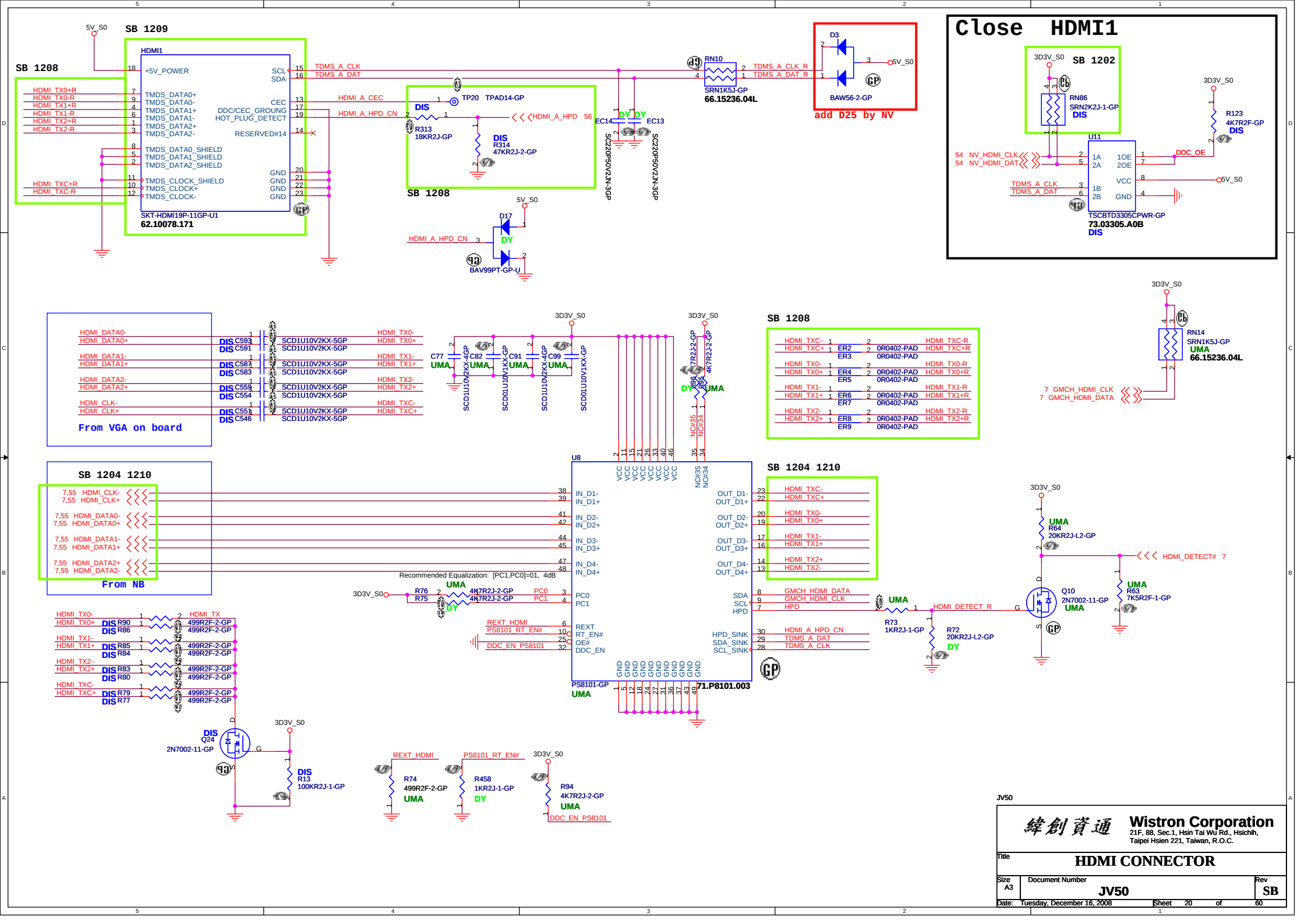
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**
Size: Document Number: **JV50** Rev: SB
Date: Tuesday, December 16, 2008 Sheet 19 of 60


Close HDMI1
SB 1208
SB 1209
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_CEC
HDMI_A_HPD_CN
HDMI_A_HPD
TP20 TPAD14-GP
R313 18KR2J-GP
R314 47KR2J-2-GP
RN10
SRN1K5J-GP
66.15236.04L
D3
BAW56-2-GP
add D25 by NV
D17
BAV99PT-GP-U
SB 1202
RN86 SRN2K2J-1-GP
R123 4K7R2F-GP
U11
TSCBTD3305CPWR-GP
73.03305.A0B
From VGA on board
From NB
SB 1204 1210
SB 1208
RN14 SRN1K5J-GP
66.15236.04L
U8
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
Q24 2N7002-11-GP
Q10 2N7002-11-GP
R74 499R2F-2-GP
R458 1KR2J-1-GP
R94 4K7R2J-2-GP
R13 100KR2J-1-GP
R64 20KR2J-L2-GP
R63 7K5R2F-1-GP
R72 20KR2J-L2-GP
R73 1KR2J-1-GP
Wistron Corporation
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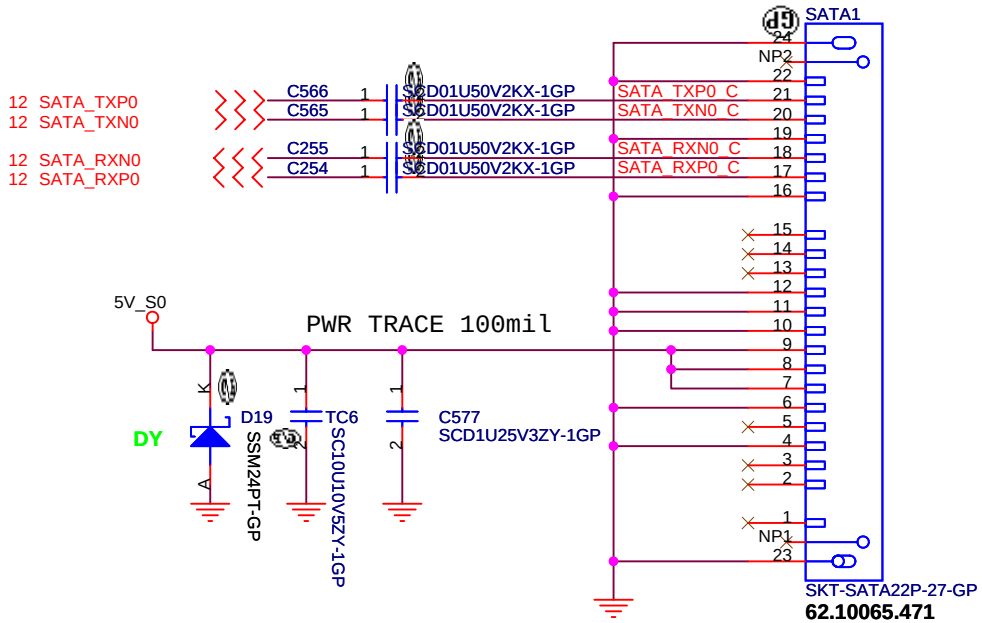
HDMI CONNECTOR
JV50
Tuesday, December 16, 2008

SATA Connector



JV50

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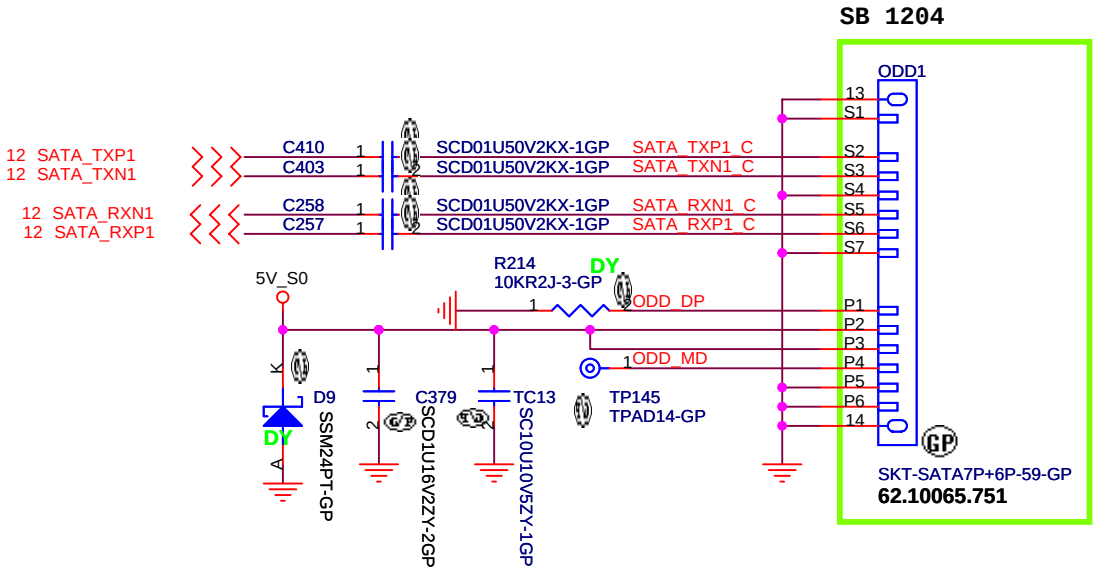
Title	***HDD CONN***	
Size	Document Number **JV50**	Rev SB
Date: Tuesday, December 16, 2008	Sheet 21 of 60	

ODD Connector



JV50

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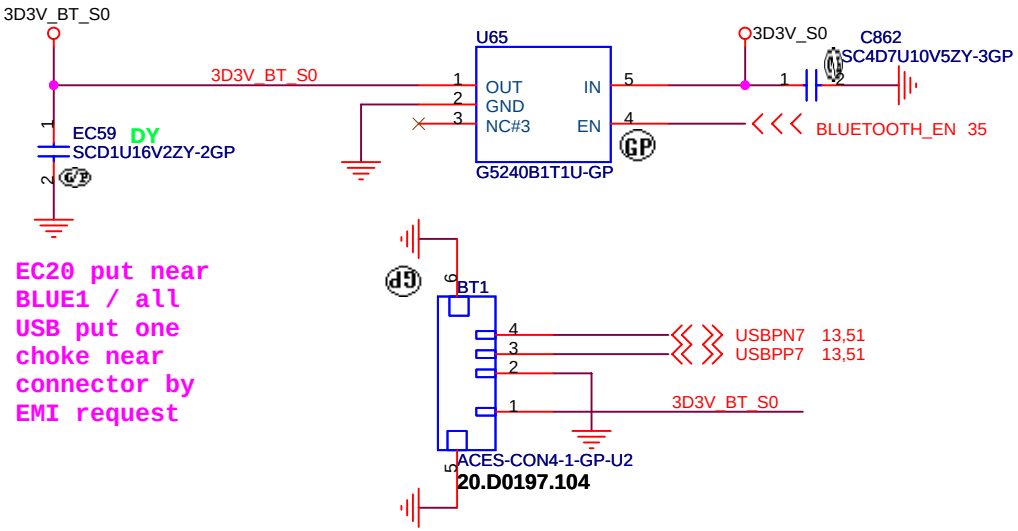
Title	***ODD***	
Size	Document Number **JV50**	Rev SB
Date: Tuesday, December 16, 2008	Sheet 22 of 60	

BLUETOOTH MODULE



JV50

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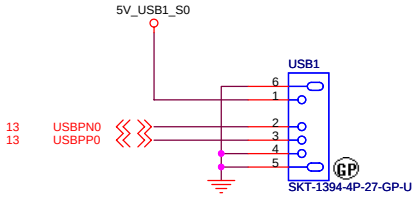
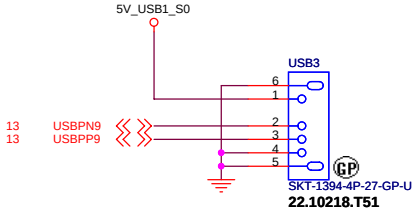
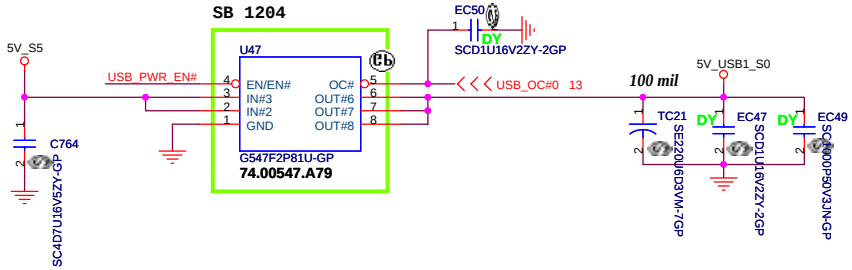
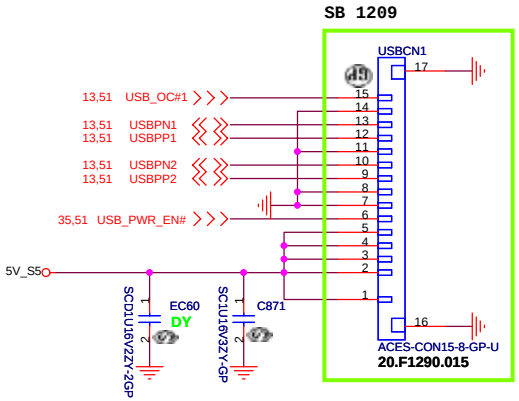
Title	***BLUETOOTH***
Size	Document Number: **JV50** — Rev: SB
Date: Tuesday, December 16, 2008	Sheet 23 of 60









JV50

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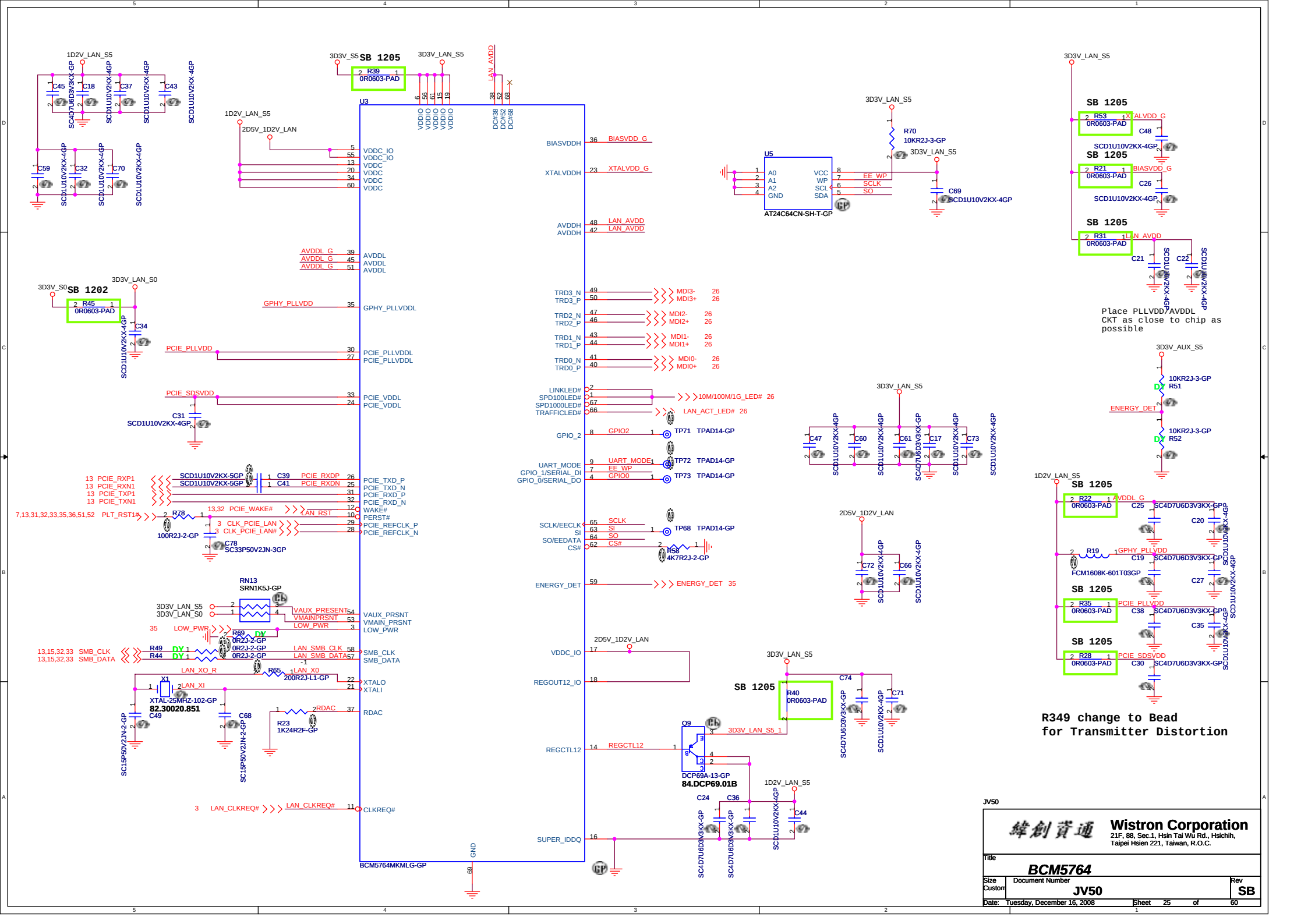
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB CONN*

Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 24 of 60

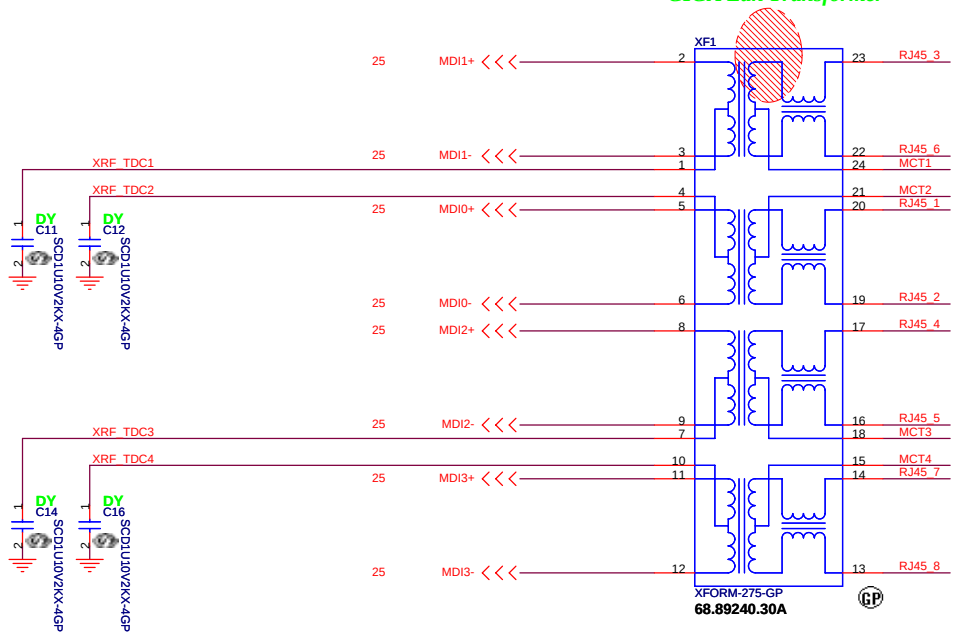

SB 1205
R39 0R0603-PAD
SB 1202
R45 0R0603-PAD
U3
BCM5764MKMLG-GP
U5
AT24C64CN-SH-T-GP
R70 10KR2J-3-GP
SB 1205
R53 0R0603-PAD
R21 0R0603-PAD
R31 0R0603-PAD
Place PLLVDD/AVDDL CKT as close to chip as possible
SB 1205
R22 0R0603-PAD
R19 FCM1608K-601T03GP
R35 0R0603-PAD
R28 0R0603-PAD
SB 1205
R40 0R0603-PAD
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
JV50
Tuesday, December 16, 2008
Sheet 25 of 60

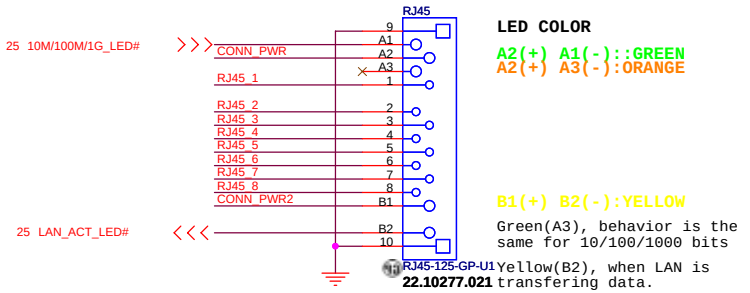
LAN Connector

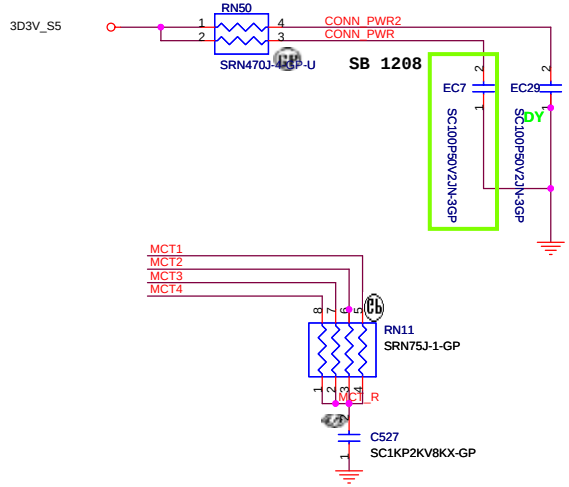
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

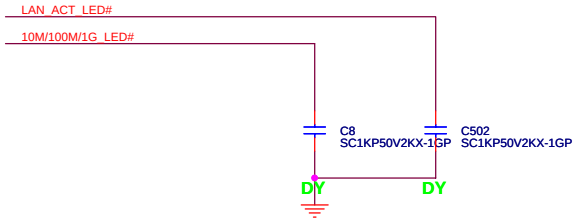
LAN Connector

GIGA Lan Transformer









JV50

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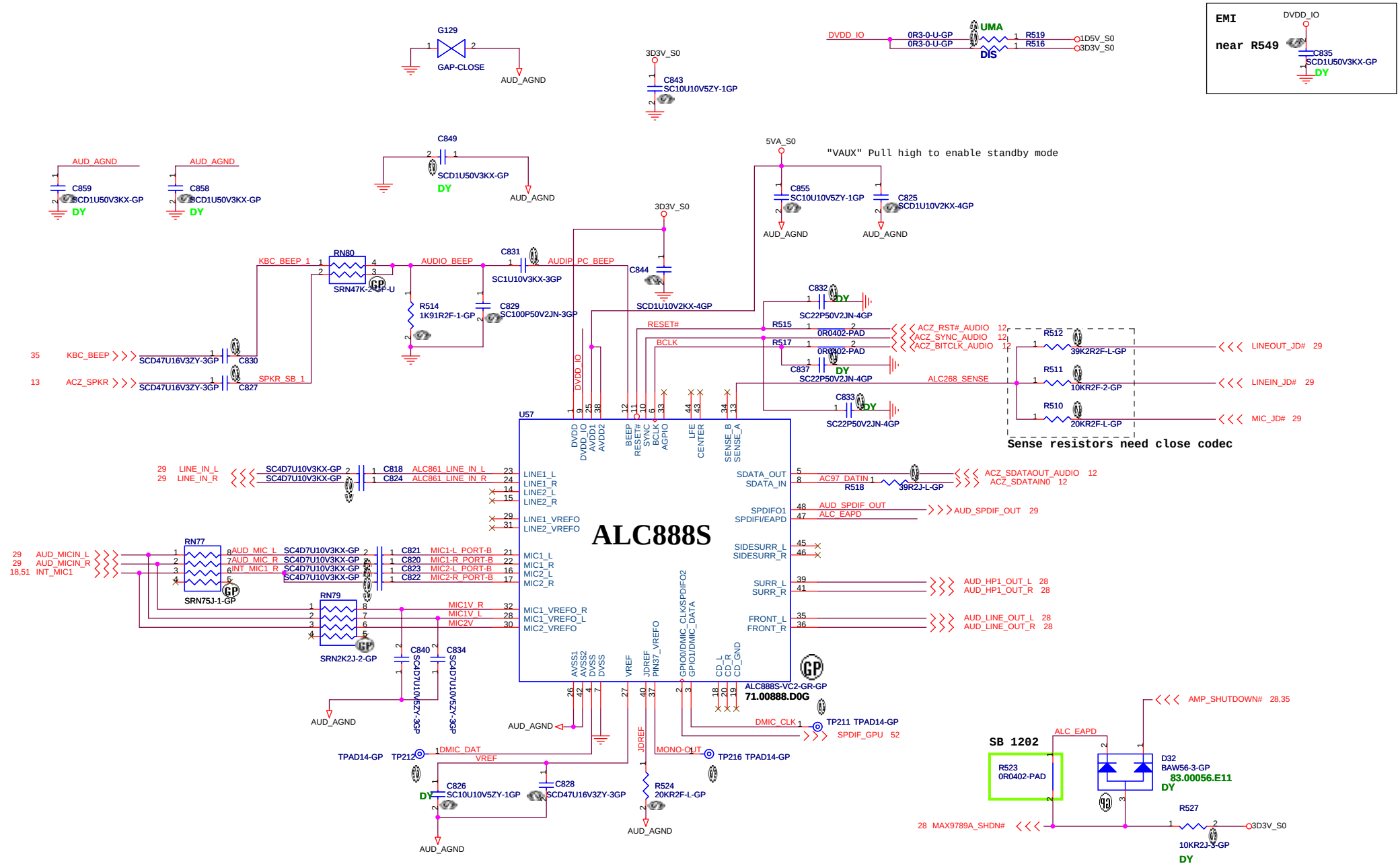
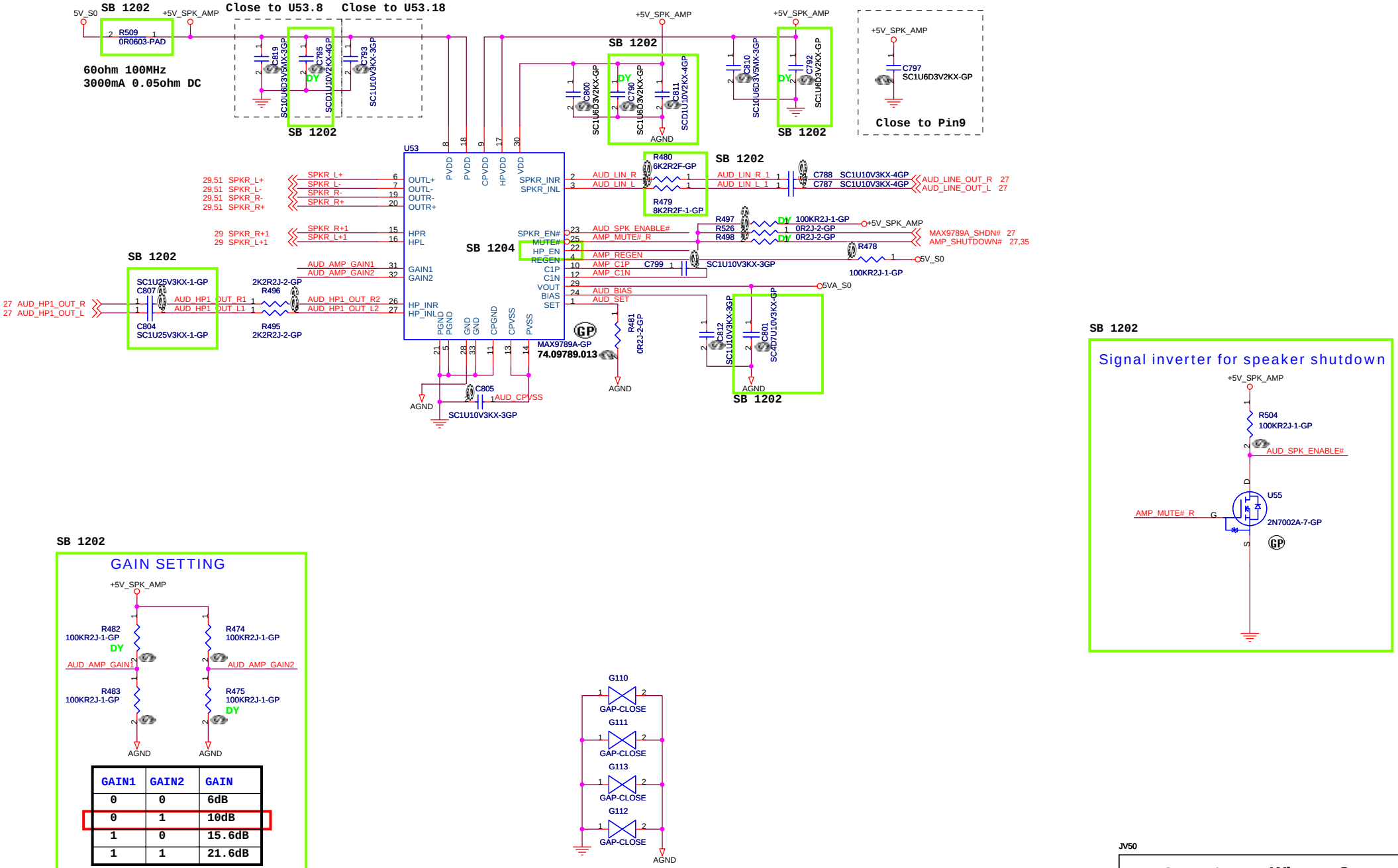
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number JV50	Rev SB
Date: Tuesday, December 16, 2008	Sheet 26 of 60	



JV50

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Azalia codec ALC888***
Size A3	Document Number **JV50** Rev **SB**
Date: Tuesday, December 16, 2008	Sheet 27 of 60



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

JV50

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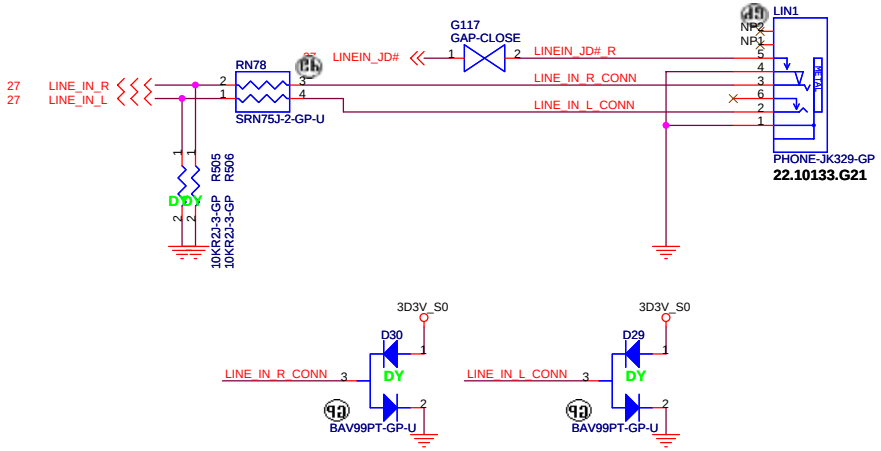
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP*

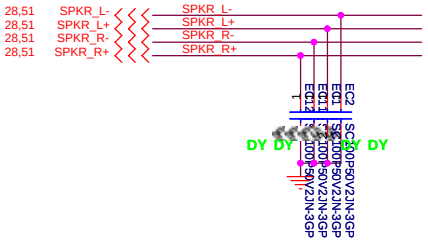
Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 28 of 60

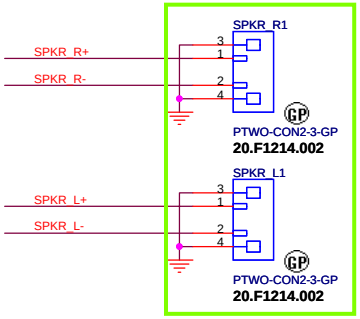
LINE IN



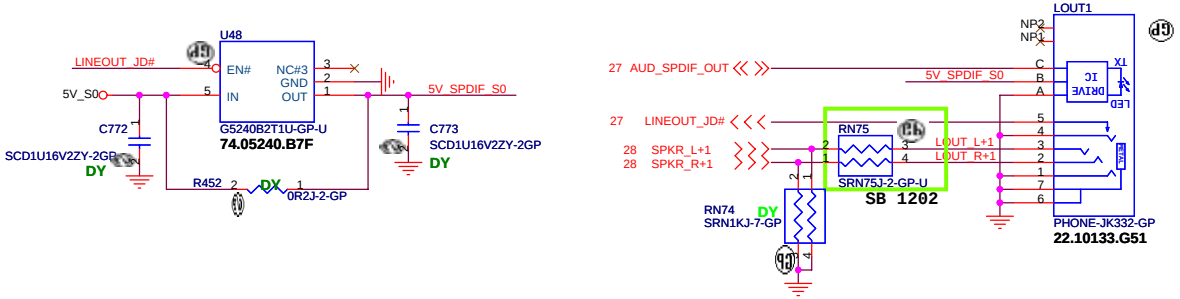
Internal Speaker



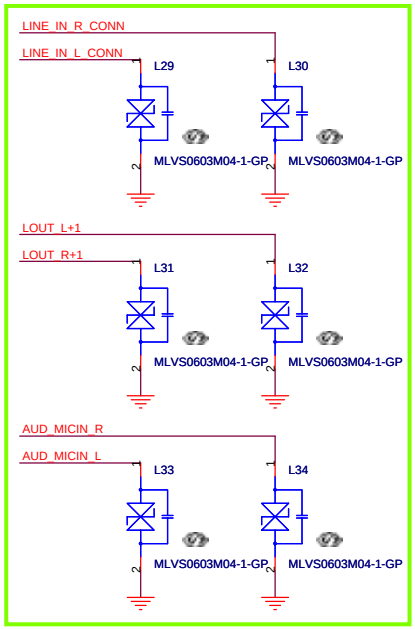
SB 1202



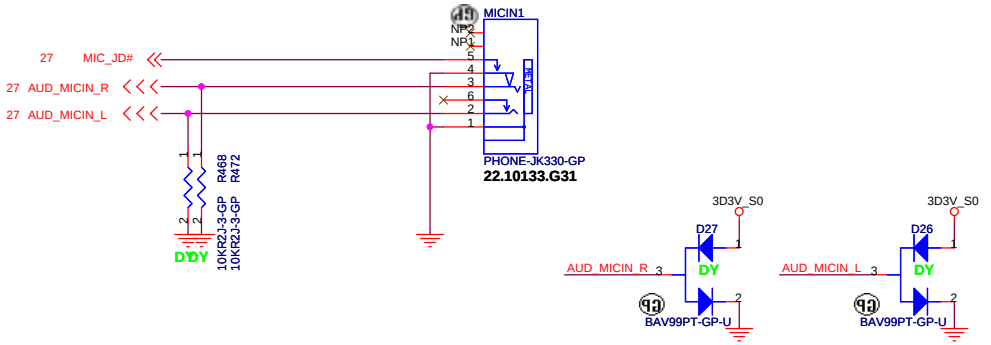
LINE OUT



SB 1202



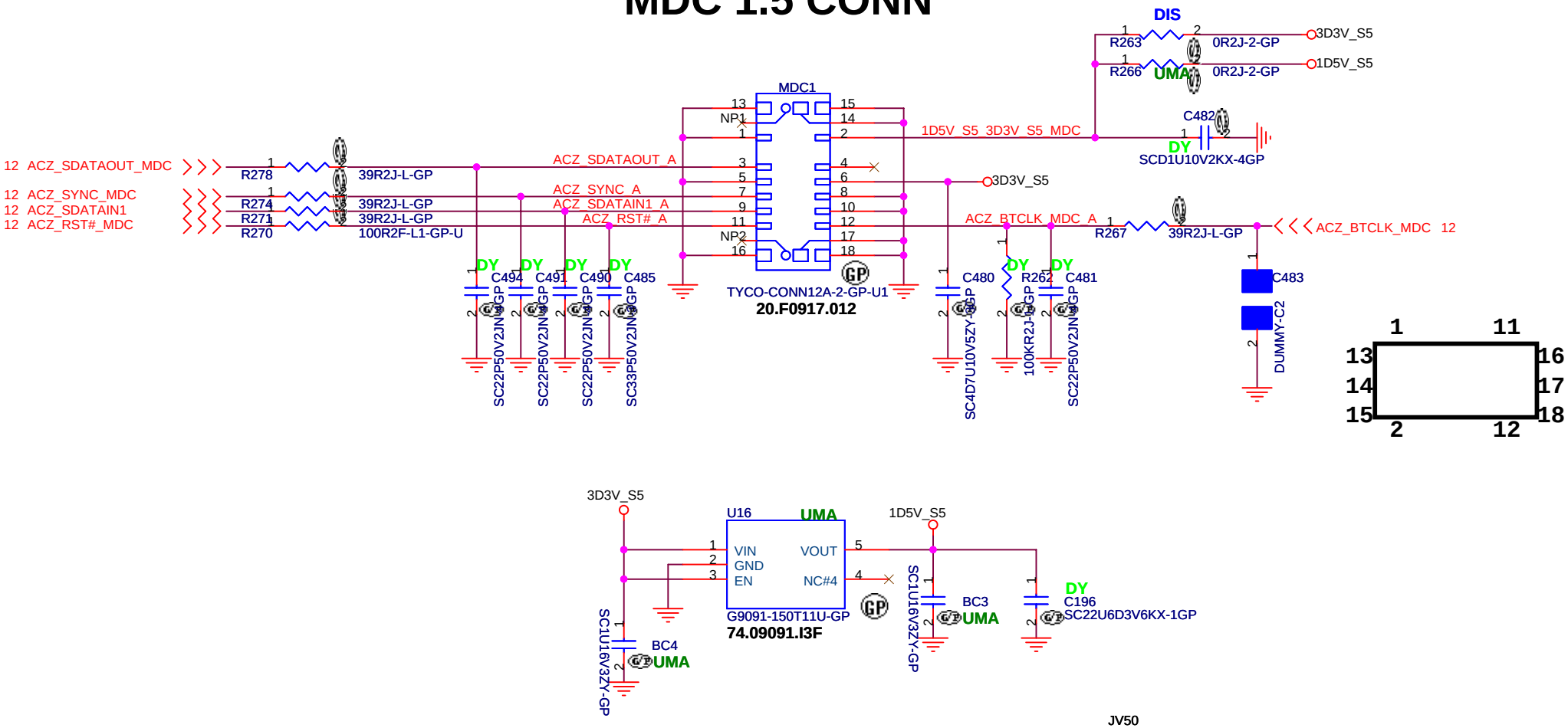
MIC IN



JV50

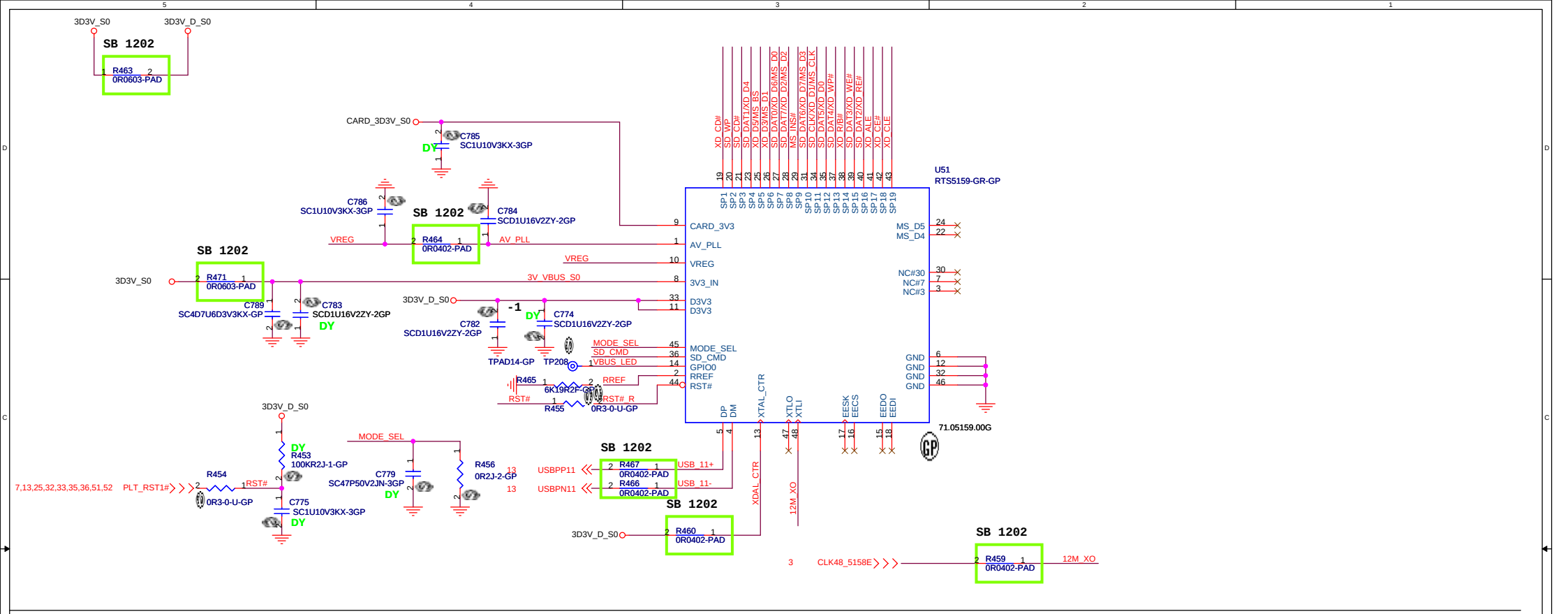
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO jack*	
Size	Document Number JV50	Rev SB
Date: Tuesday, December 16, 2008	Sheet 29 of 60	

MDC 1.5 CONN

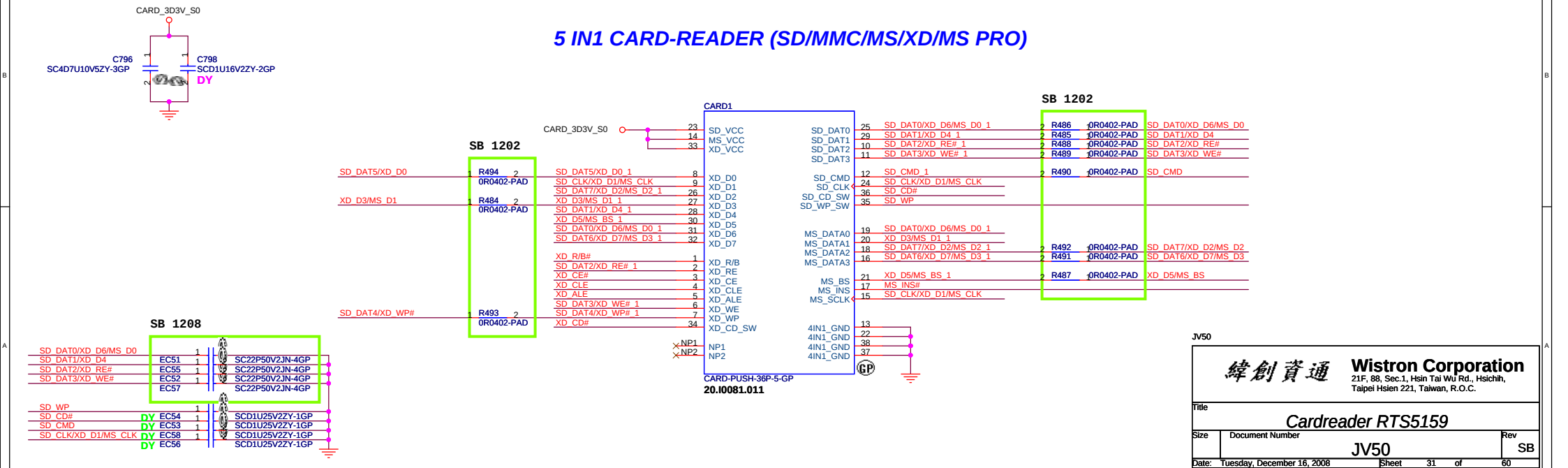


JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
Size	Document Number **JV50**	Rev SB
Date: Tuesday, December 16, 2008	Sheet 30 of 60	

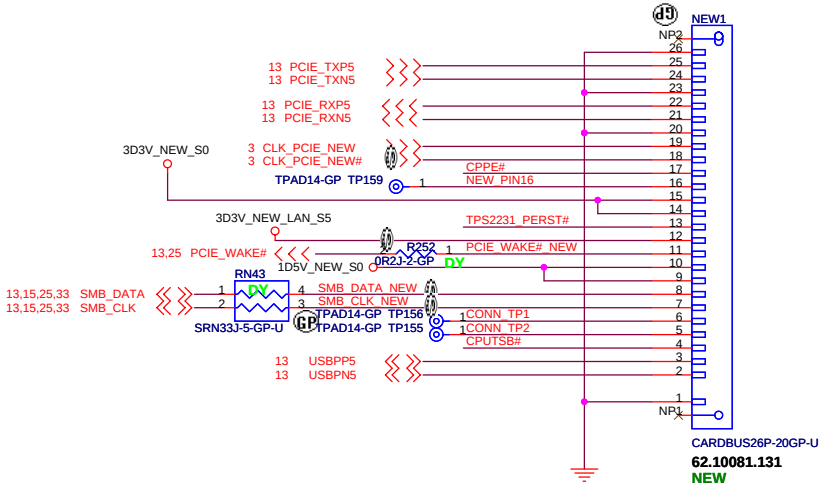


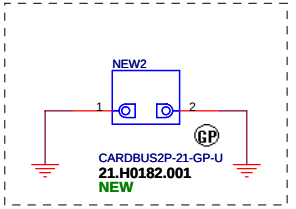
5 IN1 CARD-READER (SD/MMC/MS/XD/MS PRO)

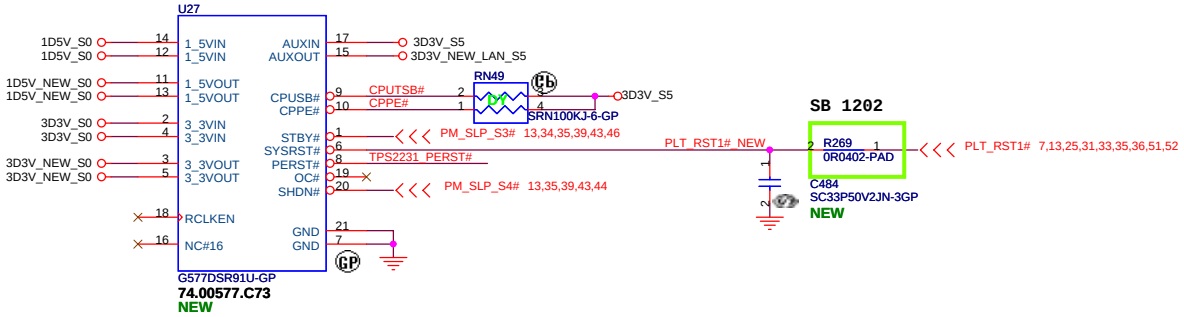


JV50

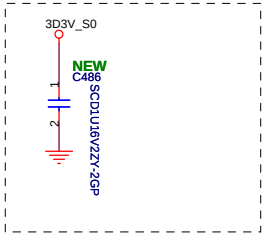
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Cardreader RTS5159*	
Size	Document Number: JV50	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 31 of 60	



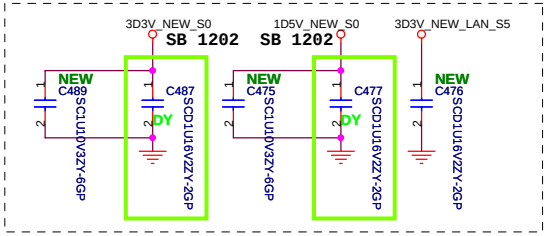




Place them Near to Chip



Place them Near to Connector



JV50

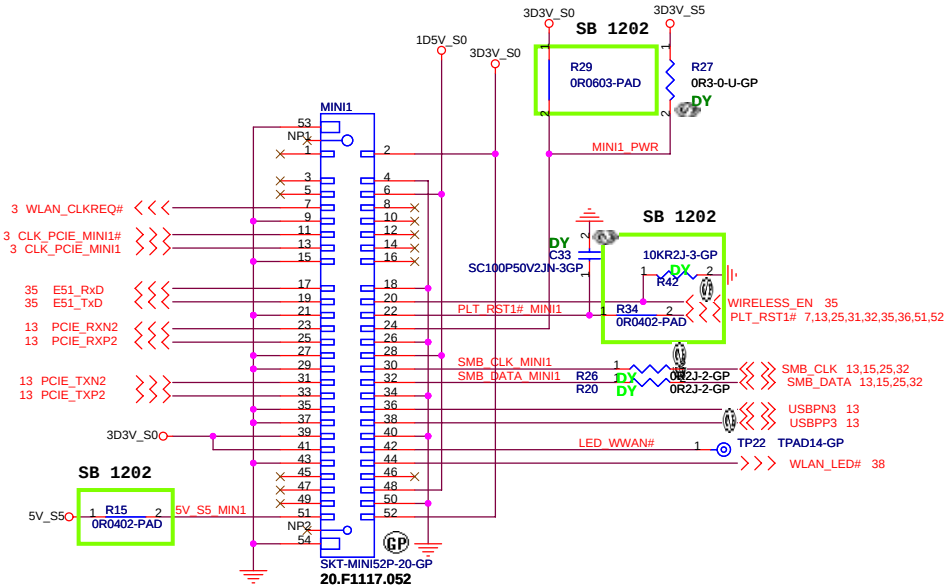
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

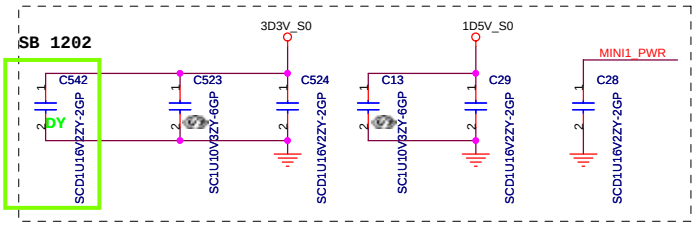
Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 32 of 60

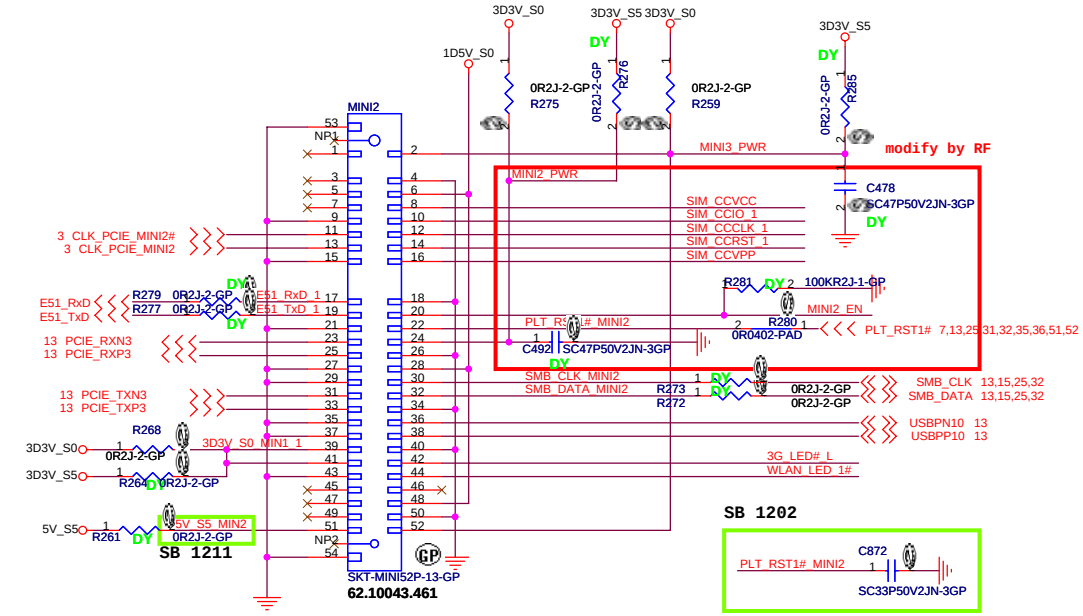
Mini Card Connector(WLAN)
Support debug-card

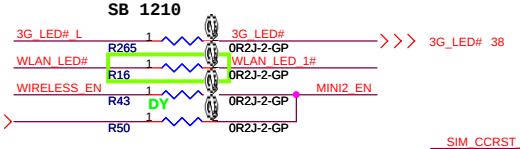


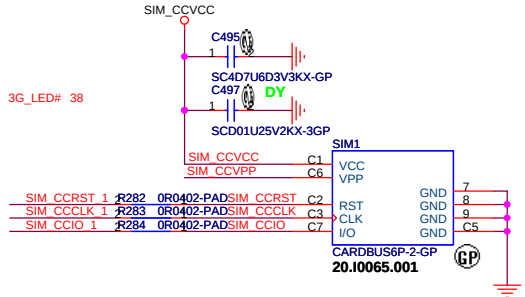
Place near MINI1



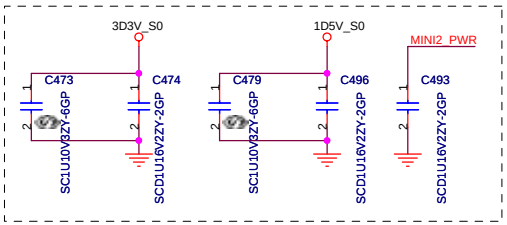
Mini Card Connector(Robson2 and 3G)







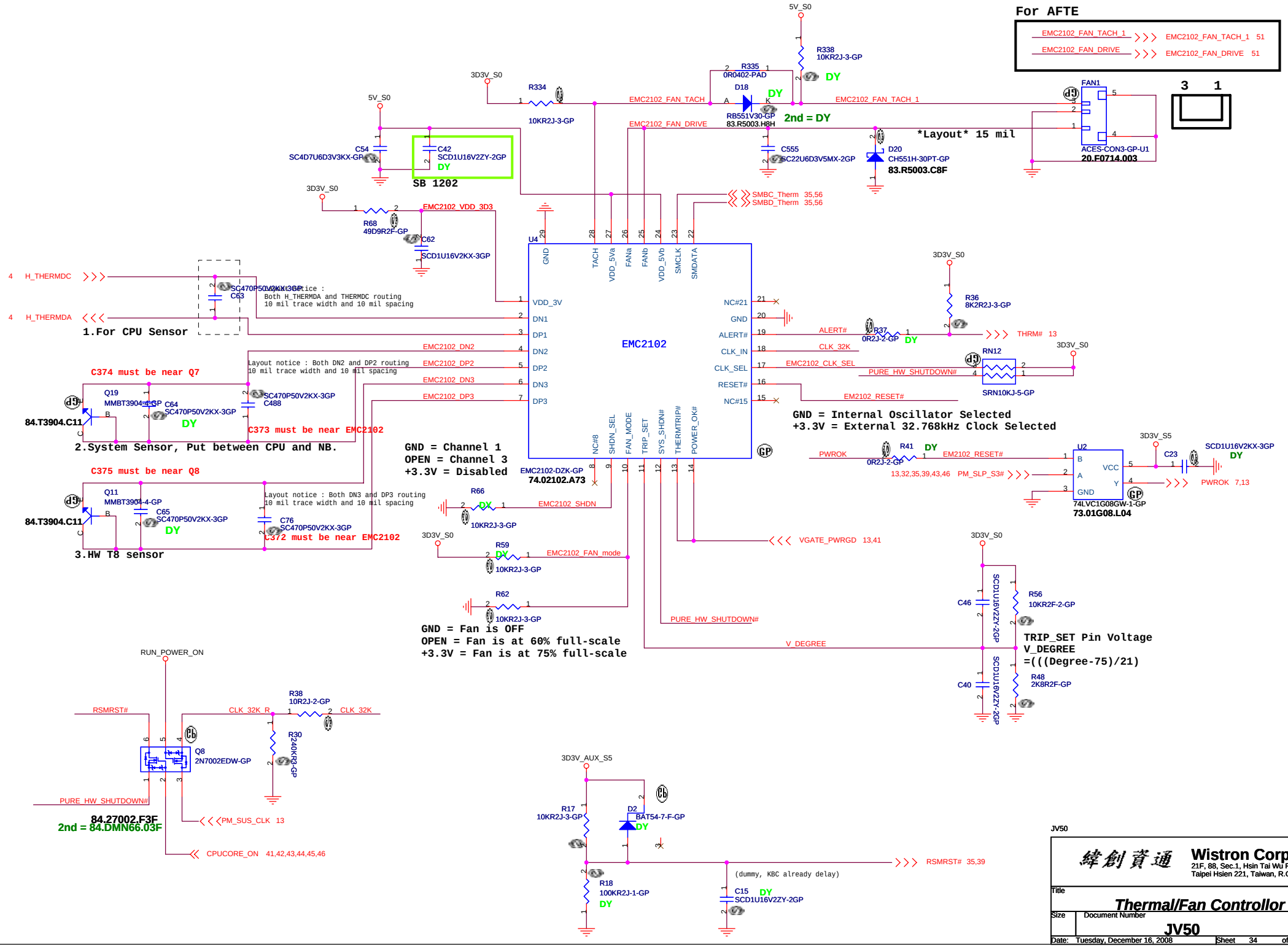
Place near MINIC2



JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MINI CARD		
Size: A3	Document Number: JV50	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 33 of 60	



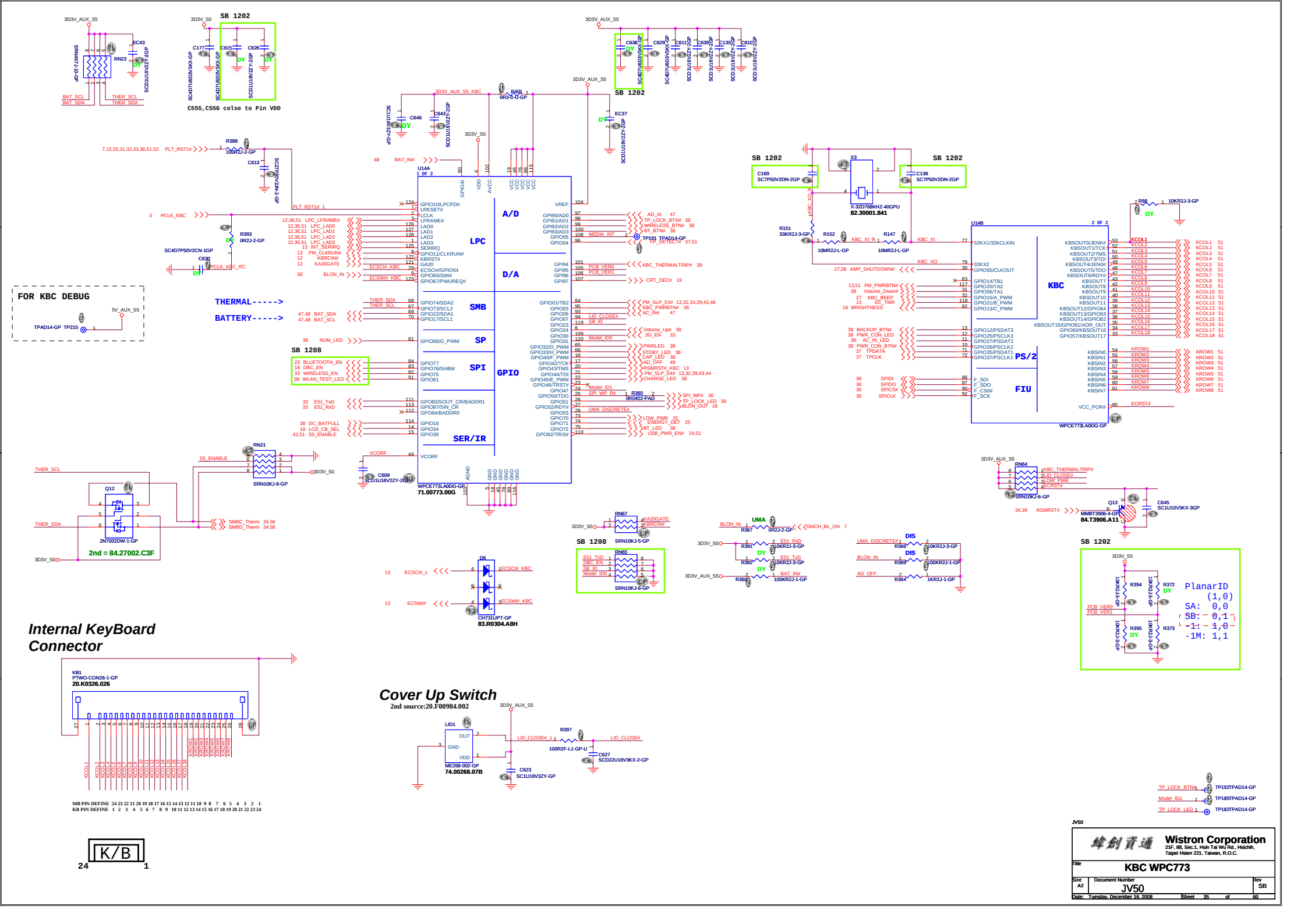
JV50

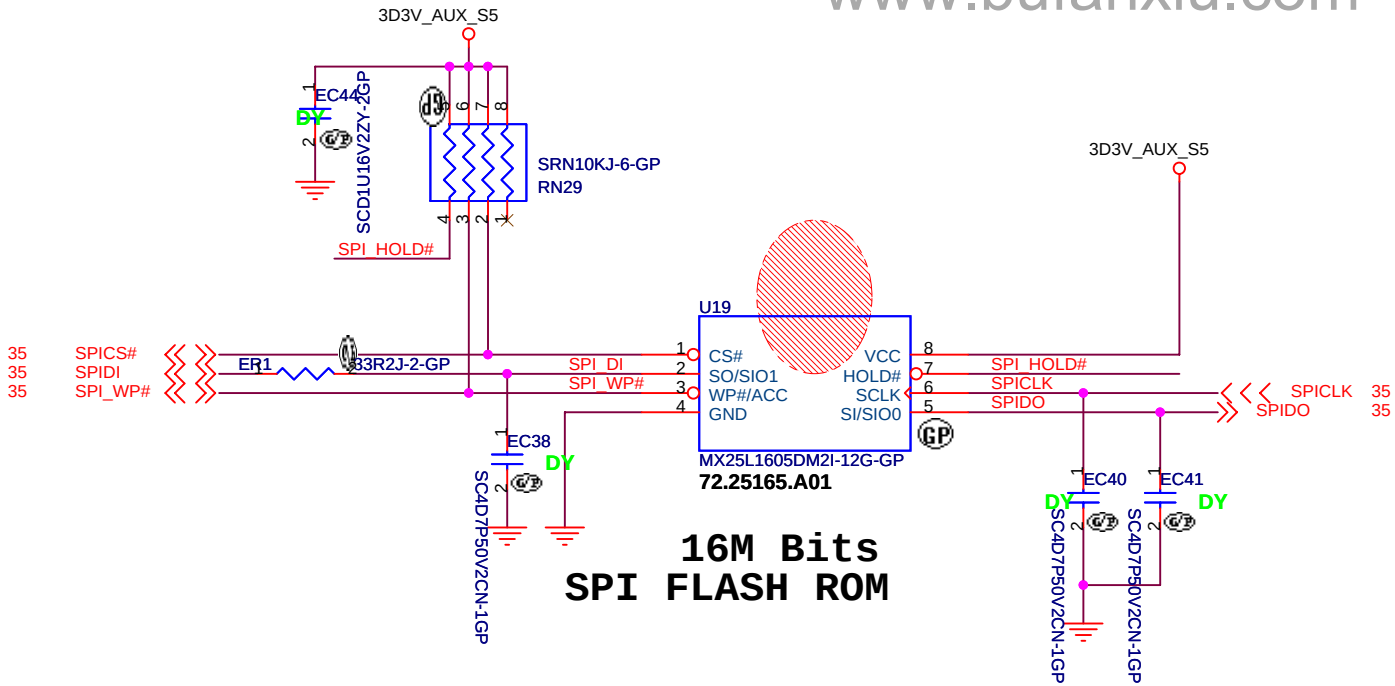
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

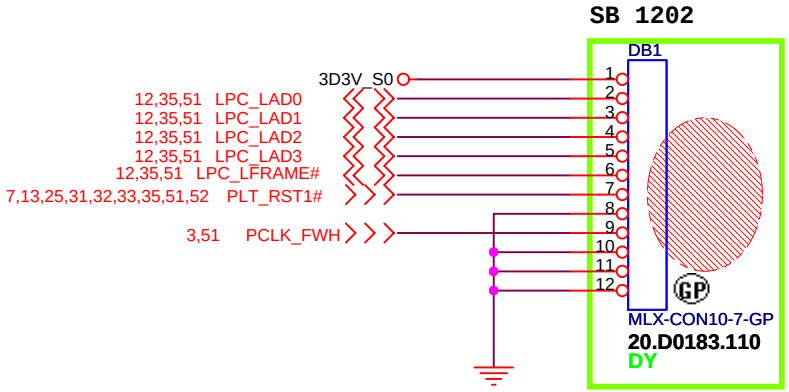
Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 34 of 60


SB 1202
C555,C556 colse to Pin VDD
U14A
WPCE773LA0DG-GP
71.00773.00G
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
FOR KBC DEBUG
THERMAL----->
BATTERY----->
SB 1202
SRN10KJ-6-GP
2N7002DW-1-GP
2nd = 84.27002.C3F
SRN10KJ-5-GP
SRN10KJ-6-GP
CH731UPT-GP
83.R0304.A8H
Internal KeyBoard Connector
KB1
PTWO-CON26-1-GP
20.K0326.026
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
Cover Up Switch
2nd source:20.F00984.002
ME268-002-GP
74.00268.07B
X-32D768KHZ-40GPU
82.30001.841
WPCE773LA0DG-GP
SRN10KJ-6-GP
MMBT3906-4-GP
84.T3906.A11
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1-: 1,0
-1M: 1,1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
JV50
Size A2
Document Number JV50
Rev SB
Date: Tuesday, December 16, 2008
Sheet 35 of 60



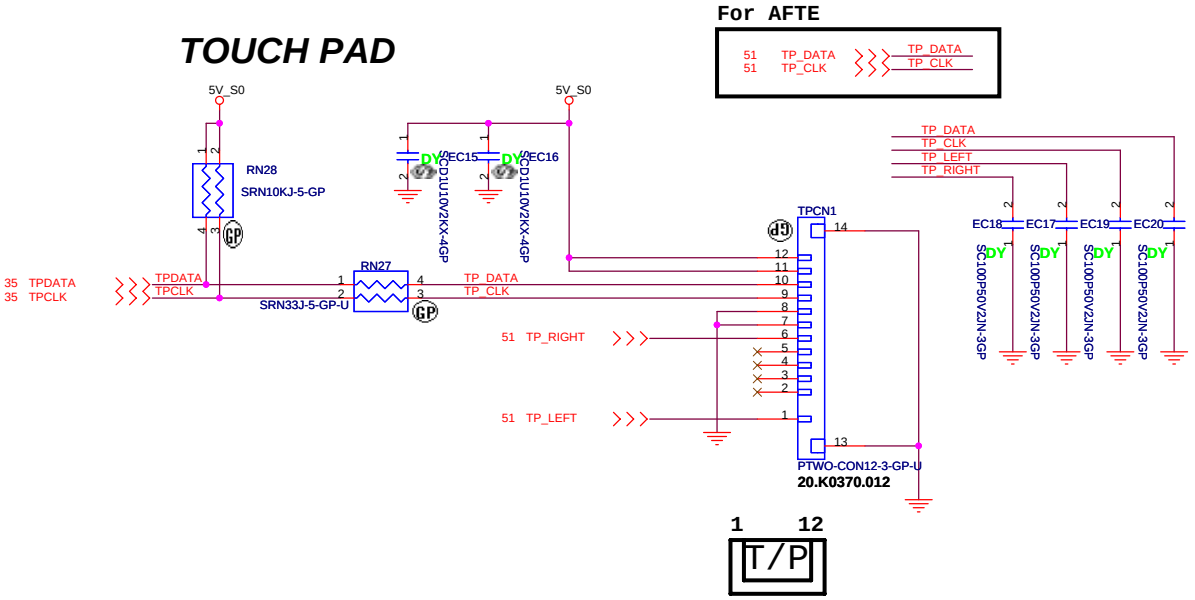
GOLDEN FINGER FOR DEBUG BOARD



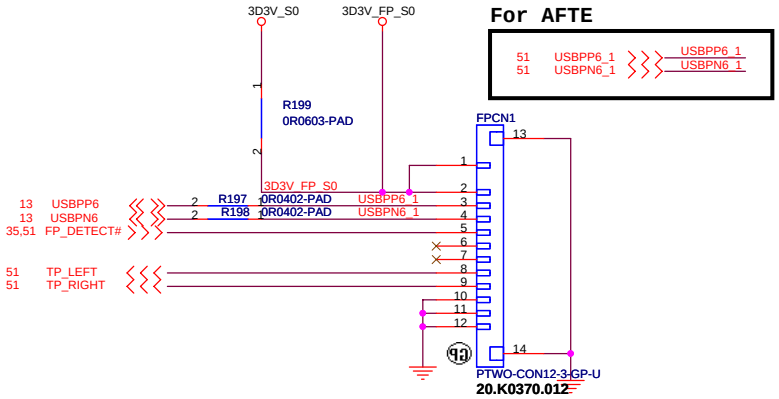
JV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **BIOS**		
Size	Document Number: **JV50**	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 36 of 60	

TOUCH PAD



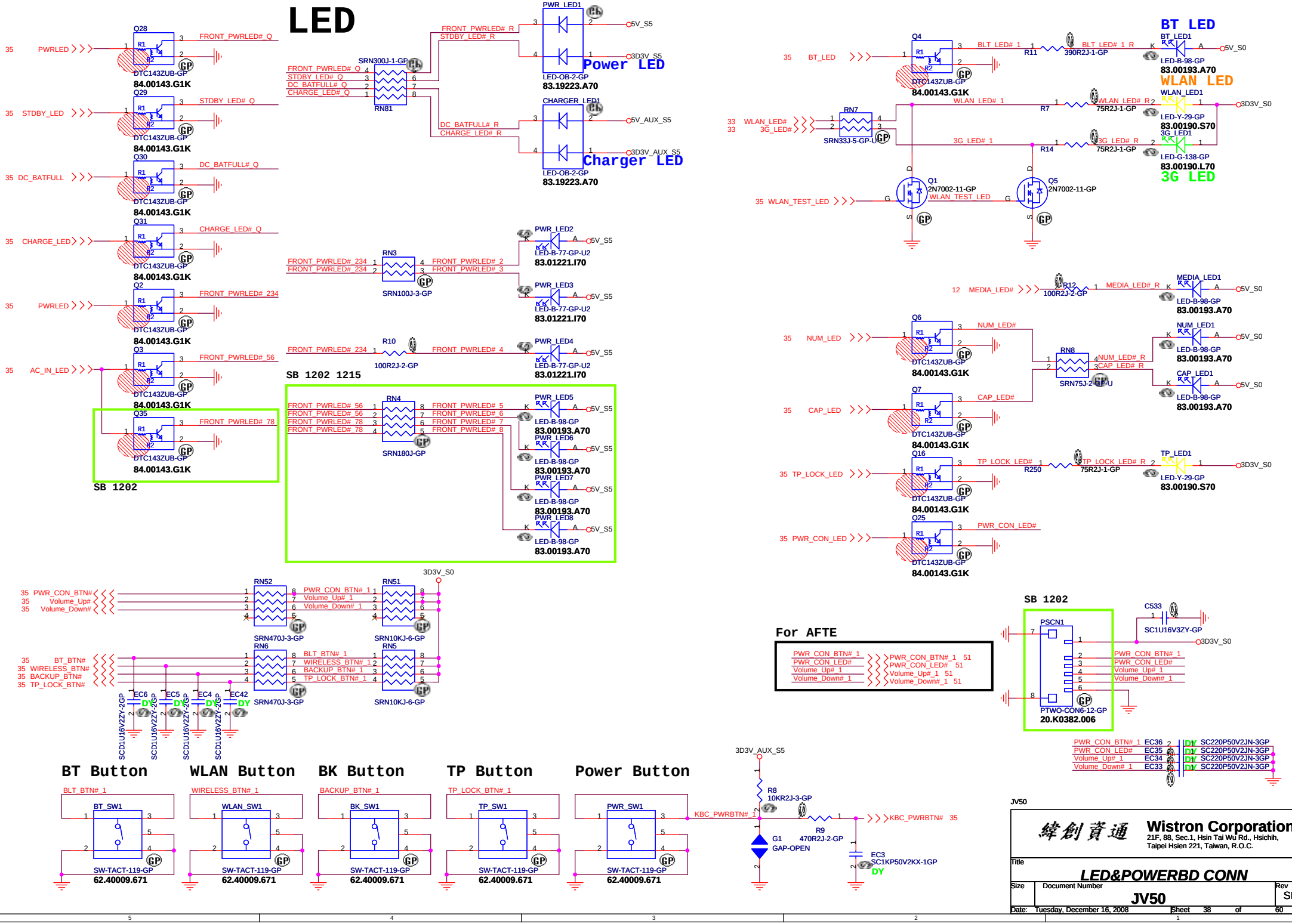
Finger printer



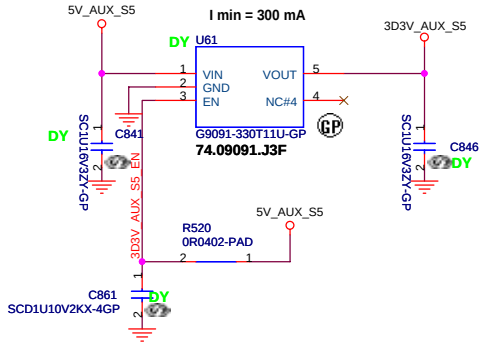
JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Touch PAD and FP*
Size / Document Number	JV50
Rev	SB
Date: Tuesday, December 16, 2008	Sheet 37 of 60

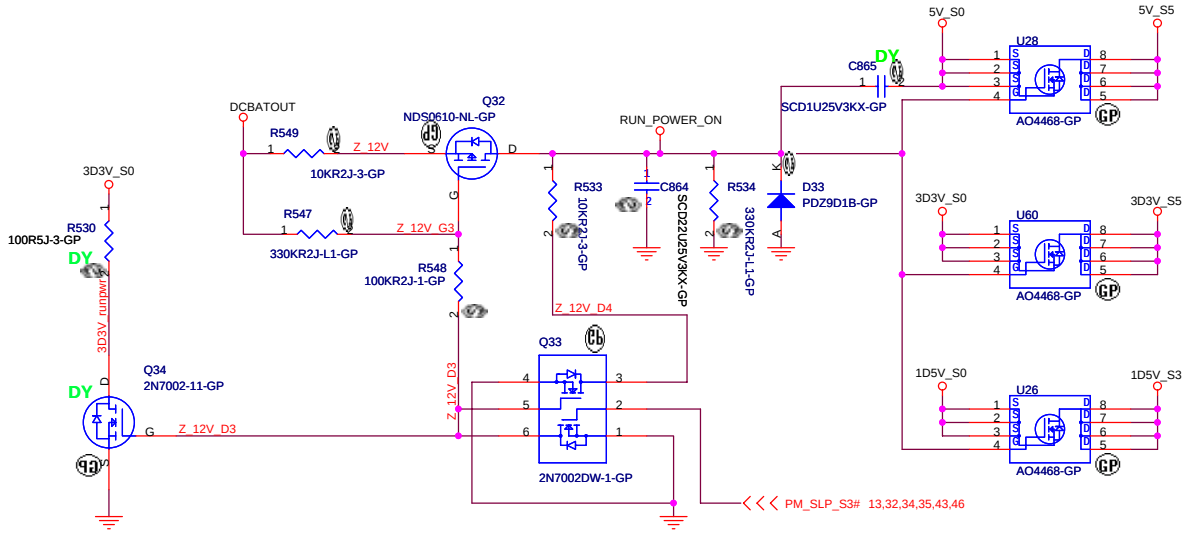
LED

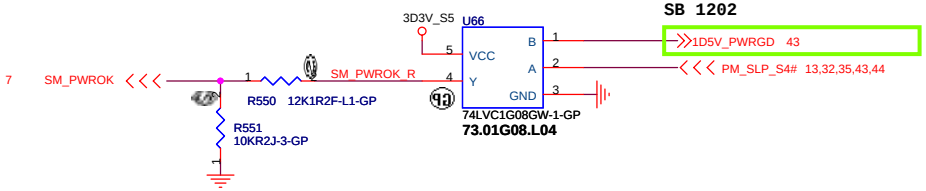

Power LED
Charger LED
BT LED
WLAN LED
3G LED
SB 1202
SB 1202 1215
For AFTE
BT Button
WLAN Button
BK Button
TP Button
Power Button
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LED&POWERBD CONN
JV50
Tuesday, December 16, 2008

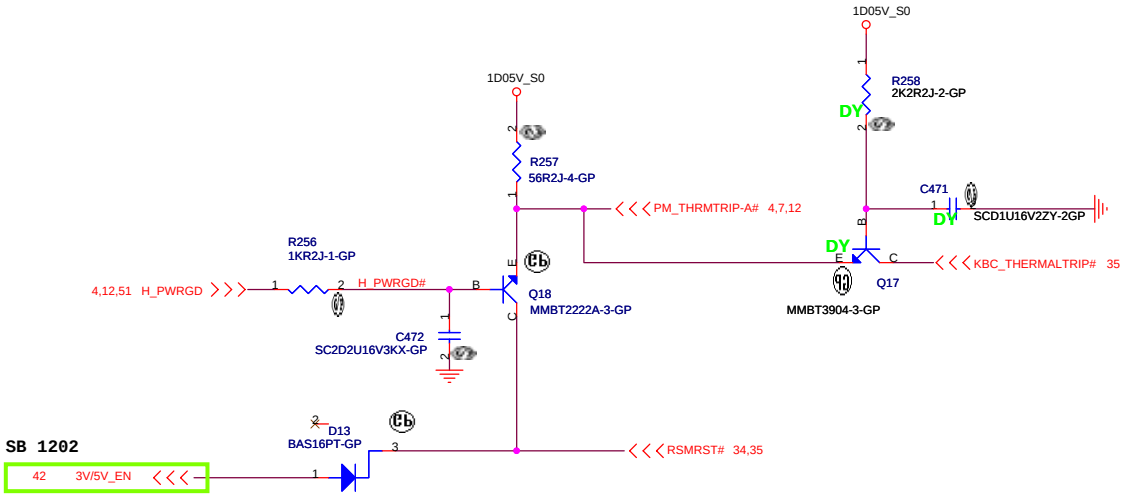
Aux Power 3D3V_AUX_S5



Run Power







JV50

Wistron Corporation
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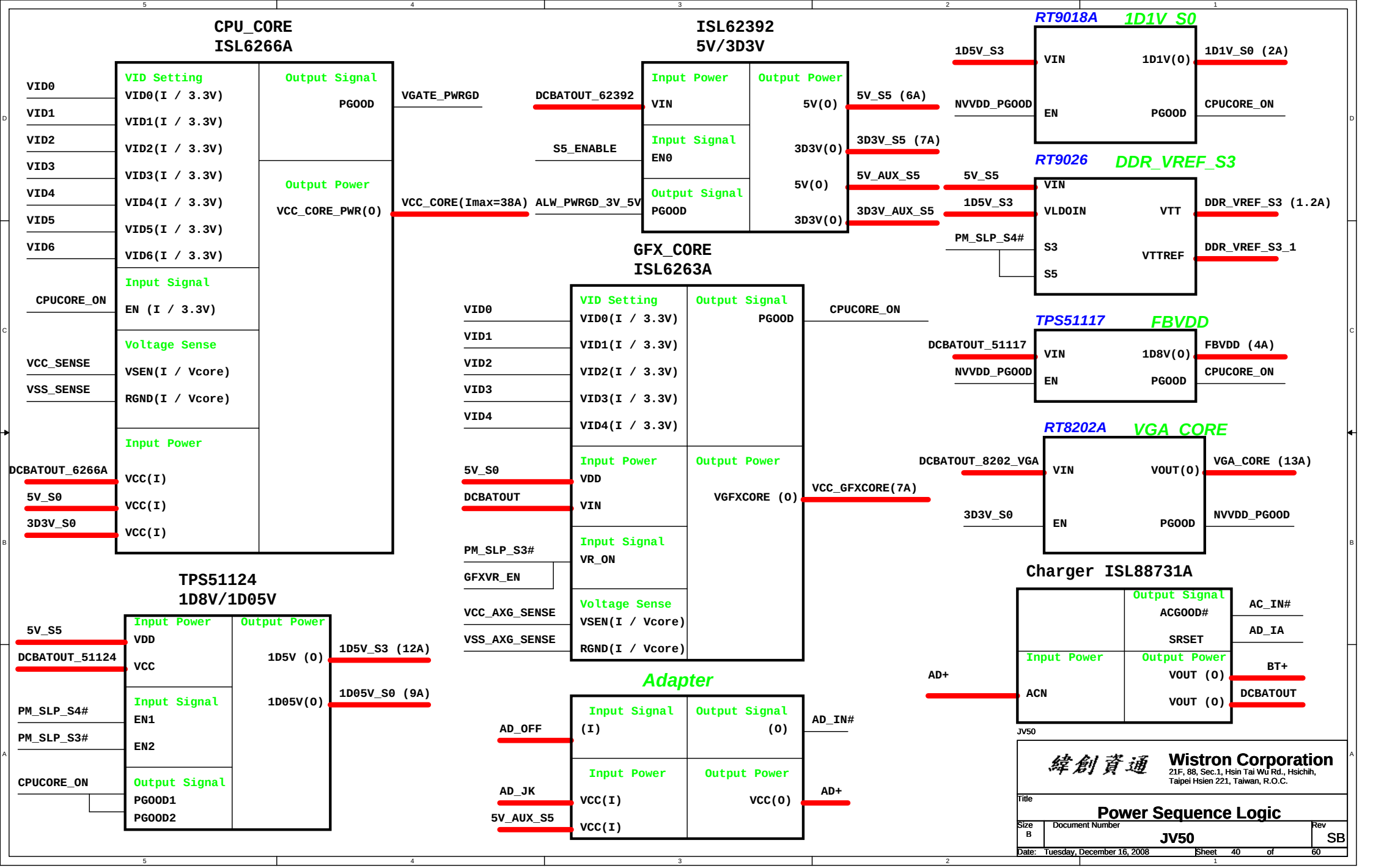
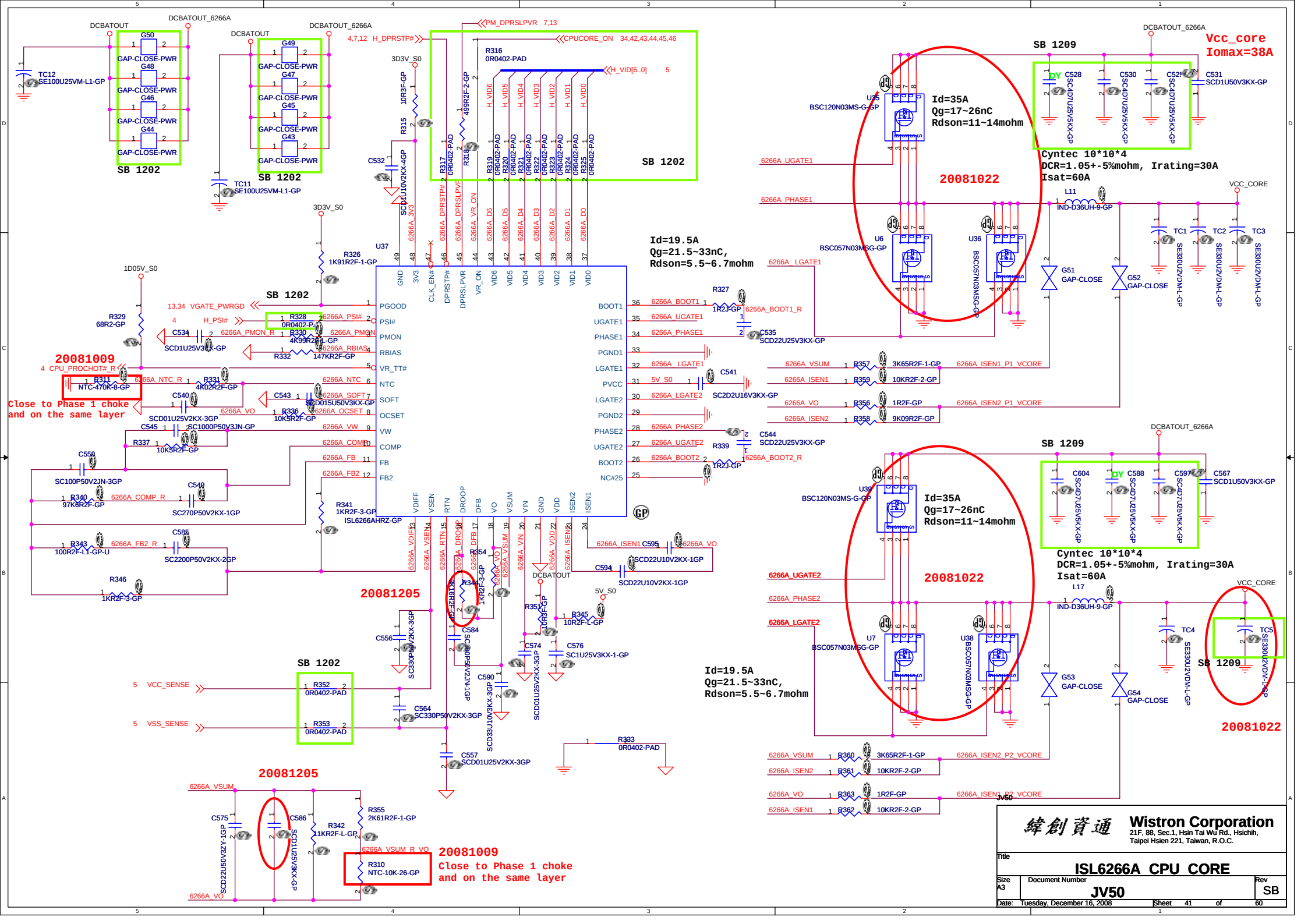
Taipei Hsien 221, Taiwan, R.O.C.

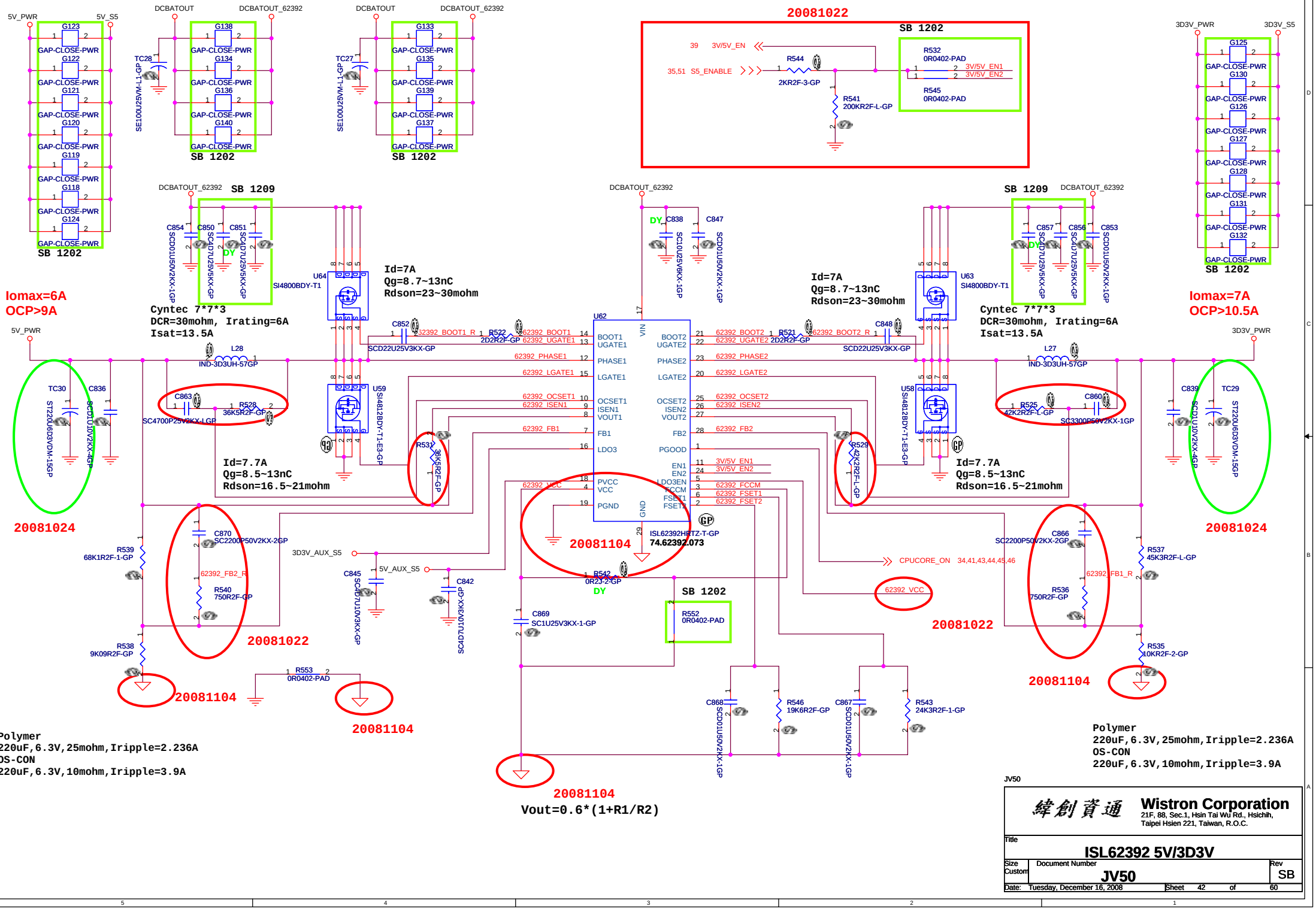
Title: RUN POWER and 3D3V_AUX_S5

Size	Document Number	Rev
	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 39 of 60

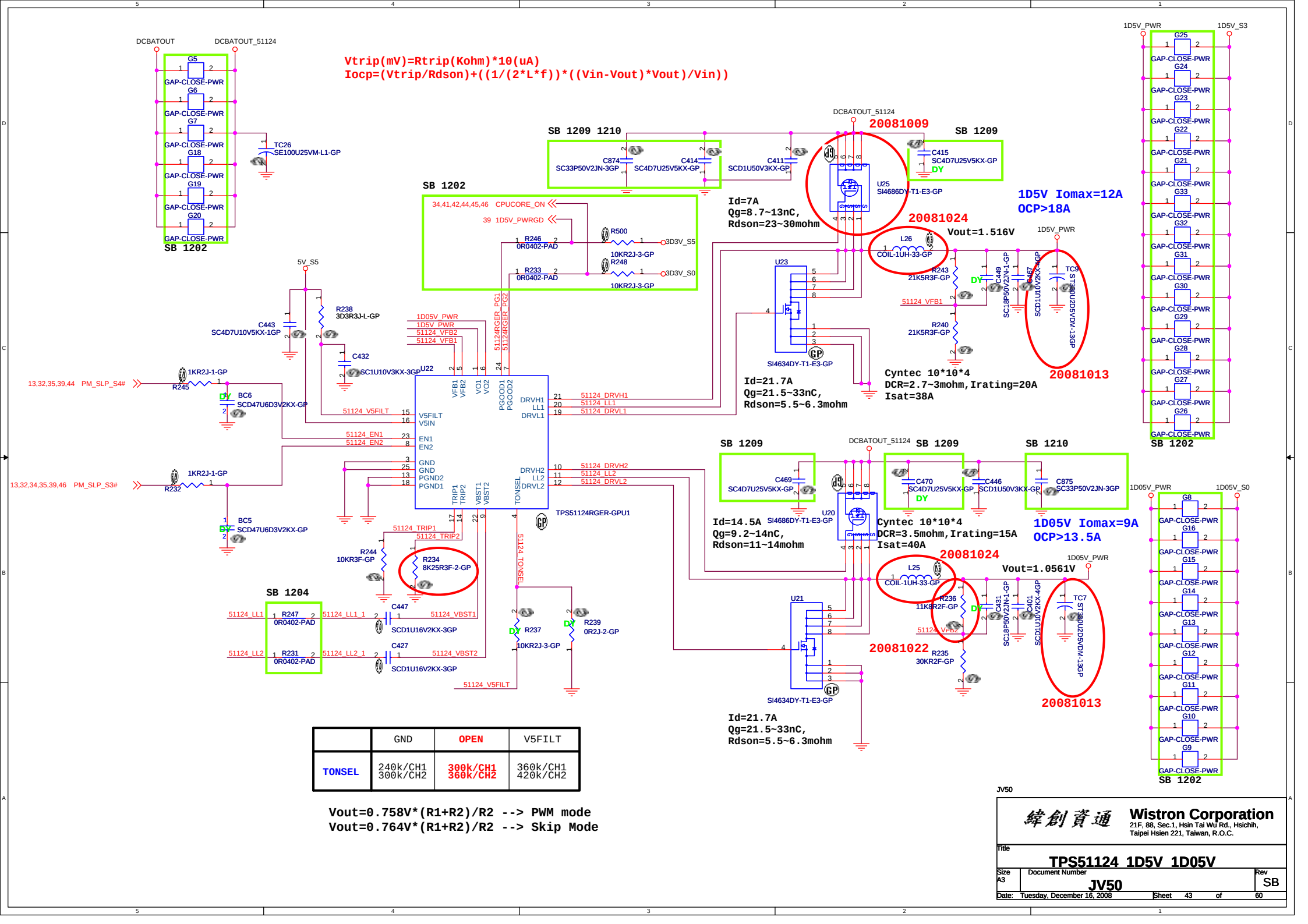

CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
ISL62392
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_62392
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (7A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D1V_S0
VIN
EN
1D1V(O)
PGOOD
1D5V_S3
NVVDD_PGOOD
1D1V_S0 (2A)
CPUCORE_ON
RT9026
DDR_VREF_S3
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D5V_S3
PM_SLP_S4#
DDR_VREF_S3 (1.2A)
DDR_VREF_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(7A)
TPS51117
FBVDD
VIN
EN
1D8V(O)
PGOOD
DCBATOUT_51117
NVVDD_PGOOD
FBVDD (4A)
CPUCORE_ON
RT8202A
VGA_CORE
VIN
EN
VOUT(O)
PGOOD
DCBATOUT_8202_VGA
3D3V_S0
VGA_CORE (13A)
NVVDD_PGOOD
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D5V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D5V_S3 (12A)
1D05V_S0 (9A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
Charger ISL88731A
Output Signal
ACGOOD#
SRSET
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
JV50
Rev
SB
Date: Tuesday, December 16, 2008
Sheet 40 of 60


DCBATOUT
DCBATOUT_6266A
G50
G48
G46
G44
G49
G47
G45
G43
GAP-CLOSE-PWR
SB 1202
TC12
SE100U25VM-L1-GP
TC11
SE100U25VM-L1-GP
PM_DPRSLPVR 7,13
CPUCORE_ON 34,42,43,44,45,46
H_VID[6..0] 5
4,7,12 H_DPRSTP#
R316
0R0402-PAD
3D3V_S0
10R3F-GP
R315
C532
SCD1U10V2KX-4GP
R317
R318
499R2F-2-GP
R319
R320
R321
R322
R323
R324
R325
H_VID6
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
6266A_DPRSTP#
6266A_DPRSLPVR
6266A_VR_ON
6266A_D6
6266A_D5
6266A_D4
6266A_D3
6266A_D2
6266A_D1
6266A_D0
6266A_3V3
1D05V_S0
U37
R326
1K91R2F-1-GP
GND
3V3
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
13,34 VGATE_PWRGD
4 H_PSI#
6266A_PSI#
6266A_PMON
6266A_PMON_R
6266A_RBIAS
6266A_NTC
6266A_NTC_R
6266A_SOFT
6266A_OCSET
6266A_VW
6266A_COMP
6266A_FB
6266A_FB2
6266A_BOOT1
6266A_BOOT1_R
6266A_UGATE1
6266A_PHASE1
6266A_LGATE1
6266A_BOOT2
6266A_BOOT2_R
6266A_UGATE2
6266A_PHASE2
6266A_LGATE2
5V_S0
R327
1R2J-GP
C535
SCD22U25V3KX-GP
C541
SC2D2U16V3KX-GP
C544
SCD22U25V3KX-GP
R339
1R2J-GP
R329
68R2-GP
R328
0R0402-PAD
R330
4K99R2F-1-GP
R332
147KR2F-GP
C534
SCD1U25V3KX-GP
R331
4K02R2F-GP
R311
NTC-470K-8-GP
C540
SCD01U25V2KX-3GP
C543
SCD015U50V3KX-GP
R336
10K5R2F-GP
C545
SC1000P50V3JN-GP
R337
10K5R2F-GP
C550
SC100P50V2JN-3GP
R340
97K6R2F-GP
C549
SC270P50V2KX-1GP
R343
100R2F-L1-GP-U
C585
SC2200P50V2KX-2GP
R346
1KR2F-3-GP
R341
1KR2F-3-GP
ISL6266AHRZ-GP
GP
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND
VDD
ISEN2
ISEN1
6266A_VDIFF
6266A_VSEN
6266A_RTN
6266A_DROOP
6266A_DFB
6266A_VSUM
6266A_VIN
6266A_VDD
6266A_ISEN2
6266A_ISEN1
R354
10R2F-GP
R352
10R2F-GP
R345
10R2F-L-GP
C584
SC1U10V2KX-3GP
C590
SC33U10V3KX-3GP
C574
SCD01U25V2KX-3GP
C576
SC1U25V3KX-1-GP
C556
SC330P50V2KX-3GP
C564
SC330P50V2KX-3GP
C557
SCD01U25V2KX-3GP
C595
SCD22U10V2KX-1GP
C594
SCD22U10V2KX-1GP
R333
0R0402-PAD
R352
0R0402-PAD
R353
0R0402-PAD
5 VCC_SENSE
5 VSS_SENSE
20081009
Close to Phase 1 choke
and on the same layer
20081205
20081205
20081009
Close to Phase 1 choke
and on the same layer
6266A_VSUM
C575
SCD22U50V3ZY-1GP
C586
SCD1U25V3KX-GP
R342
11KR2F-L-GP
R355
2K61R2F-1-GP
R310
NTC-10K-26-GP
6266A_VSUM_R_VO
6266A_VO
SB 1202
SB 1202
SB 1202
SB 1202
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
SB 1209
Vcc_core
Iomax=38A
U35
BSC120N03MS-G-GP
U6
BSC057N03MSG-GP
U36
BSC057N03MSG-GP
Id=35A
Qg=17~26nC
Rdson=11~14mohm
20081022
C528
C530
C529
C531
SC4D7U25V5KX-GP
SCD1U50V3KX-GP
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
L11
IND-D36UH-9-GP
VCC_CORE
TC1
TC2
TC3
SE330U2VDM-L-GP
G51
GAP-CLOSE
G52
GAP-CLOSE
6266A_VSUM
6266A_ISEN1
6266A_VO
6266A_ISEN2
R357
3K65R2F-1-GP
R359
10KR2F-2-GP
R356
1R2F-GP
R358
9K09R2F-GP
6266A_ISEN1_P1_VCORE
6266A_ISEN2_P1_VCORE
U39
BSC120N03MS-G-GP
U7
BSC057N03MSG-GP
U38
BSC057N03MSG-GP
Id=35A
Qg=17~26nC
Rdson=11~14mohm
20081022
C604
C588
C597
C567
SCD1U50V3KX-GP
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
L17
IND-D36UH-9-GP
TC4
TC5
G53
GAP-CLOSE
G54
GAP-CLOSE
R360
3K65R2F-1-GP
R361
10KR2F-2-GP
R363
1R2F-GP
R362
10KR2F-2-GP
6266A_ISEN2_P2_VCORE
6266A_ISEN1_P2_VCORE
JV50
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
SB 1209
SB 1209
20081022
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A CPU CORE
Size
A3
Document Number
JV50
Rev
SB
Date: Tuesday, December 16, 2008
Sheet 41 of 60



JV50

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL62392 5V/3D3V
Size: Custom	Document Number: JV50
Rev	SB
Date: Tuesday, December 16, 2008	Sheet 42 of 60



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

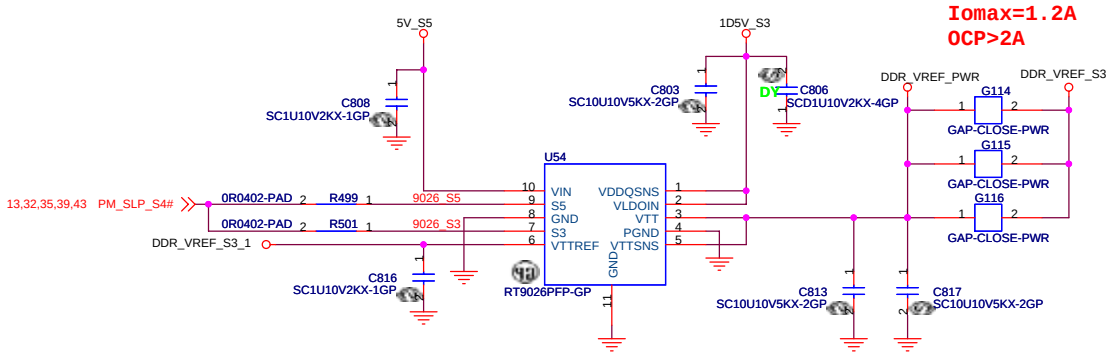
JV50

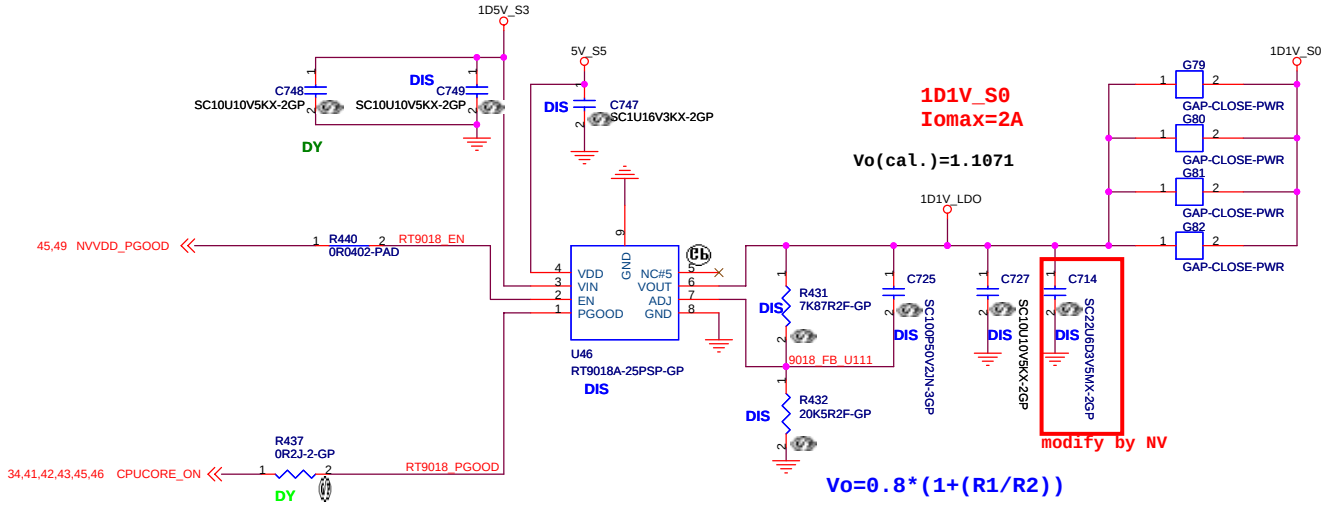
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D5V 1D05V

Size	Document Number	Rev
A3	JV50	SB

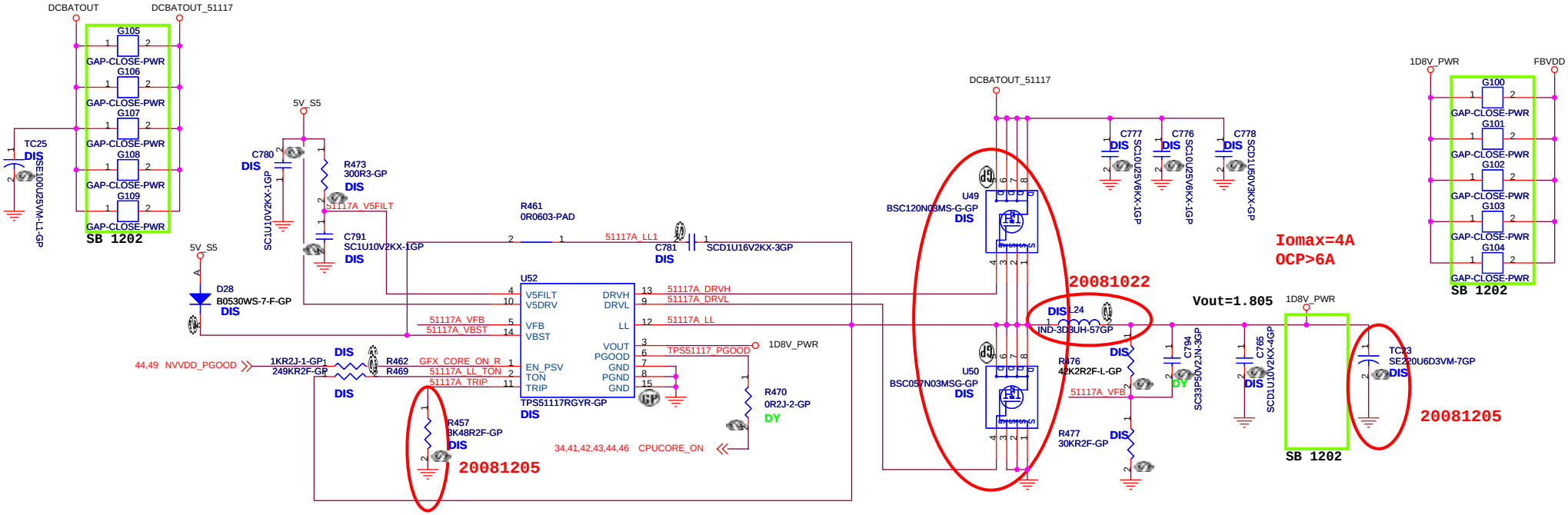
Date: Tuesday, December 16, 2008 Sheet 43 of 60





JV50

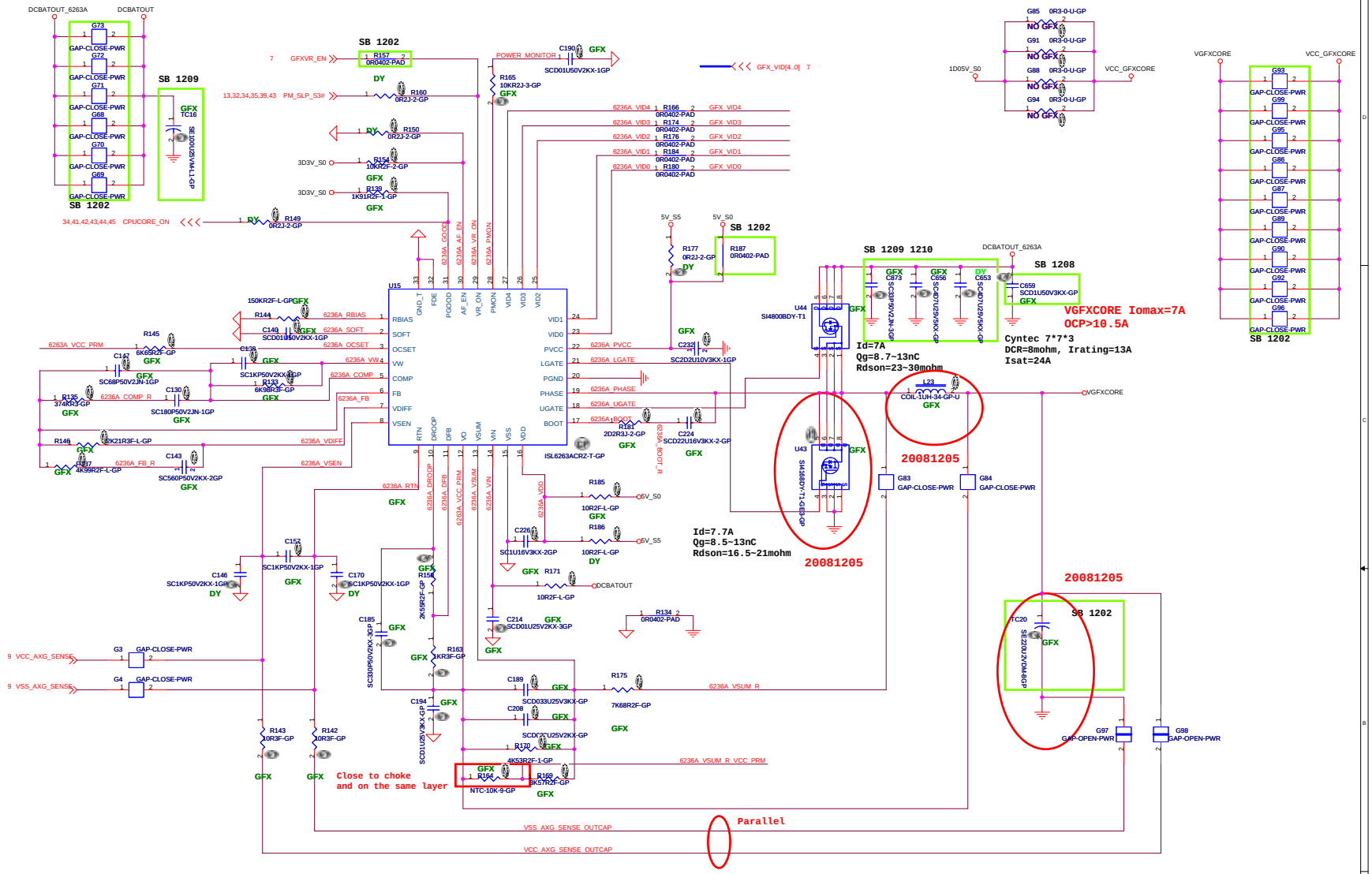
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D75V/1D1V		
Size: A3	Document Number: JV50	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 44 of 60	



Vout=0.75V*(R1+R2)/R2

JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**TPS51117 1D8V**	
Size: A3	Document Number: **JV50**	Rev: SB
Date: Tuesday, December 16, 2008	Sheet 45 of 60	



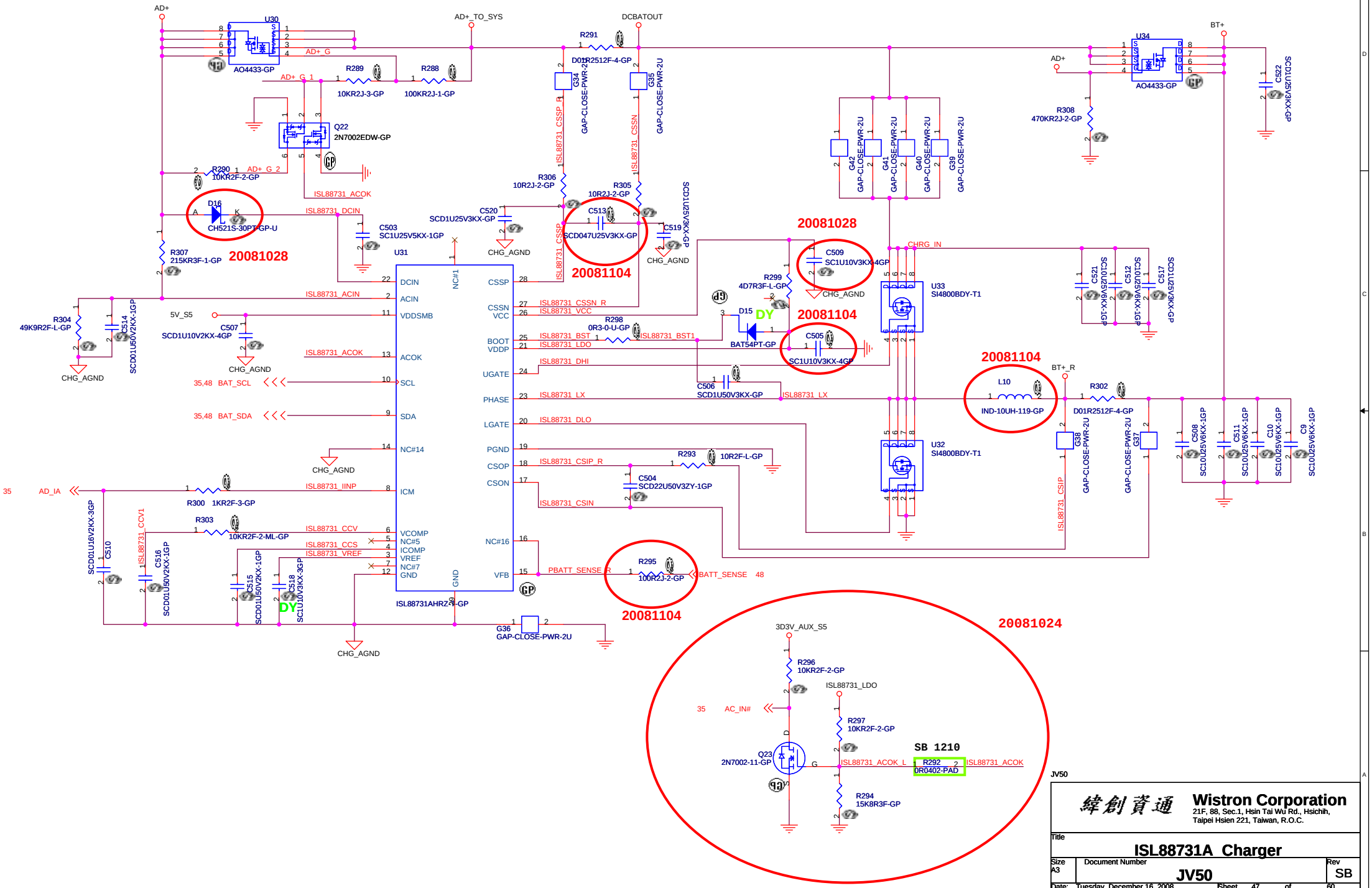
JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

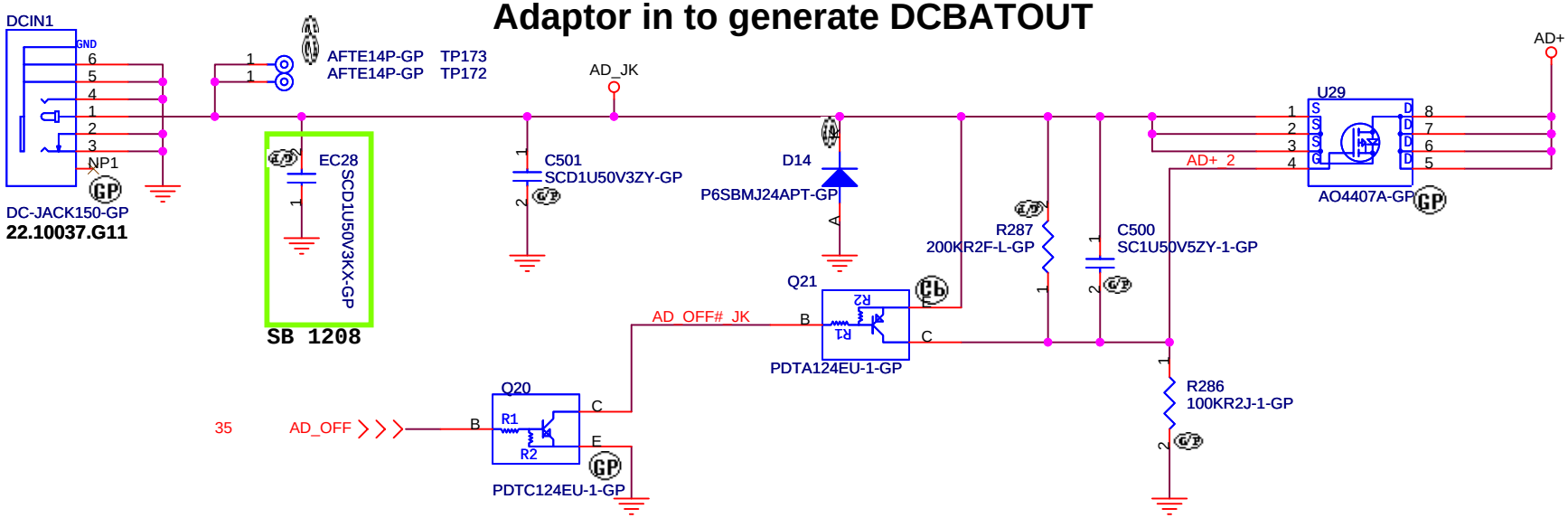
Title: ISL6263A_GFX CORE

Size	Document Number	Rev
Custom	JV50	SB

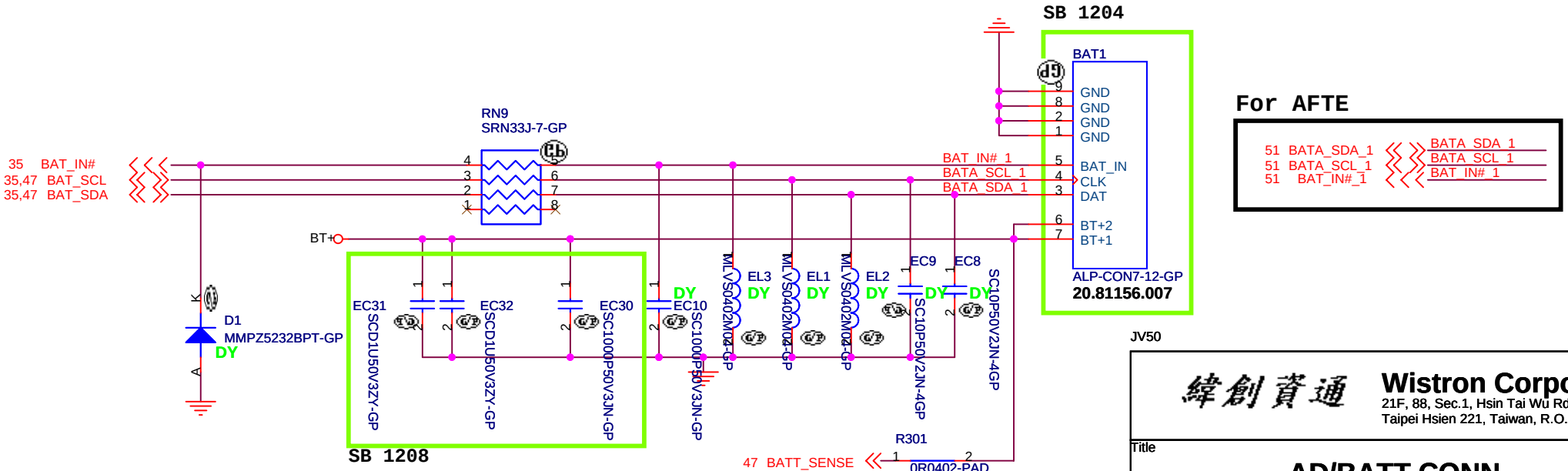
Date: Tuesday, December 16, 2008 Sheet 46 of 60


AD+
AD+_TO_SYS
DCBATOUT
BT+
U30
AO4433-GP
U34
AO4433-GP
AD+_G
AD+_G_1
AD+_G_2
R289
10KR2J-3-GP
R288
100KR2J-1-GP
R291
D01R2512F-4-GP
Q22
2N7002EDW-GP
R290
10KR2F-2-GP
R308
470KR2J-2-GP
C522
SCD1U25V3KX-GP
G34 GAP-CLOSE-PWR-2U
G35 GAP-CLOSE-PWR-2U
G42 GAP-CLOSE-PWR-2U
G41 GAP-CLOSE-PWR-2U
G40 GAP-CLOSE-PWR-2U
G39 GAP-CLOSE-PWR-2U
ISL88731_ACOK
ISL88731_DCIN
D16
CH521S-30PT-GP-U
R306
10R2J-2-GP
R305
10R2J-2-GP
C520
SCD1U25V3KX-GP
C513
SCD047U25V3KX-GP
C519
SCD1U25V3KX-GP
ISL88731_CSSP_R
ISL88731_CSSN
CHG_AGND
20081028
20081104
C503
SC1U25V5KX-1GP
R307
215KR3F-1-GP
U31
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
NC#1
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
ISL88731_VREF
PBATT_SENSE_R
R299
4D7R3F-L-GP
D15
BAT54PT-GP
DY
R298
0R3-0-U-GP
C505
SC1U10V3KX-4GP
C509
SC1U10V3KX-4GP
C506
SCD1U50V3KX-GP
CHRG_IN
U33
SI4800BDY-T1
U32
SI4800BDY-T1
L10
IND-10UH-119-GP
BT+_R
R302
D01R2512F-4-GP
G38 GAP-CLOSE-PWR-2U
G37 GAP-CLOSE-PWR-2U
C521
C512
C517
SCD1U25V3KX-GP
C508
C511
C10
C9
SC10U25V6KX-1GP
R304
49K9R2F-L-GP
C514
SCD01U50V2KX-1GP
5V_S5
C507
SCD1U10V2KX-4GP
35,48 BAT_SCL
35,48 BAT_SDA
R293
10R2F-L-GP
C504
SCD22U50V3ZY-1GP
35 AD_IA
R300
1KR2F-3-GP
R303
10KR2F-2-ML-GP
C510
SCD01U16V2KX-3GP
C516
SCD01U50V2KX-1GP
C515
SCD01U50V2KX-1GP
C518
SC1U10V3KX-3GP
R295
100R2J-2-GP
PBATT_SENSE
48 BATT_SENSE
G36 GAP-CLOSE-PWR-2U
20081024
3D3V_AUX_S5
R296
10KR2F-2-GP
35 AC_IN#
R297
10KR2F-2-GP
Q23
2N7002-11-GP
SB 1210
R292
0R0402-PAD
ISL88731_ACOK_L
ISL88731_ACOK
R294
15K8R3F-GP
JV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV50
Rev
SB
Date: Tuesday, December 16, 2008
Sheet 47 of 60

Adaptor in to generate DCBATOUT

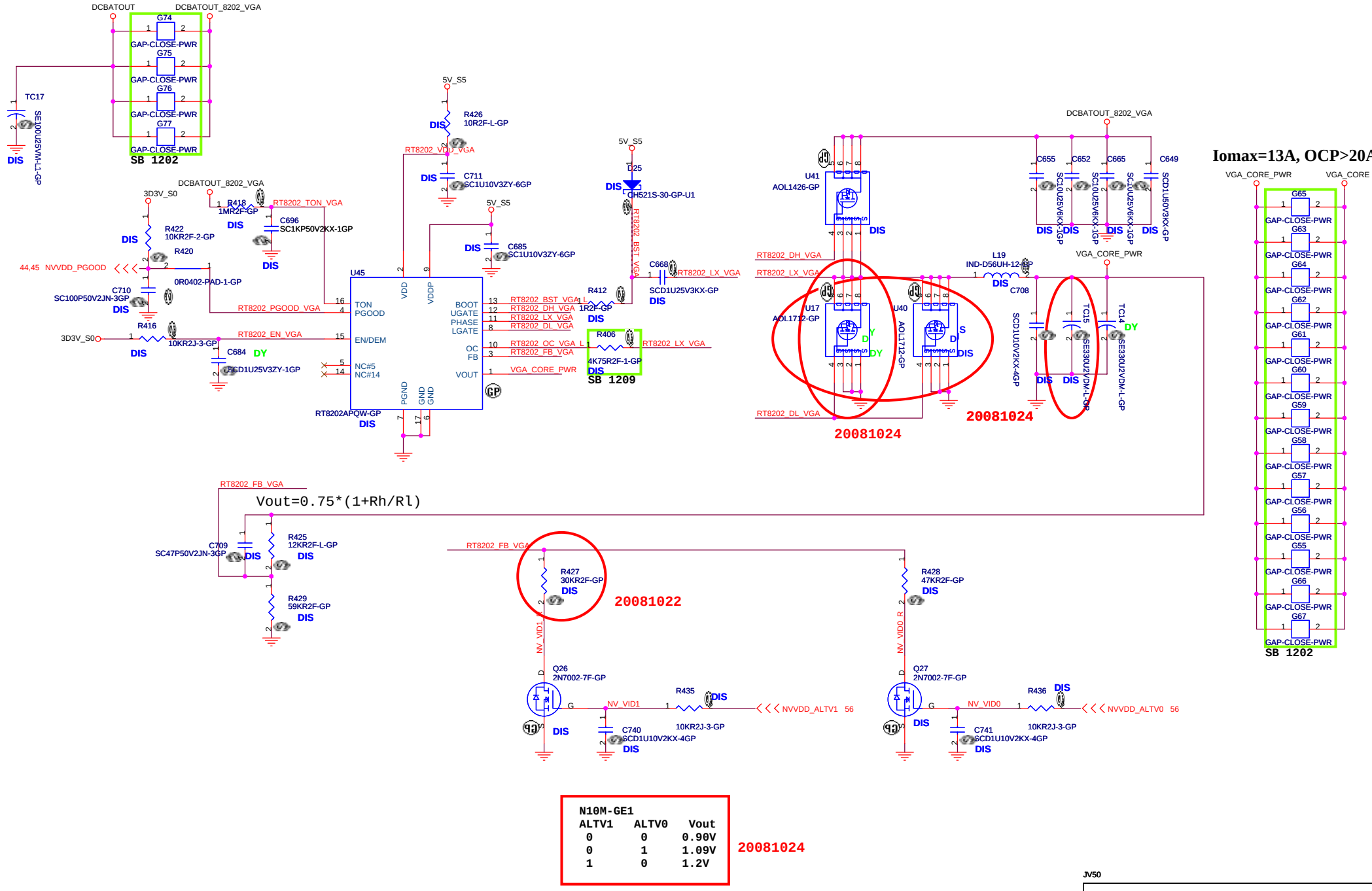


BATTERY CONNECTOR

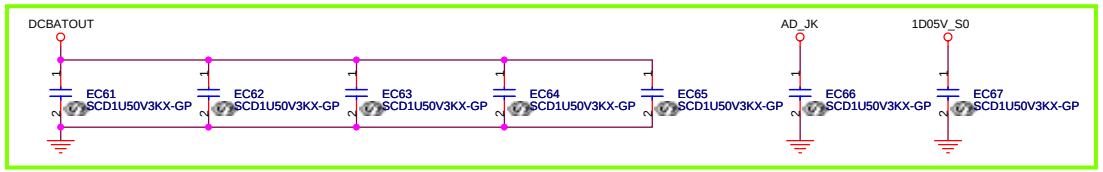


JV50

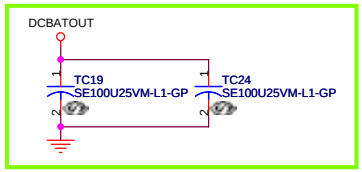
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size	Document Number **JV50**	Rev SB
Date: Tuesday, December 16, 2008	Sheet 48 of 60	


DCBATOUT
DCBATOUT_8202_VGA
G74
G75
G76
G77
GAP-CLOSE-PWR
SB 1202
TC17
SE100U25VM-L1-GP
DIS
5V_S5
R426
10R2F-L-GP
RT8202_VDD_VGA
C711
SC1U10V3ZY-6GP
C685
SC1U10V3ZY-6GP
3D3V_S0
R418
1MR2F-GP
RT8202_TON_VGA
C696
SC1KP50V2KX-1GP
R422
10KR2F-2-GP
R420
0R0402-PAD-1-GP
44,45 NVVDD_PGOOD
C710
SC100P50V2JN-3GP
RT8202_PGOOD_VGA
R416
10KR2J-3-GP
C684
SCD1U25V3ZY-1GP
U45
TON
PGOOD
EN/DEM
NC#5
NC#14
VDD
VDDP
PGND
GND
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
RT8202_BST_VGA
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA
RT8202_FB_VGA
VGA_CORE_PWR
RT8202APQW-GP
D25
CH521S-30-GP-U1
C668
SCD1U25V3KX-GP
R412
1R2F-GP
R406
4K75R2F-1-GP
SB 1209
U41
AOL1426-GP
U17
AOL1712-GP
U40
AOL1712-GP
L19
IND-D56UH-12-GP
C708
SCD1U10V2KX-4GP
TC15
SE330U2VDM-L-GP
TC14
SE330U2VDM-L-GP
C655
C652
C665
C649
SC10U25V6KX-1GP
SCD1U50V3KX-GP
20081024
Iomax=13A, OCP>20A
VGA_CORE_PWR
VGA_CORE
G65
G63
G64
G62
G61
G60
G59
G58
G57
G56
G55
G66
G67
SB 1202
RT8202_FB_VGA
Vout=0.75*(1+Rh/Rl)
C709
SC47P50V2JN-3GP
R425
12KR2F-L-GP
R429
59KR2F-GP
R427
30KR2F-GP
20081022
R428
47KR2F-GP
Q26
2N7002-7F-GP
Q27
2N7002-7F-GP
NV_VID1
NV_VID0
R435
R436
10KR2J-3-GP
C740
C741
SCD1U10V2KX-4GP
NVVDD_ALTV1 56
NVVDD_ALTV0 56
N10M-GE1
ALTV1 ALTV0 Vout
0 0 0.90V
0 1 1.09V
1 0 1.2V
20081024
JV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8202A VGA CORE
Size
A3
Document Number
JV50
Rev
SB
Date: Tuesday, December 16, 2008
Sheet 49 of 60

SB 1208



SB 1209



CPU

H1 HOLE ZZ.0HOLE.XXX
H2 HOLE ZZ.0HOLE.XXX
H3 HOLE ZZ.0HOLE.XXX
34.4Z003.001 34.4Z003.001 34.4Z003.001

NB

H4 HOLE ZZ.0HOLE.XXX
34.4Z003.001

VGA

H5 HOLE ZZ.0HOLE.XXX
H6 HOLE ZZ.0HOLE.XXX
34.4Z003.001 34.4Z003.001

MDC

H7 HOLE ZZ.0HOLE.XXX
34.42Y01.011

MINICARD

H8 HOLE ZZ.0HOLE.XXX
34.4P901.001

H9 HOLE ZZ.0HOLE.XXX
H10 HOLE ZZ.0HOLE.XXX

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND9 GND10 GND11 GND12
HOLE355X355R111-S1-GP

SPRING_GND16 SPRING-12-GP-U
SPRING_GND17 SPRING-12-GP-U
SPRING_GND18 SPRING-12-GP-U
SPRING_GND19 SPRING-12-GP-U
SPRING_GND20 SPRING-12-GP-U
34.41Y19.001

SPRING_GND14 SPRING-7
SPRING_GND15 SPRING-7
SPRING_GND21 SPRING-7
SPRING_GND22 SPRING-7
DY
34.49U26.001

SB 1208

JV50

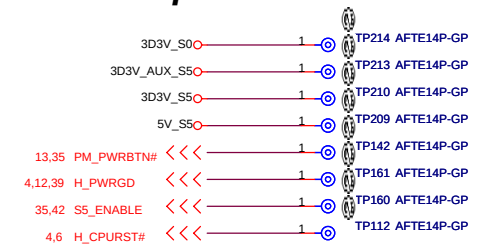
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *EMI/Spring/Boss*

Size	Document Number	Rev
	JV50	SB

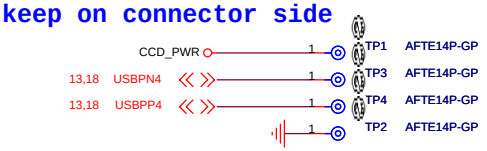
Date: Tuesday, December 16, 2008 Sheet 50 of 60

Check test point

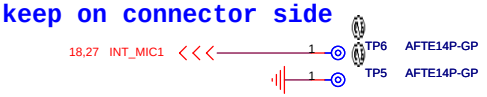


Test Point放在Dimm Door打開可量測處

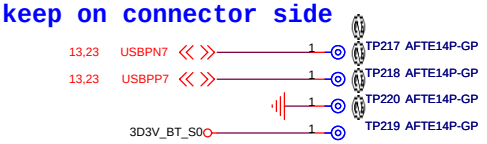
CCD1 Conn. Test Point keep on connector side



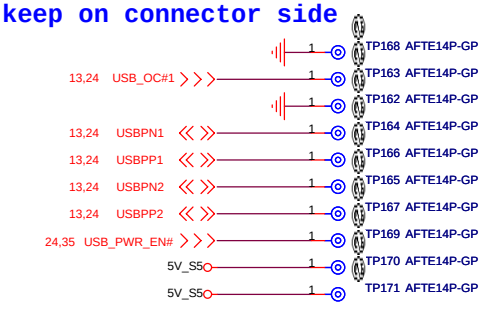
AMIC1 Conn. Test Point keep on connector side



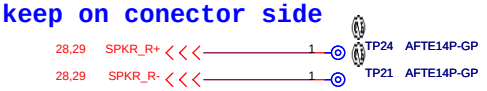
BT1 Conn. Test Point keep on connector side



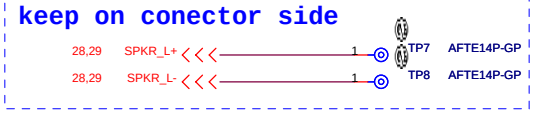
USBCN1 Conn. Test Point keep on connector side



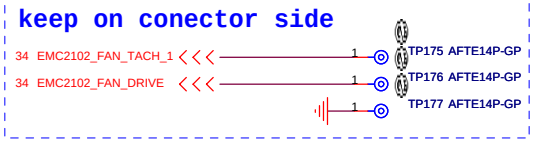
SPKR_R1 Conn. Test Point keep on conector side



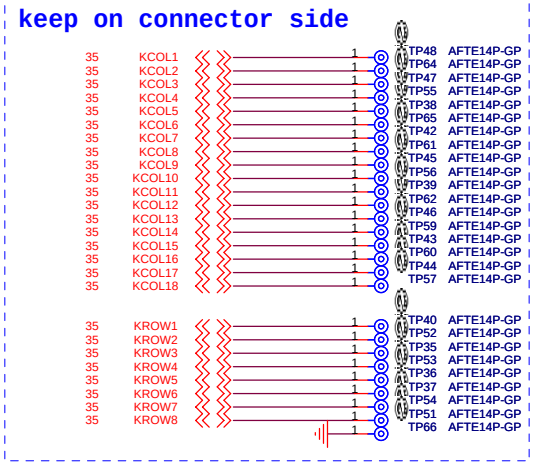
SPKR_L1 Conn. Test Point keep on conector side



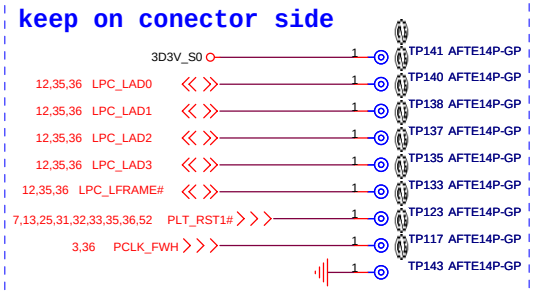
FAN1 Conn. Test Point keep on conector side



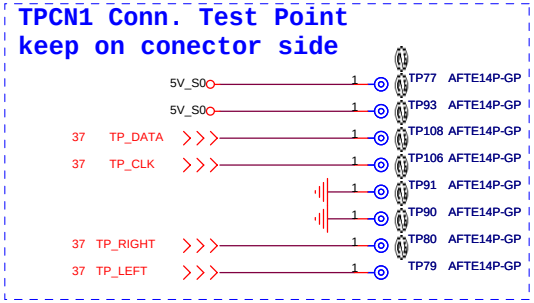
KB1 Conn. Test Point keep on connector side



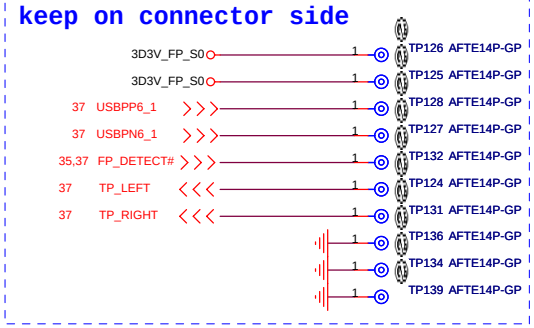
DB1 Conn. Test Point keep on conector side



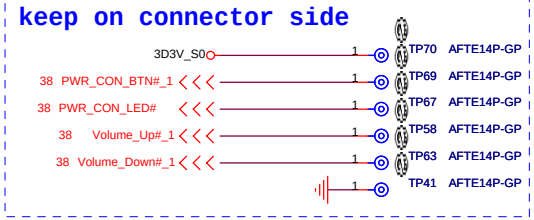
TPCN1 Conn. Test Point keep on conector side



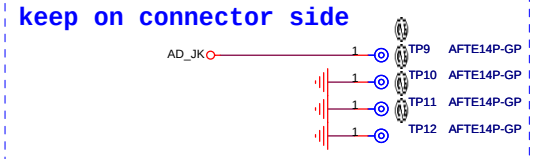
FPCN1 Conn. Test Point keep on connector side



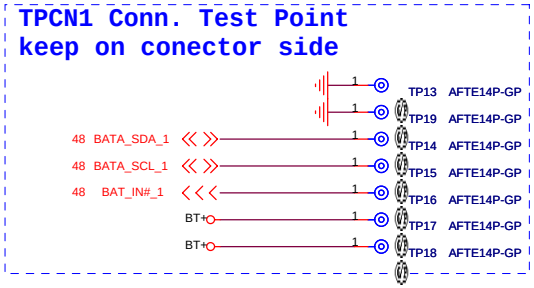
PSCN1 Conn. Test Point keep on connector side



DCIN1 Conn. Test Point keep on connector side



TPCN1 Conn. Test Point keep on conector side



JV50

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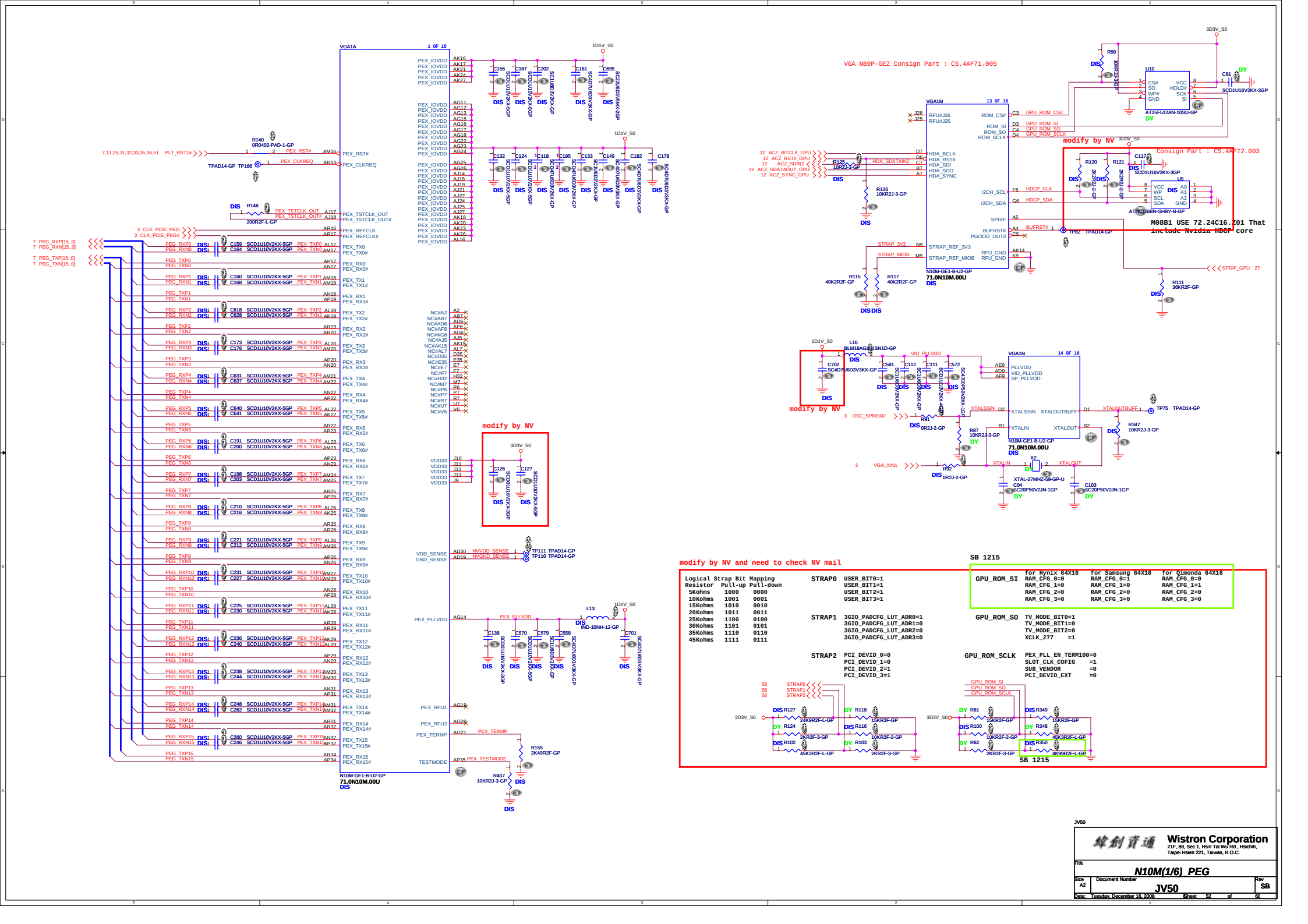
Title: **AFTE TP**

Size	Document Number	Rev
A3	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 51 of 60


VGA NB9P-GE2 Consign Part : CS.4AF71.005
modify by NV
Consign Part : CS.4AP72.003
M08B1 USE 72.24C16.201 That include Nvidia HDCP core
modify by NV and need to check NV mail
SB 1215
Logical Strap Bit Mapping
Resistor Pull-up Pull-down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111
STRAP0 USER_BIT0=1
USER_BIT1=1
USER_BIT2=1
USER_BIT3=1
STRAP1 3GIO_PADCFG_LUT_ADR0=1
3GIO_PADCFG_LUT_ADR1=0
3GIO_PADCFG_LUT_ADR2=0
3GIO_PADCFG_LUT_ADR3=0
STRAP2 PCI_DEVID_0=0
PCI_DEVID_1=0
PCI_DEVID_2=1
PCI_DEVID_3=1
GPU_ROM_SI for Hynix 64X16 for Samsung 64X16 for Qimonda 64X16
RAM_CFG_0=0 RAM_CFG_0=1 RAM_CFG_0=0
RAM_CFG_1=0 RAM_CFG_1=0 RAM_CFG_1=1
RAM_CFG_2=0 RAM_CFG_2=0 RAM_CFG_2=0
RAM_CFG_3=0 RAM_CFG_3=0 RAM_CFG_3=0
GPU_ROM_SO TV_MODE_BIT0=1
TV_MODE_BIT1=0
TV_MODE_BIT2=0
XCLK_277 =1
GPU_ROM_SCLK PEX_PLL_EN_TERM100=0
SLOT_CLK_COFIG =1
SUB_VENDOR =0
PCI_DEVID_EXT =0
Wistron Corporation
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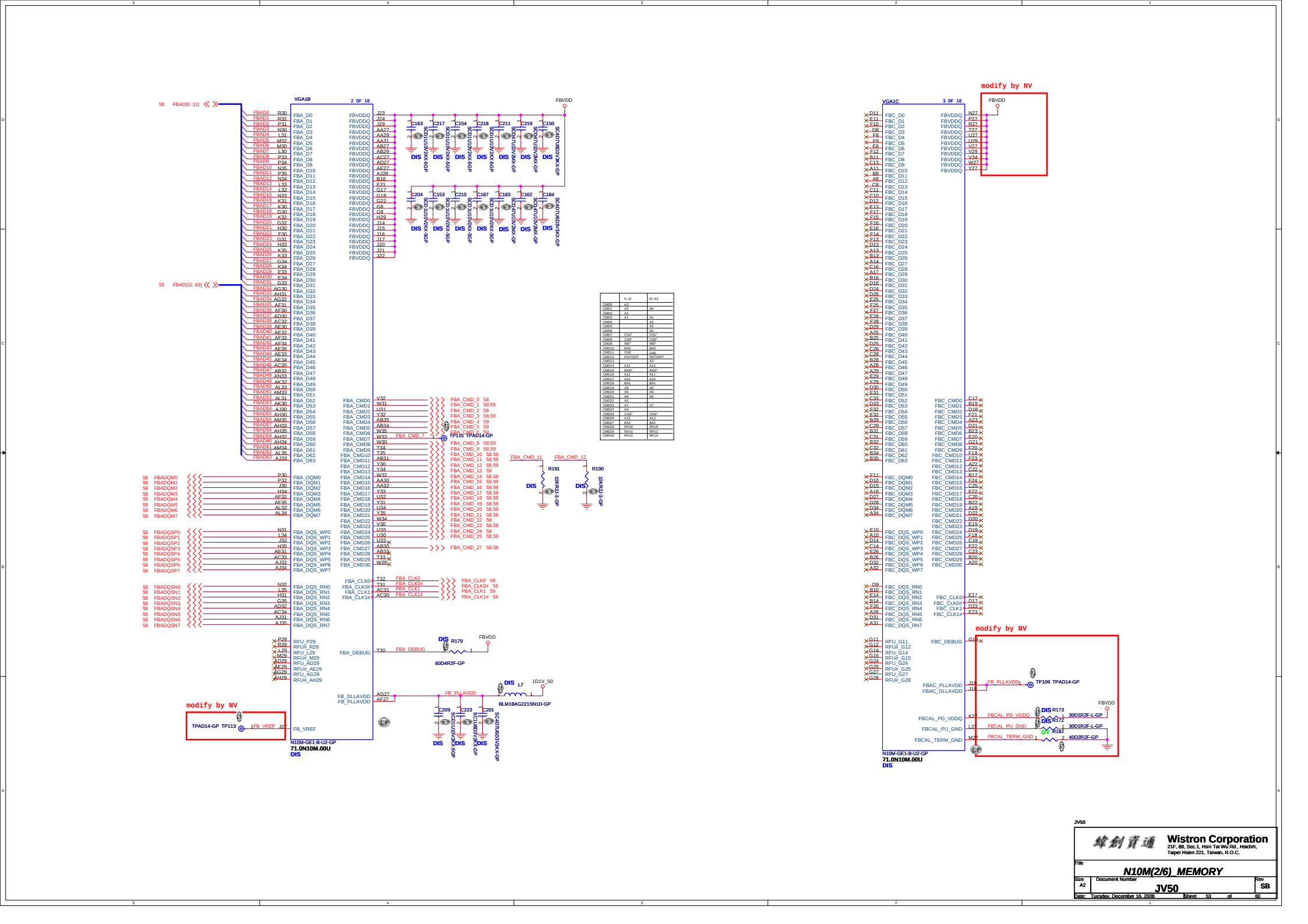
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(1/6)_PEG
Size A2
Document Number JV50
Rev SB
Date: Tuesday, December 16, 2008
Sheet 52 of 60



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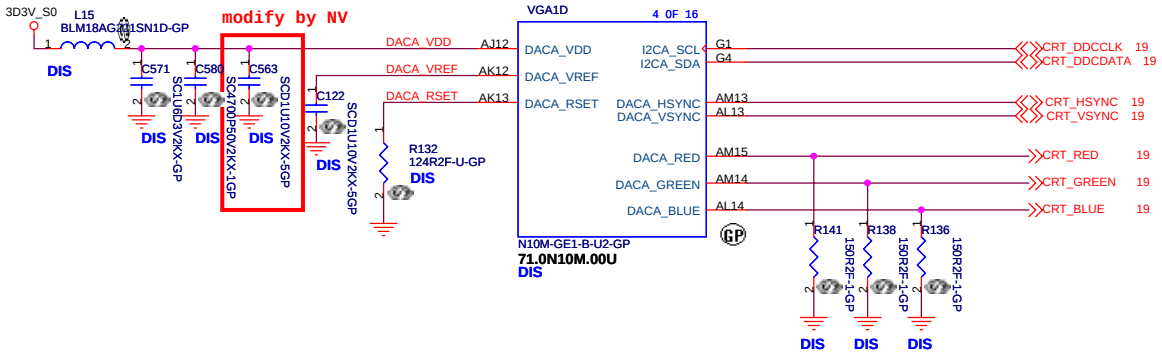
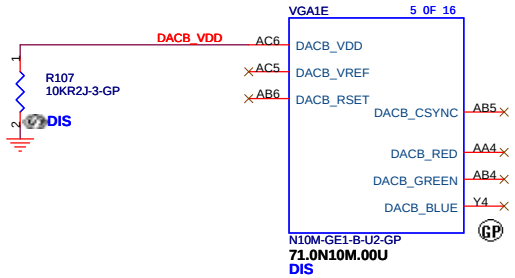
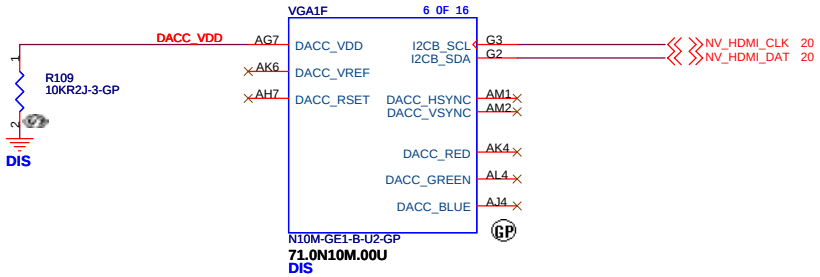
Title: N10M(2/6)_MEMORY

Size: A2 | Document Number: JV50 | Rev: SB

Date: Tuesday, December 16, 2008 | Sheet 53 of 60







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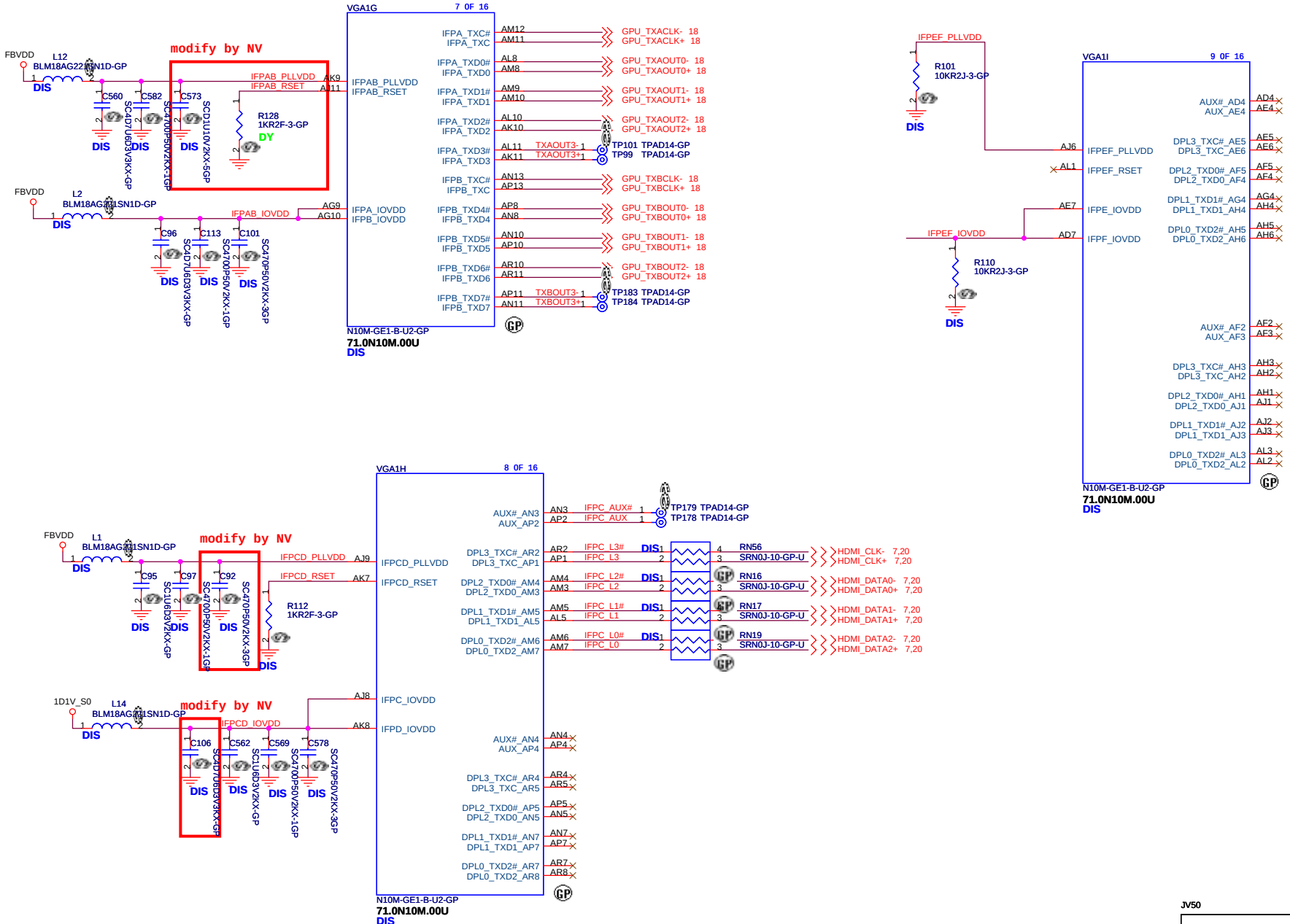
Title: ***N10M(3/6)_DAC***

Size	Document Number	Rev
A3	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 54 of 60



JV50

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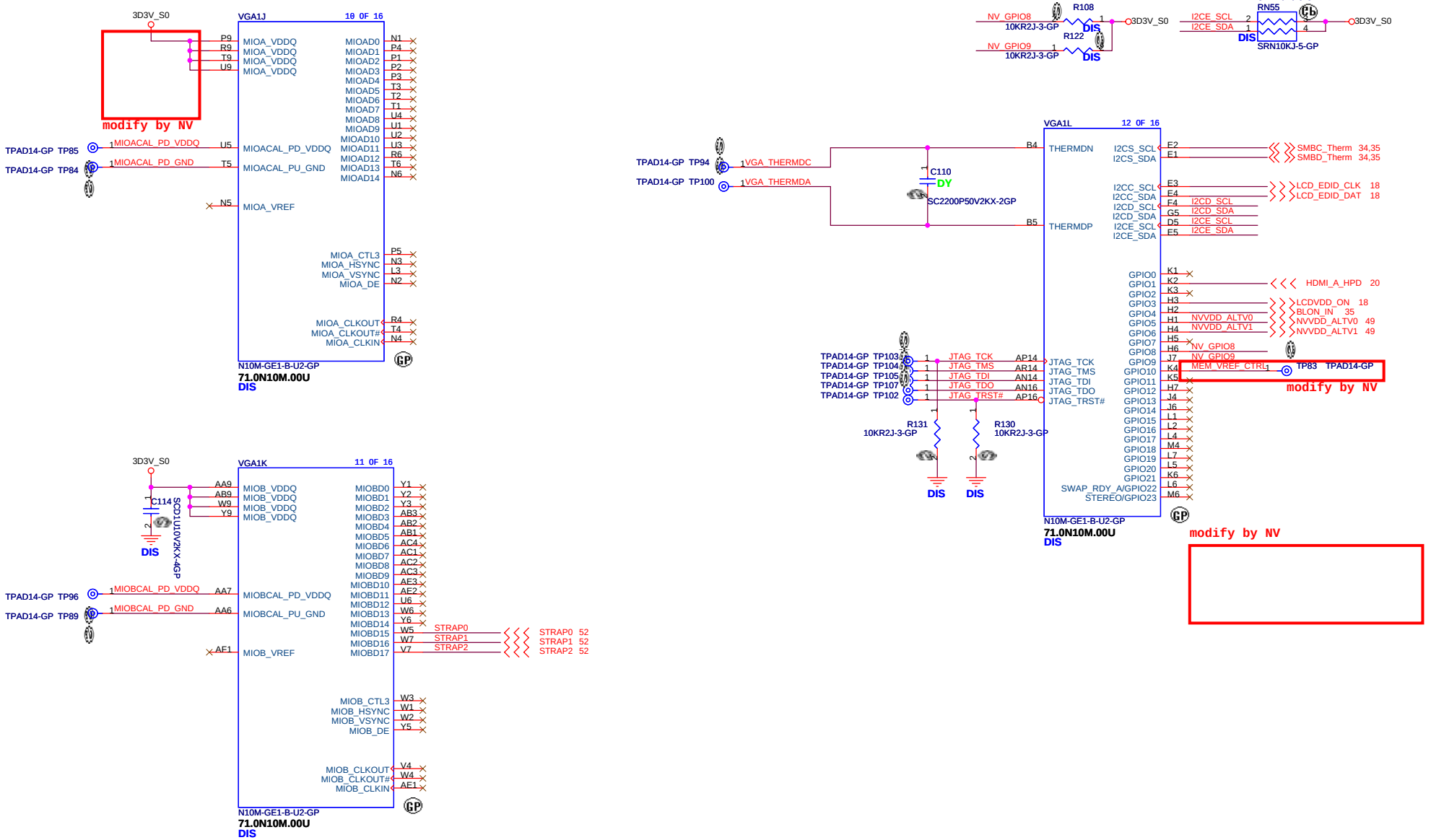
Title	***N10M(4/6)***
Size: A3	Document Number: **JV50**
Rev: SB	
Date: Tuesday, December 16, 2008	Sheet 55 of 60



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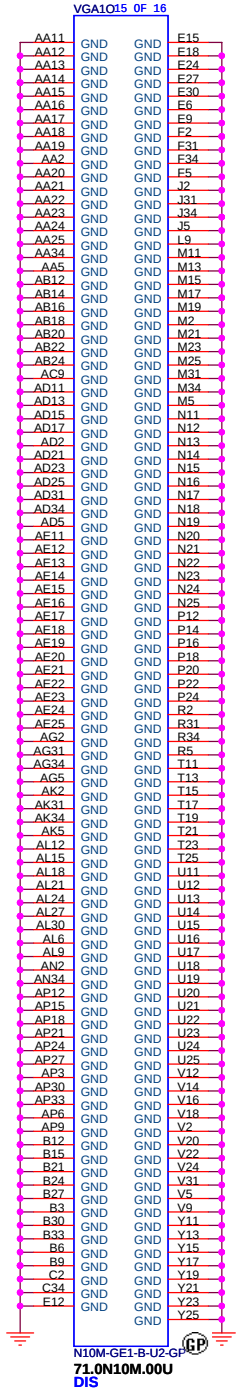
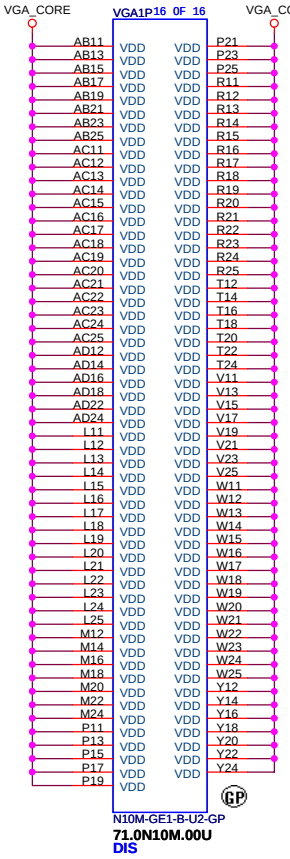
Taipei Hsien 221, Taiwan, R.O.C.

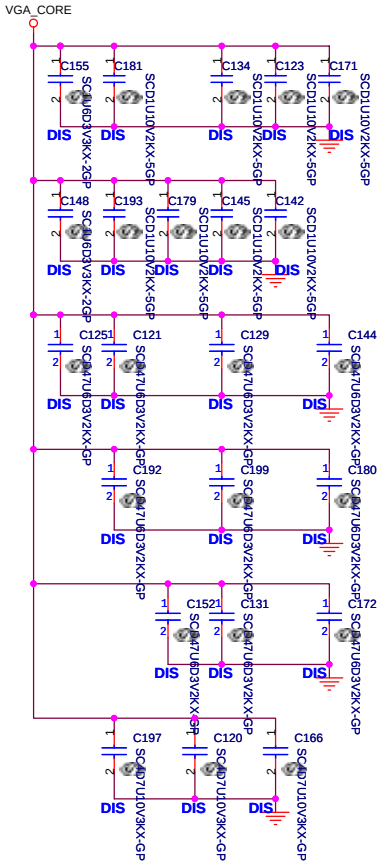
Title: ***N10M(5/6)_MIO/ GPIO***

Size	Document Number	Rev
A3	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 56 of 60







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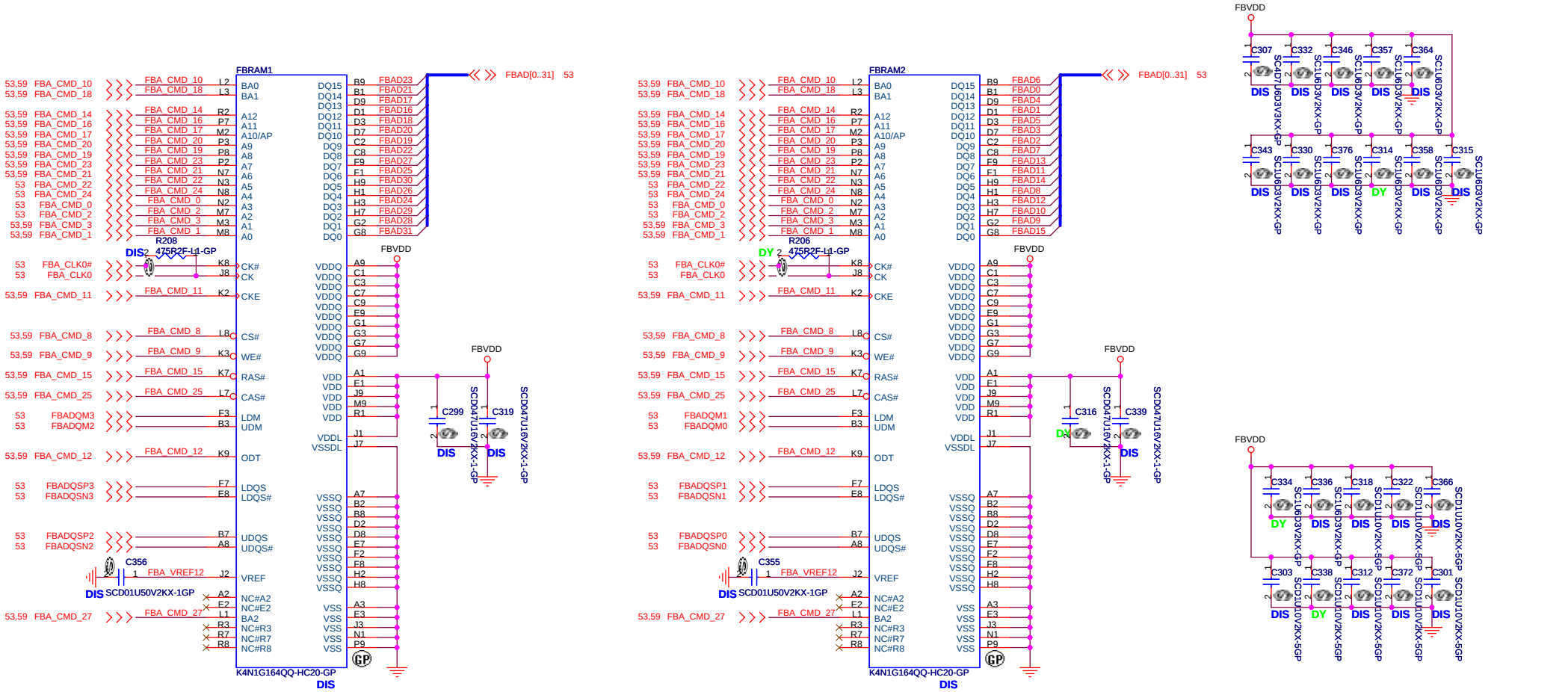
Taipei Hsien 221, Taiwan, R.O.C.

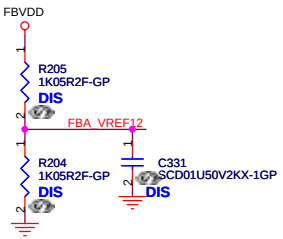
Title
N10M(6/6)_POWER

Size	Document Number	Rev
A3	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 57 of 60



modify by NV



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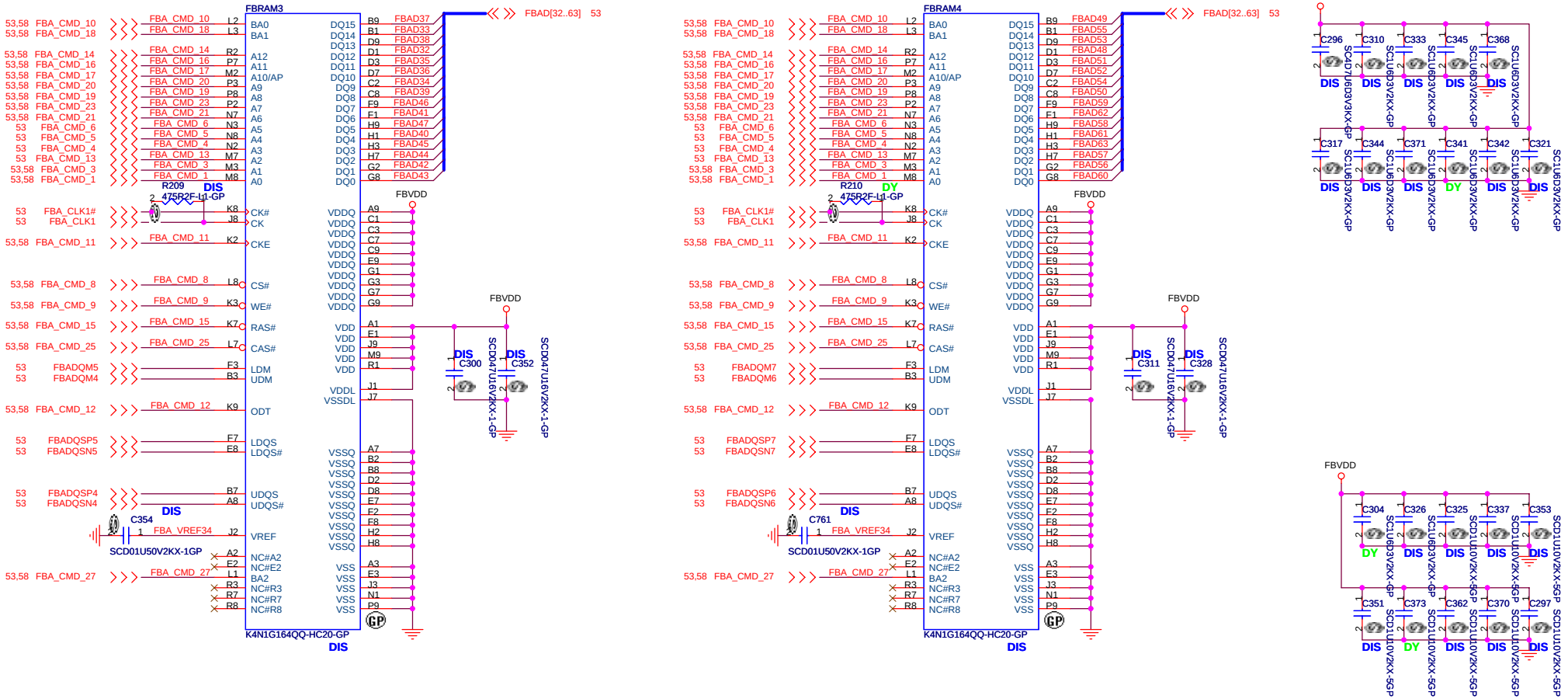
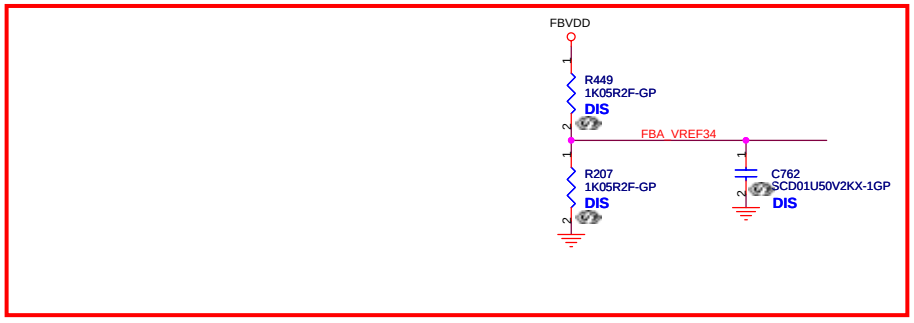
Title	***VRAM(1/2)***	
Size A3	Document Number **JV50**	Rev **SB**
Date: Tuesday, December 16, 2008	Sheet 58 of 60	



modify by NV



SB
All Component for NB9P-GE2

JV50

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Title: VRAM(2/2)

Size	Document Number	Rev
A3	JV50	SB

Date: Tuesday, December 16, 2008 Sheet 59 of 60

SB SB SC -1

12/02

Page3: change C452 C453 from 27P to 33P by vendor's request

Page33: add C872 33P for SIV

Page29: change SPKR_R1 SPKR_L1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page18: change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request

Page24: change USBCN1 from 20.F1290.015 to 20.F1035.015 by CE's request

Page38: change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request

Page18: change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page3: add R554 and change U24 pin16 from 3D3V_S0 to 3D3V_VDD48_S0

Page3: change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount

Page7: change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection

Page9: change C275 from UMA to DY and change C349 from mount to DY

Page10: change C243 C758 from mount to DY and change R167 R398 from DIS to DY

Page13: change R216 from 0ohm resistor to 0ohm pad

Page14: change C413 C252 C703 C392 C707 C734 from mount to DY

Page17: change C426 C429 from mount to DY

Page18: change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA

Page20: add RN86 for DIS HDMI SMbus

Page25: change R45 from 0ohm resistor to 0ohm pad

Page27: change R523 from 0ohm resistor to 0ohm pad

Page7: add R556 pull-low DY for A1 NB

Page28: change AGND & GND and change R509 from 0ohm resistor to 0ohm pad

Page28: change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2

Page28: combine C801 C802 two 1u to C801 4.7u

Page28: delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31

Page28: change R474 from DY to mount and change R475 from mount to DY for 10dB

Page29: add L29 L30 L31 L32 L33 L34 for ESD

Page31: change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad

Page32: change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad

Page12: change C385 C386 from 10p to 7p by vendor's request

Page35: change C136 C169 from 15p to 7p by vendor's request

Page33: change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY

Page34: change C42 from mount to DY

Page35: change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version

Page36: change DB1 from mount to DY

Page38: add Q35 PWR_LED7 PWR_LED8 and change RN4 from 4P2R to 8P4R and change PWR_LED5 PWR_LED6 from 83.01221.I70 to 83.00193.A70 for LED type

Page39: change U66 pin1 from CPUCORE_ON to 1D5V_PWRGD and change D13 pin1 from S5_ENABLE to 3V/5V_EN

Page40: update power sequence logic

Page41: change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad

Page42: change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap

Page43: change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap

Page43: change R246 pin2 from CPUCORE_ON to 1D5V_PWRGD and add R500 pull-high 10K 3D3V_S5

Page45: change G100-G109 from open gap to close gap

Page46: change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap

Page46: delete TC19 and change TC20 from DY to GFX

Page49: change G55-G67 G74-G77 from open gap to close gap

Page29: change RN75 from 47ohm to 75ohm

Page28: change C804 C807 from 4.7u to 1u 25V X5R

Page45: delete TC24

Page19: delete R104 R129

12/04

Page24: change U47 from 74.00545.A79 to 74.00547.A79

Page20: swap HDMI signals for routing

Page28: change U53 pin22 from AUD_HP1_EN to AMP_MUTE#_R

Page48: change BAT1 from 20.81094.007 to 20.81156.007

Page22: change ODD1 from 62.10065.541 to 62.10065.751

Page22: change R231 R247 from 0ohm resistor to 0ohm pad

12/05

Page25: change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad

Page46: change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request

Page41: change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request

Page41: change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request

Page45: change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request

12/08

Page26: change EC7 from DY to mount EMI's request

Page48: change EC28 EC30 EC31 EC32 from DY to mount EMI's request

Page31: change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request

Page5: change C79 C80 from DY to mount EMI's request

Page46: change C659 from DY to GFX EMI's request

Page50: change SPRING_GND16-SPRING_GND20 from DY to mount EMI's request

Page50: add EC61-EC67 0.1u by EMI's request

Page20: change R313 R314 from 10K 100K to 18K 47K by NV's request

Page35: change U14 pin83 RN65 pin2 from SHBM to DBC_EN by annie's request

Page18: change LCD1 pin35 from NC to DBC_EN by annie's request

Page20: add ER1-ER8 0ohm pad by EMI's request

Page10: change C636 from 1000p DY to 27p mount by RF's request

12/09

Page49: change R406 from 6K2 to 4K75 by power team's request

Page46: change TC16 from mount to GFX

Page50: add TC19 TC24 100u

Page41: change C528 C529 530 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY

Page46: change C656 C653 from 10u to 4.7u and change C653 from GFX to DY

Page42: change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY

Page41: change TC5 from DY to mount

Page5: change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount

Page17: change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount

Page16: change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount

Page20: change HDMI from 62.10078.161 to 62.10078.171 by CE's request

Page24: change USBCN1 from 20.F1035.015 to 20.F1290.015 by CE's request

12/10

Page46: add C873 33p GFX by RF's request

Page43: add C874 C875 33p by RF's request

Page20: swap U8 pin13 14 47 48

Page33: change R16 from DY to mount

Page47: change R292 from 0ohm resistor to 0ohm pad

12/11

Page33: change MINI2 pin 51 from 5V_S5_MIN1 to 5V_S5_MIN2

12/15

Page52: change VRAM strap R350

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

Size: A2 | Document Number: JV50 | Rev: SB

Date: Tuesday, December 16, 2008 | Sheet 60 of 60