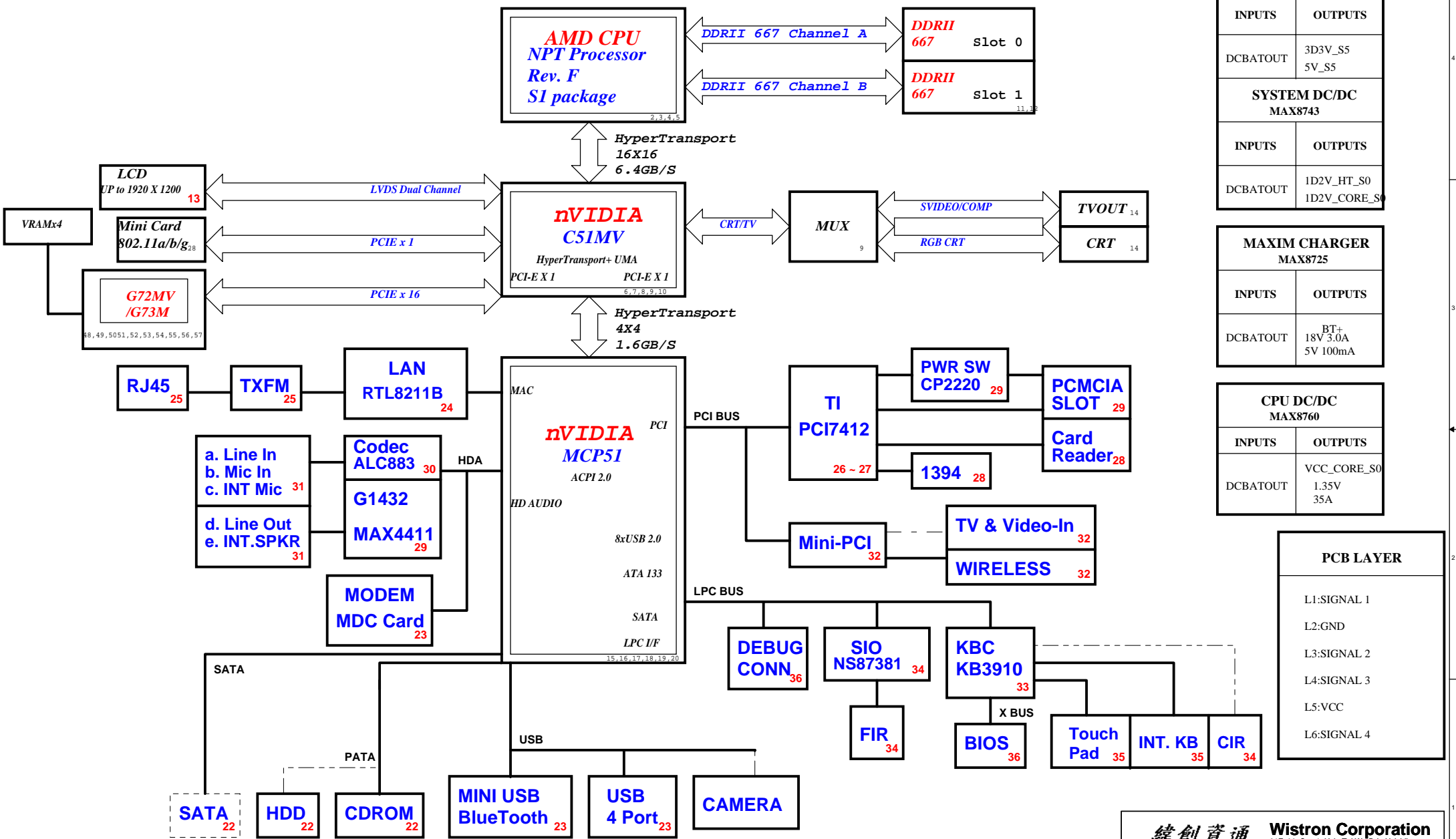


MYALL M Block Diagram

Project Code: 91.4Q901.001
 Project Name: MYALL M
 PCB Number: 06211-SA



| SYSTEM DC/DC MAX8734A | |
|--------------------------|------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 3D3V_S5 5V_S5 |

| SYSTEM DC/DC MAX8743 | |
|-------------------------|----------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D2V_HT_S0 1D2V_CORE_S0 |

| MAXIM CHARGER MAX8725 | |
|--------------------------|-----------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | BT+ 18V 3.0A 5V 100mA |

| CPU DC/DC MAX8760 | |
|----------------------|-----------------------------|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE_S0 1.35V 35A |

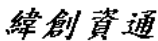
| PCB LAYER |
|--------------|
| L1: SIGNAL 1 |
| L2: GND |
| L3: SIGNAL 2 |
| L4: SIGNAL 3 |
| L5: VCC |
| L6: SIGNAL 4 |

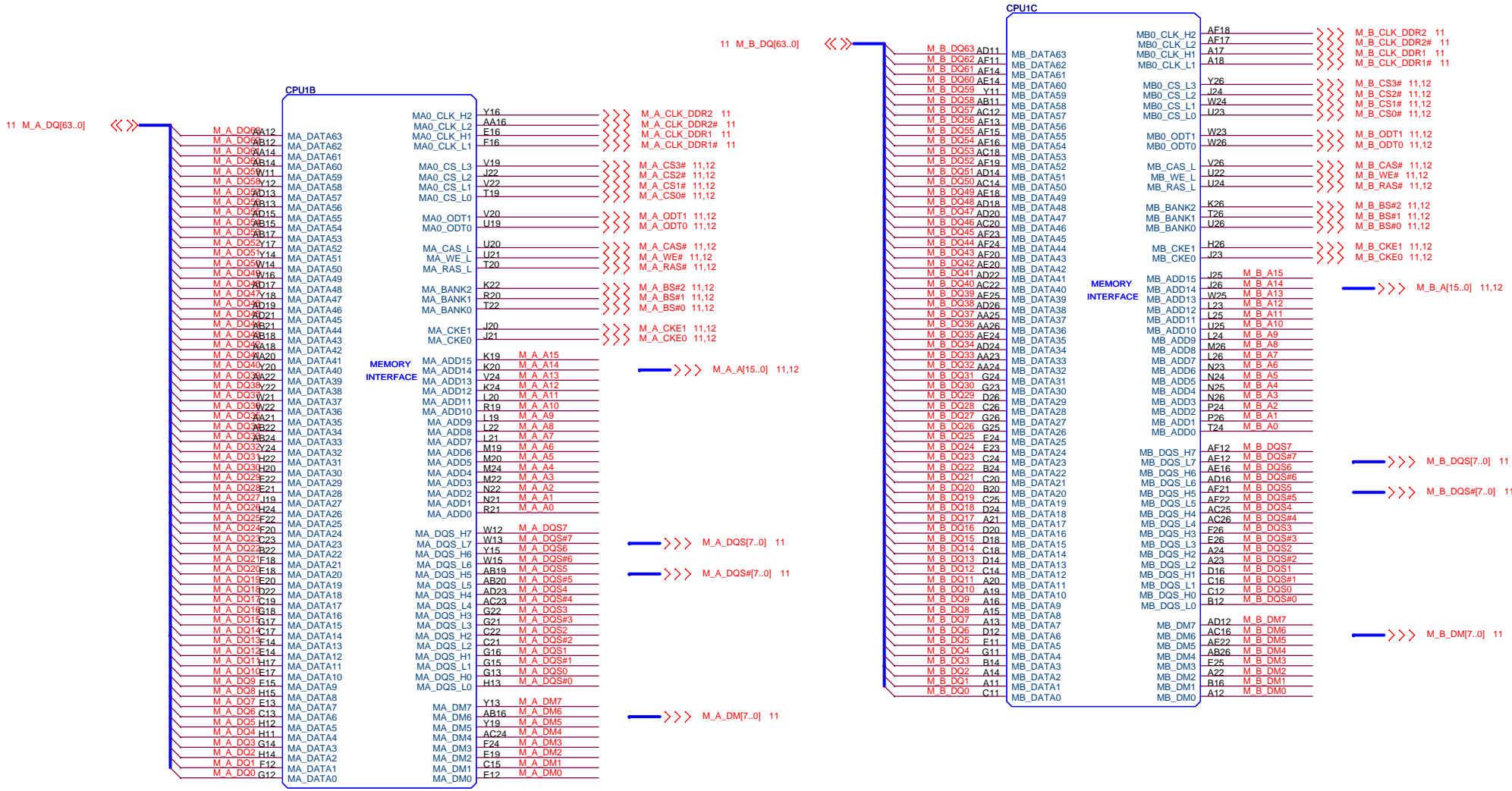
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|-------------------------------|-----------------------------------|------------------|
| Title Block Diagram | | Rev SA |
| Size Custort | Document Number MYALL M | |
| Date: Friday, June 16, 2006 | Sheet 1 of | 59 |

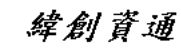


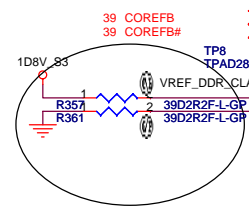
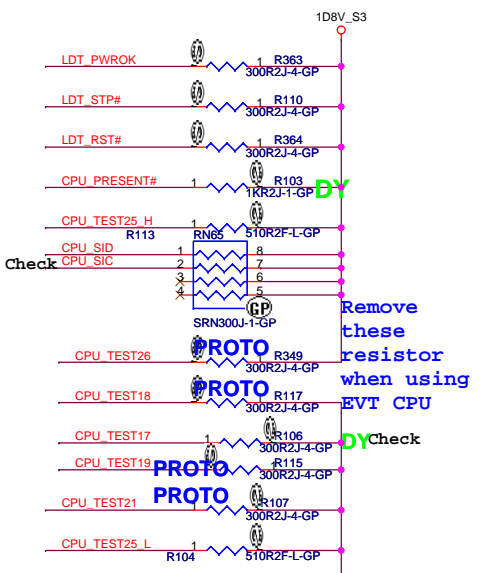
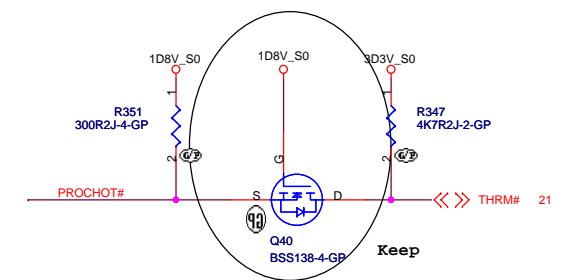
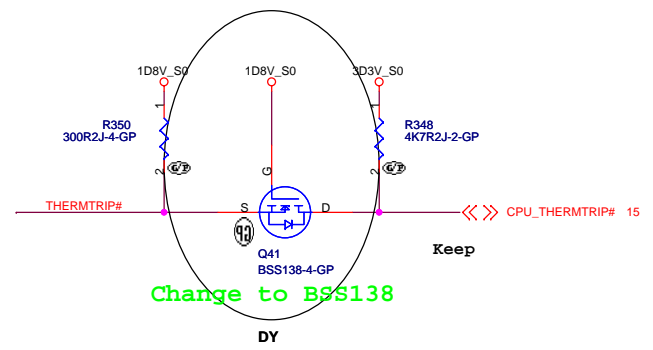
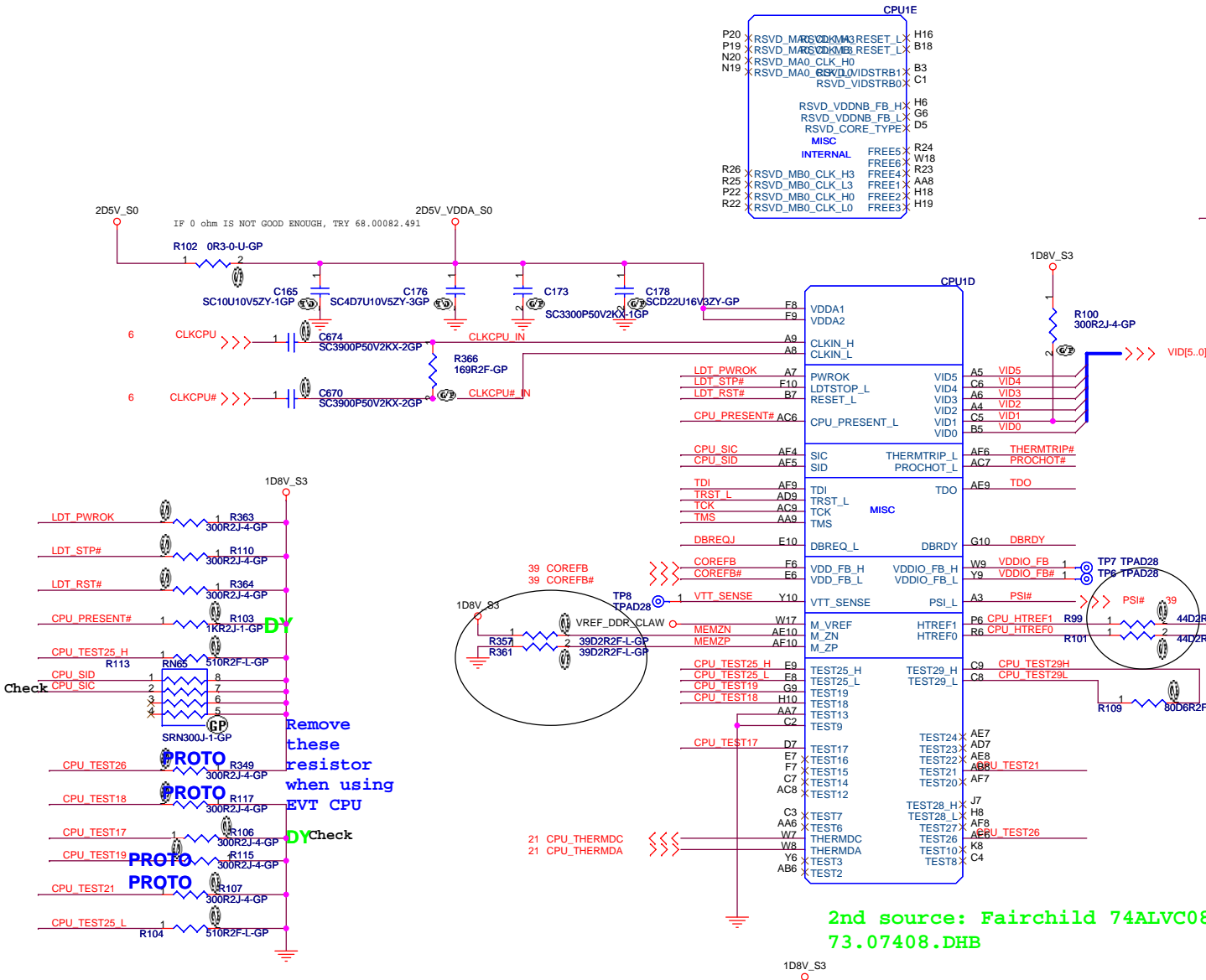
<Variant Name>

| | | |
|---|-----------------------|---------------|
|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| File CPU(1/4) HT | | |
| Size | Document Number | Rev |
| A3 | MYALL M | SA |
| Date: | Friday, June 16, 2006 | Sheet 2 of 59 |



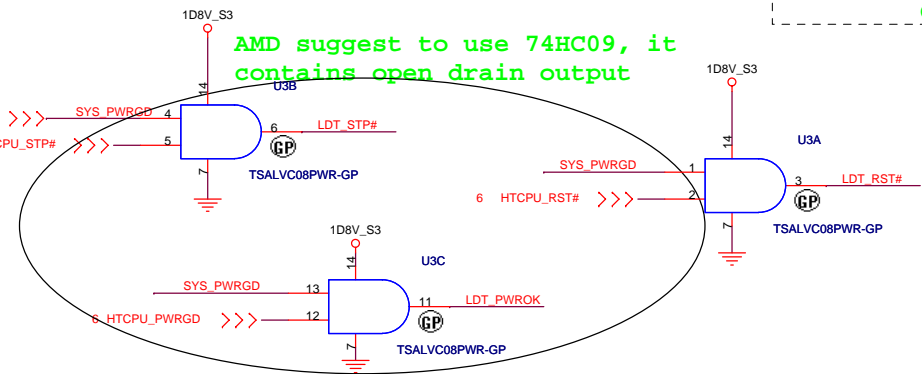
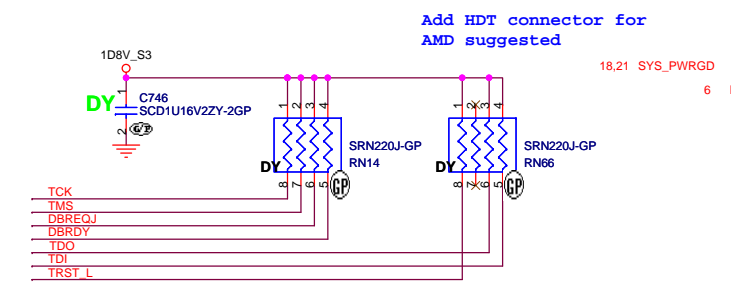
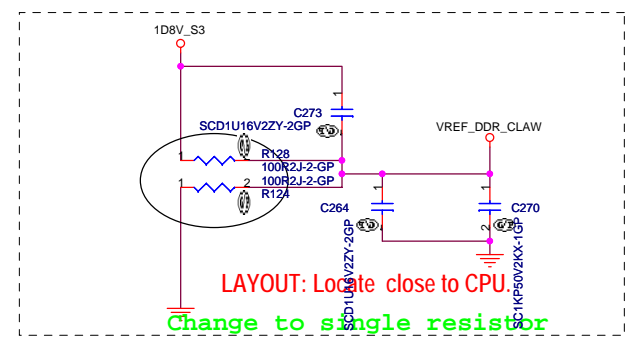
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| | |
|---|-----------------------------------|
|  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| CPU(2/4) DDR II | |
| Size A3 | Document Number MYALL M |
| Date: Friday, June 16, 2006 | Sheet 3 of 59 |



2nd source: Fairchild 74ALVC08 73.07408.DHB

AMD suggest to use 74HC09, it contains open drain output



<Variant Name>

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Title: **CPU(3/4) CONTROL**

Size: A3 Document Number: **MYALL M** Rev: **SA**

Date: Friday, June 16, 2006 Sheet: 4 of 59

CPUCADOUT[15..0] 2
CPUCADOUTJ[15..0] 2

U34F

6 OF 6

NB0CADOUT[15..0] 2
NB0CADOUTJ[15..0] 2

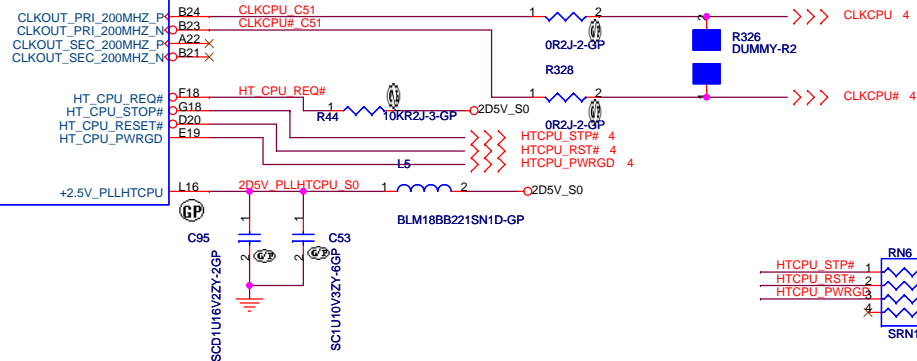
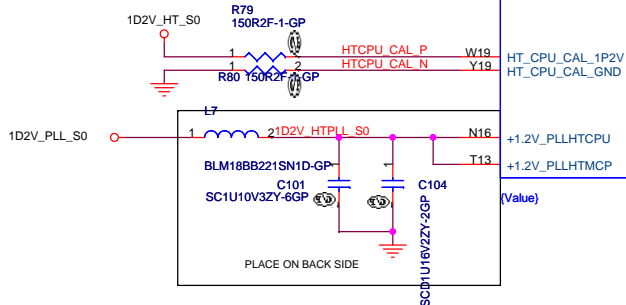
| | | | | | |
|--------------|-----|----------------|----------------|-----|--------------|
| CPUCADOUT0 | Y23 | HT_CPU_RXD0_P | HT_CPU_TXD0_P | C23 | NB0CADOUT0 |
| CPUCADOUT1 | W24 | HT_CPU_RXD1_P | HT_CPU_TXD1_P | D23 | NB0CADOUT1 |
| CPUCADOUT2 | V24 | HT_CPU_RXD2_P | HT_CPU_TXD2_P | E22 | NB0CADOUT2 |
| CPUCADOUT3 | U22 | HT_CPU_RXD3_P | HT_CPU_TXD3_P | F23 | NB0CADOUT3 |
| CPUCADOUT4 | R24 | HT_CPU_RXD4_P | HT_CPU_TXD4_P | H22 | NB0CADOUT4 |
| CPUCADOUT5 | P24 | HT_CPU_RXD5_P | HT_CPU_TXD5_P | J21 | NB0CADOUT5 |
| CPUCADOUT6 | P22 | HT_CPU_RXD6_P | HT_CPU_TXD6_P | K21 | NB0CADOUT6 |
| CPUCADOUT7 | N22 | HT_CPU_RXD7_P | HT_CPU_TXD7_P | K23 | NB0CADOUT7 |
| CPUCADOUT8 | Y21 | HT_CPU_RXD8_P | HT_CPU_TXD8_P | D21 | NB0CADOUT8 |
| CPUCADOUT9 | V21 | HT_CPU_RXD9_P | HT_CPU_TXD9_P | F21 | NB0CADOUT9 |
| CPUCADOUT10 | W21 | HT_CPU_RXD10_P | HT_CPU_TXD10_P | G20 | NB0CADOUT10 |
| CPUCADOUT11 | T21 | HT_CPU_RXD11_P | HT_CPU_TXD11_P | J19 | NB0CADOUT11 |
| CPUCADOUT12 | R18 | HT_CPU_RXD12_P | HT_CPU_TXD12_P | L17 | NB0CADOUT12 |
| CPUCADOUT13 | P16 | HT_CPU_RXD13_P | HT_CPU_TXD13_P | L17 | NB0CADOUT13 |
| CPUCADOUT14 | N20 | HT_CPU_RXD14_P | HT_CPU_TXD14_P | L20 | NB0CADOUT14 |
| CPUCADOUT15 | M17 | HT_CPU_RXD15_P | HT_CPU_TXD15_P | L18 | NB0CADOUT15 |
| CPUCADOUTJ0 | Y22 | HT_CPU_RXD0_N | HT_CPU_TXD0_N | C24 | NB0CADOUTJ0 |
| CPUCADOUTJ1 | W23 | HT_CPU_RXD1_N | HT_CPU_TXD1_N | D24 | NB0CADOUTJ1 |
| CPUCADOUTJ2 | V23 | HT_CPU_RXD2_N | HT_CPU_TXD2_N | E23 | NB0CADOUTJ2 |
| CPUCADOUTJ3 | U21 | HT_CPU_RXD3_N | HT_CPU_TXD3_N | F24 | NB0CADOUTJ3 |
| CPUCADOUTJ4 | R23 | HT_CPU_RXD4_N | HT_CPU_TXD4_N | H23 | NB0CADOUTJ4 |
| CPUCADOUTJ5 | P23 | HT_CPU_RXD5_N | HT_CPU_TXD5_N | J22 | NB0CADOUTJ5 |
| CPUCADOUTJ6 | P24 | HT_CPU_RXD6_N | HT_CPU_TXD6_N | K22 | NB0CADOUTJ6 |
| CPUCADOUTJ7 | N24 | HT_CPU_RXD7_N | HT_CPU_TXD7_N | K24 | NB0CADOUTJ7 |
| CPUCADOUTJ8 | Y20 | HT_CPU_RXD8_N | HT_CPU_TXD8_N | D22 | NB0CADOUTJ8 |
| CPUCADOUTJ9 | W20 | HT_CPU_RXD9_N | HT_CPU_TXD9_N | E20 | NB0CADOUTJ9 |
| CPUCADOUTJ10 | W22 | HT_CPU_RXD10_N | HT_CPU_TXD10_N | E21 | NB0CADOUTJ10 |
| CPUCADOUTJ11 | U20 | HT_CPU_RXD11_N | HT_CPU_TXD11_N | G19 | NB0CADOUTJ11 |
| CPUCADOUTJ12 | R19 | HT_CPU_RXD12_N | HT_CPU_TXD12_N | J18 | NB0CADOUTJ12 |
| CPUCADOUTJ13 | P17 | HT_CPU_RXD13_N | HT_CPU_TXD13_N | K17 | NB0CADOUTJ13 |
| CPUCADOUTJ14 | N19 | HT_CPU_RXD14_N | HT_CPU_TXD14_N | K19 | NB0CADOUTJ14 |
| CPUCADOUTJ15 | N18 | HT_CPU_RXD15_N | HT_CPU_TXD15_N | L19 | NB0CADOUTJ15 |

2 CPUHTTCLKOUT0 >>> CPUHTTCLKOUT0 T23 HT_CPU_RX_CLK0_P
2 CPUHTTCLKOUTJ0 >>> CPUHTTCLKOUTJ0 T22 HT_CPU_TX_CLK0_N
2 CPUHTTCLKOUT1 >>> CPUHTTCLKOUT1 R21 HT_CPU_RX_CLK1_P
2 CPUHTTCLKOUTJ1 >>> CPUHTTCLKOUTJ1 R20 HT_CPU_TX_CLK1_N

2 NB0HTTCLKOUT0 >>> NB0HTTCLKOUT0 G23 HT_CPU_TX_CLK0_P
2 NB0HTTCLKOUTJ0 >>> NB0HTTCLKOUTJ0 G24 HT_CPU_TX_CLK0_N
2 NB0HTTCLKOUT1 >>> NB0HTTCLKOUT1 G22 HT_CPU_TX_CLK1_P
2 NB0HTTCLKOUTJ1 >>> NB0HTTCLKOUTJ1 G21 HT_CPU_TX_CLK1_N

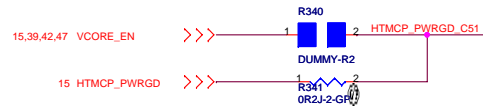
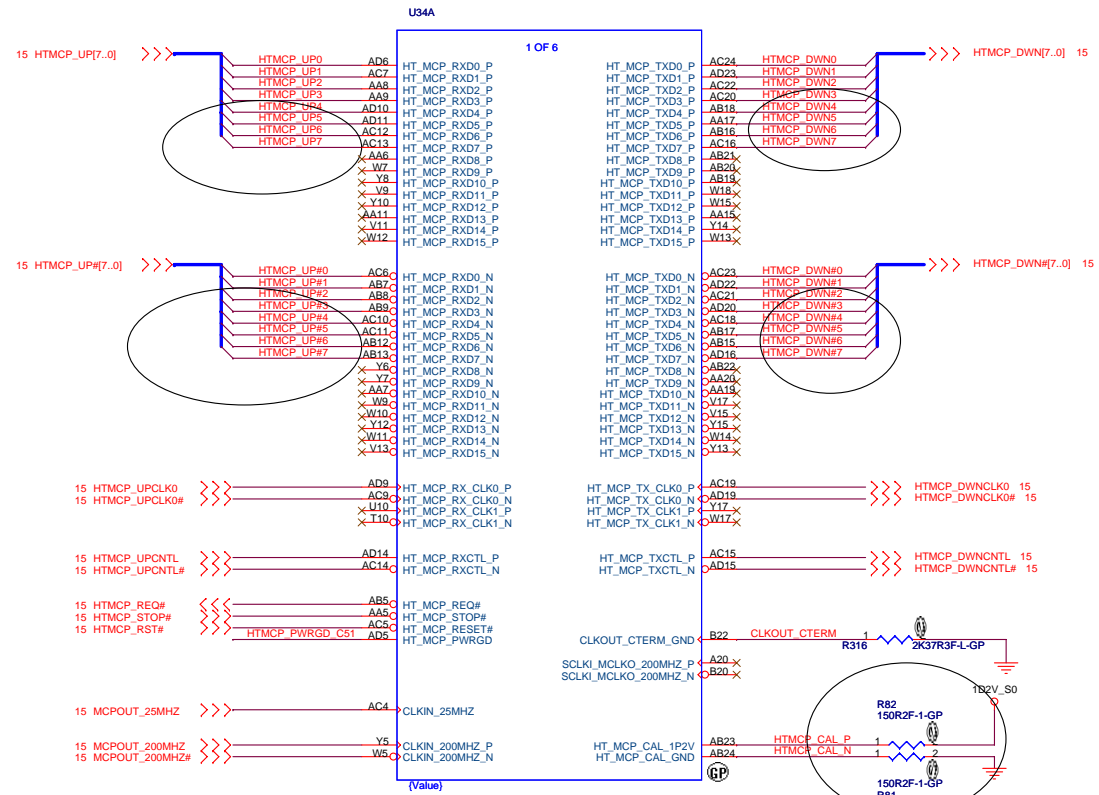
2 CPUHTTCTL0 >>> CPUHTTCTL0 M23 HT_CPU_RXCTL_P
2 CPUHTTCTL0J0 >>> CPUHTTCTL0J0 M22 HT_CPU_RXCTL_N

2 NB0HTTCTL0 >>> NB0HTTCTL0 L23 HT_CPU_TXCTL_P
2 NB0HTTCTL0J0 >>> NB0HTTCTL0J0 L24 HT_CPU_TXCTL_N



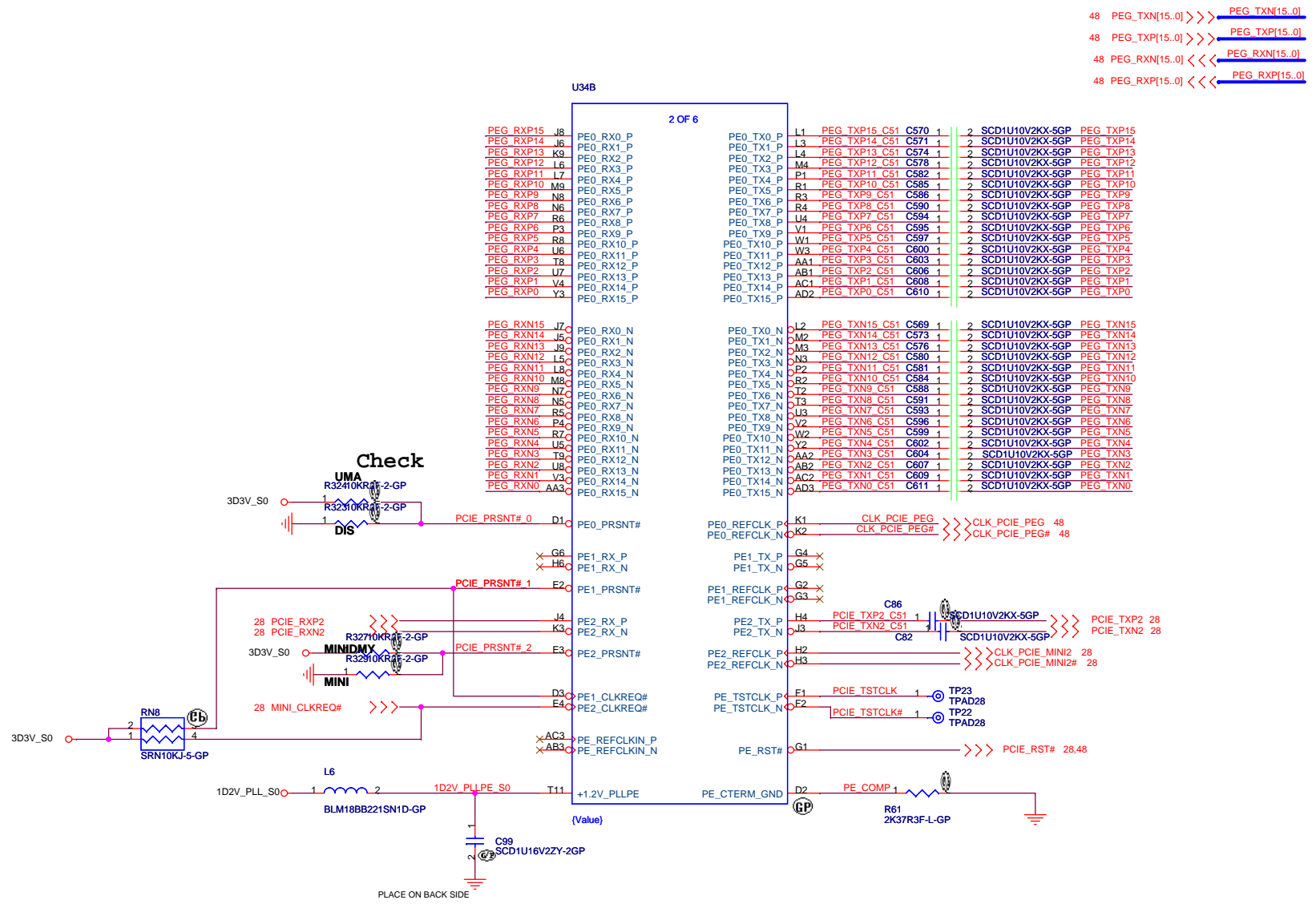
<Variant Name>

| | |
|---|--|
| | |
| Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| File C51M(1/5) HT CPU | |
| Size A3 | Document Number MYALL M |
| Date: Friday, June 16, 2006 | Rev SA |
| Sheet 6 of 59 | |



<Variant Name>

| | | | |
|--|-----------------|----------------------------|-----------|
| 緯創資通 | | Wistron Corporation | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | | |
| Title C51M(2/5)HT MCP | | | |
| Size | Document Number | | Rev |
| Customer | MYALL M | | SA |
| Date: Friday, June 16, 2006 | Sheet 7 of | | 59 |



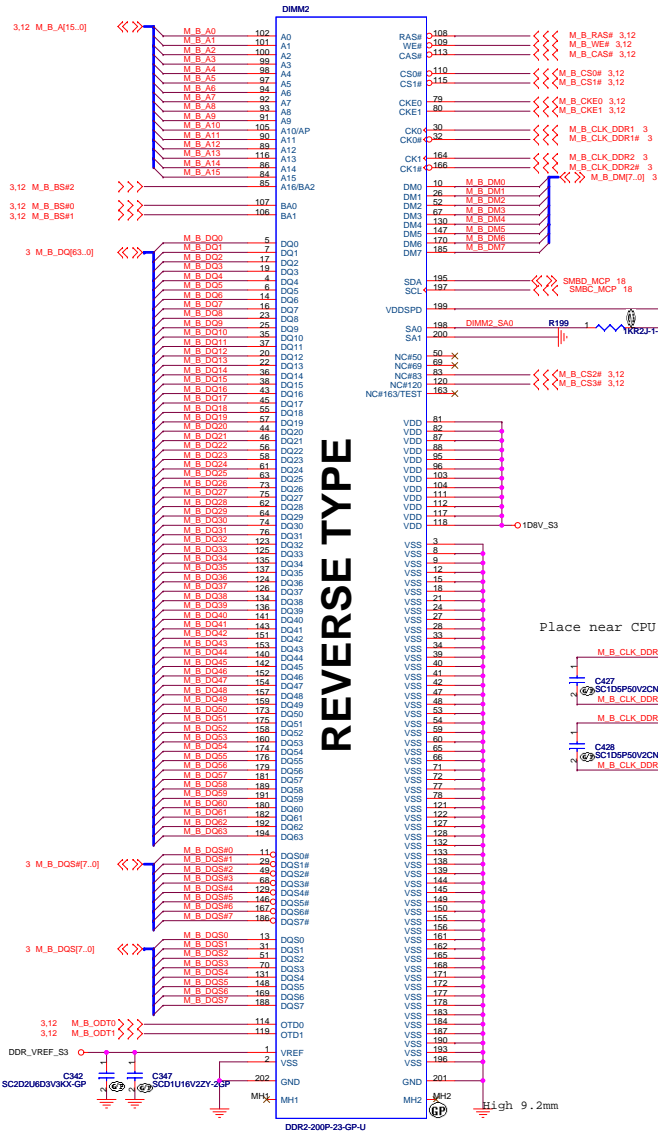
48 PEG_TXN[15..0] >>> PEG_TXN[15..0]
 48 PEG_TXP[15..0] >>> PEG_TXP[15..0]
 48 PEG_RXN[15..0] <<< PEG_RXN[15..0]
 48 PEG_RXP[15..0] <<< PEG_RXP[15..0]

Check

PLACE ON BACK SIDE

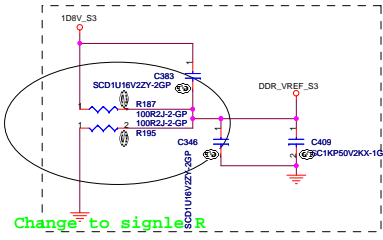
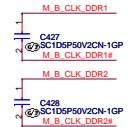
<Variant Name>

| | |
|---|-----------------|
| Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | |
| C51M(3/5)PCIE | |
| Size | Document Number |
| A3 | MYALL M |
| Date: Friday, June 16, 2006 | Sheet 8 of 59 |
| Rev | SA |

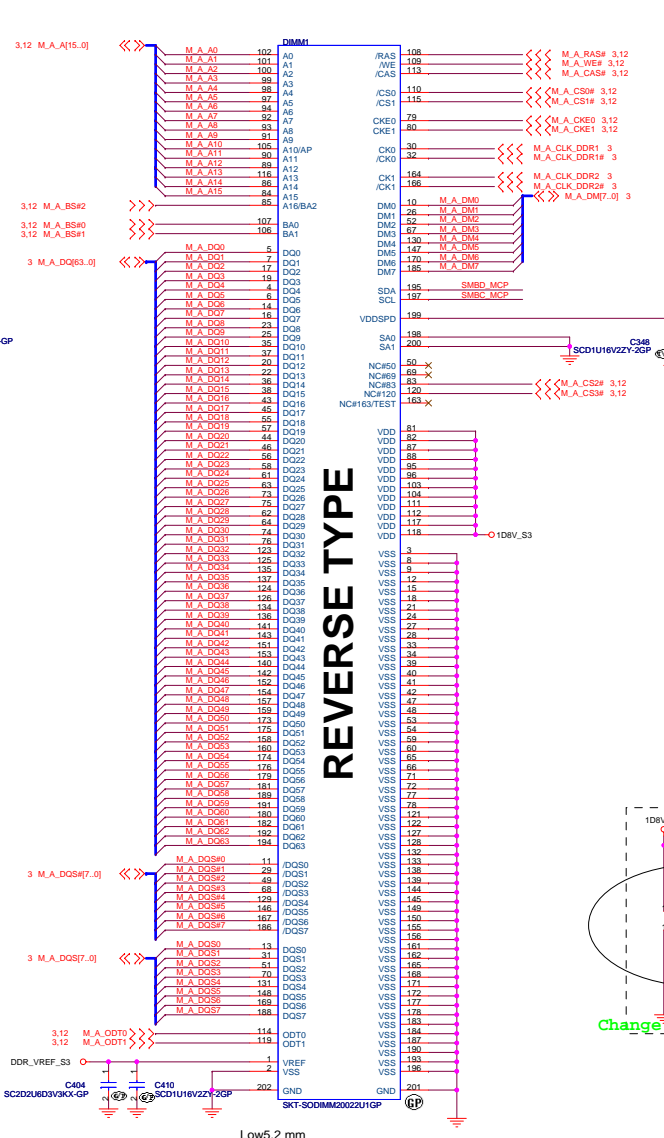


REVERSE TYPE

Place near CPU

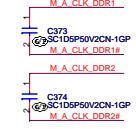


Change to signal
LAYOUT: Locate close to DIMM



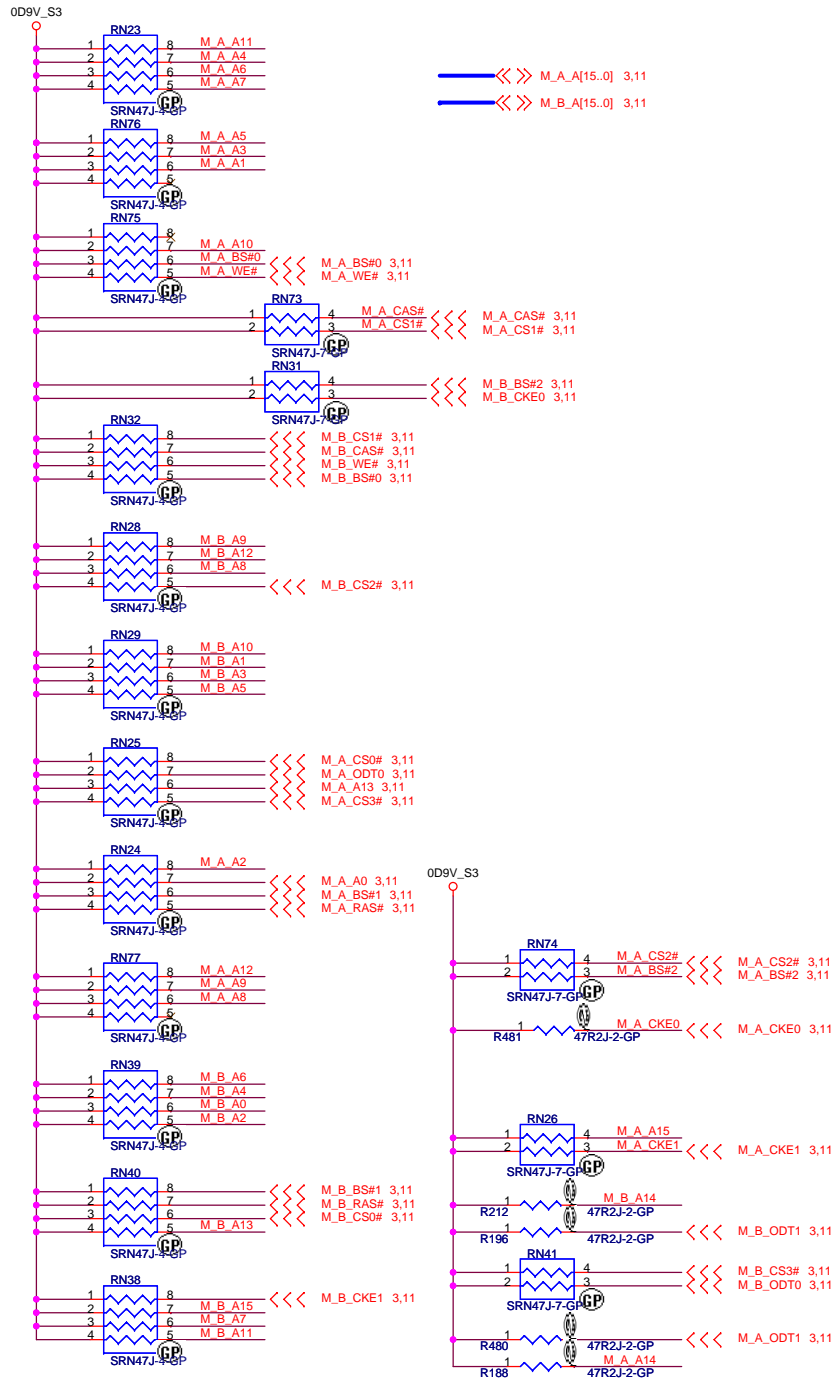
REVERSE TYPE

Place near CPU



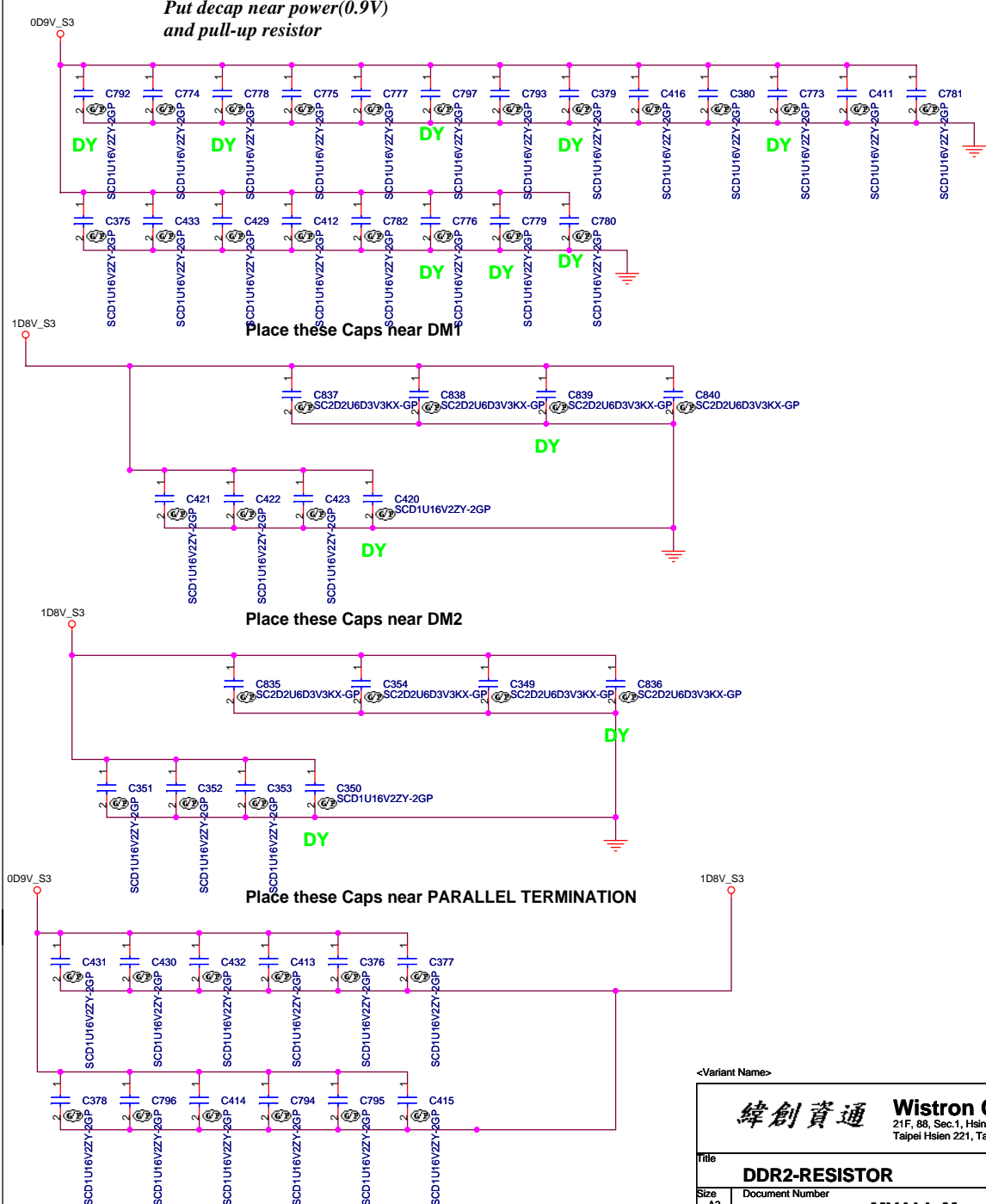
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



<Variant Name>

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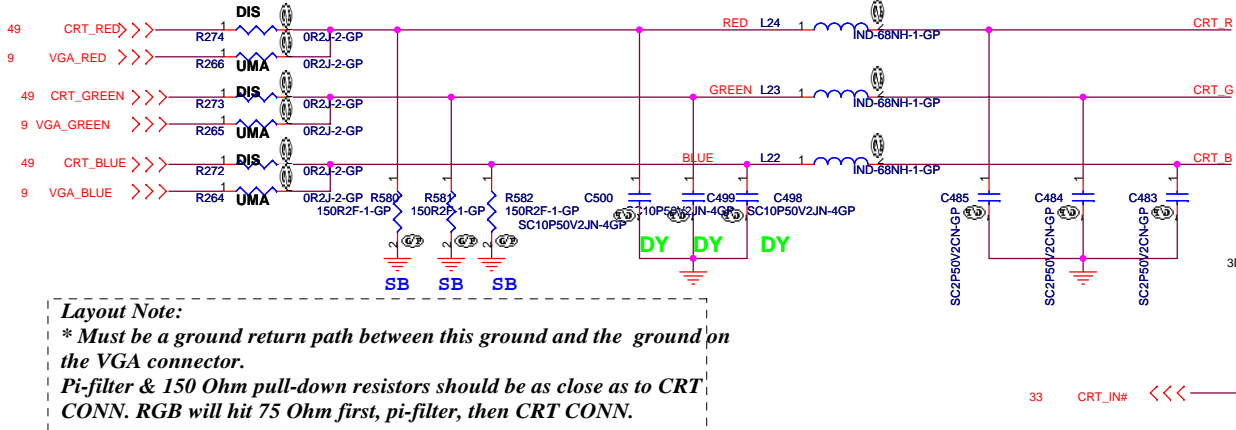
Title: **DDR2-RESISTOR**

Size: A3 Document Number: **MYALL M** Rev: **SA**

Date: Friday, June 16, 2006 Sheet 12 of 59

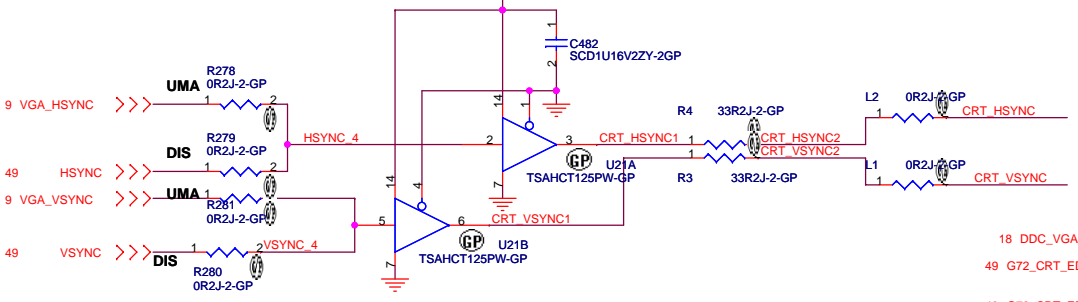
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

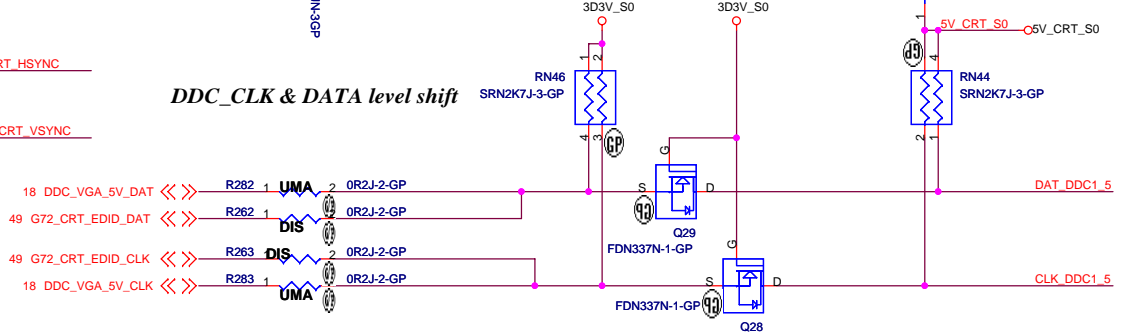


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

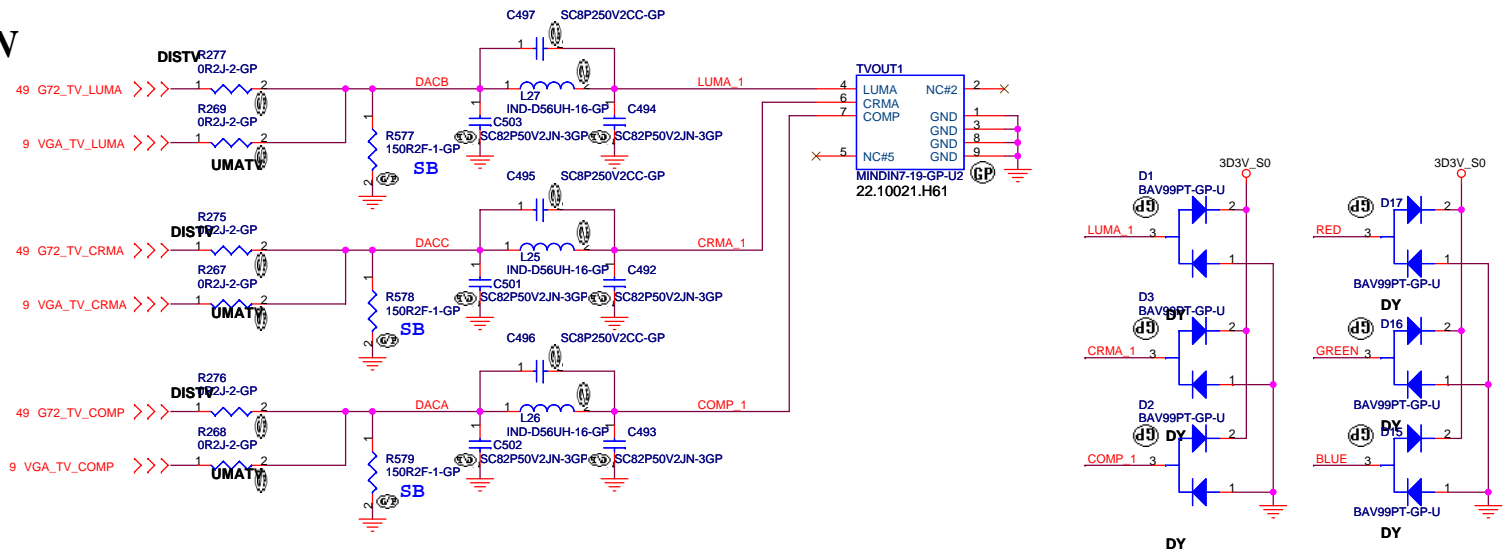
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV CONN



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Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|-----------------------------|-----------------|------------------|-------|
| Title | | CRT/TV Connector | |
| Size | Document Number | Rev | SA |
| Date: Friday, June 16, 2006 | | Sheet 14 | of 59 |

26,27,32 PCI_AD[31..0] <<<

U59A

1 OF 7

| | | |
|----------|------|----------|
| PCI_AD0 | AF19 | PCI_AD0 |
| PCI_AD1 | AB21 | PCI_AD1 |
| PCI_AD2 | AC19 | PCI_AD2 |
| PCI_AD3 | AA20 | PCI_AD3 |
| PCI_AD4 | AA19 | PCI_AD4 |
| PCI_AD5 | AE20 | PCI_AD5 |
| PCI_AD6 | AE19 | PCI_AD6 |
| PCI_AD7 | AE20 | PCI_AD7 |
| PCI_AD8 | AB20 | PCI_AD8 |
| PCI_AD9 | AB19 | PCI_AD9 |
| PCI_AD10 | AA18 | PCI_AD10 |
| PCI_AD11 | AB18 | PCI_AD11 |
| PCI_AD12 | AE18 | PCI_AD12 |
| PCI_AD13 | AE18 | PCI_AD13 |
| PCI_AD14 | AC17 | PCI_AD14 |
| PCI_AD15 | AA17 | PCI_AD15 |
| PCI_AD16 | AB15 | PCI_AD16 |
| PCI_AD17 | AE15 | PCI_AD17 |
| PCI_AD18 | AE15 | PCI_AD18 |
| PCI_AD19 | AE14 | PCI_AD19 |
| PCI_AD20 | AE14 | PCI_AD20 |
| PCI_AD21 | AA14 | PCI_AD21 |
| PCI_AD22 | AB14 | PCI_AD22 |
| PCI_AD23 | AC13 | PCI_AD23 |
| PCI_AD24 | AB13 | PCI_AD24 |
| PCI_AD25 | AE13 | PCI_AD25 |
| PCI_AD26 | AA12 | PCI_AD26 |
| PCI_AD27 | AF13 | PCI_AD27 |
| PCI_AD28 | AB12 | PCI_AD28 |
| PCI_AD29 | AE12 | PCI_AD29 |
| PCI_AD30 | AE12 | PCI_AD30 |
| PCI_AD31 | AE11 | PCI_AD31 |

| | | | |
|-----------|------|-----------|----|
| PCI_REQ#0 | AA22 | PCI_REQ#0 | 27 |
| PCI_REQ#1 | AE22 | PCI_REQ#1 | 32 |
| PCI_REQ#2 | AE21 | PCI_REQ#2 | |
| PCI_REQ#3 | AE22 | PCI_REQ#3 | |
| PCI_REQ#4 | AE23 | PCI_REQ#4 | |

| | | | |
|-----------|------|-----------|----|
| PCI_GNT#0 | AE21 | PCI_GNT#0 | 27 |
| PCI_GNT#1 | AC21 | PCI_GNT#1 | 32 |
| PCI_GNT#2 | AE21 | PCI_GNT#2 | |
| PCI_GNT#3 | AB24 | PCI_GNT#3 | |
| PCI_GNT#4 | AB22 | PCI_GNT#4 | |

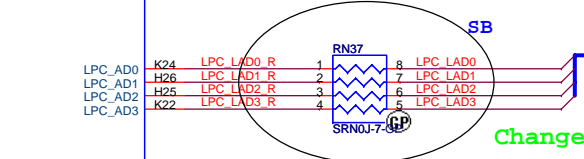
| | | | |
|-----------|------|------------|----|
| PCI_INTW# | AE11 | INT_PIRQW# | 27 |
| PCI_INTX# | AB11 | INT_PIRQX# | 32 |
| PCI_INTY# | AC11 | INT_PIRQY# | 27 |
| PCI_INTZ# | AA11 | INT_PIRQZ# | 27 |

| | | | | | | |
|-----------|------|-----------|--------|------------|-----------|----|
| PCI_CLK#0 | AE24 | PCI_CLK_0 | R498 | 22R2J-2-GP | PCLK_PCM | 27 |
| PCI_CLK#1 | AF24 | PCI_CLK_1 | R497 | 22R2J-2-GP | PCLK_MINI | 32 |
| PCI_CLK#2 | AD23 | PCI_CLK_2 | TP45 | | | |
| PCI_CLK#3 | AE23 | PCI_CLK_3 | TPAD28 | | | |
| PCI_CLK#4 | AB23 | PCI_CLK_4 | R198 | 22R2J-2-GP | | |
| PCI_CLKIN | AC23 | PCI_CLKIN | | | | |

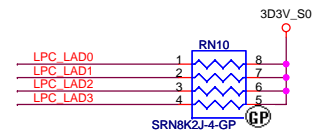
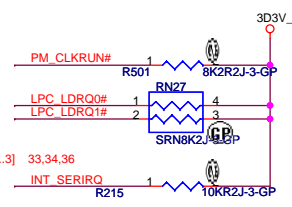
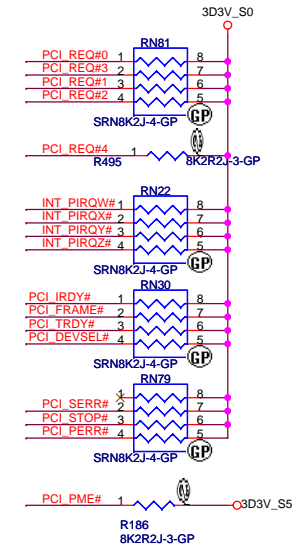
| | | |
|------------------|-------|-----------|
| 26,32 PCI_C/BE#0 | AD19C | PCI_CBE#0 |
| 26,32 PCI_C/BE#1 | AB17C | PCI_CBE#1 |
| 26,32 PCI_C/BE#2 | AA15C | PCI_CBE#2 |
| 26,32 PCI_C/BE#3 | AA13C | PCI_CBE#3 |

| | | |
|------------------------|-------|------------------|
| 27,32 PCI_FRAME# | AC15C | PCI_FRAME# |
| 27,32 PCI_IRDY# | AD15C | PCI_IRDY# |
| 27,32 PCI_TRDY# | AB16C | PCI_TRDY# |
| 27,32 PCI_STOP# | AE16C | PCI_STOP# |
| 27,32 PCI_DEVSEL# | AA16C | PCI_DEVSEL# |
| 26,32 PCI_PAR | AE17 | PCI_PAR |
| 27,32 PCI_PERR# | AF16C | PCI_PERR# |
| 27,32 PCI_SERR# | AF17C | PCI_SERR# |
| 27,32,33,34 PM_CLKRUN# | AD11C | PCI_PME# |
| | AE25C | PCI_CLKRUN#/GPIO |

| | | | |
|-------------------|----------------|-------|--------------|
| 29 PCIRST#_PCM | PCIRST#_R | AE25C | PCIRST#_PCM |
| 22 PCIRST#_IDE | PCIRST#_IDE_R | AD24C | PCIRST#_IDE |
| 32 PCIRST#_MINI | PCIRST#_MINI_R | AE26C | PCIRST#_MINI |
| 27 PCIRST#_CARD | PCIRST#_CARD_R | AE22C | PCIRST#_CARD |
| 33,34,36 LPC_RST# | LPC_RST#_R | L26C | LPC_RST# |



| | | | | | | |
|------------------|------|-------------|-------------|------------|----------|----|
| LPC_FRAME# | G25 | LPC_LFRAME# | 33,34,36 | | | |
| LPC_DRQ#0 | K21 | LPC_LDRQ0# | 34 | | | |
| LPC_DRQ#1 | K23 | LPC_LDRQ1# | | | | |
| LPC_SERIRQ | L22 | INT_SERIRQ | 27,32,33,34 | | | |
| LPC_PWRDWN#/GPIO | H24 | PSW_CLR# | 36 | | | |
| LPC_CLK#0 | F26 | LPC_CLK_R | EMI-SB | PCLK_KBC | 33 | |
| LPC_CLK#1 | G26 | LPC_CLK1_R | R531 | 22R2J-2-GP | PCLK_SIO | 34 |
| | R496 | 22R2J-2-GP | | PCLK_FWH | 36 | |



Check ! Shiba don't have this

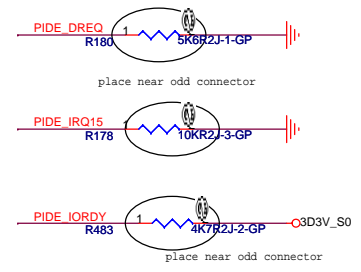
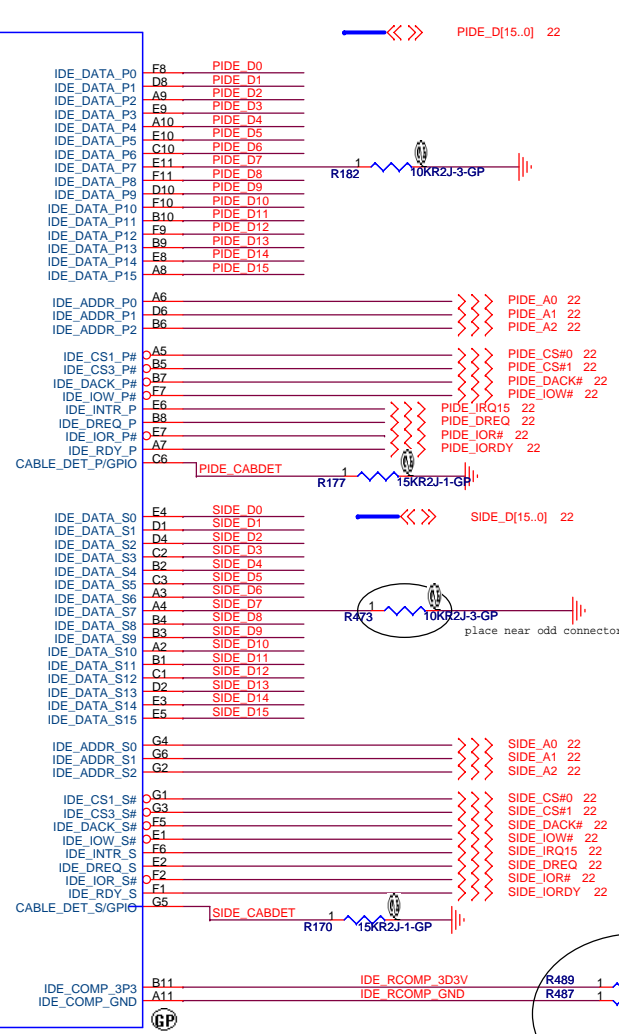
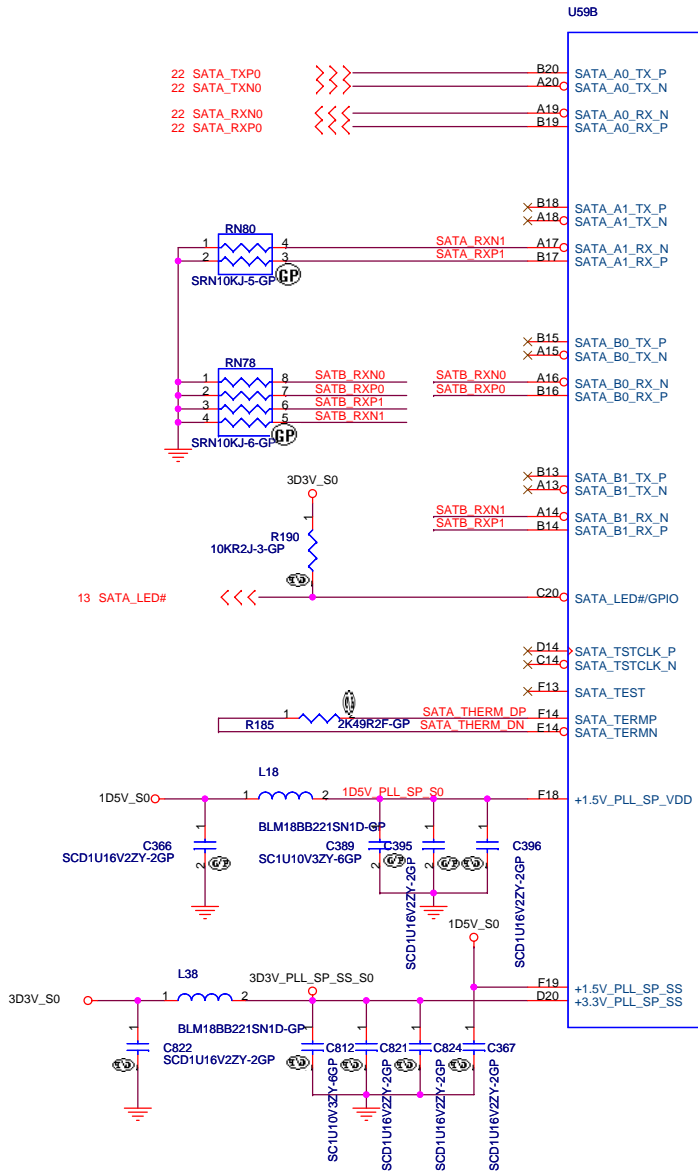
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(2/6)PCI**

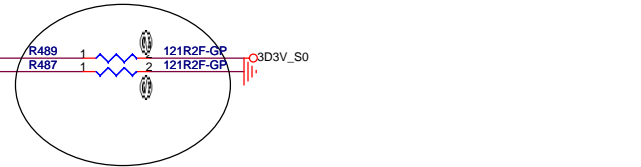
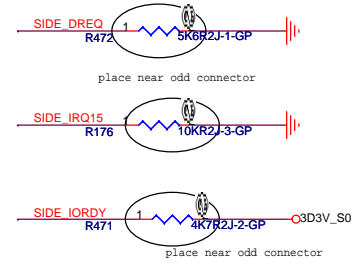
Size A3 Document Number **MYALL M** Rev **SA**

Date: Friday, June 16, 2006 Sheet 16 of 59



PIDE_D[15..0] 22

SIDE_D[15..0] 22



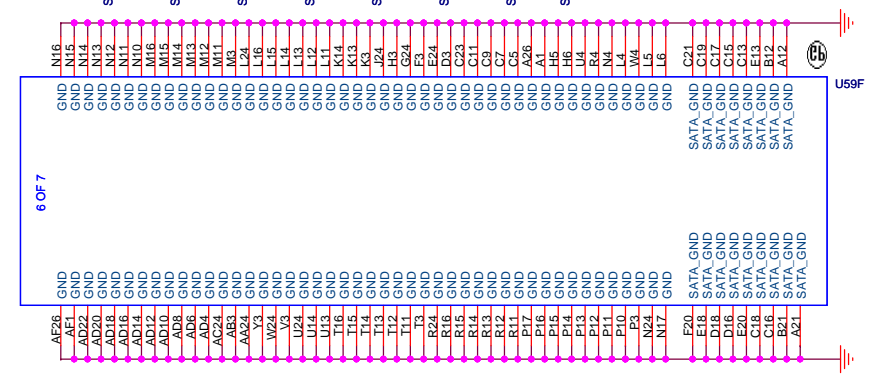
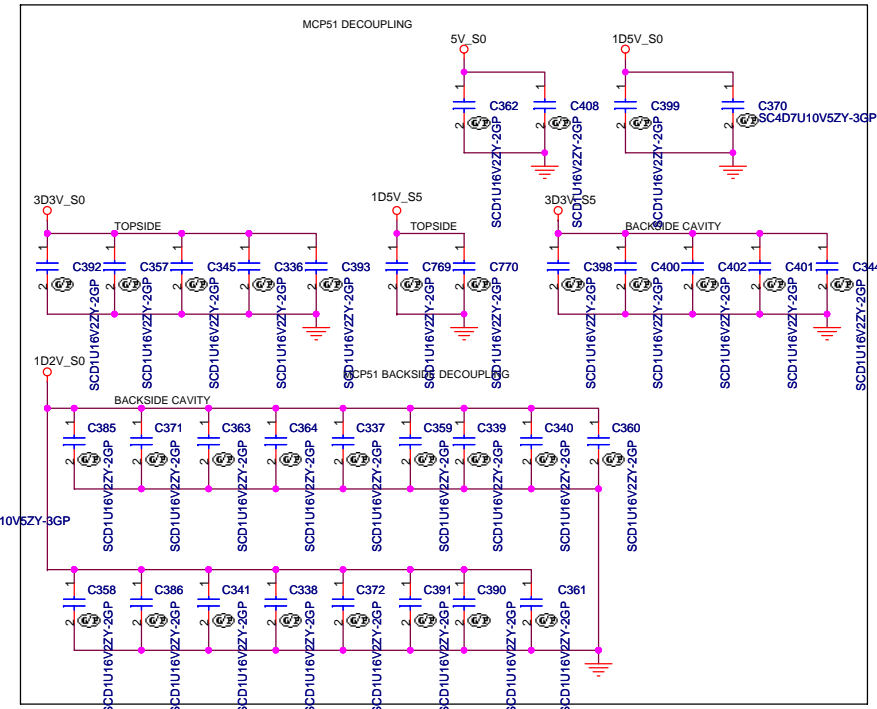
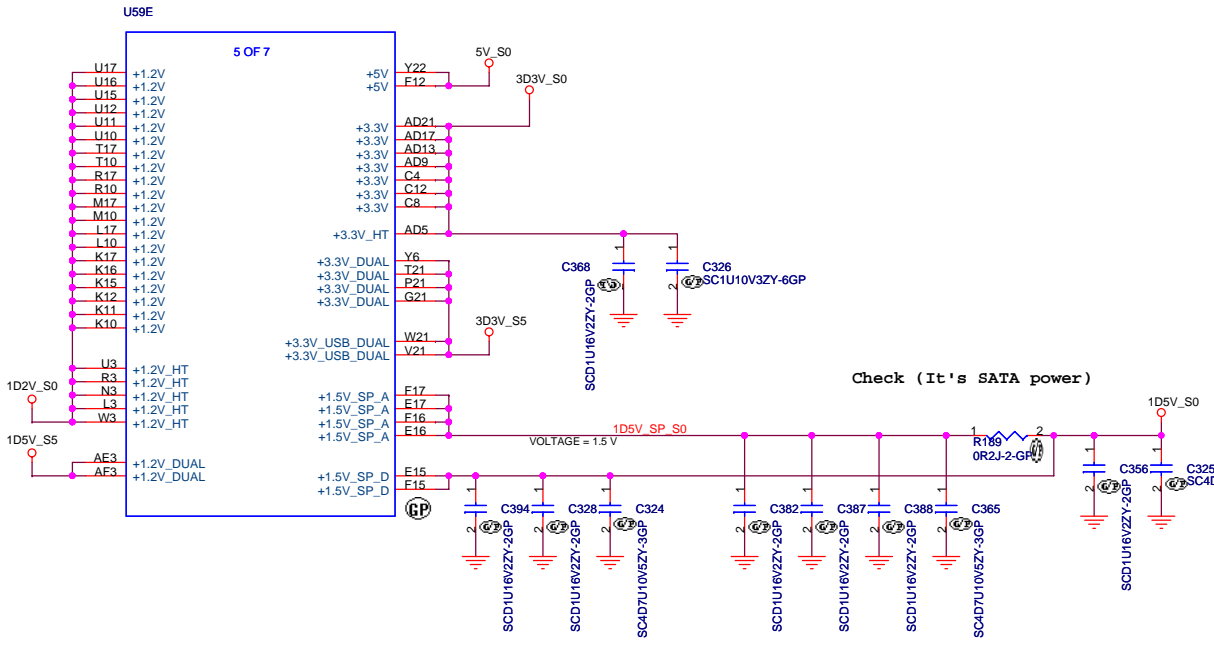
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(3/6)SATA/PATA**

Size A3 Document Number: **MYALL M** Rev: **SA**

Date: Friday, June 16, 2006 Sheet 17 of 59

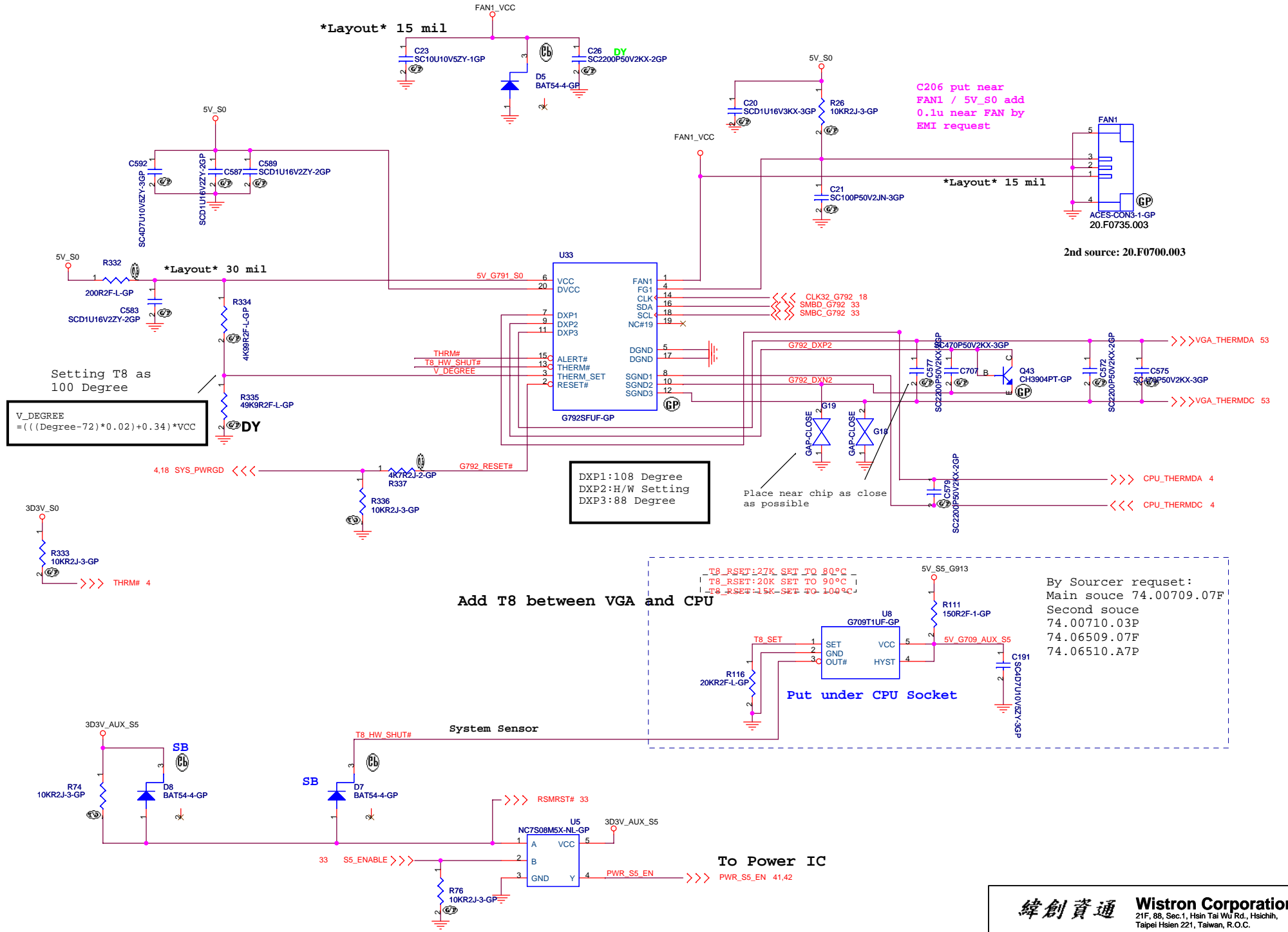


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(6/6)POWER**

| | | |
|-----------------------------|--------------------------------|---------------|
| Size A3 | Document Number MYALL M | Rev SA |
| Date: Friday, June 16, 2006 | Sheet 20 of 59 | |



Setting T8 as 100 Degree

$$V_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Add T8 between VGA and CPU

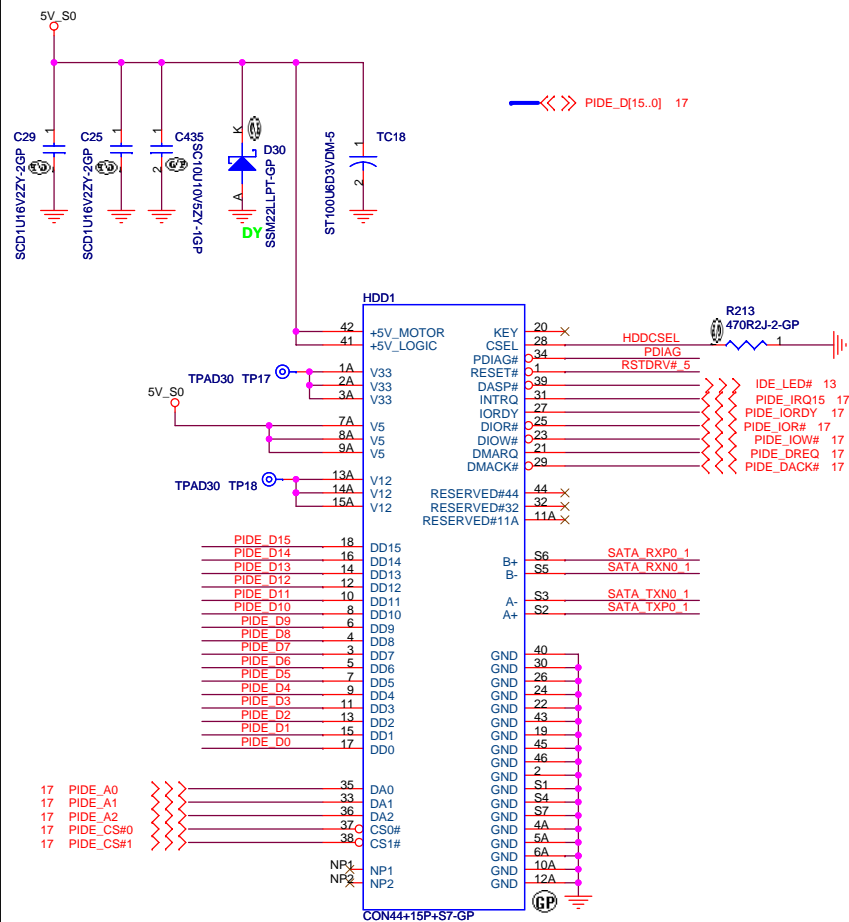
By Sourcer request:
Main souce 74.00709.07F
Second souce
74.00710.03P
74.06509.07F
74.06510.A7P

Put under CPU Socket

C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request

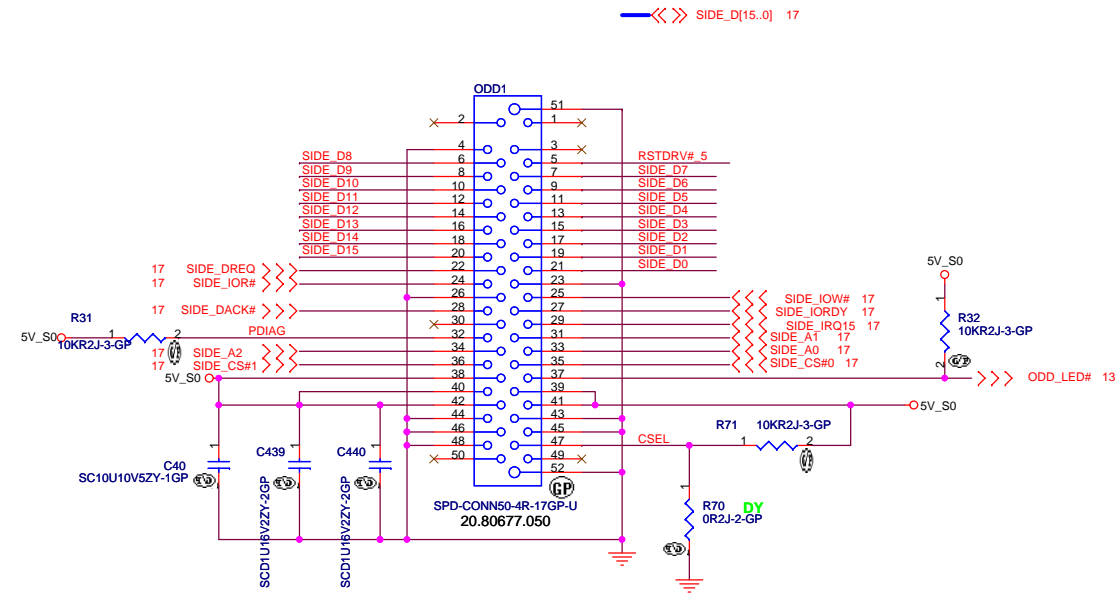
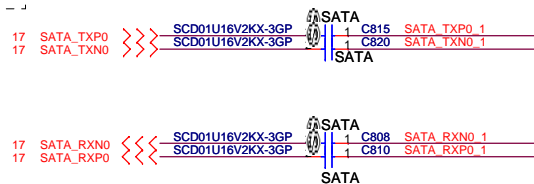
2nd source: 20.F0700.003

CD-ROM Connector

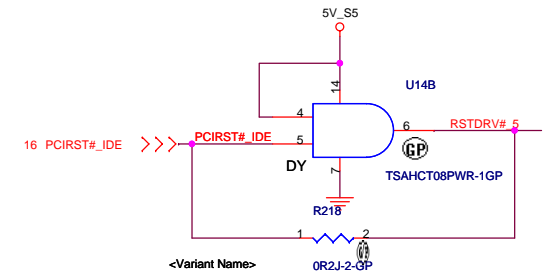
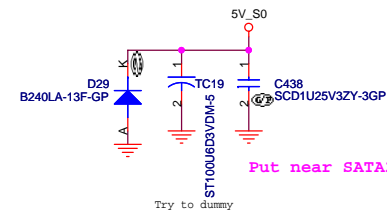


HDD Connector

SATA PN : 20.F0883.001
PATA PN : 21.E0021.222

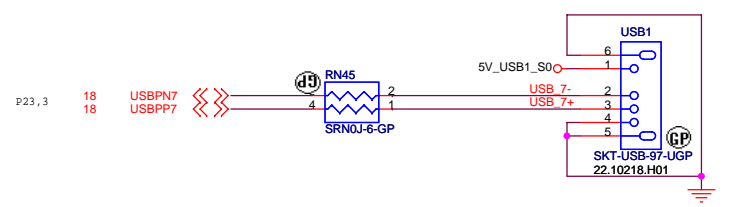
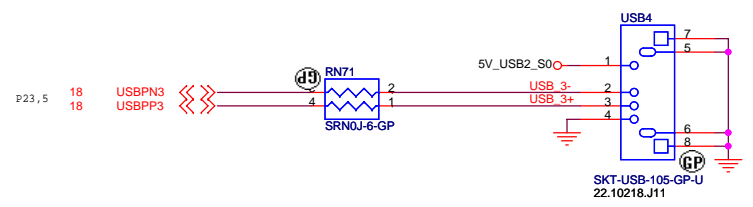
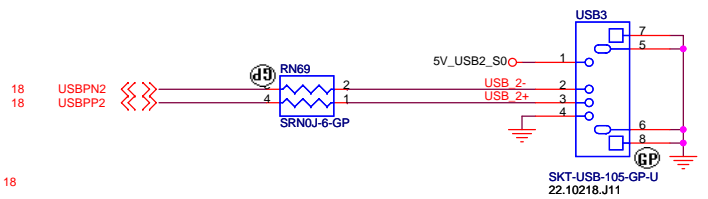
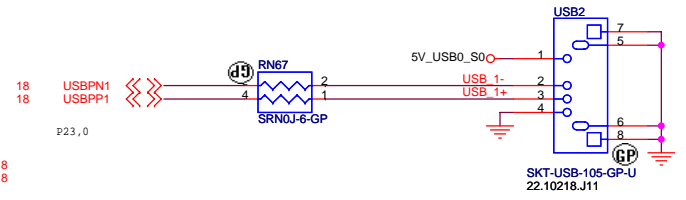
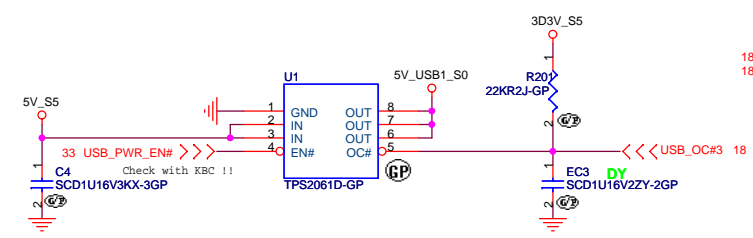
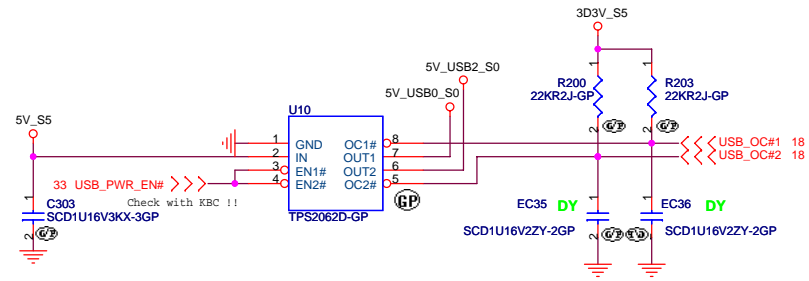
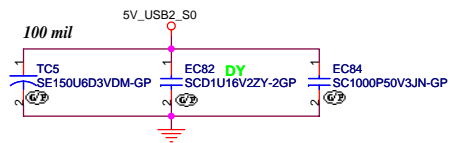
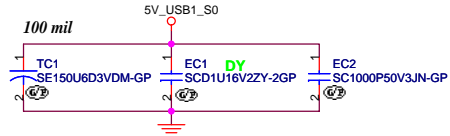
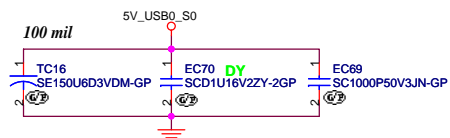


For HDD & SATA both

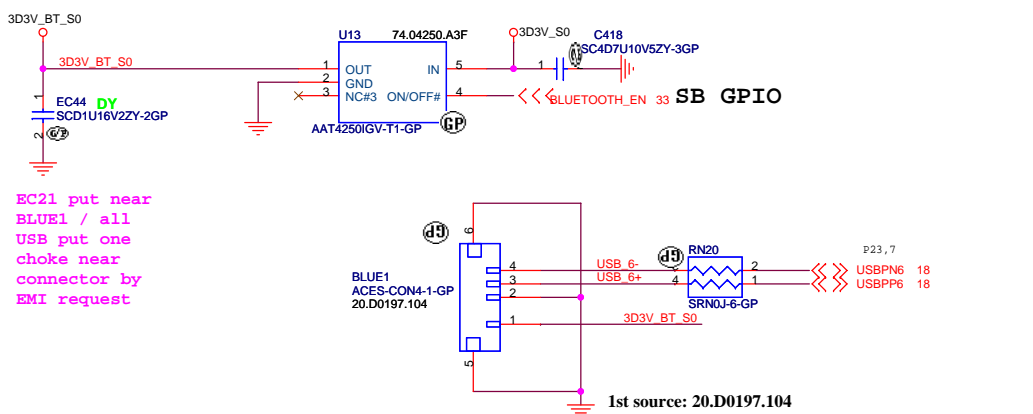


ME : 20.F0777.022

| | | | |
|-------------------------------|-----------------------|--|----------|
| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title HDD and CDROM | | | |
| Size | Document Number | Rev | SA |
| MYALL M | | | |
| Date: | Friday, June 16, 2006 | Sheet | 22 of 59 |

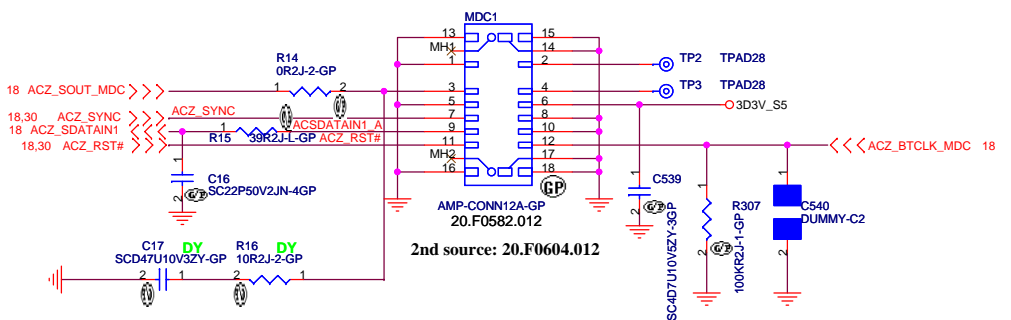


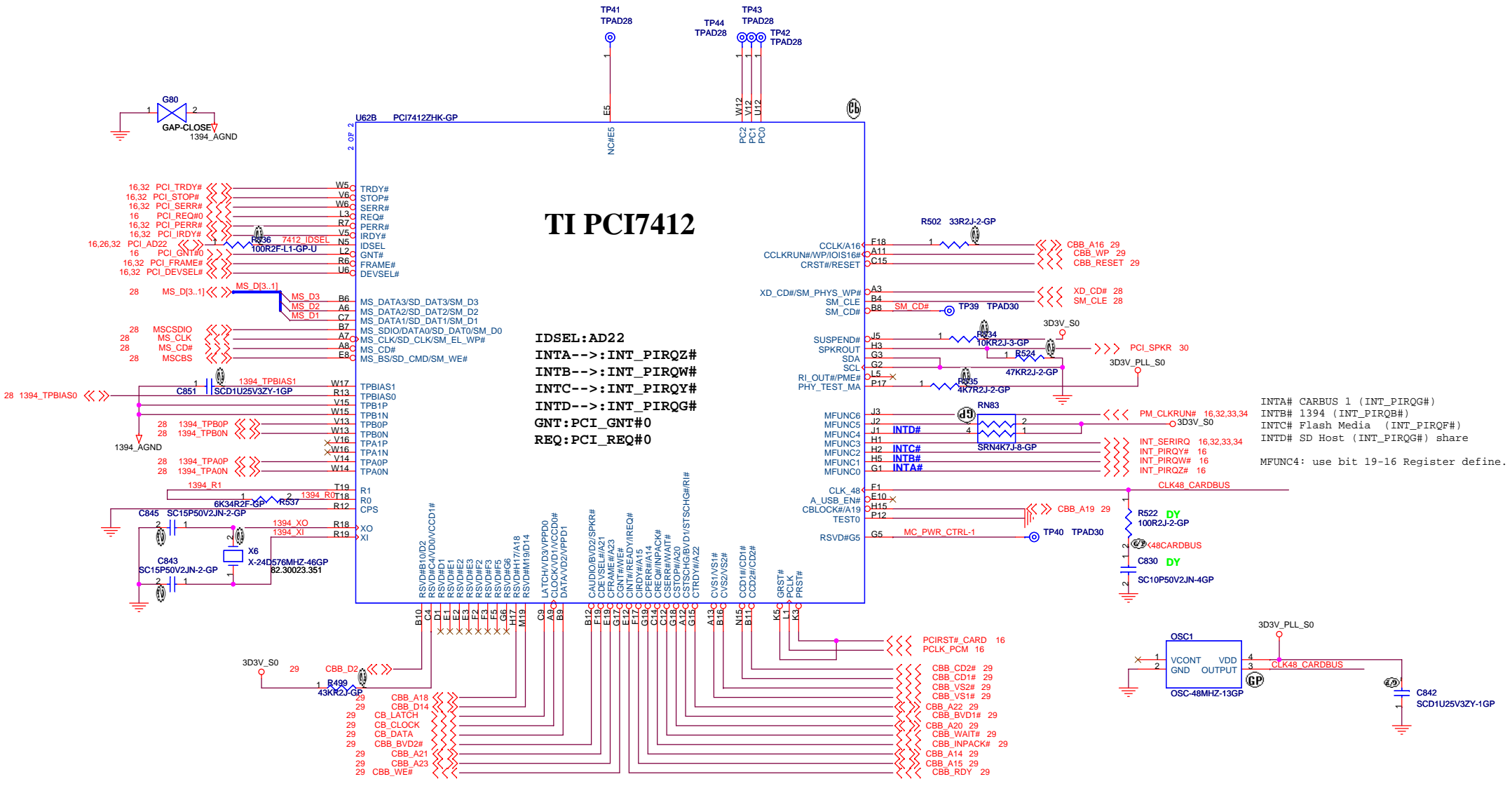
BLUETOOTH MODULE



MDC 1.5 CONNECTOR

CHANGE TO AZ





TI PCI7412

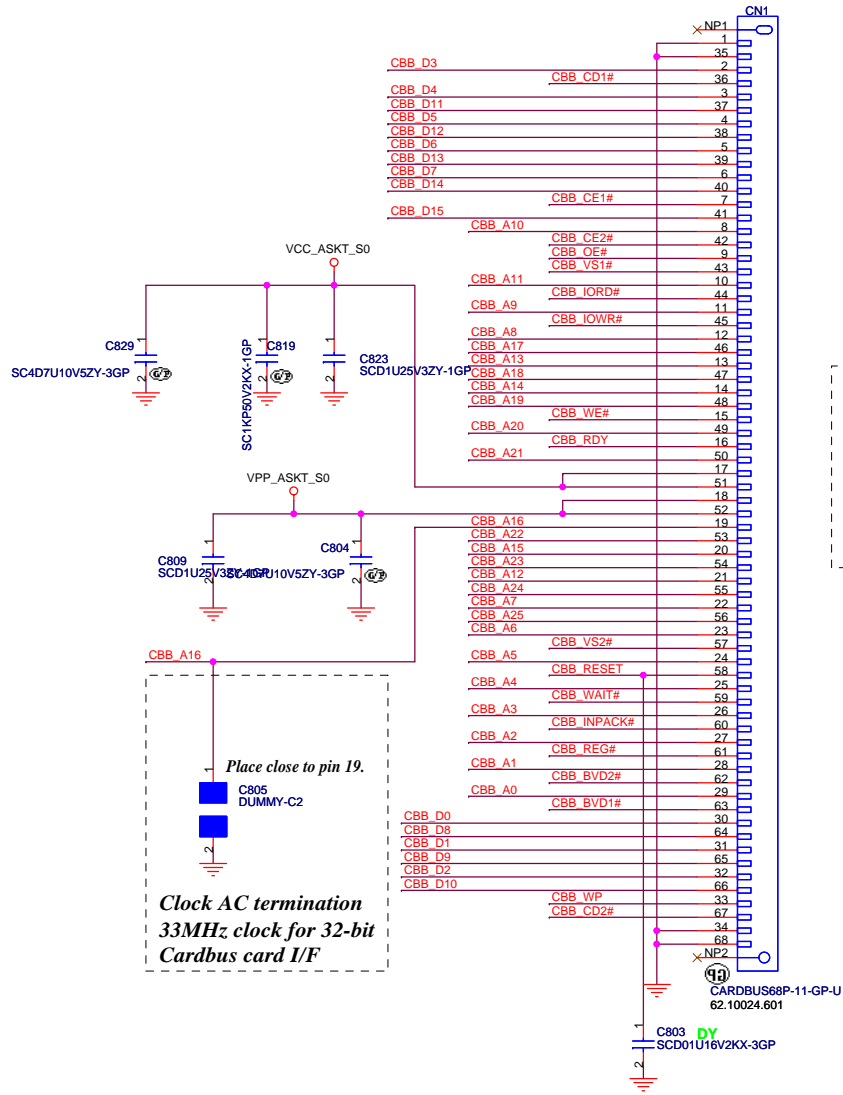
IDSEL: AD22
INTA-->: INT_PIRQ#
INTB-->: INT_PIRQ#
INTC-->: INT_PIRQ#
INTD-->: INT_PIRQ#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

INTA# CARBUS 1 (INT_PIRQ#)
 INTB# 1394 (INT_PIRQ#)
 INTC# Flash Media (INT_PIRQ#)
 INTD# SD Host (INT_PIRQ#) share
 MFUNC4: use bit 19-16 Register define.

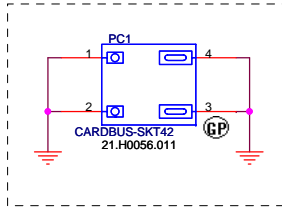
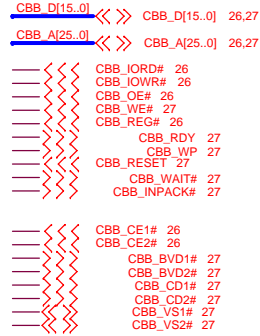
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|---------------------|-----------------|-----------------------------|----------|
| Title | | Rev | |
| TI PCI7412 (2 of 2) | | SA | |
| Size | Document Number | Date: Friday, June 16, 2006 | |
| MYALL2 | | Sheet | 27 of 59 |

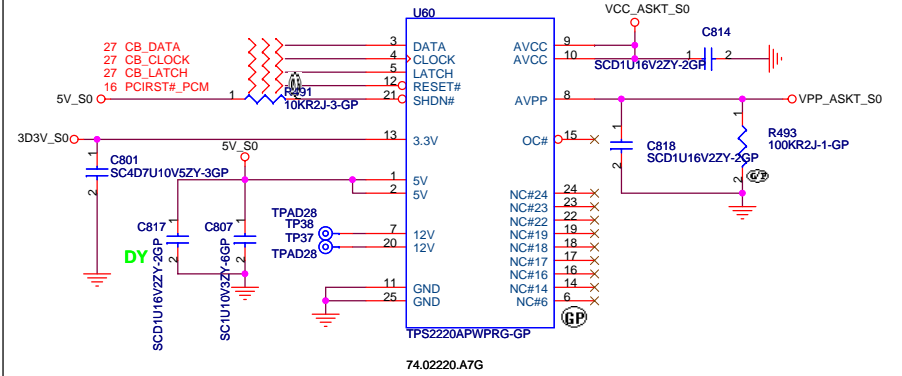
PCMCIA Socket



Cardbus I/F

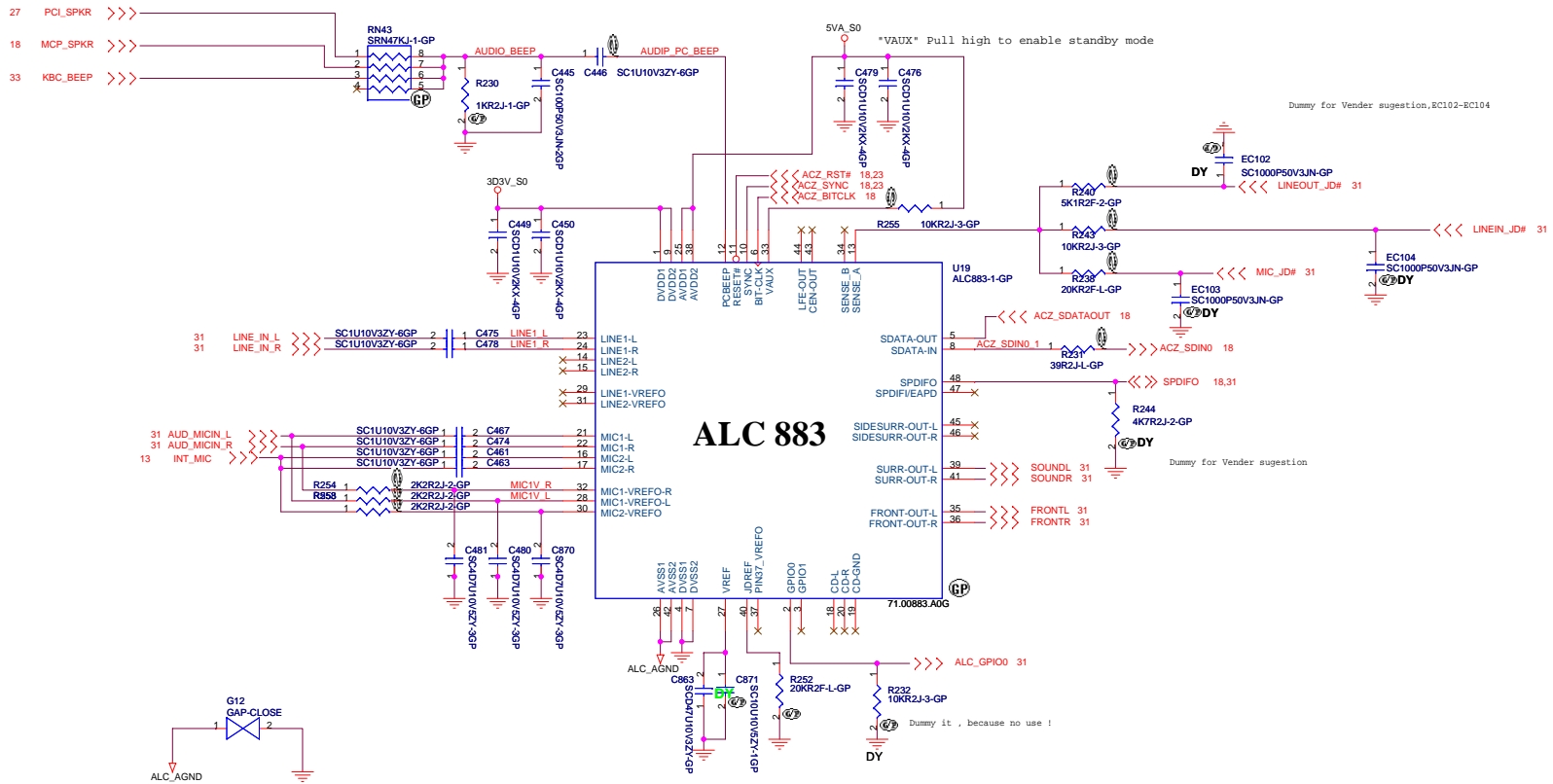


Power switch

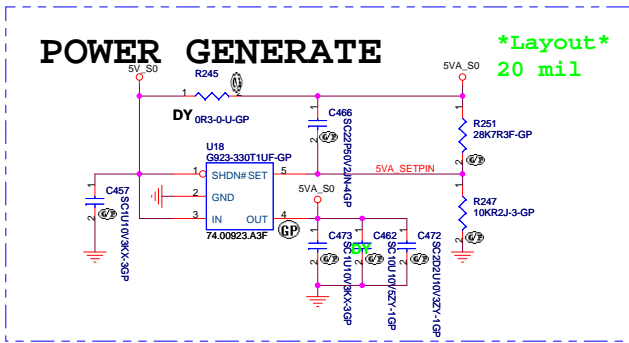


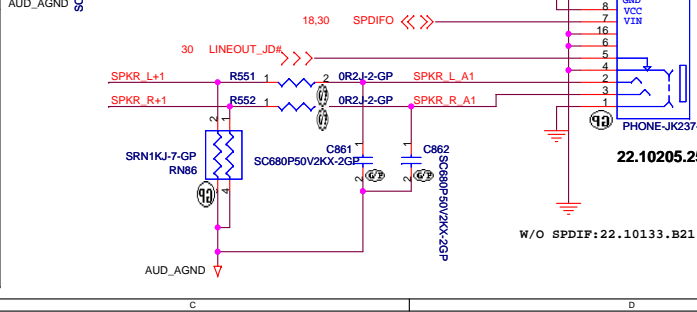
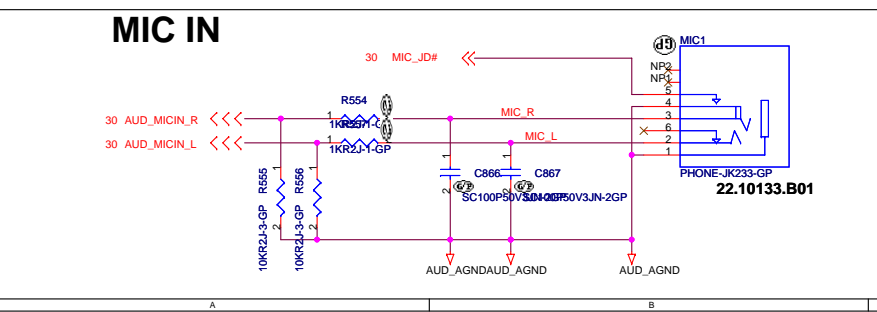
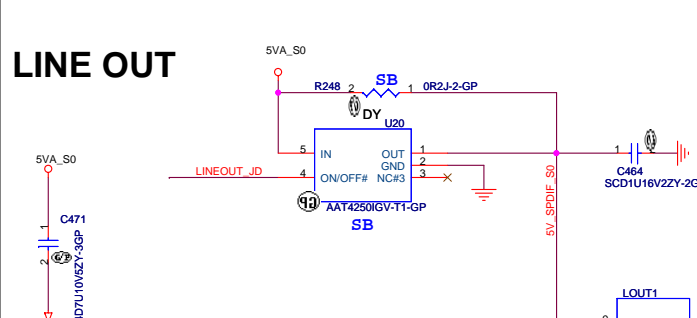
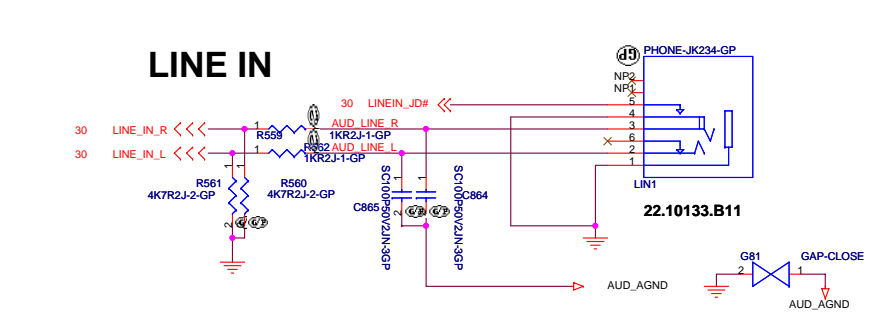
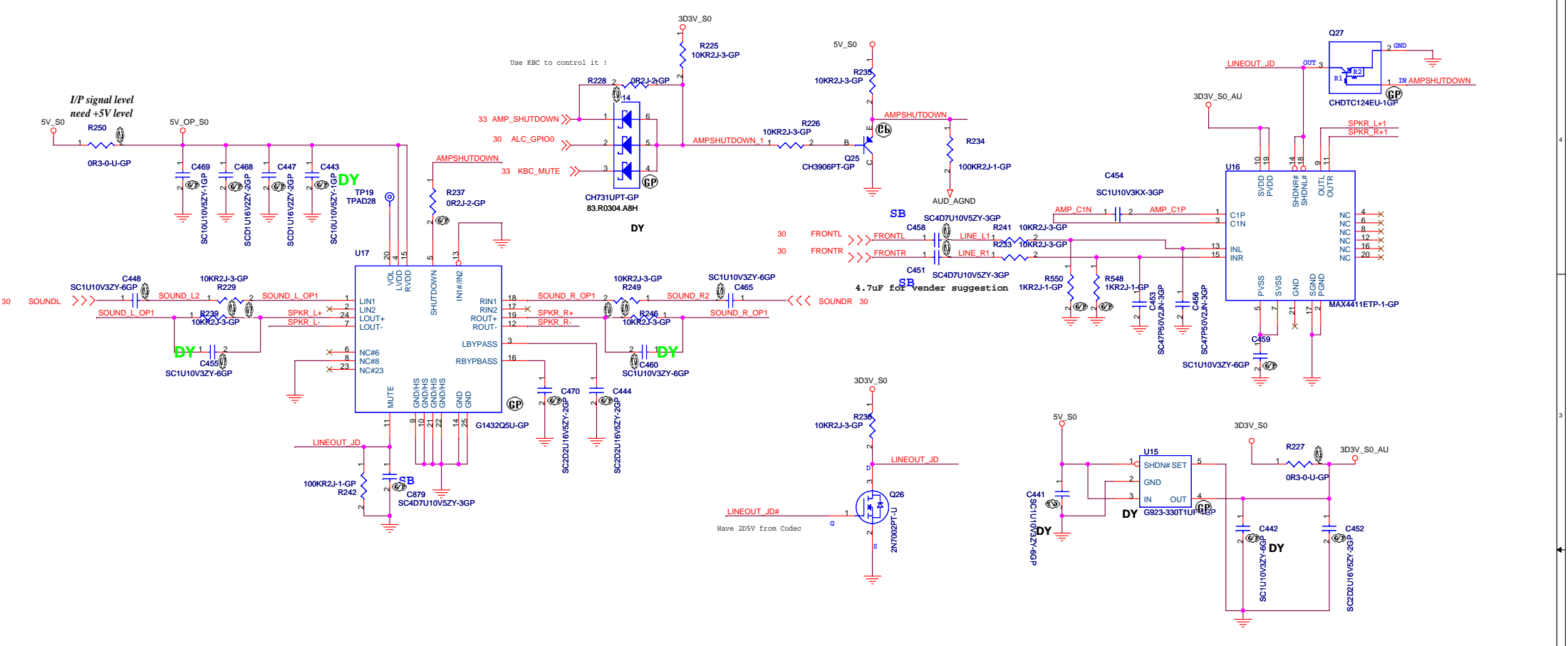
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

| | | | | | |
|---------|-----------------------|--|--------|----|-------|
| Title | | | PCMCIA | | |
| Size | Document Number | | | | Rev |
| MYALL M | | | | | SA |
| Date: | Friday, June 16, 2006 | | Sheet | 29 | of 59 |



| Pin | Symbol | Location | Re-tasking |
|-------|----------|------------|---|
| 35/36 | FRONT | | |
| 39/41 | SURR | X | |
| 43/44 | CEN/LEFT | X | |
| 45/46 | SIDESURR | X | |
| 23/24 | LINE1 | | |
| 21/22 | MIC1 | Location | Re-tasking |
| 14/15 | LINE2 | AMP, Jack1 | AMP output, line input |
| 16/17 | MIC2 | | X |
| | | | SURR-VREFO-L/R |
| | | | SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R |
| | Jack 2 | | Line input, line output |
| | Jack 3 | | Mic input, line output |
| | | | X |
| | Int. Mic | | Mic input |





Internal Speaker

SPKR L-
SPKR L+
SPKR R-
SPKR R+

20.D0197.104

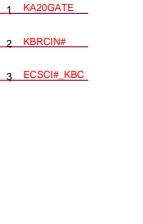
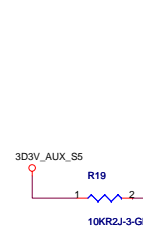
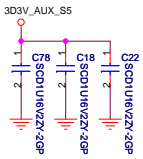
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Wistron Corporation
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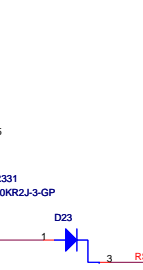
AUDIO AMP AND JACK

MYALL M
SB

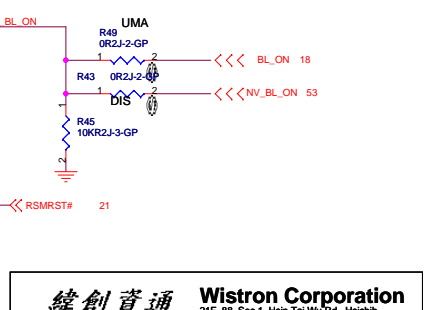
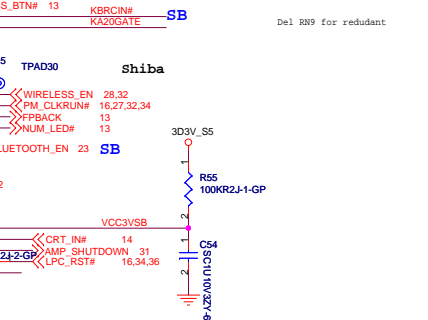
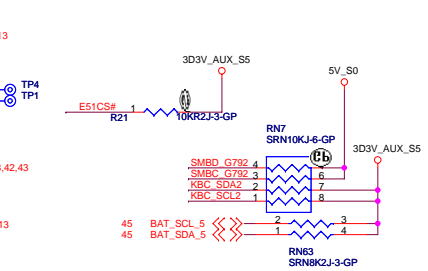
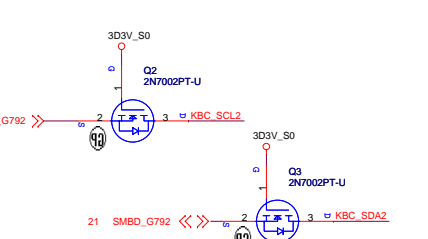
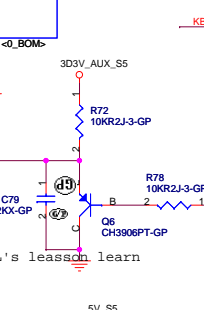
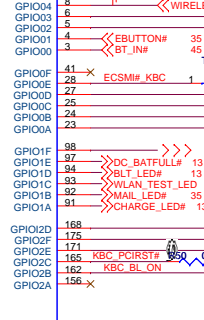
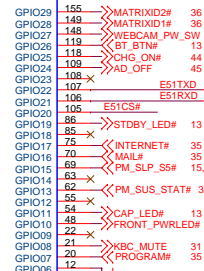
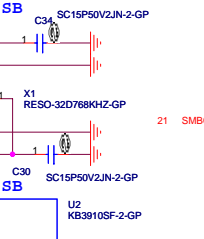
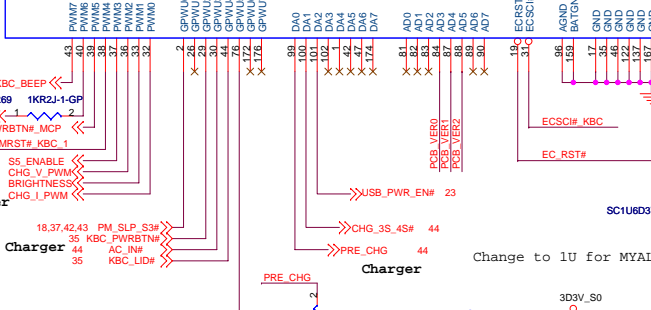
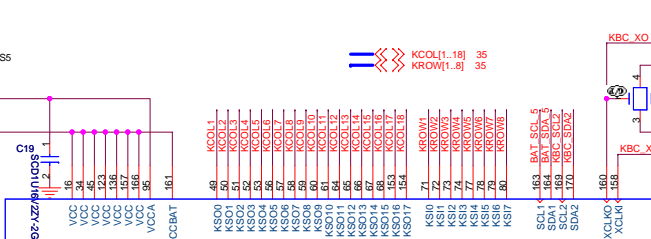
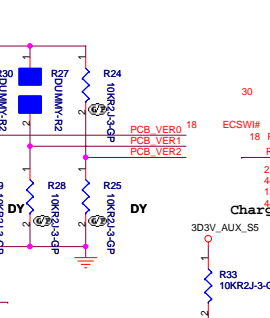
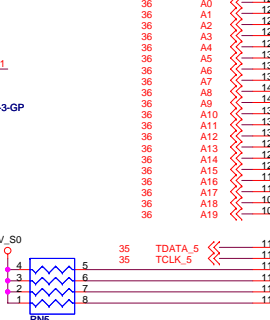
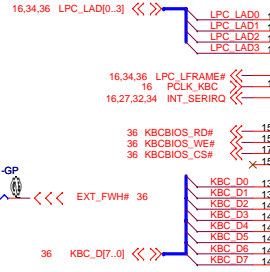
Friday, June 16, 2006



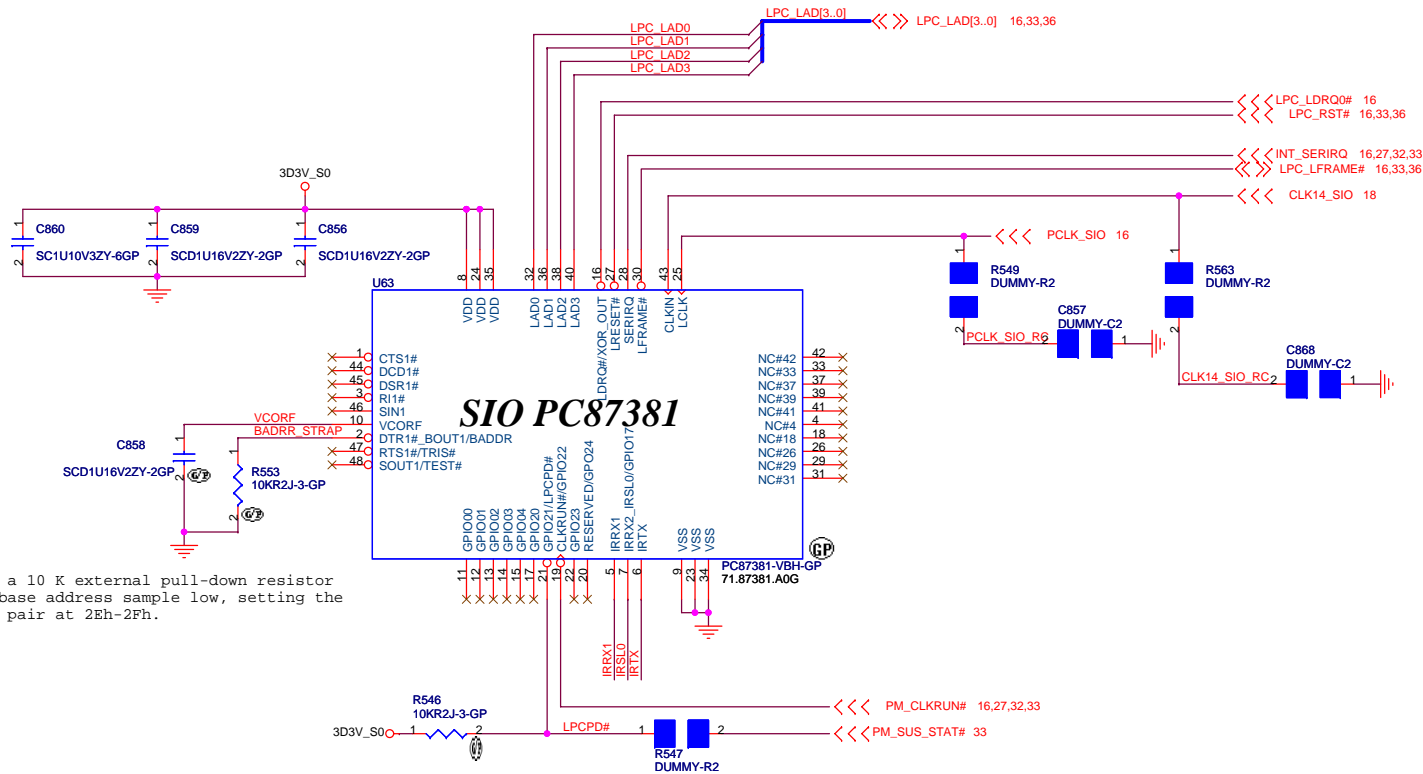
Planar ID(2,1,0)
 SA: 0,0,0
 SB: 0,0,1
 SC: 0,1,0
 SD: 0,1,1



BATS4-4GP
 A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
 A4 for DMRP==>High=Disable, Low=Enable
 A5 for EMWR==>High=Enable, Low=Disable
 GPIO05 for clock test mode==>High=Test Mode Low=32KHz clock in normal running(Recommended)
 GPIO06 for DPLL test mode==>High=Test Mode Low=Normal operation(Recommended)



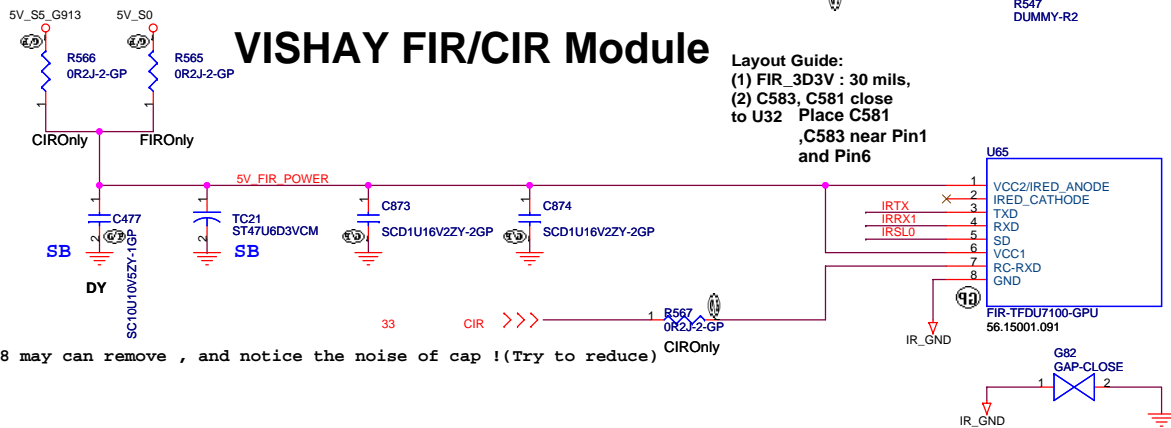
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC 3910
 MYALL M
 SA



Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

VISHAY FIR/CIR Module

- Layout Guide:
 (1) FIR_3D3V : 30 mils,
 (2) C583, C581 close to U32
 Place C581, C583 near Pin1 and Pin6

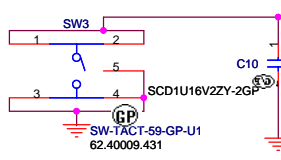


Check ! R778 may can remove , and notice the noise of cap !(Try to reduce)

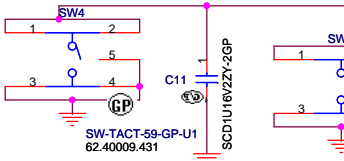
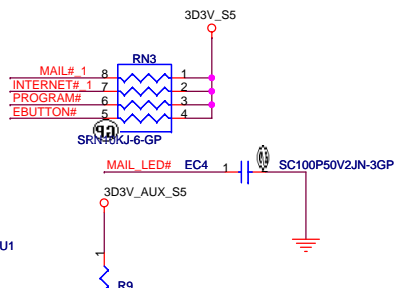
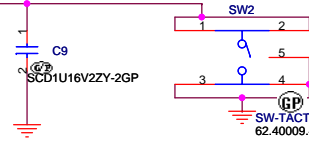
80.47615_531

| | |
|---|---------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: SIO 87381 / IR | |
| Size: Document Number | Rev: SA |
| Date: Friday, June 16, 2006 Sheet 34 of 59 | |

Internet Button

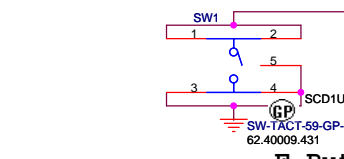


Mail Button



Power Button 2nd source: 20.K0185.012

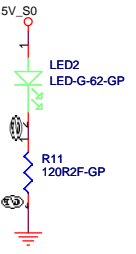
Program Button



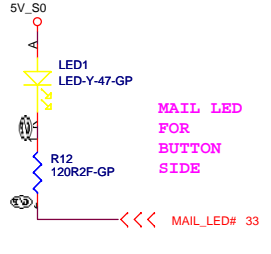
E-Button



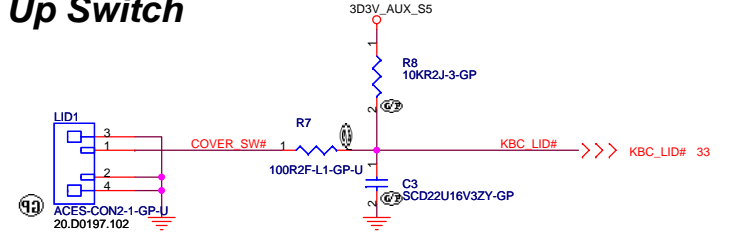
POWER LED FOR BUTTON SIDE



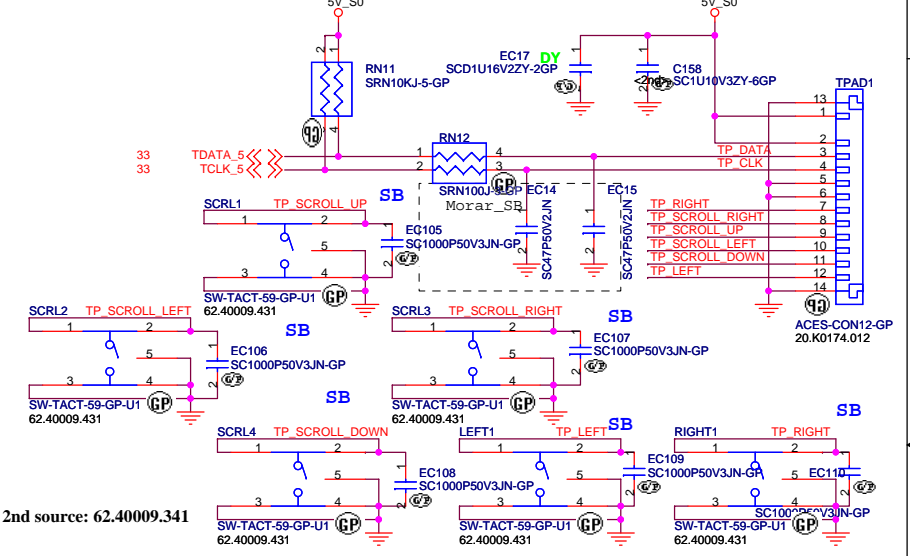
MAIL LED FOR BUTTON SIDE



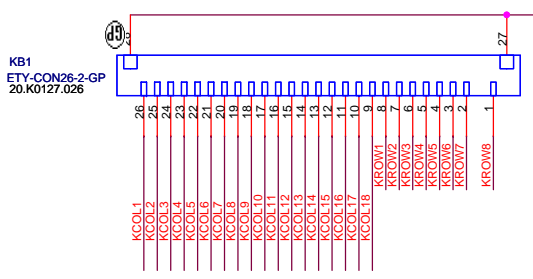
Cover Up Switch



TOUCH PAD



2nd source: 62.40009.341

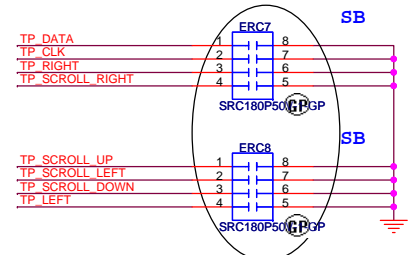
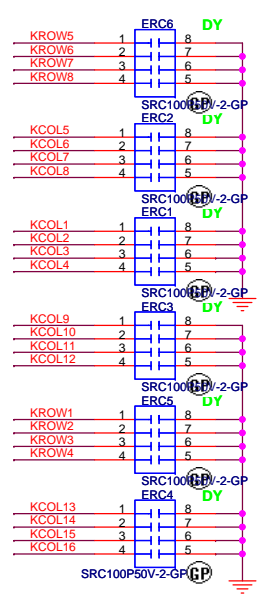


Internal KeyBoard CONN



CHECK KB SPEC. AND PIN DEFINE

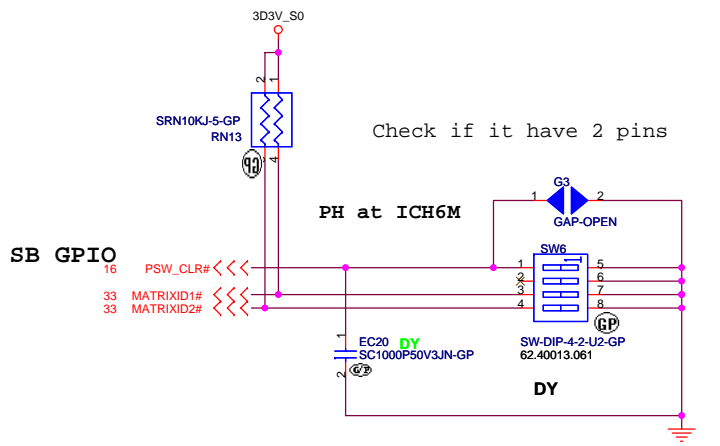
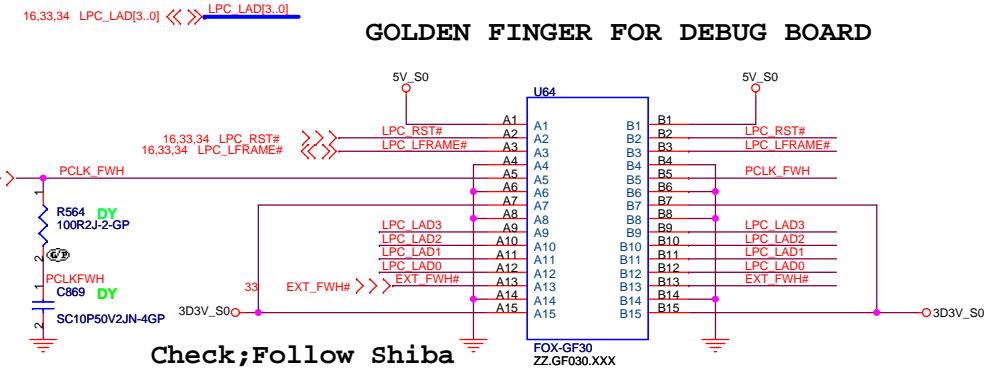
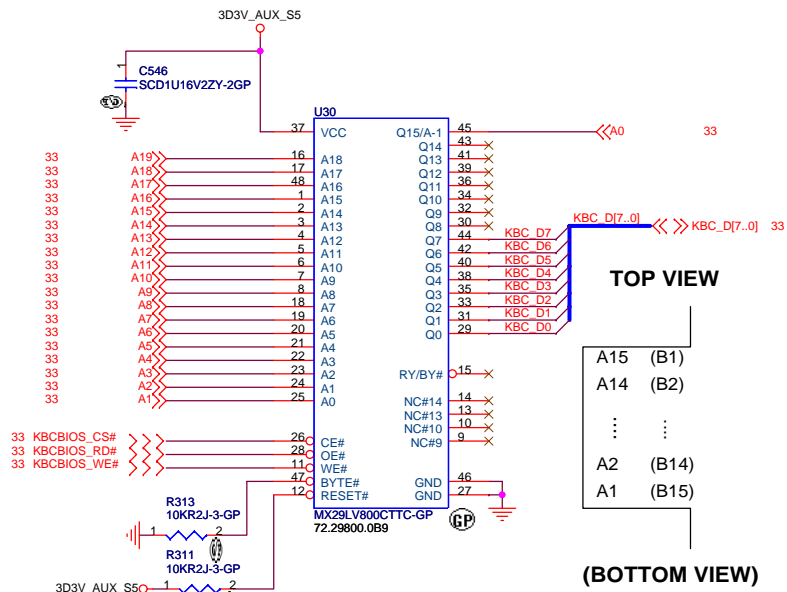
EMI Bypass cap.



EMI need to change to 270P , but no 270P array only 180 or 470

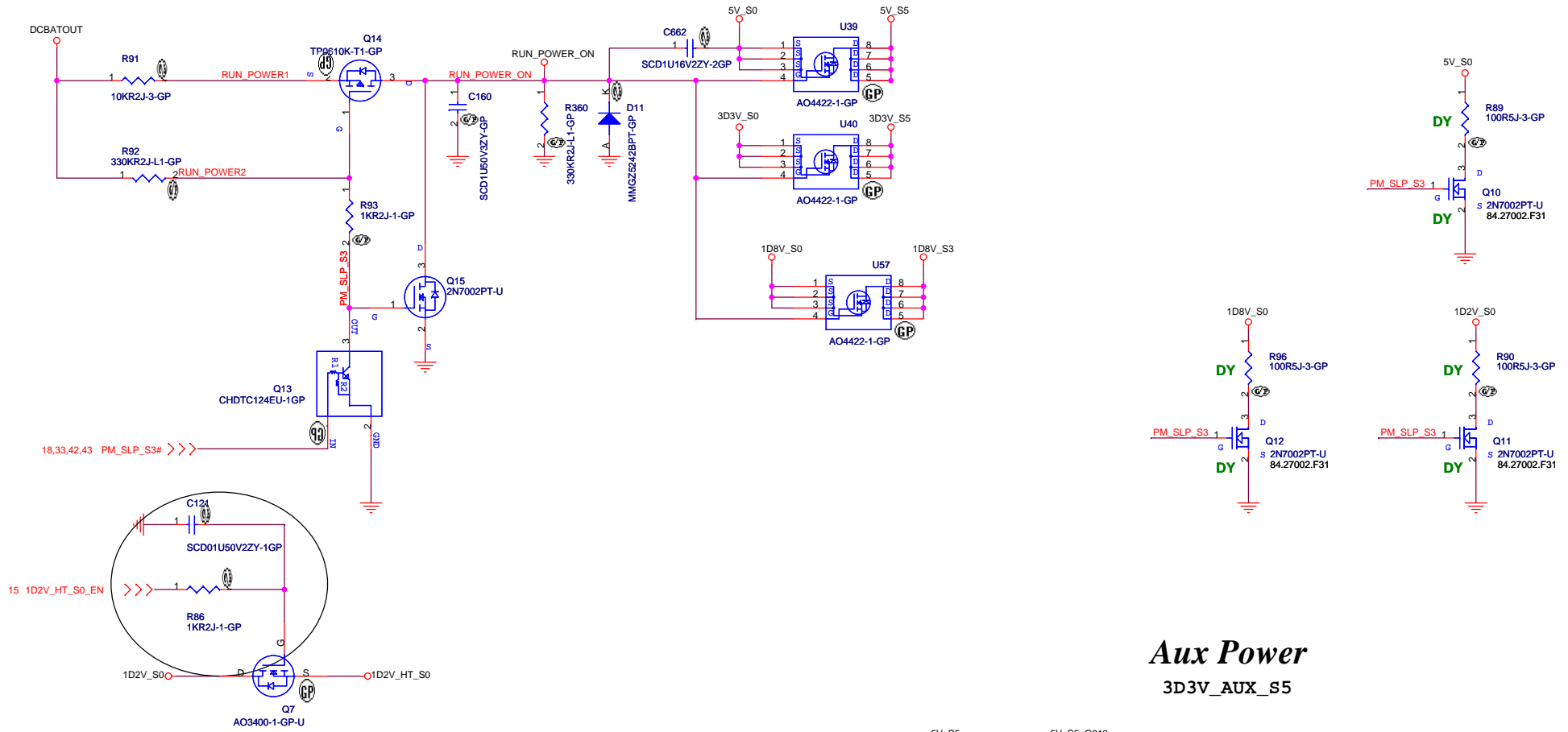
緯創資通 Wistron Corporation
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| | | | | | |
|-----------------------------|-----------------|--|-------------------------|--|----|
| Title | | | BUTTONS / KB / TOUCHPAD | | |
| Size | Document Number | | Rev | | SA |
| Date: Friday, June 16, 2006 | | | Sheet 35 of 59 | | |



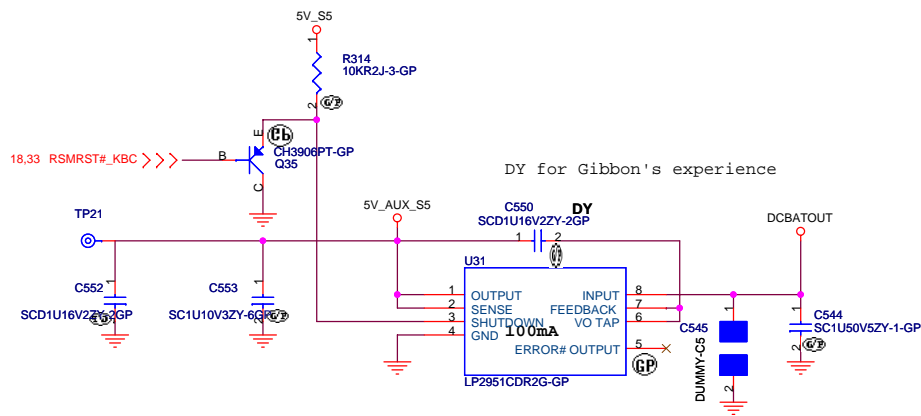
| | | |
|---|-----------------|-----------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: BIOS | | |
| Size | Document Number | Rev |
| | MYALL M | SA |
| Date: Friday, June 16, 2006 | | |
| Sheet | | of |
| 36 | | 59 |

Run Power



Aux Power

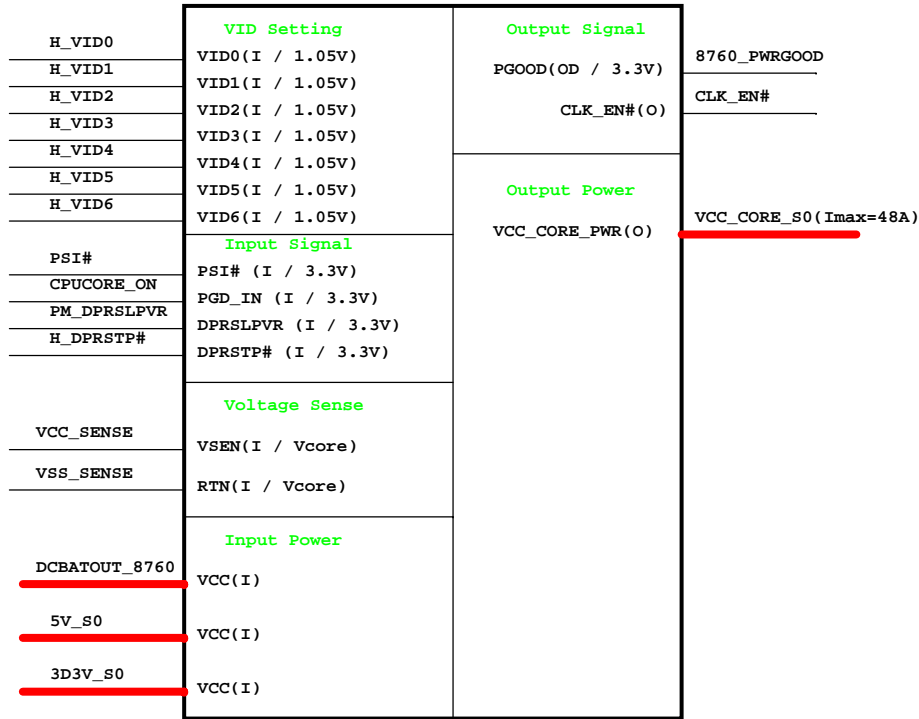
3D3V_AUX_S5



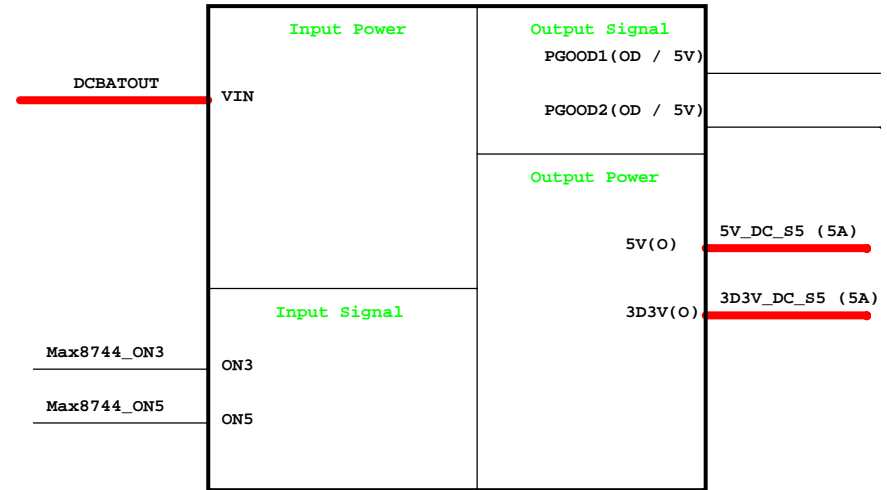
<Variant Name>

| | | | |
|--|-----------------------|--|----------|
| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title RUN POWER and 3D3V_AUX_S5 | | | |
| Size | Document Number | | Rev |
| | MYALL M | | SA |
| Date: | Friday, June 16, 2006 | Sheet | 37 of 59 |

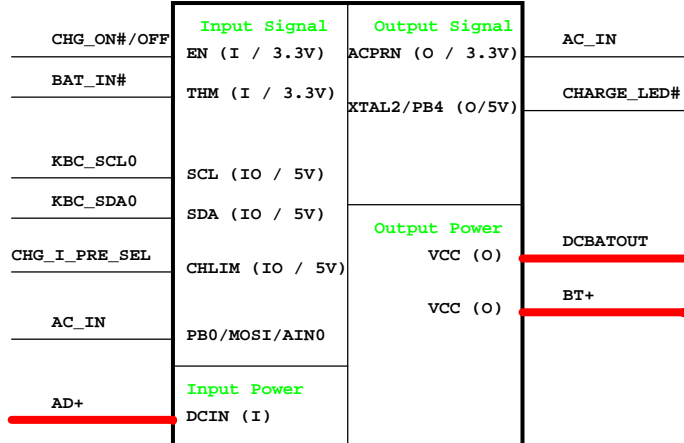
**CPU_CORE
MAX8760**



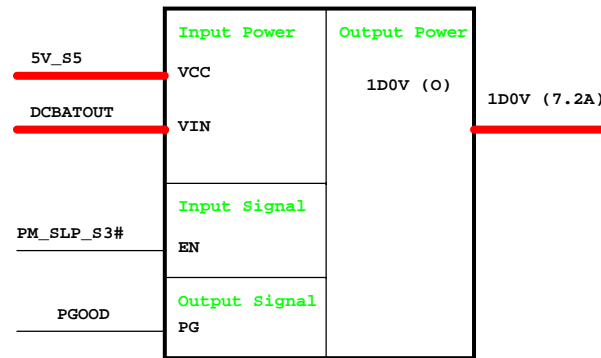
Max8744 3D3V/5V



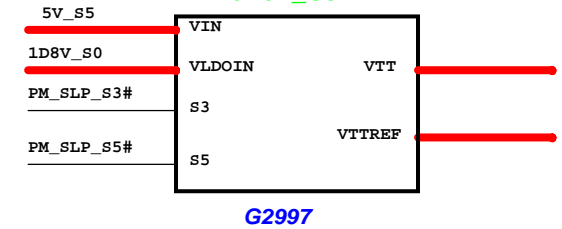
Charger_ISL6255



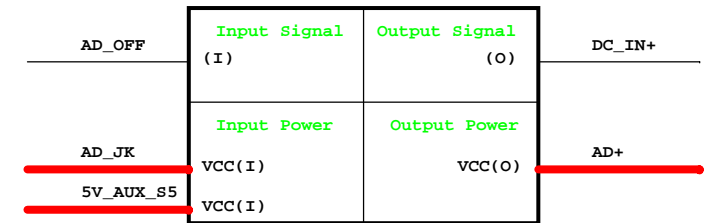
ISL6269_VGA_Core 1D1V



0D9V_S3



Adapter



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Taipei Hsien 221, Taiwan, R.O.C.

CPU_VCORE

VID=1.20V(25W)/1.15V(35W)

Iomax=21A(25W)/35A (35W)

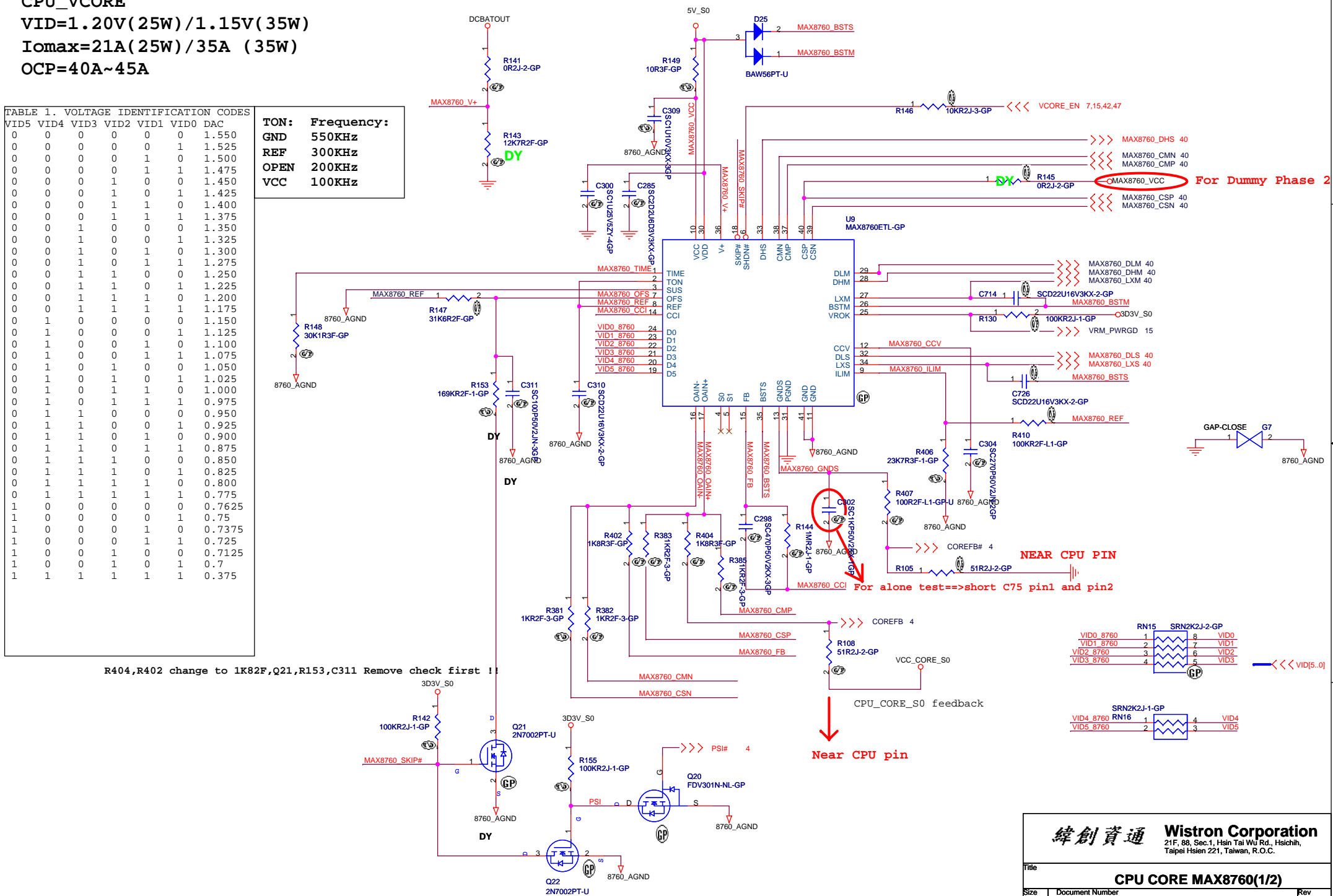
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

| VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | DAC |
|------|------|------|------|------|------|--------|
| 0 | 0 | 0 | 0 | 0 | 0 | 1.550 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.525 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.500 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.475 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.450 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.425 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.400 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.375 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1.350 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1.325 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1.300 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1.275 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1.250 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1.225 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1.200 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1.175 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1.150 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1.125 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1.100 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1.075 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1.050 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.025 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1.000 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.975 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.950 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.925 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.900 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.875 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.850 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.825 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.800 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.775 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.7625 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.75 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.7375 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.725 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.7125 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.7 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.375 |

TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz

R404,R402 change to 1K82F,Q21,R153,C311 Remove check first !!

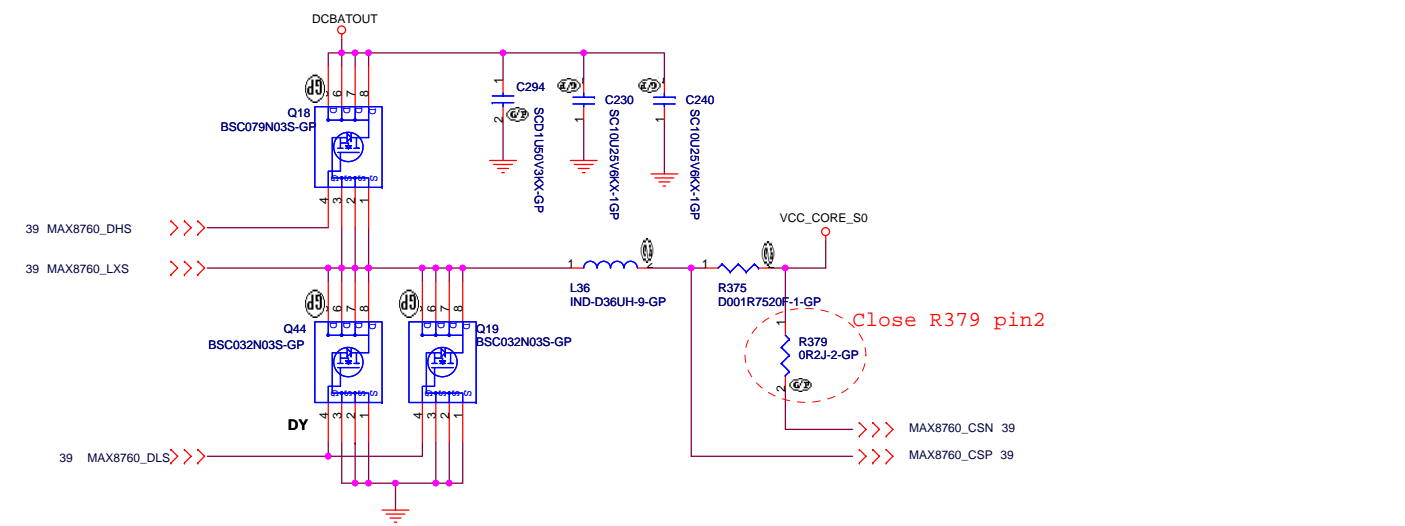
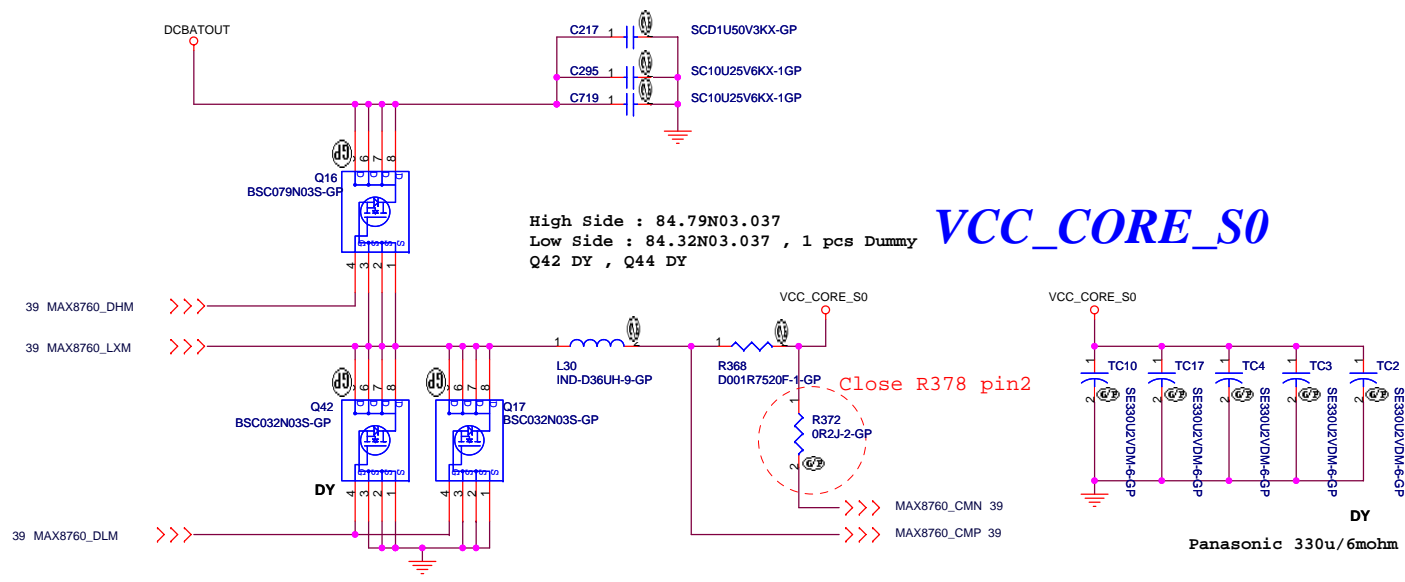


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Title: **CPU CORE MAX8760(1/2)**

Size A3 Document Number: **MYALL M** Rev: **SA**

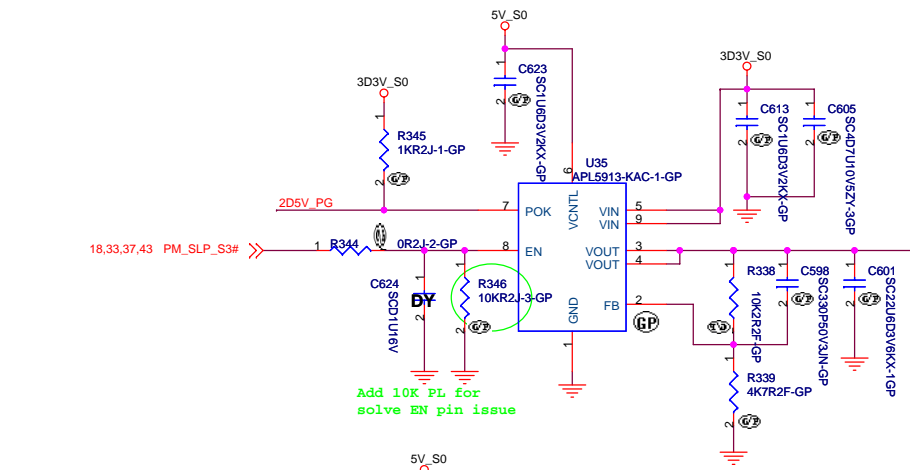
Date: Friday, June 16, 2006 Sheet 39 of 59



0D9V

2D5V_S0 Iomax<684mA

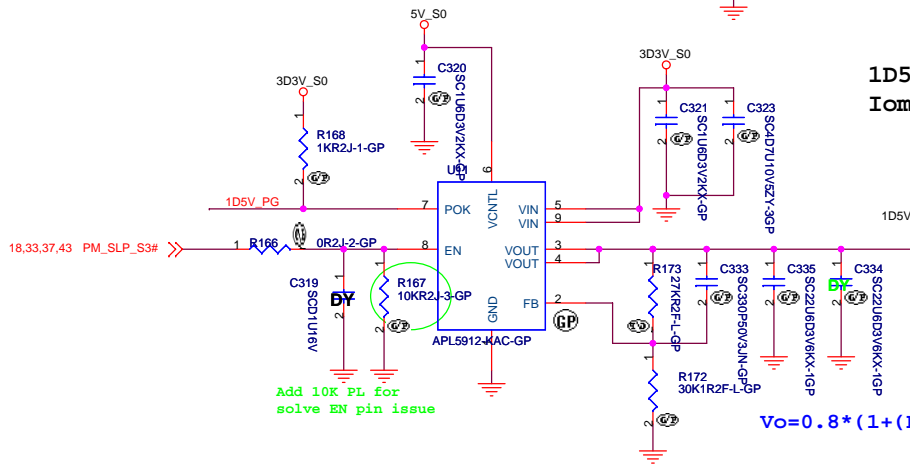
$$V_o = 0.8 * (1 + (R1/R2))$$



Add 10K PL for solve EN pin issue

1D5V_S0 Iomax<1100mA

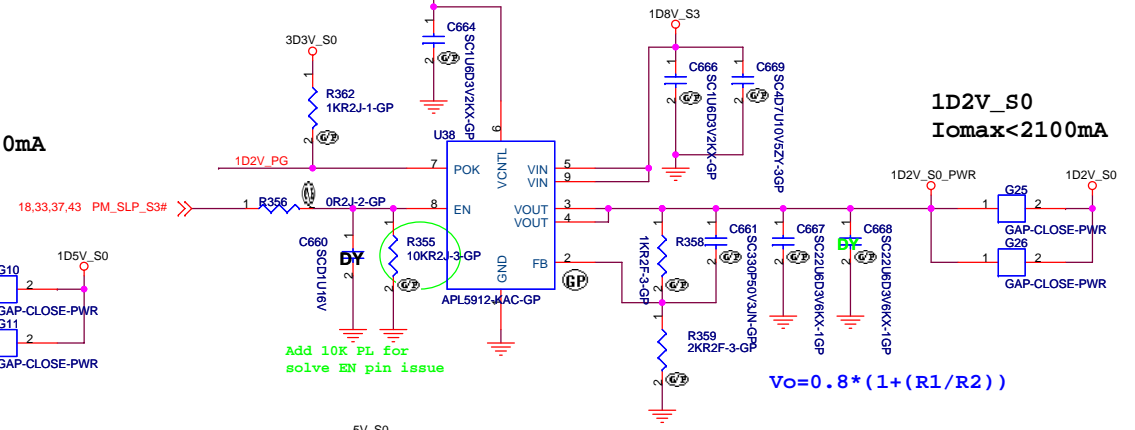
$$V_o = 0.8 * (1 + (R1/R2))$$



Add 10K PL for solve EN pin issue

1D2V_S0 Iomax<2100mA

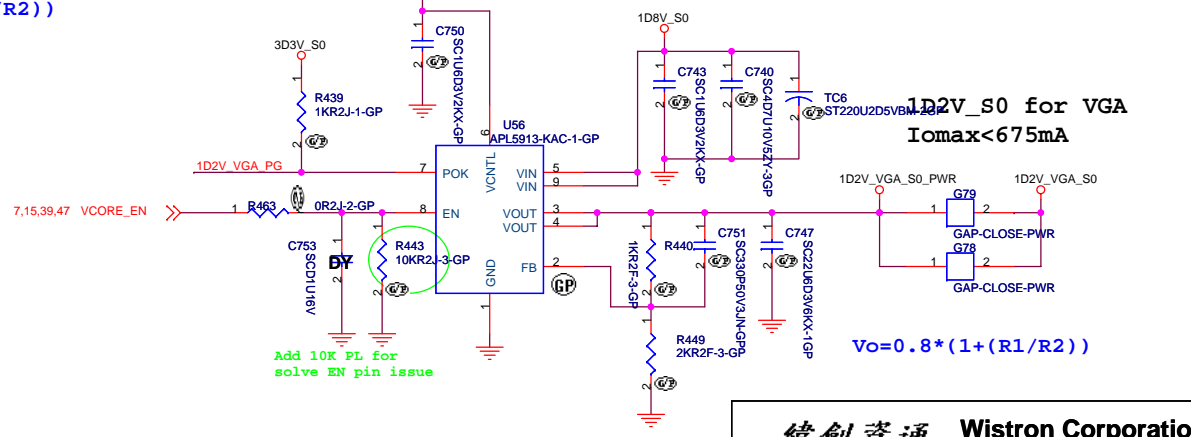
$$V_o = 0.8 * (1 + (R1/R2))$$



Add 10K PL for solve EN pin issue

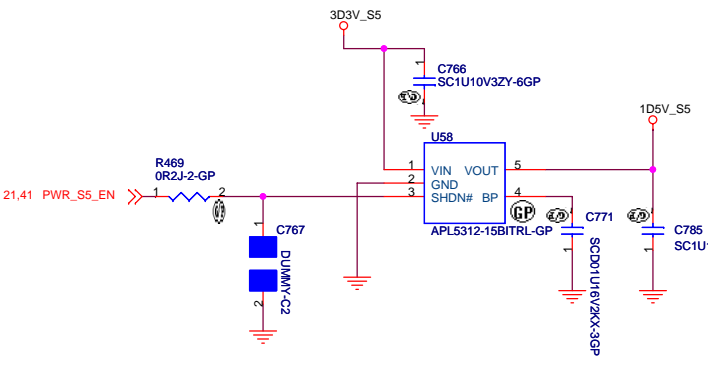
1D2V_S0 for VGA Iomax<675mA

$$V_o = 0.8 * (1 + (R1/R2))$$

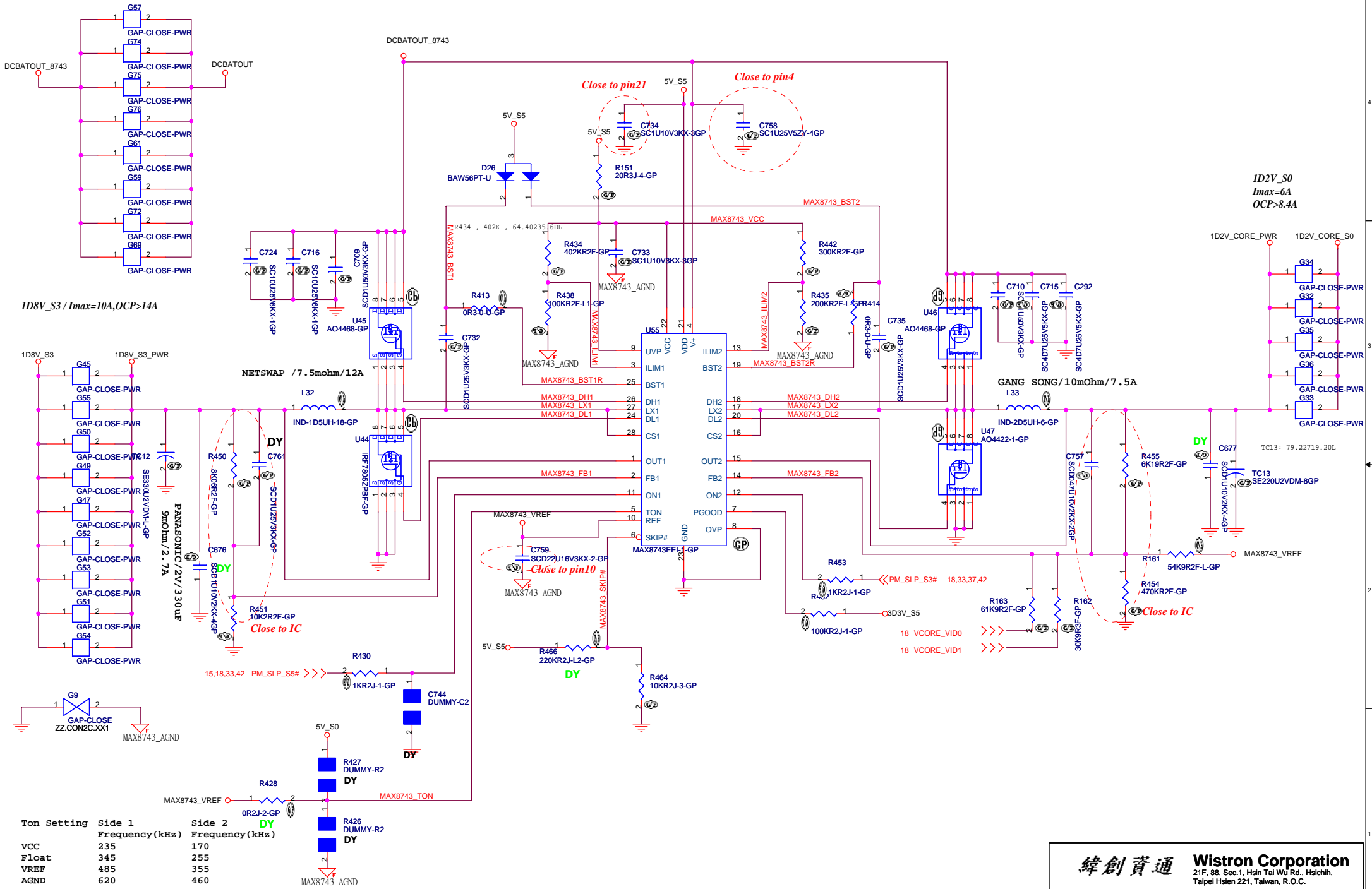


Add 10K PL for solve EN pin issue

1D5V_S5 Iomax<100mA



| | |
|---|--------------------------------|
| | |
| Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title 2D5V_S0/1D5V_S0/0D9V/1D2(LD) | |
| Size A3 | Document Number MYALL M |
| Date Friday, June 16, 2006 | Rev SA |
| Sheet 42 of 59 | |



1D8V_S3 / I_{max}=10A, OCP>14A

NETSWAP / 7.5mohm/1.2A

IND-1D5UH-18-GP

IND-2D5UH-6-GP

1D8V_S3

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

1D8V_S3_PWR

| Ton Setting | Side 1 | Side 2 |
|-------------|-----------------|-----------------|
| | Frequency (kHz) | Frequency (kHz) |
| VCC | 235 | 170 |
| Float | 345 | 255 |
| VREF | 485 | 355 |
| AGND | 620 | 460 |

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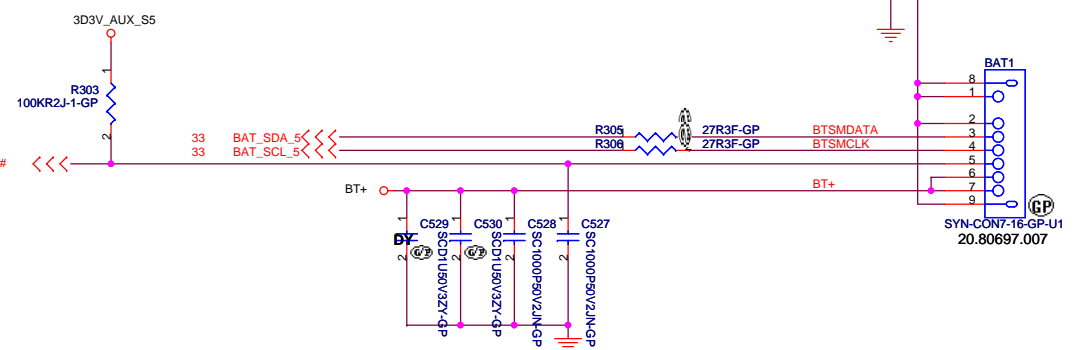
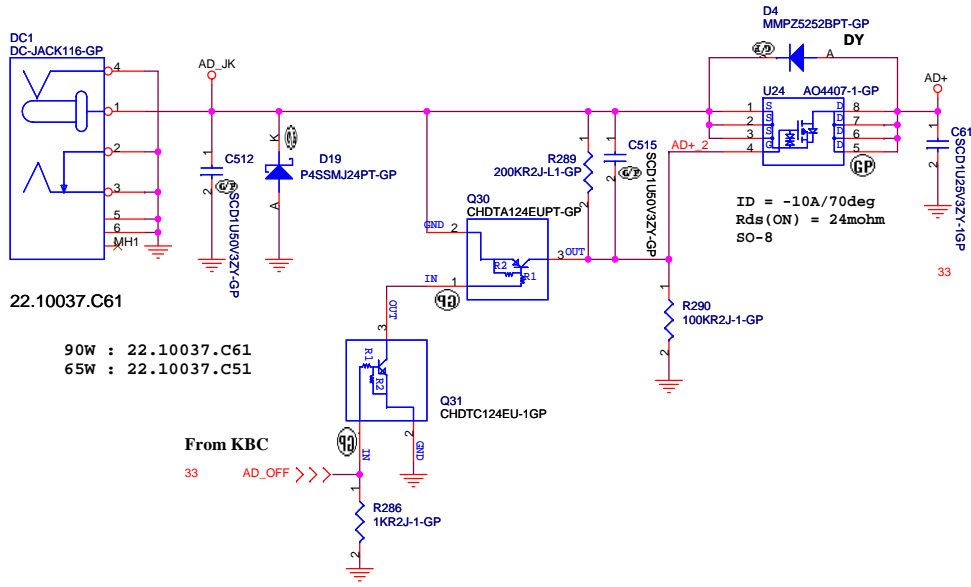
Title: DC / DC : 1D8V_S3 / 1D2V_CORE_S0 (MAX8743)

Size A3 Document Number: MYALL M Rev SA

Date: Friday, June 16, 2006 Sheet 43 of 59

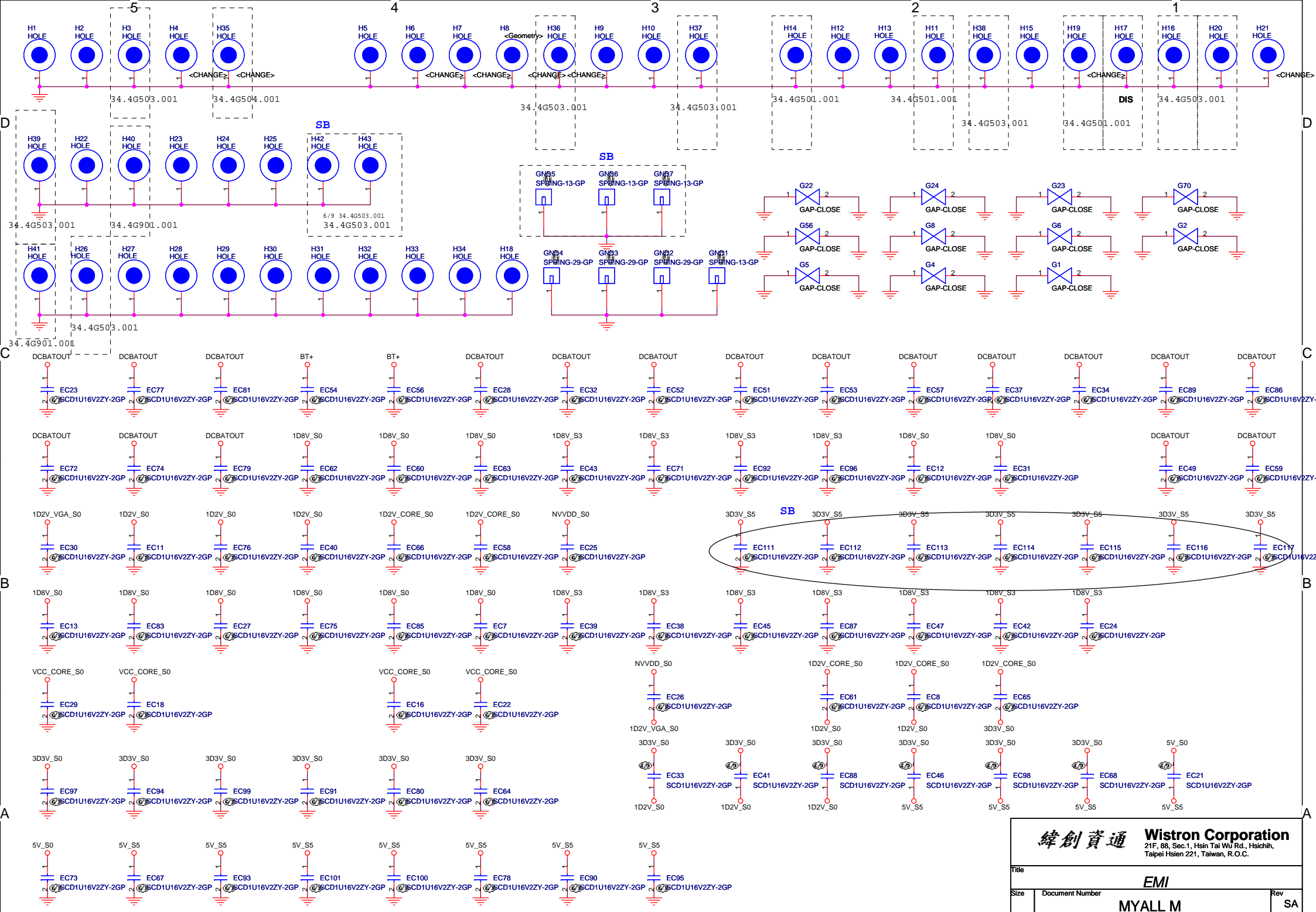
Adaptor-In to generate DCBATOUT

Battery connector



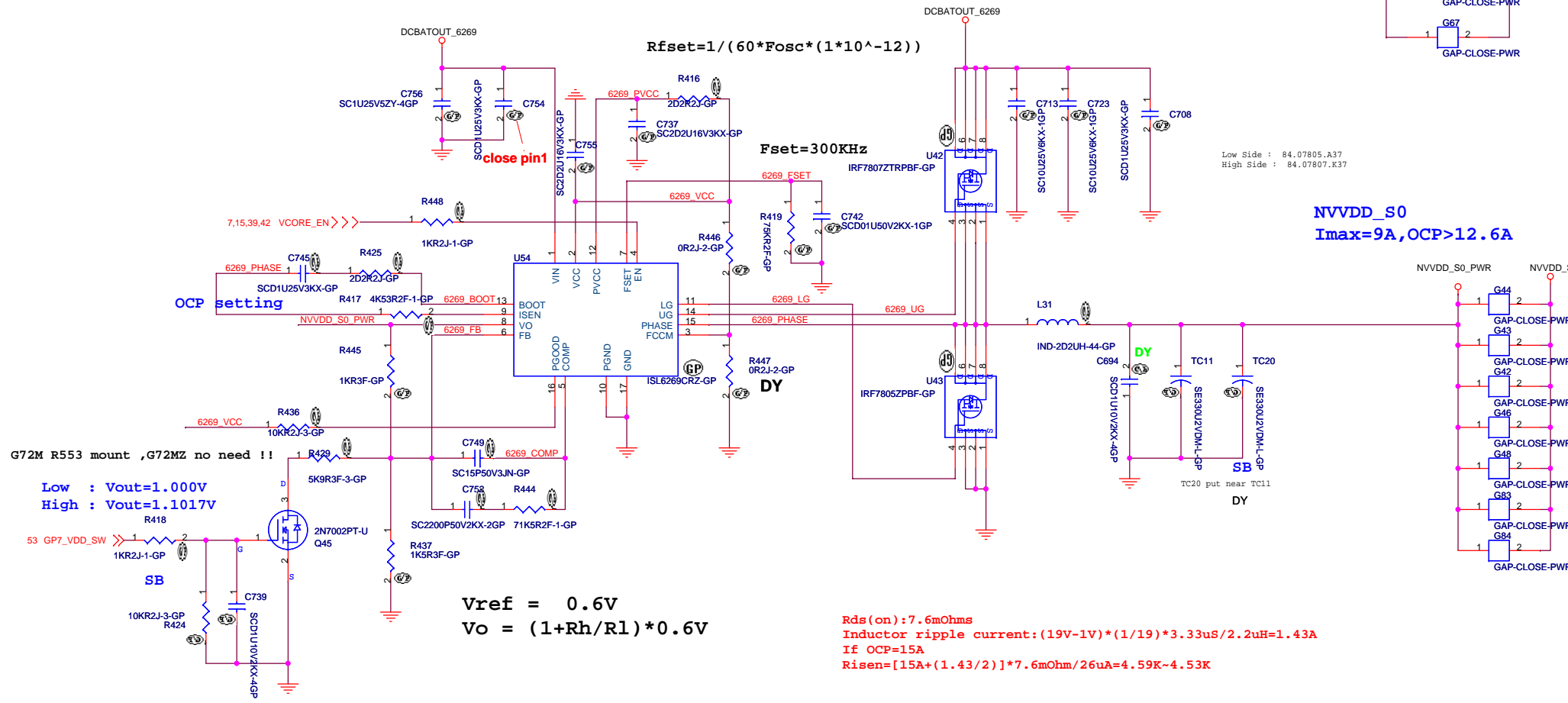
22.10037.C61
 90W : 22.10037.C61
 65W : 22.10037.C51

From KBC
 33 AD_OFF >>>



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| | | |
|-----------------------------|-----------------|-----|
| Title | | |
| EMI | | |
| Size | Document Number | Rev |
| | MYALL M | SA |
| Date: Friday, June 16, 2006 | Sheet 46 of 59 | |



$$R_{fset} = 1 / (60 * F_{osc} * (1 * 10^{-12}))$$

Fset=300KHz

OCP setting

Low : Vout=1.000V
High : Vout=1.1017V

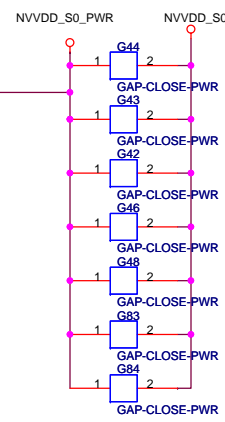
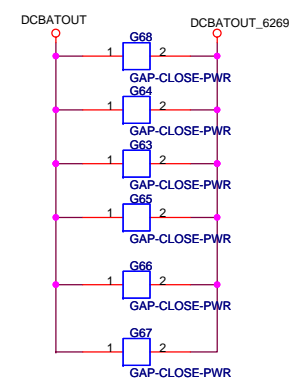
$$V_{ref} = 0.6V$$

$$V_o = (1 + R_h/R_l) * 0.6V$$

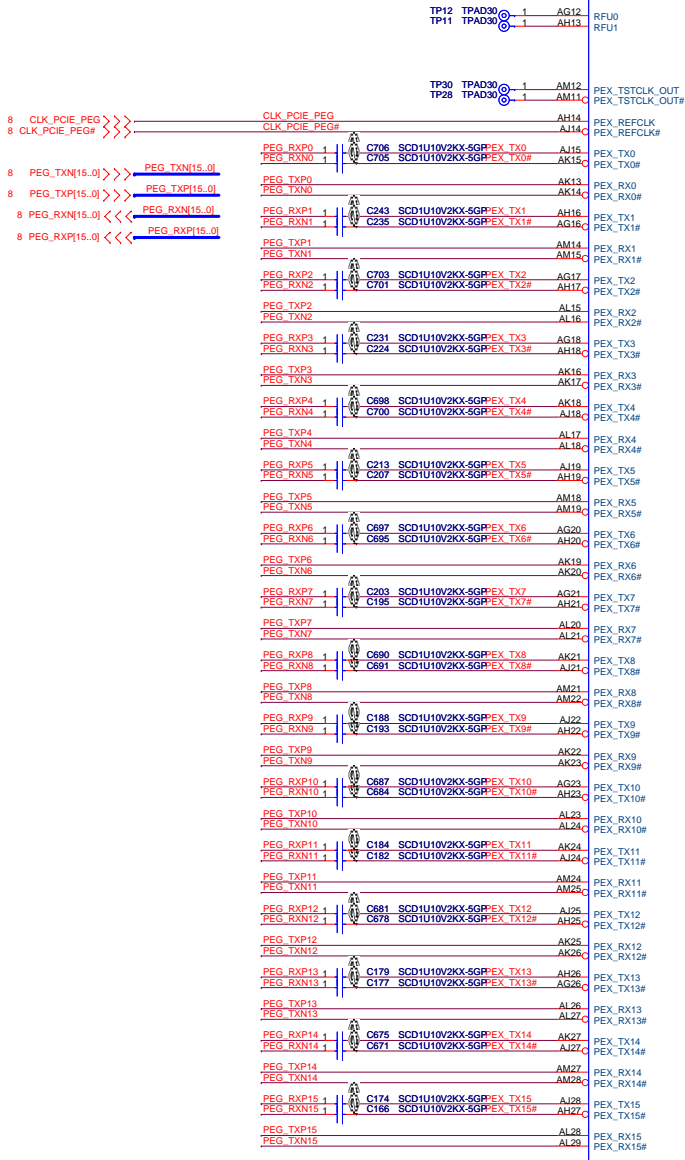
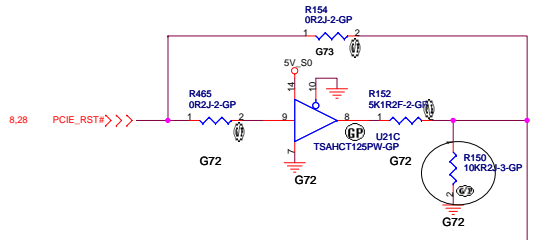
Rds(on) : 7.6mOhms
Inductor ripple current: $(19V-1V) * (1/19) * 3.33\mu s / 2.2\mu H = 1.43A$
If OCP=15A
Risen = $[15A + (1.43/2)] * 7.6m\Omega / 26\mu A = 4.59K \sim 4.53K$

Low Side : 84.07805.A37
High Side : 84.07807.K37

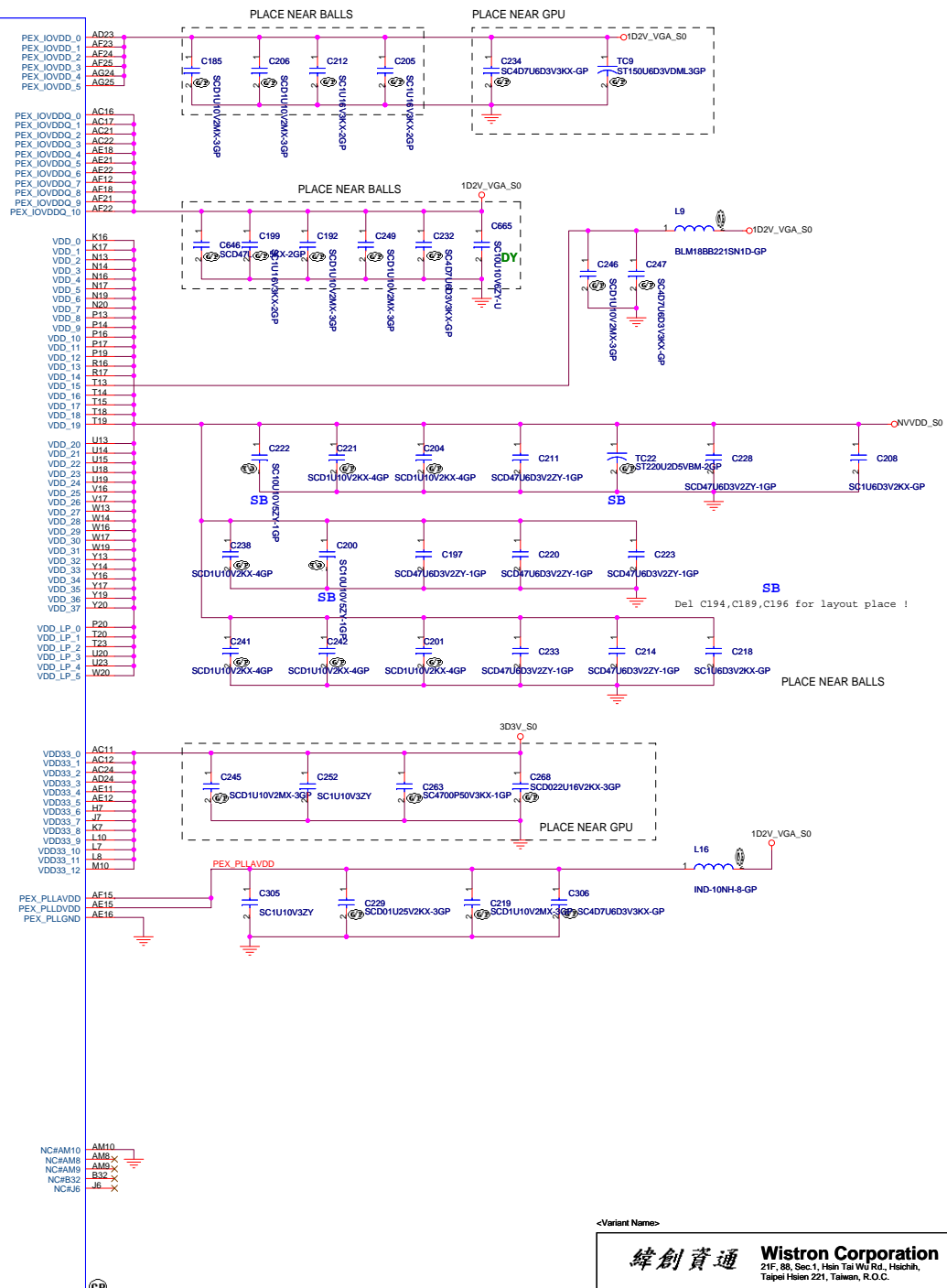
NVDD_S0
Imax=9A, OCP>12.6A



| | | |
|---|-----------------------------------|------------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| DC/DC NVDD_S0(ISL6269) | | |
| Title Size A3 | Document Number MYALL M | Rev SA |
| Date: Friday, June 16, 2006 Sheet 47 of 59 | | |



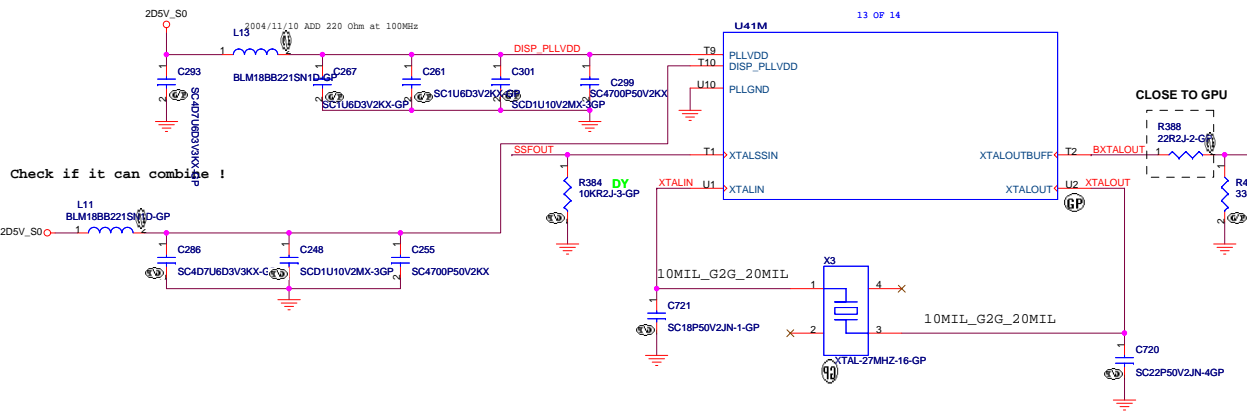
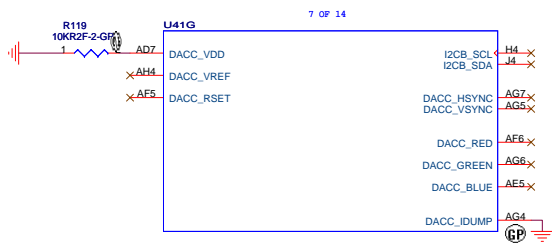
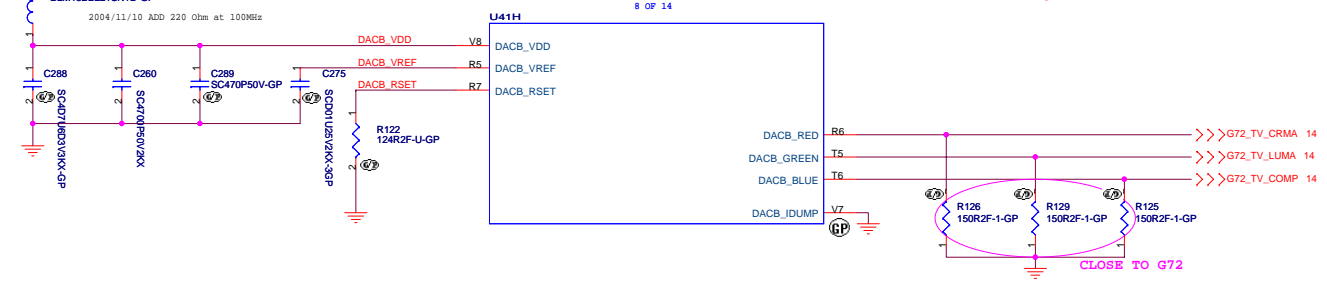
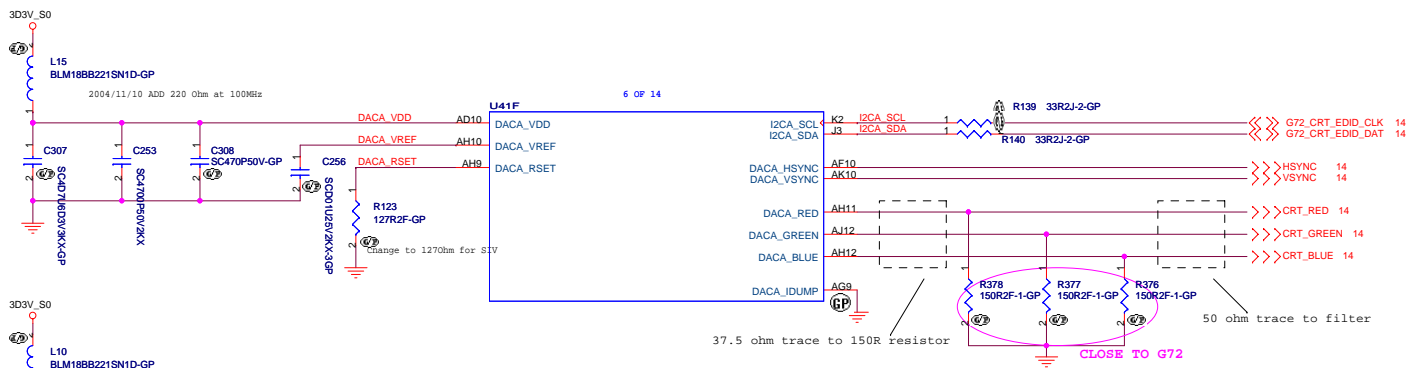
1 OF 14



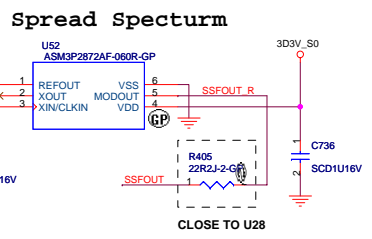
<Variant Name>

緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

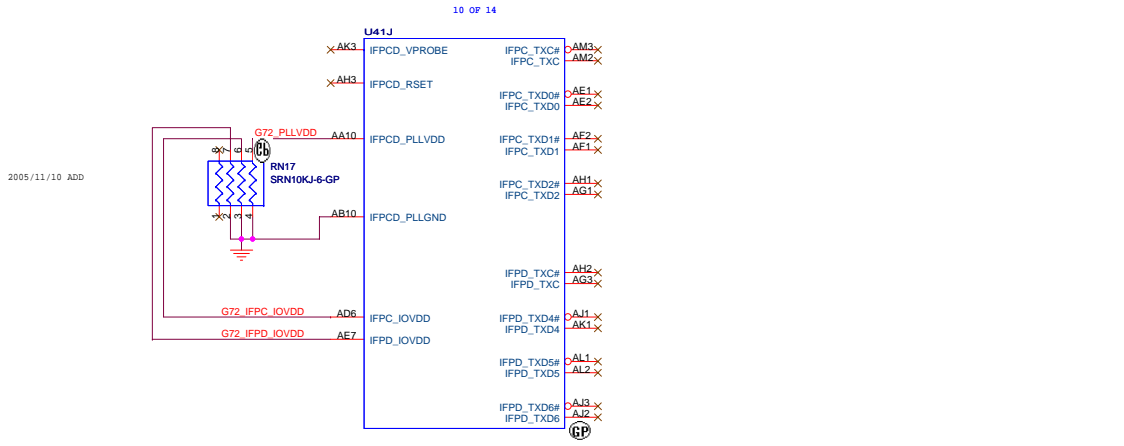
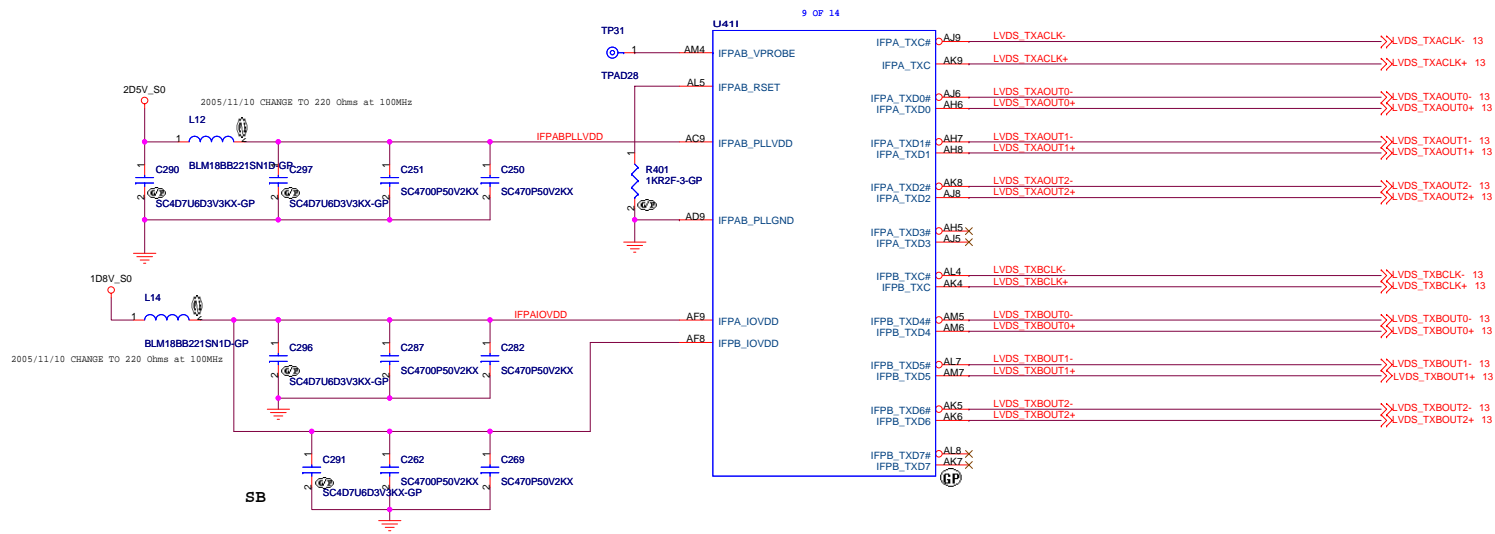
| | | | |
|-----------------------------|-----------------|------------------|----|
| Title | | G72M PCIE | |
| Size | Document Number | Rev | SA |
| | MYALL M | | |
| Date: Friday, June 16, 2006 | Sheet 48 | of 59 | |

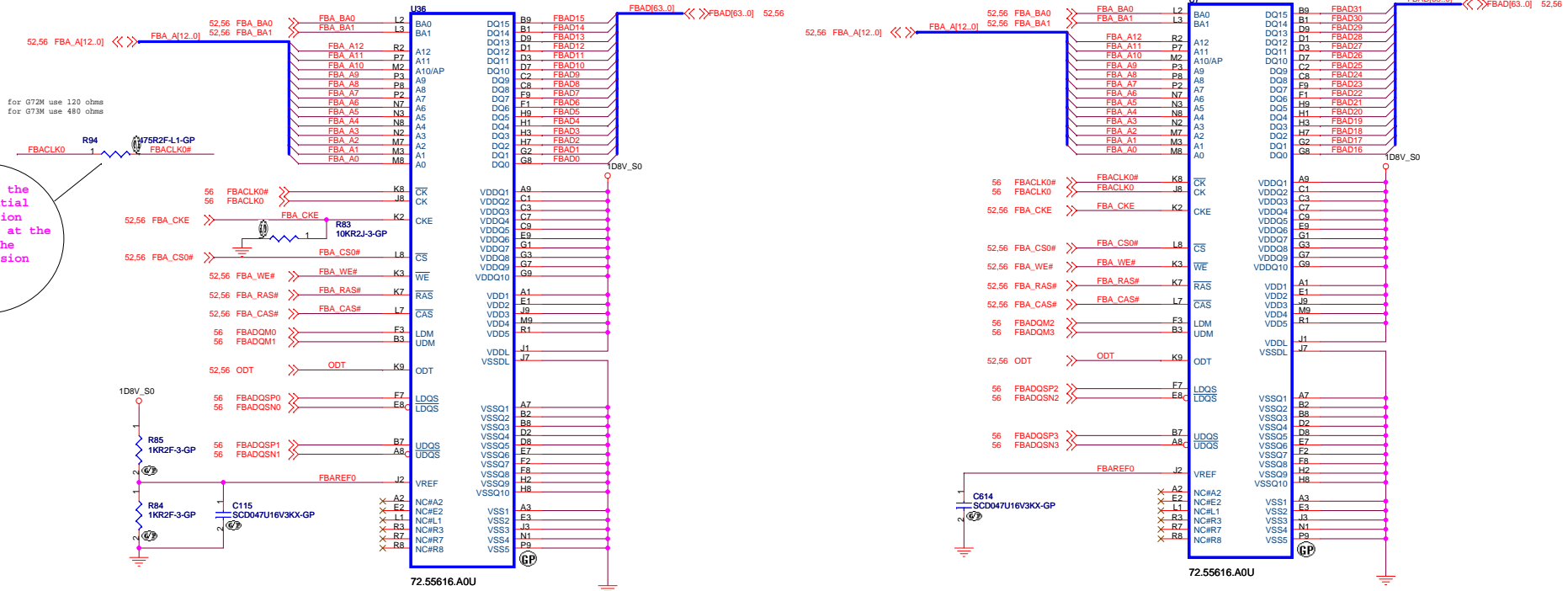


BIOS can do it ! check !! If no need XTALSSIN mount 10K!!

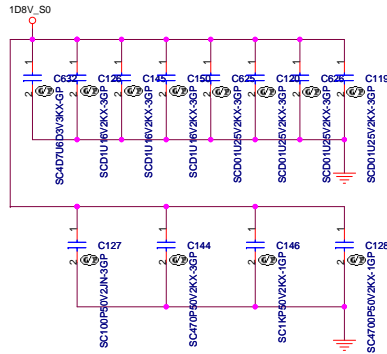


Check if it can combine !

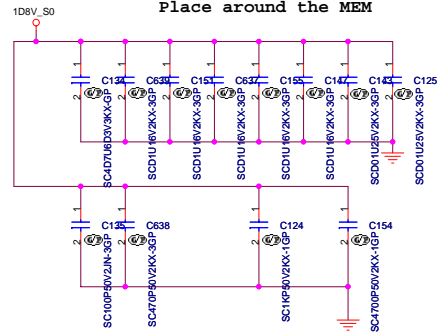




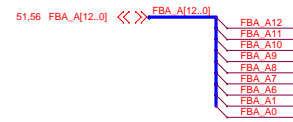
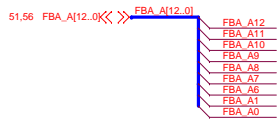
Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM

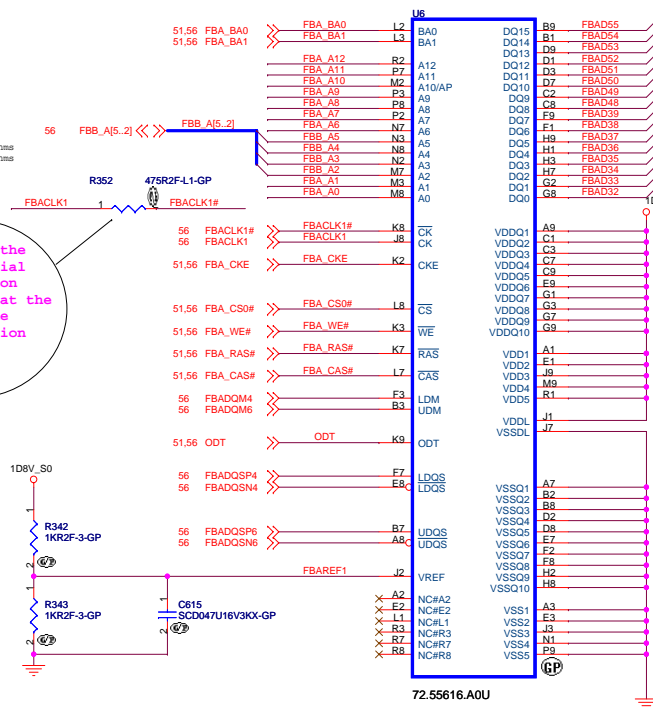


- 72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
- 72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
- 72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
- 72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by infineon(16M*16, 400Mhz)

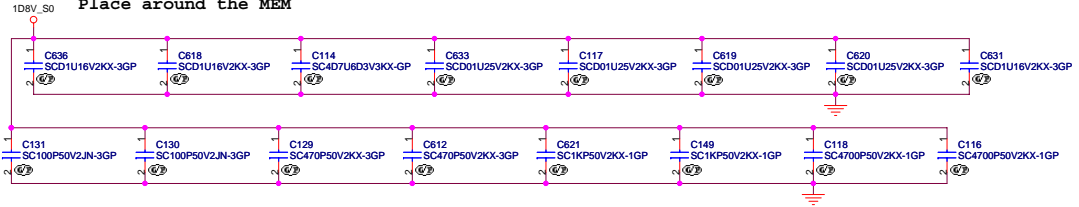


for 072M use 120 ohms
for 073M use 480 ohms

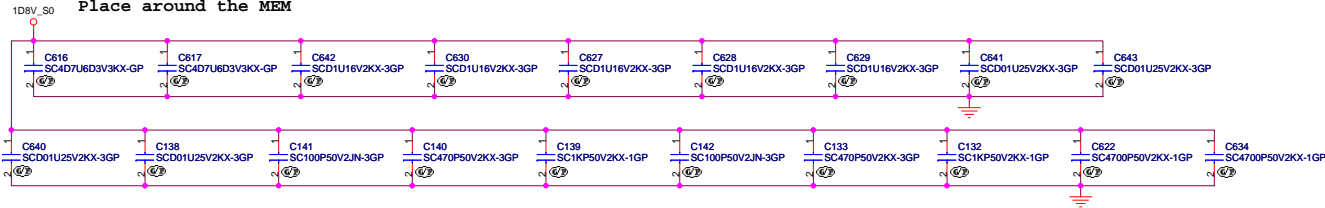
* "Place the differential termination resistor at the end of the transmission line"



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



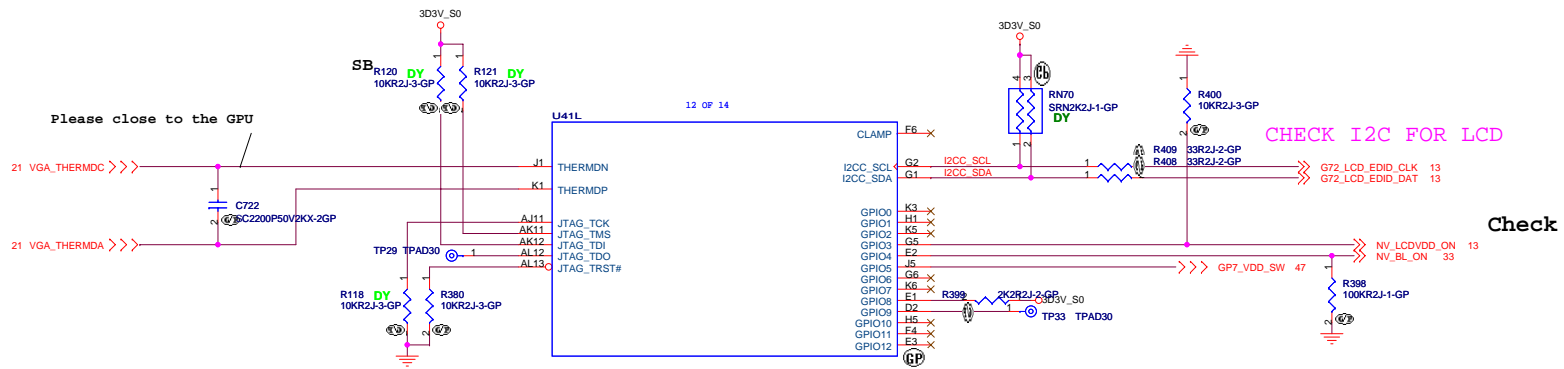
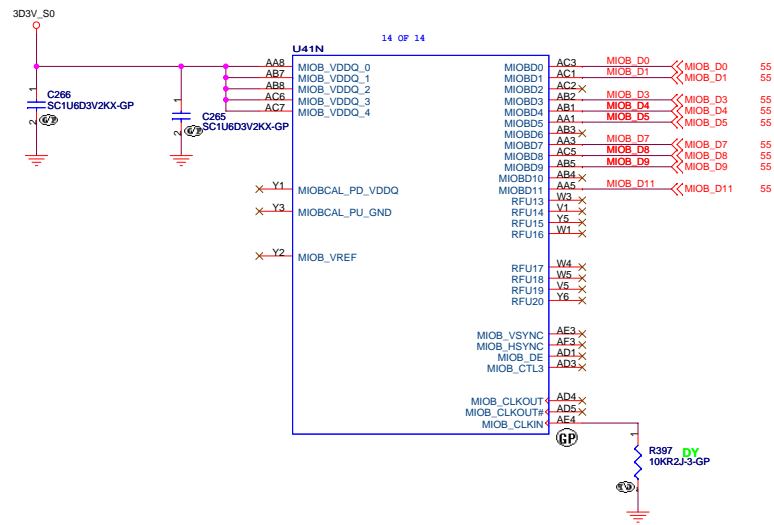
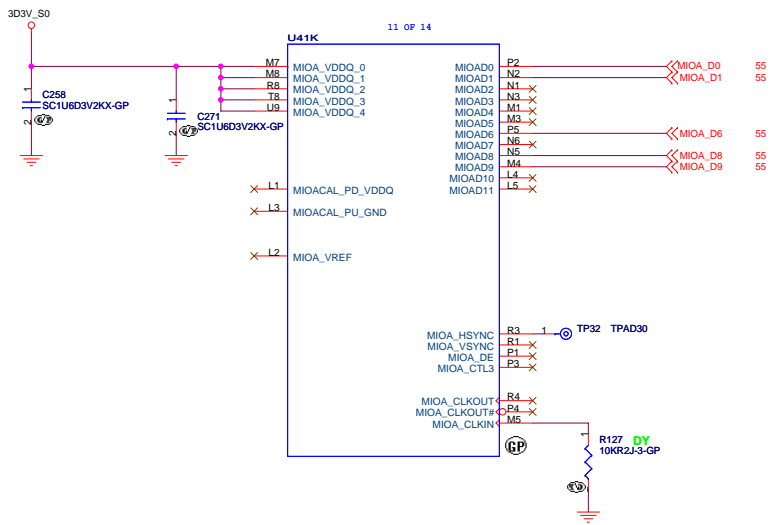
~Variant Name~

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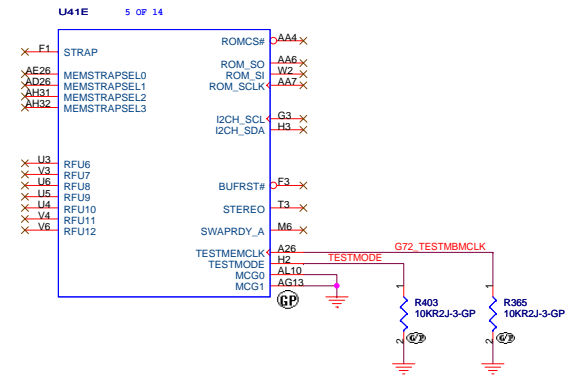
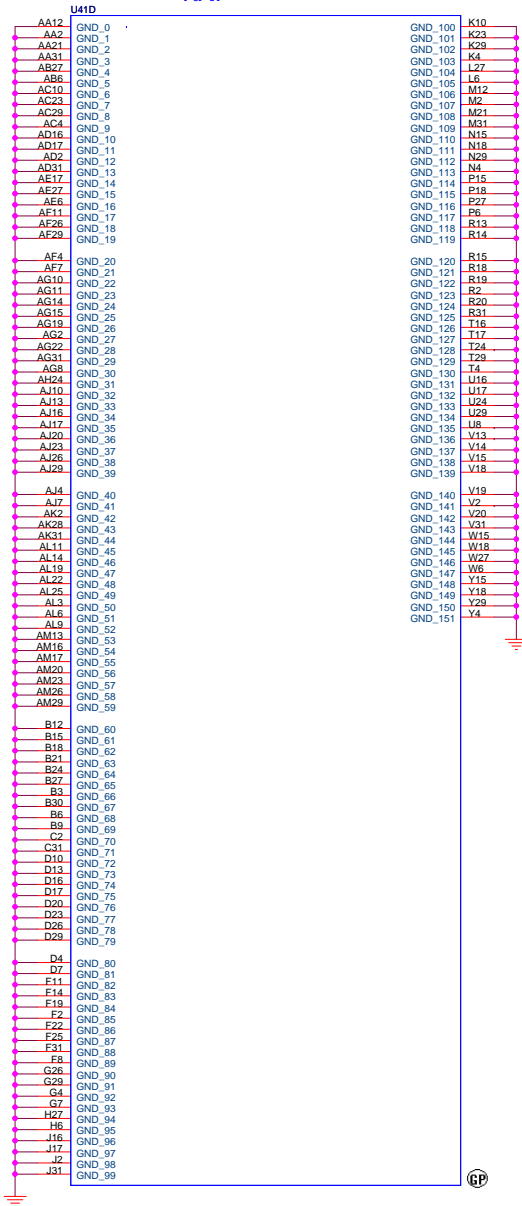
Title: **G72M VRAM (1ST 2/2)**

Size: Document Number: **MYALL M** Rev: **SA**

Date: Friday, June 16, 2006 Sheet 52 of 59



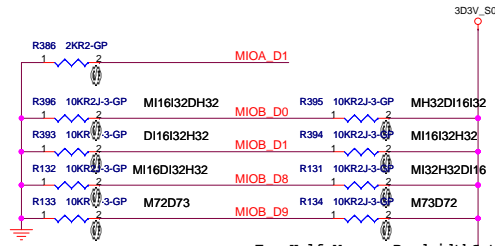
<-Variant Name>



STRAPS, Mechanical Parts

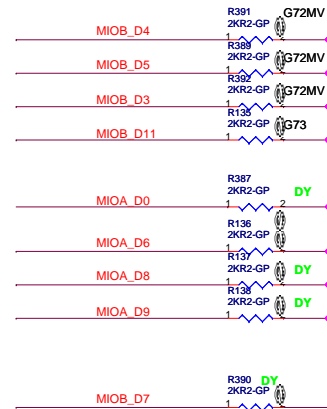
Check

| | | | | |
|-----------------|--------|--------|-------|--------|
| Hynix256MB : | R364_0 | R93_1 | R86_1 | R91_1 |
| Hynix128MB : | R364_0 | R370_0 | R86_1 | R91_1 |
| Hynix64MB : | R85_1 | R370_0 | R86_1 | R91_1 |
| Infineon256MB : | R364_0 | R93_1 | R86_1 | R369_0 |
| Infineon128MB : | R364_0 | R370_0 | R86_1 | R369_0 |
| Infineon64MB : | R85_1 | R370_0 | R86_1 | R369_0 |



For Half Memory BandwidthSet

| | | | |
|----|----------|----|----------|
| 53 | MIOA_D0 | << | MIOA_D0 |
| 53 | MIOA_D1 | << | MIOA_D1 |
| 53 | MIOA_D6 | << | MIOA_D6 |
| 53 | MIOA_D8 | << | MIOA_D8 |
| 53 | MIOA_D9 | << | MIOA_D9 |
| 53 | MIOB_D0 | << | MIOB_D0 |
| 53 | MIOB_D1 | << | MIOB_D1 |
| 53 | MIOB_D3 | << | MIOB_D3 |
| 53 | MIOB_D4 | << | MIOB_D4 |
| 53 | MIOB_D5 | << | MIOB_D5 |
| 53 | MIOB_D7 | << | MIOB_D7 |
| 53 | MIOB_D8 | << | MIOB_D8 |
| 53 | MIOB_D9 | << | MIOB_D9 |
| 53 | MIOB_D11 | << | MIOB_D11 |



| Bit Signal | Values |
|----------------------------------|---|
| MIOA_D1: SUB_VENDOR | 0 NO_BIOS 1 READ FROM BIOS |
| MIOB_D0: RAM_CFG_0 | 0000 RFU 0001 8Mx32 BGA 1.8V 0010 RFU 0011 RFU 0100 4Mx32 BGA 1.8V 0101 RFU 0110 RFU 0111 RFU 0011 16MX16 |
| MIOB_D1: RAM_CFG_1 | 1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU |
| MIOB_D8: RAM_CFG_2 | |
| MIOB_D9: RAM_CFG_3 | |
| MIOB_D2: CRYSTAL_0 | 00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN |
| MIOB_D6: CRYSTAL_1 | |
| MIOA_D7: TV_MODE_0 | 00 SECAM 01 NTSC 10 PAL 11 CRT |
| MIOA_D10: TV_MODE_1 | |
| MIOB_D4: PCI_DEVID_0 | |
| MIOB_D5: PCI_DEVID_1 | 1000 (default 0x00FC) |
| MIOB_D3: PCI_DEVID_2 | |
| MIOB_D11: PCI_DEVID_3 | 0111 G72MV G72MZ=6 , G73=8 |
| MIOA_D0: PEX_PLL_EN_TERM100 | 0 ENABLED 1 DISABLED |
| MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0] | 0 DESKTOP 1 MOBILE |
| MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1] | |
| MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2] | 010 DEFAULT |
| MIOB_D7: MOBILE_GPIO | 0 GPIO_PULLDN 1 GPIO_FLOAT |

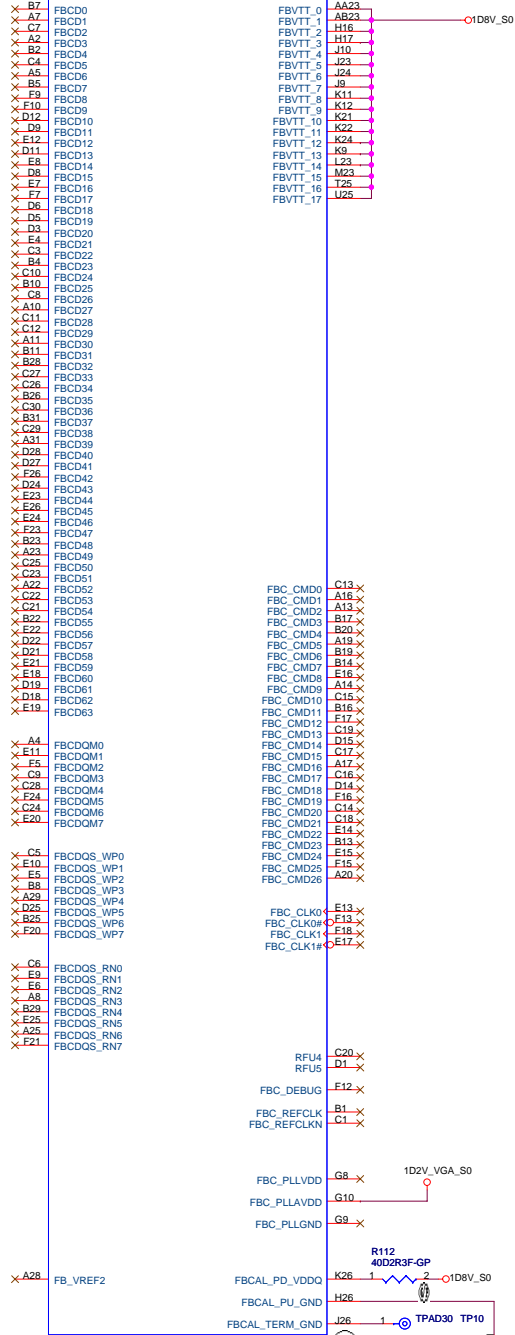
For MEM strapping, Please use below table:

| RAM_CFG[3:0] | Config | FB Bus Width | Definitions |
|--------------|-------------|--------------|-------------|
| 0000 | 16Mx16 DDR2 | 64-bit | Elpida |
| 0001 | 16Mx16 DDR2 | 64-bit | Samsung |
| 0010 | 16Mx16 DDR2 | 64-bit | Infineon |
| 0011 | 16Mx16 DDR2 | 64-bit | Hynix |
| 0100 | 32Mx16 DDR2 | 64-bit | Elpida |
| 0101 | 32Mx16 DDR2 | 64-bit | Samsung |
| 0110 | 32Mx16 DDR2 | 64-bit | Infineon |
| 0111 | 32Mx16 DDR2 | 64-bit | Hynix |

<-Variant Name>

| | | | |
|-----------------------------|-----------------|--|----|
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| | | 21F, 88, Sec-1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
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| G72M STRAPPING | | | |
| Size | Document Number | Rev | SA |
| | MYALL M | | |
| Date: Friday, June 16, 2006 | | | |
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U41C



NOTE

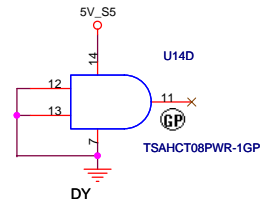
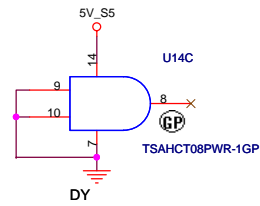
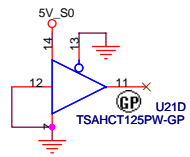
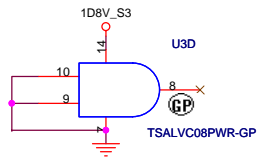
G73 R549 : 64.40R25.6DL
G72 : 64.30R15.6DL

<Variant Name>

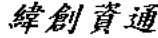
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| | MYALL M | SA |



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| Title | |
| Unused CMOS/TTL | |
| Size | Document Number |
| A3 | MYALL M |
| Date: | Rev |
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SA 4/18 Add R414~R417 for headphone sound decrease

4/21 Add R718-R720,Q45-Q47 for discharge circuit
Add U68,R721-R725 ,C917-C923 for 1D2V_S0
Add U69,R726~R730,C924-C929 for 1D2V_VGA_S0

4/24 Update GPIO ,check Lan , Add bead into NB,SB's power

4/26 Correct CRT,TV bead and cap , Add EMI cap ,Change Transformer according vender's suggest

4/28 Change spec to Phy

5/4 Reduce Lan cap

SB 5/18 R144 chang to 64.30R15.6DL,Correct SB P/N

5/25 Correct VRAM setting; D9 become mount , C79 become lu for sometimes can't power on !

6/1 Del RN9 for redudant ; Correct BTSMCLK,BTSMCLK;Dummy R244,EC102-EC104; Change C451,C458 to 4.7u ! ; U20 mount , R248 Dummy; Del RN64-1 AMP_SHUTDOWN;
Change XF1 and XF2 CT to AVDD18 for WOL ;Change C504 to 78.1022N.24L; Add WEBCAM_PW_SW at KBC GPIO27, and U66,F1,F2,C875,R284

6/5 Power , CPU High Side : 84.79N03.037,Low Side : 84.32N03.037 ,Dummy Q42, Q44 ; R159 , 64.66515.6DL ;TC13 change to 79.22719.20L;
R434 change to 64.40235.6DL;R404,R402 change to 64.18015.55L;Q21,R153,C311 Dummy ; Change SKU;Change U49,U50,U45,U46 to 84.04468.037

6/8 Q39 change to 84.27002.F31 ! Add D31,RN87,R576 for Leakage !(Ask KBC change DA2 to open drain);Change R111 source power to 5V_S5_G913

6/9 Add R577-R579 for Dis impedance; Add H42,H43 for ME request;Correct AV-IN pin ;

6/10-13 Add U66,F1,F2,R284,C875 for power switch ! ; add R597,R598 for brightness choice from KBC or SB ; Del Q33,Q32 to reduce MOS ; Change RN37 to 0 Ohm;
Bluetooth_EN change to KBC control; Add CIR_DET(R586,R587);DY RN21 for redudant;Change X4 for vender's suggestion;change C34 and C30 for vender's suggestion;
Add TC21 for accoustic noise;add EC105-EC111,Mount ERC7,ERC8,GND5-GND7 for EMI request;

6/14 Del R46,Change R47 to bigger one ,Change C55 to 10U,add C880 --> for 1D2V_S0 power quality

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| Size | Document Number | Rev | SA |
| | MYALL M | | |
| Date: Friday, June 16, 2006 | Sheet 59 | of | 59 |