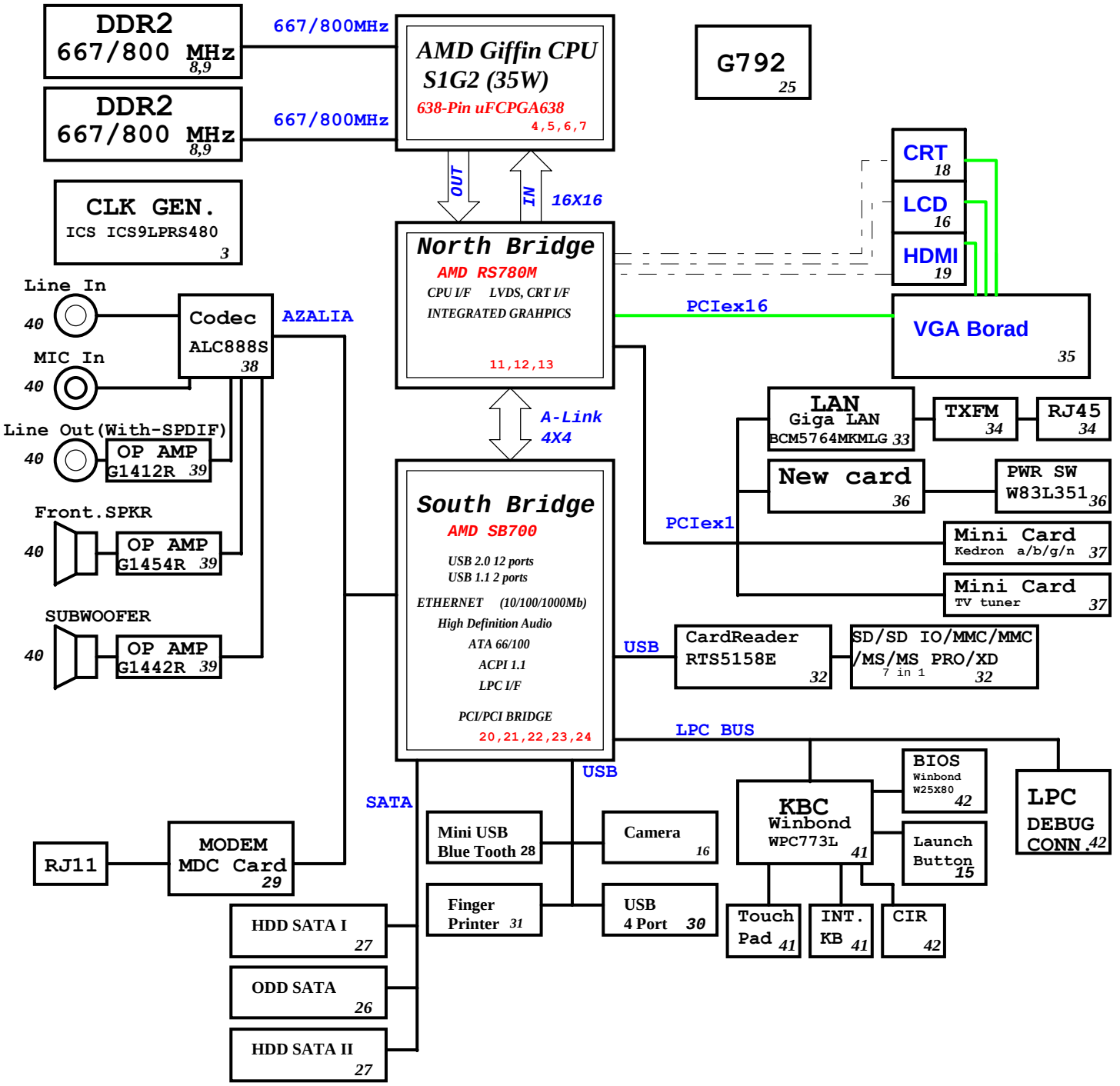
Big Bear 2A (AS 18") Block Diagram

Project code: 91.4AJ01.001
PCB P/N : 48.4AJ01.001
REVISION : 08208-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 48	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 50	
1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)

RT9166 50	
3D3V_S0	2D5V_S0 (300mA)

G957 50	
3D3V_S0	1D5V_S0(1A)

G9161 50	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731A 51	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Big Bear 2A	SC

Date: Monday, October 27, 2008 Sheet 1 of 55

<Core Design>

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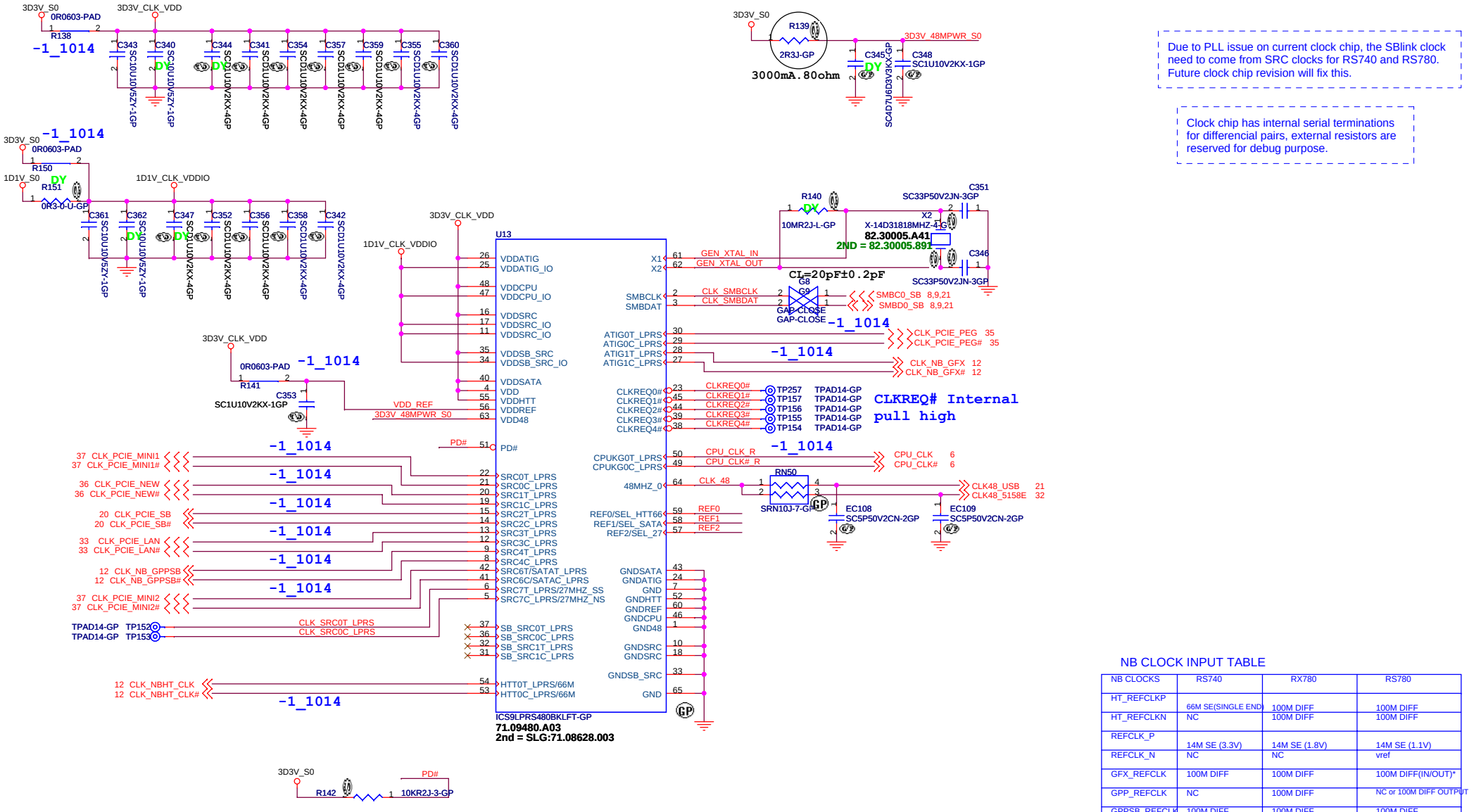
Title
HISTORY

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 2 of 55



SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

* default

CPU_CLK(200MHz)

OSC_14M_NB
RS780M 1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

<Core Design>

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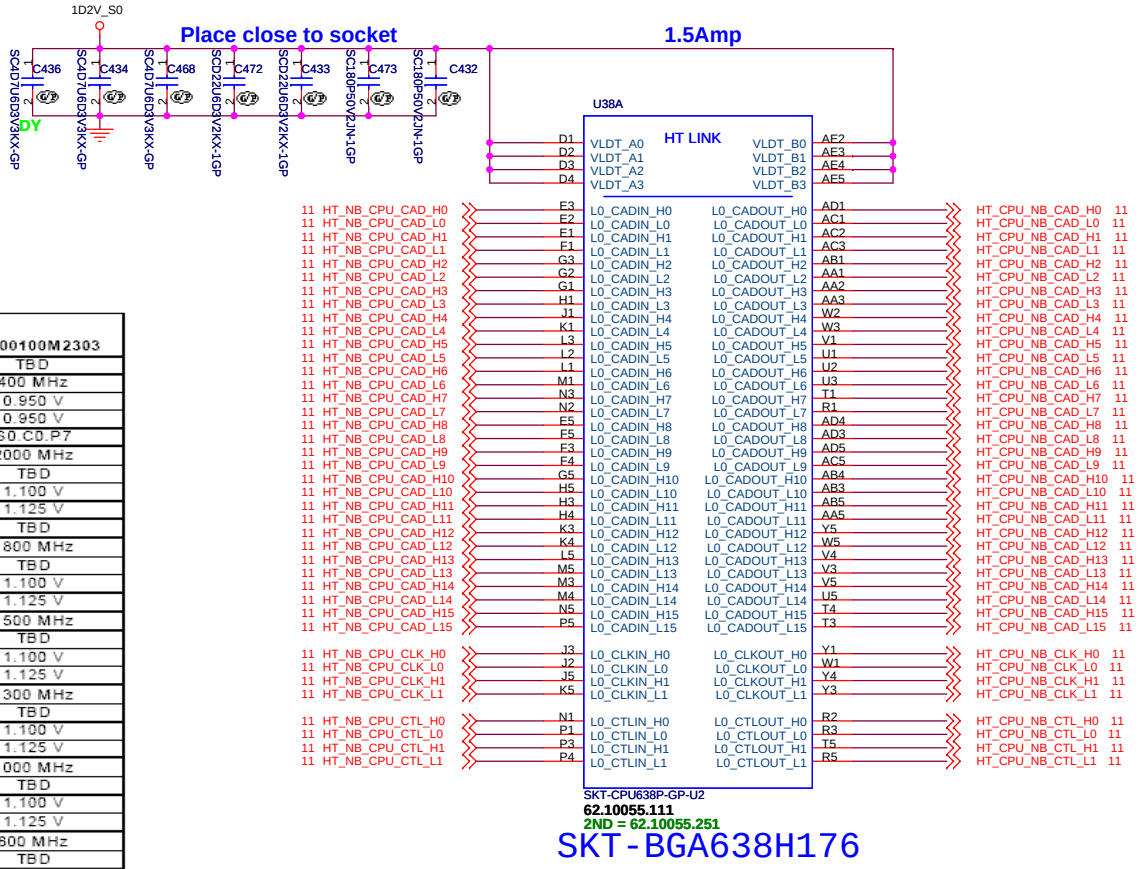
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 3 of 55



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

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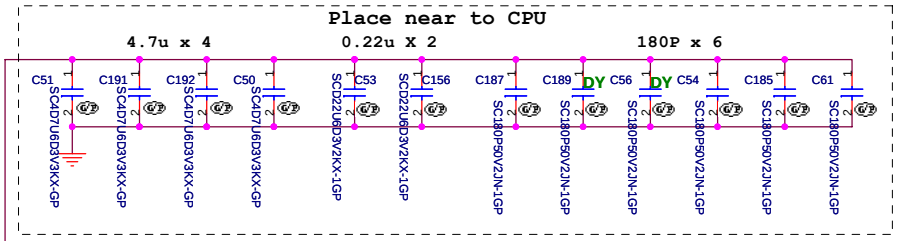
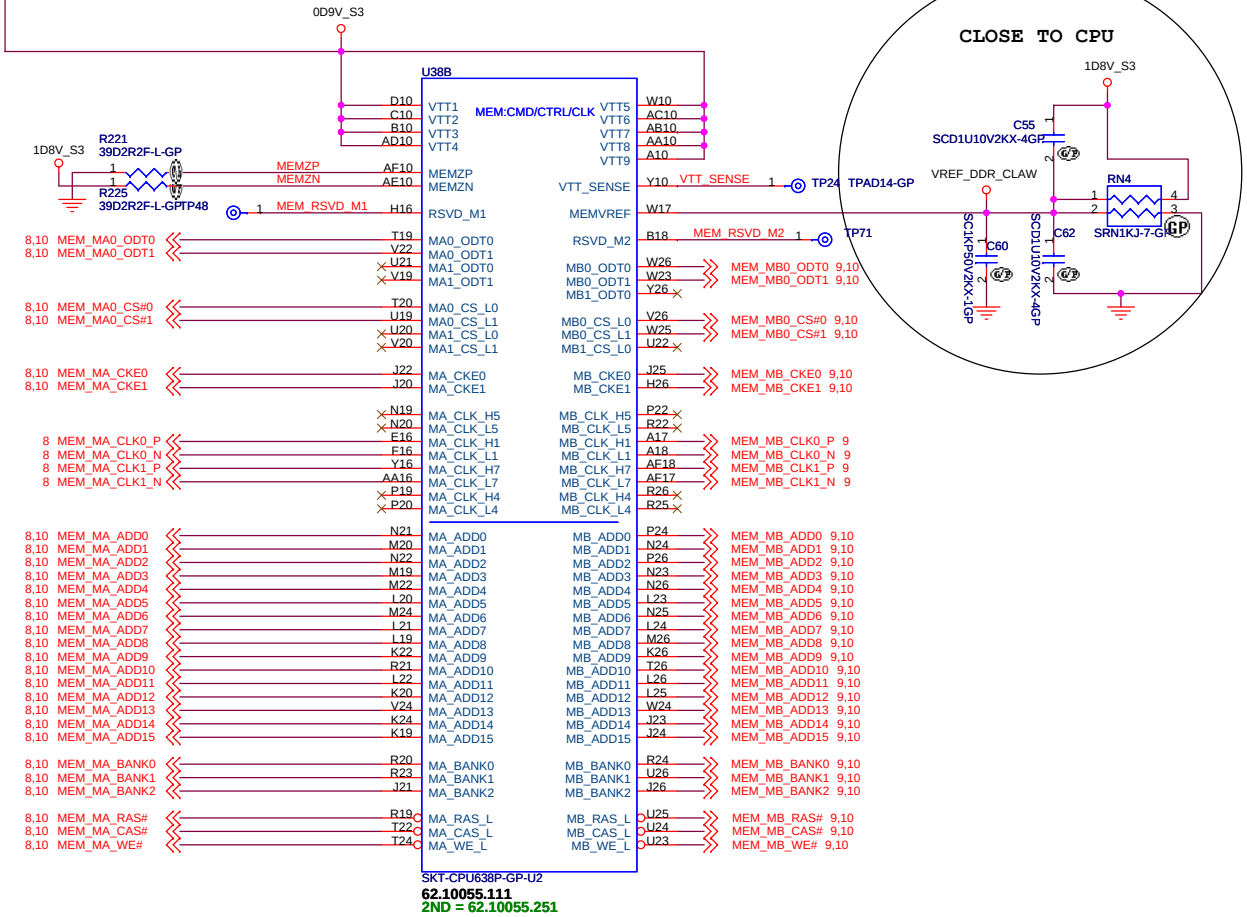
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

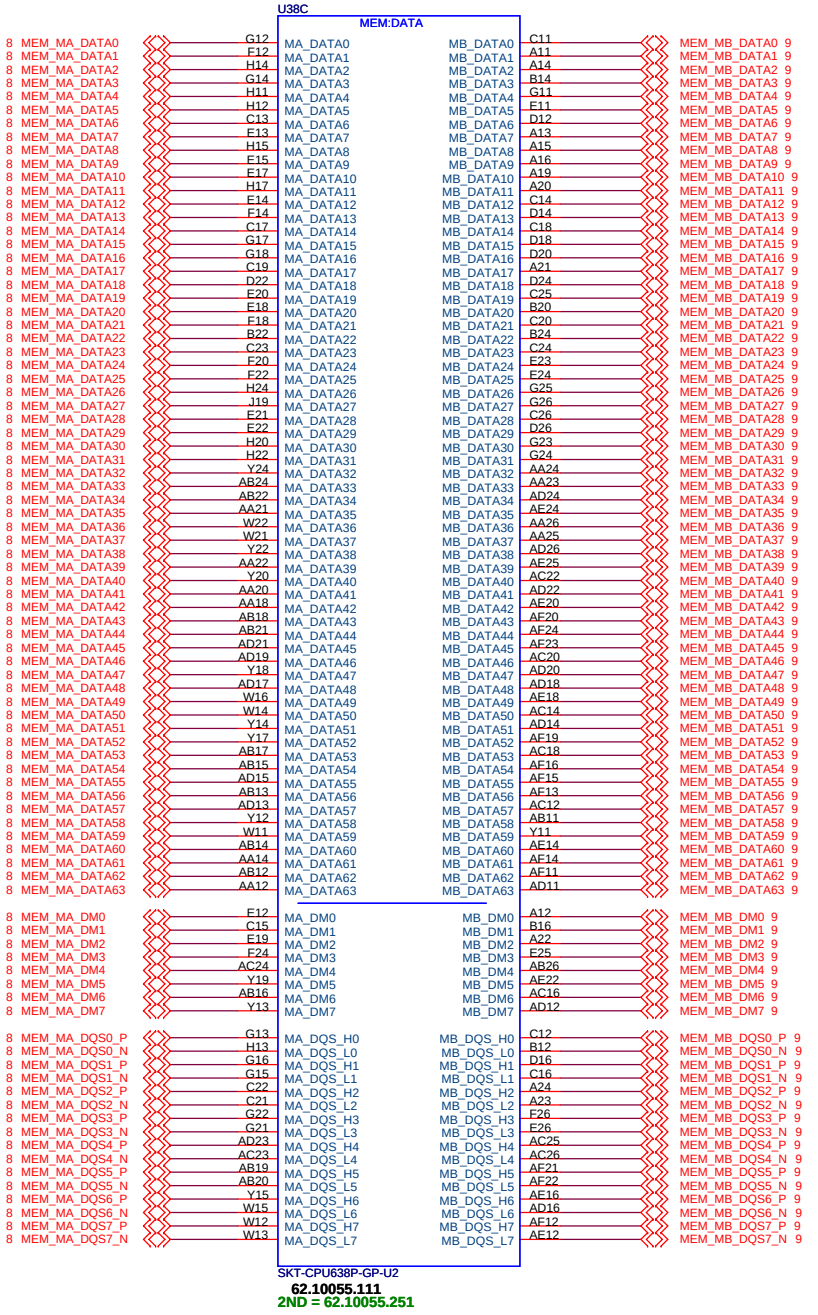
Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 4 of 55







<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 5 of 55

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

1D8V_S0
RN31 SRN300J-1-GP
-1_1014
20,53 CPU_LDT_RST# — R257 0R0402-PAD — LDT_RST#_CPU
20,53 CPU_PWRGD — R258 0R0402-PAD — LDT_PWROK
20 CPU_LDT_STOP# — R62 0R0402-PAD — LDT_STP#_CPU 12
12,20 ALLOW_LDTSTOP — R255 0R0402-PAD — CPU_LDT_REQ#_CPU
SB with 0402 PAD

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
2D5V_S0 — R55 0R3-0-U-GP — 2D5V_VDDA_S0
C162 DY SC10U10V5ZY-1GP
C163 SC4D7U6D3V3KX-2GP
C153 SC3300P50V2KX-1GP
C164 SC3300P50V2KX-1GP
C161 SCD22U10V3KX-2GP
Cloce To CPU
3 CPU_CLK — C481 SC3900P50V2KX-2GP — R263 169R2F-GP — CLKCPU_IN
3 CPU_CLK# — C488 SC3900P50V2KX-2GP — CLKCPU# IN
LDT_RST# CPU
HDT_RST# — R256 0R0402-PAD
For HDT DBG
1D2V_S0 — R48 44D2R2F-GP — R49 44D2R2F-GP
46 CPU_VDD0_RUN_FB_H
46 CPU_VDD0_RUN_FB_L
46 CPU_VDD1_RUN_FB_H
46 CPU_VDD1_RUN_FB_L
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
TP69 CPU_TEST23
CPU_TEST18
CPU_TEST19
TP65 CPU_TEST25_H
TP64 CPU_TEST25_L
CPU_TEST21
TP176 CPU_TEST20
CPU_TEST24
CPU_TEST22
CPU_TEST12
CPU_TEST27
RN84 SRN300J-1-GP — R254 0R0402-PAD — CPU_TEST9
TPAD14-GP180 CPU_SIC
TPAD14-GP175 CPU_SID
TPAD14-GP174 CPU_ALERT#
CPU_HTREF0
CPU_HTREF1

U38D
VDDA1 VDDA2 CLKIN_H CLKIN_L RESET_L PWROK LDTSTOP_L LDTREQ_L SIC SID ALERT_L HT_REF0 HT_REF1 VDD0_FB_H VDD0_FB_L VDD1_FB_H VDD1_FB_L DBRDY TMS TCK TRST_L TDI TEST23 TEST18 TEST19 TEST25_H TEST25_L TEST21 TEST20 TEST24 TEST22 TEST12 TEST27 TEST9 TEST6 RSVD1 RSVD2 RSVD3 RSVD4 RSVD5
KEY1 KEY2 SVC SVD THERMTRIP_L PROCHOT_L MEMHOT_L THERMDC THERMDA VDDIO_FB_H VDDIO_FB_L VDDNB_FB_H VDDNB_FB_L DBREQ_L TDO TEST28_H TEST28_L TEST17 TEST16 TEST15 TEST14 TEST7 TEST10 TEST8 TEST29_H TEST29_L RSVD10 RSVD9 RSVD8 RSVD7 RSVD6
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251

1D8V_S3
RN30 SRN1KJ-7-GP
A6 CPU_SVC 46
A4 CPU_SVD 46
RN65 SRN300J-1-GP
CPU_TEST27
CPU_DBREQ#
R433 300R2J-4-GP DY
-1_1014
AF6 THERMTRIP#
AC7 PROCHOT#
AA8 CPU_MEMHOT#
R227 0R0402-PAD — PROCHOT#_SB 20
internal pull high 300 ohm
W7 H_THERMDC 25
W8 H_THERMDA 25
C58 DY SC100P50V2JN-3GP
W9 CPU_VDDIO_SUS_FB_H — TP28
Y9 CPU_VDDIO_SUS_FB_L — TP27
H6 CPU_VDDNB_RUN_FB_H 46
G6 CPU_VDDNB_RUN_FB_L 46
E10 CPU_DBREQ#
AE9 CPU_TDO
J7 CPU_TEST28_H — TP52
H8 CPU_TEST28_L — TP54
D7 CPU_TEST17 — TP68
E7 CPU_TEST16 — TP63
F7 CPU_TEST15
C7 CPU_TEST14
C3
K8
C4
C9 CPU_TEST29H — TP184
C8 CPU_TEST29L — TP185
H18 H19 AA7 D5 C5

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

-1_1014
46 CPU_PWRGD_SVID_REG — R259 0R0402-PAD — LDT_PWROK
C483 DY SCD1U16V2ZY-2GP
Near CPU PIN

LDT_PWROK
R261 2K2R2J-2-GP
C482 1D8V_3US_Q2 SCD1U16V2ZY-2GP
Q21 MMBT3904-4-GP
THERMTRIP# — KBC_THERMTRIP# 25,41
84.T3904.C11
2ND = 84.03904.T11
CPU exceeds to 125℃

CPU_TEST19 — R226 300R2J-4-GP DY
CPU_TEST18 — R45 300R2J-4-GP DY
CPU_TEST14 — R431 300R2J-4-GP DY
CPU_TEST15 — R432 300R2J-4-GP DY

HDT Connectors

CPU_DBREQ#	TP17	TPAD14-GP
CPU_DBRDY	TP50	TPAD14-GP
CPU_TCK	TP21	TPAD14-GP
CPU_TMS	TP23	TPAD14-GP
CPU_TDI	TP20	TPAD14-GP
CPU_TRST#	TP19	TPAD14-GP
CPU_TDO	TP18	TPAD14-GP
1D8V_S3	TP29	TPAD14-GP
HDT_RST#	TP183	TPAD14-GP

<Core Design>

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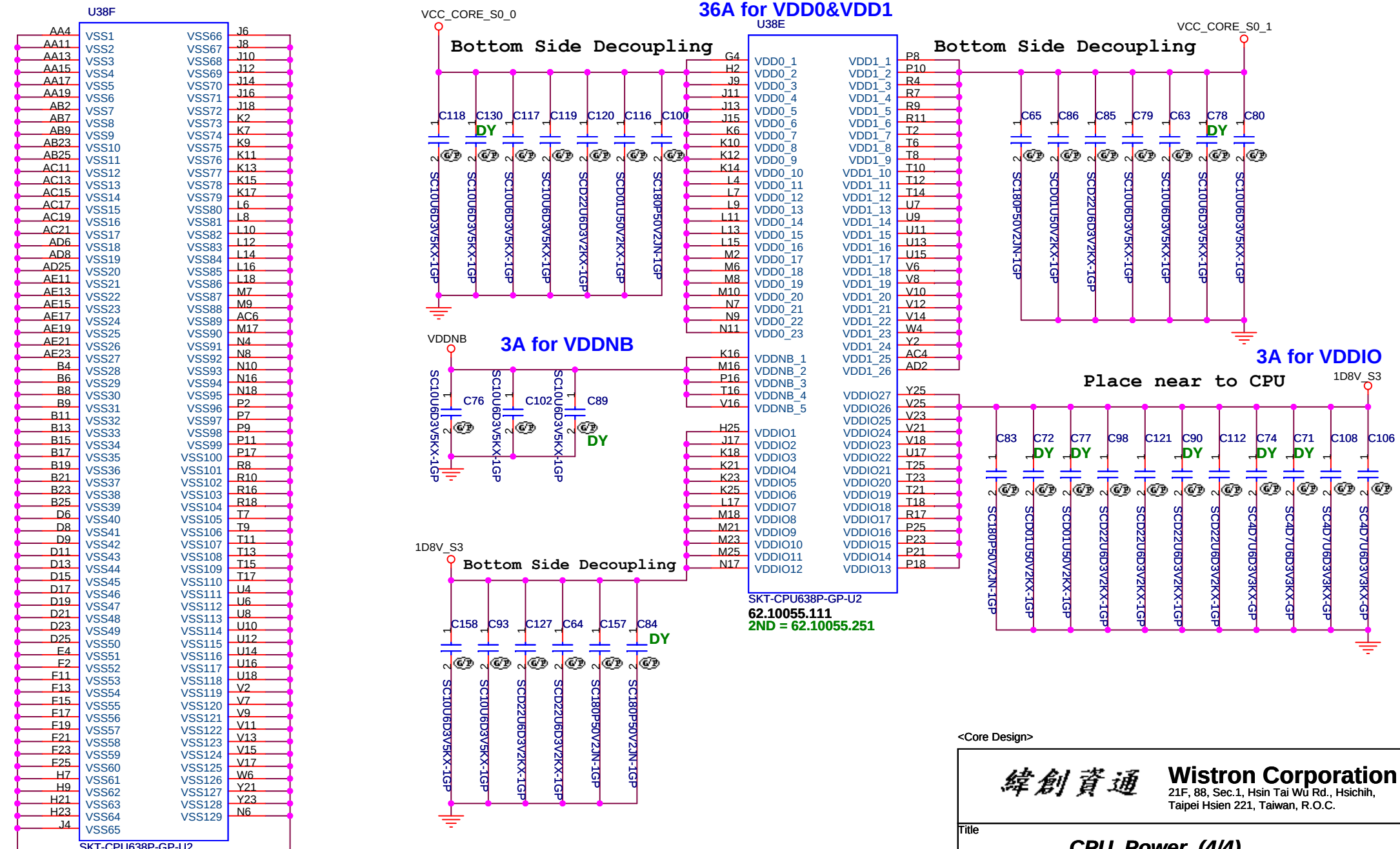
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)
Size: A3 | Document Number: Big Bear 2A | Rev: SC
Date: Monday, October 27, 2008 | Sheet 6 of 55



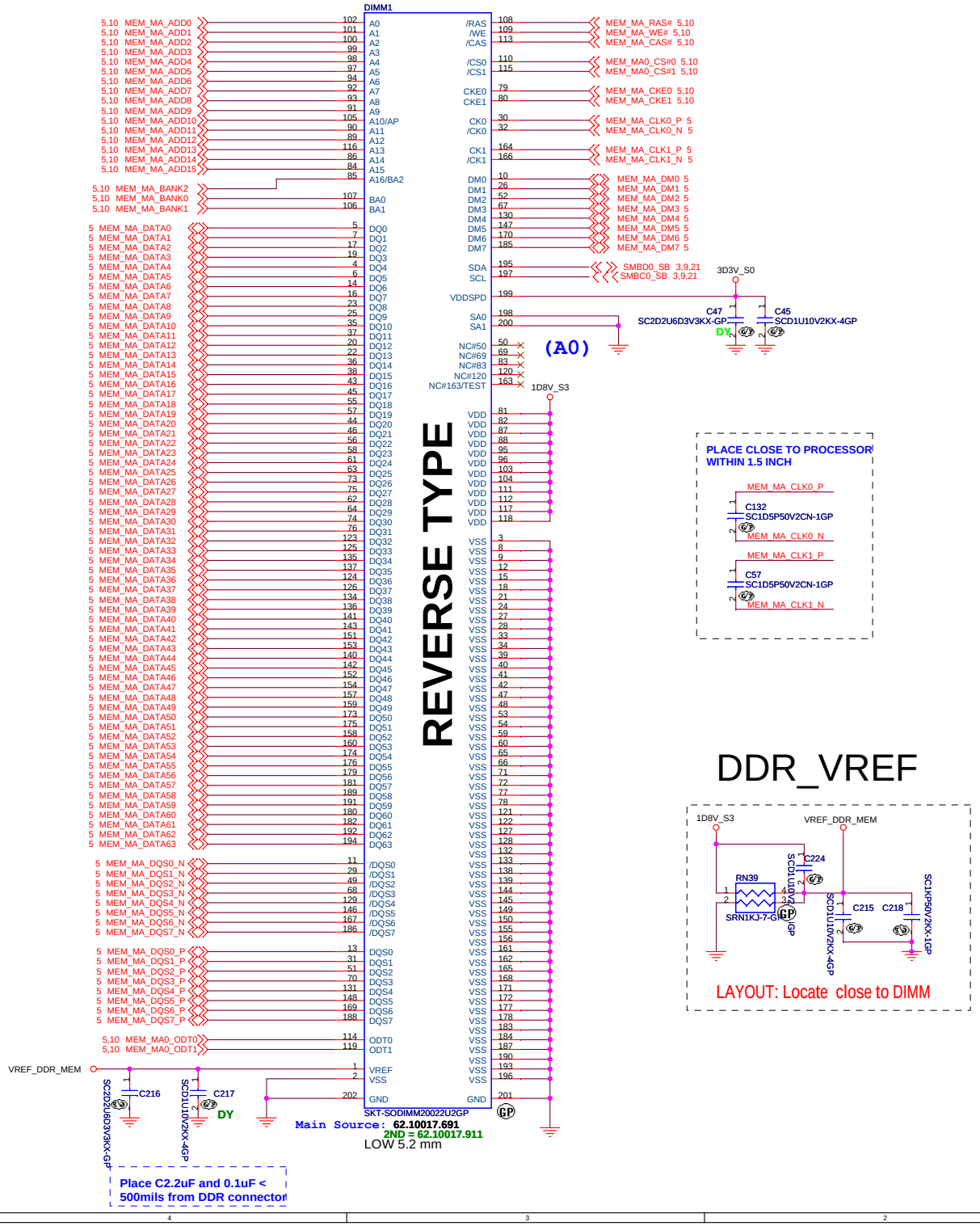
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_Power_(4/4)***

Size	Document Number	Rev
A4	**Big Bear 2A**	SA

Date: Monday, October 27, 2008 Sheet 7 of 55



<Core Design>

Wistron Corporation
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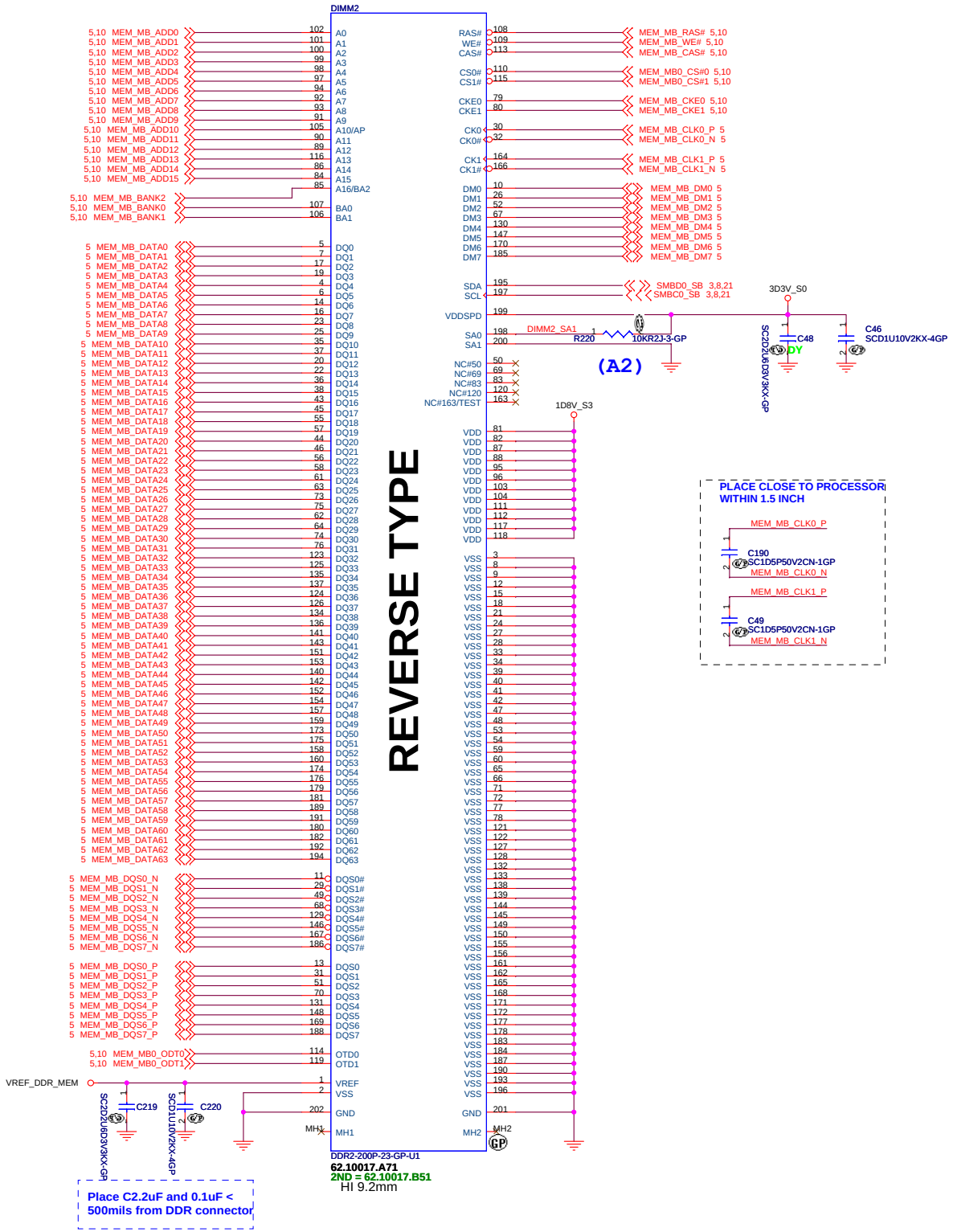
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 8 of 55



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

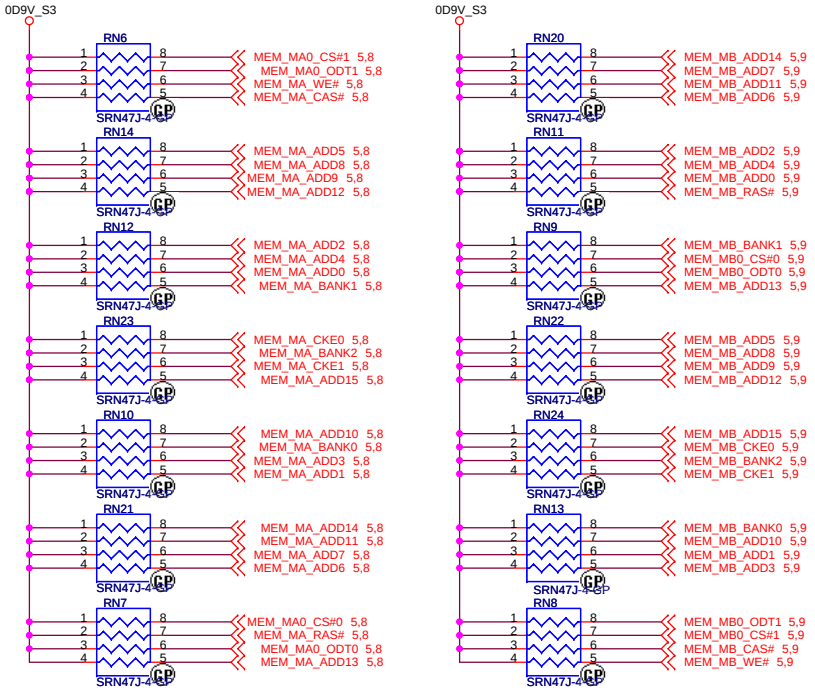
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 9 of 55

PARALLEL TERMINATION

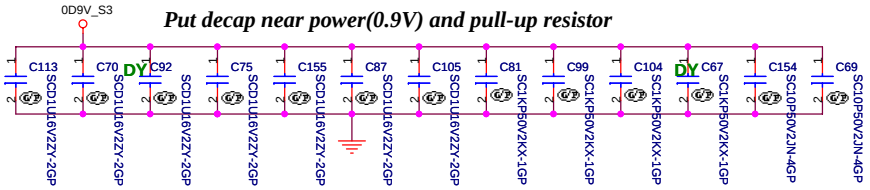
Put decap near power(0.9V) and pull-up resistor



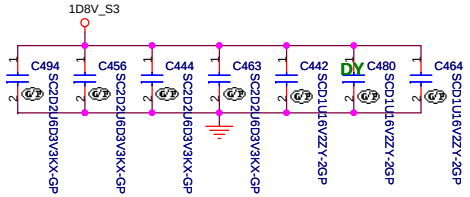
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

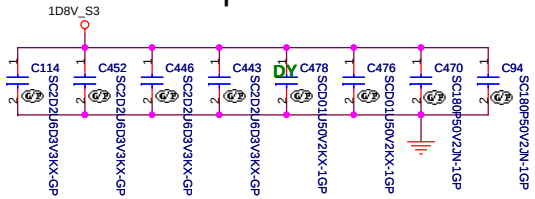


Place these Caps near DM1



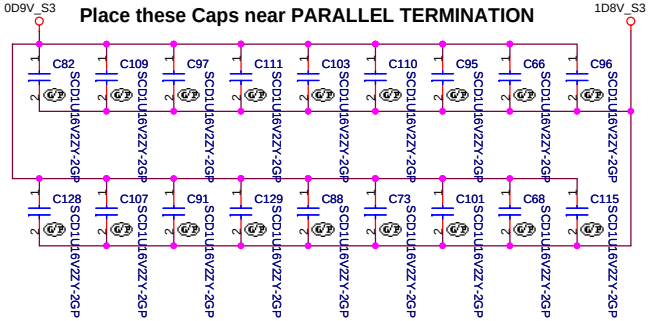
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



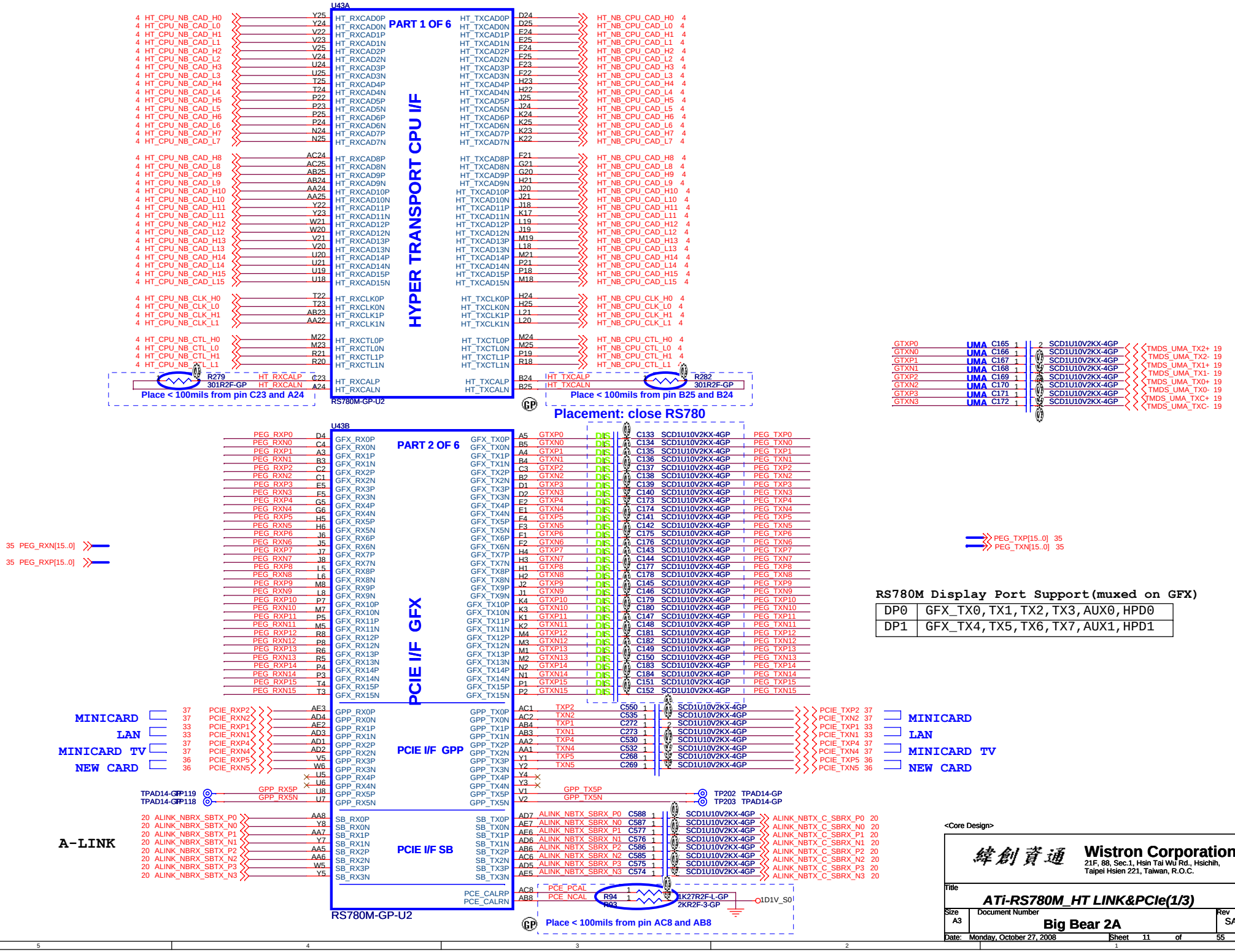
<Core Design>

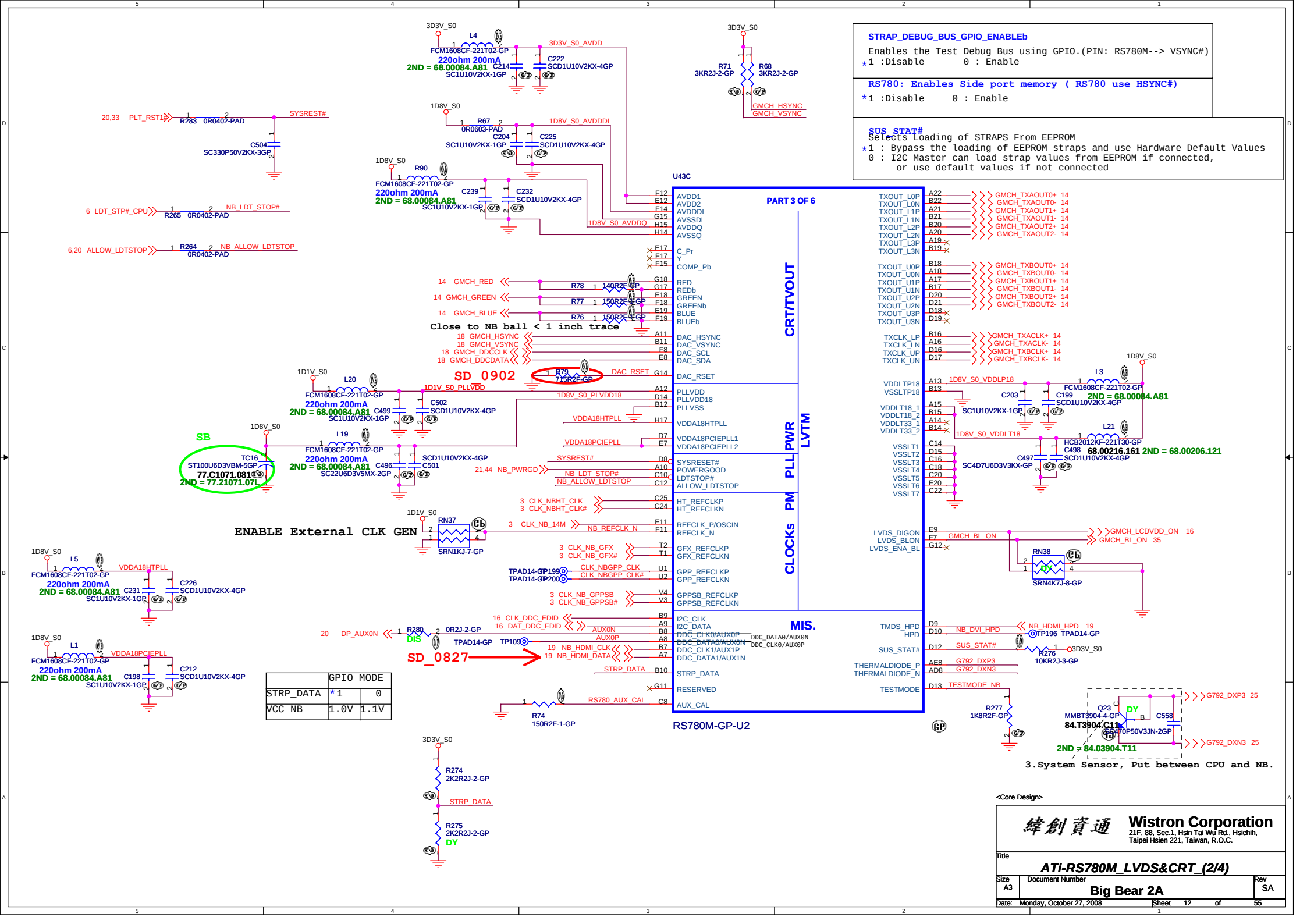
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

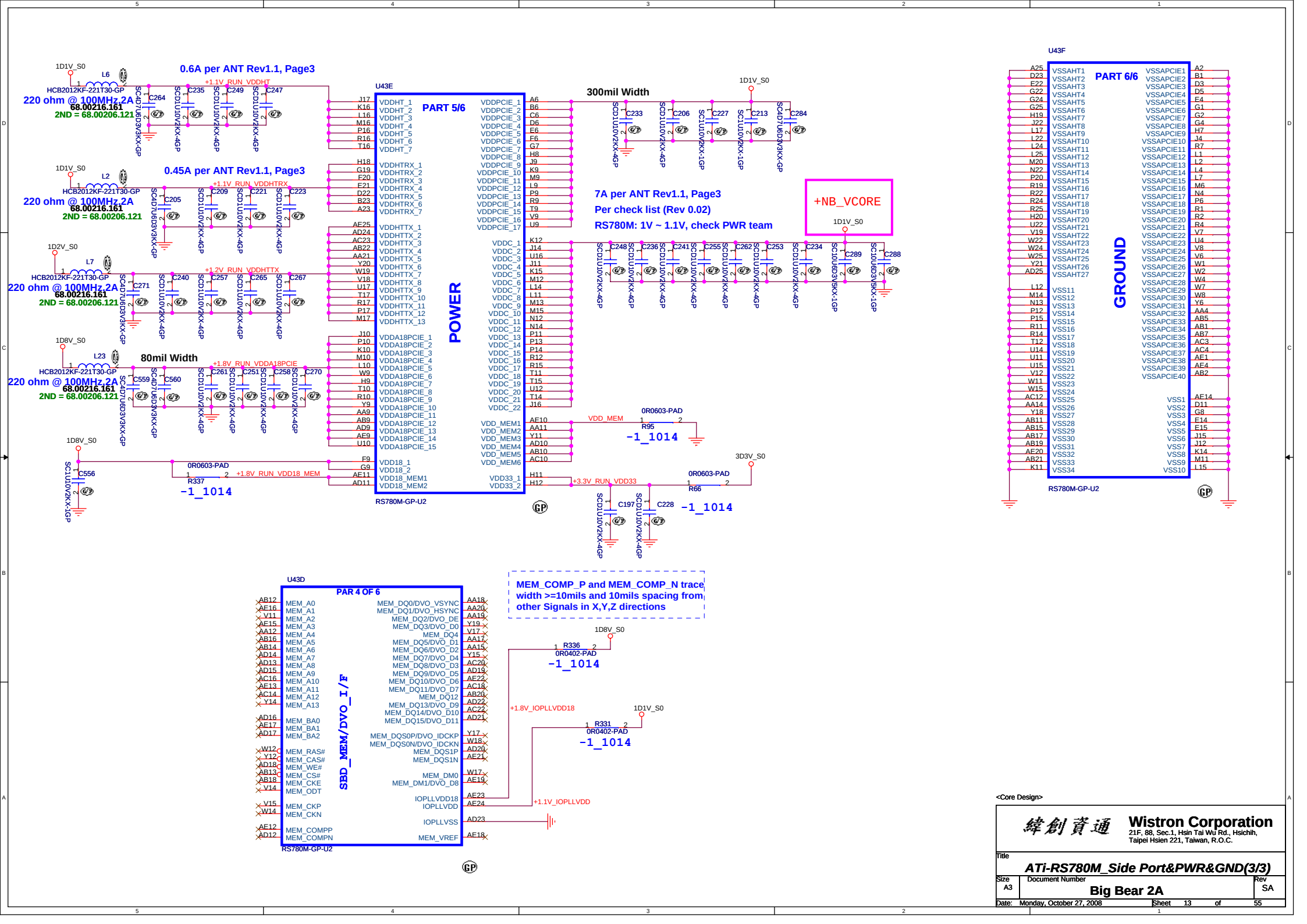
Title: ***DDR_DAMPING & TERMINATION***

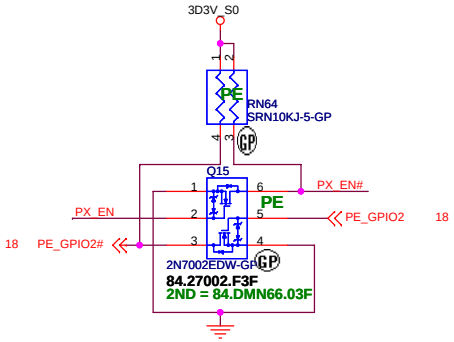
Size	Document Number	Rev
A3	Big Bear 2A	SA

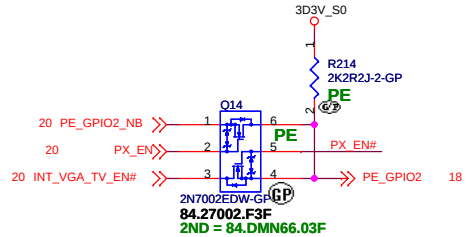
Date: Monday, October 27, 2008 Sheet 10 of 55


U43A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U43B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
A-LINK
MINICARD
LAN
MINICARD TV
NEW CARD
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 11 of 55


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
U43C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
LVTM
PLL/PWR
CLOCKs
PM
MIS.
Close to NB ball < 1 inch trace
SD_0902
SD_0827
ENABLE External CLK GEN
SB
DIS
3.System Sensor, Put between CPU and NB.
GPIO MODE
STRP_DATA *1 0
VCC_NB 1.0V 1.1V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_LVDS&CRT_(2/4)
Big Bear 2A
Monday, October 27, 2008

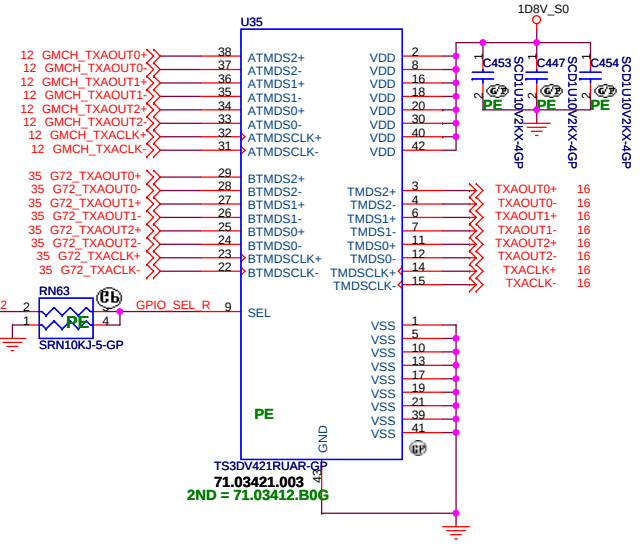

0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
PART 5/6
POWER
PART 6/6
GROUND
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
RS780M-GP-U2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_Side Port&PWR&GND(3/3)
Big Bear 2A
Monday, October 27, 2008

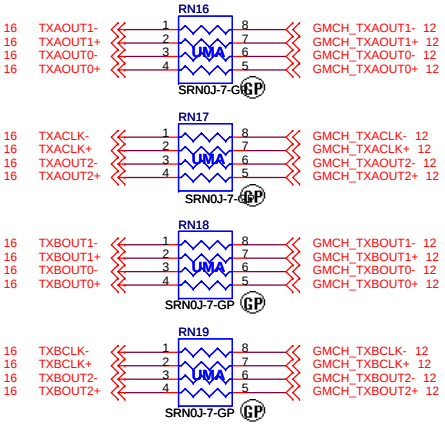


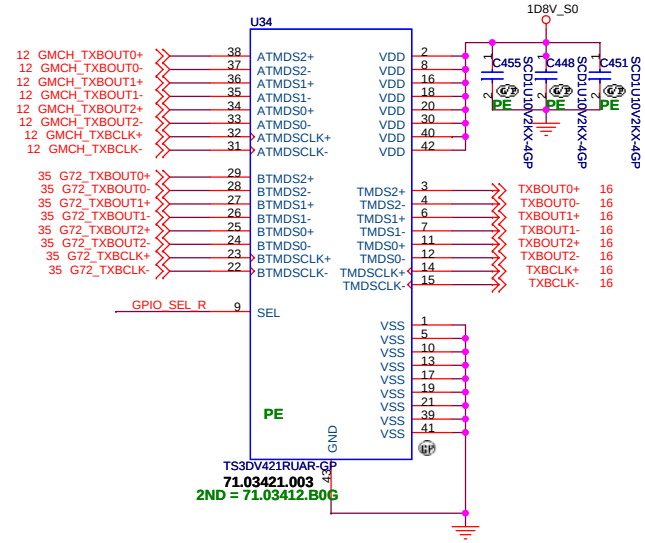


FUNCTION TABLE

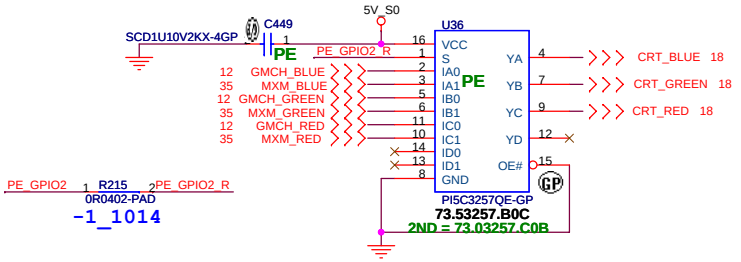
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

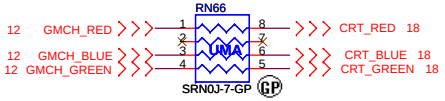






$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1





<Core Design>

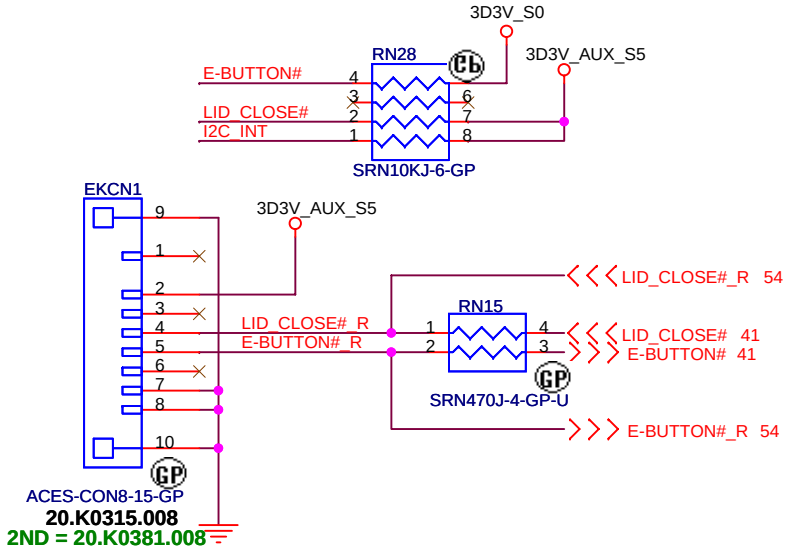
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

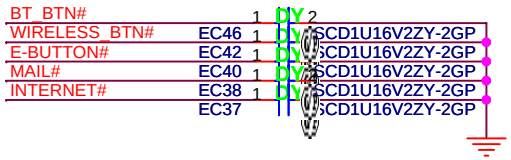
Title: **SWITCH**

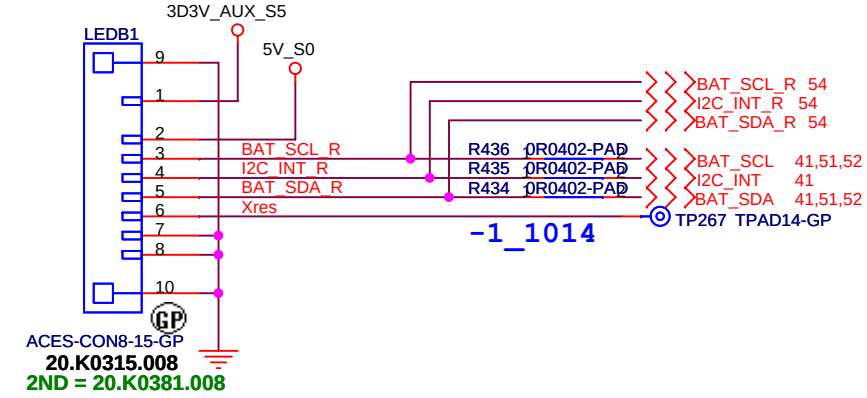
Size	Document Number	Rev
A3	Big Bear 2A	SB

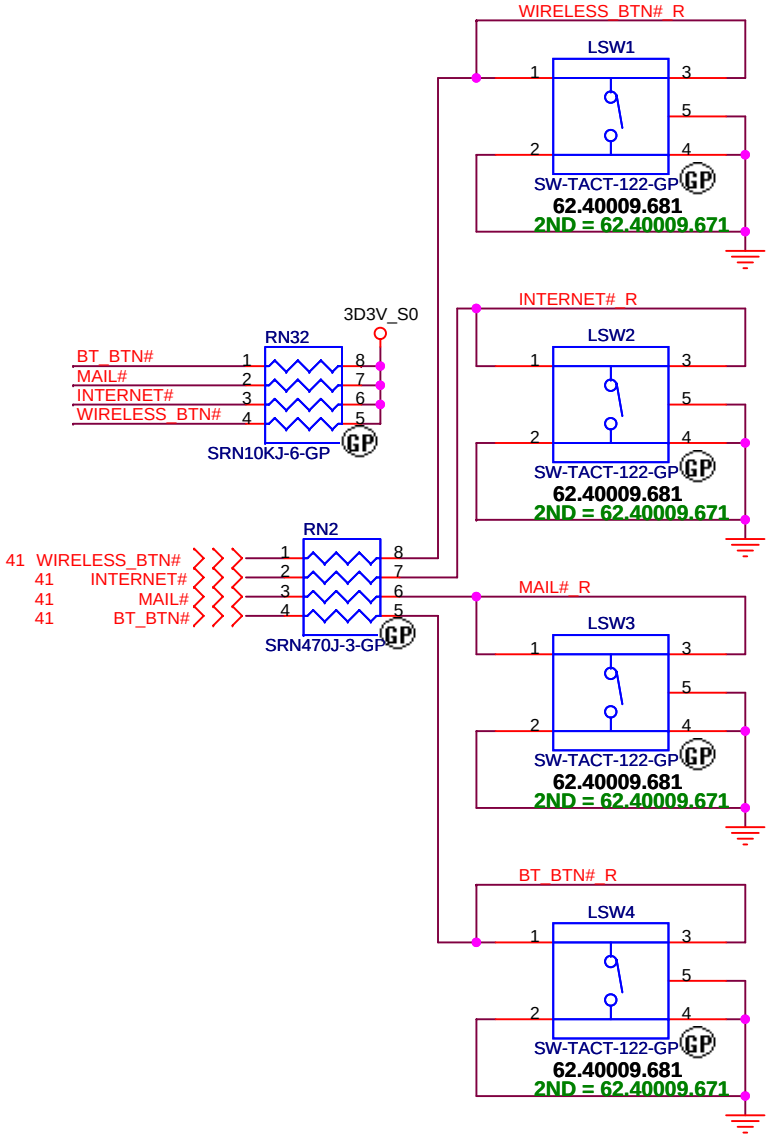
Date: Monday, October 27, 2008 Sheet 14 of 55

LAUNCH









<Core Design>

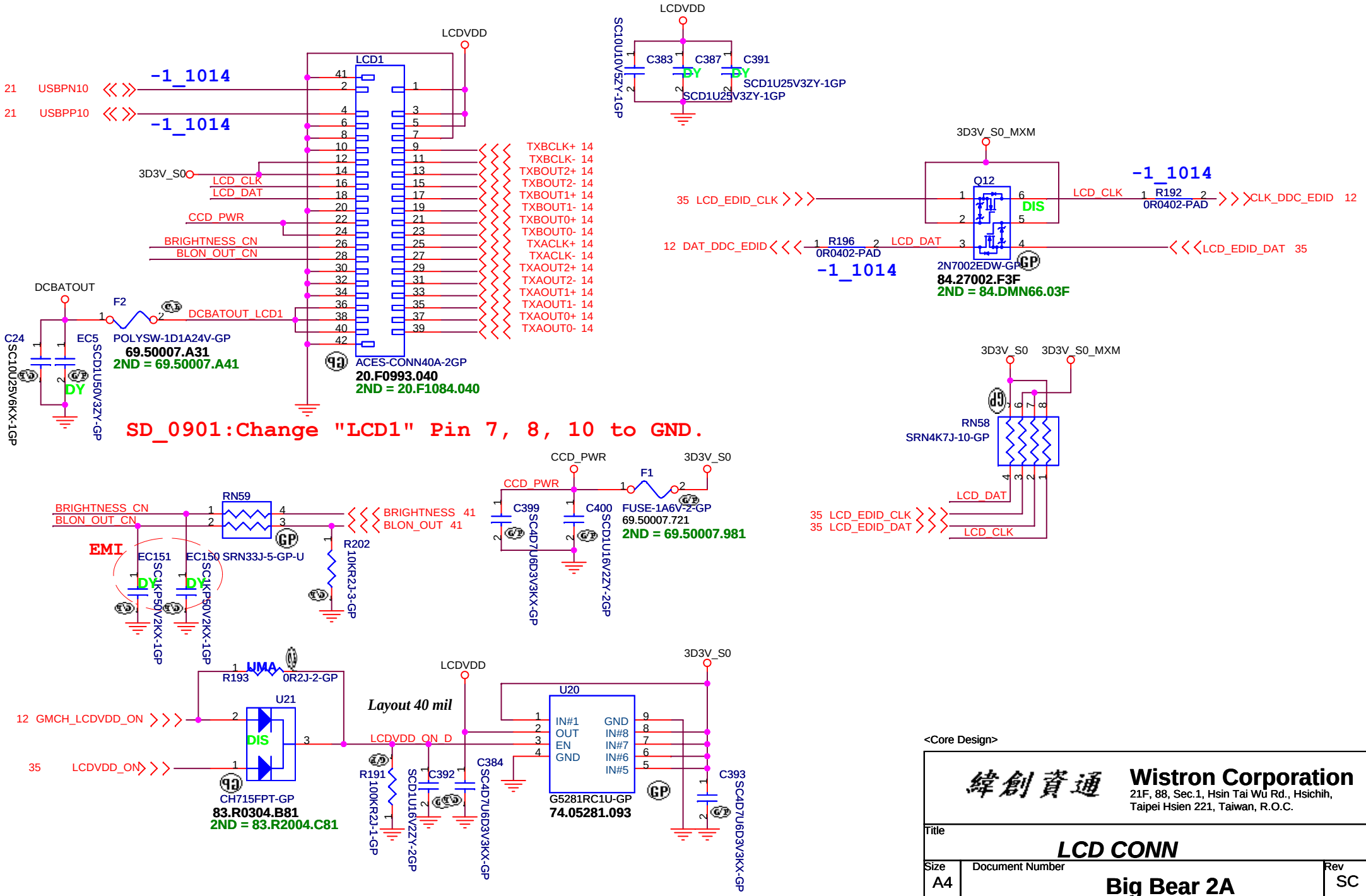
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAUNCH & LID***

Size	Document Number	Rev
A4	**Big Bear 2A**	SC

Date: Monday, October 27, 2008 Sheet 15 of 55

LCD/INVERTER/CCD CONN



<Core Design>

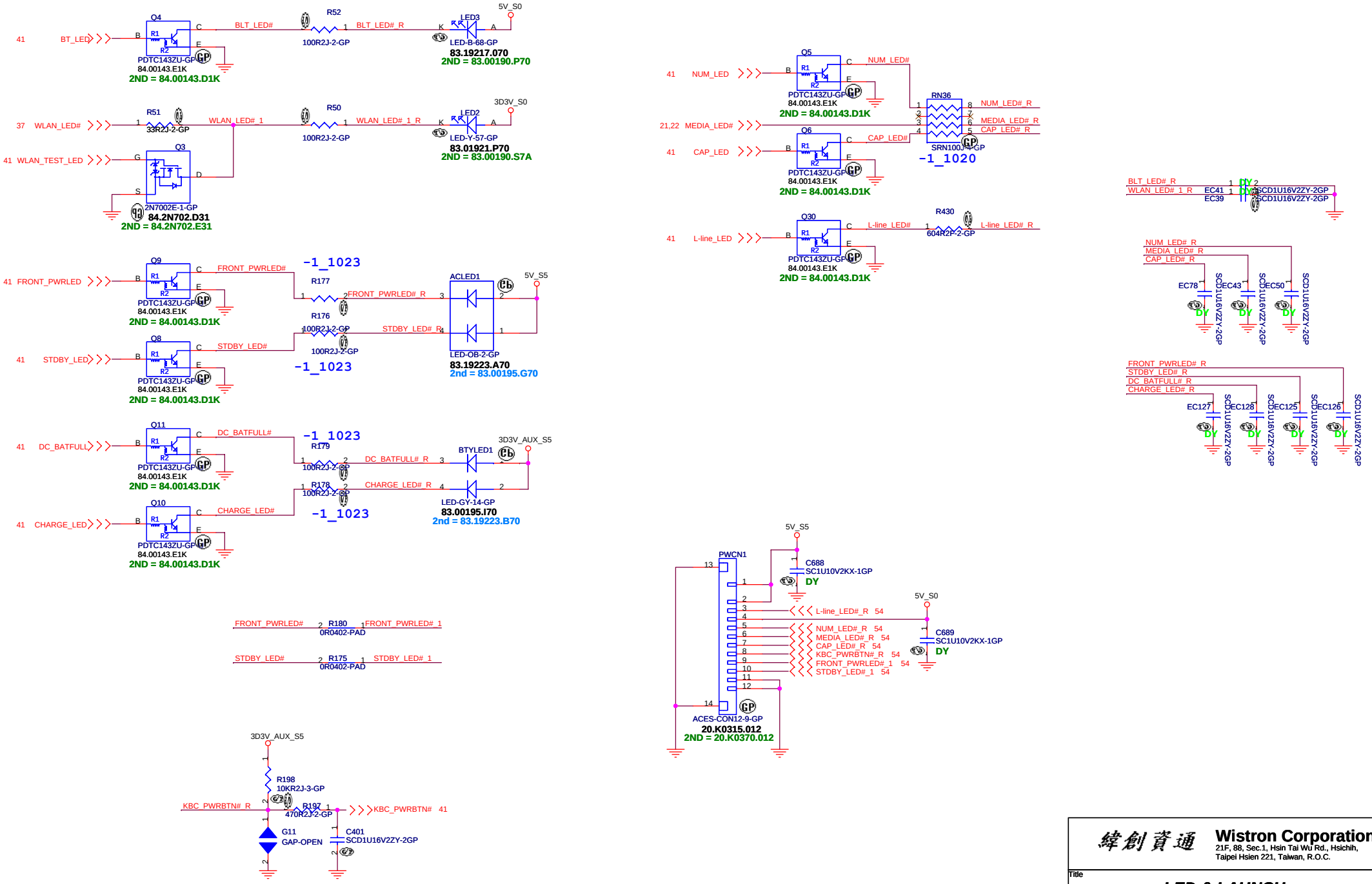
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size	Document Number	Rev
A4	Big Bear 2A	SC

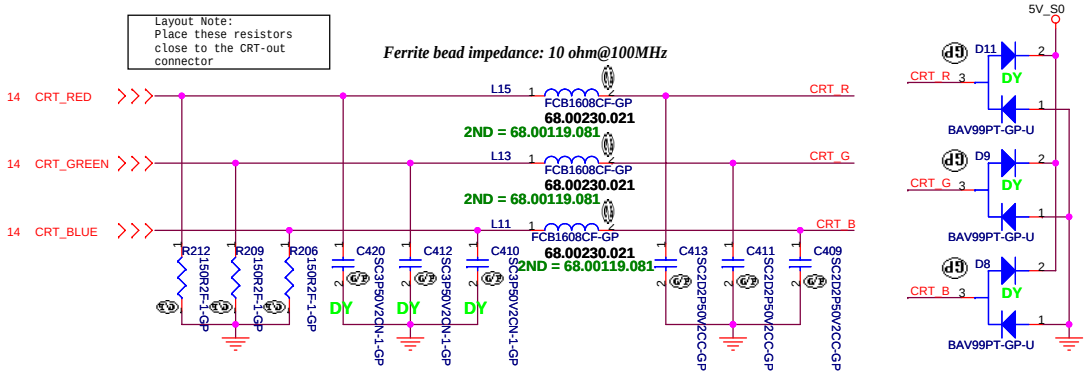
Date: Monday, October 27, 2008 Sheet 16 of 55

LED



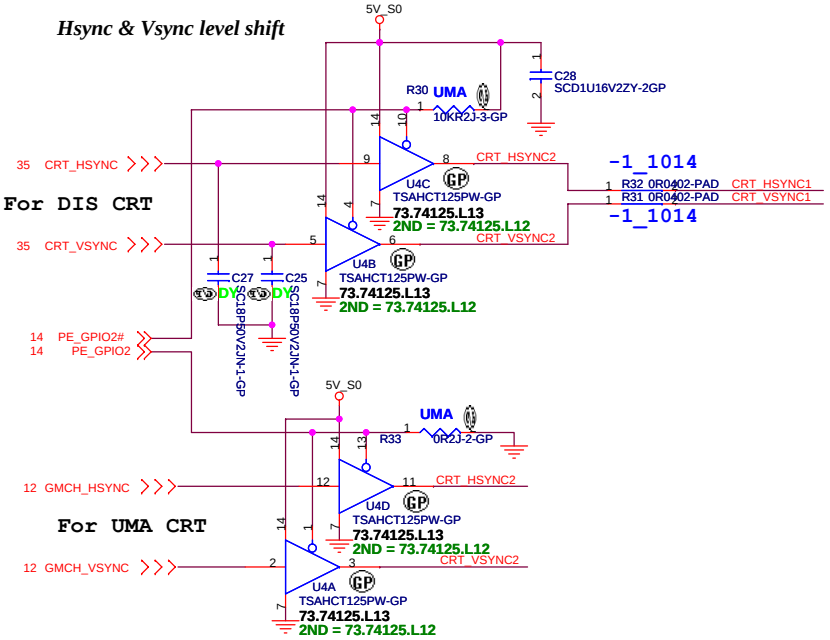
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**LED & LAUNCH**	
Size: A3	Document Number: **Big Bear 2A**	Rev: SC
Date: Monday, October 27, 2008	Sheet 17 of 55	

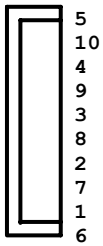


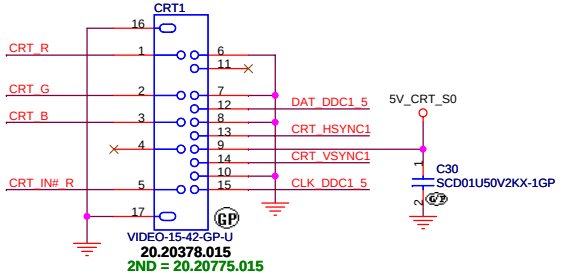
Change C409; C411, C413 to 1.5pF (78.1R574.1FL) in UMA

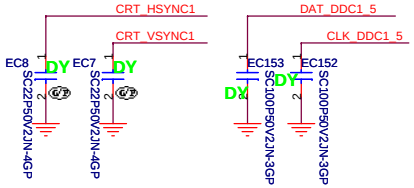
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

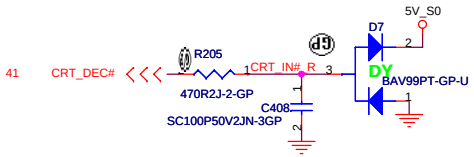


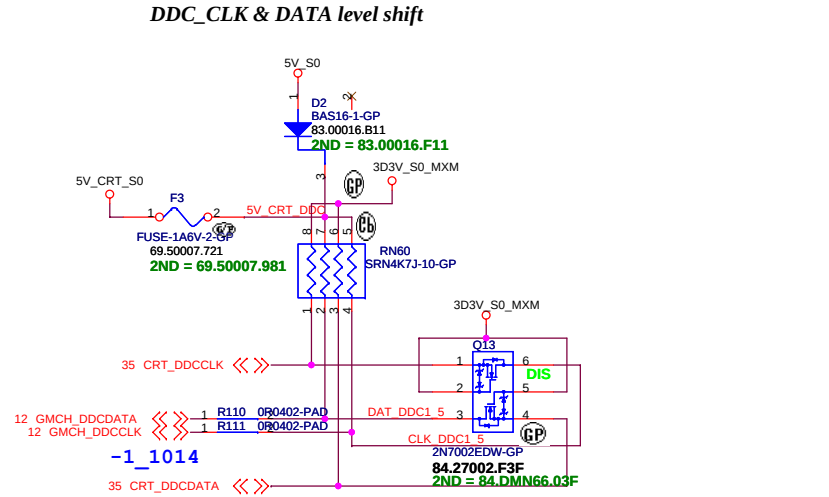
CRT I/F & CONNECTOR









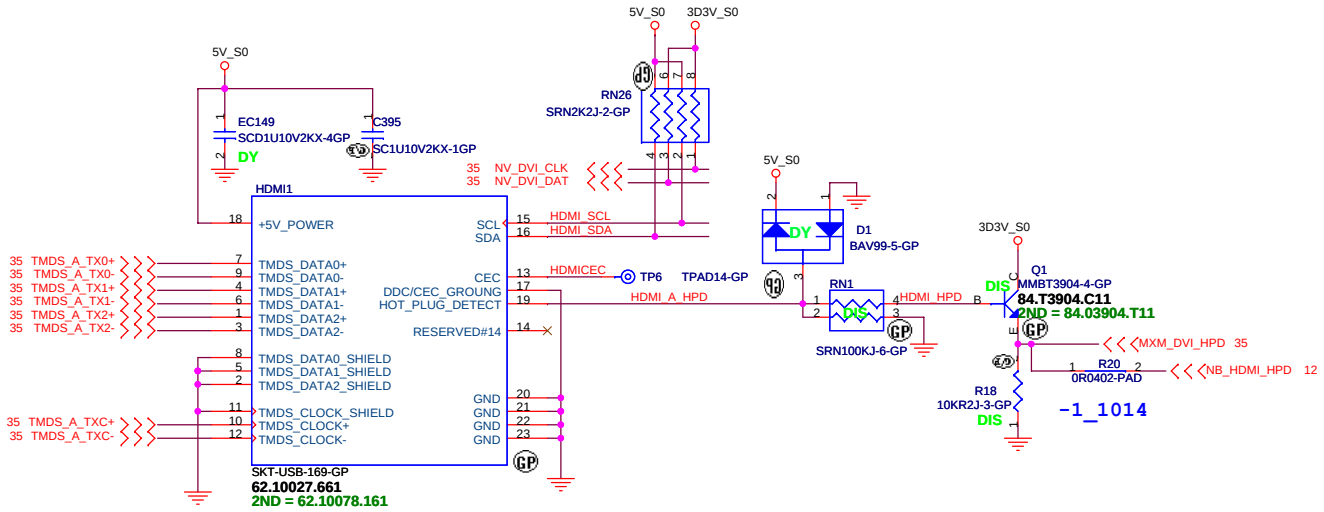


<Core Design>

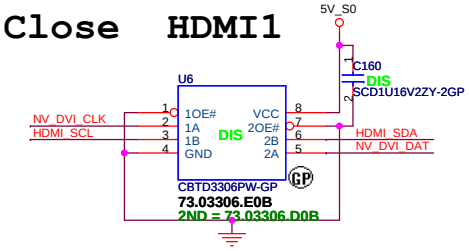
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

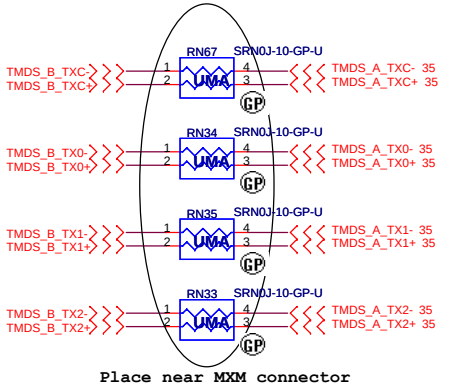
Title	***CRT Connector***	
Size	Document Number **Big Bear 2A**	Rev SA
Date: Monday, October 27, 2008	Sheet 18 of 55	

HDMI SM BUS LEVEL shifter

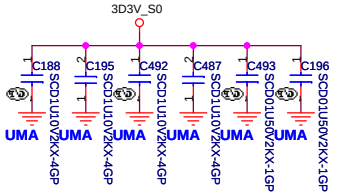


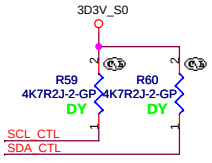
Close HDMI1

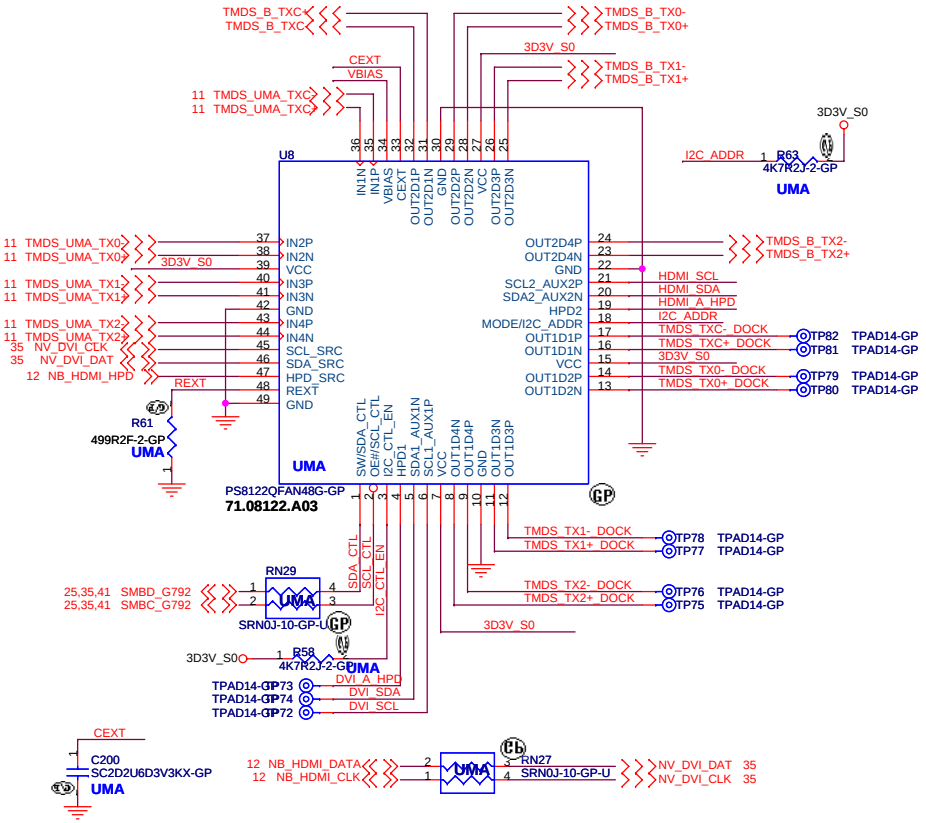




Place near MXM connector







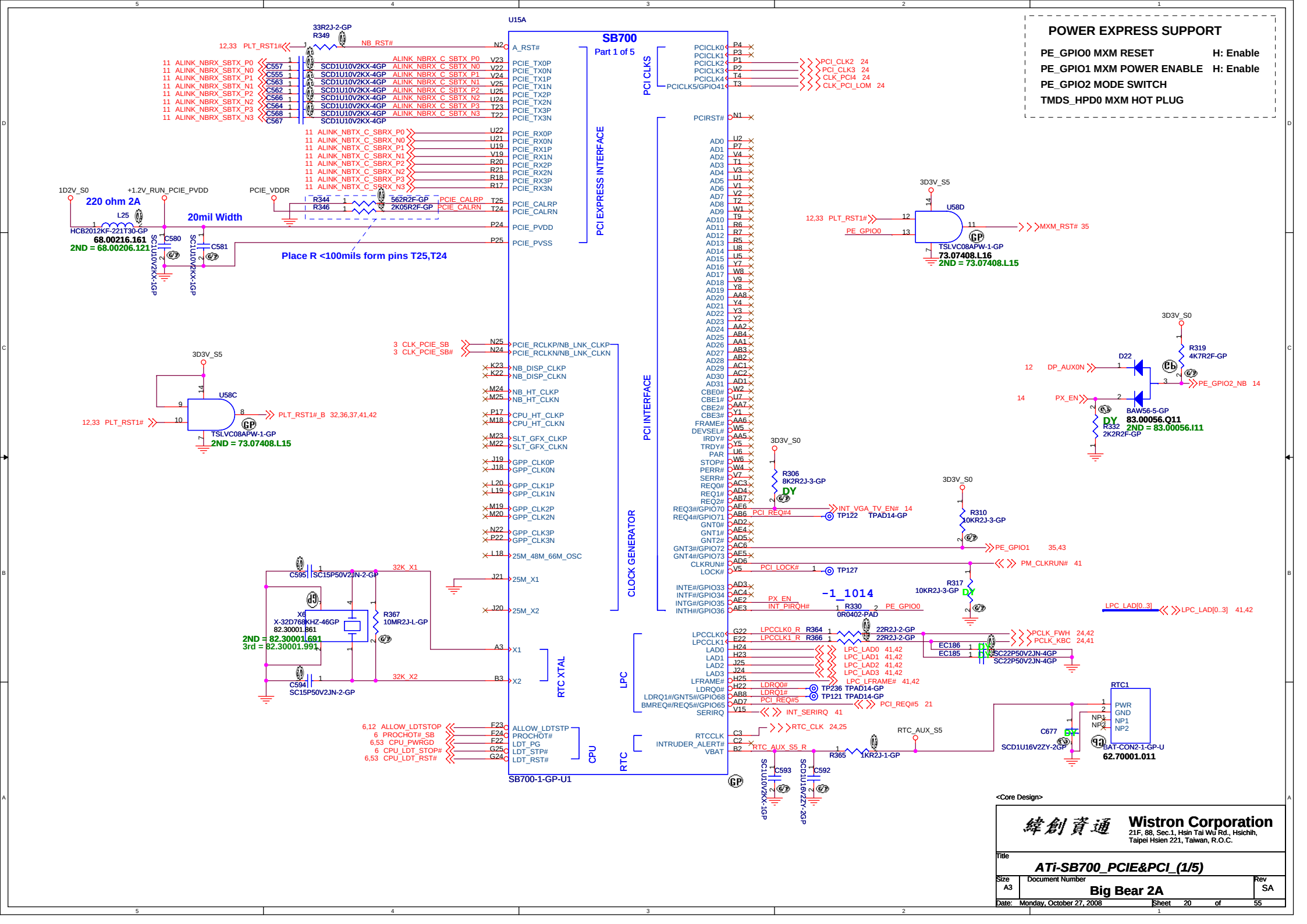
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI CONNECTOR**

Size	Document Number	Rev
A3	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 19 of 55



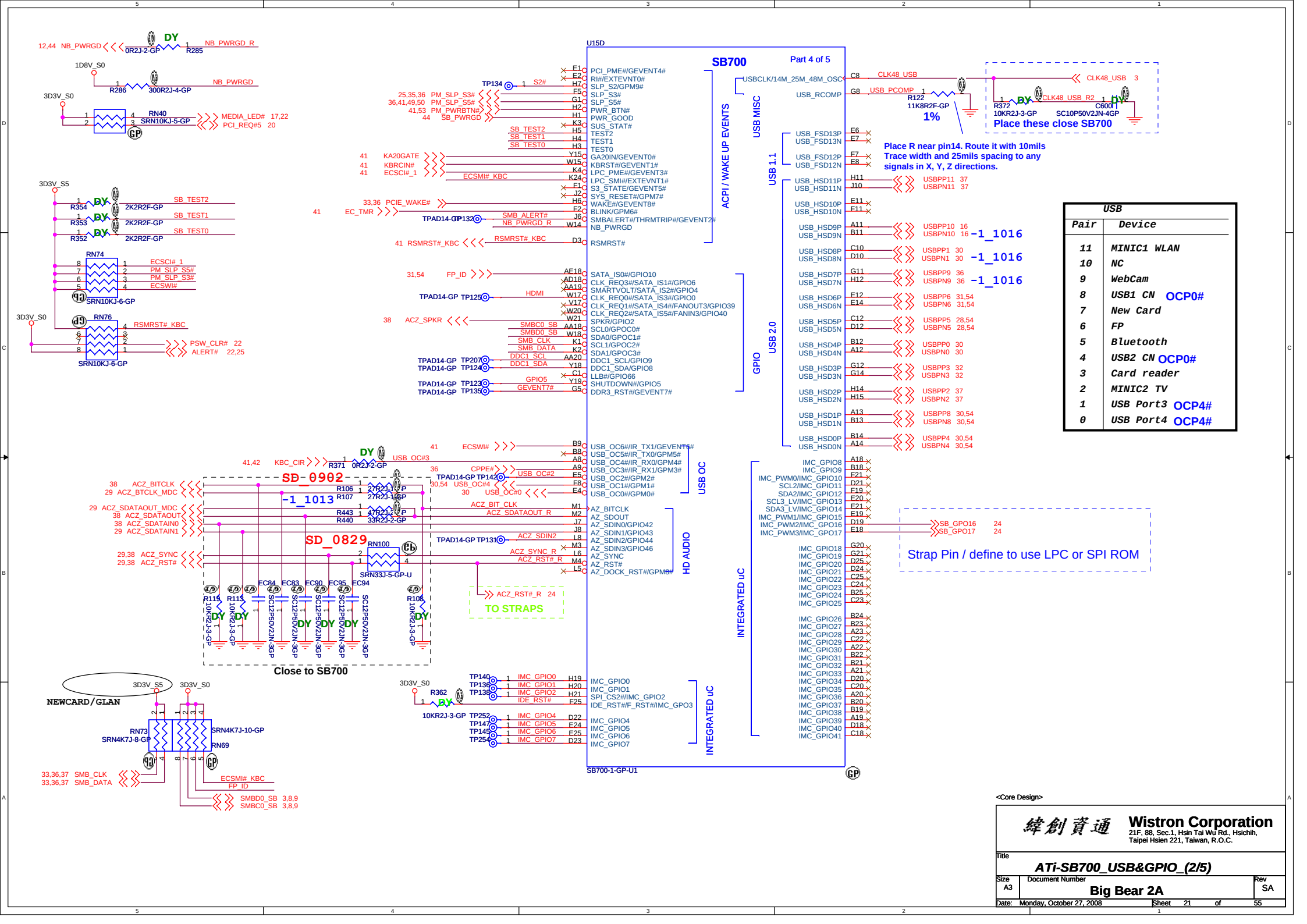
<Core Design>

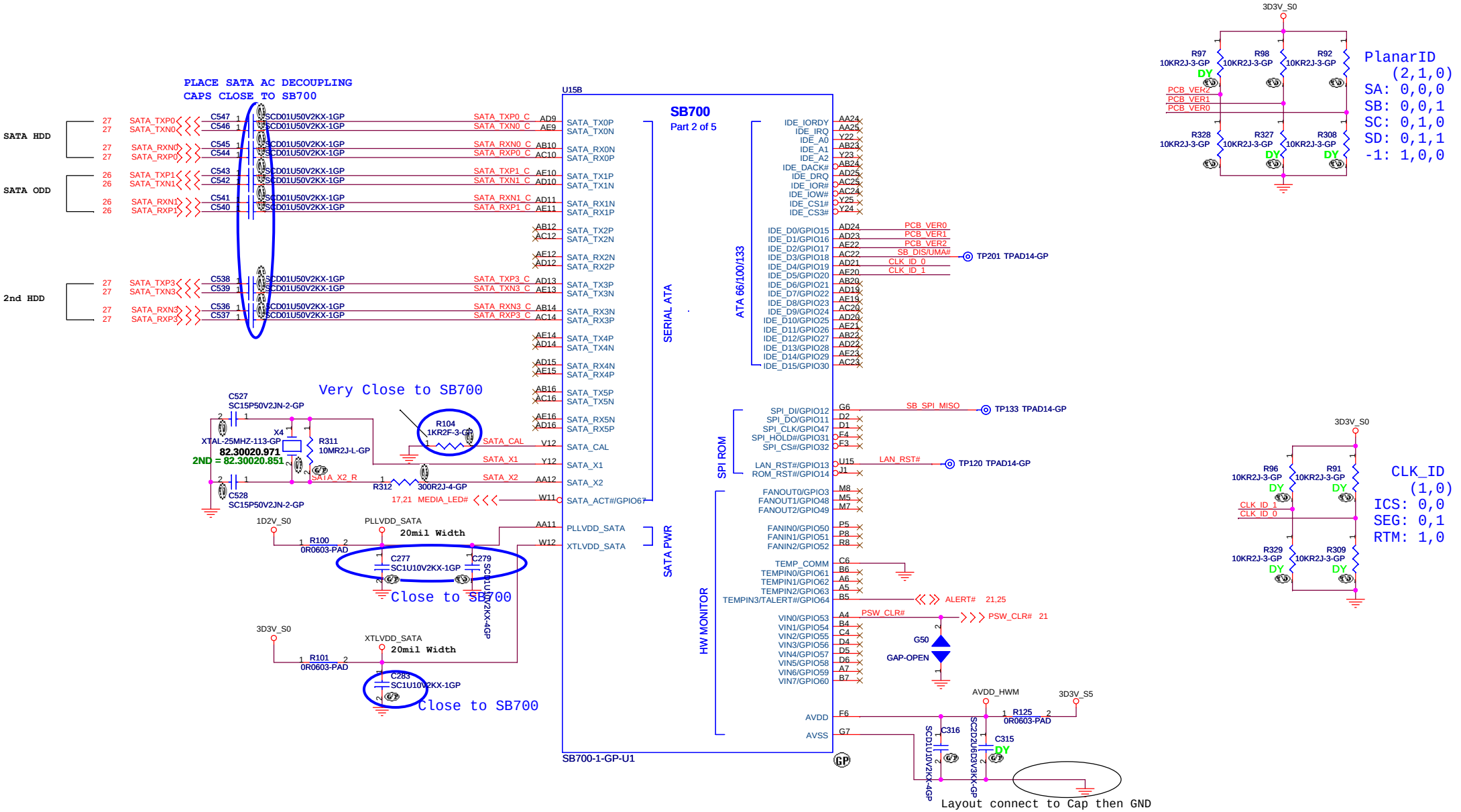
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_PCIE&PCI_(1/5)

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 20 of 55


SB700
Part 4 of 5
U15D
SB700-1-GP-U1
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
Place these close SB700
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
Close to SB700
SD_0902
-1_1013
SD_0829
NEWCARD/GLAN
USB
Pair | Device
11 | MINIC1 WLAN
10 | NC
9 | WebCam
8 | USB1 CN OCP0#
7 | New Card
6 | FP
5 | Bluetooth
4 | USB2 CN OCP0#
3 | Card reader
2 | MINIC2 TV
1 | USB Port3 OCP4#
0 | USB Port4 OCP4#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 21 of 55



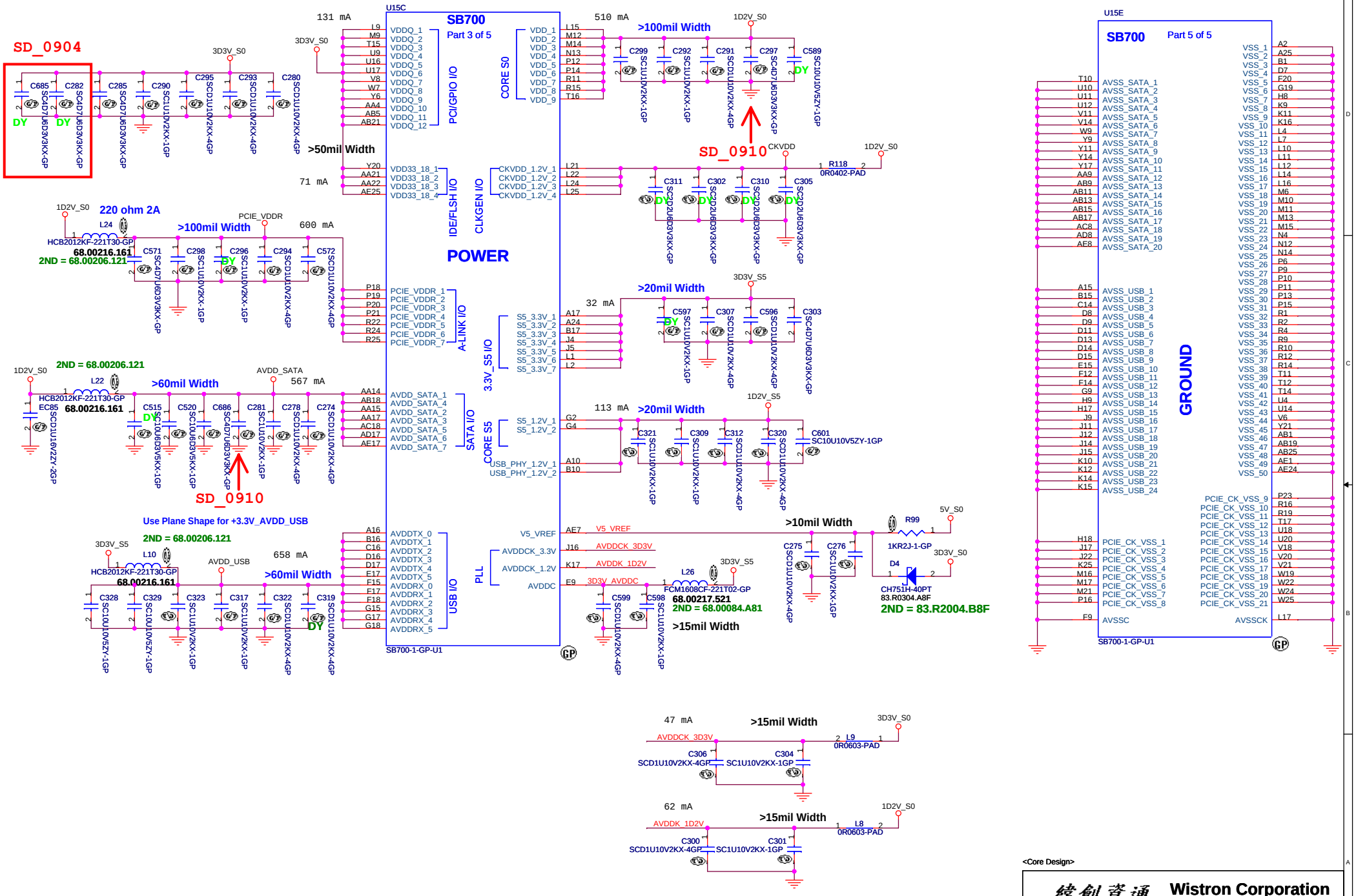
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)

Size: A3 | Document Number: Big Bear 2A | Rev: SB

Date: Monday, October 27, 2008 | Sheet 22 of 55



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

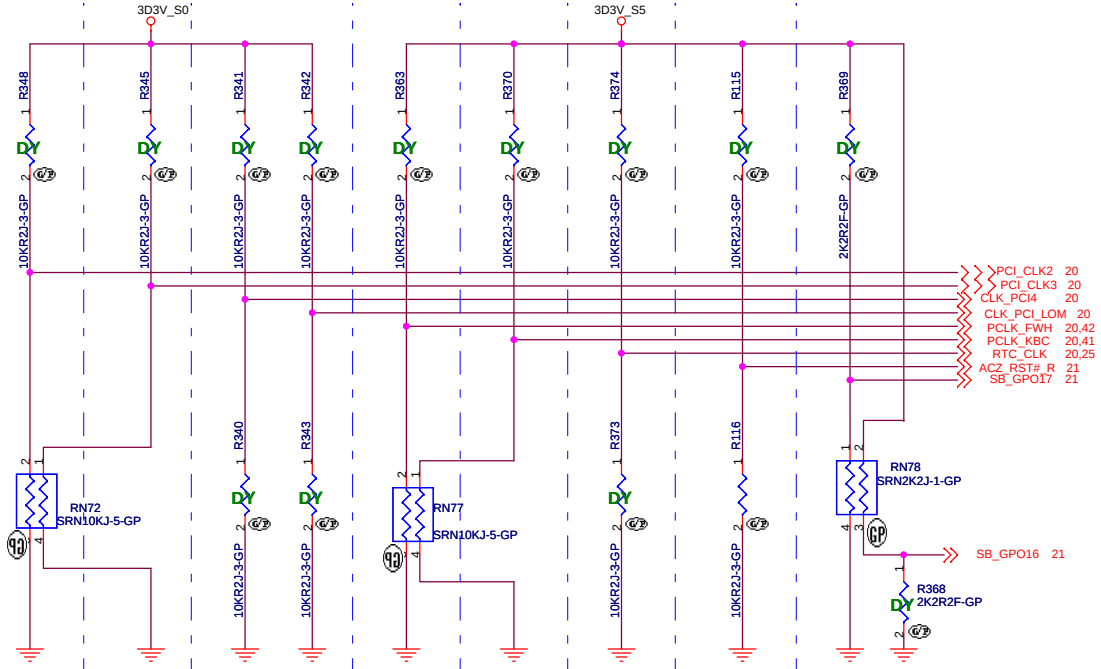
Title: ATi-SB700_POWER&GND_(4/5)

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 23 of 55

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

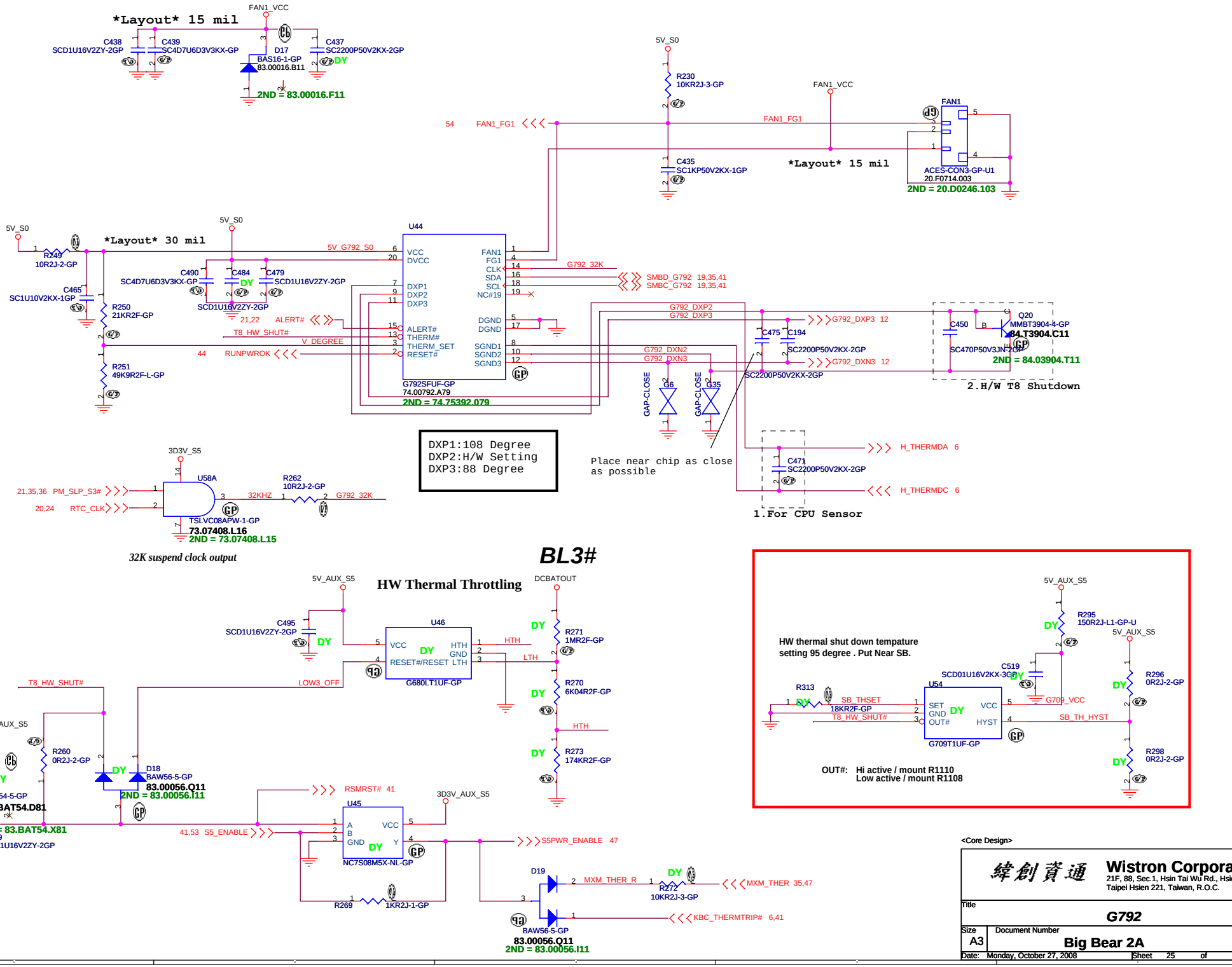
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

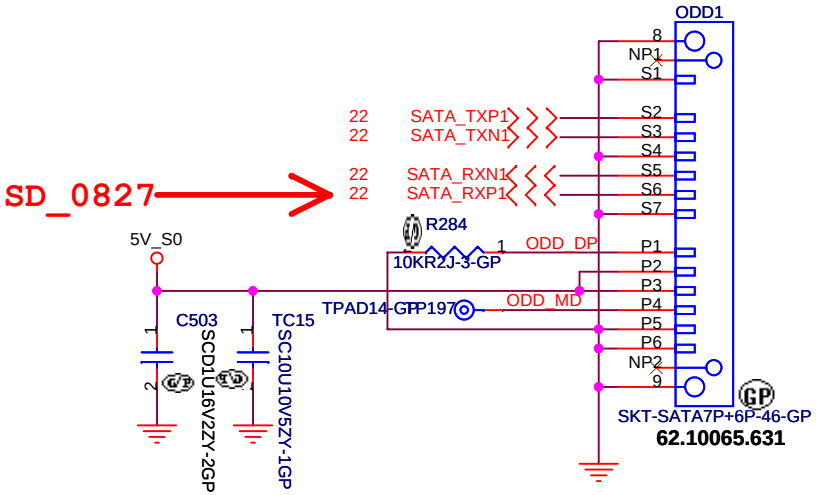
Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

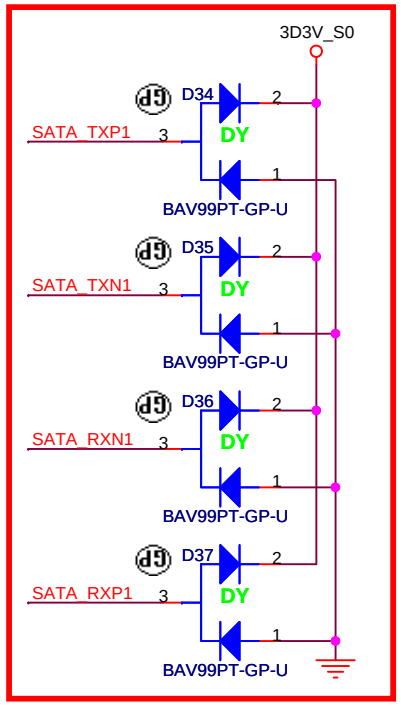
Date: Monday, October 27, 2008 | Sheet 24 of 55


Layout 15 mil
FAN1_VCC
C438 SCD1U16V2ZY-2GP
C439 SC4D7U6D3V3KX-GP
D17 BAS16-1-GP 83.00016.B11
C437 SC2200P50V2KX-2GP
DY
2ND = 83.00016.F11
5V_S0
R230 10KR2J-3-GP
FAN1_VCC
54 FAN1_FG1
FAN1_FG1
FAN1
C435 SC1KP50V2KX-1GP
Layout 15 mil
ACES-CON3-GP-U1 20.F0714.003
2ND = 20.D0246.103
5V_S0
Layout 30 mil
R249 10R2J-2-GP
C465 SC1U10V2KX-1GP
R250 21KR2F-GP
R251 49K9R2F-L-GP
5V_S0
C490 SC4D7U6D3V3KX-GP
C484 DY
C479 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
U44
5V_G792_S0
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
DGND
DGND
SGND1
SGND2
SGND3
FAN1
FG1
CLK
SDA
SCL
NC#19
G792_32K
SMBD_G792 19,35,41
SMBC_G792 19,35,41
21,22 ALERT#
T8_HW_SHUT#
V_DEGREE
44 RUNPWROK
G792SFUF-GP
74.00792.A79
2ND = 74.75392.079
G792_DXP2
G792_DXP3
G792_DXP3 12
C475 C194
SC2200P50V2KX-2GP
G792_DXN2
G792_DXN3
G792_DXN3 12
SC2200P50V2KX-2GP
GAP-CLOSE
G6
GAP-CLOSE
G35
C450
Q20 MMBT3904-4-GP 84.T3904.C11
SC470P50V3JN-2GP
2ND = 84.03904.T11
2.H/W T8 Shutdown
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C471 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
U58A
21,35,36 PM_SLP_S3#
20,24 RTC_CLK
32KHZ
R262 10R2J-2-GP
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
32K suspend clock output
BL3#
HW Thermal Throttling
5V_AUX_S5
C495 SCD1U16V2ZY-2GP
DY
U46
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1UF-GP
DCBATOUT
R271 1MR2F-GP
R270 6K04R2F-GP
R273 174KR2F-GP
HTH
LTH
T8_HW_SHUT#
LOW3_OFF
3D3V_AUX_S5
R260 0R2J-2-GP
R266 10KR2J-3-GP
D20 BAT54-5-GP 83.BAT54.D81
2ND = 83.BAT54.X81
C489 SCD1U16V2ZY-2GP
D18 BAW56-5-GP 83.00056.Q11
2ND = 83.00056.I11
RSMRST# 41
41,53 S5_ENABLE
U45
A
B
GND
VCC
Y
NC7S08M5X-NL-GP
3D3V_AUX_S5
S5PWR_ENABLE 47
R269 1KR2J-1-GP
D19
MXM_THER_R
R272 10KR2J-3-GP
MXM_THER 35,47
KBC_THERMTRIP# 6,41
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.I11
HW thermal shut down tempature setting 95 degree . Put Near SB.
5V_AUX_S5
R295 150R2J-L1-GP-U
C519 SCD01U16V2KX-3GP
R313 18KR2F-GP
SB_THSET
T8_HW_SHUT#
U54
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
G709_VCC
SB_TH_HYST
R296 0R2J-2-GP
R298 0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 25 of 55

ODD Connector



SD_0828



<Core Design>

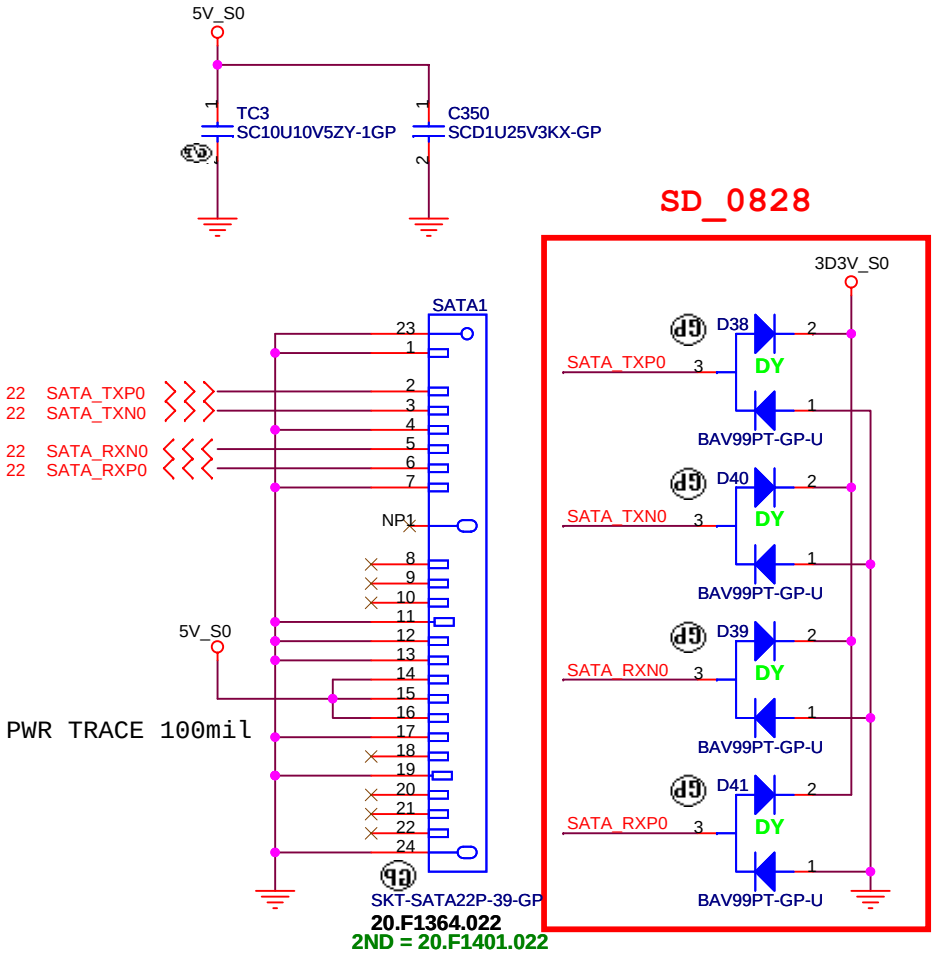
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM

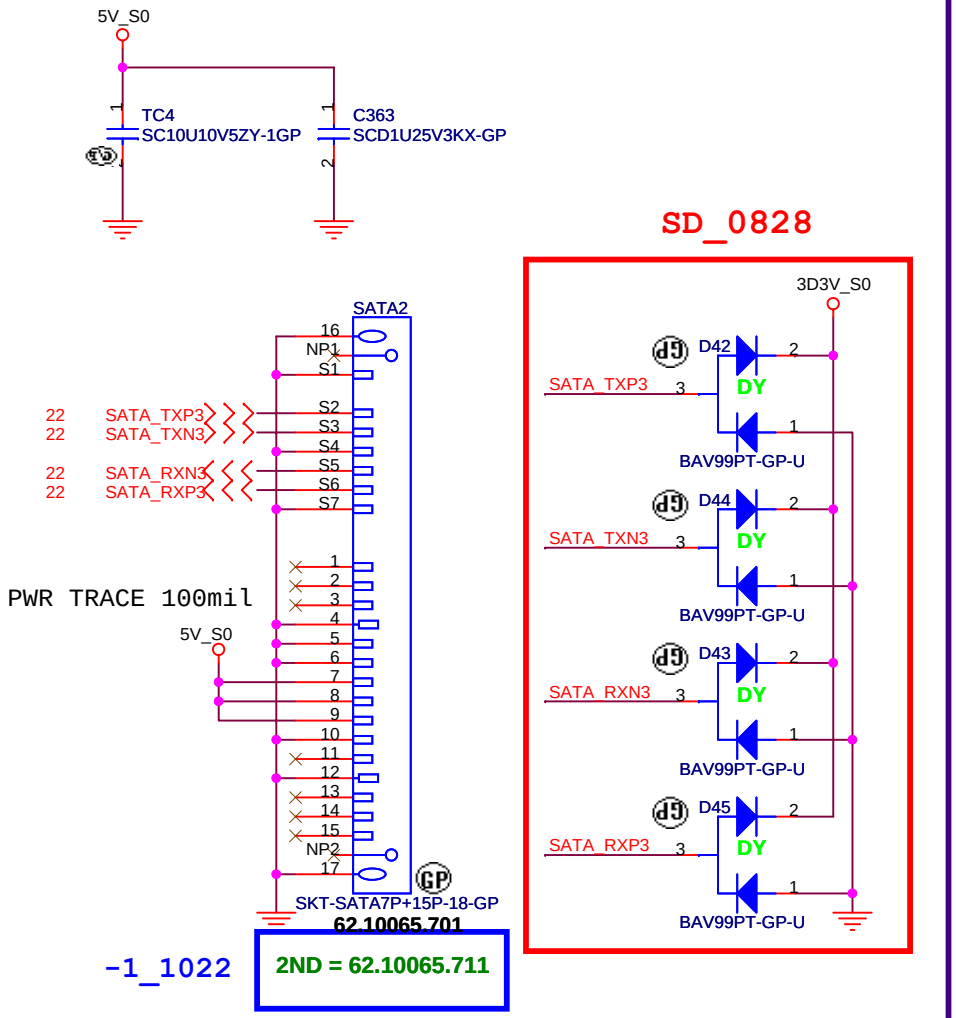
Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 26 of 55

SATA HDD Connector



2ND SATA HDD Connector

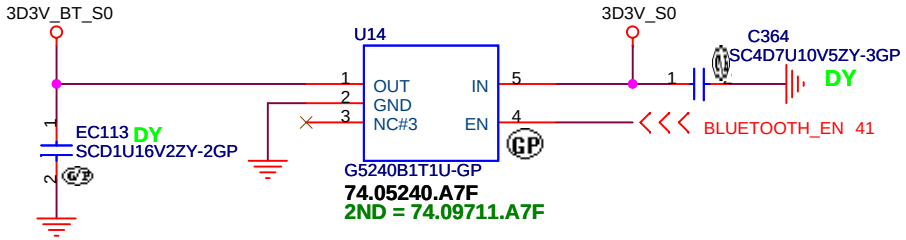


<Core Design>

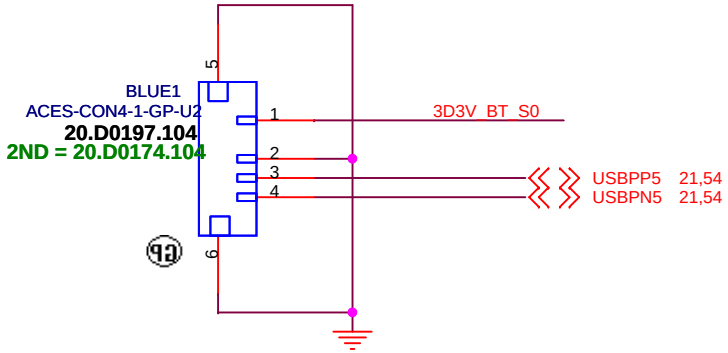
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD***		
Size: A4	Document Number: **Big Bear 2A**	Rev: SD
Date: Monday, October 27, 2008	Sheet 27 of 55	

BLUETOOTH MODULE



EC40 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



<Core Design>

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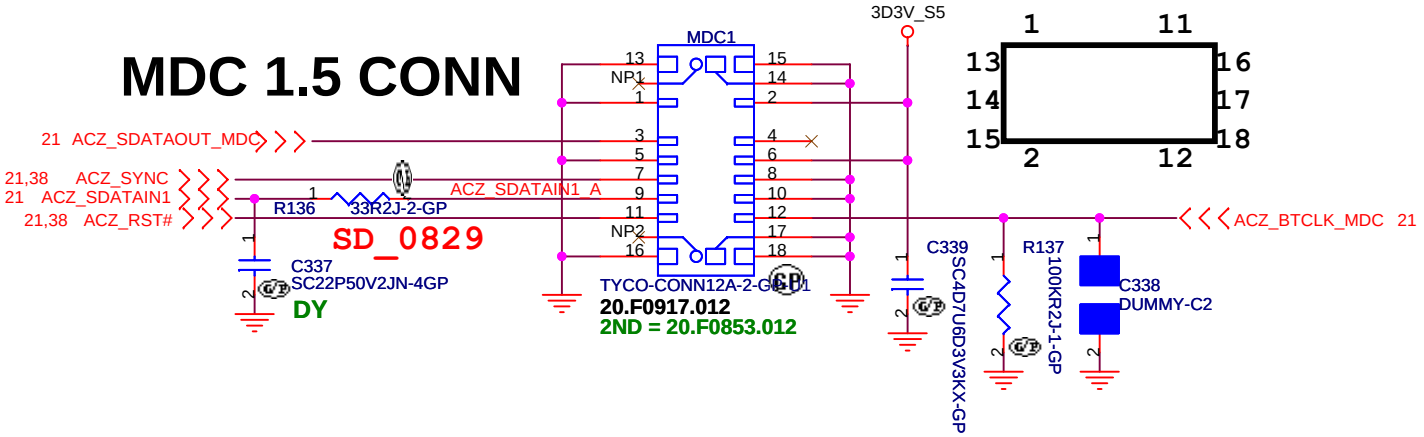
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***

Size	Document Number	Rev
A4	Big Bear 2A	SA

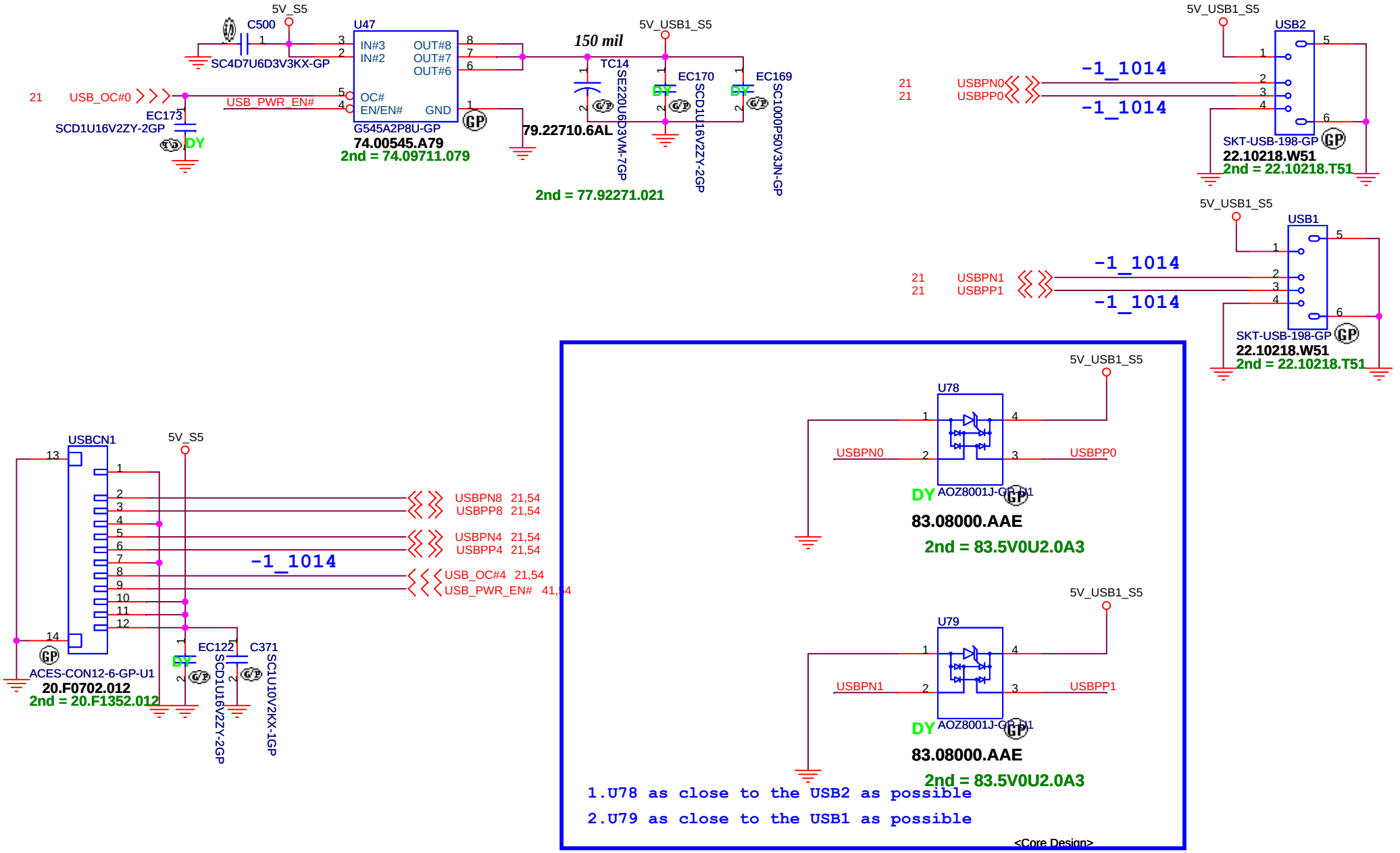
Date: Monday, October 27, 2008 Sheet 28 of 55

MDC 1.5 CONN



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MDC***
Size: A4	Document Number: **Big Bear 2A** — Rev: SA
Date: Monday, October 27, 2008	Sheet 29 of 55



ESD Protection

緯創資通 Wistron Corporation
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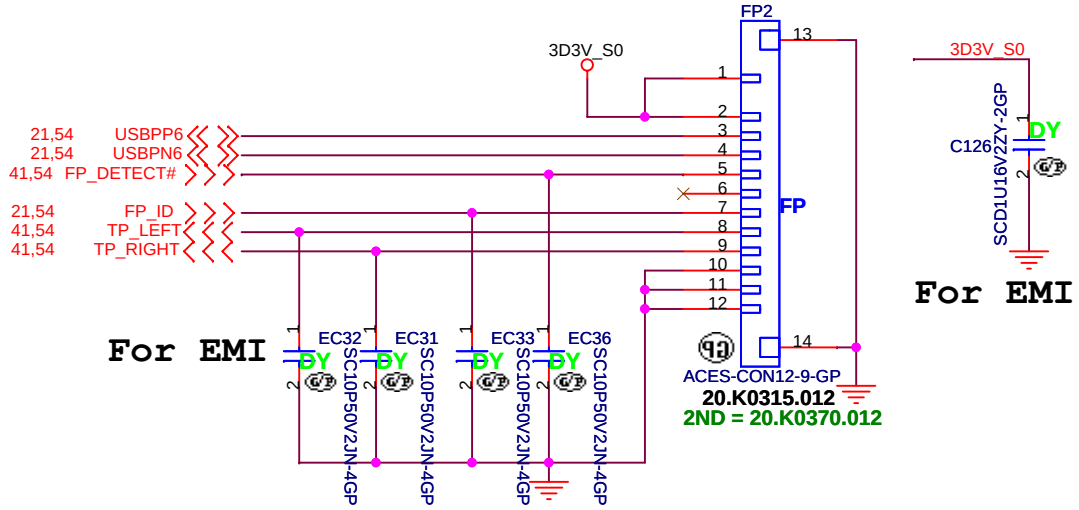
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB**

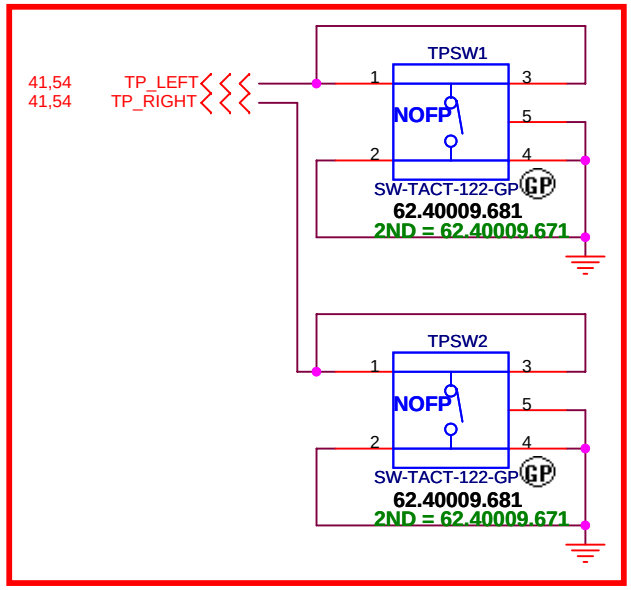
Size	Document Number	Rev
A4	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 30 of 55

Finger printer



SD_0903



<Core Design>

緯創資通 **Wistron Corporation**
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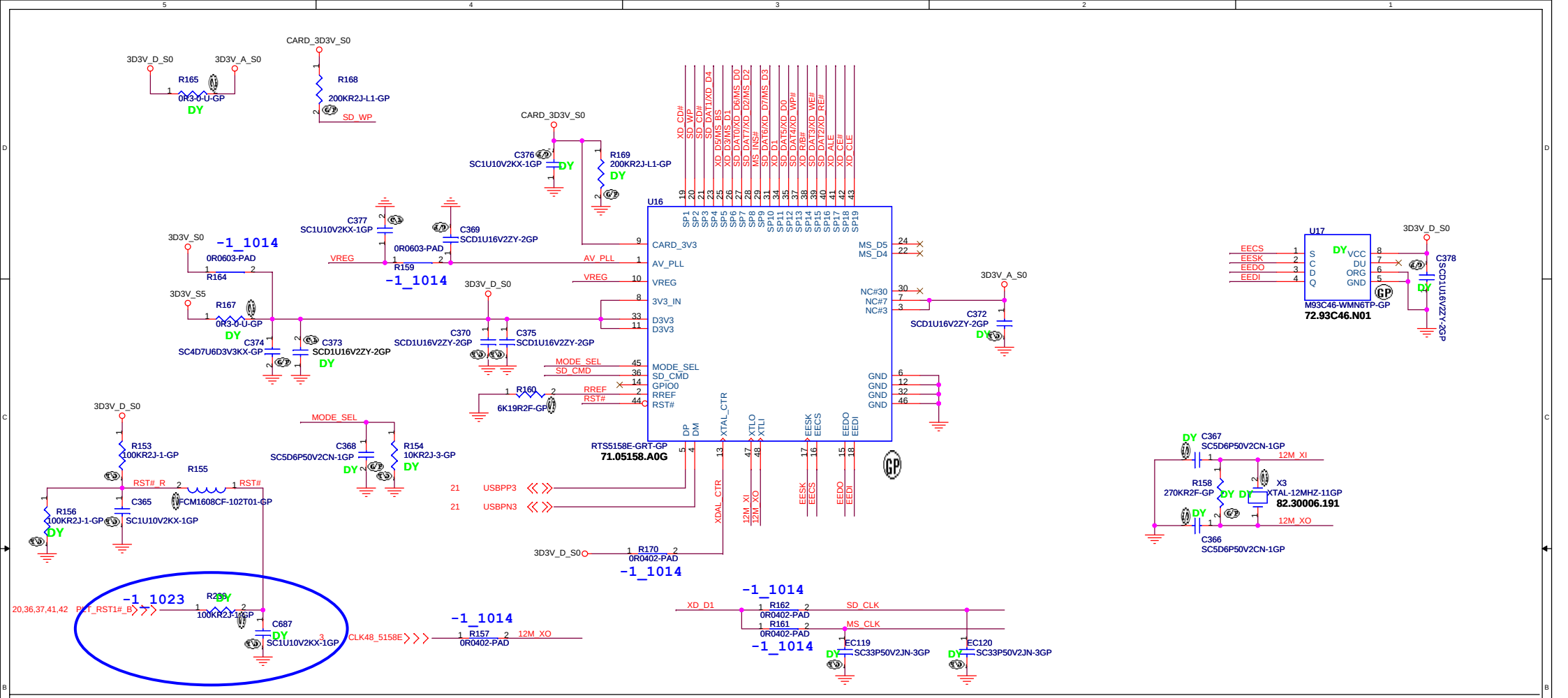
Taipei Hsien 221, Taiwan, R.O.C.

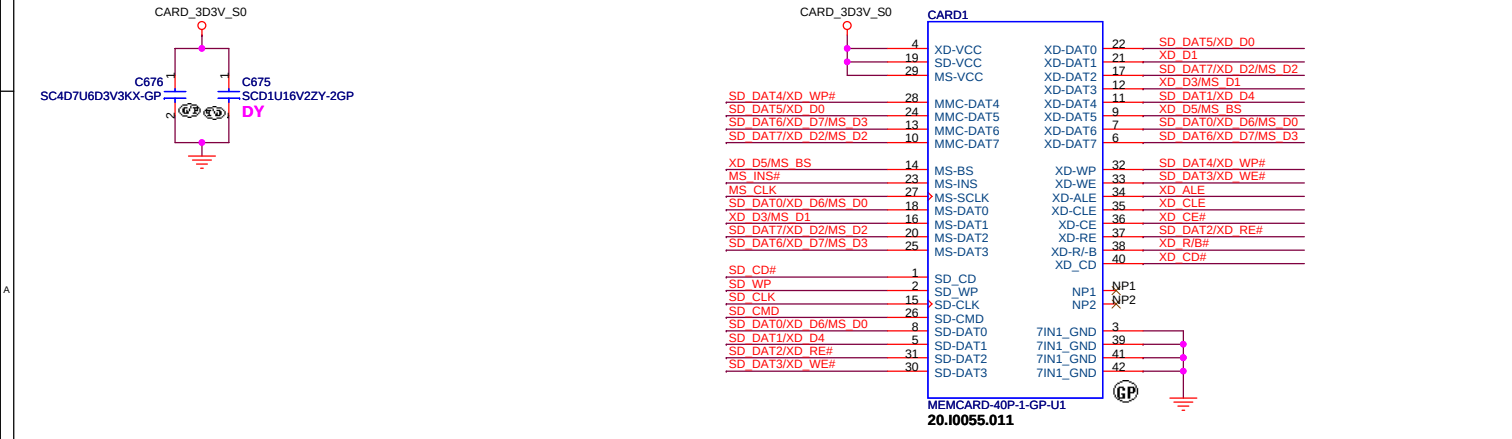
Title: ***Finger Printer***

Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 31 of 55



7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



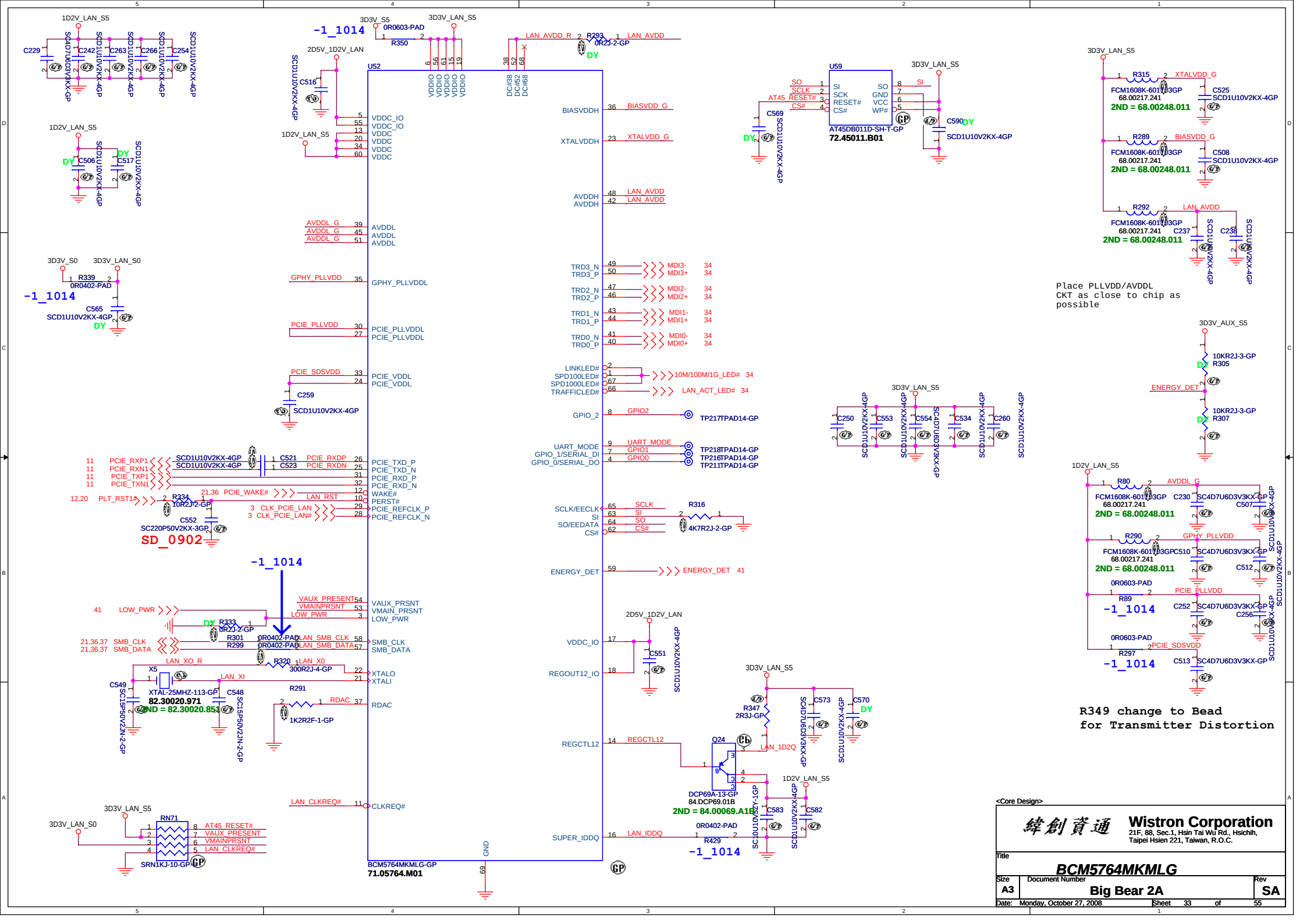
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

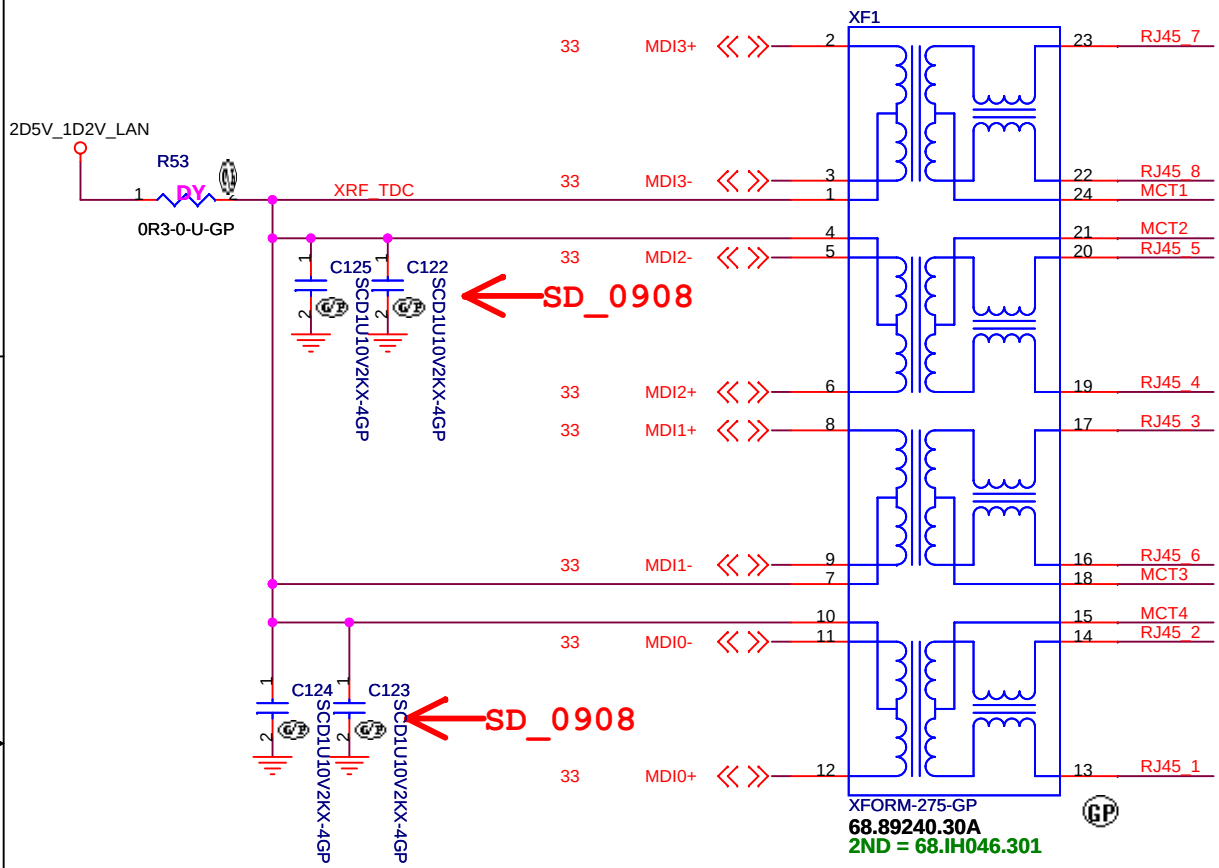
Title: Card Reader Connector

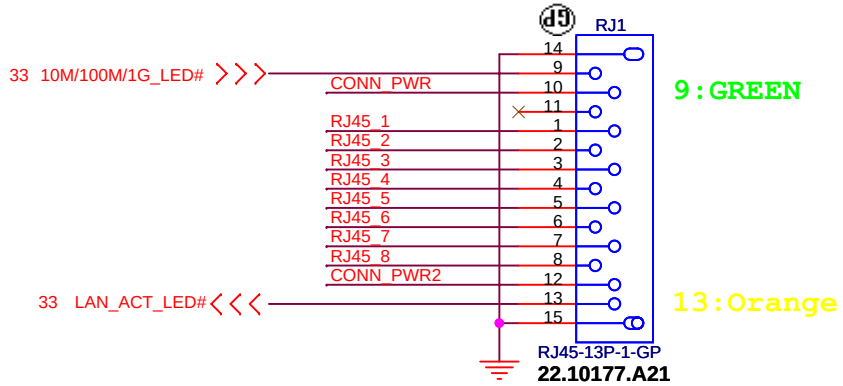
Size	Document Number	Rev
A3	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 32 of 55


U52
BCM5764MKMLG-GP
71.05764.M01
U59
AT45DB011D-SH-T-GP
72.45011.B01
Q24
DCP69A-13-GP
84.DCP69.01B
2ND = 84.00069.A1B
X5
XTAL-25MHZ-113-GP
82.30020.971
2ND = 82.30020.851
RN71
SRN1KJ-10-GP
-1_1014
SD_0902
DY
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R349 change to Bead
for Transmitter Distortion
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size
A3
Document Number
Big Bear 2A
Rev
SA
Date: Monday, October 27, 2008
Sheet 33 of 55

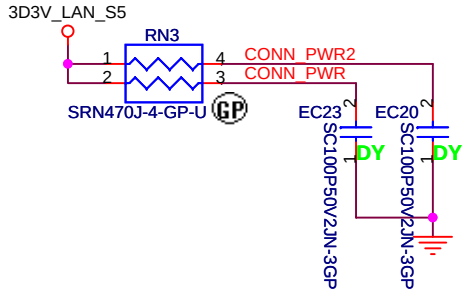
LAN Connector

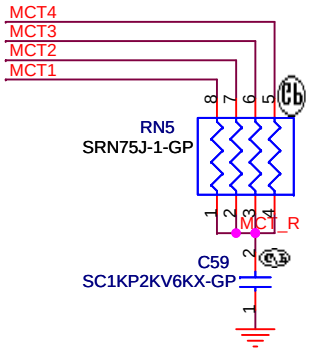




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

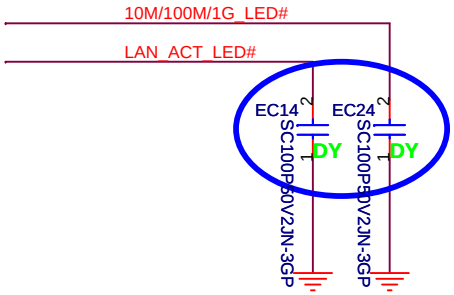
LAN Data: Yellow(B2), when LAN is transfering data.





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For EMI Near LAN1 CONN



<Core Design>

綽創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**		
Size: A4	Document Number: Big Bear 2A	Rev: SB
Date: Monday, October 27, 2008	Sheet 34 of 55	

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

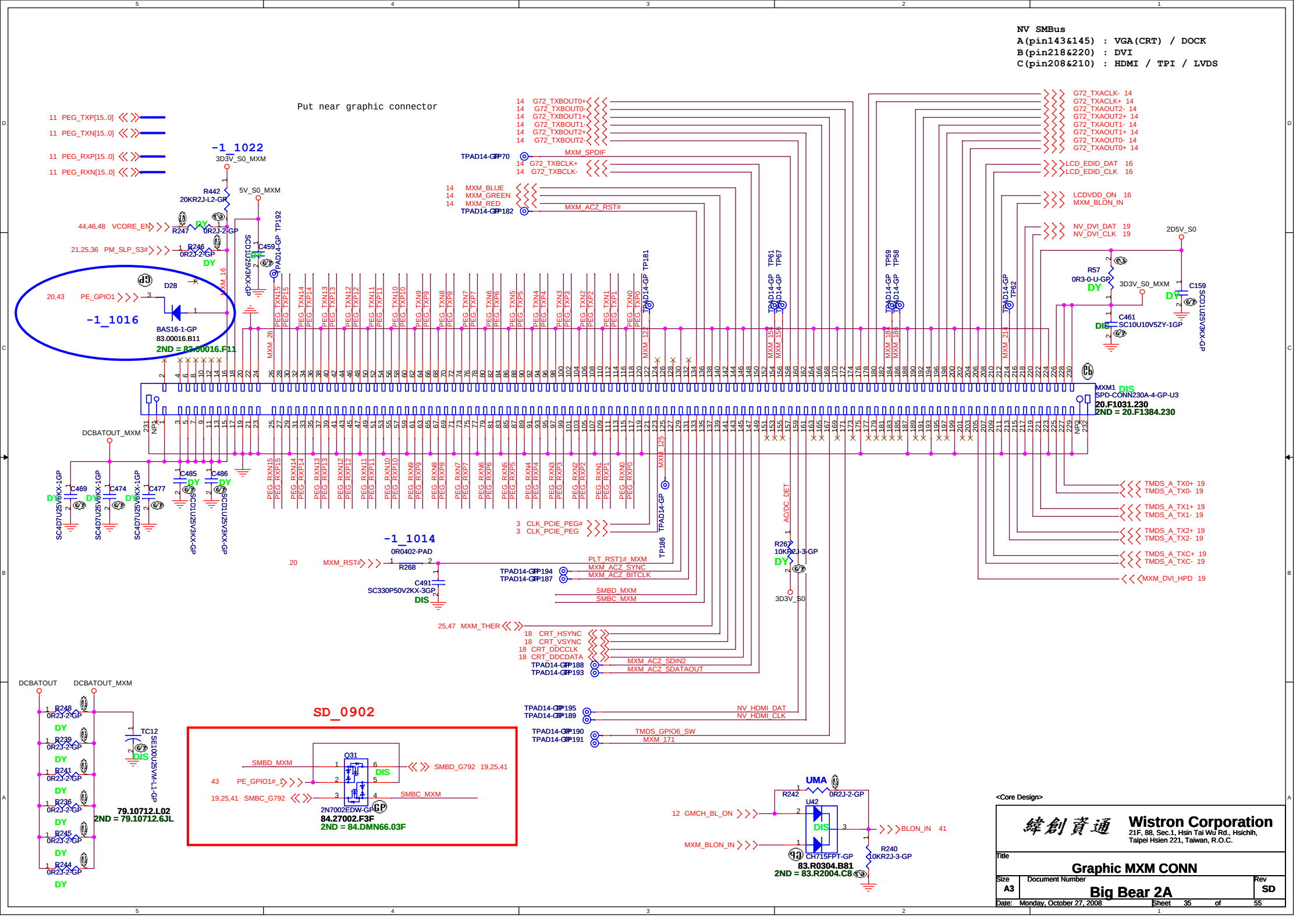
Put near graphic connector

-1_1022

-1_1016

-1_1014

SD_0902



<Core Design>

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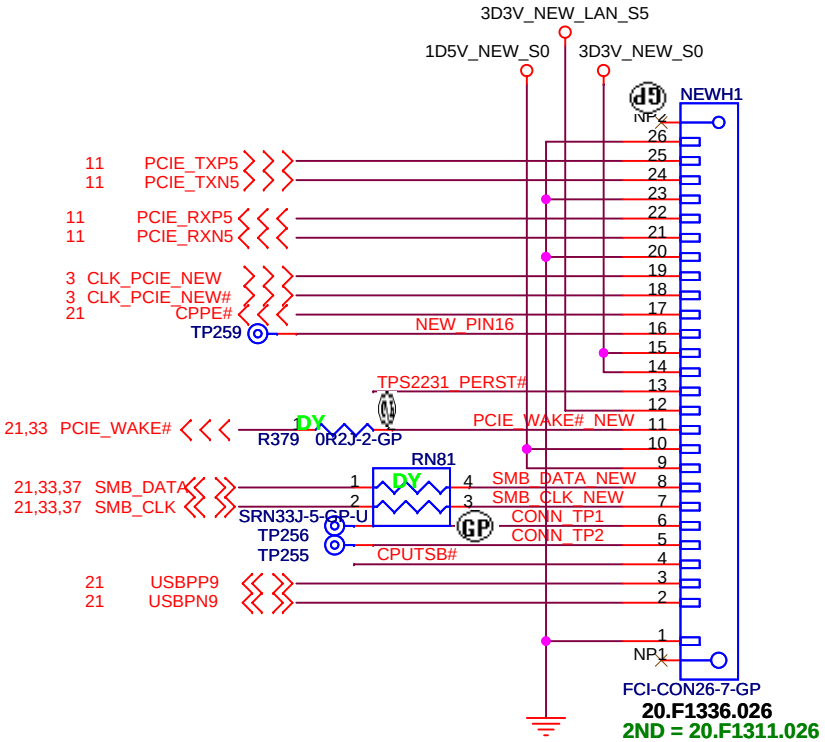
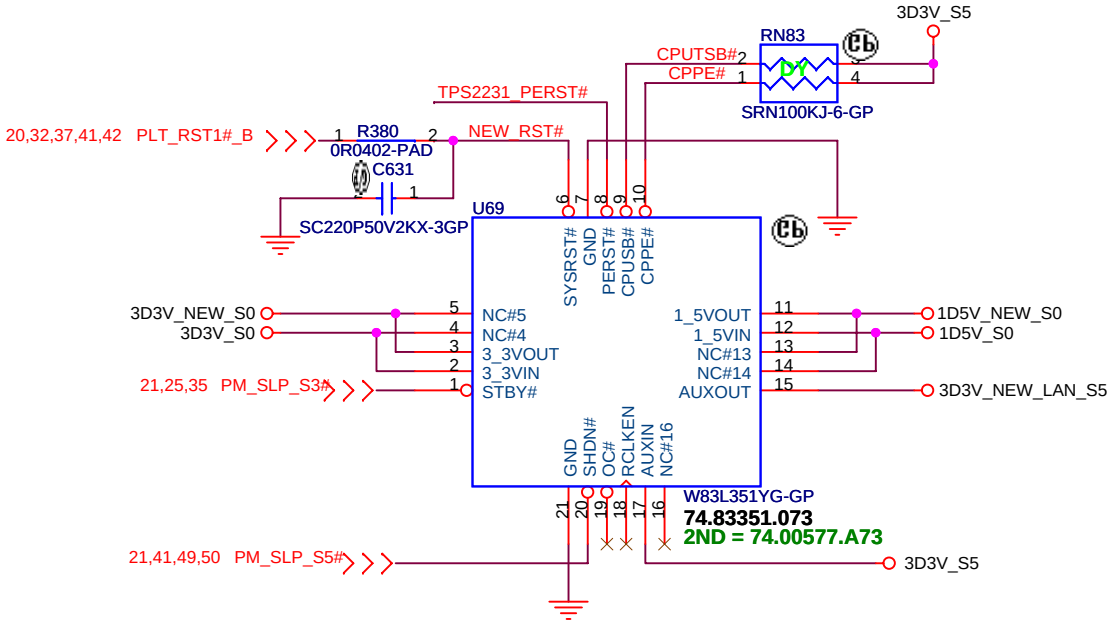
Title: Graphic MXM CONN

Size: A3 | Document Number: Big Bear 2A | Rev: SD

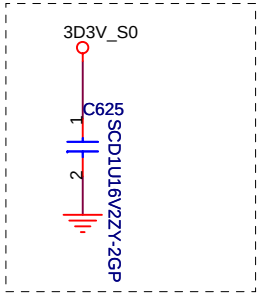
Date: Monday, October 27, 2008 | Sheet 35 of 55

NEWCARD Connector

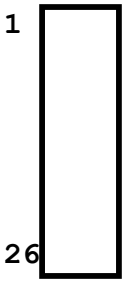


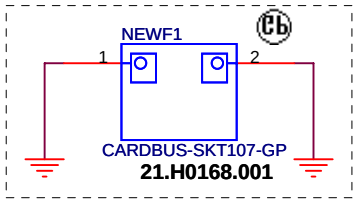


Place them Near to Chip

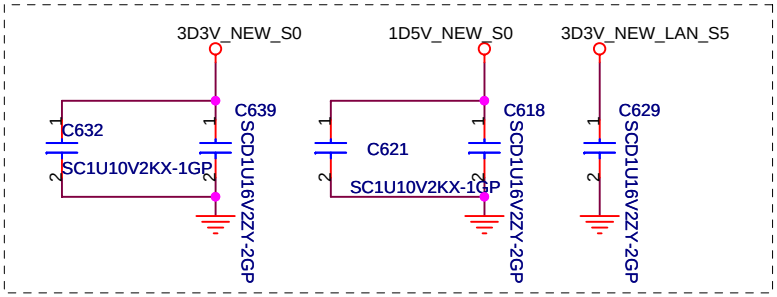


TOP VIEW





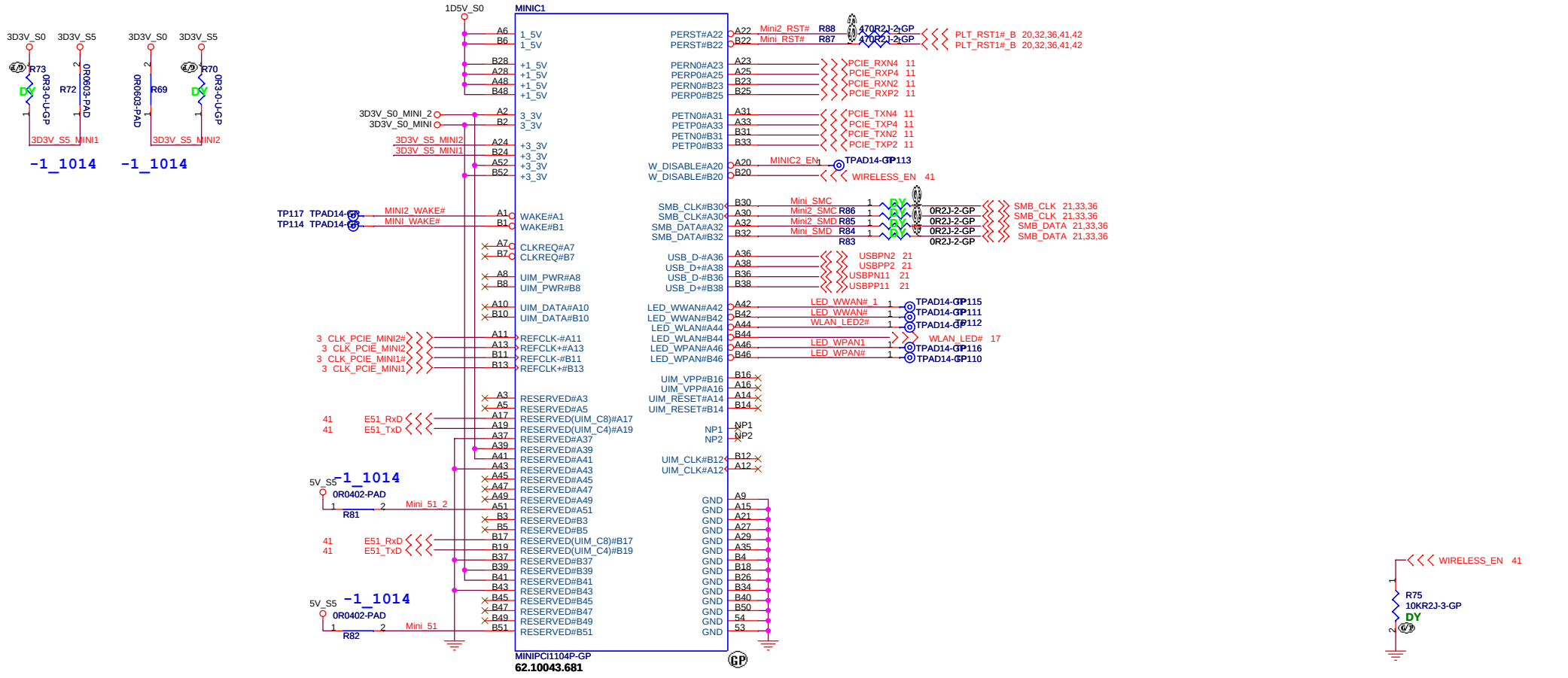
Place them Near to Connector

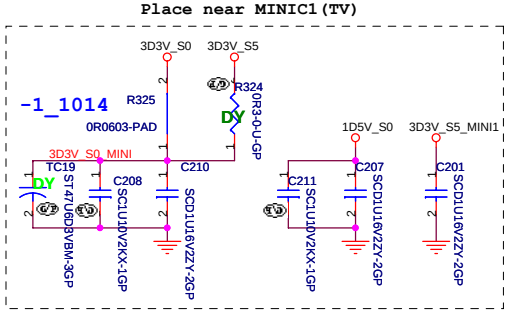


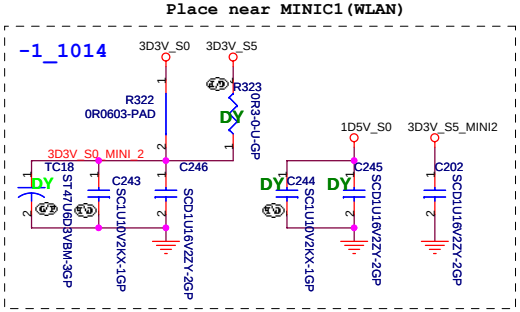
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: NEW CARD		
Size: A4	Document Number: Big Bear 2A	Rev: SC
Date: Monday, October 27, 2008	Sheet 36 of 55	

Mini Card Connector(TV) UPPER SLOT
Mini Card Connector(WLAN) LOWER SLOT







<Core Design>

Wistron Corporation
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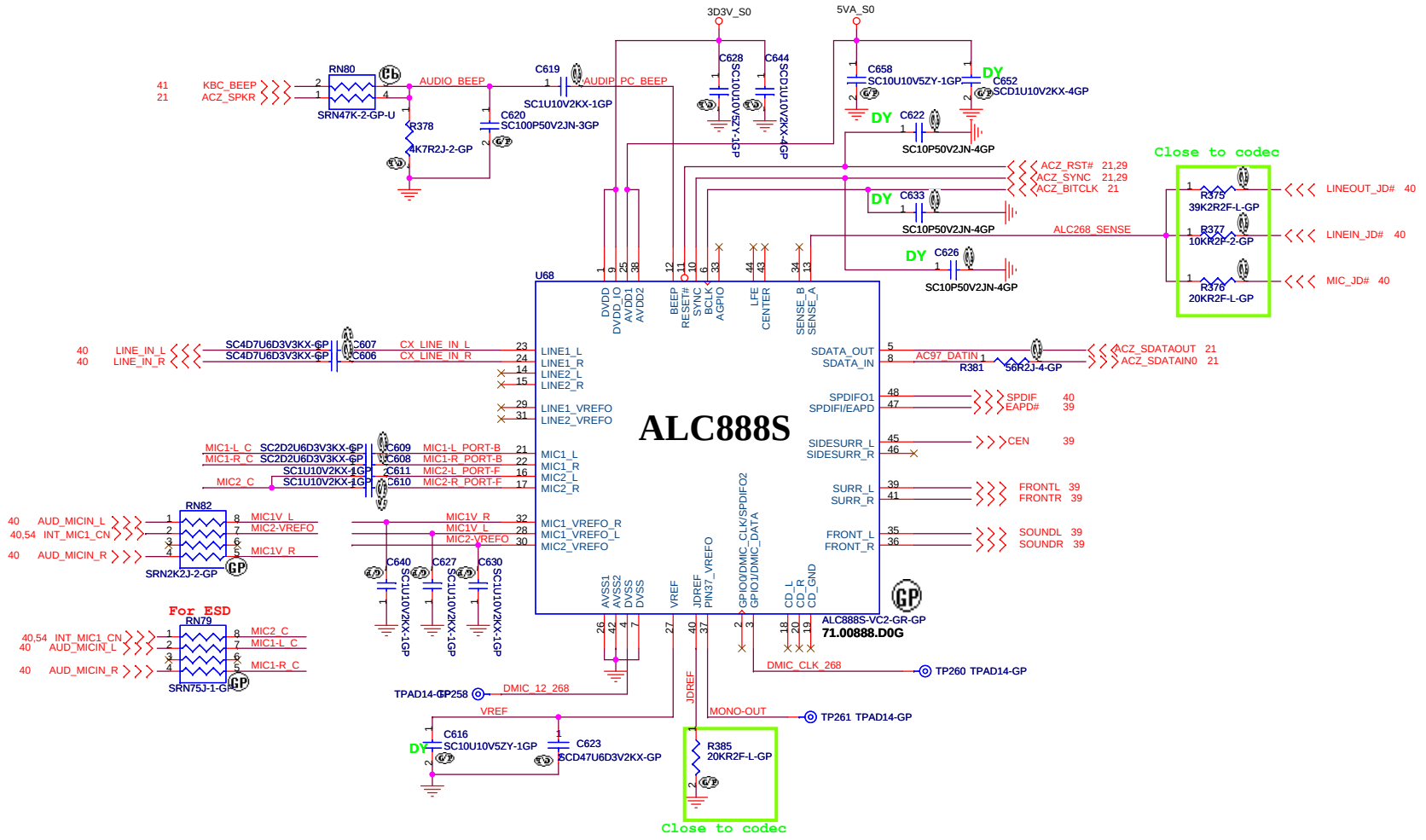
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 37 of 55



<Core Design>

Wistron Corporation
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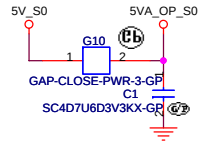
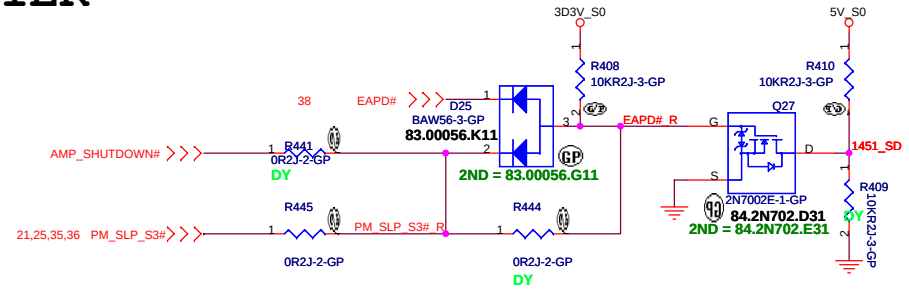
Title: ***Azalia codec ALC268***

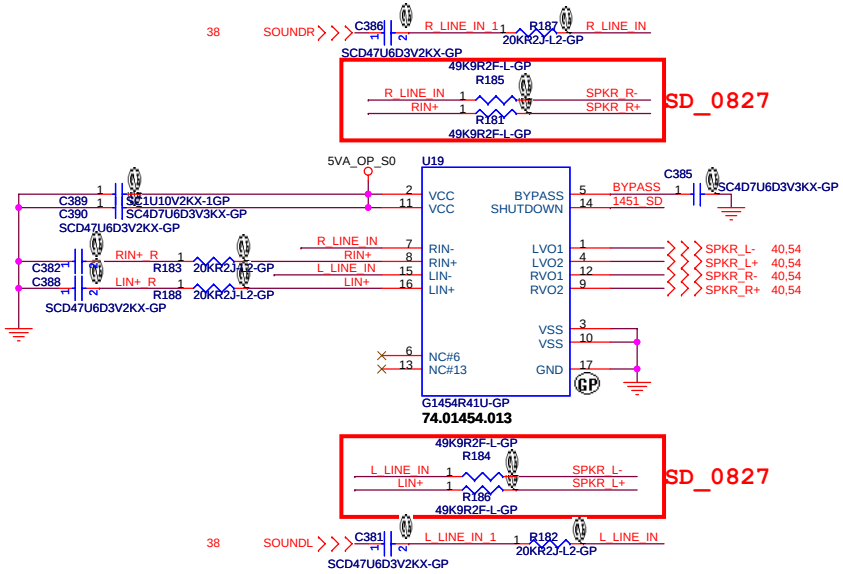
Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 38 of 55

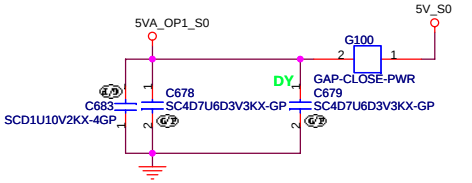
AUDIO OP AMPLIFIER

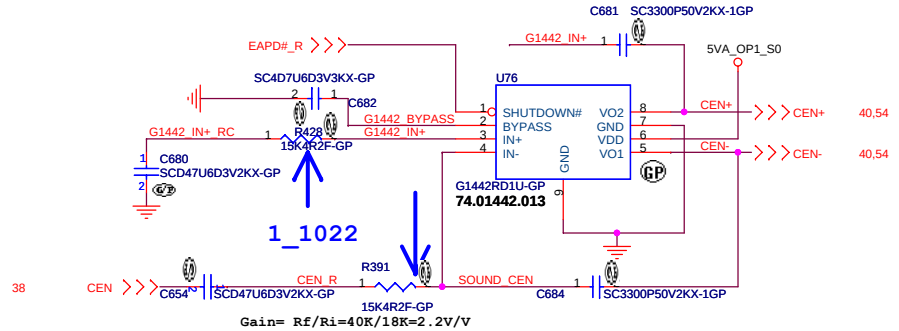






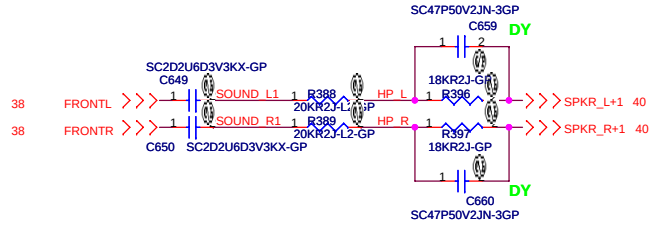
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W



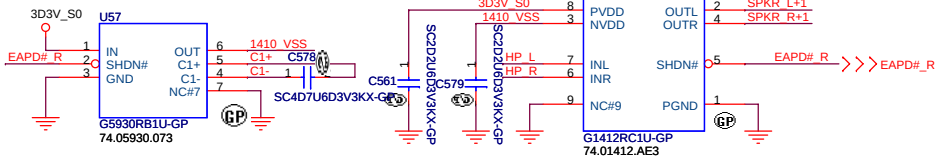


Gain= Rf/Ri=40K/18K=2.2V/V
f(HP)=1/(2 Pi*18K*0.47uf)=18Hz
If VIN= 1.54V Gain=2.2V/V RL=4Ω VO(peak) =3.38V V(rms)=2.390V
Power= 2.390^2/4=1.428W

KBC_MUTE_GPIO8



Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?



<Core Design>

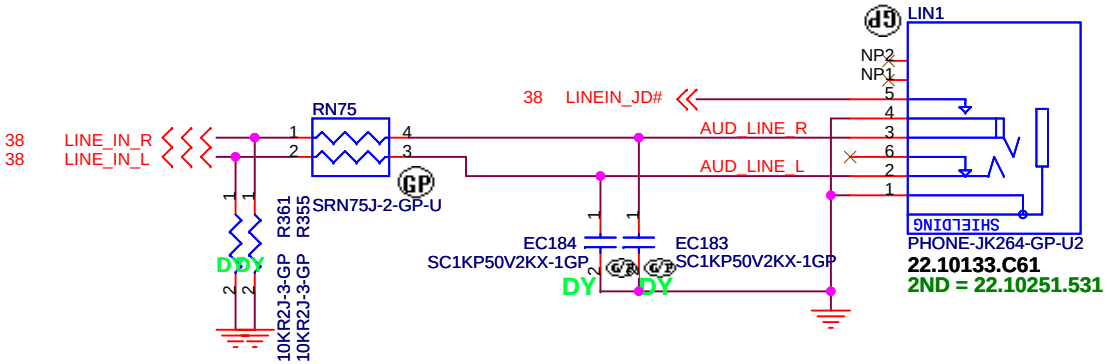
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

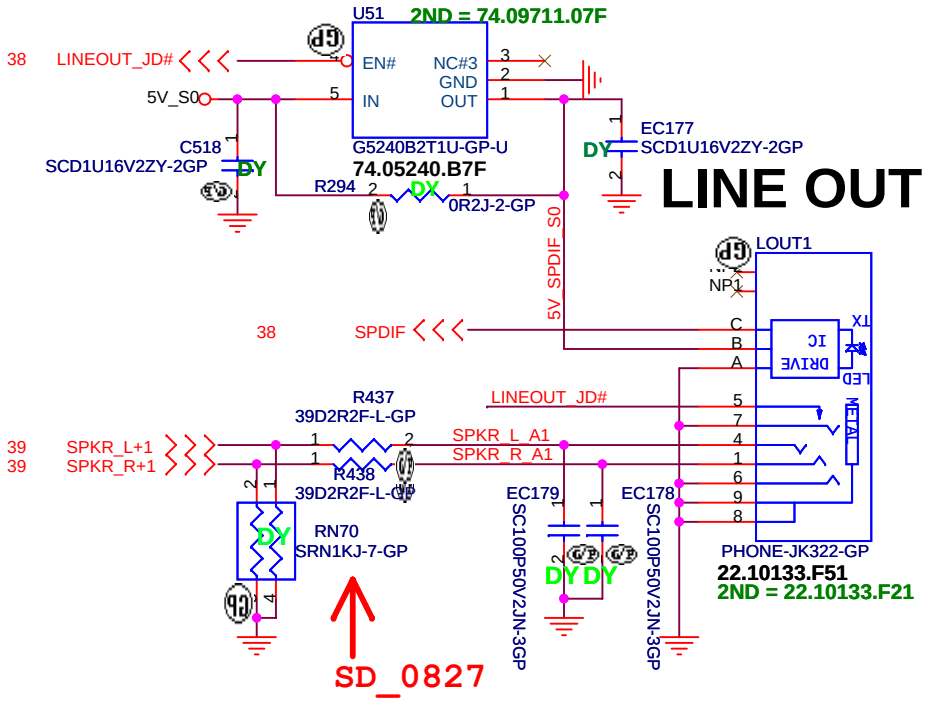
Size	Document Number	Rev
A3	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 39 of 55

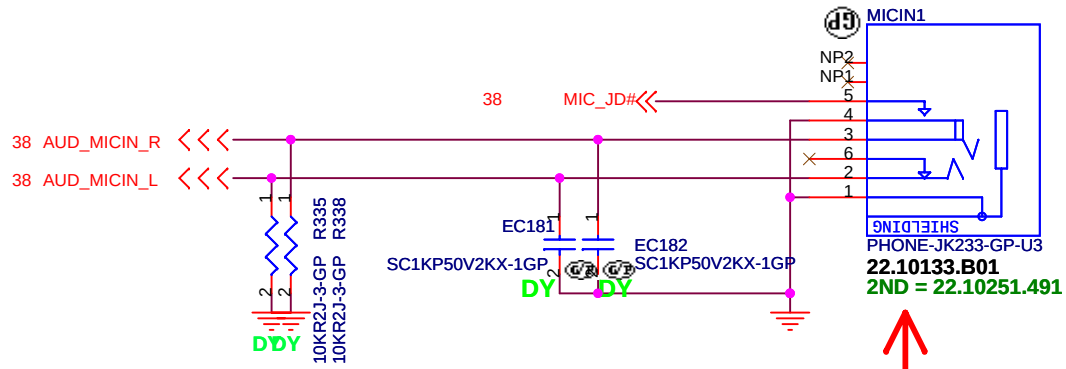
LINE IN



LINE OUT

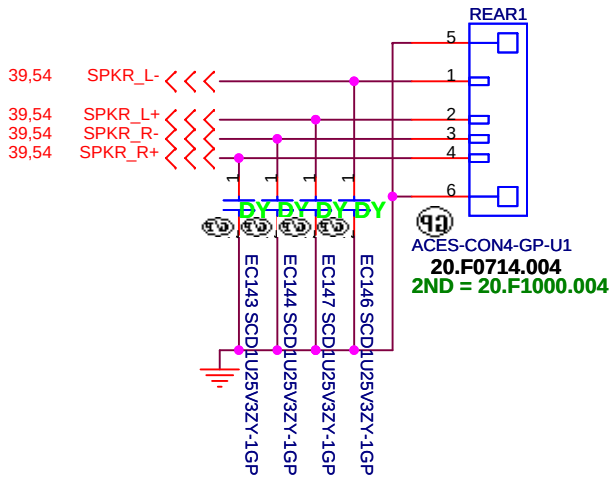


MIC IN

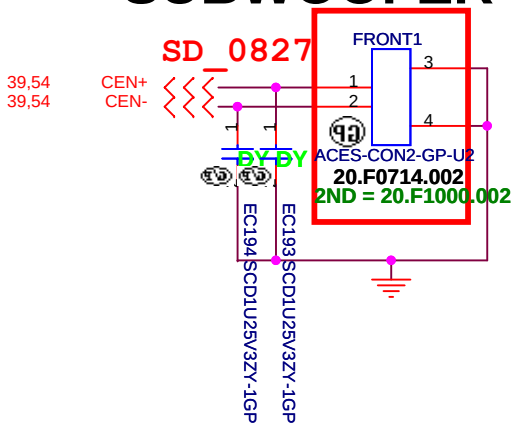


SD_0912 change 2nd

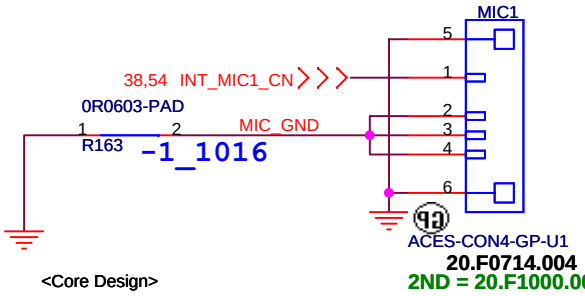
REAR Speaker



SUBWOOFER



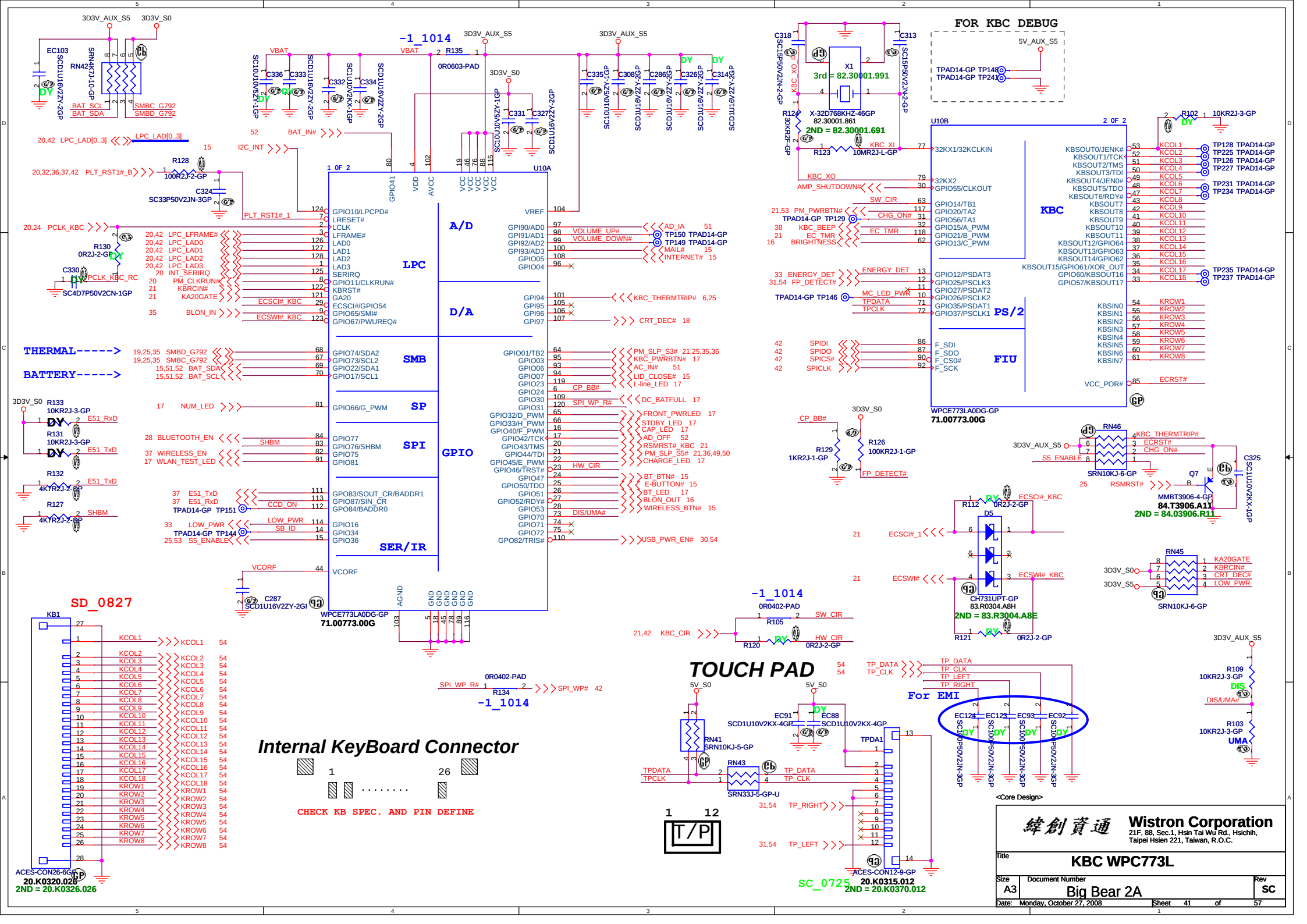
INT. MIC



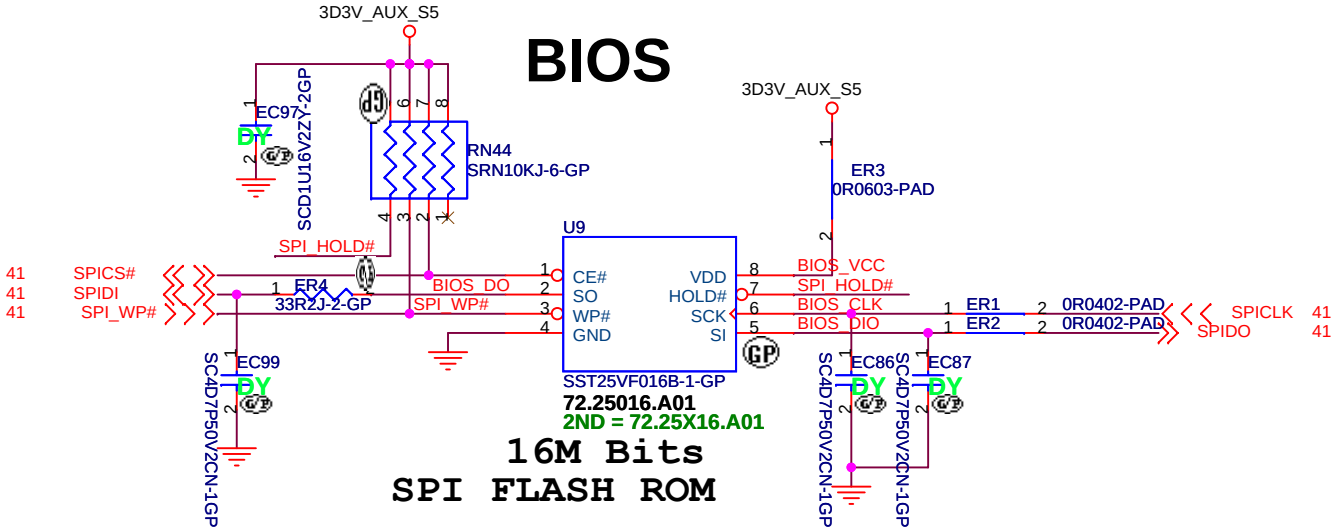
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
Size: A4	Document Number: Big Bear 2A	Rev: SD
Date: Monday, October 27, 2008	Sheet 40 of 55	

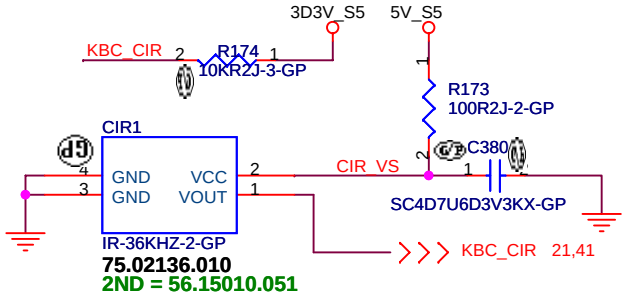

FOR KBC DEBUG
-1_1014
SD_0827
TOUCH PAD
Internal KeyBoard Connector
CHECK KB SPEC. AND PIN DEFINE
For EMI
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
WPCE773LA0DG-GP
71.00773.00G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
Big Bear 2A
Monday, October 27, 2008

BIOS



16M Bits
SPI FLASH ROM

CIR Module

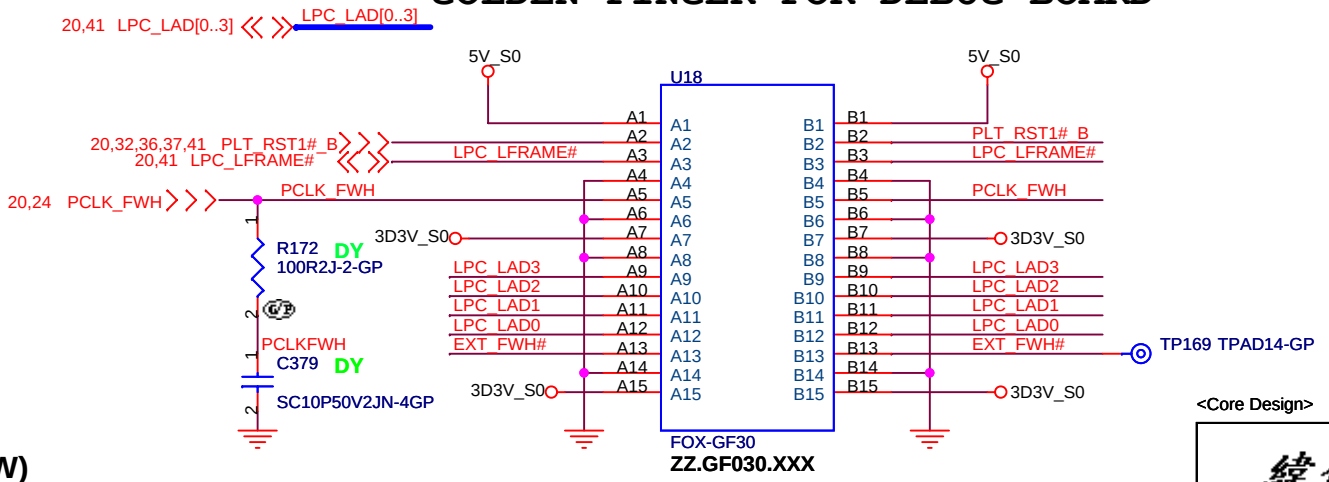


GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



<Core Design>

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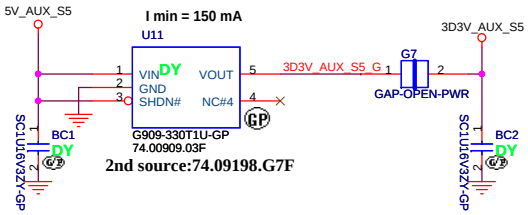
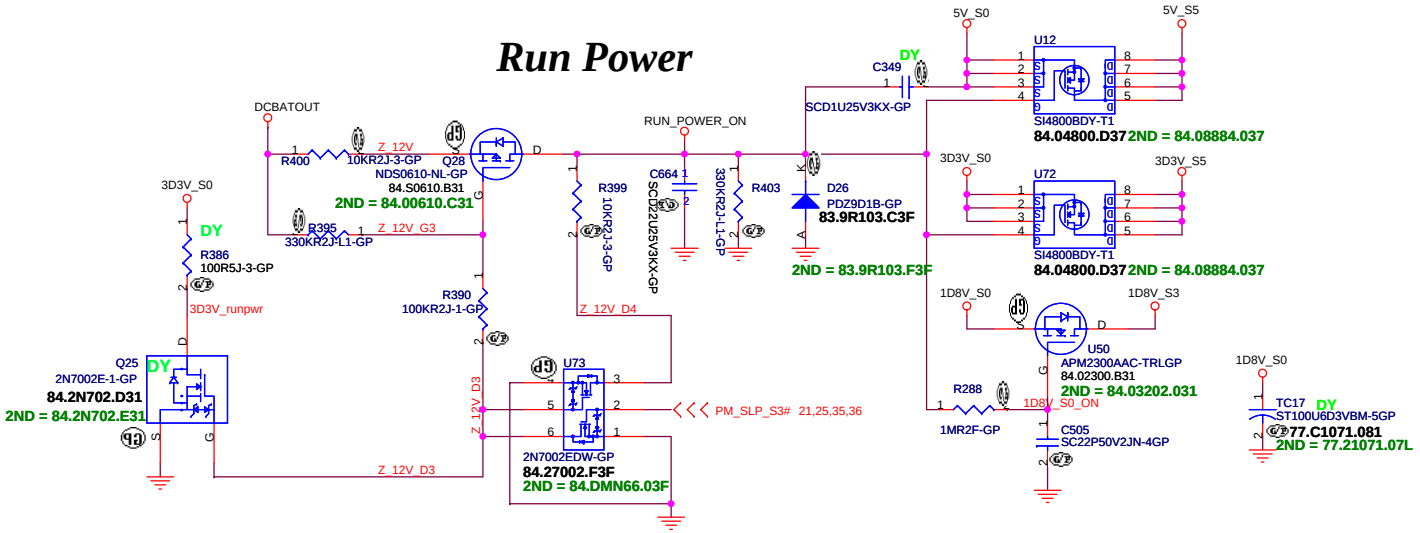
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS & CIR***	
Size: A4	Document Number: **Big Bear 2A**	Rev: SB
Date: Monday, October 27, 2008	Sheet 42 of 57	

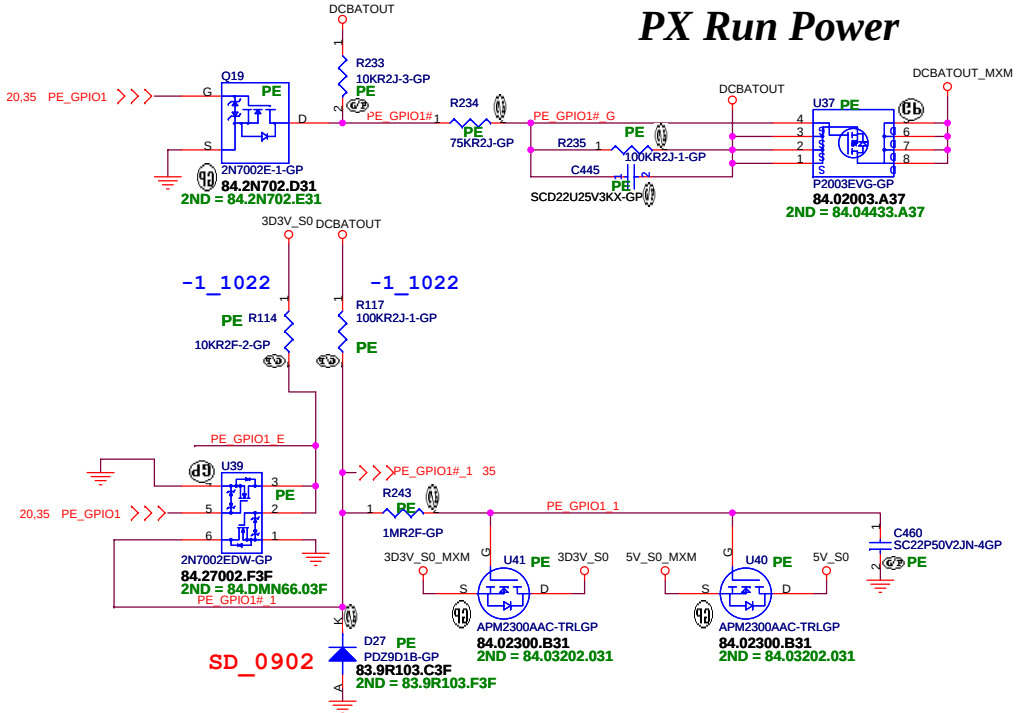
Aux Power 3D3V_AUX_S5



Run Power

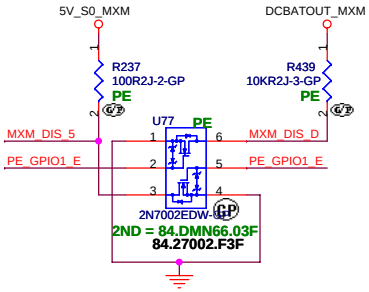


PX Run Power



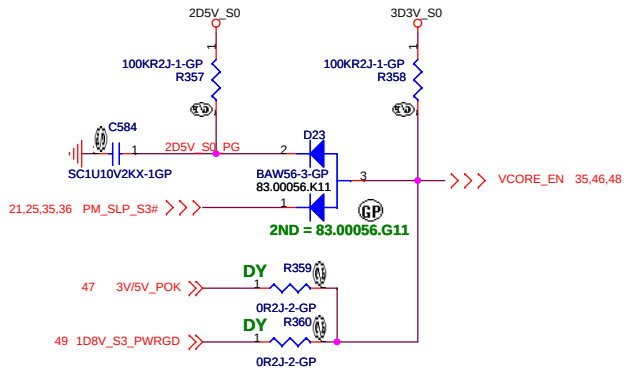
SD_0902

PX Run Power Discharge circuit

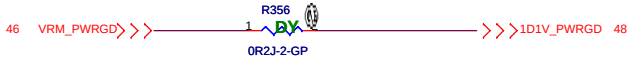


<Core Design>

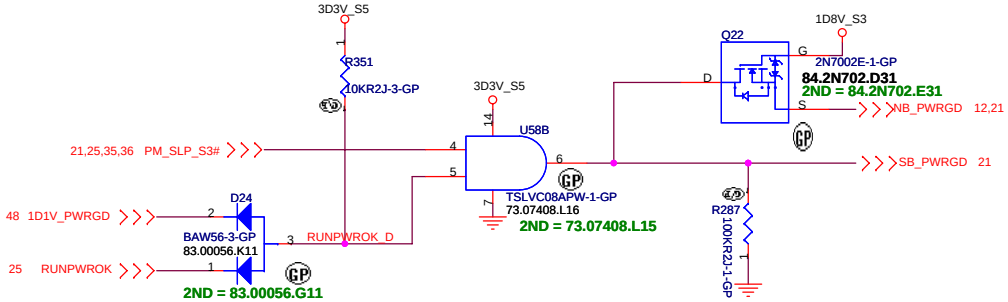
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**RUN POWER and 3D3V_AUX_S5**
Size: A3	Document Number: **Big Bear 2A**
Rev: SD	
Date: Monday, October 27, 2008	Sheet 43 of 57



P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

緯創資通 **Wistron Corporation**
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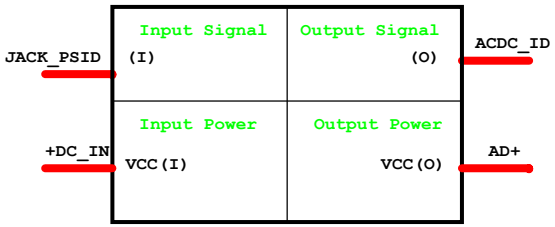
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER ON LOGIC***

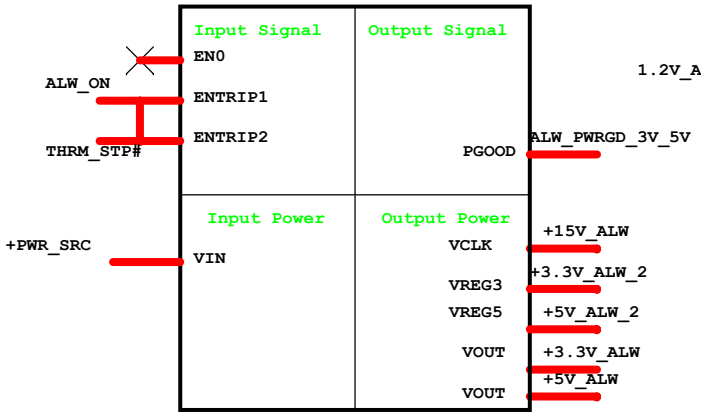
Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 44 of 57

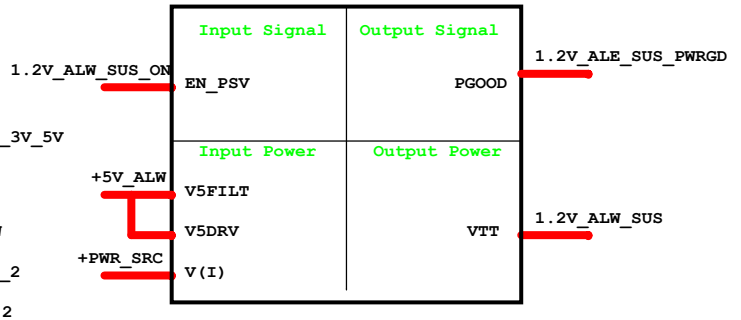
Adapter



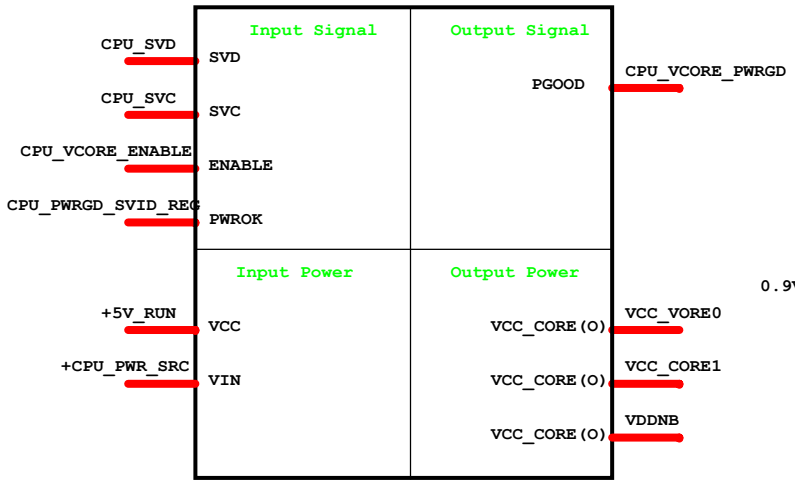
SN0608098



DCDC 1D2V(TPS5117)

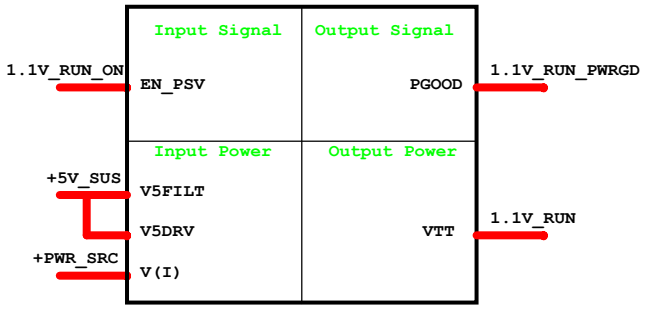


CPU_CORE
ISL6265HRTZ

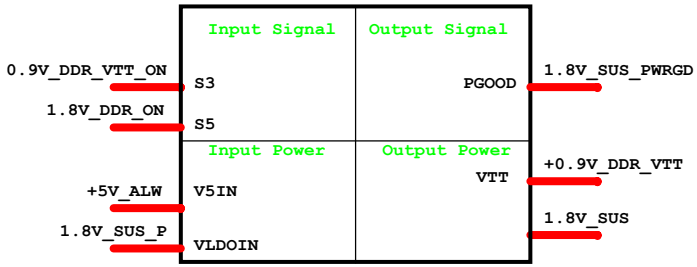


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

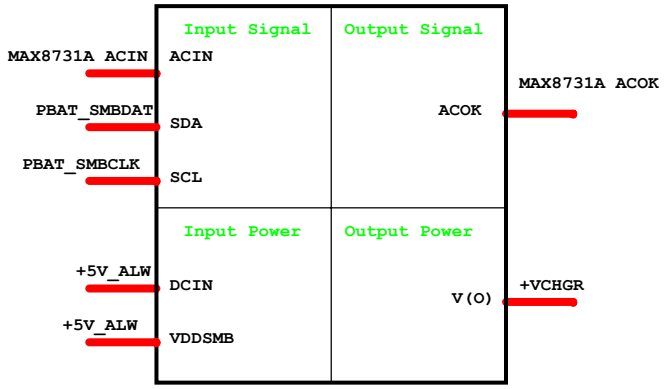
1D1V(TPS5117)



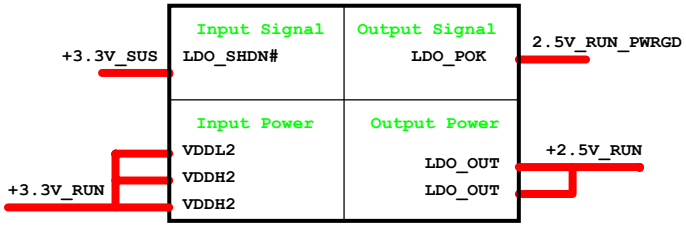
1D8V/0D9V(TPS5116)



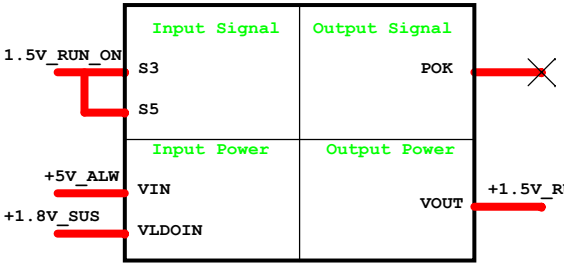
CHARGER BQ24745



2.5V LDO
EMC4002



1.5V_LDO



<Core Design>

Wistron Corporation
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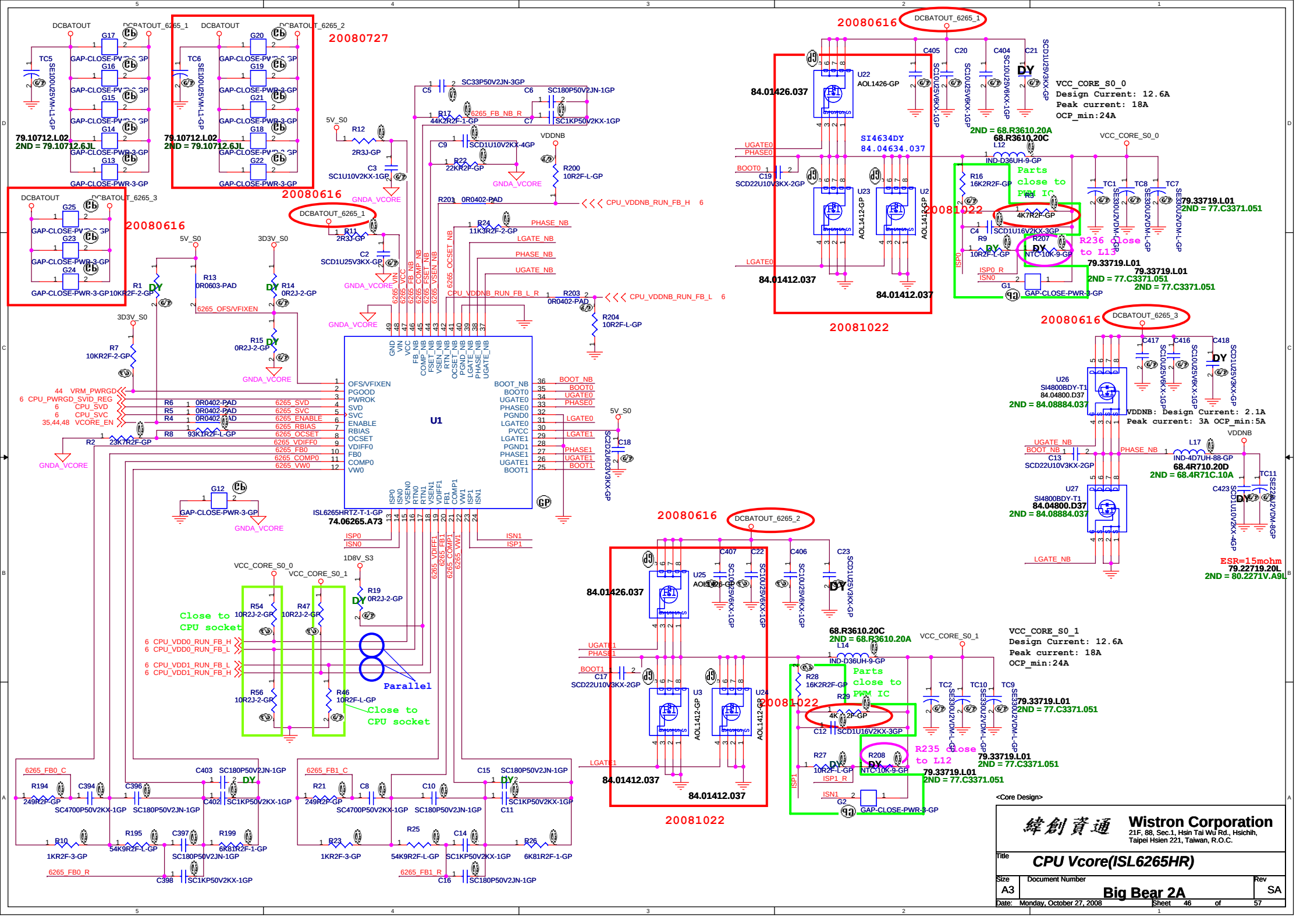
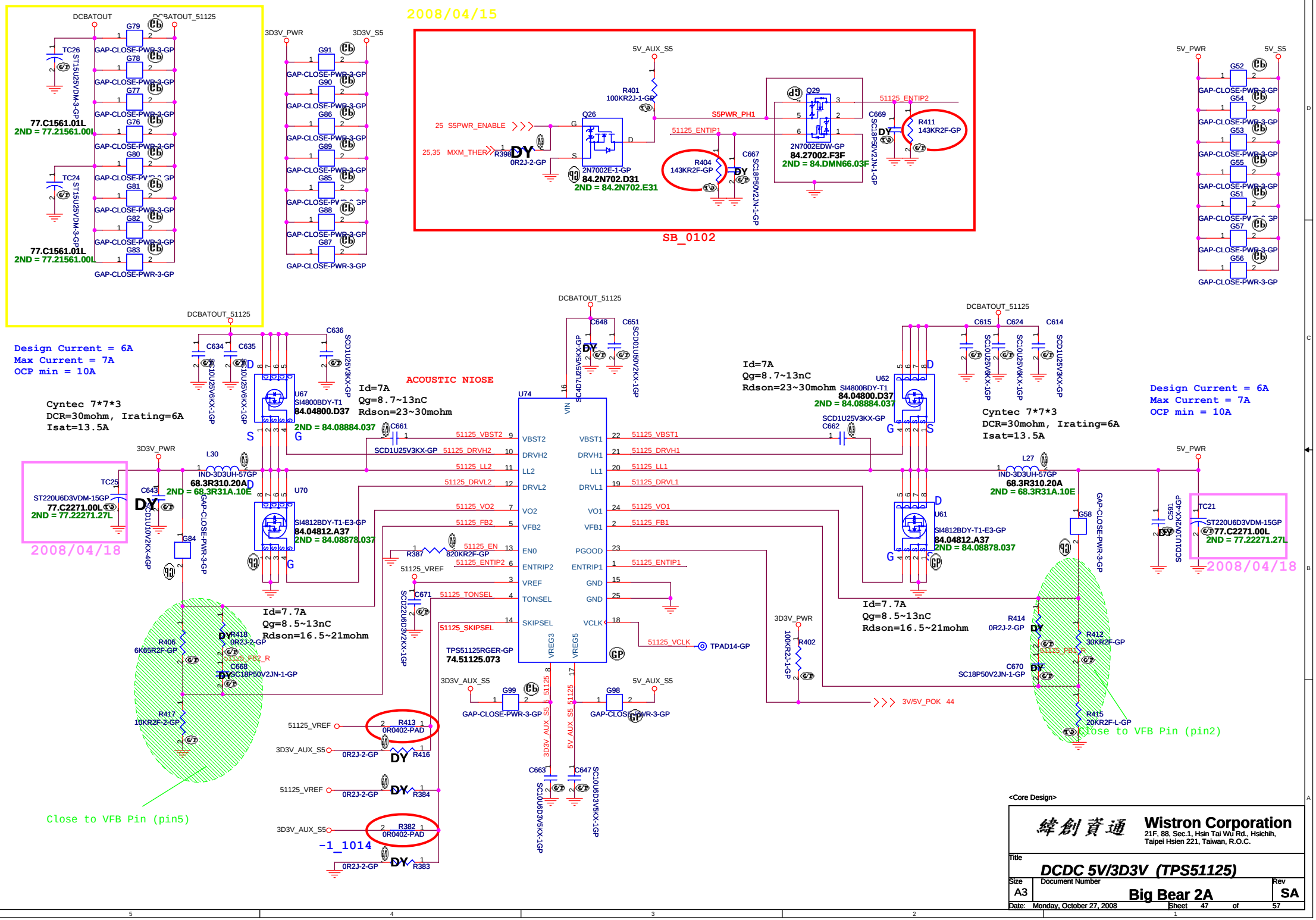
Taipei Hsien 221, Taiwan, R.O.C.

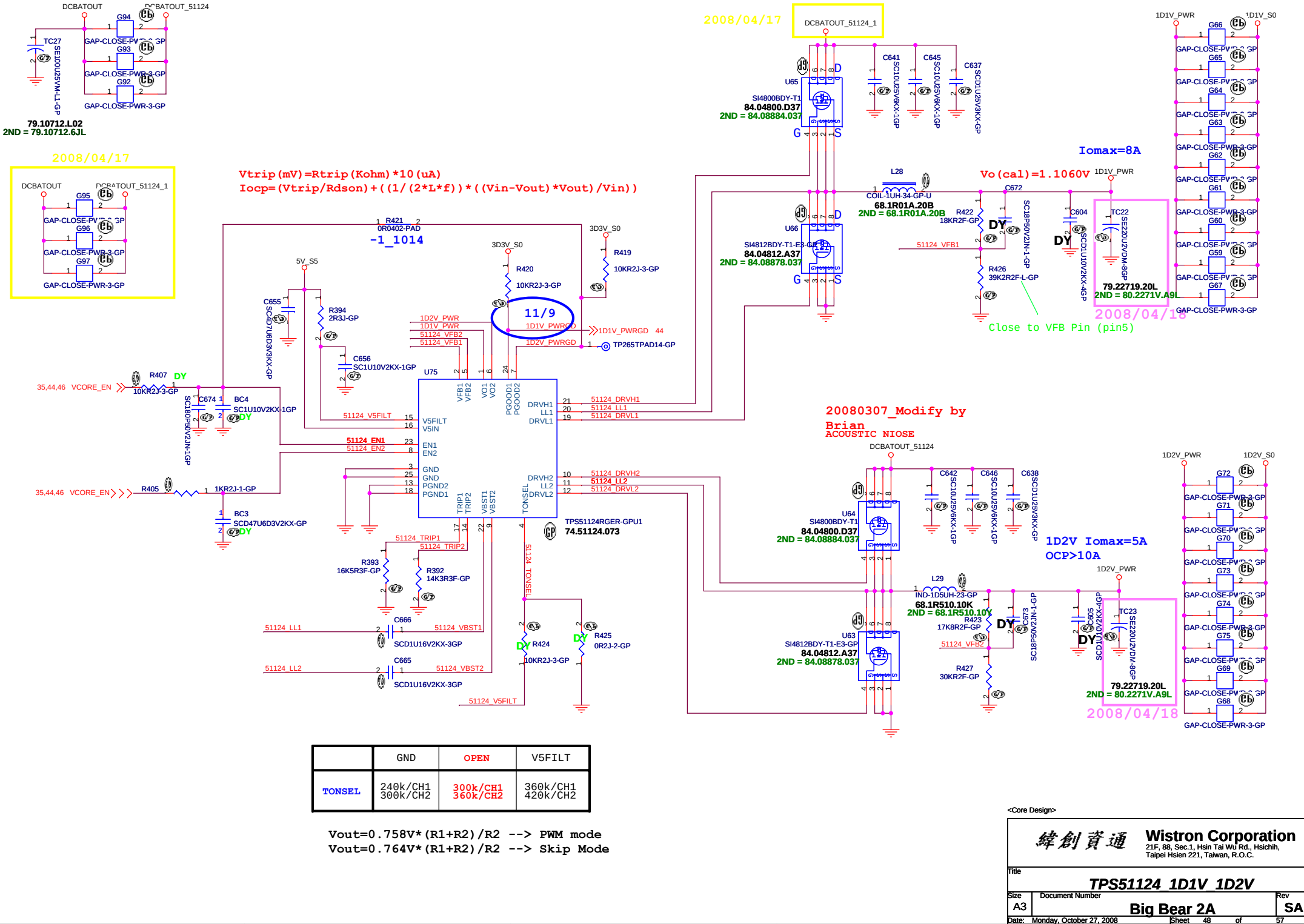
Title: Power Block Diagram

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 45 of 57


20080727
20080616
20081022
U1
ISL6265HRTZ-T-1-GP
74.06265.A73
OFS/VFIXEN
PGOOD
PWROK
SVD
SVC
ENABLE
RBIAS
OCSET
VDIFF0
FB0
COMP0
VW0
GND
VIN
VCC
FB_NB
COMP_NB
FSET_NB
VSEN_NB
RTN_NB
OCSET_NB
PGND_NB
LGATE_NB
PHASE_NB
UGATE_NB
BOOT_NB
BOOT0
UGATE0
PHASE0
PGND0
LGATE0
PVCC
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISP0
ISN0
VSEN0
RTN0
VSEN1
RTN1
VDIFF1
FB1
COMP1
VW1
ISP1
ISN1
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Close to CPU socket
Parallel
Parts close to PWM IC
R235 close to L12
R236 close to L13
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Big Bear 2A
Size A3
Rev SA
Date: Monday, October 27, 2008
Sheet 46 of 57


2008/04/15
SB_0102
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
ACOUSTIC NIOSE
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
-1_1014
2008/04/18
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Big Bear 2A
Monday, October 27, 2008



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

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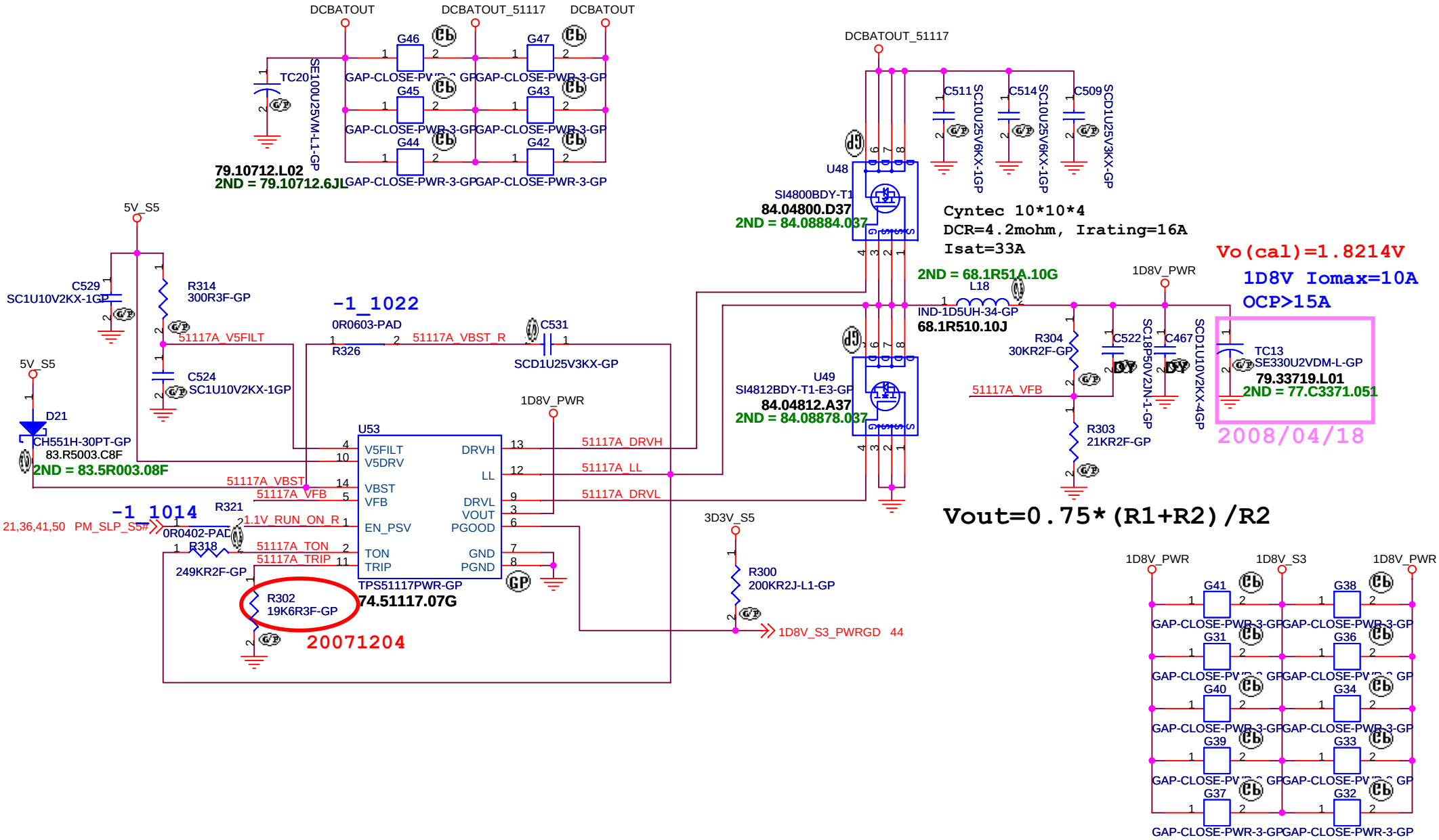
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 48 of 57

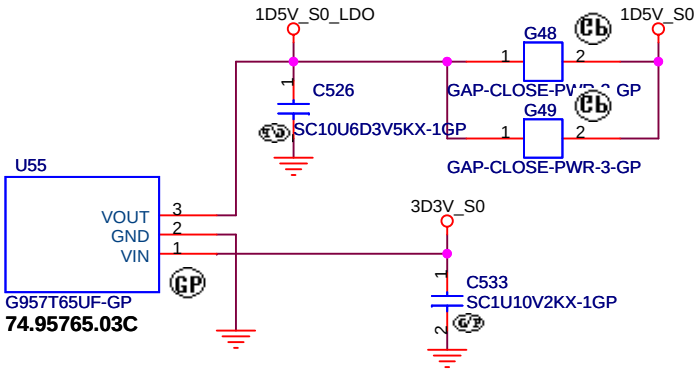


<Core Design>

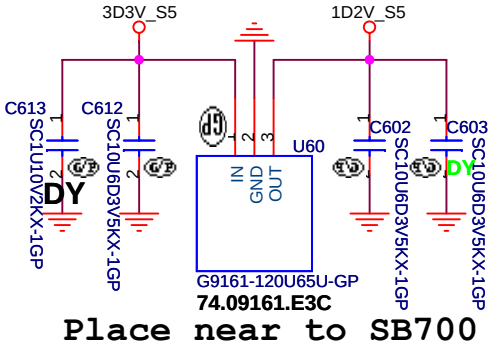
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***1D8V(TPS5117)***	
Size: A4	Document Number: **Big Bear 2A**	Rev: SB
Date: Monday, October 27, 2008	Sheet 49 of 57	

G957

1D5V_S0
Iomax=1A

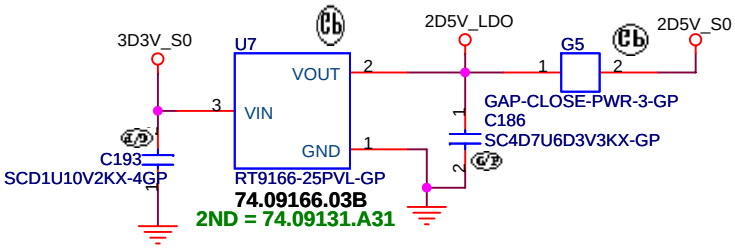


1D2V_S5
Iomax=400mA

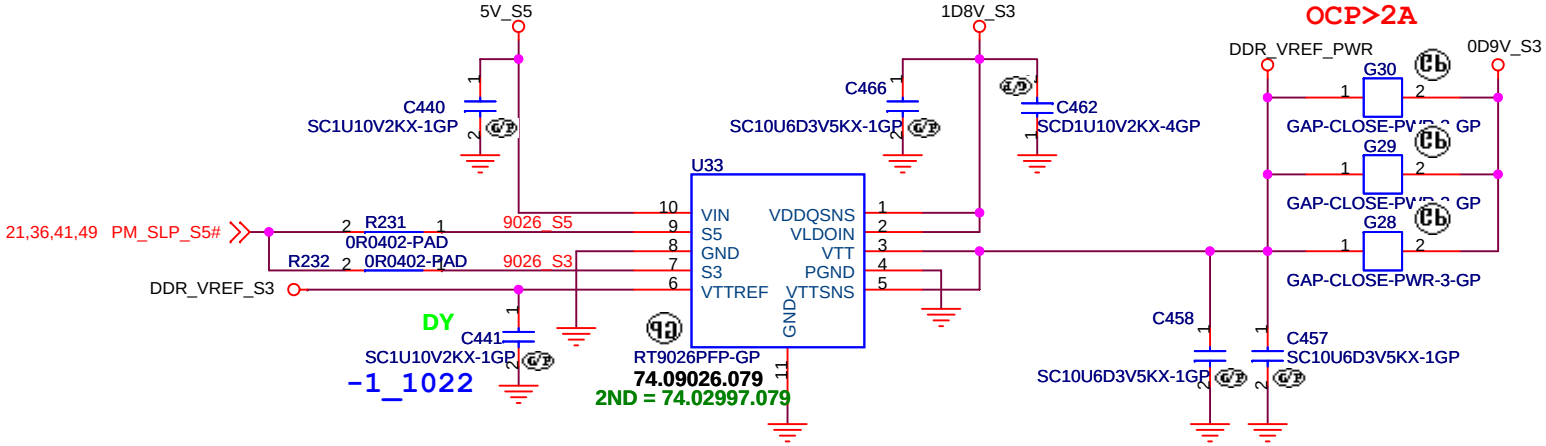


Place near to SB700

2D5V_S0
Iomax=0.3A 2D5V/300mA



Iomax=1A
OCP>2A



<Core Design>

緯創資通 Wistron Corporation
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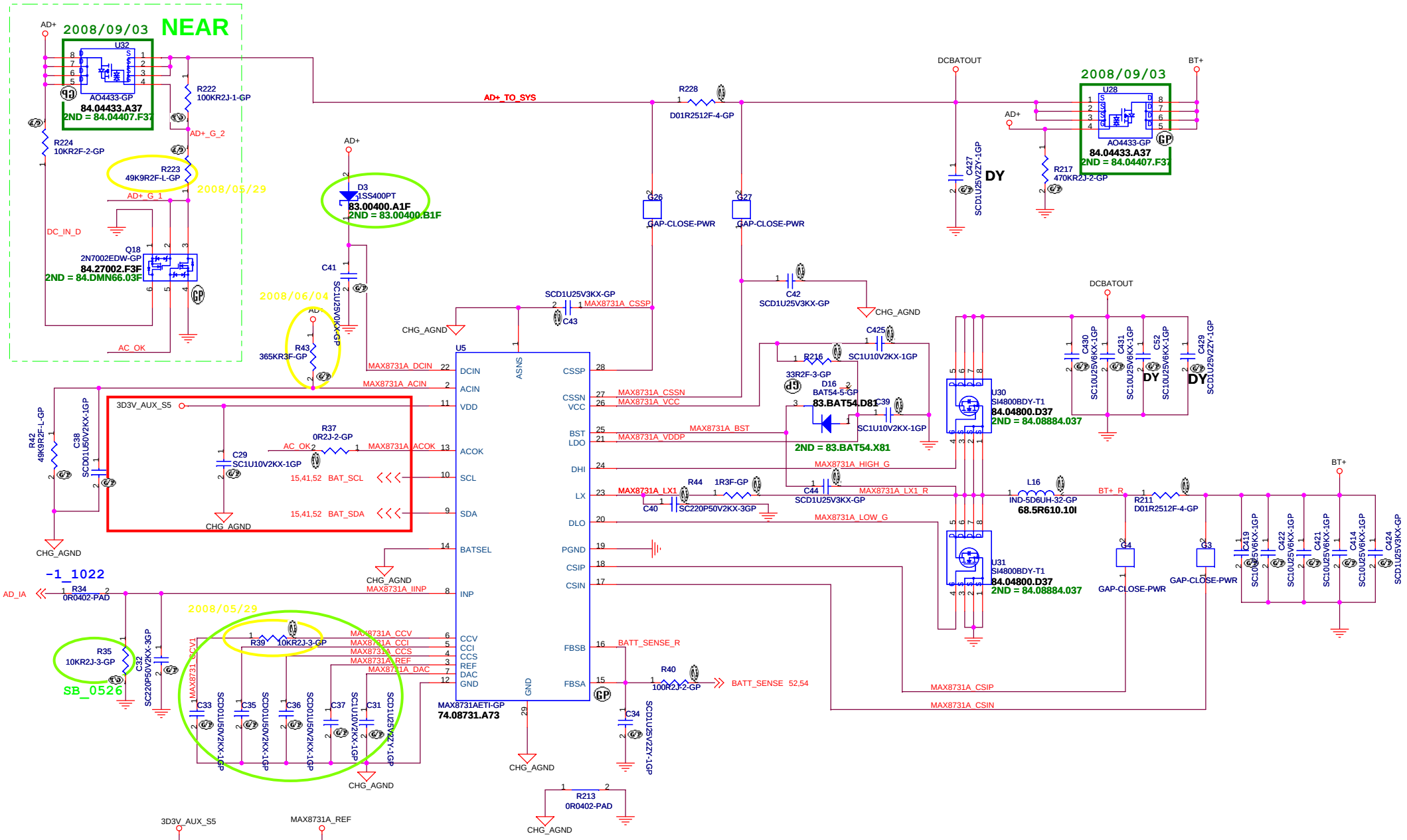
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V&2D5V&1D25V&1D5V

Size	Document Number	Rev
A4	Big Bear 2A	SB

Date: Monday, October 27, 2008 Sheet 50 of 57



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緯創資通 **Wistron Corporation**
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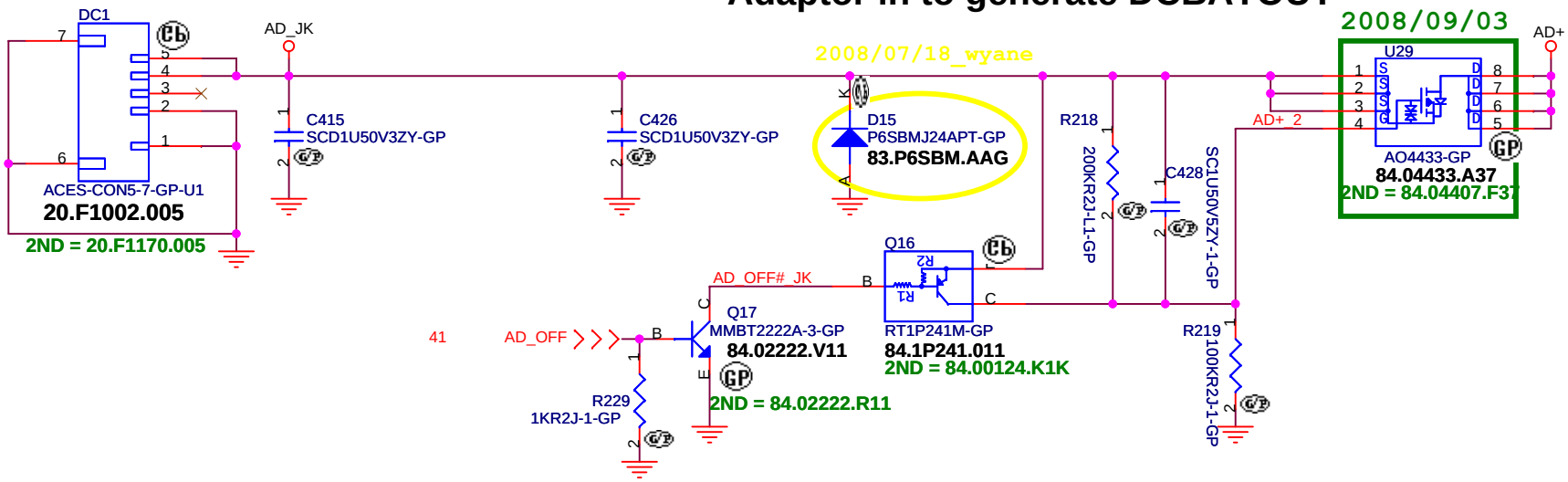
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX8731A Charger**

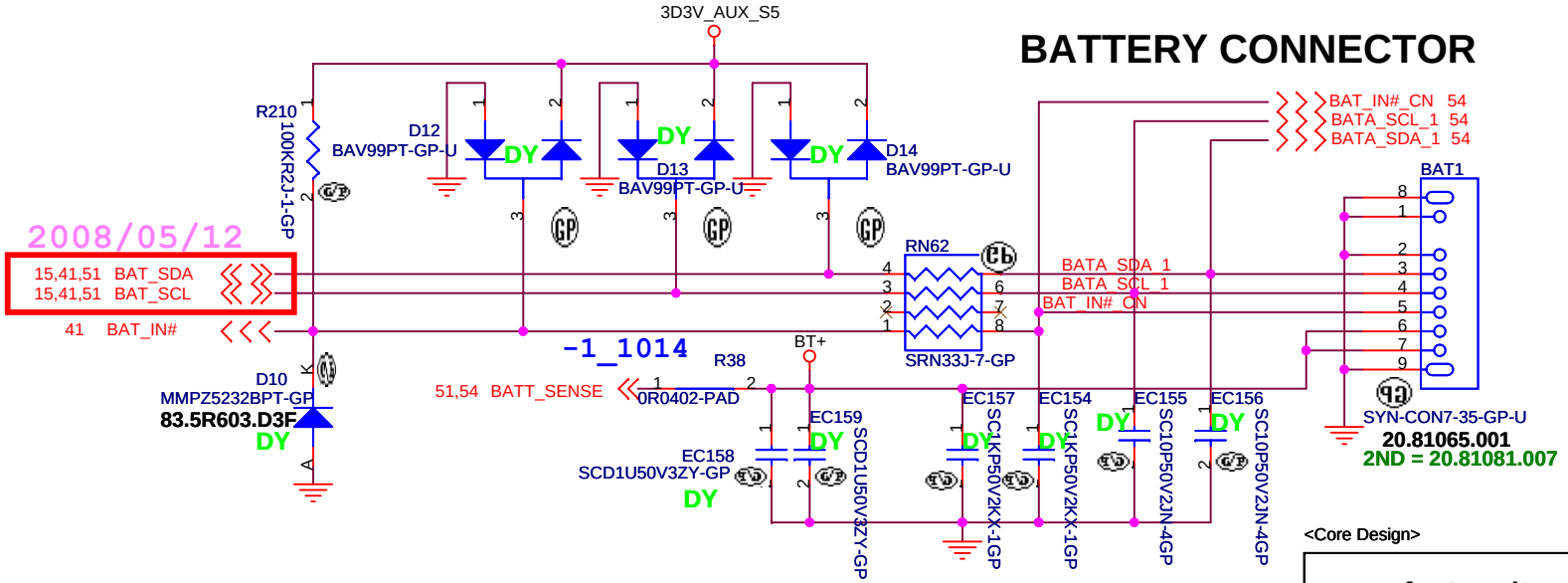
Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 51 of 57

Adaptor in to generate DCBATOUT

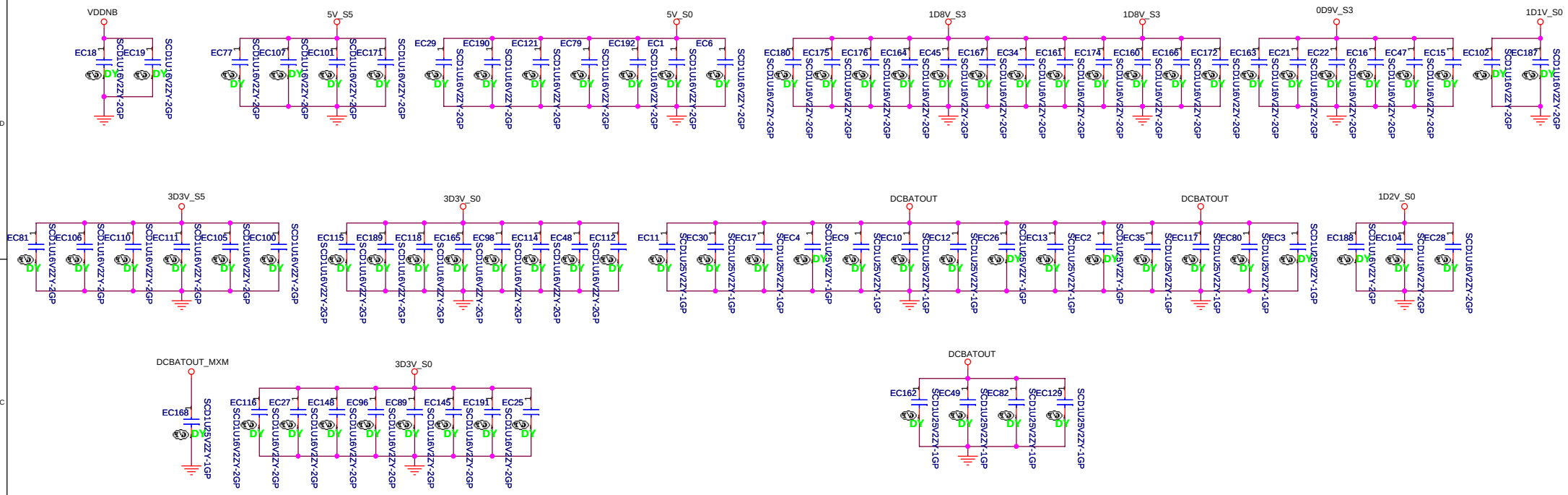


BATTERY CONNECTOR



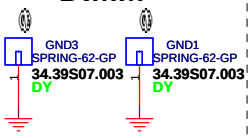
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size: **A4**	Document Number: **Big Bear 2A**	Rev: SA
Date: Monday, October 27, 2008	Sheet 52 of 57	

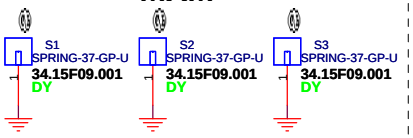


SPRING ON BOTTOM

DIMM



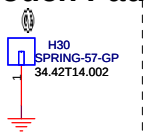
MXM



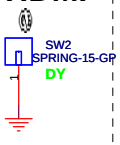
SPRING ON TOP

SD_0903

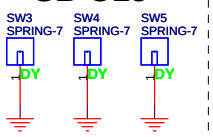
Touch Pad



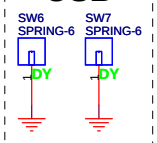
HDMI



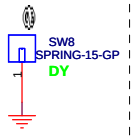
SB-U15



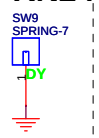
USB



Jack

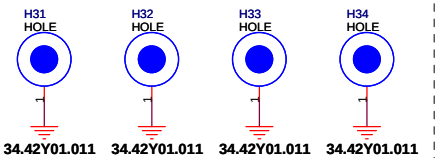


RN24

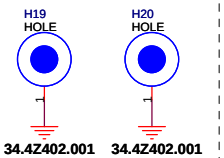


STAND OFF ON BOTTOM

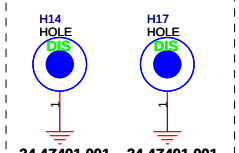
CPU & NB



Mini Card

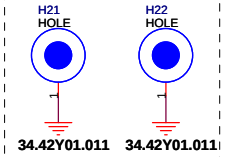


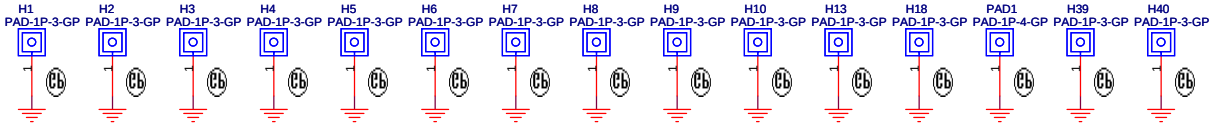
MXM



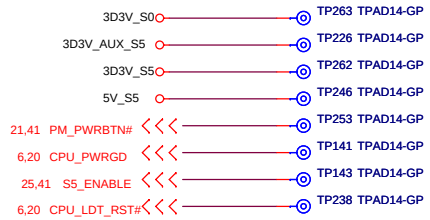
STAND OFF ON TOP

MDC





Check test point



Test Point放在Dimm Door打開可量測處

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size: A3 | Document Number: **Big Bear 2A** | Rev: SD

Date: Monday, October 27, 2008 | Sheet 53 of 57

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Size: A3 | Document Number: **Big Bear 2A** | Rev: SC

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