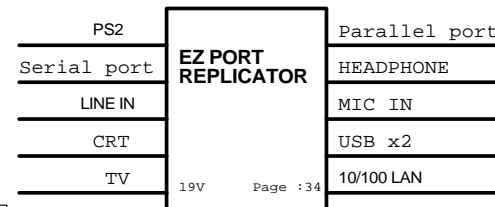
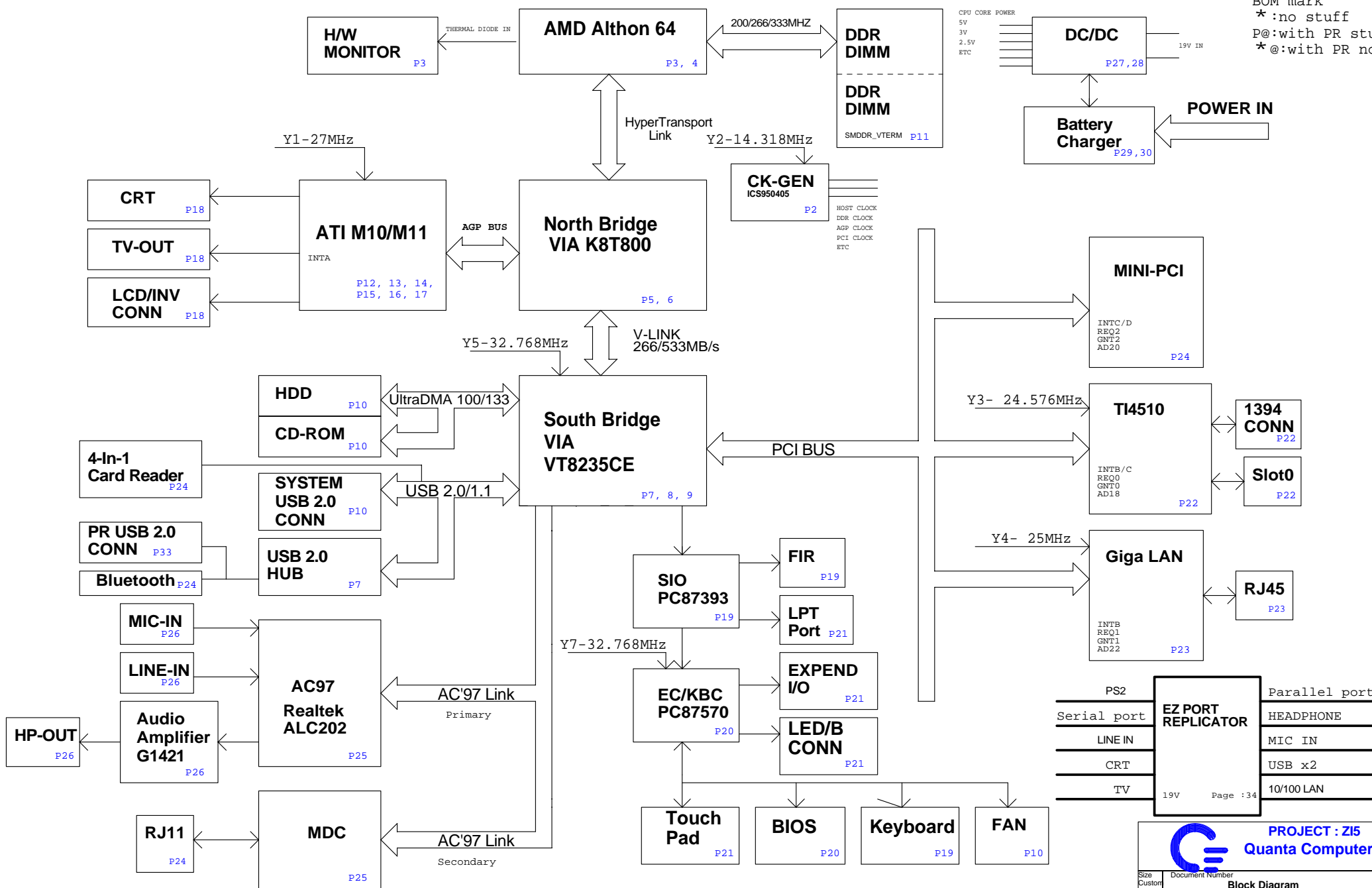
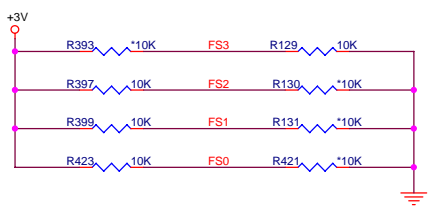
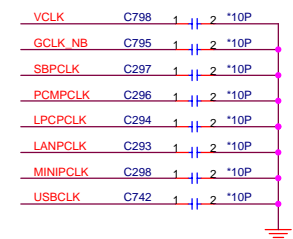
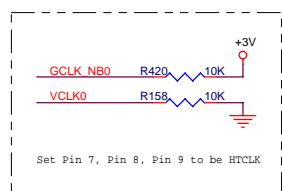
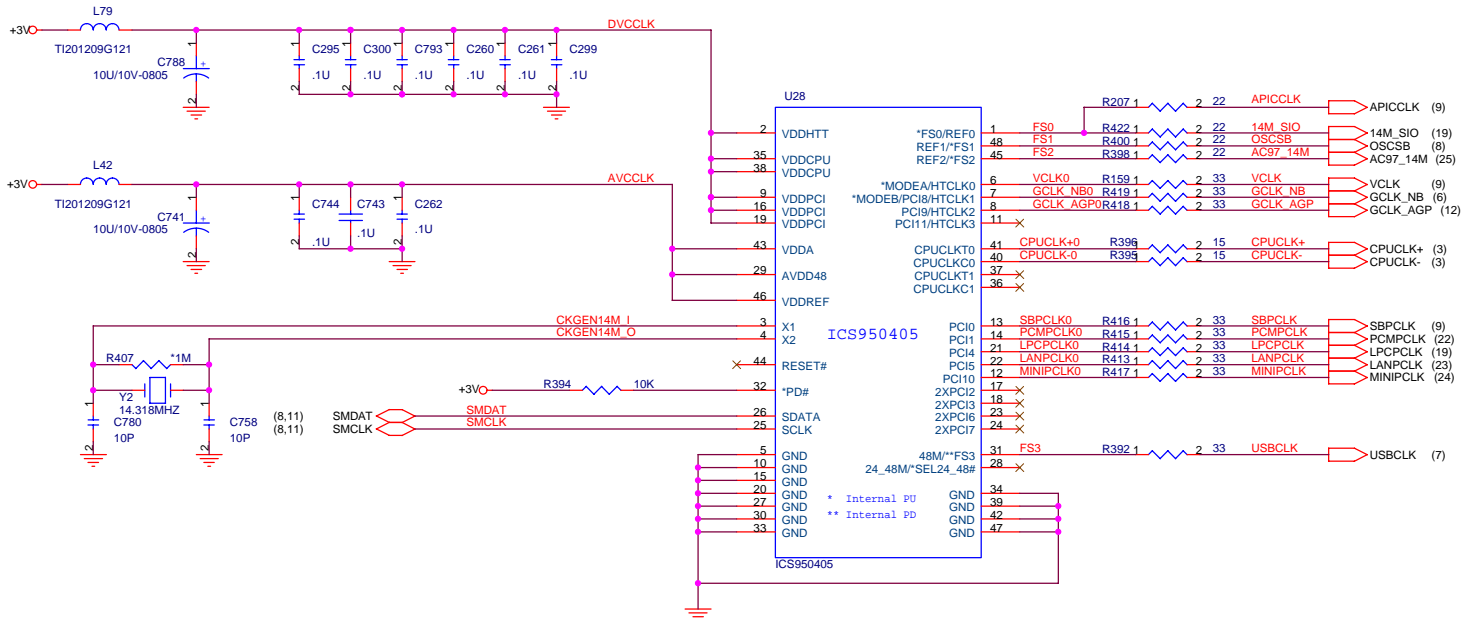


ZI5 SYSTEM BLOCK DIAGRAM

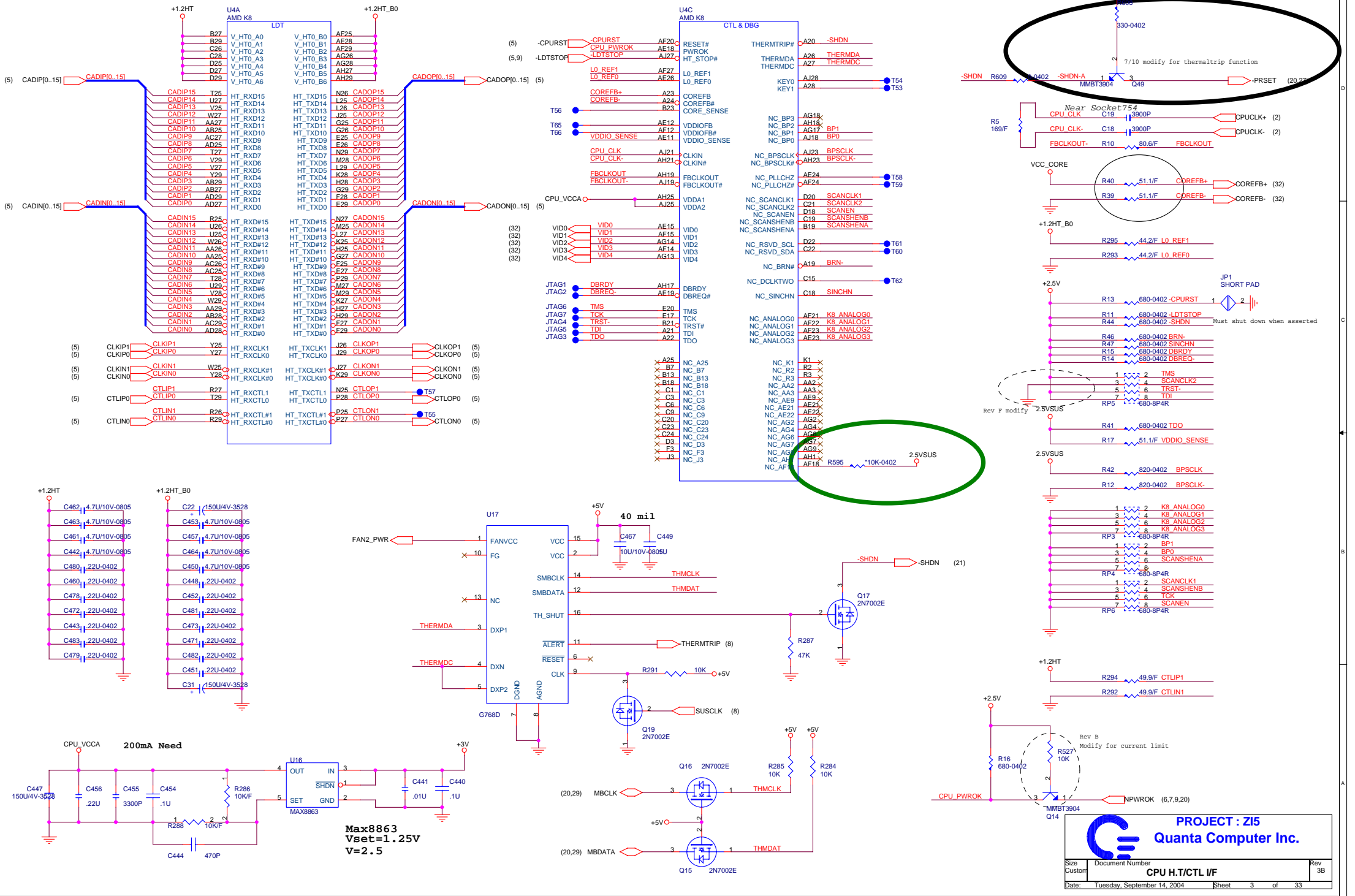
BOM mark
 * :no stuff
 P@:with PR stuff
 *@:with PR no stuff





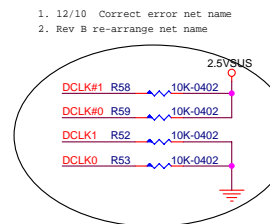
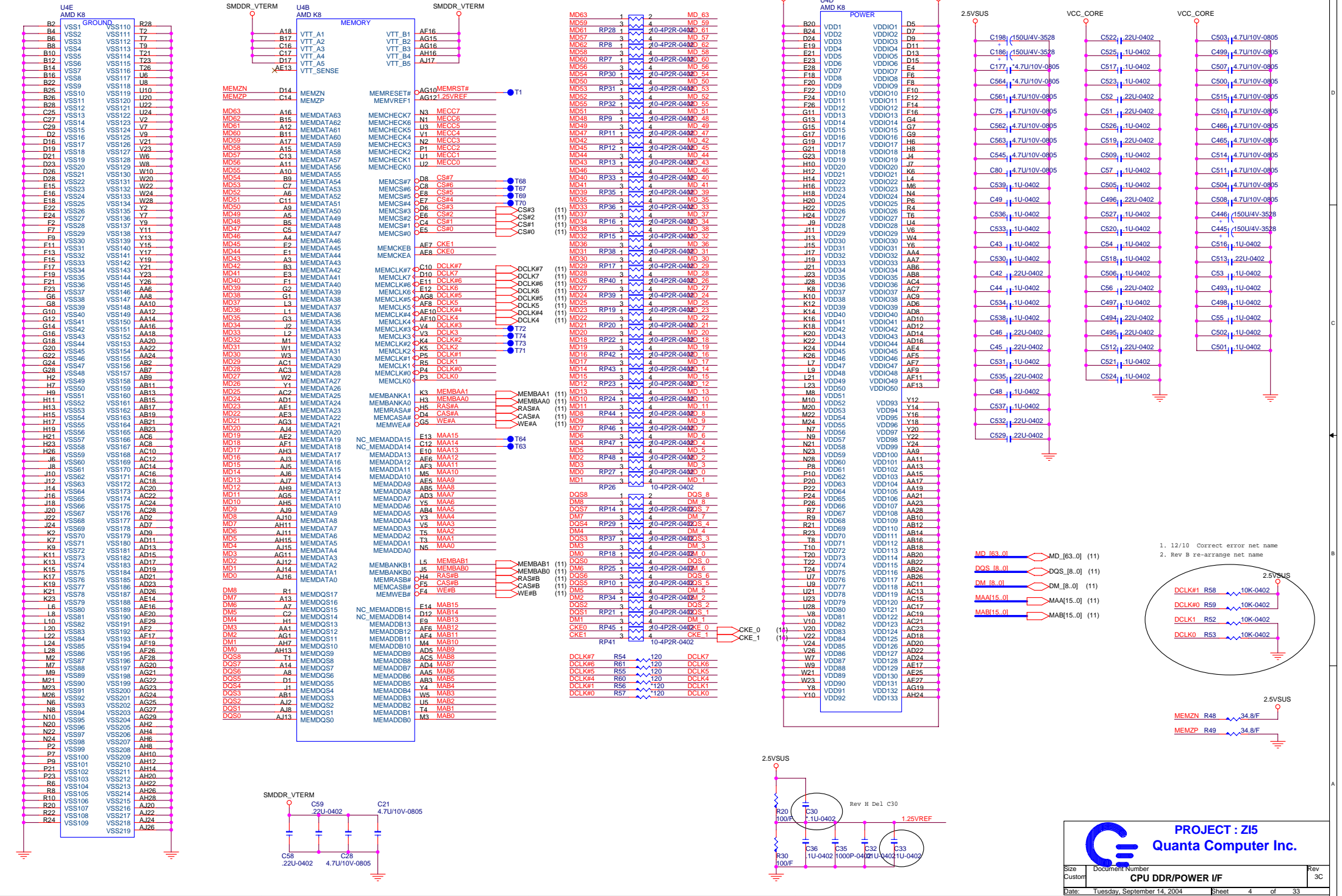
FS3	FS2	FS1	FS0	CPUCLK MHZ	HTT MHZ	PCICLK MHZ
0	0	0	0	100.90	67.27	33.63
1	1	1	1	133.90	66.95	33.48
0	0	0	1	168.00	67.20	33.60
0	0	1	0	202.00	67.33	33.67
1	0	0	0	100.20	66.80	33.40
0	1	1	1	133.50	66.75	33.38
1	1	1	0	166.70	66.68	33.34
0	0	0	0	200.40	66.80	33.40
1	0	0	0	150.00	66.00	33.00
0	1	0	0	210.00	70.00	35.00
0	0	0	0	240.00	60.00	33.00
1	1	1	1	270.00	67.75	33.75
1	1	1	0	233.33	66.67	33.33
1	1	1	1	300.00	75.00	37.50

CPU H.T/CTL I/F



		PROJECT : Z15 Quanta Computer Inc.	
		Size: Document Number Custom: CPU H.T/CTL I/F Date: Tuesday, September 14, 2004 Sheet 3 of 33	

CPU DDR/POWER I/F



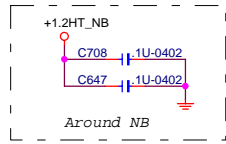
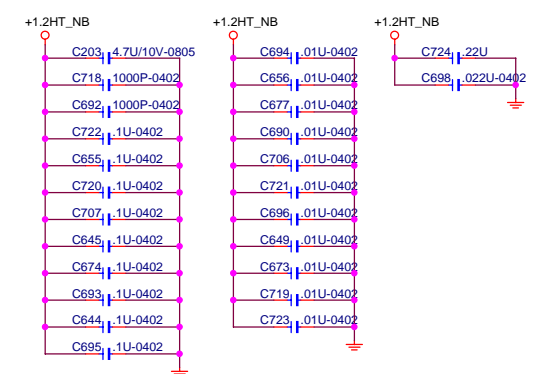
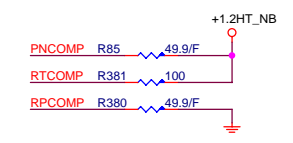
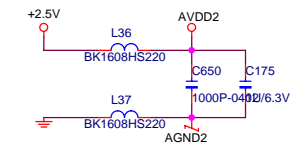
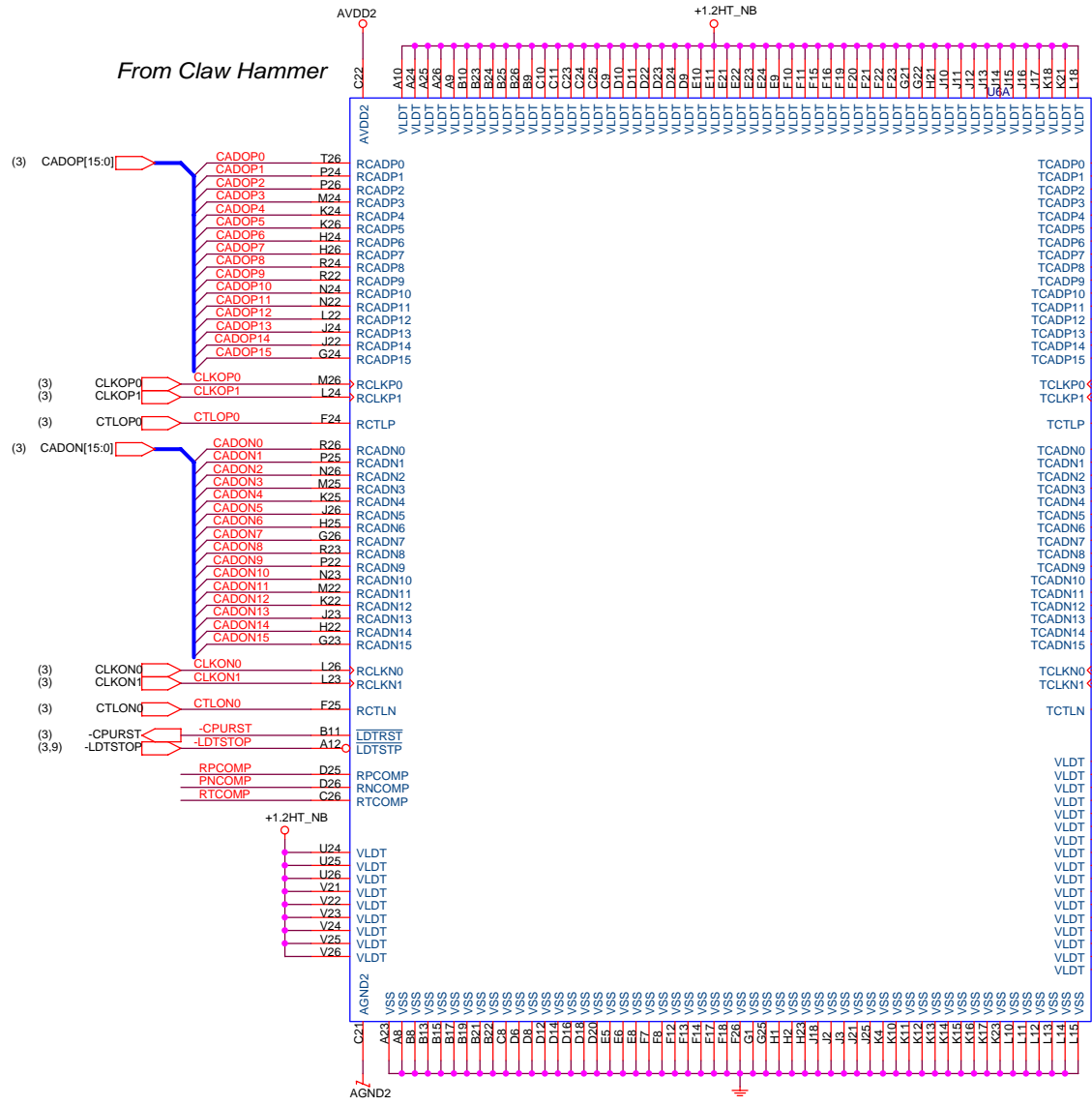
PROJECT : Z15
Quanta Computer Inc.

Size: Custom Document Number: **CPU DDR/POWER I/F** Rev: 3C

Date: Tuesday, September 14, 2004 Sheet: 4 of 33

From Claw Hammer

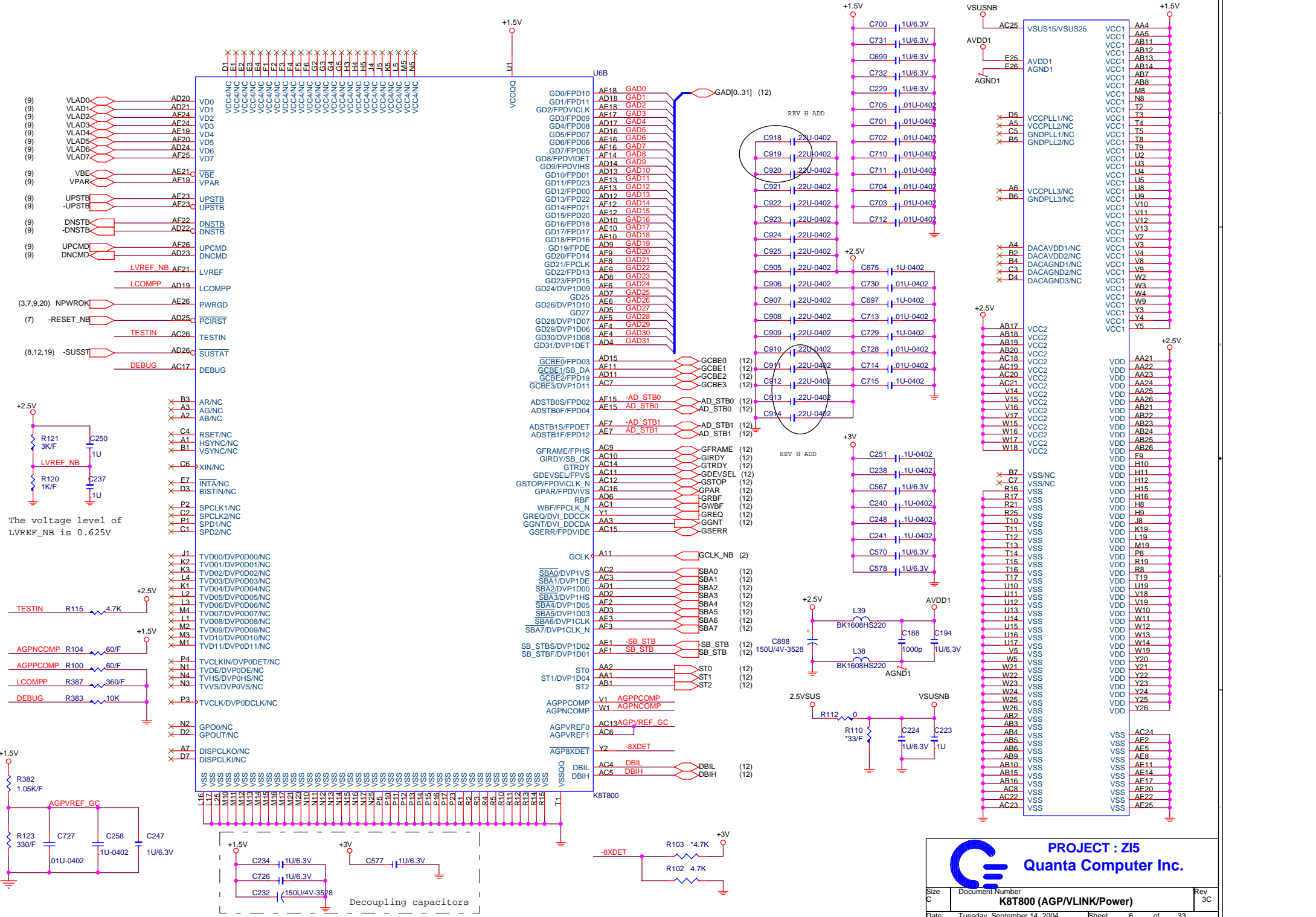
To Claw Hammer



K8T800

PROJECT : Z15
Quanta Computer Inc.

Size C	Document Number K8T800 (HOST)	Rev 1A
Date:	Tuesday, September 14, 2004	Sheet 5 of 33



PROJECT : Z15
Quanta Computer Inc.

(22,23,24) AD[0..31] ADI0_311

- AD0 G2
- AD1 J4
- AD2 J3
- AD3 H3
- AD4 F1
- AD5 G1
- AD6 H4
- AD7 F2
- AD8 E1
- AD9 G3
- AD10 E3
- AD11 D1
- AD12 G4
- AD13 D2
- AD14 D3
- AD15 F3
- AD16 M4
- AD17 L3
- AD18 K2
- AD19 K1
- AD20 M4
- AD21 L2
- AD22 N4
- AD23 L1
- AD24 M2
- AD25 M4
- AD26 P4
- AD27 N3
- AD28 N2
- AD29 N1
- AD30 P1
- AD31 P2

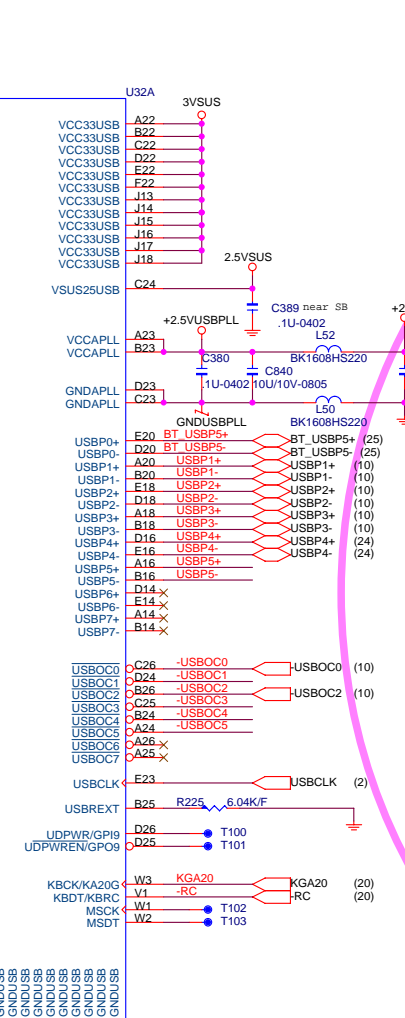
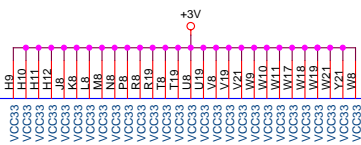
- (22,23,24) -CBE0 E2
- (22,23,24) -CBE1 C1
- (22,23,24) -CBE2 L4
- (22,23,24) -CBE3 M3

- (22,23,24) -FRAME J1
- (22,23,24) -DEVSEL H2
- (22,23,24) -IRDY J2
- (22,23,24) -TRDY H4
- (22,23,24) -STOP K4
- (22,23,24) -SERR C2
- (22,23,24) PAR F4
- (22,23,24) -PERR R3
- (22,23,24) -PCIRST R1

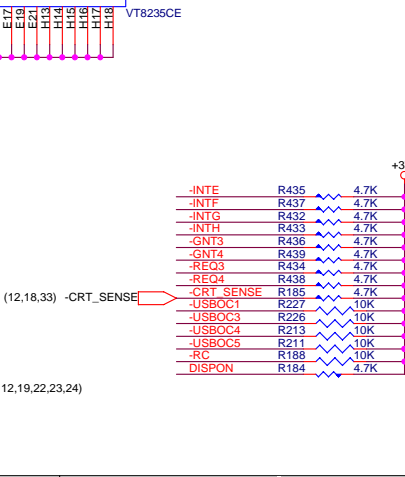
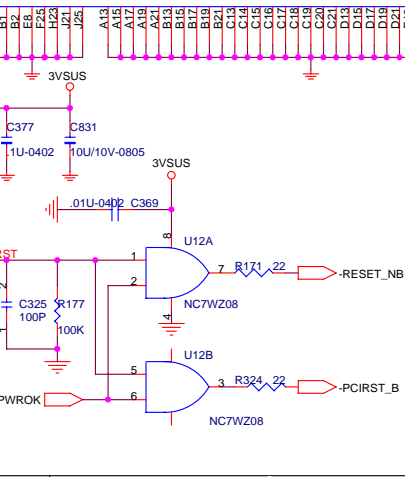
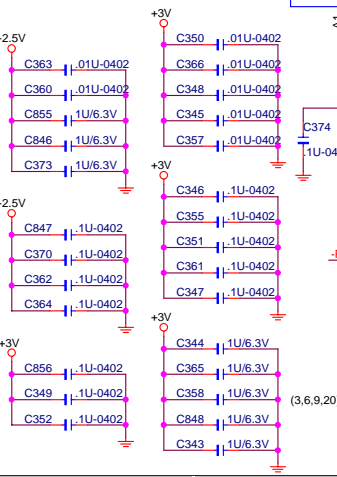
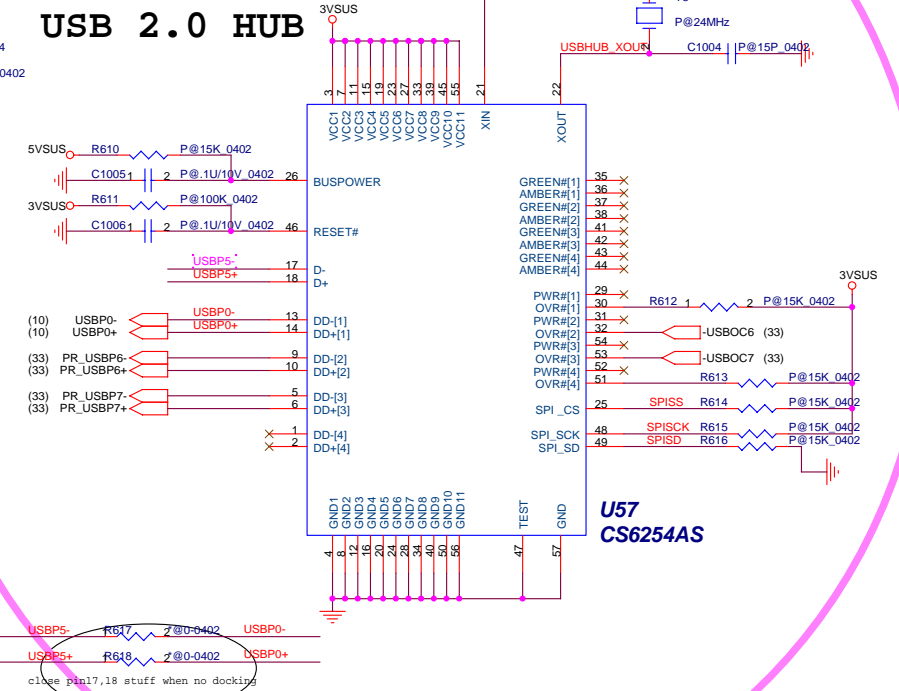
- (12) -INTA A4
- (22,23) -INTB B4
- (22,24) -INTC C4
- (24) -INTD D4
- INTE E4
- INTF F4
- INTG G4
- INTH H4

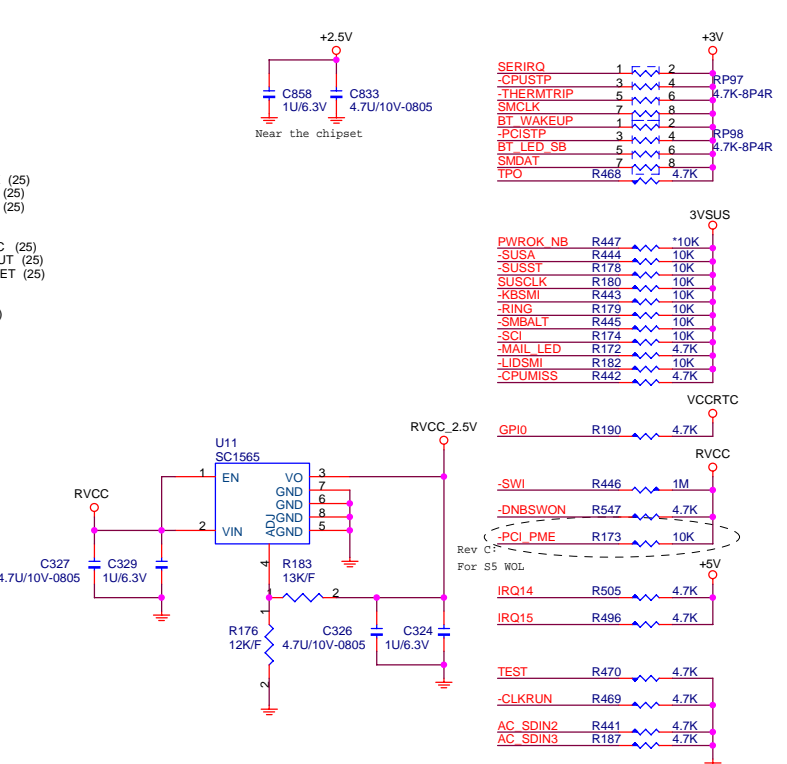
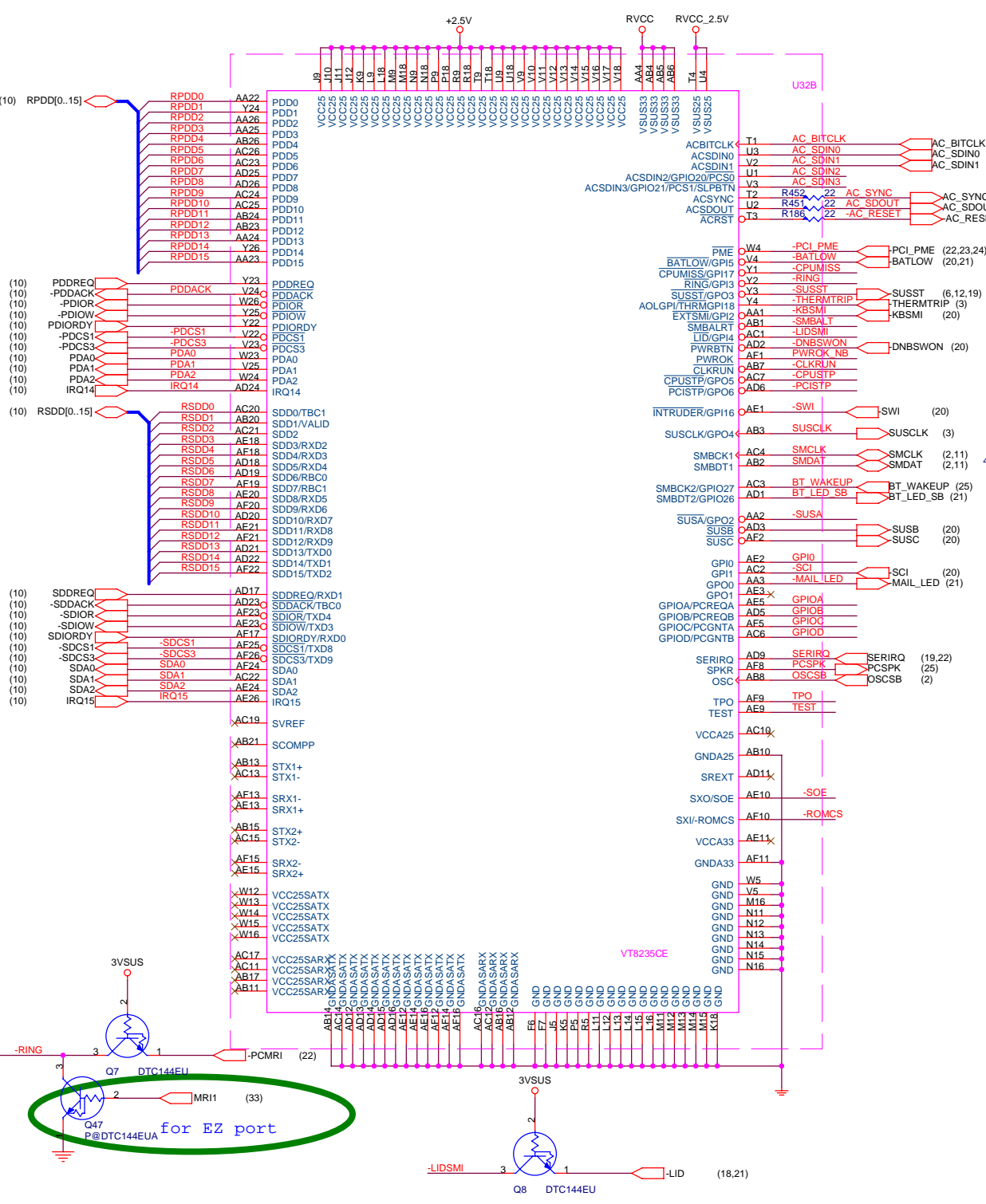
- (22) -REQ0 A5
- (23) -REQ1 B6
- (24) -REQ2 C5
- REQ3 D5
- REQ4 P3
- CRT SENSE R3

- (22) -GNT0 A6
- (23) -GNT1 D6
- (24) -GNT2 E5
- GNT3 E5
- GNT4 R4
- (18) DISPON R2



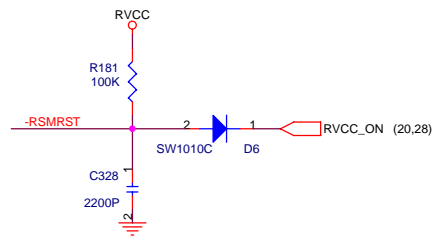
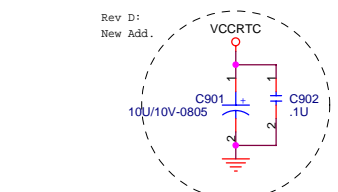
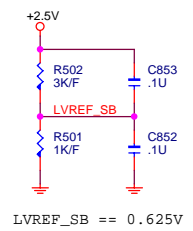
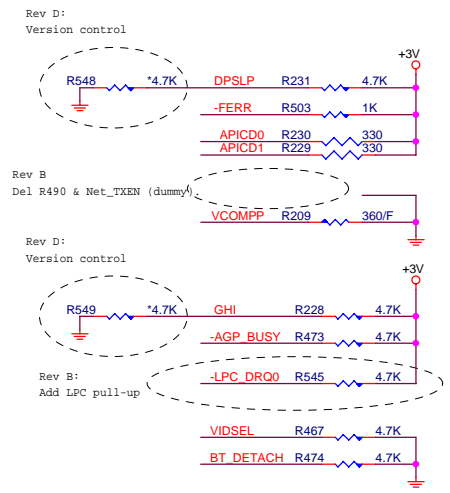
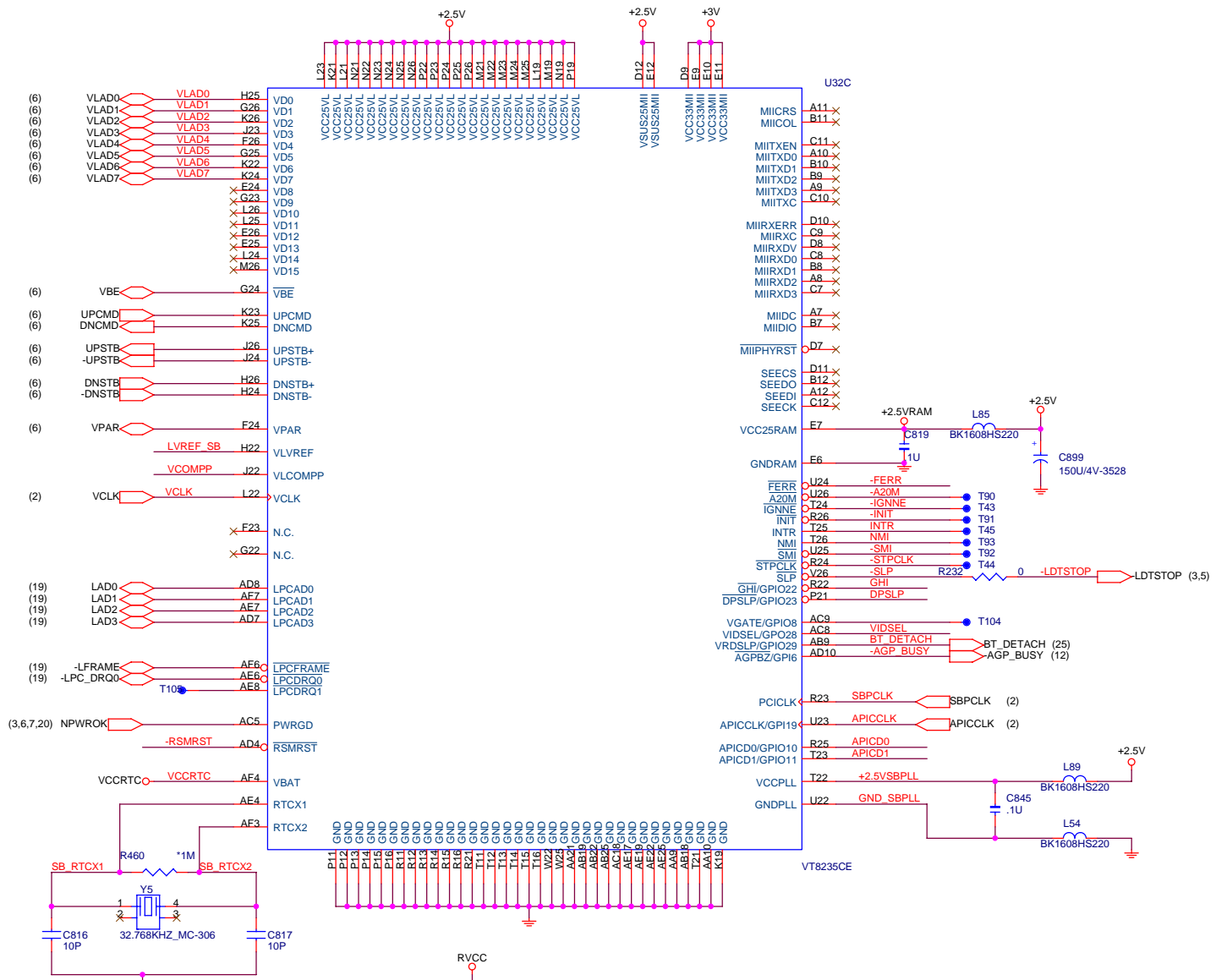
USB 2.0 HUB





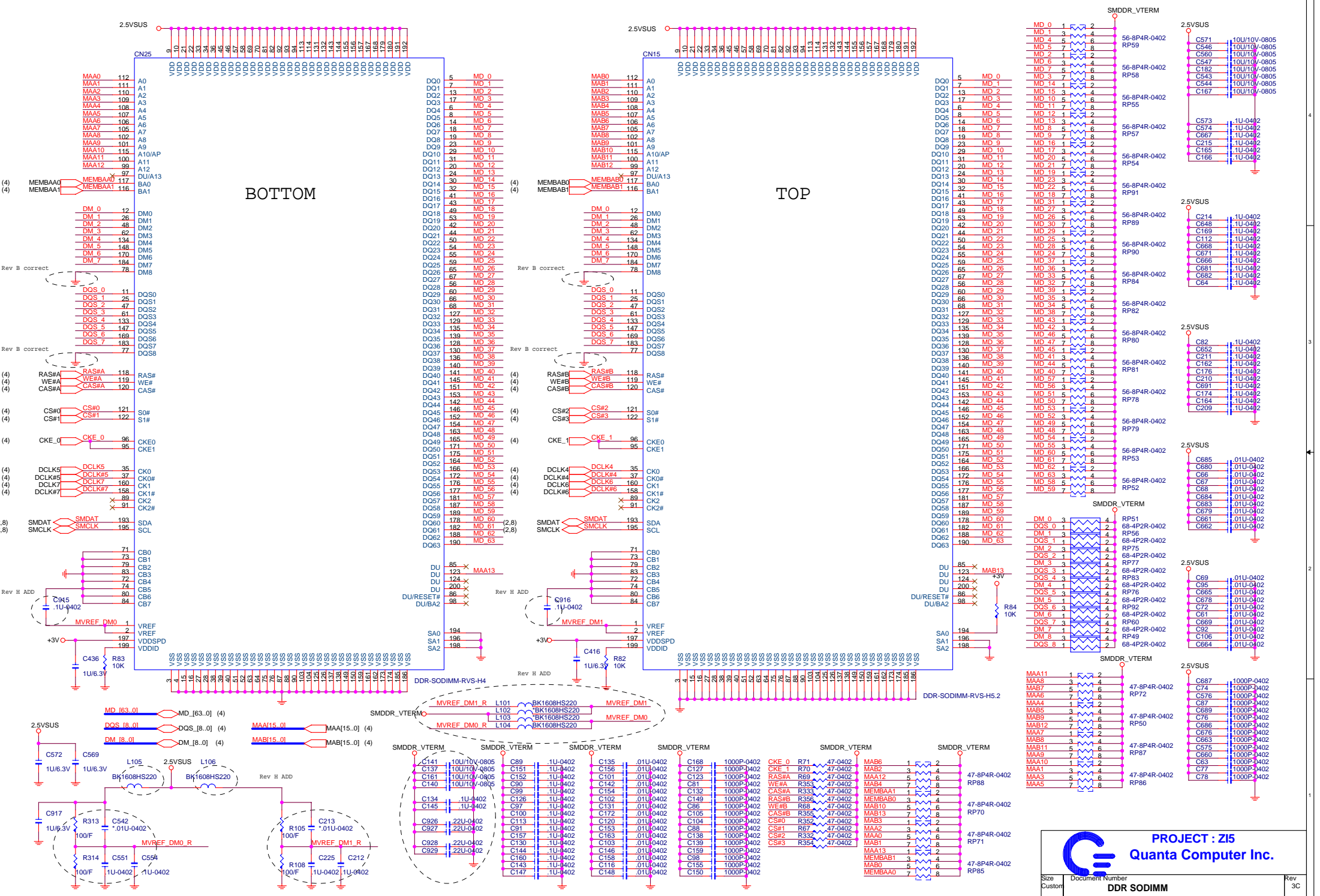
Power Up Strappings :

- GPIO[A,C] => LDT Frequency (VD[1:0])**
 - 00 - 200Mhz (Default)
 - 01 - 400Mhz
 - 10 - 600Mhz
 - 11 - 800Mhz
- GPIOB => LDT Width (VD[2])**
 - 0 - 8-Bit (Default)
 - 1 - 16-Bit
- GPIOD => Transmit PLL Skew Control 1 (VD[3])**
- SDA0 => Transmit PLL Skew Control 2 (VD[4])**
- SDA1 => External loop test mode (VD[5])**
 - 0 - Disable (Default)
 - 1 - Enable
- SDA2 => ROMSIP Select (VD[6])**
 - 0 - Disable
 - 1 - Enable
- SDCS3 => Test Mode Select (VD[7])**
 - 0 - Disable (Default)
 - 1 - Enable
- SDCS1 => Internal EEPROM Strapping**
 - 0 - BIOS porting - ACR
 - 1 - External EEPROM (On board)/(Default)
- ROMCS => LPC ROM Select**
 - 0 - Disable LPC ROM
 - 1 - Enable LPC ROM (Default)
- PCSPK => CPU Frequency Strapping**
 - 0 - Enable
 - 1 - Disable
- SOE => Auto Reboot**
 - 0 - Enable
 - 1 - Disable



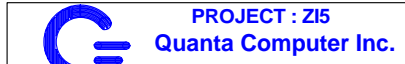
PROJECT : Z15
Quanta Computer Inc.

Size C	Document Number VT8235CE (LPC/LAN/VLINK)	Rev 3B
Date: Tuesday, September 14, 2004 Sheet 9 of 33		



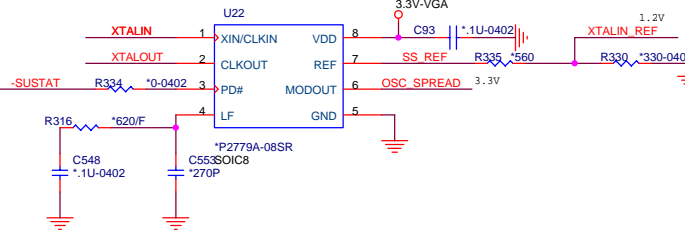
BOTTOM

TOP

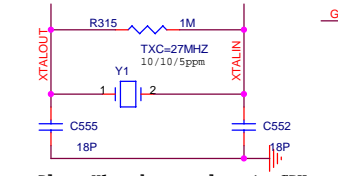


PROJECT : Z15
Quanta Computer Inc.

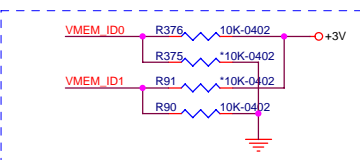
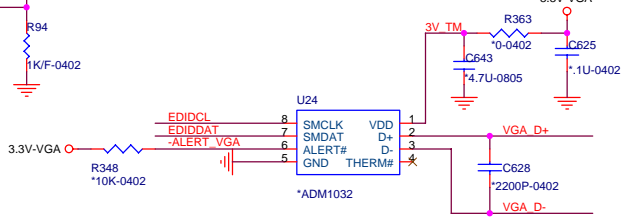
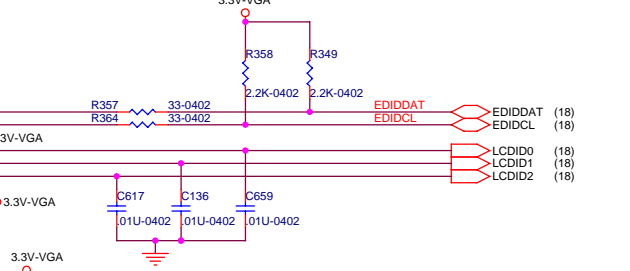
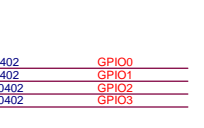
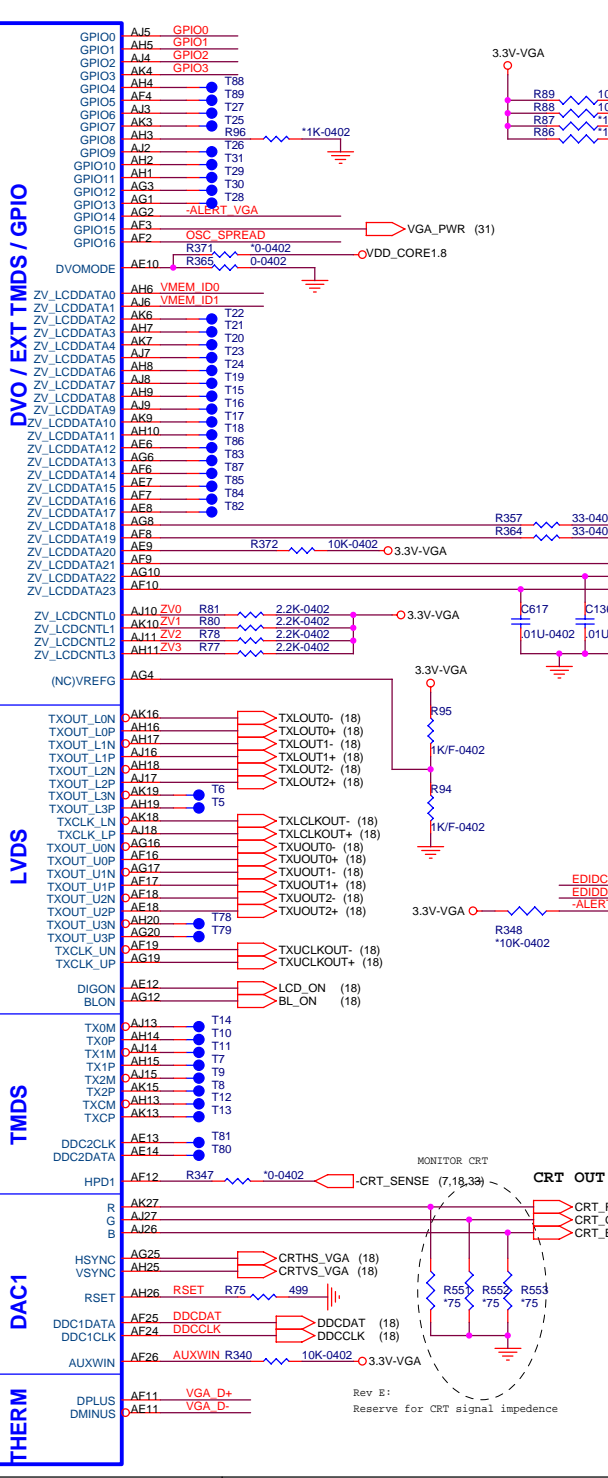
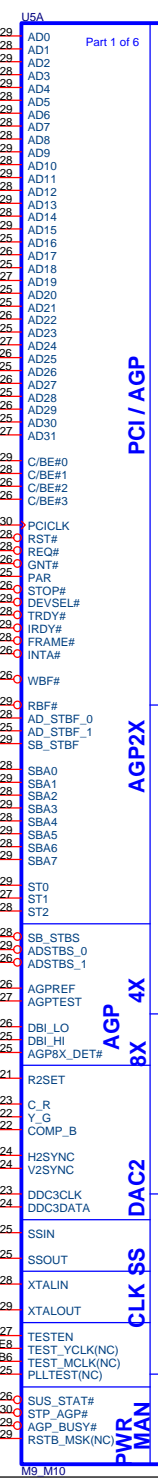
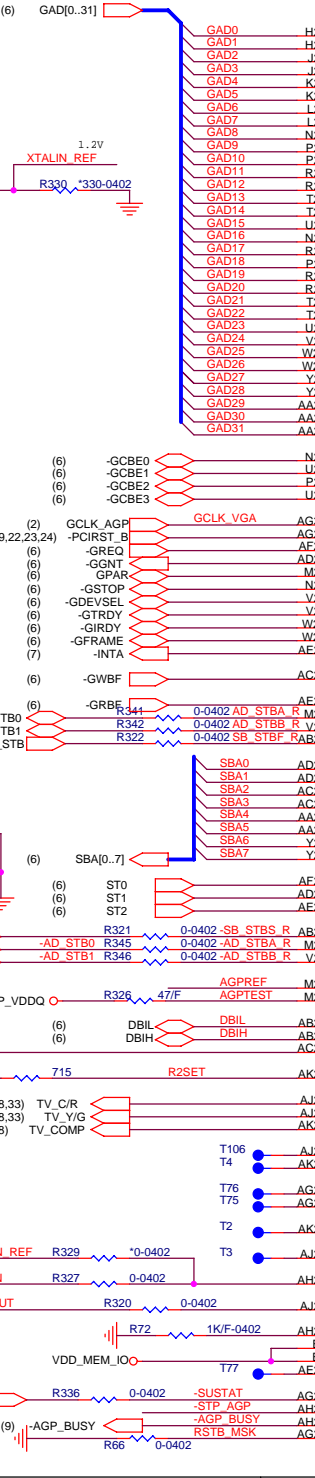
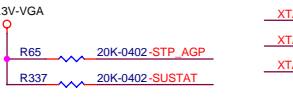
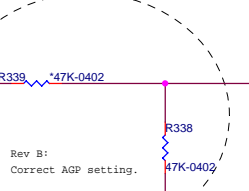
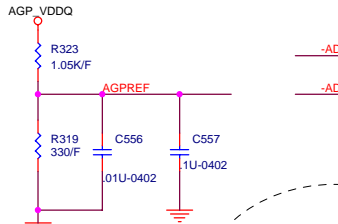
CLK SS



XTAL 27M

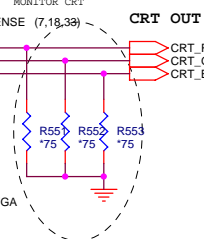


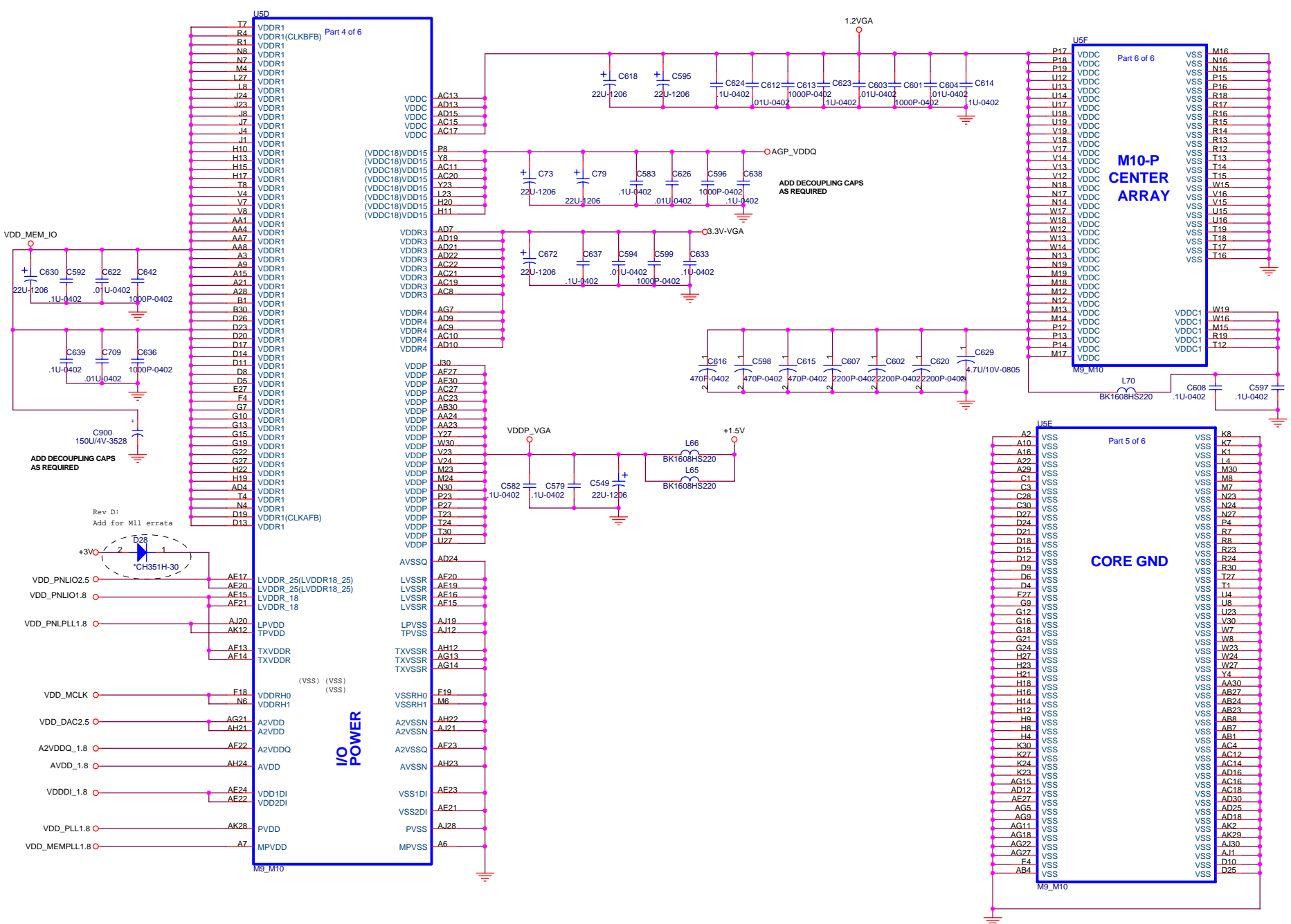
Place Y1 and caps close to GPU




Hynix 128MB	
ID1	0
ID0	1

VRAM configuration



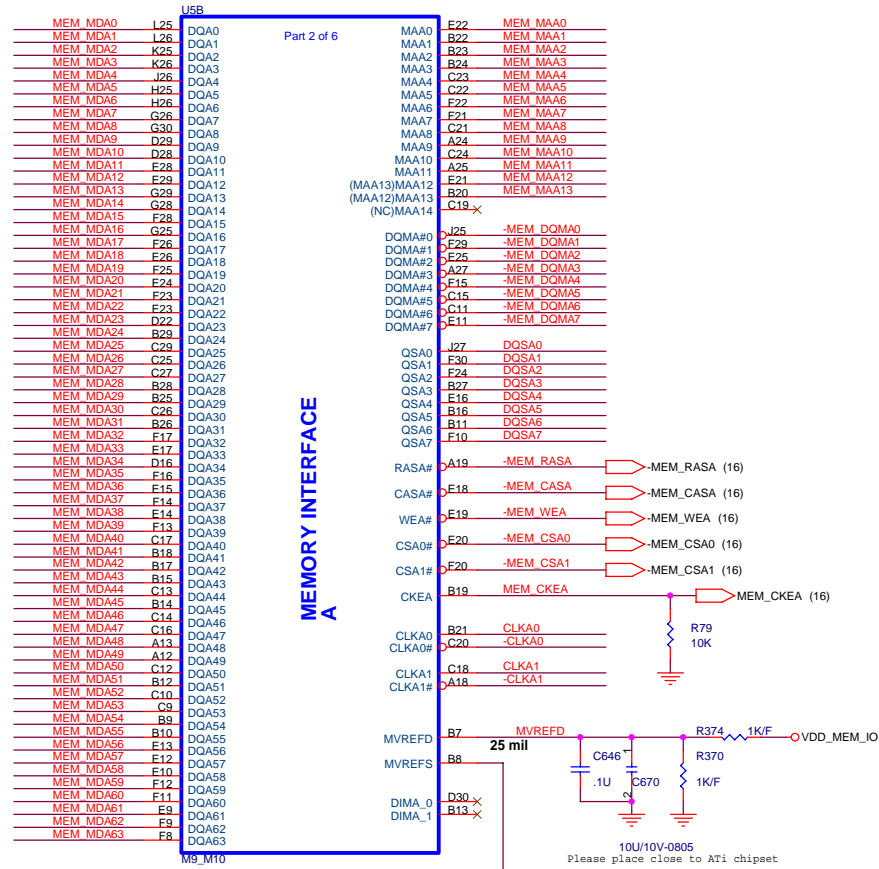




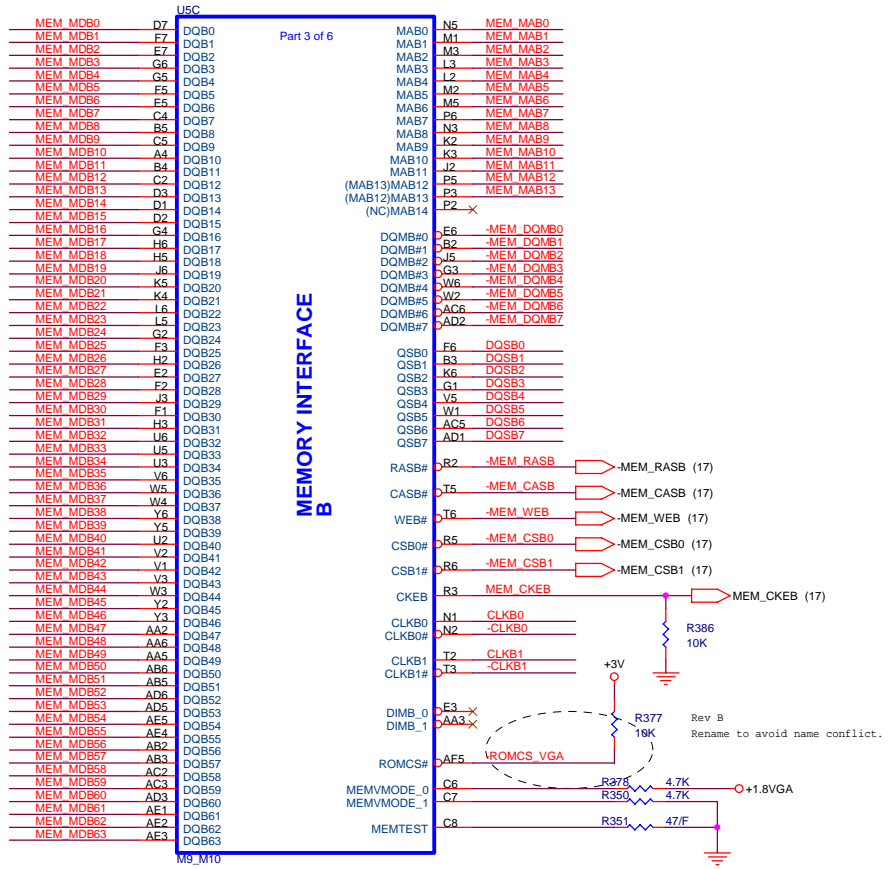
PROJECT : Z15
Quanta Computer Inc.

Size Custom	Document Number AGP-M10_POWER&GND	Rev 1A
Date: Tuesday, September 14, 2004 Sheet 13 of 33		

MEMORY CHANNEL A

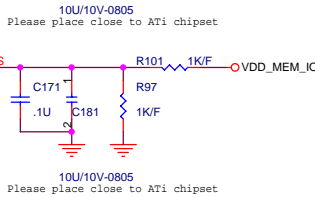
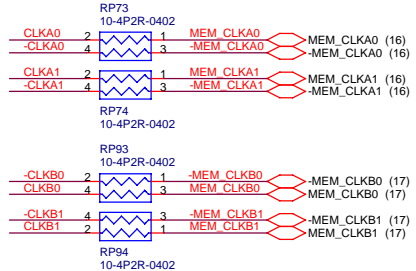
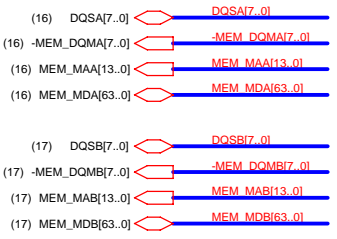


MEMORY CHANNEL B



MEMORY INTERFACE A

MEMORY INTERFACE B

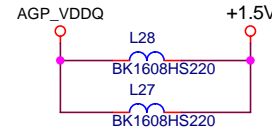
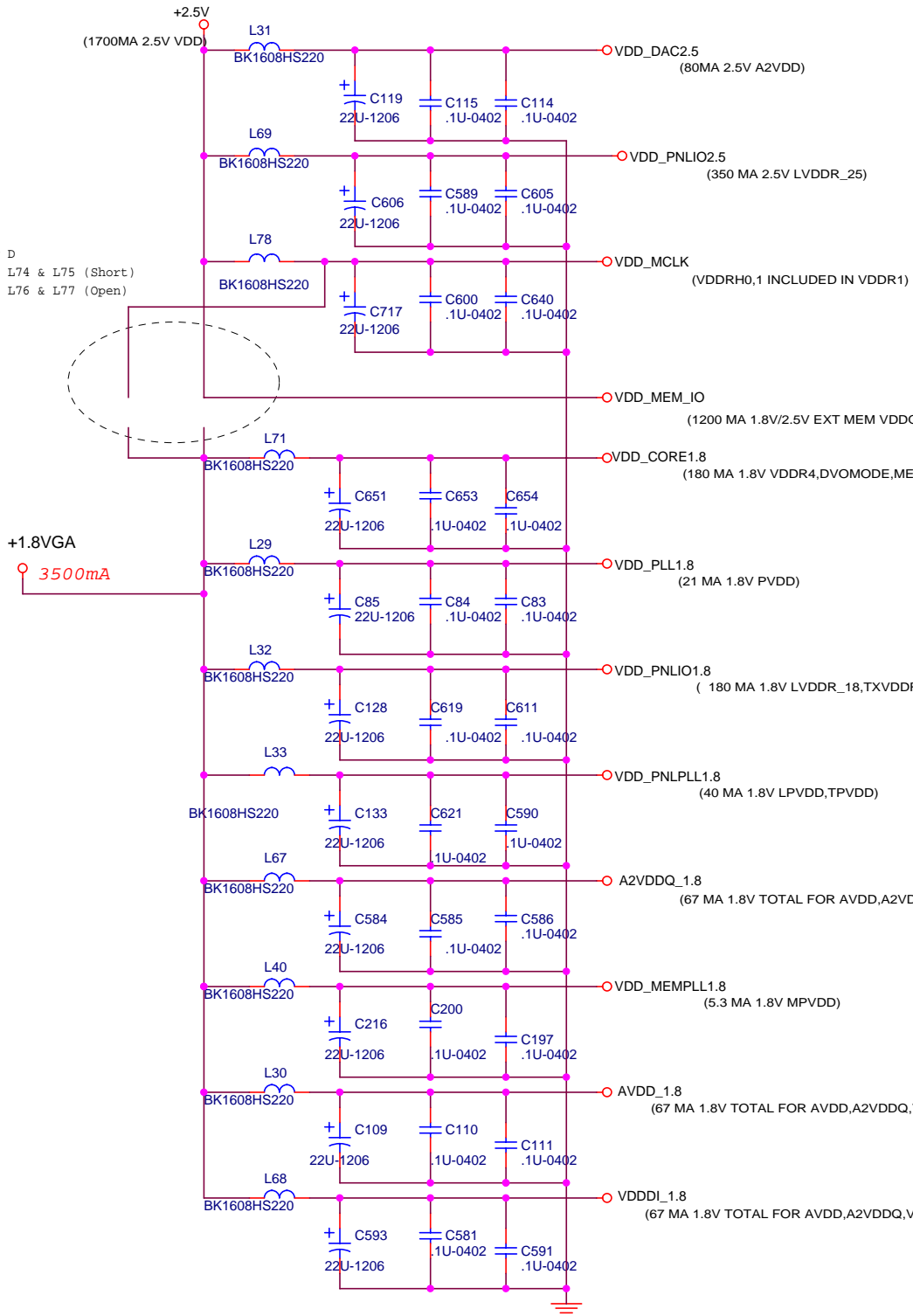


MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V (DDR)
1 0	1.8V (DDR)
1 1	3.3V (SDR)

PROJECT : Z15
Quanta Computer Inc.

Size Custom	Document Number AGP-M10_VRAM I/F	Rev 1A
Date:	Tuesday, September 14, 2004	Sheet 14 of 33

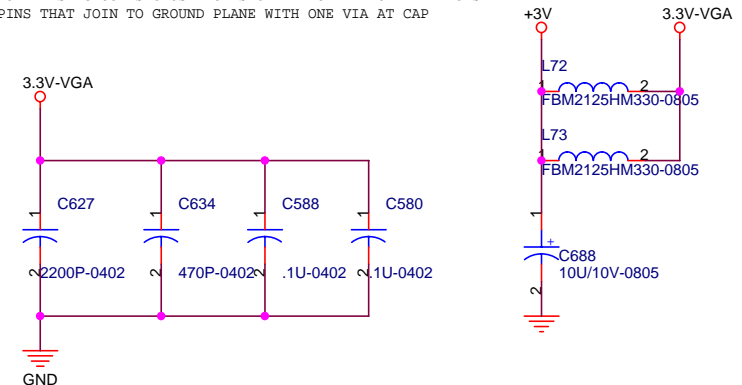
Rev D
 Del L74 & L75 (Short)
 Del L76 & L77 (Open)



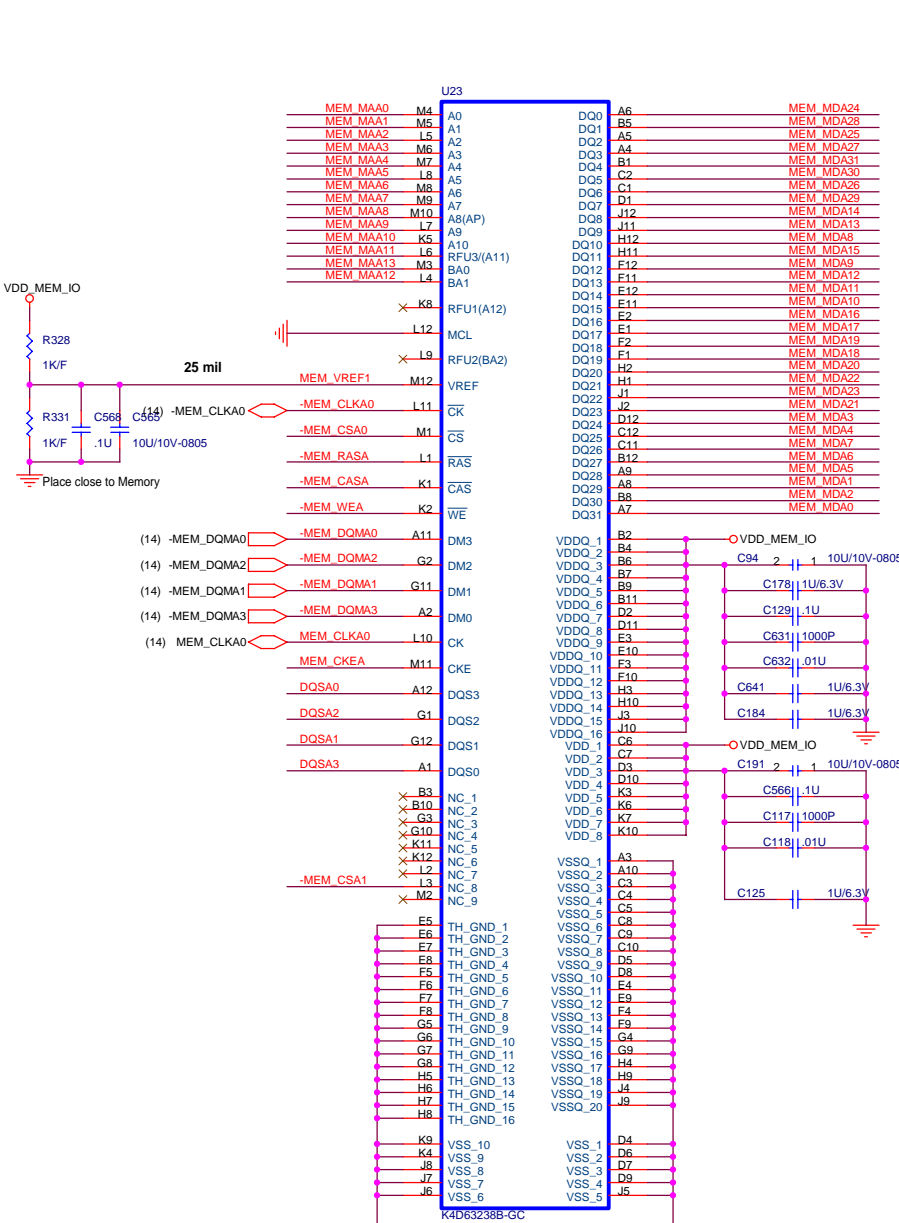
VDDRH, VDDQ AND VDDR1 VOLTAGE SELECTION

VDD_MEM_IO	FBa	FBb	FBc	FBd
1.8V (ELPIDA)	IN	OUT	OUT	IN
2.5V	OUT	IN	IN	OUT

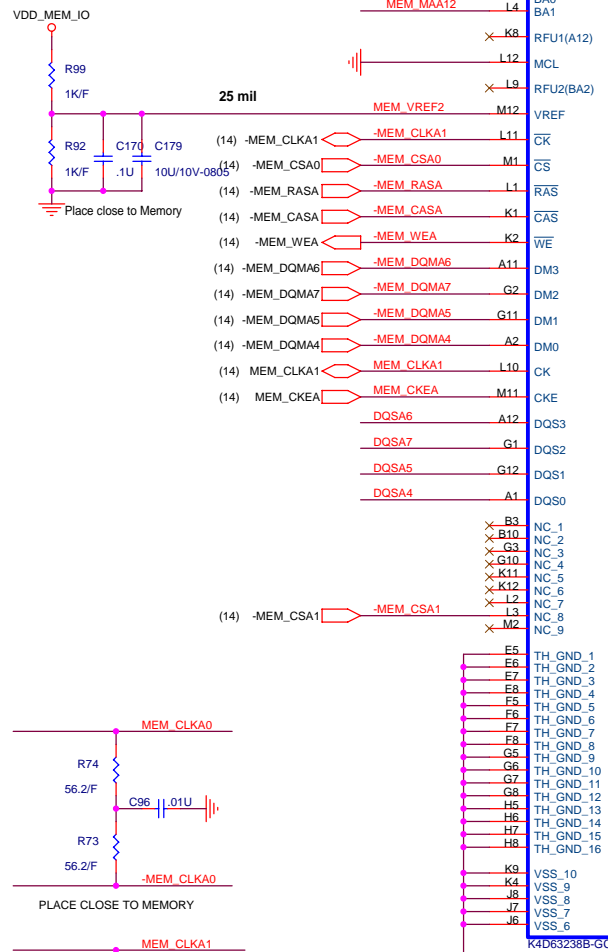
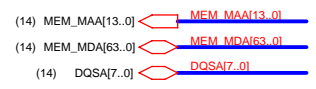
PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS THAT JOIN TO GROUND PLANE WITH ONE VIA AT CAP



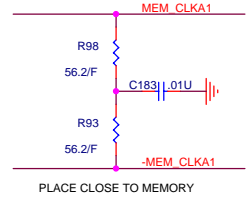
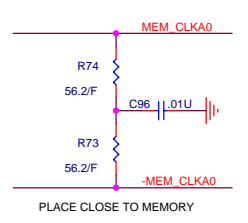
PROJECT : Z15
Quanta Computer Inc.



4MX32 DDR BGA Memory

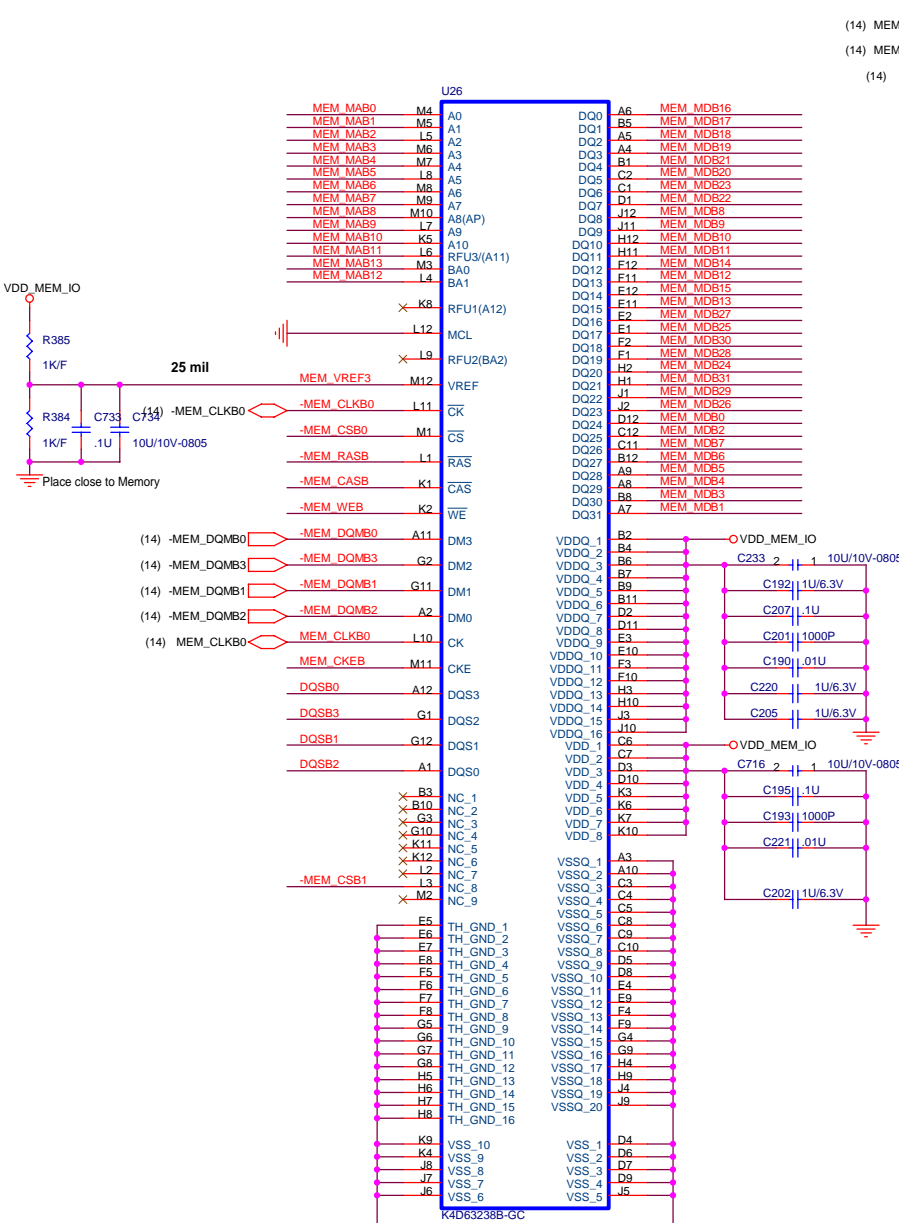


4MX32 DDR BGA Memory



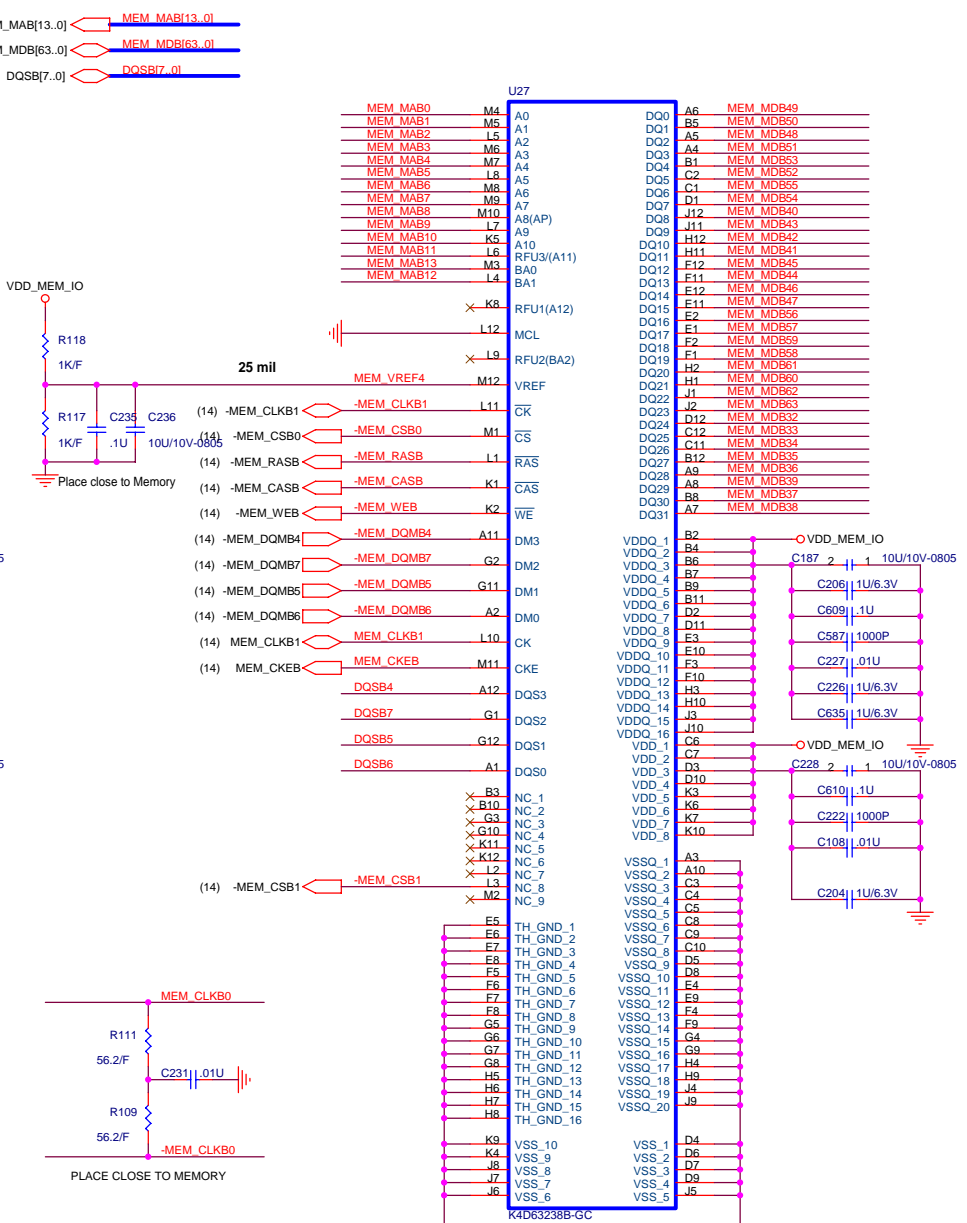
PROJECT : Z15
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
VIDEO DDR MEMORY 1		
Date: Tuesday, September 14, 2004	Sheet 16 of 33	

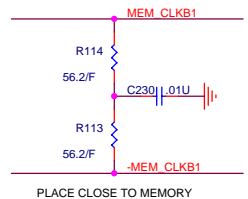
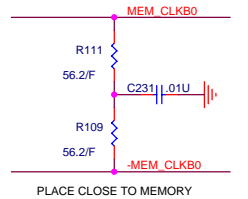


4MX32 DDR BGA Memory

- (14) MEM_MAB[13..0] MEM_MAB13..01
- (14) MEM_MDB[63..0] MEM_MDB63..01
- (14) DQSB[7..0] DQSB7..01



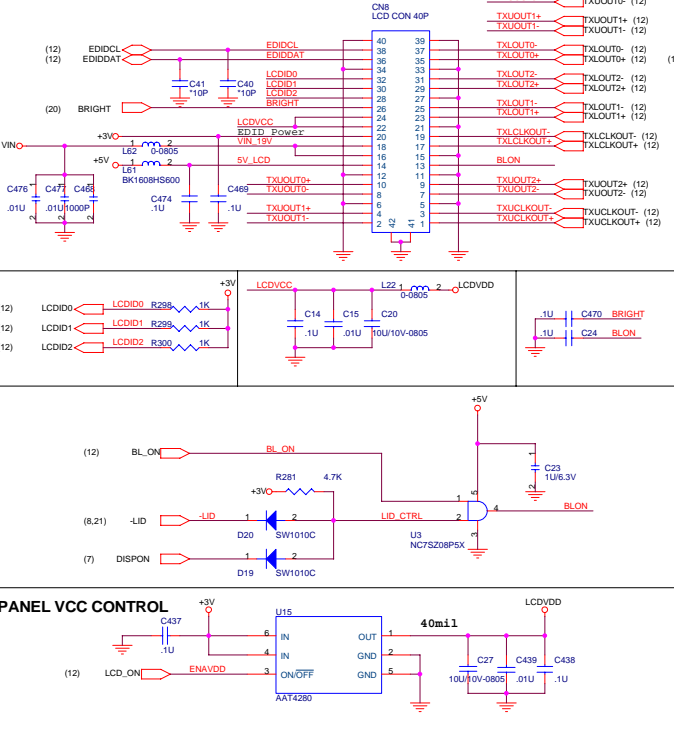
4MX32 DDR BGA Memory



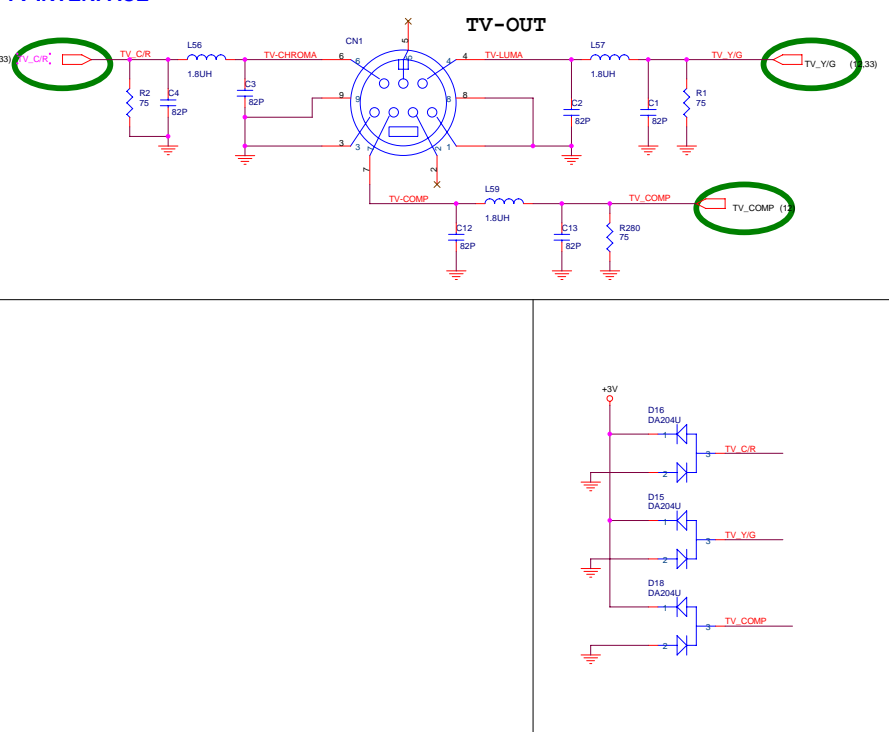
PROJECT : Z15
Quanta Computer Inc.

Size Custom	Document Number VIDEO DDR MEMORY 2	Rev 1A
Date: Tuesday, September 14, 2004		Sheet 17 of 33

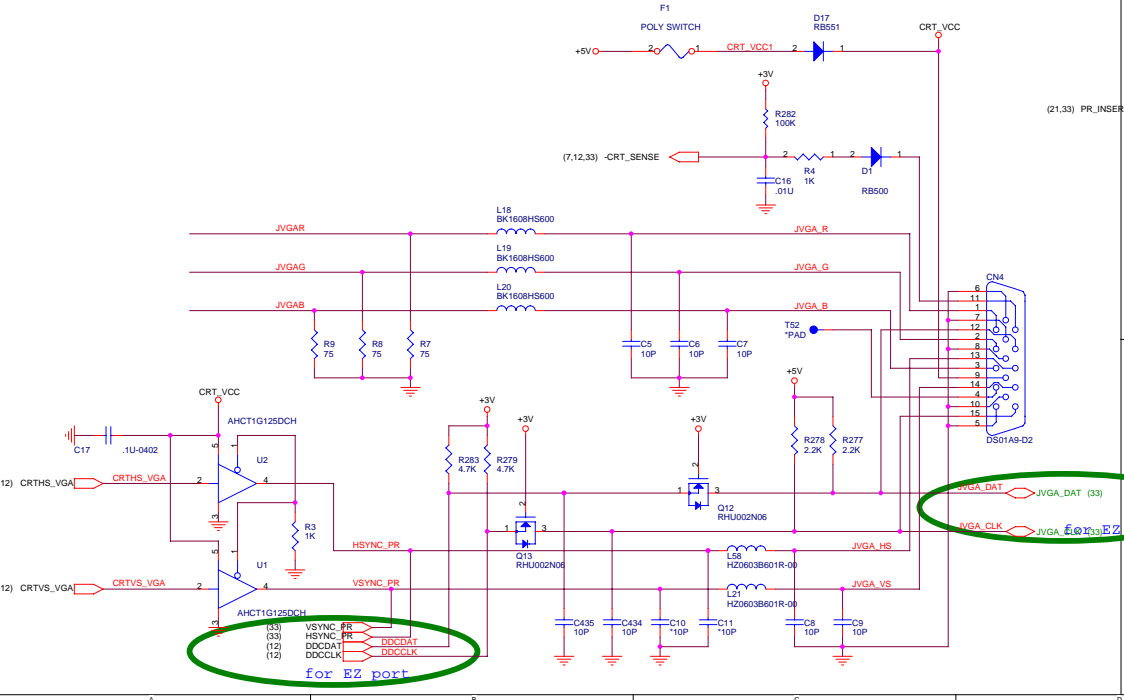
LCD INTERFACE



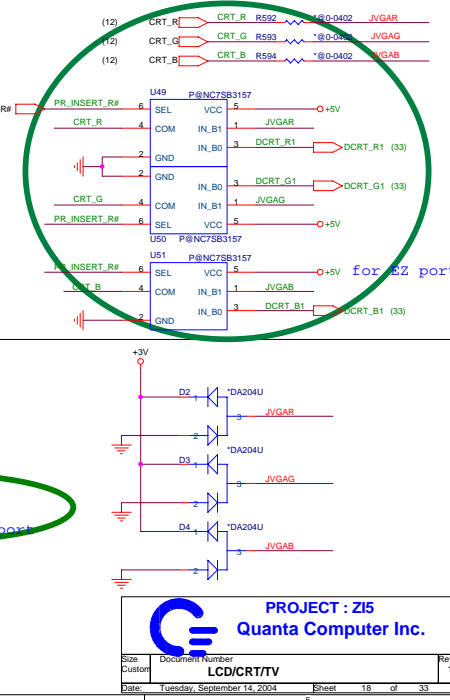
TV INTERFACE

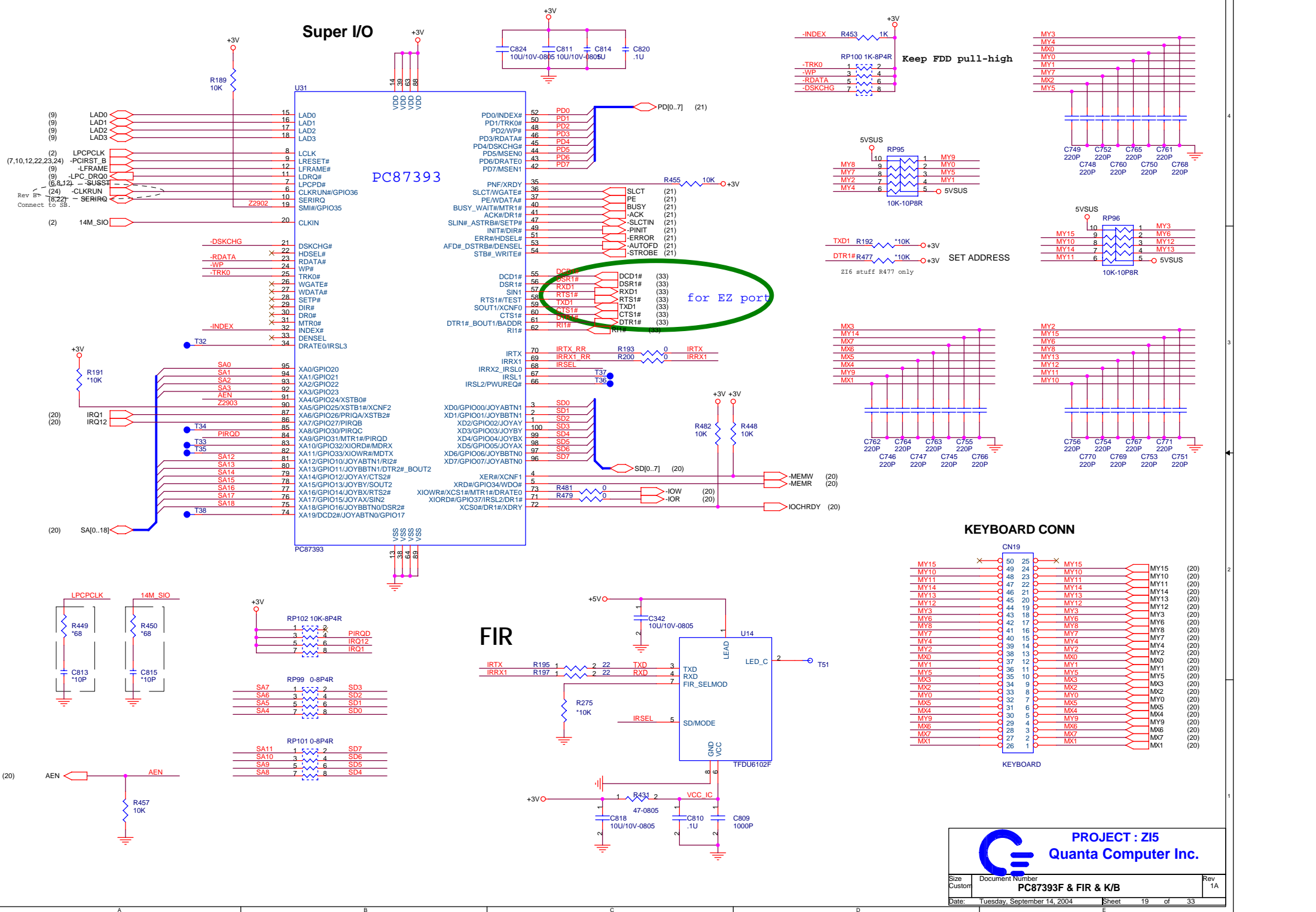


CRT INTERFACE

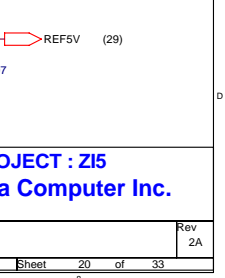
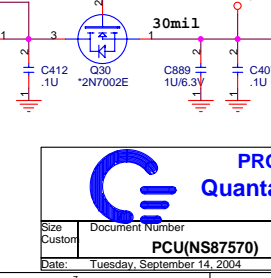
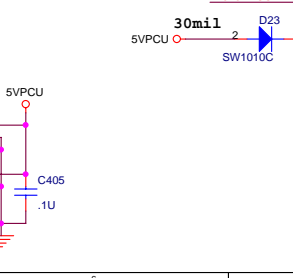
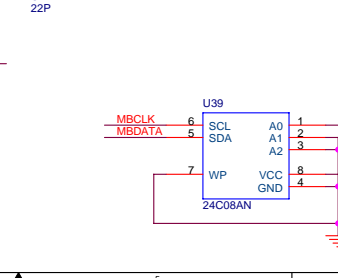
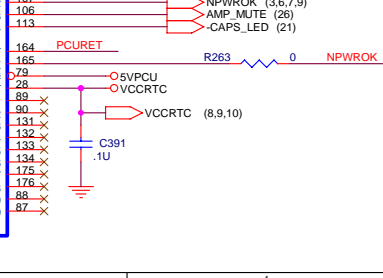
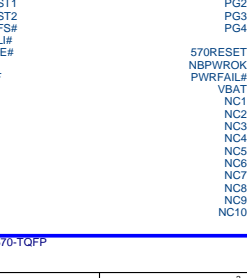
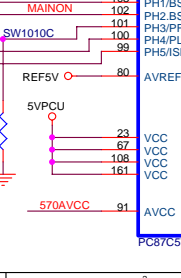
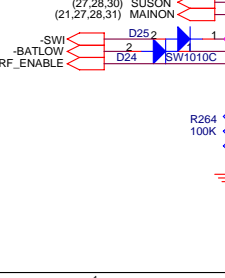
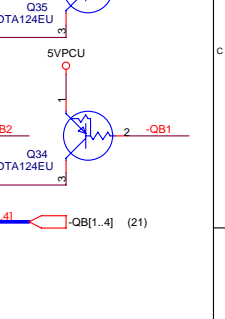
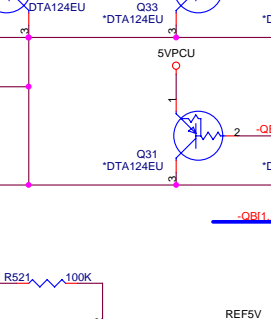
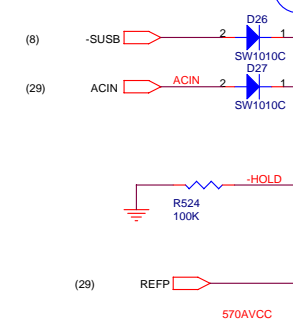
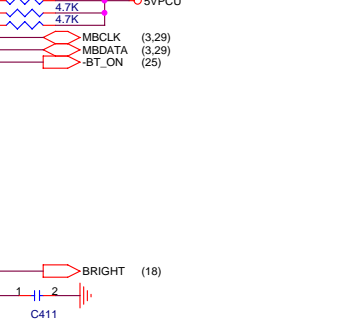
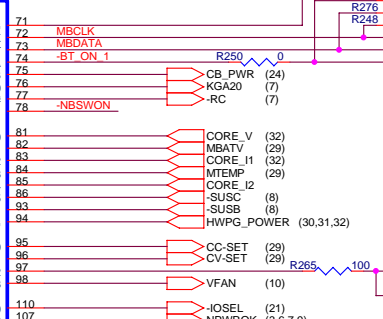
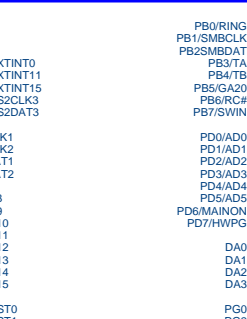
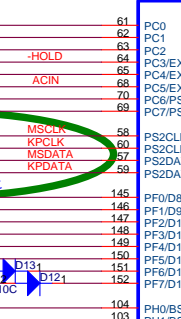
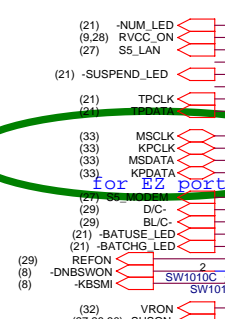
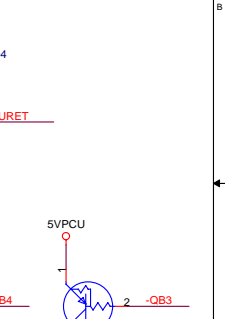
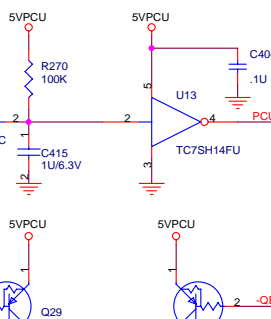
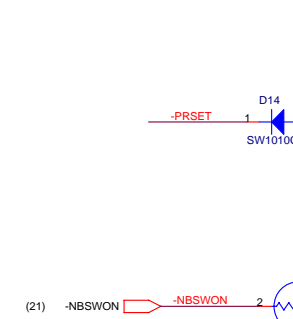
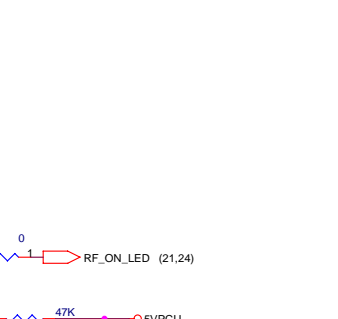
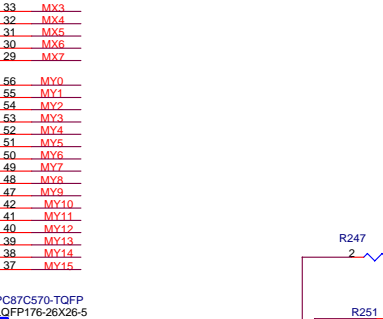
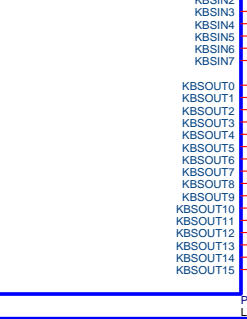
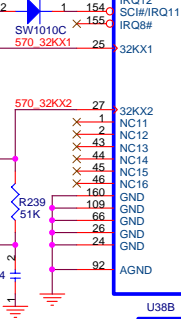
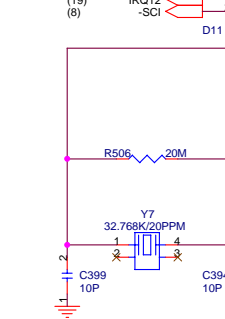
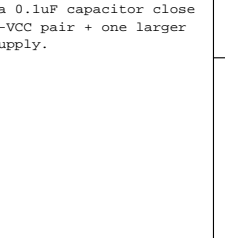
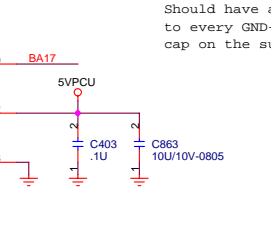
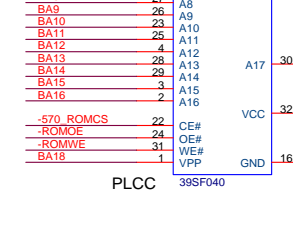
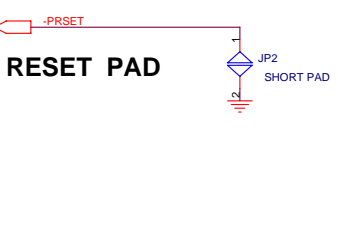
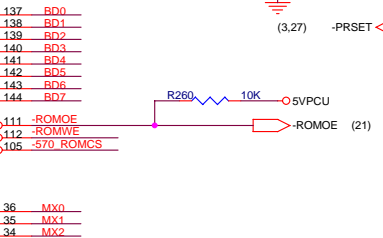
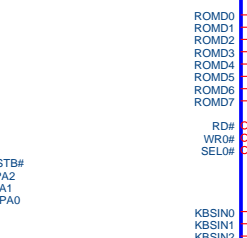
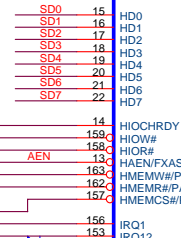
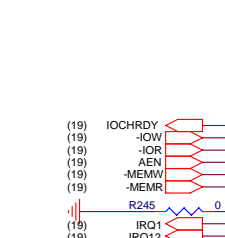
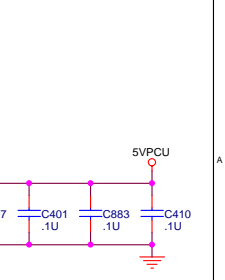
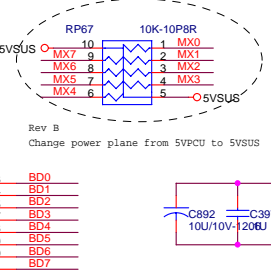
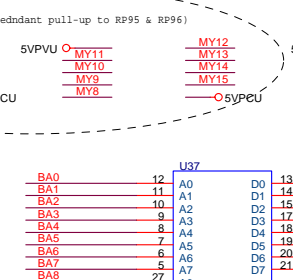
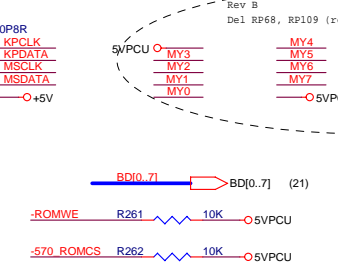
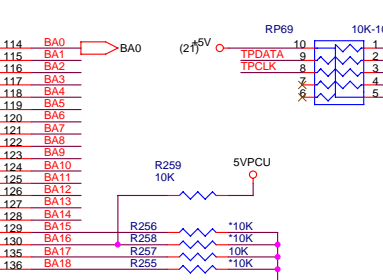
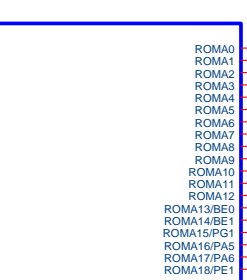
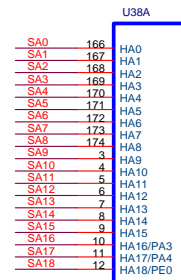


stuff R for ZI5 stuff switch for ZI5-2

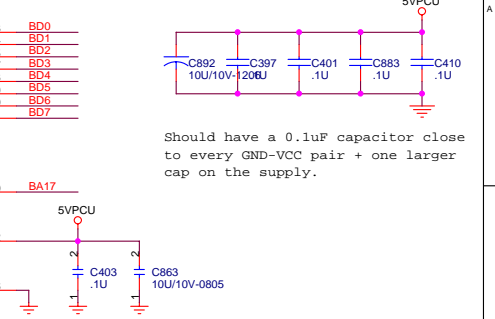
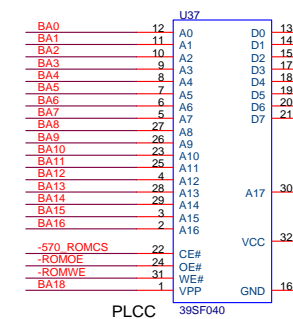




(19) SA10..18] SA10..18]
(19) SD10..7] SD10..7]
(19) MX0..7] MX0..7]
(19) MY0..15] MY0..15]



RESET PAD



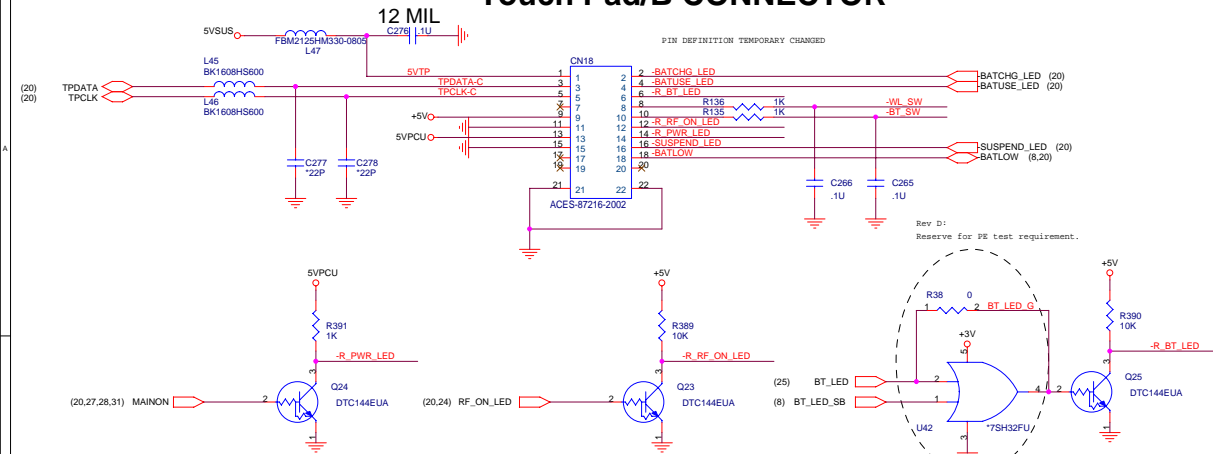
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

for EZ port

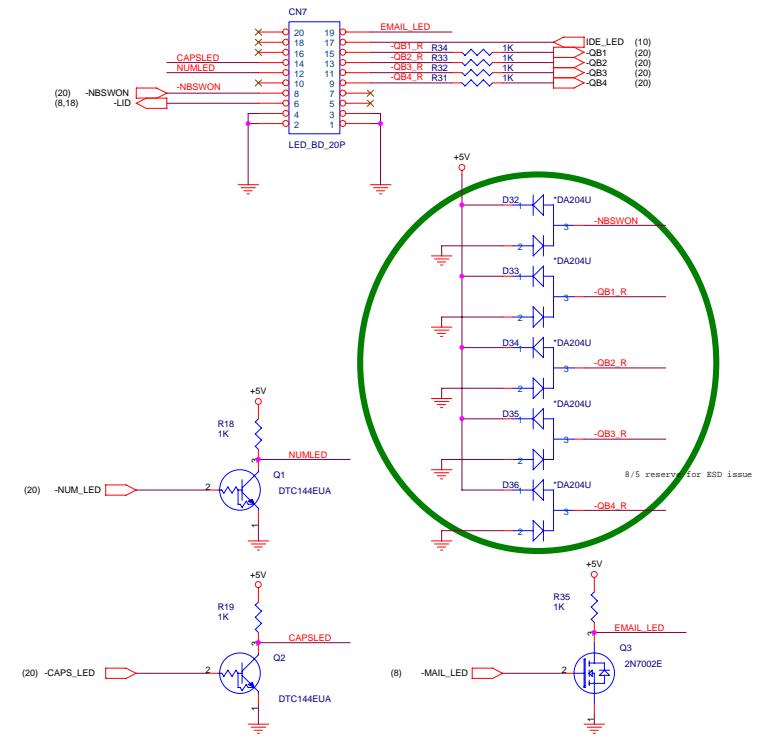
PROJECT : Z15
Quanta Computer Inc.

Size Custom	Document Number	Rev 2A
PCU(NS87570)		
Date: Tuesday, September 14, 2004	Sheet 20	of 33

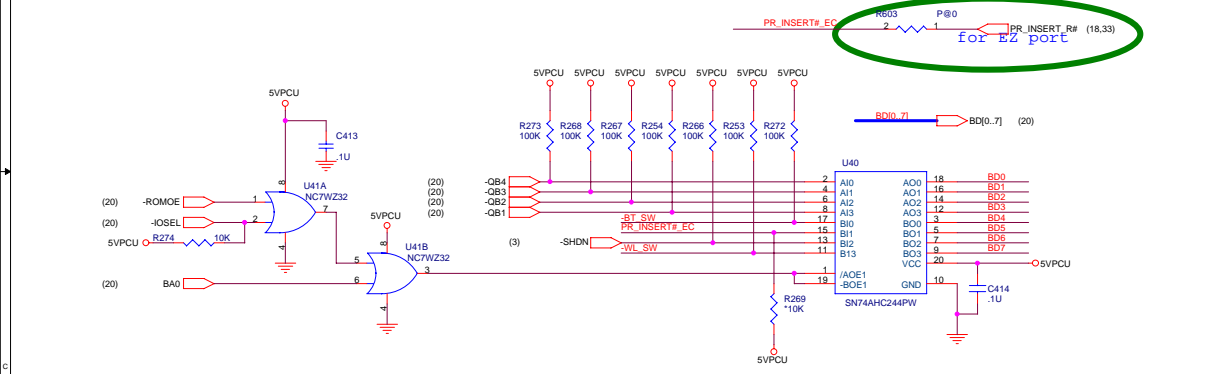
Touch Pad/B CONNECTOR



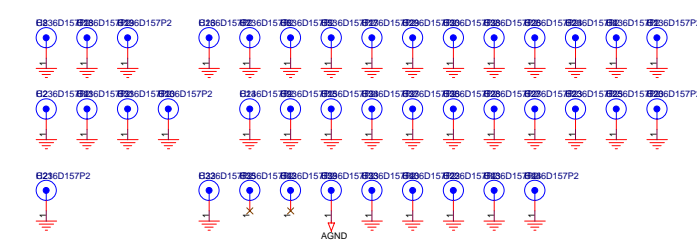
LED/B CONNECTOR



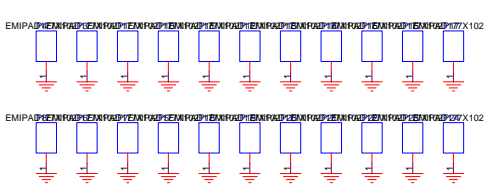
570 EXPEND I/O



Screw Holes

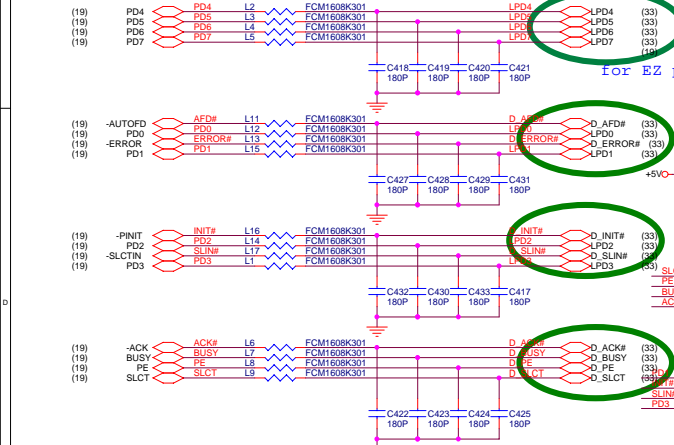


EMI Pads

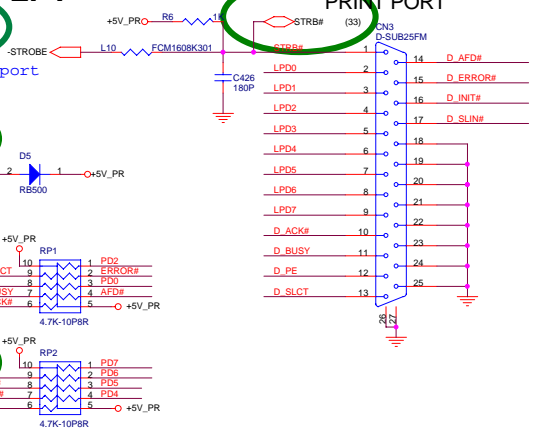


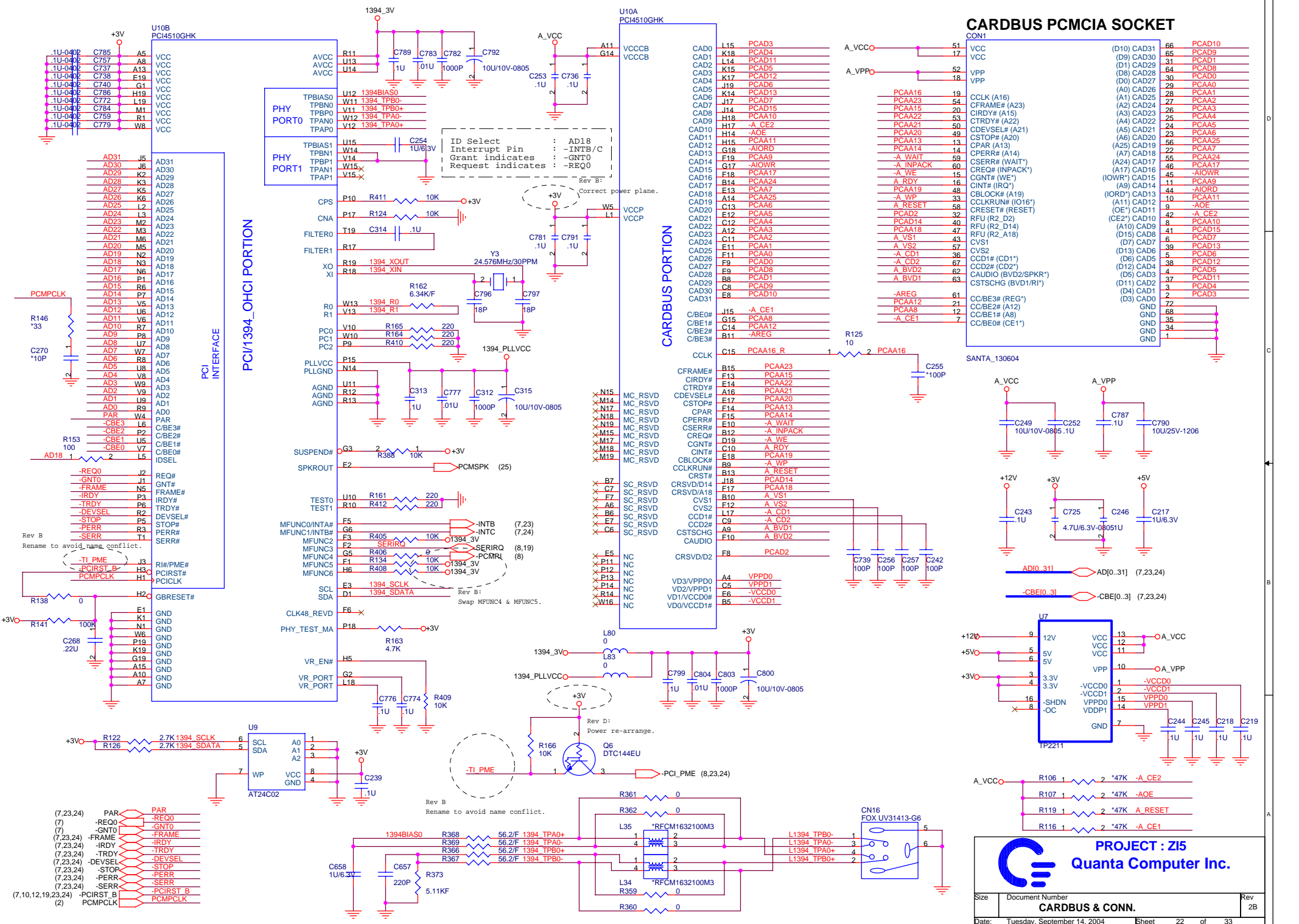
6/14 DEL H3, H11, H12, H13, P9

LPT

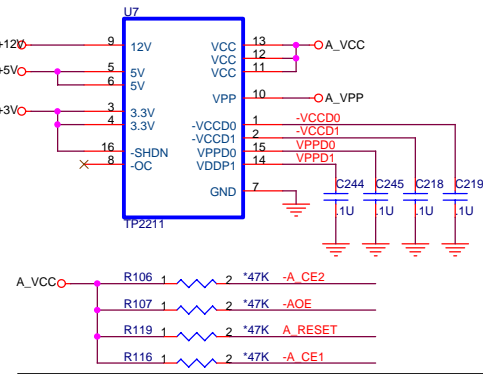
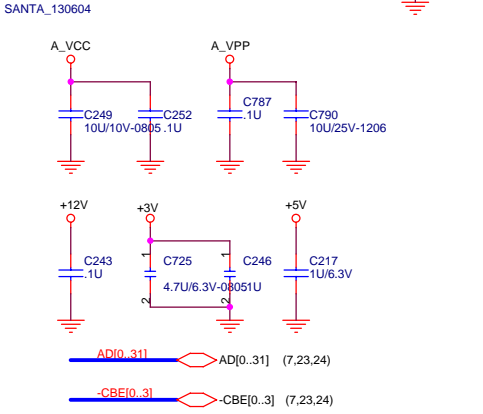
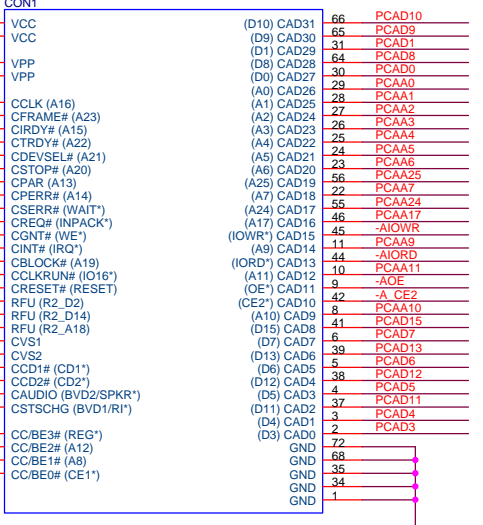


PRINT PORT





CARDBUS PCMCIA SOCKET



PROJECT : Z15

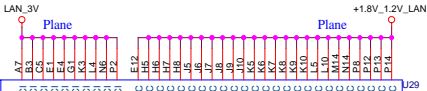
Quanta Computer Inc.

Size	Document Number	Rev
	CARDBUS & CONN.	2B
Date:	Tuesday, September 14, 2004	Sheet 22 of 33



3V_LAN & +3V are from system power

TX3N_R0	TX3N_R1	TX3N_R1	TX3N_R
TX2P_R0	TX2P_R1	TX2P_R1	TX2P_R
TX1P_R0	TX1P_R1	TX1P_R1	TX1P_R
TX0N_R0	TX0N_R1	TX0N_R1	TX0N_R
TX3P_R0	TX3P_R1	TX3P_R1	TX3P_R
TX2N_R0	TX2N_R1	TX2N_R1	TX2N_R
TX1N_R0	TX1N_R1	TX1N_R1	TX1N_R
TX0P_R0	TX0P_R1	TX0P_R1	TX0P_R



BCM5788M

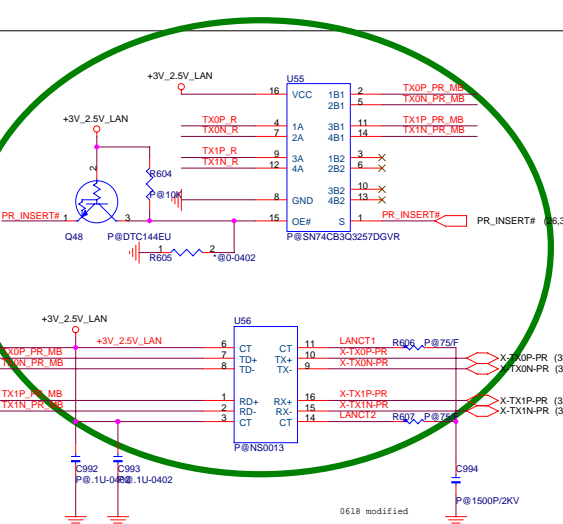
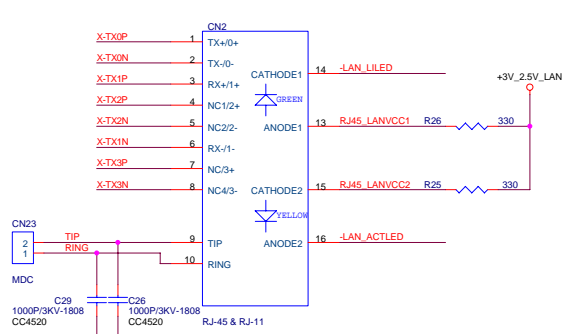
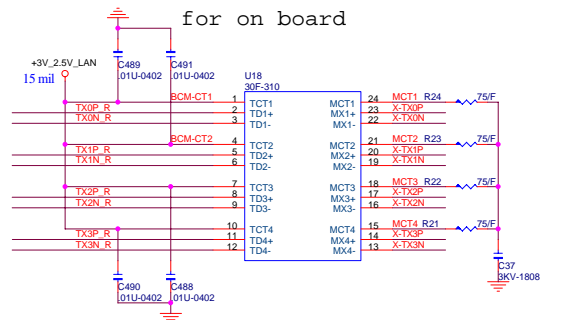
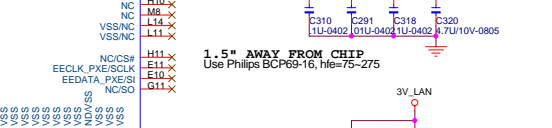
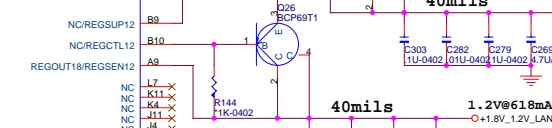
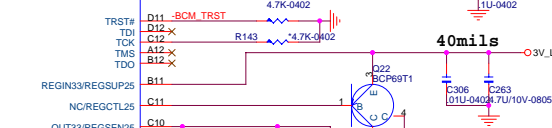
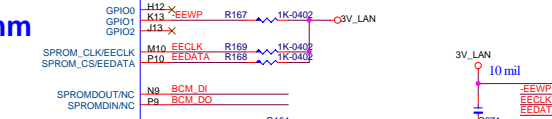
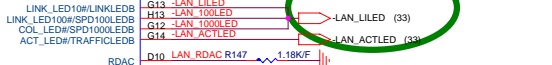
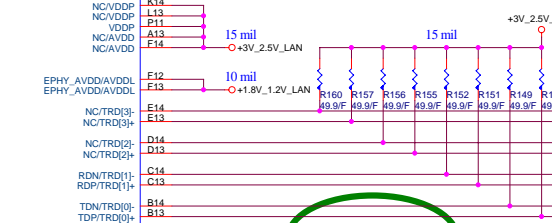
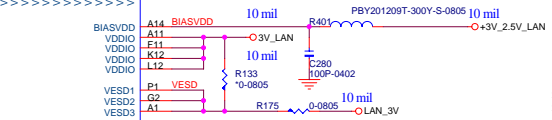
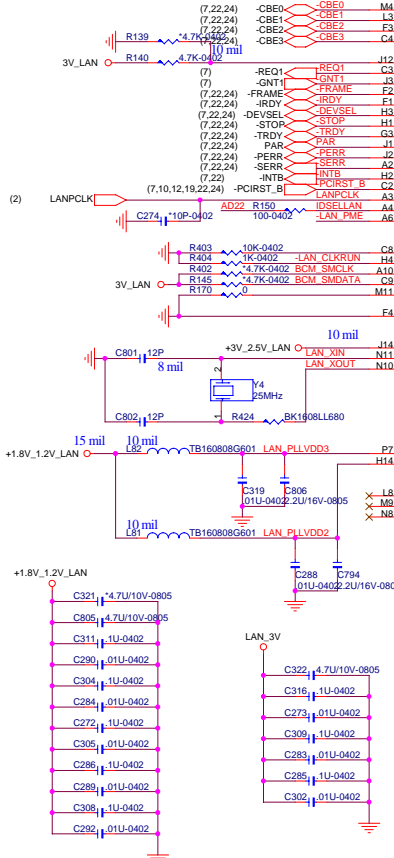
BCM5788M LAN

```

ID Select      : AD22
Interrupt Pin  : -INTB
Request indicates : -REQ0
Grant indicates : -GNT1
  
```

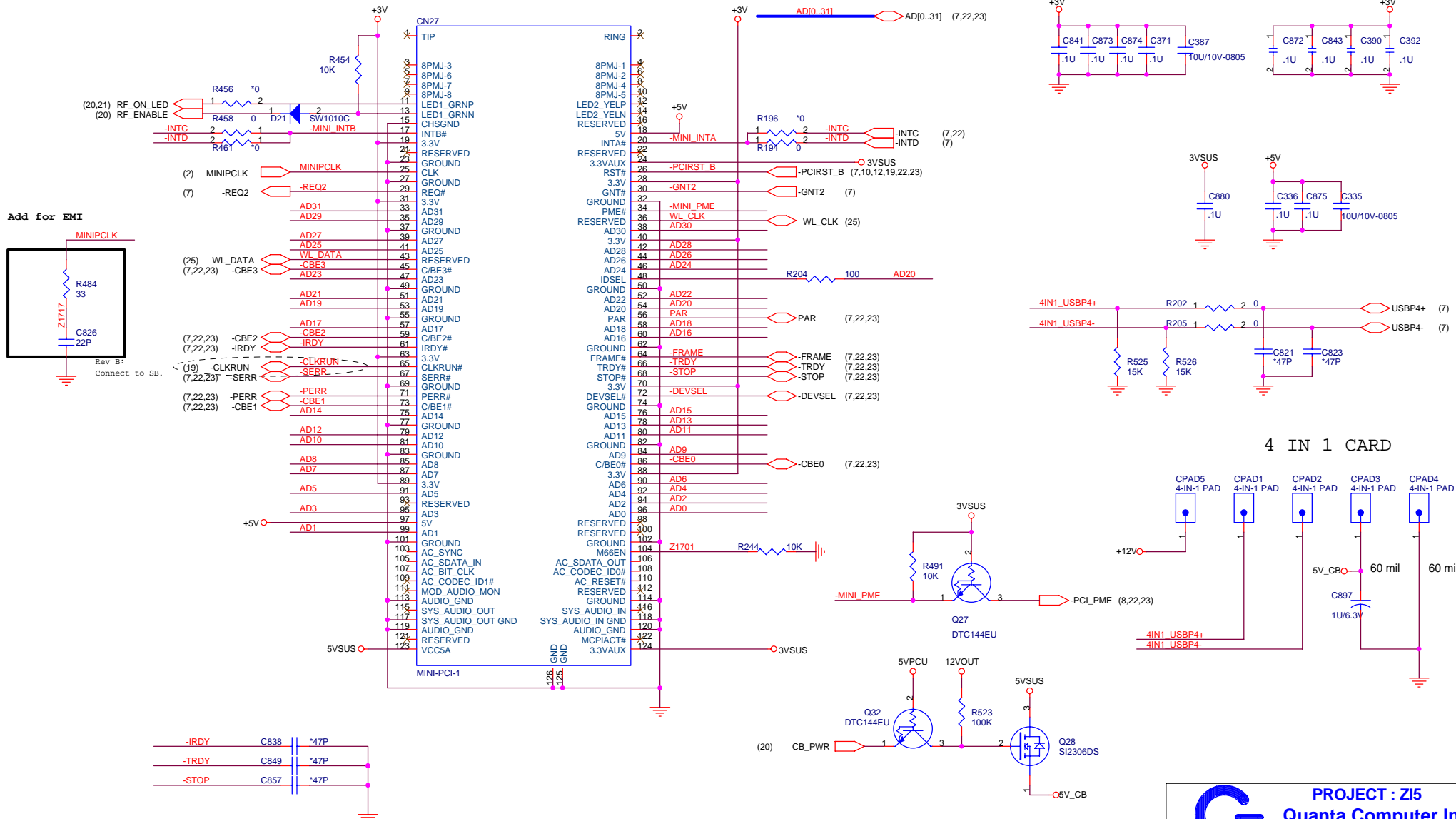
AD0	N7	AD0
AD1	M7	AD1
AD2	P6	AD2
AD3	P5	AD3
AD4	N5	AD4
AD5	M4	AD5
AD6	P4	AD6
AD7	N4	AD7
AD8	P3	AD8
AD9	M3	AD9
AD10	N2	AD10
AD11	M1	AD11
AD12	P2	AD12
AD13	N1	AD13
AD14	M0	AD14
AD15	L2	AD15
AD16	K1	AD16
AD17	E3	AD17
AD18	D1	AD18
AD19	D2	AD19
AD20	D3	AD20
AD21	C1	AD21
AD22	B1	AD22
AD23	B2	AD23
AD24	A4	AD24
AD25	A5	AD25
AD26	B5	AD26
AD27	B6	AD27
AD28	C6	AD28
AD29	C7	AD29
AD30	A6	AD30
AD31	B8	AD31

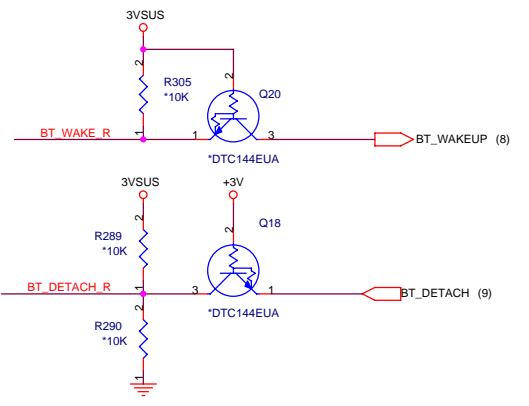
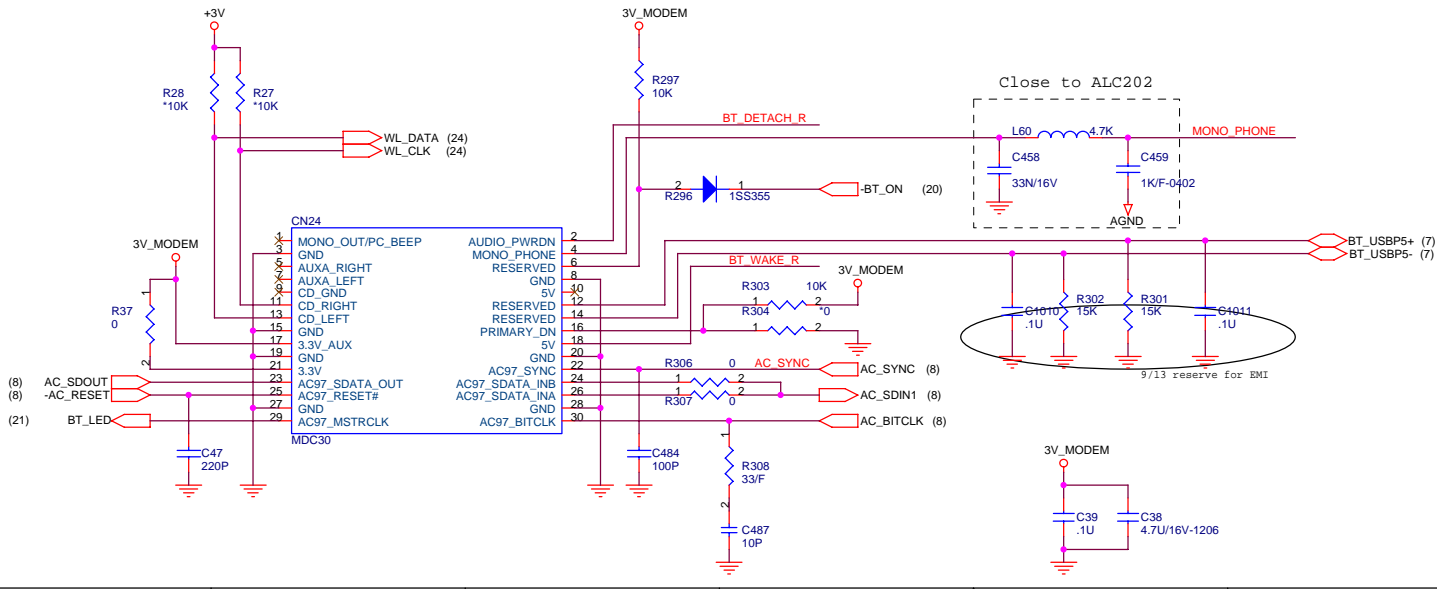
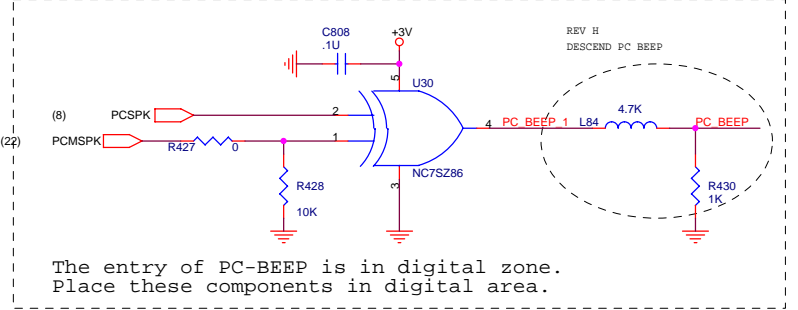
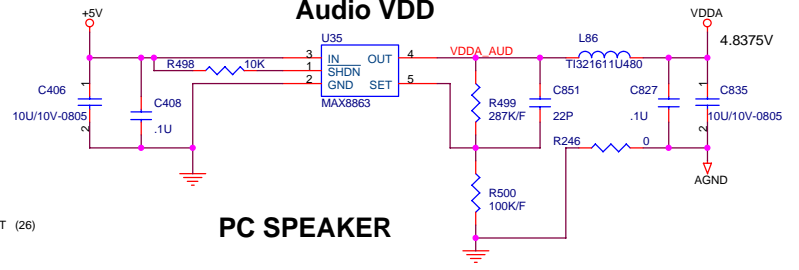
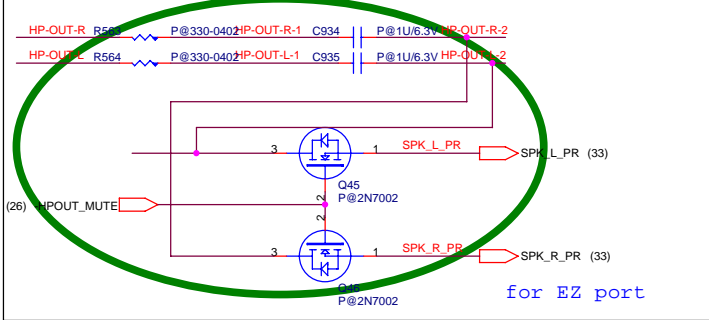
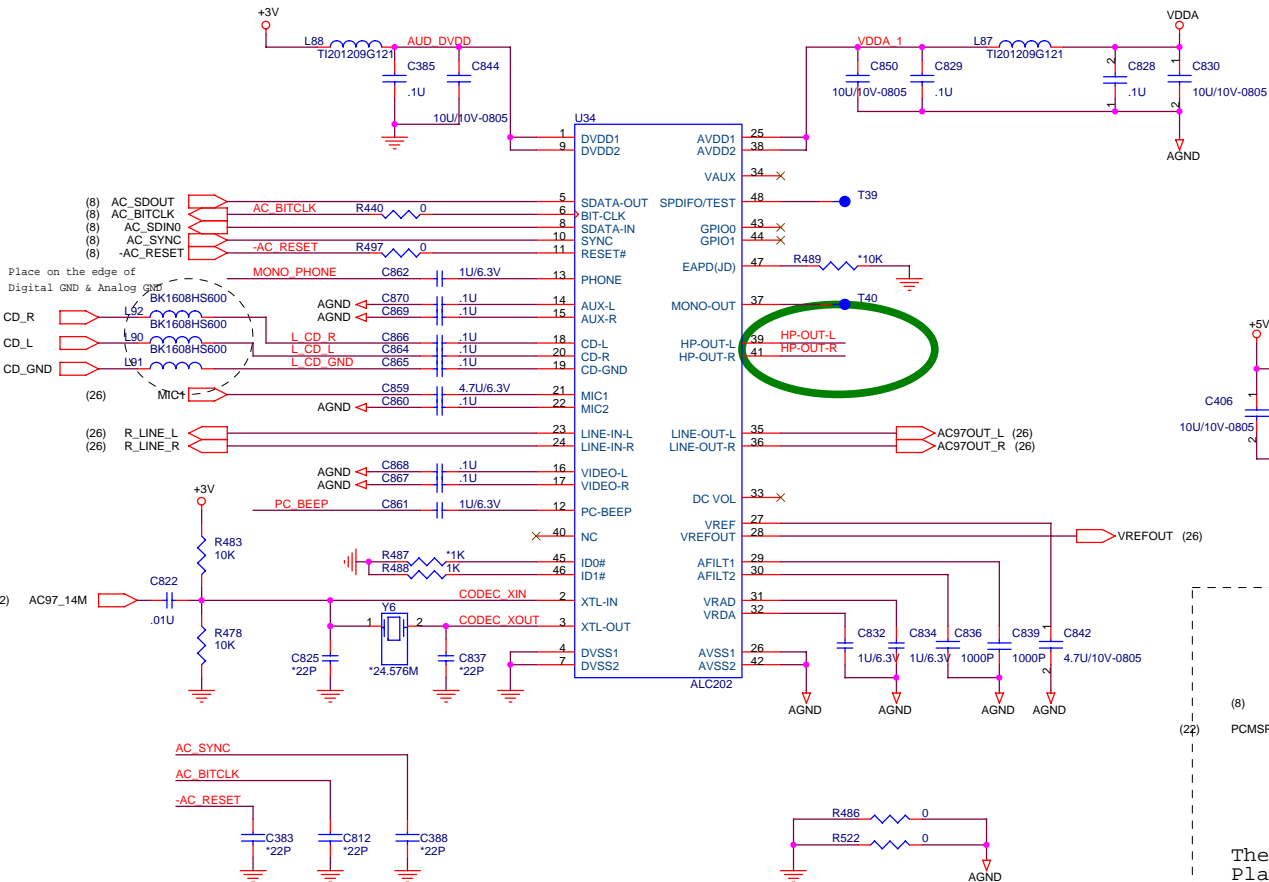
15mm x 15mm BGA196



ID Select : AD20
 Interrupt Pin : -INTC/D
 Grant indicates : -GNT2
 Request indicates : -REQ2

TYPE III MINI PCI SOCKET

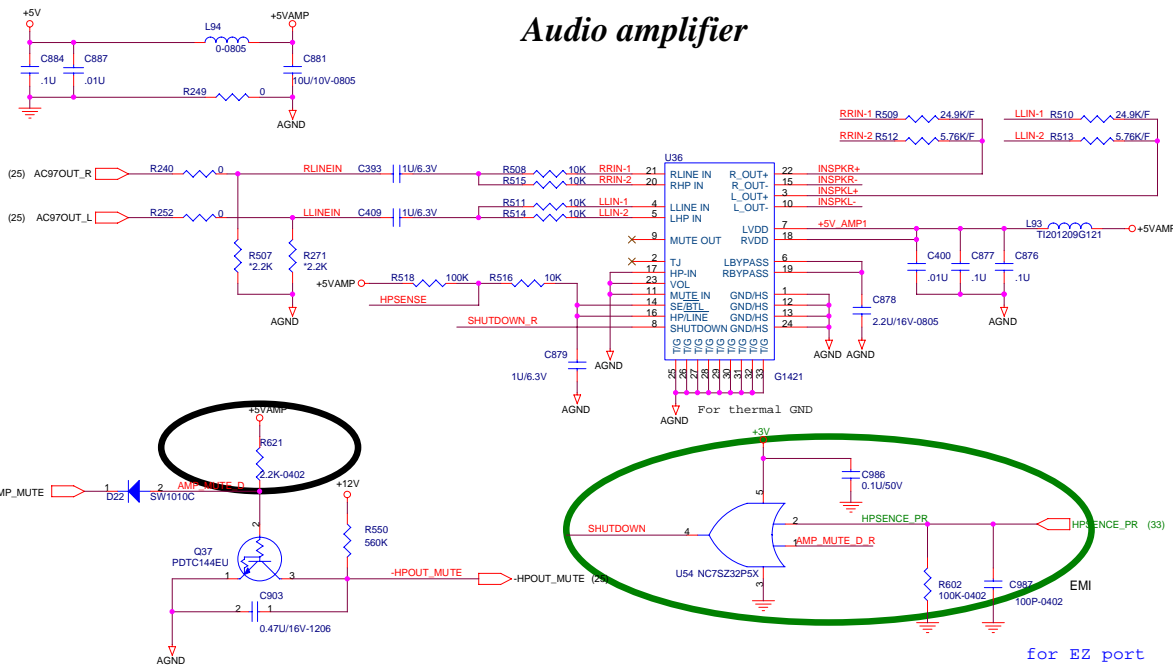




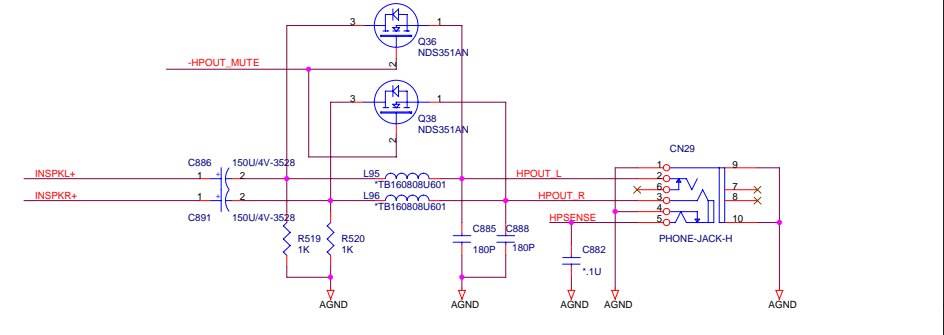
PROJECT : Z15
Quanta Computer Inc.

Size Custom	Document Number	Rev 3C
AC97 CODEC		
Date: Tuesday, September 14, 2004	Sheet 25 of 33	

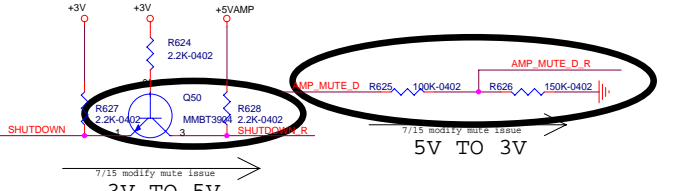
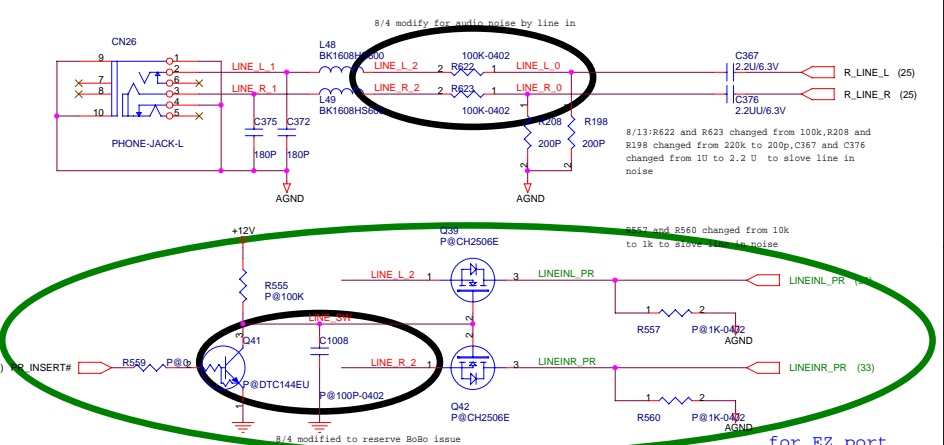
Audio amplifier



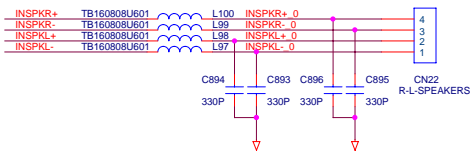
Headphone out



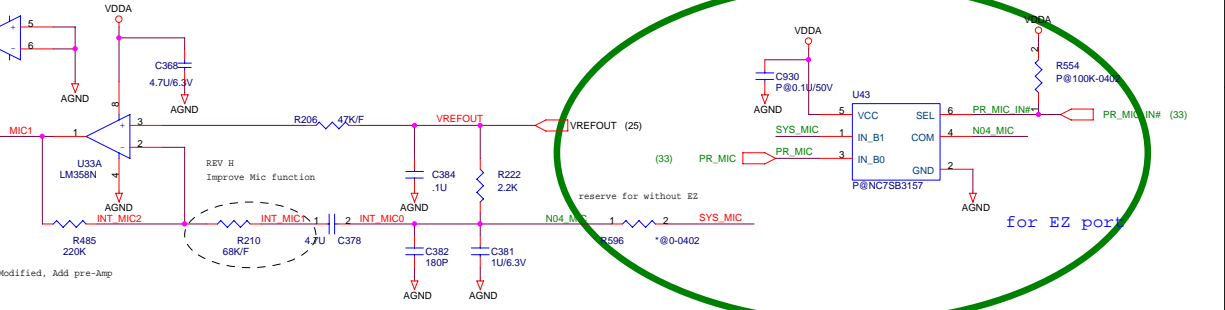
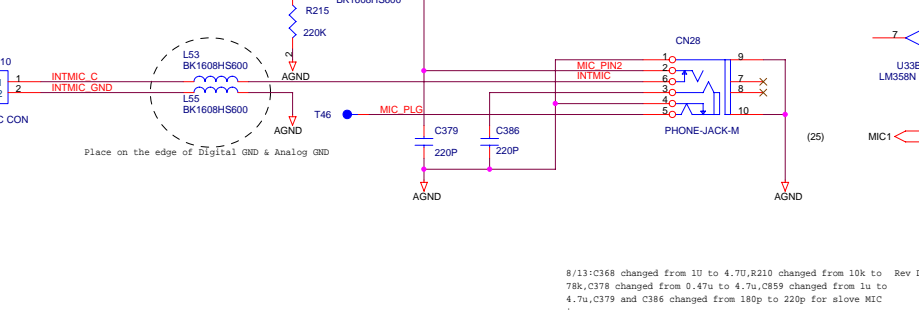
Line in



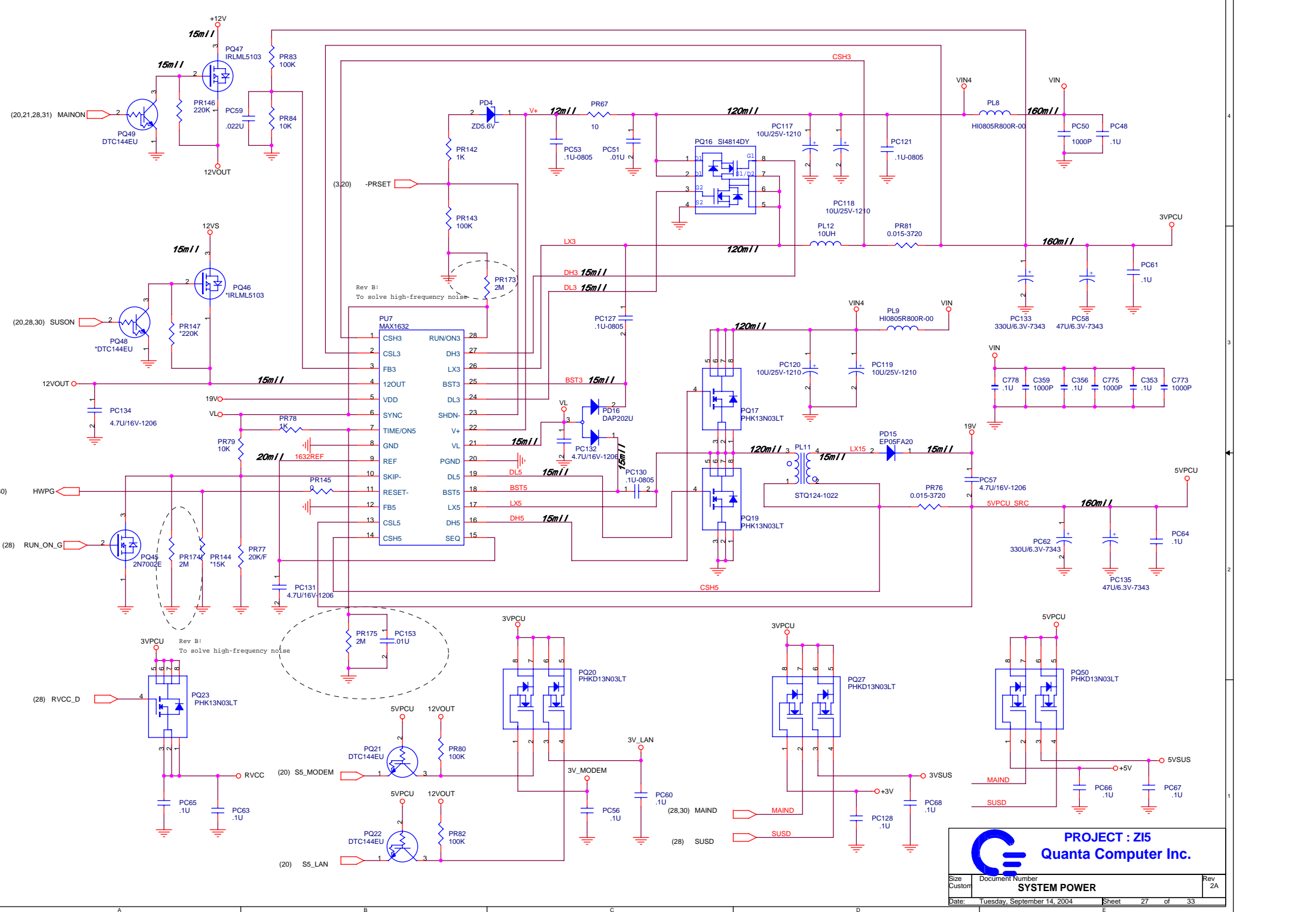
INT. SPEAKER



Mic in

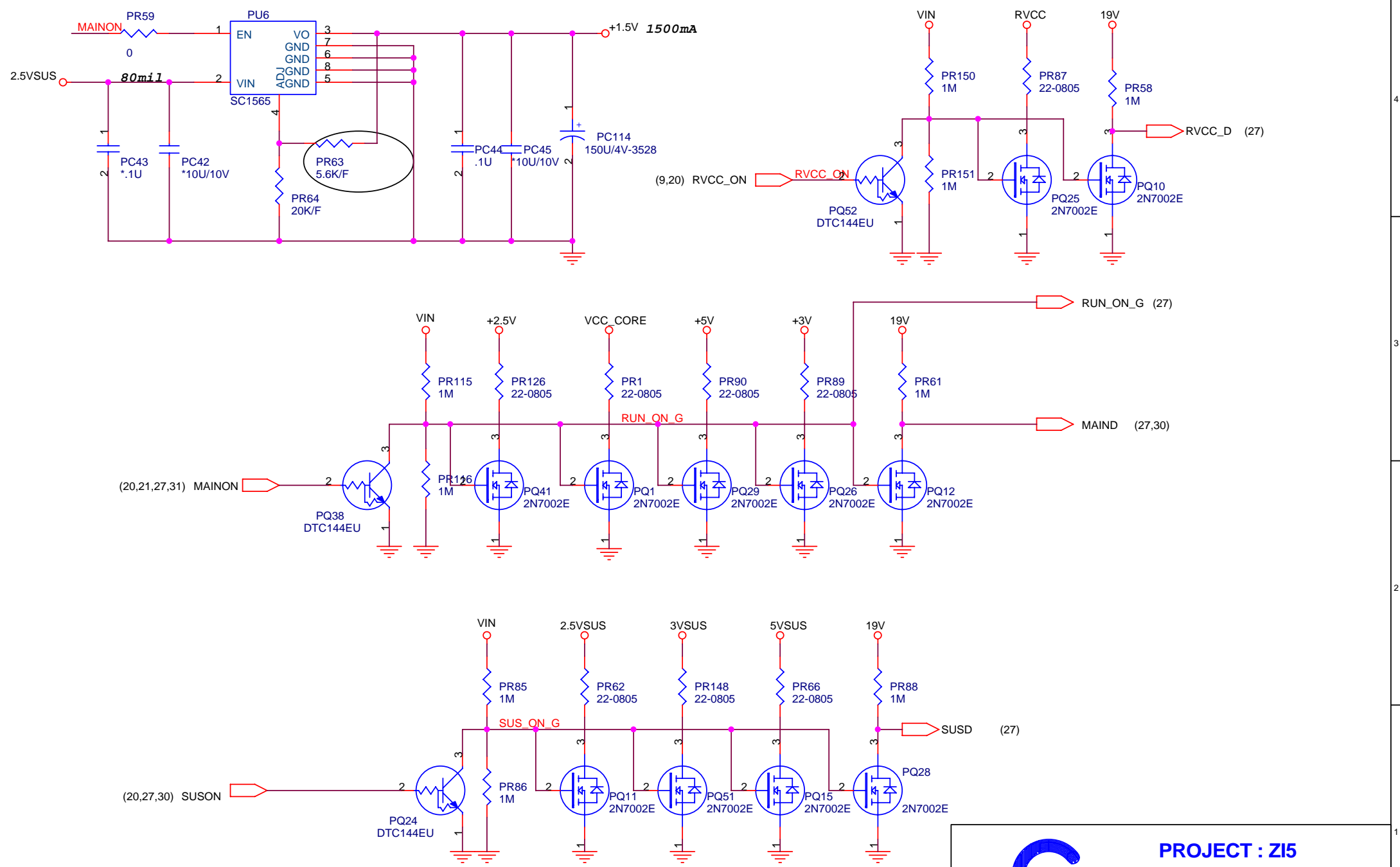



8/13: C368 changed from 1u to 4.7u, R210 changed from 10k to 78k, C378 changed from 0.47u to 4.7u, C859 changed from 1u to 4.7u, C379 and C386 changed from 180p to 220p for solve MIC issue



PROJECT : Z15
Quanta Computer Inc.

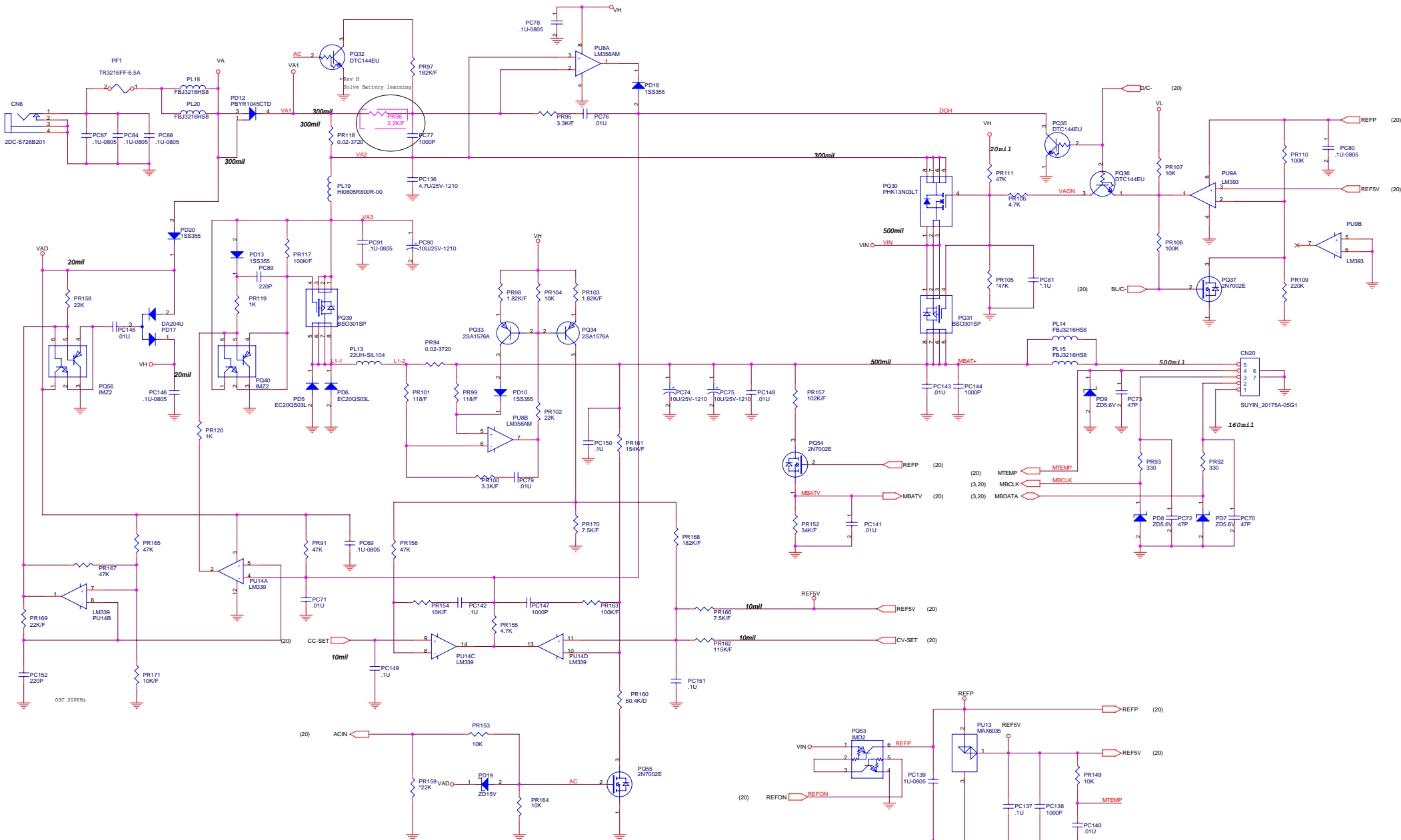
Size	Document Number	Rev
Custom	SYSTEM POWER	2A
Date:	Tuesday, September 14, 2004	Sheet 27 of 33

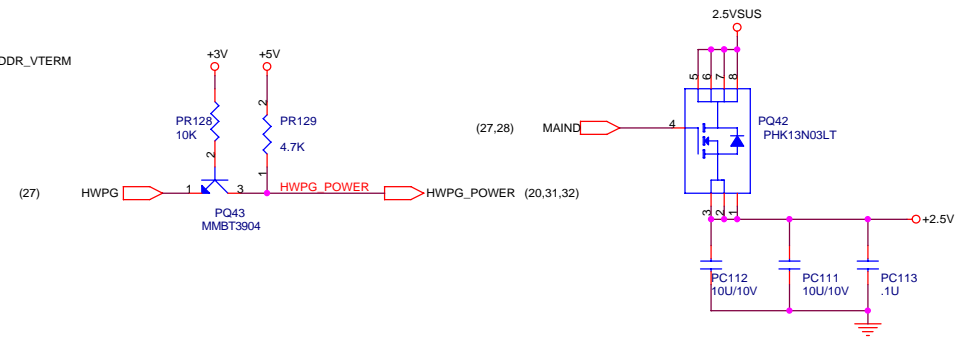
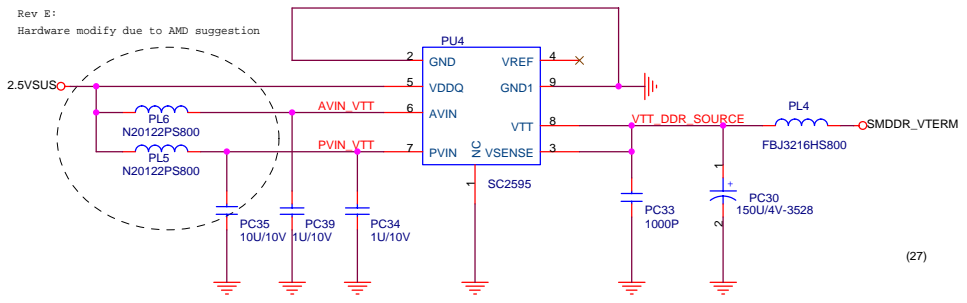
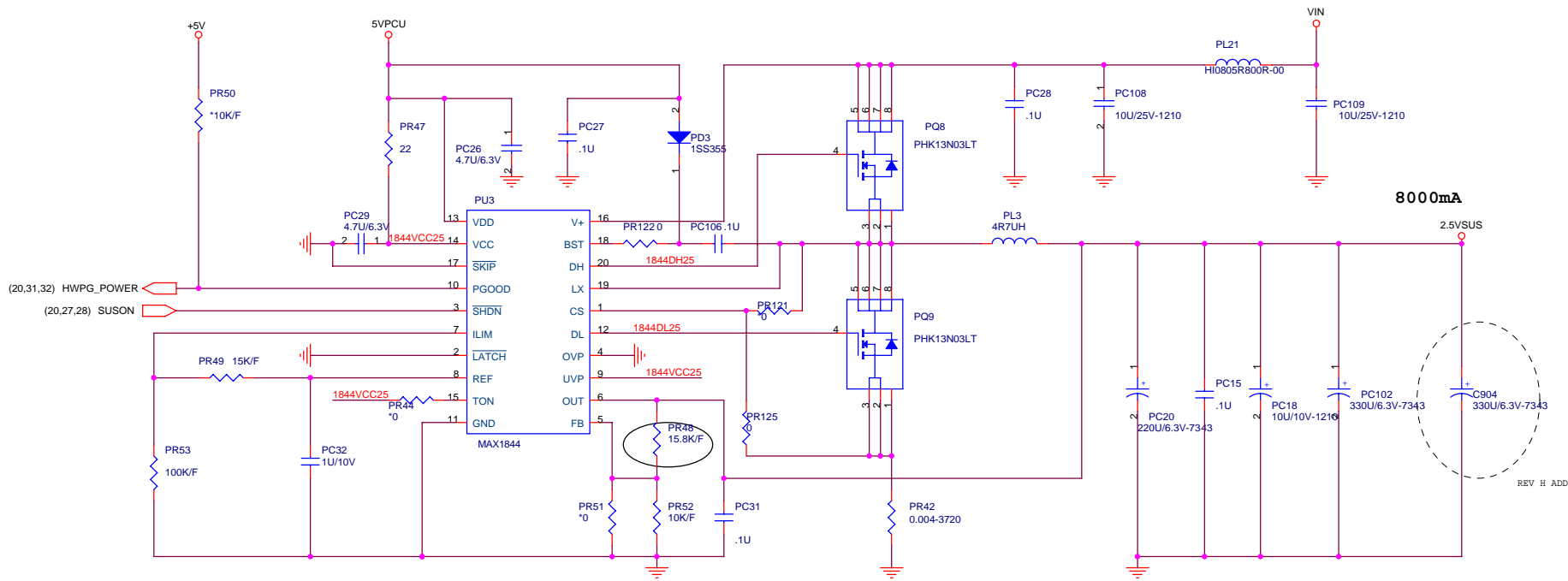


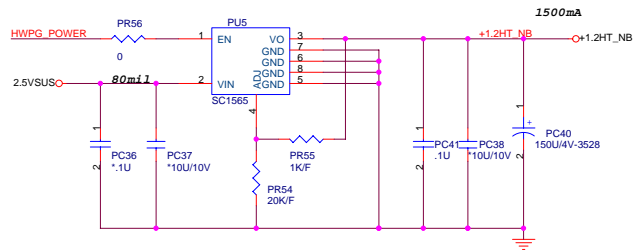
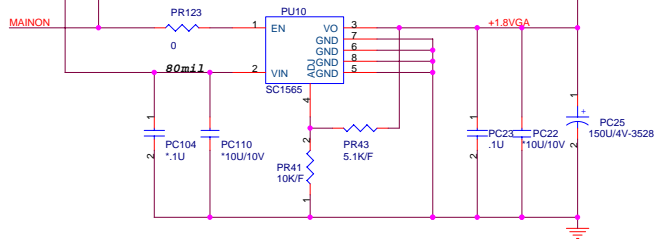
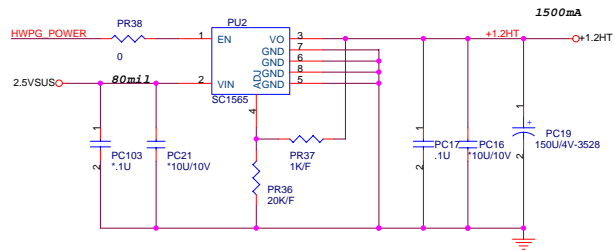
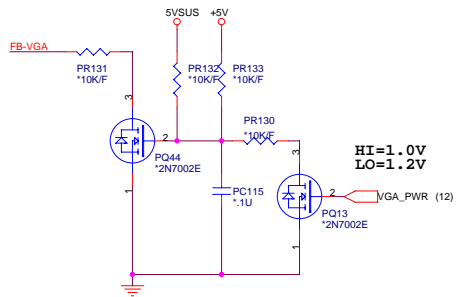
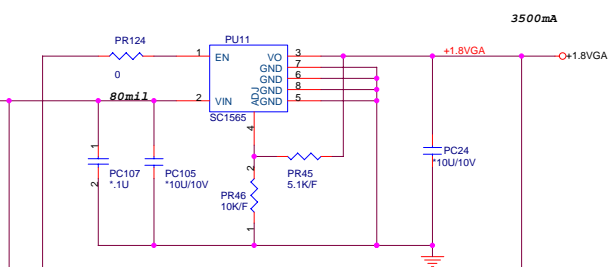
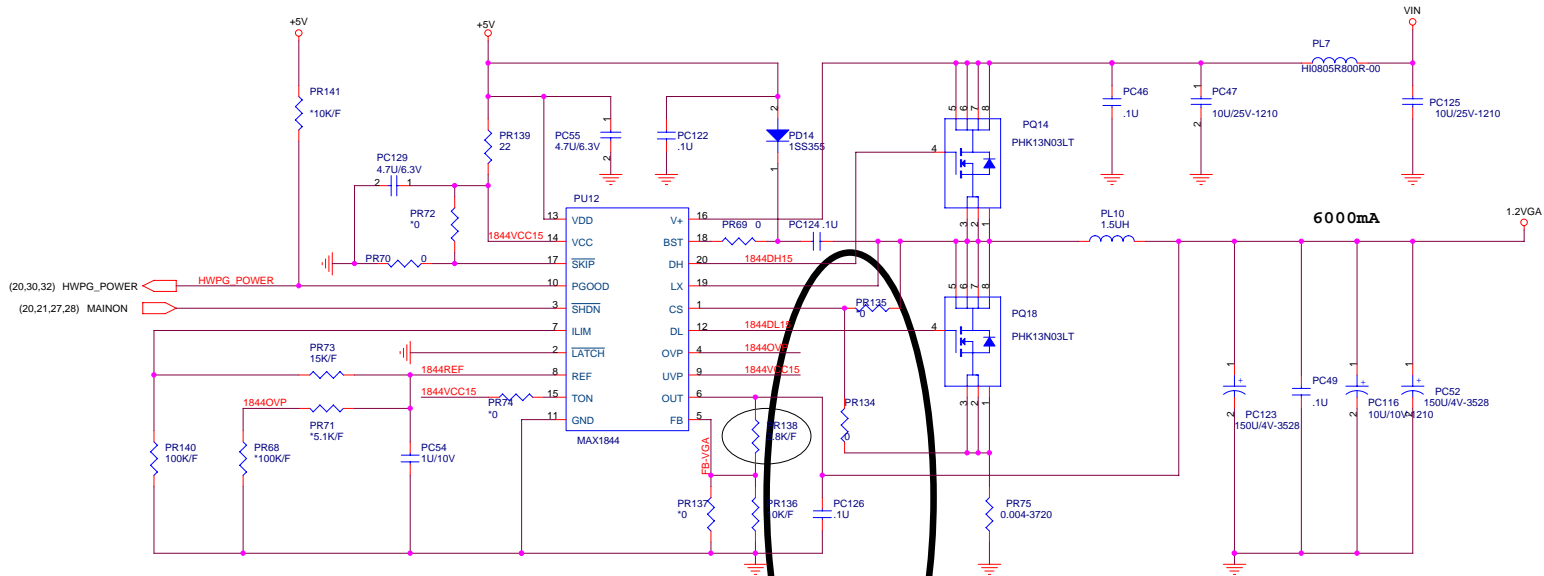


PROJECT : Z15
Quanta Computer Inc.

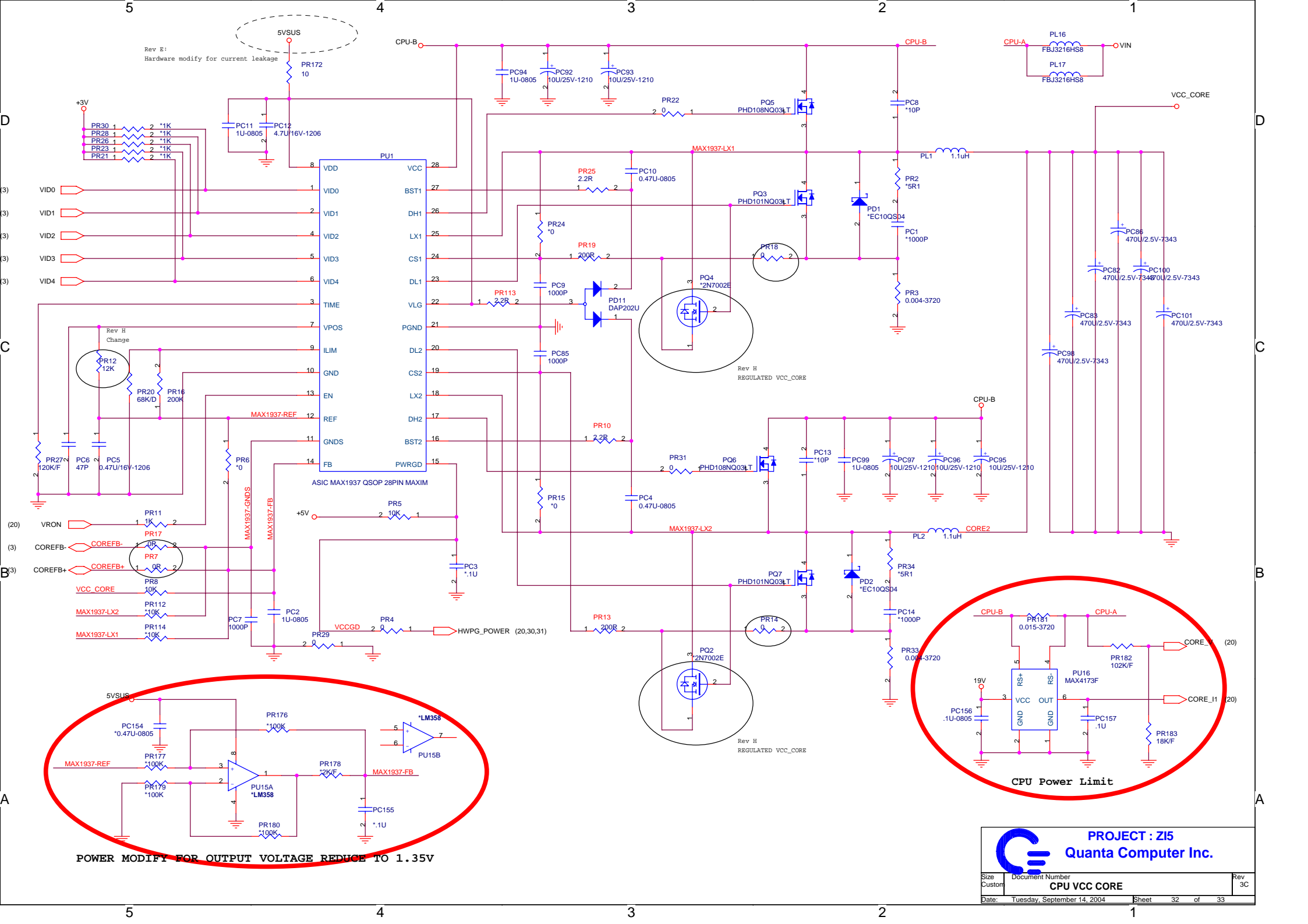
Size Custom	Docu. Number	Rev 1A
DISCHARGE CIRCUIT		
Date: Tuesday, September 14, 2004		Sheet 28 of 33







8/4 modified for 1.2V 3D
fail----change PR134 and PR135



Rev B:
Hardware modify for current leakage

PR30 1 2 *1K
PR28 1 2 *1K
PR26 1 2 *1K
PR23 1 2 *1K
PR21 1 2 *1K

Rev H
Change

Rev H
REGULATED VCC_CORE

POWER MODIFY FOR OUTPUT VOLTAGE REDUCE TO 1.35V

CPU Power Limit

PROJECT : Z15
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU VCC CORE	3C
Date:	Tuesday, September 14, 2004	Sheet 32 of 33

