BAP/BXP30

A02 Build

2010.05.22

INVENTEC			
TITLE: BAP/BXP30			
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01
CHANGE by: IEC	DATE: Saturday, May 22, 2010	SHEET: 1 of 41	

1. Schematic Page Description :

BAP30/BXP30 Schematic Ver : X01

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
None	

PCIINT	CHIP	Interface
None		

REQ	CHIP
None	

3. USB & PCI-Express & SATA Description :

USB Port	DEVICE	USB Port	DEVICE
Port 0	System (ESATA)	Port 7	Bluetooth
Port 1	System	Port 8	
Port 2	System	Port 9	Web Cam
Port 3	System	Port 10	
Port 4	CardReader	Port 11	FingerPrint
Port 5		Port 12	
Port 6		Port 13	3G

PCI-E	DEVICE
Port 1	New Card
Port 2	Docking
Port 3	Mini Card(WLAN)
Port 4	Mini Card(3G)
Port 5	Mini Card(ROBSON)
Port 6	Giga-LAN

SATA	DEVICE
Port 1	HDD
Port 2	E-SATA
Port 4	BAY
Port 5	None

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TITLE: BAP/BXP30
schematics page DESCR

SIZE	CODE	DOC.NUMBER	REV
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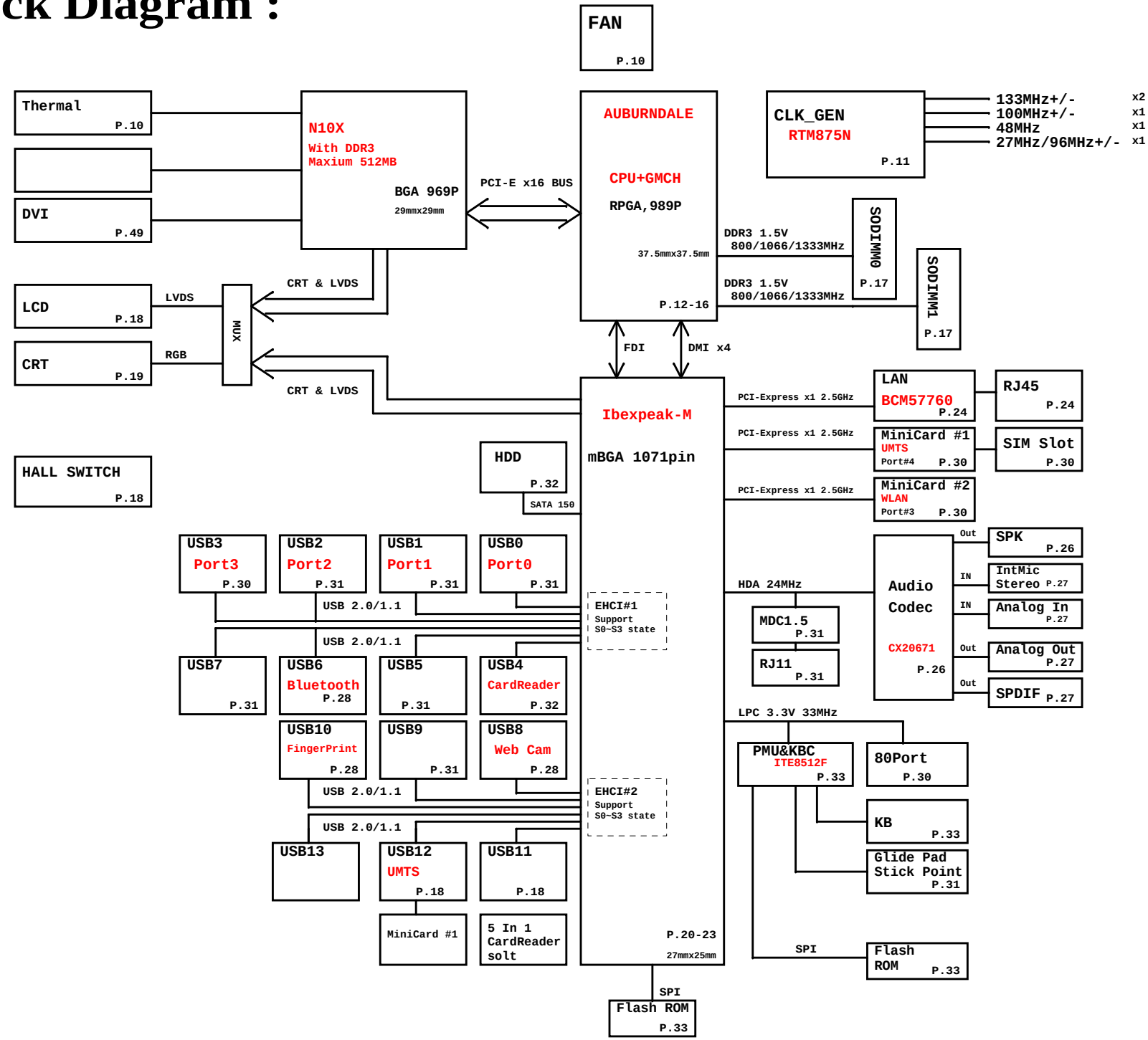
3. Block Diagram :



INVENTEC

TITLE: BAP/BXP30
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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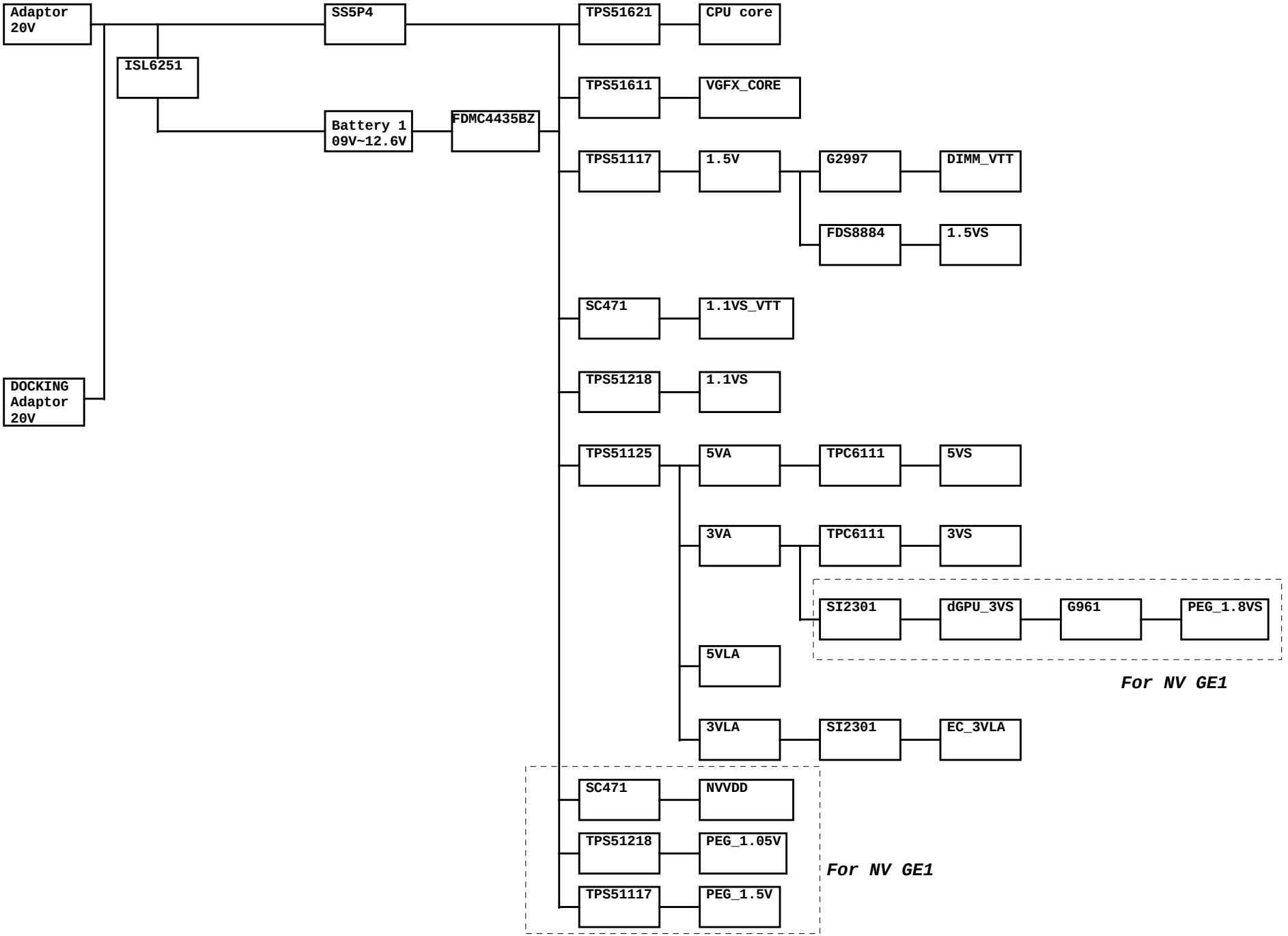
Power Block Diagram :



INVENTEC			
TITLE: BAP/BXP30 Power Block Diagram			
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X02
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4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
EC_3VLA	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
3VM	3.3V power rail by SUSM#
1.05VM	1.05V switched power rail by SUSM#
1.5V	1.5V switched power rail by SUSC#
1.8V	1.8V power rail by SUSC#
3VS	3.3V power rail by SUSB#
5VS	5.0V power rail by SUSB#
1.5VS	1.5V power rail by SUSB#
1.05VS	1.05V power rail by SUSB#
PWR_DIMM_VTT	0.75V DDR Termination Voltage by SUSB#
VGFX_CORE	1.05V power rail for UMA by SUSB#
PEG_1.8VS	1.8V switched power rail for NB9x by SUSB#
PEG_PEX_1.1VS	1.1V switched power rail for NB9x by SUSB#
PEG_NVDD	Variable switched power rail for NB9x by SUSB#
Vcore_CPU	Core switched power rail for CPU

Part Naming Conventions

C	=	Capacitor	Q	=	Transistor
CN	=	Connector	R	=	Resistor
D	=	Diode	RP	=	Resistor Pack
F	=	Fuse	U	=	Arbitrary Logic Device
L	=	Inductor	Y	=	Crystal and Osc

Name Suffix

#	=	Active Low signal
NU	=	No Stuff

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn HFM:	1.3319V~1.4375V~1.4591V	36A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn: AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GM: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GM: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GM:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GM:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GM:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GM:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GM:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GM:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GM: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GM: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GM: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GM: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GM: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GM: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GM: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GM: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GM: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS397BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:	3.0V~3.3V~3.6V	
	Super I/O: IT8305E		
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:82567LM	1.0V and 1.8V	Each 1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: GL827	3.0V~3.3V~3.6V	
	Azalia Codec: ALC262	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	ODD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
	Audio AMP: G1432		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	1.5A
	USB and ESATA	5VA	2A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

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INVENTEC

TITLE: BAP/BXP30 Annotations

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6.Schematic modify Item and History :

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INVENTEC

TITLE: BAP/BXP30
schematics modify

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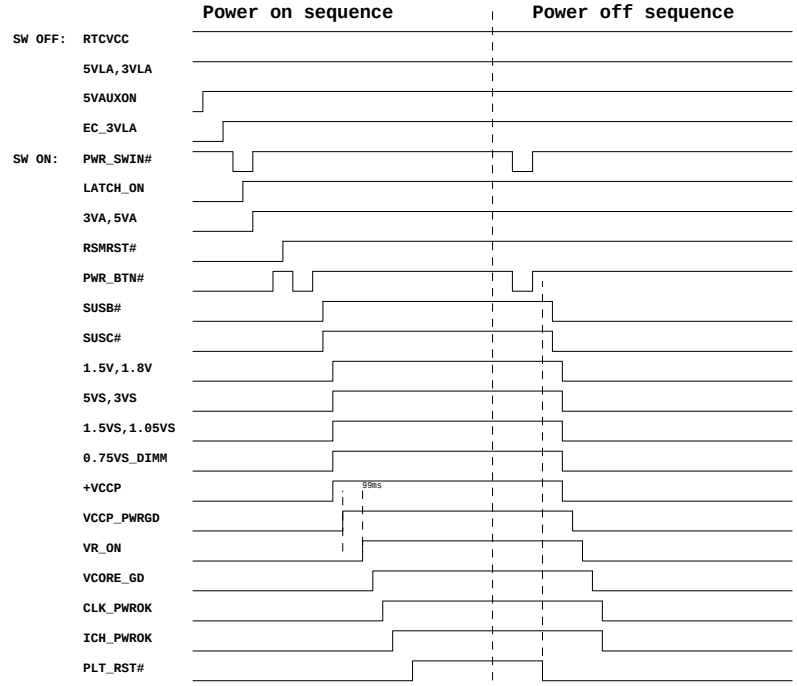
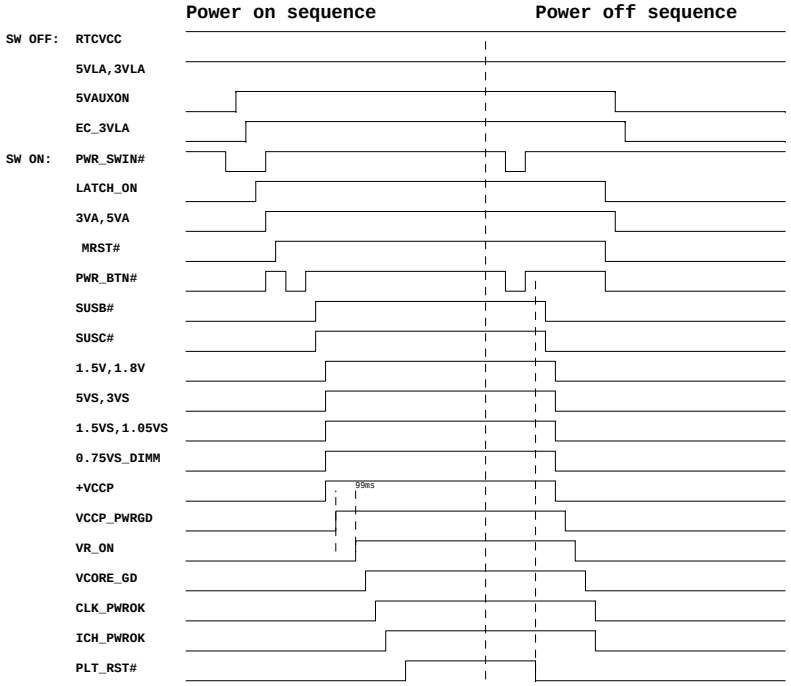
8.SYSTEM POWER SEQUENCE :

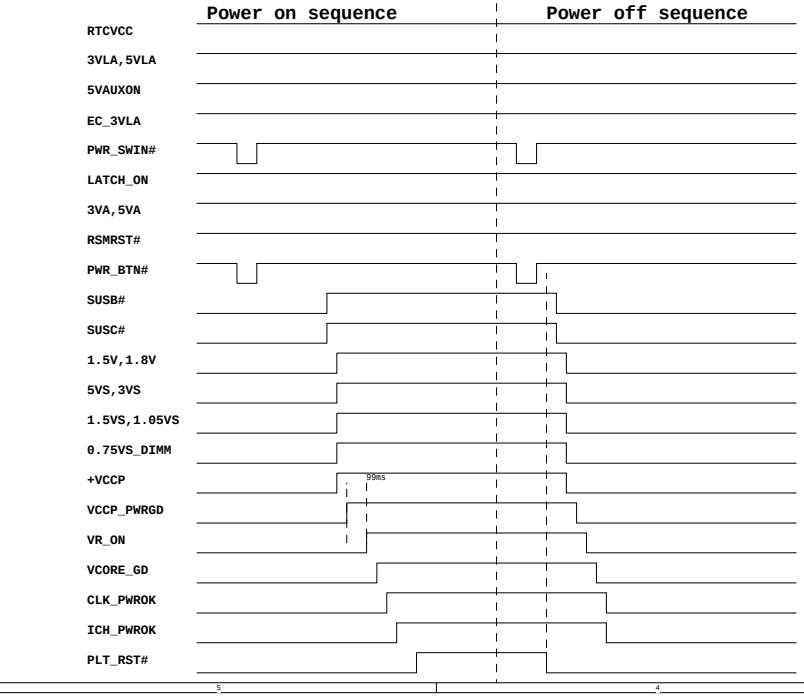
Power on/off sequence AC insert(First)



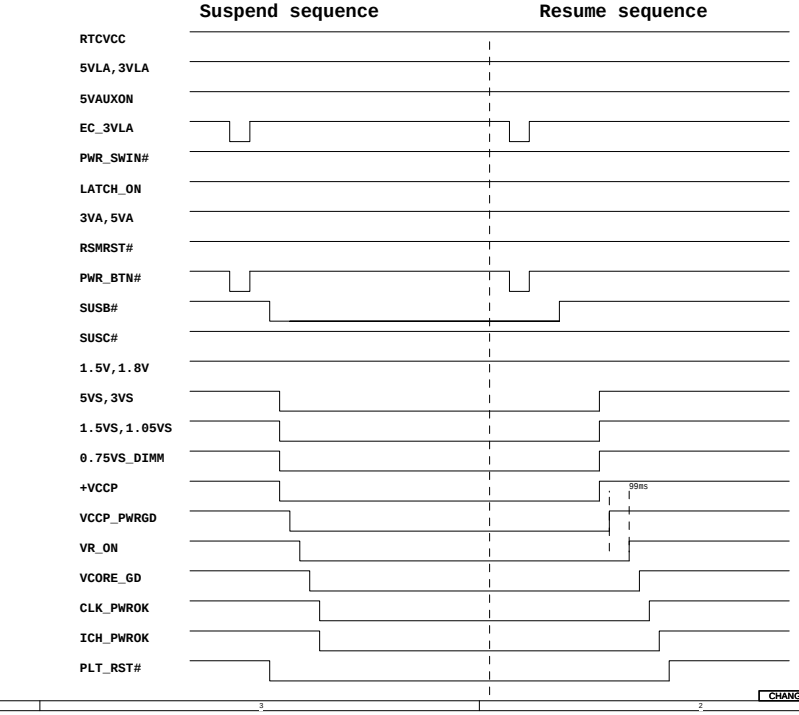
Battery only Power on/off sequence



Power on/off sequence AC insert(S4)



Suspend resume sequence(S3)



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INVENTEC

TITLE: BAP/BXP30
Timing Diagram

SIZE	CODE	DOC.NUMBER	REV
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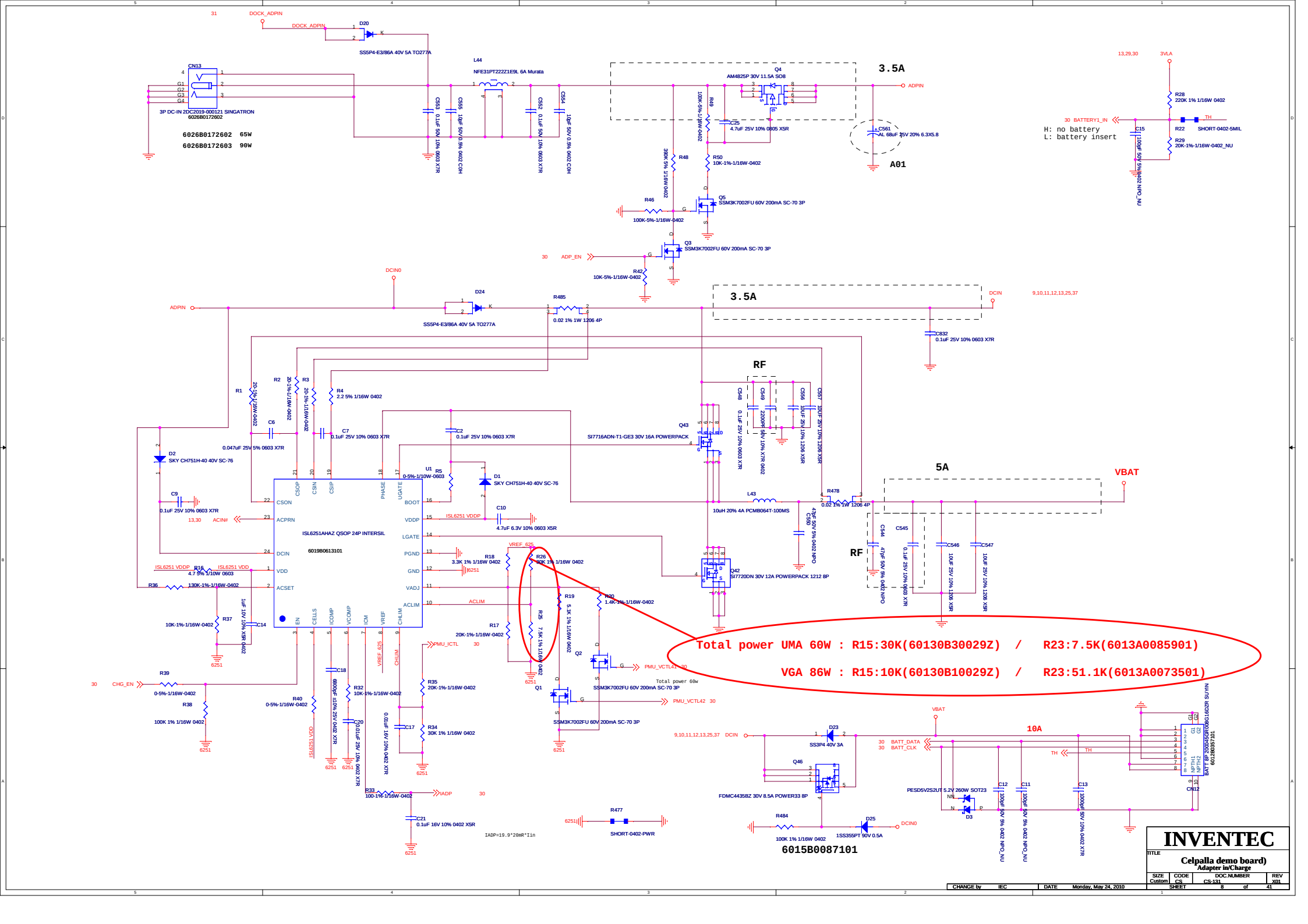
DOCK_ADPIN
D20
SSSP4-E3/86A 40V 5A TO277A
CN13
3P DC-IN 2DC2019-000121 SINGATRON
6026B0172602
6026B0172602 65W
6026B0172603 90W
L44
NFE31PT222Z1E9L 6A Murata
C553 0.1uF 50V 10% 0603 X7R
C555 10uF 50V 0.5% 0402 C0H
C552 0.1uF 50V 10% 0603 X7R
C554 10uF 50V 0.5% 0402 C0H
Q4
AM4825P 30V 11.5A SO8
3.5A
ADPIN
R49 10K-5%-1/16W-0402
C25 4.7uF 25V 10% 0805 X5R
C561 AL 68uF 25V 20% 6.3X5.8
A01
R48 383K 5% 1/16W 0402
R50 10K-1%-1/16W-0402
R46 100K-5%-1/16W-0402
Q5 SSM3K7002FU 60V 200mA SC-70 3P
Q3 SSM3K7002FU 60V 200mA SC-70 3P
ADP_EN
R42 10K-5%-1/16W-0402
13,29,30
3VLA
R28 220K 1% 1/16W 0402
30 BATTERY1_IN
H: no battery
L: battery insert
C15 1000pF 50V 5% 0402 NPO_NU
R22 SHORT-0402-5MIL
R29 20K-1%-1/16W-0402_NU
DCIN0
D24
SSSP4-E3/86A 40V 5A TO277A
R485 0.02 1% 1W 1206 4P
3.5A
DCIN
9,10,11,12,13,25,37
C832 0.1uF 25V 10% 0603 X7R
RF
C548 0.1uF 25V 10% 0603 X7R
C549 2200pF 50V 10% X7R 0402
C556 10uF 25V 10% 1206 X5R
C557 100uF 25V 10% 1206 X5R
Q43
SI7716ADN-T1-GE3 30V 16A POWERPACK
R1 20-1%-1/16W-0402
R2 20-1%-1/16W-0402
R3 20-1%-1/16W-0402
R4 2.2 5% 1/16W 0402
C6 0.047uF 25V 5% 0603 X7R
C7 0.1uF 25V 10% 0603 X7R
C2 0.1uF 25V 10% 0603 X7R
D2 SKY CH751H-40 40V SC-76
C9 0.1uF 25V 10% 0603 X7R
13,30 ACIN#
U1
ISL6251AHAZ QSOP 24P INTERSIL
6019B0613101
CSON
ACPRN
DCIN
VDD
ACSET
CSOP
CSIN
CSIP
PHASE
UGATE
BOOT
VDDP
LGATE
PGND
GND
VADJ
ACLIM
EN
CELLS
IOMP
VCOMP
IOM
VREF
CHLIM
R5 0-5%-1/10W-0603
D1 SKY CH751H-40 40V SC-76
C10 4.7uF 6.3V 10% 0603 X5R
ISL6251 VDDP
ISL6251 VDD
R16 4.7 5% 1/10W 0603
R36 130K-1%-1/16W-0402
R37 10K-1%-1/16W-0402
C14 1uF 10V 10% X5R 0402
6251
VREF_625
R18 3.3K 1% 1/16W 0402
R17 20K-1%-1/16W-0402
R26 40K 1% 1/16W 0402
R25 7.5K 1% 1/16W 0402
R19 5.1K 1% 1/16W 0402
R40 1.4K-1% 1/16W-0402
ACLIM
PMU_ICTL 30
Q2
Q1
SSM3K7002FU 60V 200mA SC-70 3P
PMU_VCTL41 30
PMU_VCTL42 30
Total power 60w
L43
10uH 20% 4A PCMB064T-100MS
R478 0.02 1% 1W 1206 4P
C550 470pF 50V 5% 0402 NPO
Q42
SI7720DN 30V 12A POWERPACK 1212 8P
5A
VBAT
RF
C544 470pF 50V 5% 0402 NPO
C545 0.1uF 25V 10% 0603 X7R
C546 10uF 25V 10% 1206 X5R
C547 10uF 25V 10% 1206 X5R
Total power UMA 60W : R15:30K(60130B30029Z) / R23:7.5K(6013A0085901)
VGA 86W : R15:10K(60130B10029Z) / R23:51.1K(6013A0073501)
30 CHG_EN
R39 0-5%-1/16W-0402
R38 100K 1% 1/16W 0402
R40 0-5%-1/16W-0402
C18 6800pF 100V 25V 0402 X7R
R32 10K-1%-1/16W-0402
C20 0.01uF 25V 10% 0402 X7R
C17 0.01uF 16V 10% 0402 X7R
R35 20K-1%-1/16W-0402
R34 30K 1% 1/16W 0402
R33 100-1% 1/16W-0402
IADP 30
C21 0.1uF 16V 10% 0402 X5R
IADP=19.9*20mR*Iin
R477 SHORT-0402-PWR
9,10,11,12,13,25,37 DCIN
D23 SS3P4 40V 3A
Q46
FDMC4435BZ 30V 8.5A POWER33 8P
R484 100K 1% 1/16W 0402
D25 1SS355PT 90V 0.5A
DCIN0
6015B0087101
VBAT
10A
30 BATT_DATA
30 BATT_CLK
TH
PESD5V2S2UT 5.2V 260W SOT23
D3
C12 1000pF 50V 5% 0402 NPO_NU
C11 1000pF 50V 5% 0402 NPO_NU
C13 1000pF 50V 10% 0402 X7R
CN12
BATT BP-2000450-0060160328 SU YIN
6012B035701
INVENTEC
TITLE
Celpalla demo board)
Adapter in/Charge
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
CHANGE by IEC
DATE Monday, May 24, 2010
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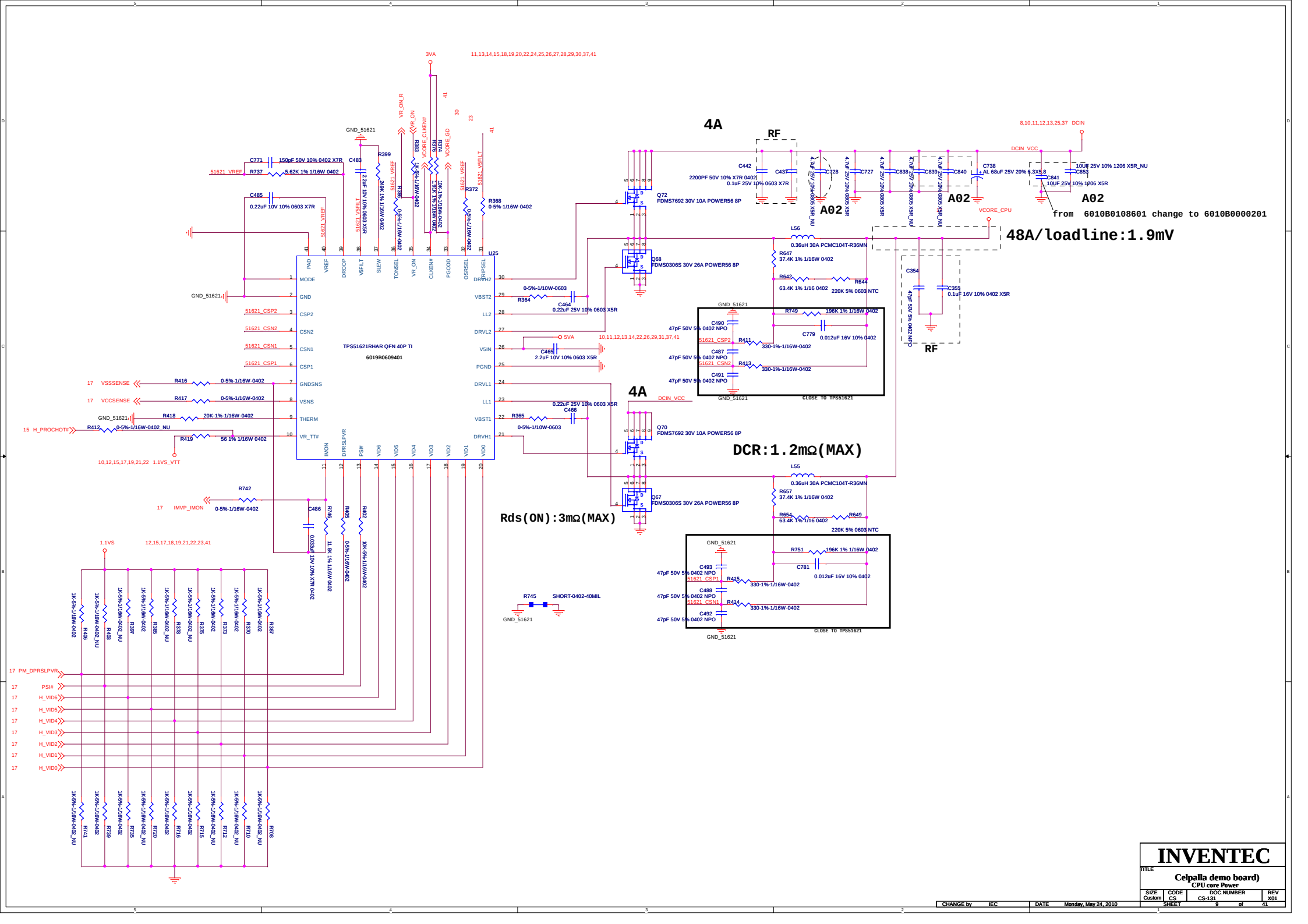
4A
RF
A02
48A/loadline:1.9mV
from 6010B0108601 change to 6010B0000201
4A
DCR:1.2mΩ(MAX)
Rds(ON):3mΩ(MAX)
TPS51621RHAR QFN 40P TI
6019B0609401
Q72 FDMS7692 30V 10A POWER56 8P
Q68 FDMS0306S 30V 26A POWER56 8P
Q70 FDMS7692 30V 10A POWER56 8P
Q67 FDMS0306S 30V 26A POWER56 8P
L56 0.36uH 30A PCMC104T-R36MN
L55 0.36uH 30A PCMC104T-R36MN
CLOSE TO TPS51621
CLOSE TO TPS51621
INVENTEC
Celpalla demo board)
CPU core Power
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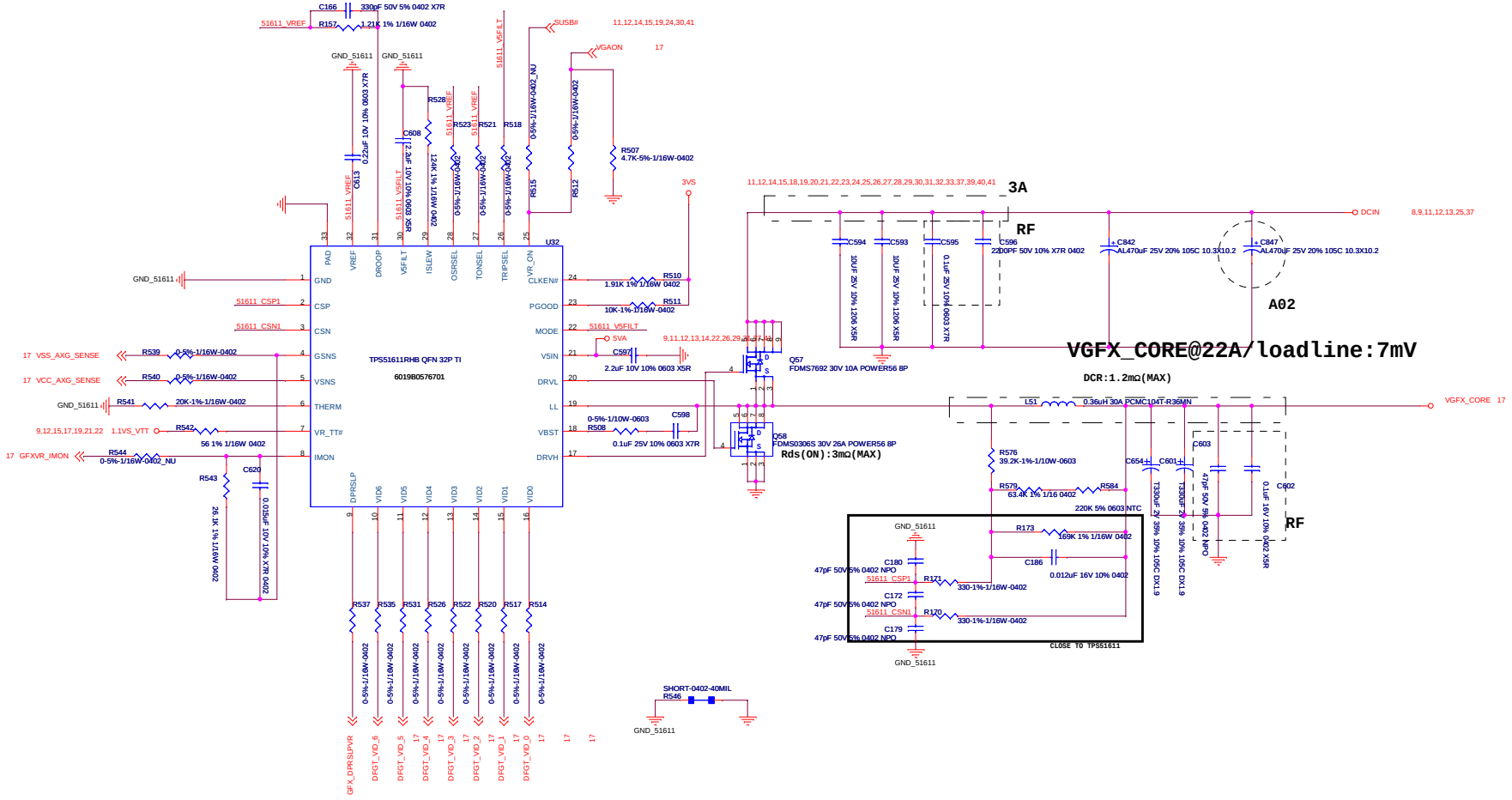

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INVENTEC

TITLE: Celpalla demo board)
VGFX

SIZE	CODE	DOC.NUMBER	REV
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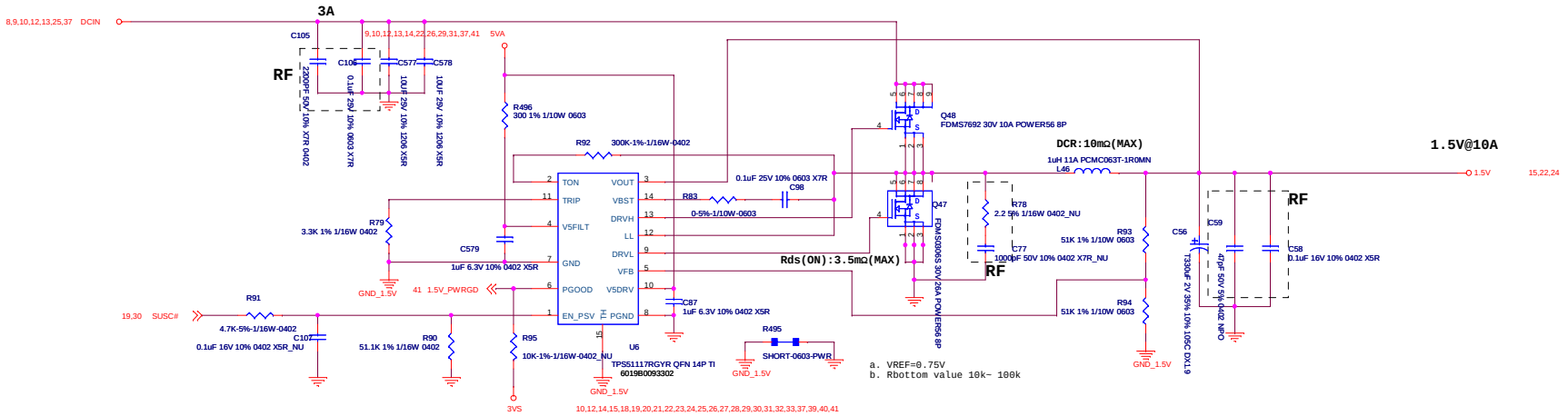
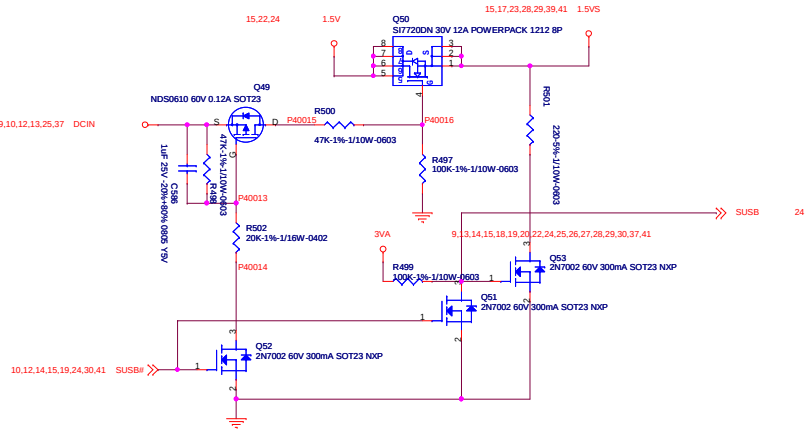
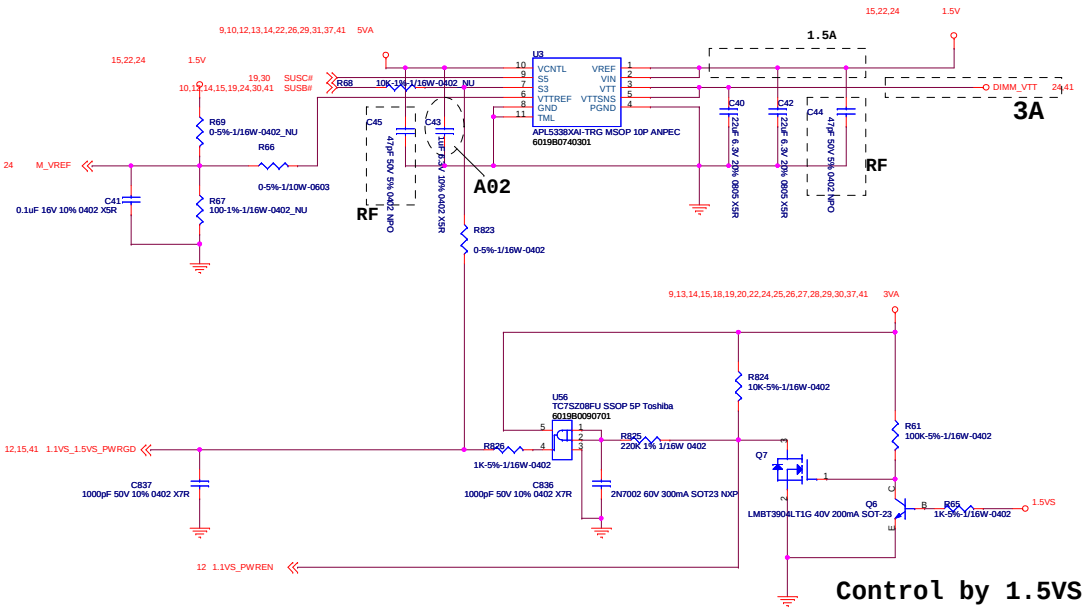
DDR POWER







INVENTEC			
TITLE: Celpalla demo board) DDR PWR			
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01
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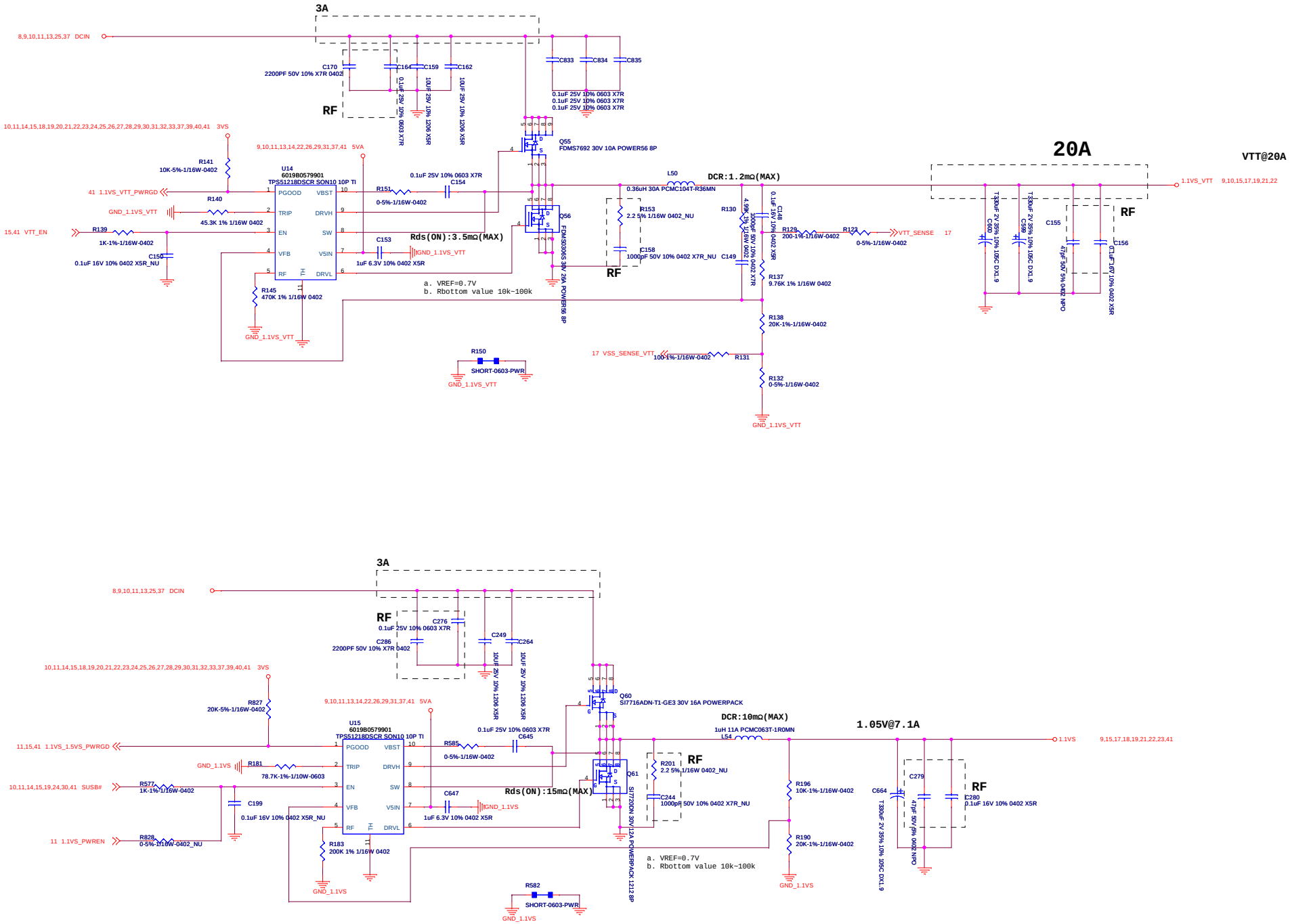

INVENTEC

TITLE: Celpalla demo board)
1.1VS_VTT/1.1VS

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

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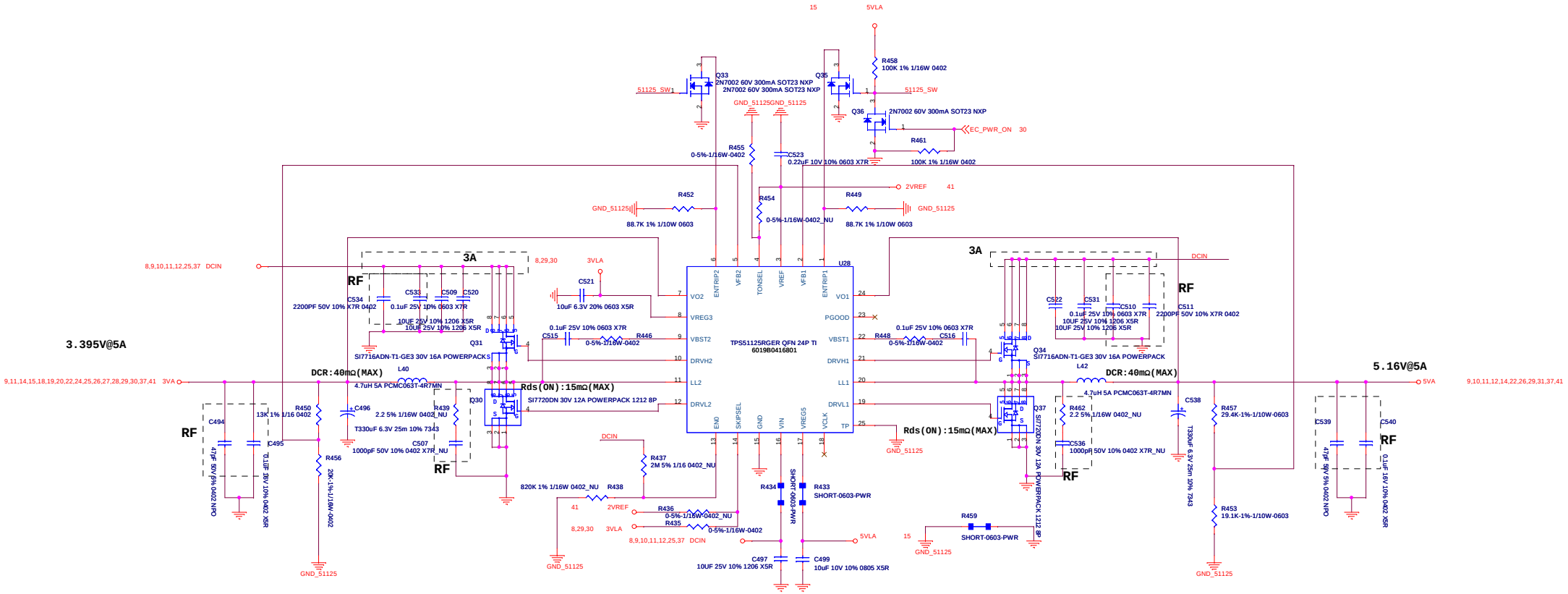

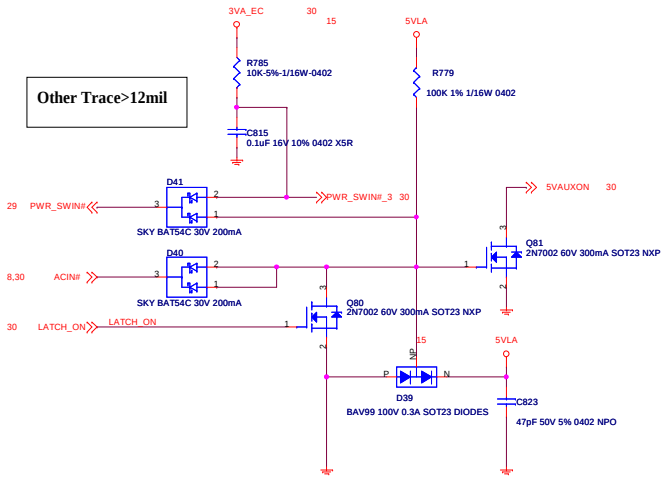

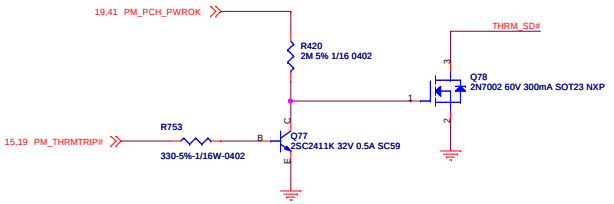

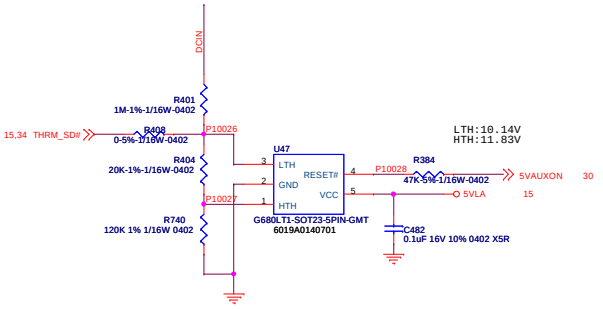

INVENTEC					
TITLE: Celpalla demo board) 5VA/5VLA/3VA/3VLA					
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01		
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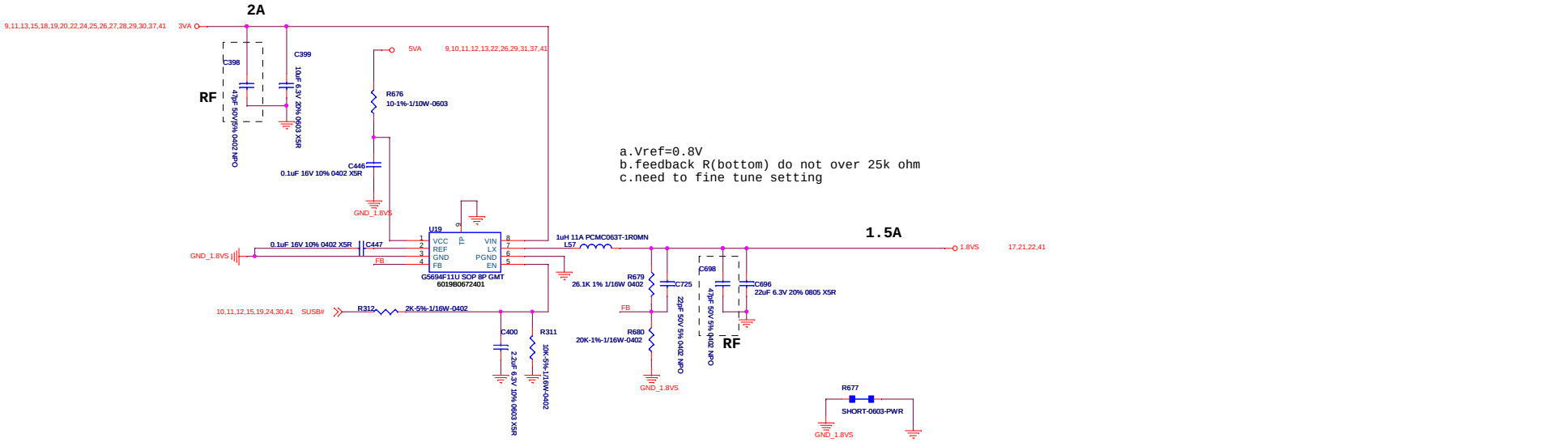
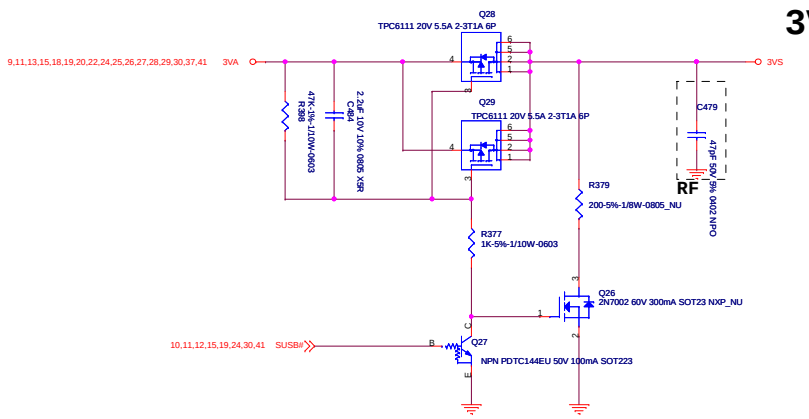
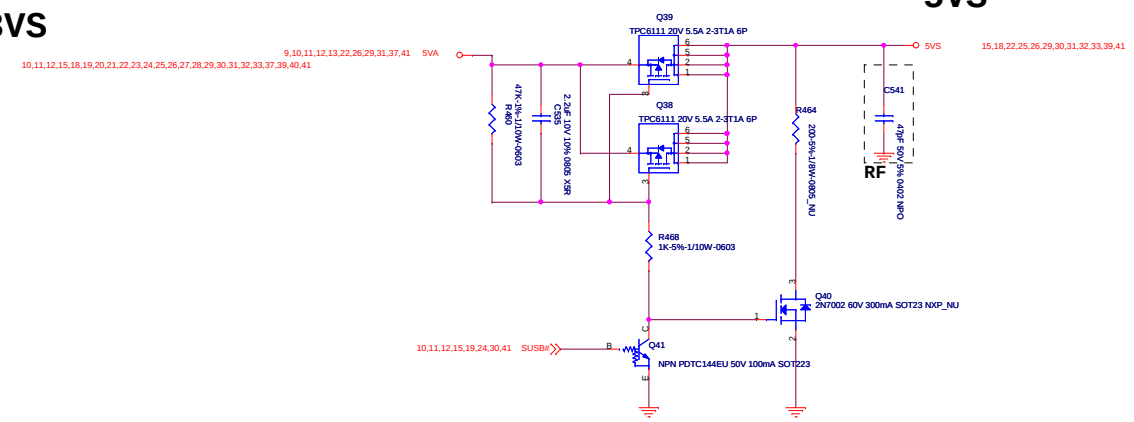


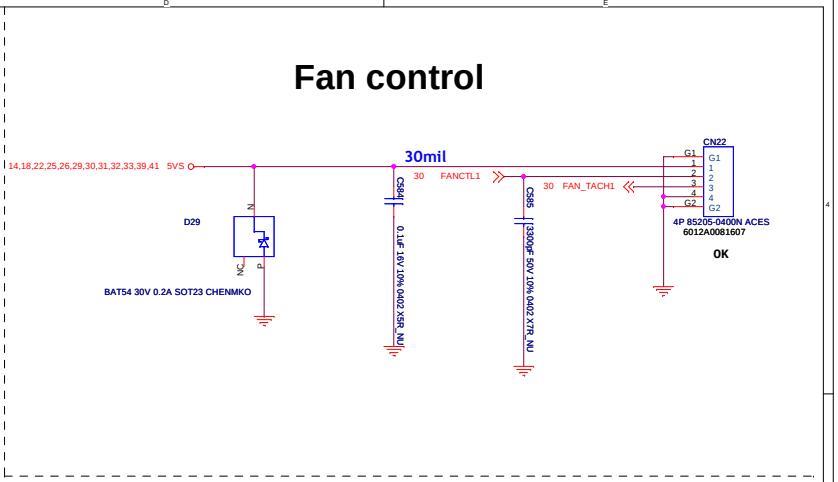
a.Vref=0.8V
b.feedback R(bottom) do not over 25k ohm
c.need to fine tune setting

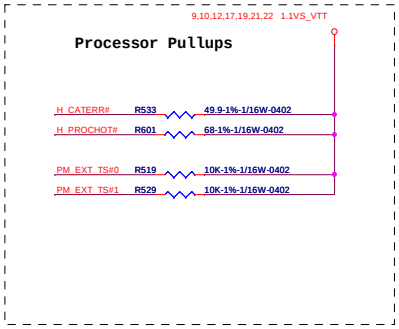


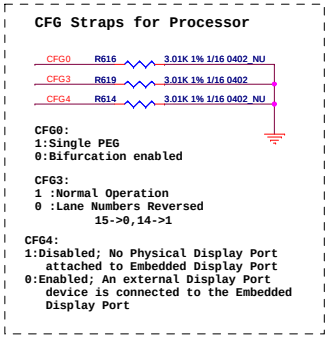


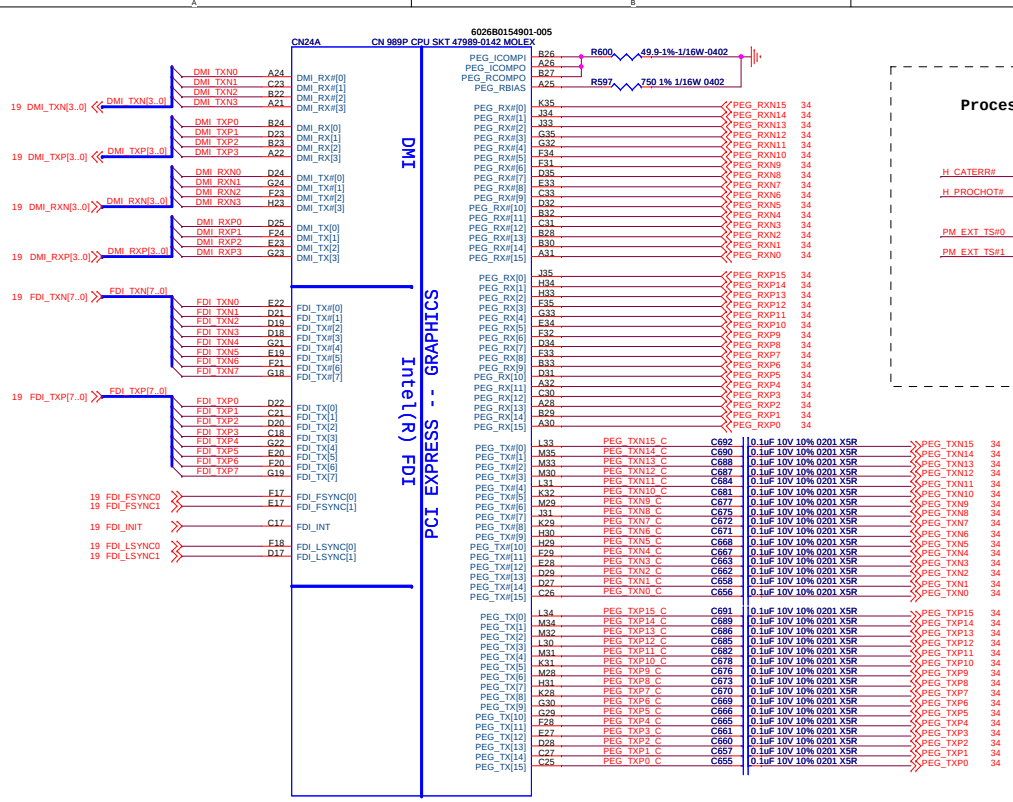
INVENTEC			
TITLE: Celpalla demo board) 3VS/5VS/1.8VS/3VM			
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01
CHANGE by: IEC	DATE: Monday, May 24, 2010	SHEET: 14 of 41	

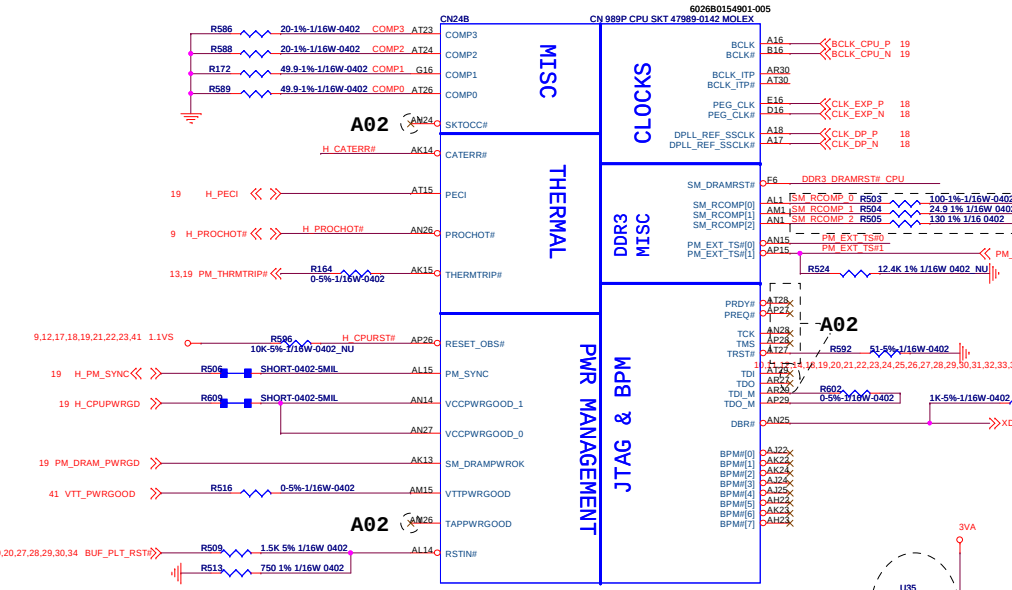
Fan control

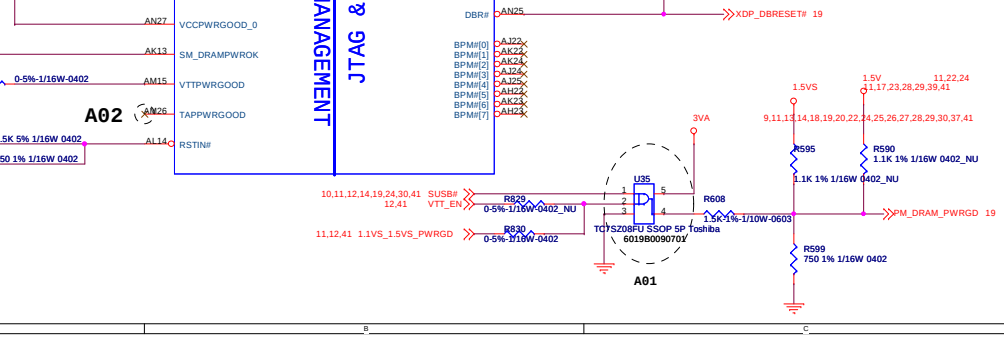


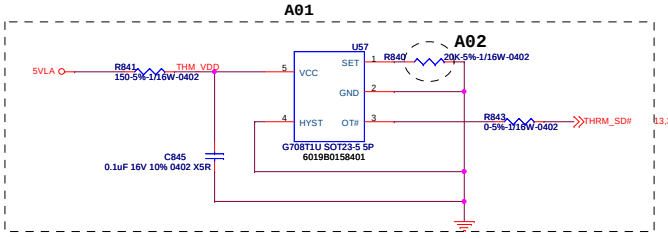


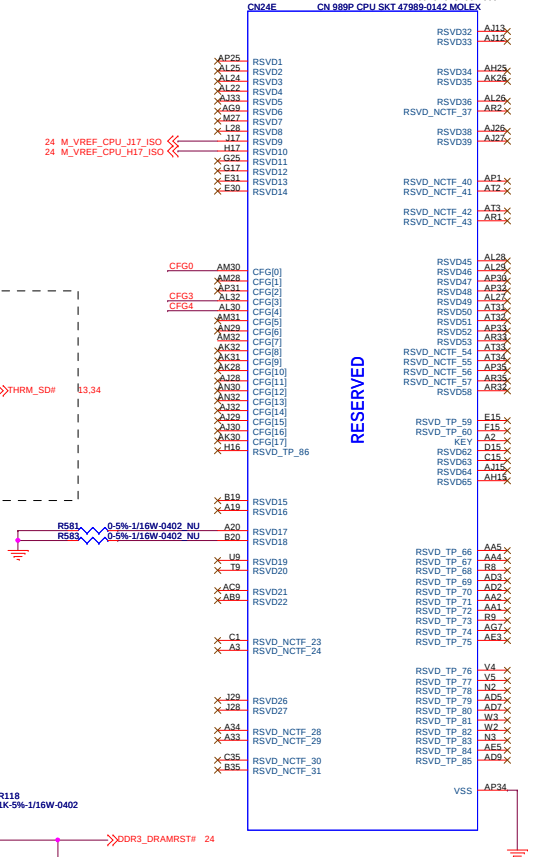


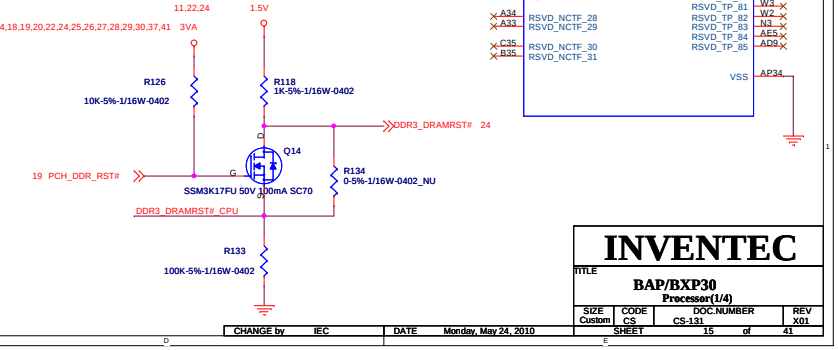










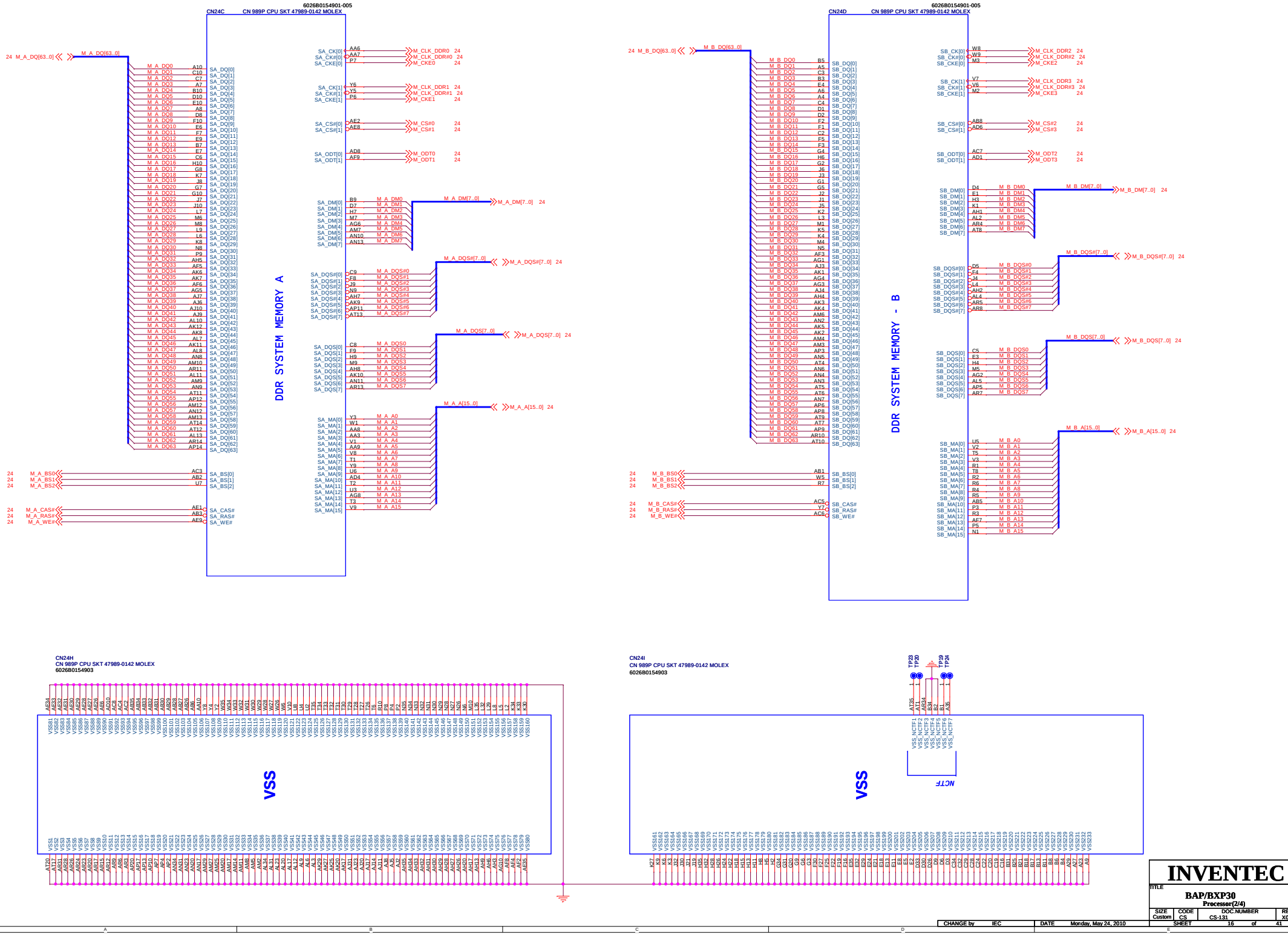


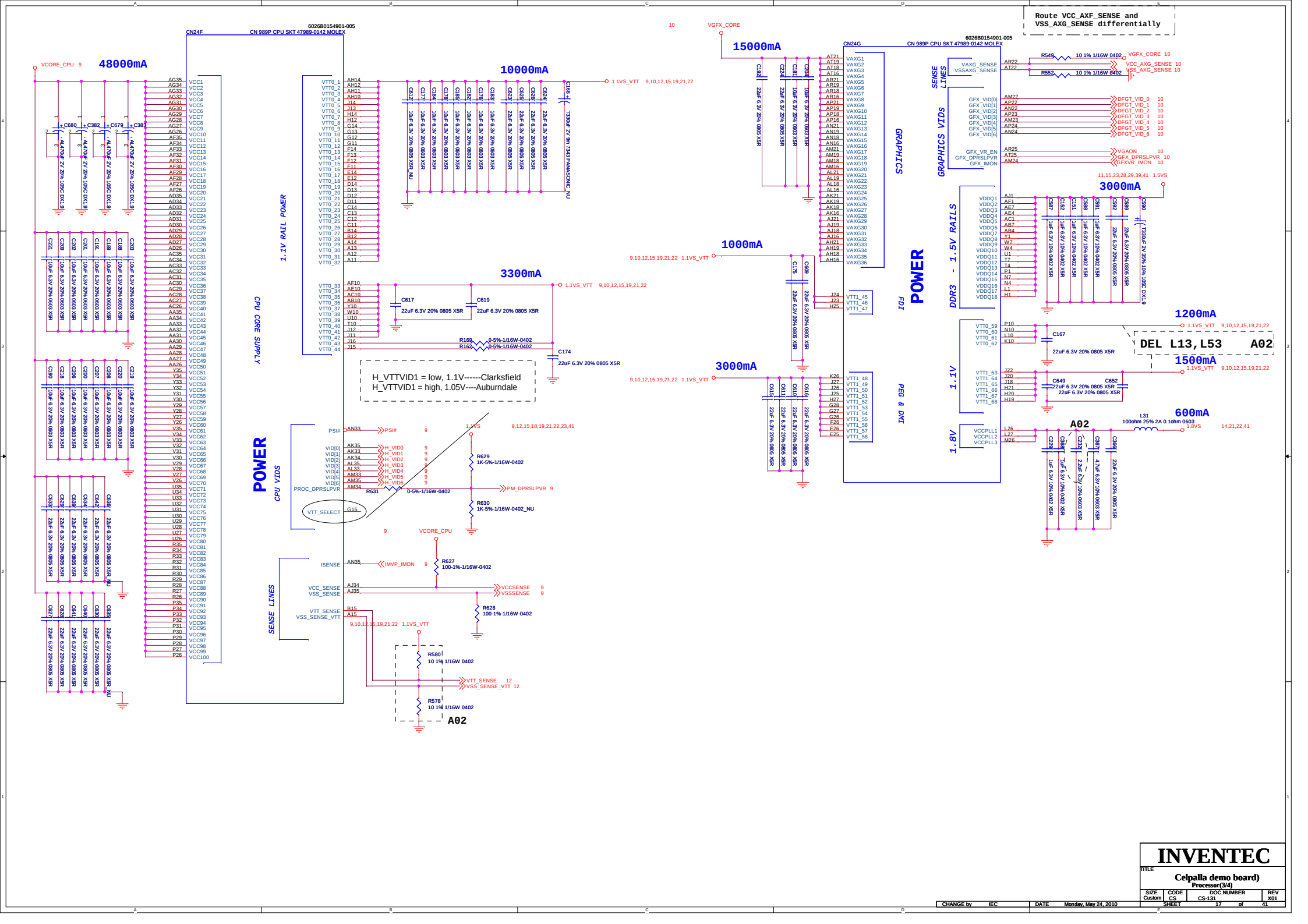
INVENTEC

TITLE: BAP/BXP30
Processor(1/4)

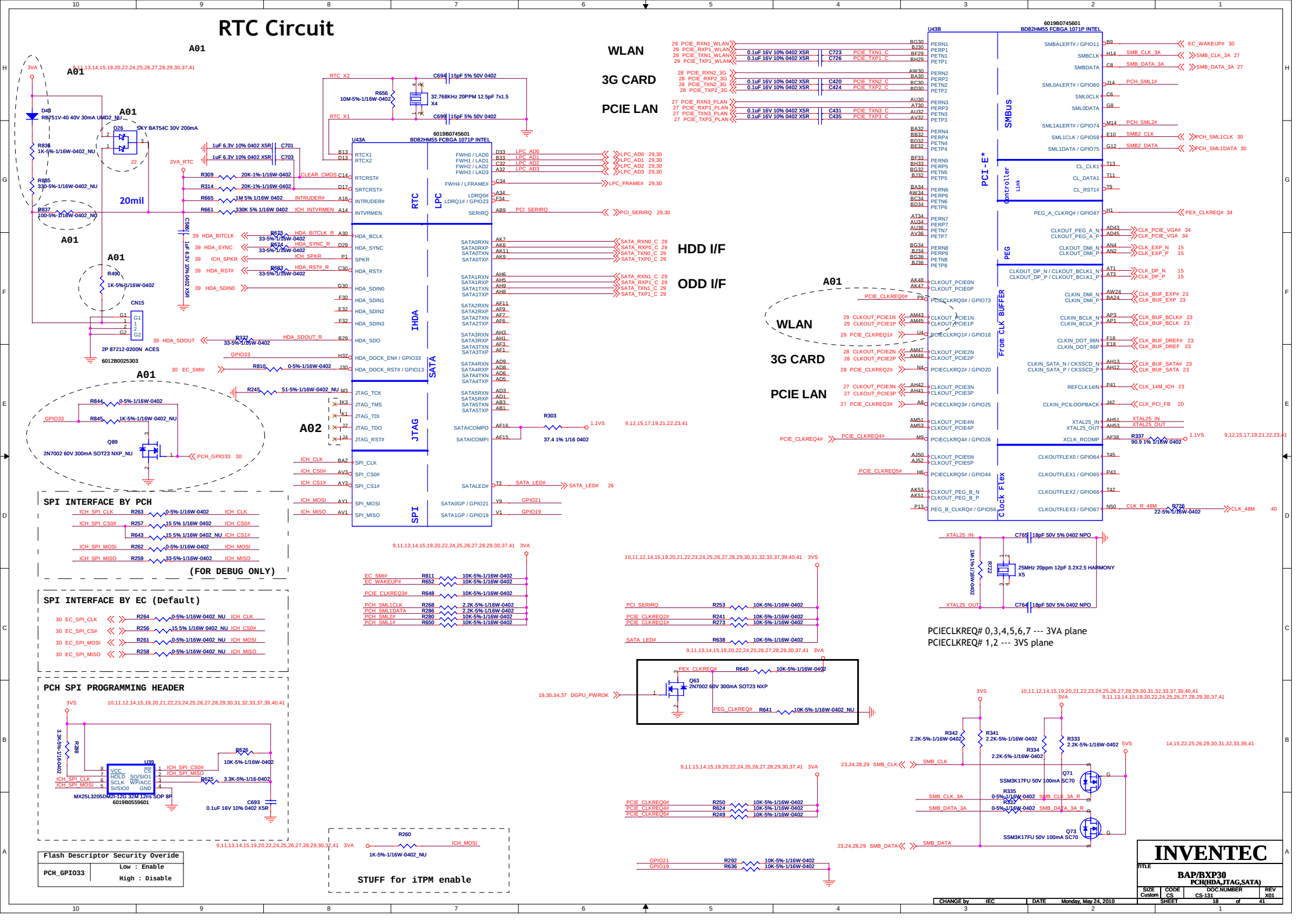
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

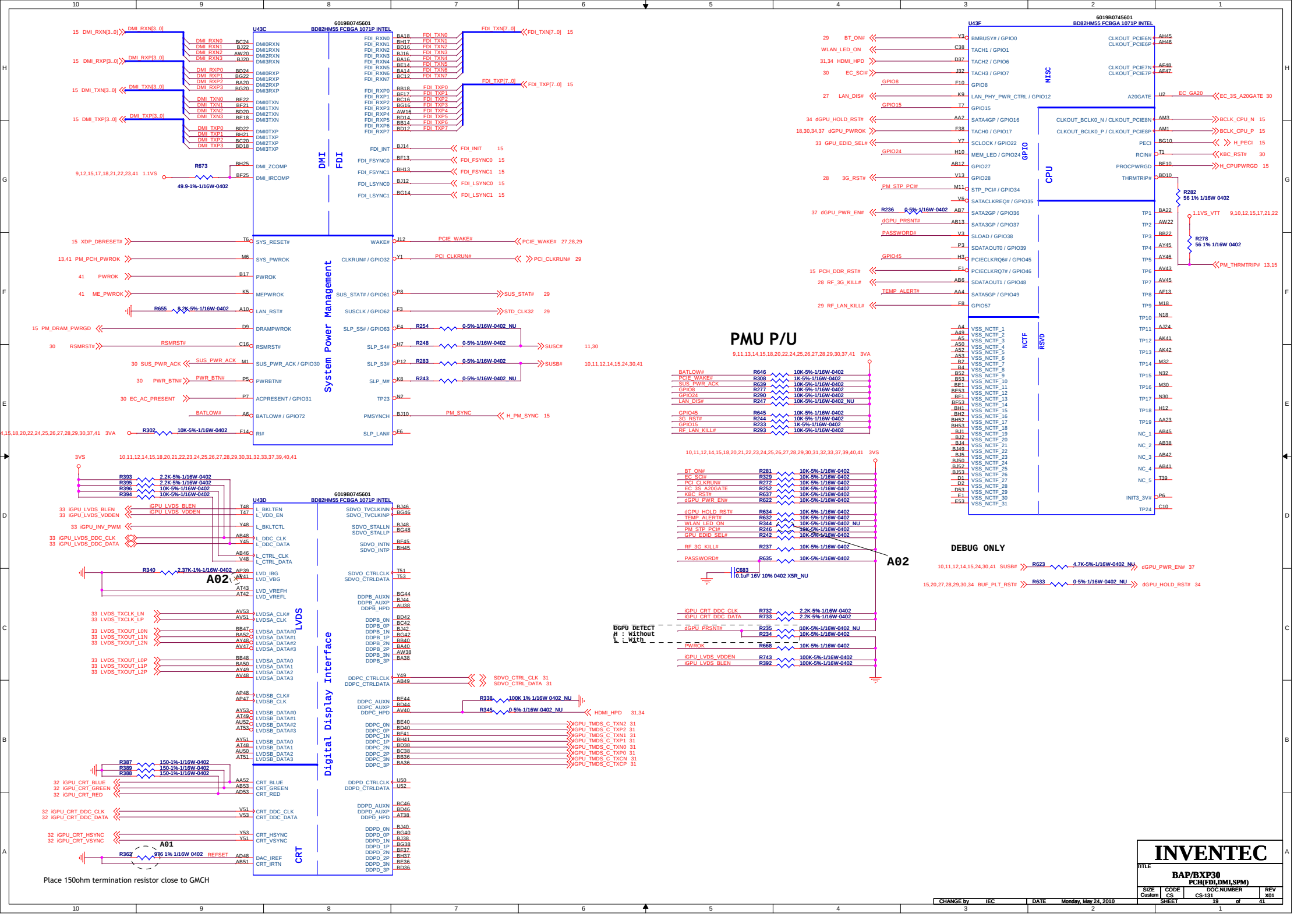
CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 15 of 41

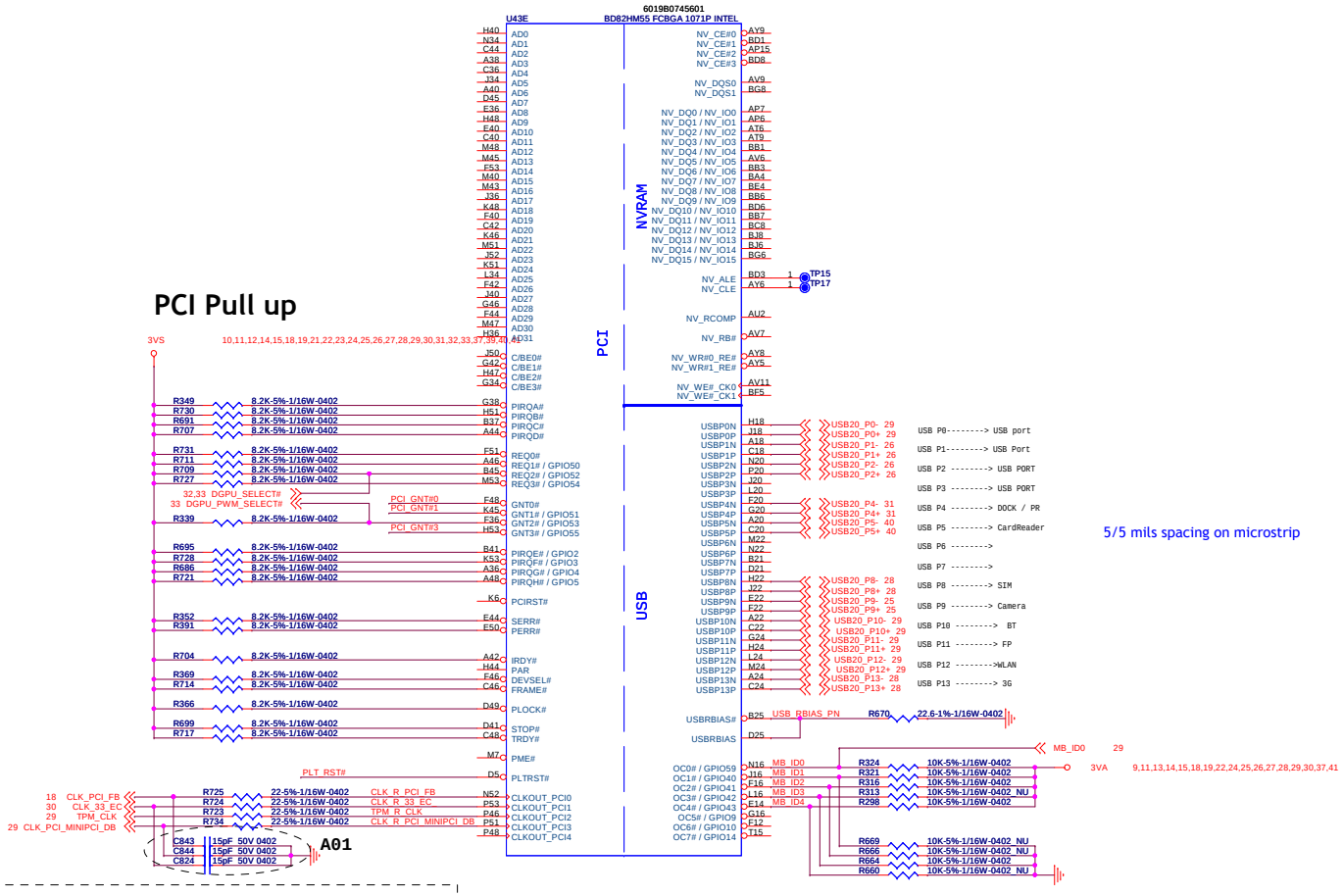

6026B0154901-005
CN24C
CN 989P CPU SKT 47989-0142 MOLEX
DDR SYSTEM MEMORY A
6026B0154901-005
CN24D
CN 989P CPU SKT 47989-0142 MOLEX
DDR SYSTEM MEMORY - B
CN24H
CN 989P CPU SKT 47989-0142 MOLEX
6026B0154903
VSS
CN24I
CN 989P CPU SKT 47989-0142 MOLEX
6026B0154903
VSS
NCTF
INVENTEC
BAP/BXP30
Processor(2/4)
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
SHEET 16 of 41
CHANGE by IEC
DATE Monday, May 24, 2010


Route VCC_AXF_SENSE and VSS_AXG_SENSE differentially
POWER
CPU VIDS
CPU CORE SUPPLY
1.1V RAIL POWER
SENSE LINES
GRAPHICS VIDS
DDR3 - 1.5V RAILS
1.1V
1.8V
FDI
PEG & DMI
GRAPHICS
48000mA
15000mA
10000mA
3300mA
1000mA
3000mA
1200mA
1500mA
600mA
CN24F
CN24G
6026B0154901-005
CN 989P CPU SKT 47989-0142 MOLEX
H_VTTVID1 = low, 1.1V------Clarksfield
H_VTTVID1 = high, 1.05V----Auburndale
DEL L13,L53 A02
A02

RTC Circuit


A01
A02
WLAN
3G CARD
PCIE LAN
HDD I/F
ODD I/F
RTC
LPC
IHDA
SATA
JTAG
SPI
SMBus
PCI-E*
Controller
Link
PEG
From CLK BUFFER
Clock Flex
U43A
BD82HM55 FCBGA 1071P INTEL
6019B0745601
6019B0559601
SPI INTERFACE BY PCH
(FOR DEBUG ONLY)
SPI INTERFACE BY EC (Default)
PCH SPI PROGRAMMING HEADER
MX25L3205DM2I-12G 32M 12ns SOP 8P
Flash Descriptor Security Overide
PCH_GPIO33
Low : Enable
High : Disable
STUFF for iTPM enable
PCIECLKREQ# 0,3,4,5,6,7 --- 3VA plane
PCIECLKREQ# 1,2 --- 3VS plane
INVENTEC
BAP/BXP30
PCH(HDA,JTAG,SATA)
Monday, May 24, 2010


U43C
6019B0745601
BD82HM55 FCBGA 1071P INTEL
DMI
FDI
System Power Management
U43D
LVDS
Digital Display Interface
CRT
U43F
CPU
GPIO
MISC
NCTF
RSVD
PMU P/U
A02
A01
DEBUG ONLY
DGPU DETECT
H : Without
L : With
Place 150ohm termination resistor close to GMCH
INVENTEC
BAP/BXP30
PCH(FDI,DMI,SPM)
CHANGE by IEC
DATE Monday, May 24, 2010
SHEET 19 of 41



BIOS ID setting

Project	MB_ID4	MB_ID3	MB_ID2	MB_ID1	MB_ID0
BAP10 (UMA)	1	1	1	1	1
BXP10 (UMA)	1	1	1	1	0
BAP30 (UMA)	1	1	1	0	1
BXP30 (UMA)	1	1	1	0	0
BAD50 (UMA)	1	1	0	1	1
BXD50 (UMA)	1	1	0	1	0
SJM40 (UMA)	1	1	0	0	1
SJM40 (dGPU)	1	1	0	0	0
BAP30 (dGPU)	1	0	1	1	1
BXP30 (dGPU)	1	0	1	1	0
BAD50 (dGPU)	1	0	1	0	1
BXD50 (dGPU)	1	0	1	0	0
SJM40 (dGPU optimus)	1	0	0	1	1
BAP30 (dGPU optimus)	1	0	0	0	1
BXP30 (dGPU optimus)	1	0	0	0	0

INVENTEC

TITLE: BAP/BXP30
PCH(USB, PCI)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

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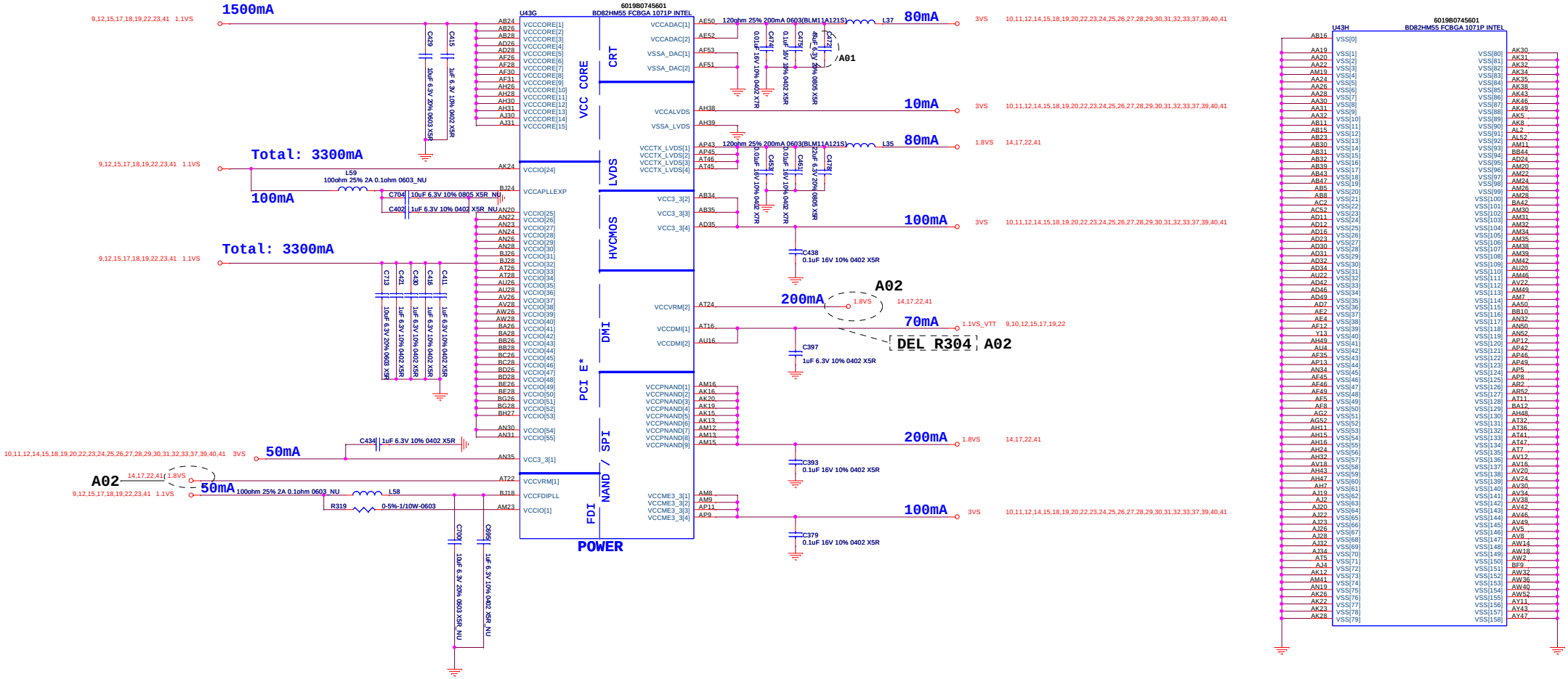
CHANGE by IEC DATE Monday, May 24, 2010

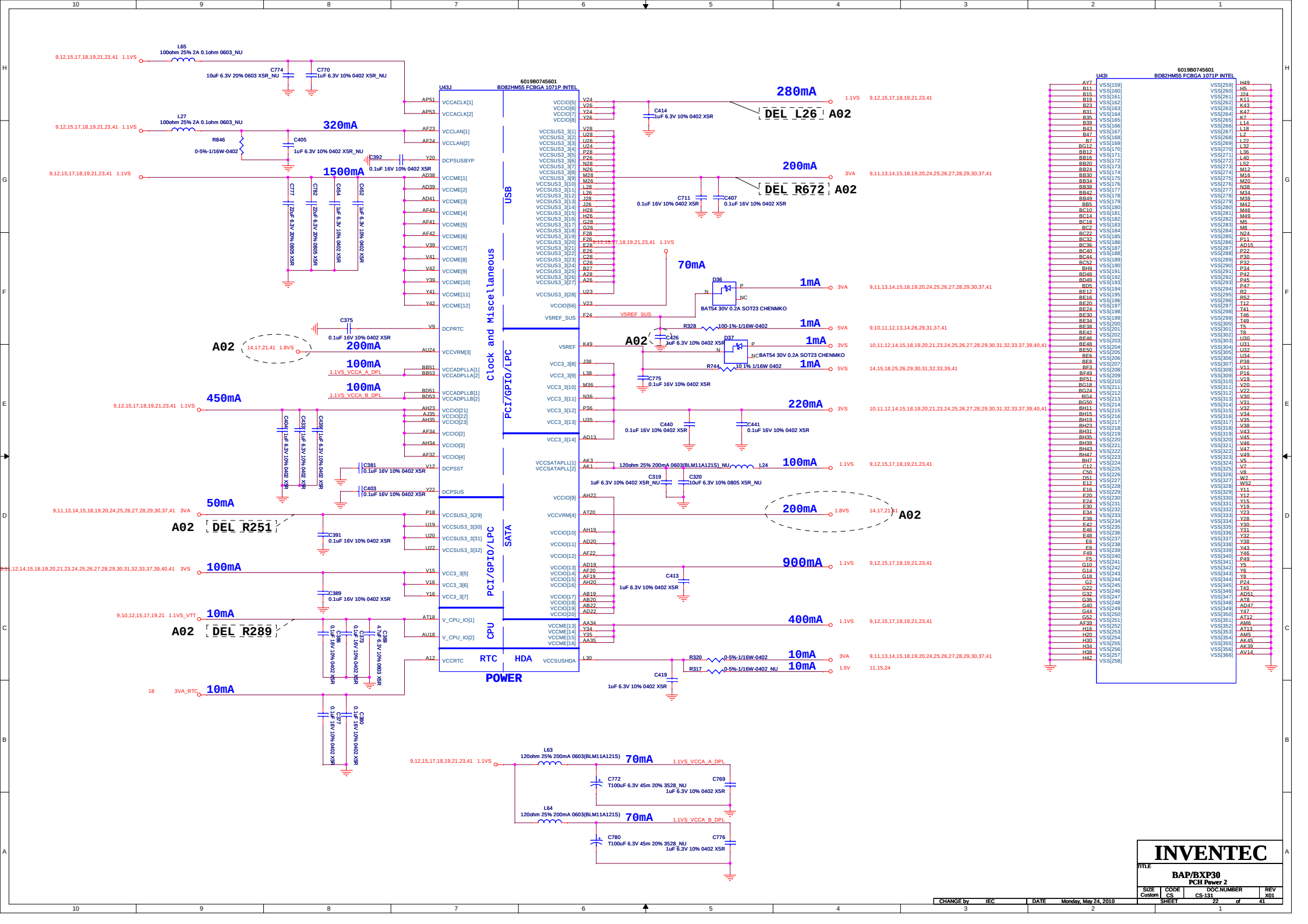


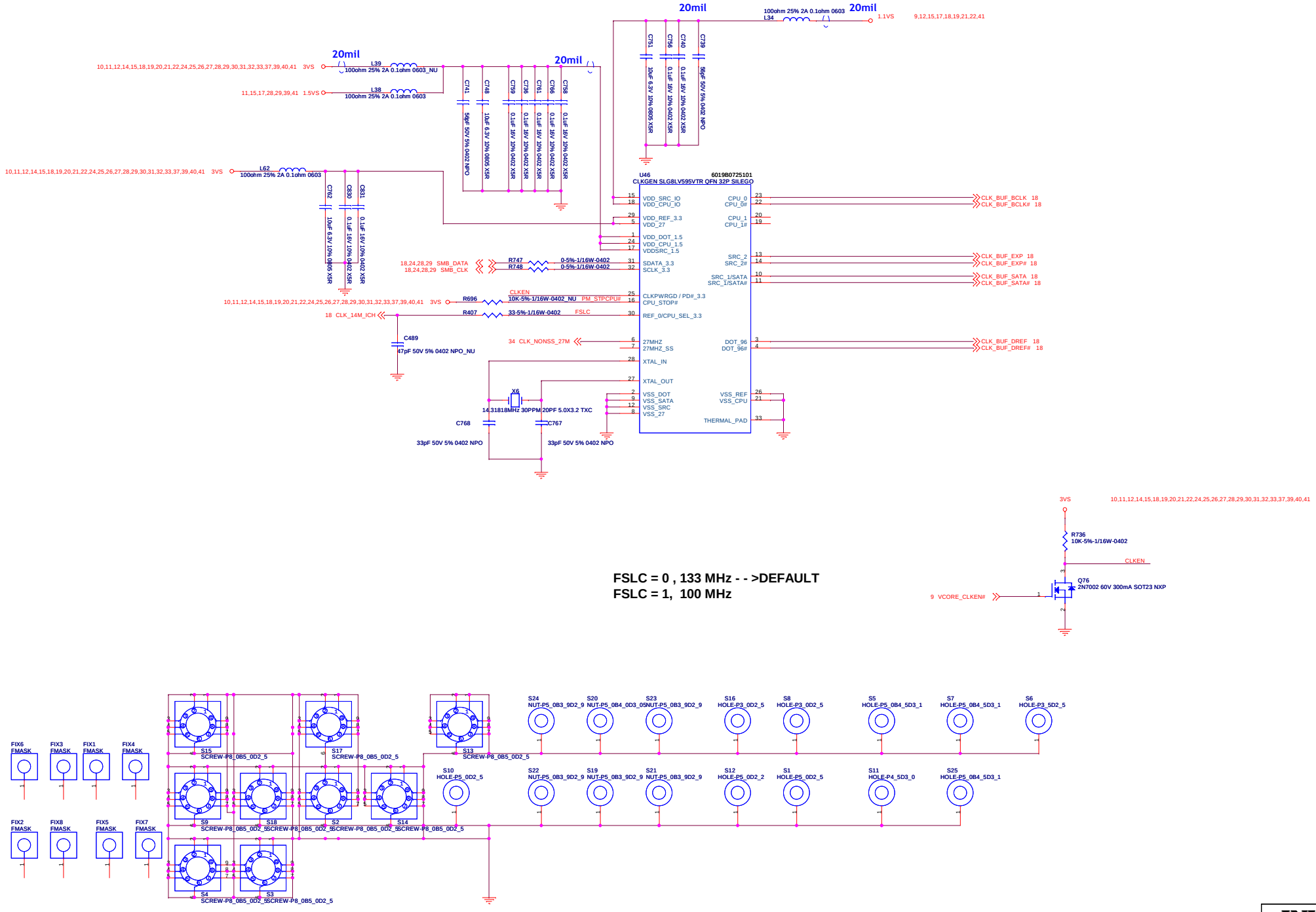
CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

TITLE: **BAP/BXP30**
PCH Power 1

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01
		SHEET 21 of 41	


U43J
6019B0745601
BD82HM55 FCBGA 1071P INTEL
U43I
6019B0745601
BD82HM55 FCBGA 1071P INTEL
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
POWER
L65
100ohm 25% 2A 0.1ohm 0603_NU
L27
100ohm 25% 2A 0.1ohm 0603_NU
L63
120ohm 25% 200mA 0603(BLM11A121S)
L64
120ohm 25% 200mA 0603(BLM11A121S)
120ohm 25% 200mA 0603(BLM11A121S)_NU
280mA
DEL L26 A02
200mA
DEL R672 A02
70mA
1mA
BAT54 30V 0.2A SOT23 CHENMKO
1mA
BAT54 30V 0.2A SOT23 CHENMKO
1mA
220mA
100mA
200mA
A02
900mA
400mA
10mA
10mA
320mA
1500mA
200mA
100mA
100mA
450mA
50mA
A02 DEL R251
100mA
10mA
A02 DEL R289
10mA
70mA
70mA
INVENTEC
BAP/BXP30
PCH Power 2
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
SHEET 22 of 41
CHANGE by IEC
DATE Monday, May 24, 2010

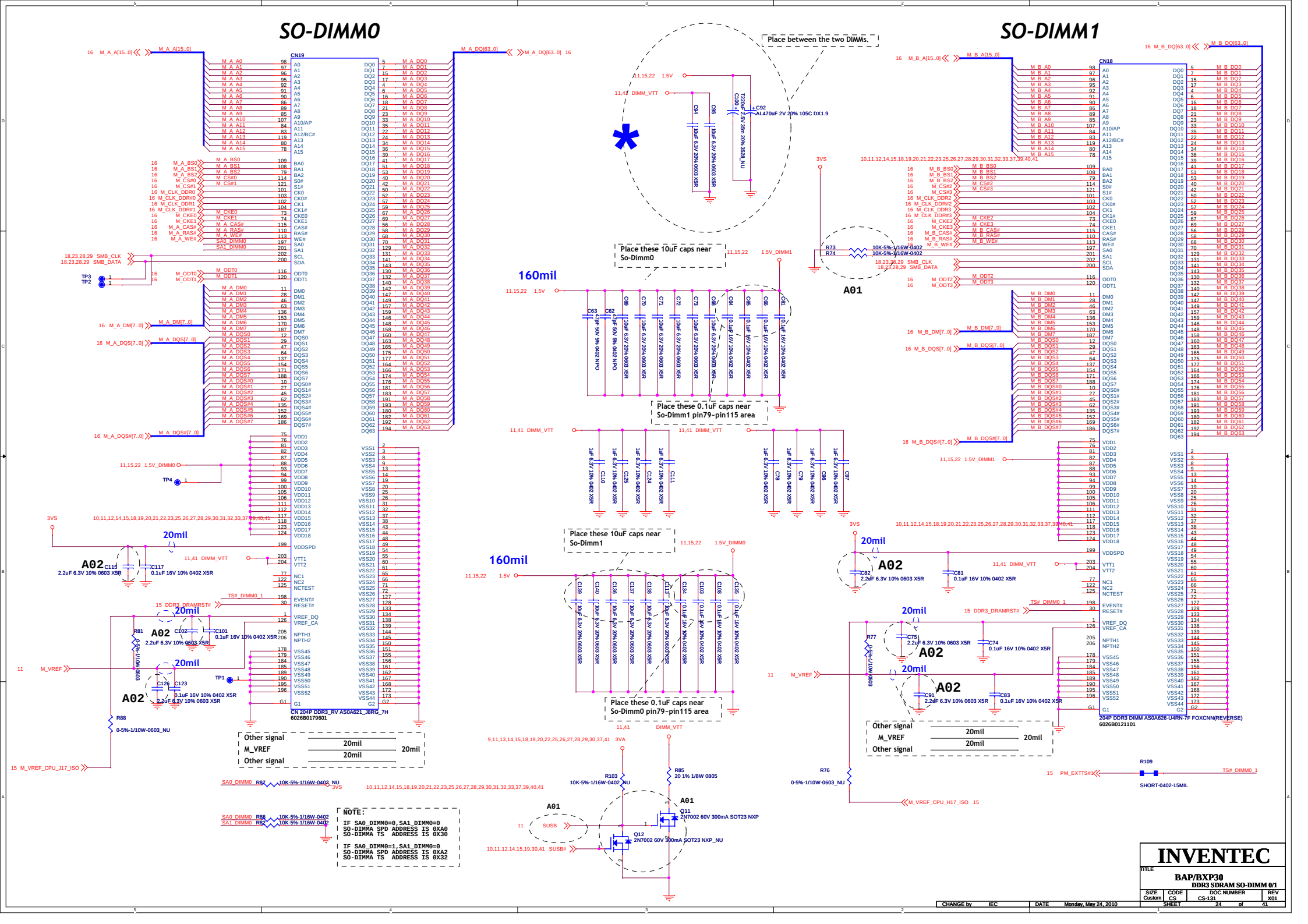


INVENTEC

TITLE: BAP/BXP30
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 23 of 41


SO-DIMM0
SO-DIMM1
Place between the two DIMMs.
Place these 10uF caps near So-Dimm0
Place these 0.1uF caps near So-Dimm1 pin79-pin115 area
Place these 10uF caps near So-Dimm1
Place these 0.1uF caps near So-Dimm0 pin79-pin115 area
160mil
20mil
A01
A02
CN19
CN18
CN 204P DDR3_RV AS0A621_J8RG_7H
6026B0179601
204P DDR3 DIMM AS0A626-U4RN-7F FOXCNN(REVERSE)
6026B0121101
Other signal
M_VREF
Other signal
NOTE:
IF SA0_DIMM0=0,SA1_DIMM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30
IF SA0_DIMM0=1,SA1_DIMM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32
INVENTEC
BAP/BXP30
DDR3 SDRAM SO-DIMM 0/1
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
CHANGE by IEC
DATE Monday, May 24, 2010
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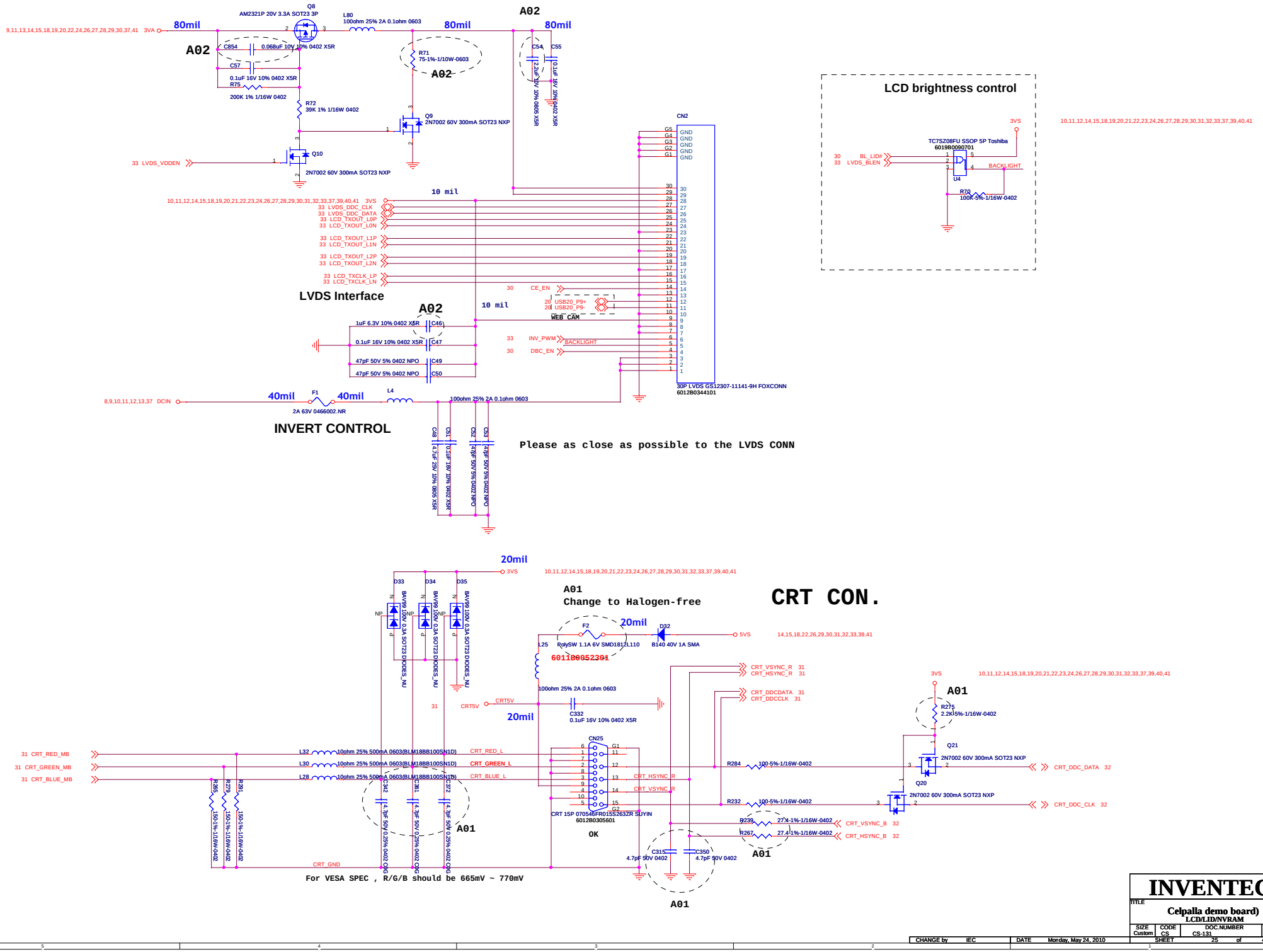
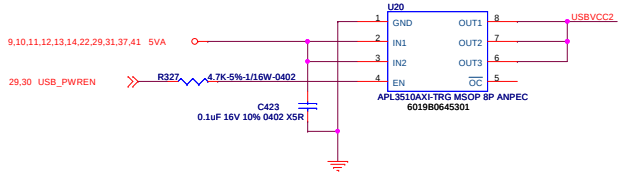
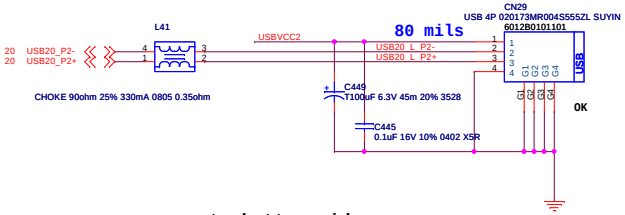
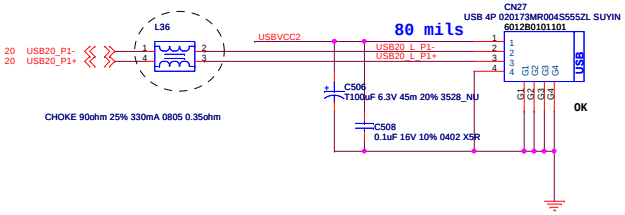

LCD brightness control
LVDS Interface
INVERT CONTROL
Please as close as possible to the LVDS CONN
CRT CON.
A01
Change to Halogen-free
For VESA SPEC , R/G/B should be 665mV ~ 770mV
INVENTEC
Celpalla demo board)
LCD/LID/NVRAM

USB

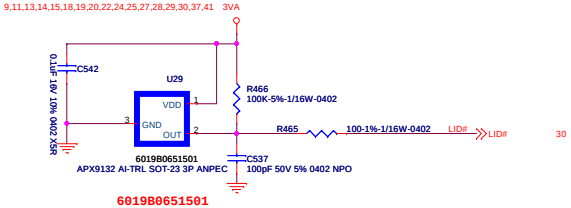


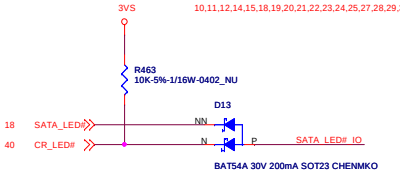


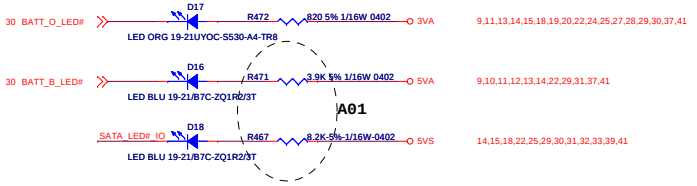
move to bottom side

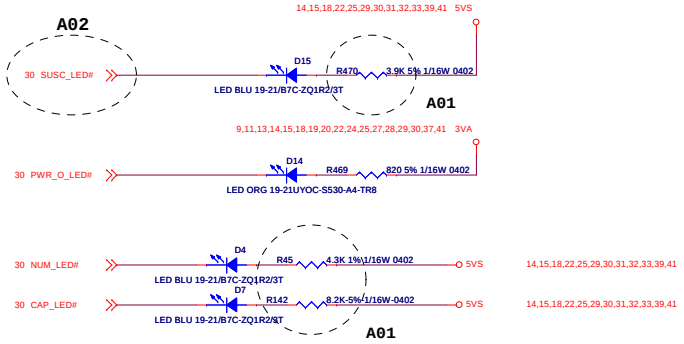


HALL Switch

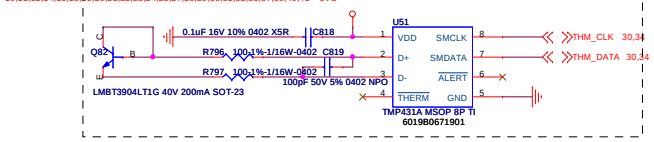








REMOTE thermal sensor
Place near the hottest spot area under Palm-rest

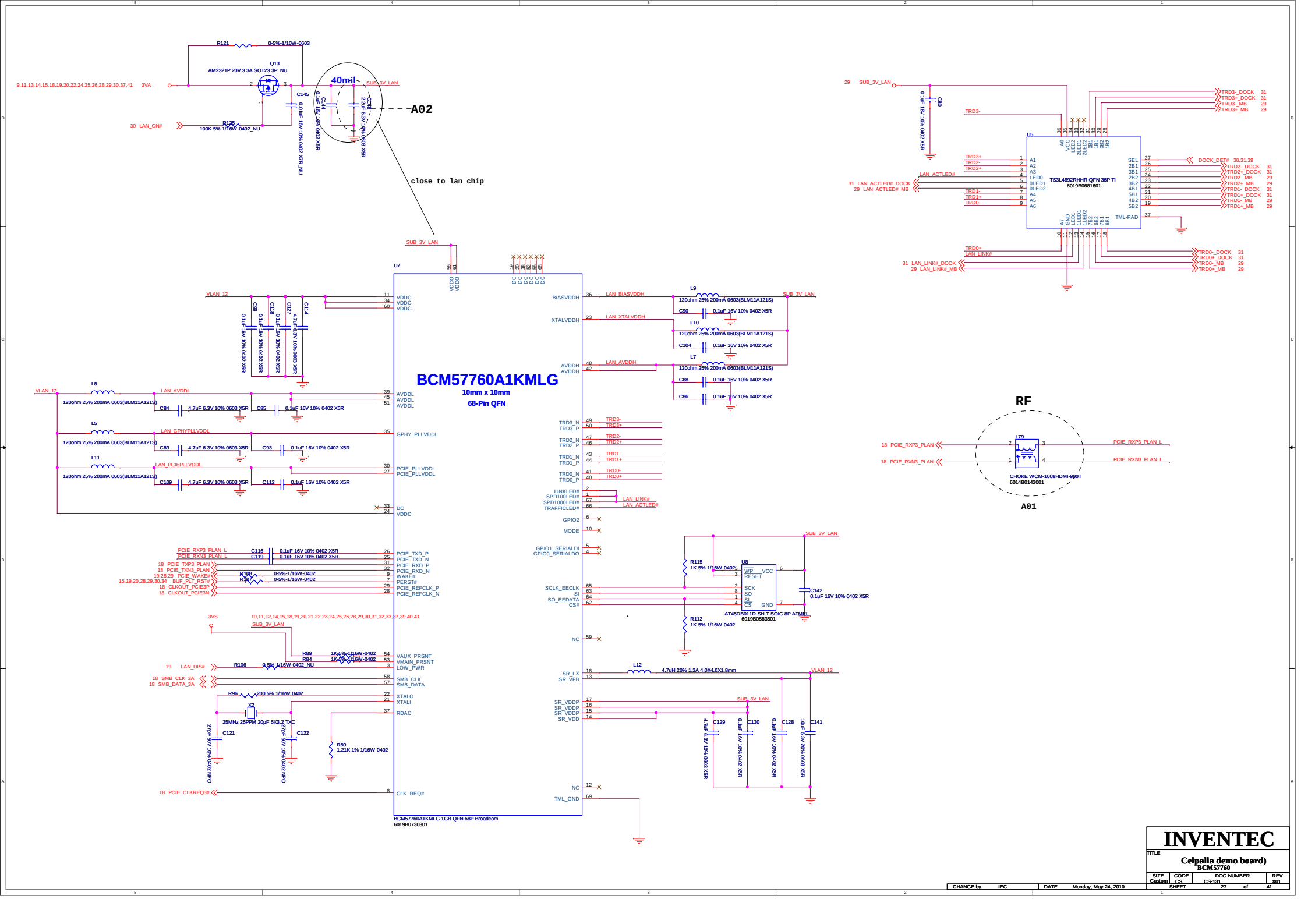


CHANGE by	IEC	DATE	Monday, May 24, 2010	SHEET	26 of 41

INVENTEC

TITLE **BAP/BXP30**
HDD/DAUGHTER CONNECTOR

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01



CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

TITLE: Celpalla demo board)
BCM57760

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

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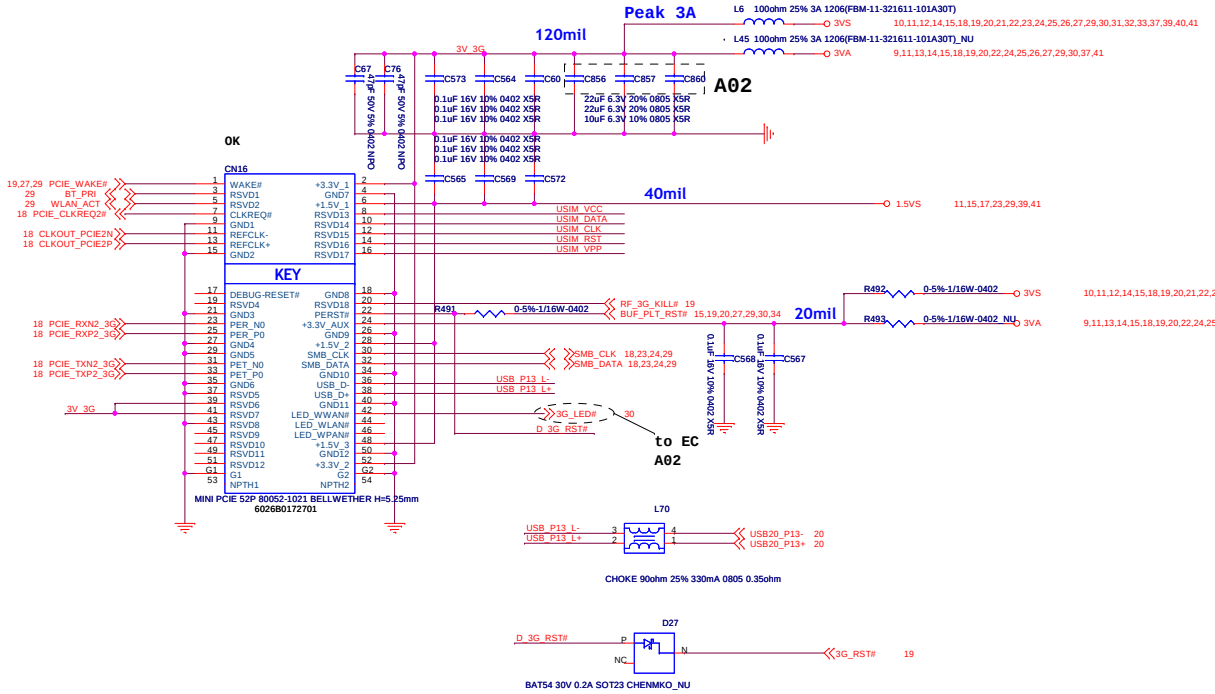
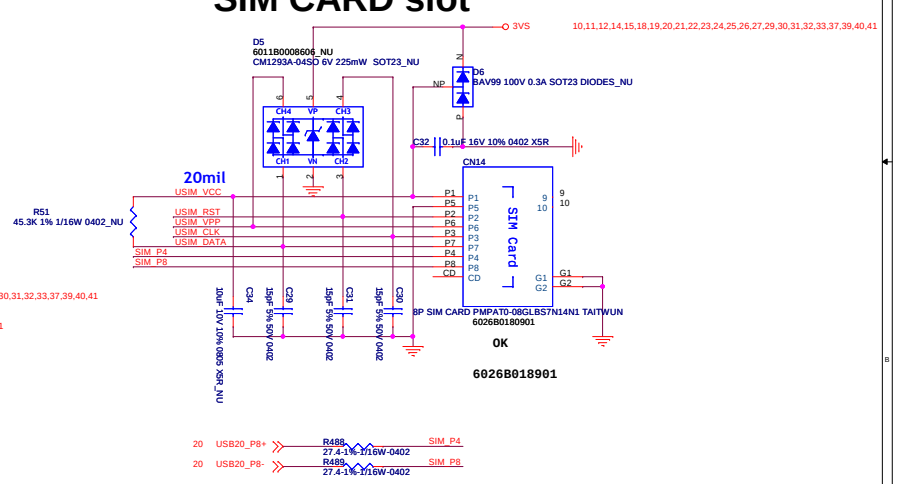
PCIE Mini Card for 3G

On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.



SIM CARD slot



CHANGE by	IEC	DATE	Monday, May 24, 2010		

INVENTEC

TITLE: BAP/BXP30 WLAN/3G

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

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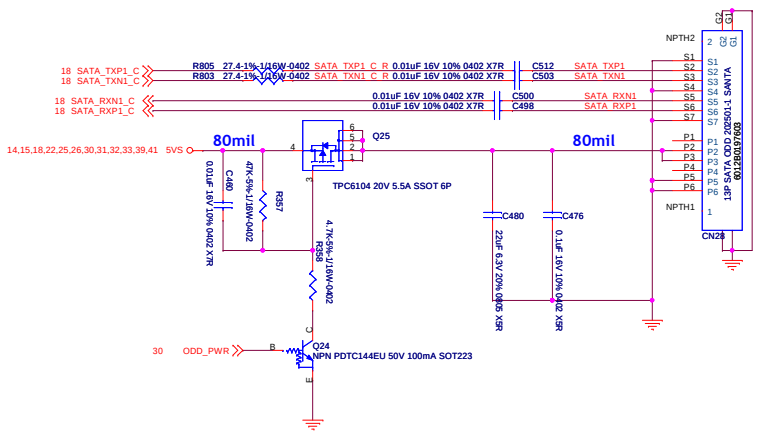
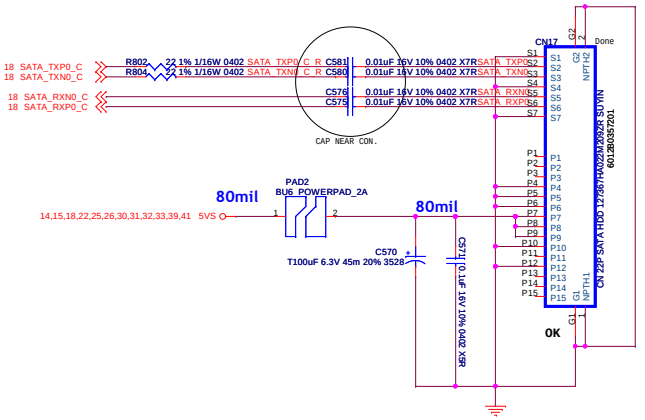
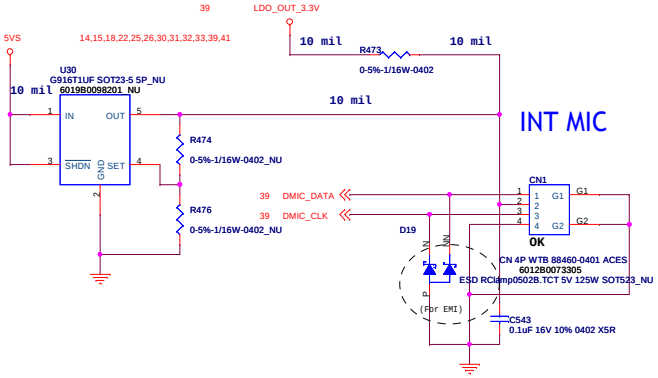
ODD I/F



HDD I/F

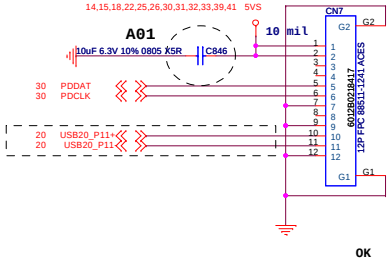


DMIC CNN

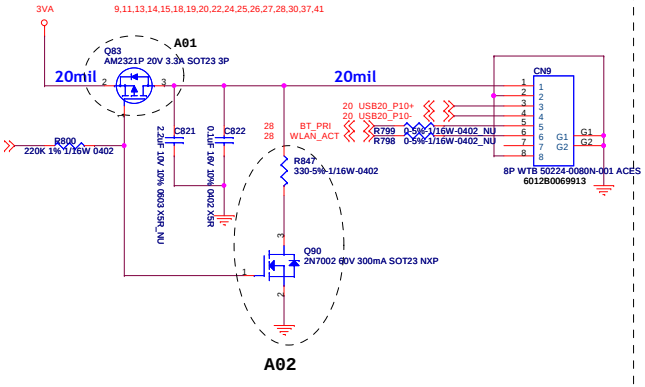


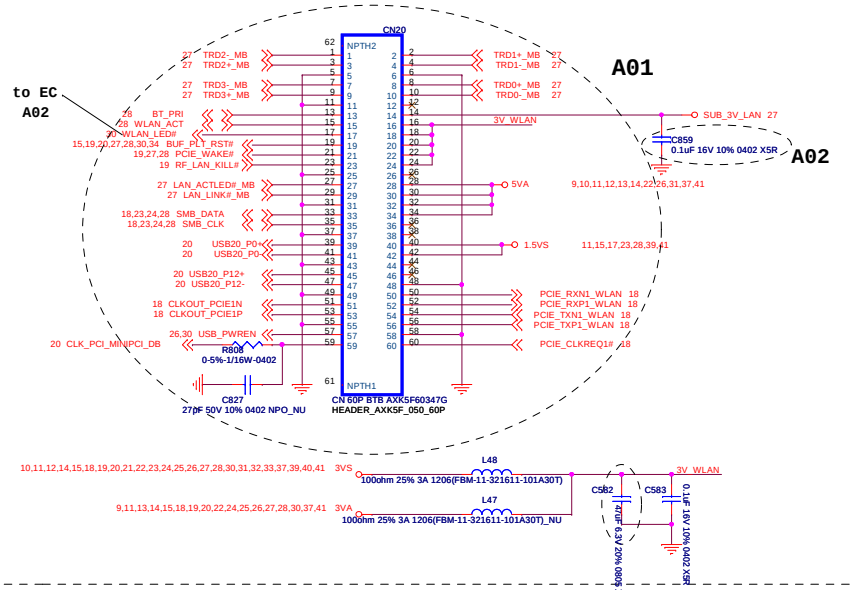
TO USB/WLAN BOARD

GP + FP CNN.

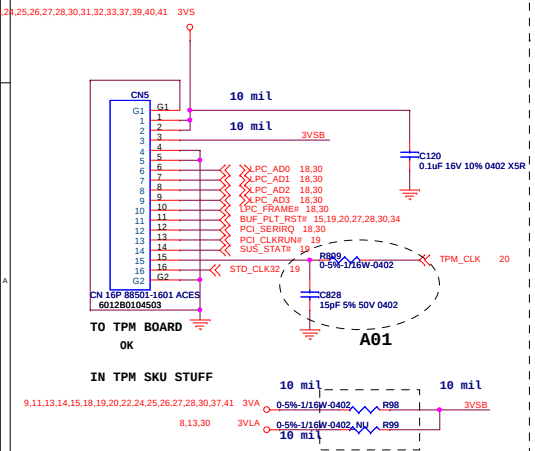


Bluetooth CNN.

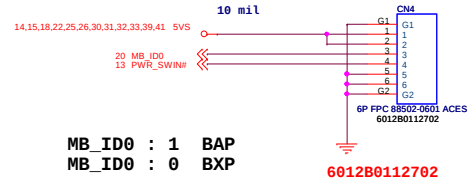




TPM CNN



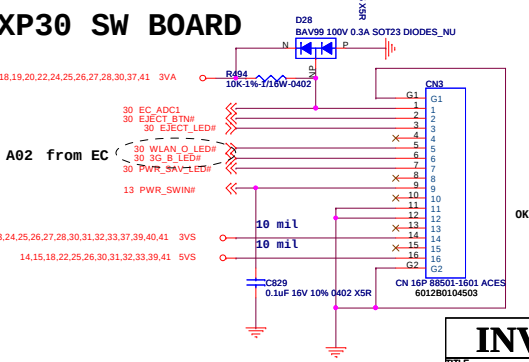
FOR BXP30 POWER BUTTON BOARD



MB_ID0 : 1 BAP
MB_ID0 : 0 BXP

6012B0112702

FOR BAP/BXP30 SW BOARD



CHANGE by	IEC	DATE	Monday, May 24, 2010		

INVENTEC

TITLE: Celpalla demo board)
USB/eSATA/G-sensor/CON

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

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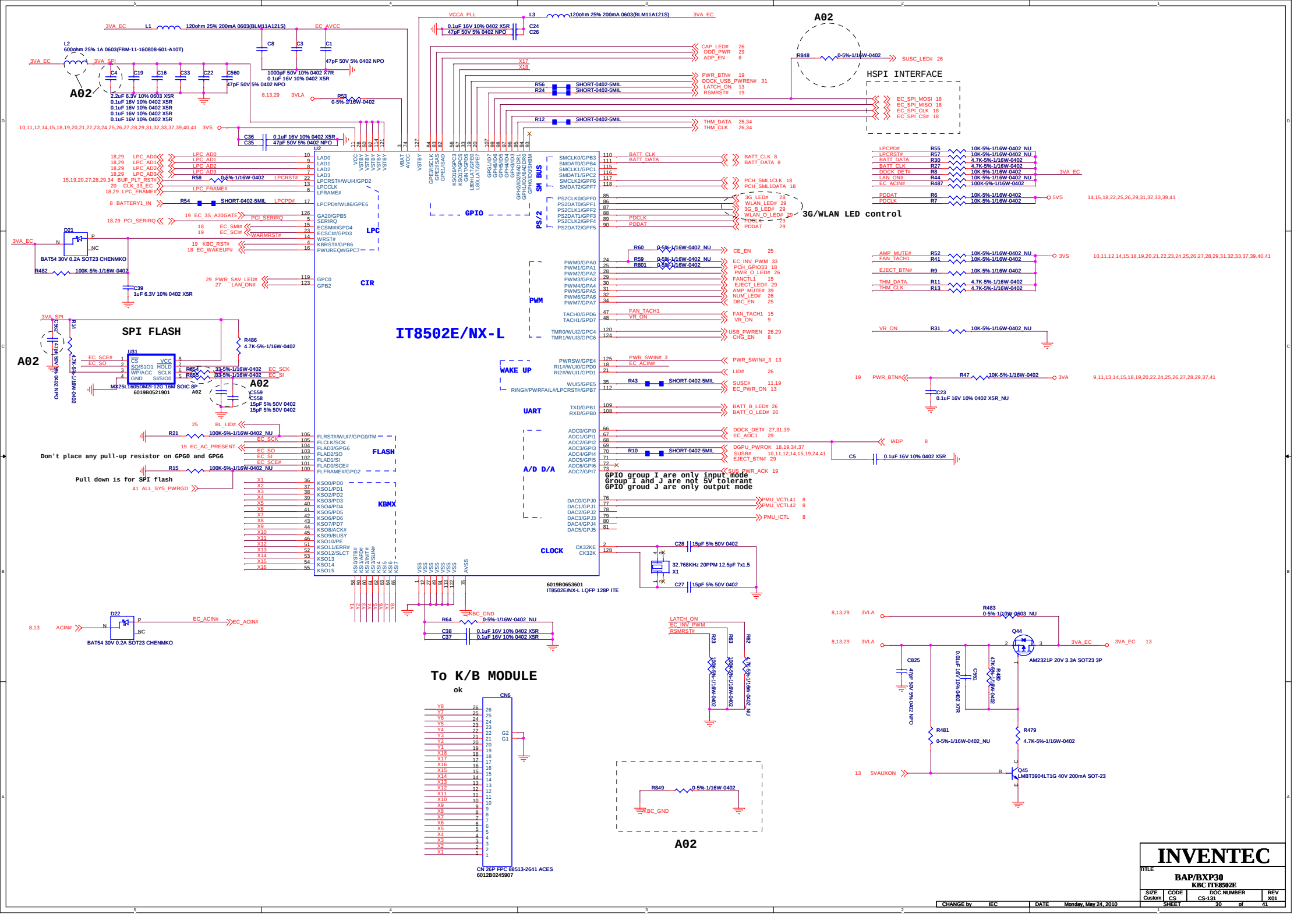
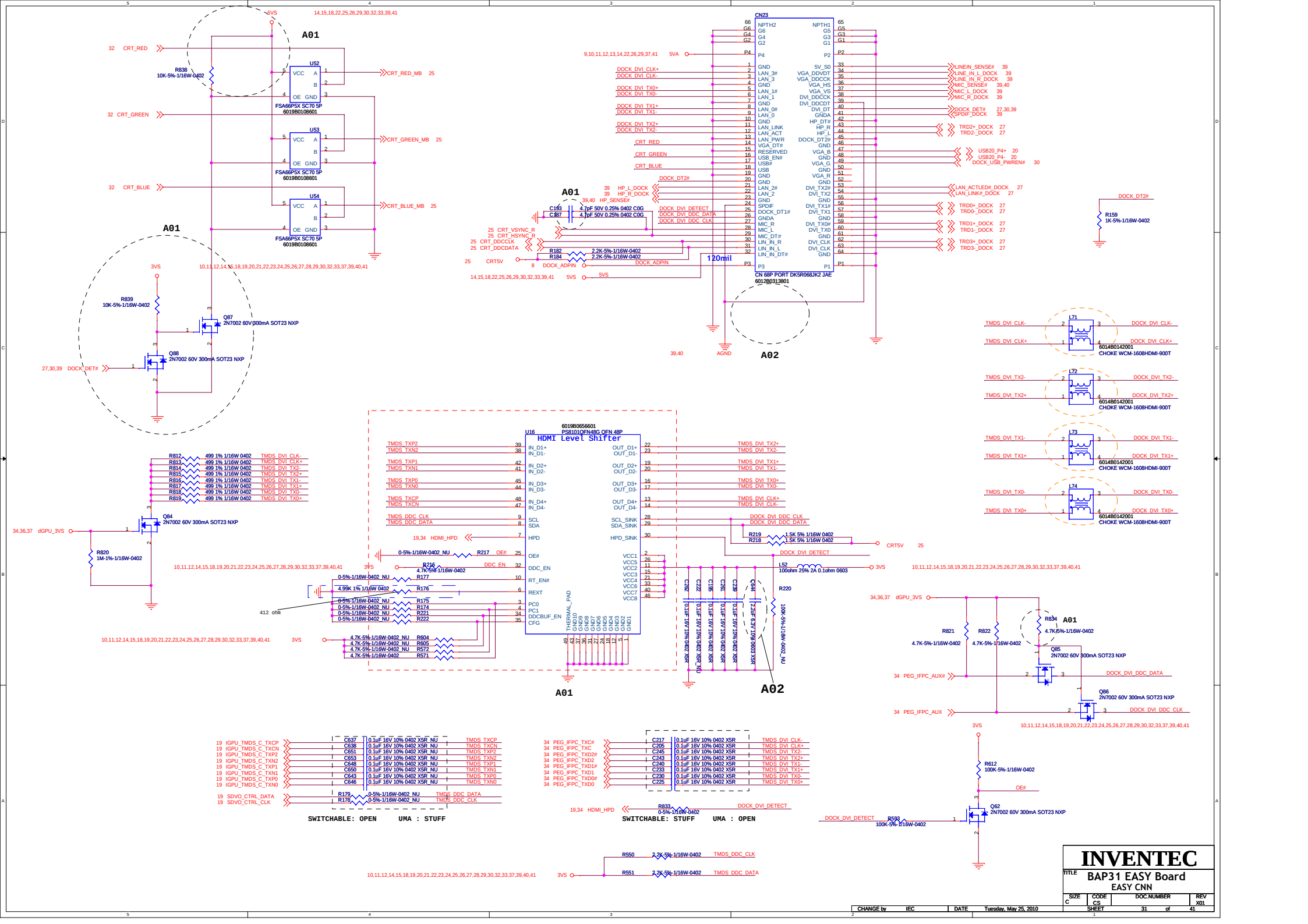
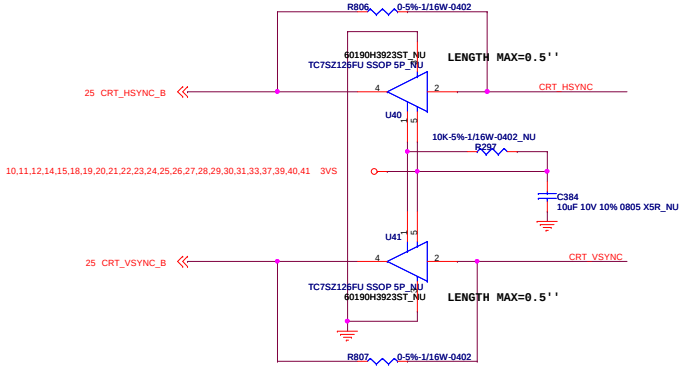
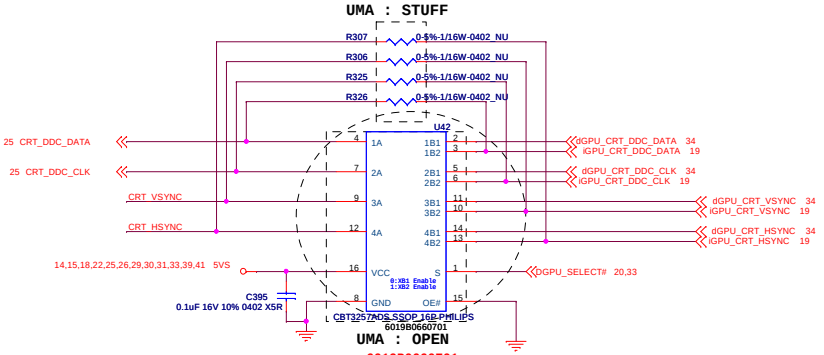

IT8502E/NX-L
SPI FLASH
HSPI INTERFACE
3G/WLAN LED control
To K/B MODULE
Don't place any pull-up resistor on GPG0 and GPG6
Pull down is for SPI flash
GPIO group I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode
6019B0653601
IT8502E/NX-L LQFP 128P ITE
CN 26P FPC 88513-2641 ACES
6012B0245907
INVENTEC
BAP/BXP30
KBC ITE8502E
Monday, May 24, 2010


A01
A02
CN23
CN 68P PORT DK5R068JK2 JAE
6012B0313801
120mil
U52
U53
U54
FSA66P5X SC70 5P
6019B0108601
U16
6019B0656601
PS8101QFN48G QFN 48P
HDMI Level Shifter
SWITCHABLE: OPEN UMA : STUFF
SWITCHABLE: STUFF UMA : OPEN
INVENTEC
BAP31 EASY Board
EASY CNN
SIZE C
CODE CS
DOC.NUMBER
REV X01
SHEET 31 of 41
CHANGE by IEC
DATE Tuesday, May 25, 2010

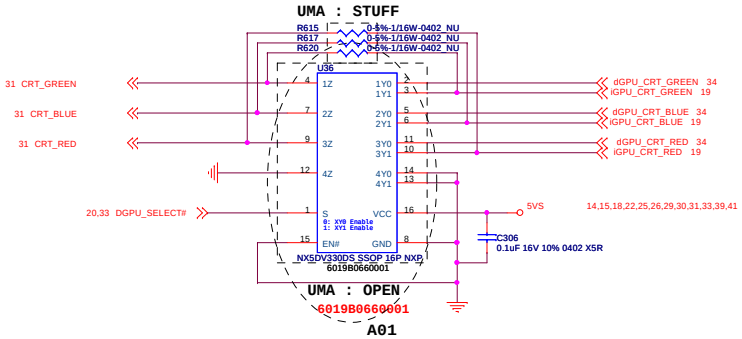
CRT HSYNC/VSYNC SW For Dock



CRT HSYNC/VSYNC/DDC SW



CRT R/G/B SW



Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
DGPU_PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
GPU_EDID_SEL#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

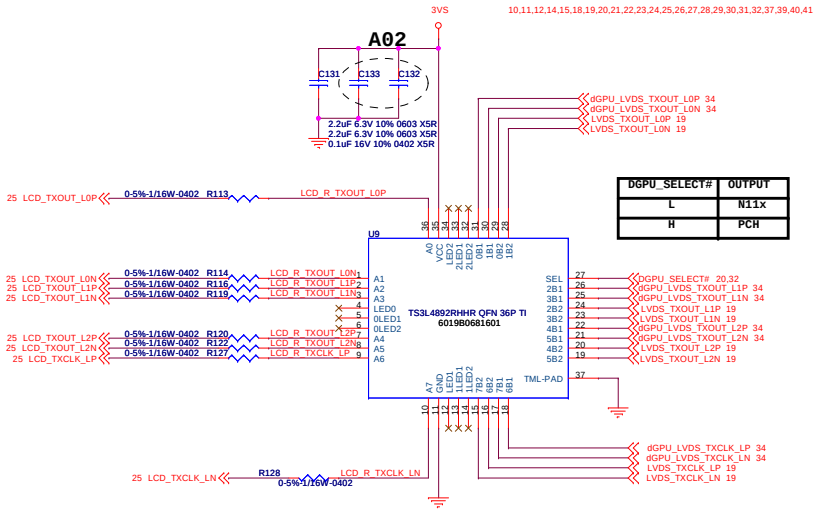
INVENTEC

TITLE: BAP/BXP30
Hybird Switch (1/2)

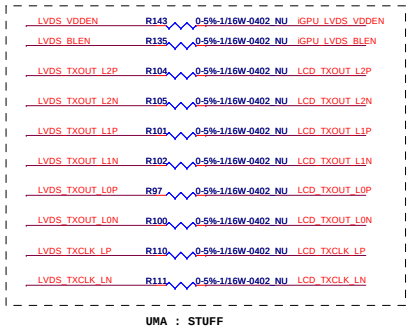
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

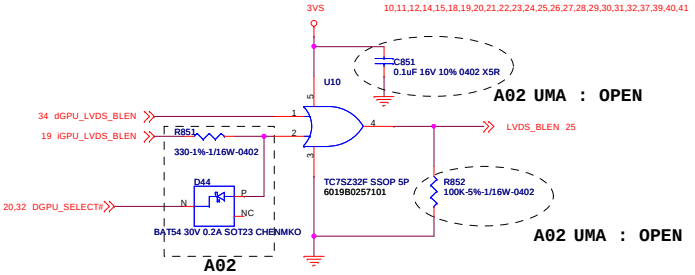
CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 32 of 41

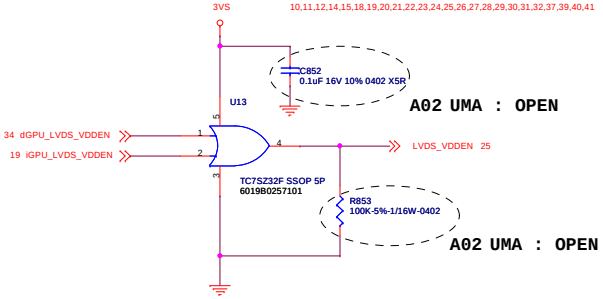
LVDS SW



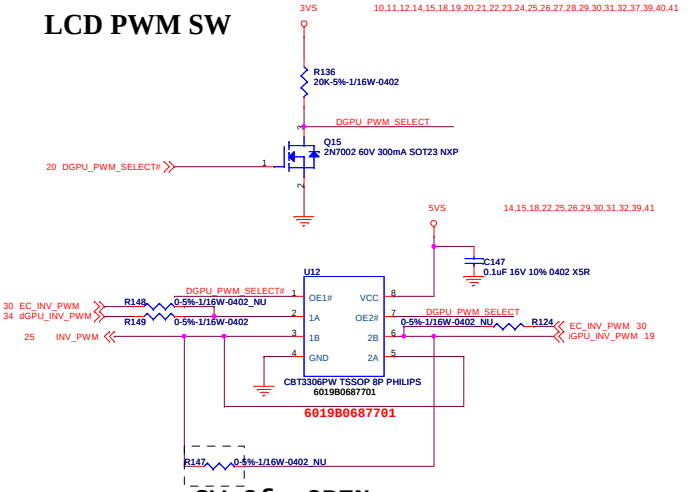
DGPU_SELECT#	OUTPUT
L	N11x
H	PCH





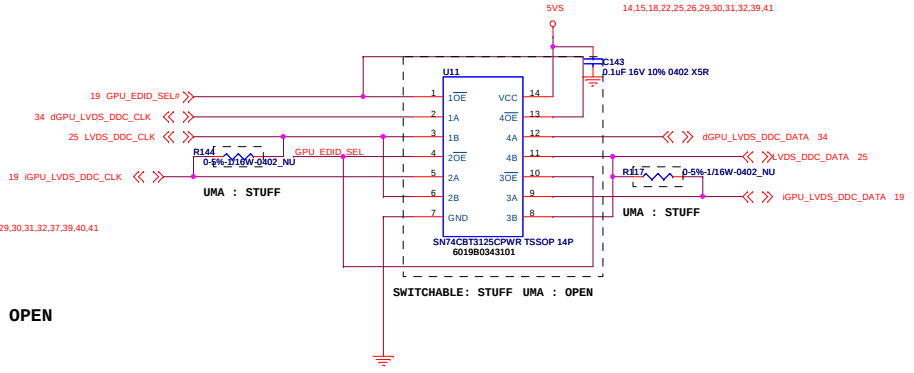


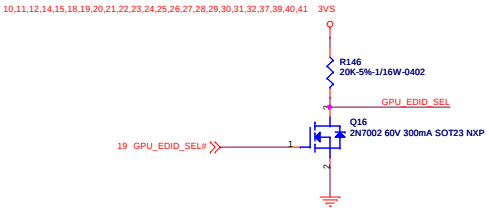
LCD PWM SW



SW Gfx:OPEN
UMA:Stuff

LCD DDC SW



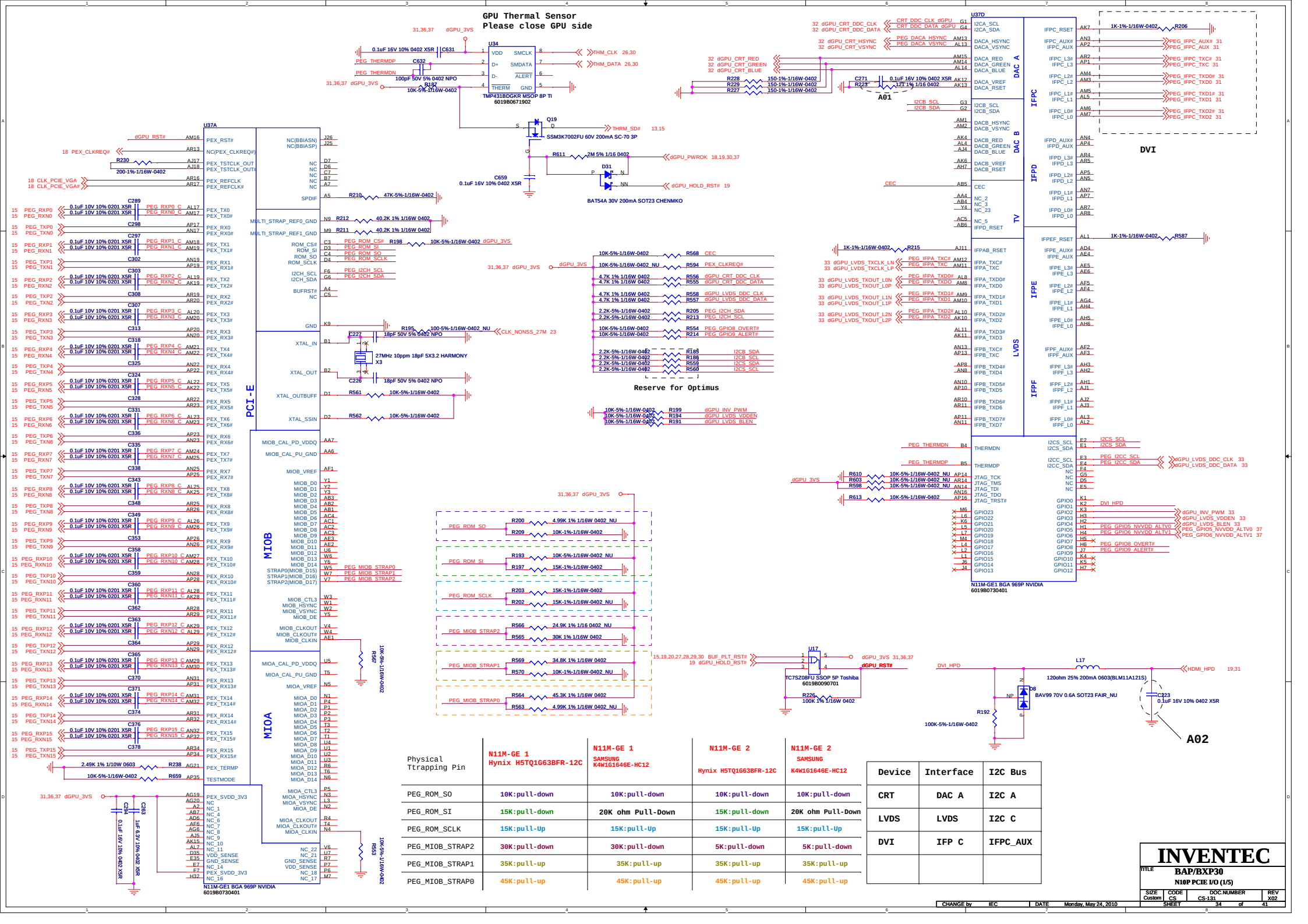


CHANGE by	IEC	DATE	Monday, May 24, 2010	SHEET	33 of 41

INVENTEC

TITLE: **BAP/BXP30**
Hybird Switch (2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01



Physical Ttrapping Pin	N11M-GE 1 Hynix H5TQ1G63BFR-12C	N11M-GE 1 SAMSUNG K4W1G1646E-HC12	N11M-GE 2 Hynix H5TQ1G63BFR-12C	N11M-GE 2 SAMSUNG K4W1G1646E-HC12
PEG_ROM_SO	10K:pull-down	10K:pull-down	10K:pull-down	10K:pull-down
PEG_ROM_SI	15K:pull-down	20K ohm Pull-Down	15K:pull-down	20K ohm Pull-Down
PEG_ROM_SCLK	15K:pull-Up	15K:pull-Up	15K:pull-Up	15K:pull-Up
PEG_MIOB_STRAP2	30K:pull-down	30K:pull-down	5K:pull-down	5K:pull-down
PEG_MIOB_STRAP1	35K:pull-up	35K:pull-up	35K:pull-up	35K:pull-up
PEG_MIOB_STRAP0	45K:pull-up	45K:pull-up	45K:pull-up	45K:pull-up

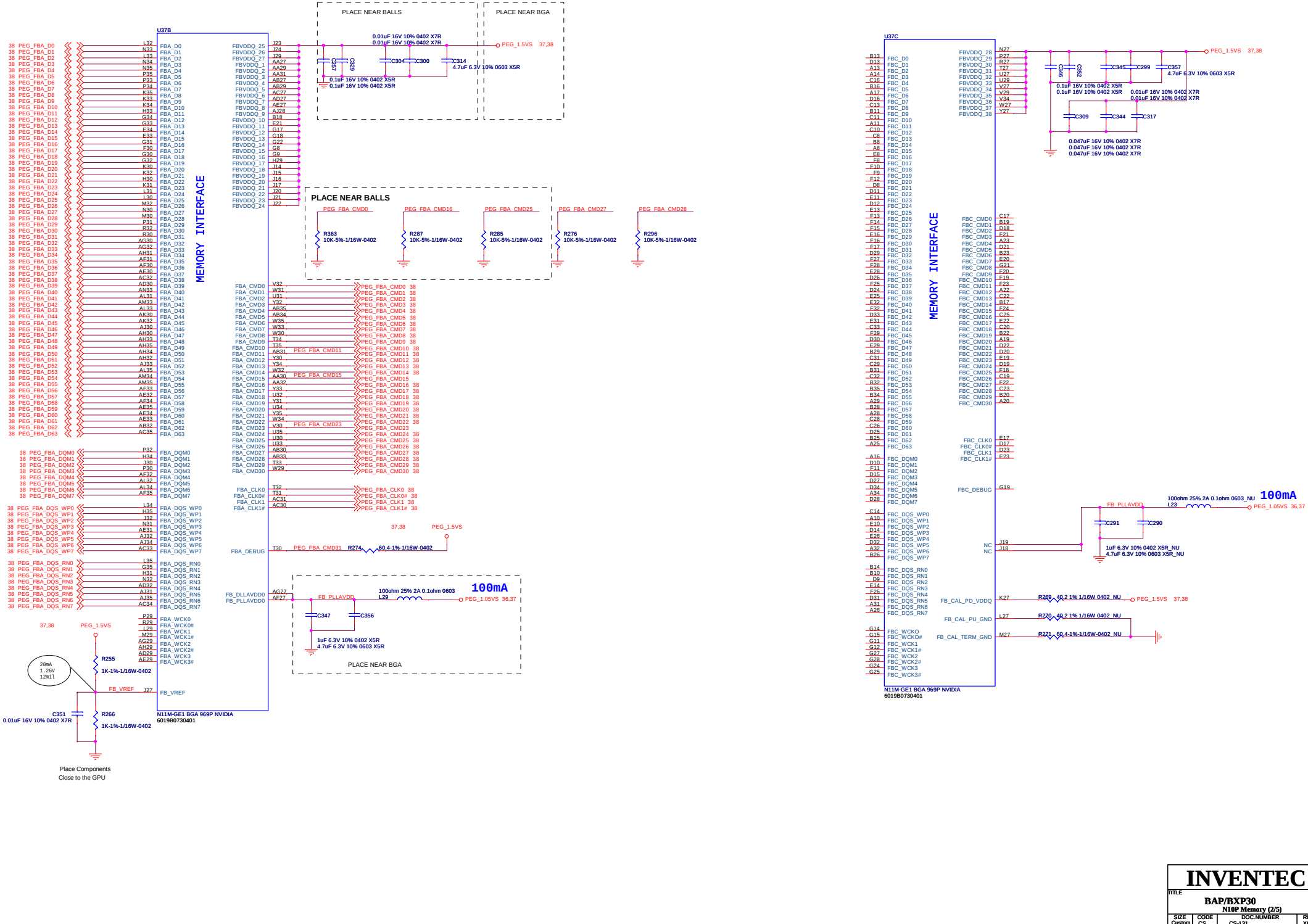
Device	Interface	I2C Bus
CRT	DAC A	I2C A
LVDS	LVDS	I2C C
DVI	IFP C	IFPC_AUX

INVENTEC

TITLE: BAP/BXP30
N10P PCIE I/O (1/5)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02

CHANGE by: IEC | DATE: Monday, May 24, 2010 | SHEET 34 of 41



CHANGE by	IEC	DATE	Monday, May 24, 2010	

INVENTEC

TITLE: **BAP/BXP30**
N10P Memory (2/5)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02

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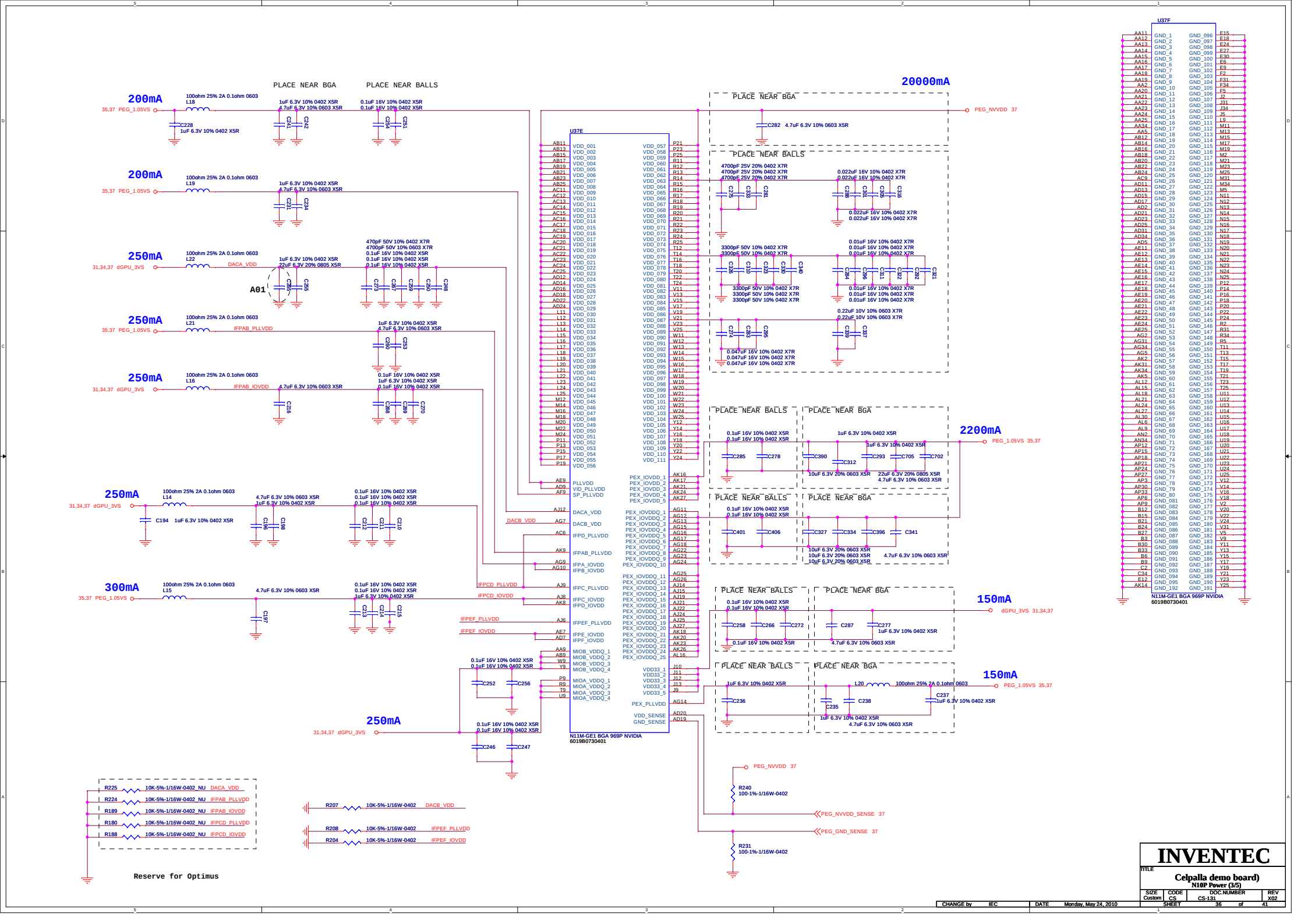
200mA
35,37 PEG_1.05VS
100ohm 25% 2A 0.1ohm 0603
L18
C228
1uF 6.3V 10% 0402 X5R
PLACE NEAR BGA
1uF 6.3V 10% 0402 X5R
4.7uF 6.3V 10% 0603 X5R
C241
C242
PLACE NEAR BALLS
0.1uF 16V 10% 0402 X5R
0.1uF 16V 10% 0402 X5R
C254
C251
200mA
L19
C231
C234
250mA
31,34,37 dGPU_3VS
L22
DACA_VDD
A01
22uF 6.3V 20% 0805 X5R
C233
C255
470pF 50V 10% 0402 X7R
4700pF 50V 10% 0603 X7R
0.1uF 16V 10% 0402 X5R
C227
C207
C259
C260
C248
250mA
L21
IFPAB_PLLVDD
C260
C253
250mA
L16
IFPAB_IOVDD
C216
C268
C269
C270
300mA
L14
C194 1uF 6.3V 10% 0402 X5R
C196
C199
C212
C211
C210
300mA
L15
C197
C213
C214
C215
IFPCD_PLLVDD
IFPCD_IOVDD
IFPEF_PLLVDD
IFPEF_IOVDD
250mA
31,34,37 dGPU_3VS
C252
C256
C246
C247
U37E
N11M-GE1 BGA 969P NVIDIA
6019B0730401
VDD_001
VDD_002
VDD_003
VDD_004
VDD_005
VDD_006
VDD_007
VDD_008
VDD_009
VDD_010
VDD_011
VDD_012
VDD_013
VDD_014
VDD_015
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VDD_106
VDD_107
VDD_108
VDD_109
VDD_110
VDD_111
PLLVDD
VID_PLLVDD
SP_PLLVDD
DACA_VDD
DACB_VDD
IFPD_PLLVDD
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
IFPC_PLLVDD
IFPC_IOVDD
IFPD_IOVDD
IFPEF_PLLVDD
IFPE_IOVDD
IFPF_IOVDD
MIOB_VDDQ_1
MIOB_VDDQ_2
MIOB_VDDQ_3
MIOB_VDDQ_4
MIOA_VDDQ_1
MIOA_VDDQ_2
MIOA_VDDQ_3
MIOA_VDDQ_4
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
PEX_IOVDDQ_20
PEX_IOVDDQ_21
PEX_IOVDDQ_22
PEX_IOVDDQ_23
PEX_IOVDDQ_24
PEX_IOVDDQ_25
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
PEX_PLLVDD
VDD_SENSE
GND_SENSE
20000mA
PLACE NEAR BGA
C282 4.7uF 6.3V 10% 0603 X5R
PEG_NVVDD 37
PLACE NEAR BALLS
4700pF 25V 20% 0402 X7R
4700pF 25V 20% 0402 X7R
C225
C233
C281
0.022uF 16V 10% 0402 X7R
0.022uF 16V 10% 0402 X7R
C228
C301
C305
C316
0.022uF 16V 10% 0402 X7R
0.022uF 16V 10% 0402 X7R
3300pF 50V 10% 0402 X7R
3300pF 50V 10% 0402 X7R
C308
C310
C322
C330
C340
3300pF 50V 10% 0402 X7R
3300pF 50V 10% 0402 X7R
3300pF 50V 10% 0402 X7R
0.01uF 16V 10% 0402 X7R
0.01uF 16V 10% 0402 X7R
0.01uF 16V 10% 0402 X7R
C284
C296
C311
C292
C321
0.01uF 16V 10% 0402 X7R
0.01uF 16V 10% 0402 X7R
0.01uF 16V 10% 0402 X7R
0.22uF 10V 10% 0603 X7R
0.22uF 10V 10% 0603 X7R
C274
C283
C295
C339
C337
0.047uF 16V 10% 0402 X7R
0.047uF 16V 10% 0402 X7R
0.047uF 16V 10% 0402 X7R
2200mA
PLACE NEAR BALLS
PLACE NEAR BGA
0.1uF 16V 10% 0402 X5R
0.1uF 16V 10% 0402 X5R
C285
C278
1uF 6.3V 10% 0402 X5R
1uF 6.3V 10% 0402 X5R
C390
C312
C293
C705
C702
10uF 6.3V 20% 0603 X5R
22uF 6.3V 20% 0805 X5R
4.7uF 6.3V 10% 0603 X5R
PEG_1.05VS 35,37
PLACE NEAR BALLS
PLACE NEAR BGA
0.1uF 16V 10% 0402 X5R
0.1uF 16V 10% 0402 X5R
C401
C406
C327
C334
C396
C341
10uF 6.3V 20% 0603 X5R
10uF 6.3V 20% 0603 X5R
10uF 6.3V 20% 0603 X5R
4.7uF 6.3V 10% 0603 X5R
150mA
PLACE NEAR BALLS
PLACE NEAR BGA
0.1uF 16V 10% 0402 X5R
0.1uF 16V 10% 0402 X5R
C258
C266
C272
C287
C277
1uF 6.3V 10% 0402 X5R
0.1uF 16V 10% 0402 X5R
4.7uF 6.3V 10% 0603 X5R
dGPU_3VS 31,34,37
150mA
PLACE NEAR BALLS
PLACE NEAR BGA
1uF 6.3V 10% 0402 X5R
C236
L20
100ohm 25% 2A 0.1ohm 0603
C235
C238
C237
1uF 6.3V 10% 0402 X5R
1uF 6.3V 10% 0402 X5R
4.7uF 6.3V 10% 0603 X5R
PEG_1.05VS 35,37
PEG_NVVDD 37
R240
100-1%-1/16W-0402
PEG_NVVDD_SENSE 37
PEG_GND_SENSE 37
R231
100-1%-1/16W-0402
R225 10K-5%-1/16W-0402_NU DACA_VDD
R224 10K-5%-1/16W-0402_NU IFPAB_PLLVDD
R189 10K-5%-1/16W-0402_NU IFPAB_IOVDD
R180 10K-5%-1/16W-0402_NU IFPCD_PLLVDD
R188 10K-5%-1/16W-0402_NU IFPCD_IOVDD
Reserve for Optimus
R207 10K-5%-1/16W-0402 DACB_VDD
R208 10K-5%-1/16W-0402 IFPEF_PLLVDD
R204 10K-5%-1/16W-0402 IFPEF_IOVDD
U37F
N11M-GE1 BGA 969P NVIDIA
6019B0730401
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
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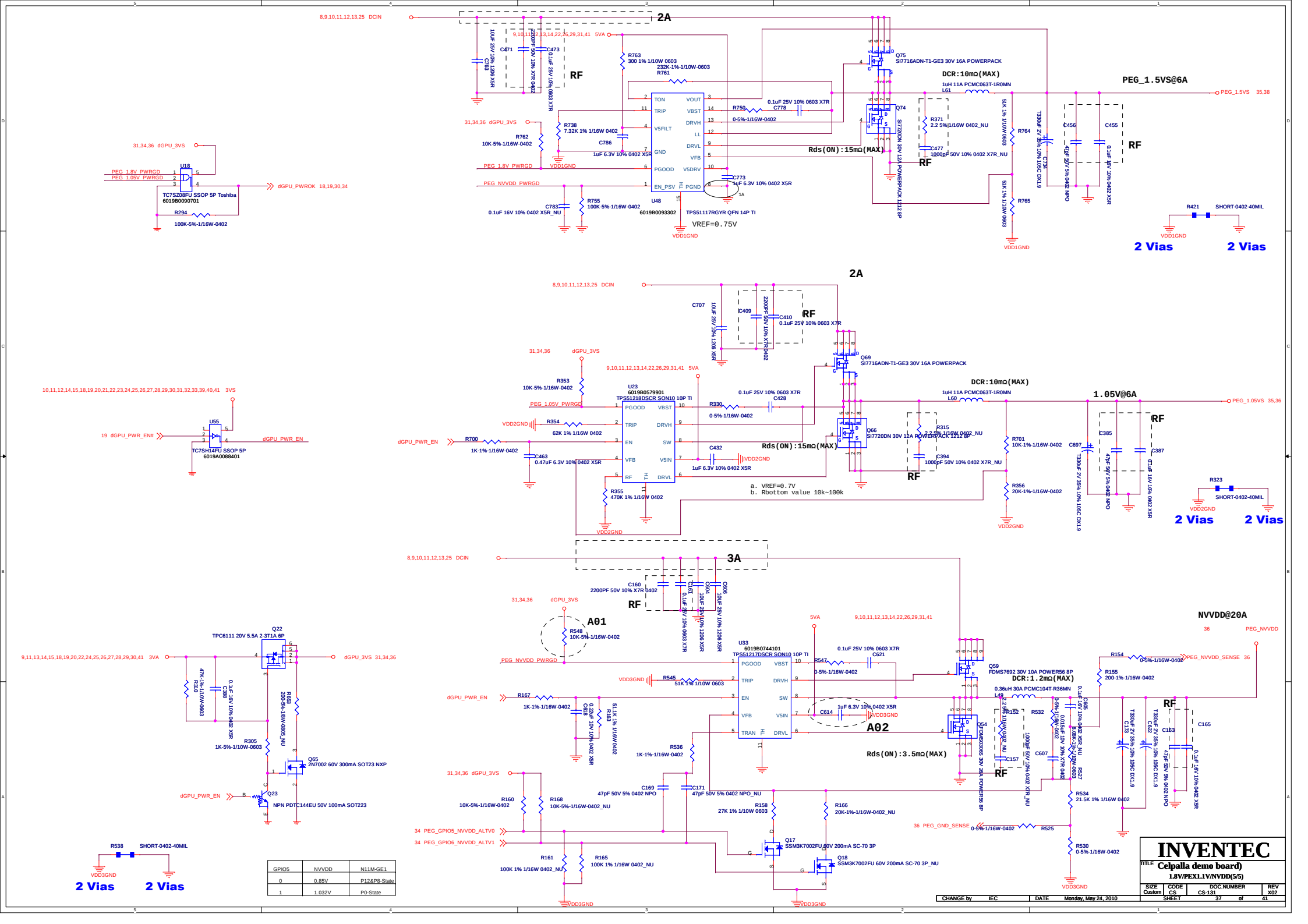
GND_182
GND_183
GND_184
GND_185
GND_186
GND_187
GND_188
GND_189
GND_190
GND_191
INVENTEC
TITLE
Celpalla demo board)
N10P Power (3/5)
SIZE
Custom
CODE
CS
DOC.NUMBER
CS-131
REV
X02
CHANGE by IEC
DATE Monday, May 24, 2010
SHEET 36 of 41



GPIO5	NVVDD	N11M-GE1
0	0.85V	P12&P8-State
1	1.032V	P0-State

CHANGE by	IEC	DATE	Monday, May 24, 2010

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02

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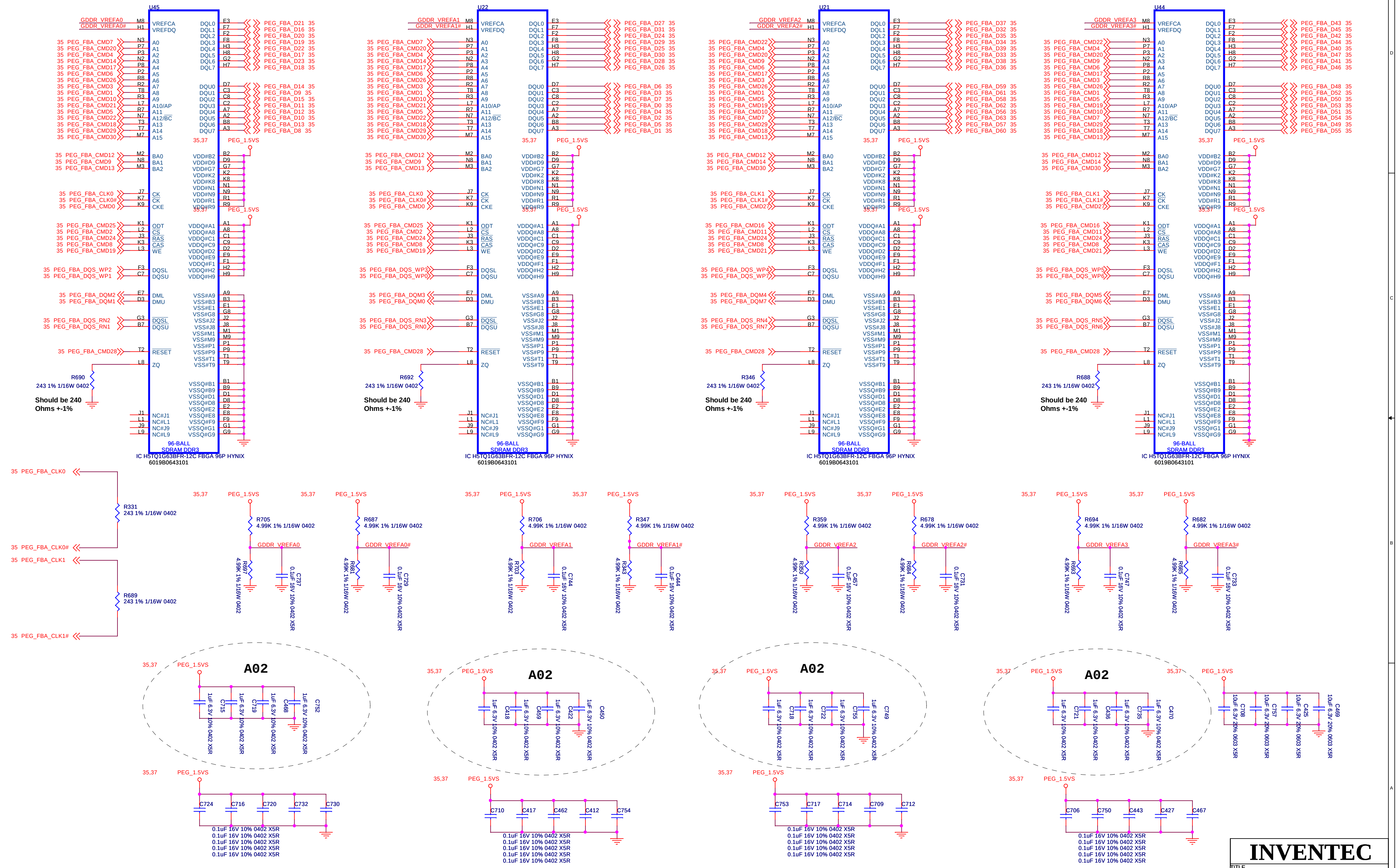


INVENTEC

TITLE
Celpalla demo board)
VRAM

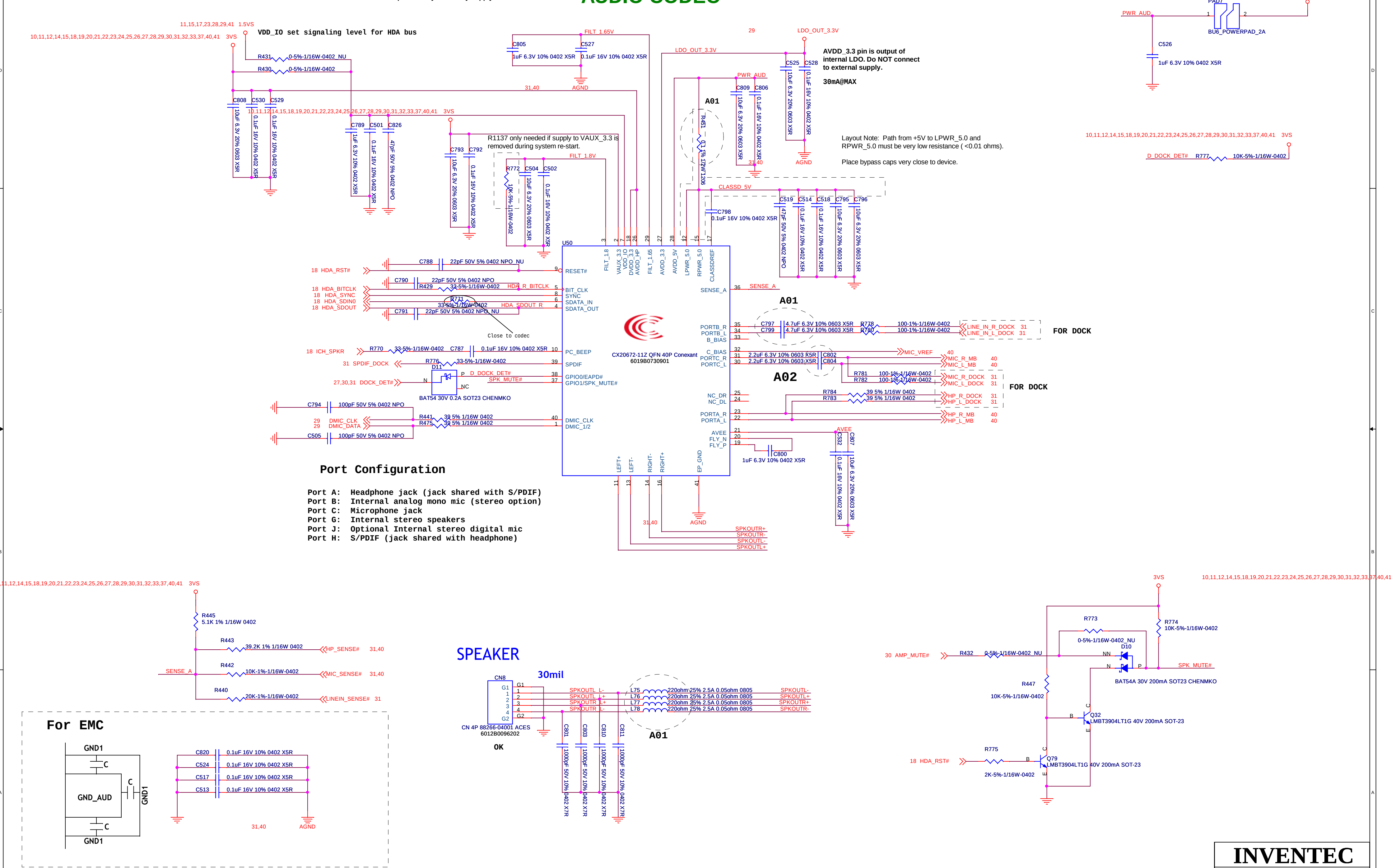
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Tuesday, May 25, 2010 | SHEET 38 of 41

AUDIO CODEC

Note:

To support Wake-on-Jack, the CODEC VAUX_3.3 pins must be powered by a Standby supply.



Port Configuration

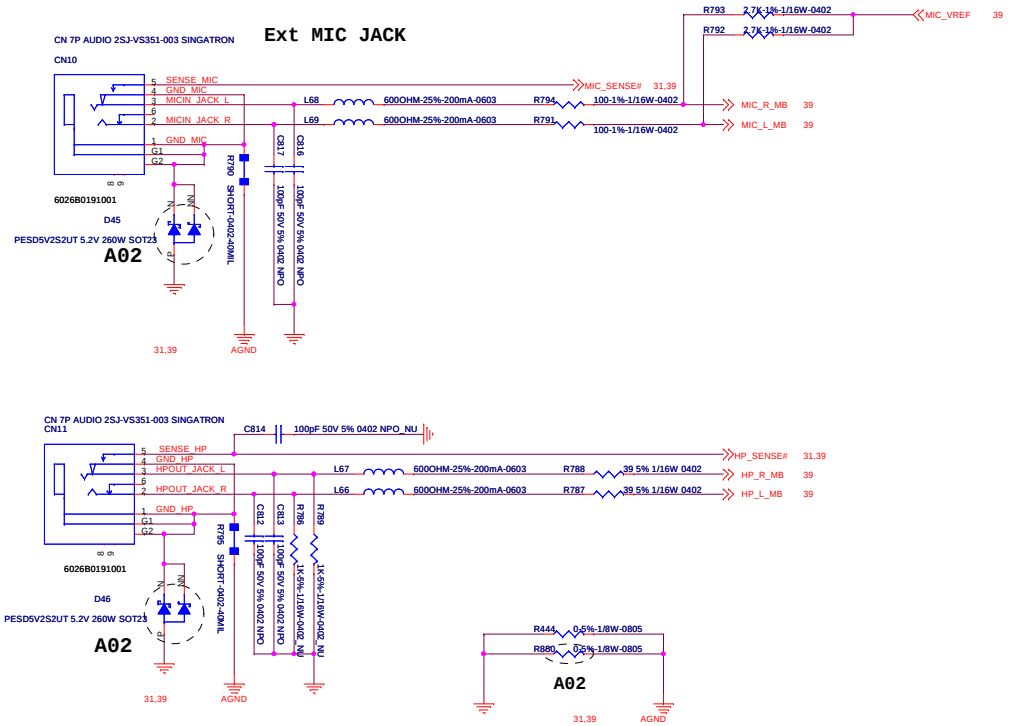
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono mic (stereo option)
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)

INVENTEC

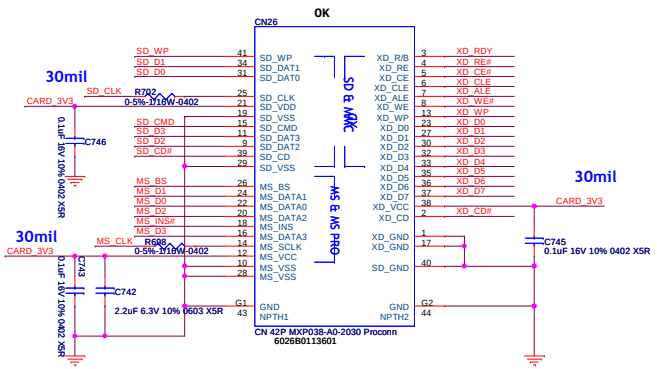
TITLE: Celpalla demo board)
Audio Codec /AMP

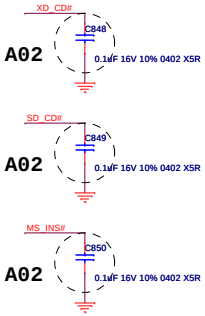
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

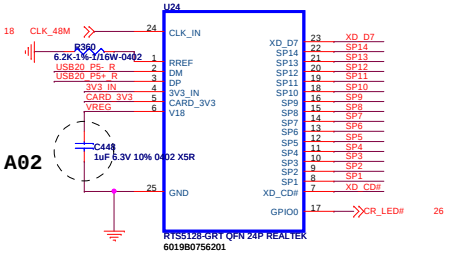
CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 39 of 41

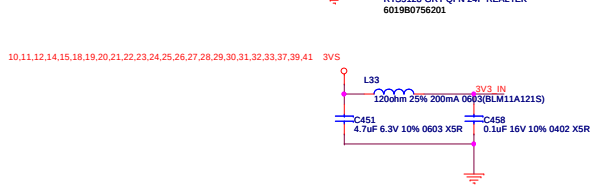


5 in 1 CARDREADER









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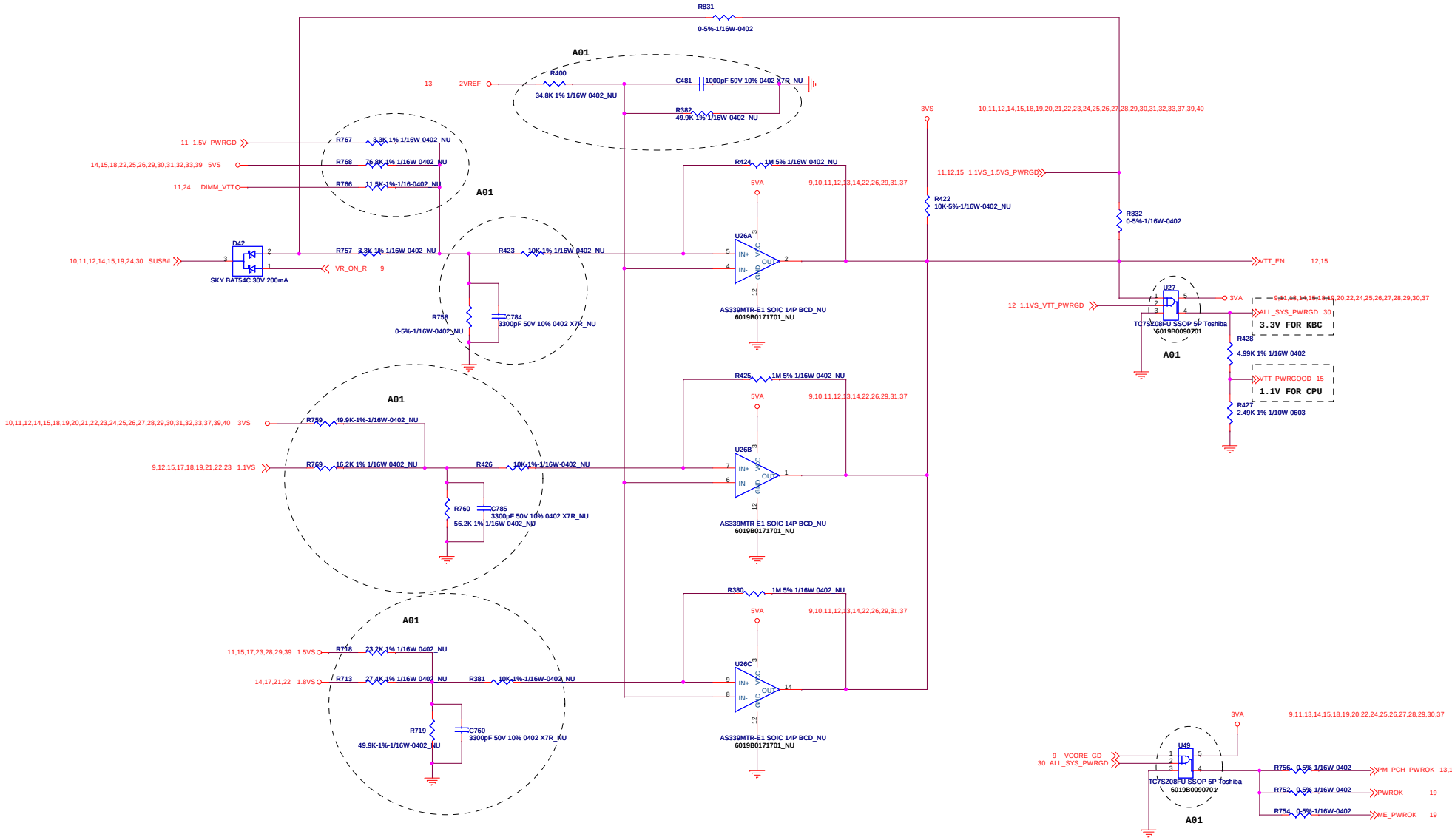
TITLE: BAP/BXP30 CARD READER/AUDIO BOARD			
SIZE: Custom	CODE: A03	DOC.NUMBER: D-CS-1310A2271201-ALG	REV: A03
CHANGE by: <CHANGE by>	DATE: Monday, May 24, 2010	SHEET: 40 of 41	



CHANGE by	<CHANGE by>	DATE	Monday, May 24, 2010

INVENTEC

TITLE: BAP/BXP30
POWER SEQUENCE

SIZE	CODE	DOC.NUMBER	REV
Custom	A03		A03

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