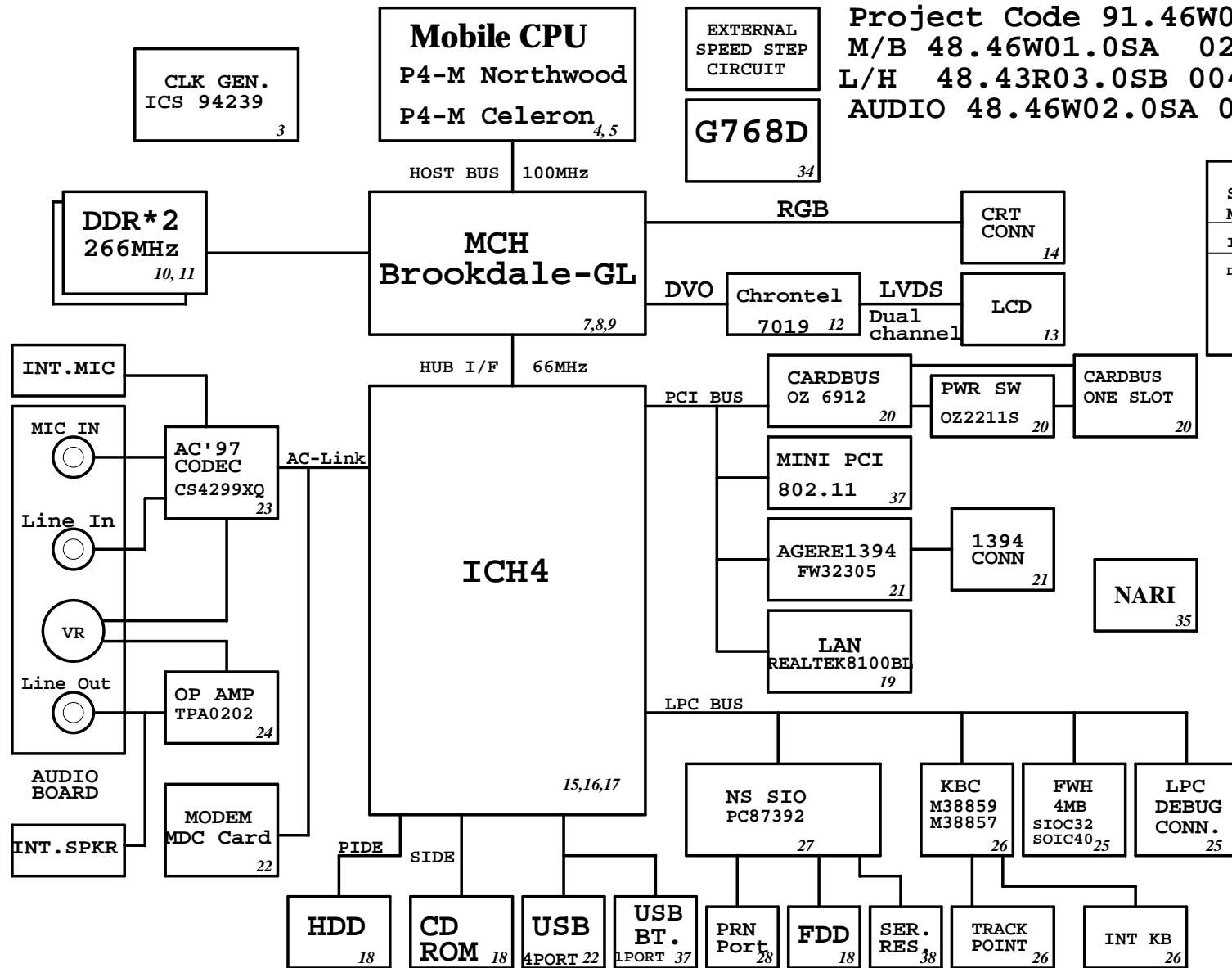


Pelican Block Diagram SB

Membership :
 Alen Hsu 2002/11/21
 Gene Feng
 Howard Sun

Project Code 91.46W01.001
 M/B 48.46W01.0SA 02217-SB
 L/H 48.43R03.0SB 00426-SB
 AUDIO 48.46W02.0SA 02401-SB



SYSTEM DC/DC MAX1631 30	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 5V_S3 5V_S0 3D3V_S5 3D3V_S3 3D3V_S0 3D3V_LANAC
SYSTEM DC/DC MAX1715 29	
INPUTS	OUTPUTS
DCBATOUT	2D5V_S3 1D5V_S0
CM8500 29	
2D5V_S3	1D25V_S3

CPU DC/DC Switching Power MAX1718/1887 6	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 1.3V 44A +VID 1.2V 0.3A

O2 CHARGER OZ982A/ATTINY12 UP 32,33	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A UP+5V 5V 25mA

PCB LAYER	
L1: Signal 1	
L2: GND	
L3: Signal 2	
L4: VCC	
L5: Signal 3	
L6: GND	
L7: Signal 4	
L8: Signal 5	

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Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
Custom	Pelican	SB
Date: Thursday, November 21, 2002	Sheet 1 of 39	

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
AGERE 1394	AD19	F	REQ0# / GNT0#
LAN RTL8100BL	AD21	D	REQ4# / GNT4#
PCMCIA OZ6912	AD25	B	REQ1# / GNT1#
Mini-PCI	AD22	C,E	REQ2# / GNT2#
AGP	AD17(Int.)	A,B	
USB	AD29	A,D,C	
Hub-to-PCI	AD30		
LPC Bridge/ IDE/AC97/ SMBus	AD15		

緯創資通

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Title

Table of Content / HISTORY

Size
A3

Document Number

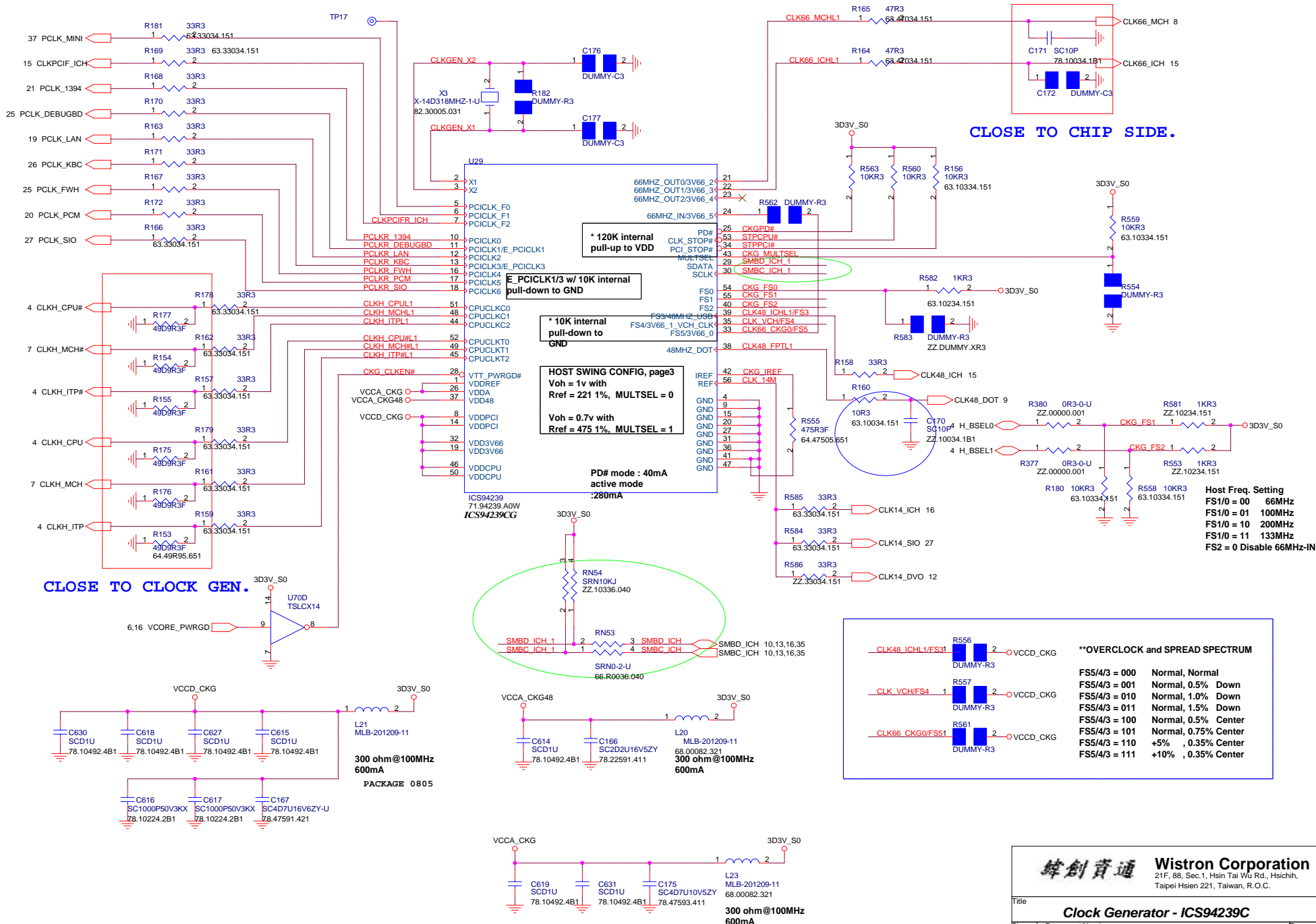
Pelican

Rev
SB

Date: Thursday, November 21, 2002

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39



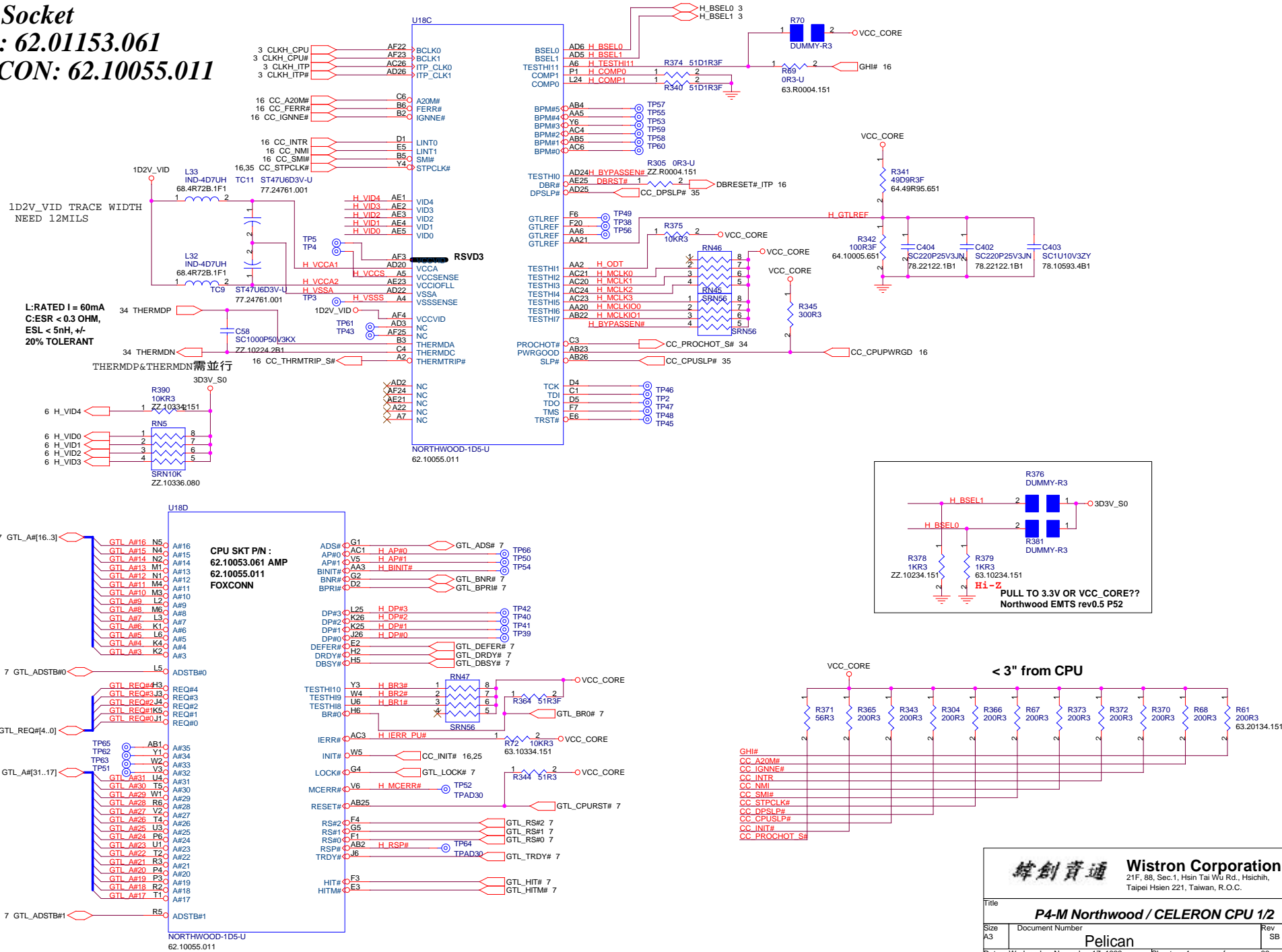
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

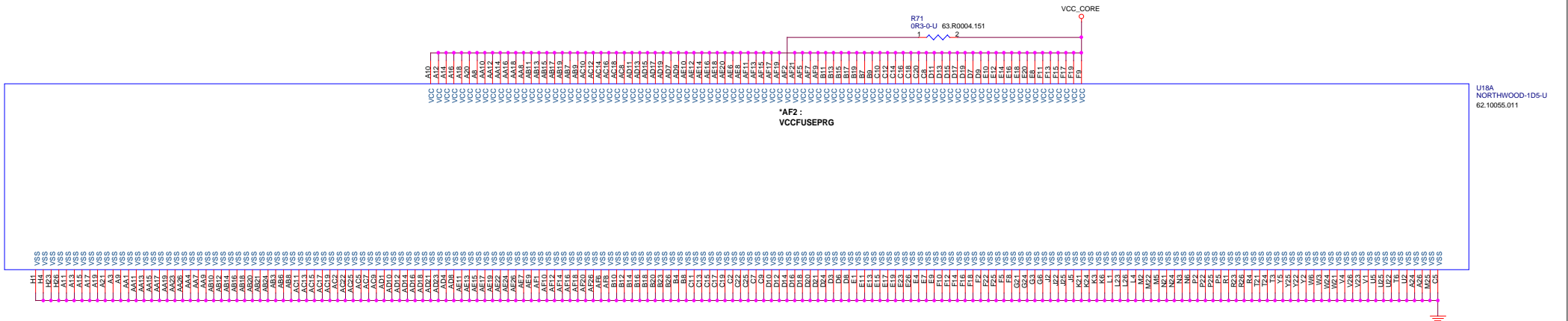
Title: **Clock Generator - ICS94239C**

Size	Document Number	Rev
Custom	Pelican	SB

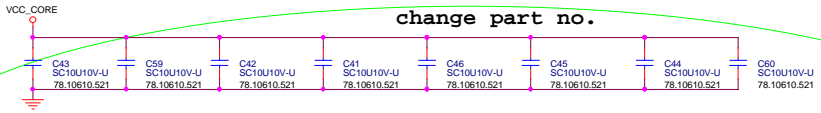
Date: Wednesday, November 17, 1999 Sheet 3 of 39

CPU Socket
AMP: 62.01153.061
FOXCON: 62.10055.011

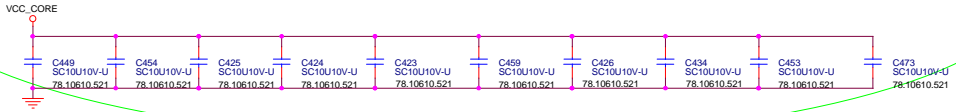




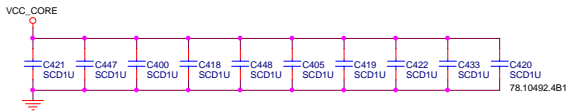
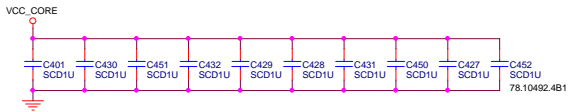
10U/X7R 1210 DECOUPLING CAPS
8X IN SOCKET CAVITY
10X IN CRB



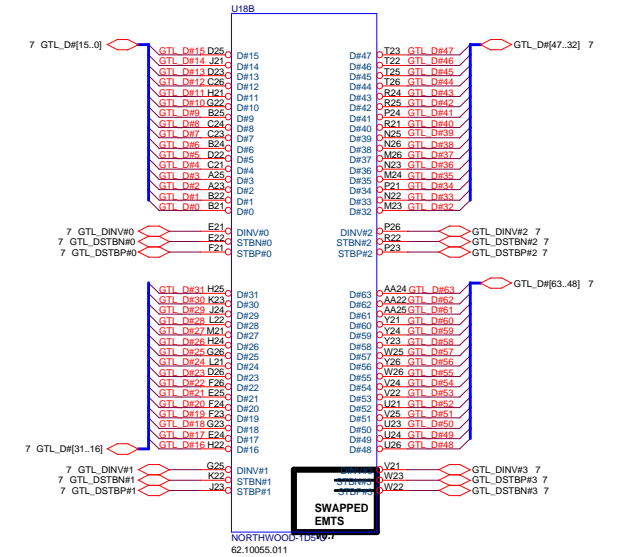
10U/X7R 1210 DECOUPLING CAPS
10X AROUND SOCKET
28X IN CRB



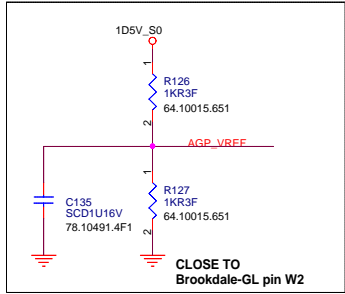
0.1U/X5R 0603 DECOUPLING CAPS
20X AROUND SOCKET
0.47U/X5R 0603 10X IN CRB



CHANGE NOTES
 CHANGE SC10U10V-U P/N:78.10613.2A1 (1210) (X7R)
 P/N:78.10620.221 (1206) (X7R)
 P/N:78.10610.521 (1206) (X5R)

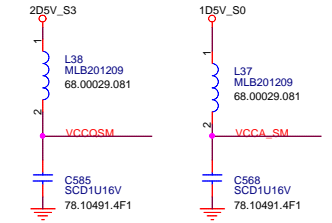
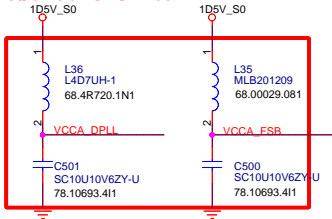


NORTHWOOD-1D5-07
62.10055.011

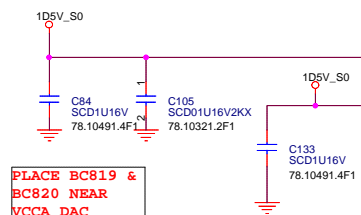


CLOSE TO Brookdale-GL pin W2

The choke and capacitor should be close to GMCH ball

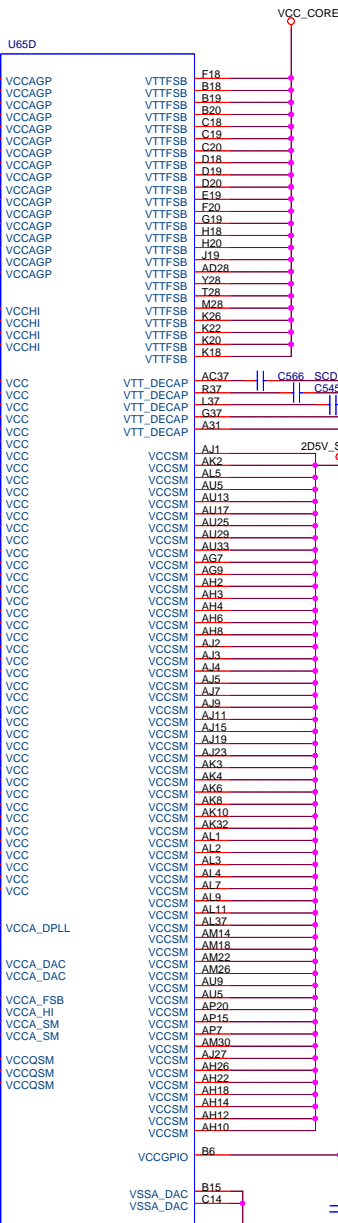


VCCA_DAC

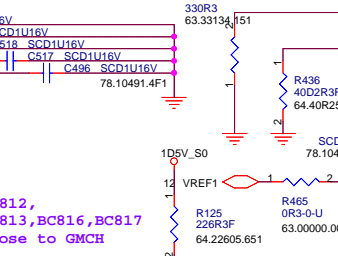
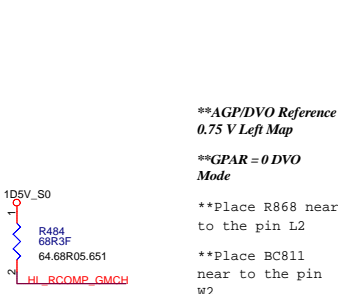


PLACE BC819 & BC820 NEAR VCCA_DAC BALLS

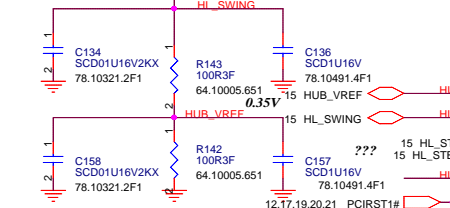
PLACE NEAR VCCA_HI BALLS



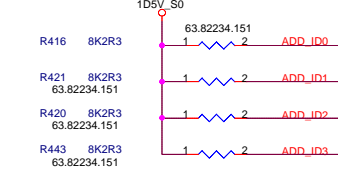
BROOKDALE-GL-U
71.BROOK.M05



BC812, BC813, BC816, BC817 close to GMCH

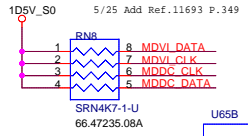


BC230 & BC229 close to Divider

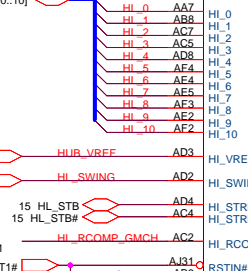
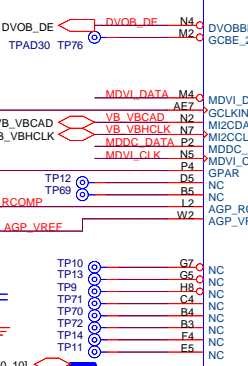


AD_ID[1,2,3,4,6,7] No stuff on 8K2R3
AD_ID[0,5] No stuff on 330R3 FOR Intel ID Select
Add. : 01000001

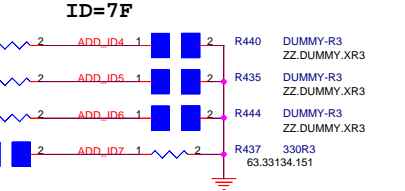
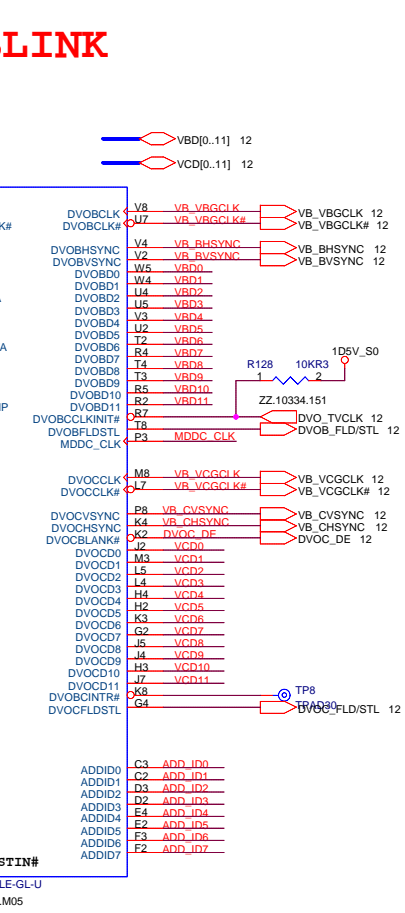
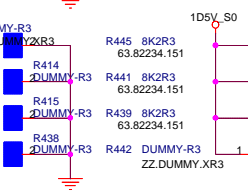
AGP / HUBLINK



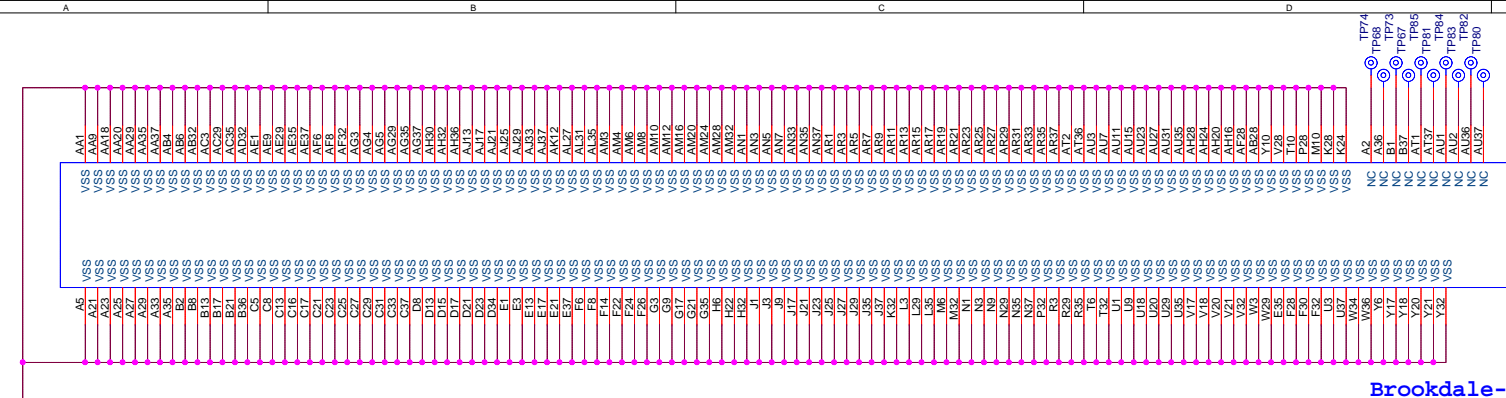
**AGP/DVO Reference 0.75 V Left Map
**RPAR = 0 DVO Mode
**Place R868 near to the pin L2
**Place BC811 near to the pin W2



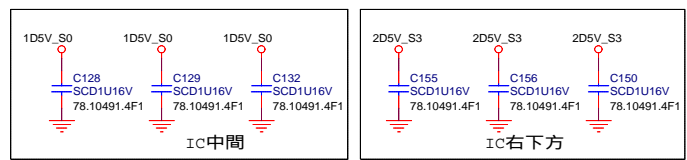
BC230 & BC229 close to Divider



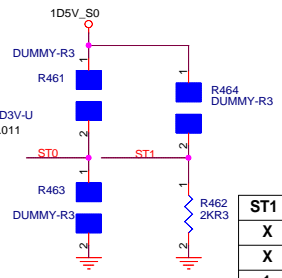
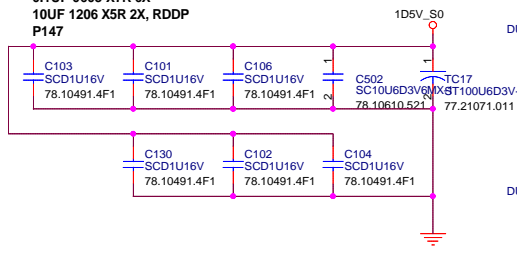
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Brookdale-G 788 : 71.BROOK.D0U
 Brookdale-G 760 : 71.BROOK.EOU
 Brookdale-G 824 : 71.BROOK.FOU
 Brookdale-GL 760 : 71.BROOK.POU

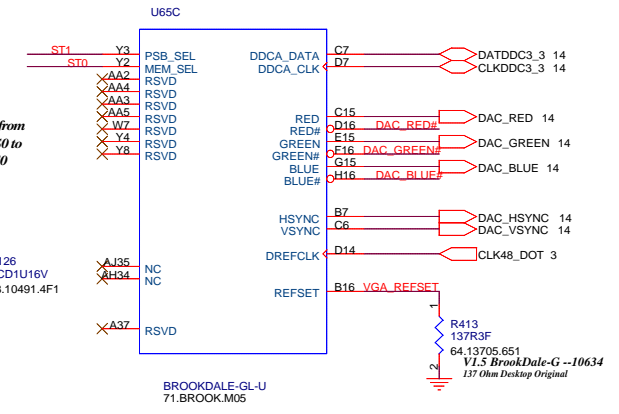
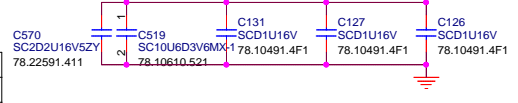


AGP HF DECOUPLING CAPS
0.1UF 0603 X7R 6X
10UF 1206 X5R 2X, RDDP P147

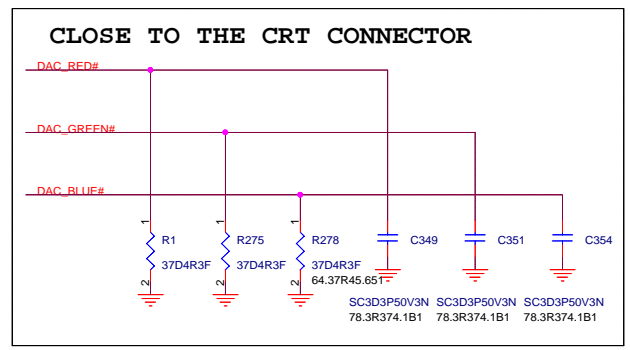
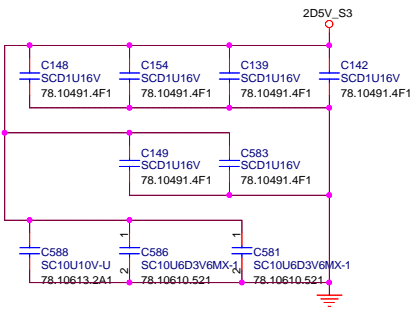
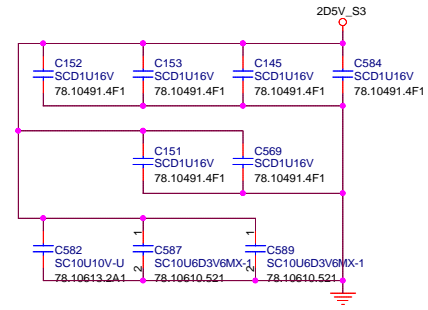
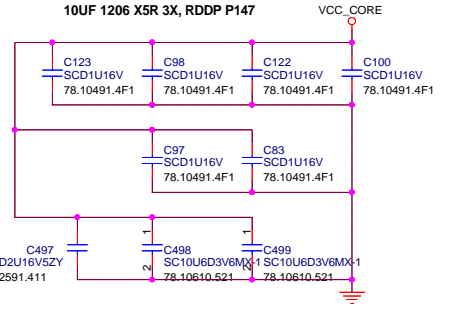


ST1	ST0	MCH STRAP
X	X	DDR
X	0	SDR
1	X	533 MHz
0	X	400 MHz

Change from 1D5V_S0 to 1D5V_S0
E-Note

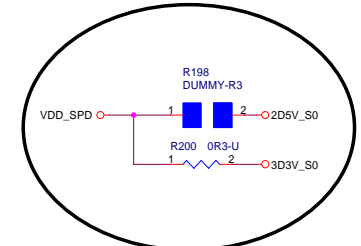
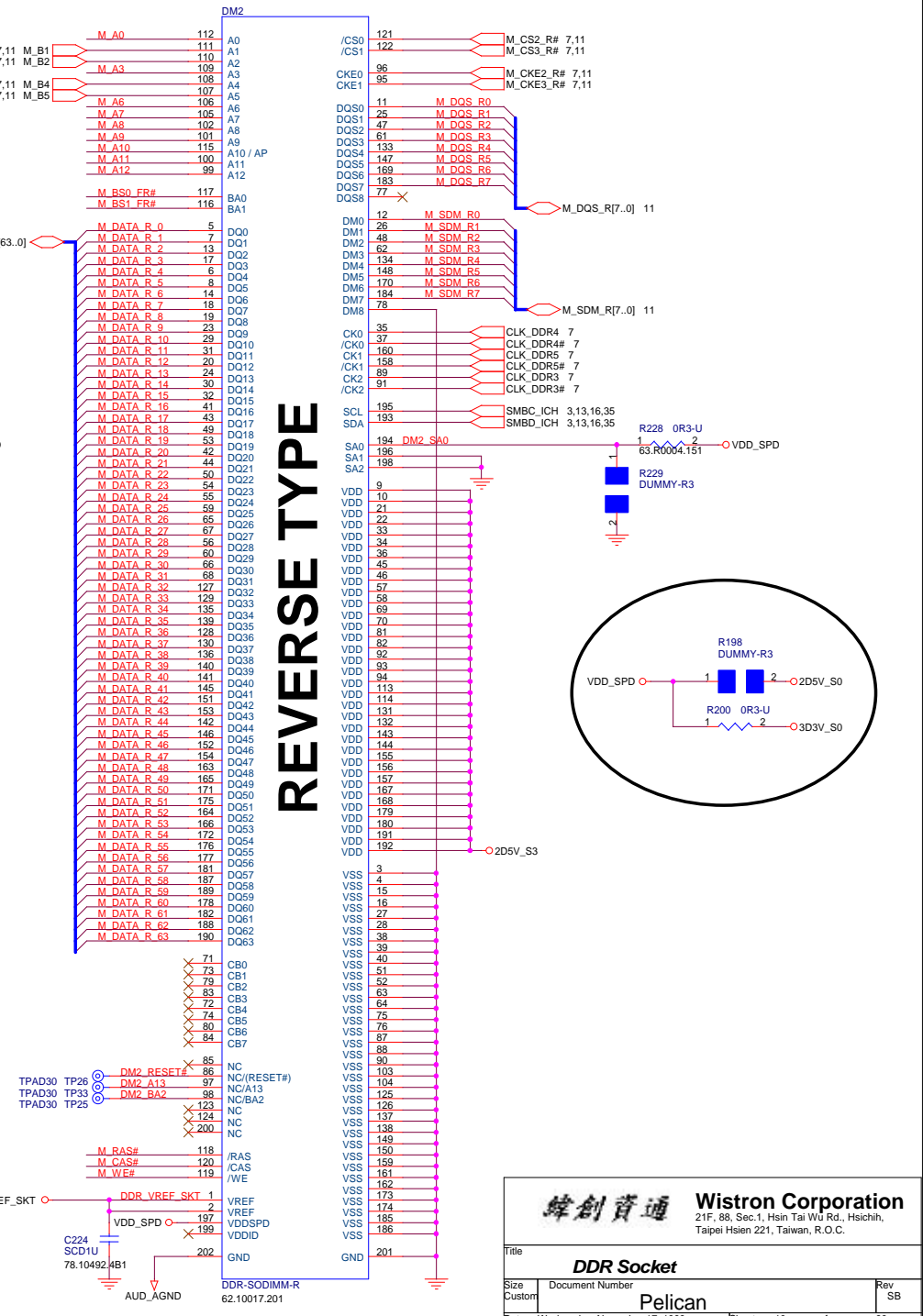
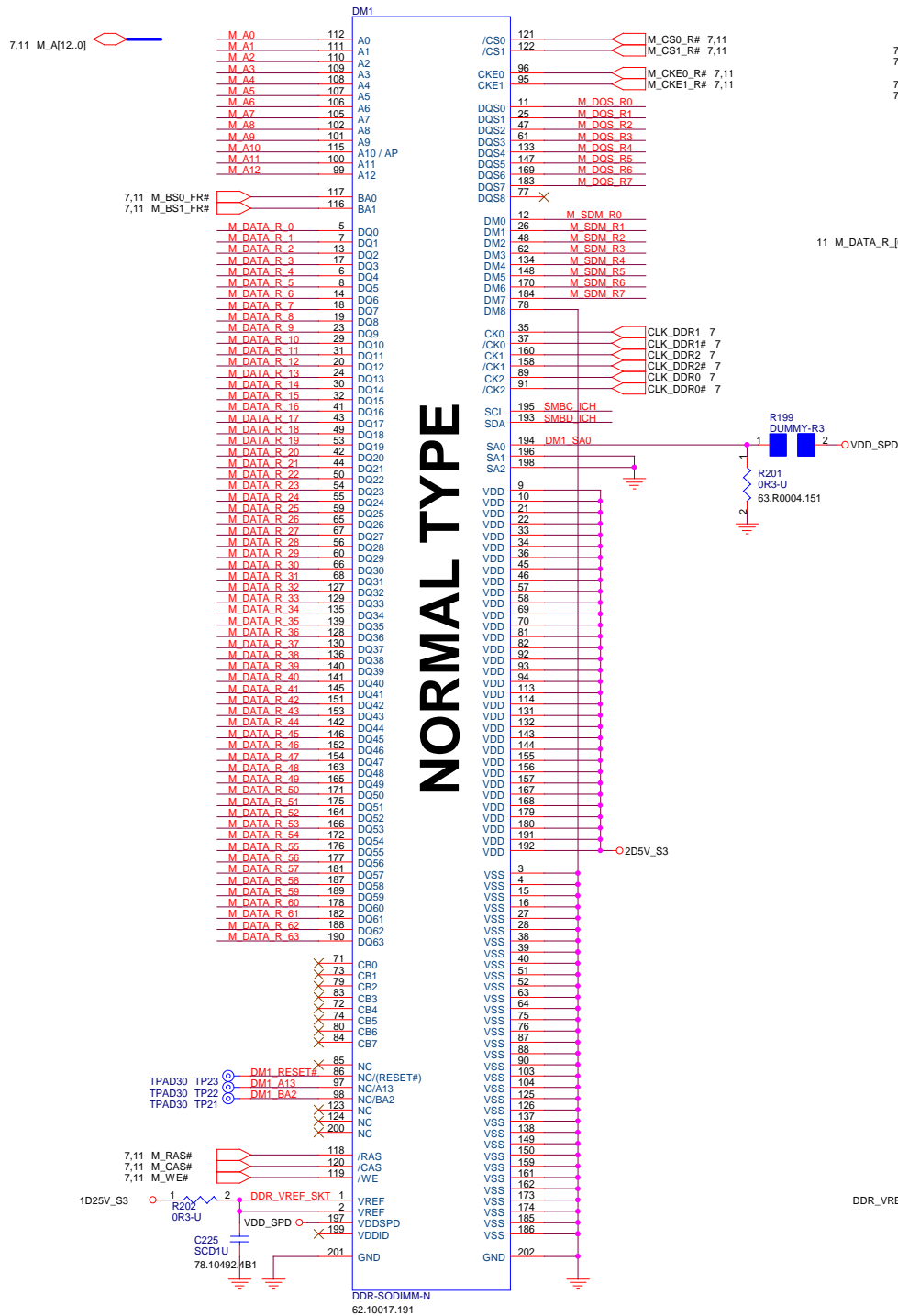


AGTL+ HF DECOUPLING CAPS
0.1UF 0603 X7R 10X
10UF 1206 X5R 3X, RDDP P147



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Title: **BROOKDALE(3/3)**
 Size: A3 Document Number: Pelican Rev SB
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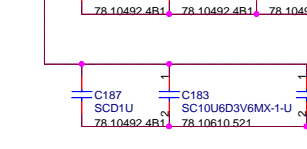
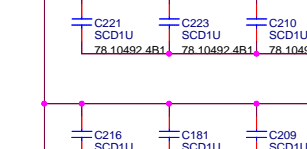
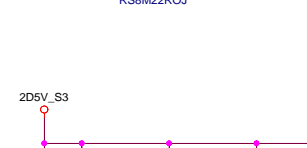
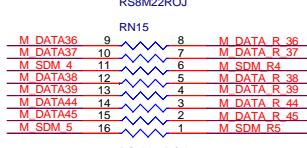
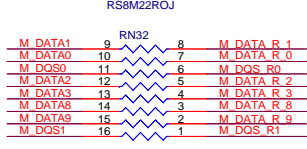
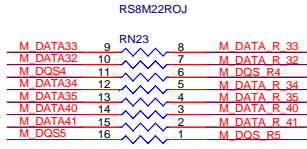
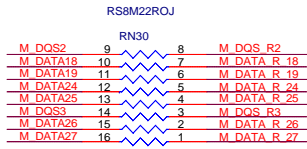
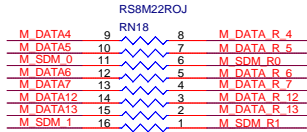
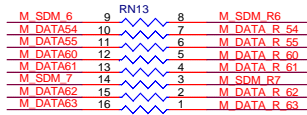
緯創資通 Wistron Corporation
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Title: **DDR Socket**

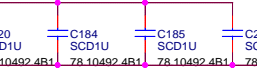
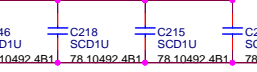
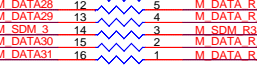
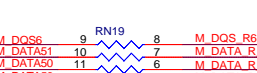
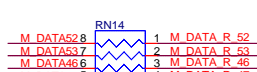
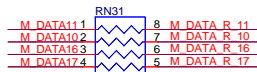
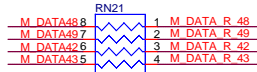
Size	Document Number	Rev
Custom	Pelican	SB

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SERIES DAMPING

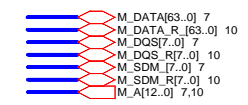
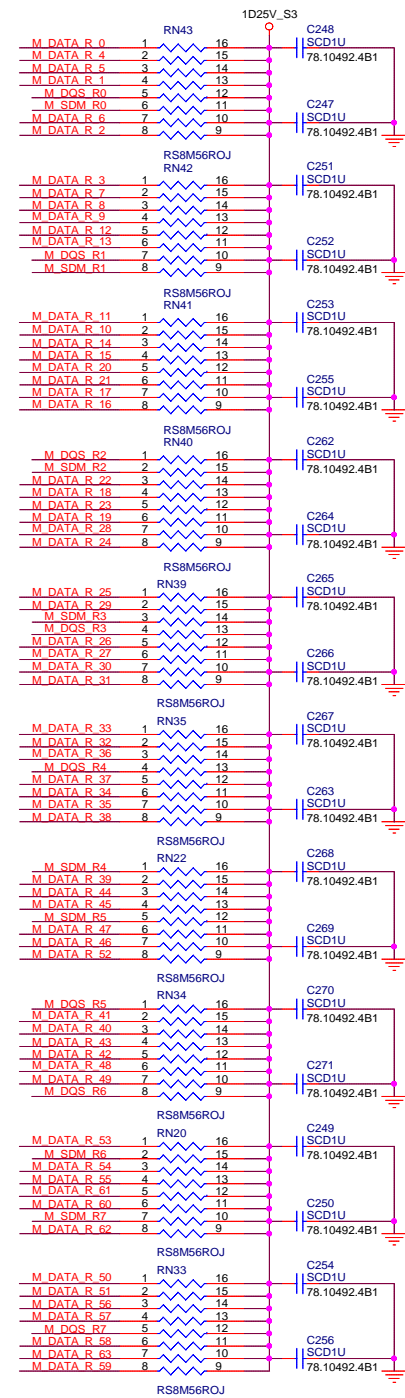


PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

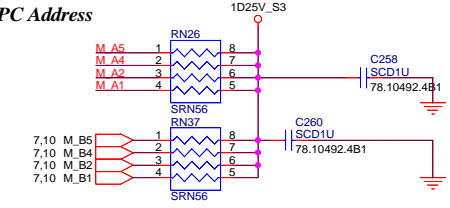


PARALLEL TERMINATION

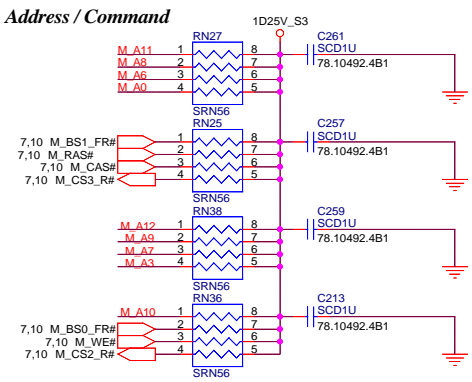
PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION



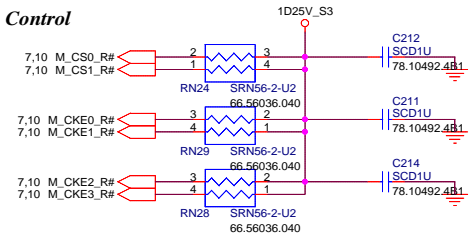
CPC Address



Address / Command

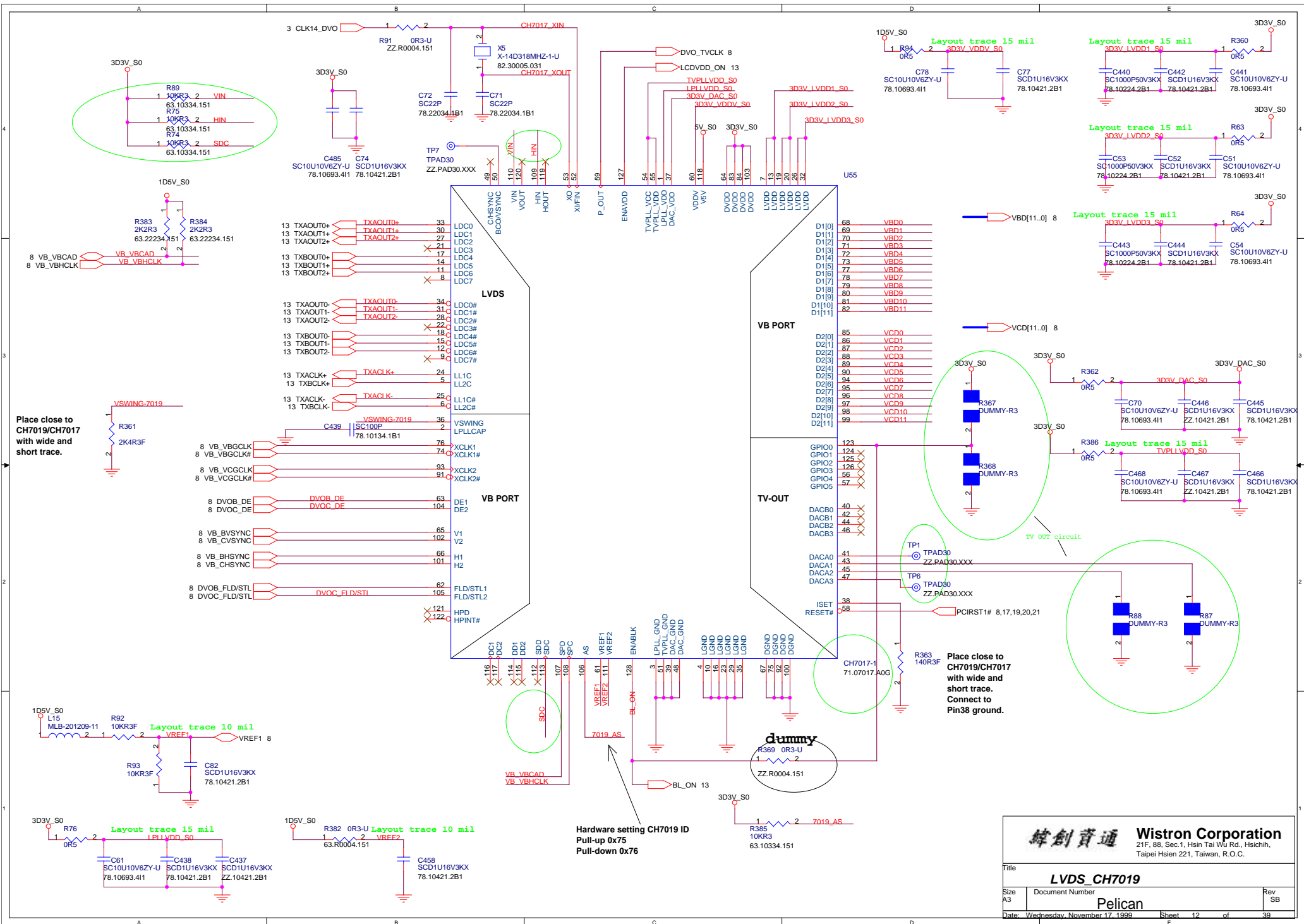


Control

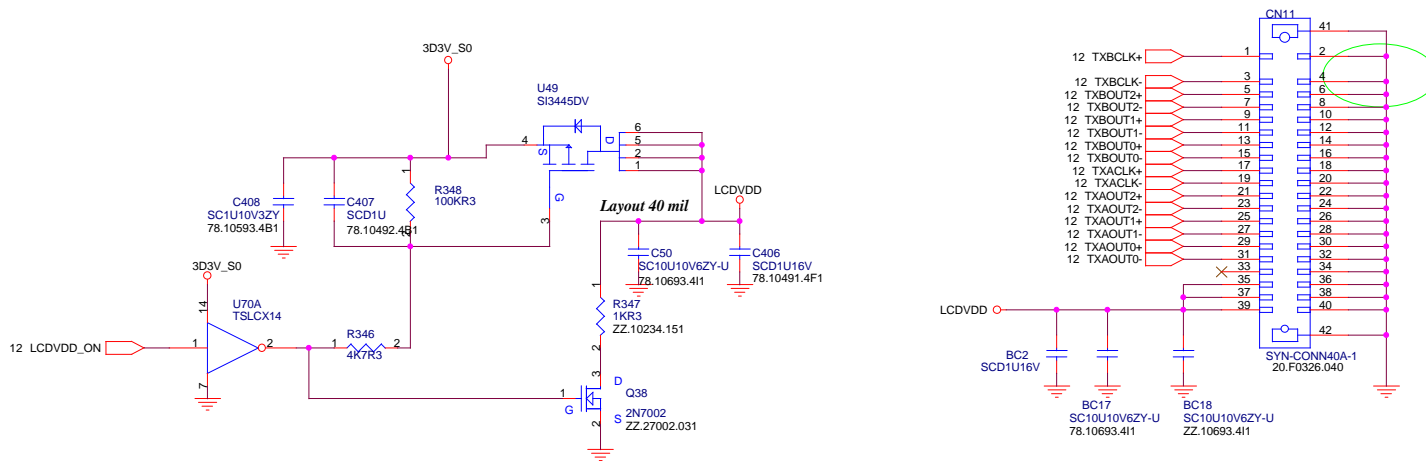
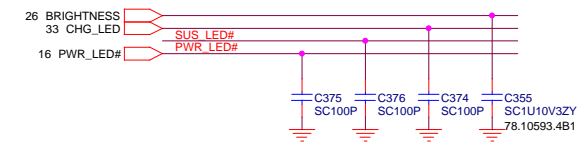
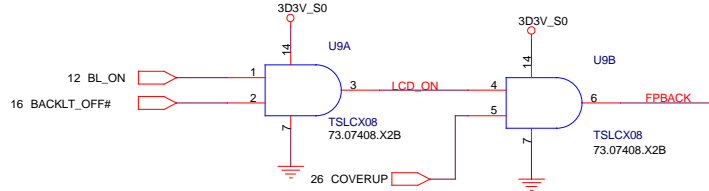
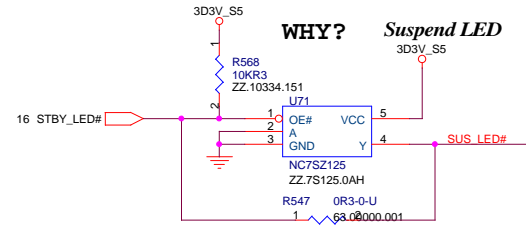
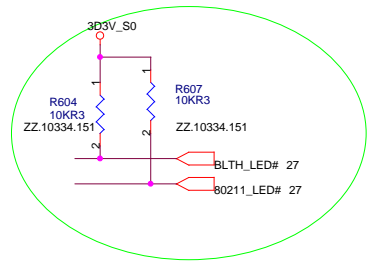
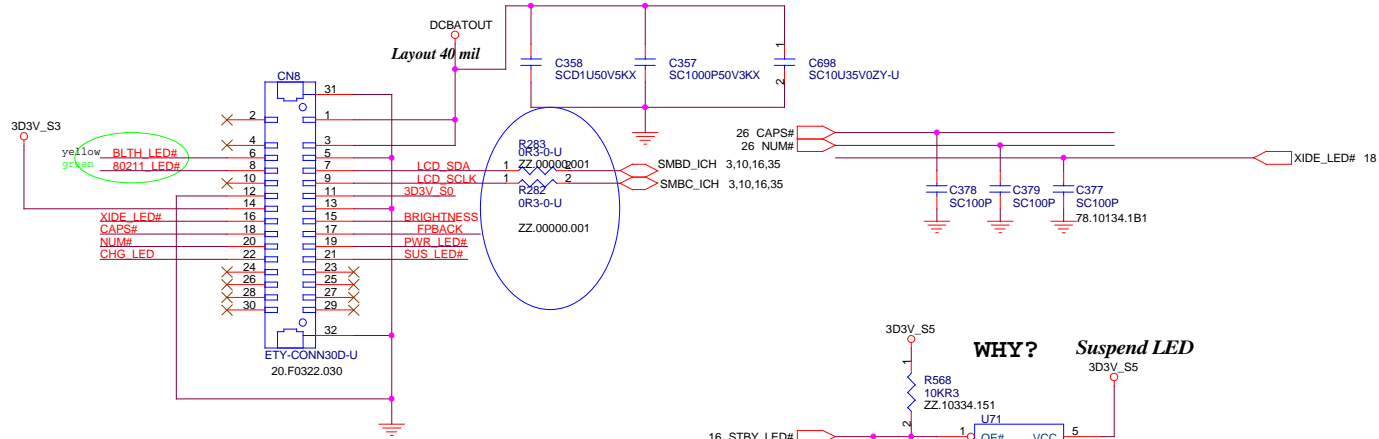


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Taipei Hsien 221, Taiwan, R.O.C.

Title		
DDR Serial/Terminator Resistor		
Size	Document Number	Rev
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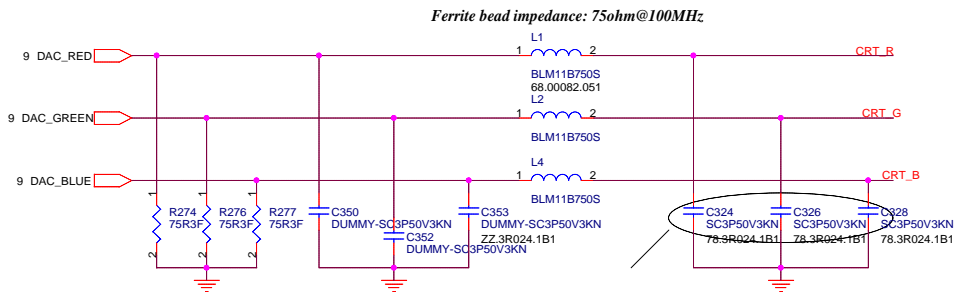


LCD / INVERTER INTERFACE



緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD/Inverter Connector			
Size	Document Number	Rev	
Custom	Pelican	SB	
Date:	Wednesday, November 17, 1999	Sheet	13 of 39

CRT I/F & CONNECTOR

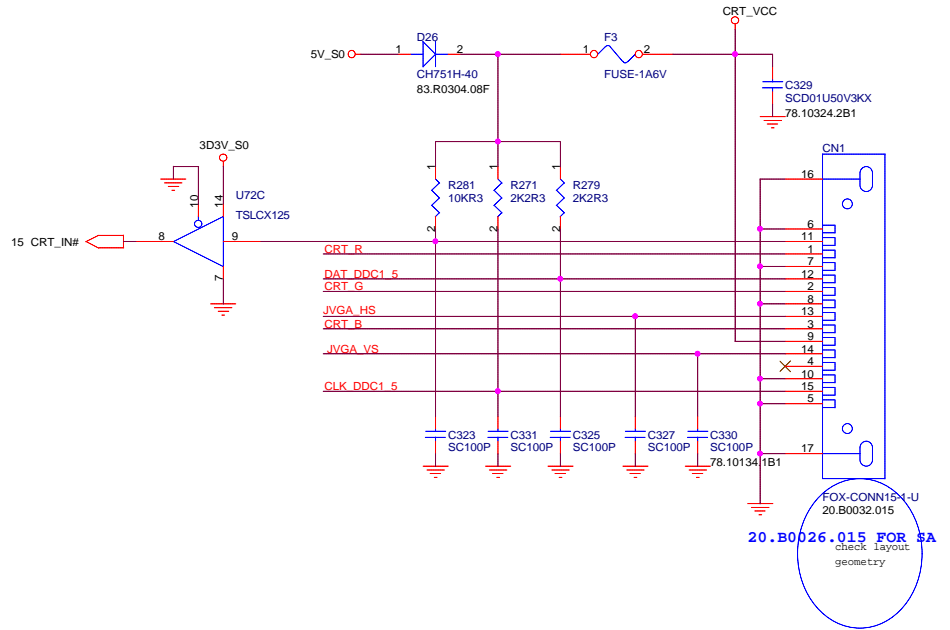


Layout Note:

- * Must be a ground return path between this ground and the ground on the VGA connector.
- * 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.

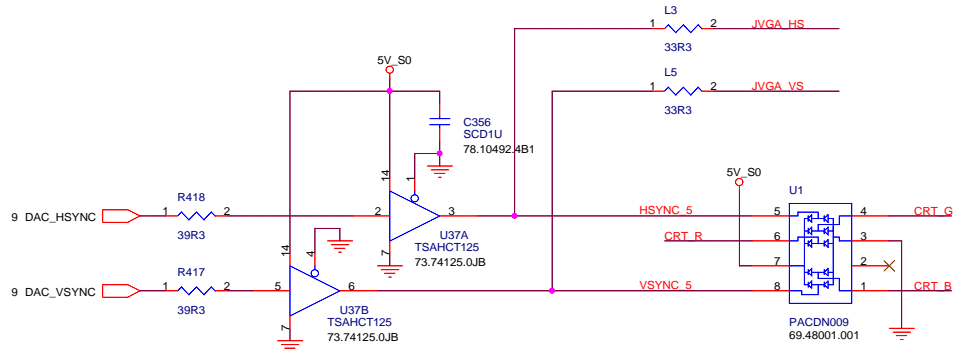
Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

RDDP 1.0

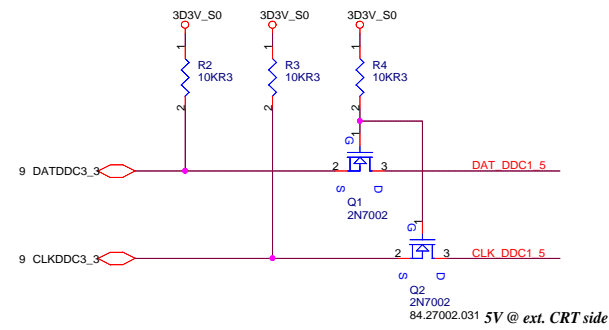


FOX-CONN154-U
20.B0032.015
20.B0026.015 FOR SA
check layout geometry

Hsync & Vsync level shift



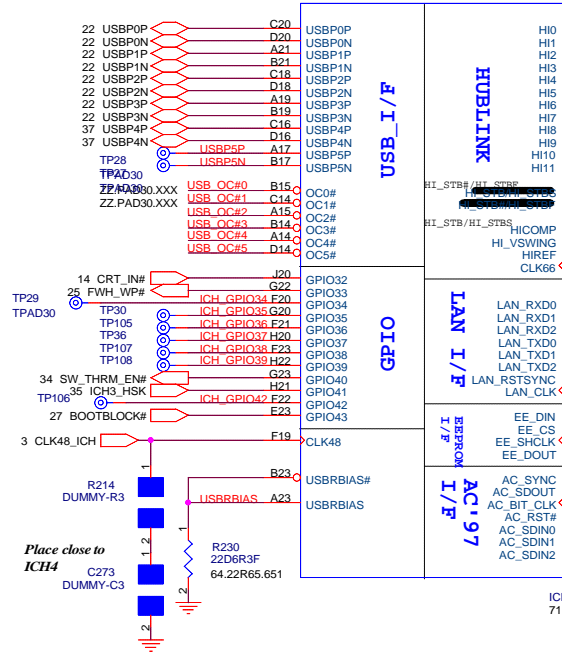
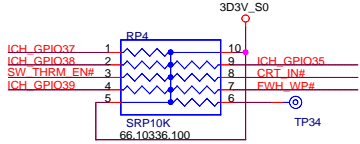
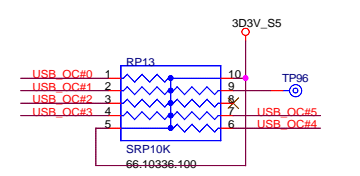
DDC_CLK & DATA level shift



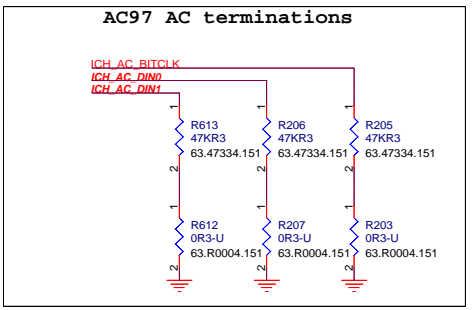
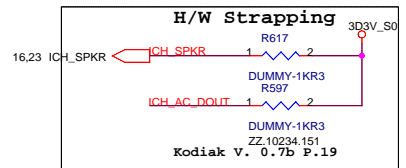
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CRT Connector			Rev SB
Size A3	Document Number Pelican		
Date: Wednesday, November 17, 1999	Sheet 14	of	39

U77A



$[(1.5-0.7)/0.7]*60 = 68 \text{ Ohm}$
60: trace impedance
Place near chip

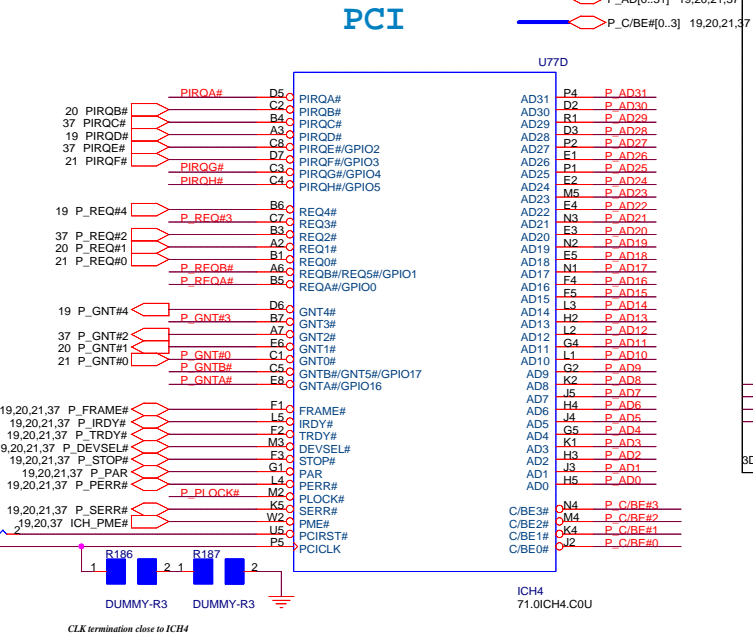


Place close to ICH4
C273
DUMMY-C3

ICH4 Integrated Pull-up and Pull-down Resistors

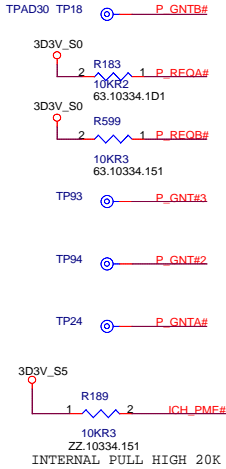
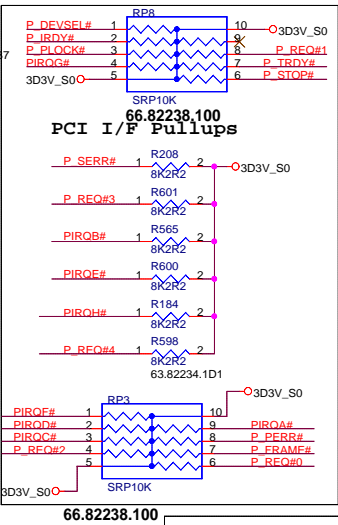
EE_DIN , EE_DOUT, LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	internal 20K pull-ups
LAN_RXD[2:0]	internal 10K pull-ups
AC_BITCLK, AC_SDIN[0] , AC_SDOUT, AC_SDIN[1]/GPIO[9] , AC_SYNC,	internal 20K pull-downs
SPKR	internal 20K pull-downs
PDD[7]/SDD[7] , PDDREQ / SDDREQ	internal 11.5K pull-downs
DPRSLPVR	internal 20K pull-downs
LAN_CLK	internal 100K pull-downs
USB[5:0][P,N]	internal 15K pull-downs

REF. NO. 11450 P.52



PCI

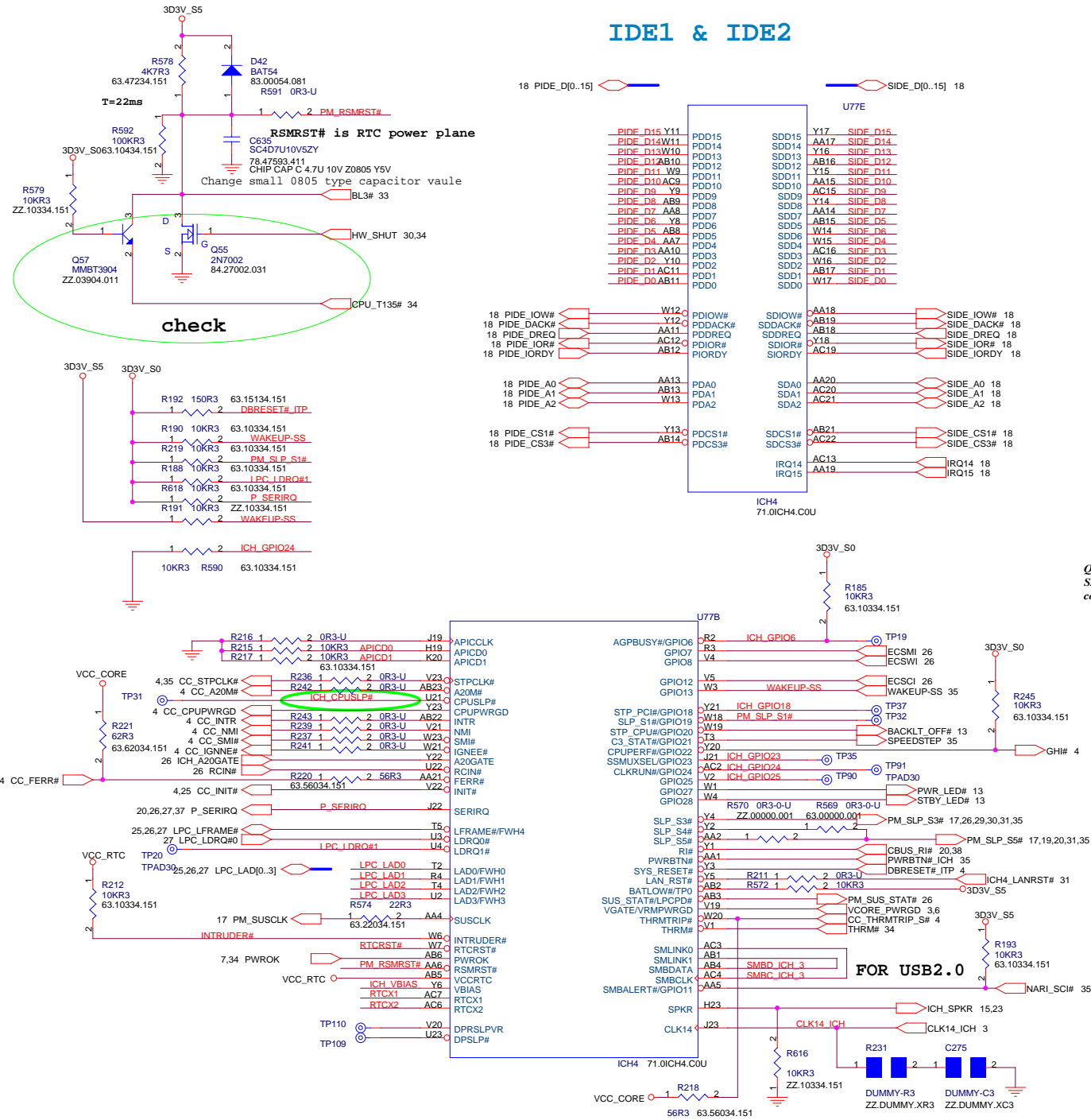
Interrupt I/F Pullups



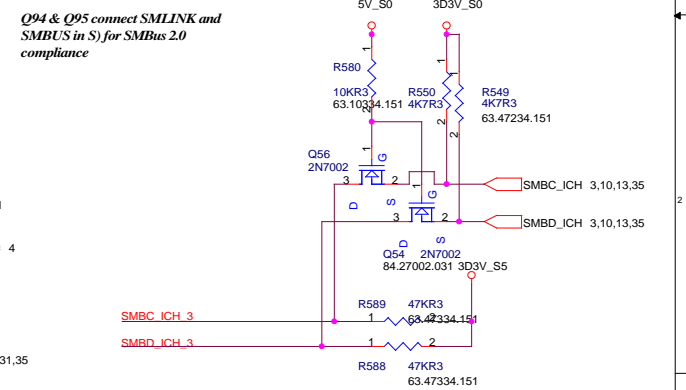
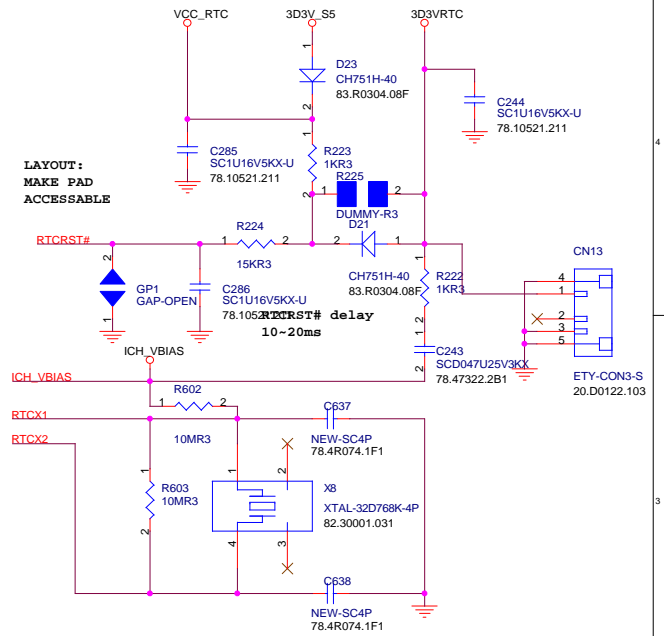
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH4(1/3)**
Size: A3 Document Number: Pelican Rev SB
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IDE1 & IDE2



RTC Circuitry

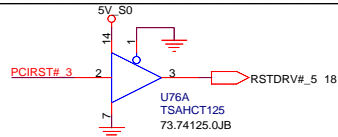
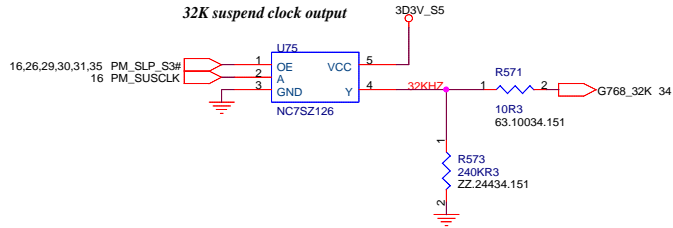


緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

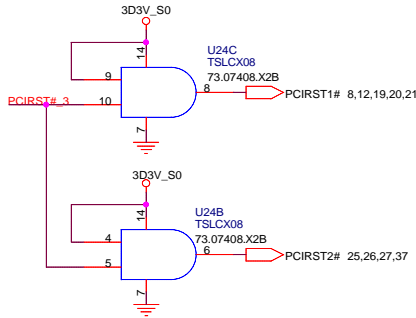
Title: **ICH4(2/3)**

Size A3	Document Number	Rev SB
Pelican		
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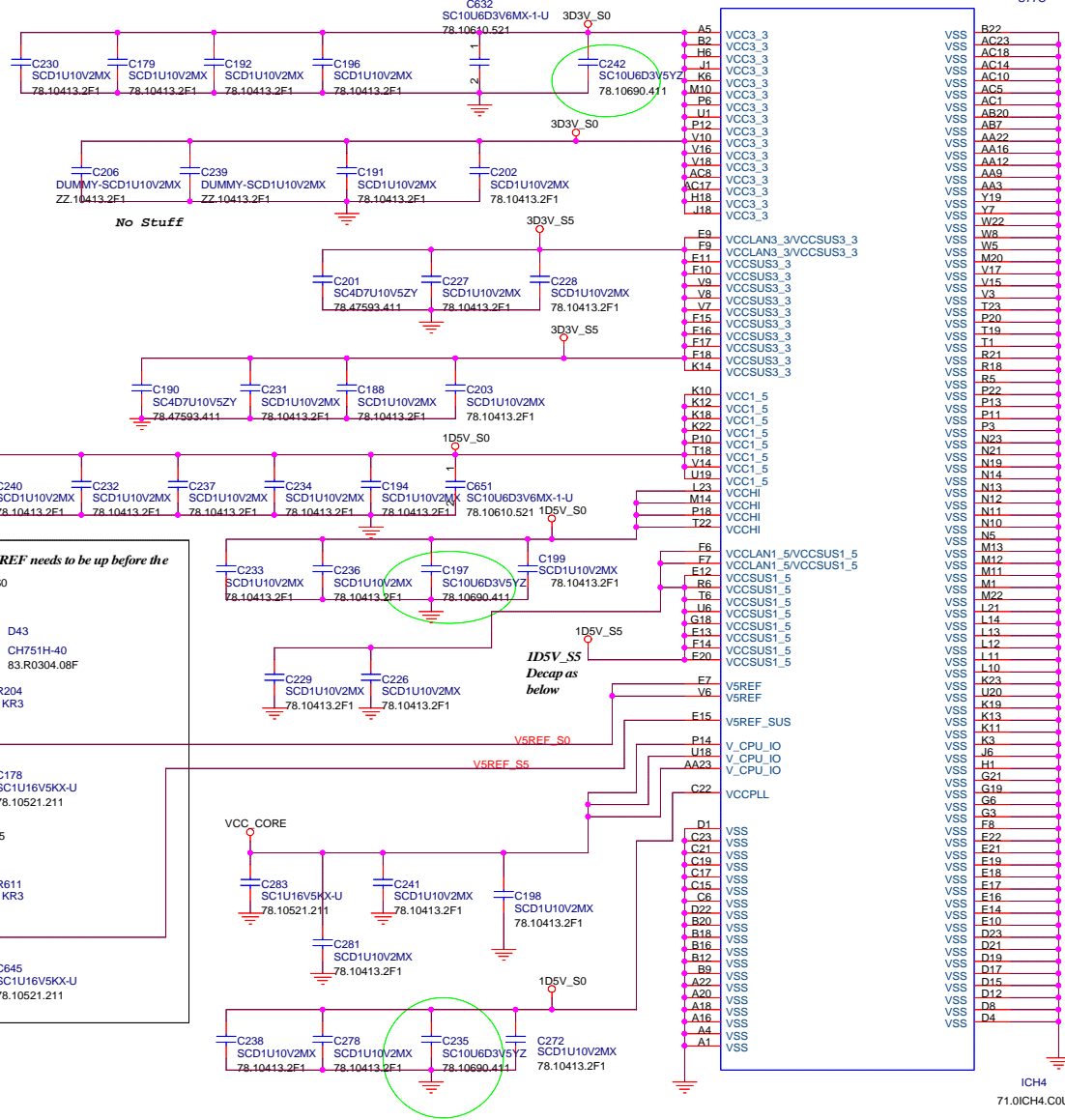
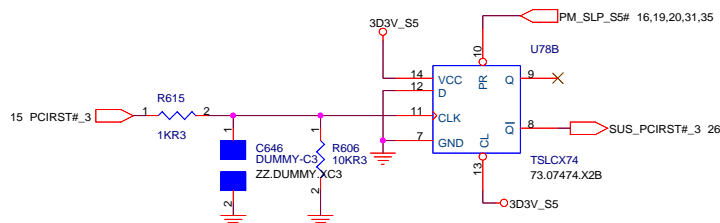
32K suspend clock output



PCIRST# 3V to 5V level shift for HDD & CDROM



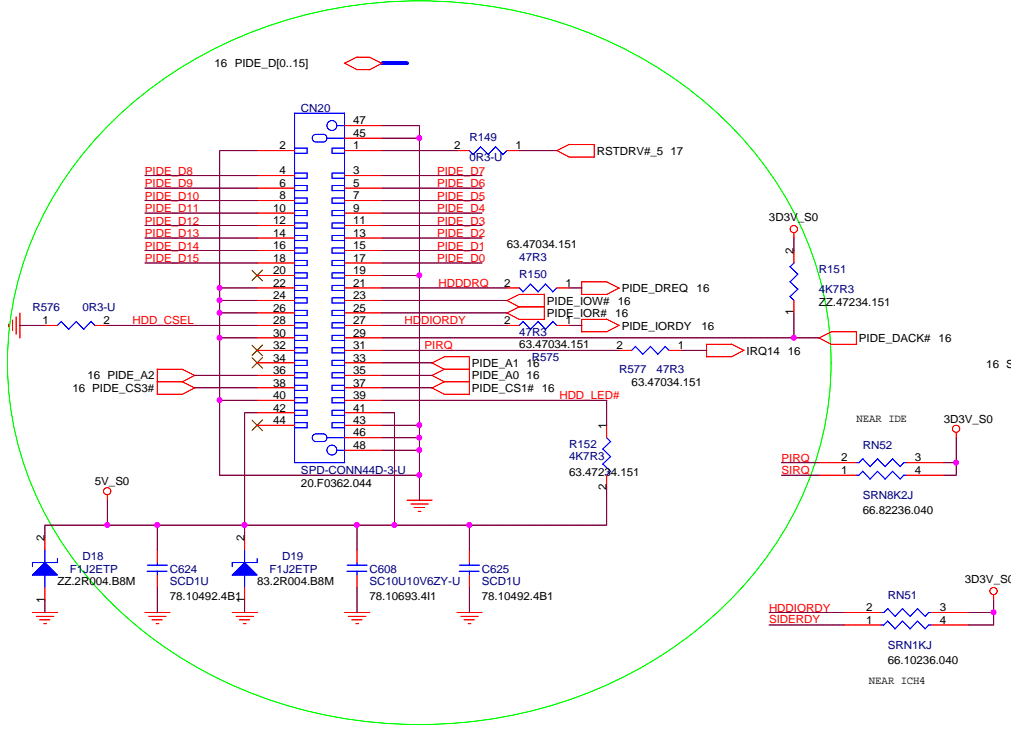
PCIRST# Buffer to enhance the driving strength



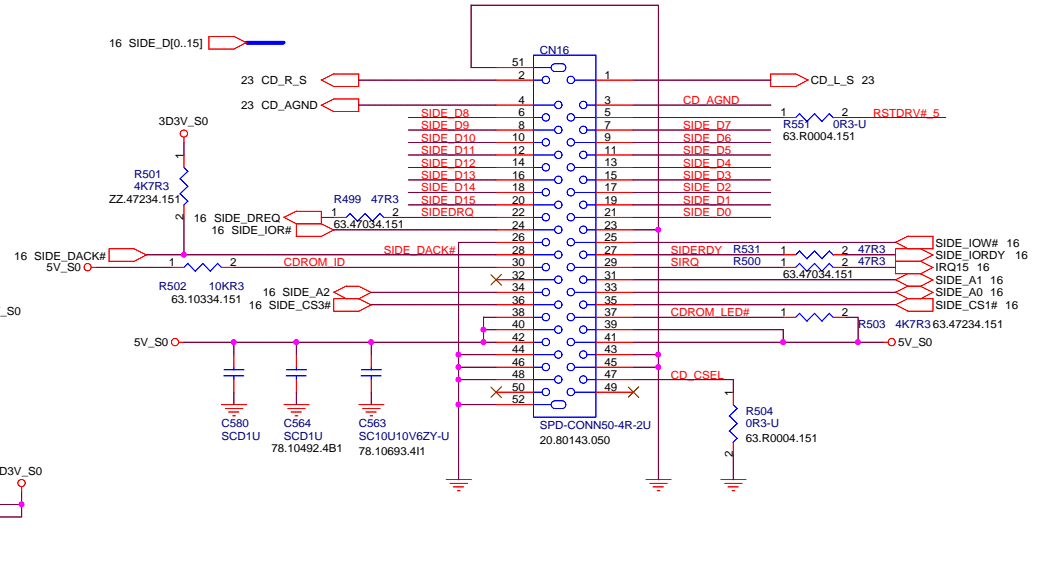
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH4(3/3)**
 Size: A3 Document Number: **Pelican** Rev: SB
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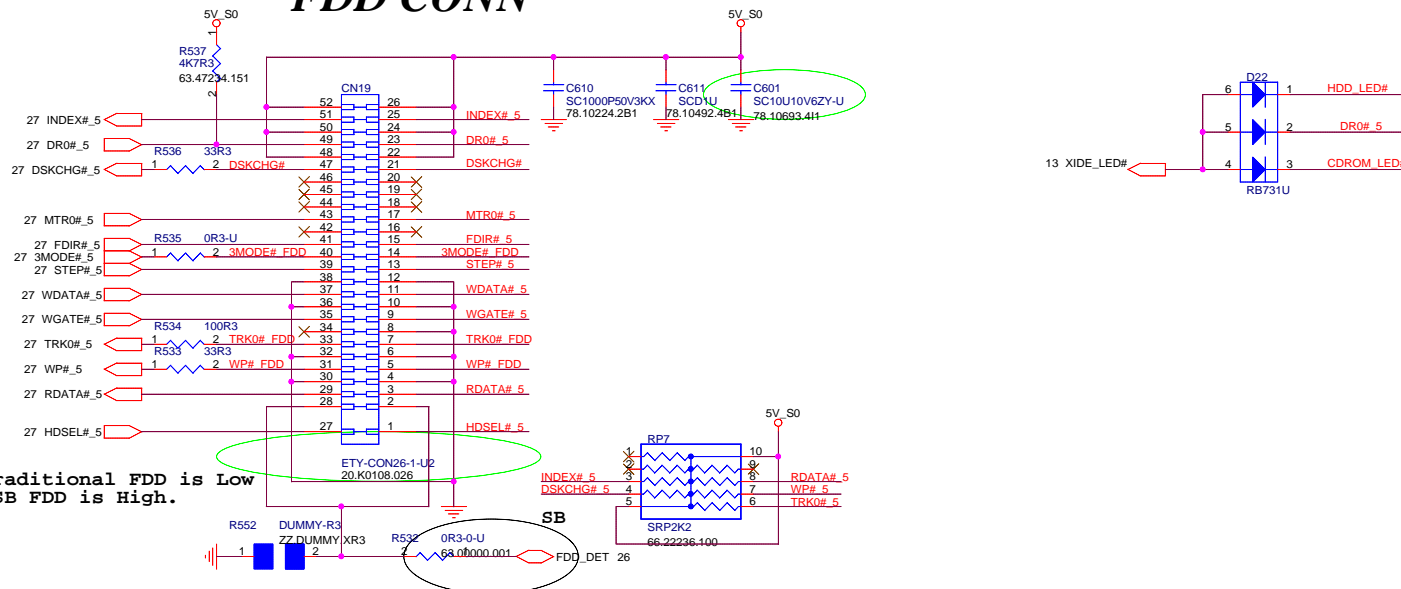
HDD CONN



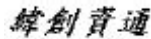
CD-ROM CONN

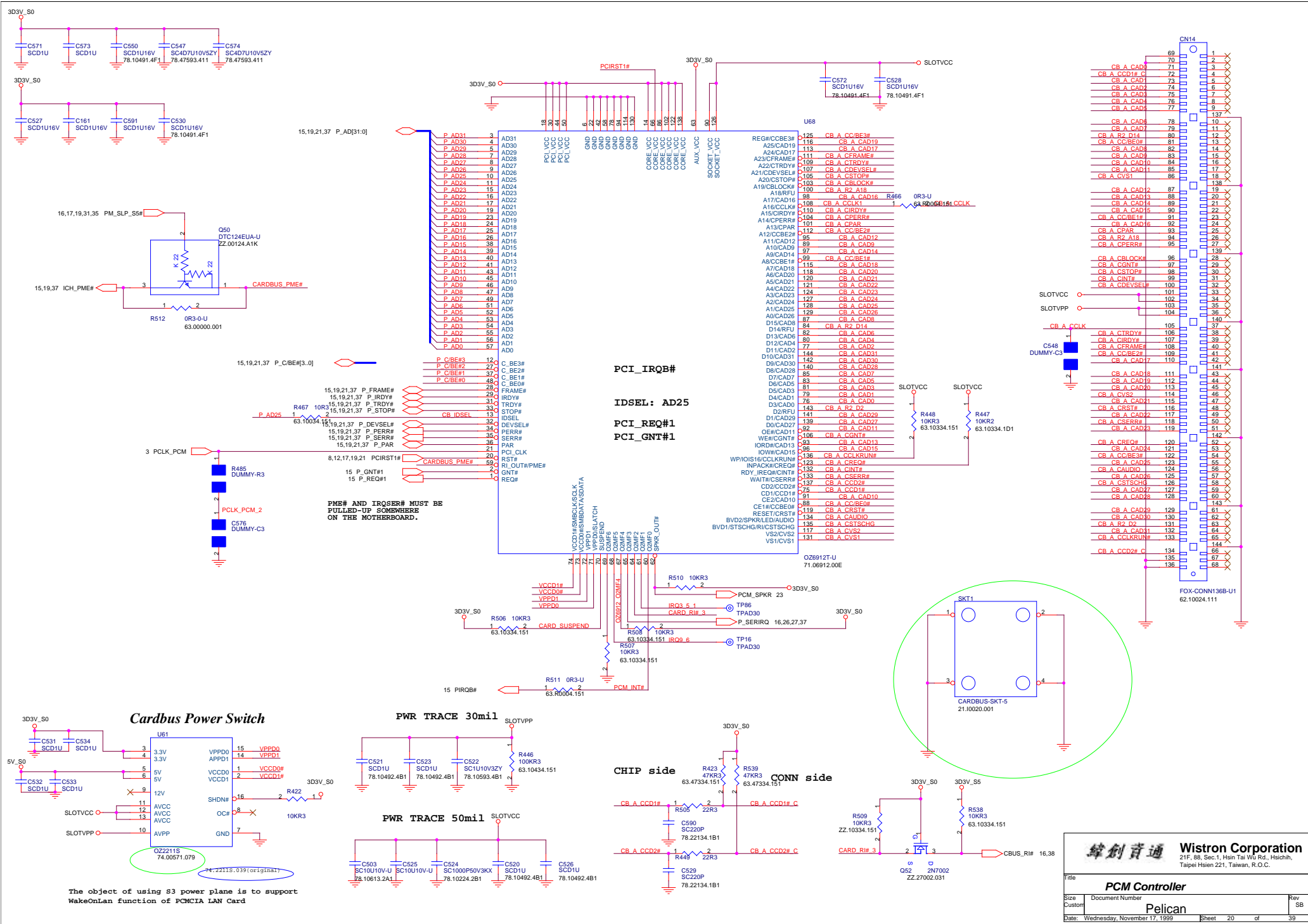


FDD CONN



Use Traditional FDD is Low
Use USB FDD is High.

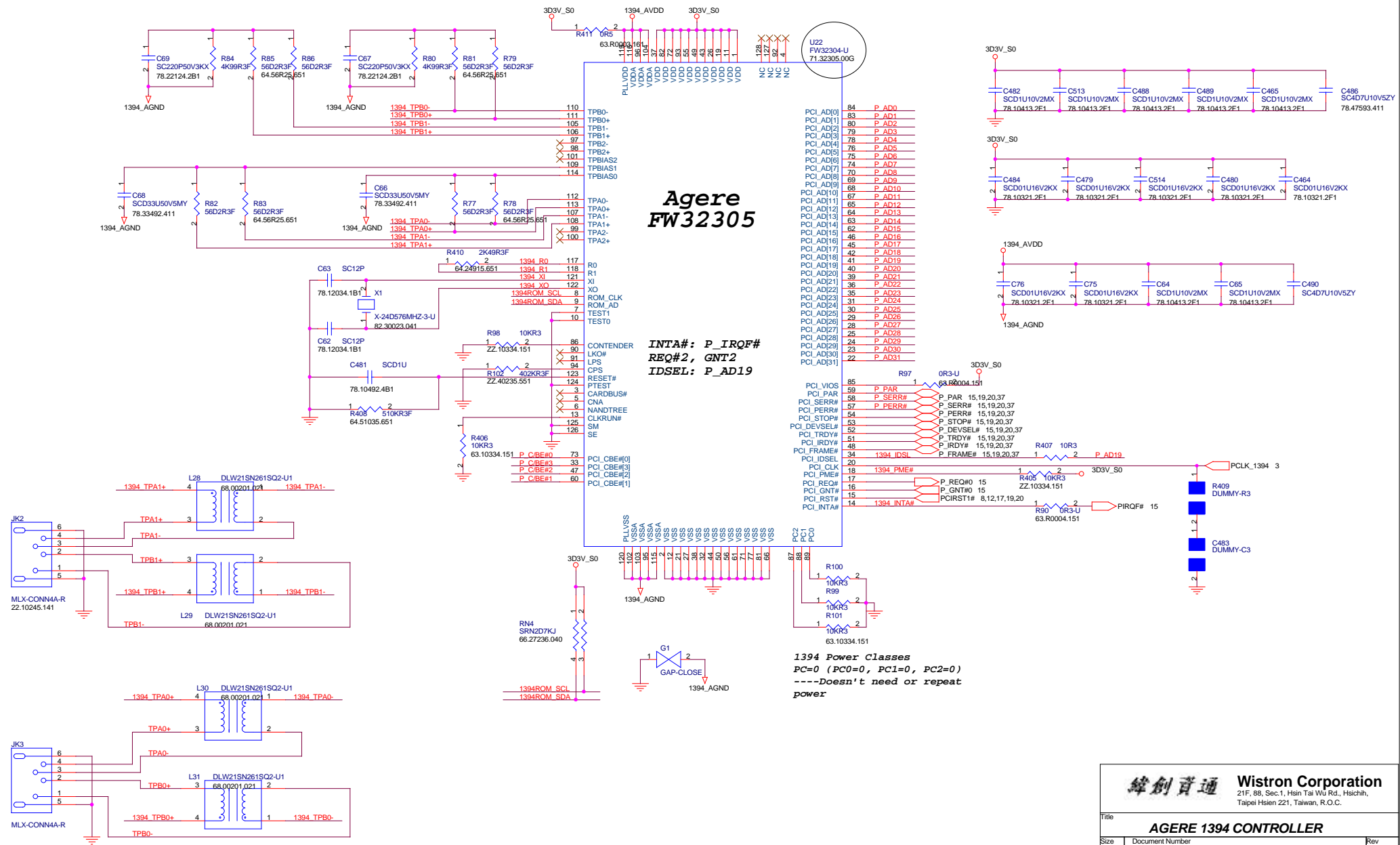
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title HDD and CDROM and FDD CONN		
Size A3	Document Number Pelican	Rev SB
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The object of using 53 power plane is to support WakeOnLan function of PCMCIA LAN Card

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		
PCM Controller		
Size	Document Number	Rev
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P_AD[31..0] 15,19,20,37
P_CBE[3..0] 15,19,20,37

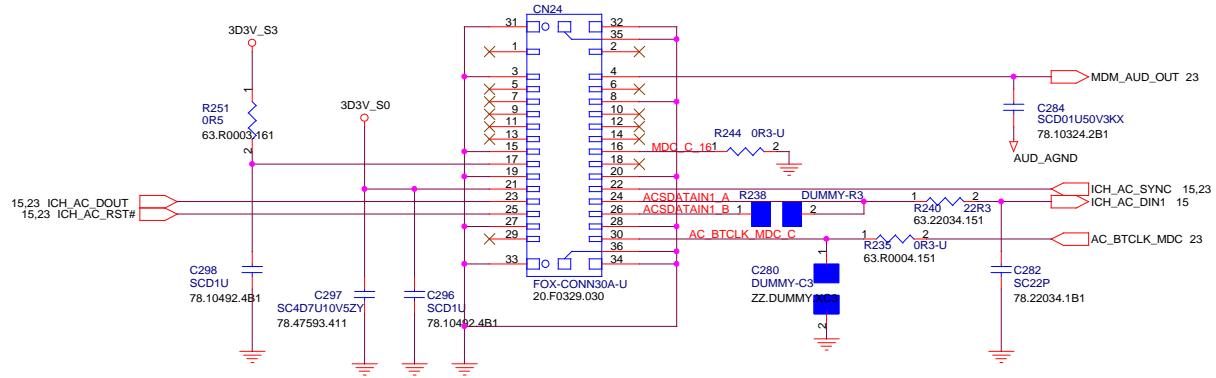


**INTA# : P_IRQF#
REQ#2, GNT2
IDSEL : P_AD19**

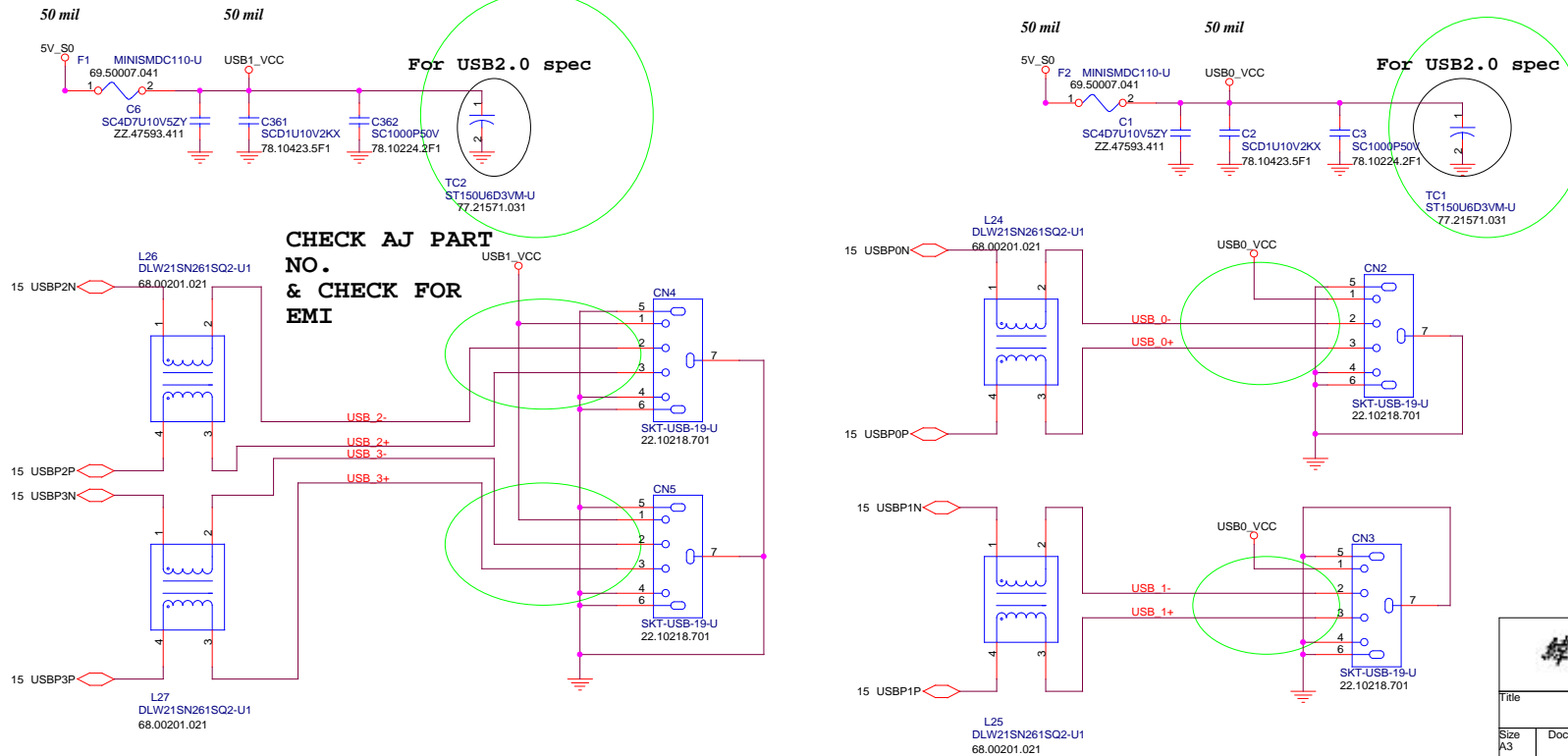
**1394 Power Classes
PC=0 (PC0=0, PC1=0, PC2=0)
----Doesn't need or repeat
power**

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title AGERE 1394 CONTROLLER			
Size	Document Number	Pelican	
Custom			Rev SB
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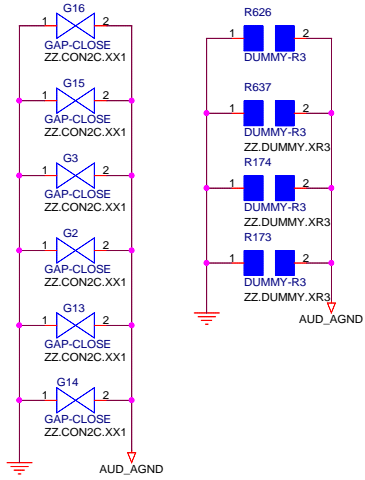
MDC Connector



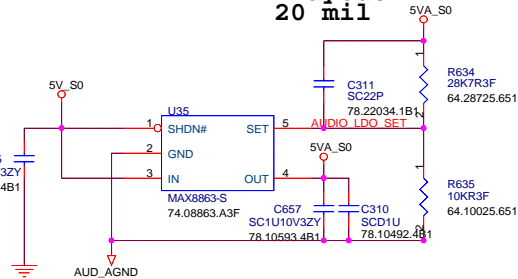
USB PORT



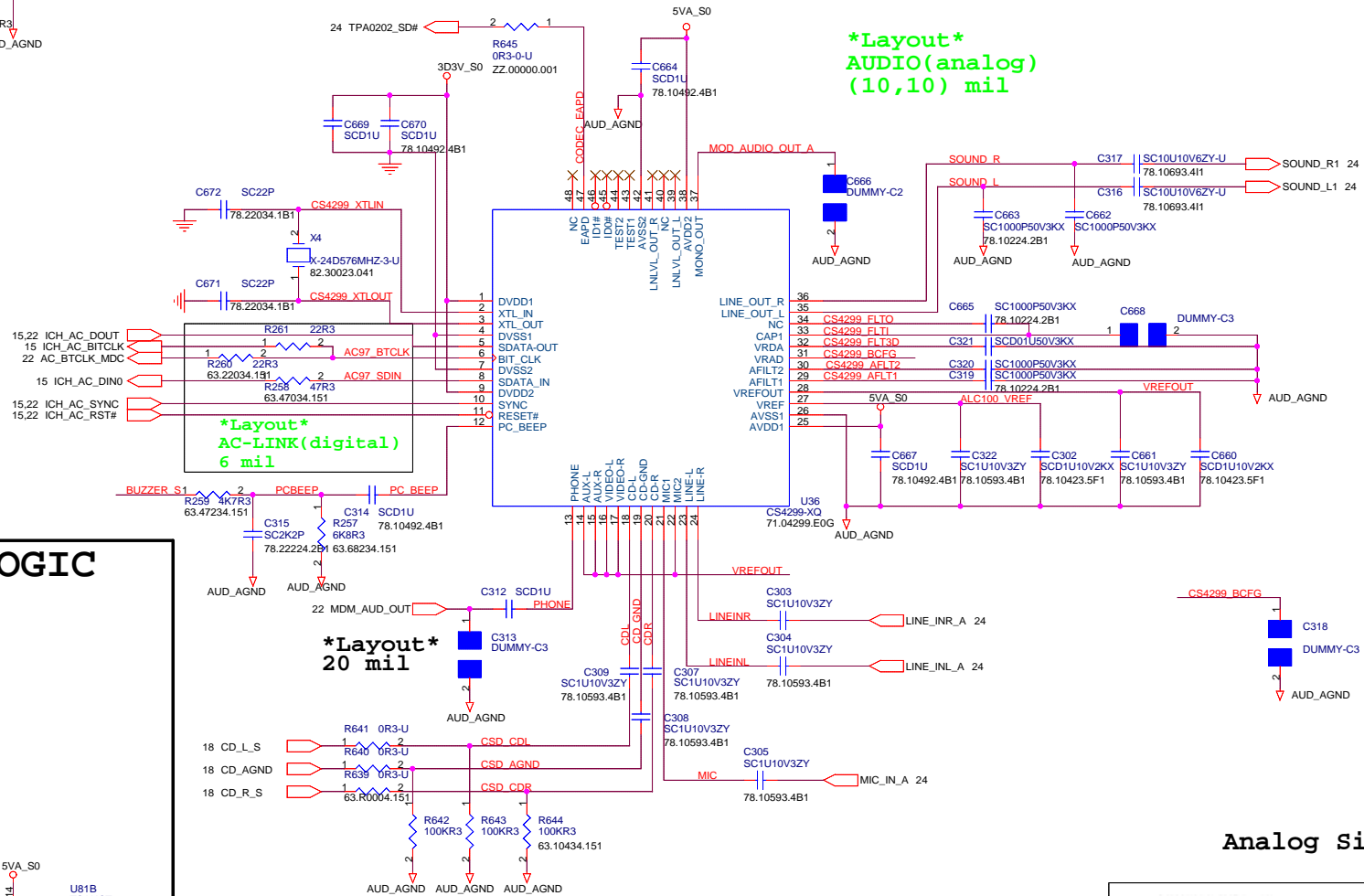
CUT MOAT



***Layout*
20 mil**

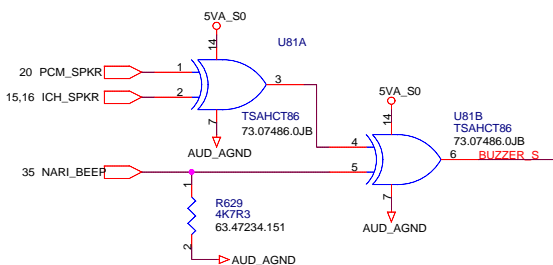


***Layout*
AUDIO(analog)
(10,10) mil**



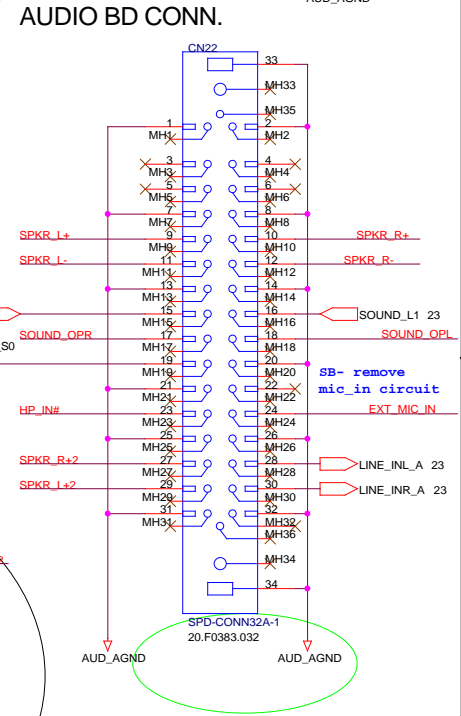
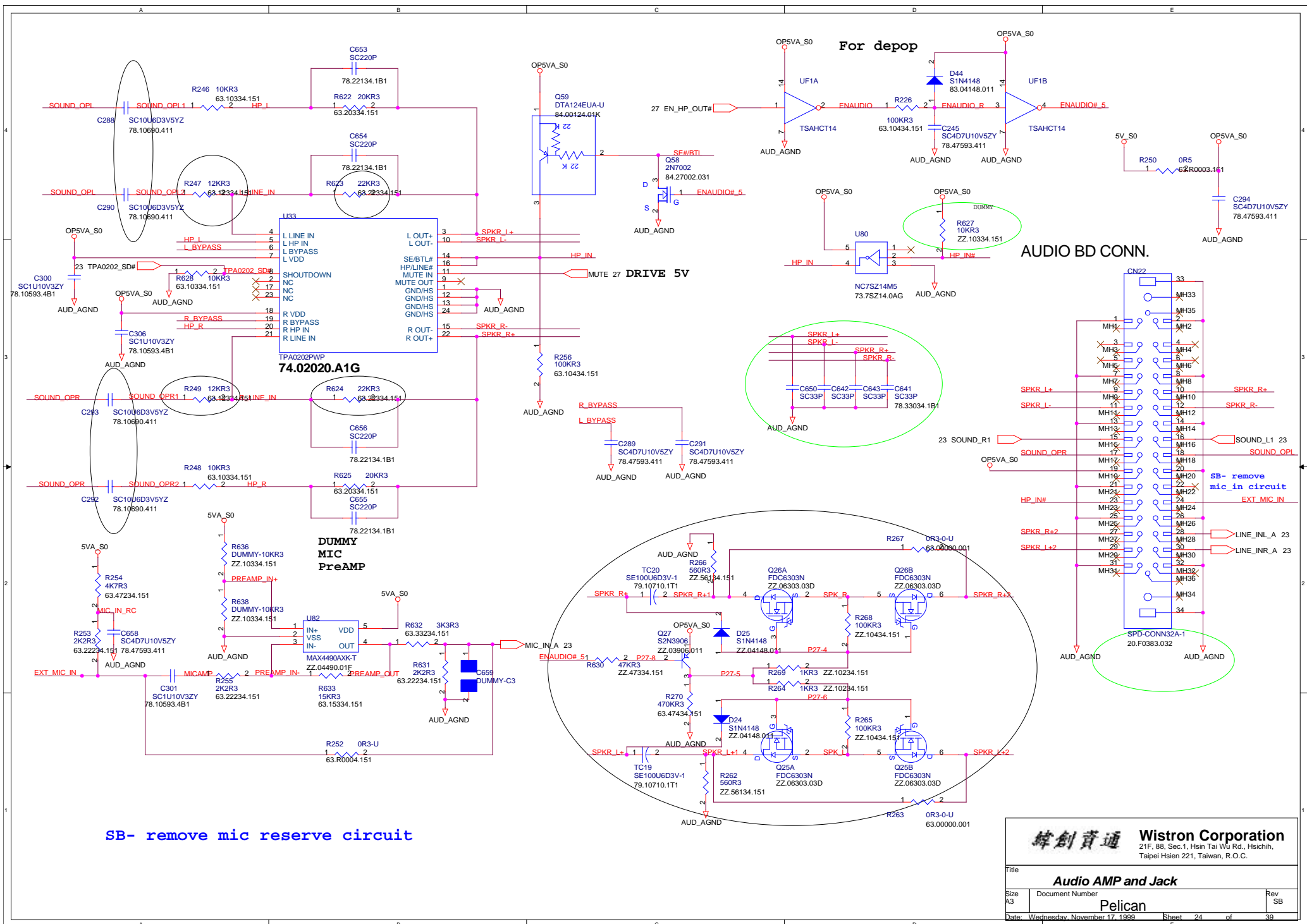
BEEP SOUND LOGIC

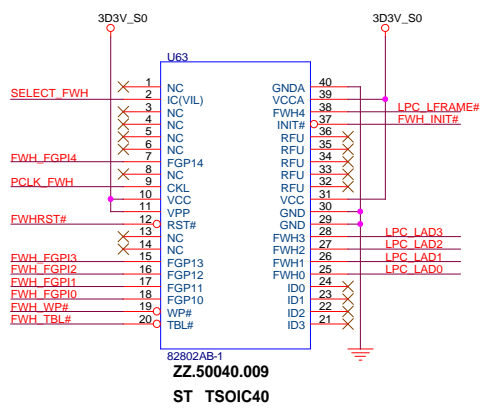
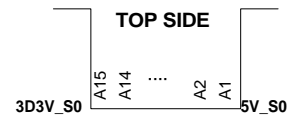
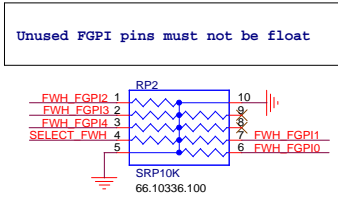
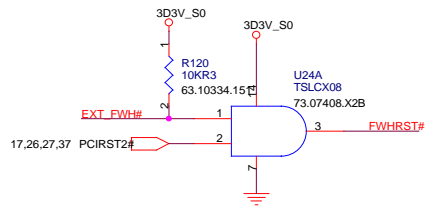
Layout
locate near audio
moat opening 6
mil



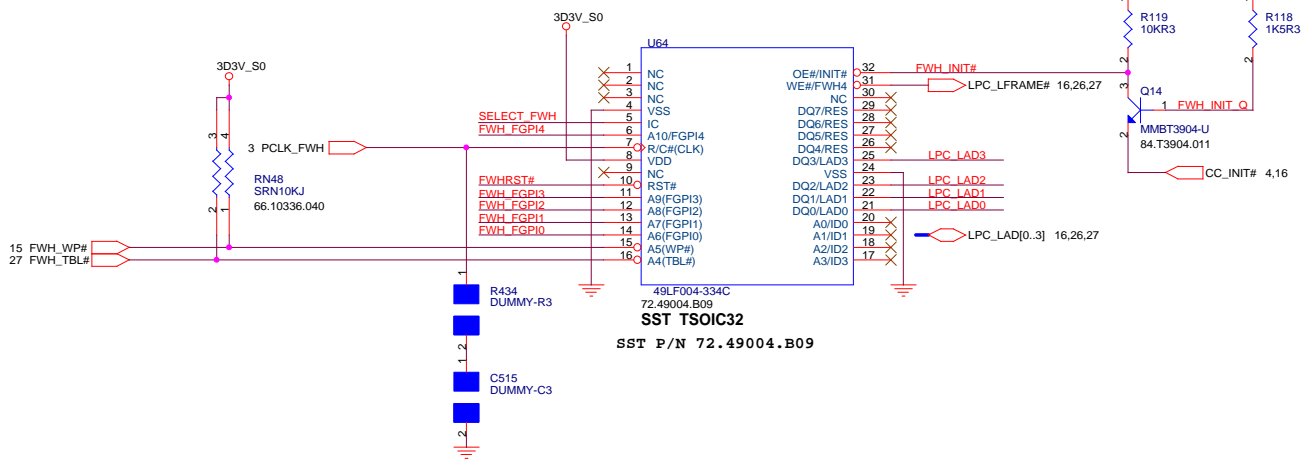
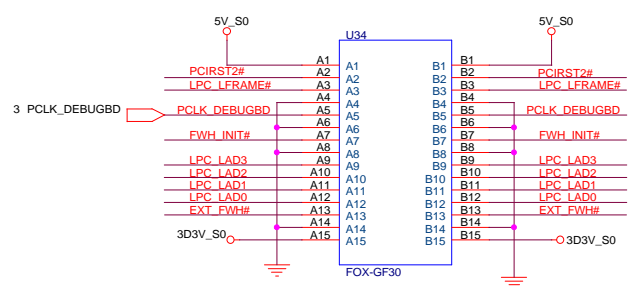
Analog Signal

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AC97 Codec	
Size	Document Number
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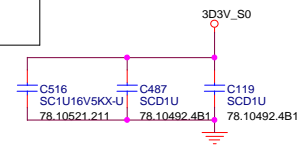


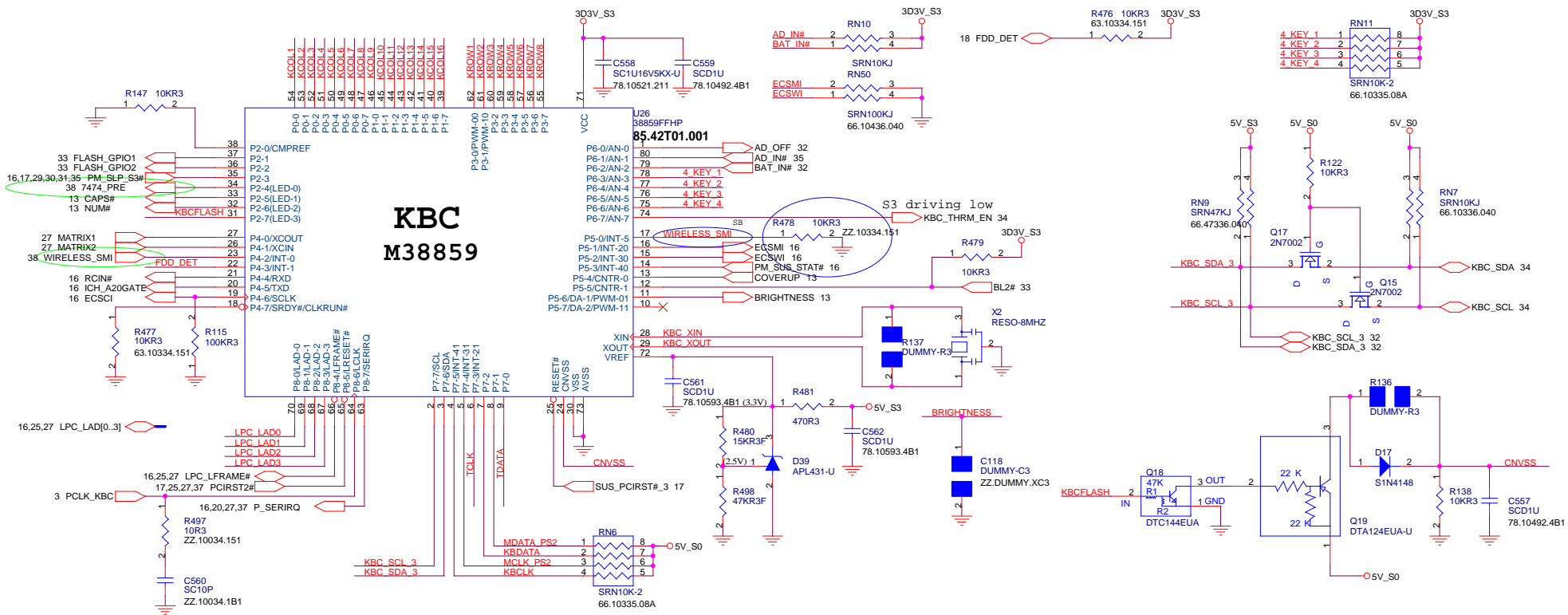


GOLDEN FINGER FOR DEBUG BOARD



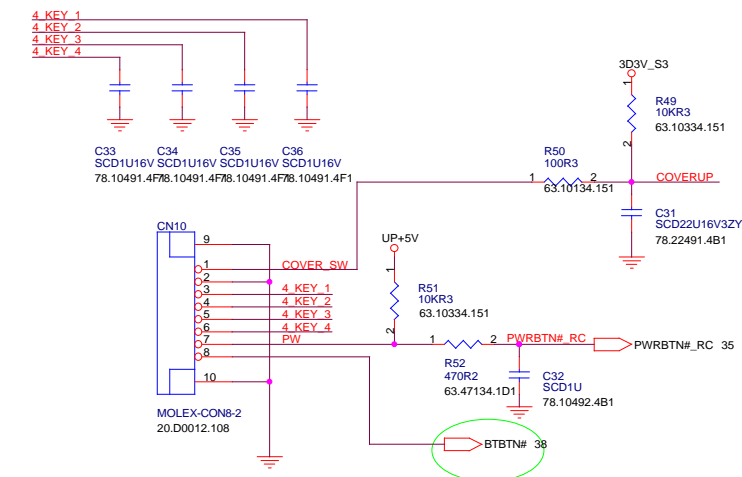
Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46



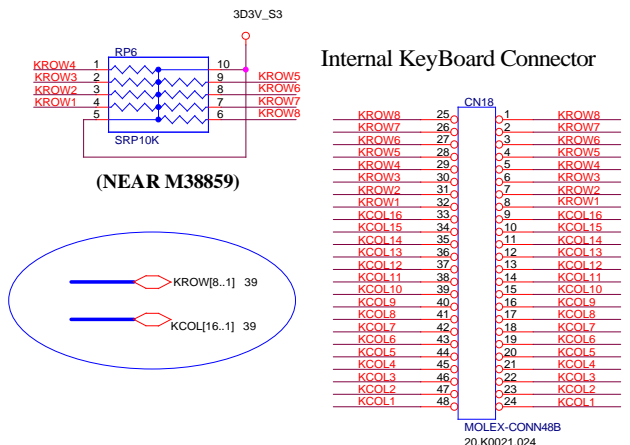


KBC M38859

TouchPad Connector



POWER SWITCH



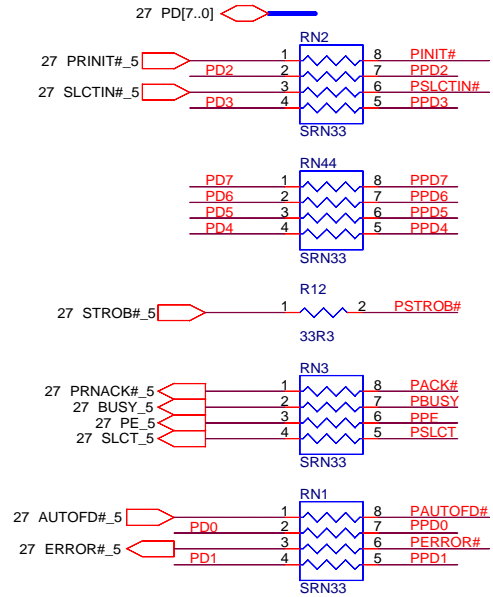
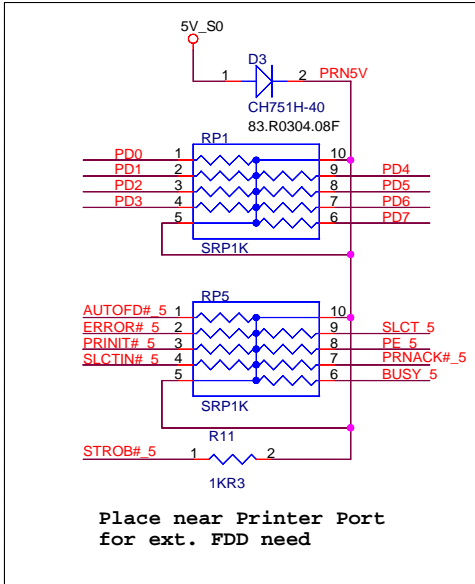
Internal Keyboard Connector

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

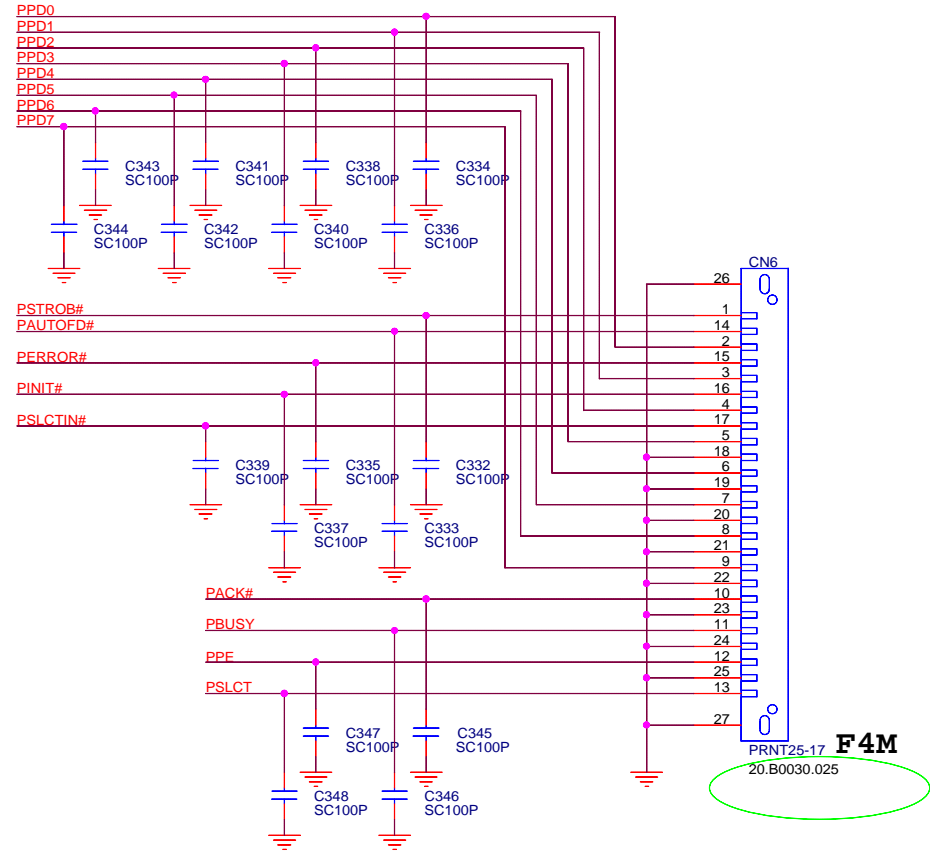
Title: **KBC**

Size: A3	Document Number: Pelican	Rev: SB
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Place CAPs close to CONN **Printer Port**



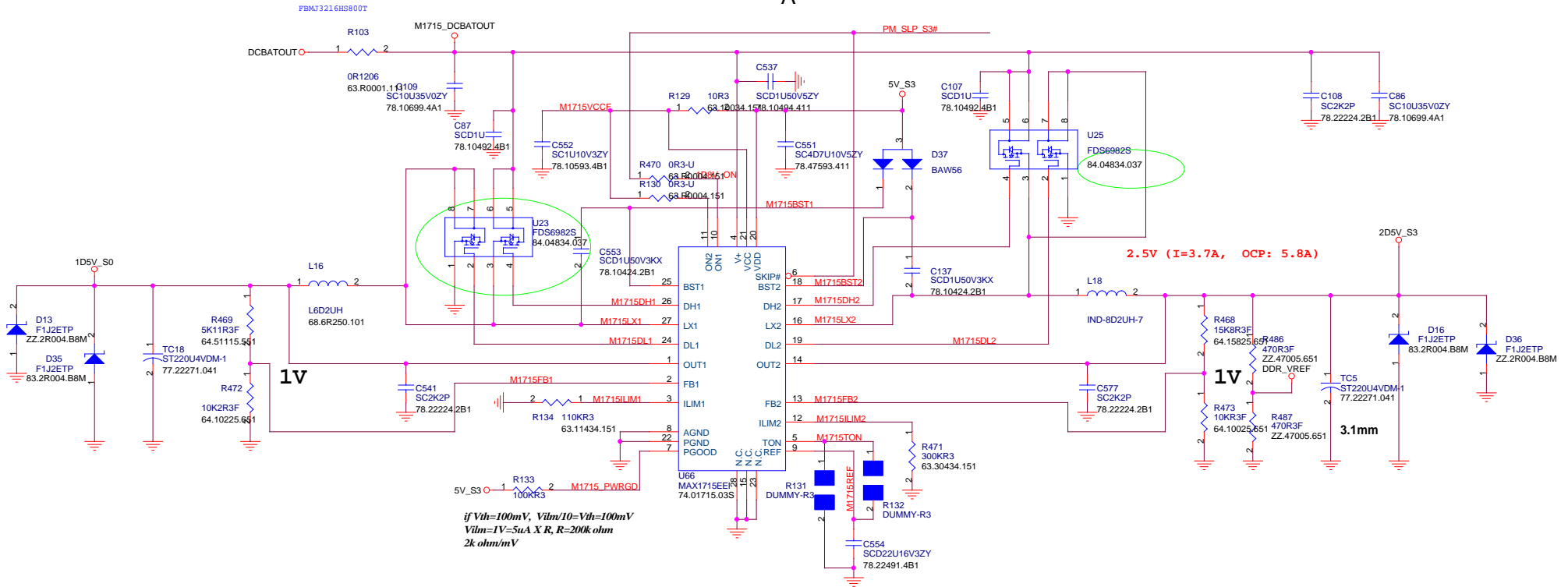
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **Parallel Port**

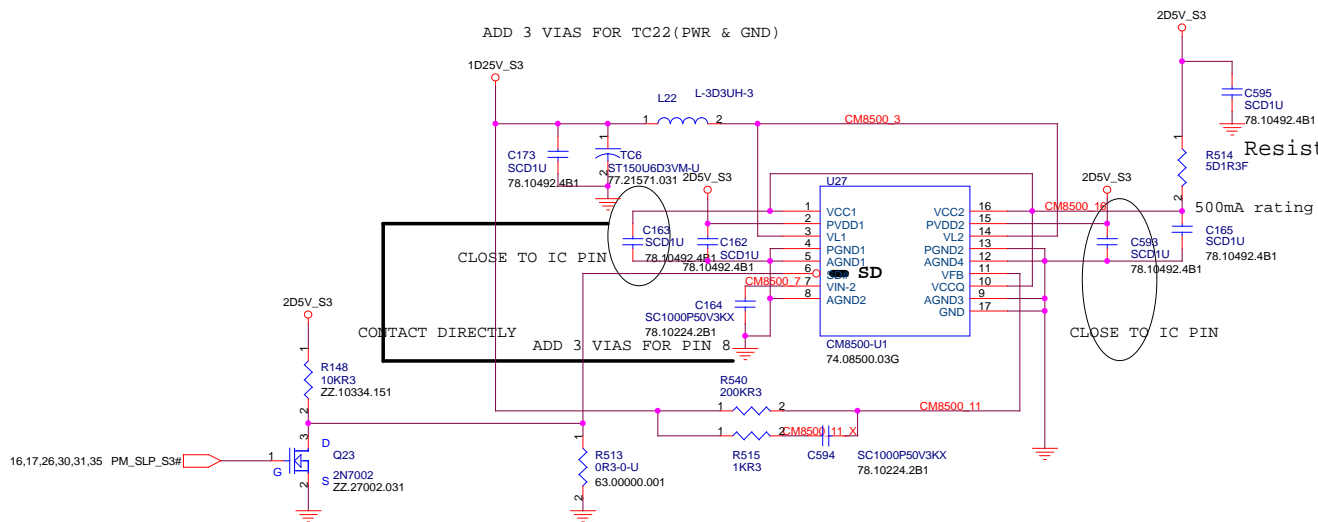
Size Custom Document Number **Pelican** Rev SB

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A



ADD 3 VIAS FOR TC22(PWR & GND)



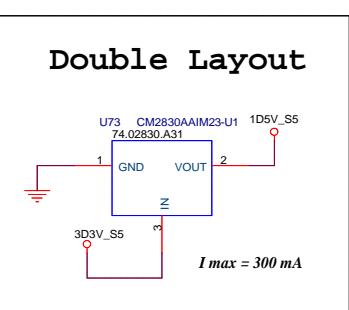
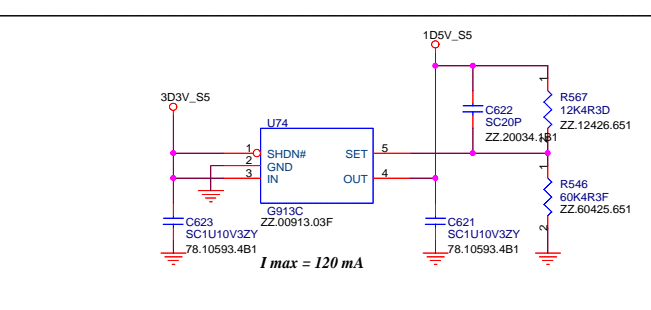
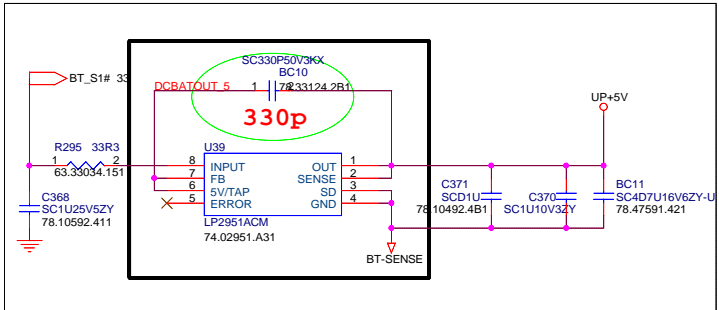
Resistor Rating

500mA rating

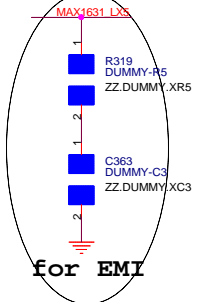
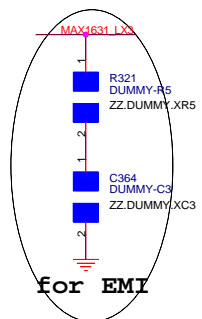
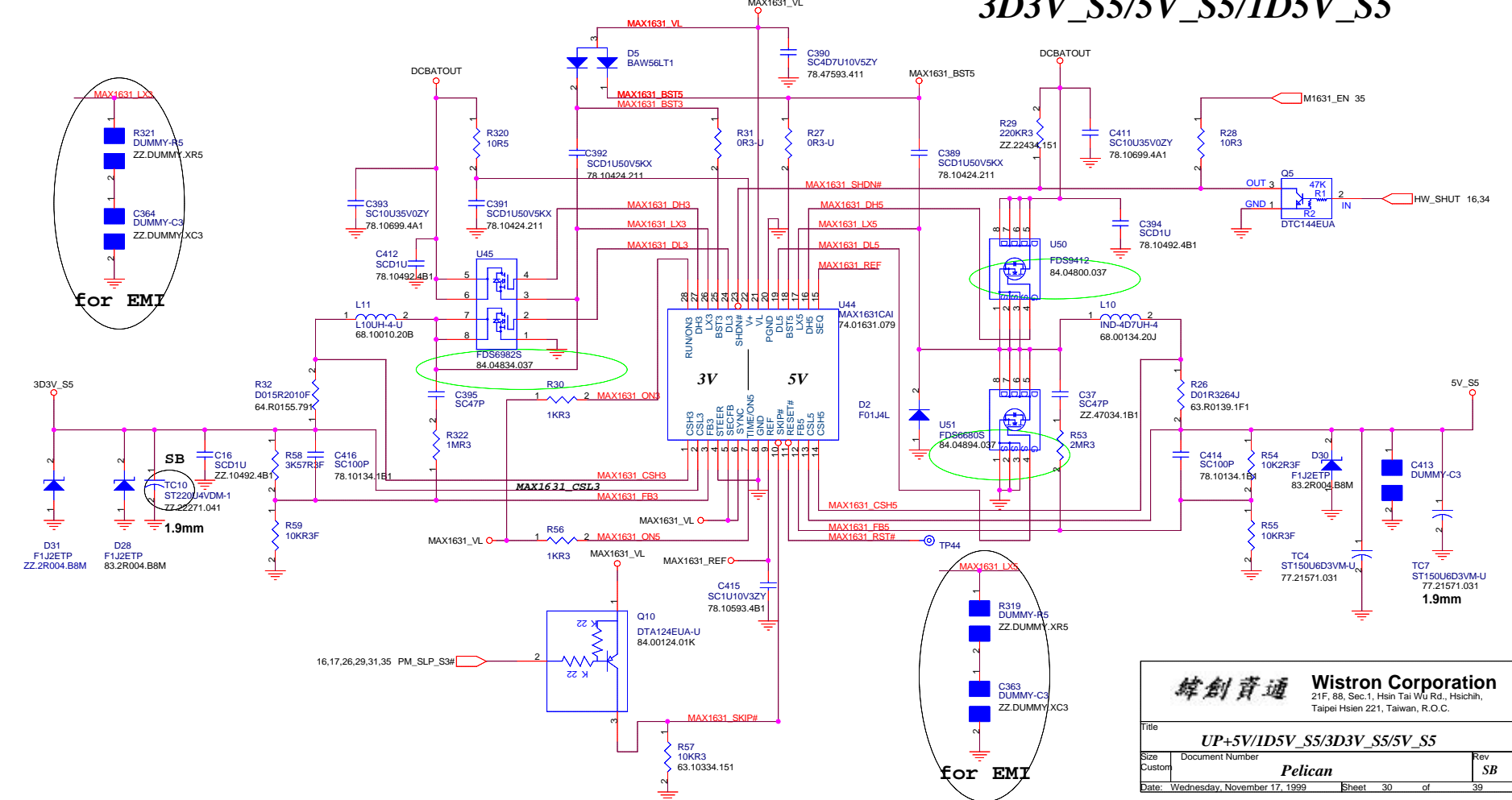
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			
2D5V_S3/1D25V_S3/1D5V_S0			
Size	Document Number	Rev	SB
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A



SYSTEM DC/DC 3D3V_S5/5V_S5/1D5V_S5



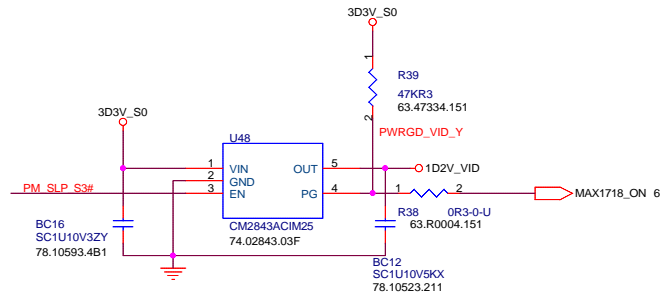
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **UP+5V/1D5V_S5/3D3V_S5/5V_S5**

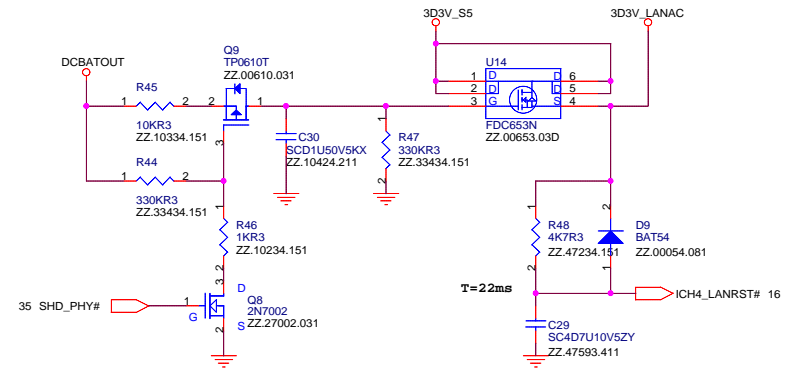
Size	Document Number	Rev
Custom	Pelican	SB
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CPU VID(1D2V)

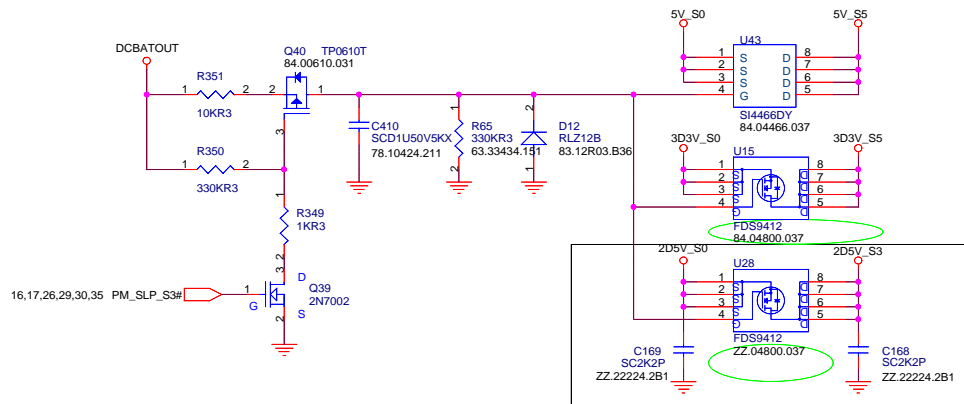
SPEC. FOR DT NORTHWOOD CPU =>150mA
 FOR MB NORTHWOOD CPU =>300mA
 MB NORTHWOOD CPU ACTUAL CURRENT=23mA



3D3V_S5 — FDC653N —> 3D3V_LANAC

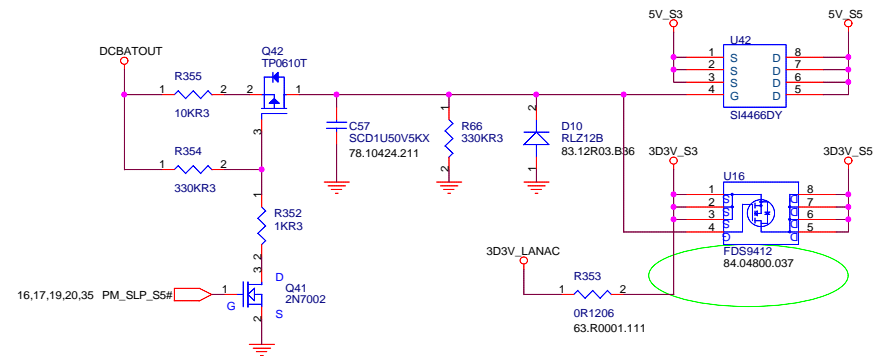


Run Power



Suspend Power

Support standby wakeup LAN only

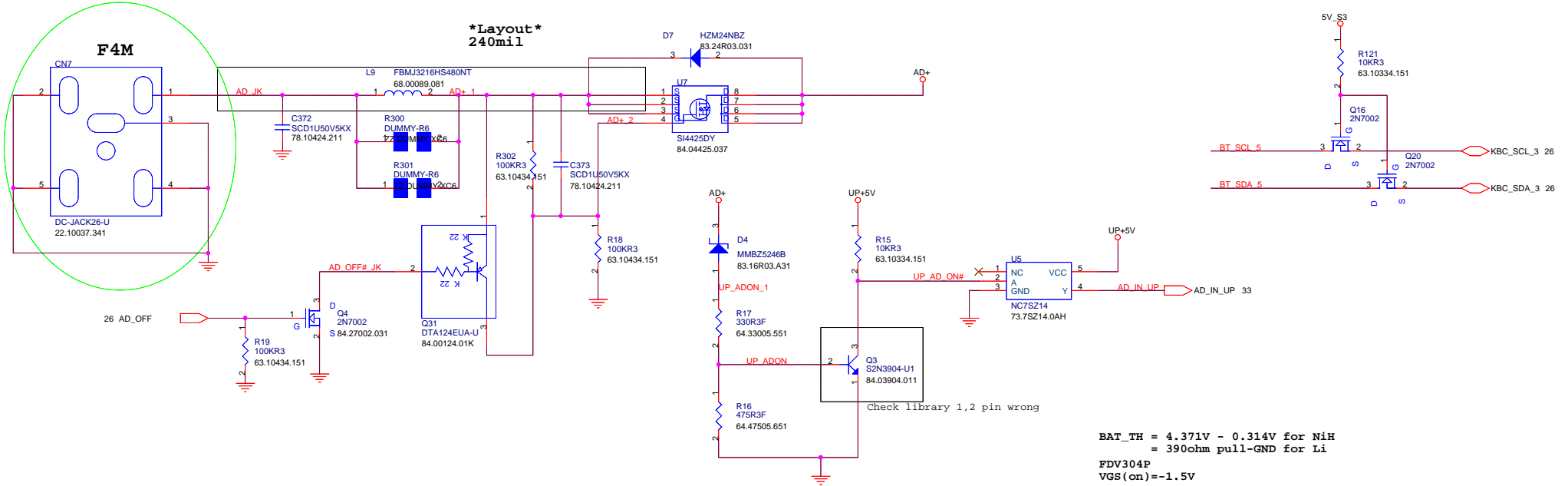


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
PWRPLANE&RESETLOGIC		
Size	Document Number	Rev
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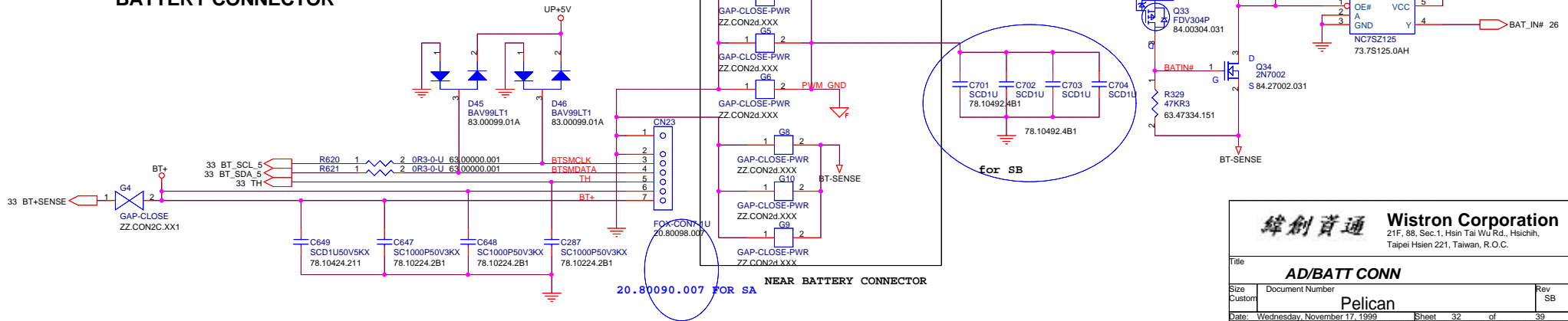
Adaptor in to generate DCBATOUT

Layout
240mil



BAT_TH = 4.371V - 0.314V for NiH
= 390ohm pull-GND for Li
FDV304P
VGS(on)=-1.5V

BATTERY CONNECTOR



緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien Z21, Taiwan, R.O.C.	
Title AD/BATT CONN	
Size	Document Number
Custom	Pelican
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Charger Max
Current Sensor
Scaling 20mV/A

R51 MUST BE AS CLOSS TO
U20 PIN6 AS POSSIBLE

THE TRACE LENGTH FOR U20
PIN 6 & PIN 7 MUST BE THE
SAME

R42 MUST BE AS CLOSS TO
U20 PIN4 AS POSSIBLE

THE TRACE LENGTH FOR U20
PIN 4 & PIN 5 MUST BE THE
SAME

Adapter Max
Current Sensor
40mv/15m ohm=2.6 A

DCBATOUT1

Layout
200mil

CHECK F3M

Layout
100mil

Layout
200mil

BT+
♀

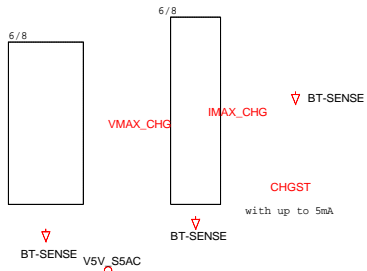
Layout
200mil

注意O/P電容

6/8
Imax = $R74 / (R75 + R74) * Vref(2.5v) * 2$
(2A/V) = 4A

Vmax = $R59 / (R60 + R59) * Vref(2.5v) * 10$
= 17.00V

OZ_VREF



CHG_HDR1

BC485 MUST BE AS CLOSS TO
U20 PIN1 AND PIN 3 AS POSSIBLE

BC490 MUST BE AS CLOSS TO
U20 PIN 26 AND PIN 28 AS
POSSIBLE

CHG_CHIGH
CHG_GAC
CHG_HDR BT-SENSE
CHG_LDR
CHG_CLOW

CHG_LDR1

CHGST

CHGST_G

CHGST_G#_1

CHGST_G#

CHG_IChP
CHG_IChM

CHG_GCH
CHG_COMP BT-SENSE V5V_S5AC
CHG_COMP_1

BT_S1#

243KR3F

ADINUP

BT_S1#_1

4.2V

357KR5F

換C0版本 SB

CHECK F3M

AD_IN_UP

FLASH_GPIO2_1
FLASH2 UP+5V ♀

CHARGE_LED#

FLASH_GPIO2_ADIN

CHARGER MicroP

♀

FLASH1

BT_SCL_5
BT_SDA_5

FLASH_GPIO1_1
FLASH1_1

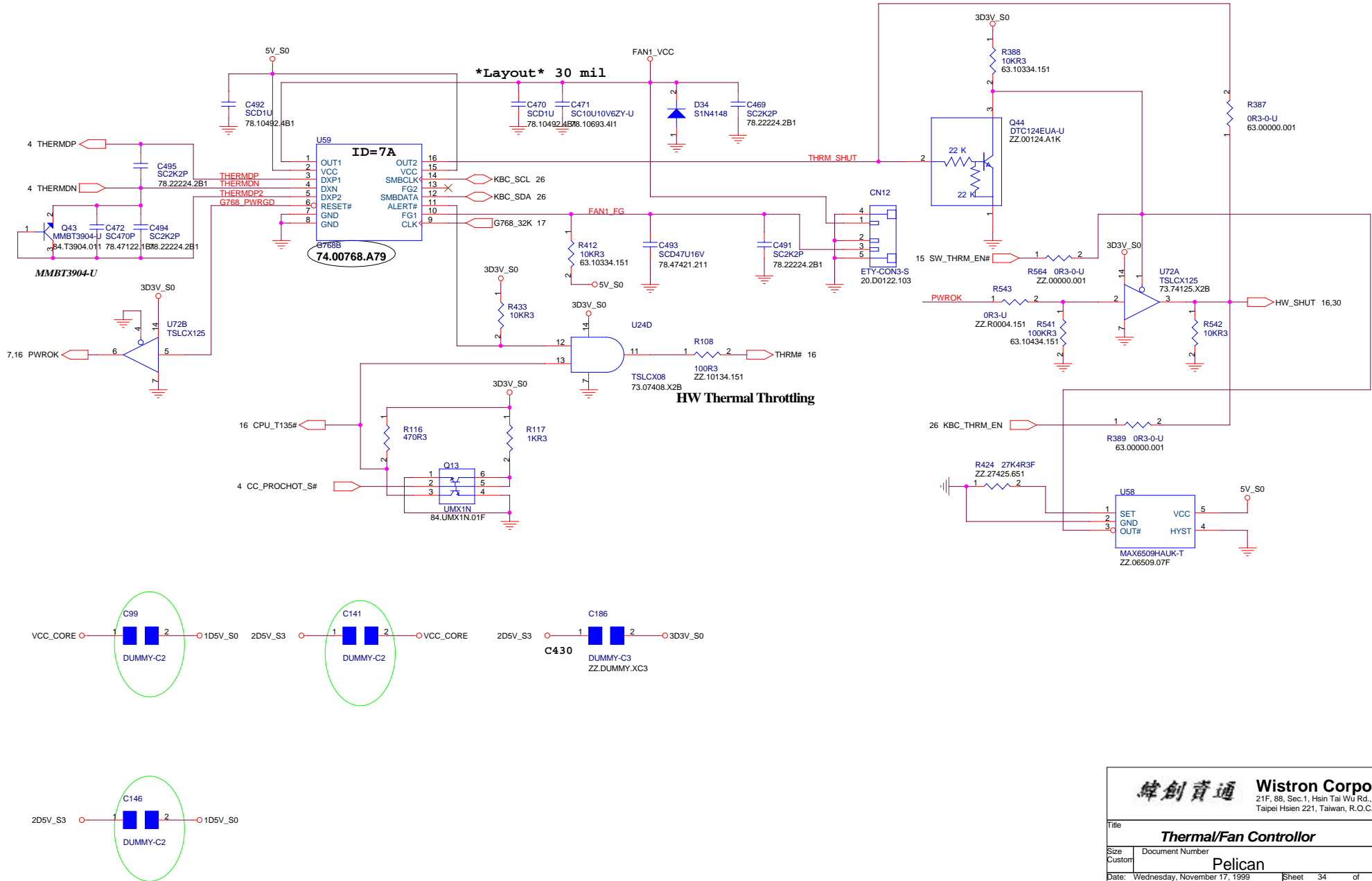
BT-SENSE

R299 360k
SB
SA-95K3R5F

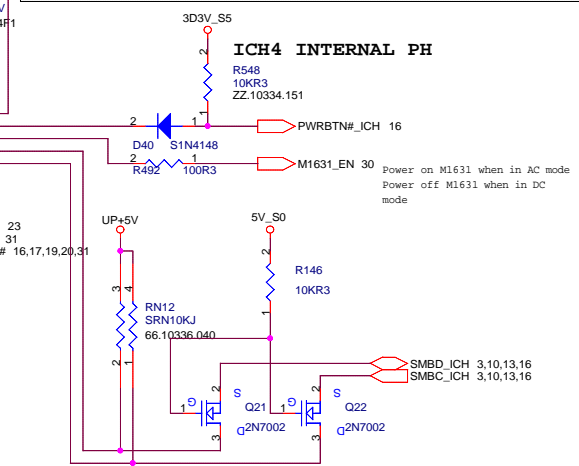
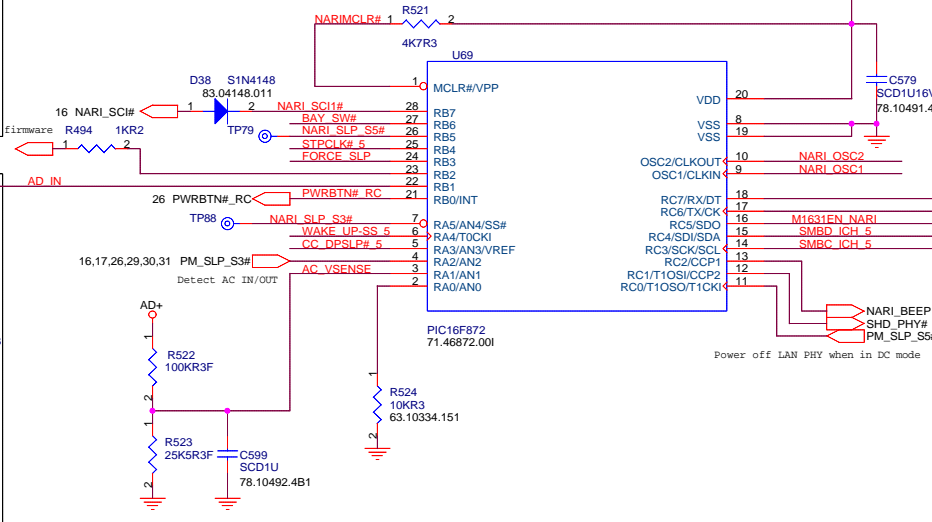
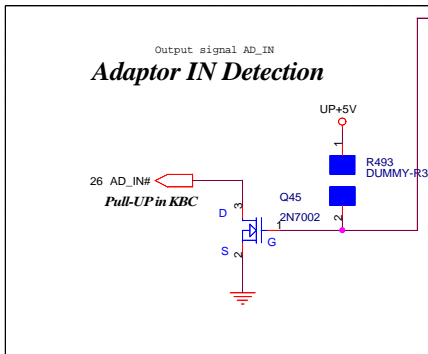
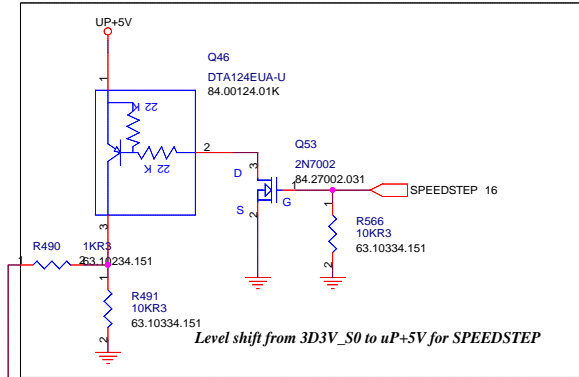
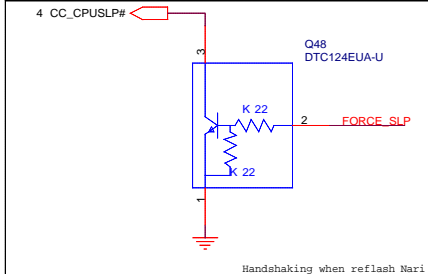
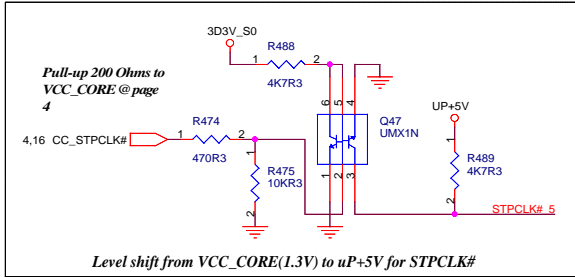
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Title CHARGER&MicroP		
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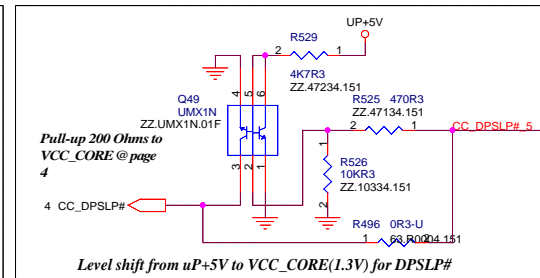
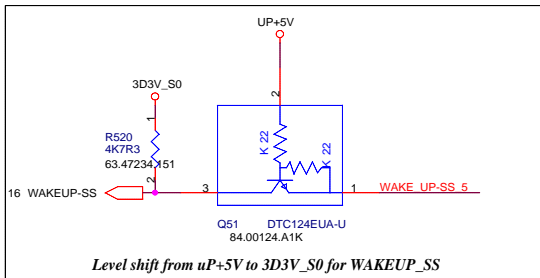
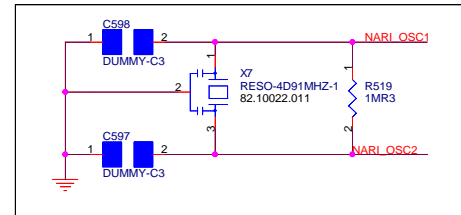
G768D thermal sensor & Fan controller



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Title	
Thermal/Fan Controller	
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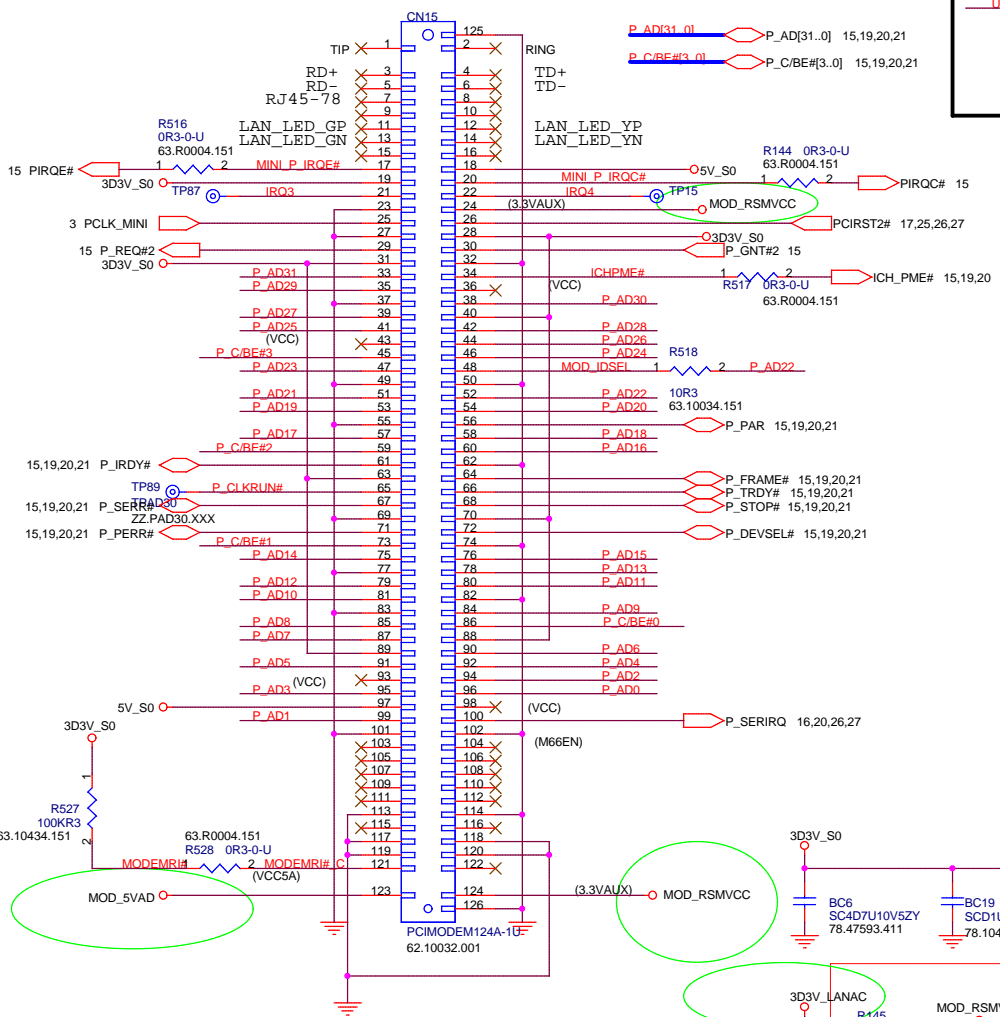
MicroChip Part Number
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PIC16F73 : 71.16F73.001



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Title Nari/SPEEDSTEP		
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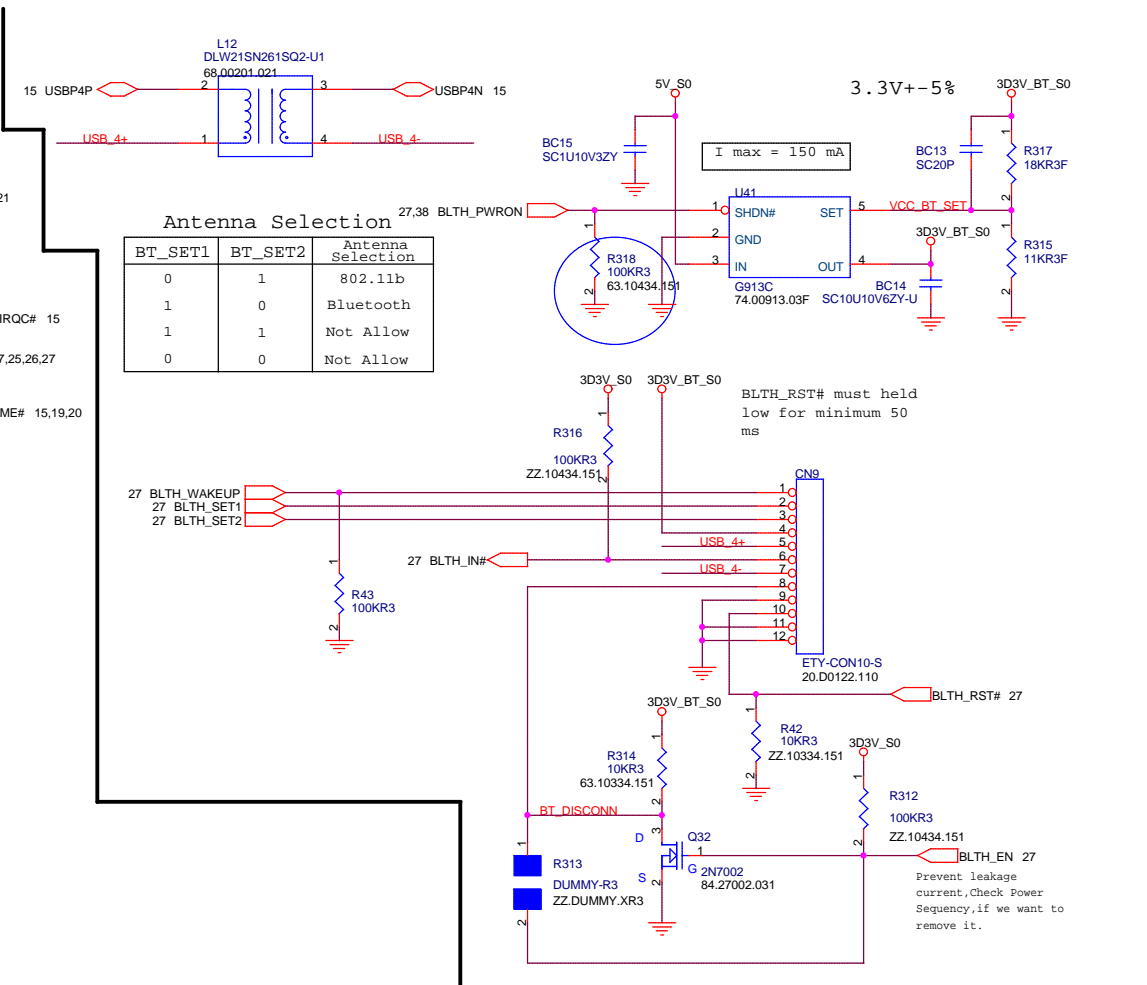
MINI PCI CONNECTOR

/WIRELESS

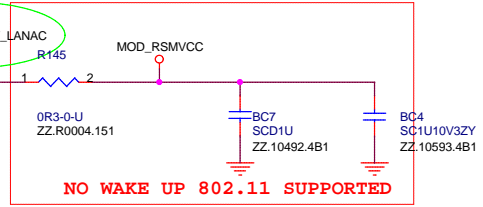


Antenna Selection

BT_SET1	BT_SET2	Antenna Selection
0	1	802.11b
1	0	Bluetooth
1	1	Not Allow
0	0	Not Allow



which power does 802.11 need?

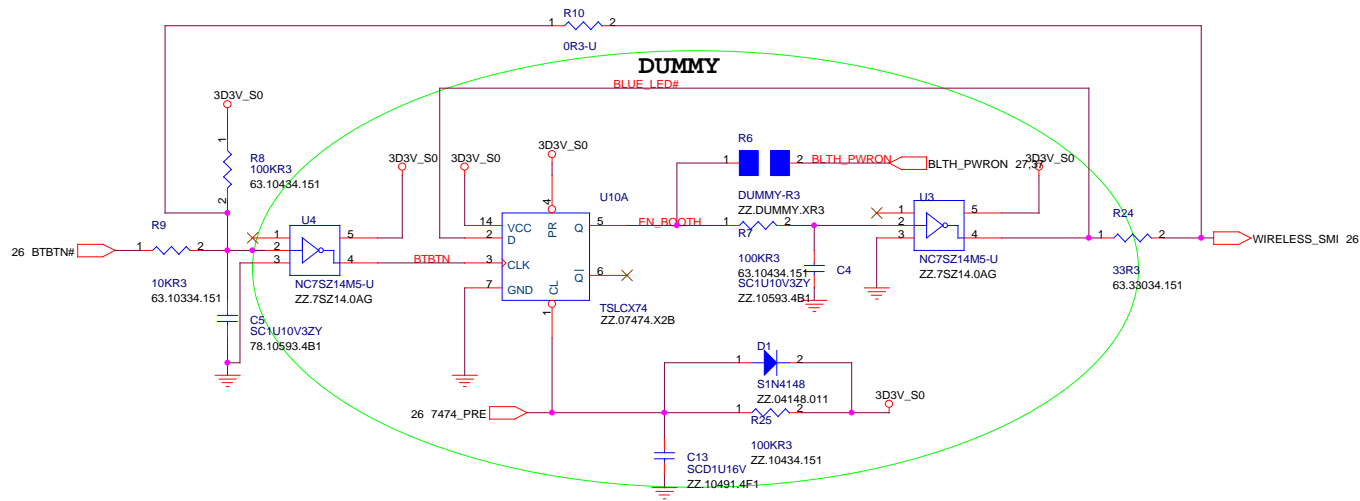


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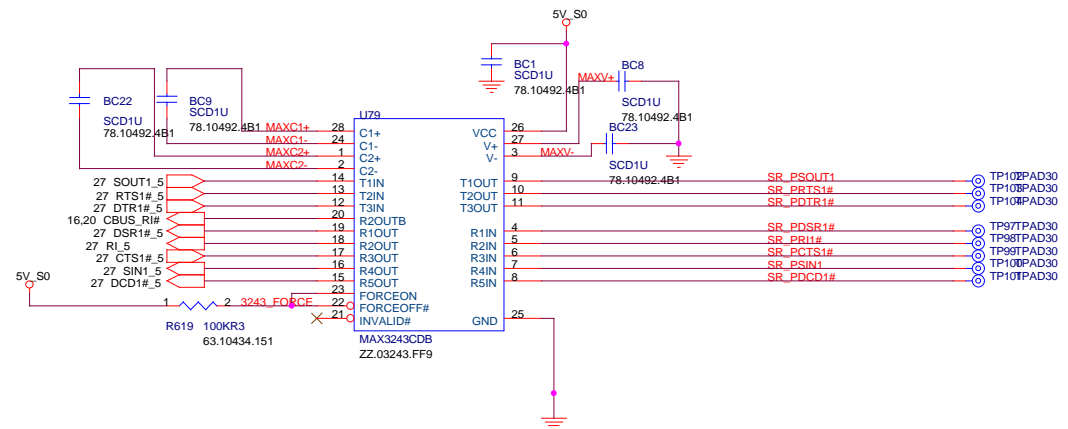
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SERIAL PORT

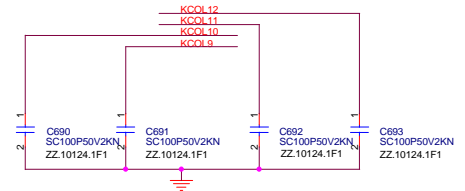
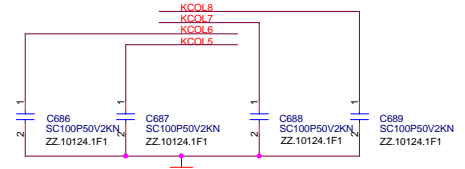
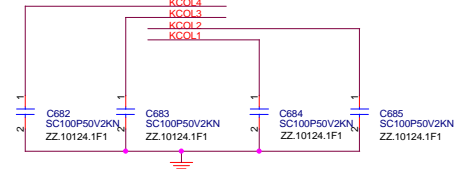
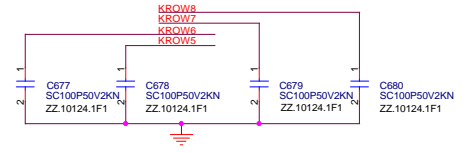
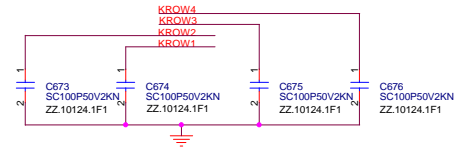
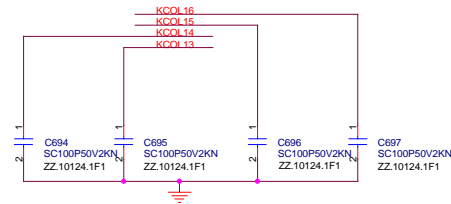
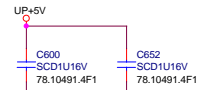
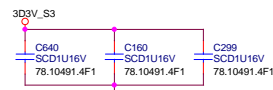
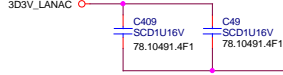
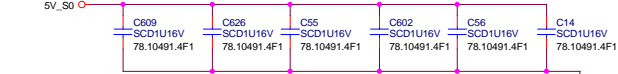
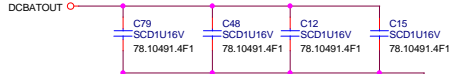
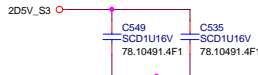
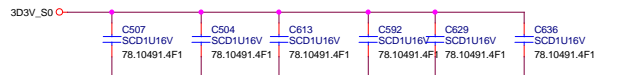
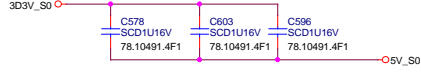
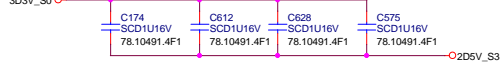
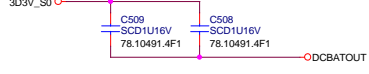
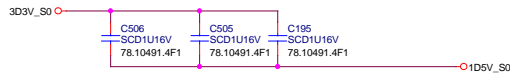
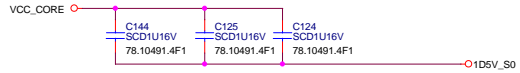
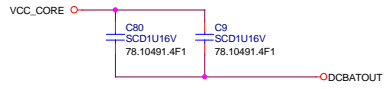


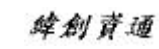
BYPASS CAP FOR EMI



 KROW[8..1] 26

 KCOL[16..1] 26




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