Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
PCB P/N : 48.4T301.01M
REVISION : -1M

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U 4, 5

G792 20

HOST BUS 667/800MHz@1.05V

DDR2 533/667 MHz 12,13
533/667MHz

DDR2 533/667 MHz 12,13
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.00U 6,7,8,9,10,11

TV Out 14
CRT 15
LCD 14
DVI 44
VGA Borad 28

X4 DMI 400MHz
C-Link0

PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

Line In
MIC In 14
31 INT.SPKR
Line Out (No-SPDIF)

Codec ALC268 30
AZALIA

OP AMP G1431Q 31
OP AMP G1412 31

RJ11
MODEM MDC Card 22

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U
16,17,18,19

PCI BUS

TI PCI7412
Cardbus Cardreader
25/26

PCMCIA I/F
PCMCIA SLOT Support TypeII 27
PWR SW CP2211F 26
1394 CONN 27
MS/MS Pro/xD/ MMC/SD 5 in 1 27

LAN GIGA BCM5787M 23
TXFM 24
RJ45 24

PCIex1
Mini Card Kedron a/b/g/n 29

LPC BUS

New card 29
PCI Express
P2231NFC1 29

SATA
HDD 21

PATA
CDROM 21

USB
MINI USB BlueTooth 22
Finger print 34
USB 4 Port 22
CAMERA 13

KBC Winbond WPC8768L 32
SPI I/F
BIOS W25X80-VSS 34
LPC DEBUG CONN. 35
Touch Pad 33
INT. KB 33
FIR 32

SYSTEM DC/DC
MAX8744 38

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC
Max8717 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

TPS51100 41

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5915 41

1D8V_S3	1D25V_S0 (2A)

APL531230

3D3V_S0	2D5V_S0 (300mA)

APW5912 40

3D3V_S5	1D5V_S3 (7.5A)

ISL CHARGER
ISL6255 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
MAX8770 35,36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M
Date: Thursday, June 07, 2007 | Sheet 1 of 45

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE X1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

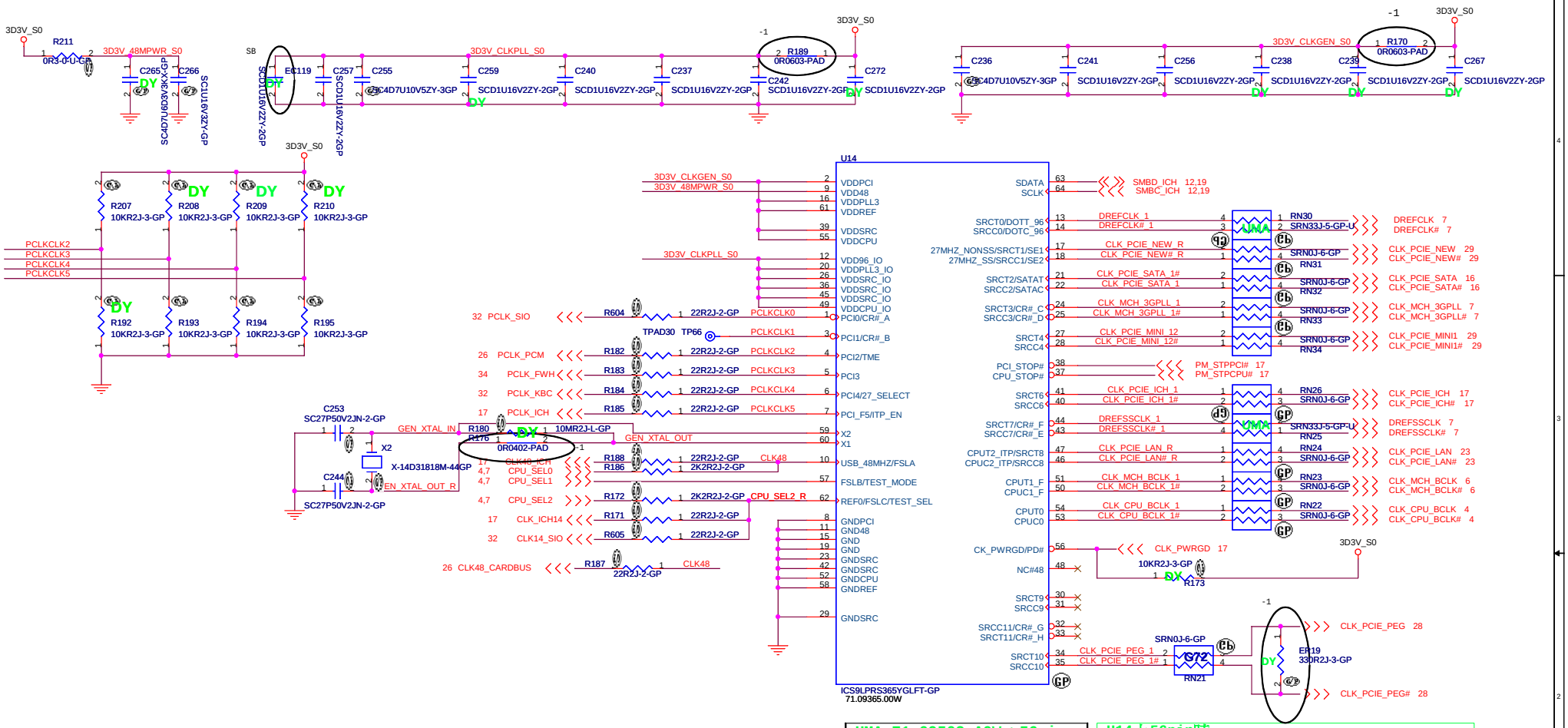
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 2 of 45



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

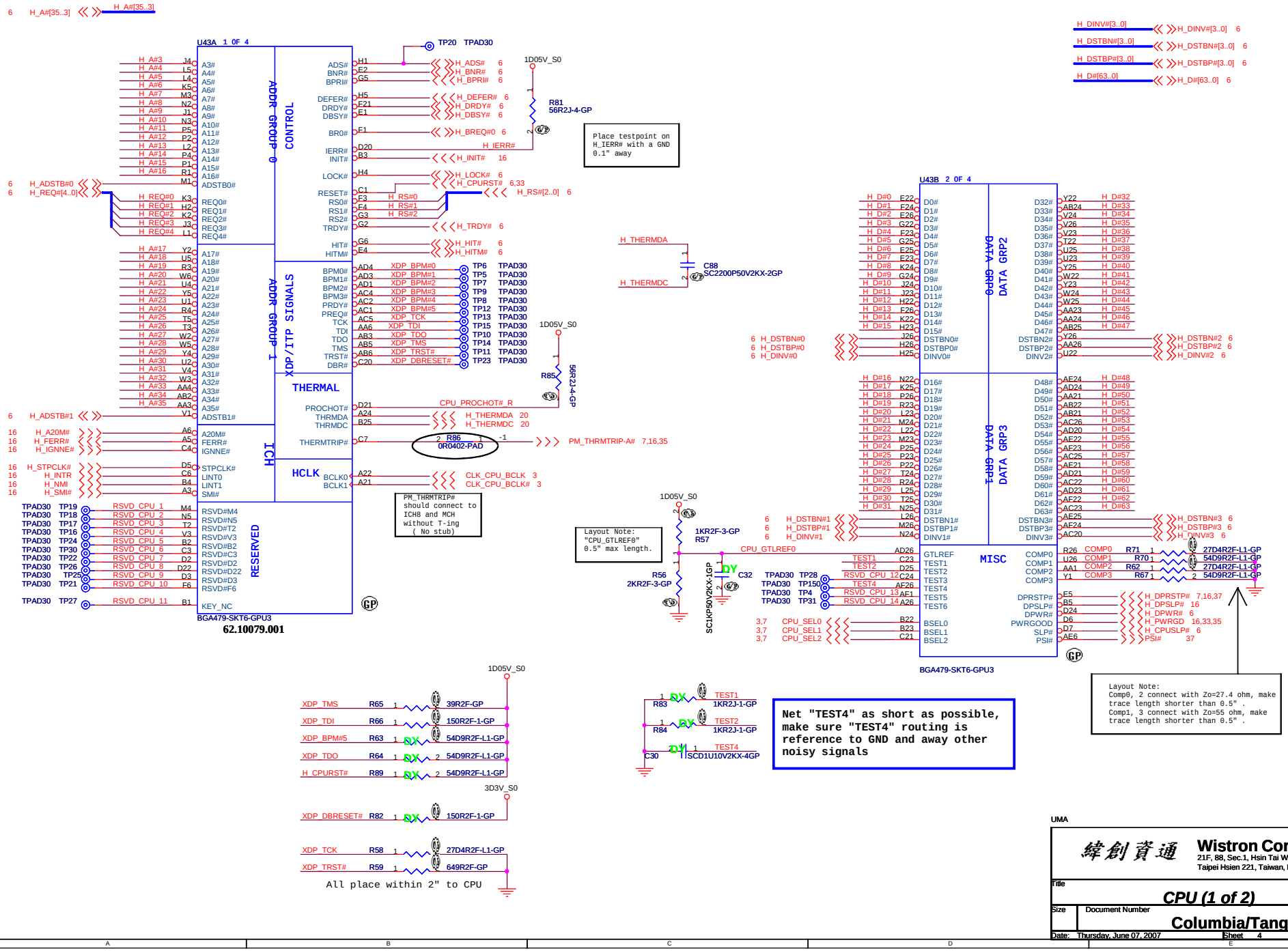
UMA

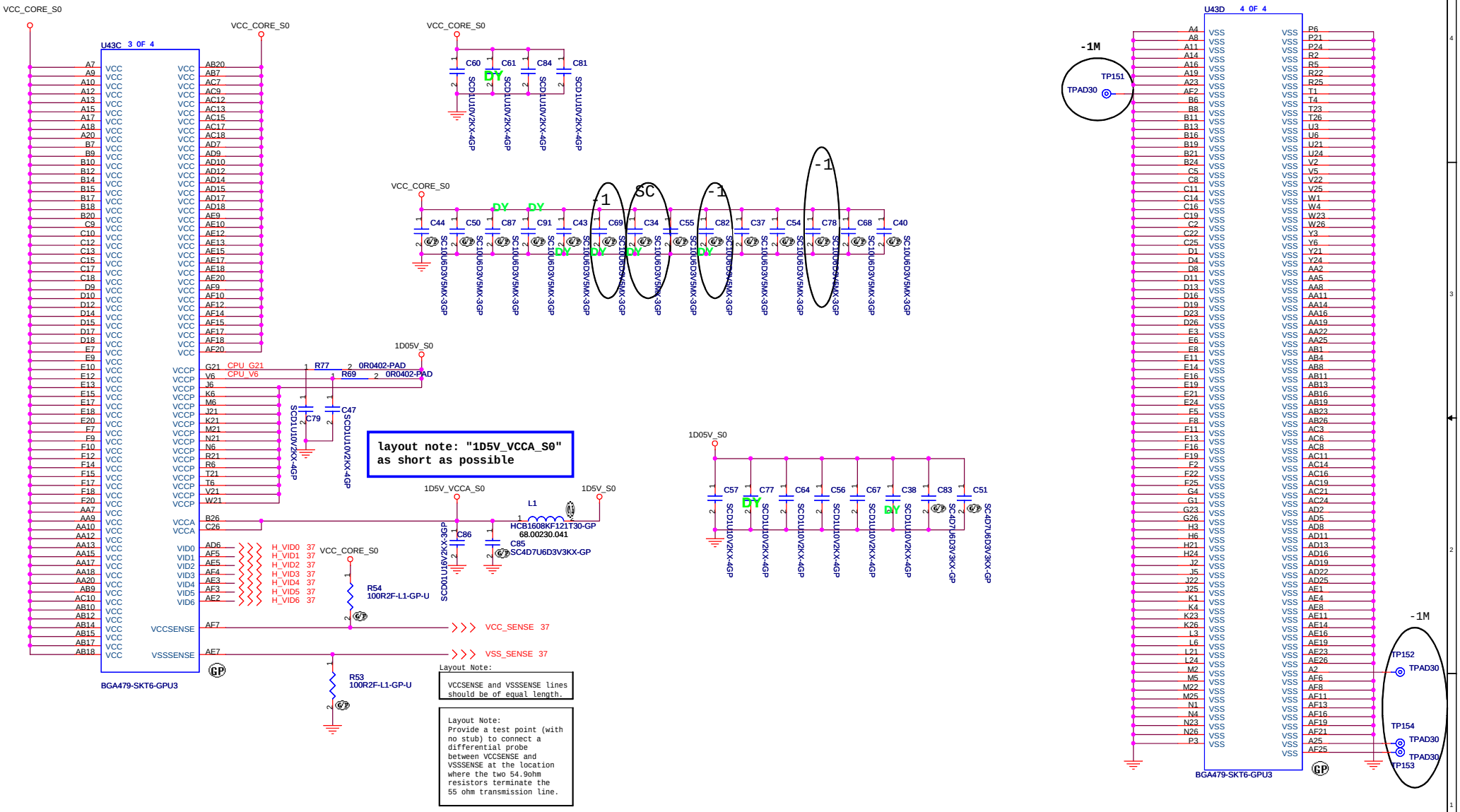
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size | Document Number: Columbia/Tangiz | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 3 of 45

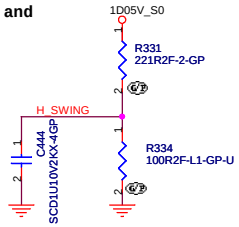

U43A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU3
62.10079.001
U43B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU3
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH8 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Net "TEST4" as short as possible, make sure "TEST2" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (1 of 2)
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Thursday, June 07, 2007
Sheet 4 of 45



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (2 of 2)		
Size	Document Number: Columbia/Tangiz	Rev: -1M
Date: Thursday, June 07, 2007	Sheet 5 of 45	

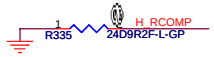
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



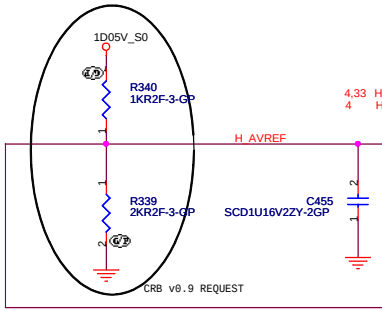
H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

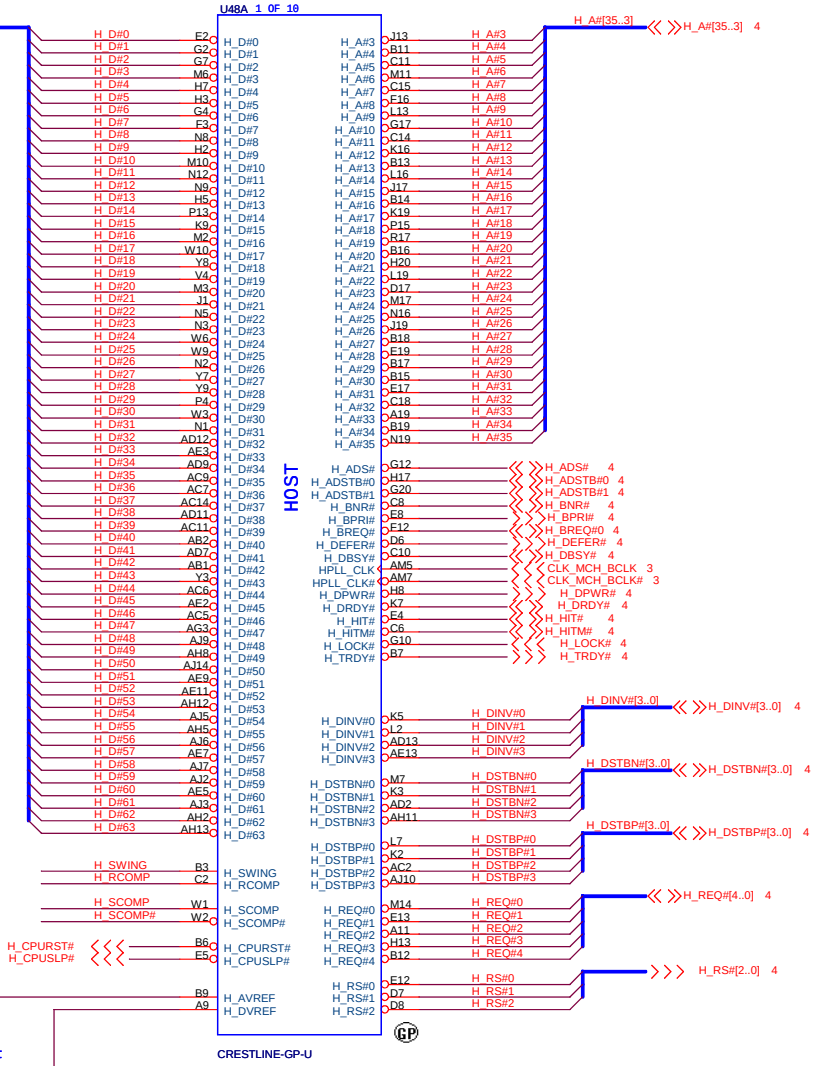
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





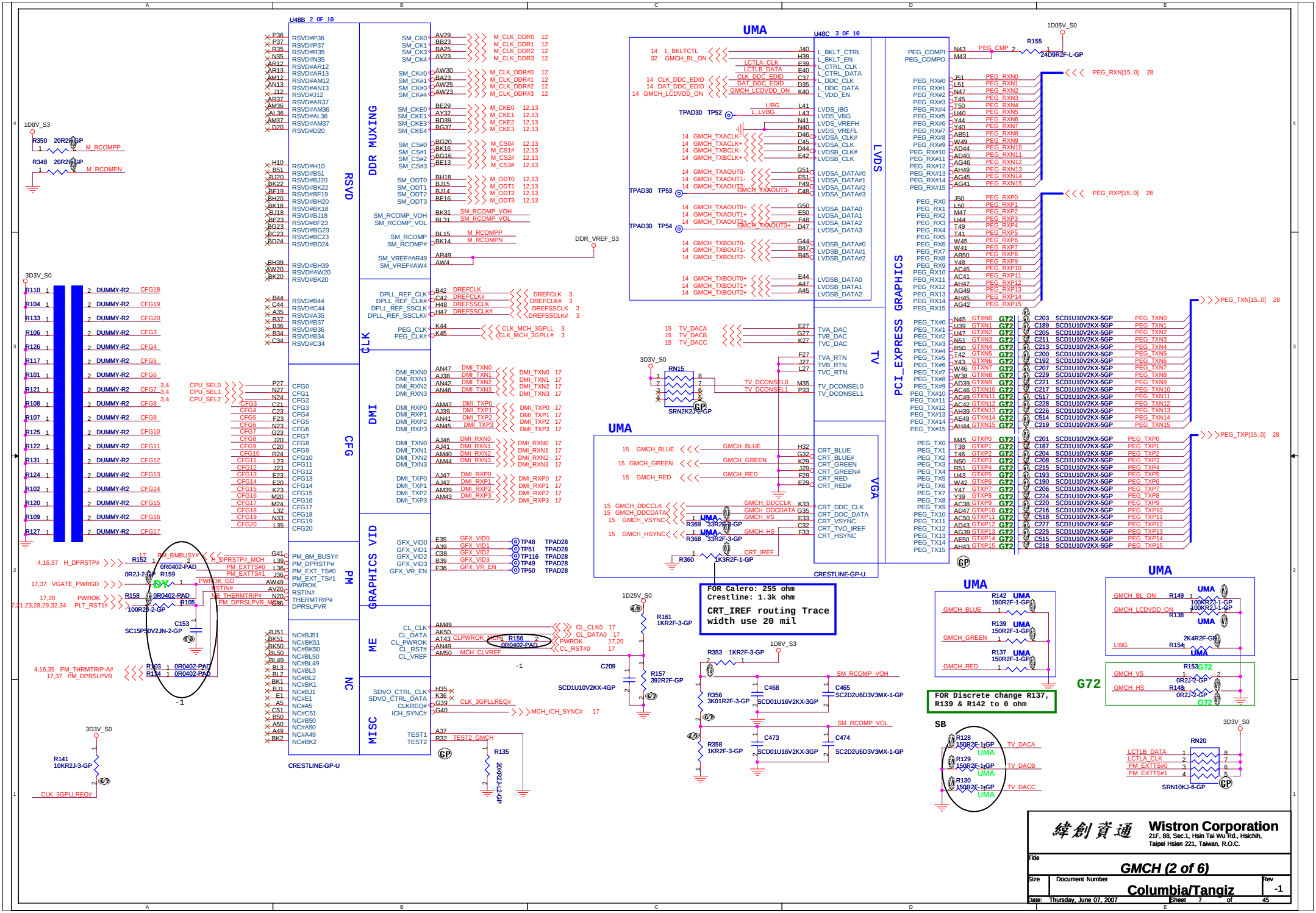
UMA

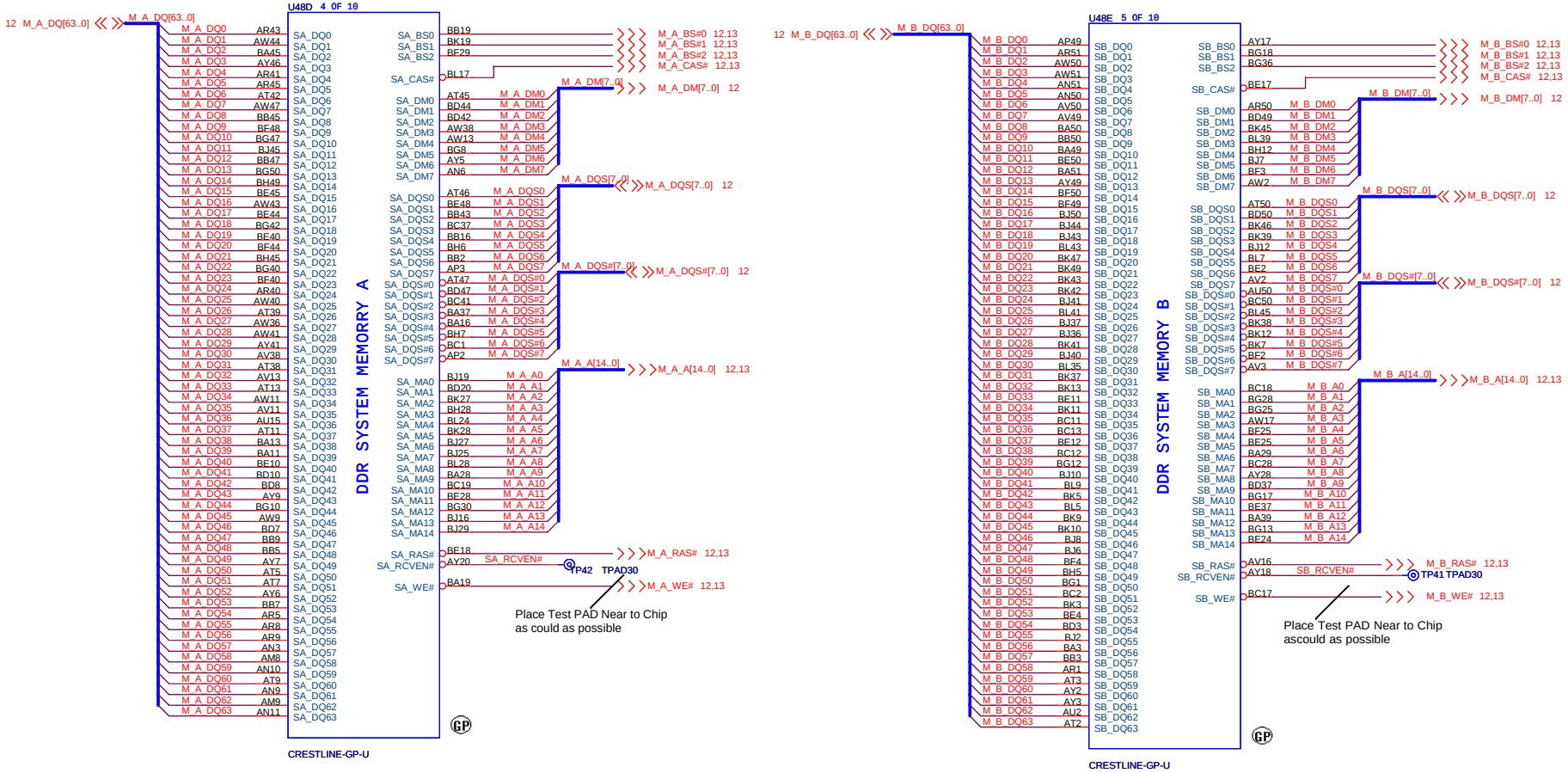
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (1 of 6)***

Size | Document Number: **Columbia/Tangiz** | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 6 of 45


U48B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
PM
GRAPHICS VID
ME
NC
MISC
CRESTLINE-GP-U
UMA
U48C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Discrete change R137, R139 & R142 to 0 ohm
SB
G72
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 6)
Size
Document Number
Columbia/Tangiz
Rev
-1
Date: Thursday, June 07, 2007
Sheet 7 of 45



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GMCH (3 of 6)***	
Size	Document Number **Columbia/Tangiz**	Rev -1
Date: Thursday, June 07, 2007	Sheet 8 of 45	

VCC_NCTF + VCC=1573mA

1573mA

POWER

VCC_AXG_NCTF + VCC_AXG=7700mA

SB:Remove R123,R132,R136,R144

SB:DIS remove 0 ohm on C129,C210,C158,C161

FOR VCC CORE AND VCC NCTF

FOR VCC CORE

Coupling CAP 370 mils from the Edge

FOR VCC AXM NCTF AND VCC AXM

VCC_AXM_NCTF + VCC_AXM=540mA

FOR VCC SM

Place CAP where LVDS and DDR2 taps

Place on the Edge

3138mA

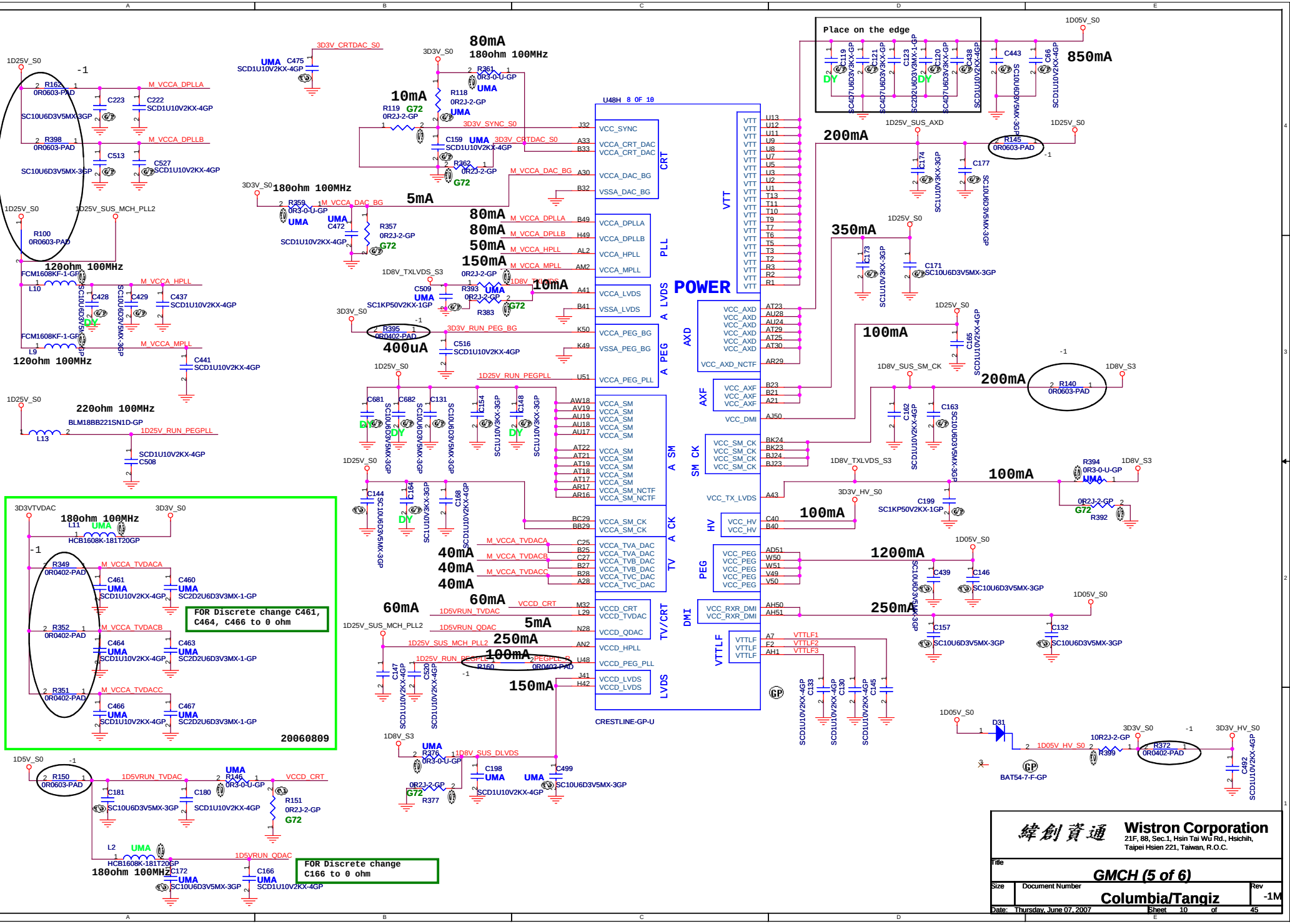
CRESTLINE-GP-U

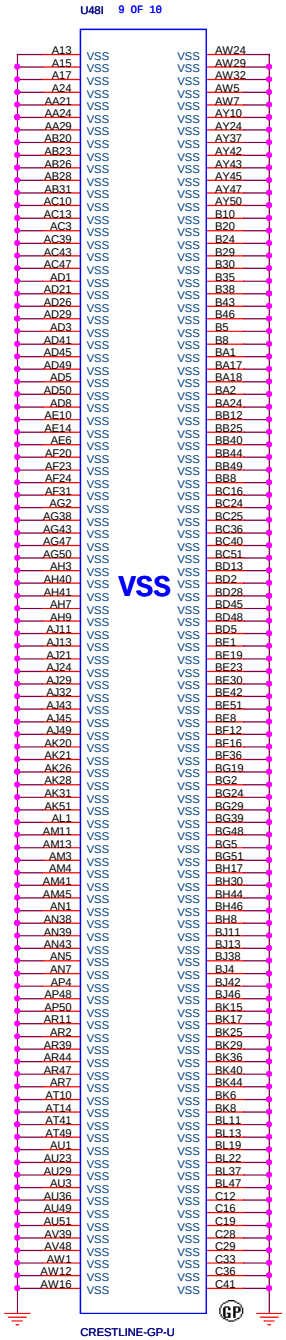
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

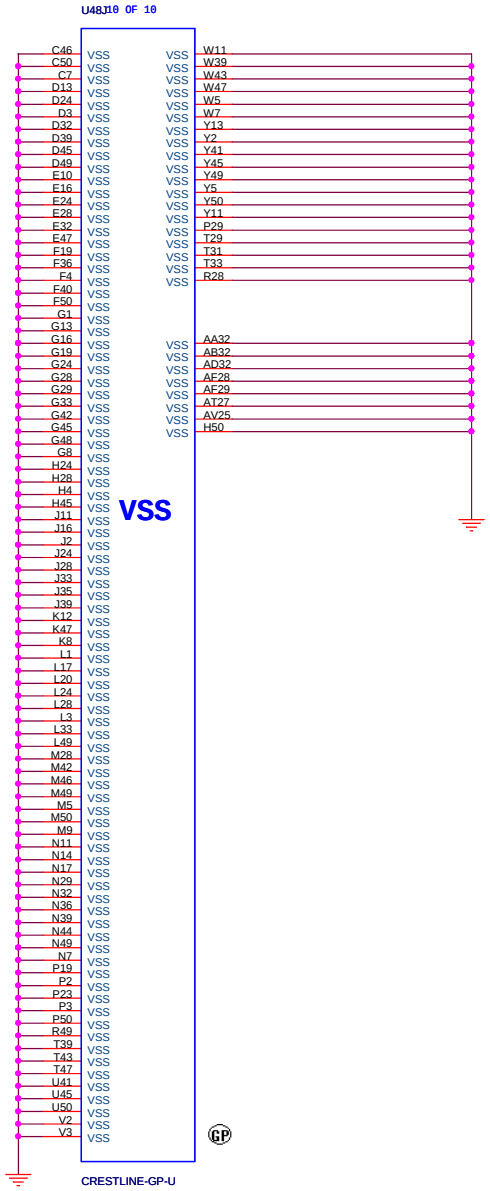
Title: GMCH (4 of 6)

Size: Columbia/Tangiz | Rev: -1M

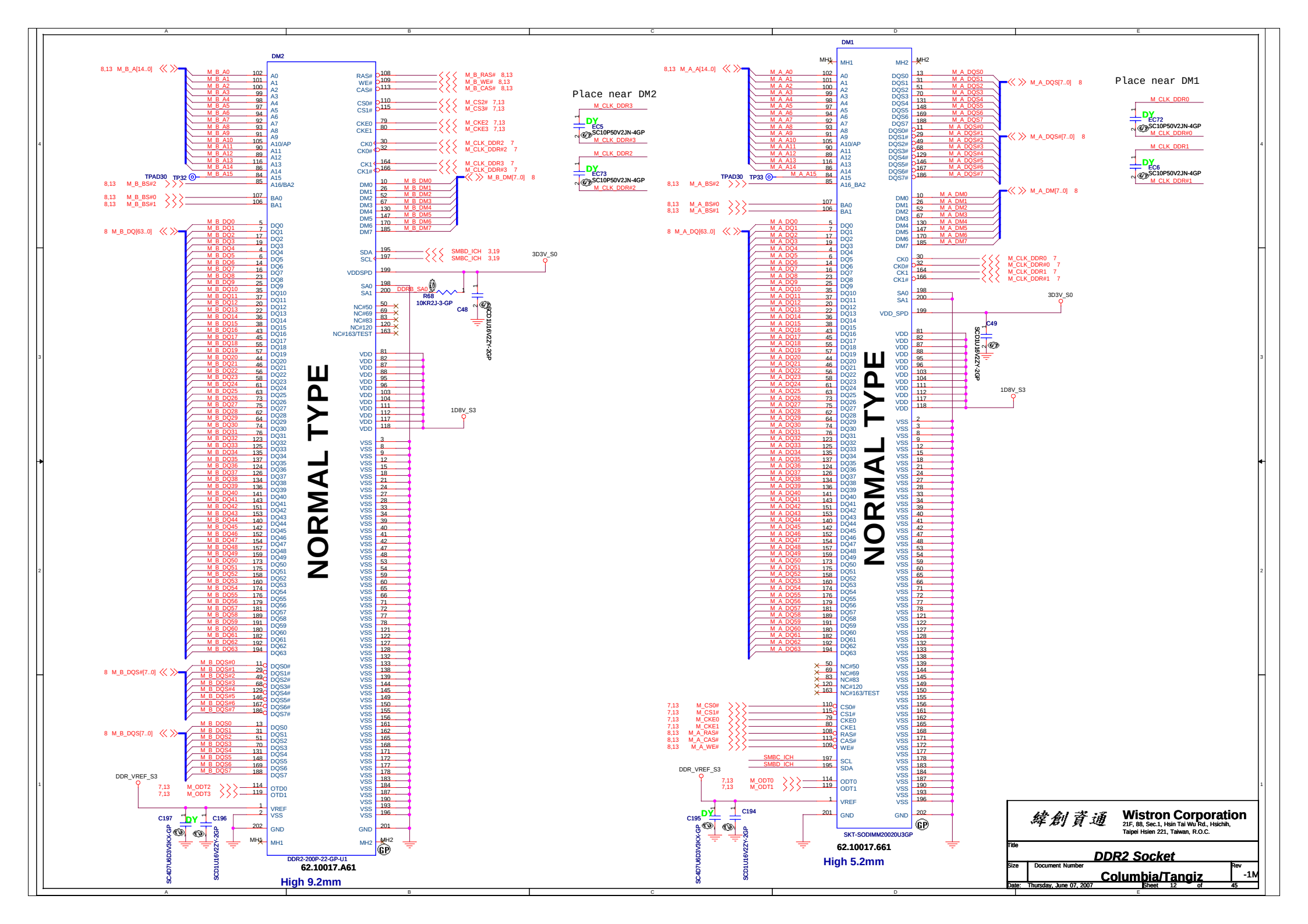
Date: Thursday, June 07, 2007 | Sheet 9 of 45


POWER
U48H 8 OF 10
CRESTLINE-GP-U
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
TV/CRT
LVDS
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
VCC_SYNC
VCCA_CRT_DAC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_CK
VCCA_SM_CK_NCTF
VCCA_TVA_DAC
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
VCCA_TVC_DAC
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VCCD_LVDS
VCC_AXD
VCC_AXD_NCTF
VCC_AXF
VCC_DMI
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_RXR_DMI
VTTLF
Place on the edge
80mA
180ohm 100MHz
10mA
5mA
80mA
80mA
50mA
150mA
10mA
400uA
40mA
40mA
40mA
60mA
5mA
250mA
100mA
150mA
200mA
350mA
100mA
200mA
100mA
100mA
1200mA
250mA
850mA
120ohm 100MHz
220ohm 100MHz
180ohm 100MHz
180ohm 100MHz
FOR Discrete change C461, C464, C466 to 0 ohm
20060809
FOR Discrete change C166 to 0 ohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GMCH (5 of 6)
Columbia/Tangiz
-1M
Thursday, June 07, 2007
10 of 45



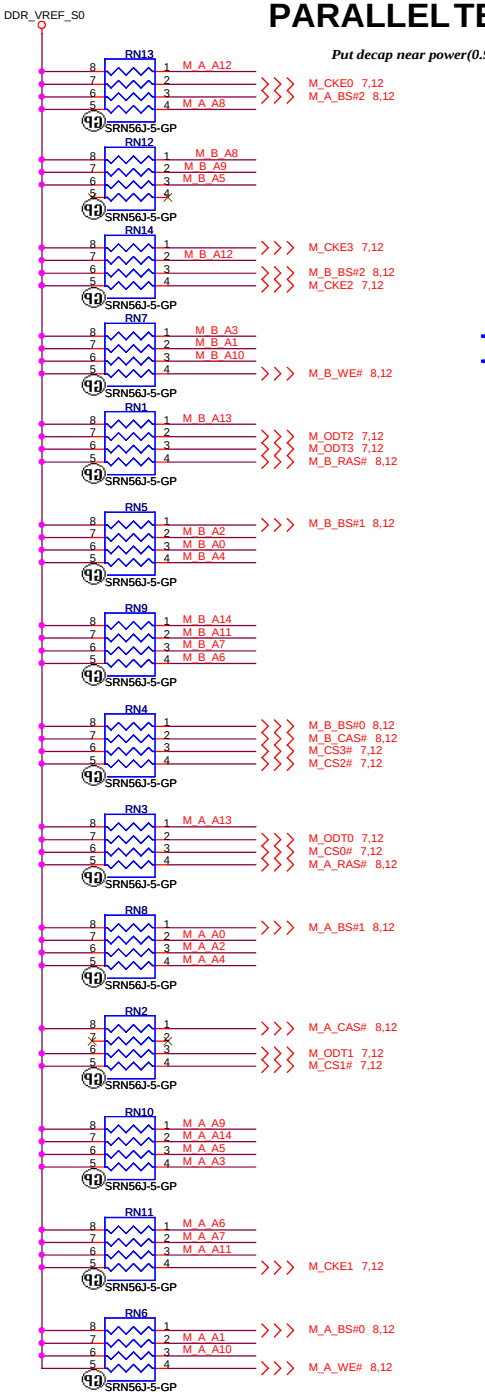


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GMCH (6 of 6)***	
Size	Document Number **Columbia/Tangiz**	Rev -1M
Date: Thursday, June 07, 2007	Sheet 11 of 45	


DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
Place near DM2
M_CLK_DDR3
M_CLK_DDR2
EC5
EC73
SC10P50V2JN-4GP
TP32
TPAD30
R68
10KR2J-3-GP
C48
C197
C196
C195
C194
DDR_VREF_S3
3D3V_S0
1D8V_S3
SMBD_ICH 3,19
SMBC_ICH 3,19
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
Place near DM1
M_CLK_DDR0
M_CLK_DDR1
EC72
EC6
C49
TP33
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Thursday, June 07, 2007
Sheet 12 of 45

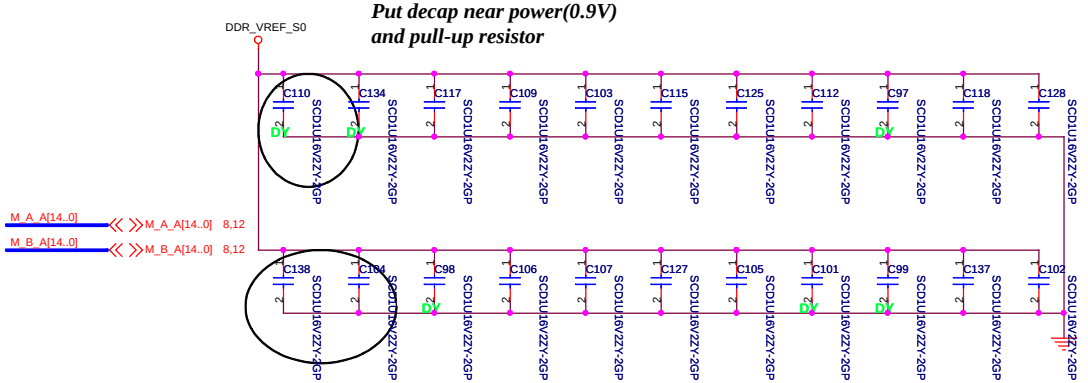
PARALLEL TERMINATION

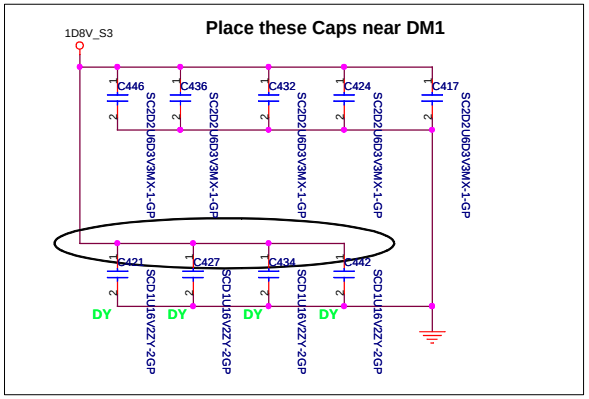
Put decap near power(0.9V) and pull-up resistor

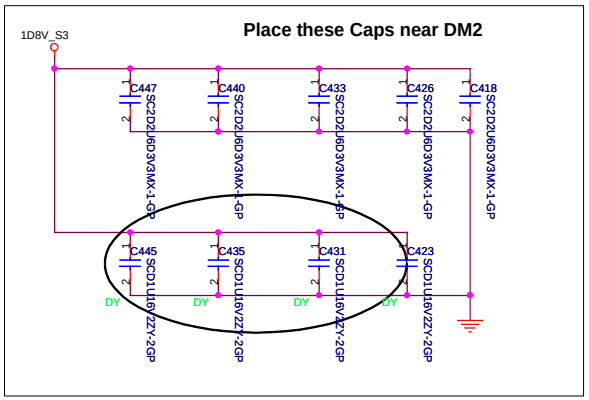


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor







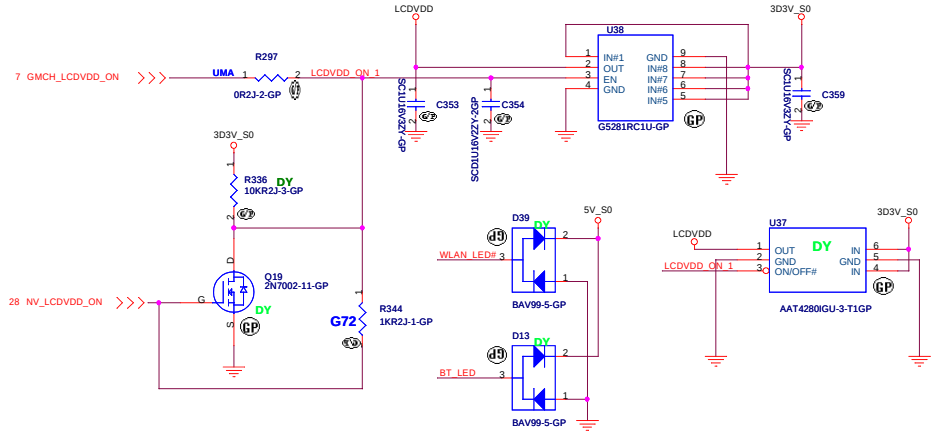
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

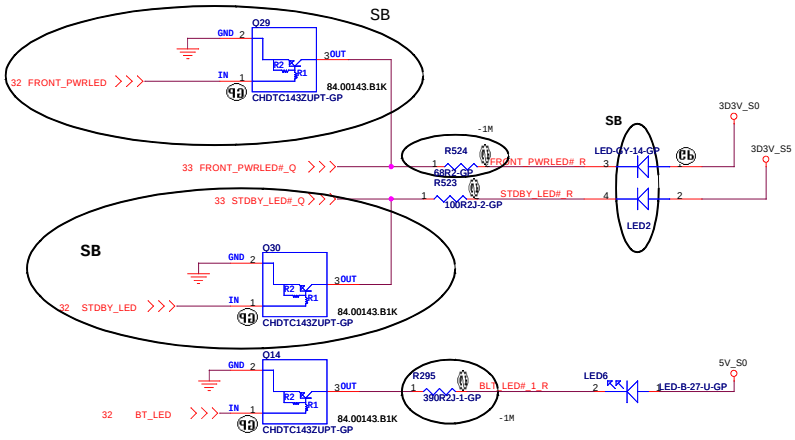
Title: ***DDR2 Termination Resistor***

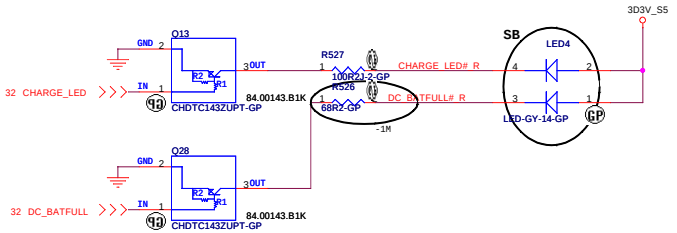
Size | Document Number: **Columbia/Tangiz** | Rev: -1M

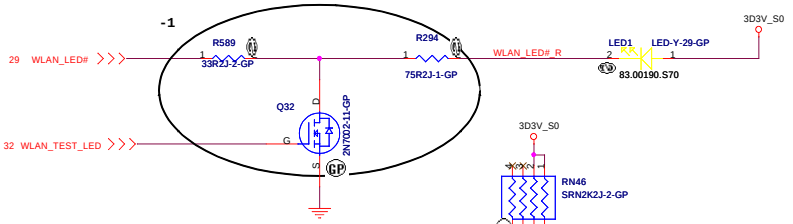
Date: Thursday, June 07, 2007 | Sheet 13 of 45

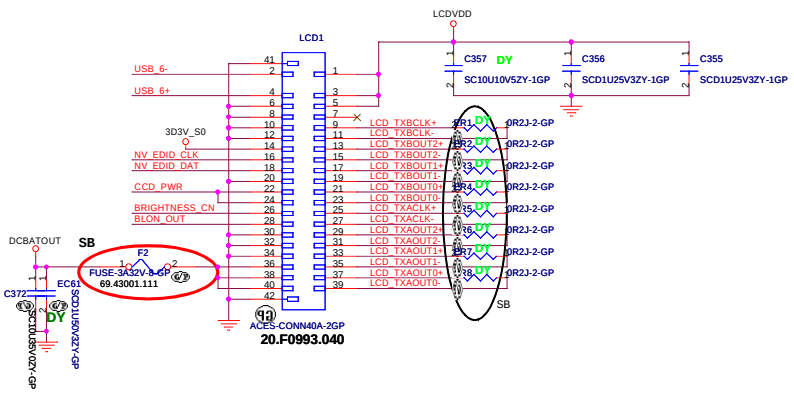
LCD/INVERTER CONN

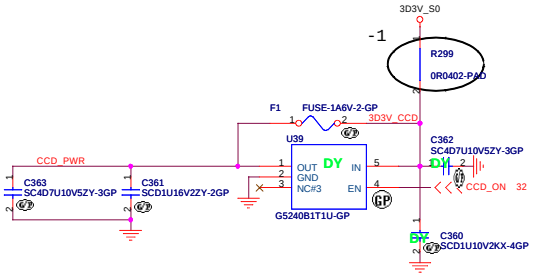


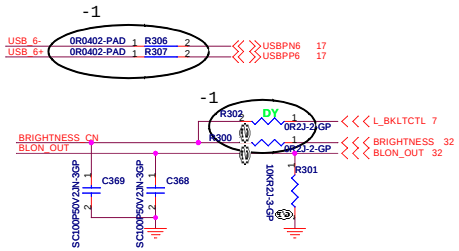


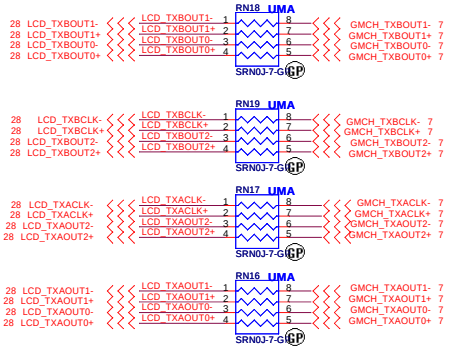


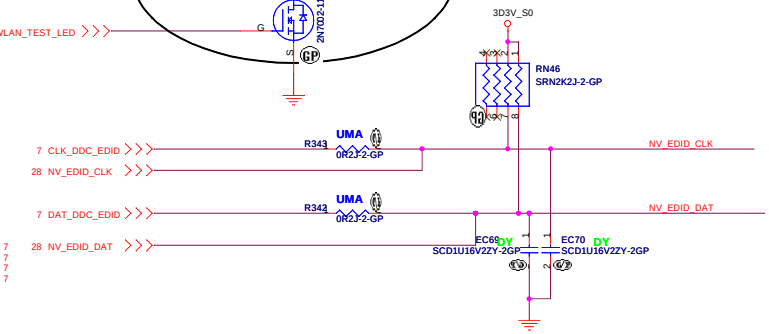












<variant_name>

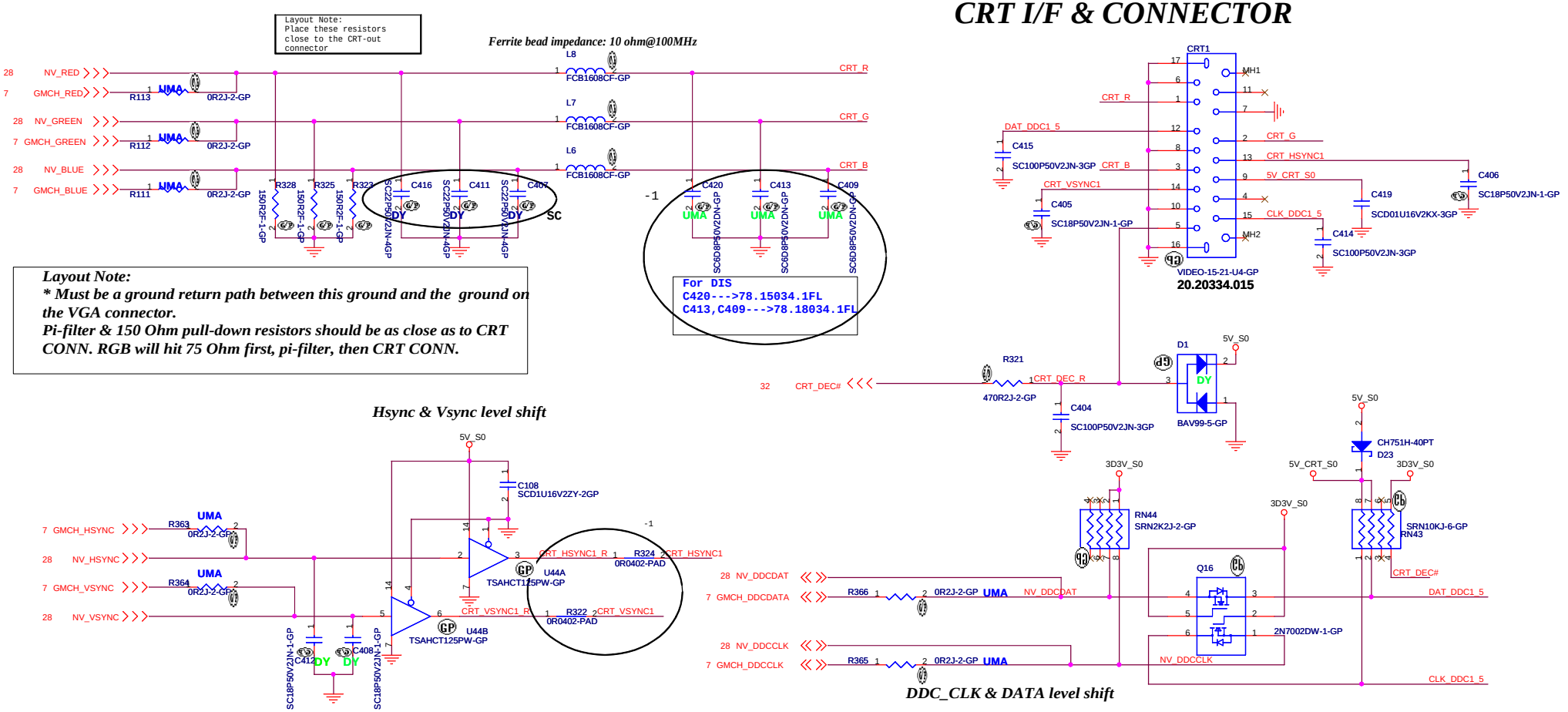
緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

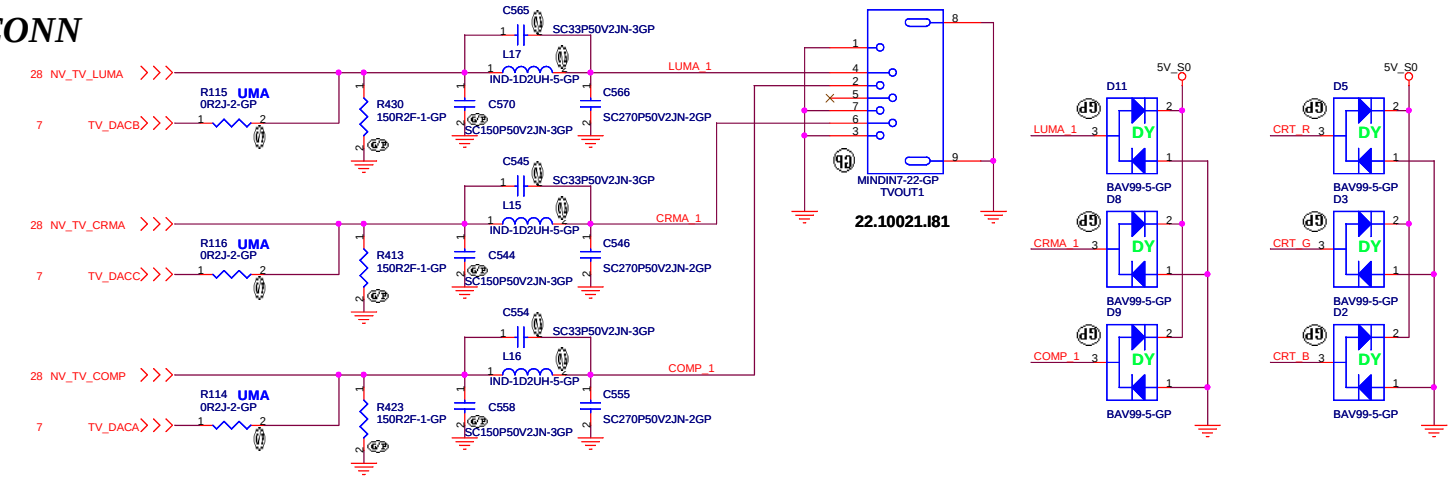
Size: | Document Number: Columbia/Tangiz | Rev: -1

Date: Thursday, June 07, 2007 | Sheet 14 of 45

CRT I/F & CONNECTOR



TV CONN

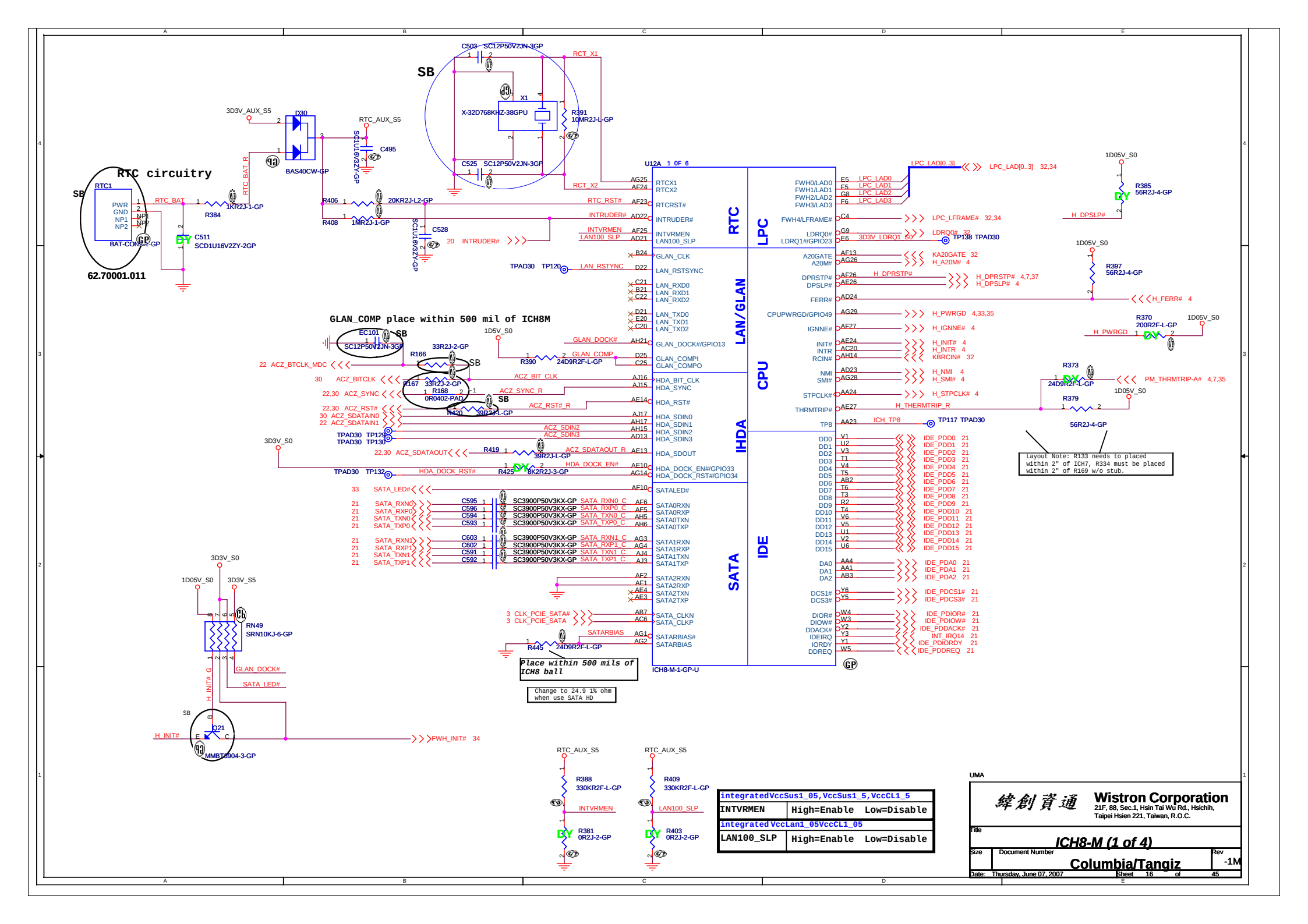


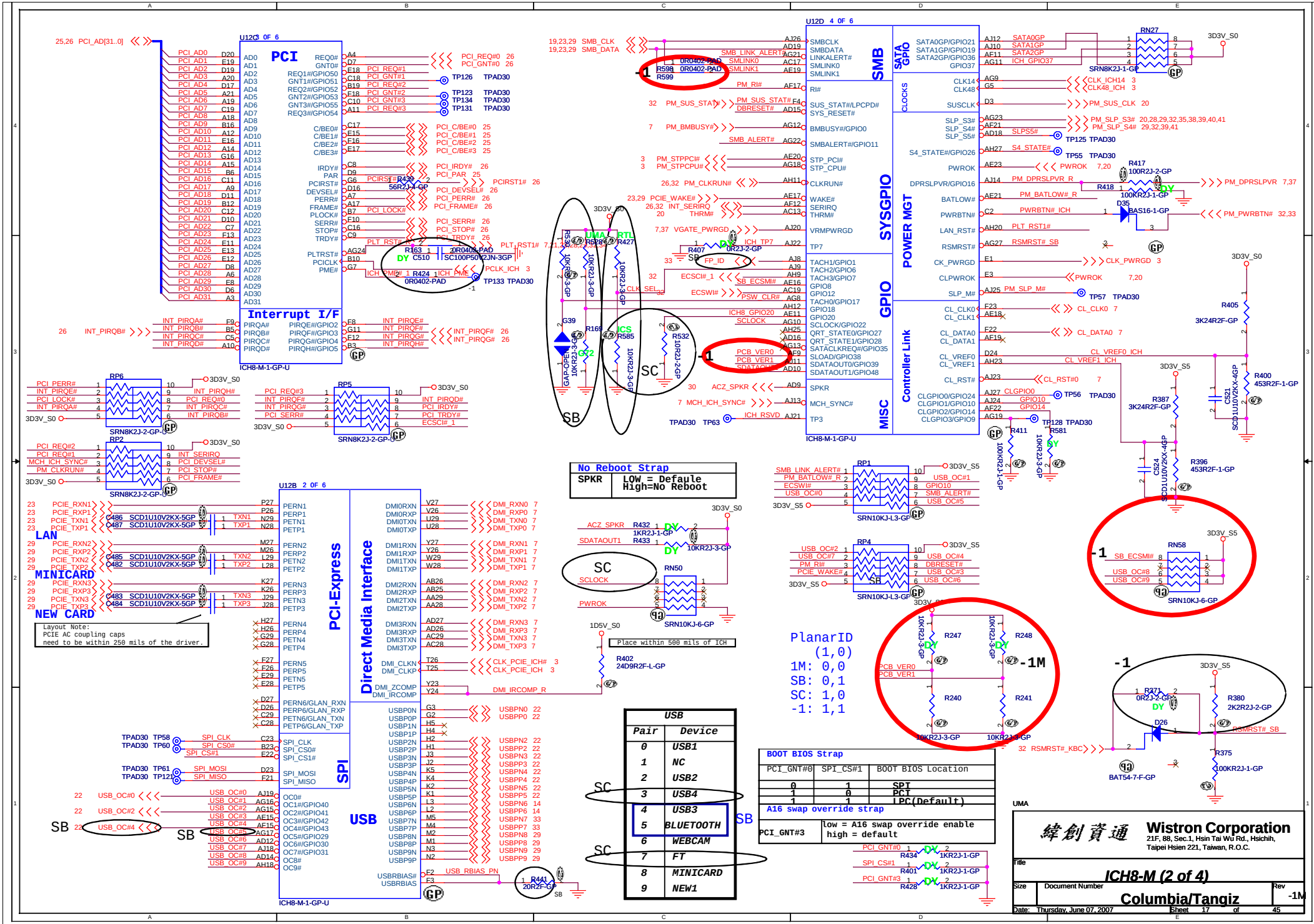
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

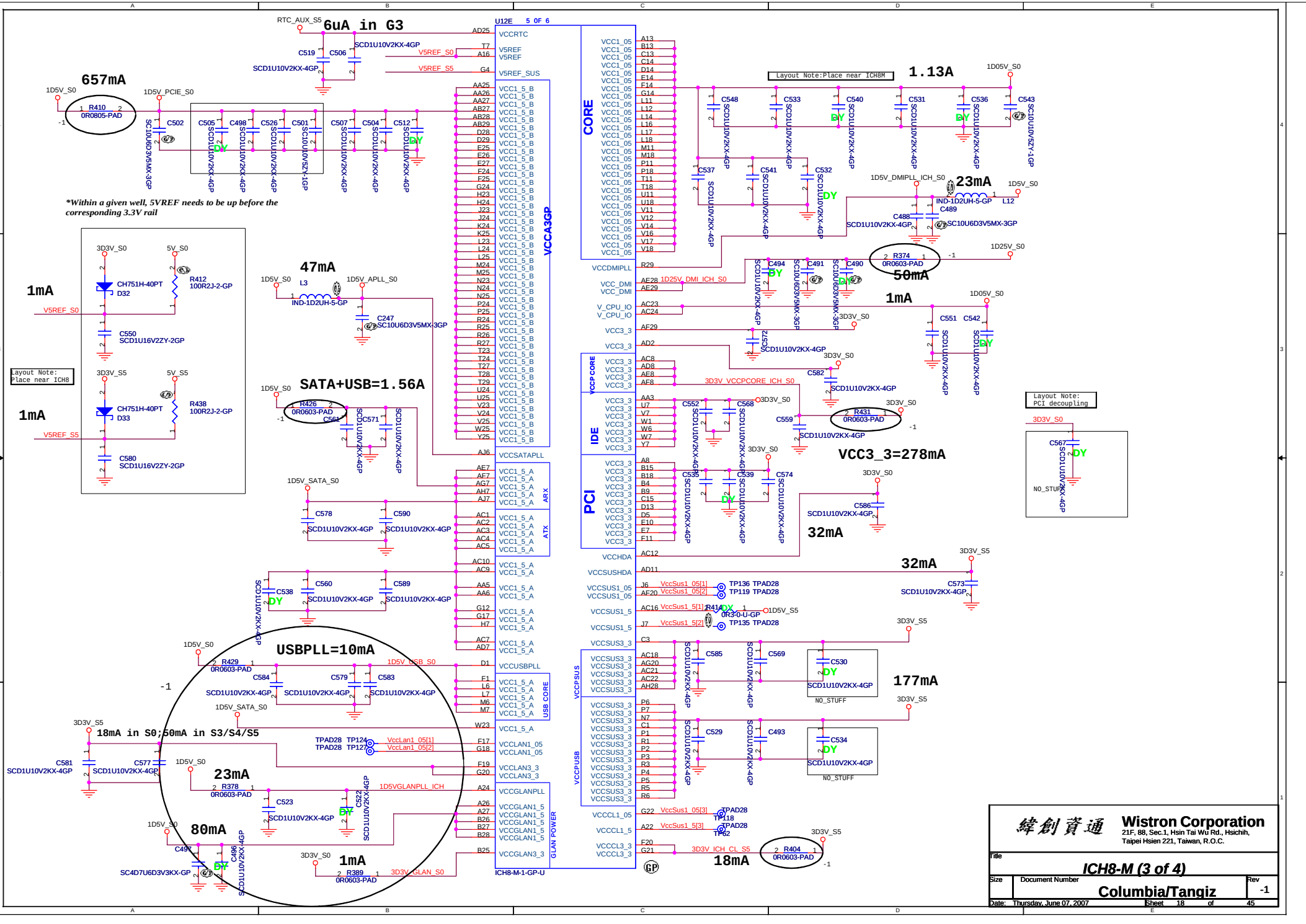
Title: CRT/TV Connector

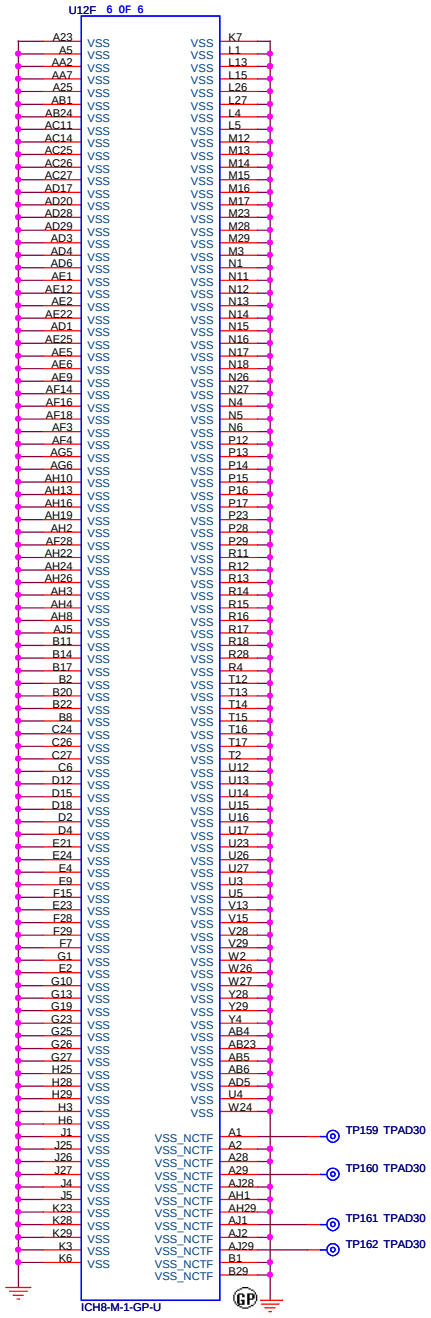
Size	Document Number	Rev
	Columbia/Tangiz	-1

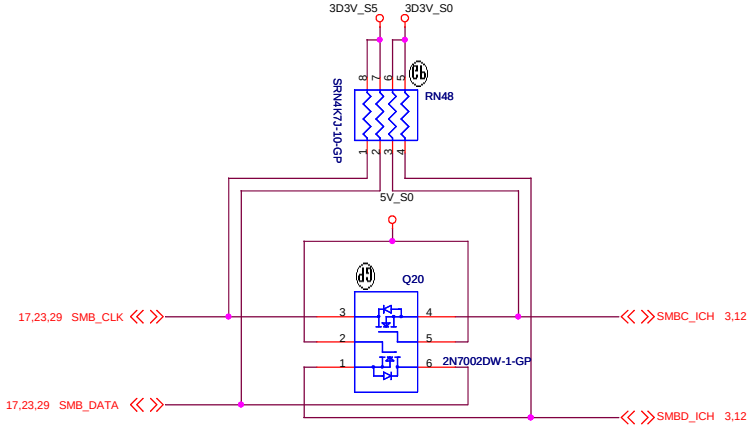
Date: Thursday, June 07, 2007 Sheet 15 of 45


RTC circuitry
62.70001.011
GLAN_COMP place within 500 mil of ICH8M
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
U12A 1 OF 6
ICH8-M-1-GP-U
RTC
LPC
LAN/GLAN
CPU
IHDA
IDE
SATA
integratedVccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integratedVccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (1 of 4)
Columbia/Tangiz
-1M
Thursday, June 07, 2007
Sheet 16 of 45


PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
SYSGPIO
GPIO
MISC
SATA GPIO
CLOCKS
POWER MGT
Controller Link
LAN
MINICARD
NEW CARD
PCI-Express
Direct Media Interface
SPI
USB
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
PlanarID
(1,0)
1M: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
USB
Pair
Device
0 USB1
1 NC
2 USB2
3 USB4
4 USB3
5 BLUETOOTH
6 WEBCAM
7 FT
8 MINICARD
9 NEW1
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (2 of 4)
Columbia/Tangiz
-1M
Thursday, June 07, 2007
17 of 45


6uA in G3
657mA
1D5V_S0
1D5V_PCIE_S0
R410
0R0805-PAD
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1mA
3D3V_S0
5V_S0
CH751H-40PT
D32
R412
100R2J-2-GP
V5REF_S0
C550
SCD1U16V2ZY-2GP
Layout Note: Place near ICH8
3D3V_S5
5V_S5
D33
R438
V5REF_S5
C580
47mA
L3
IND-1D2UH-5-GP
C247
SC10U6D3V5MX-3GP
SATA+USB=1.56A
R426
0R0603-PAD
1D5V_SATA_S0
USBPLL=10mA
R429
1D5V_USB_S0
18mA in S0;50mA in S3/S4/S5
23mA
R378
1D5VGLANPLL_ICH
80mA
SC4D7U6D3V3KX-GP
1mA
R389
3D3V_GLAN_S0
RTC_AUX_S5
V5REF_S0
V5REF_S5
U12E 5 OF 6
VCCRTC
V5REF
V5REF_SUS
VCCA3GP
VCCSATAPLL
ICH8-M-1-GP-U
CORE
VCCDMIPLL
VCC_DMI
V_CPU_IO
VCCP CORE
IDE
PCI
VCCHDA
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCP SUS
VCCPUSB
VCCCL1_05
VCCCL1_5
VCCCL3_3
USB CORE
GLAN POWER
1D25V_DMI_ICH_S0
3D3V_VCCPCORE_ICH_S0
VCC3_3=278mA
1.13A
Layout Note:Place near ICH8M
1D5V_DMIPLL_ICH_S0
23mA
IND-1D2UH-5-GP
L12
50mA
R374
0R0603-PAD
1D25V_S0
R431
0R0603-PAD
32mA
R414
0R3-0-U-GP
TP136 TPAD28
TP119 TPAD28
TP135 TPAD28
177mA
NO_STUFF
18mA
R404
0R0603-PAD
3D3V_ICH_CL_S5
Layout Note: PCI decoupling
NO_STUFF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (3 of 4)
Size
Document Number
Columbia/Tangiz
Rev
-1
Date: Thursday, June 07, 2007
Sheet 18 of 45





Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

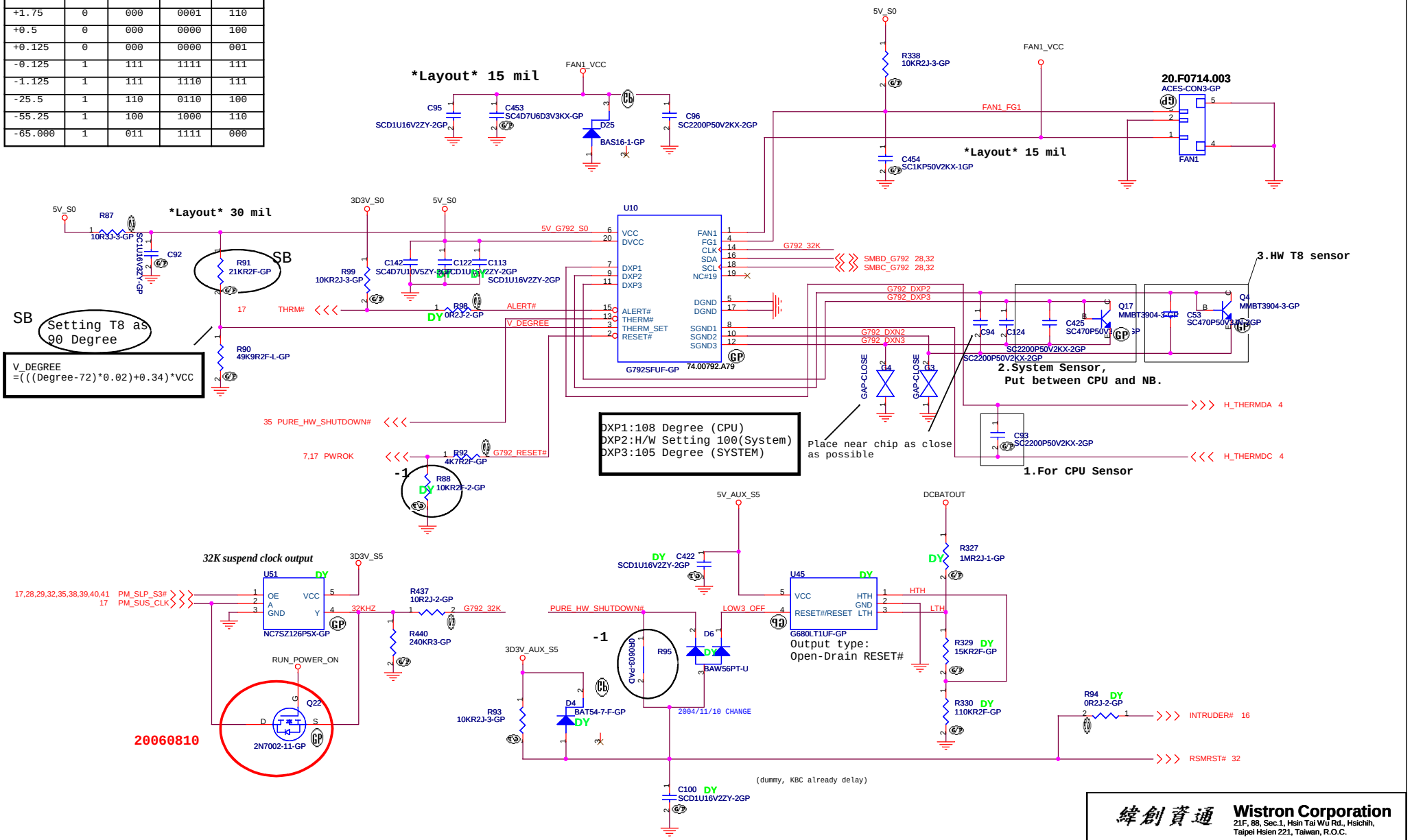
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH8-M (4 of 4)*

Size | Document Number: Columbia/Tangiz | Rev: -1

Date: Thursday, June 07, 2007 Sheet 19 of 45

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



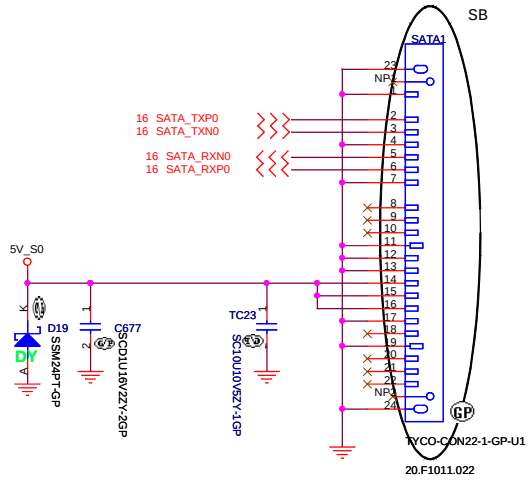
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

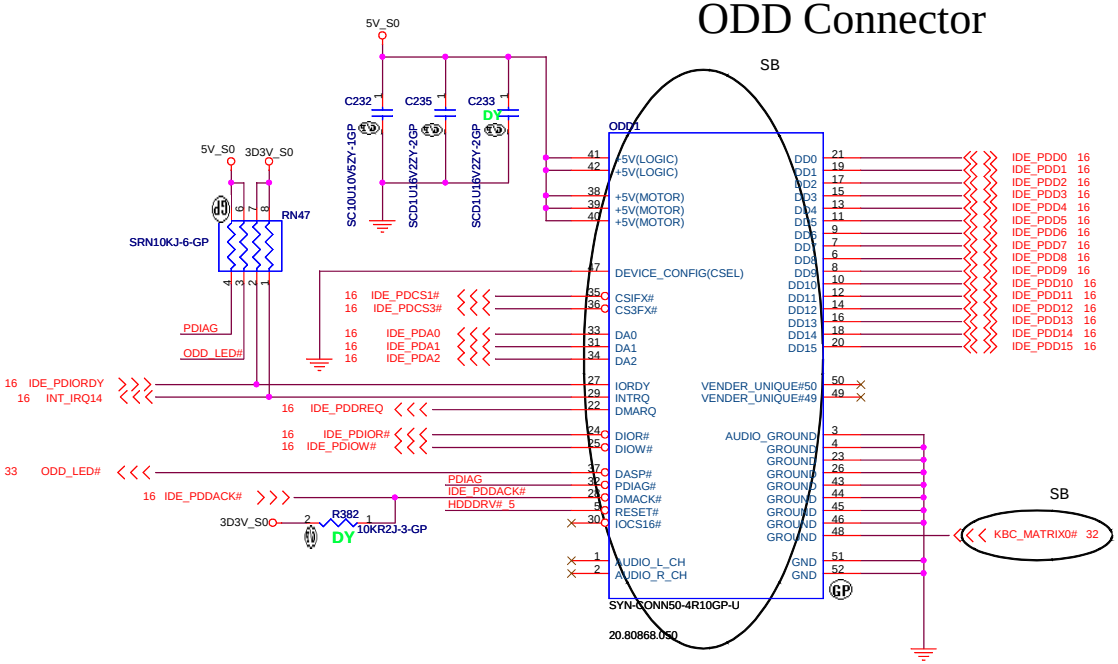
Size | Document Number: **Columbia/Tangiz** | Rev: -1M

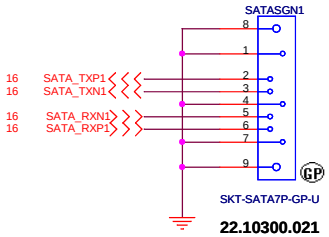
Date: Thursday, June 07, 2007 | Sheet 20 of 45

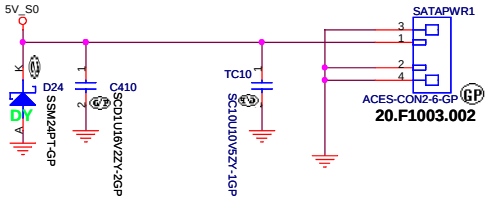
SATA HD Connector

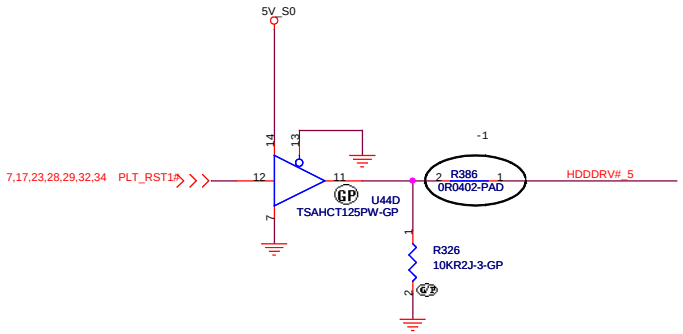


ODD Connector



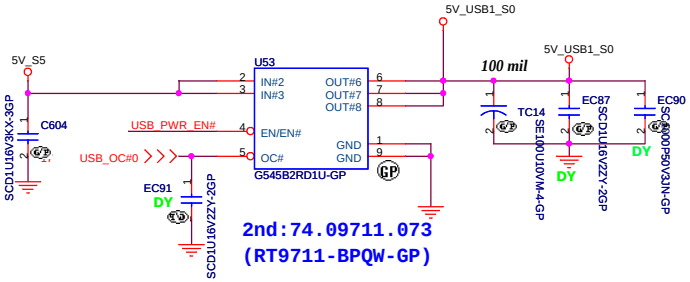


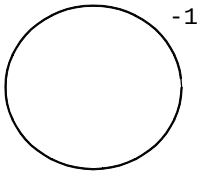


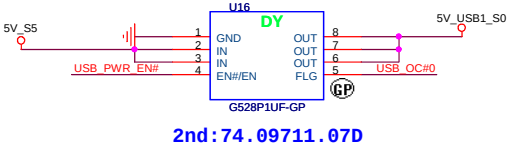


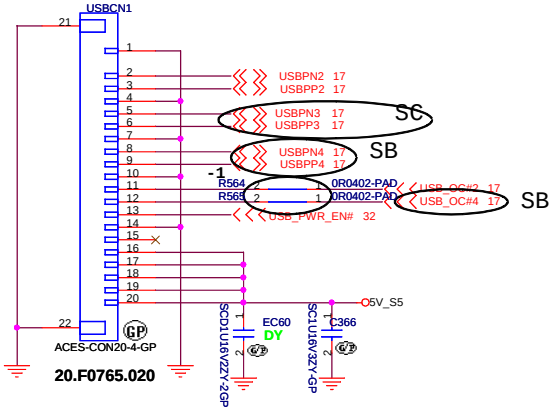
bom1

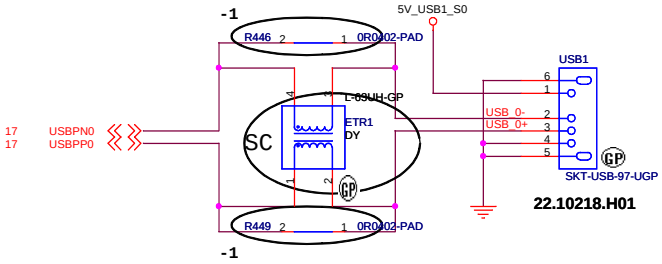
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD and CDROM***	
Size	Document Number **Columbia/Tangiz**	Rev -1M
Date: Thursday, June 07, 2007	Sheet 21 of 45	



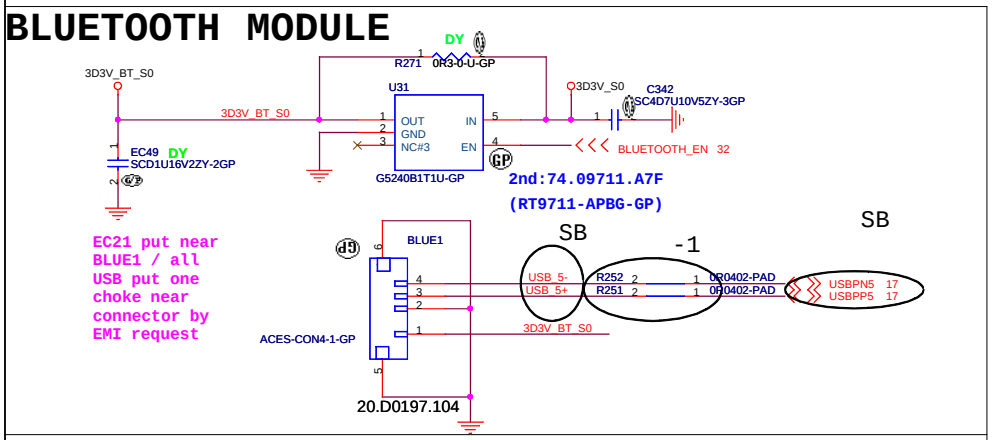




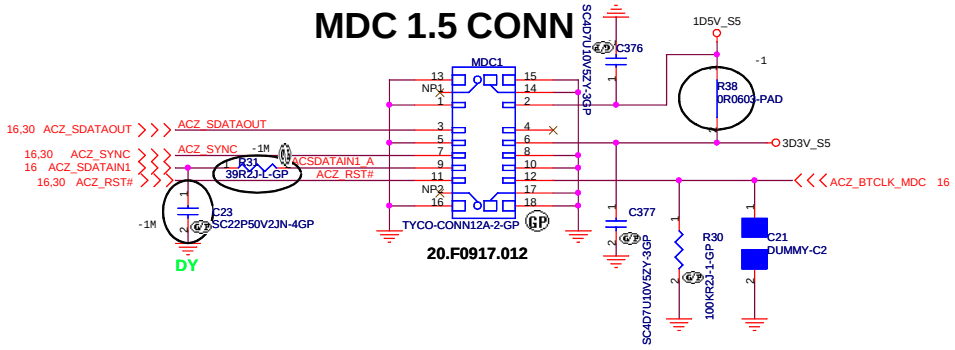


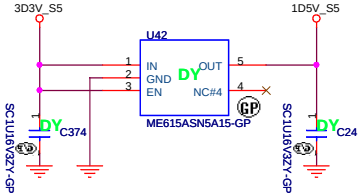


BLUETOOTH MODULE



MDC 1.5 CONN





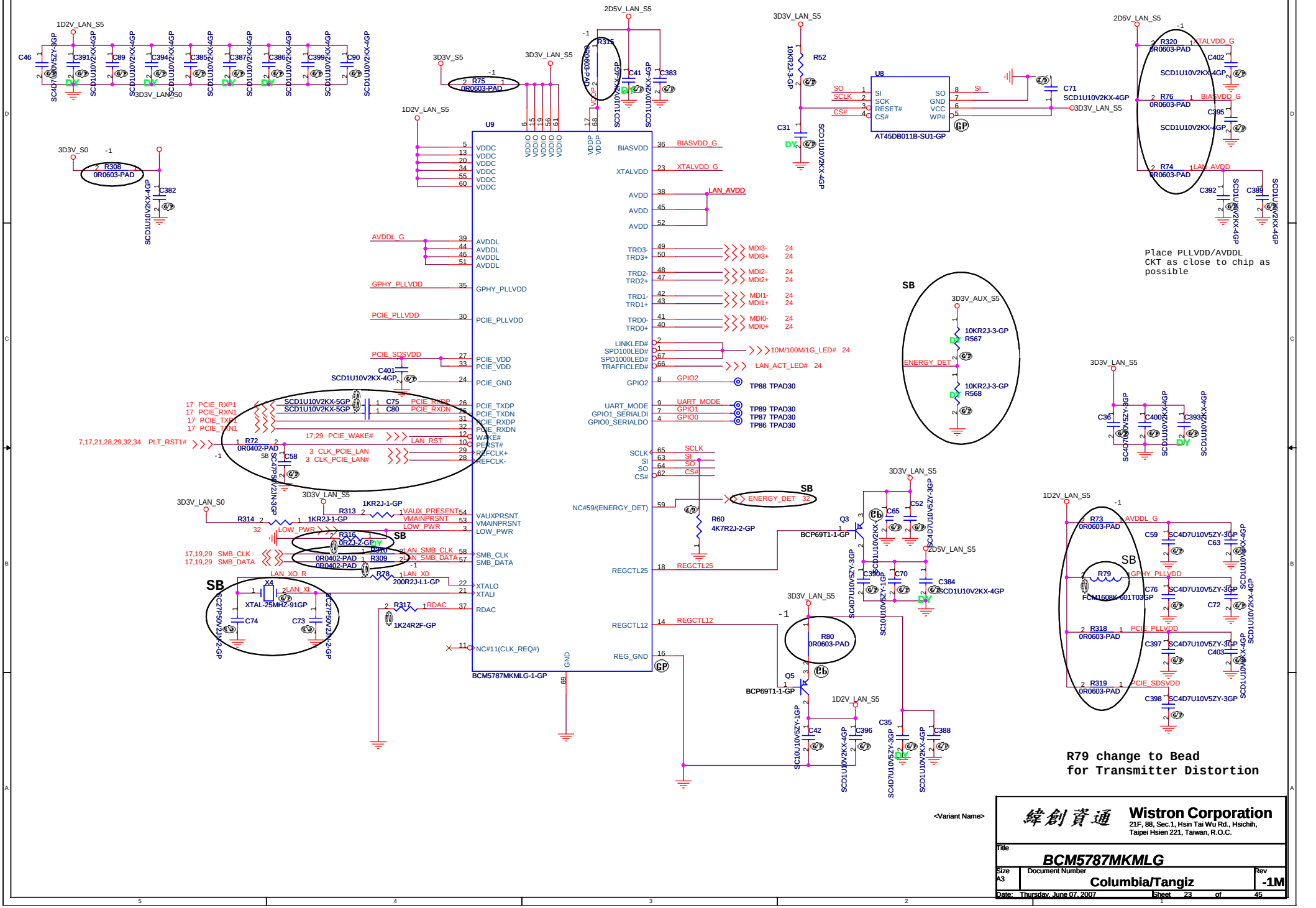
bom1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC / BLUETOOTH**

Size | Document Number: Columbia/Tangiz | Rev: -1M

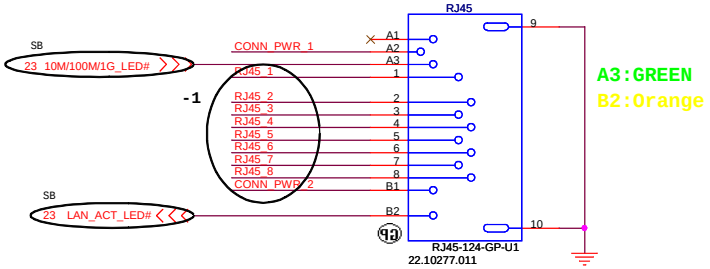
Date: Thursday, June 07, 2007 | Sheet 22 of 45


BCM5787MKMLG-1GP
U9
U8
AT45DB011B-SU1-GP
U4
XTAL-25MHZ-91GP
Q3
BCP69T1-1-GP
Q5
BCP69T1-1-GP
Place PLLVDD/AVDDL CKT as close to chip as possible
R79 change to Bead for Transmitter Distortion
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number
Columbia/Tangiz
Rev -1M
Date: Thursday, June 07, 2007
Sheet 23 of 45

LAN Connector

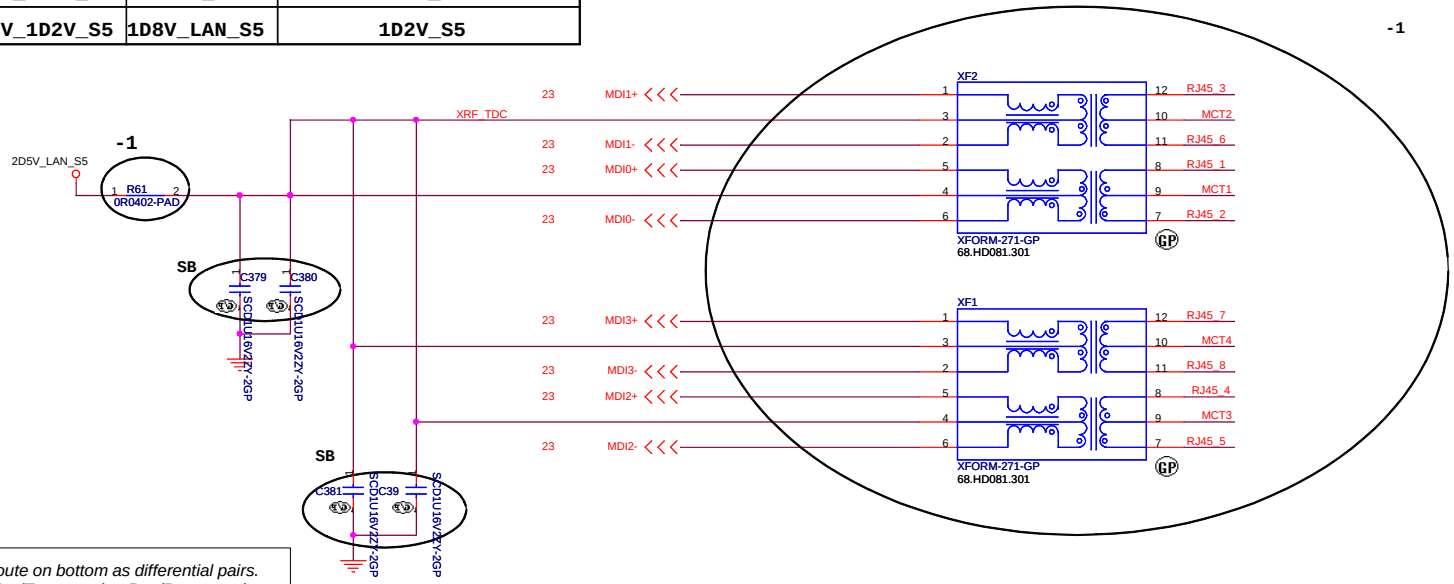
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

GIGA Lan Transformer



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

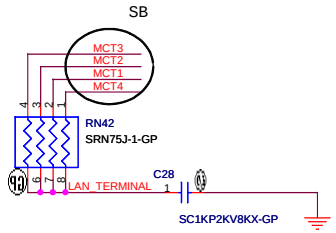


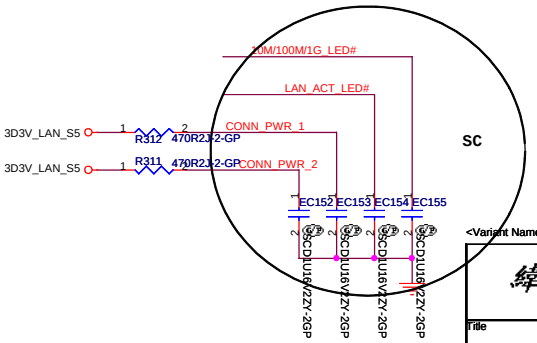
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

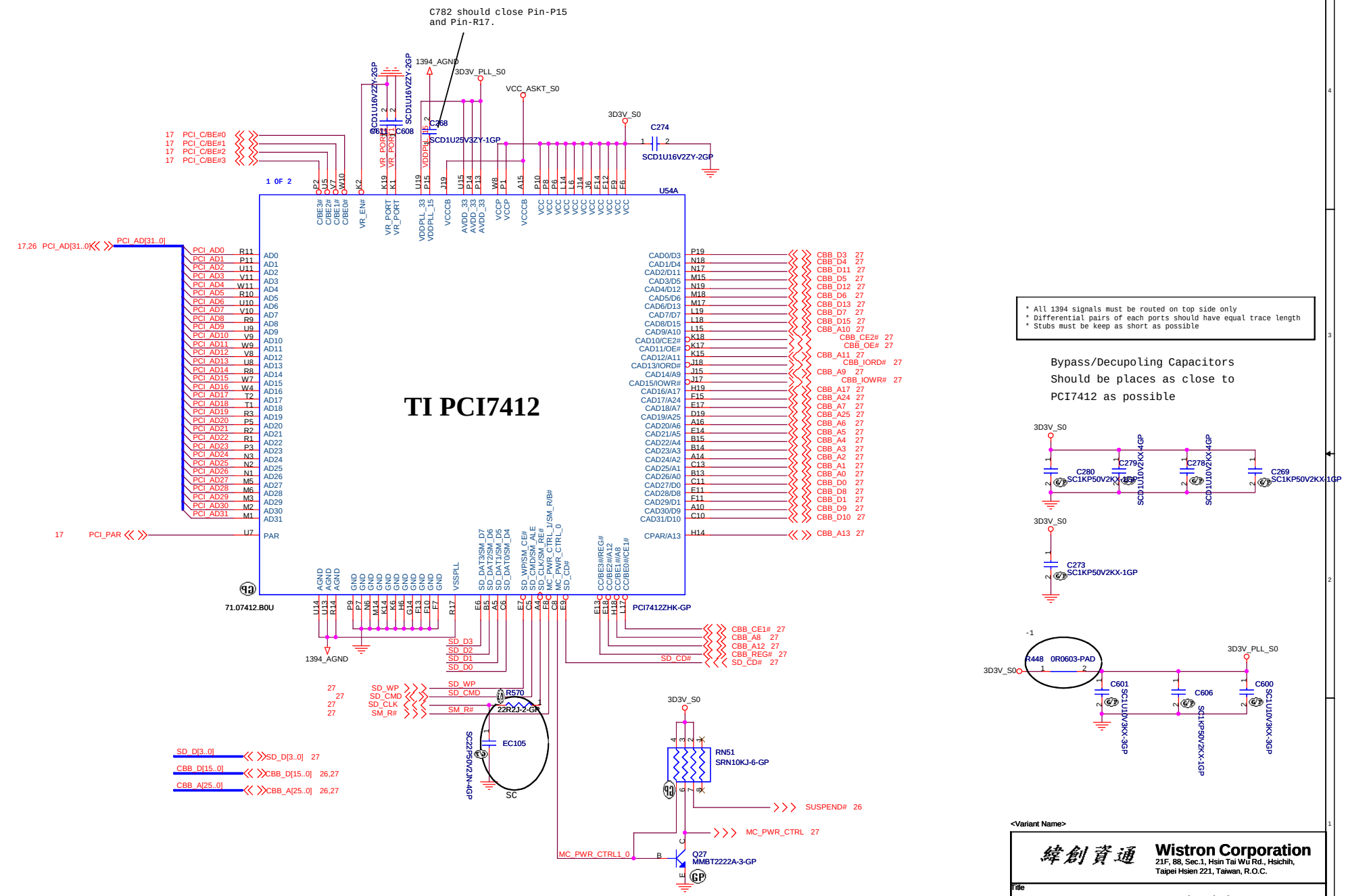


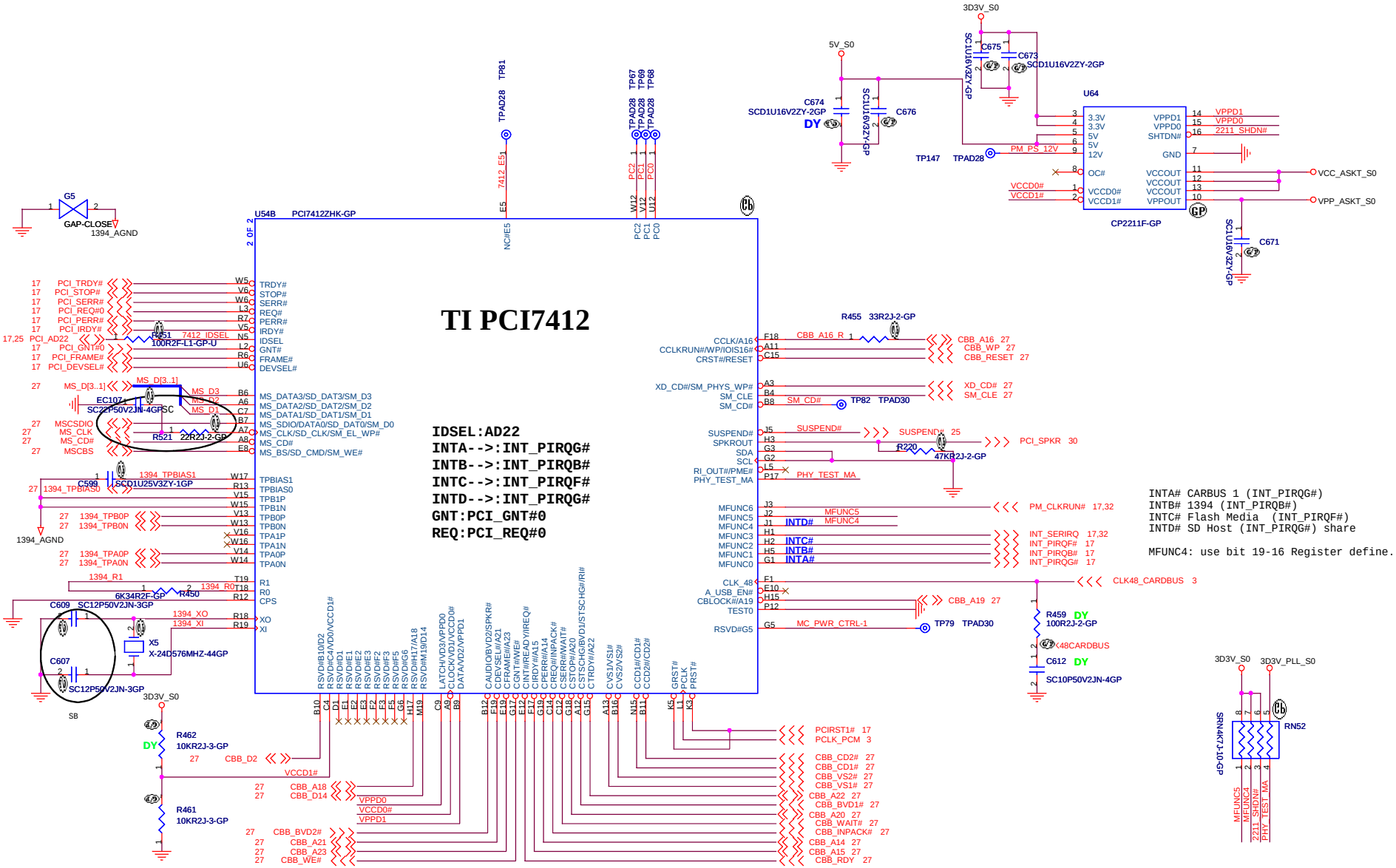


<variant_name>

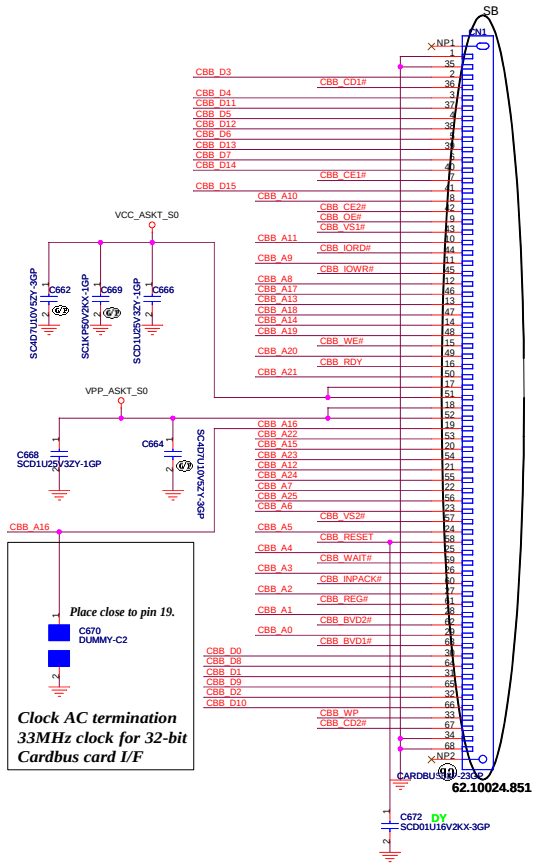
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M
Date: Thursday, June 07, 2007 | Sheet 24 of 45

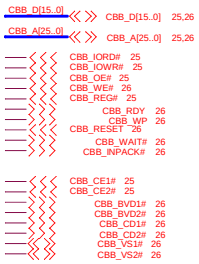

C782 should close Pin-P15
and Pin-R17.
1394_AGND
3D3V_PLL_S0
VCC_ASKT_S0
3D3V_S0
SCD1U16V2ZY-2GP
SCD1U25V3ZY-1GP
C274
C608
C611
C768
1 0F 2
U54A
TI PCI7412
PCI7412ZHK-GP
71.07412.B0U
PCI_AD[31..0]
PCI_PAR
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#2
PCI_C/BE#3
SD_D[3..0]
CBB_D[15..0]
CBB_A[25..0]
SD_WP
SD_CMD
SD_CLK
SM_R#
R570
22R2J-2-GP
EC105
SC22P50V2JN-4GP
SC
RN51
SRN10KJ-6-GP
SUSPEND# 26
MC_PWR_CTRL 27
MC_PWR_CTRL1_0
Q27
MMBT2222A-3-GP
SD_CD#
CBB_CE1# 27
CBB_A8 27
CBB_A12 27
CBB_REG# 27
* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible
Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible
C280
C279
C278
C269
C273
R448
0R0603-PAD
C601
C606
C600
SC1U10V3KX-3GP
SC1KP50V2KX-1GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (1 of 2)
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Thursday, June 07, 2007
Sheet 25 of 45

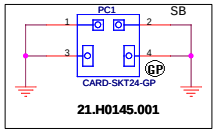

TI PCI7412
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share
MFUNC4: use bit 19-16 Register define.
U54B PCI7412ZHK-GP
CP2211F-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TI PCI7412 (2 of 2)
Columbia/Tangiz
-1M
Date: Thursday, June 07, 2007
Sheet 26 of 45

PCMCIA Socket

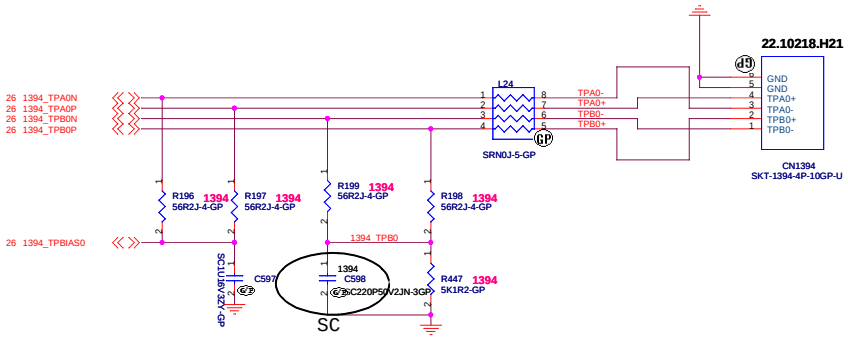


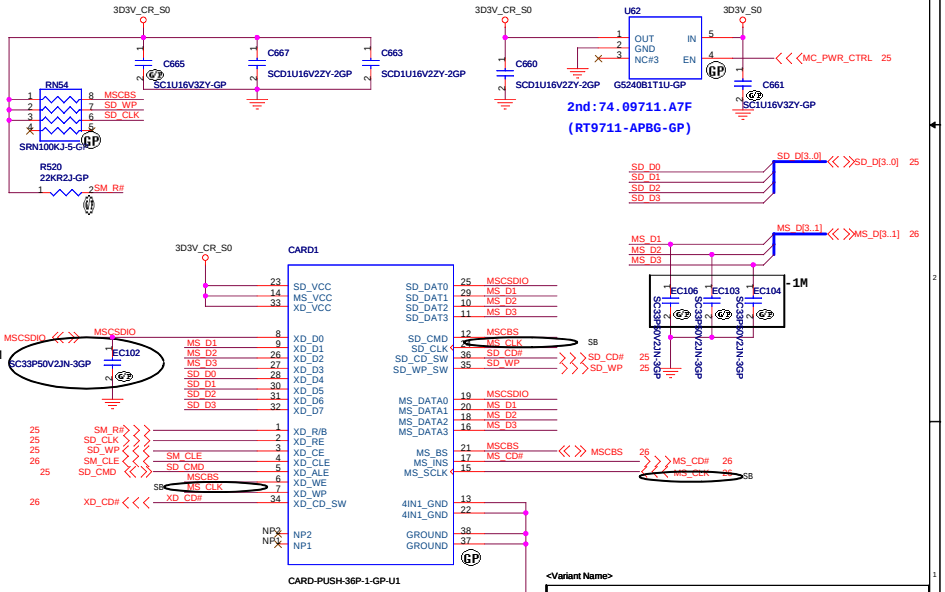
Cardbus I/F





1394 Connector





<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

Size | Document Number: Columbia/Tangiz | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 27 of 45

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

5V_S0
1D8V_S0
3D3V_S0
2D5V_S0

37,38,39,40,41 CPUCORE_ON
17,20,29,32,35,38,39,40,41 PM_SLP_S3#

R347 0R21-2-GP
R337 0R21-2-GP
C457 SCD1U25V3KX-GP
R579 0R0-0-U-GP
C456 SC10U10V5ZY-1GP
C458 SCD1U25V3KX-GP
C691 SCD1U25V3KX-GP
C692 SCD1U25V3KX-GP

MXM1
TYCO-CONN230A-GP-U3
20.F0871.230

14 LCD_TXBOUT0+
14 LCD_TXBOUT0-
14 LCD_TXBOUT1+
14 LCD_TXBOUT1-
14 LCD_TXBOUT2+
14 LCD_TXBOUT2-
14 LCD_TXBCLK+
14 LCD_TXBCLK-
LCD_TXACLK- 14
LCD_TXACLK+ 14
LCD_TXAOUT2- 14
LCD_TXAOUT2+ 14
LCD_TXAOUT1- 14
LCD_TXAOUT1+ 14
LCD_TXAOUT0- 14
LCD_TXAOUT0+ 14

15 NV_BLUE
15 NV_GREEN
15 NV_RED
15 NV_TV_COMP
15 NV_TV_LUMA
15 NV_TV_CRMA
NV_EDID_DAT 14
NV_EDID_CLK 14
NV_LCDVDD_ON 14
NV_BLON 32
NV_DVI_DAT 44
NV_DVI_CLK 44

TMDS_A_TX0+ 44
TMDS_A_TX0- 44
TMDS_A_TX1+ 44
TMDS_A_TX1- 44
TMDS_A_TX2+ 44
TMDS_A_TX2- 44
TMDS_A_TXC+ 44
TMDS_A_TXC- 44
DVI_A_HPD 44

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG

7,17,21,23,29,32,34 PLT_RST1#
PLT_RST1#_MXM
R367 0R0402-PAD
C478
SC100P50V2JN-3GP

20,32 SMBD_G792
20,32 SMBC_G792
R586 0R0402-PAD
R587 0R0402-PAD
SMBD_MXM
SMBC_MXM

35 MXM_THER

15 NV_HSYNC
15 NV_VSYNC
15 NV_DDCCLK
15 NV_DDCDAT

TPAD30 TP44 SPDIF_HDMI
TPAD30 TP112 GPU_BUFRST#
TPAD30 TP107 MP_INT
TPAD30 TP99 GPU_PRGM#
TPAD30 TP98 IGP_UTX2#
TPAD30 TP103 IGP_UTX2
TPAD30 TP108 TMDS_GPIO6_SW
TPAD30 TP148

TMDS_B_TX0+ TP115 TPAD30
TMDS_B_TX0- TP114 TPAD30
TMDS_B_TX1+ TP105 TPAD30
TMDS_B_TX1- TP104 TPAD30
TMDS_B_TX2+ TP111 TPAD30
TMDS_B_TX2- TP110 TPAD30
G72_27MHZ TP102 TPAD30
G72_27MHZSS TP113 TPAD30
DVI_B_HPD TP109 TPAD30
TMDS_B_TXC+ TP101 TPAD30
TMDS_B_TXC- TP100 TPAD30

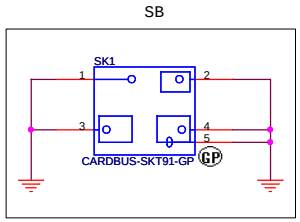
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

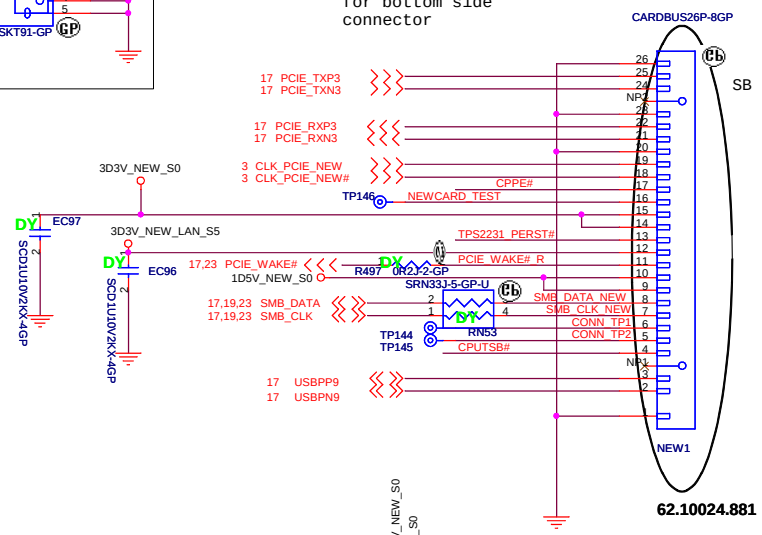
Title: Graphic MXM CONN
Size: A3
Document Number: Columbia/Tangiz
Rev: -1M
Date: Thursday, June 07, 2007
Sheet 28 of 45

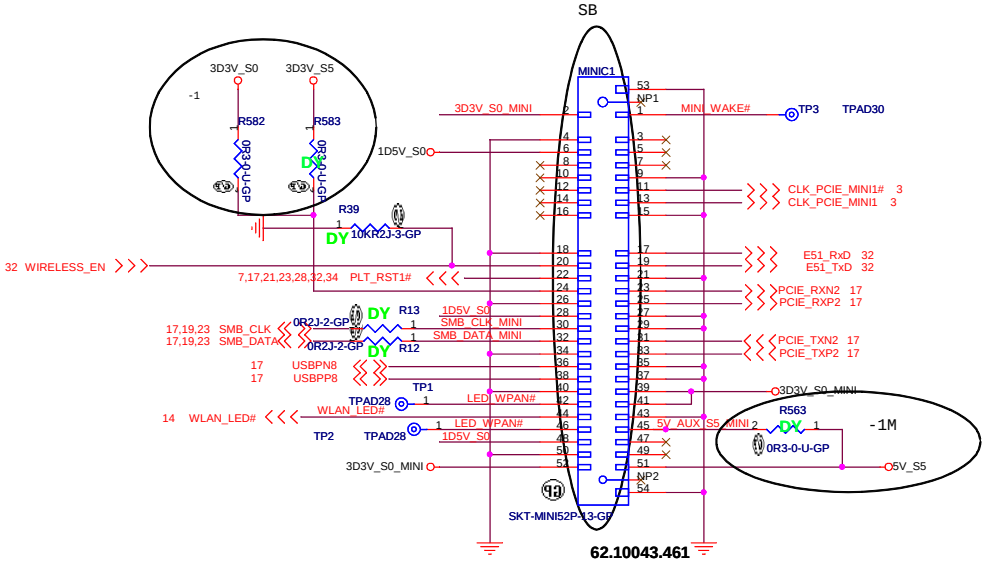
Mini Card Connector

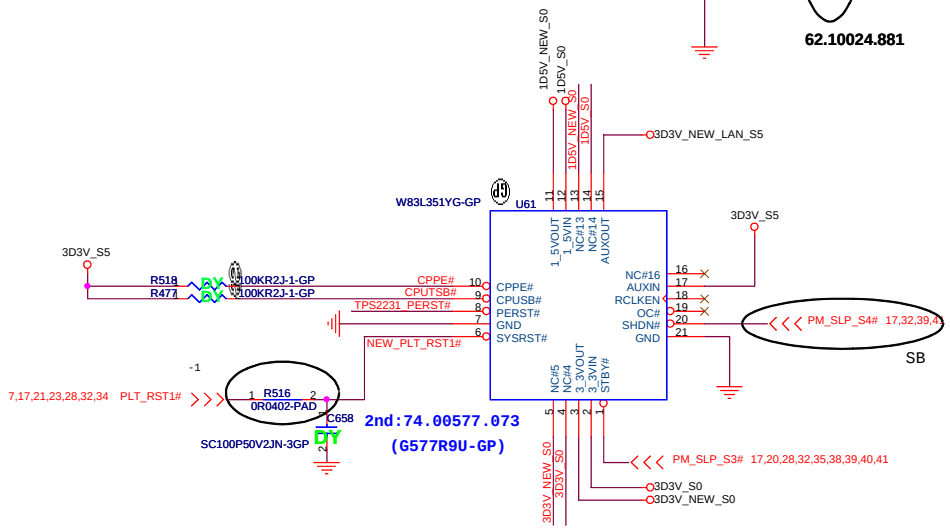
NEWCARD Connector

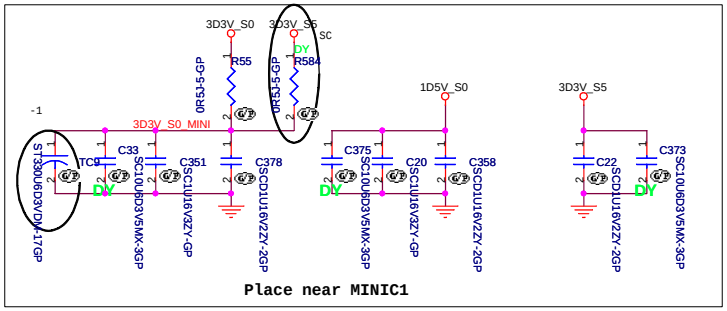


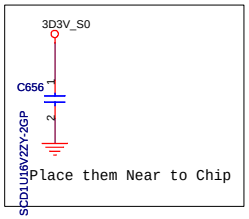
Reserve the symbol for bottom side connector

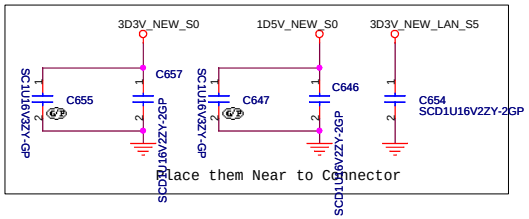






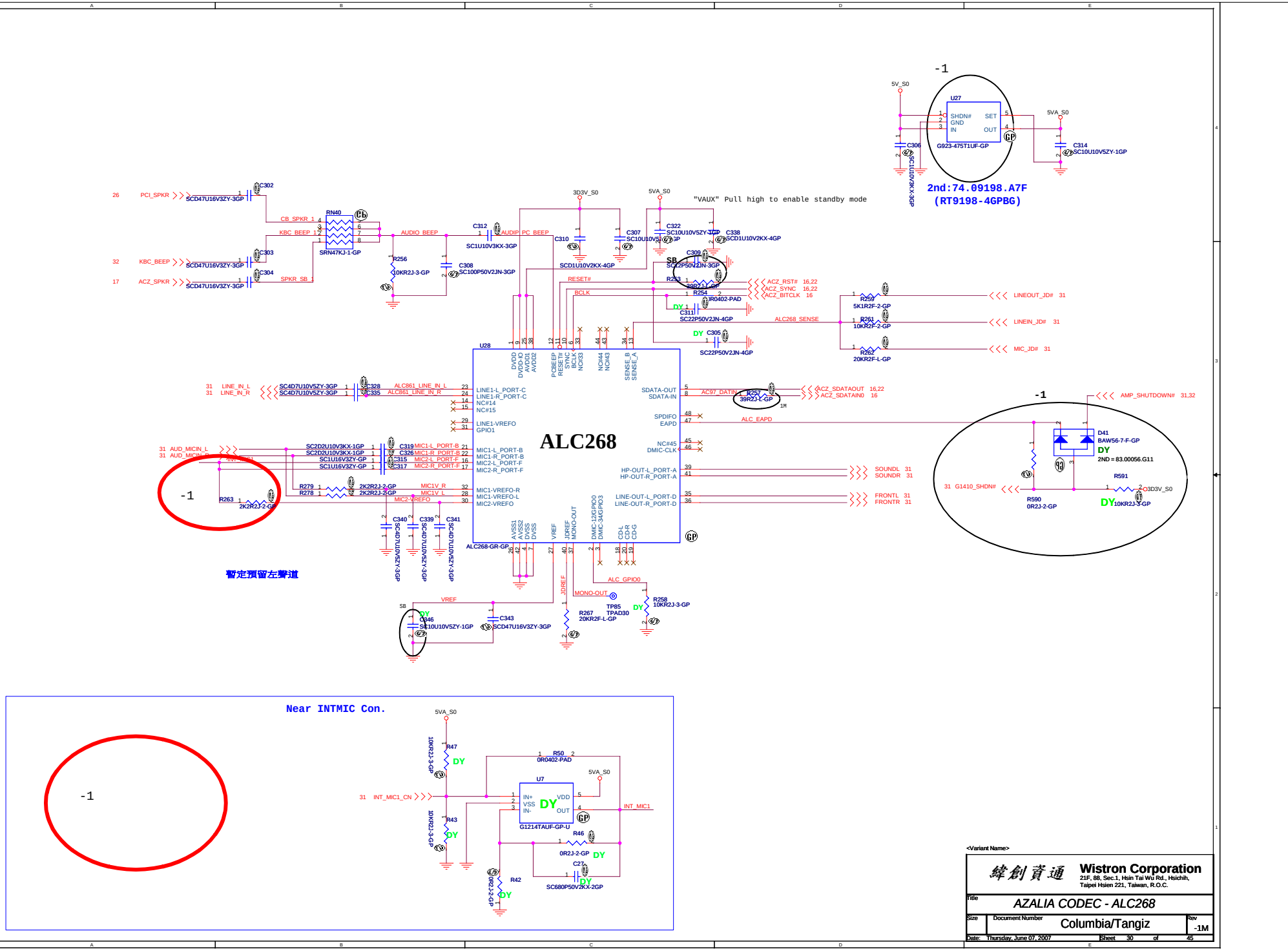






bom1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size	Document Number: Columbia/Tangiz	Rev: -1M
Date: Thursday, June 07, 2007	Sheet 29 of 45	


ALC268
U28
ALC268-GR-GP
"VAUX" Pull high to enable standby mode
2nd:74.09198.A7F
(RT9198-4GPBG)
U27
G923-475T1UF-GP
暫定預留左聲道
Near INTMIC Con.
U7
G1214TAUF-GP-U
-1
DY
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AZALIA CODEC - ALC268
Columbia/Tangiz
-1M
Thursday, June 07, 2007
Sheet 30 of 45

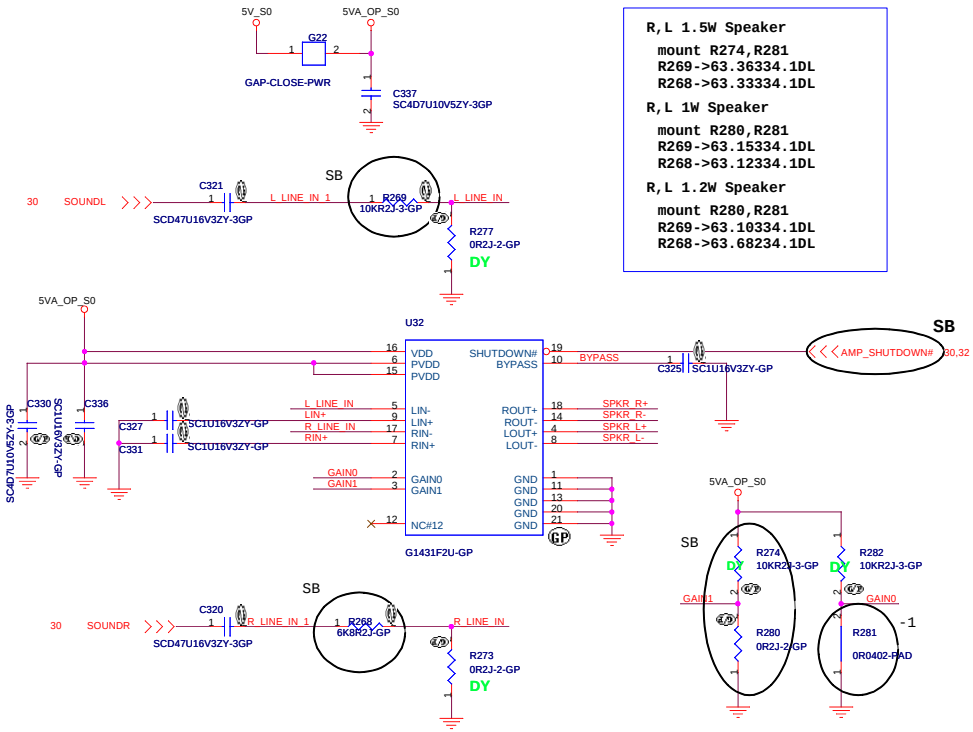
AUDIO OP AMPLIFIER

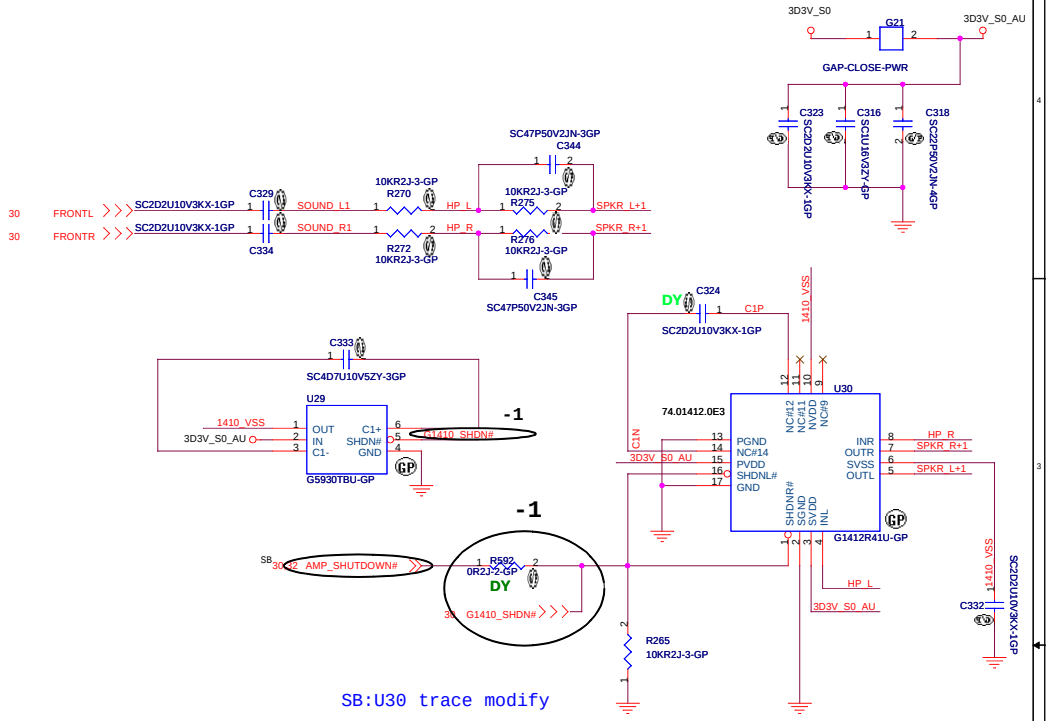
R,L 1.5W Speaker
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

R,L 1W Speaker
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

R,L 1.2W Speaker
mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

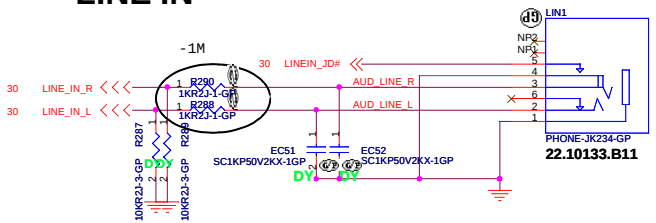
KBC_MUTE_GPIO8



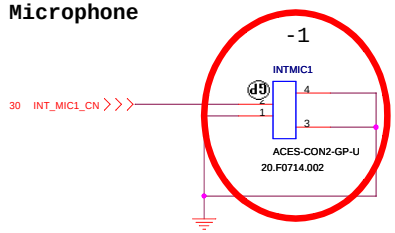


SB:U30 trace modify

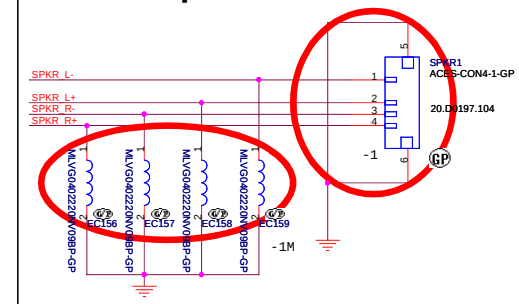
LINE IN



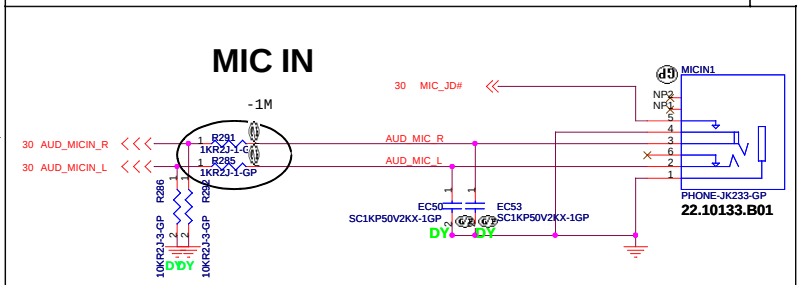
Internal Microphone



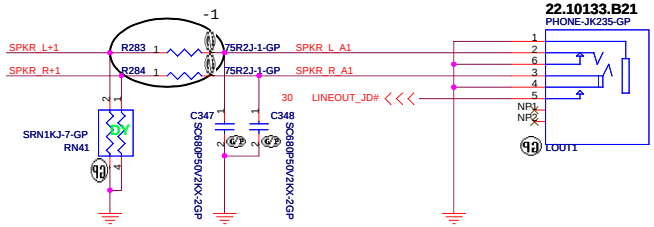
Internal Speaker



MIC IN

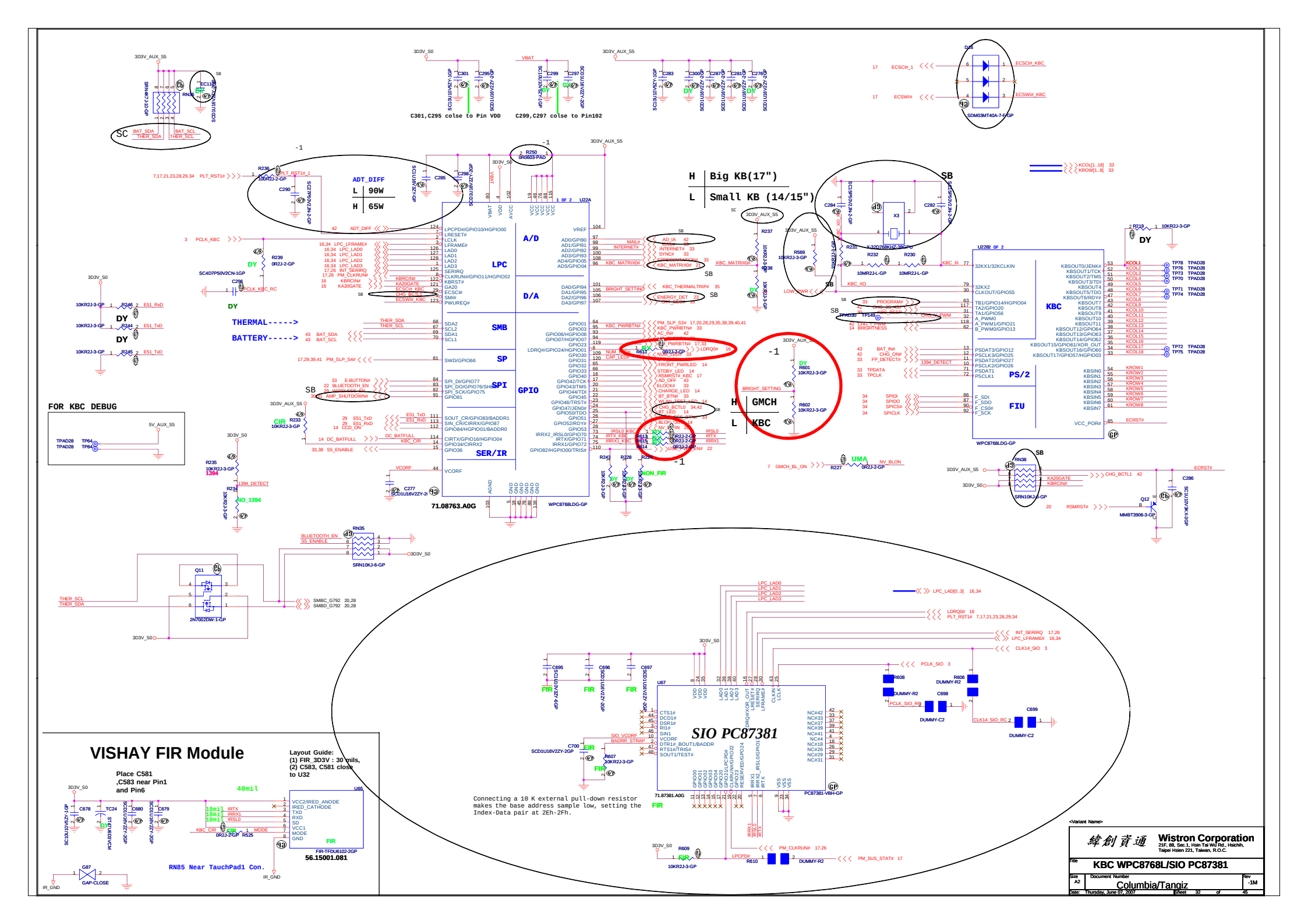


LINE OUT



<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO AMP AND JACK*	
Size	Document Number: Columbia/Tangiz	Rev: -1
Date: Thursday, June 07, 2007	Sheet 31 of 45	



VISHAY FIR Module

Place C581 ,C583 near Pin1 and Pin6

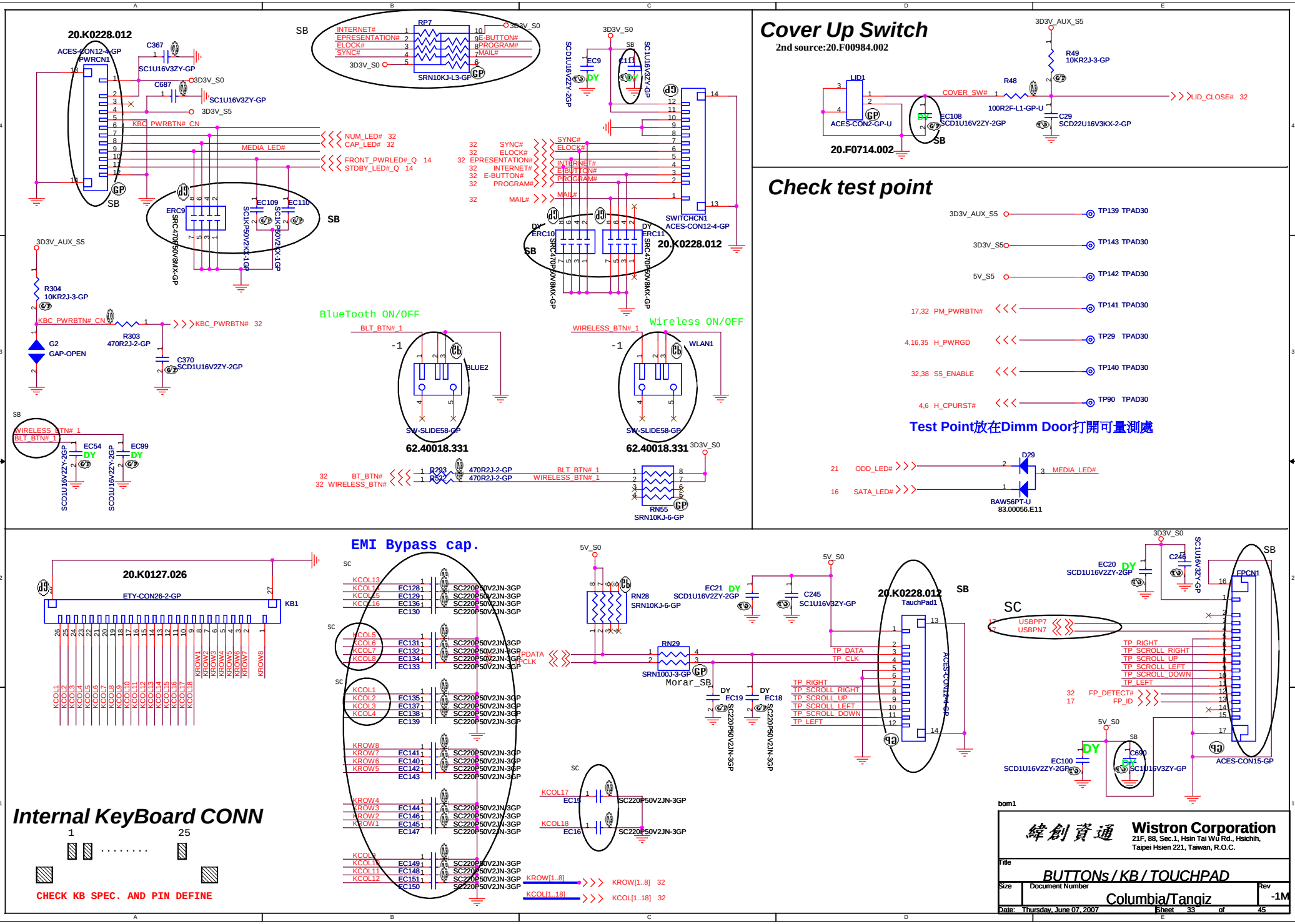
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

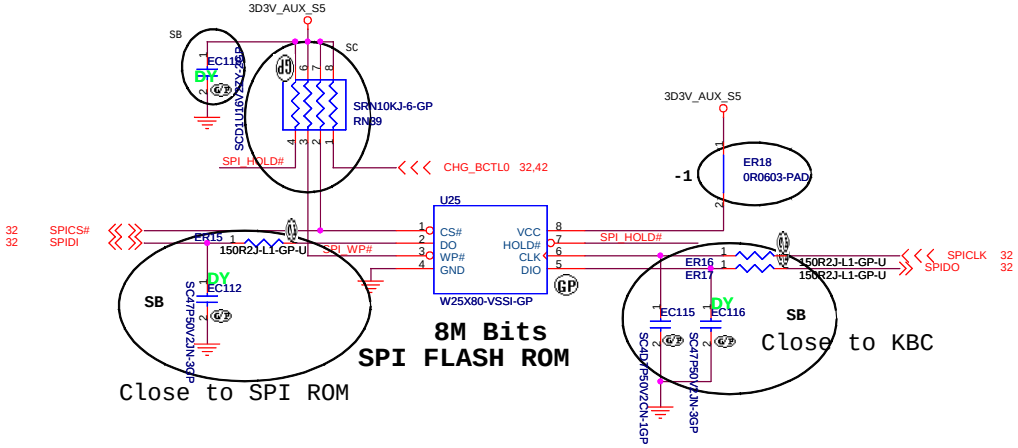
40mil

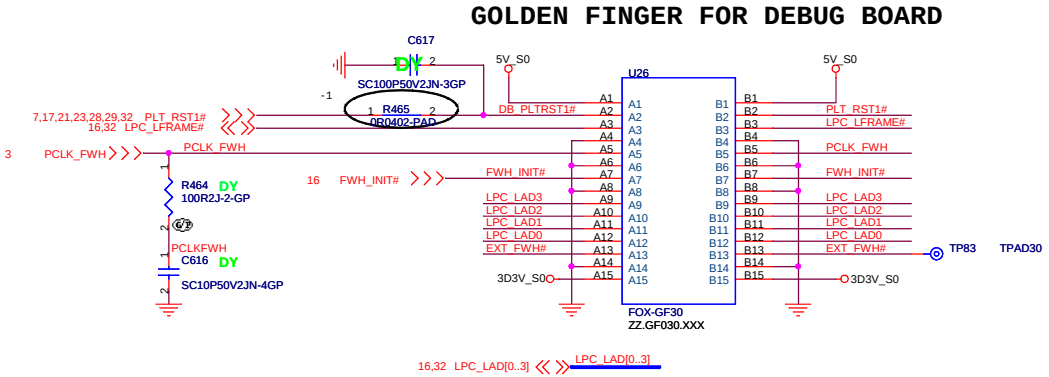
RN85 Near TauchPad1 Con.

56.15001.081

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC WPC8768L/SIO PC87381
Size A2	Document Number Columbia/Tangiz
Rev	-1M
Date: Thursday, June 07, 2007	Sheet 32 of 45


20.K0228.012
ACES-CON12-4-GP
PWRCN1
SB
C367
SC1U16V3ZY-GP
C687
SC1U16V3ZY-GP
3D3V_S0
3D3V_S5
KBC_PWRBTN#_CN
NUM_LED# 32
CAP_LED# 32
MEDIA_LED#
FRONT_PWRLED#_Q 14
STDBY_LED#_Q 14
ERC9
SRC470P50V8MX-GP
EC109
EC110
SCK1P50V2KX-1GP
SCK1P50V2KX-1GP
3D3V_AUX_S5
R304
10KR2J-3-GP
KBC_PWRBTN#_CN
R303
470R2J-2-GP
KBC_PWRBTN# 32
G2
GAP-OPEN
C370
SCD1U16V2ZY-2GP
WIRELESS_BTN#_1
BLT_BTN#_1
EC54
DY
EC99
DY
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
RP7
INTERNET#
EPRESENTATION#
ELOCK#
SYNC#
E-BUTTON#
PROGRAM#
MAIL#
SRN10KJ-L3-GP
SCD1U16V2ZY-2GP
EC9
DY
C111
SC1U16V3ZY-GP
SYNC#
ELOCK#
INTERNET#
E-BUTTON#
PROGRAM#
MAIL#
SWITCHCN1
ACES-CON12-4-GP
ERC10
ERC11
SRC470P50V8MX-GP
SRC470P50V8MX-GP
20.K0228.012
BlueTooth ON/OFF
BLT_BTN#_1
BLUE2
SW-SLIDE58-GP
62.40018.331
Wireless ON/OFF
WIRELESS_BTN#_1
WLAN1
SW-SLIDE58-GP
62.40018.331
BT_BTN#
WIRELESS_BTN#
R293
R522
470R2J-2-GP
470R2J-2-GP
BLT_BTN#_1
WIRELESS_BTN#_1
RN55
SRN10KJ-6-GP
Cover Up Switch
2nd source:20.F00984.002
3D3V_AUX_S5
R49
10KR2J-3-GP
LID1
ACES-CON2-GP-U
R48
100R2F-L1-GP-U
COVER_SW#
LID_CLOSE# 32
EC108
SCD1U16V2ZY-2GP
C29
SCD22U16V3KX-2-GP
20.F0714.002
Check test point
3D3V_AUX_S5
TP139 TPAD30
3D3V_S5
TP143 TPAD30
5V_S5
TP142 TPAD30
17,32 PM_PWRBTN#
TP141 TPAD30
4,16,35 H_PWRGD
TP29 TPAD30
32,38 S5_ENABLE
TP140 TPAD30
4,6 H_CPURST#
TP90 TPAD30
Test Point放在Dimm Door打開可量測處
21 ODD_LED#
16 SATA_LED#
D29
MEDIA_LED#
BAW56PT-U
83.00056.E11
20.K0127.026
ETY-CON26-2-GP
KB1
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KCOL17
KCOL18
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
EMI Bypass cap.
SC
SC220P50V2JN-3GP
KROW[1..8]
KCOL[1..18]
KROW[1..8] 32
KCOL[1..18] 32
RN28
SRN10KJ-6-GP
RN29
SRN100J-3-GP
Morar_SB
EC21
DY
SCD1U16V2ZY-2GP
C245
SC1U16V3ZY-GP
EC19
DY
EC18
DY
20.K0228.012
TauchPad1
ACES-CON14-GP
TP_DATA
TP_CLK
TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT
EC20
DY
SCD1U16V2ZY-2GP
C246
SC1U16V3ZY-GP
FPCN1
USBPP7
USBPN7
FP_DETECT#
FP_ID
EC100
DY
SCD1U16V2ZY-2GP
C690
DY
SC1U16V3ZY-GP
ACES-CON15-GP
Internal KeyBoard CONN
1
25
CHECK KB SPEC. AND PIN DEFINE
bom1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD
Size
Document Number
Columbia/Tangiz
Rev
-1M
Date: Thursday, June 07, 2007
Sheet 33 of 45





<Variant Name>

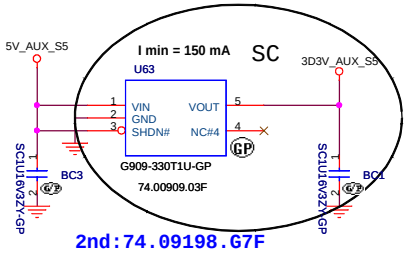
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

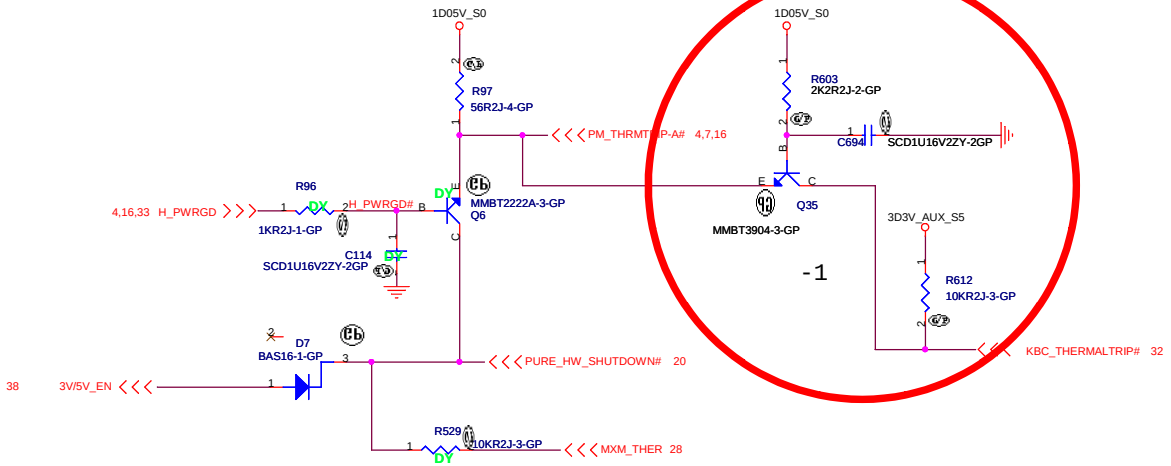
Title: BIOS

Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M

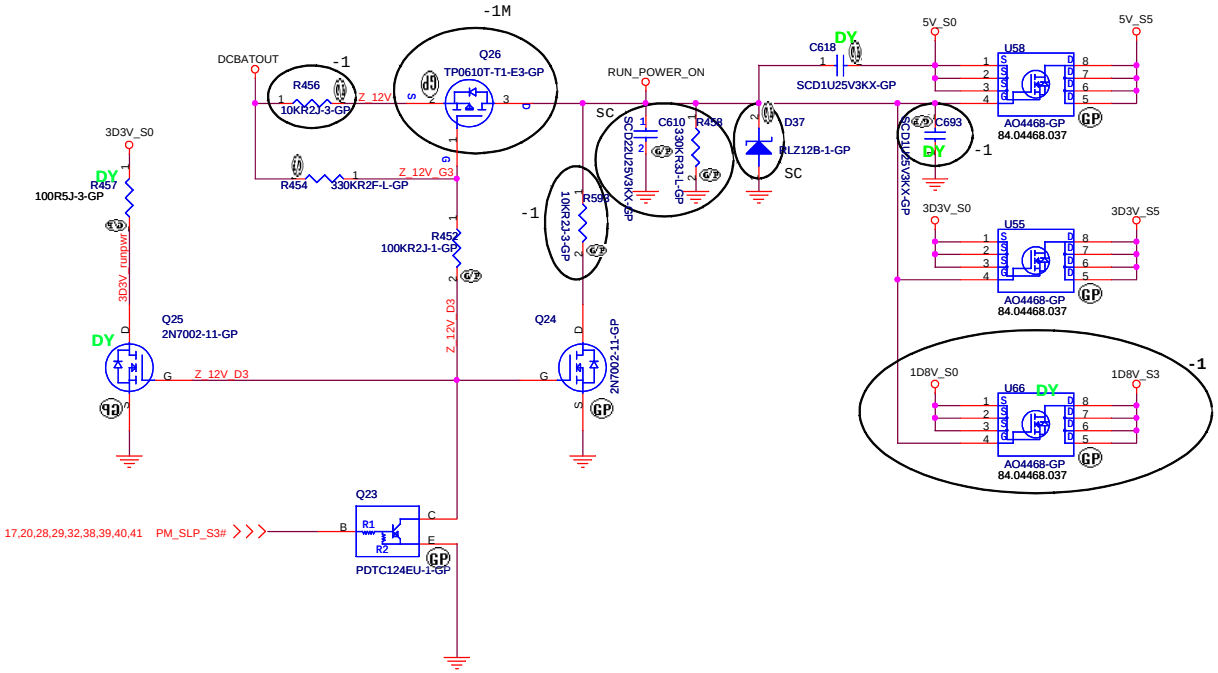
Date: Thursday, June 07, 2007 | Sheet 34 of 45

Aux Power 3D3V_AUX_S5





Run Power



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size | Document Number: Columbia/Tangiz | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 35 of 45

CPU_CORE
MAX8770

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#

VCC_SENSE
VSS_SENSE

DCBATOUT_6262
5V_S0
5V_S0

VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)

Input Signal
PSI# (I / 3.3V)
SHDN#(I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)

Voltage Sense
CCI(I / Vcore)
GNDS(I / Vcore)

Input Power
VCC(I)
VCC(I)
VDD(I)

Output Signal
PWRG(OD / 3.3V)

Output Power
VCC_CORE_PWR(O)

VGATE_PWRGD
VCC_CORE_S0(Imax=47A)

MAX8717
1D8V/1D05V

5V_S0
DCBATOUT_8717

PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (8.5A)
1D05V_S0 (9.5A)

0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D9V_S0 (1.5A)
0D9V_S3

TPS51100

1D25V_S0

1D5V_S0
PM_SLP_S3#

VIN
EN
1D25V(O)
POK

1D25V_S0 (4A)
CPUCORE_ON

APL5915

MAX8744
5V/3D3V

8744_SHDN#
S5_ENABLE
S5_ENABLE

DCBATOUT_8744

Input Signal
SHDN#
ON3
ON5

Input Power
VIN

Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)

Output Power
PGOOD5(O)
PGOOD3(O)

CPUCORE_ON
CPUCORE_ON
5V_S5 (6A)
3D3V_S5 (7A)

2D5V_S0

3D3V_S0

VIN
1D05V(O)

2D5V_S0 (300mA)

APL5308

1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
POK

1D5V_S0 (4A)
CPUCORE_ON

APL5912

Charger ISL6255

CHGON#/OFF
BT_TH

AD+

Input Signal
ICTL
PKPRES

Input Power
ACIN

Output Signal
BATT
ACOK

Output Power
VOUT (O)
VOUT (O)

BT+SENSE
AC_IN
BT+
DCBATOUT

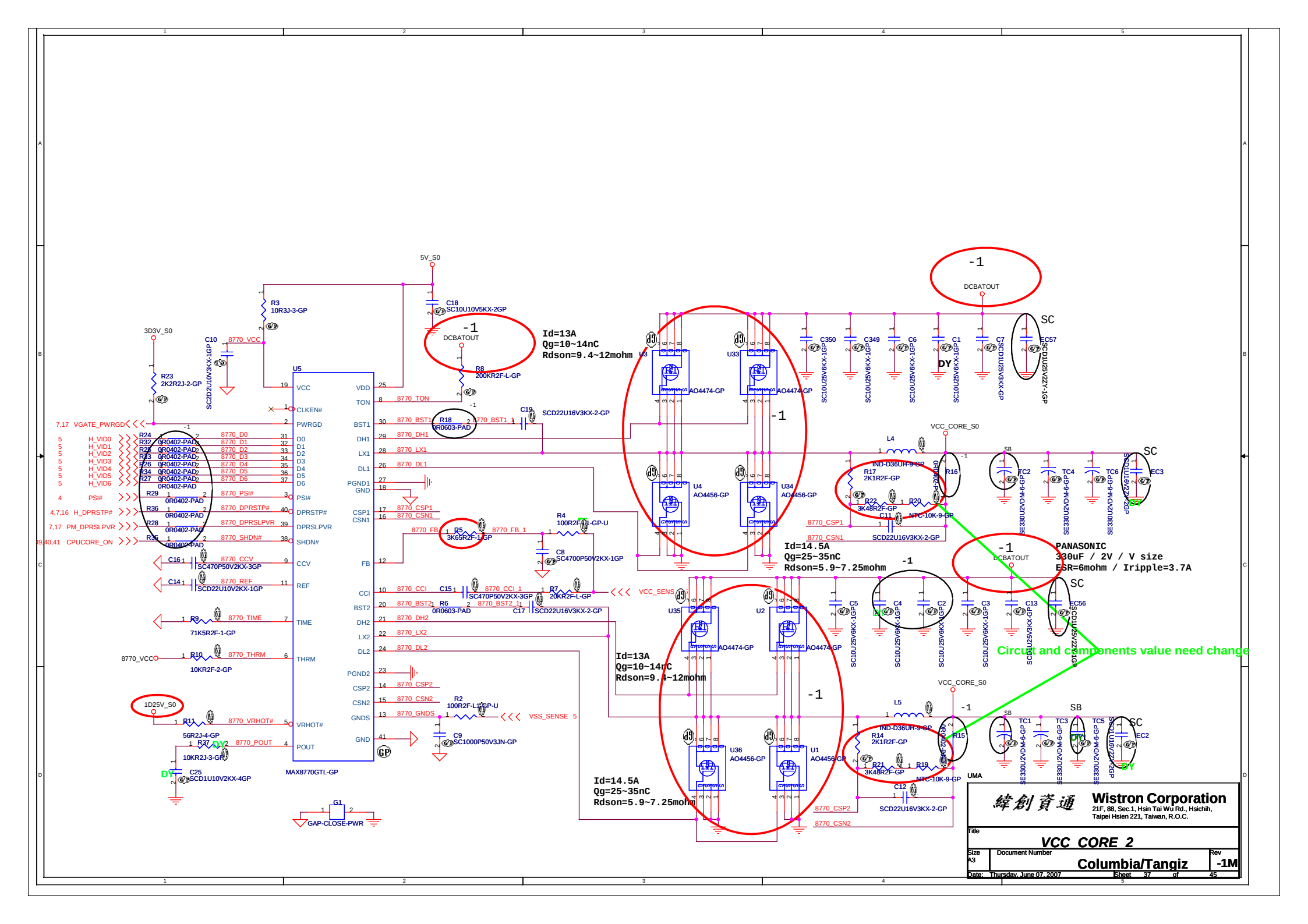
<Variant Name>

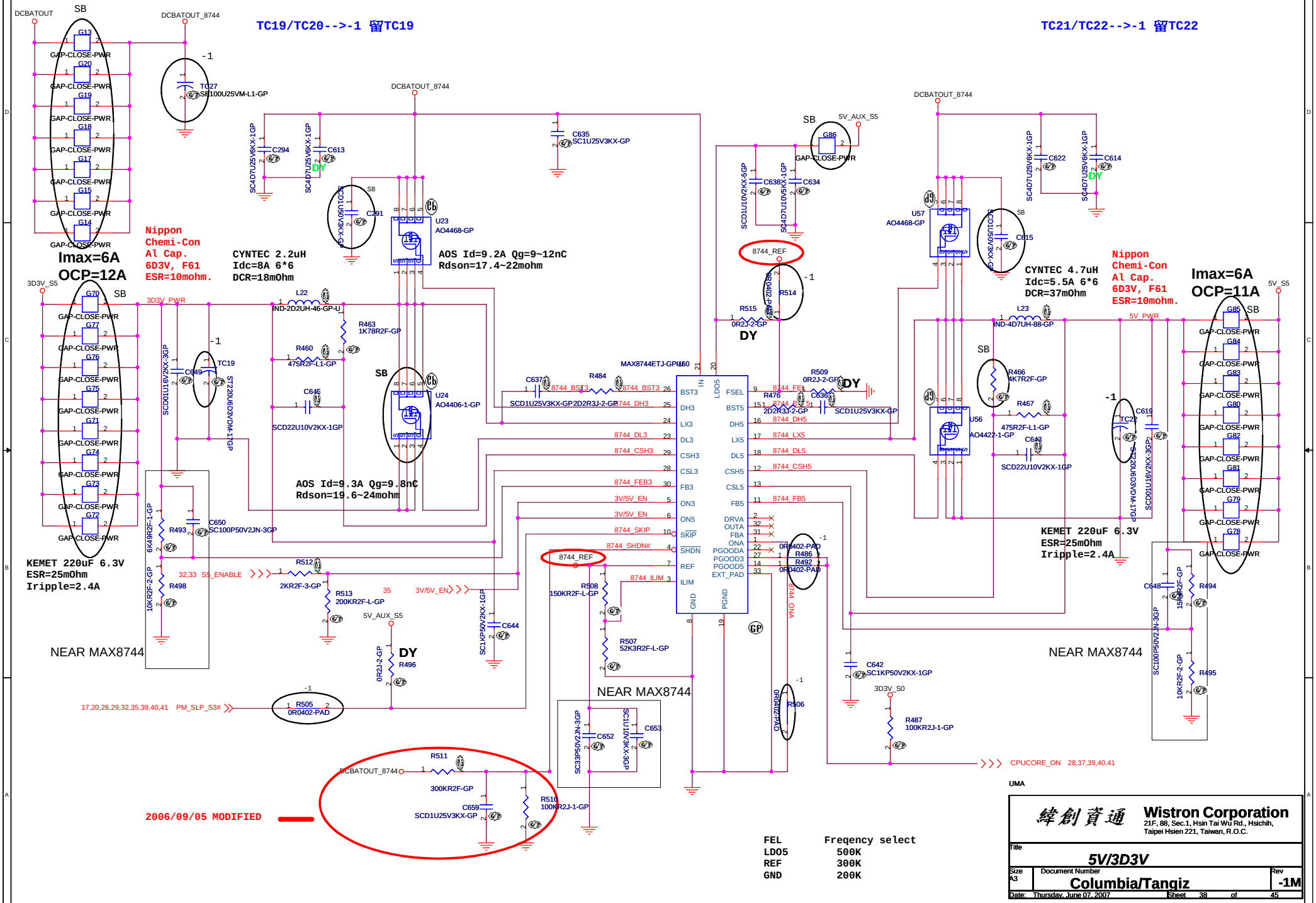
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

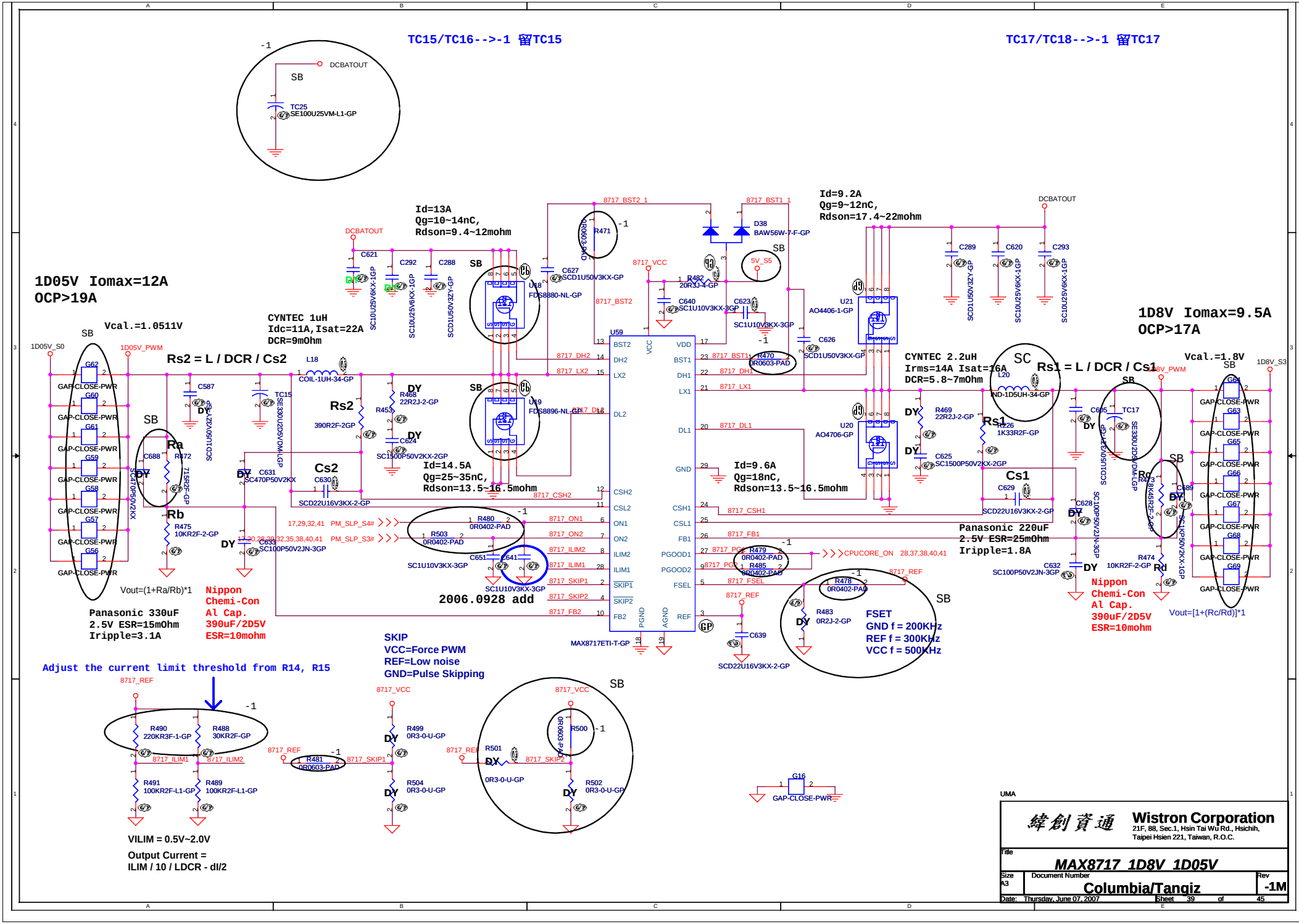
Title: **Power Block Diagram**

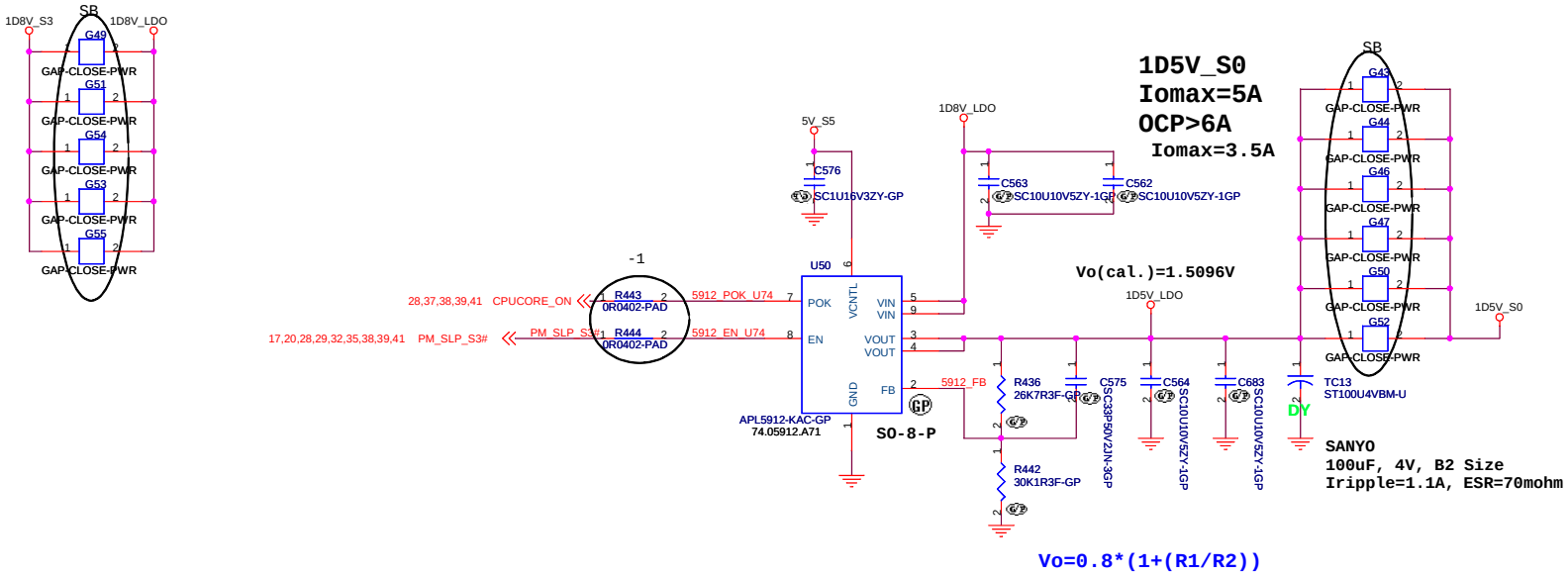
Size: A3 | Document Number: Columbia/Tangiz | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 36 of 45


5V_S0
3D3V_S0
1D25V_S0
8770_VCC
U5
MAX8770GTL-GP
VCC
CLKEN#
PWRGD
D0
D1
D2
D3
D4
D5
D6
PSI#
DPRSTP#
DPRSLPVR
SHDN#
CCV
REF
TIME
THRM
VRHOT#
POUT
VDD
TON
BST1
DH1
LX1
DL1
PGND1
GND
CSP1
CSN1
FB
CCI
BST2
DH2
LX2
DL2
PGND2
CSP2
CSN2
GNDS
GND
7,17 VGATE_PWRGD
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
4 PSI#
4,7,16 H_DPRSTP#
7,17 PM_DPRSLPVR
9,40,41 CPUCORE_ON
8770_TON
8770_BST1
8770_DH1
8770_LX1
8770_DL1
8770_CSP1
8770_CSN1
8770_FB
8770_FB_1
8770_CCI
8770_CCI_1
8770_BST2
8770_BST2_1
8770_DH2
8770_LX2
8770_DL2
8770_CSP2
8770_CSN2
8770_GNDS
VSS_SENSE 5
VCC_SENS
R3 10R3J-3-GP
R23 2K2R2J-2-GP
C10 SCD2U10V3KX-1GP
C18 SC10U10V5KX-2GP
R8 200KR2F-L-GP
C19 SCD22U16V3KX-2-GP
R18 0R0603-PAD
R24 R32 R25 R23 R26 R34 R27 0R0402-PAD
R29 0R0402-PAD
R36 0R0402-PAD
R28 0R0402-PAD
R35 0R0402-PAD
C16 SC470P50V2KX-3GP
C14 SCD22U10V2KX-1GP
R9 71K5R2F-1-GP
R10 10KR2F-2-GP
R11 56R2J-4-GP
R37 10KR2J-3-GP
C25 SCD1U10V2KX-4GP
R5 3K65R2F-1-GP
R4 100R2F-L-GP-U
C8 SC4700P50V2KX-1GP
C15 SC470P50V2KX-3GP
R7 20KR2F-L-GP
R6 0R0603-PAD
C17 SCD22U16V3KX-2-GP
R2 100R2F-L-GP-U
C9 SC1000P50V3JN-GP
G1 GAP-CLOSE-PWR
DCBATOUT
-1
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
U3 U33 U4 U34 U35 U2 U36 U1
AO4474-GP
AO4456-GP
C350 C349 C6 C1 C7 SC10U25V6KX-1GP
EC57 SCD1U25V2ZZ-1GP
DY
VCC_CORE_S0
L4 L5 IND-D36UH-9-GP
R17 2K1R2F-GP
R22 3K48R2F-GP
R20 NTC-10K-9-GP
C11 SCD22U16V3KX-2-GP
R16 R15 0R0402-PAD
SB
TC2 TC4 TC6 SE330U2VDM-6-GP
EC3 EC2 SCD1U25V2ZZ-1GP
SC
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=7.7A
C5 C4 C2 C3 C13 SC10U25V6KX-1GP
EC56 SCD1U25V3KX-GP
Circuit and components value need change
R14 2K1R2F-GP
R21 3K48R2F-GP
R19 NTC-10K-9-GP
C12 SCD22U16V3KX-2-GP
TC1 TC3 TC5 SE330U2VDM-6-GP
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VCC_CORE_2
Size A3
Document Number
Columbia/Tangiz
Rev -1M
Date: Thursday, June 07, 2007
Sheet 37 of 45


TC19/TC20-->-1 留TC19
TC21/TC22-->-1 留TC22
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
Imax=6A OCP=12A
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
Imax=6A OCP=11A
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
NEAR MAX8744
NEAR MAX8744
2006/09/05 MODIFIED
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
5V/3D3V
Columbia/Tangiz
-1M
Thursday, June 07, 2007
38 of 45


TC15/TC16-->-1 留TC15
TC17/TC18-->-1 留TC17
1D05V Iomax=12A
OCP>19A
Vcal.=1.0511V
Rs2 = L / DCR / Cs2
CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm
Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm
Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
1D8V Iomax=9.5A
OCP>17A
Vcal.=1.8V
Rs1 = L / DCR / Cs1
CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm
Vout=(1+Ra/Rb)*1
Vout=[1+(Rc/Rd)]*1
Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
2006.0928 add
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R14, R15
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dl/2
MAX8717ETI-T-GP
U59
U18 FDS8880-NL-GP
U19 FDS8896-NL-GP
U20 AO4706-GP
U21 AO4406-1-GP
D38 BAW56W-7-F-GP
L18 COIL-1UH-34-GP
L20 IND-1D5UH-34-GP
Rs2 390R2F-2GP
Rs1 1K33R2F-GP
Ra 715R2F-GP
Rb R475 10KR2F-2-GP
Rc 38K45R2F-2-GP
Rd R474 10KR2F-2-GP
Cs2 SCD22U16V3KX-2-GP
Cs1 SCD22U16V3KX-2-GP
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MAX8717_1D8V_1D05V
Columbia/Tangiz
-1M
Date: Thursday, June 07, 2007
Sheet 39 of 45

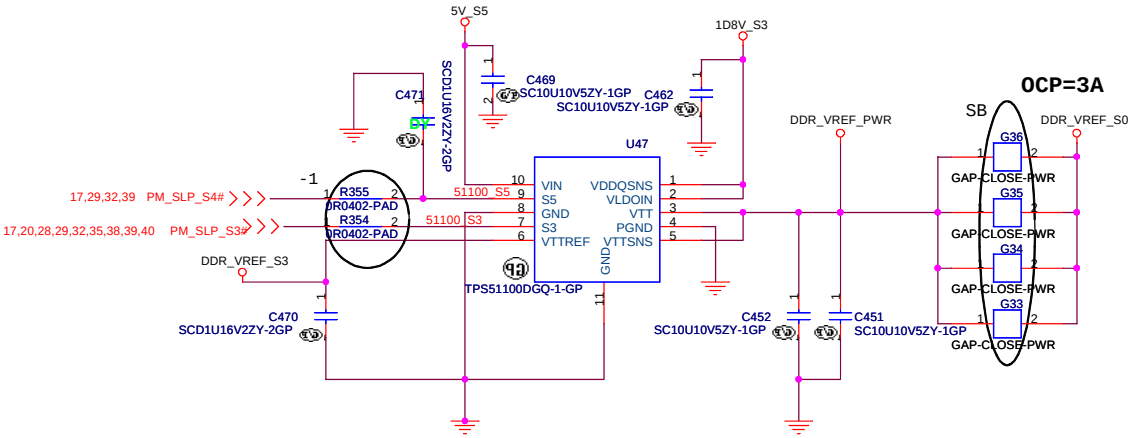


UMA

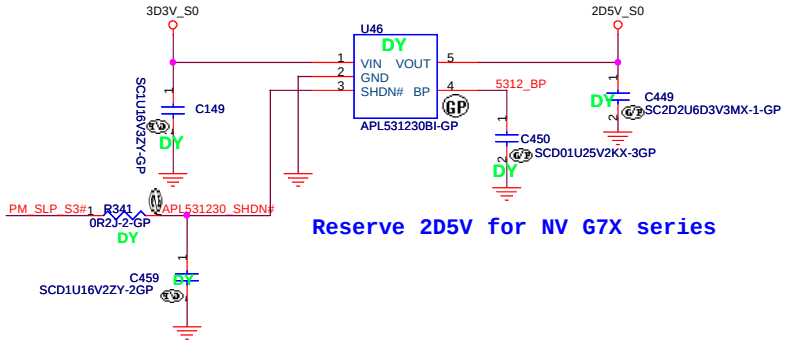
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***APW5912_1D5V***	
Size	Document Number: **Columbia/Tangiz**	Rev: -1M
Date: Thursday, June 07, 2007	Sheet 40 of 45	

0D9V_S3
Iomax=1.2A

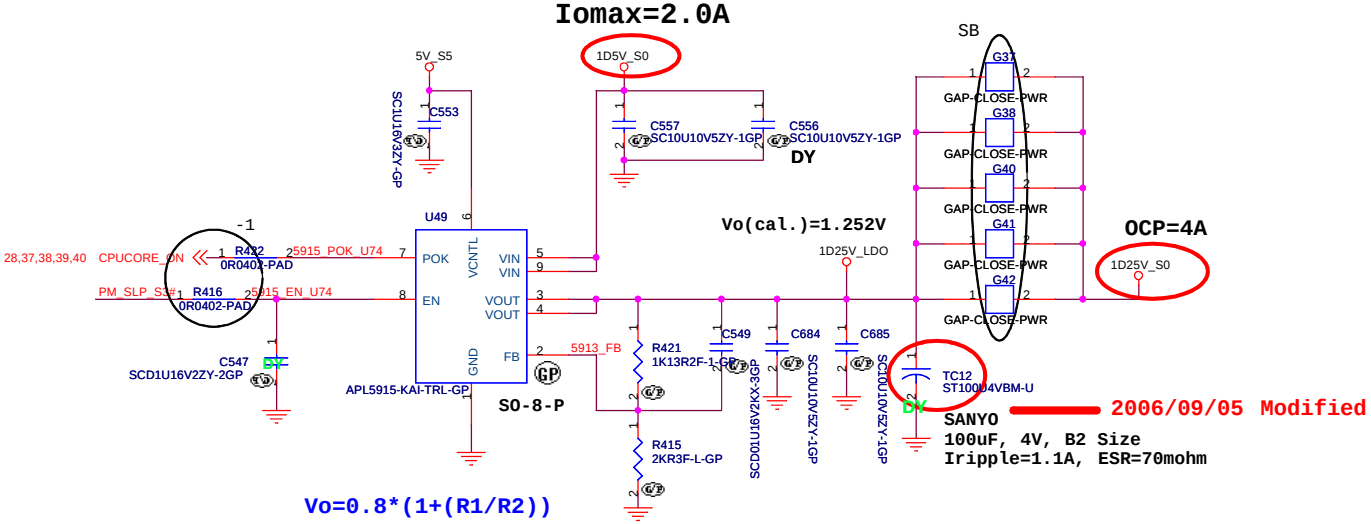


2D5V
Iomax=130mA



Reserve 2D5V for NV G7X series

1D25V_S0
Iomax=2.0A



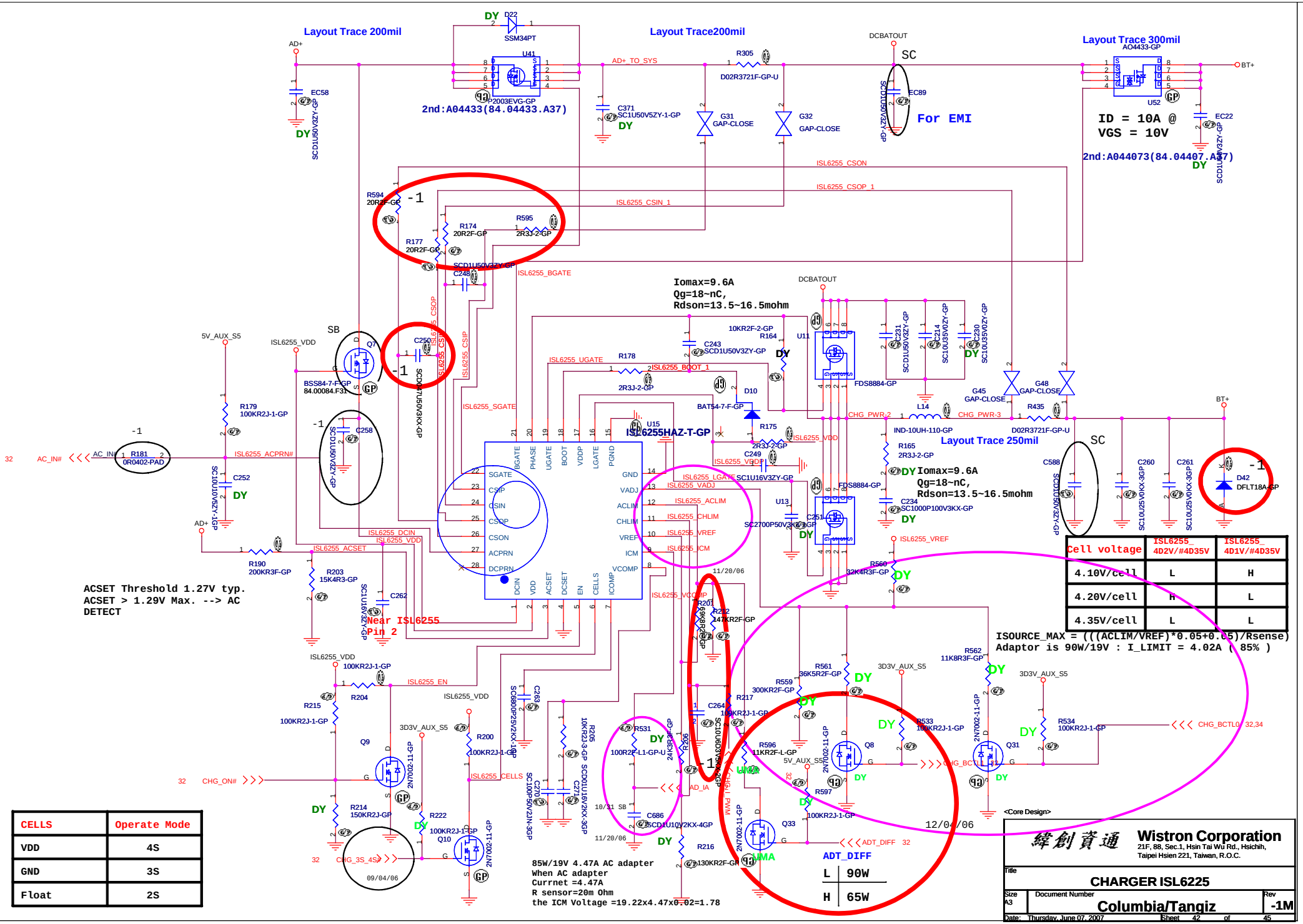
Vo=0.8*(1+(R1/R2))

2006/09/05 Modified

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

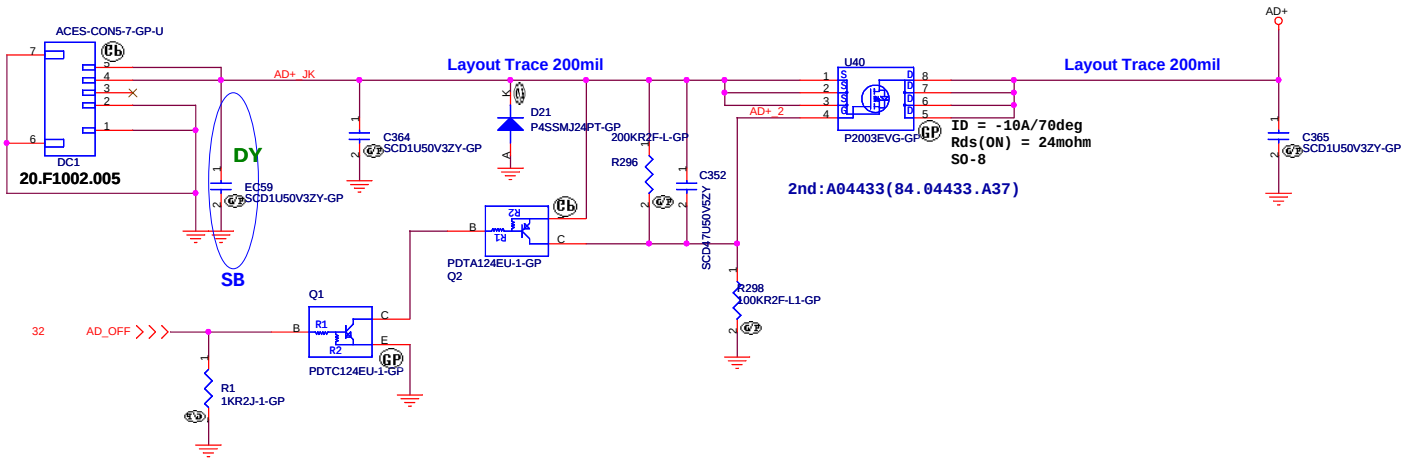
Title	***1D25V/2D5V//1D05V/0D9V***	
Size: B	Document Number: **Columbia/Tangiz**	Rev: **-1M**
Date: Thursday, June 07, 2007	Sheet 41 of 45	



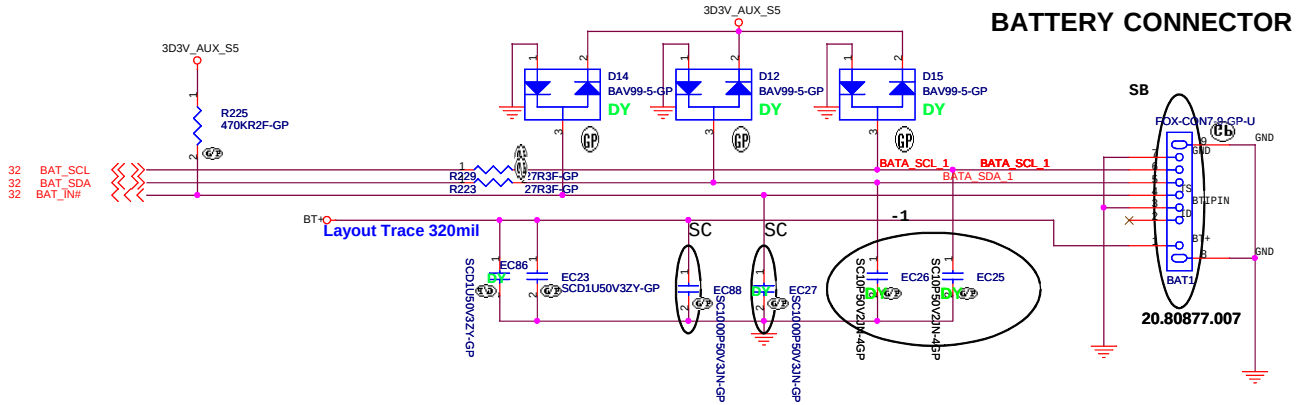
Cell voltage	ISL6255_ 4D2V/#4D35V	ISL6255_ 4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT

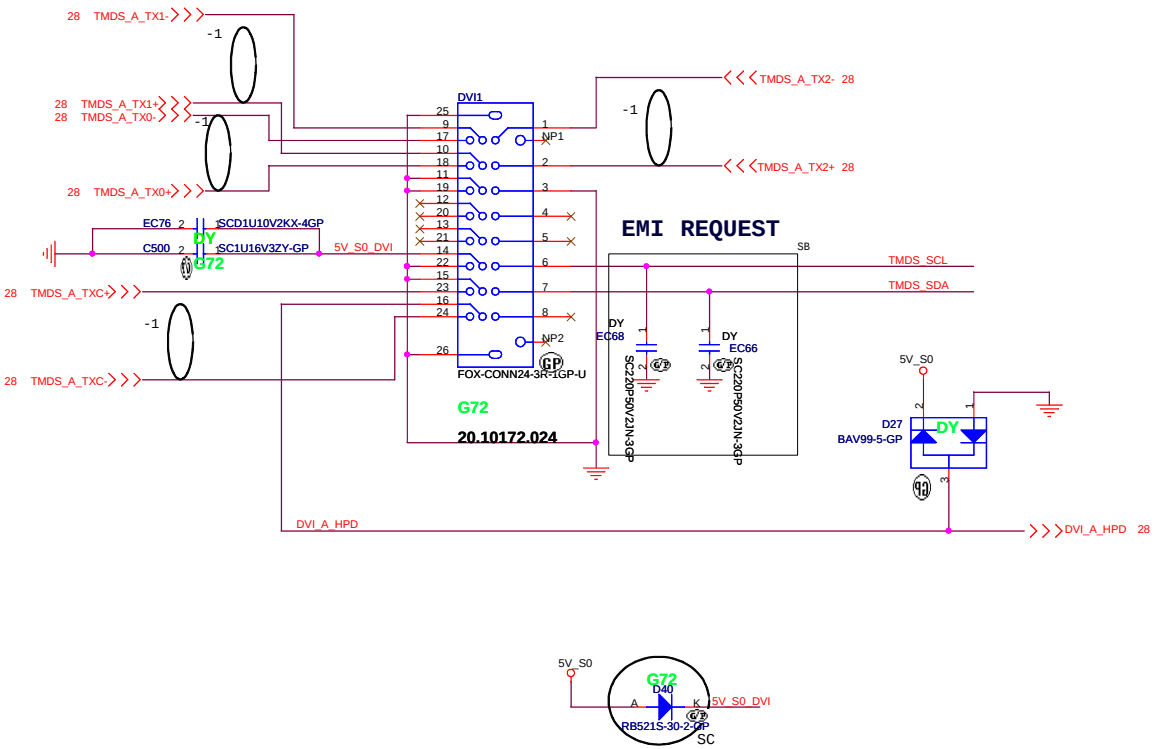


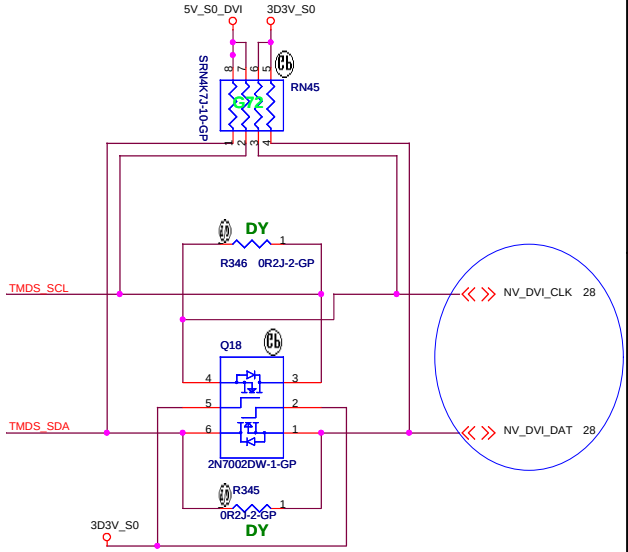
BATTERY CONNECTOR



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size A3	Document Number **Columbia/Tangiz**	Rev **-1M**
Date: Thursday, June 07, 2007	Sheet 43 of 45	





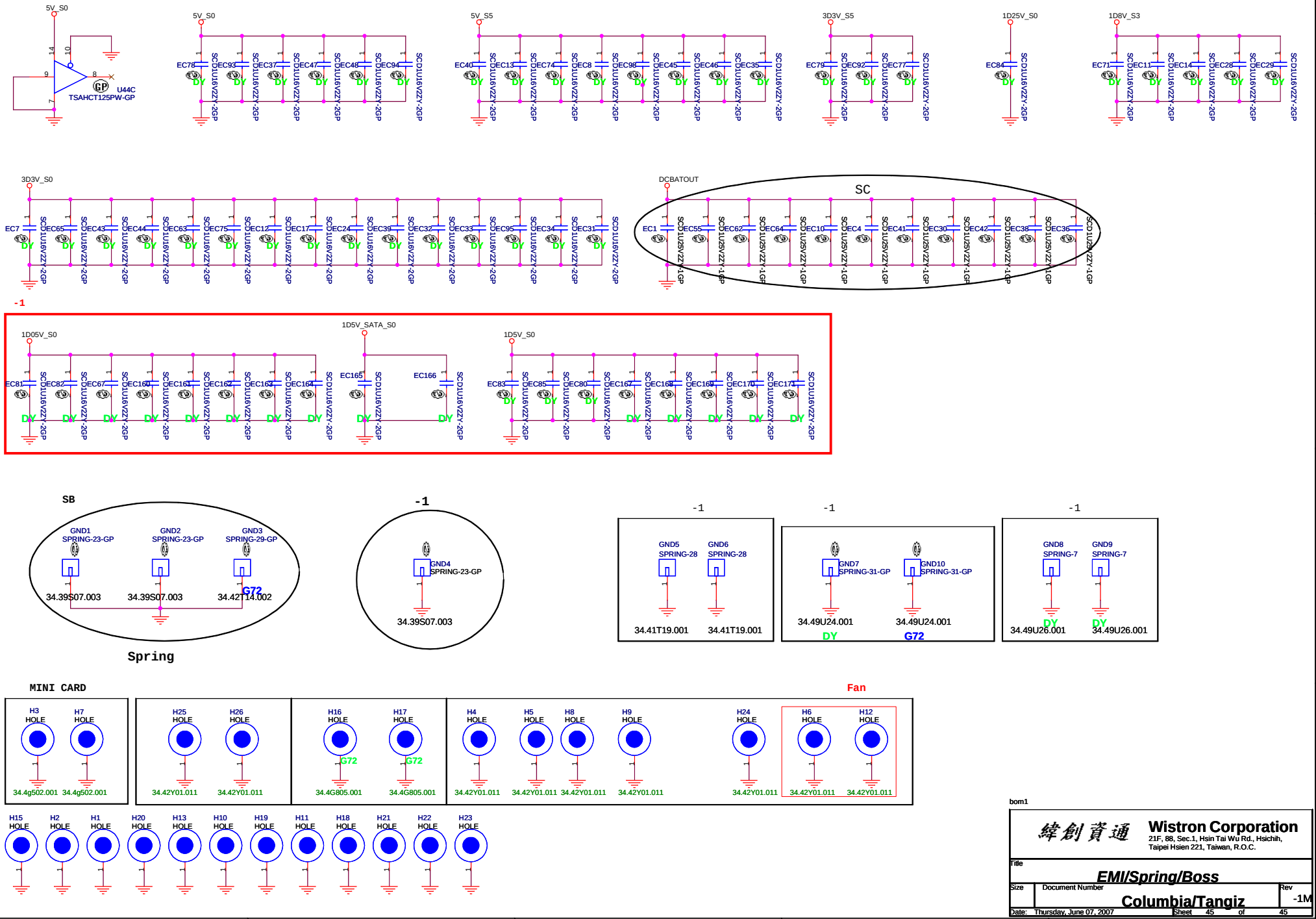
<variant_name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DVI CONNECTOR**

Size	Document Number	Rev
A3	Columbia/Tangiz	-1M

Date: Thursday, June 07, 2007 Sheet 44 of 45



bom1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **Columbia/Tangiz** | Rev: -1M

Date: Thursday, June 07, 2007 | Sheet 45 of 45