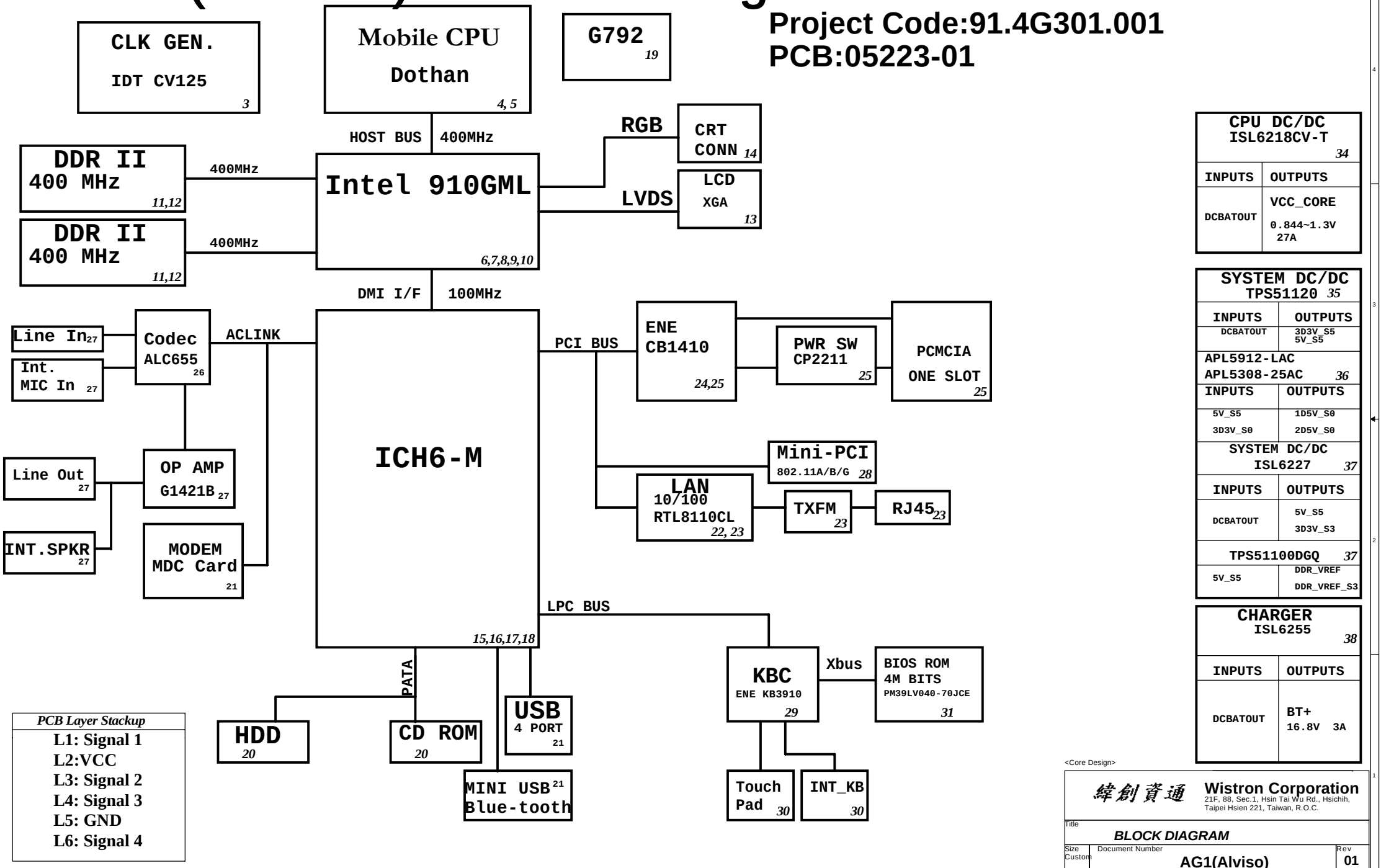
AG1(Alviso) Block Diagram 2005/11/01

Project Code:91.4G301.001
PCB:05223-01



CPU DC/DC
ISL6218CV-T *34*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC
TPS51120 *35*

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5912-LAC
APL5308-25AC *36*

INPUTS	OUTPUTS
5V_S5 3D3V_S0	1D5V_S0 2D5V_S0

SYSTEM DC/DC
ISL6227 *37*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DGQ *37*

INPUTS	OUTPUTS
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER
ISL6255 *38*

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 4
L5: GND
L6: Signal 4

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLOCK DIAGRAM***

Size: Custom | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Tuesday, November 01, 2005 | Sheet 1 of 40

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT,ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

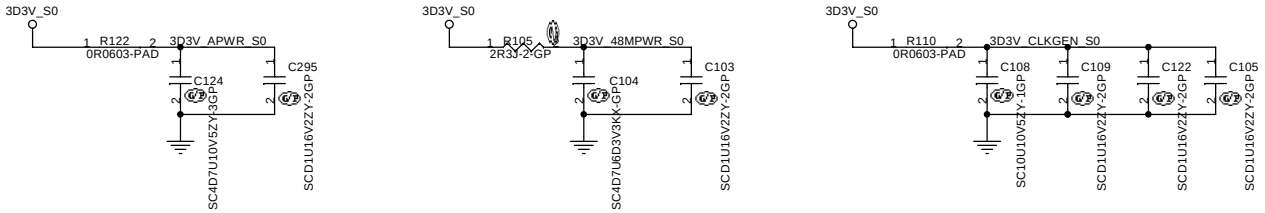
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

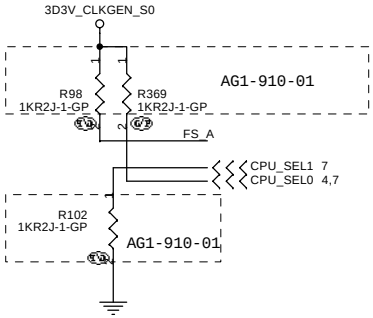
Title: *Memo*

Size: A3 | Document Number: AG1(Alviso) | Rev: 01

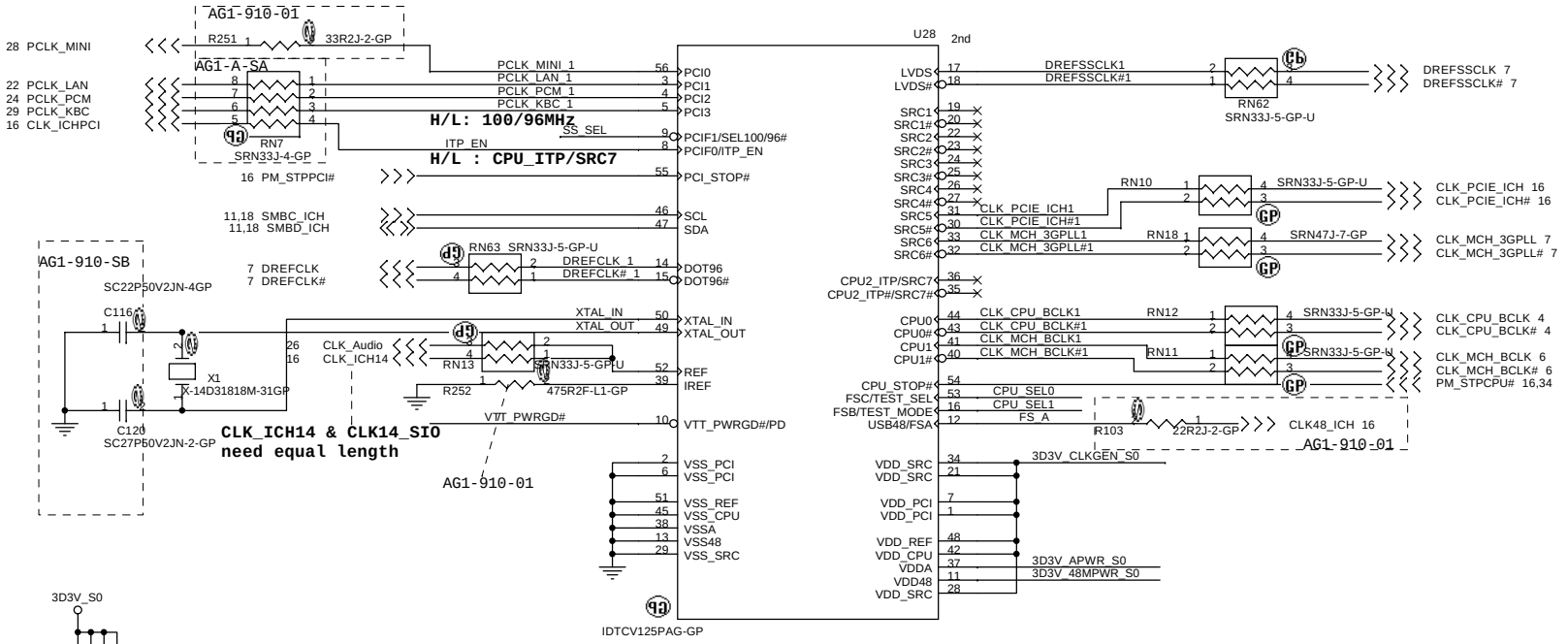
Date: Tuesday, November 01, 2005 | Sheet 2 of 40

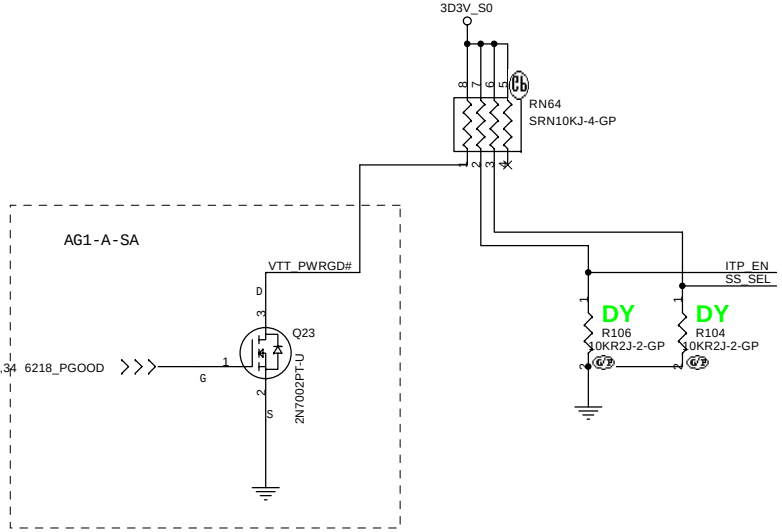


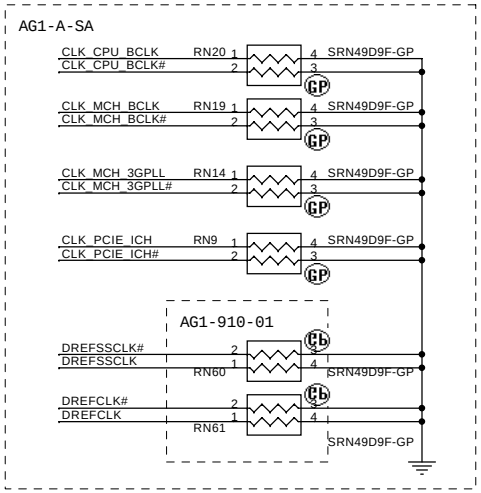
IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

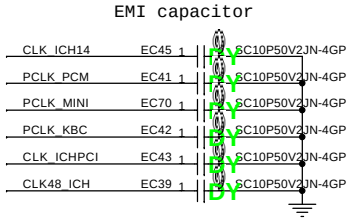


FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved









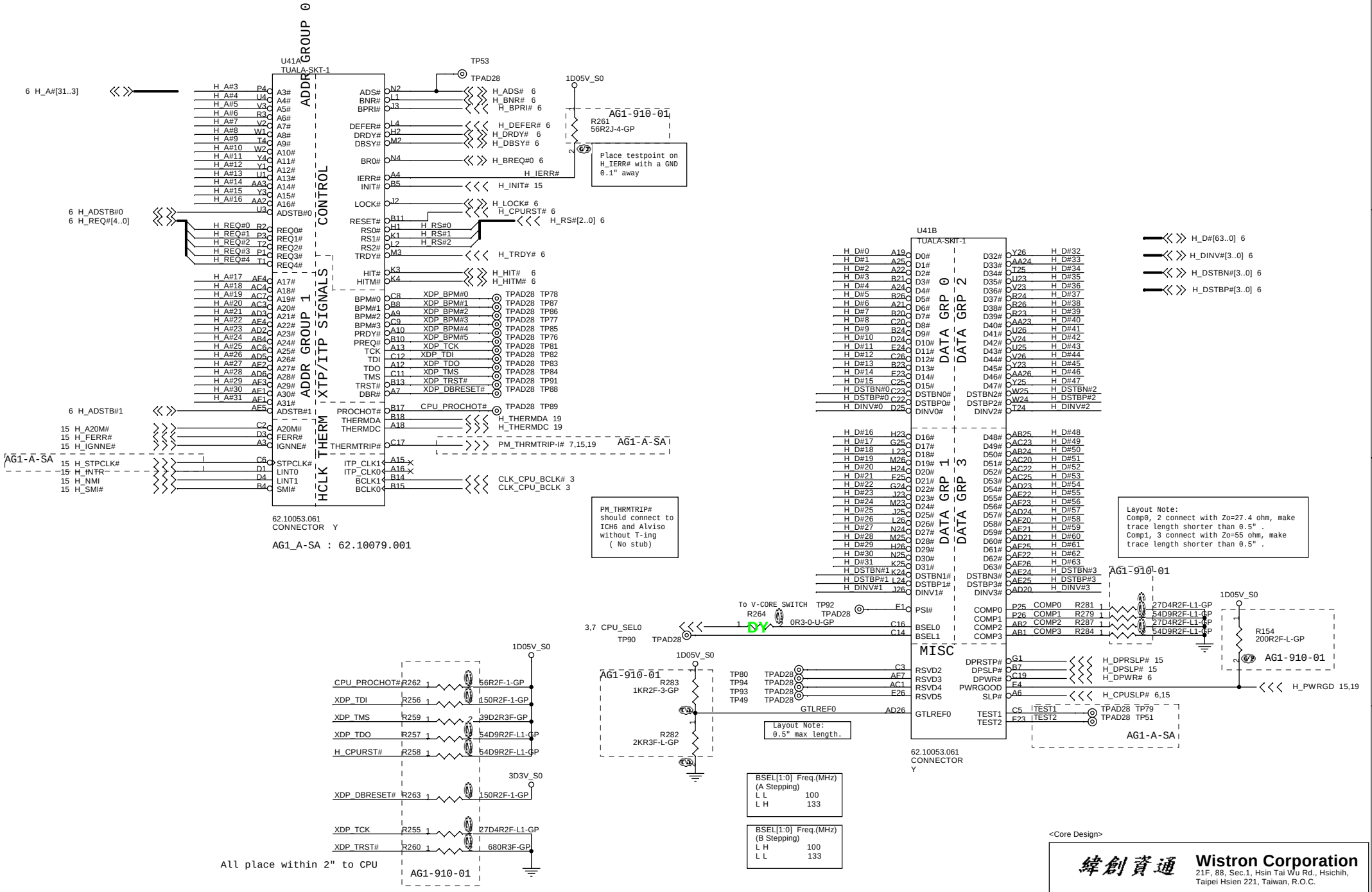
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock Generator - IDT125***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Friday, October 28, 2005 Sheet 3 of 40



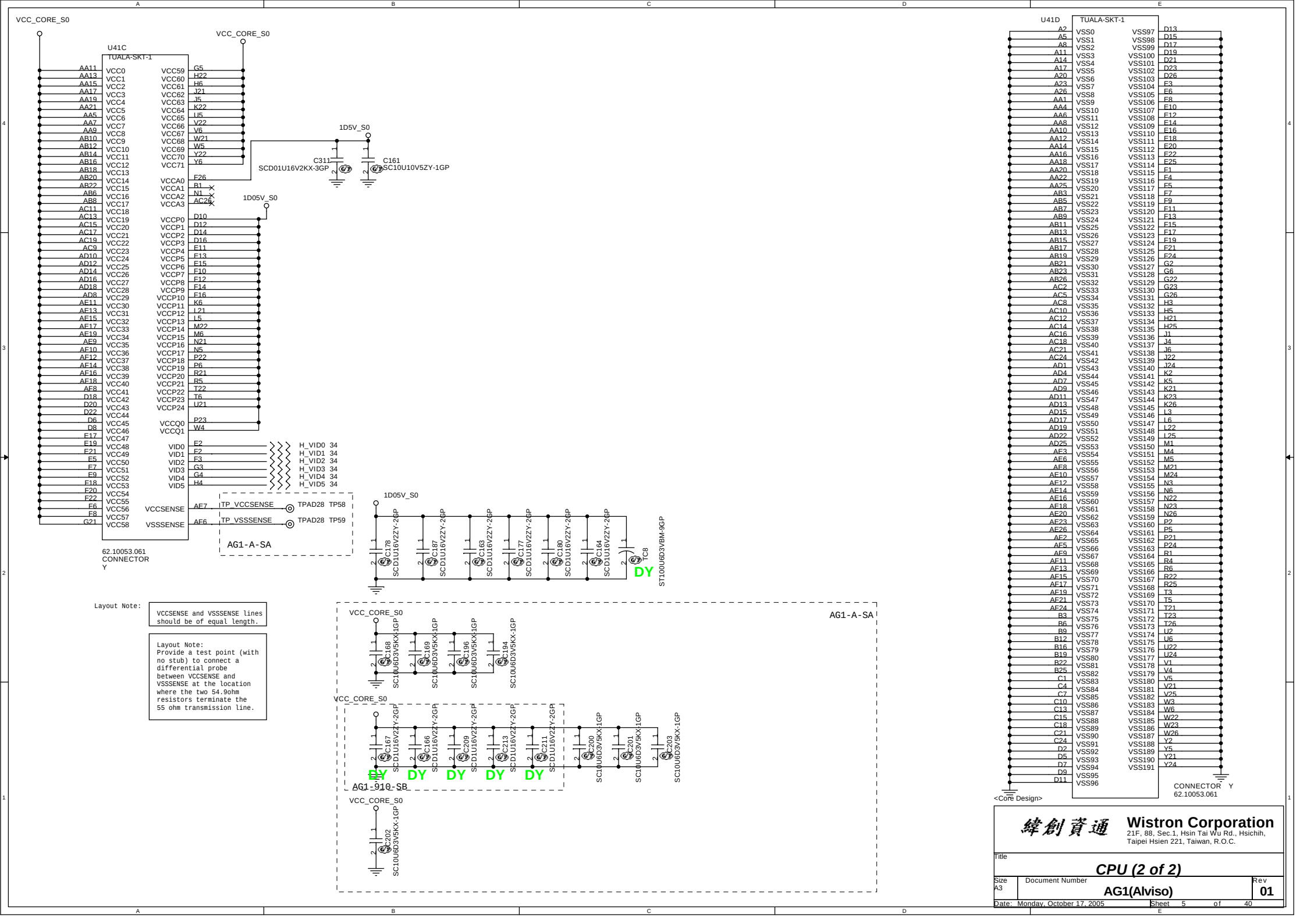
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

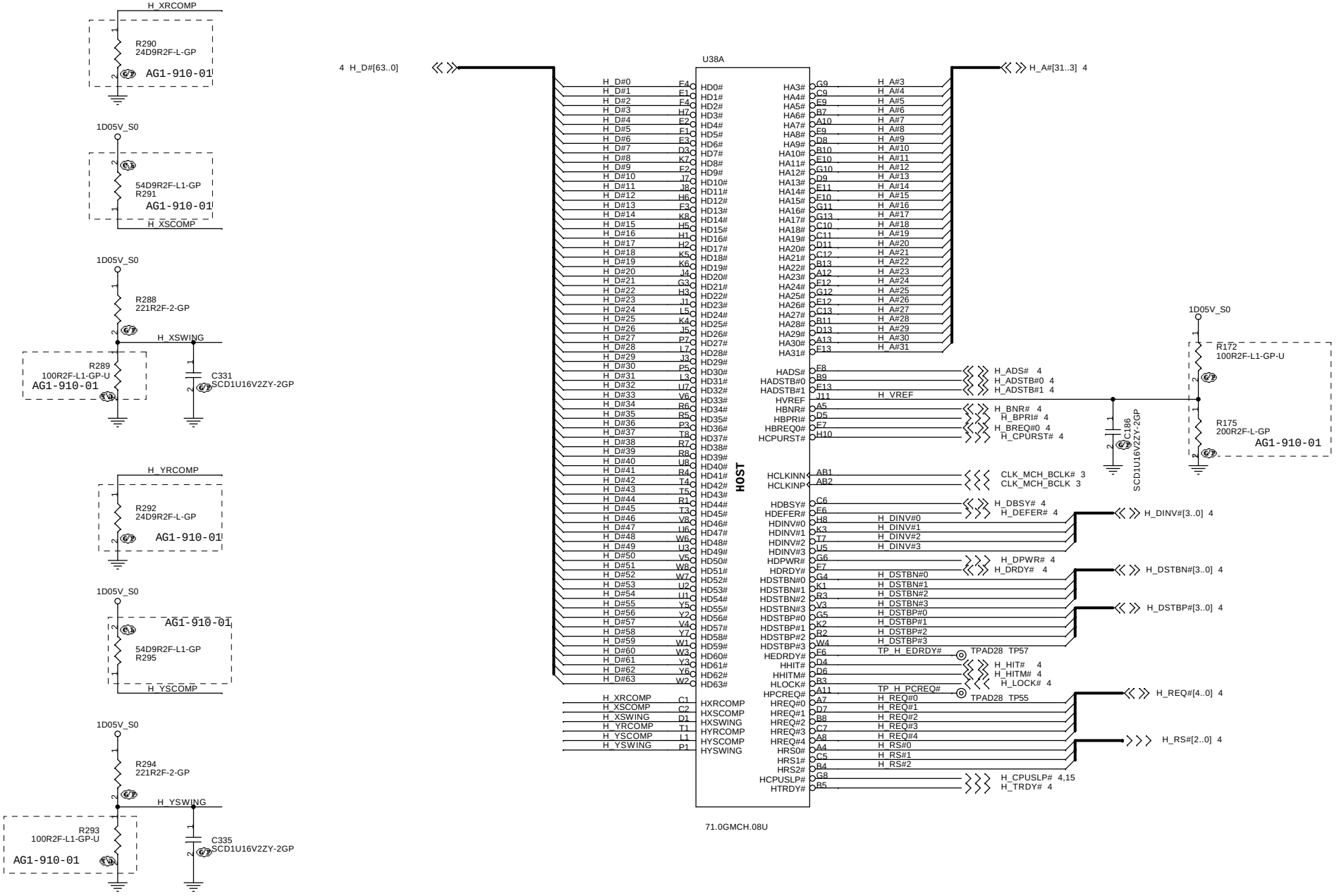
Title: **CPU (1 of 2)**

Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Monday, October 31, 2005 | Sheet 4 of 40



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***CPU (2 of 2)***		
Size A3	Document Number **AG1(Alviso)**		Rev **01**
Date: Monday, October 17, 2005	Sheet 5 of 40		



Place them near to the chip

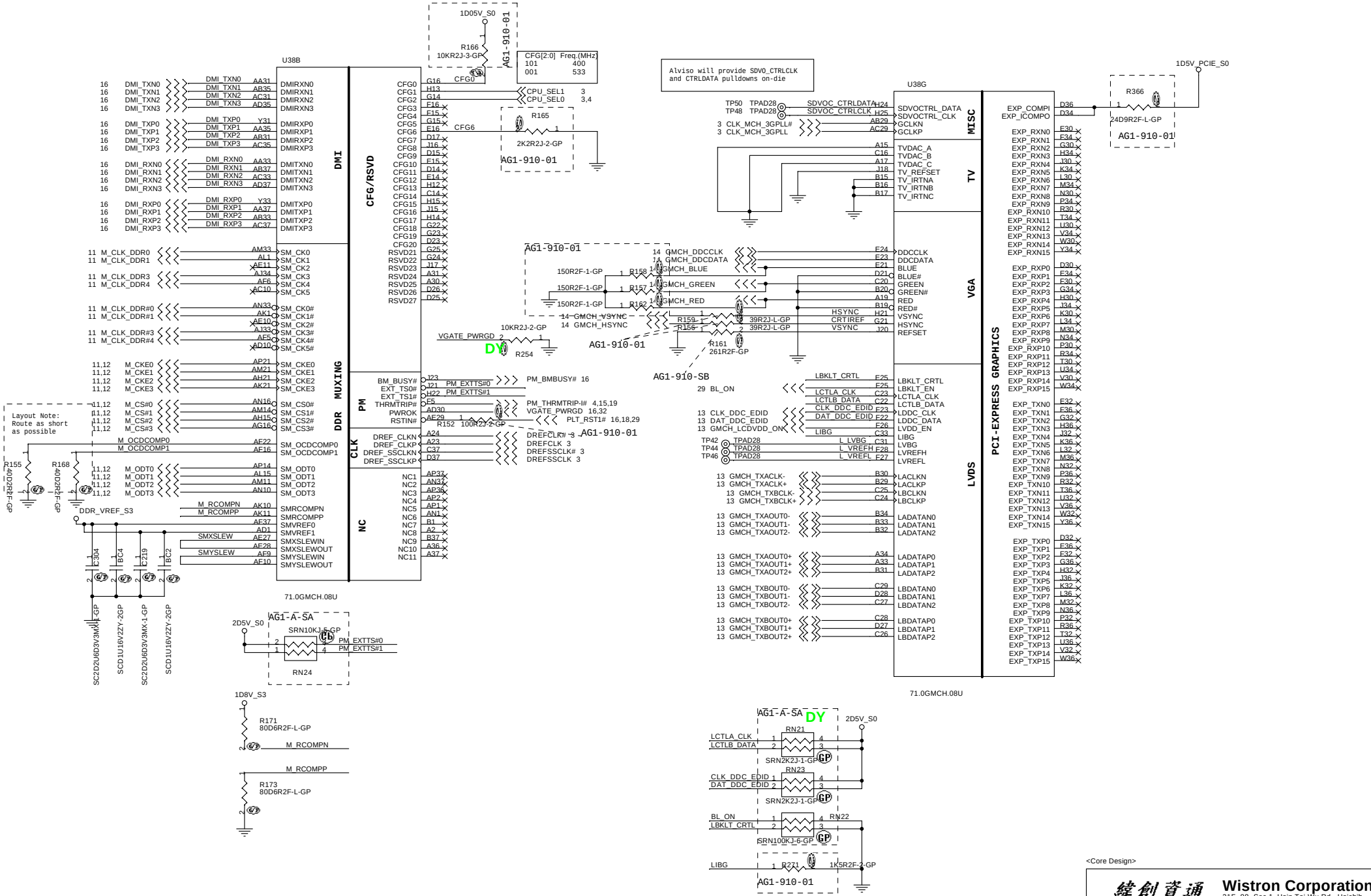
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

Date: Tuesday, October 25, 2005 Sheet 6 of 40



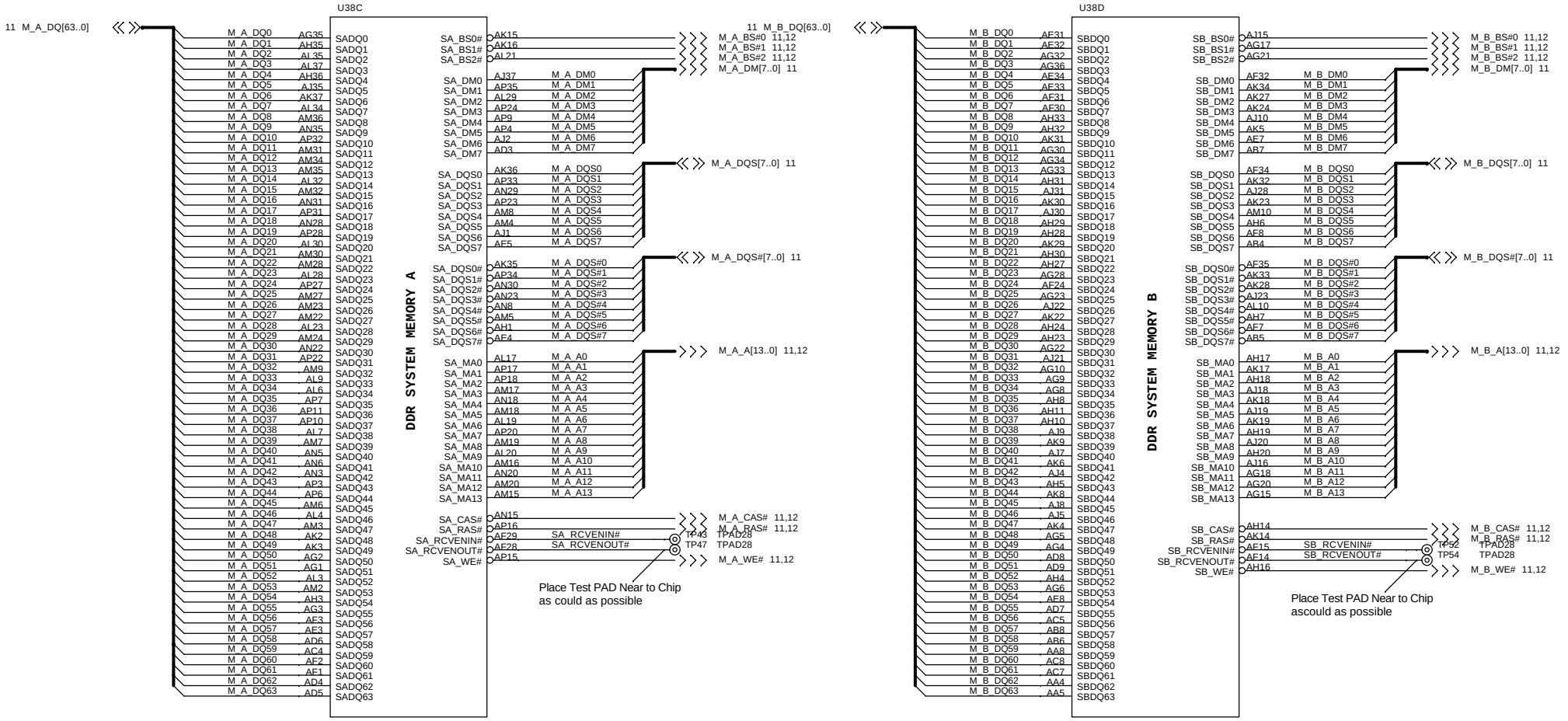
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (2 of 5)

Size: Custom | Document Number: AG1(Alviso) | Rev: 01

Date: Tuesday, October 25, 2005 | Sheet 7 of 40



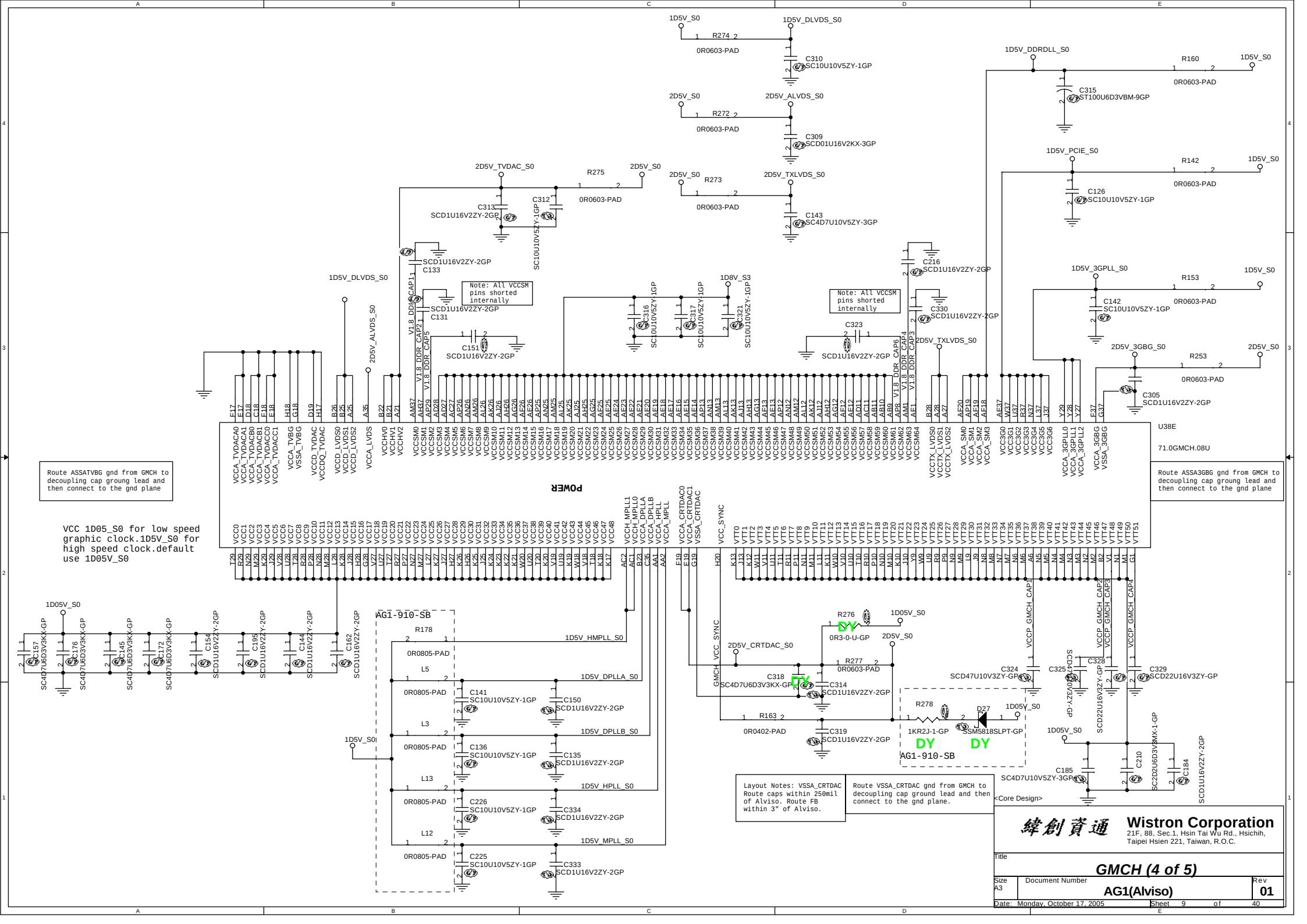
<Core Design>

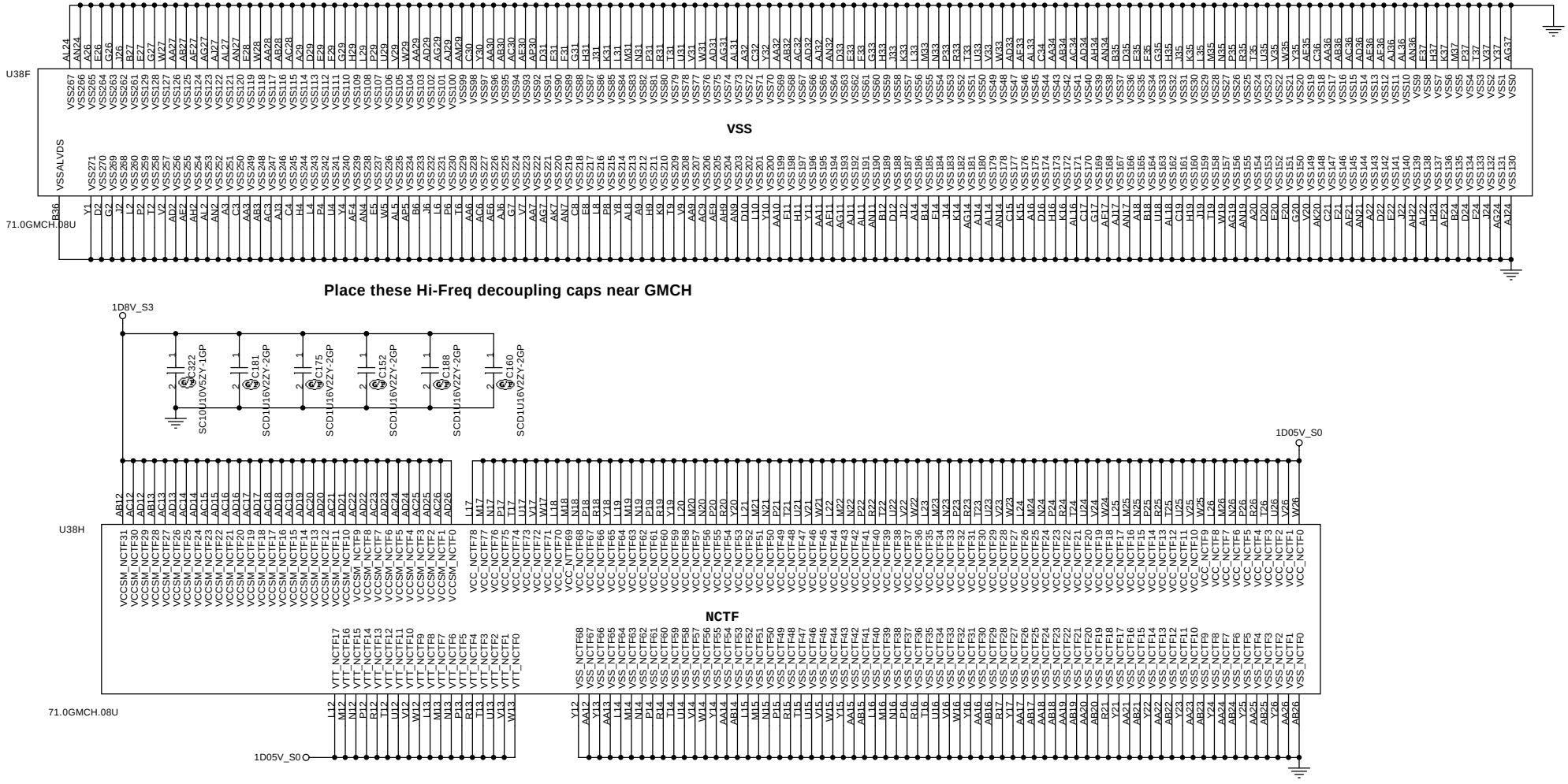
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (3 of 5)***

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

Date: Monday, October 17, 2005 Sheet 8 of 40


1D5V_S0
1D5V_DLVDS_S0
R274
0R0603-PAD
C310
SC10U10V5ZY-1GP
1D5V_DDRDLL_S0
R160
C315
ST100U6D3VBM-9GP
2D5V_S0
2D5V_ALVDS_S0
R272
C309
SCD01U16V2KX-3GP
1D5V_PCIE_S0
R142
C126
2D5V_TVDAC_S0
R275
C313
SCD1U16V2ZY-2GP
C312
SC10U10V5ZY-1GP
2D5V_TXLVDS_S0
R273
C143
SC4D7U10V5ZY-3GP
1D5V_3GPLL_S0
R153
C142
C133
C131
C151
1D8V_S3
C316
C317
C321
C323
C216
C330
2D5V_3GBG_S0
R253
C305
SCD1U16V2ZY-2GP
Note: All VCCSM pins shorted internally
V1.8 DDR CAP1
V1.8 DDR CAP2
V1.8 DDR CAP5
V1.8 DDR CAP4
V1.8 DDR CAP3
V1.8 DDR CAP6
U38E
71.0GMCH.08U
POWER
Route ASSATVBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
Route ASSA3GBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0
AG1-910-SB
R178
0R0805-PAD
1D5V_HMPLL_S0
L5
1D5V_DPLLA_S0
L3
1D5V_DPLLB_S0
L13
1D5V_HPLL_S0
L12
1D5V_MPLL_S0
C141
C150
C136
C135
C226
C334
C225
C333
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
R276
0R3-0-U-GP
DY
R277
0R0603-PAD
C318
SC4D7U6D3V3KX-GP
C314
R163
0R0402-PAD
C319
R278
1KR2J-1-GP
D27
SSM5818SLPT-GP
C324
SCD47U10V3ZY-GP
C325
C328
C329
SCD22U16V3ZY-GP
SCD22U6D3V3KX-GP
SC4D7U10V5ZY-3GP
C185
C210
C184
SC2D2U6D3V3MX-1-GP
SCD1U16V2ZY-2GP
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size A3
Document Number
AG1(Alviso)
Rev 01
Date: Monday, October 17, 2005
Sheet 9 of 40



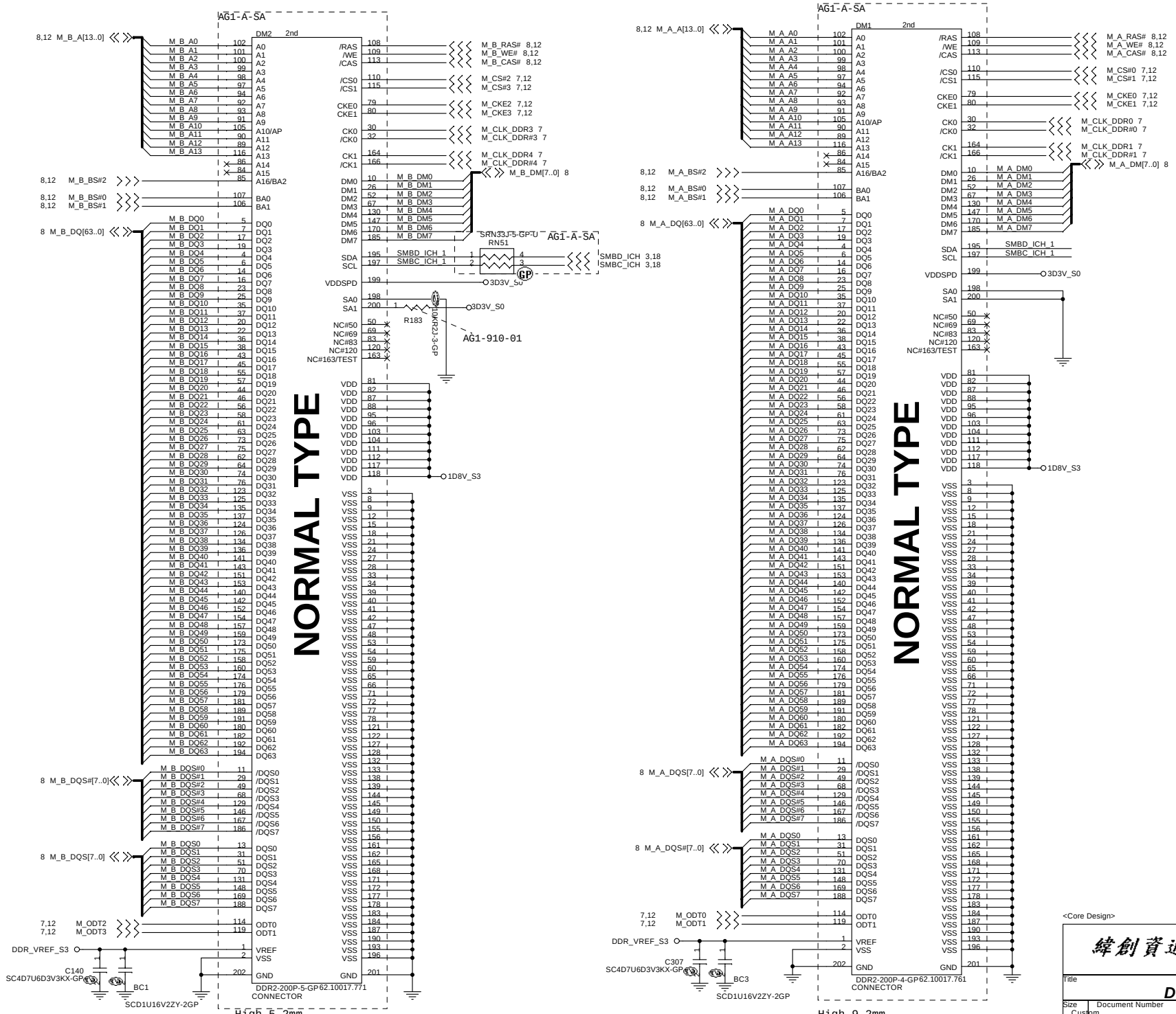
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMCH (5 of 5)***

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

Date: Monday, October 17, 2005 Sheet 10 of 40



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

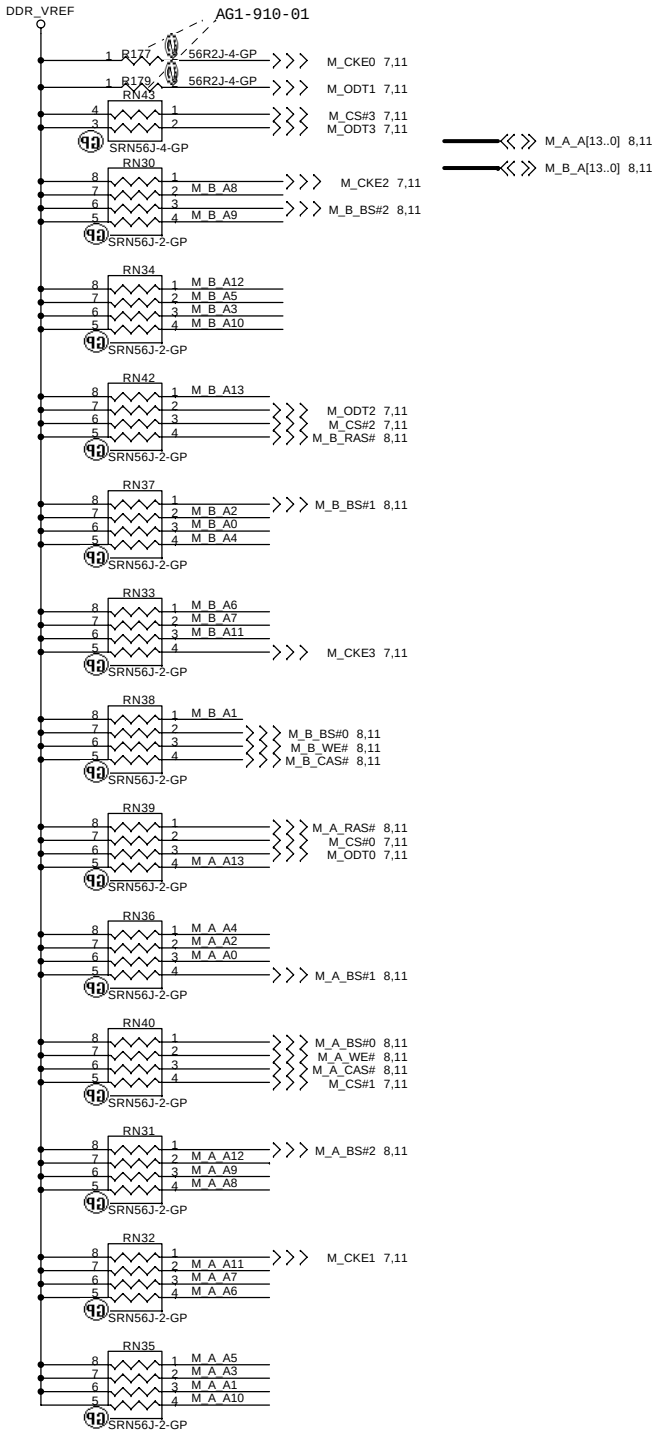
Title: ***DDR Socket***

Size	Document Number	Rev
Custom	**AG1(Alviso)**	**01**

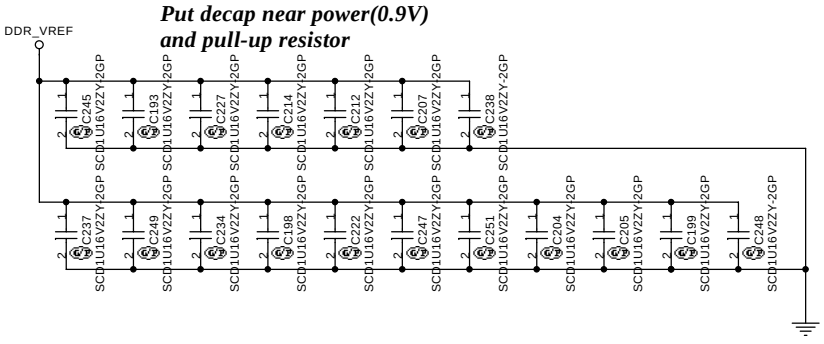
Date: Tuesday, October 25, 2005 Sheet 11 of 40

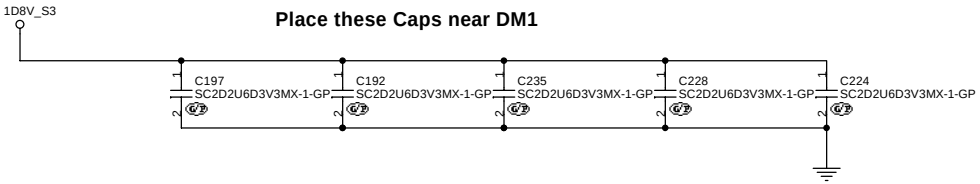
PARALLEL TERMINATION

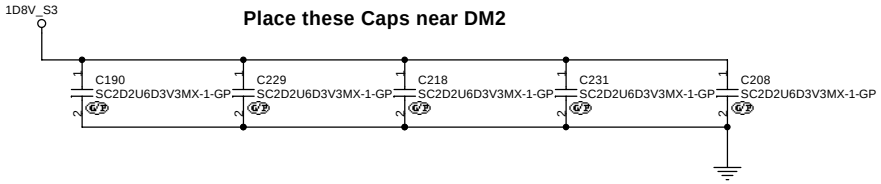
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor



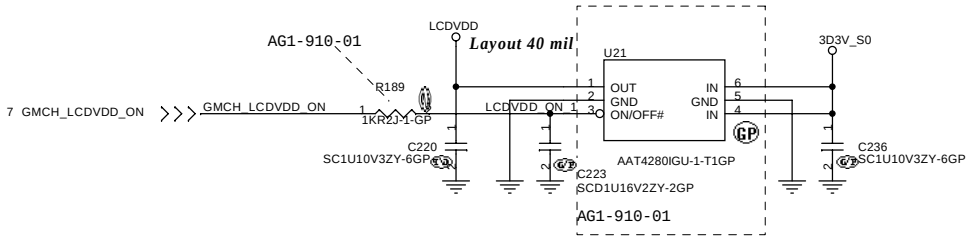


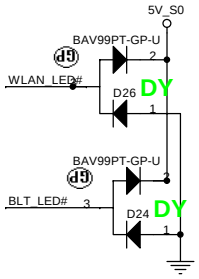


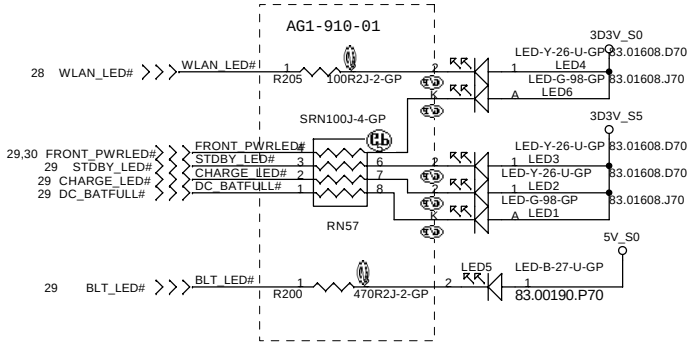
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR2 Termination Resistor***	
Size: A3	Document Number: **AG1(Alviso)**	Rev: **01**
Date: Tuesday, October 25, 2005	Sheet 12 of 40	

LED







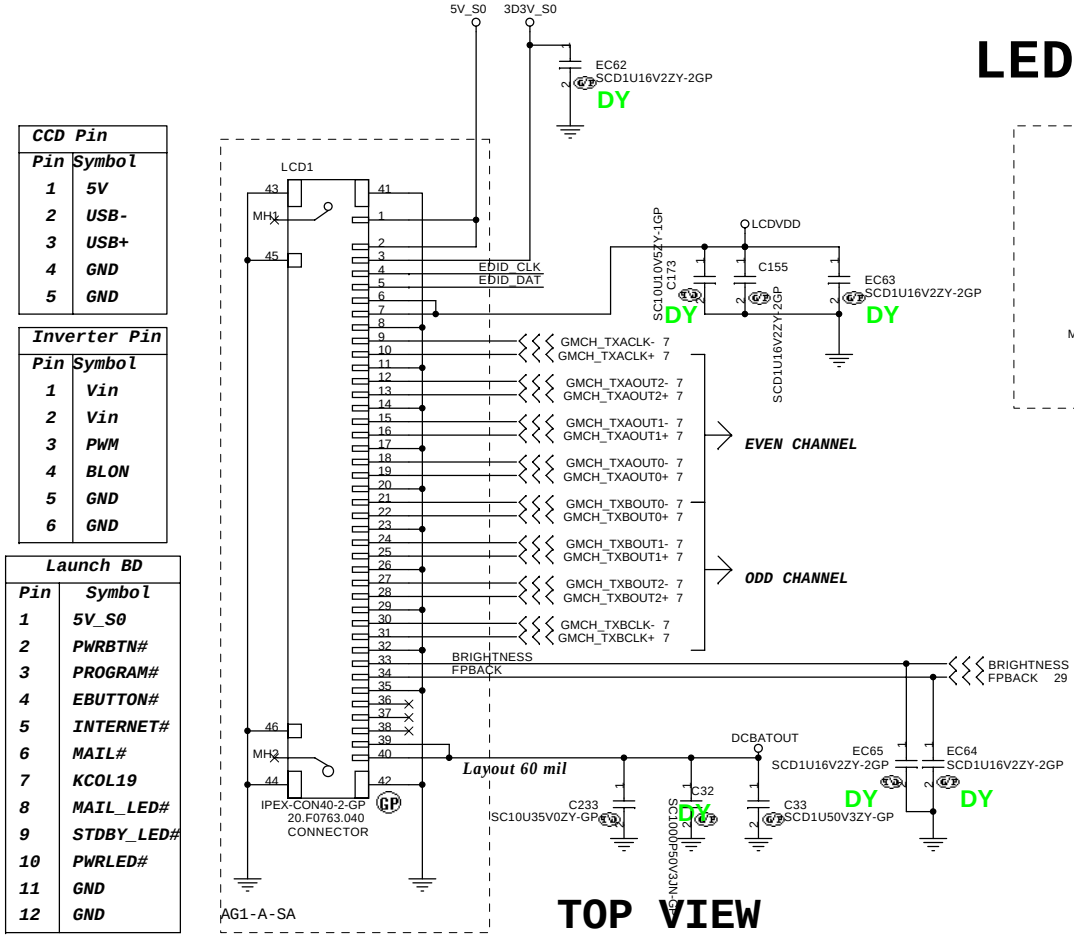
LCD/INVERTER/CCD CONN

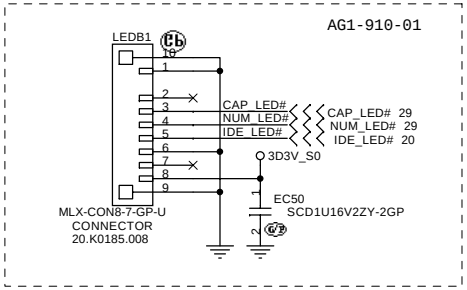
LED BD CONN

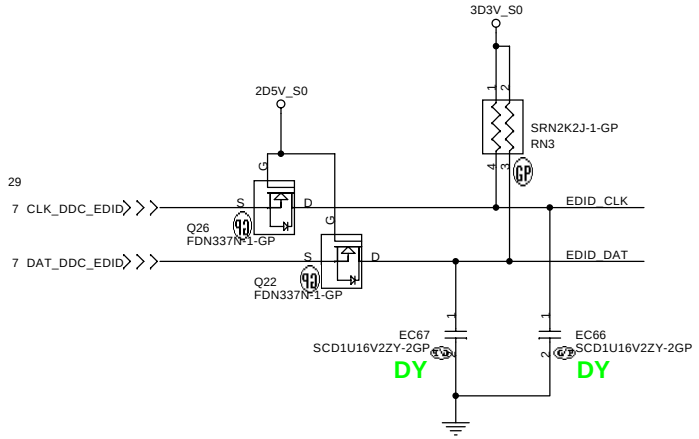
CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	5V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	KCOL19
8	MAIL_LED#
9	STDBY_LED#
10	PWRLED#
11	GND
12	GND







TOP VIEW

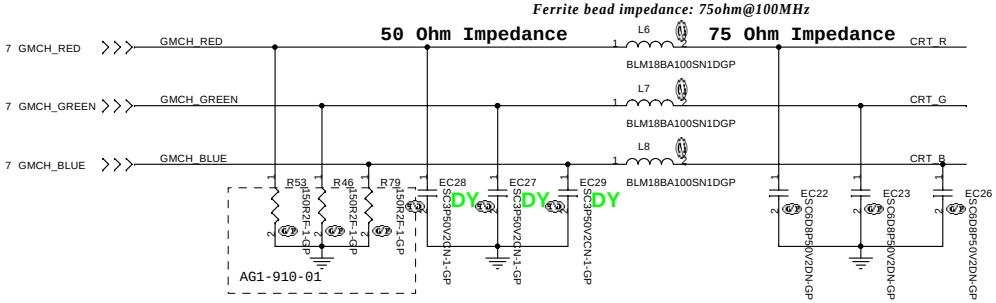
LCD

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

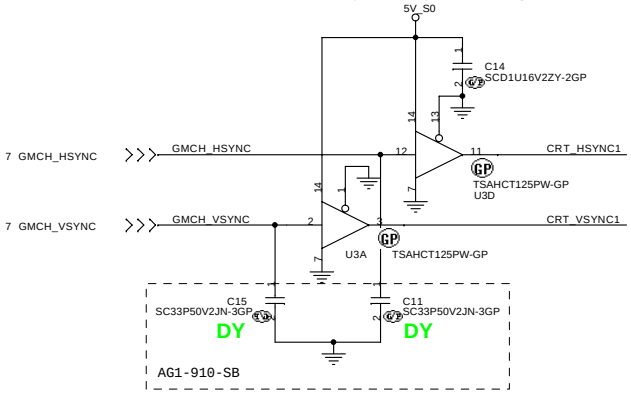
Title: LCD CONN & LED
Size: A3
Document Number: AG1(Alviso)
Rev: 01
Date: Friday, October 28, 2005
Sheet 13 of 40

CRT CONNECTOR

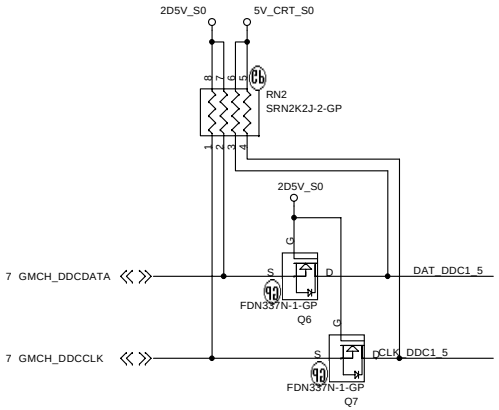
Ferrite bead impedance: 75ohm@100MHz

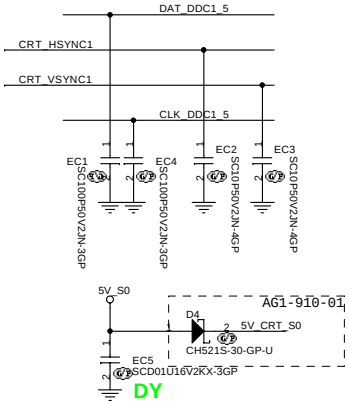


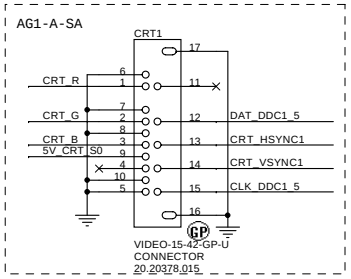
Hsync & Vsync level shift



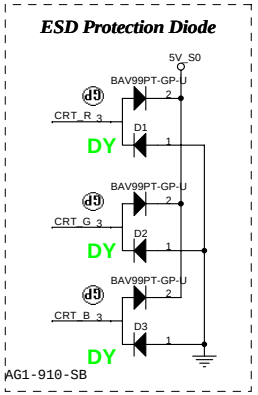
DDC_CLK & DATA level shift







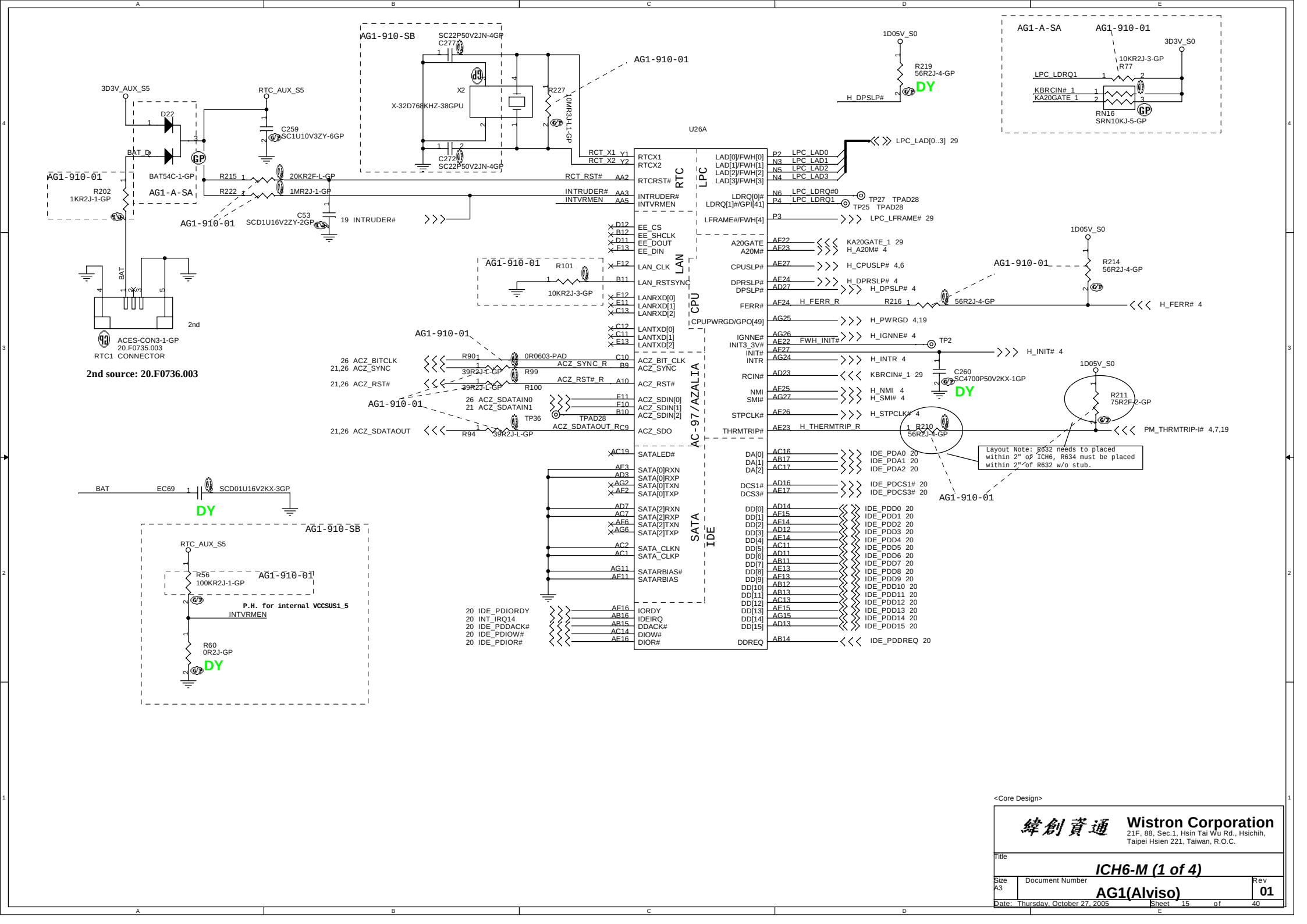
ESD Protection Diode



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: Custom
Document Number: AG1(Alviso)
Rev: 01
Date: Friday, October 28, 2005
Sheet 14 of 40



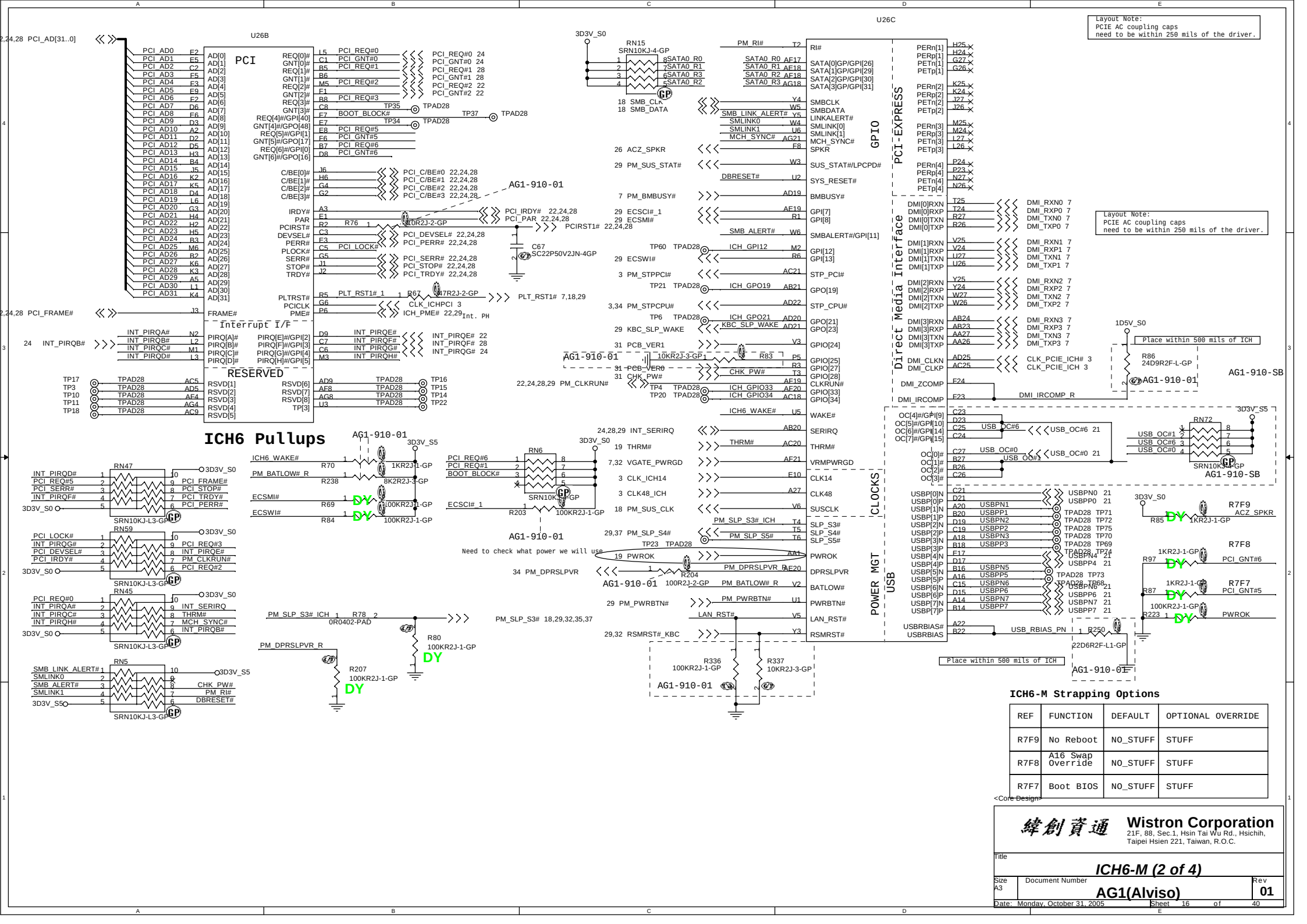
<Core Design>

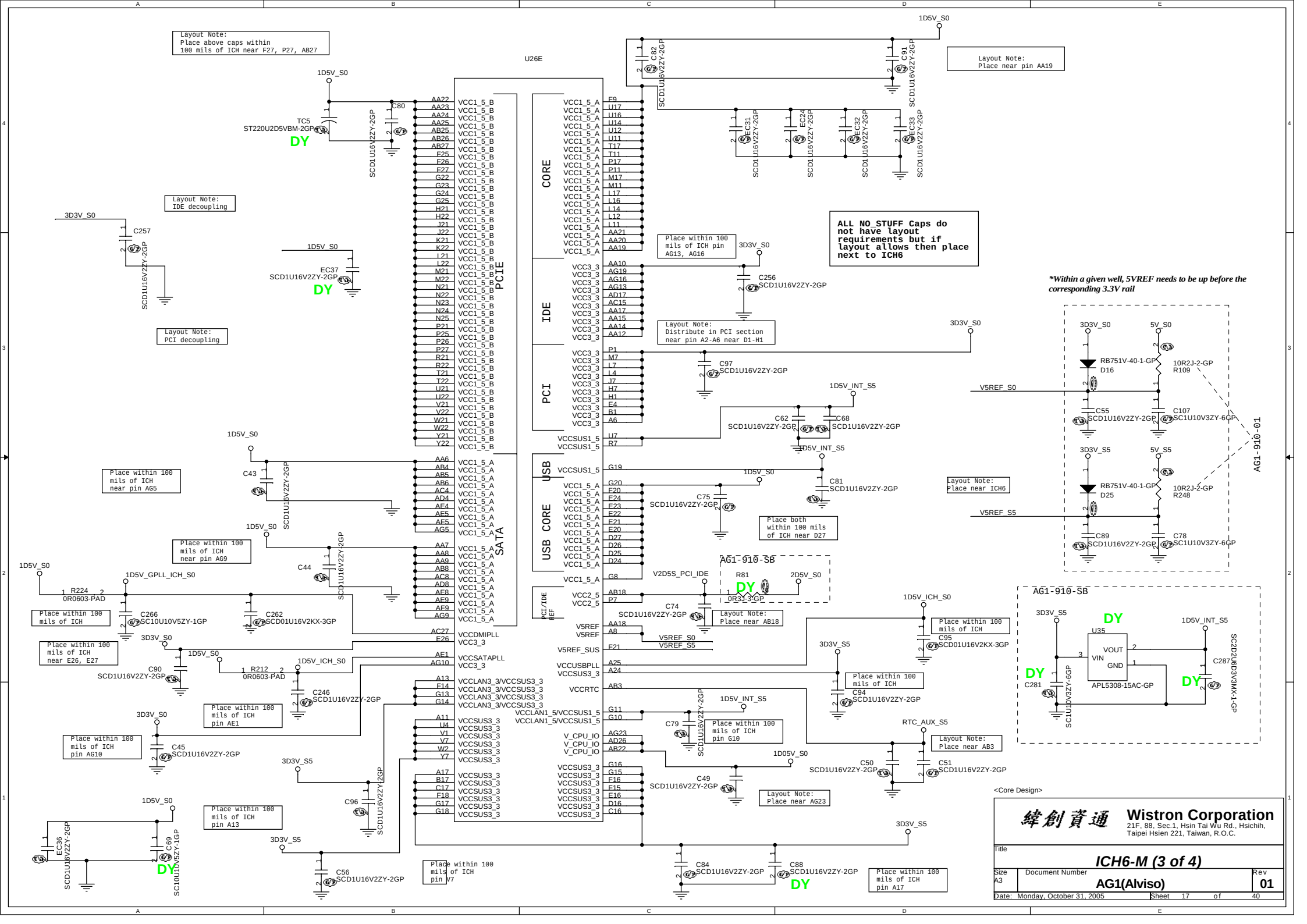
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

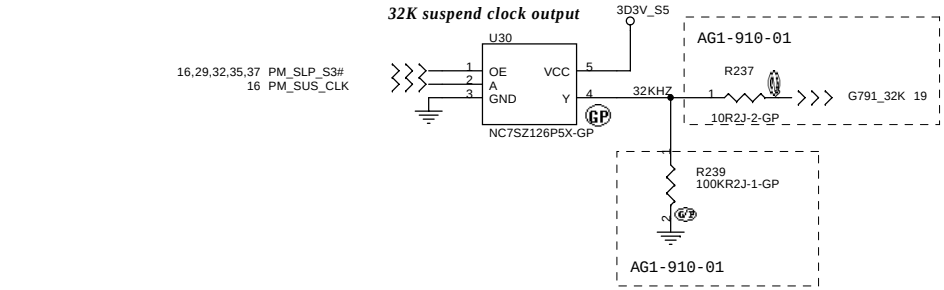
Title: **ICH6-M (1 of 4)**

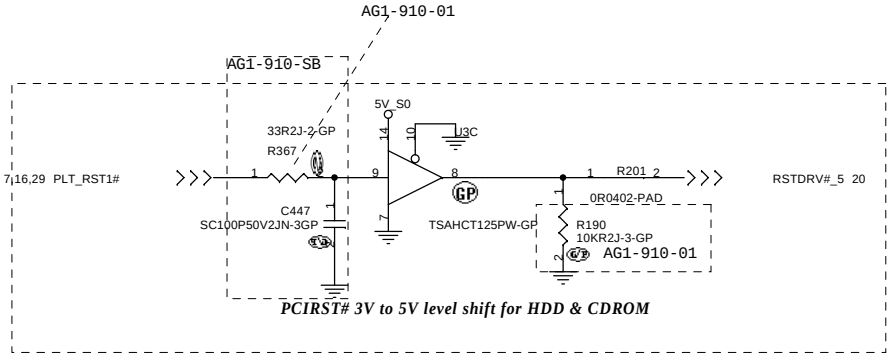
Size	Document Number	Rev
A3	AG1(Alviso)	01

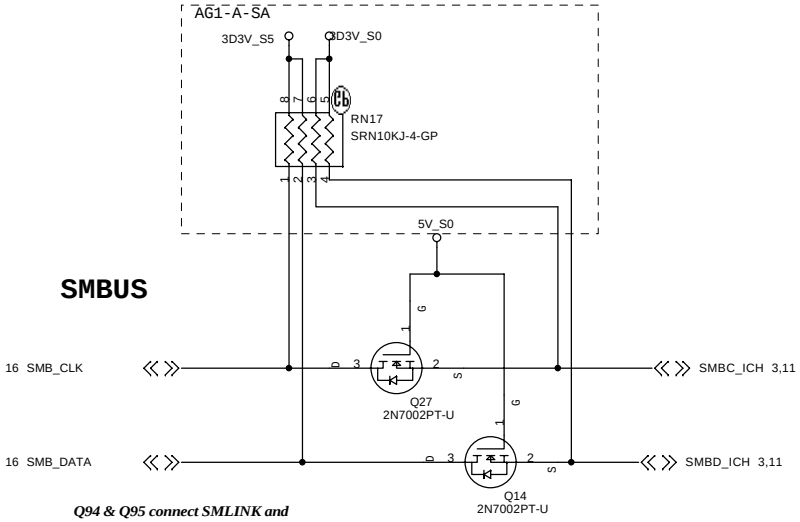
Date: Thursday, October 27, 2005 Sheet 15 of 40

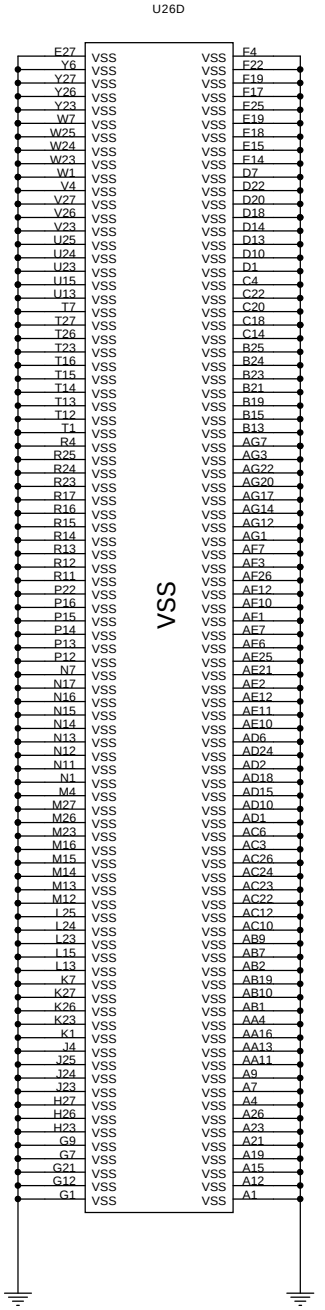

U26B
PCI
Interrupt I/F
RESERVED
U26C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
USB
POWER MGT
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
ICH6 Pullups
AG1-910-01
AG1-910-SB
Need to check what power we will use
Place within 500 mils of ICH
ICH6-M Strapping Options
REF
FUNCTION
DEFAULT
OPTIONAL OVERRIDE
R7F9
No Reboot
NO_STUFF
STUFF
R7F8
A16 Swap Override
NO_STUFF
STUFF
R7F7
Boot BIOS
NO_STUFF
STUFF
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (2 of 4)
Size
A3
Document Number
AG1(Alviso)
Rev
01
Date: Monday, October 31, 2005
Sheet 16 of 40


Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27
U26E
1D5V_S0
C80
SCD1U16V2ZY-2GP
TC5
ST220U2D5VBM-2GP
DY
Layout Note:
IDE decoupling
3D3V_S0
C257
SCD1U16V2ZY-2GP
EC37
Layout Note:
PCI decoupling
Place within 100
mils of ICH
near pin AG5
C43
Place within 100
mils of ICH
near pin AG9
C44
1D5V_GPLL_ICH_S0
R224
0R0603-PAD
C266
SC10U10V5ZY-1GP
C262
SCD01U16V2KX-3GP
Place within 100
mils of ICH
Place within 100
mils of ICH
near E26, E27
C90
SCD1U16V2ZY-2GP
R212
0R0603-PAD
1D5V_ICH_S0
C246
Place within 100
mils of ICH
pin AE1
Place within 100
mils of ICH
pin AG10
C45
Place within 100
mils of ICH
pin A13
C96
C56
SCD1U16V2ZY-2GP
Place within 100
mils of ICH
pin V7
EC36
C69
SC10U10V5ZY-1GP
DY
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
VCC1_5_B
VCC1_5_A
VCC3_3
VCCSUS1_5
VCCSUS3_3
VCCDMIPLL
VCCSATAPLL
VCCCLAN3_3/VCCSUS3_3
VCCCLAN1_5/VCCSUS1_5
V_CPU_IO
VCCRTC
V5REF
V5REF_SUS
VCCUSBPLL
VCC2_5
Layout Note:
Place near pin AA19
ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6
Place within 100
mils of ICH pin
AG13, AG16
C256
SCD1U16V2ZY-2GP
Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1
C97
SCD1U16V2ZY-2GP
1D5V_INT_S5
C62
SCD1U16V2ZY-2GP
C68
SCD1U16V2ZY-2GP
C81
SCD1U16V2ZY-2GP
C75
SCD1U16V2ZY-2GP
Place both
within 100 mils
of ICH near D27
AG1-910-SB
V2D5S_PCI_IDE
R81
0R3J-3-GP
2D5V_S0
C74
SCD1U16V2ZY-2GP
Layout Note:
Place near AB18
V5REF_S0
V5REF_S5
3D3V_S5
C79
Place within 100
mils of ICH
pin G10
1D05V_S0
C49
SCD1U16V2ZY-2GP
Layout Note:
Place near AG23
1D5V_ICH_S0
Place within 100
mils of ICH
C95
SCD01U16V2KX-3GP
C94
SCD1U16V2ZY-2GP
RTC_AUX_S5
Layout Note:
Place near AB3
C50
SCD1U16V2ZY-2GP
C51
SCD1U16V2ZY-2GP
C84
SCD1U16V2ZY-2GP
C88
SCD1U16V2ZY-2GP
Place within 100
mils of ICH
pin A17
*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail
5V_S0
RB751V-40-1-GP
D16
10R2J-2-GP
R109
C55
SCD1U16V2ZY-2GP
C107
SC1U10V3ZY-6GP
5V_S5
D25
R248
C89
SCD1U16V2ZY-2GP
C78
SC1U10V3ZY-6GP
AG1-910-01
Layout Note:
Place near ICH6
AG1-910-SB
U35
VOUT
VIN
GND
APL5308-15AC-GP
C281
SC1U10V3ZY-6GP
C287
SC2D2U6D3V3MX-1-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size
A3
Document Number
AG1(Alviso)
Rev
01
Date: Monday, October 31, 2005
Sheet 17 of 40









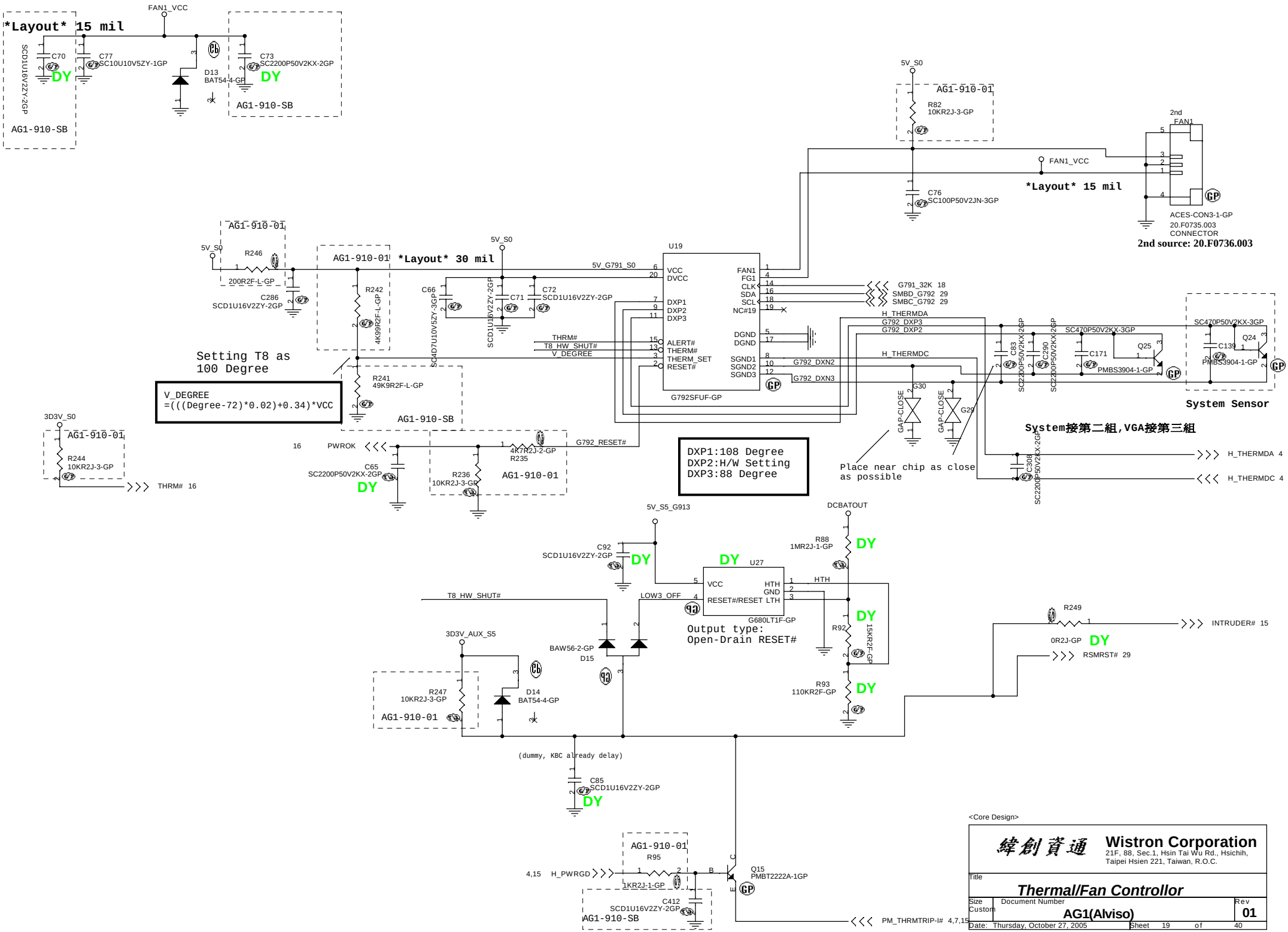
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

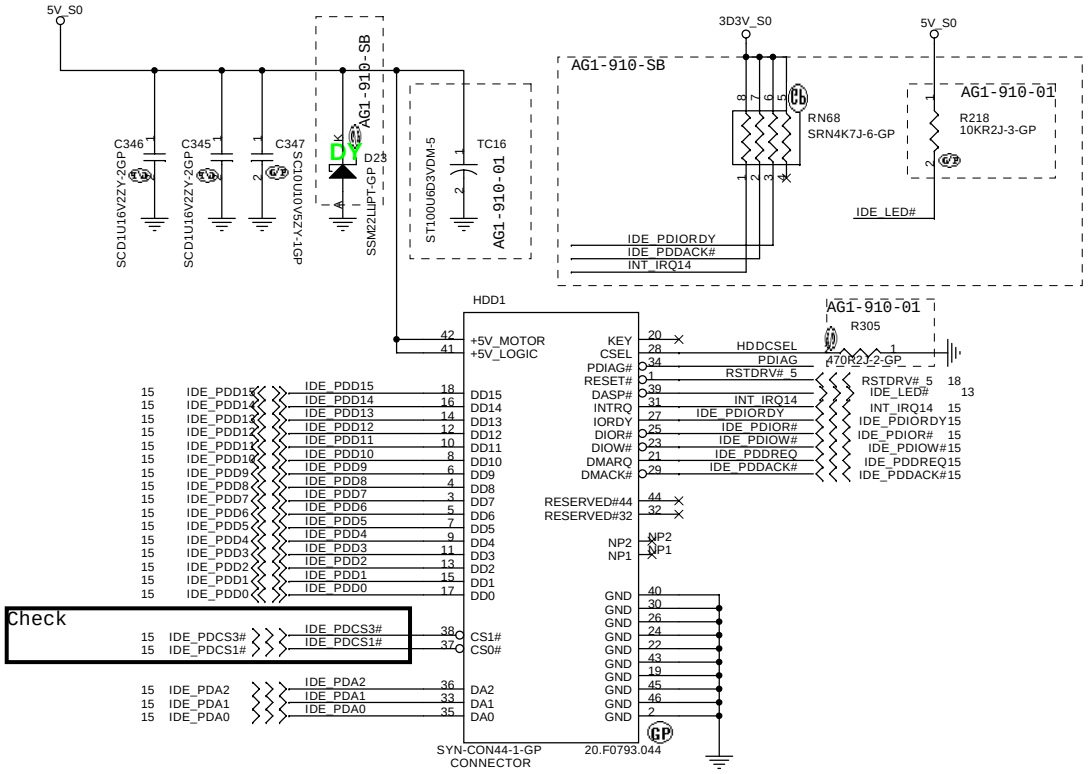
Title: *ICH6-M (4 of 4)*

Size	Document Number	Rev
A3	AG1(Alviso)	01

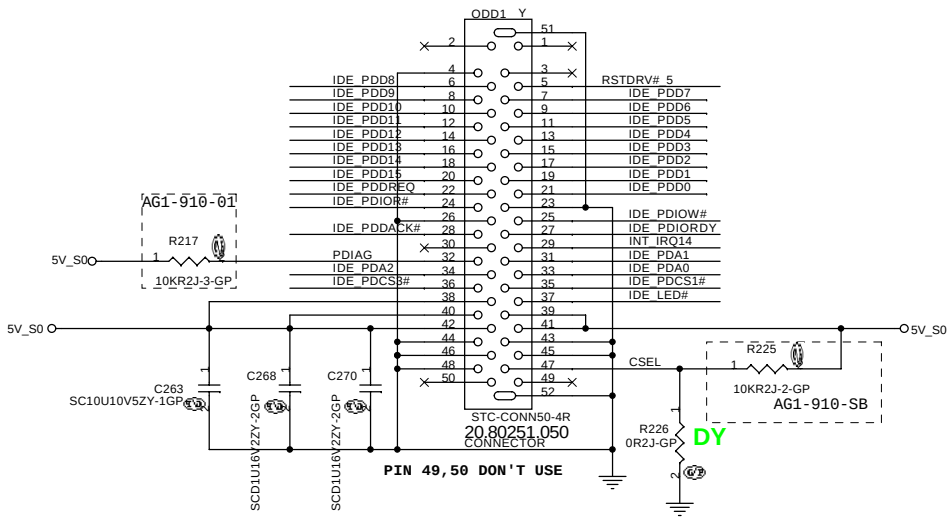
Date: Tuesday, October 25, 2005 Sheet 18 of 40


Layout 15 mil
FAN1_VCC
C70
SCD1U16V2ZY-2GP
C77
SC10U10V5ZY-1GP
D13
BAT54-4-GP
C73
SC2200P50V2KX-2GP
DY
AG1-910-SB
5V_S0
AG1-910-01
R82
10KR2J-3-GP
C76
SC100P50V2JN-3GP
FAN1_VCC
Layout 15 mil
2nd FAN1
ACES-CON3-1-GP
20.F0735.003
CONNECTOR
2nd source: 20.F0736.003
R246
200R2F-L-GP
C286
SCD1U16V2ZY-2GP
R242
4K99R2F-L-GP
Layout 30 mil
5V_G791_S0
C66
SC4D7U10V5ZY-3GP
C71
SCD1U16V2ZY-2GP
C72
SCD1U16V2ZY-2GP
U19
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
G791_32K
SMBD_G792
SMBC_G792
H_THERMDA
G792_DXP3
G792_DXP2
H_THERMDC
G792_DXN2
G792_DXN3
THRM#
T8_HW_SHUT#
V_DEGREE
Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
R241
49K9R2F-L-GP
SC470P50V2KX-3GP
C83
C290
C171
Q25
PMBS3904-1-GP
C139
Q24
System Sensor
System接第二組,VGA接第三組
G30
G29
GAP-CLOSE
Place near chip as close
as possible
C308
SC2200P50V2KX-2GP
H_THERMDA 4
H_THERMDC 4
3D3V_S0
R244
10KR2J-3-GP
THRM# 16
PWROK
G792_RESET#
4K7R2J-2-GP
R235
C65
SC2200P50V2KX-2GP
R236
10KR2J-3-GP
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
5V_S5_G913
C92
SCD1U16V2ZY-2GP
U27
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1F-GP
Output type:
Open-Drain RESET#
DCBATOUT
R88
1MR2J-1-GP
R92
15KR2F-GP
R93
110KR2F-GP
R249
0R2J-GP
INTRUDER# 15
RSMRST# 29
LOW3_OFF
3D3V_AUX_S5
BAW56-2-GP
D15
R247
10KR2J-3-GP
D14
BAT54-4-GP
(dummy, KBC already delay)
C85
SCD1U16V2ZY-2GP
R95
1KR2J-1-GP
Q15
PMBT2222A-1GP
4,15 H_PWRGD
C412
SCD1U16V2ZY-2GP
PM_THRMTRIP-I# 4,7,15
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size Custom
Document Number
AG1(Alviso)
Rev 01
Date: Thursday, October 27, 2005
Sheet 19 of 40

HDD Connector



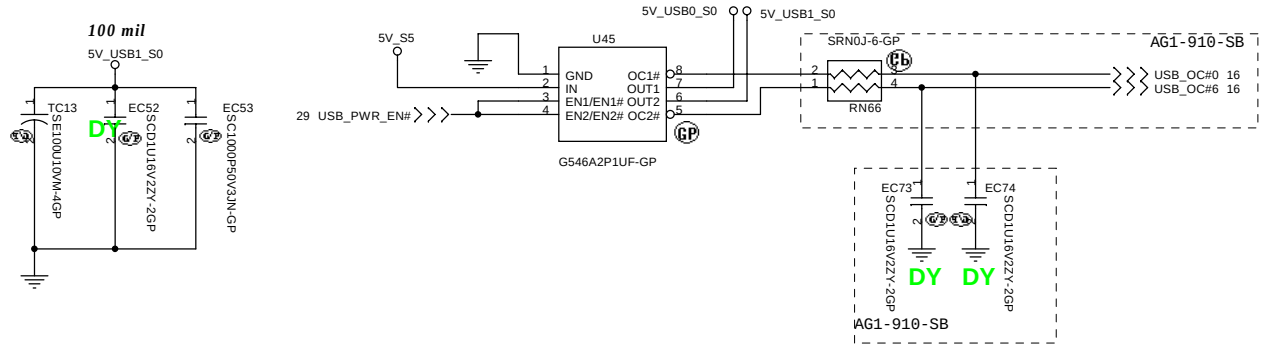
CD-ROM Connector

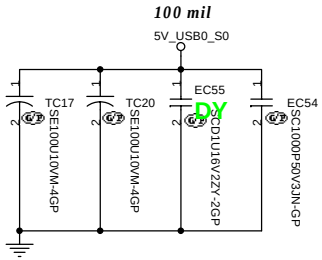


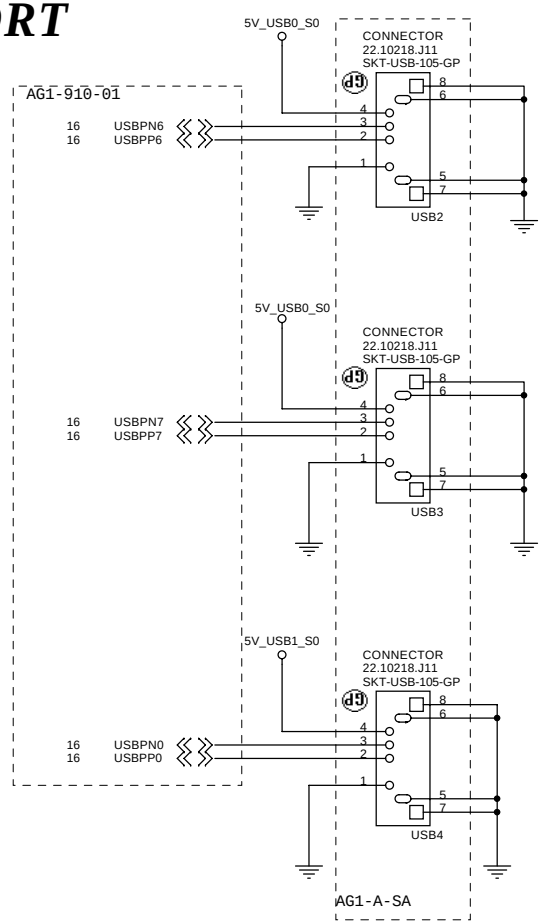
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD and CDROM***	
Size A3	Document Number AG1(Alviso)	Rev **01**
Date: Monday, October 31, 2005	Sheet 20 of 40	

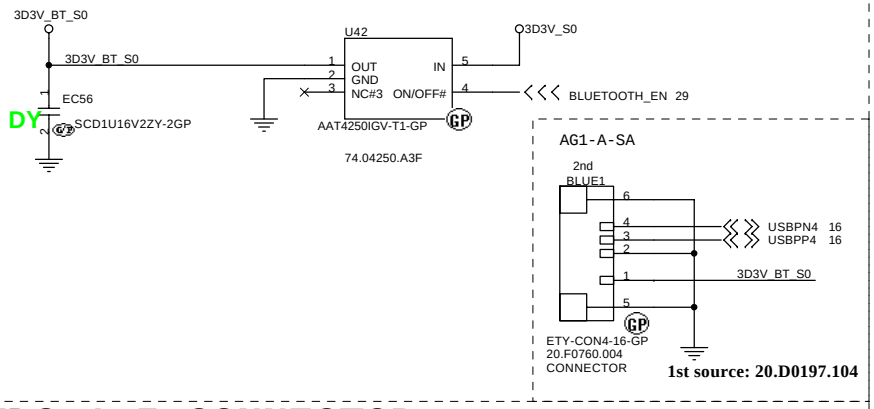
USB PORT



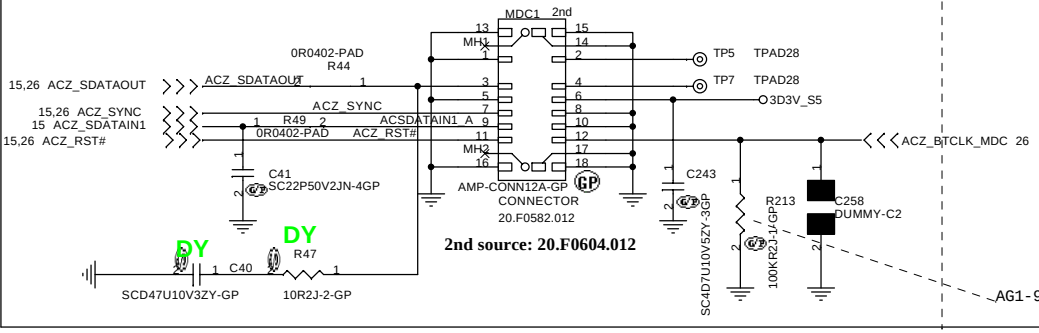




BLUETOOTH MODULE



MDC 1.5 CONNECTOR



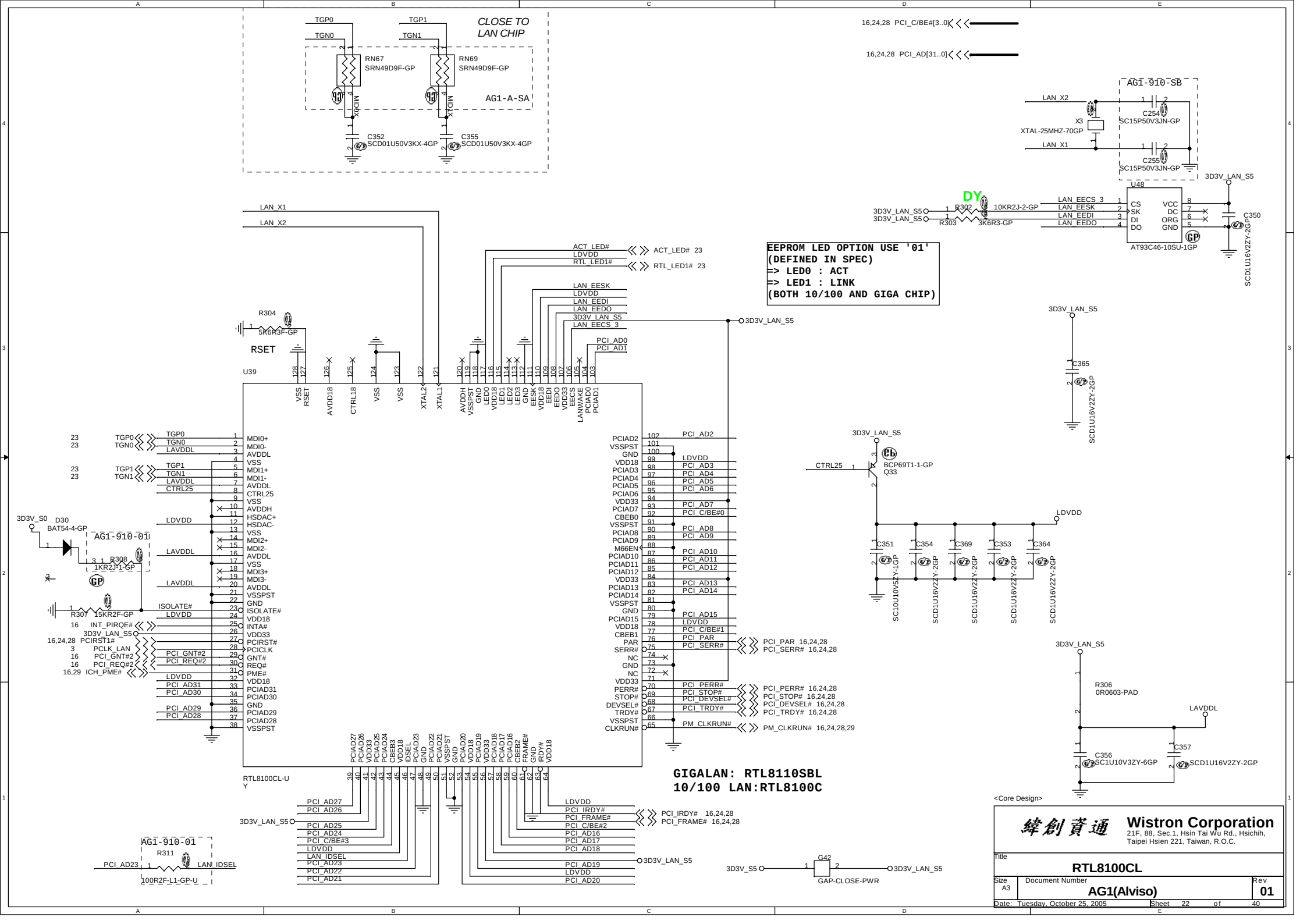
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

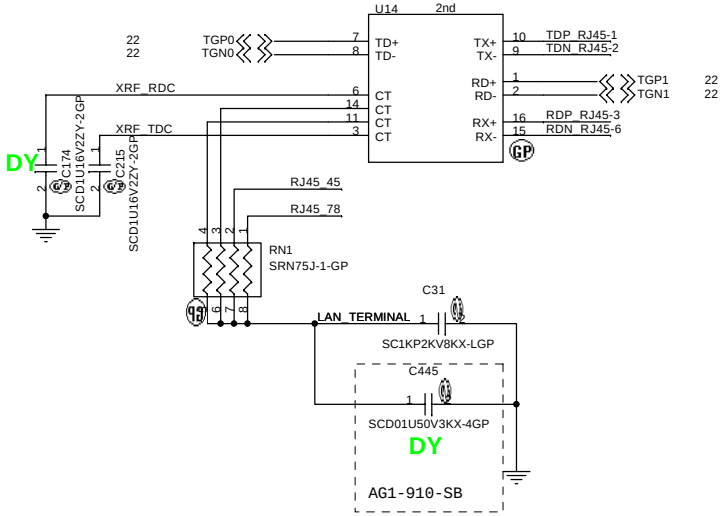
Title: **USB / MDC / BLUETOOTH**

Size	Document Number	Rev
A3	AG1(Alviso)	01

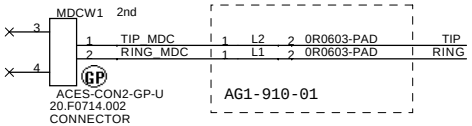
Date: Friday, October 28, 2005 Sheet 21 of 40


CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
RN67 SRN49D9F-GP
RN69 SRN49D9F-GP
AG1-A-SA
C352 SCD01U50V3KX-4GP
C355 SCD01U50V3KX-4GP
16,24,28 PCI_C/BE#[3..0]
16,24,28 PCI_AD[31..0]
AG1-910-SB
LAN_X2
X3 XTAL-25MHZ-70GP
LAN_X1
C254 SC15P50V3JN-GP
C255 SC15P50V3JN-GP
3D3V_LAN_S5
DY
R302 10KR2J-2-GP
R303 3K6R3-GP
U48
CS SK DI DO
VCC DC ORG GND
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
AT93C46-10SU-1GP
C350 SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
LAN_X1
LAN_X2
R304 5K6R3F-GP
RSET
U39
ACT_LED# 23
RTL_LED1# 23
LAN_EESK
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
VSS RSET AVDD18 CTRL18 VSS VSS XTAL2 XTAL1
AVDDH VSSPST GND LED0 VDD18 LED1 LED2 LED3 GND EESK VDD18 EEDI EEDO VDD33 EECS LANWAKE PCIAD0 PCIAD1
MDI0+ MDI0- AVDDL VSS MDI1+ MDI1- AVDDL CTRL25 VSS AVDDH HSDAC+ HSDAC- VSS MDI2+ MDI2- AVDDL VSS MDI3+ MDI3- AVDDL VSSPST GND
ISOLATE# VDD18 INTA# VDD33 PCIRST# PCICLK GNT# REQ# PME# VDD18 PCIAD31 PCIAD30 GND PCIAD29 PCIAD28 VSSPST
PCIAD2 VSSPST GND VDD18 PCIAD3 PCIAD4 PCIAD5 PCIAD6 VDD33 PCIAD7 CBEB0 VSSPST PCIAD8 PCIAD9 M66EN PCIAD10 PCIAD11 PCIAD12 VDD33 PCIAD13 PCIAD14 VSSPST GND PCIAD15 VDD18 CBEB1 PAR SERR# NC GND NC VDD33 PERR# STOP# DEVSEL# TRDY# VSSPST CLKRUN#
PCI_AD2 LDVDD PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_C/BE#0 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 LDVDD PCI_C/BE#1 PCI_PAR PCI_SERR# PCI_PERR# PCI_STOP# PCI_DEVSEL# PCI_TRDY# PM_CLKRUN#
PCI_PAR 16,24,28
PCI_SERR# 16,24,28
PCI_PERR# 16,24,28
PCI_STOP# 16,24,28
PCI_DEVSEL# 16,24,28
PCI_TRDY# 16,24,28
PM_CLKRUN# 16,24,28,29
TGP0 TGN0 LAVDDL TGP1 TGN1 LAVDDL CTRL25
LDVDD LAVDDL LAVDDL
3D3V_S0 D30 BAT54-4GP
AG1-910-01
R308 1KR2J-1-GP
R307 15KR2F-GP
ISOLATE#
INT_PIRQE# 16
3D3V_LAN_S5
PCIRST1# 16,24,28
PCLK_LAN 3
PCI_GNT#2 16
PCI_REQ#2 16
ICH_PME# 16,29
LDVDD
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_GNT#2
PCI_REQ#2
RTL8100CL-U Y
PCIAD27 PCIAD26 VDD33 PCIAD25 PCIAD24 CBEB3 VDD18 IDSEL PCIAD23 GND PCIAD22 PCIAD21 VSSPST GND PCIAD20 VDD18 VDD33 PCIAD18 PCIAD17 PCIAD16 CBEB2 FRAME# GND IRDY# VDD18
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_C/BE#3
LDVDD
LAN_IDSEL
PCI_AD23
PCI_AD22
PCI_AD21
LDVDD
PCI_IRDY#
PCI_FRAME#
PCI_C/BE#2
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
LDVDD
PCI_AD20
PCI_IRDY# 16,24,28
PCI_FRAME# 16,24,28
3D3V_LAN_S5
AG1-910-01
R311
PCI_AD23
LAN_IDSEL
100R2F-L1-GP-U
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
3D3V_LAN_S5
C365 SCD1U16V2ZY-2GP
CTRL25
BCP69T1-1-GP Q33
LDVDD
C351 SC10U10V5ZY-1GP
C354 SCD1U16V2ZY-2GP
C369 SCD1U16V2ZY-2GP
C353 SCD1U16V2ZY-2GP
C364 SCD1U16V2ZY-2GP
R306 0R0603-PAD
LAVDDL
C356 SC1U10V3ZY-6GP
C357 SCD1U16V2ZY-2GP
3D3V_S5
G42
GAP-CLOSE-PWR
3D3V_LAN_S5
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8100CL
Size A3
Document Number
AG1(Alviso)
Rev 01
Date: Tuesday, October 25, 2005
Sheet 22 of 40

10/100M Lan Transformer

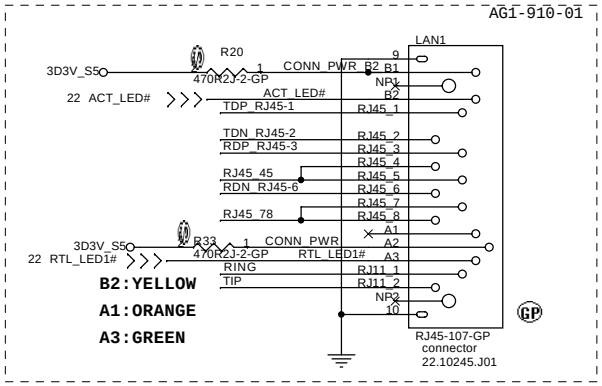


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



2nd source: 20.D0196.102

LAN Connector



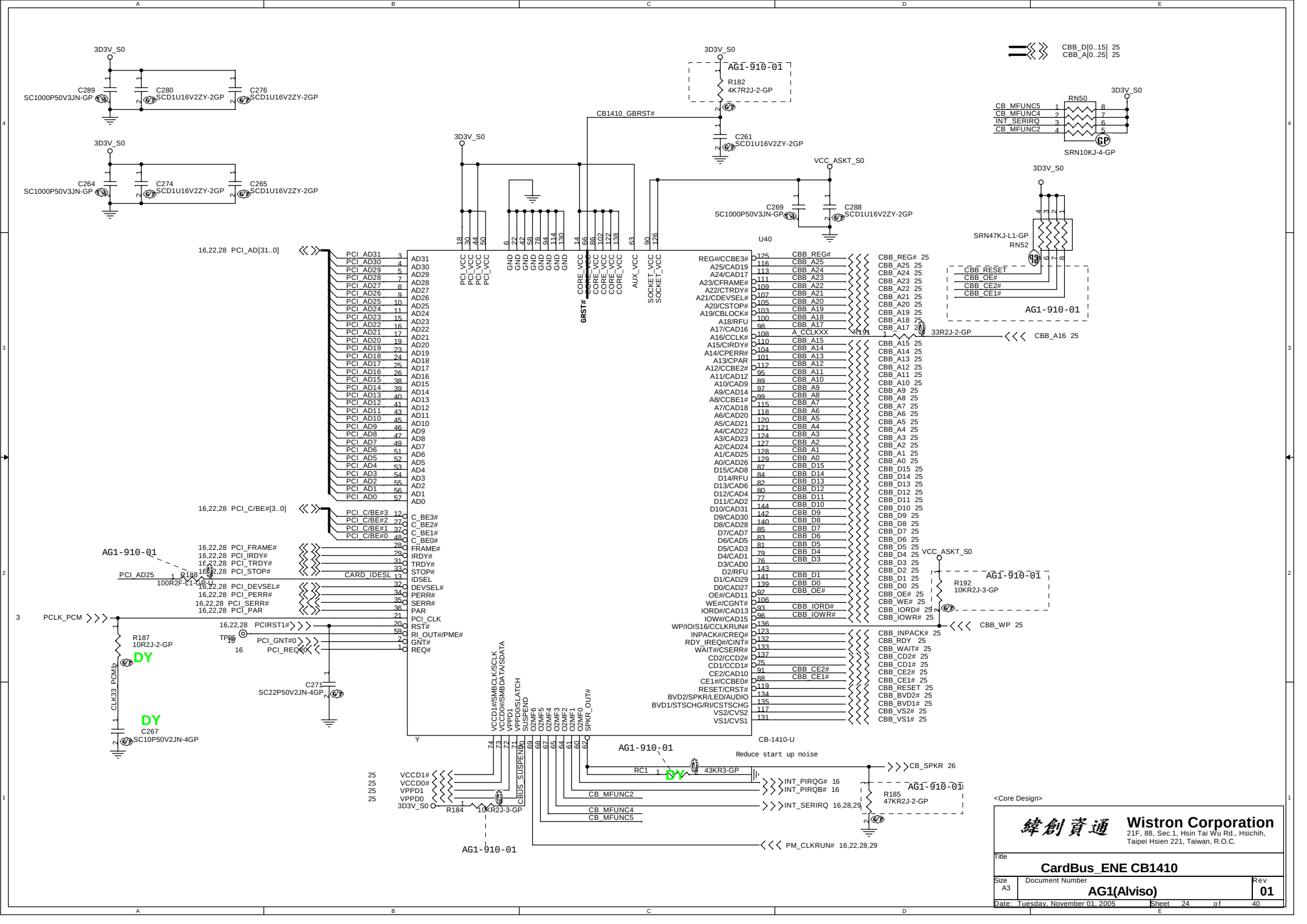
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

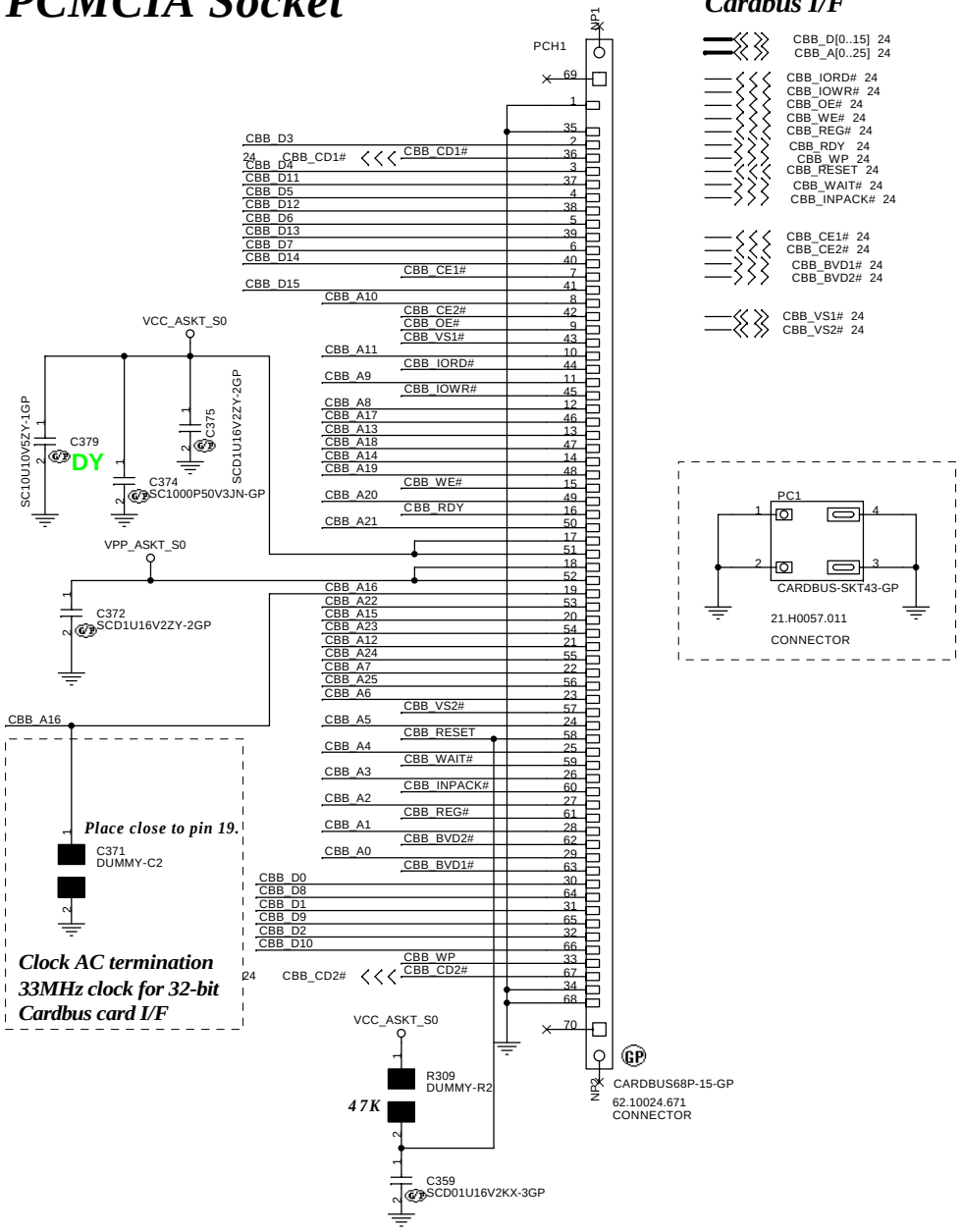
Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Saturday, October 29, 2005 | Sheet 23 of 40



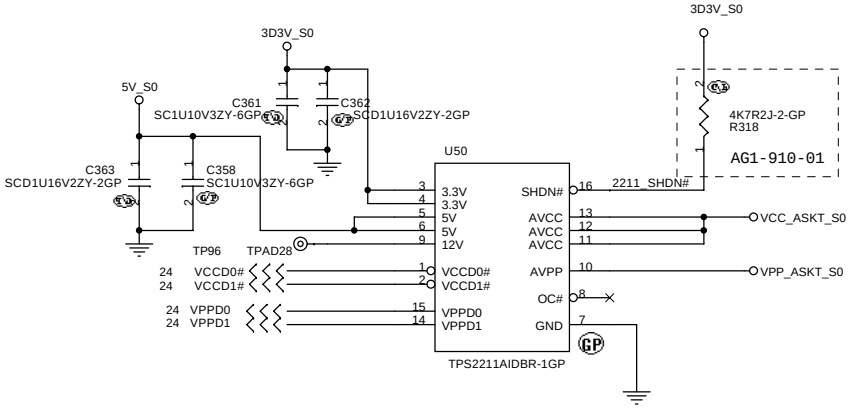
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CardBus_ENE CB1410
Size A3	Document Number AG1(Alviso) Rev 01
Date: Tuesday, November 01, 2005	Sheet 24 of 40

PCMCIA Socket



Cardbus I/F

Power switch

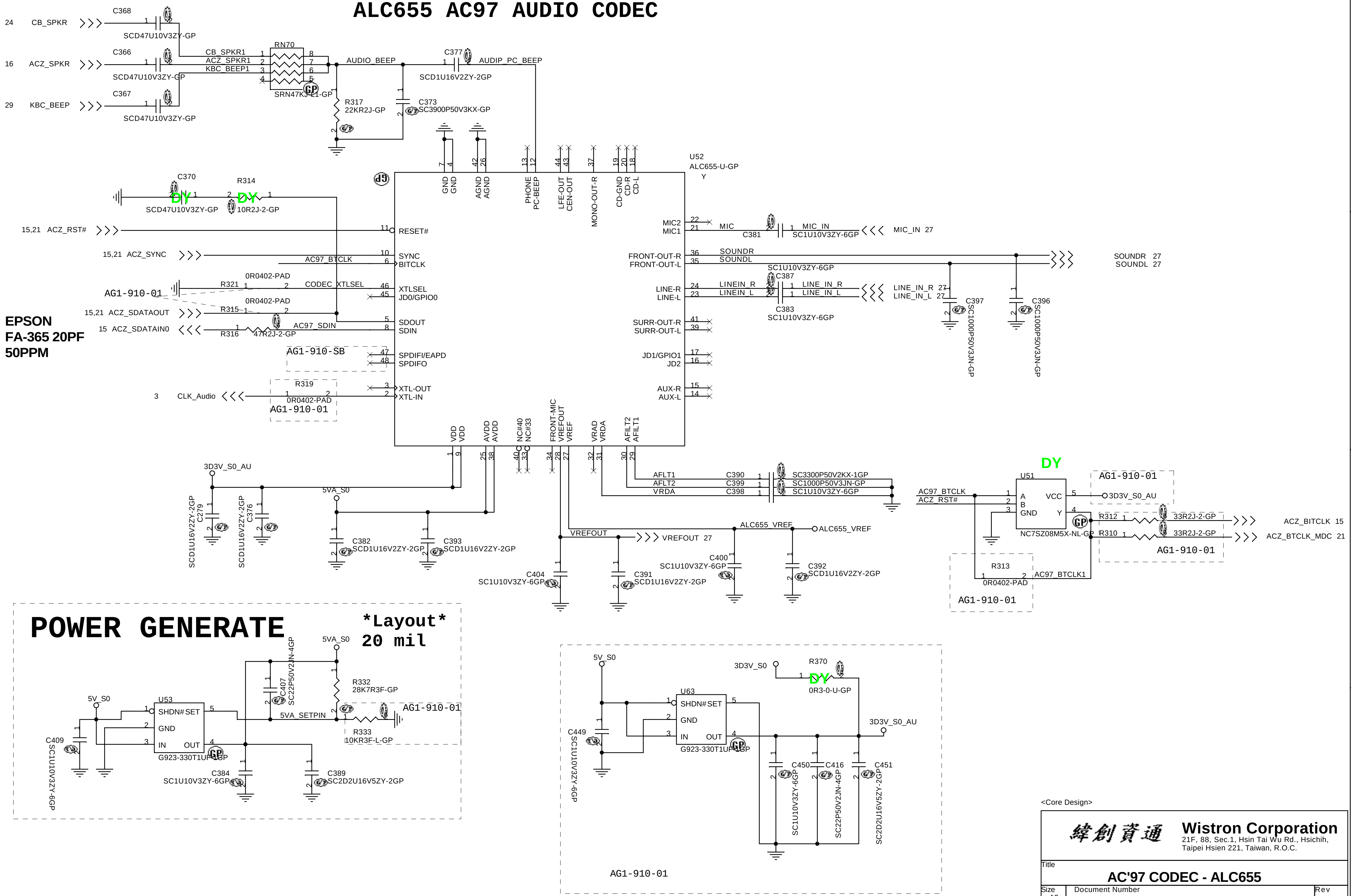


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCA		
Size: A3	Document Number: AG1(Alviso)	Rev: 01
Date: Tuesday, October 25, 2005	Sheet 25 of 40	

ALC655 AC97 AUDIO CODEC

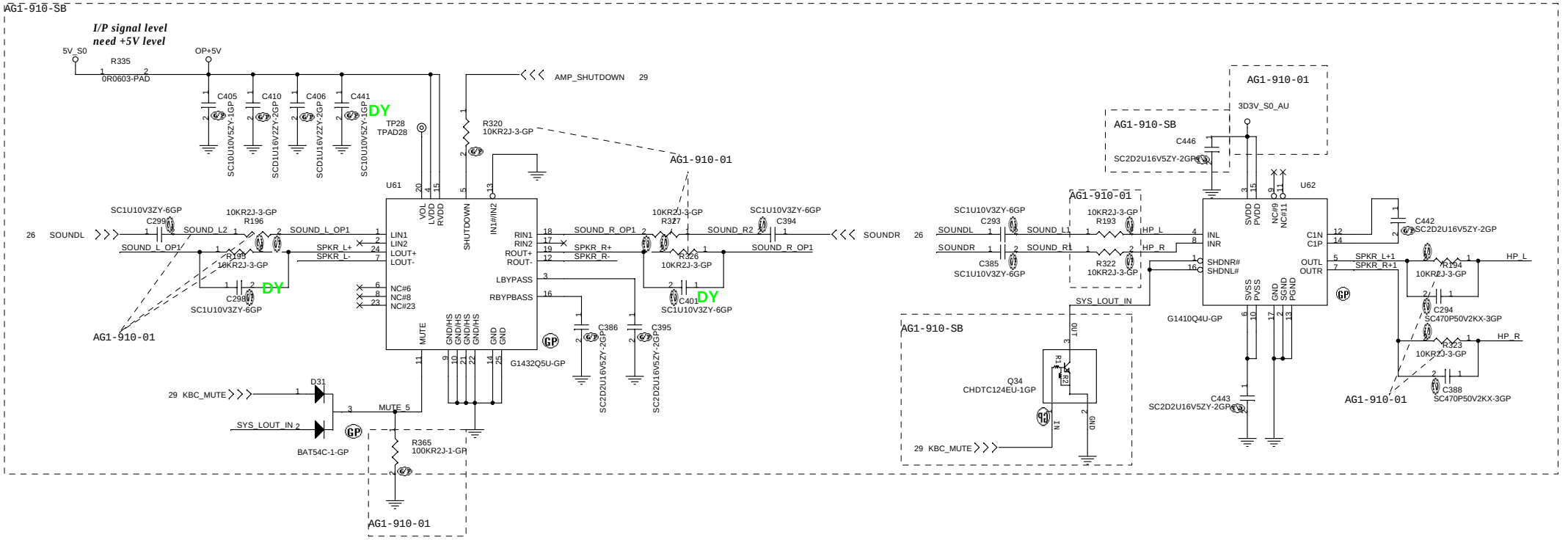


<Core Design>

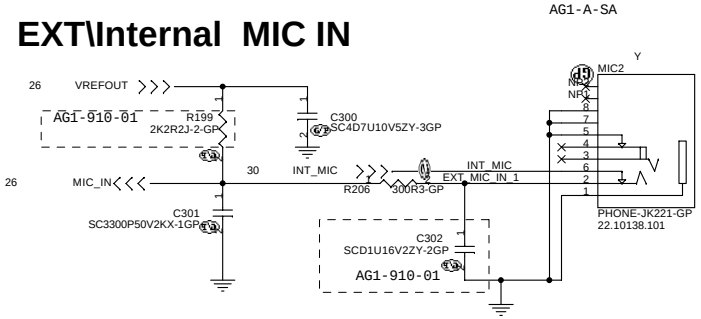
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
AC'97 CODEC - ALC655		
Size: A3	Document Number: AG1(Alviso)	Rev: 01
Date: Tuesday, November 01, 2005	Sheet 26 of 40	

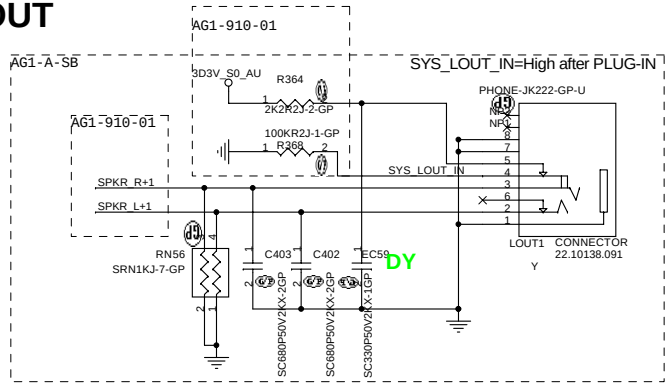
AUDIO OP AMPLIFIER



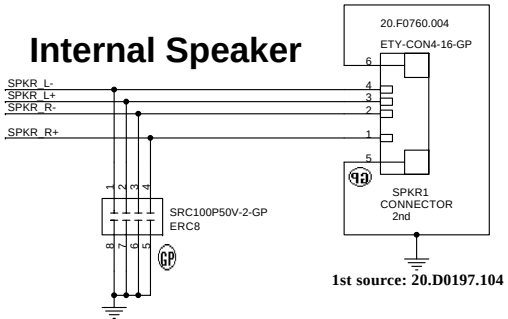
EXT\Internal MIC IN



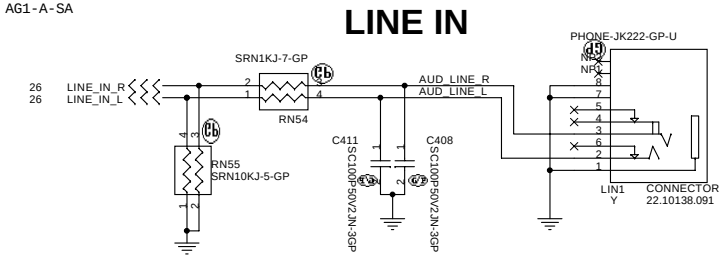
LINE OUT



Internal Speaker



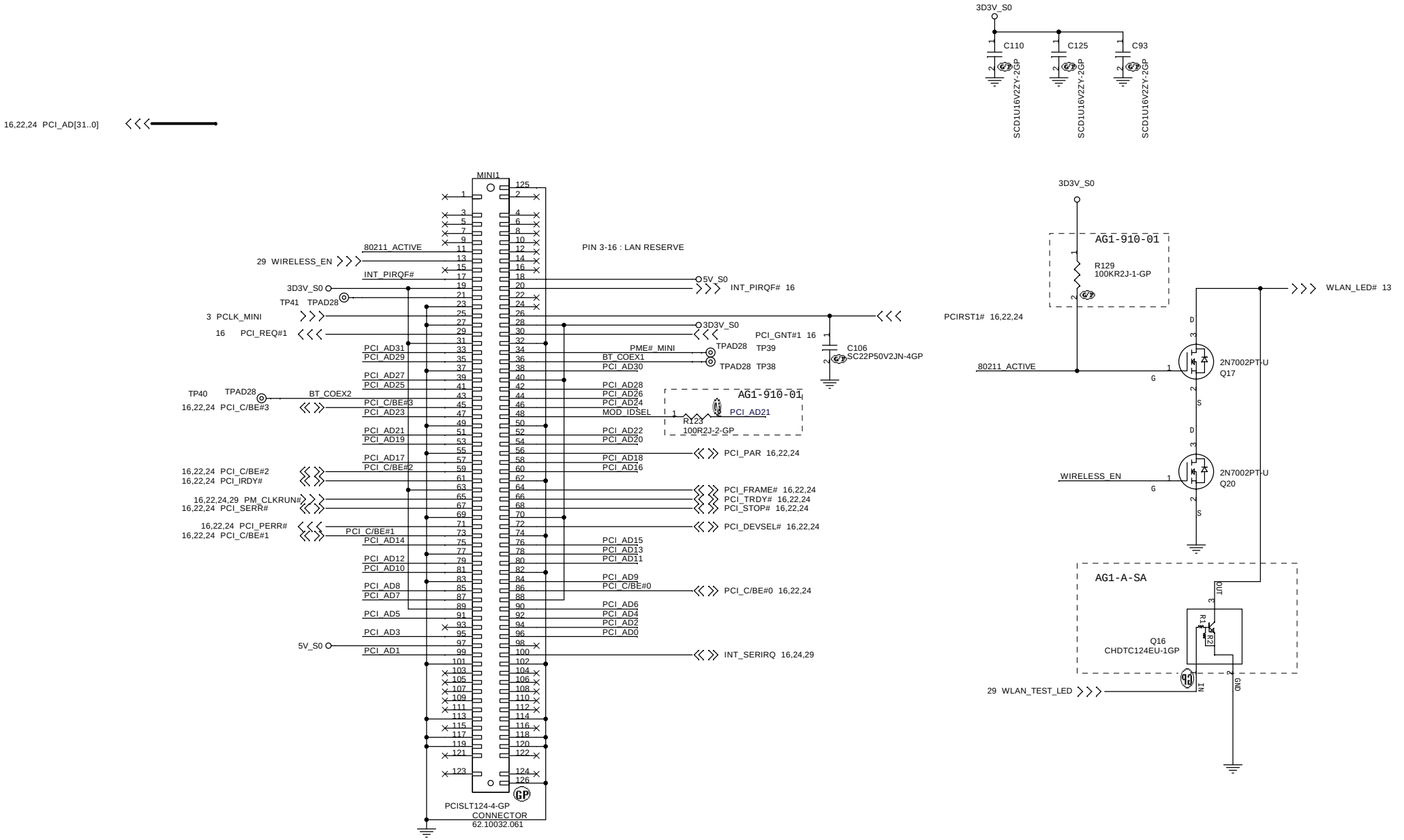
LINE IN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio AMP and Jack		
Size	Document Number	Rev
	AG1(Alviso)	**01**
Date: Monday, October 31, 2005	Sheet 27 of 40	



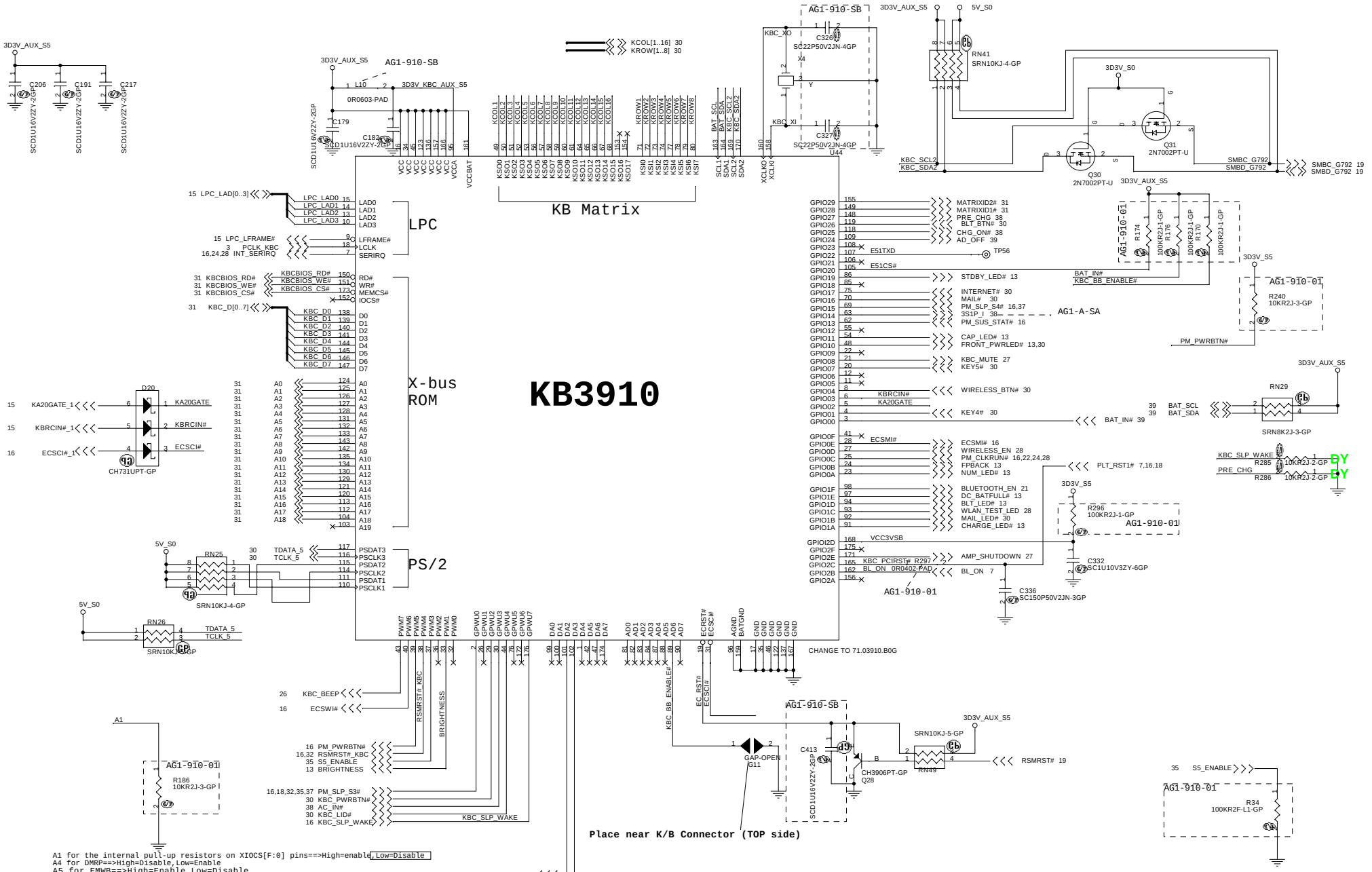
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

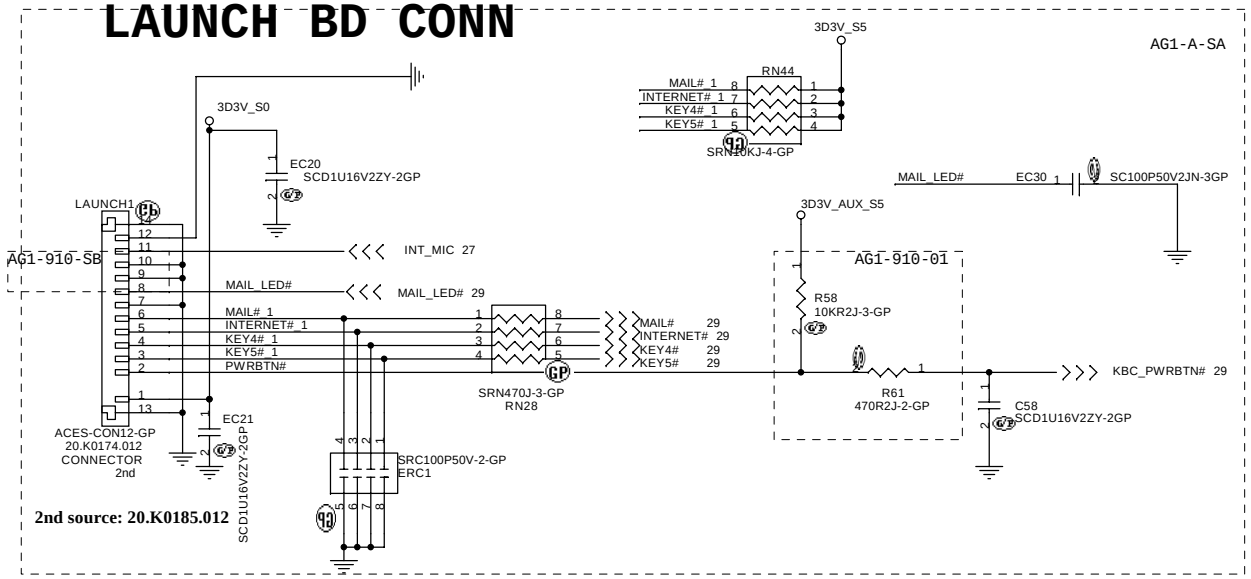
Title: ***MINI-PCI***

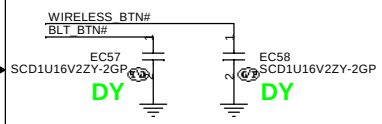
Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

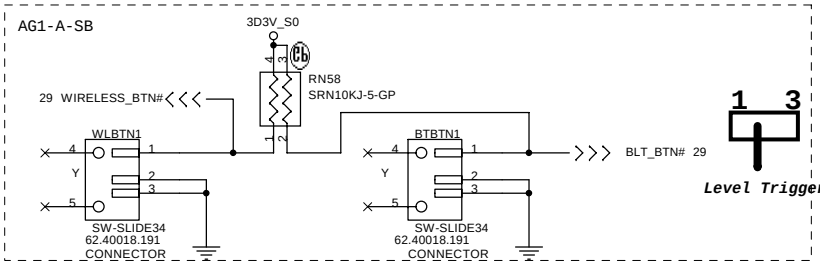
Date: Tuesday, October 25, 2005 | Sheet 28 of 40


KB3910
LPC
KB Matrix
X-bus ROM
PS/2
AG1-910-SB
AG1-910-01
AG1-A-SA
CHANGE TO 71.03910.B0G
Place near K/B Connector (TOP side)
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==> High=Test Mode,Low=Normal operation(Recommended)
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC ENE
Size Custom
Document Number
AG1(Alviso)
Rev 01
Date: Thursday, October 27, 2005
Sheet 29 of 40

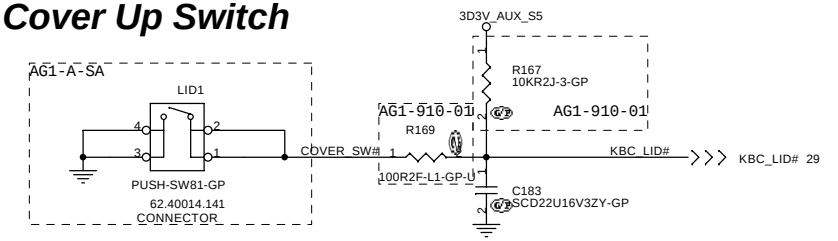
LAUNCH BD CONN



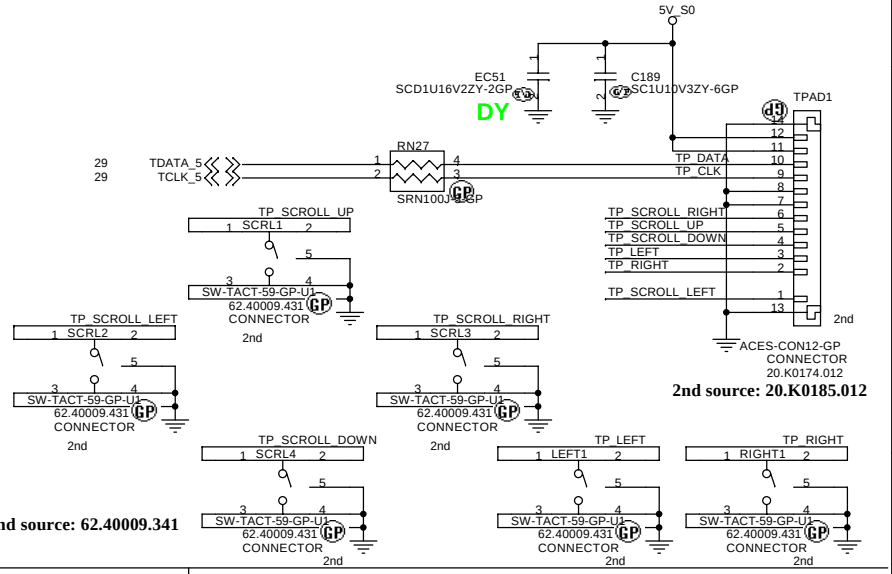




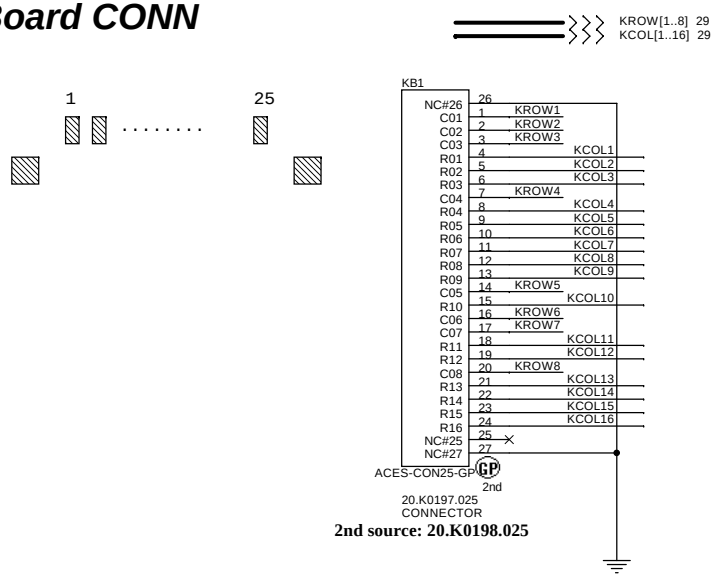
Cover Up Switch



TOUCH PAD

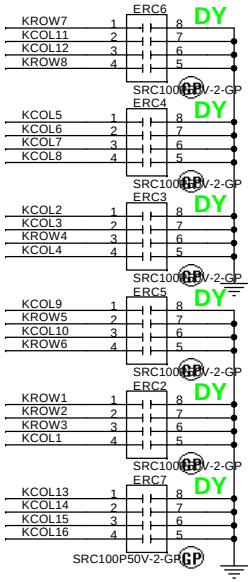


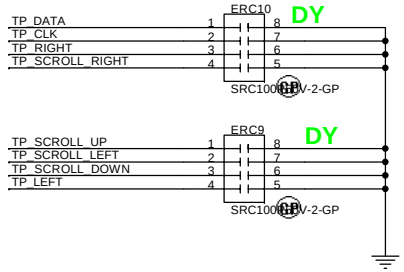
Internal KeyBoard CONN



Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.





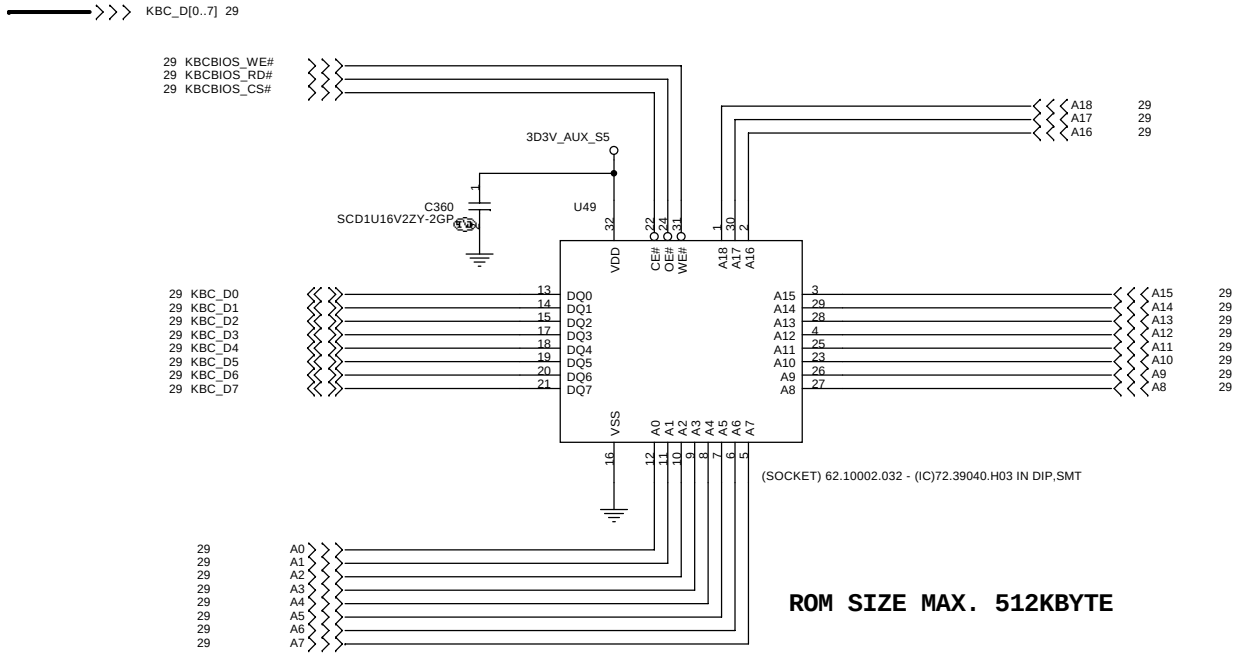
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONs / KB / TOUCHPAD**

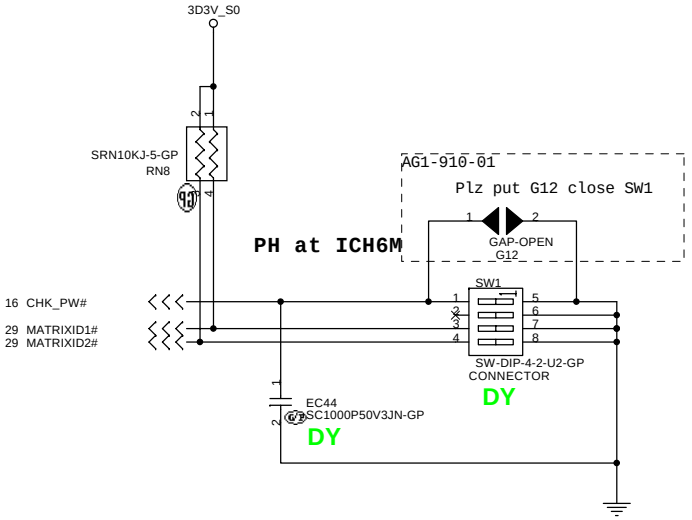
Size	Document Number	Rev
A3	AG1-910	01

Date: Tuesday, November 01, 2005 Sheet 30 of 40



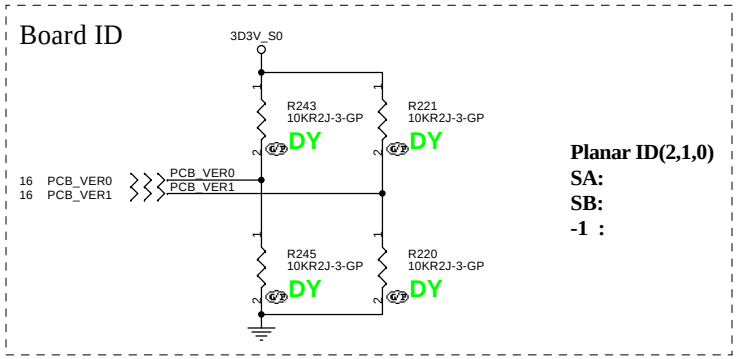
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0



Planar ID(2,1,0)
SA:
SB:
-1 :

<Core Design>

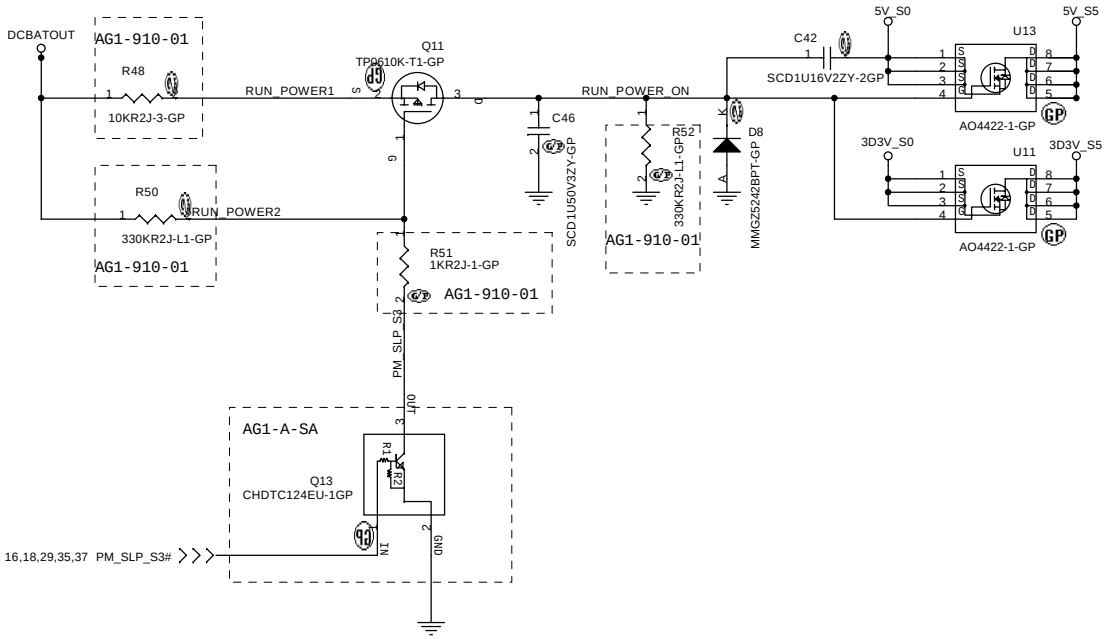
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

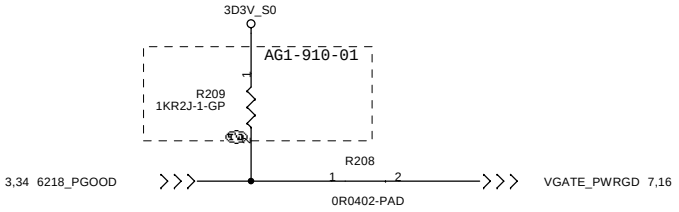
Size: A3 | Document Number: **AG1-910** | Rev: **01**

Date: Tuesday, November 01, 2005 | Sheet 31 of 40

Run Power



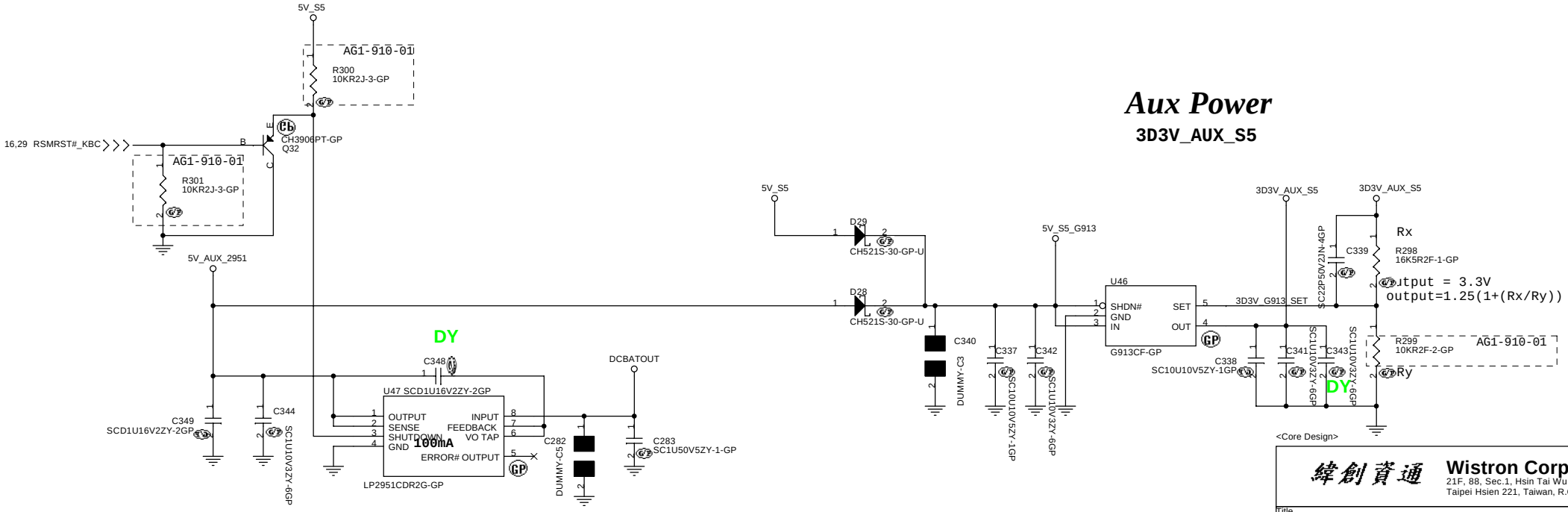
PWRGD for NB and SB



PWRGD to Turn on CPU_Core_Power

Aux Power

3D3V_AUX_S5



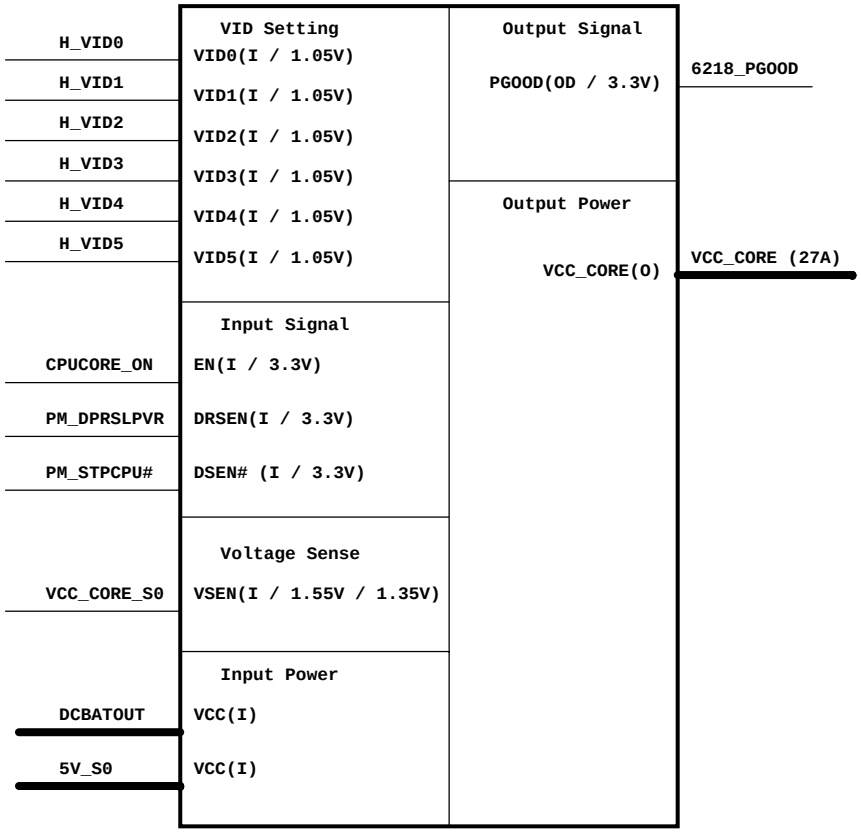
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

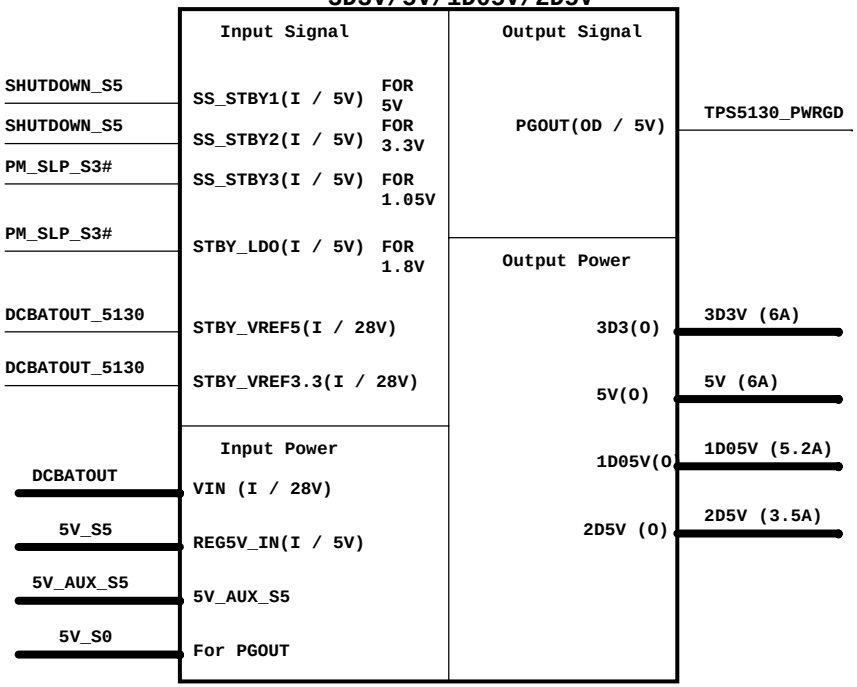
Size: A3 | Document Number: AG1-910 | Rev: 01

Date: Tuesday, October 25, 2005 | Sheet 32 of 40

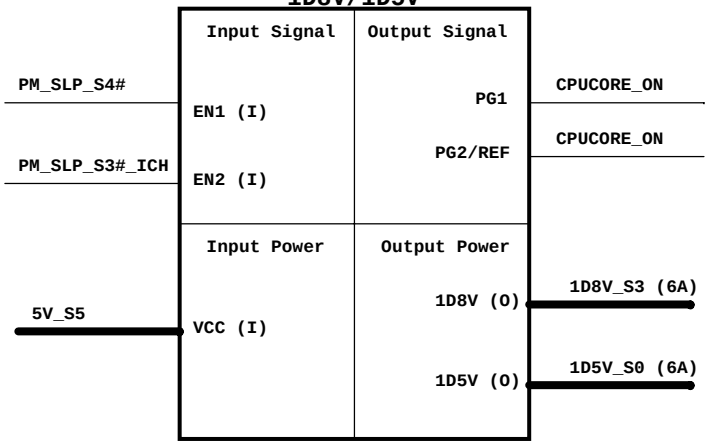
CPU_CORE ISL6218CV



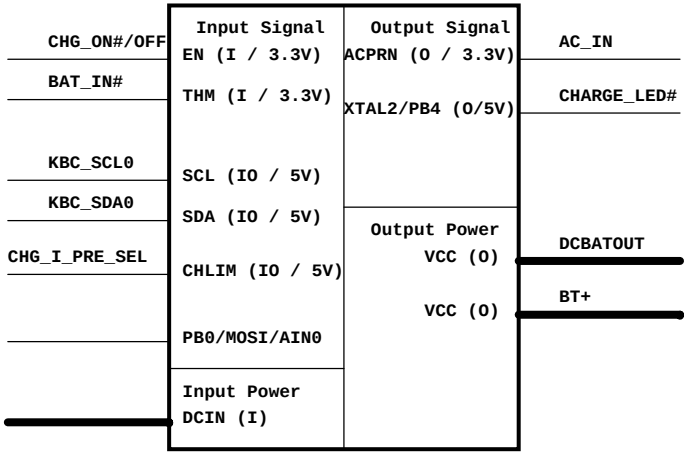
TPS5130 3D3V/5V/1D05V/2D5V



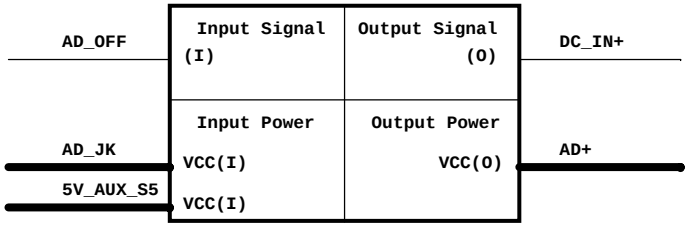
ISL6227 1D8V/1D5V



Charger_ISL6255



Adapter



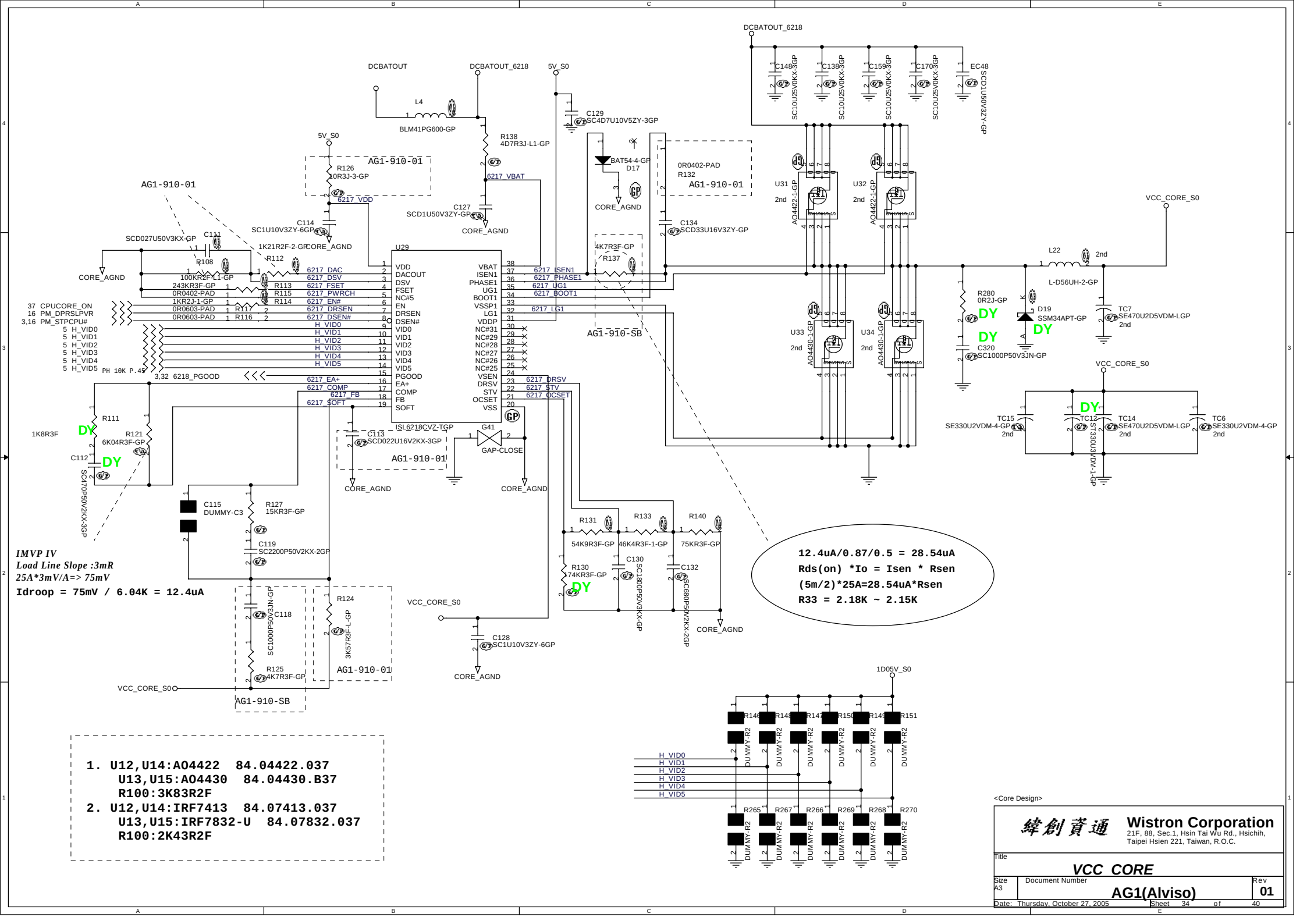
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Diagram***

Size	Document Number	Rev
A3	AG1(Alviso)	01

Date: Monday, October 17, 2005 Sheet 33 of 40



IMVP IV
Load Line Slope :3mR
*25A*3mV/A=> 75mV*
Idroop = 75mV / 6.04K = 12.4uA

12.4uA/0.87/0.5 = 28.54uA
Rds(on) *Io = Isen * Rsen
(5m/2)*25A=28.54uA*Rsen
R33 = 2.18K ~ 2.15K

1. U12,U14:AO4422 84.04422.037
   U13,U15:AO4430 84.04430.B37
   R100:3K83R2F
2. U12,U14:IRF7413 84.07413.037
   U13,U15:IRF7832-U 84.07832.037
   R100:2K43R2F

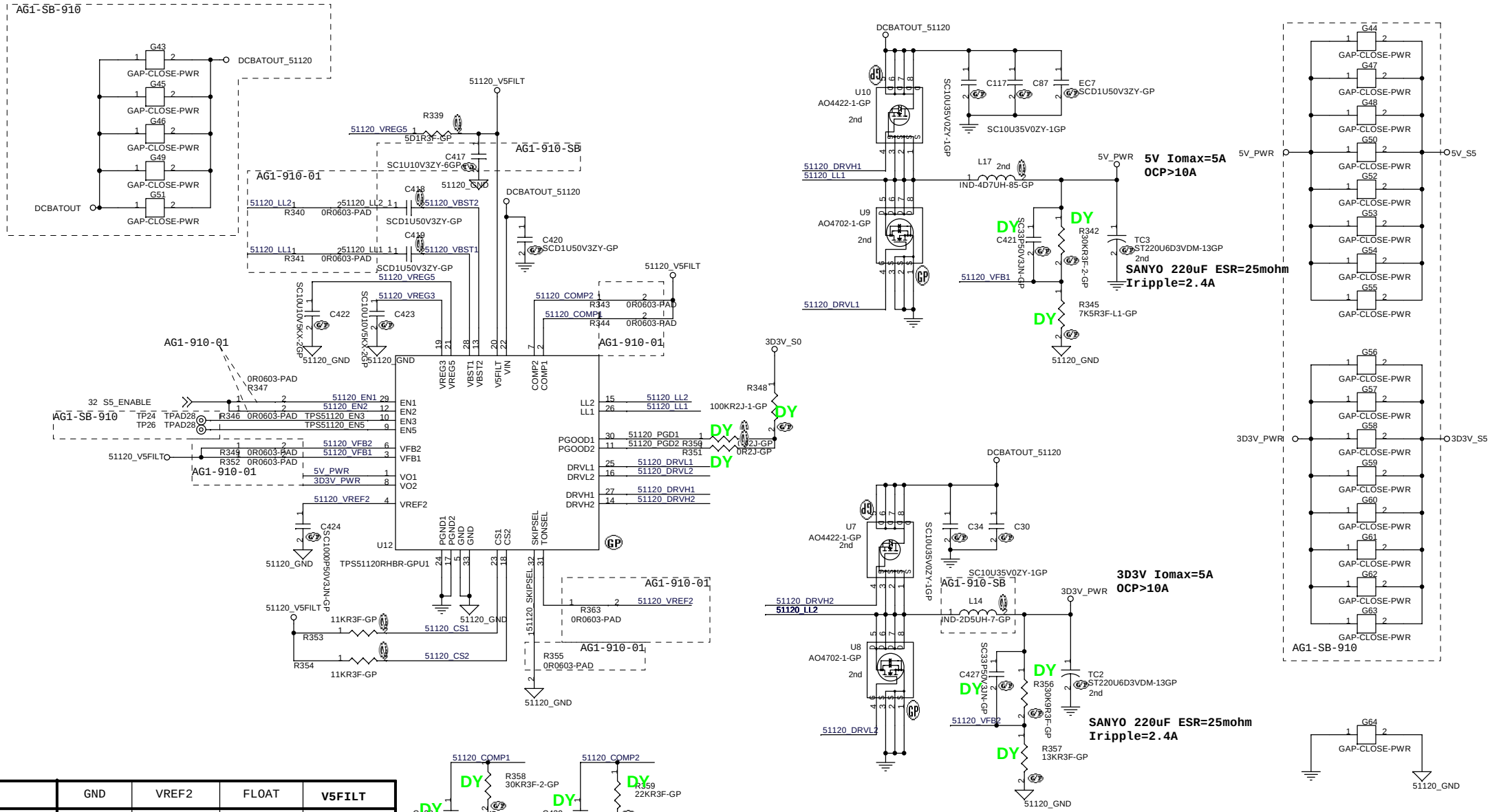
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VCC CORE***

Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Thursday, October 27, 2005 | Sheet 34 of 40



	GND	VREF2	FLOAT	**V5FILT**
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

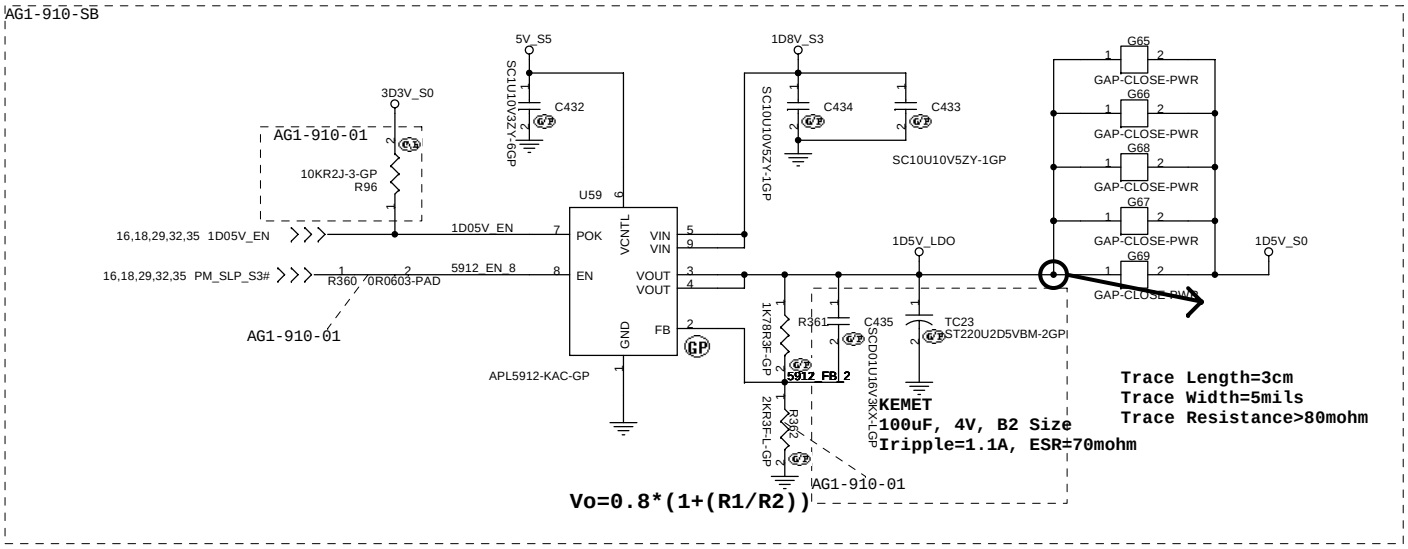
<Core Design>

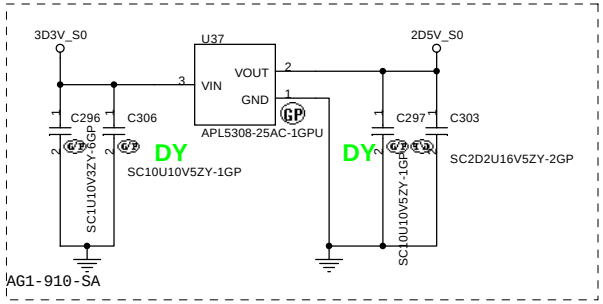
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51120 3D3V 5V***

Size: A3 | Document Number: **AG1(Alviso)** | Rev: **01**

Date: Friday, October 28, 2005 | Sheet 35 of 40





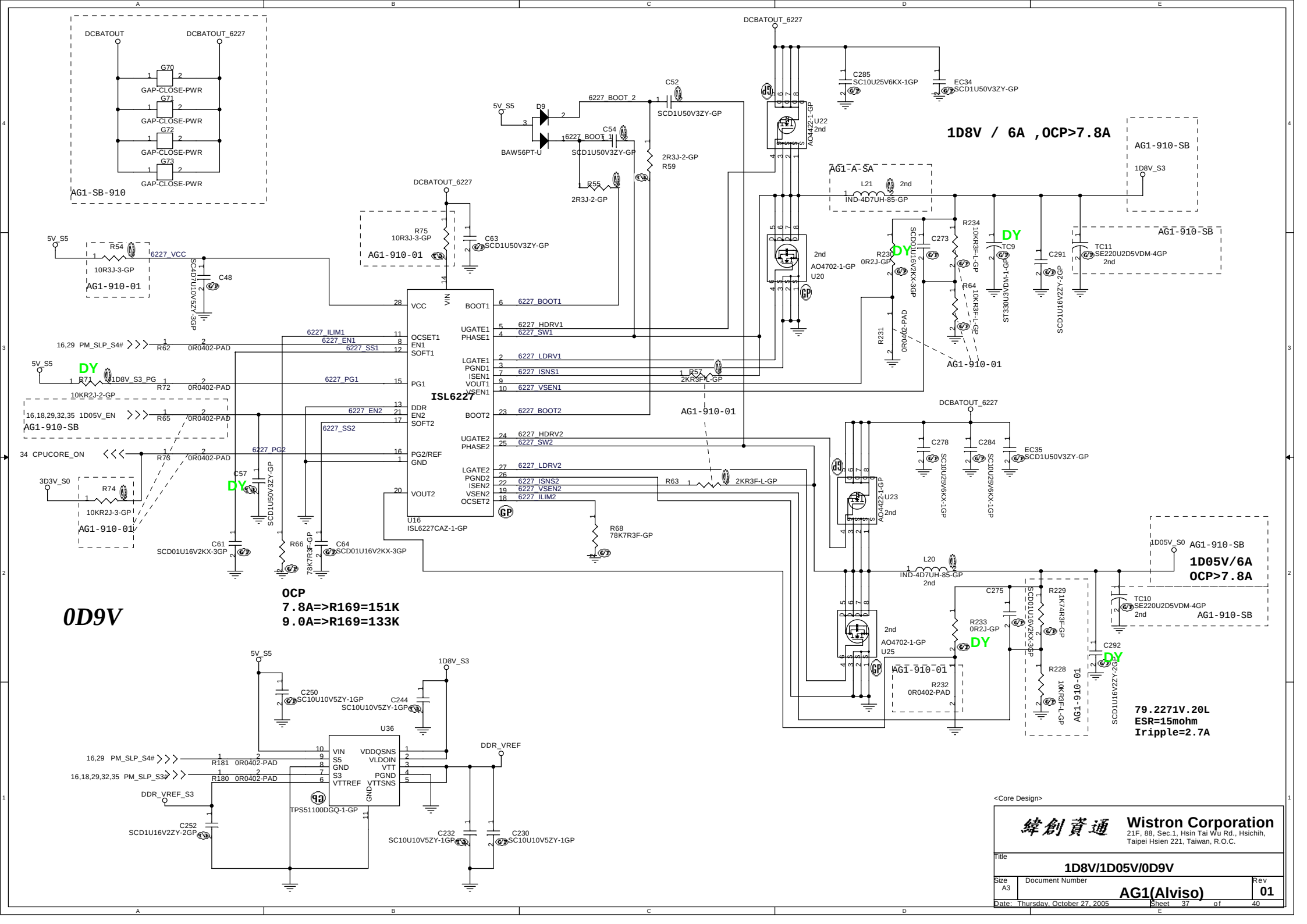
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***1D5V/2D5V(LDO)***

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

Date: Monday, October 31, 2005 Sheet 36 of 40



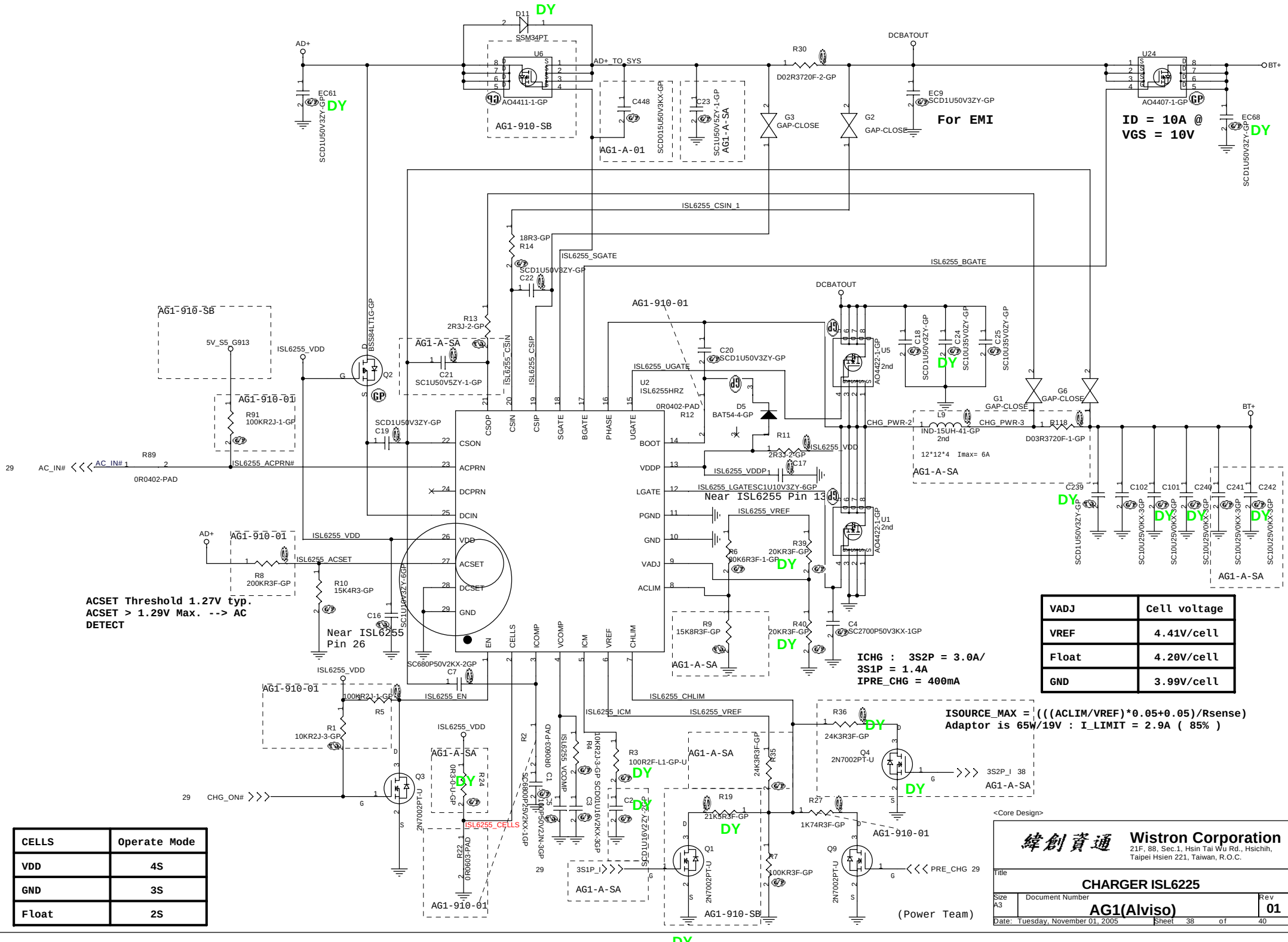
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **1D8V/1D05V/0D9V**

Size	Document Number	Rev
A3	AG1(Alviso)	01

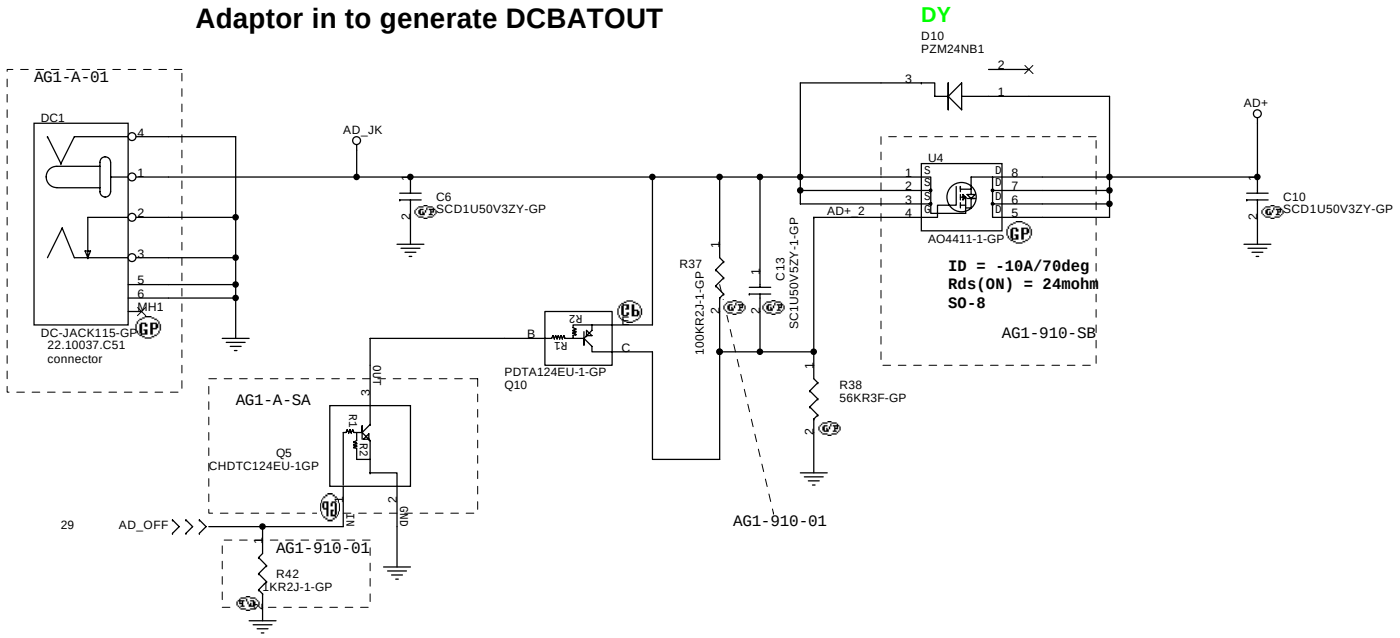
Date: Thursday, October 27, 2005 Sheet 37 of 40



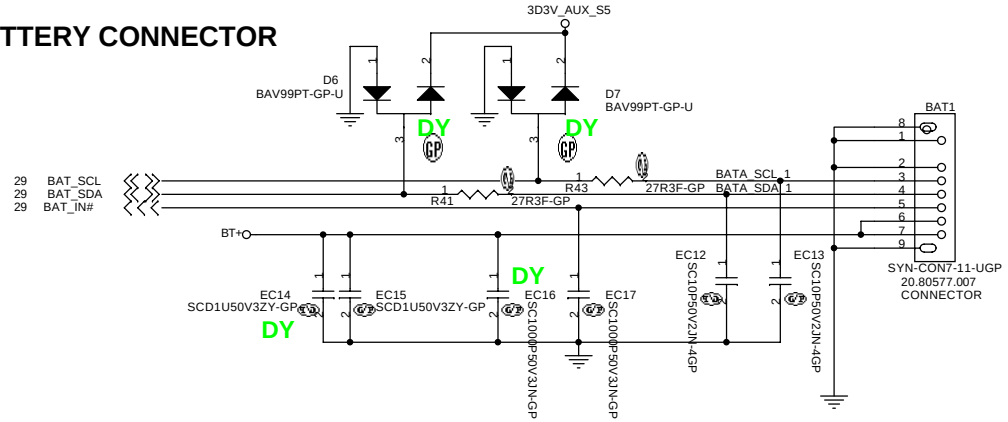
VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT

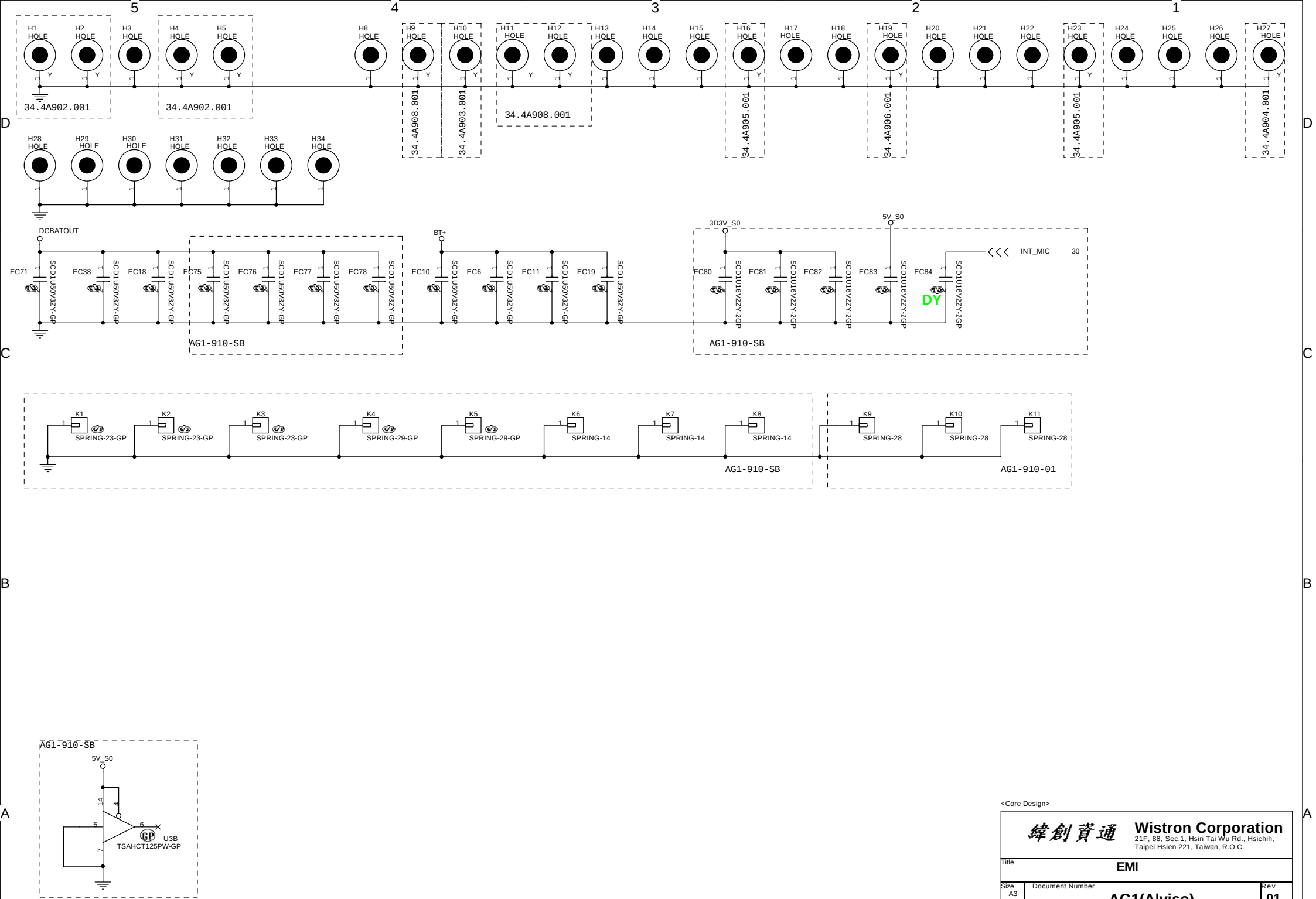


BATTERY CONNECTOR



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AD/BATT CONN
Size: A3	Document Number: AG1(Alviso)
Rev	01
Date: Tuesday, November 01, 2005	Sheet 39 of 40



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI**

Size	Document Number	Rev
A3	**AG1(Alviso)**	**01**

Date: Wednesday, November 02, 2005 Sheet 40 of 40