

Compal Confidential

HCL51 Schematics Document

Intel Yonah Processor with ATIRC410MD/E + DDRII + SB460M

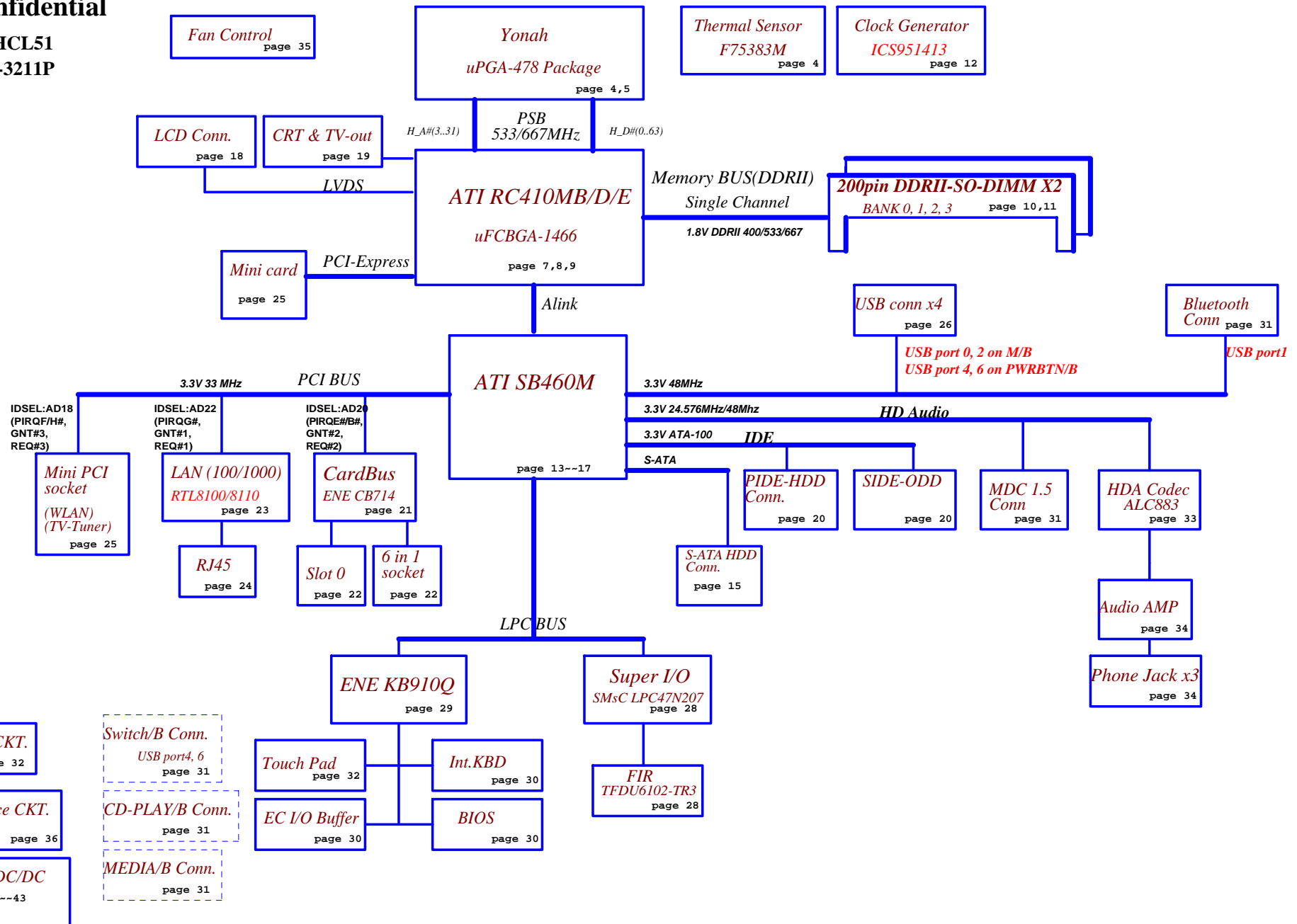
2006-04-05

REV: 1.0

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				HCL51 LA-3211P	0.4
				Date: 星期二, 四月 11, 2006	Sheet 1 of 43

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Model Name : HCL51
File Name : LA-3211P



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				HCL51 LA-3211P
				Rev 0.4
				Date: 星期二, 四月 11, 2006
				Sheet 2 of 43

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQA
LAN(10/100)	AD22	1	PIRQG
Mini-PCI(WLAN/TV-Tuner)	AD18	3	PIRQF/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

SB460M SM Bus address

Device	Address
Clock Generator (ICS951413)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.2
2	0.2
3	
4	
5	
6	
7	

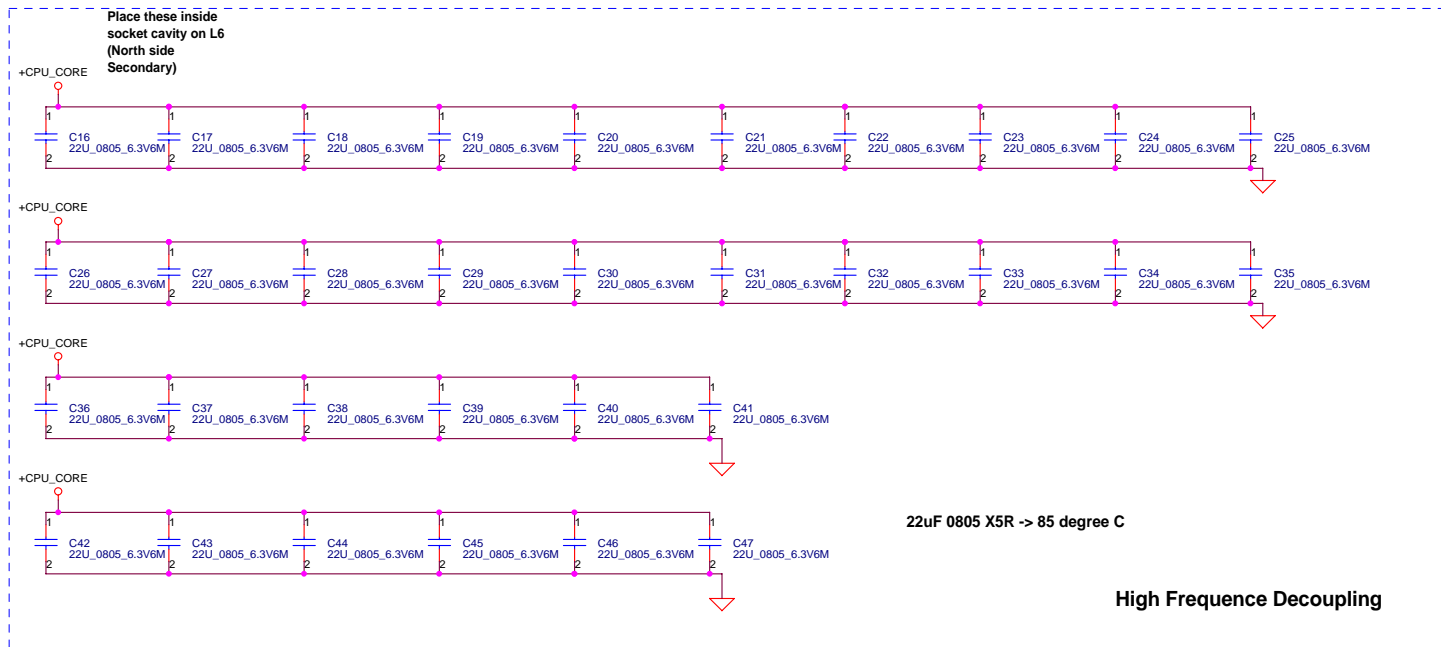
BTO Option Table

BTO Item	BOM Structure
LAN(10/100)	8100C@
LAN(GIGA)	8110S@
FIR	FIR@
MINI CARD1	MINI1@
SATA HDD	SATA@
CardReader	4IN1@

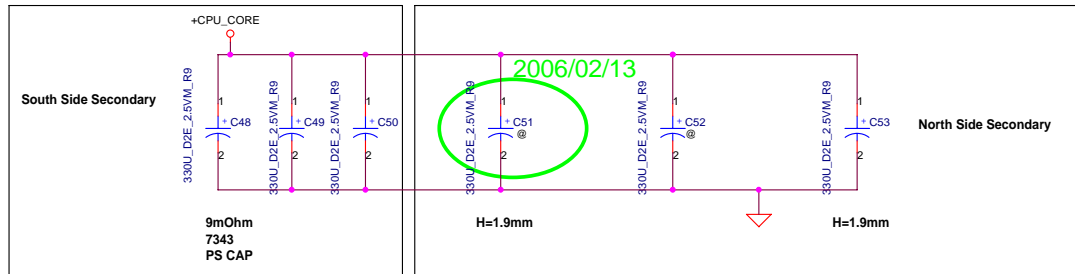
SKU ID Table

SKU ID	SKU
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1	
2	
3	
4	
5	
6	
7	

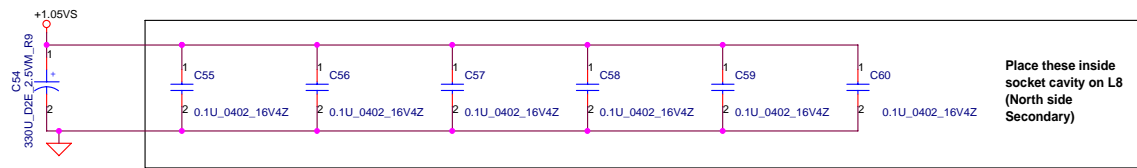
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				Date:	星期二, 四月 11, 2006	Sheet	3 of 43



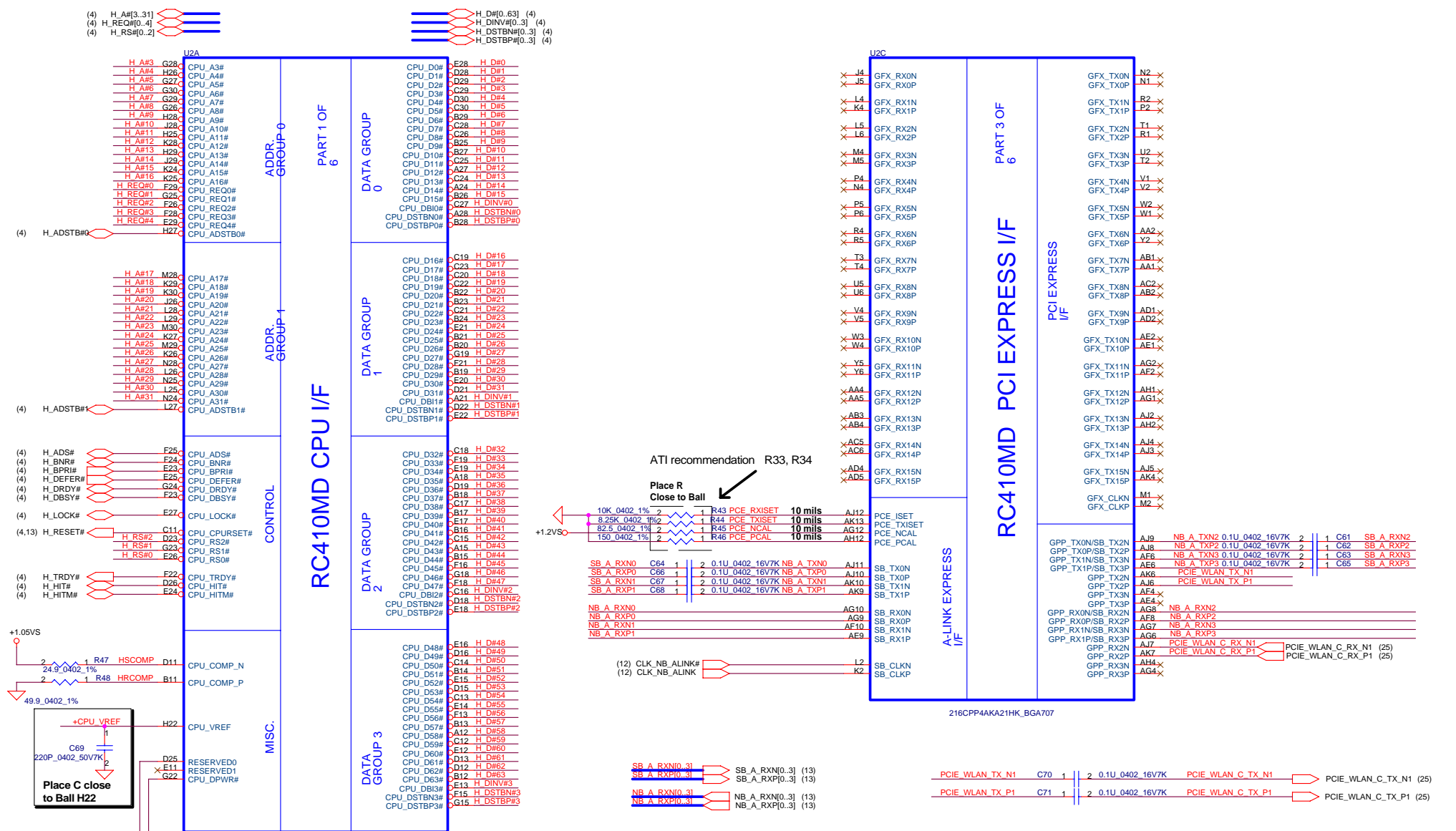
Near VCORE regulator.



ESR <= 1.5m ohm
Capacitor > 1980uF

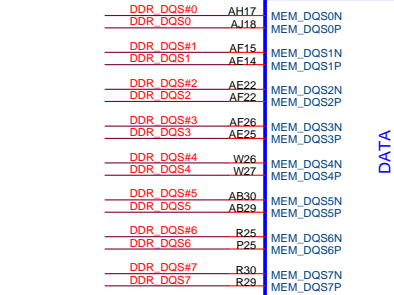
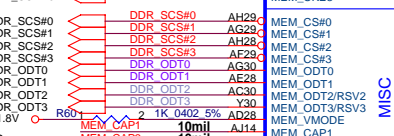
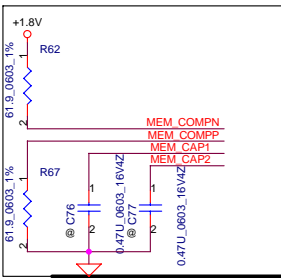
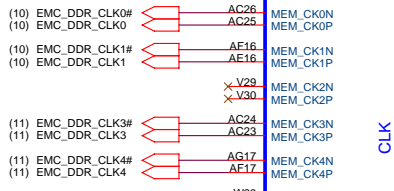
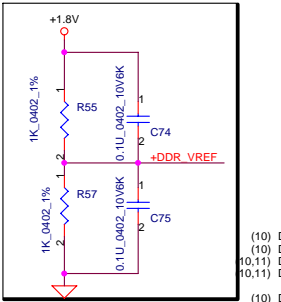
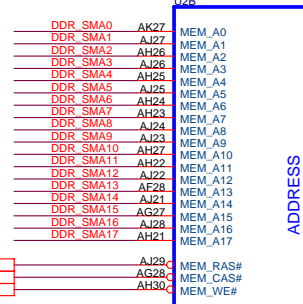
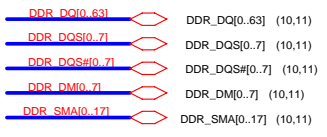


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				Rev
				0.4
Date: 星期二, 四月 11, 2006				Sheet 6 of 43

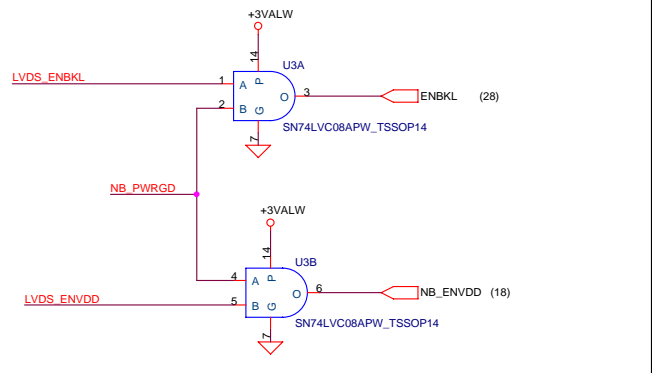
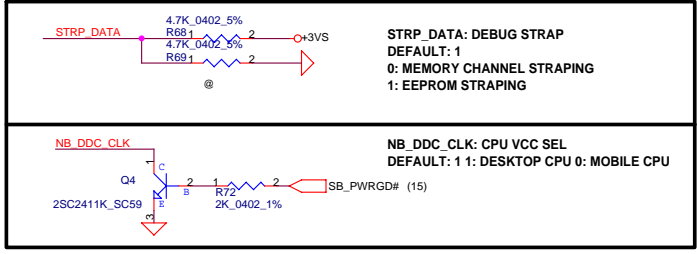
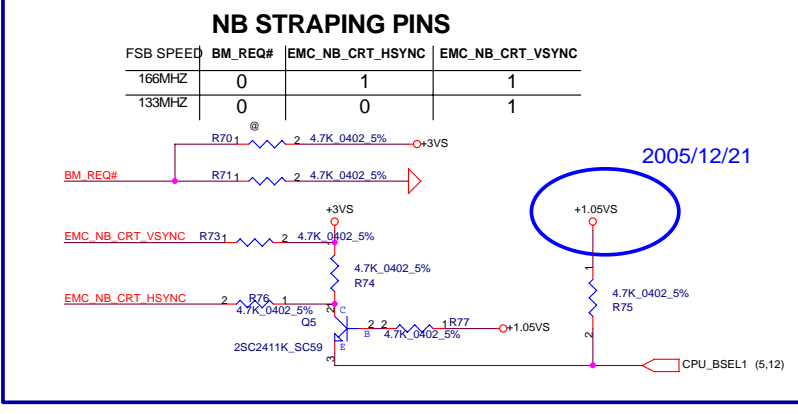
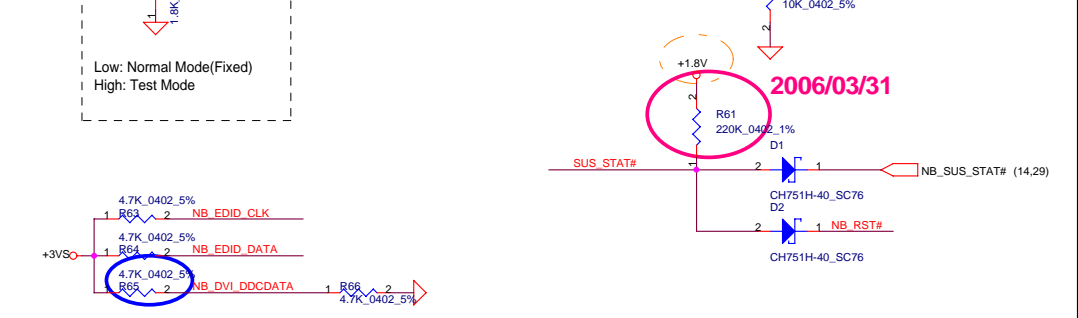
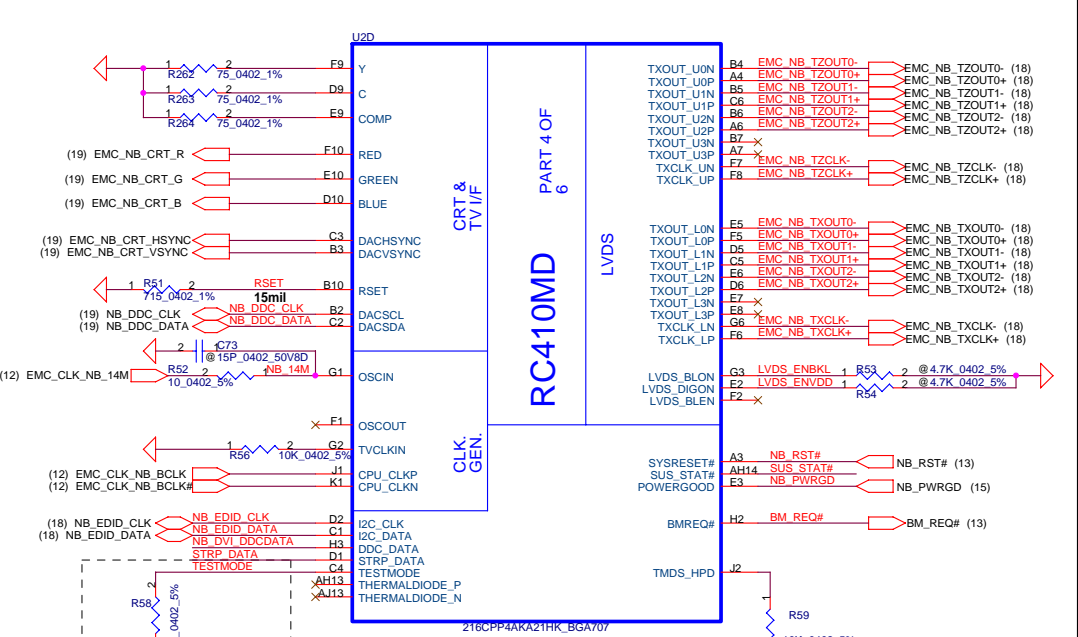
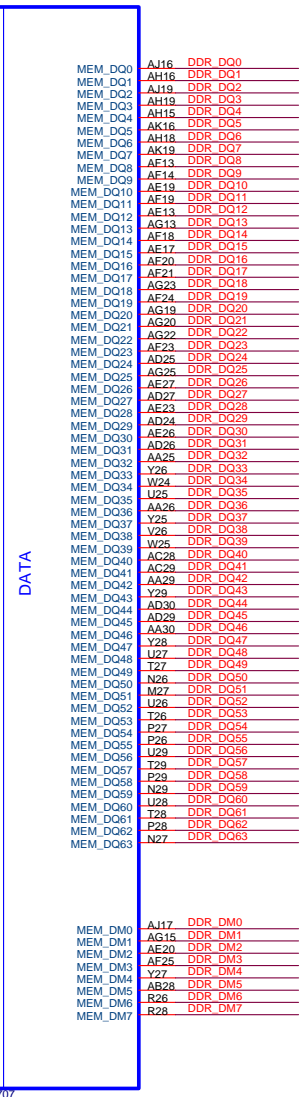


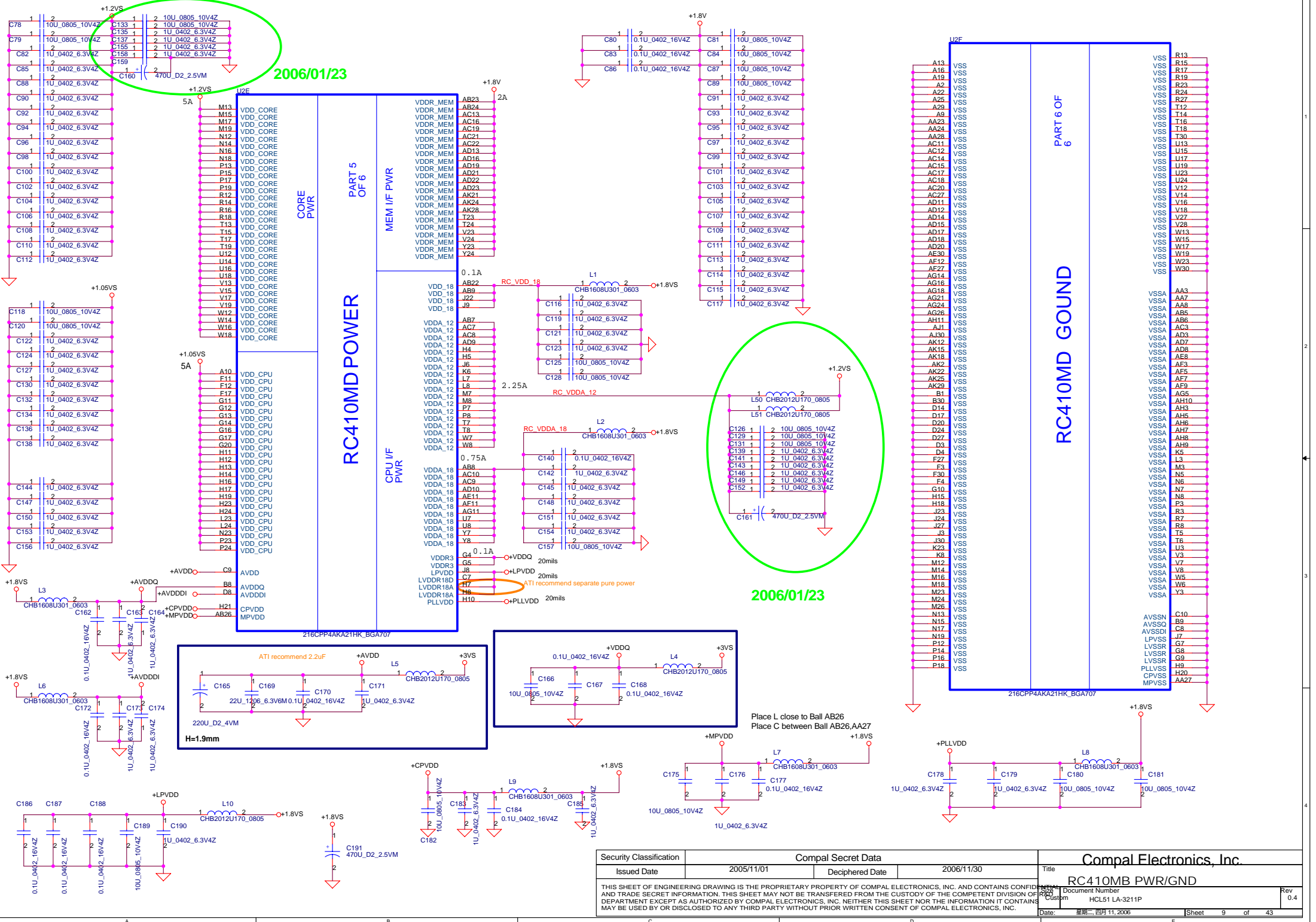
To SB A-PCIE Link

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Document Number	HCL51 LA-3211P		Rev	0.4
Date	星期二, 四月 11, 2006	Sheet	7	of 43



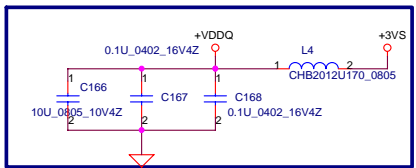
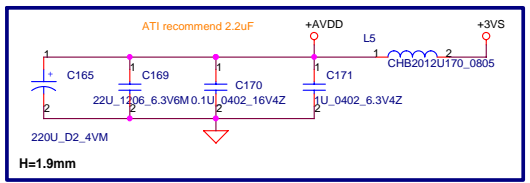
RC410MD MEMORY I/F





2006/01/23

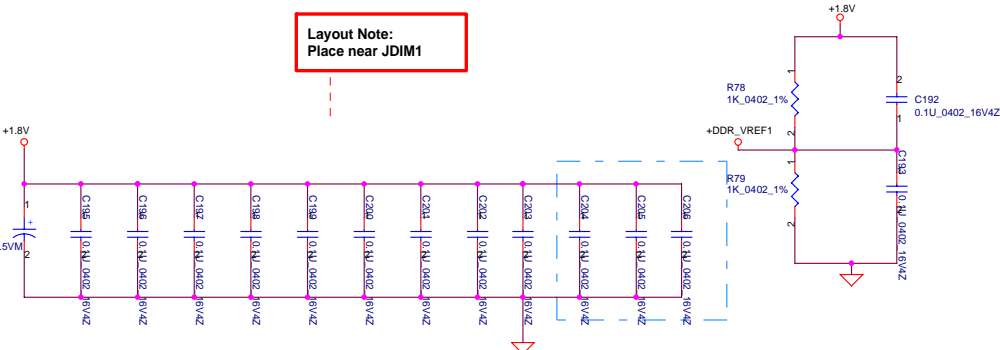
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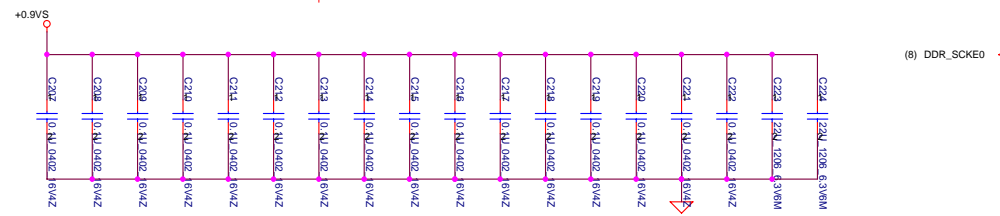
Place L close to Ball AB26
Place C between Ball AB26,AA27

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Issued Date	2005/11/01	Deciphered Date	2006/11/30	RC410MB PWR/GND
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Document Number	HCL51-LA-3211P		Rev	0.4
Date	星期二, 四月 11, 2006	Sheet	9	of 43

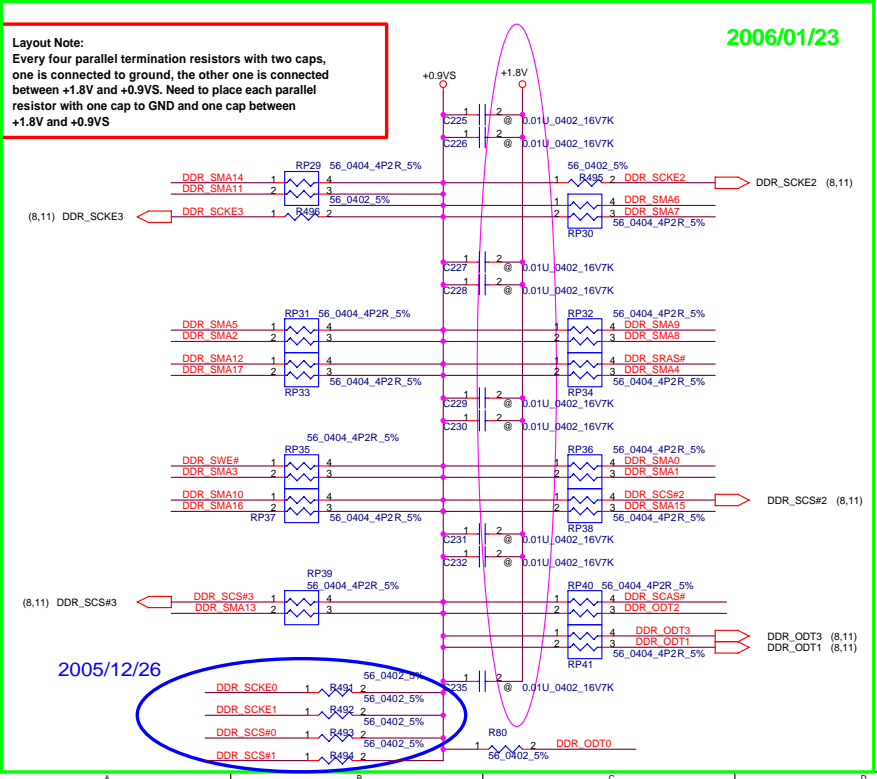
Layout Note:
Place near JDIM1



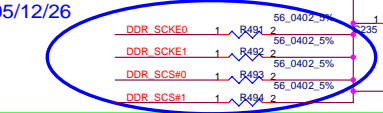
Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF



Layout Note:
Every four parallel termination resistors with two caps, one is connected to ground, the other one is connected between +1.8V and +0.9VS. Need to place each parallel resistor with one cap to GND and one cap between +1.8V and +0.9VS



2006/01/23



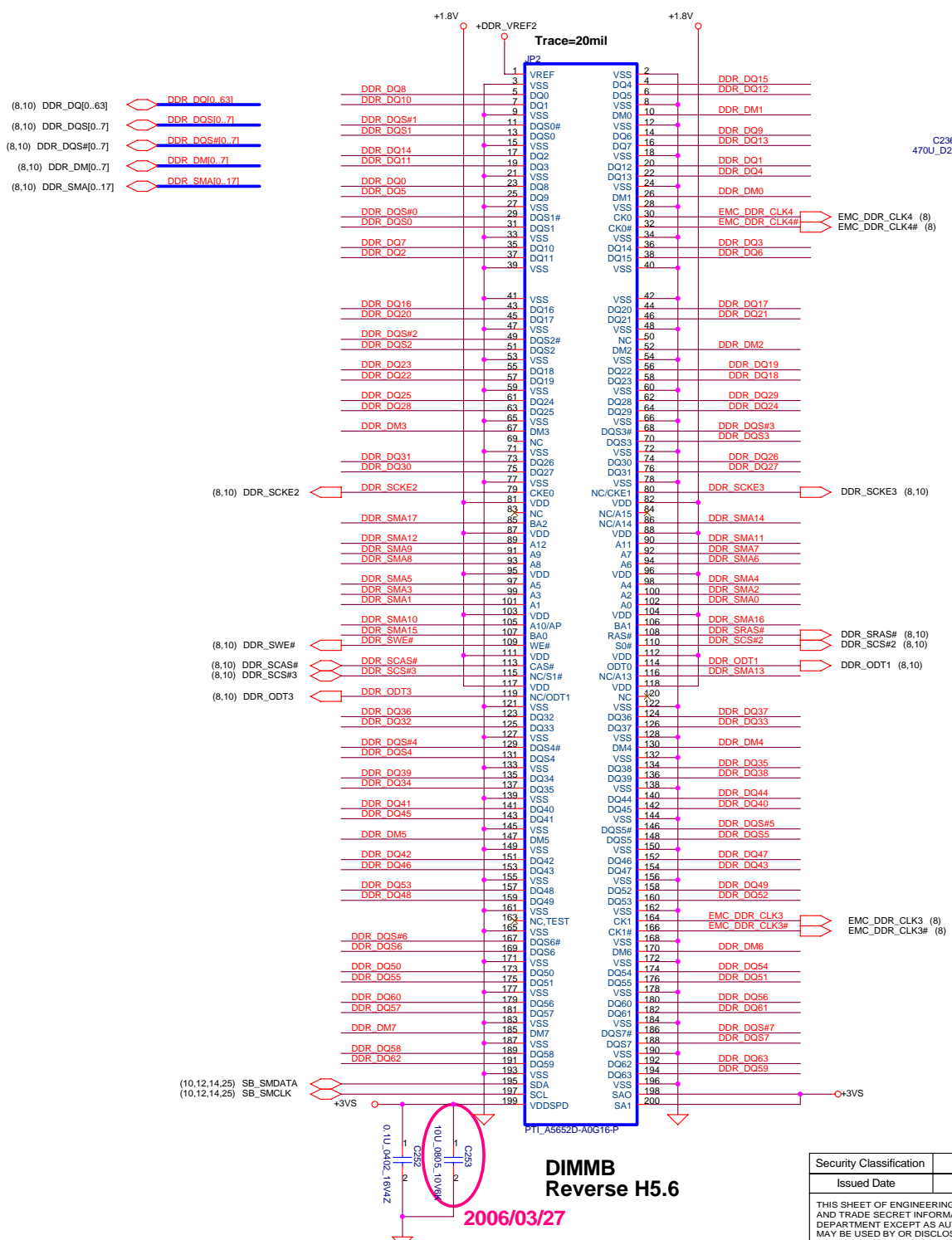
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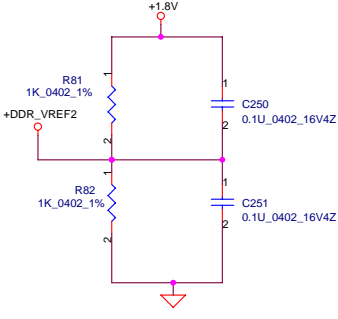
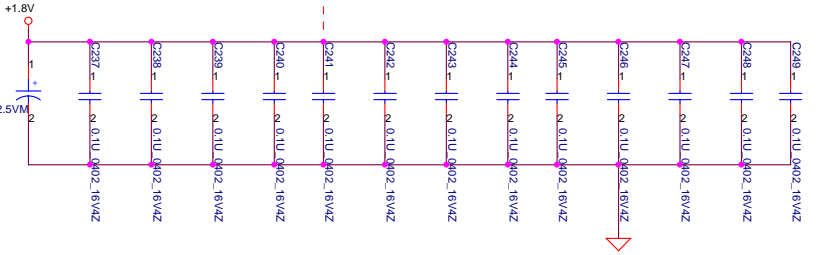
DIMM Reverse H9.2

2006/03/27

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Date:	星期二, 四月 11, 2006	Sheet	10 of 43



Layout Note:
Place near JDIM1

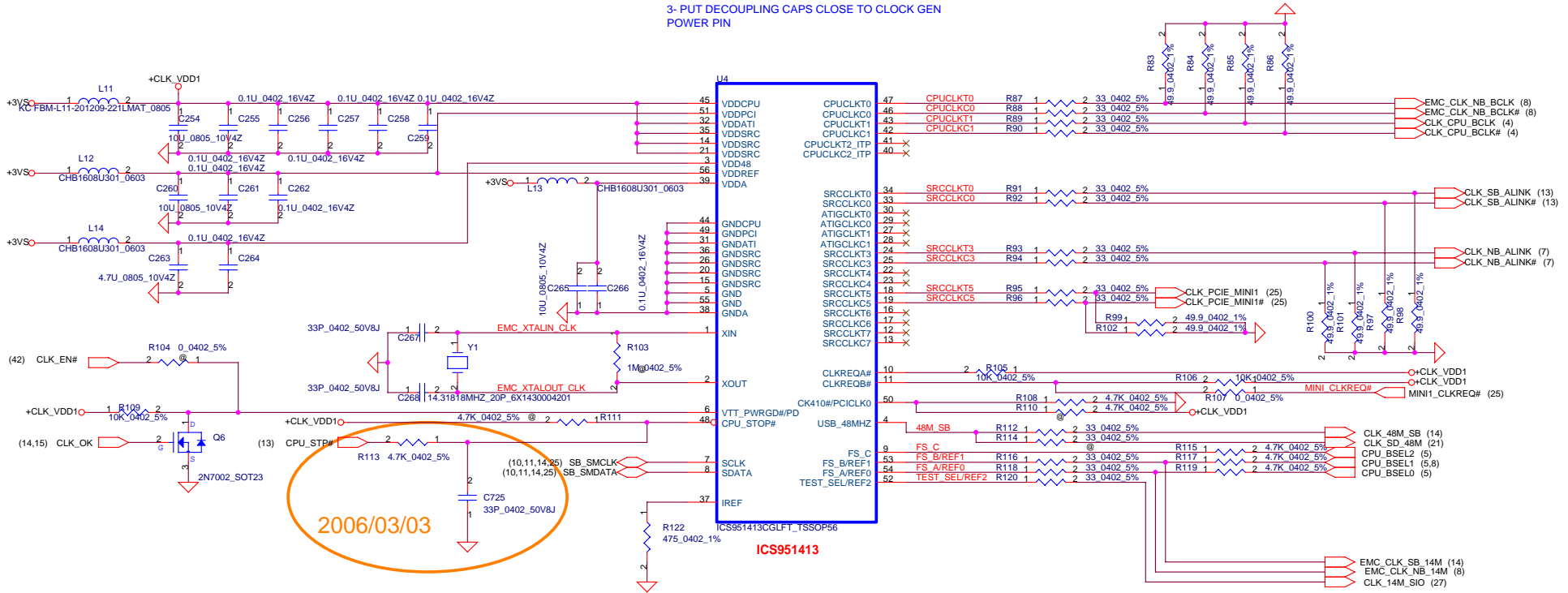


(10,12,14,25) SB_SMDATA
(10,12,14,25) SB_SMCLK

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				DDR-II SODIMM1
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Date:	星期二, 四月 11, 2006	Sheet	11	of 43

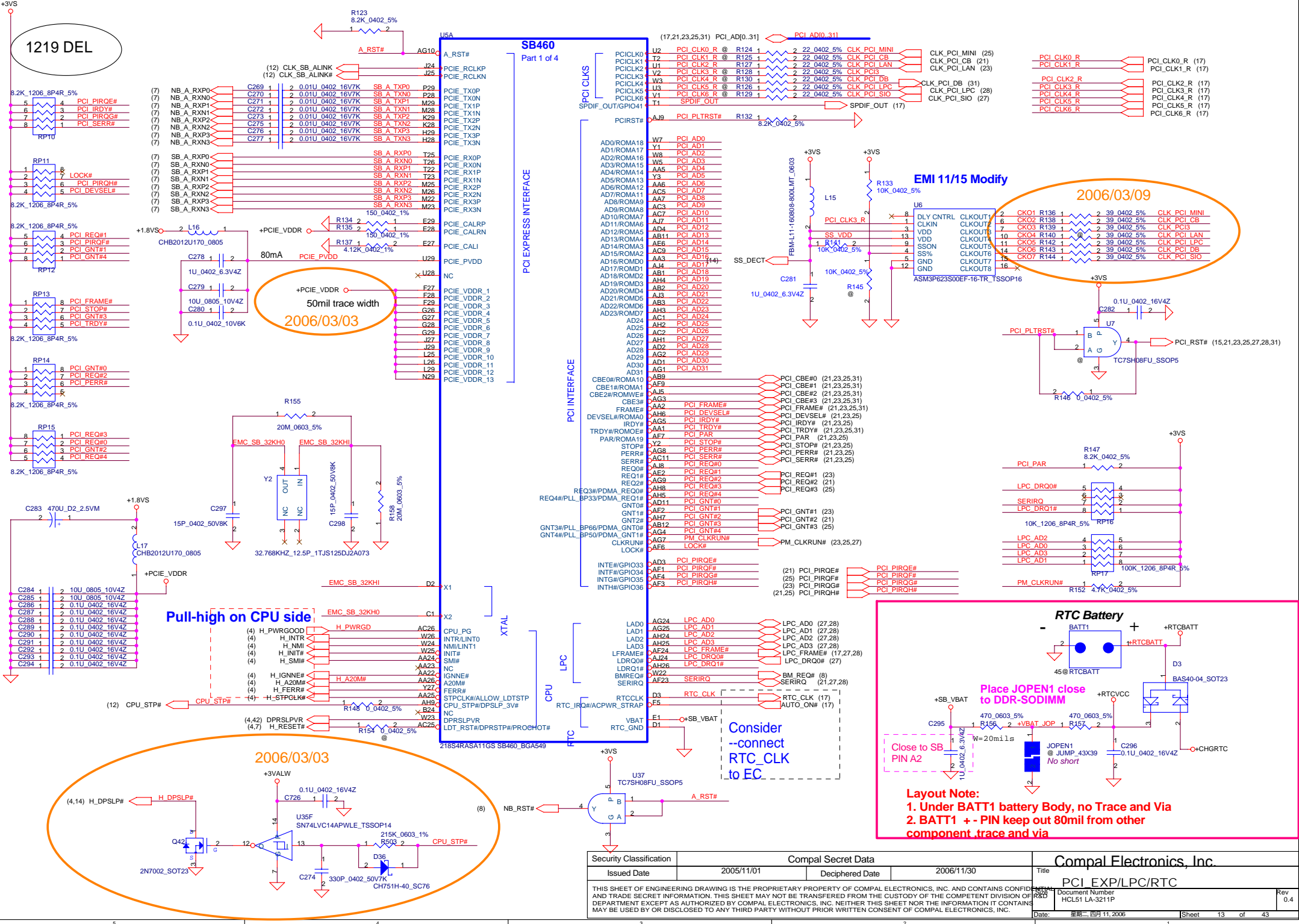
Clock Generator

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK#, NBCLK#, ITPCLK# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

1219 DEL



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Date	星期二, 四月 11, 2006	Sheet	13	of 43	

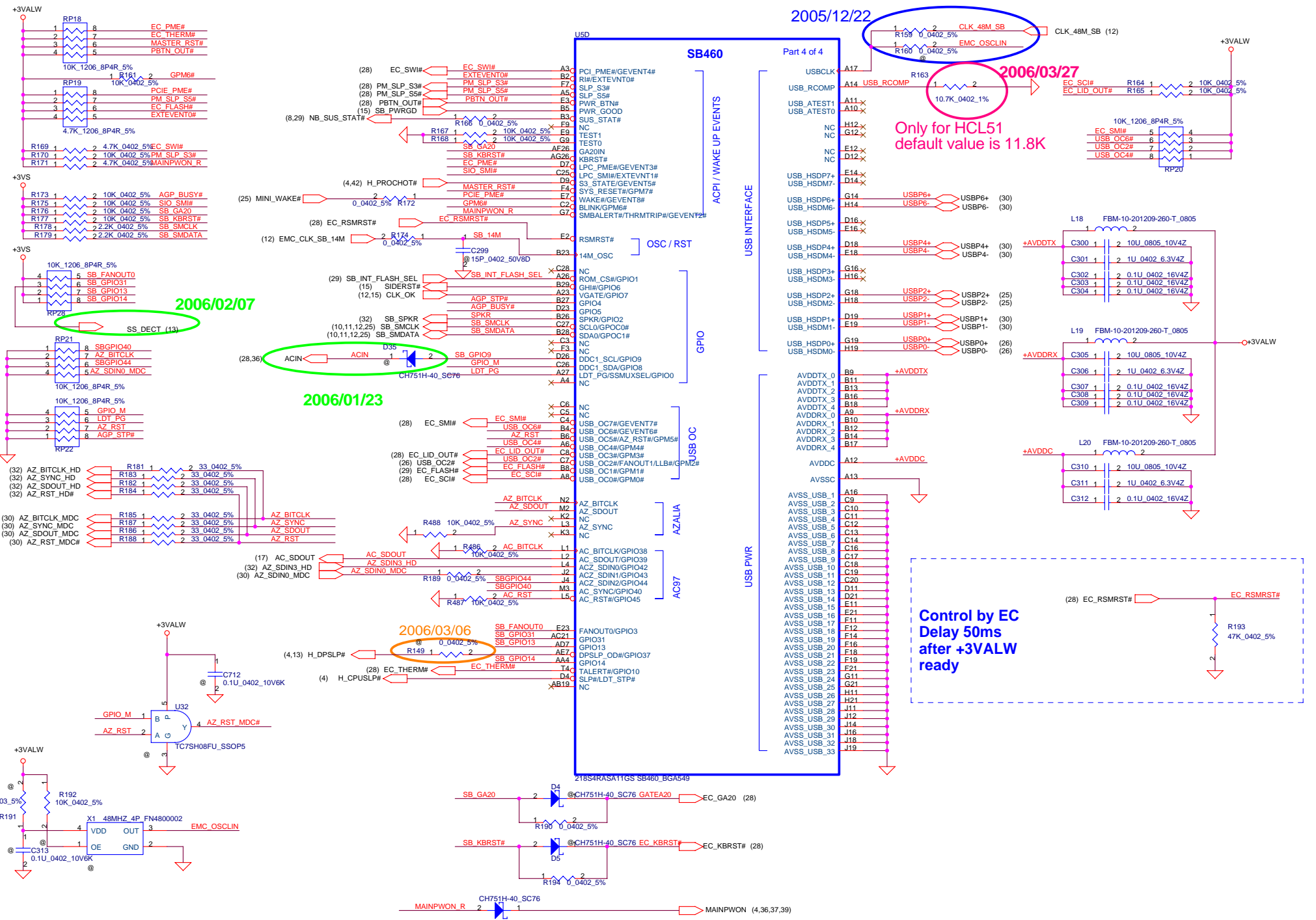
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2006/03/27

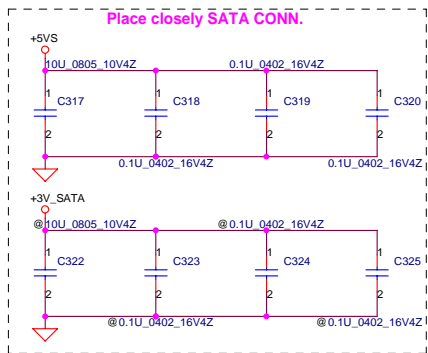
2006/02/07

2006/01/23

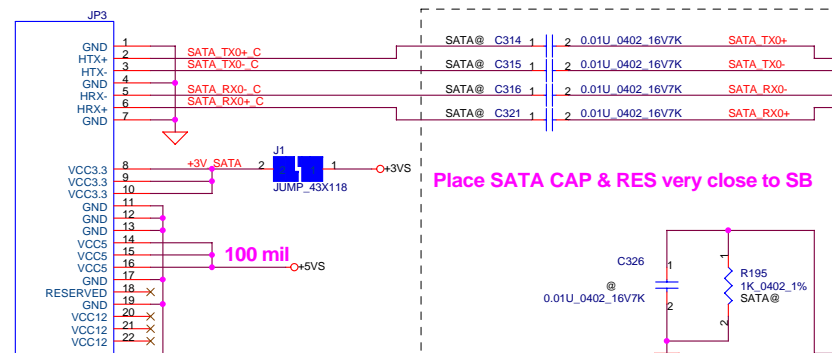
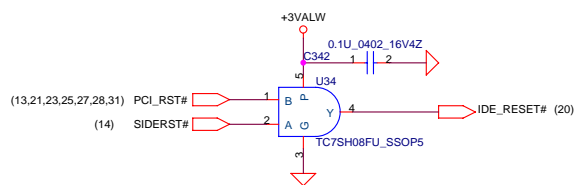
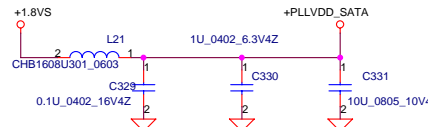
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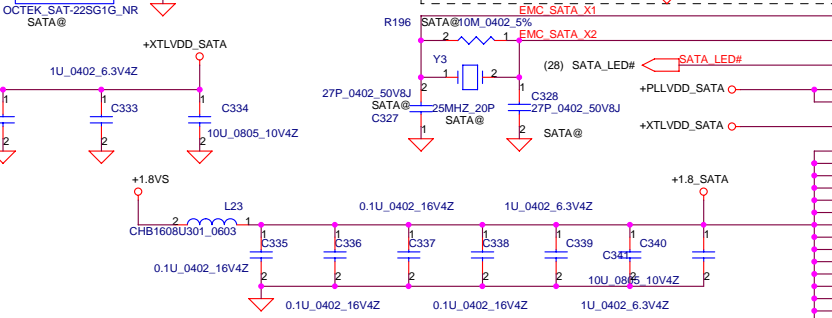
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Document Number	HCL51 LA-3211P	Rev	0.4	Date	星期二, 四月 11, 2006
Sheet	14	of	43		



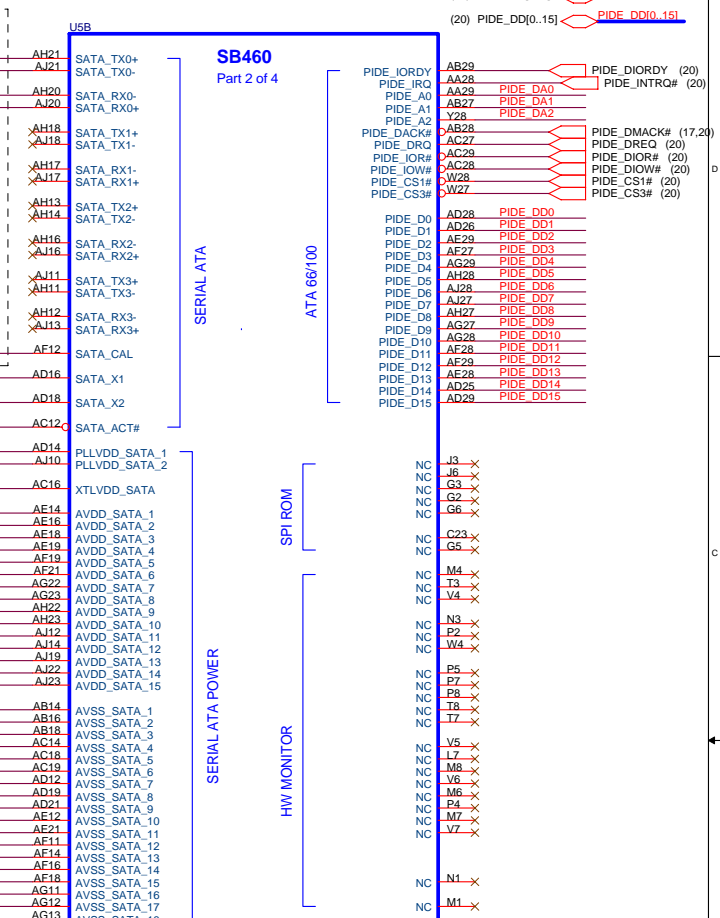
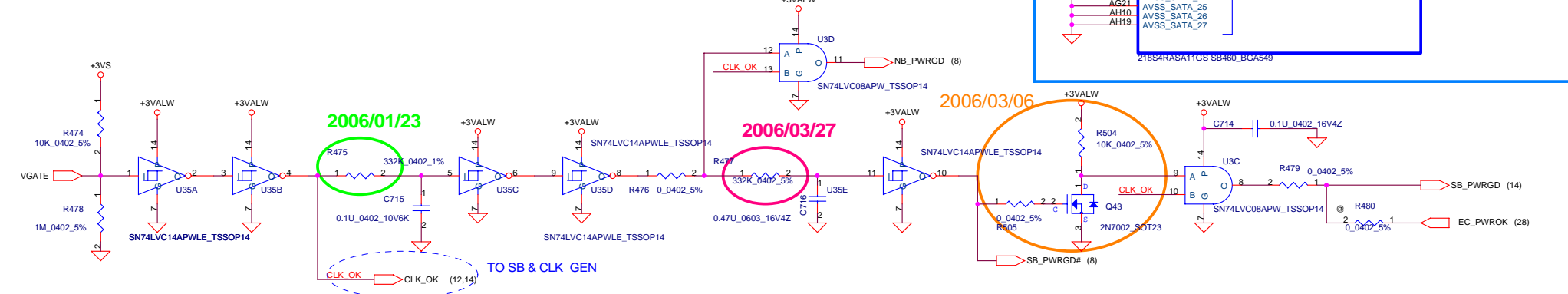
SATA HDD CONNECTOR



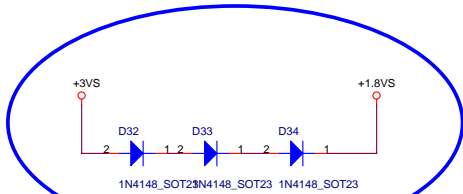
Place SATA CAP & RES very close to SB



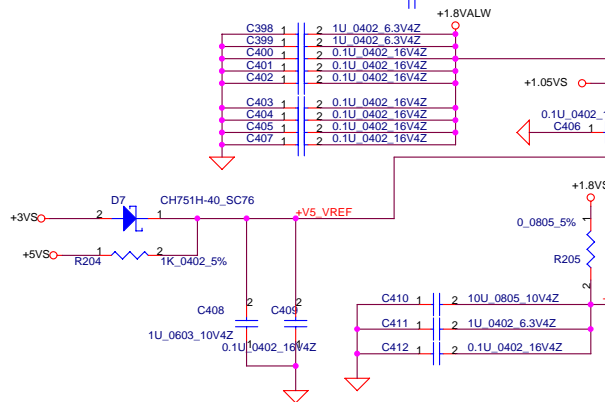
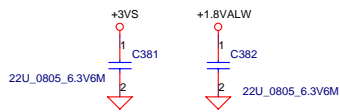
NB & SB POWER GOOD



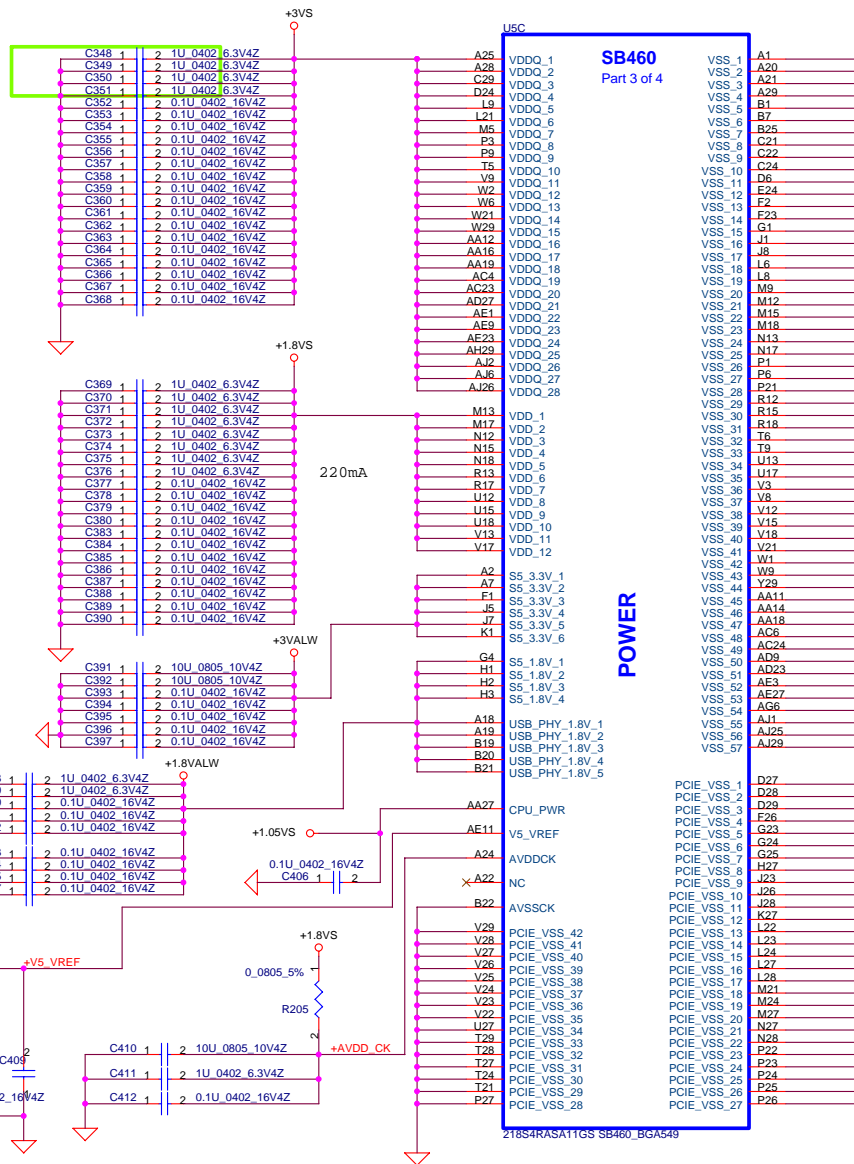
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Date: 星期二, 四月 11, 2006				Rev 0.4



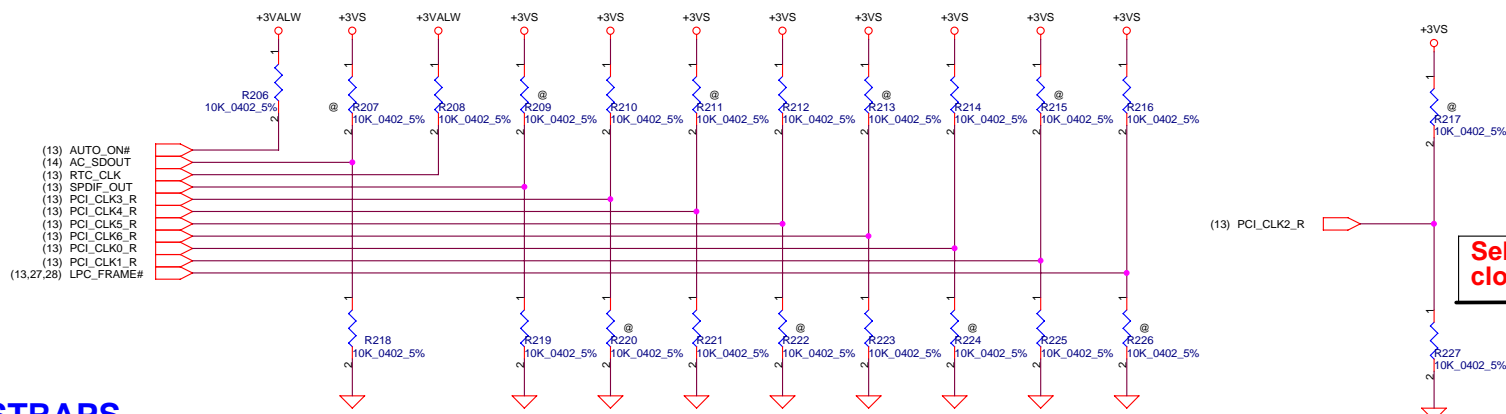
2005/12/21



+V5_VREF (20mils)
+AVDD_CK(40mils)



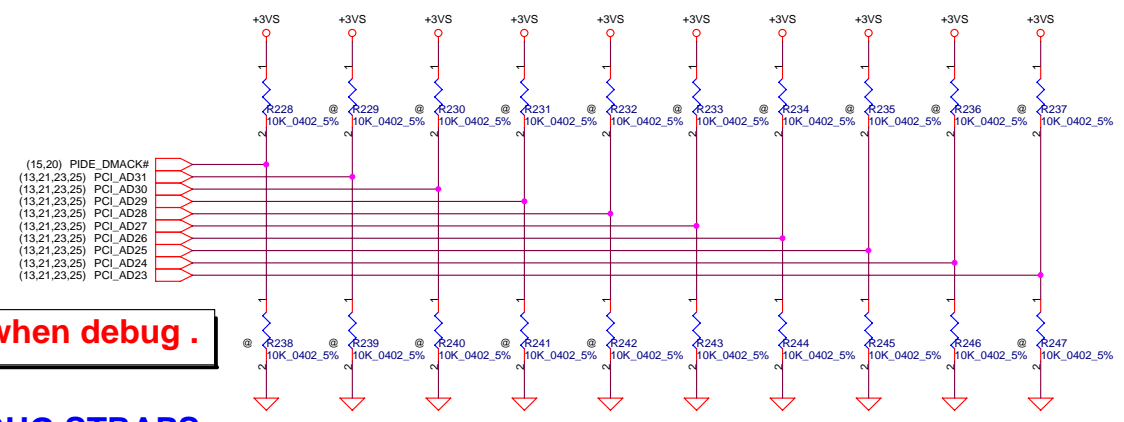
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Date: 星期二, 四月 11, 2006				Sheet 16 of 43



REQUIRED STRAPS



	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI4	CLK_PCI5	PCI_CLK6	PCI_CLK0	PCI_CLK1	LFRAME#	CLK_PCI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL	PCIE AUTO detect DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM		THERMTRIP# ENABLE DEFAULT	Crystal Pad
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE	External Clock DEFAULT	Forcing PCIE to 2 lanes (debug only)	CPU I/F = P4 DEFAULT	H,L = LPC ROM I L,H = LPC ROM II L,L = FWH ROM		THERMTRIP# DISABLE DEFAULT	Clock input buffer DEFAULT



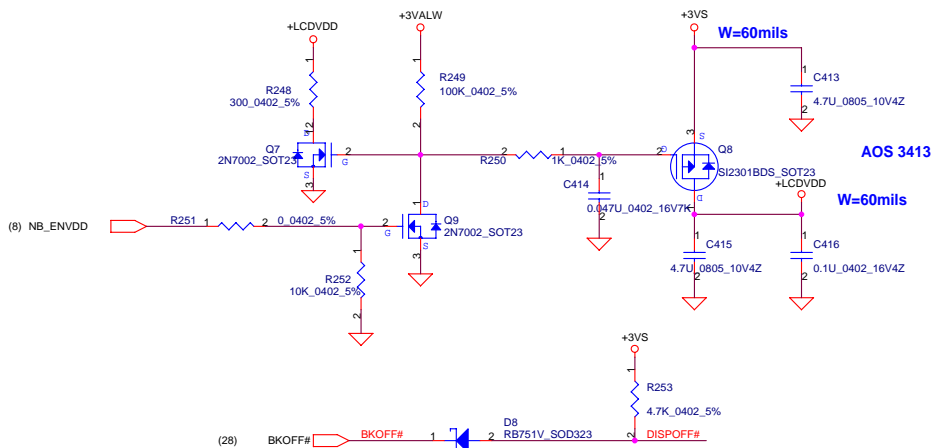
Pop R634 when debug .

DEBUG STRAPS

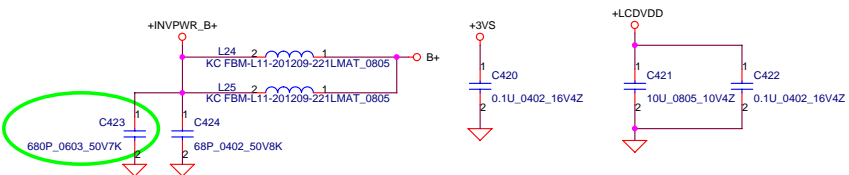
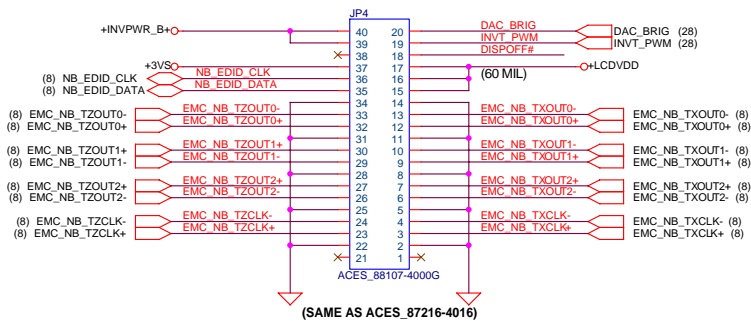
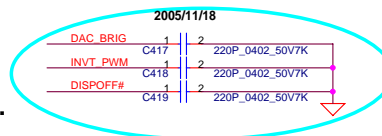
	PIDE_DMACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

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				HARDWARE TRAP
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Document Number	Rev			
Custom HCL51 LA-3211P	0.4			
Date: 星期三, 四月 11, 2006	Sheet 17	of 43		

LCD POWER CIRCUIT

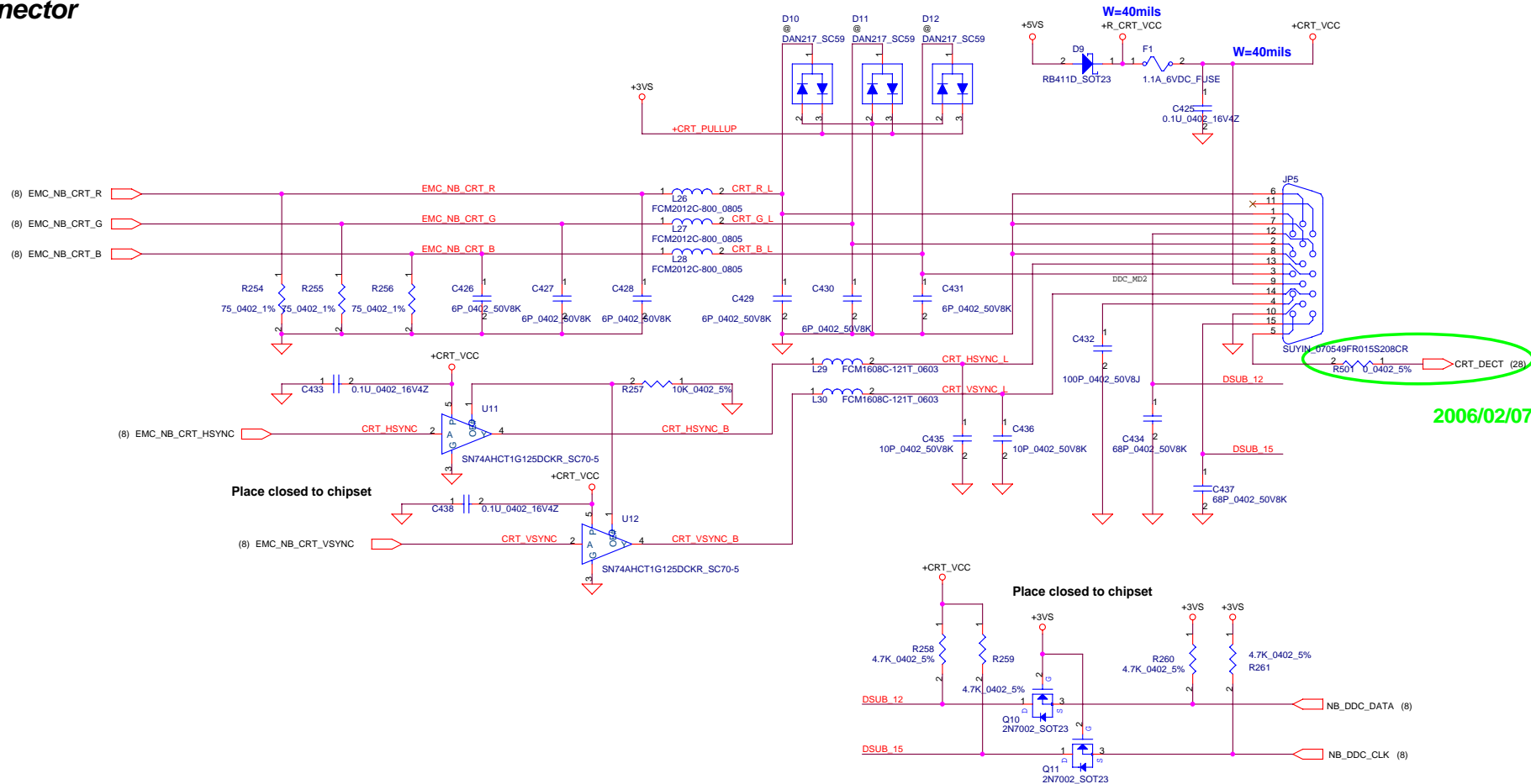


LCD/PANEL BD. Conn.



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				HCL51 LA-3211P
				Rev 0.4
				Date: 2006年04月11日
				Sheet 18 of 43

CRT Connector



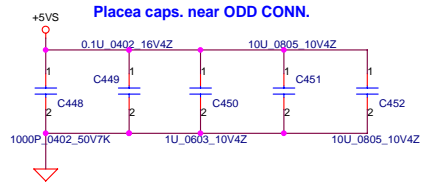
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Document Number
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Date: 星期二, 四月 11, 2006				Sheet 19 of 43

Compal Electronics, Inc.

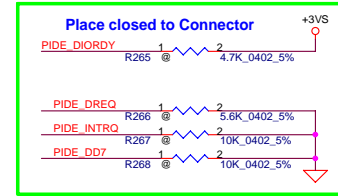
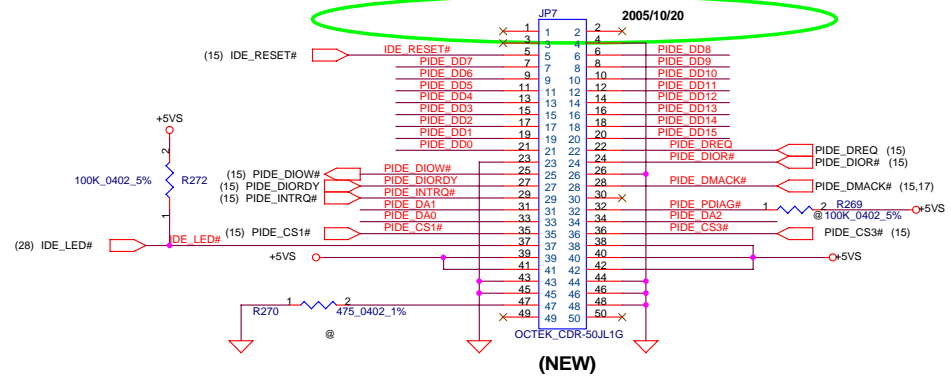
CRT & TV-OUT Connector

HCL51 LA-3211P

Rev 0.4

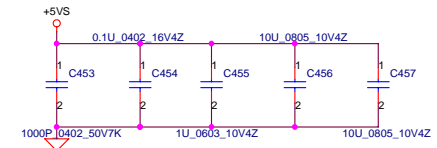


ODD Conn.

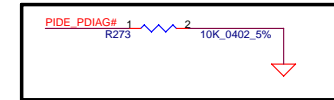
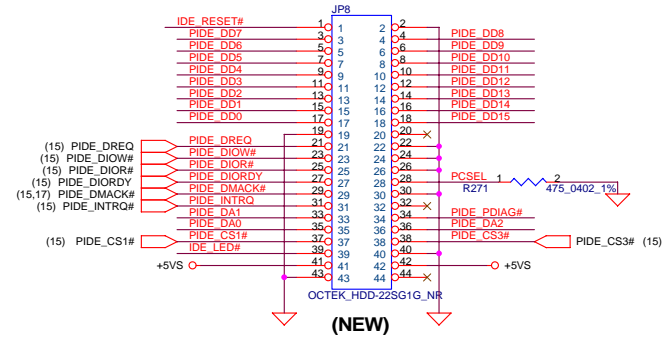


(15) PIDE_DA[0..2] \hookrightarrow PIDE_DA[0..2]

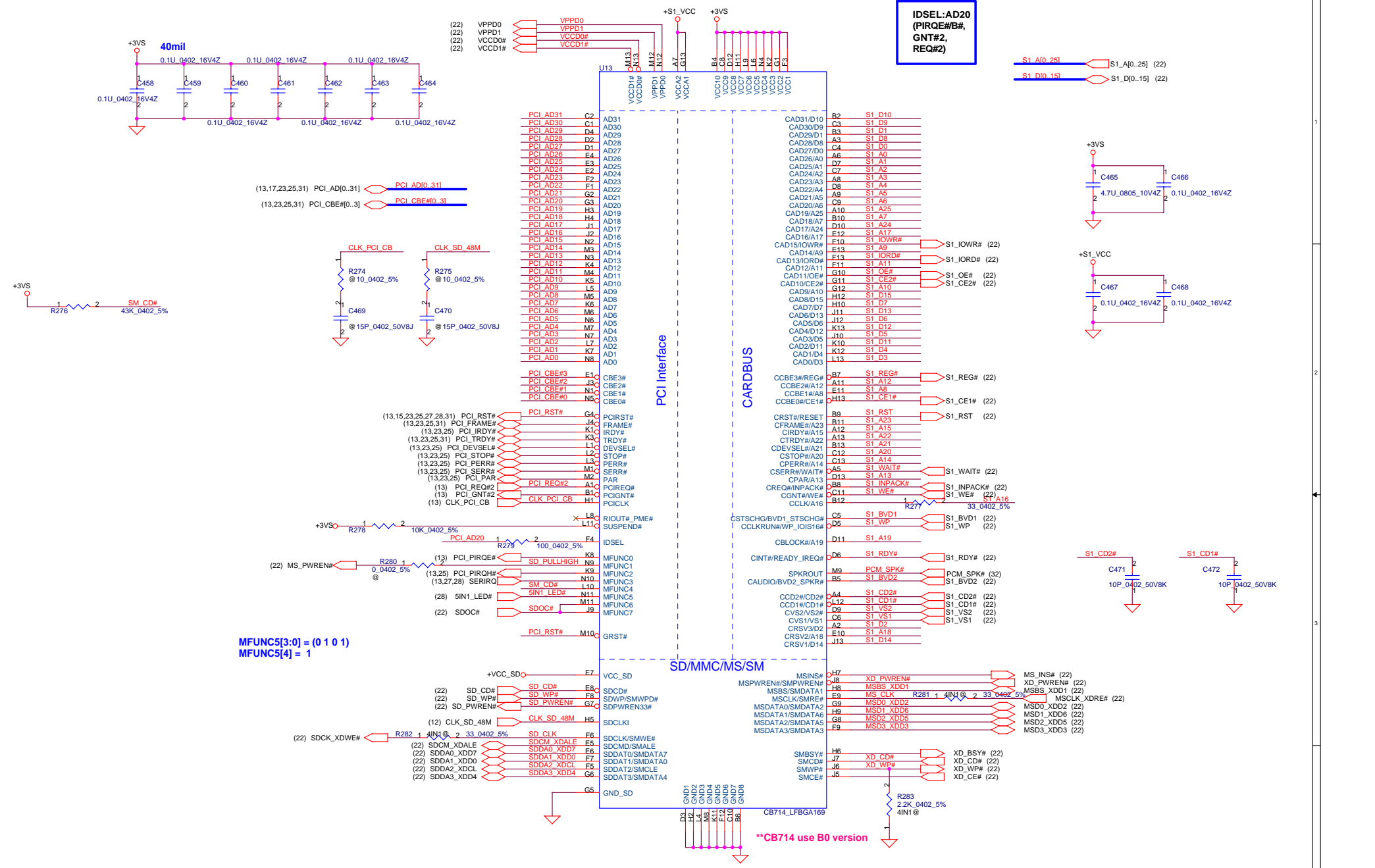
(15) PIDE_DD[0..15] \hookrightarrow PIDE_DD[0..15]



PATA HDD Conn.

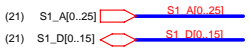
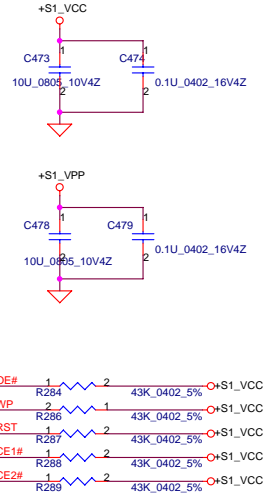
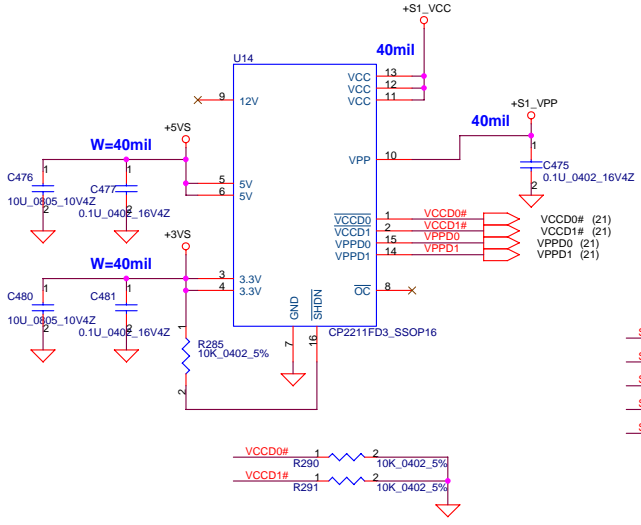


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			HCL51 LA-3211P	0.4
			Date: 星期二, 四月 11, 2006	Sheet 20 of 43

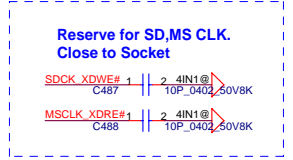
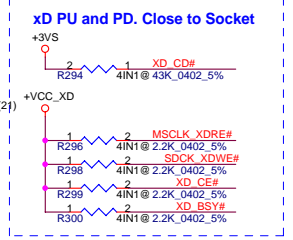
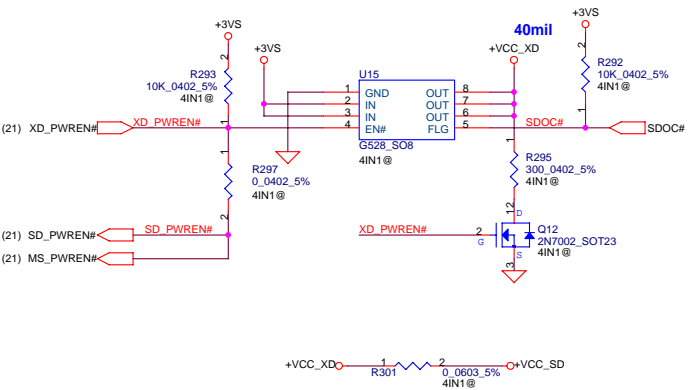


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				Rev 0.4 Sheet 21 of 43

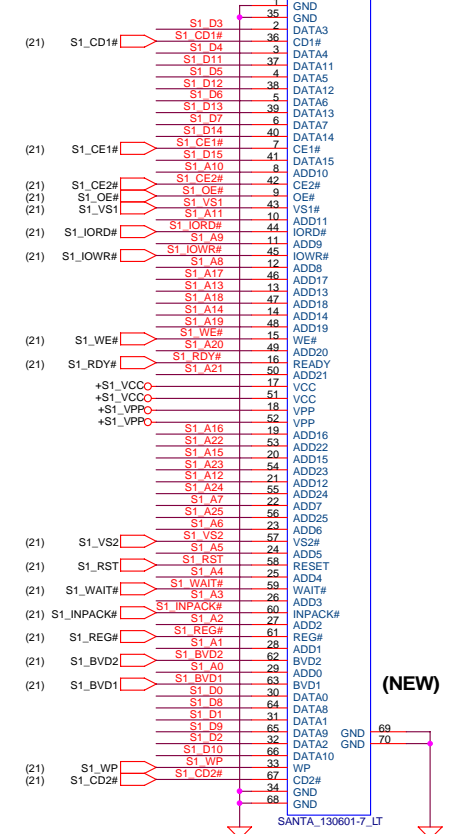
PCMCIA Power Control



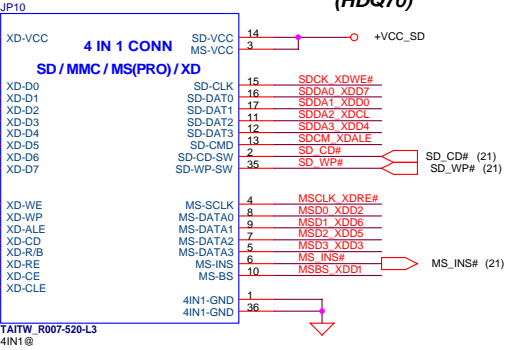
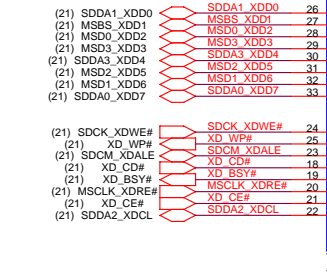
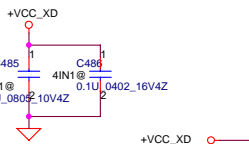
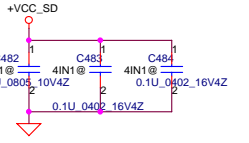
SD/MS Power Control XD Power Control



PCMCIA Socket



4 IN 1 Socket (HDQ70)



(13,17,21,25,31) PCI_AD[0..31] PCI_AD[0..31]

**IDSEL:AD22
(PIRQG#,
GNT#1,
REQ#1)**

- PCI AD0 104
- PCI AD1 103
- PCI AD2 102
- PCI AD3 98
- PCI AD4 97
- PCI AD5 96
- PCI AD6 95
- PCI AD7 93
- PCI AD8 90
- PCI AD9 89
- PCI AD10 87
- PCI AD11 86
- PCI AD12 85
- PCI AD13 83
- PCI AD14 82
- PCI AD15 79
- PCI AD16 58
- PCI AD17 58
- PCI AD18 57
- PCI AD19 55
- PCI AD20 53
- PCI AD21 50
- PCI AD22 49
- PCI AD23 47
- PCI AD24 43
- PCI AD25 42
- PCI AD26 40
- PCI AD27 39
- PCI AD28 37
- PCI AD29 36
- PCI AD30 34
- PCI AD31 33

- (13,21,25,31) PCI_CBE#0
- (13,21,25,31) PCI_CBE#1
- (13,21,25,31) PCI_CBE#2
- (13,21,25,31) PCI_CBE#3
- PCI AD22 LAN IDSEL
- (13,21,25) PCI_PAR
- (13,21,25,31) PCI_FRAME#
- (13,21,25) PCI_IRDY#
- (13,21,25,31) PCI_TRDY#
- (13,21,25) PCI_DEVSEL#
- (13,21,25) PCI_STOP#
- (13,21,25) PCI_PERR#
- (13,21,25) PCI_SERR#
- (13) PCI_REQ#1
- (13) PCI_GNT#1
- (13) PCI_PIRQG#
- (25,28) LAN_PME#
- (13,15,21,25,27,28,31) PCI_RST#
- (13) CLK_PCI_LAN
- (13,25,27) PM_CLKRUN#

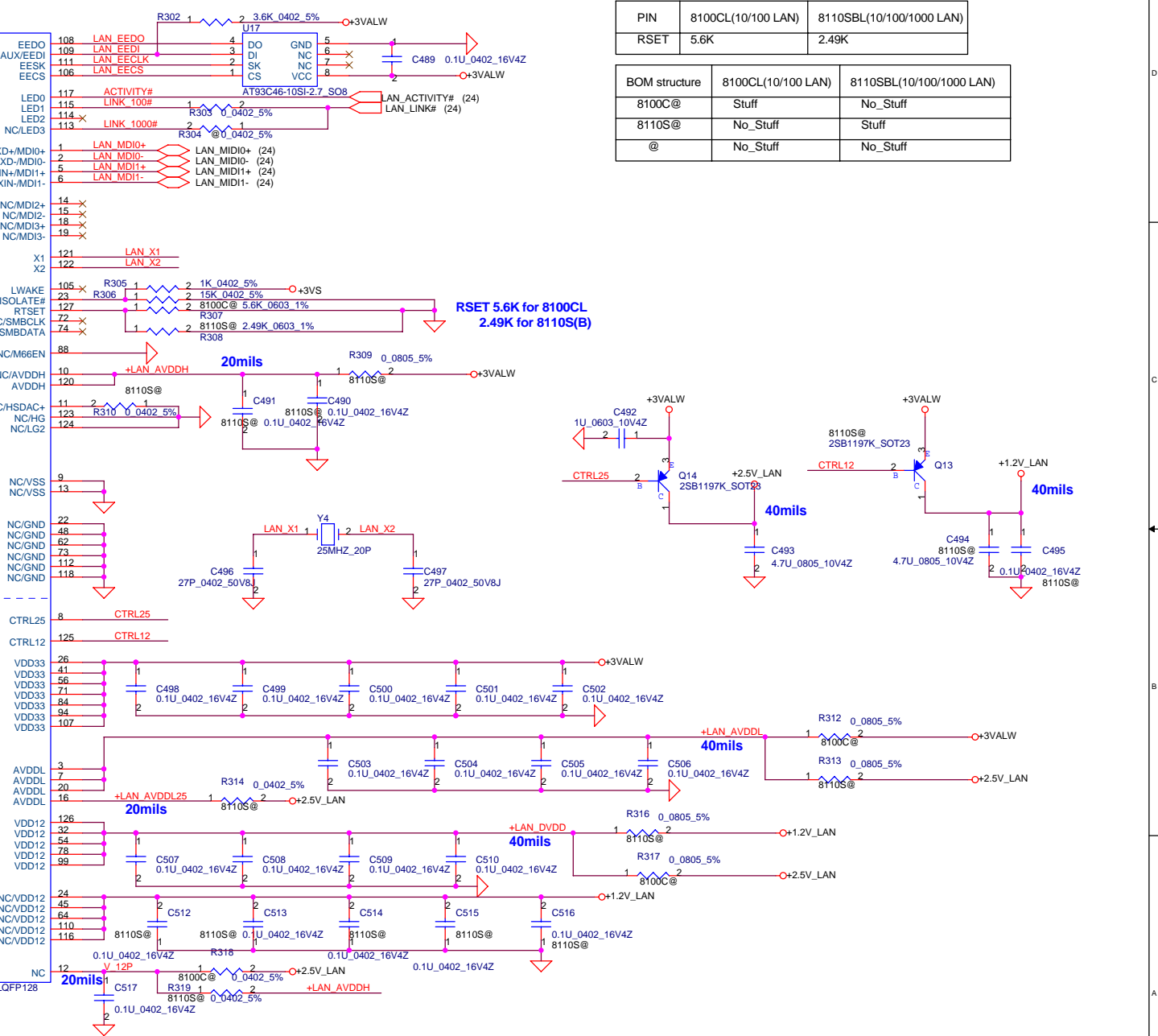
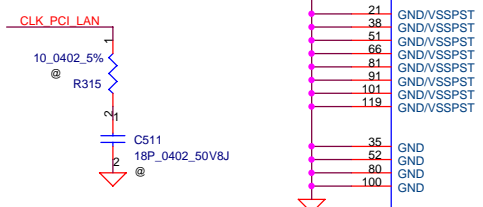
PCI I / F

LAN I / F

Power

PIN	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
RSET	5.6K	2.49K

BOM structure	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
8100C@	Stuff	No_Stuff
8110S@	No_Stuff	Stuff
@	No_Stuff	No_Stuff



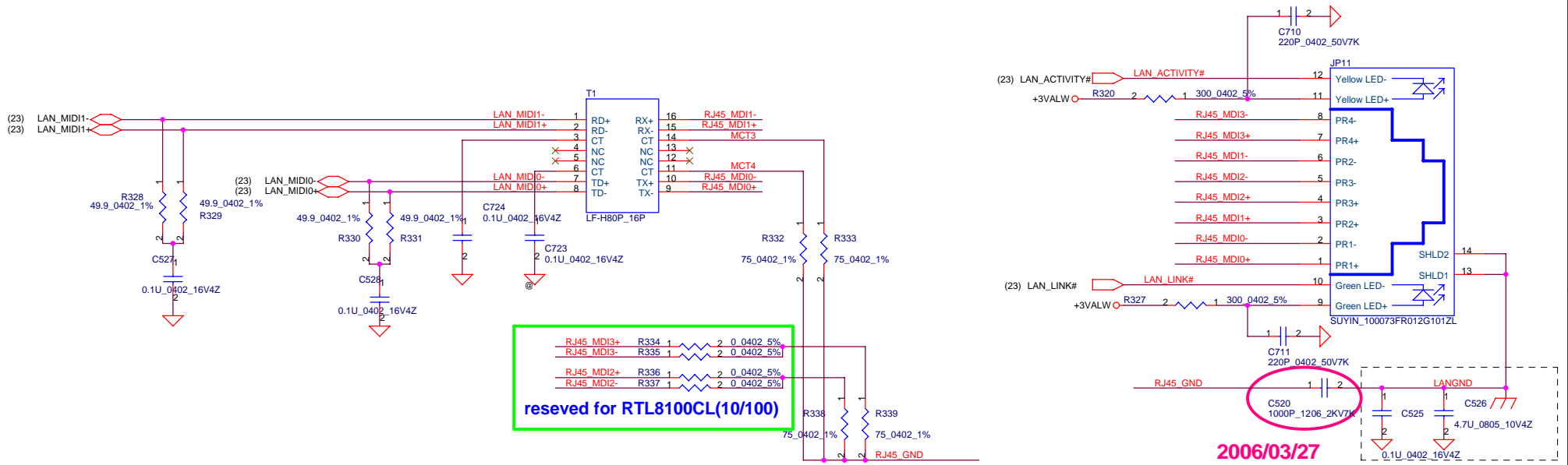
RTL8110SBL change to Ver.D

8100CL(10/100 LAN) P/N:SA081000310 ver.A.2

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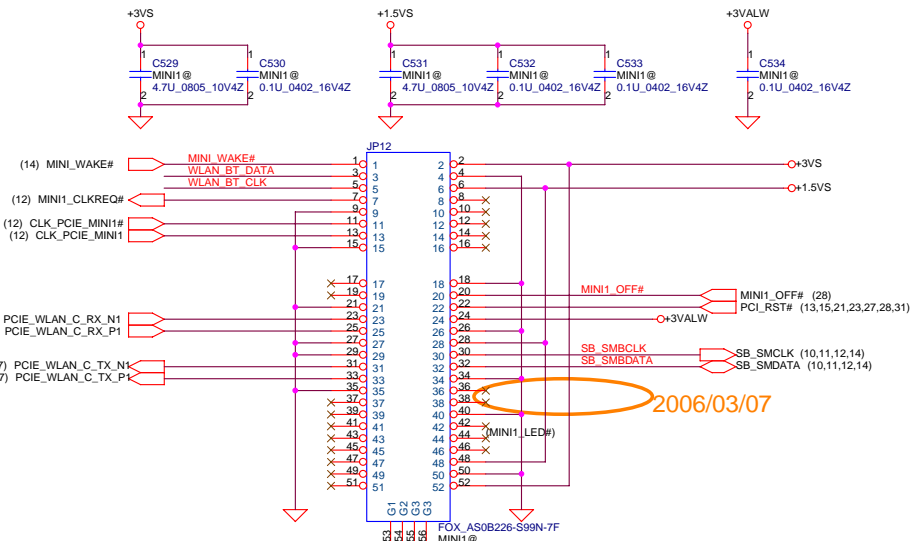
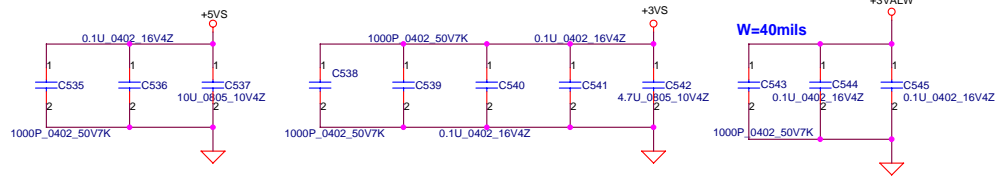
Compal Electronics, Inc.		
LAN RTL8110SBL		
Title	Document Number	Rev
	HCL51 LA-3211P	0.4
Date:	星期二, 四月 11, 2006	Sheet 23 of 43

LAN RTL8100CL

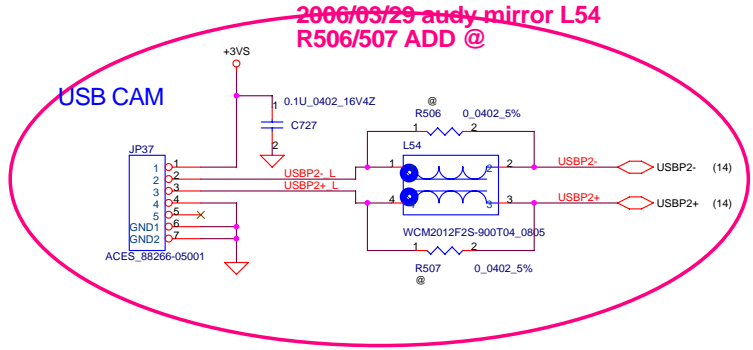
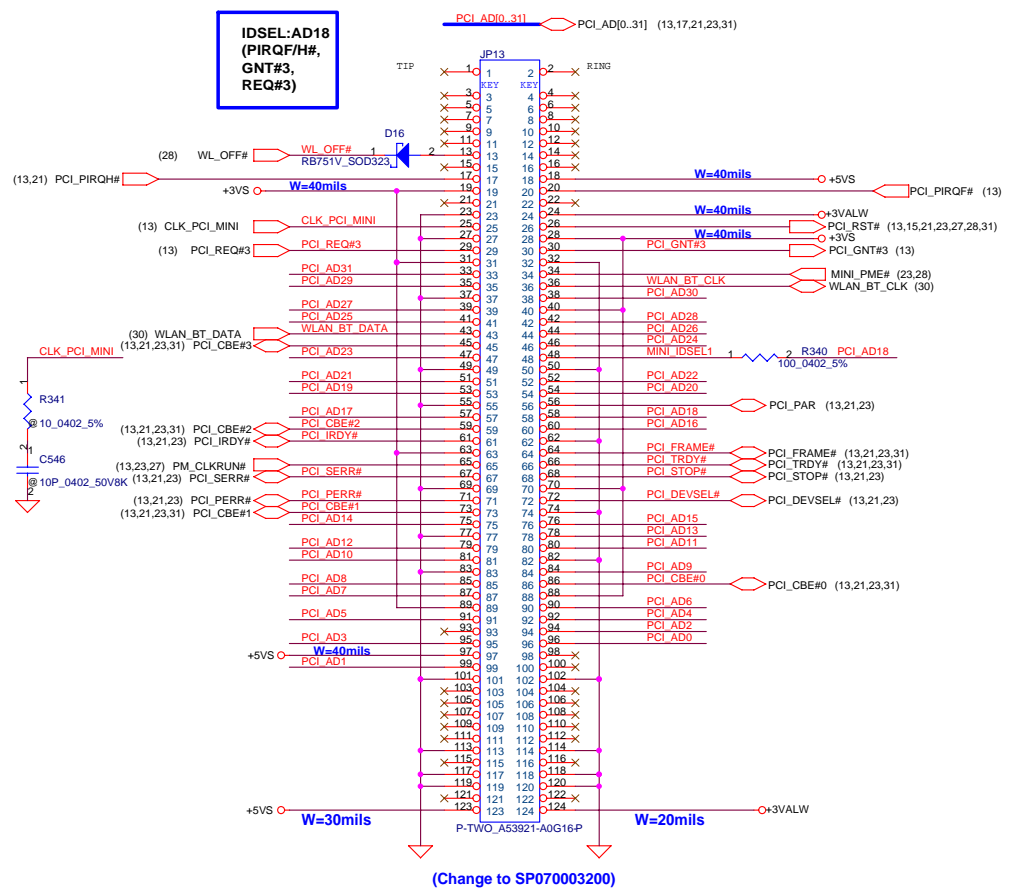


2006/03/27

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				Rev 0.4
				Sheet 24 of 43



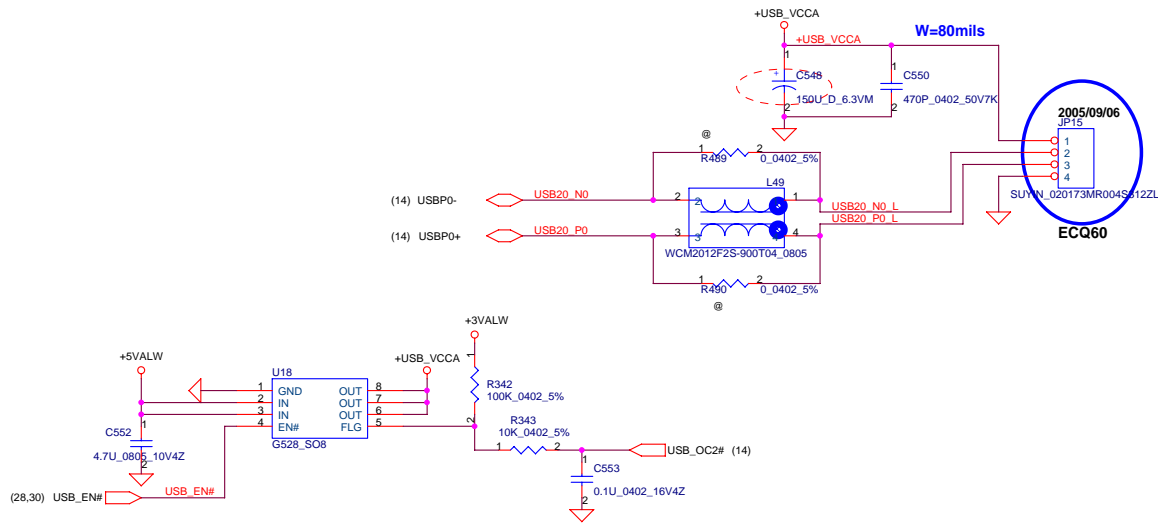
**IDSEL:AD18
(PIRQF/H#,
GNT#3,
REQ#3)**



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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Date: 星期二, 四月 11, 2006				Rev 0.4
Sheet 25 of 43				

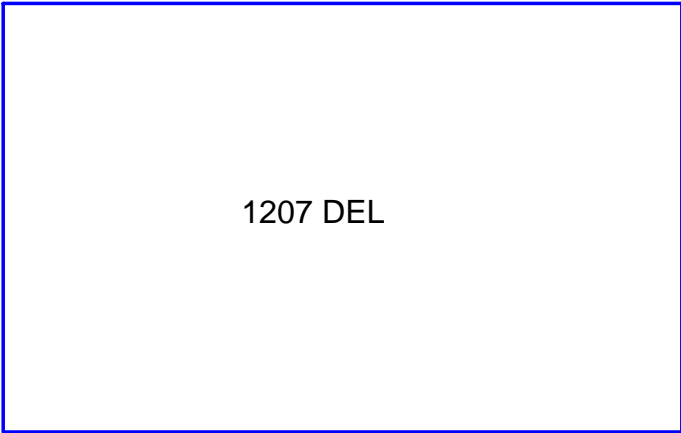
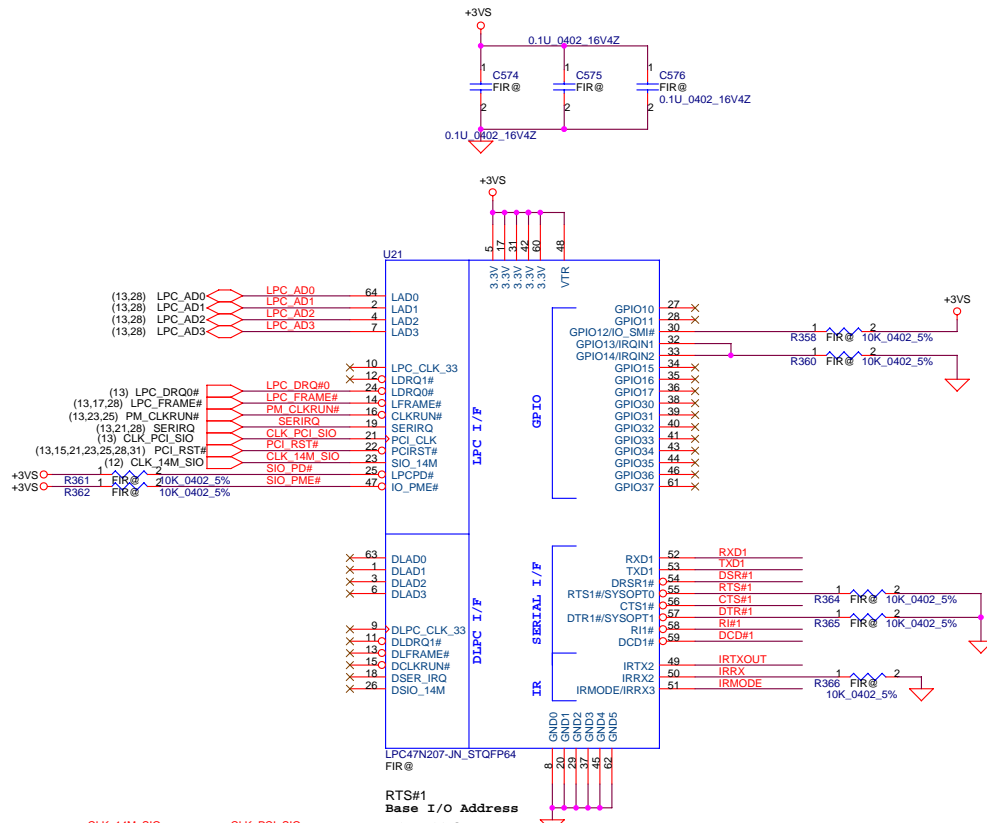
USB CONN. 1 & 2



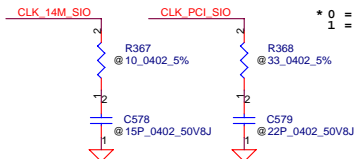
1207 DEL

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Date: 星期二, 四月 11, 2006			Document Number	Rev
			HCL51 LA-3211P	0.4
			Sheet 26 of 43	

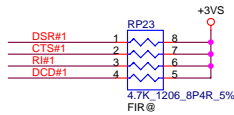
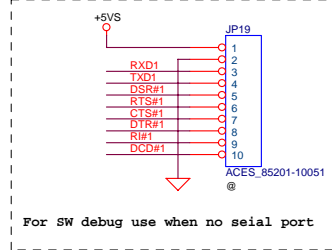
SUPER I/O SMsC LPC47N207



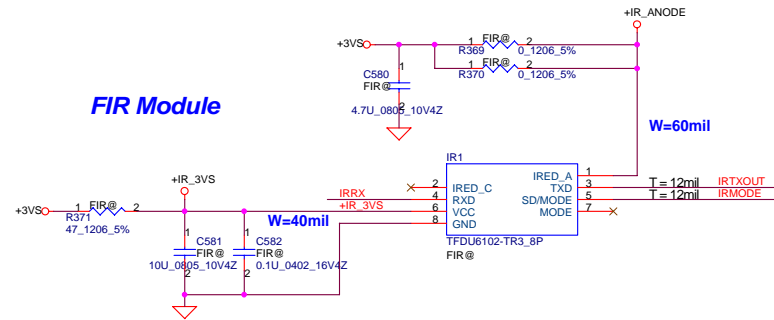
RTS#1
Base I/O Address
* 0 = 02Eh
1 = 04Eh



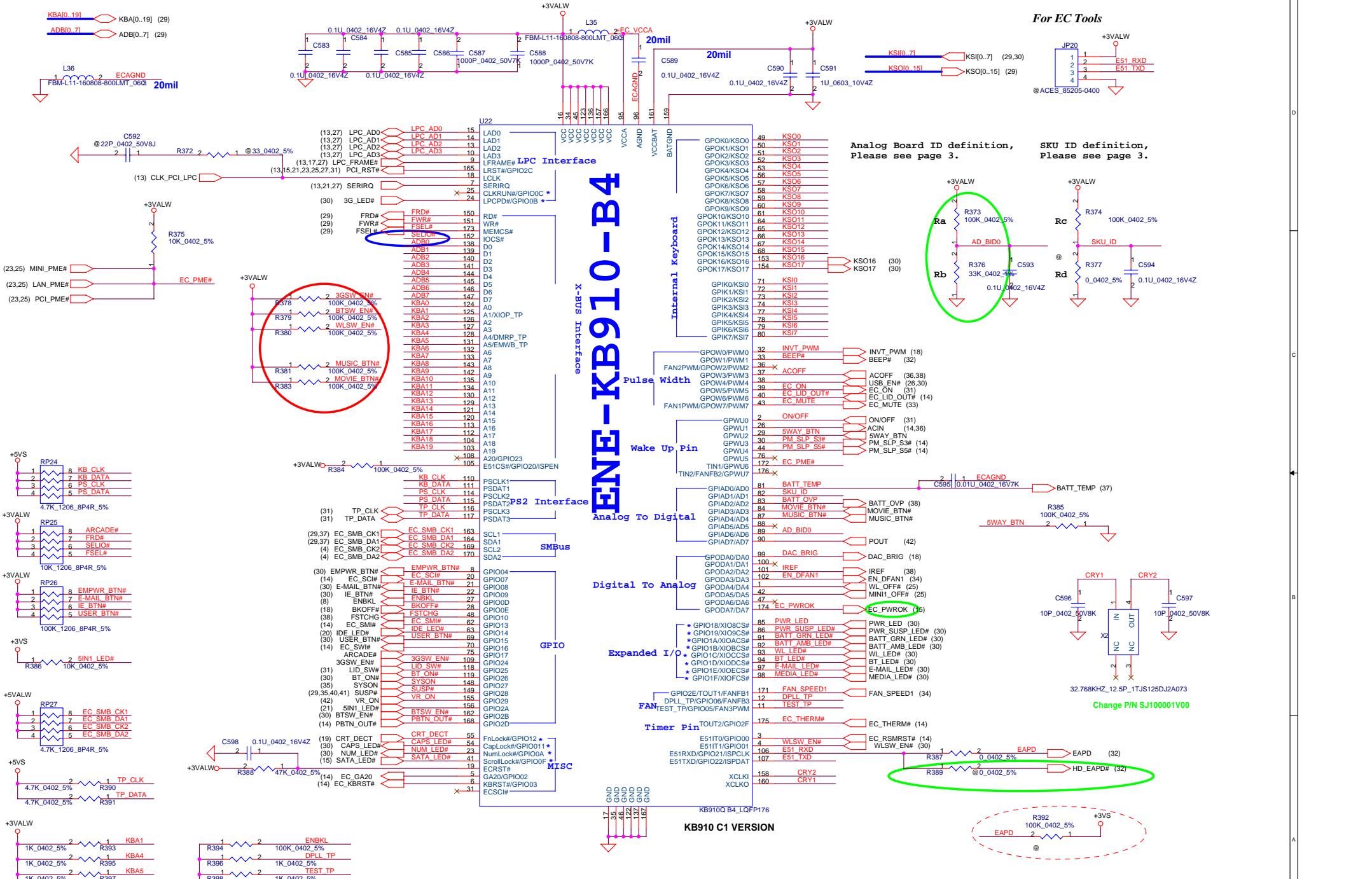
Place on the BOT side (near MINIPCI conn.)



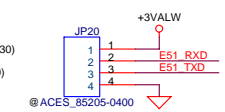
FIR Module



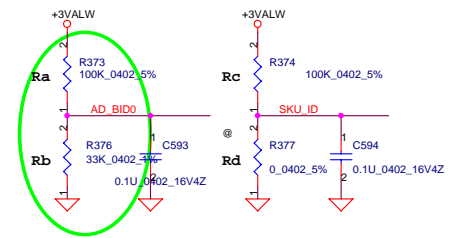
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	SIO1036 & FIR
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Date: 星期二, 四月 11, 2006				Sheet 27 of 43



For EC Tools

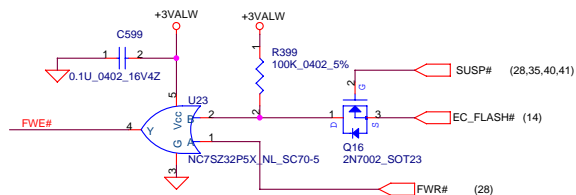


Analog Board ID definition, Please see page 3.
SKU ID definition, Please see page 3.

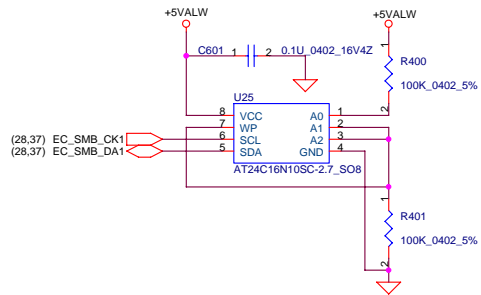


ENE-KB910-B4
 Internal Keyboard
 Pulse Width
 Wake Up Pin
 Analog To Digital
 Digital To Analog
 Expanded I/O
 Timer Pin
 MISC
 Internal Keyboard
 PS2 Interface
 SMBus
 GPIO
 MISC
 EC_VCCA
 ECAGND
 +3VALW
 EC_PME#
 EC_PWROK
 EC_THERM#
 EC_RSMRST#
 WLSW_EN#
 EC_PWROK
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 EC_PWROK
 EC_THERM#
 EC_RSMRST#
 WLSW_EN#

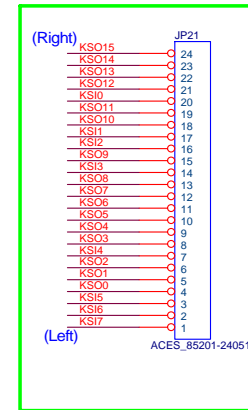
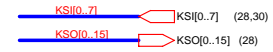
Security Classification	Compal Secret Data		Title
Issued Date	2005/06/20	Deciphered Date	
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			Rev 0.4 Sheet 28 of 43



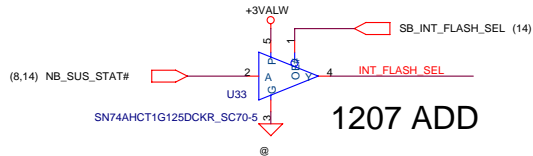
Check PCB Footprint



INT_KBD Conn.

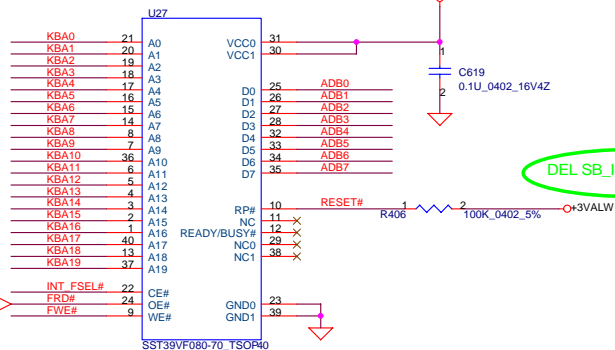
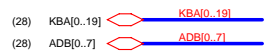


FOR DEBUG ONLY

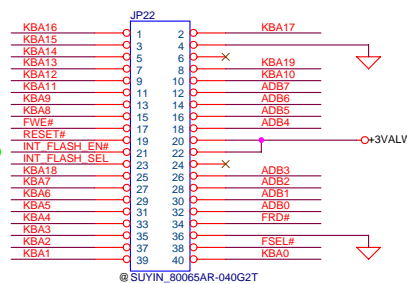


1207 ADD

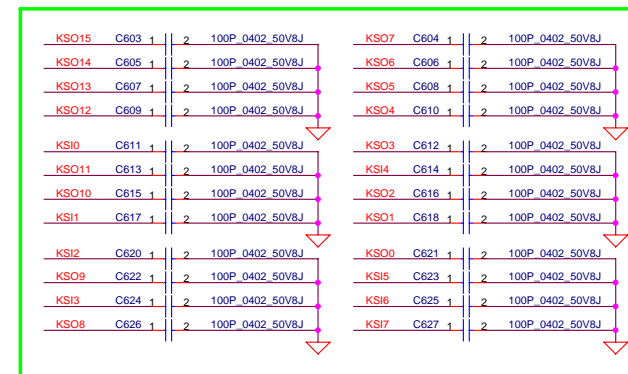
1MB Flash ROM



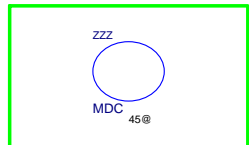
1MB ROM Socket



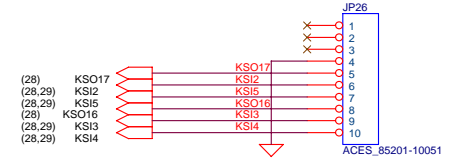
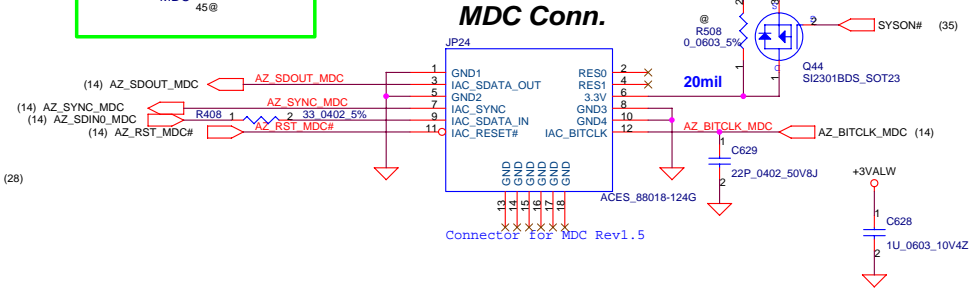
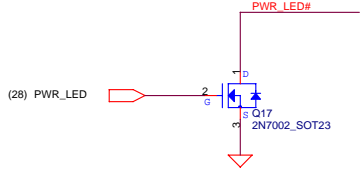
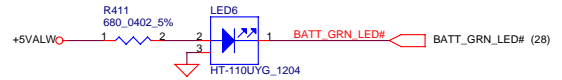
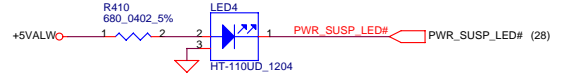
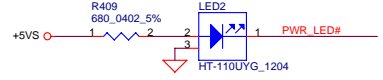
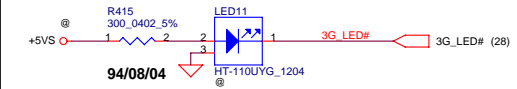
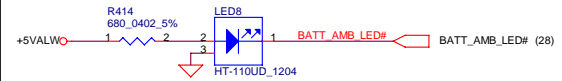
2006/01/23
DEL SB_INT_FLASH_SEL



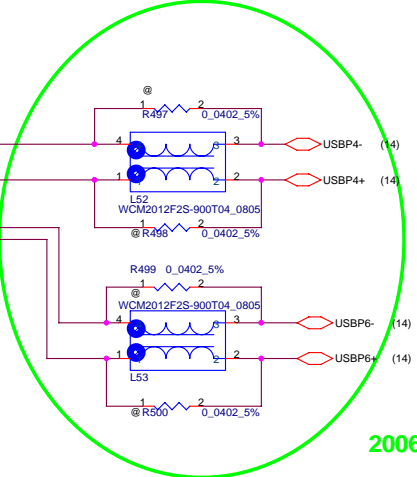
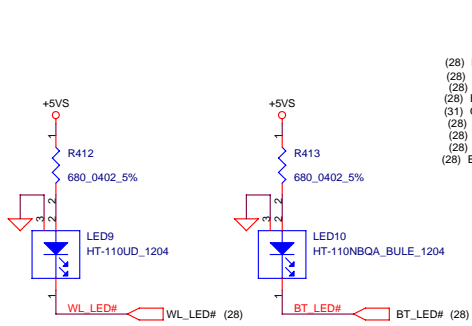
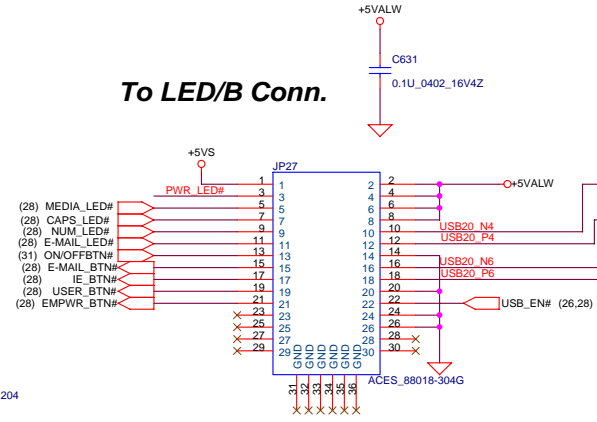
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	BIOS, I/O Port & K/B Connector	
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				HCL51 LA-3211P	0.4
Date: 星期二, 四月 11, 2006				Sheet	29 of 43



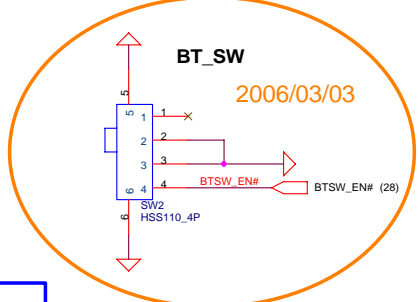
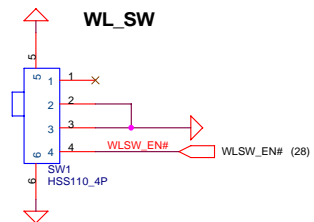
2006/01/23



To LED/B Conn.

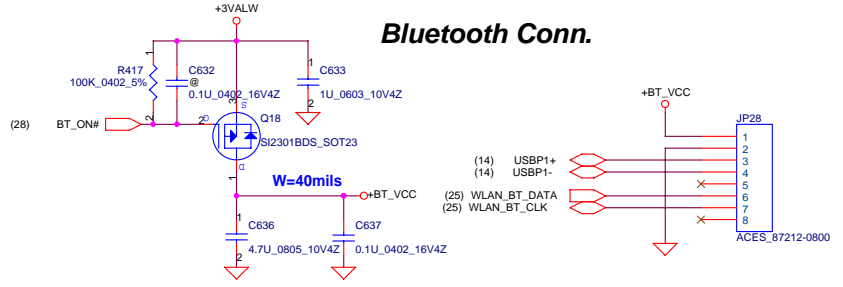


2006/01/24



2006/03/03

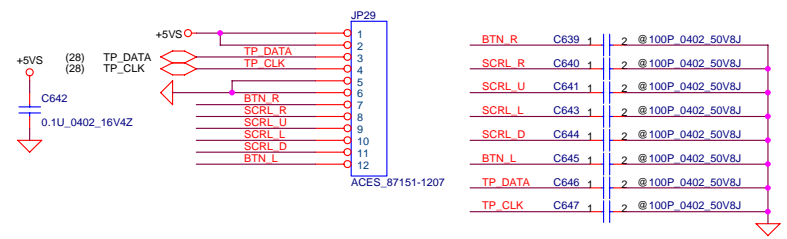
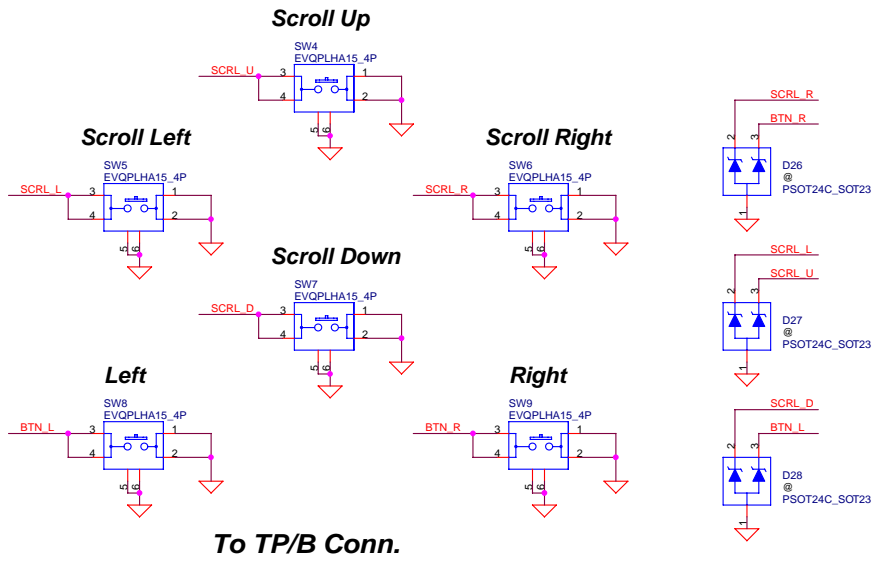
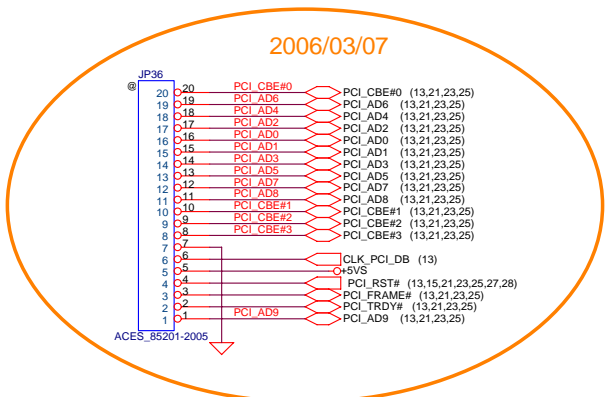
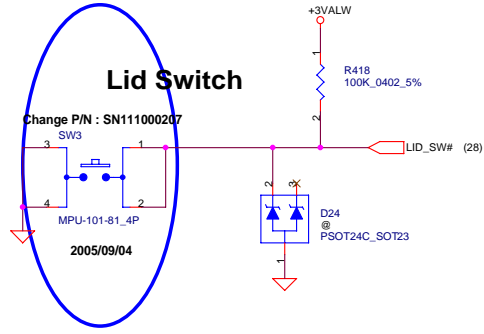
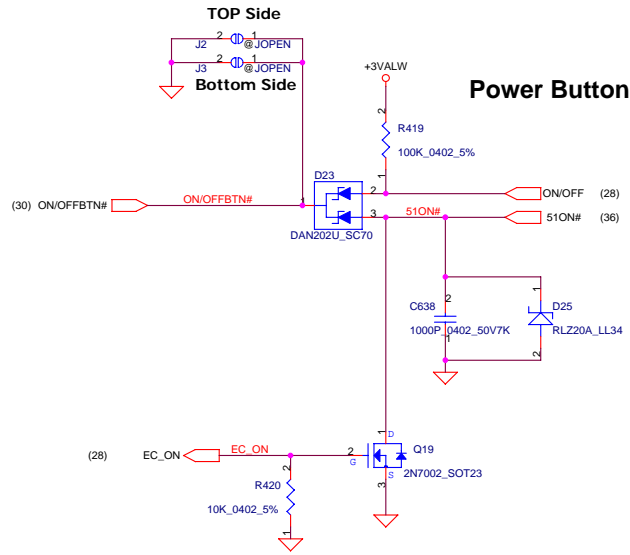
Bluetooth Conn.



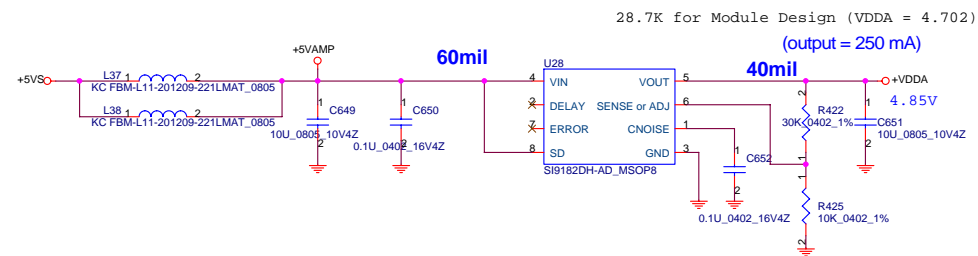
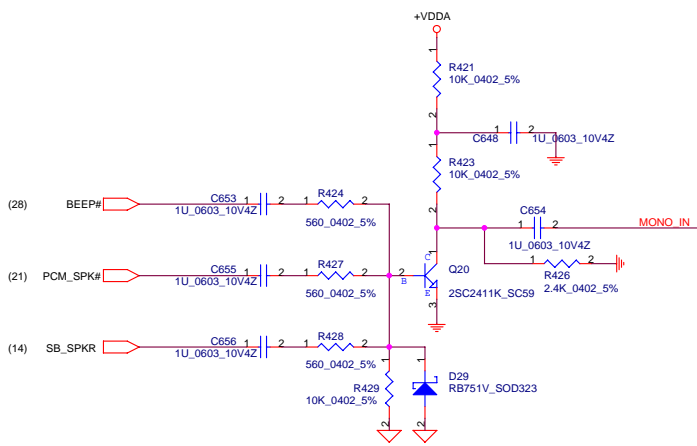
Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER	KSI2	PLAY	
KSI3	STOP		KSI3	STOP	VOL_UP
KSI4	NEXT		KSI4	NEXT	VOL_DOWN
KSI5	REV		KSI5	REV	ARCADE_TV
KSI6		RECORD			

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				HCL51 LA-3211P	0.4
Date: 星期二, 四月 11, 2006				Sheet	30 of 43

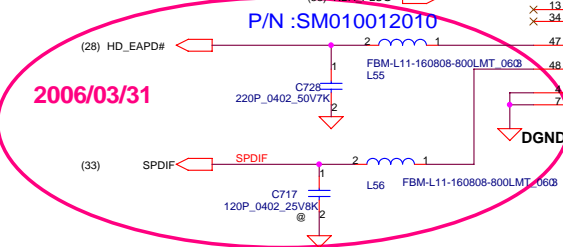
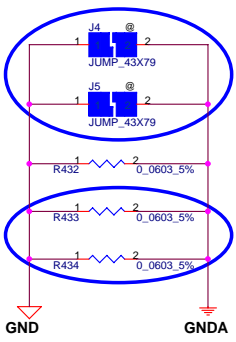
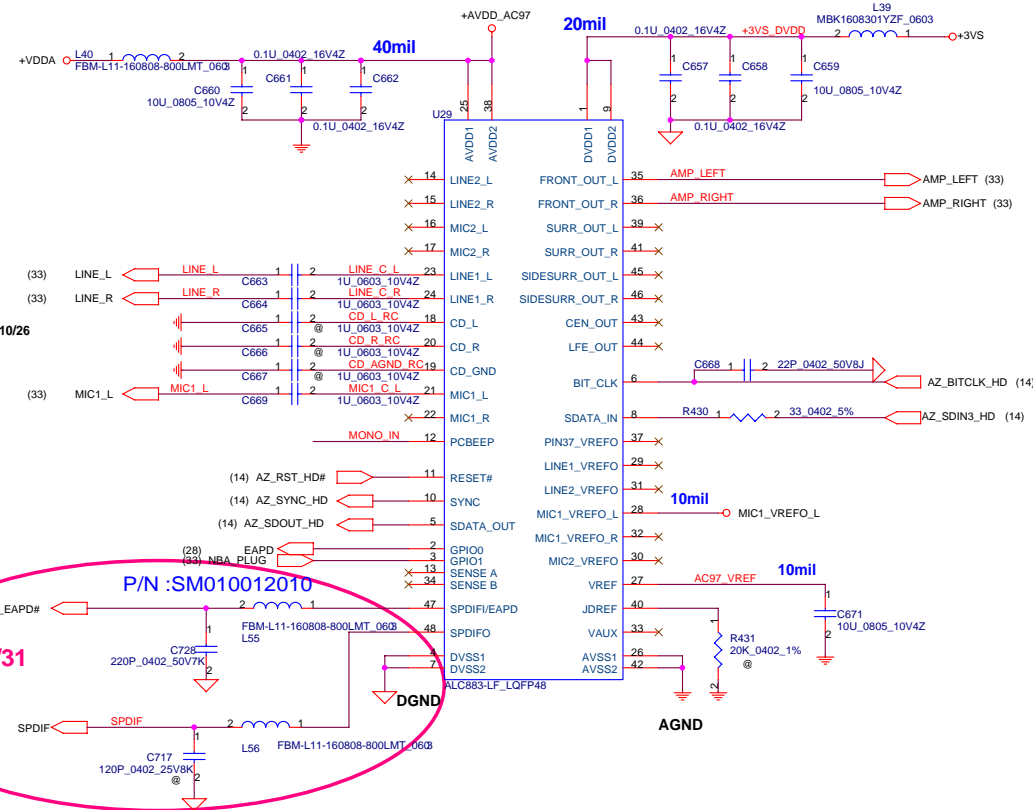
ON/OFF switch



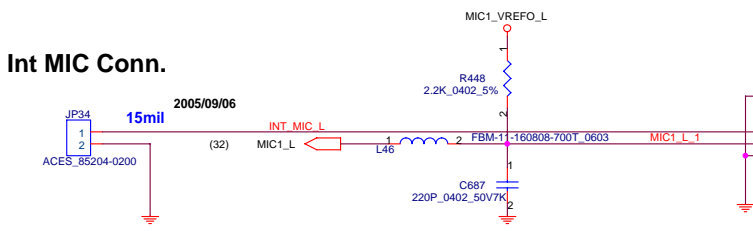
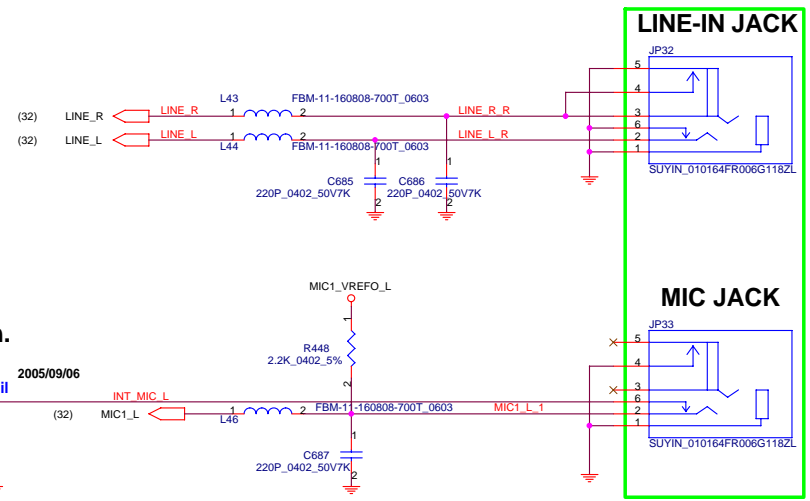
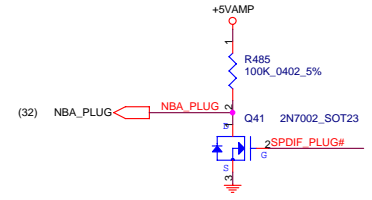
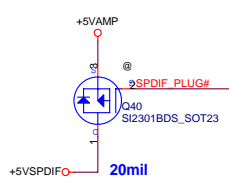
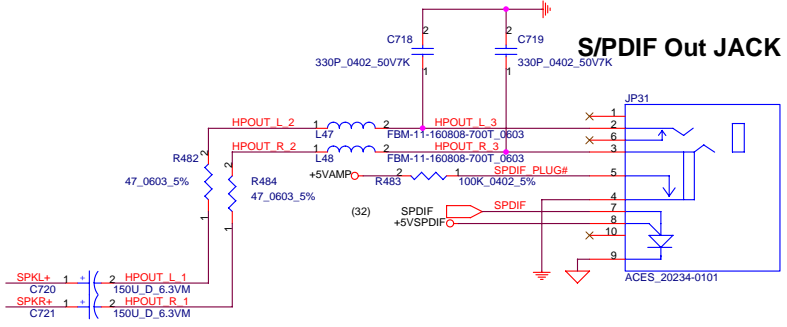
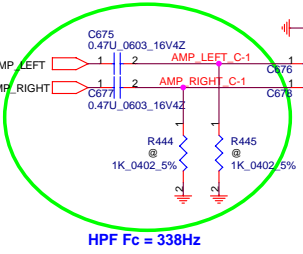
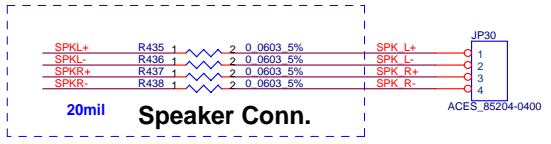
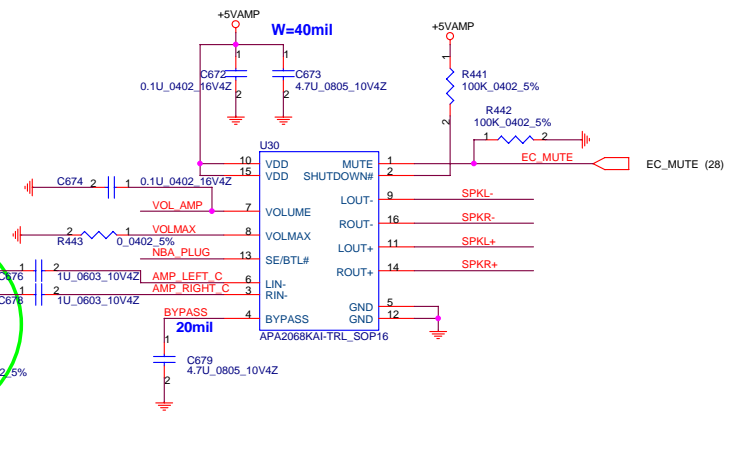
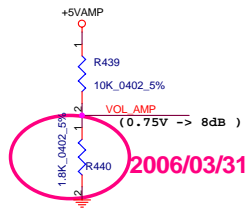
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				HCL51 LA-3211P
				Rev 0.4
Date: 星期二, 四月 11, 2006				Sheet 31 of 43



HD Audio Codec

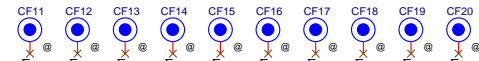
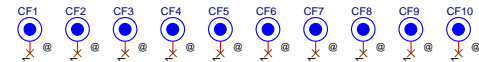
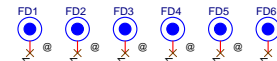
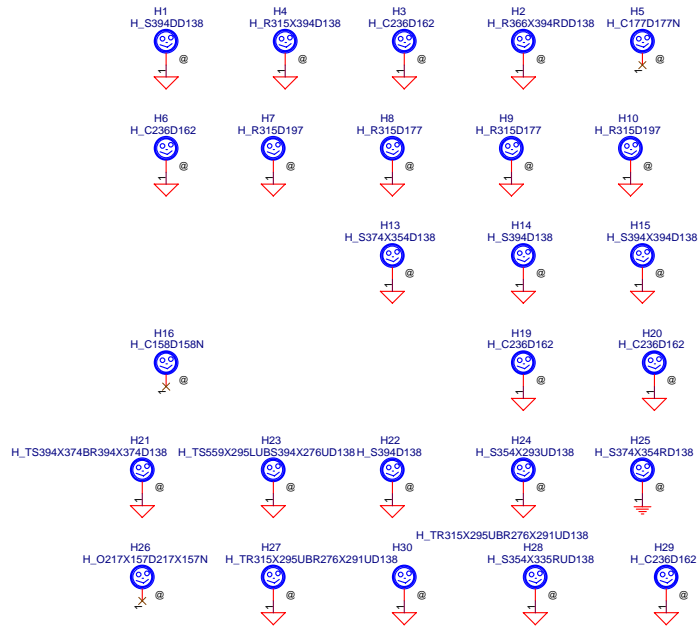
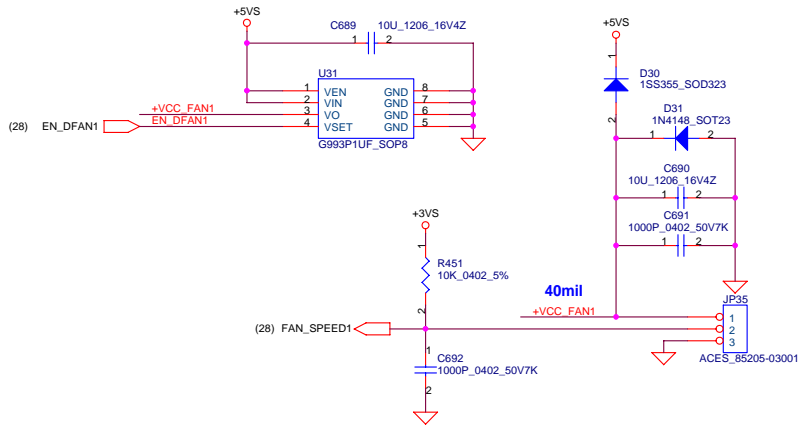


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				HCL51 LA-3211P
				Rev 0.4
				Date: 星期二, 四月 11, 2006
				Sheet 32 of 43



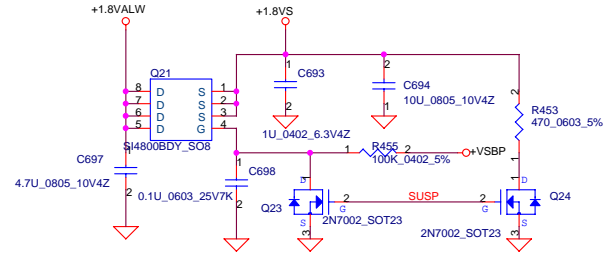
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				HCL51 LA-3211P
				Rev 0.4
				Date: 星期二, 四月 11, 2006
				Sheet 33 of 43

FAN1 Conn

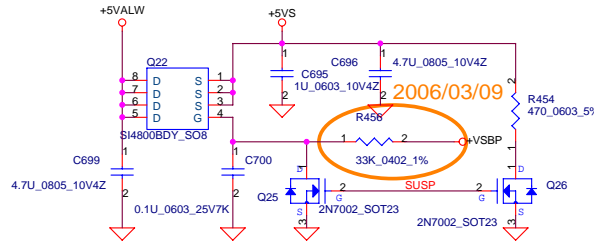


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				HCL51 LA-3211P	0.4
Date: 星期二, 四月 11, 2006				Sheet	34 of 43

+1.8VALW TO +1.8VS

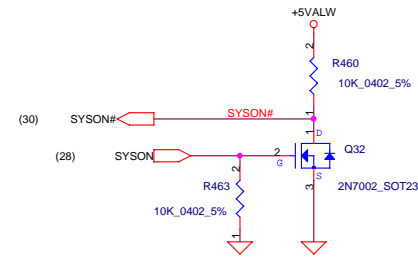
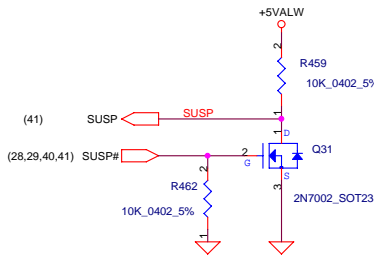
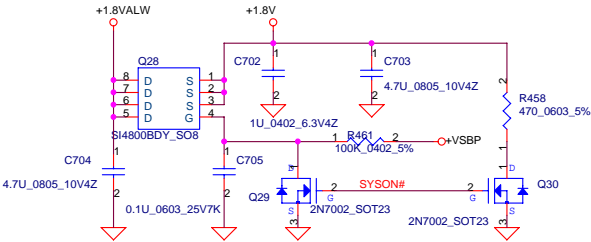


+5VALW TO +5VS

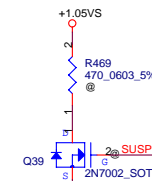
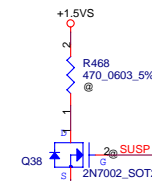
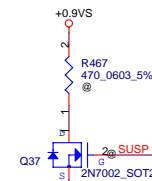
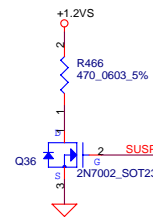
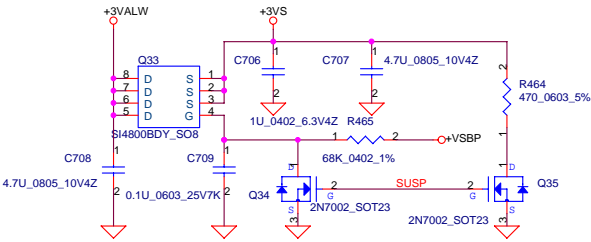


1207 DEL

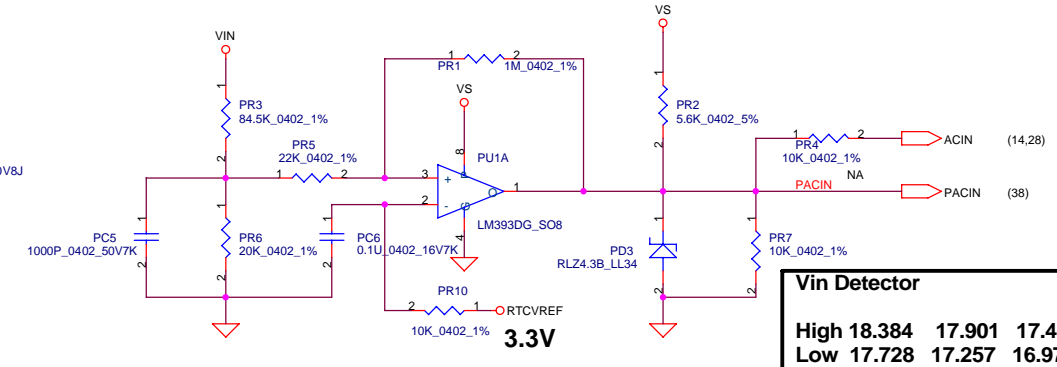
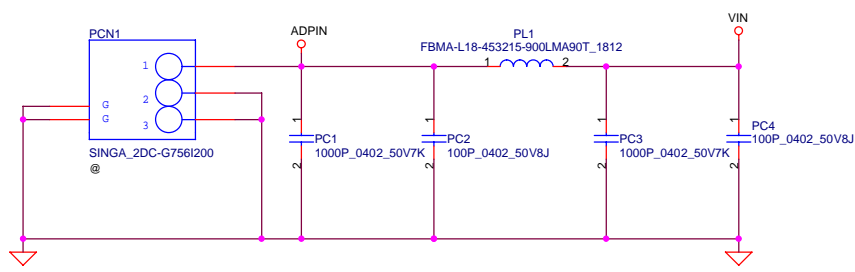
+1.8VALW TO +1.8V



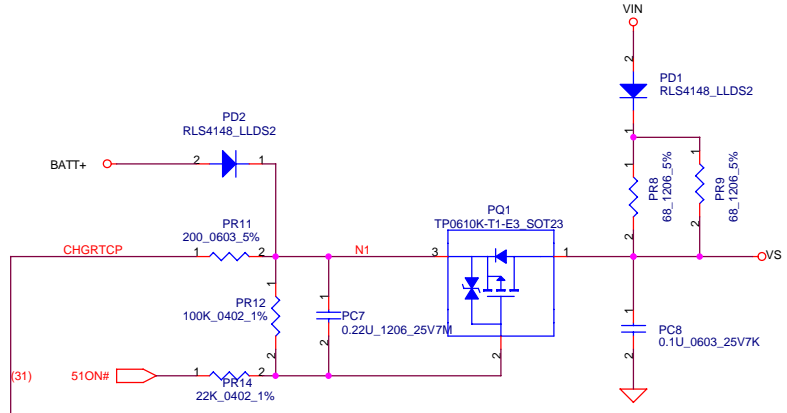
+3VALW TO +3VS



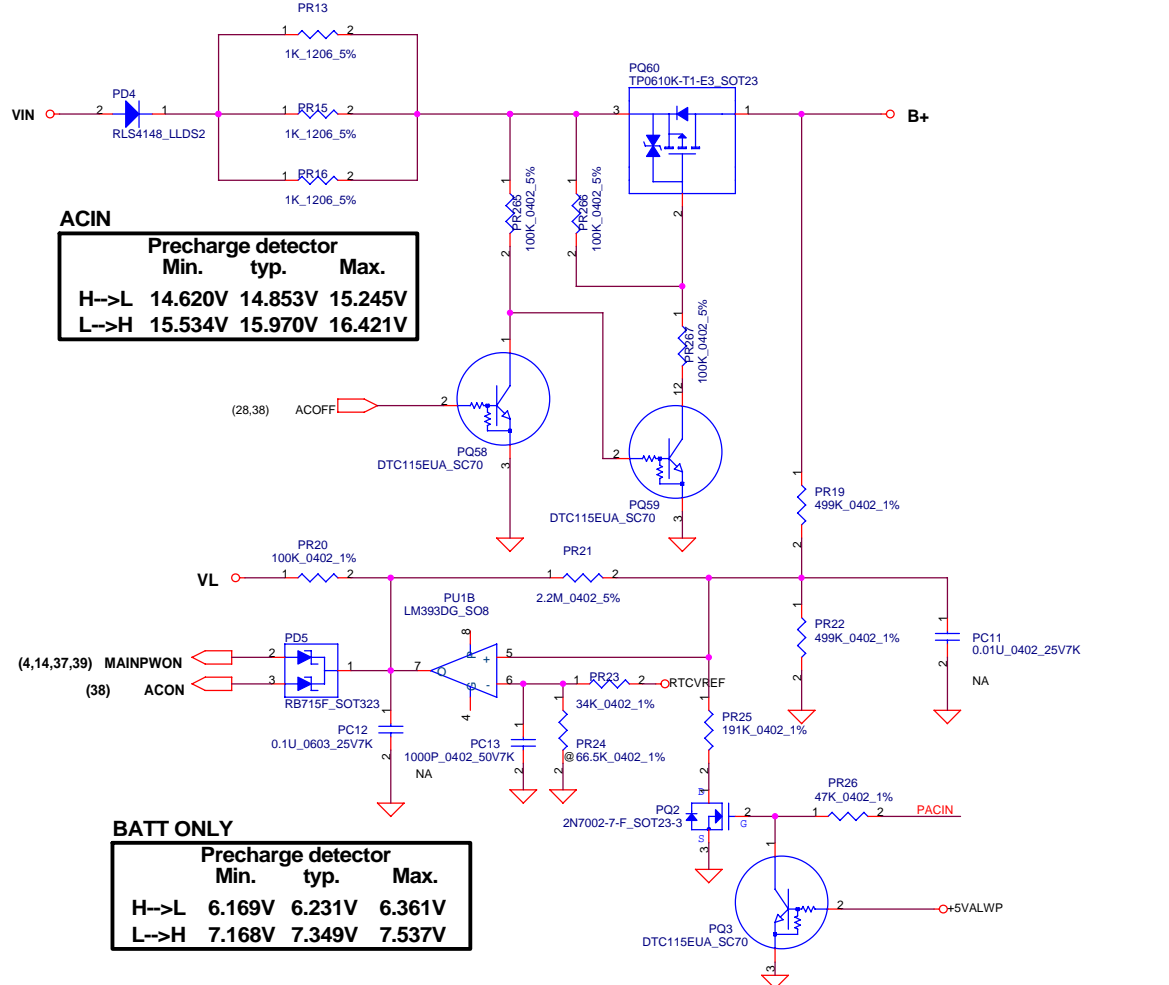
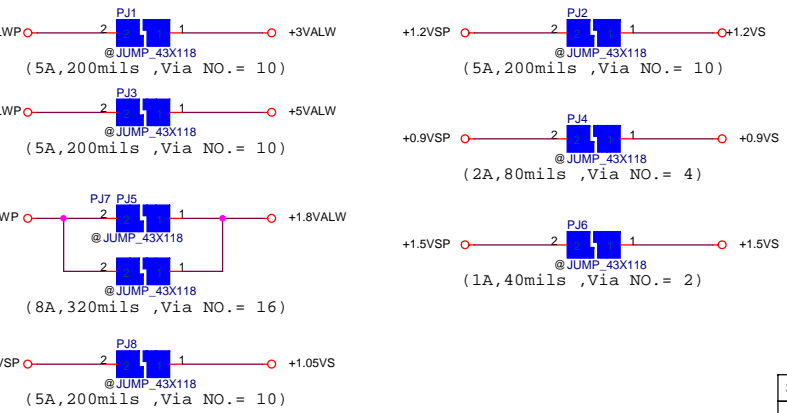
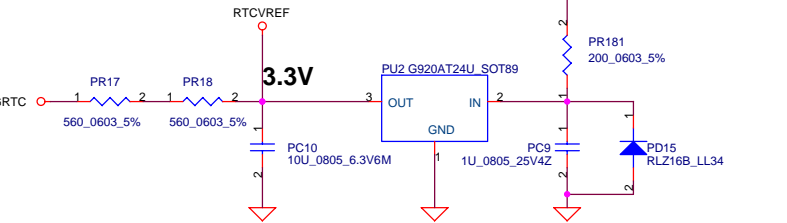
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Document Number			Rev	
HCL51 LA-3211P			0.4	
Date:	星期三, 四月 11, 2006	Sheet	35	of 43



Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



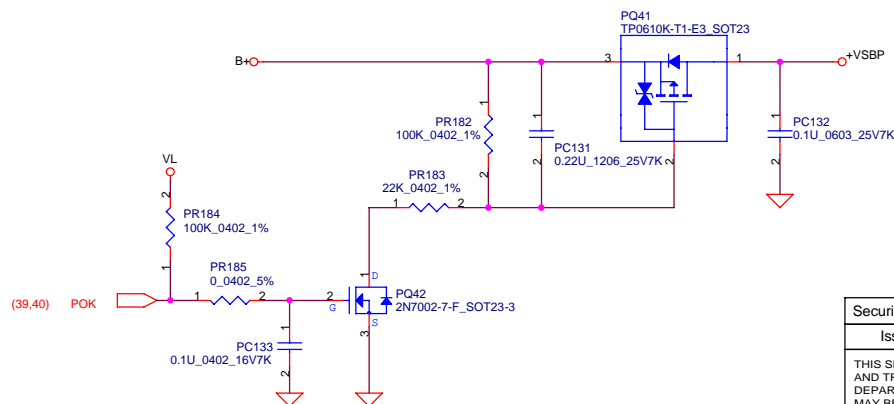
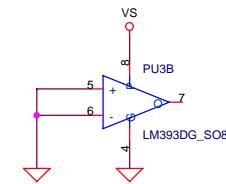
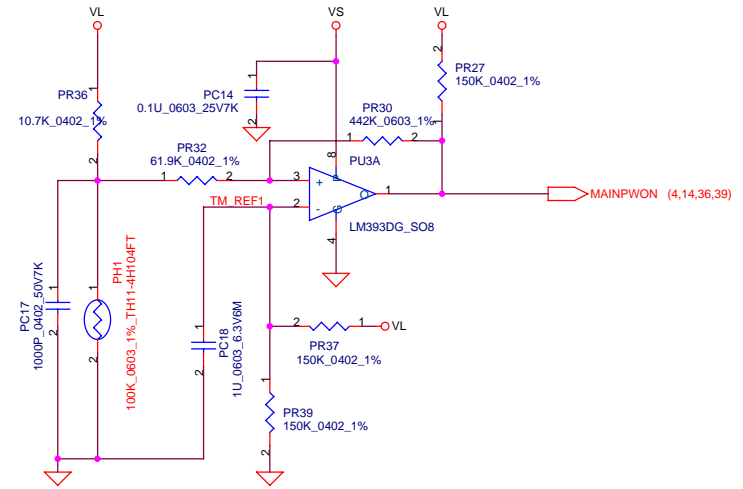
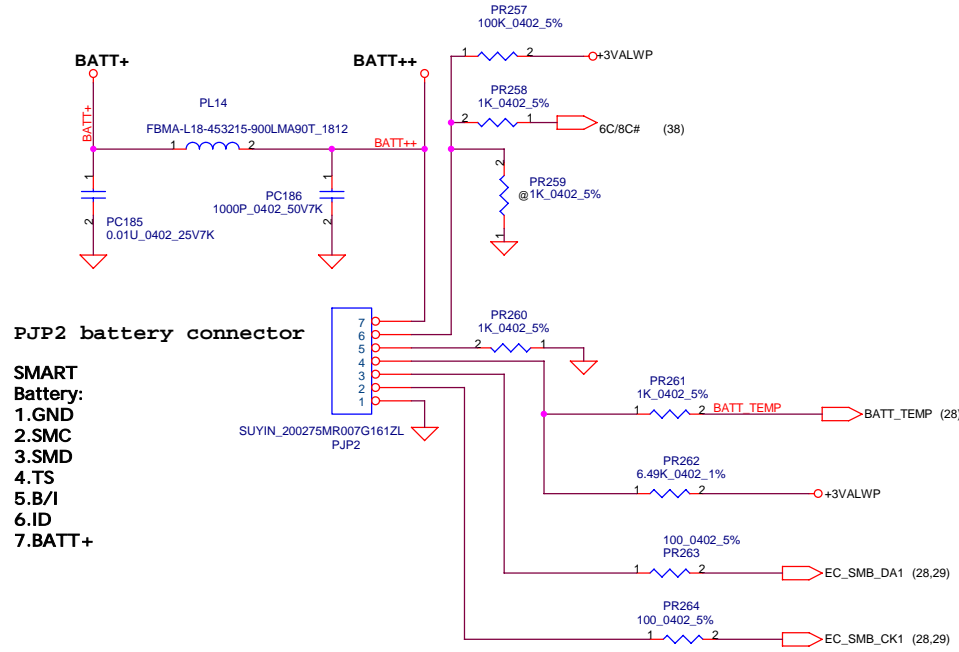
ACIN
 Precharge detector
 Min. typ. Max.
 H->L 14.620V 14.853V 15.245V
 L->H 15.534V 15.970V 16.421V



BATT ONLY
 Precharge detector
 Min. typ. Max.
 H->L 6.169V 6.231V 6.361V
 L->H 7.168V 7.349V 7.537V

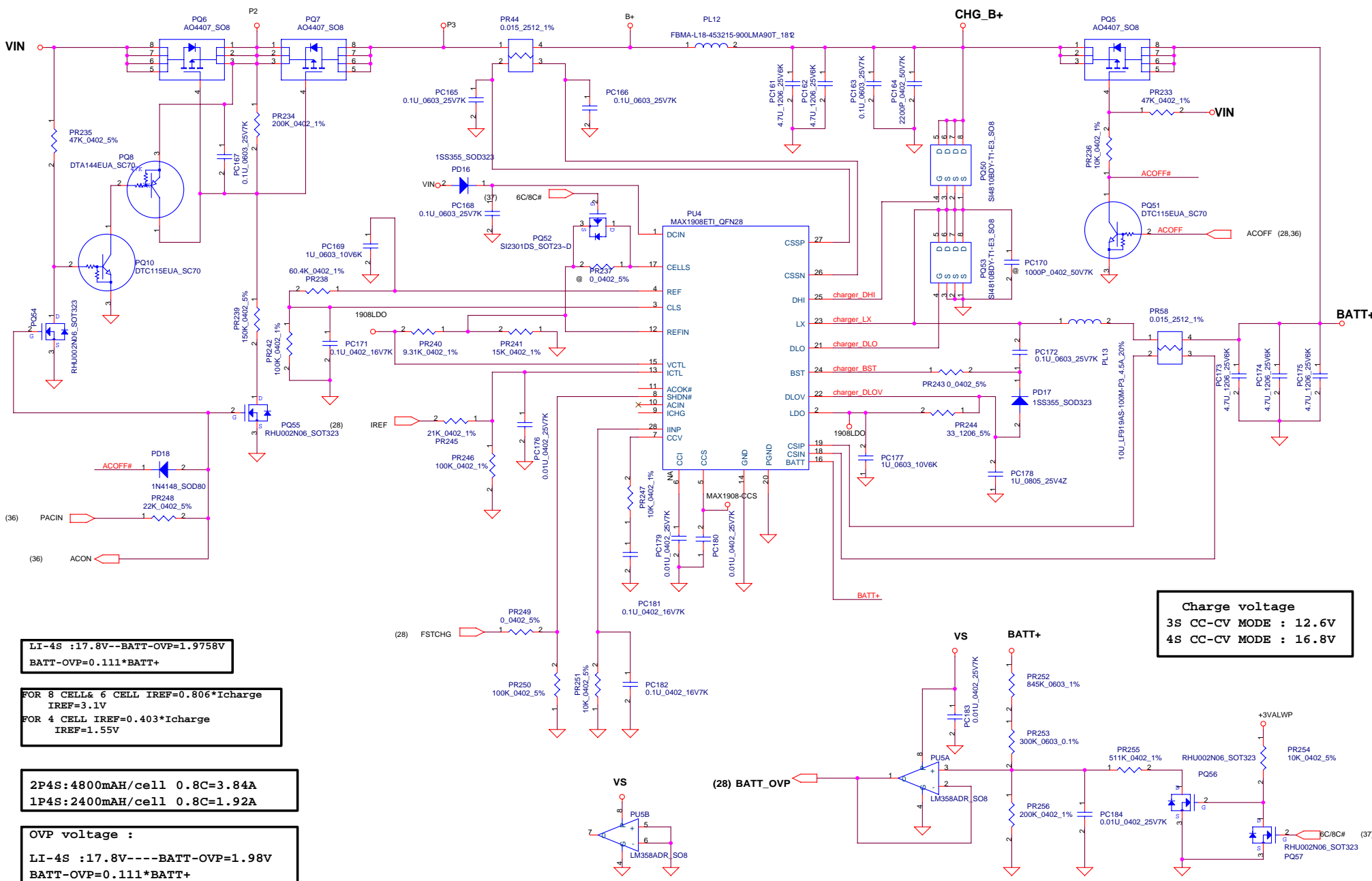
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Date:	星期二, 四月 11, 2006	Sheet	36	of 43

PH1 under CPU botten side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C



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				HCL51 LA-3211P
				Rev
				0.4
Date:	星期二, 四月 11, 2006	Sheet	37	of 43

$I_{adp} = 0 \sim 3.117A (65W)$



Charge voltage
 3S CC-CV MODE : 12.6V
 4S CC-CV MODE : 16.8V

LI-4S : 17.8V -- BATT-OVP = 1.9758V
 BATT-OVP = 0.111 * BATT+

FOR 8 CELL & 6 CELL IREF = 0.806 * Icharge
 IREF = 3.1V
 FOR 4 CELL IREF = 0.403 * Icharge
 IREF = 1.55V

2P4S : 4800mAh/cell 0.8C = 3.84A
 1P4S : 2400mAh/cell 0.8C = 1.92A

OVP voltage :
 LI-4S : 17.8V --- BATT-OVP = 1.98V
 BATT-OVP = 0.111 * BATT+
 LI-3S : 13.35V --- BATT-OVP = 1.98V
 BATT-OVP = 0.111 * BATT+

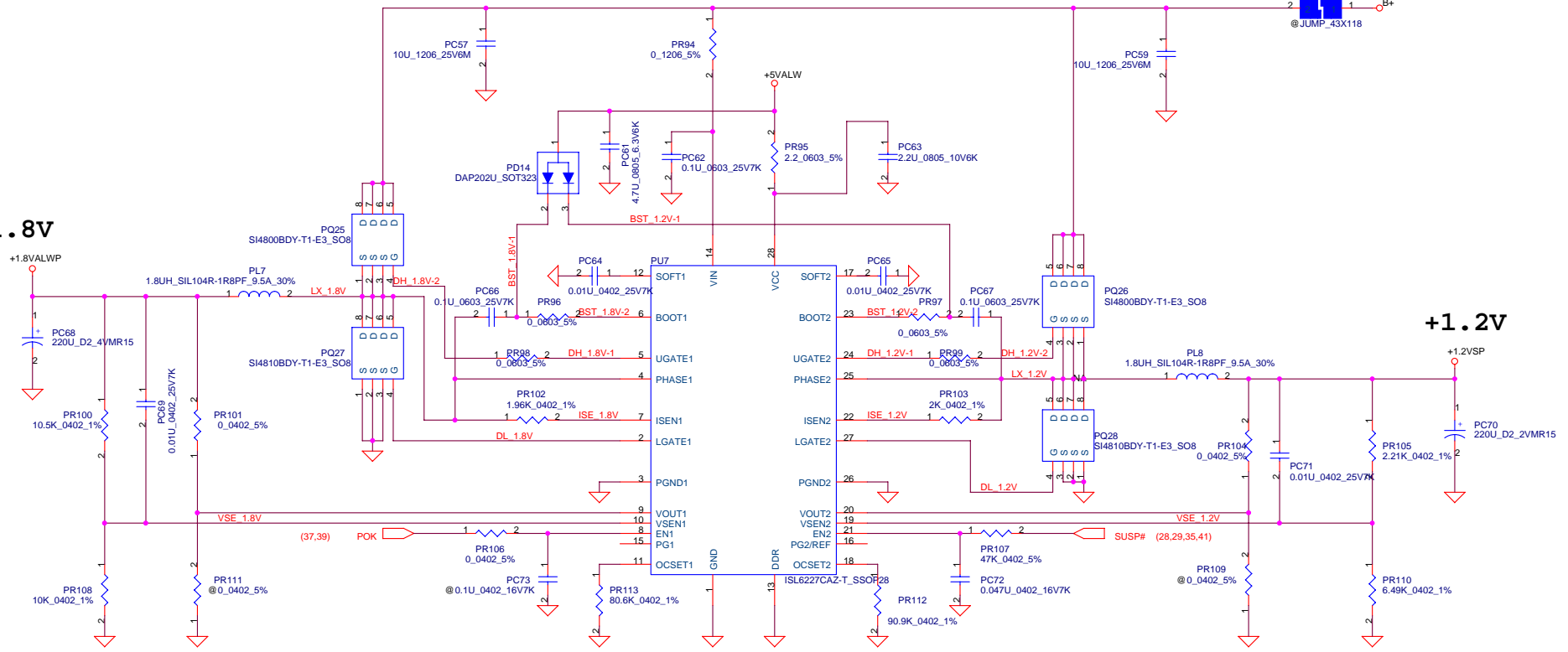
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Date: 星期二, 四月 11, 2006				Sheet 38 of 43

+1.8VP O.C.P= 9.68A~15.72A

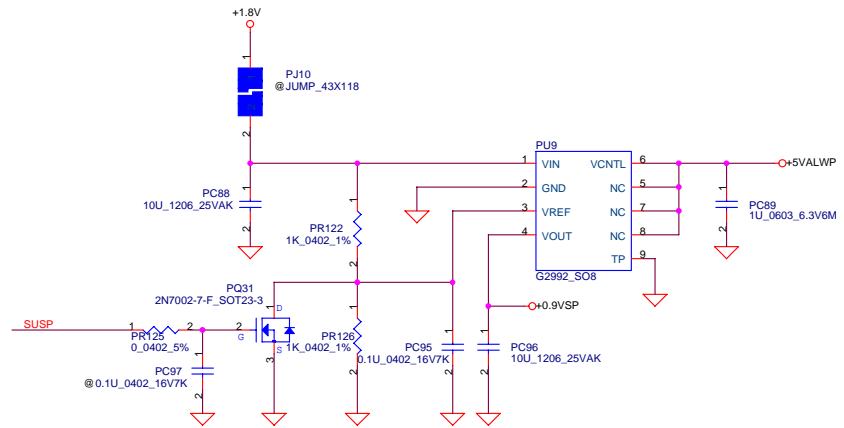
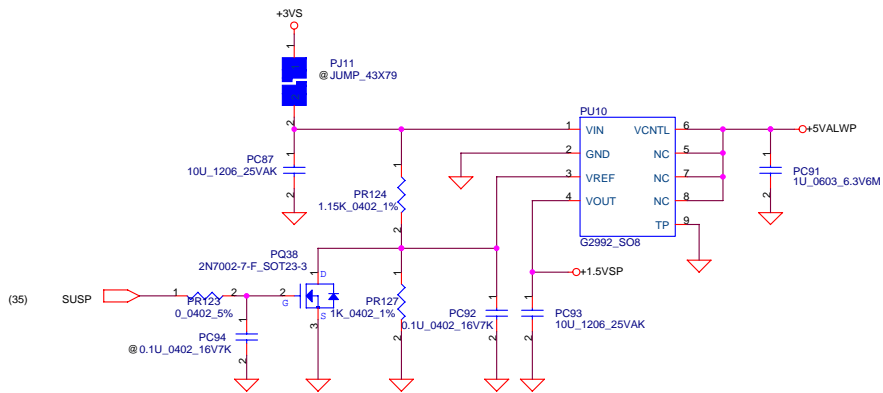
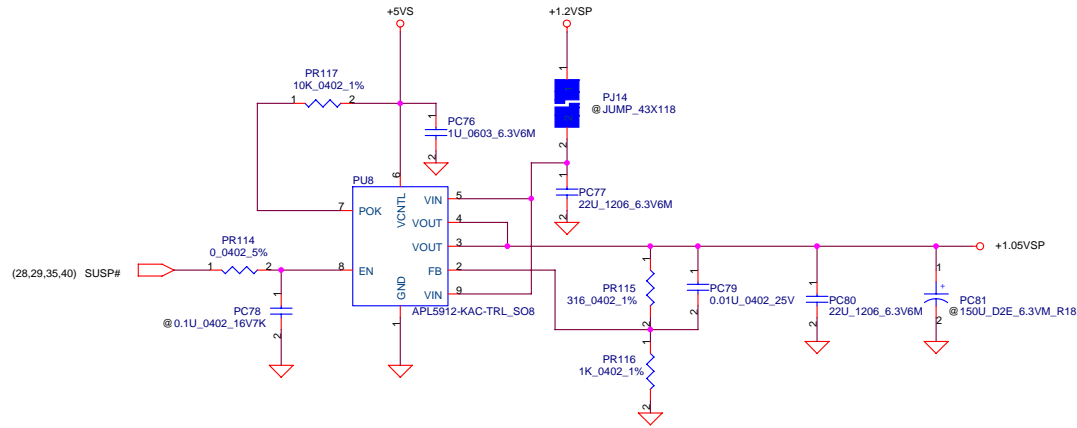
+1.2VP O.C.P= 8.67A~14.09A

+1.8V

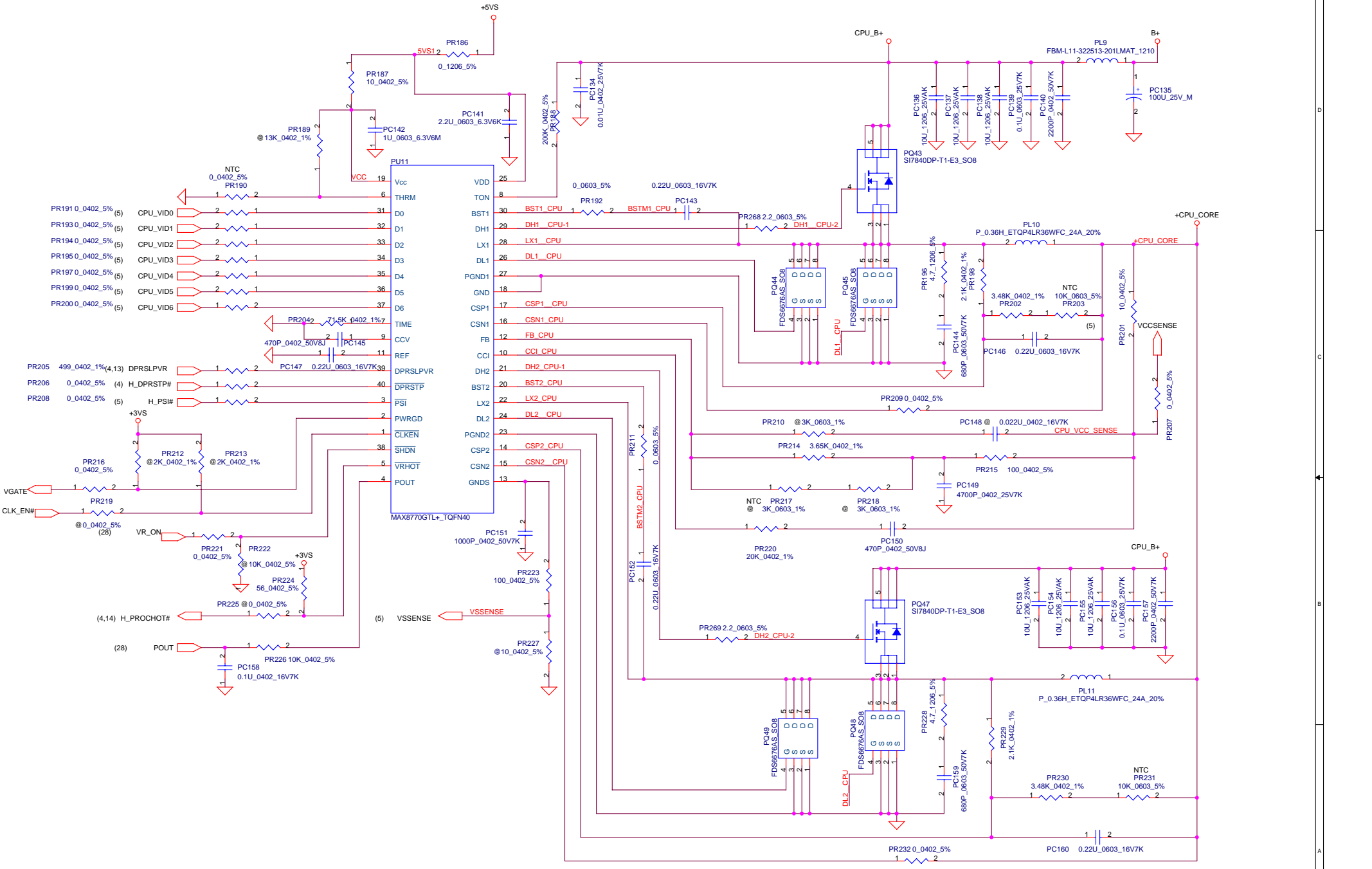
+1.2V



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				+CPU_CORE
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Date:	星期二, 四月 11, 2006	Sheet	42 of 43	Rev 0.4

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		For EMI require CPU core change from 0 to 2.2		42	MODIFY PR268/PR269 FROM 0 TO 2.2		DVT
2		modify 1.2V sequence(HW require)		40	change PR107 from 0 to 1k ;add PC72: :0.01uF		DVT
3		modify 1.2V sequence(HW require)		40	change PR107 from 1K to 47K ;change PC72: : from 0.01uF to 0.047uF		PVT
4							
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Title PIR (PWR)			
Size	Document Number	Rev	0.4
Date: 星期二, 四月 11, 2006	Sheet 43	of	43