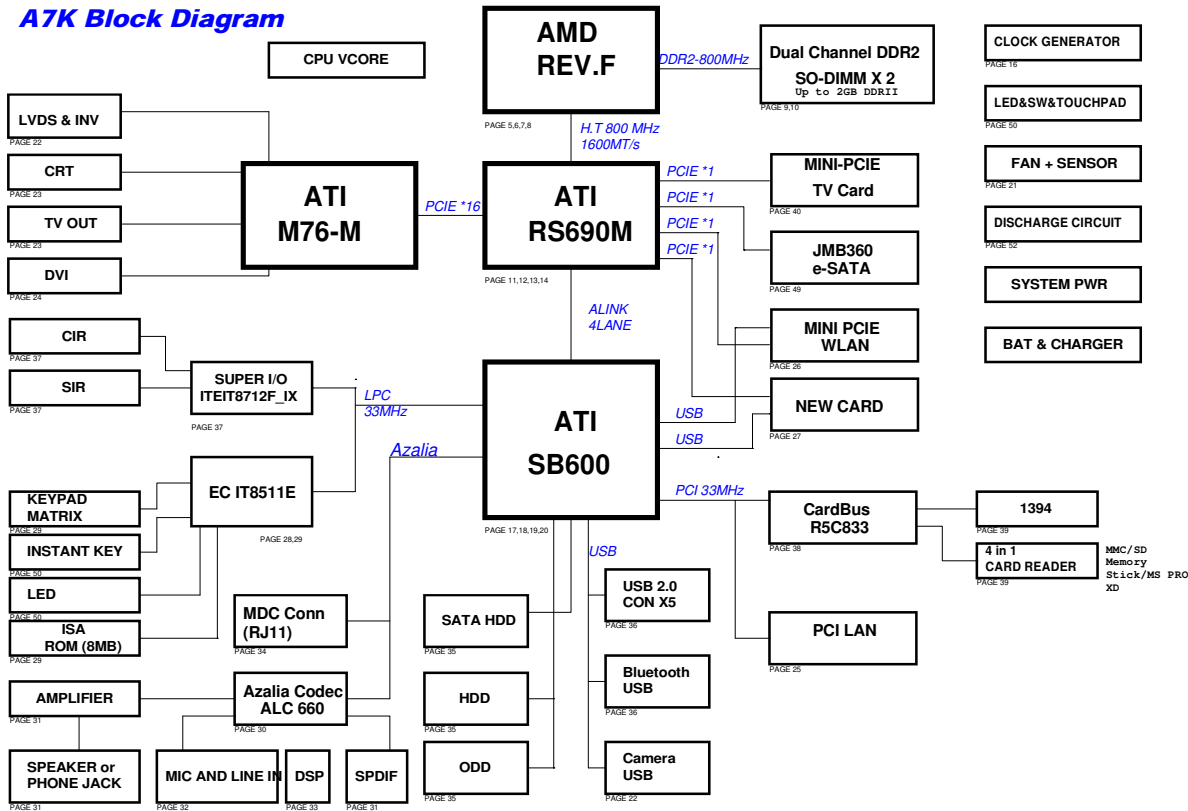


A7K Block Diagram

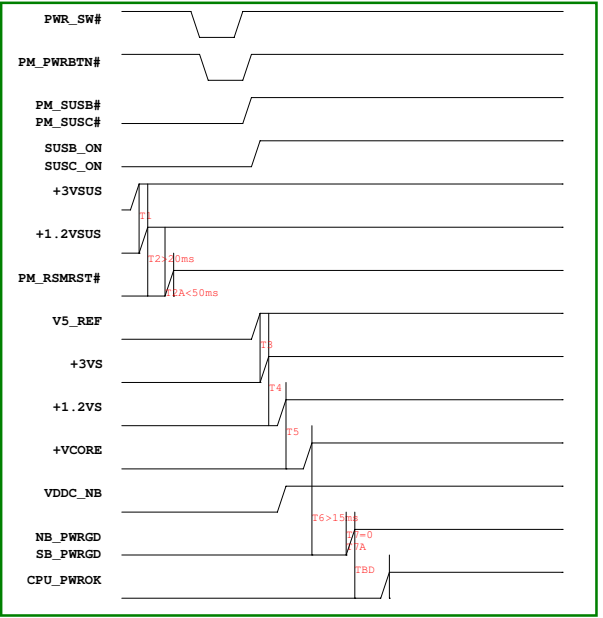


<< Kennedy_Zhang >>

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- P02.TABLE OF CONTENTS
- P03.POWER BUDGET
- P04.CLOCK DISTRIBUTION
- P05.TURION HT I/F
- P06.TURION DDR2 MEMORY I/F
- P07.TURION CNTL/DEBUG/THERM
- P08.TURION POWER
- P09.DDR2_SODIMM
- P10.DDR2_TERMINATIONS
- P11.RS690M-HT LINK0 I/F
- P12.RS690M-PCI-E LINK I/F
- P13.RS690M-SYSTEM I/F&CLKGEN
- P14.RS690M-POWER
- P15.BLANK
- P16.EXTERNAL CLOCK GENERATOR
- P17.SB600-PCI-E/PCI/CPU/LPC
- P18.SB600-ACPI/GPIO/USB/AC97/AZA
- P19.SB600-SATA/IDE/HWM/SPI
- P20.SB600-POWERDECOUPLING
- P21.THERMAL FAN CONTROL
- P22.LVDS AND INVERTER
- P23.CRT AND TV CONNECTOR
- P24.DVI
- P25.PCI LAN
- P26.MINI PCI-E WLAN
- P27.NEW CARD
- P28.EC I78510TE(1/2)
- P29.EC I78510TE(2/2)-ISA ROM
- P30.AC97
- P31.AMP AND HEADPHONE
- P32.MIC AND LINE IN
- P33.DSP
- P34.MDC
- P35.HDD AND ODD
- P36.USB CONNECTOR AND BT
- P37.SIO AND SIR
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- P39.1394 AND CARD READER
- P40.MINI PCI-E(TV)
- P41.M76(1/5)PCI-E I/F
- P42.M76(2/5)DVI&DAC&DDC&PLL&VID
- P43.M76(3/5)MEMORY I/F
- P44.M76(4/5)BLANK
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- P46.GDDR2 MEMORY(1/2)
- P47.GDDR2 MEMORY(2/2)
- P48.BLANK
- P49.BLANK
- P50.FUNCTION KEY
- P51.POWER SEQUENCE
- P52.DISCHARGE

DEVICE	IDSEL#	REQ/GNT#	PCI INT	CLOCK
NB VGA	N/A	N/A	A	
SB	AD31(INT)	N/A	N/A	
ATA100	AD31	N/A	A	INT
AC97/AZALIA	AD31	N/A	B	INT
USB	AD30	N/A	D	INT
CARD BUS	AD17	0	F,G	PCI_CLK0
PCI LAN	AD18	1	E	PCI_CLK1

SOURCE	SIGNAL NAME	LINKED DEVICES
NB	DAC_SCL/DAC_SDAT	CRT/LVDS
	I2C_CLK/I2C_DATA	LVDS
	I2C_CLK/DDC_DATA	DVI
SB	SCLK0/SDATA0	SO-DIMMs/CLK_GEN/DSP
	SCLK1/SDATA1	MINI-PCI-E(WLAN)/NEW CARD/MINI-PCI-E(TV)
EC	SMCLK0/SMDAT0	BATTERY
	SMCLK1/SMDAT1	THERMAL(CPU:98H GPU:4CH)



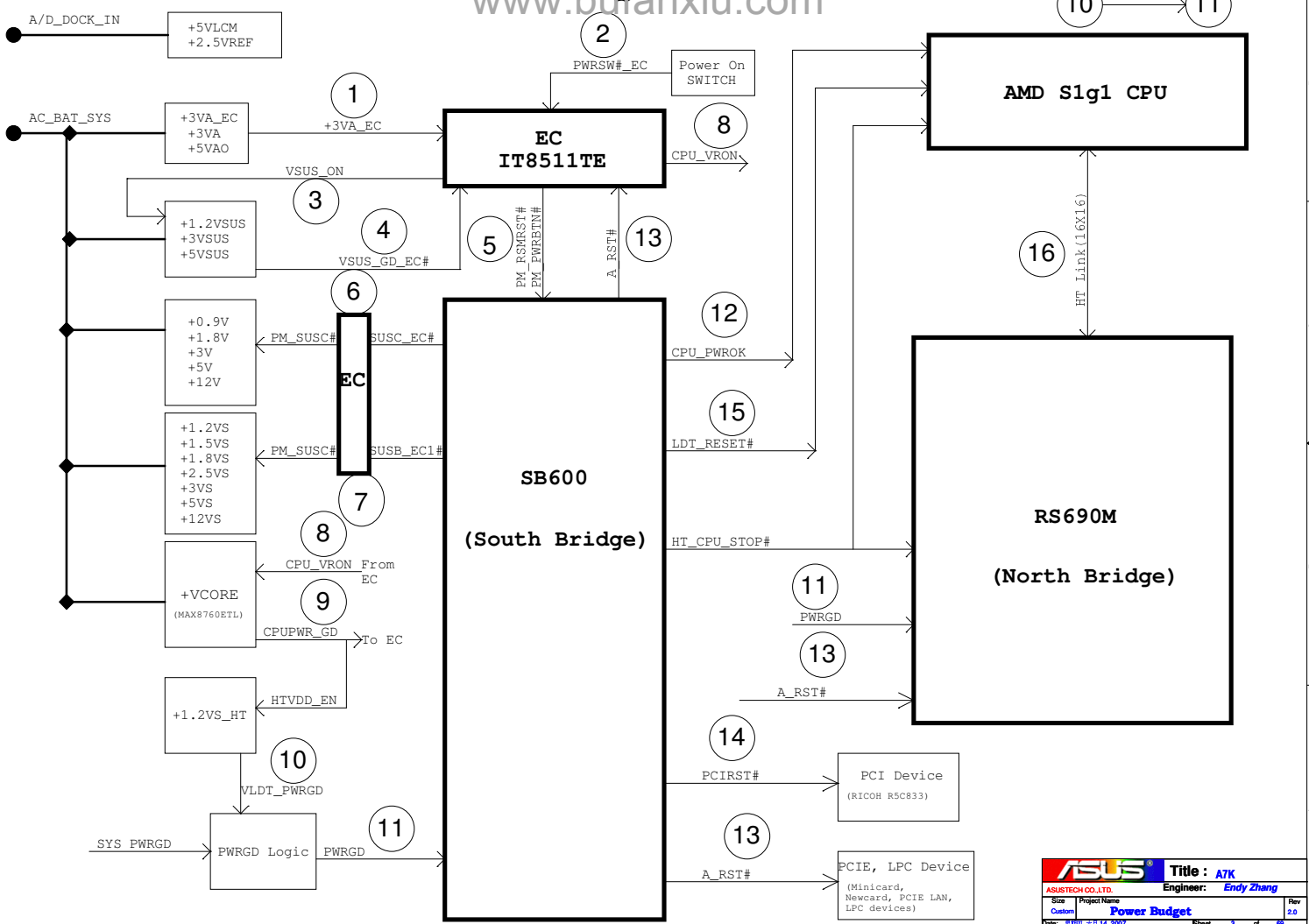
NE	ST/P_DATA	SEL_VCC_NB	TUNE NB VOLTAGE	OUTPUT
SB	RHEXTEVINT0#	KB_SCF#	KEYBOARD SCI	INPUT
	LPC_PME#/GEVENT#	LPC_PME#	PME FROM EC	INPUT
	LPC_SM#/EXTEVT#	LPC_SM#	SMI FROM EC	INPUT
	WAKE#/EVENT#	SB_WAKE#	PCI-E WAKE	INPUT
	GPIO0	BT_DET#	BLUETOOTH DETECT	INPUT
	GPIO5	BT_LED_EN#	BLUETOOTH LED	OUTPUT
	GPIO4	802_LED_EN#	WIRELESS LAN LED	OUTPUT
	GPIO5	CB_HWSUSPEND	CARDBUS SUSPEND	OUTPUT
	GPIO5	BT_ON#	BLUETOOTH ENABLE(OPTION)	OUTPUT
	GPIO0	WLAN_ON#	WIRELESS LAN ENABLE	OUTPUT
	LLB#/GPIO6	BAT_LLE	BATTERY LOW(OPTION)	INPUT
	TEMPIN0	CPU_THERM	CPU TEMPERATURE(OPTION)	INPUT
	TEMPIN1	NB_THERM	NB TEMPERATURE	INPUT
	GPIO11	SB_THRO_CUPU	CPU OVER TEMP AND SHUT	OUTPUT
	GPIO12	TV_ON#	TV ENABLE	OUTPUT
	GPIO4	PM_THERM#	THERM ALERT FROM EC	INPUT
EC	ECSMI#/GPM0	EXSMI#	SMI TO SB	OUTPUT
	ECSC#/GPD3	EXIT_SC#	SCIT0 SB	OUTPUT
	SM0	SM_BAT	SMIBUS TO BATTERY	OUTPUT
	SM1	SMB1	SMIBUS TO THERMAL	OUTPUT
	ADCC/GPK0	BATO_AD	BATTERY VOLTAGE	INPUT
	ADCC/GPK2	AC_AD	AC ADAPTER VOLTAGE	INPUT
	GPK4	KIDD	KEYBOARD ID0	INPUT
	GPK5	KID1	KEYBOARD ID1	INPUT
	DAC2/GPJ0	FAN_DA	FAN CONTROL(OPTION)	OUTPUT
	DAC2/GPJ2	BRIGHT_PWM	LCD BRIGHT CONTROL	OUTPUT
	GPJ3	BATSEL_2P#	2P BATTERY	INPUT
	PMH1/GPA1	FAN_PWM	FAN CONTROL	OUTPUT
	GPA4	CHG_LED_UP#	CHARGE LED	OUTPUT
	GPA5	PWR_LED_UP#	POWER LED	OUTPUT
	GPA6	BATSEL_3S#	3S BATTERY	INPUT
	GPA7	BACK_OFF#	LED BACK OFF	INPUT
	GPB0	NUM_LED	NUM LOCK LED	OUTPUT
	GPB1	CAP_LED	CAP LOCK LED	OUTPUT
	GPB2	THRO_CUPU	CPU OVER TEMP AND SHUT	OUTPUT
	GPC0	DJ_LED#	AUDIO DJ LED	OUTPUT
	GPC2	EMAIL_LED#	EMAIL LED	OUTPUT
	GPC4	ADCN_OC#	ADAPTER IN	INPUT
	GPC5	OP_SD#	AUDIO SHUTDOWN	OUTPUT
	GPC6	BAT_IN_OC#	BATTERY IN	INPUT
	GPC7	EC_IDE_RST#	EC CONTROL IDE RST	INPUT
	R1#/WUI0/GPD0	PM_SUSB#	SB SUSB IN	INPUT
	R2#/WUI1/GPD1	PM_SUSC#	SB SUSC IN	INPUT
	GPD4	RF_OFF_SW#	RF SWITCH OFF	INPUT
	GPD6	FAN0_TACH	FAN TACH	INPUT
	GPE0	EMAIL_SW#	EMAIL SWITCH	INPUT
	GPE1	INTERNET#	INTERNET SWITCH	INPUT
	GPE2	MARATHON#	POWER GEAR	INPUT
	GPE3	DIST_SW#	DISABLE TOUCHPAD	INPUT
	PWRSE/GPE4	PWRSW_EC	POWER SWITCH	INPUT
	GPE6	LID_EC#	LID STATUS IN	INPUT
	GPE7	BT_ON#	BLUETOOTH ENABLE	OUTPUT
	PS2CLK2/GPF4	TPAD_CLK	TOUCHPAD CLK	OUTPUT
	PS2DAT2/GPF5	TPAD_DAT	TOUCHPAD DATA	OUTPUT
	GPF6	PWR_LMT#	POWER LIMIT	OUTPUT
	GPF7	DJ_SW#	DJ SWITCH	INPUT
	GPG4	THRM_CPU	ALERT FROM THERMAL IC	INPUT
	GPG6	PM_THERM#	THERM ALERT TO SB	OUTPUT
	GPG7	AC_APPR_UC#	ADAPTER POWER OK	INPUT
	GPH0	VSUS_ON	ENABLE VSUS POWER	OUTPUT
	GPH1	VSUS_GD_EC#	VSUS OK	INPUT
	GPH2	IMVPOK#	CPU POWER OK	INPUT
	GPH3	PM_PWRBTN#	PWRBTN TO SB	OUTPUT
	GPH4	SUSC_ON	SUSC_ON	OUTPUT
	GPH5	SUSB_ON	SUSB_ON	OUTPUT
	GPH6	CPU_VRON	ENABLE VCORE	OUTPUT
	GPH7	PM_RSMRST#	SB RSMRST	OUTPUT
	GPI1	WATCH_DOG#	WATCH_DOG CONTROL FAN	OUTPUT
	GPI3	CHG_EN#	ENABLE CHARGE	OUTPUT
	GPI4	PRECHG	BATTERY PRECHARGE	OUTPUT
	GPI5	BAT_LLE	BATTERY LOW	OUTPUT
	GPI6	BAT_LEARN	BATTERY LEARN	OUTPUT
SIO	PME#	LCP_PME#	PME TO SB	OUTPUT

ASUS Title: A7K
 ASUSTECH CO., LTD. Engineer: Endy Zhang
 Size: Project Name: Rev: 2.0
 Custom: Table of Contents
 Date: 2007.12.14.2007 Page: 2 of 26

<< Kennedy_Zhang >>

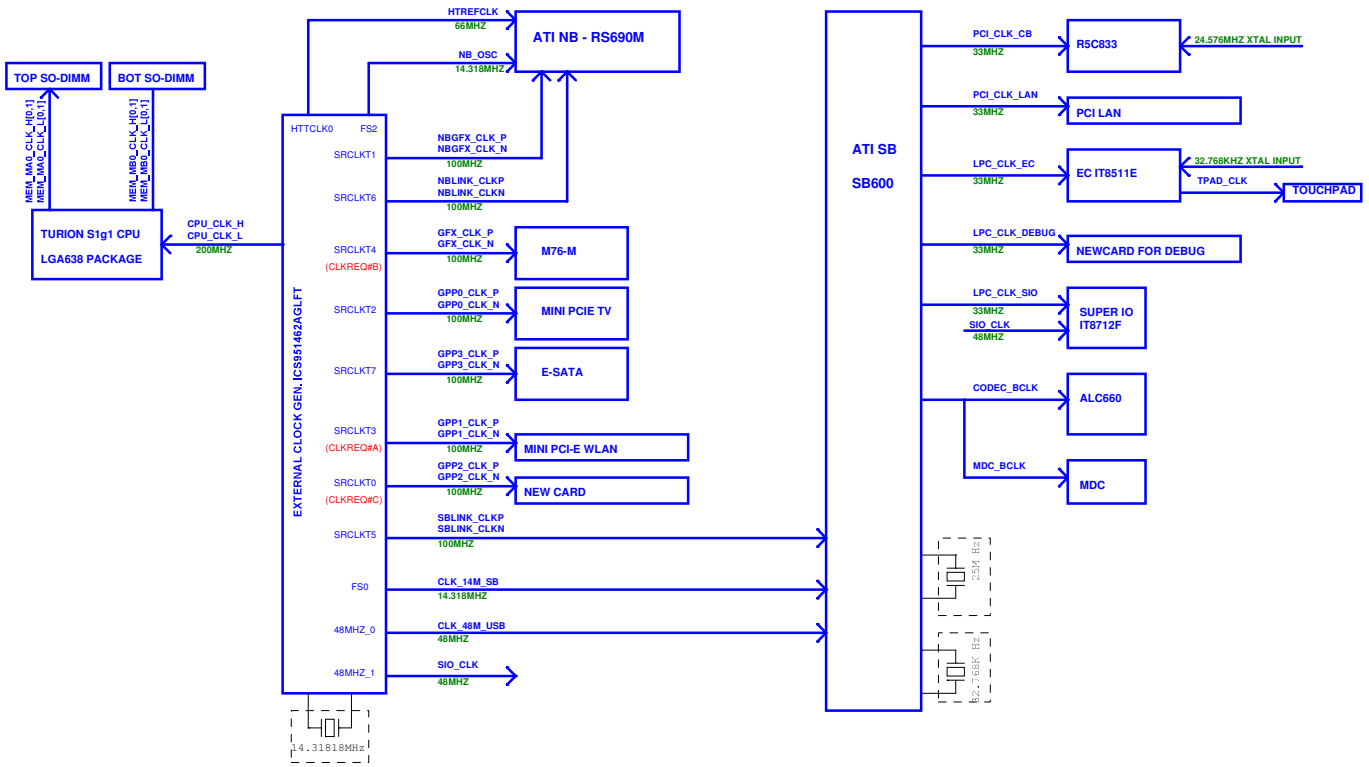
A7K POWER ON SEQUENCE BLOCK

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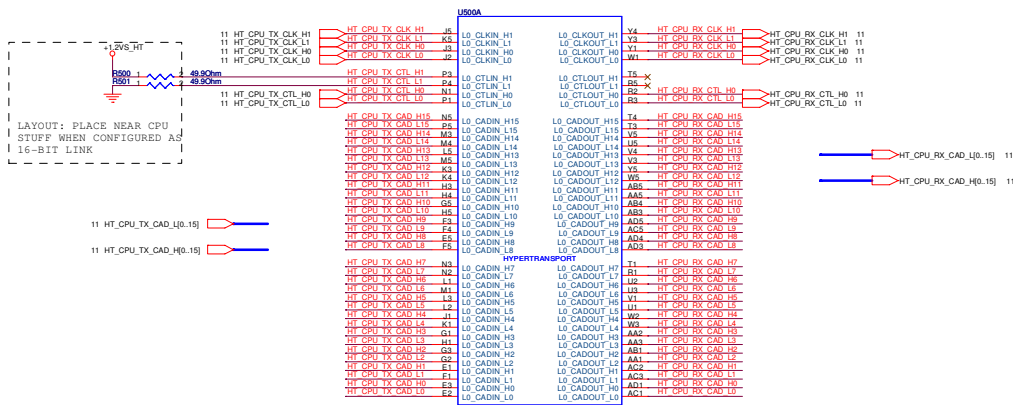


ASUS		Title: A7K
ASUSTECH CO. LTD.		Engineer: Andy Zhang
Size	Project Name	Rev
Custom	Power Budget	2.0
Date: JUN 14 2007	Sheet	3 of 69

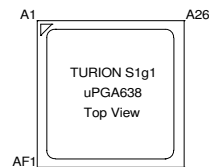
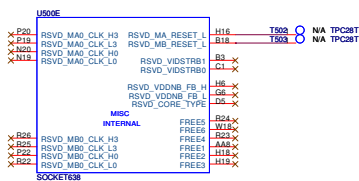
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<< Kennedy_Zhang >>



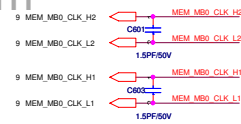
Do not cross plane.



<< Kennedy_Zhang >>

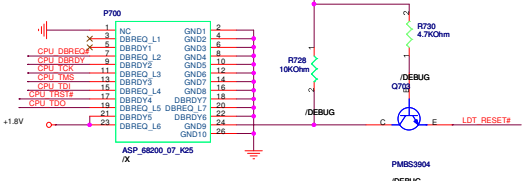
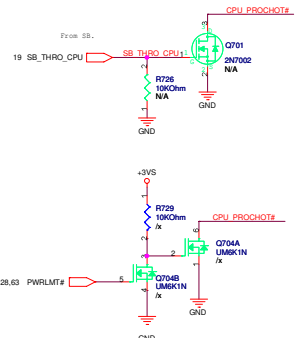
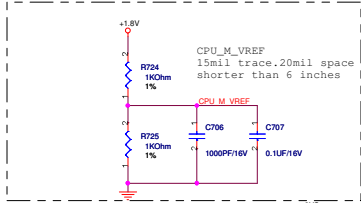
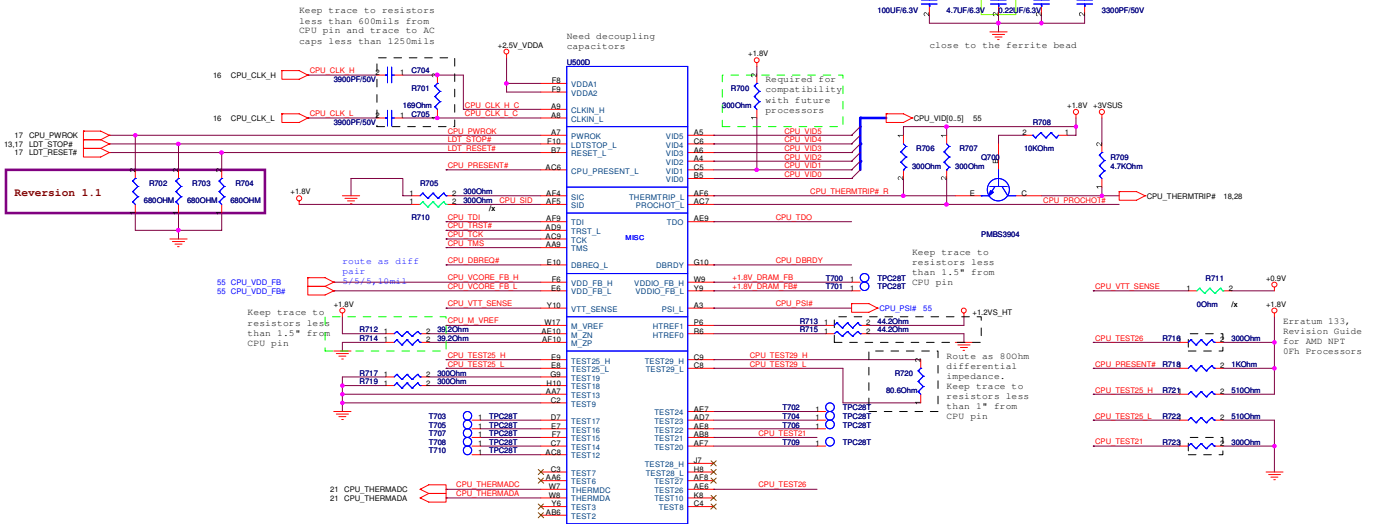
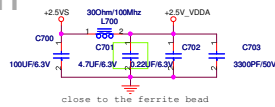


the cap close to cpu less than 1200mil
max neckdown to & from caps is 500mil



ASUS		Title : A7K
ASUSTECH CO. LTD.		Engineer: Andy Zhang
Size	Project Name	Rev
Custom	Turion DDR2 Memory 1/F	2.0
Date: 2007.06.14.2007	Sheet	6 of 69

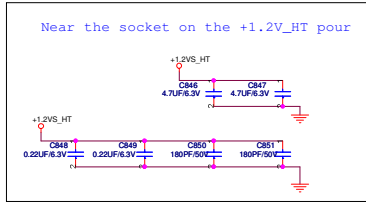
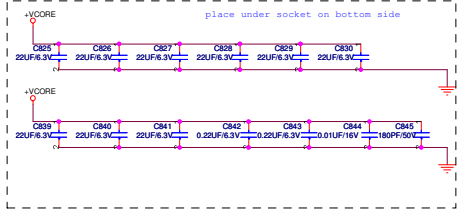
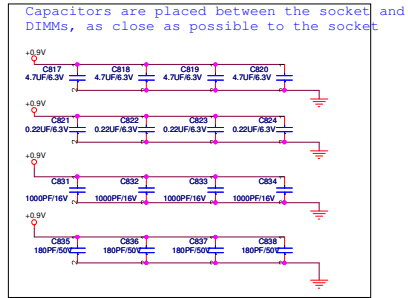
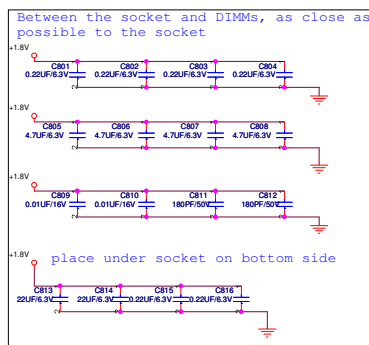
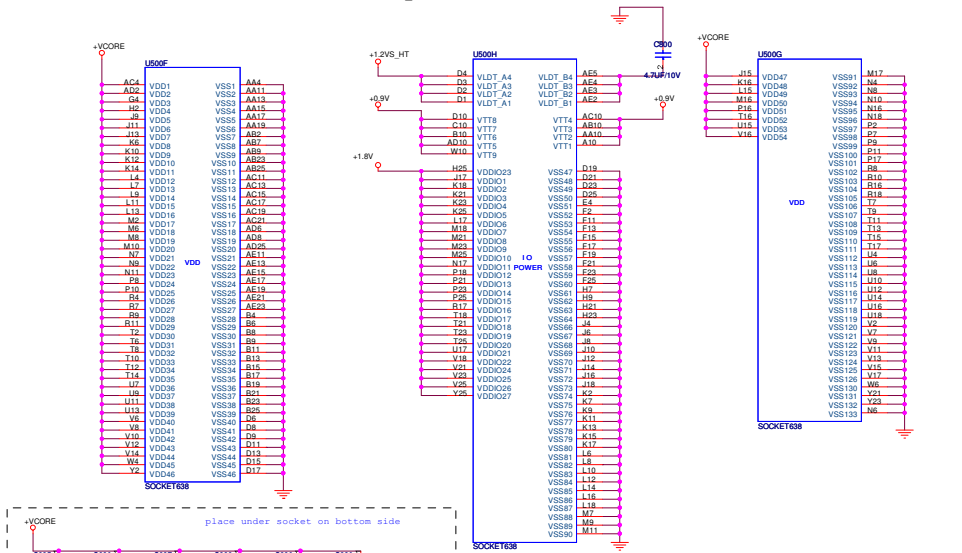
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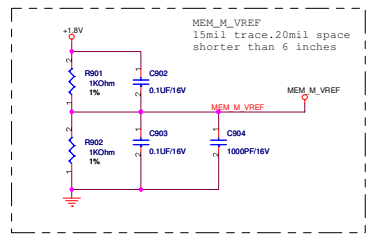
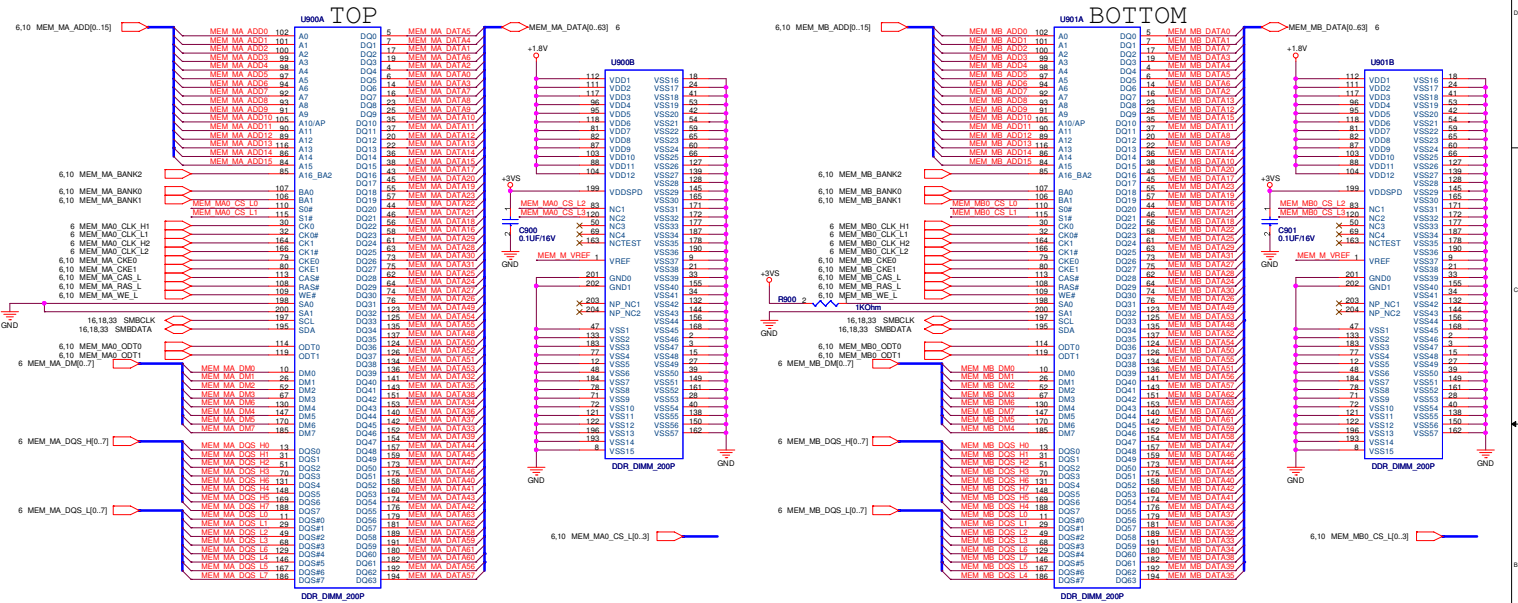
ASUS Logo
ASUSTECH CO. LTD.
Title: A7K
Engineer: Endy Zhang
Size: Custom
Project Name: Turion CNRL/DEBUG/THERM
Date: 2007.07.14.2007
Sheet: 7 of 69

<< Kennedy_Zhang >>

DRAM_VTT 0.9V

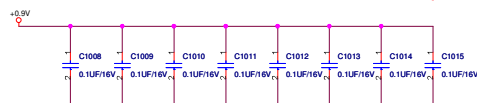
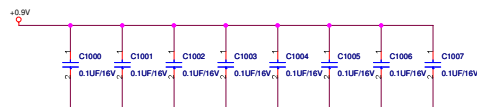
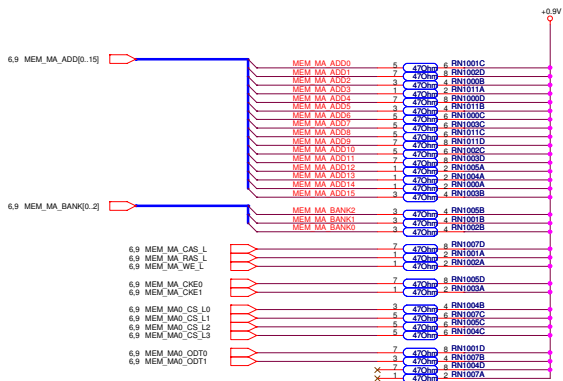


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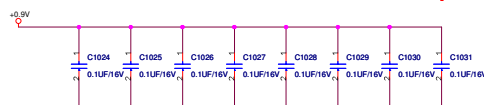
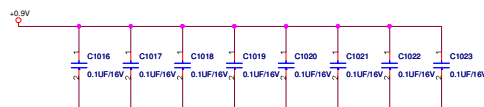
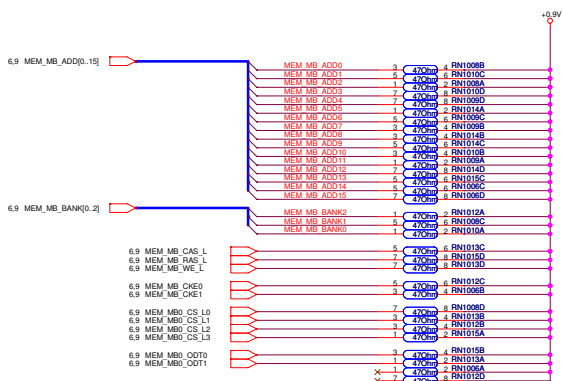


ASUS Title: **A7K**
 ASUSTECH CO. LTD. Engineer: **Endy Zhang**
 Size: Project Name: **DDR2 SODIMM** Rev: **2.0**
 Date: 2007.07.14.2007 Sheet: **9** of **99**

<< Kennedy_Zhang >>

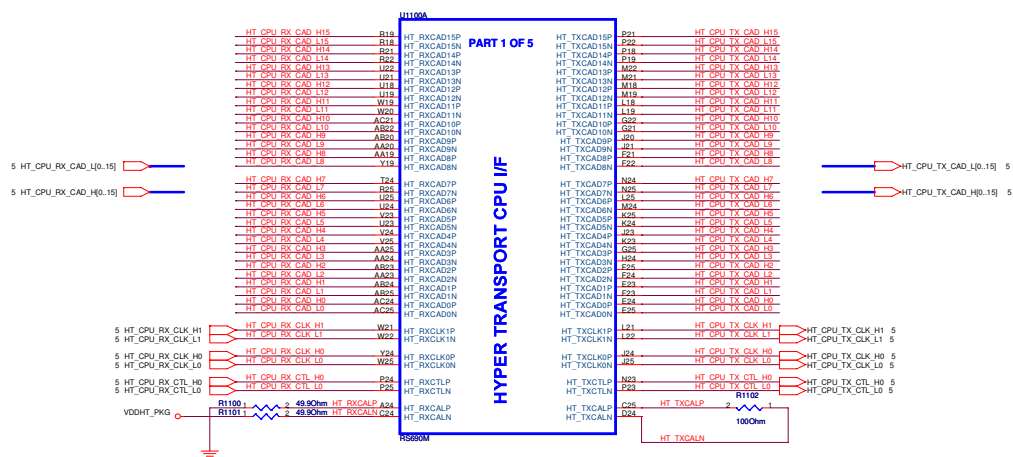


place behind DIMMs



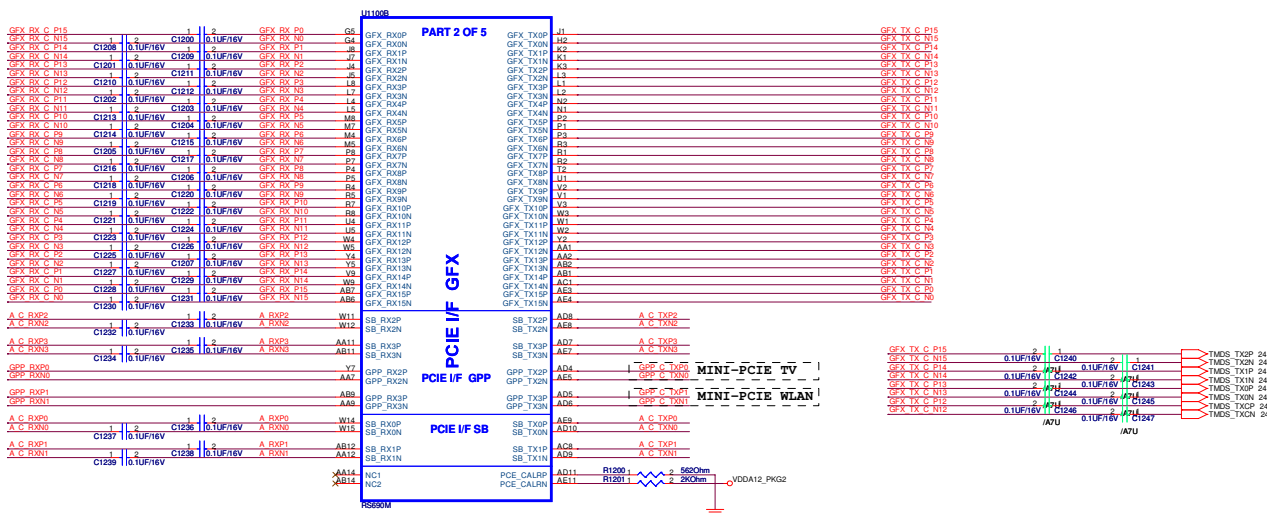
place behind DIMMs

<< Kennedy_Zhang >>

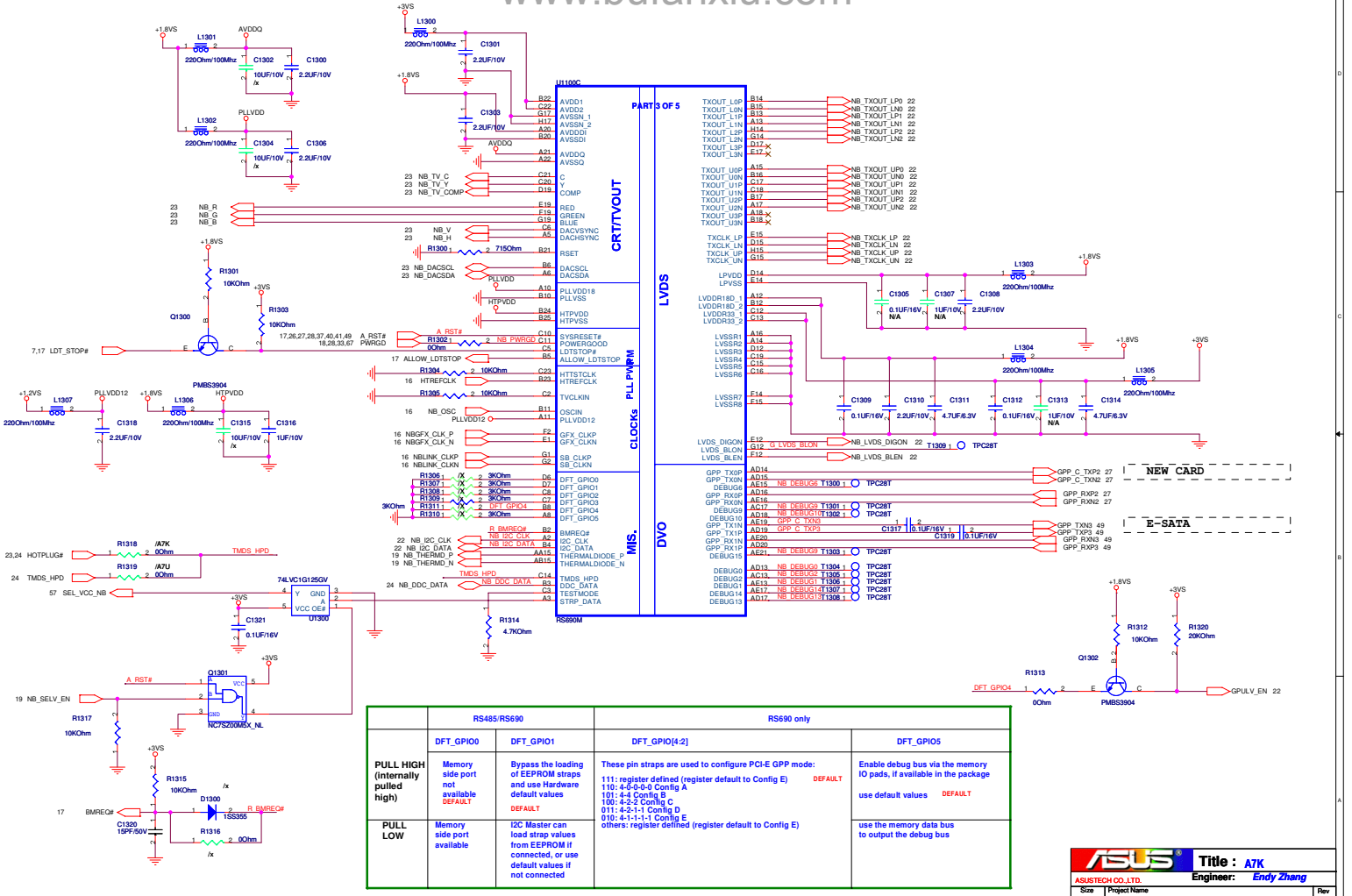


		Title : A7K
ASUSTECH CO., LTD.		Engineer : Endy Zhang
Size	Project Name	Rev
Custom	RS690M HT Link0 I/F	2.0
Date: 2007.11.14	Sheet	11 of 69

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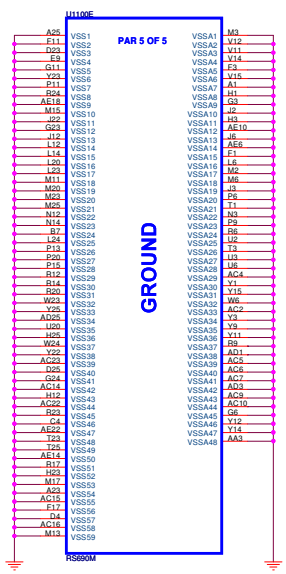
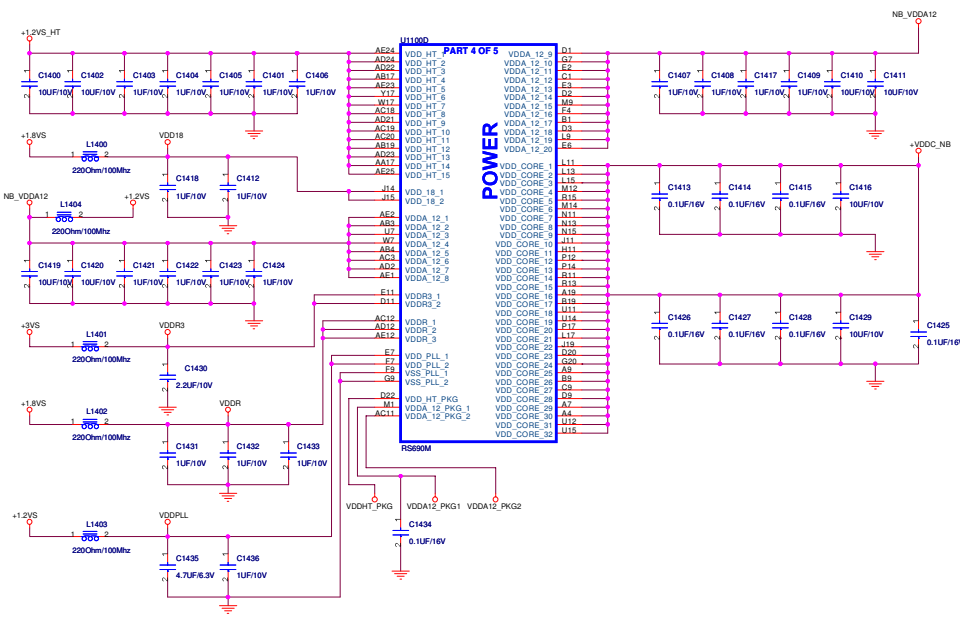
<< Kennedy_Zhang >>



	RS485/RS690		RS690 only	
	DFT_GPI00	DFT_GPI01	DFT_GPI0[4:2]	DFT_GPI05
PULL HIGH (internally pulled high)	Memory side port not available DEFAULT	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	These pin straps are used to configure PCIe GPP mode: 111: register defined (register default to Config E) 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1-1 Config E others: register defined (register default to Config E)	Enable debug bus via the memory IO pads, if available in the package use default values DEFAULT
PULL LOW	Memory side port available	I2C Master can load strap values from EEPROM if connected, or use default values if not connected		use the memory data bus to output the debug bus

ASUS Title: **A7K**
 ASUSTECH CO., LTD. Engineer: **Endy Zhang**
 Size: Project Name: **RS690M System I/F & CLKGEN** Rev: **2.0**
 Custom: Date: **2007.12.15.2007** Sheet: **13** of **19**

<< Kennedy_Zhang >>

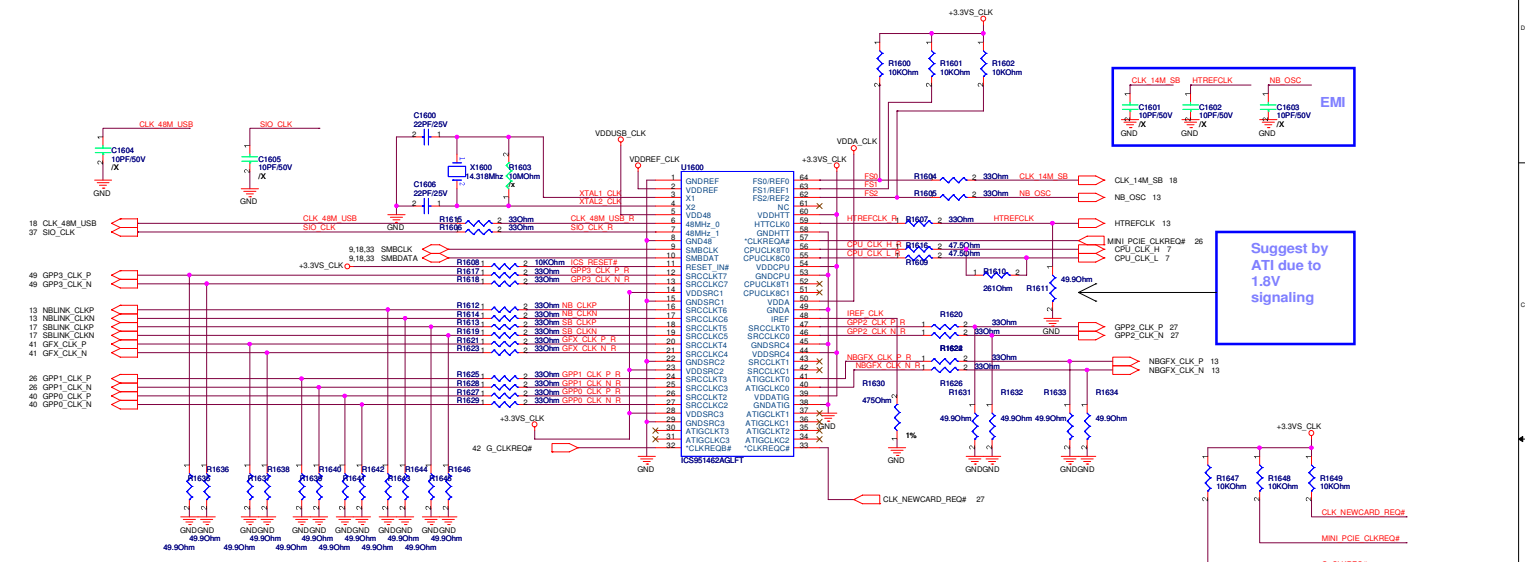


ASUS		Title : A7K
ASUSTECH CO., LTD.	Engineer: Endy Zhang	
Size	Project Name	Rev
Custom	RS690M Power	2.0
Date: 2007.07.14.2007	Sheet	14 of 69

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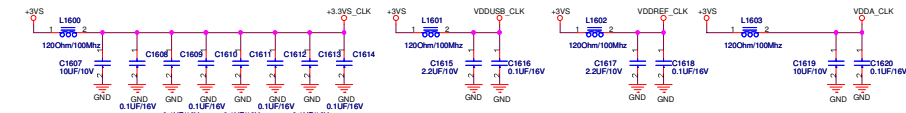
		Title : A7KM
ASUSTECH CO., LTD.		Engineer: <i>Andy Zhang</i>
Size	Project Name	Rev
Custom	<Doc>	2.0
Date: 2007.11.14		Sheet 15 of 69

<< Kennedy_Zhang >>



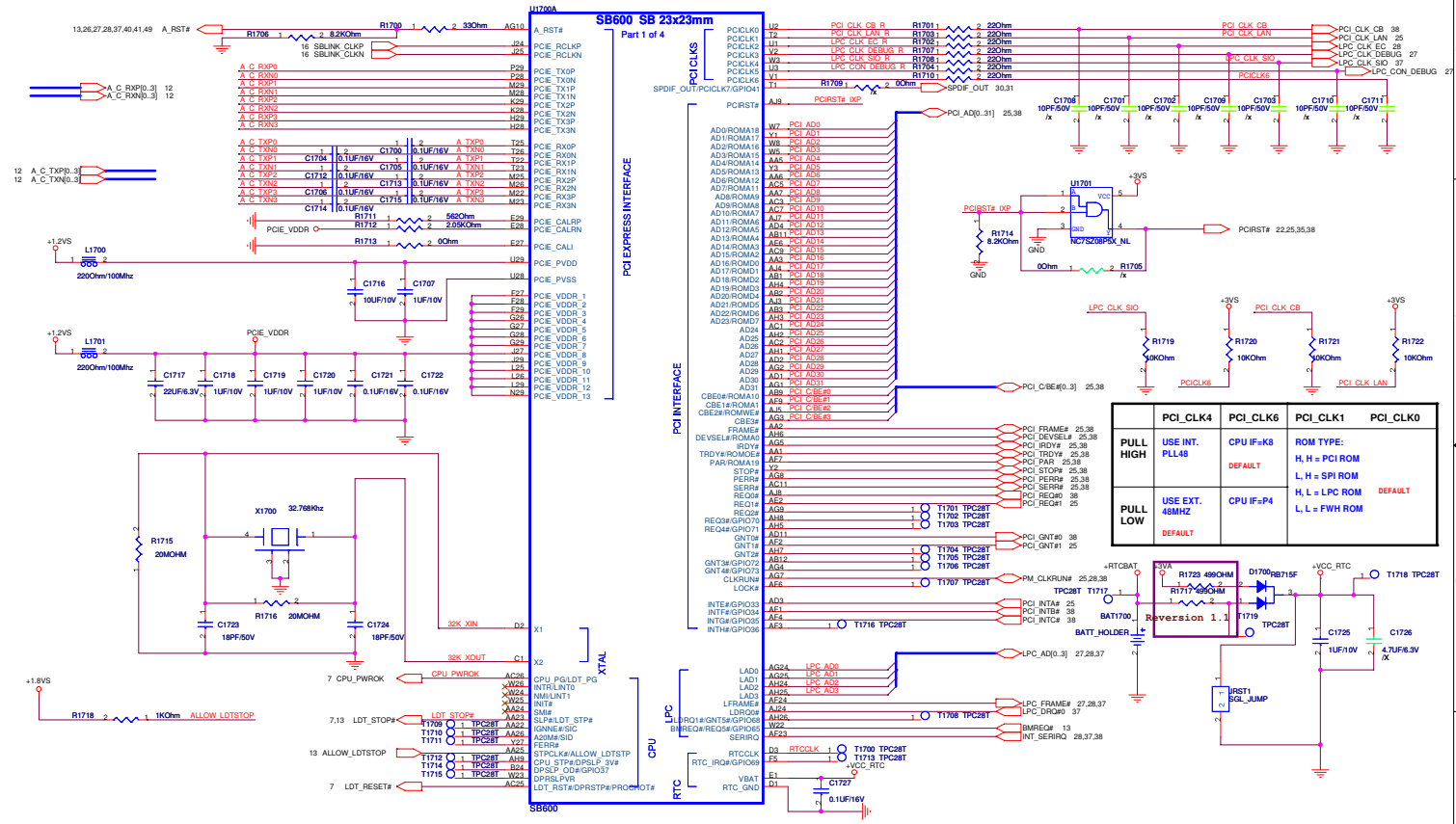
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCLK [F-1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



ASUS Title: A7K
 ASUSTECH CO. LTD. Engineer: Endy Zhang
 Size: Custom Project Name: External Clock Generator Rev: 2.0
 Date: 2007.07.14.2007 Sheet: 16 of 69

<< Kennedy_Zhang >>



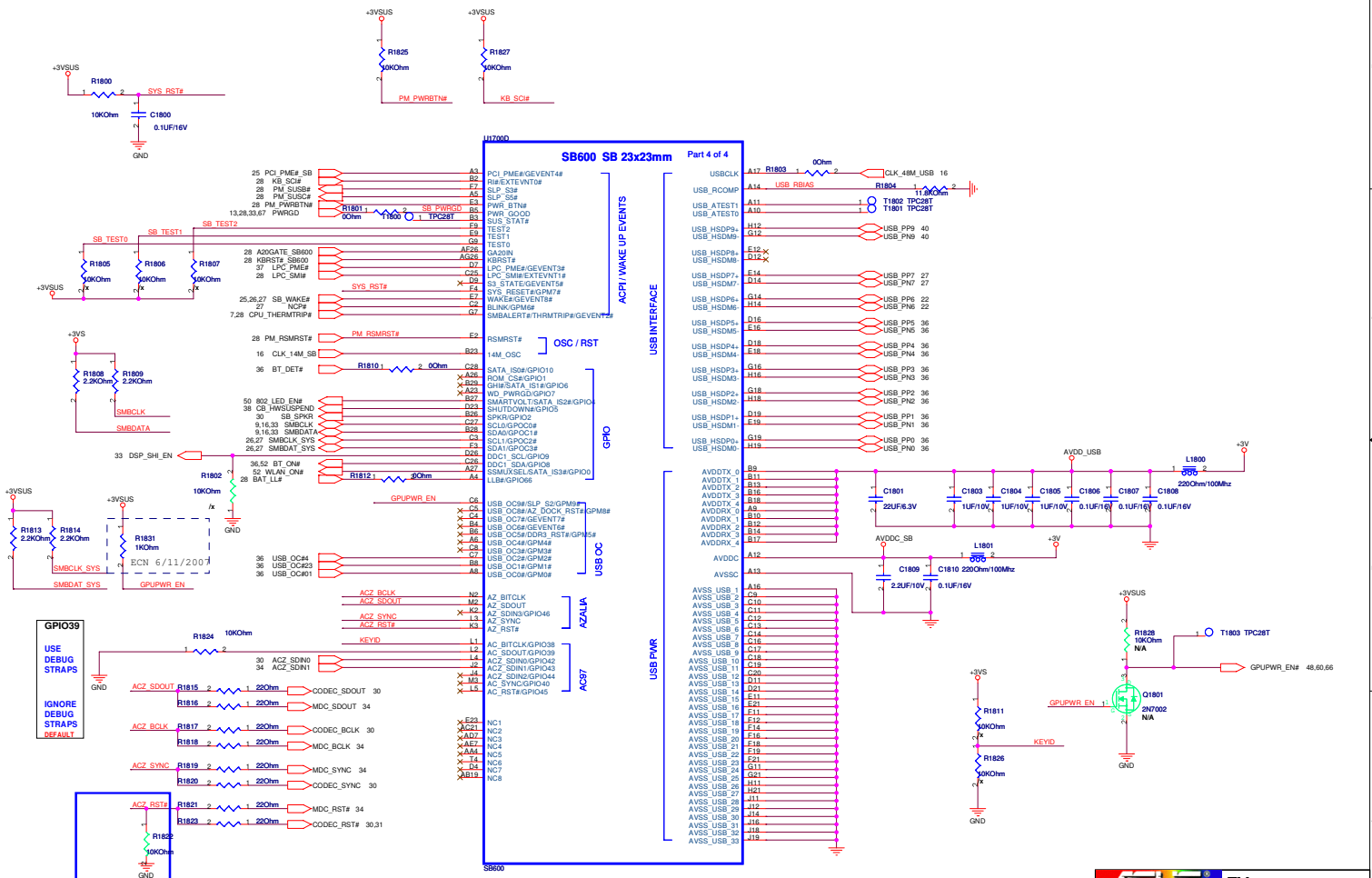
	PCI_CLK4	PCI_CLK6	PCI_CLK1	PCI_CLK0
PULL HIGH	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM L, H = SPI ROM L, L = LPC ROM	DEFAULT
PULL LOW	USE EXT. 48MHZ	CPU IF=P4	H, L = FWH ROM	DEFAULT

ASUS Title: **A7K**

ASUSTECH CO., LTD. Engineer: **Endy Zhang**

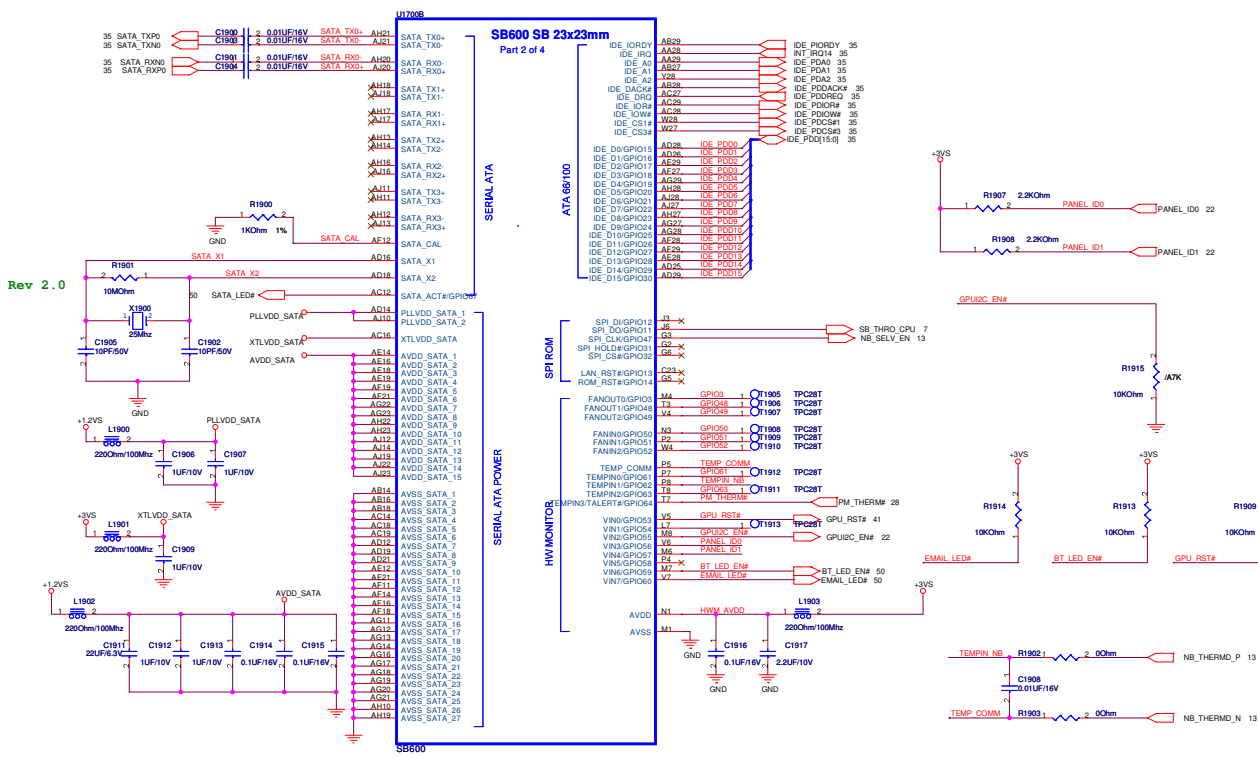
Size: [] Project Name: []
 Custom: **SB600 PCIE/PCI/CPU/LPC** Rev: 2.0
 Date: 2008-11-15 2007 Sheet 17 of 18

<< Kennedy_Zhang >>



ASUS		Title : ATK
ASUSTECH CO., LTD.		Engineer: Endy Zhang
SB600 ACPI/GPIO/USB/AC97/AZA		Rev: 2.0
Date: 2007.12.14.2007	Sheet: 18	of 28

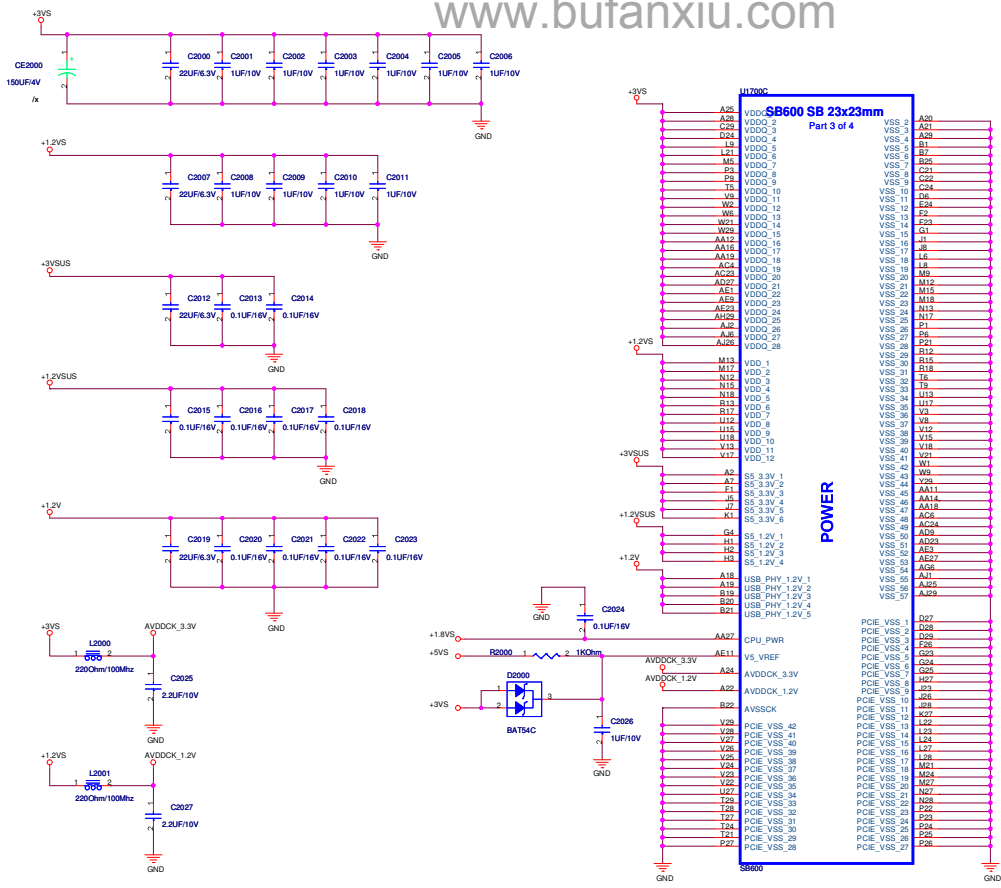
<< Kennedy_Zhang >>



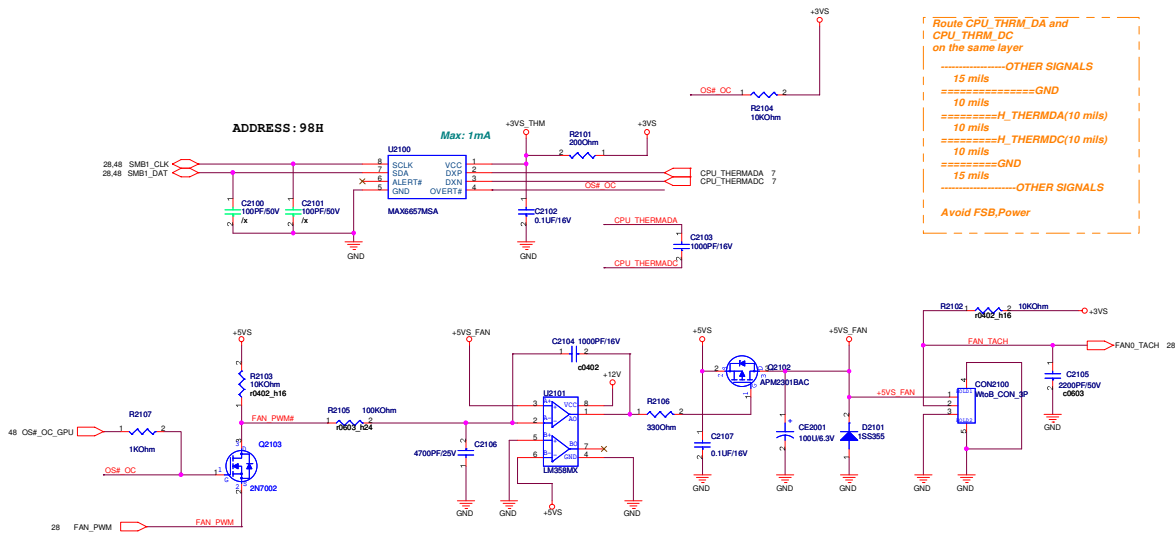
Rev 2.0

ASUS		Title : A7K
ASUSTECH CO., LTD.		Engineer: Endy Zhang
Size	Project Name	Rev
Custom	SB600 SATA/IDE/HWM/SPI	2.0
Date: 2007.07.14.2007	Sheet	19 of 69

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



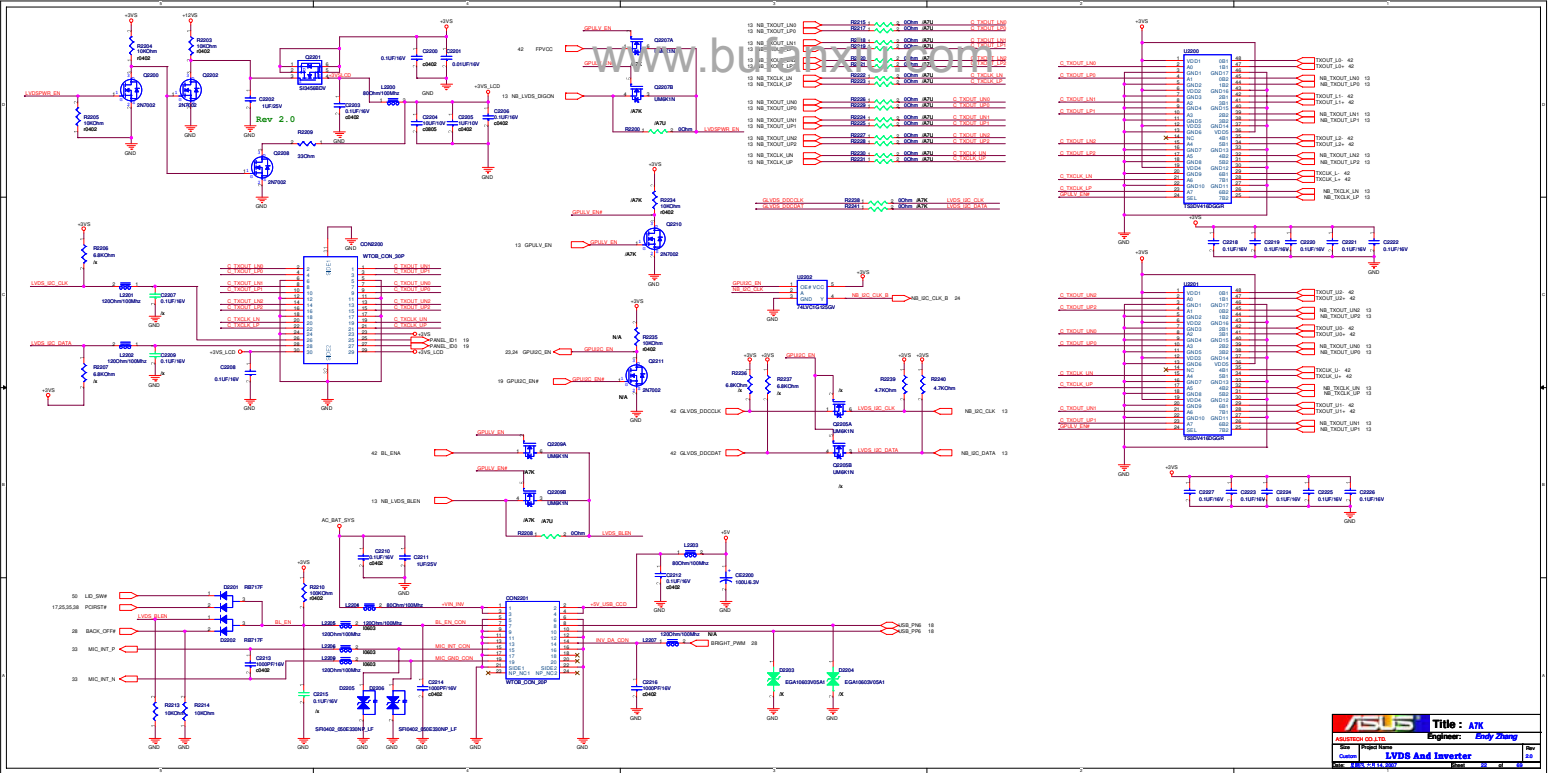
Route CPU_THRM_DA and CPU_THRM_DC on the same layer

-----OTHER SIGNALS
15 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
15 mils
-----OTHER SIGNALS

Avoid FSB_Power

ASUS		Title : ATK	
ASUSTECH CO.,LTD.		Engineer: Endy Zhang	
Size	Project Name	Rev	
Custom	Thermal Fan Control	2.0	
Date: 2007.12.14.2007	Sheet	21	of 29

<< Kennedy_Zhang >>

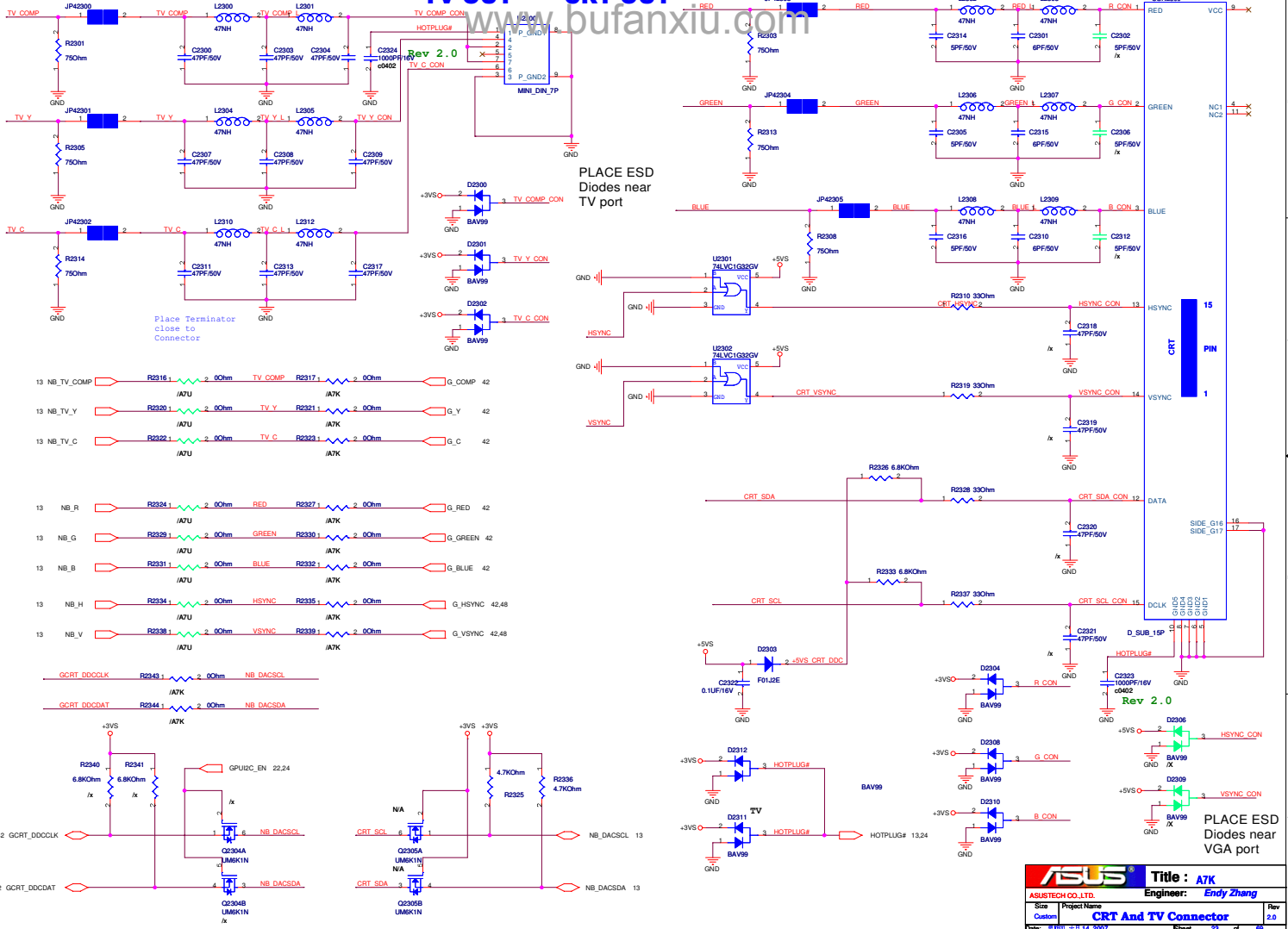


<< Kennedy_Zhang >>

L change to 09G023472000!!!!

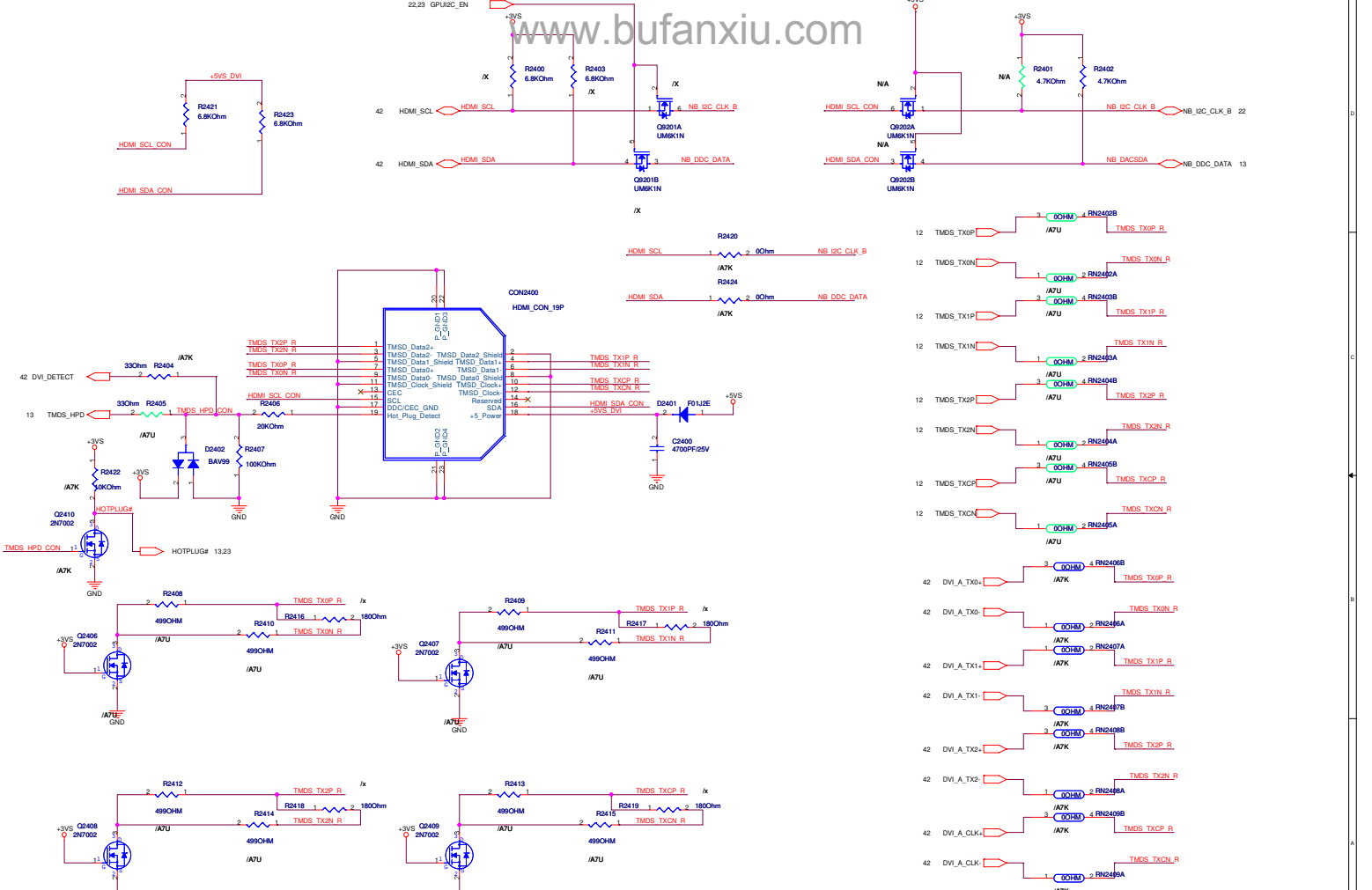
TV OUT CRT OUT

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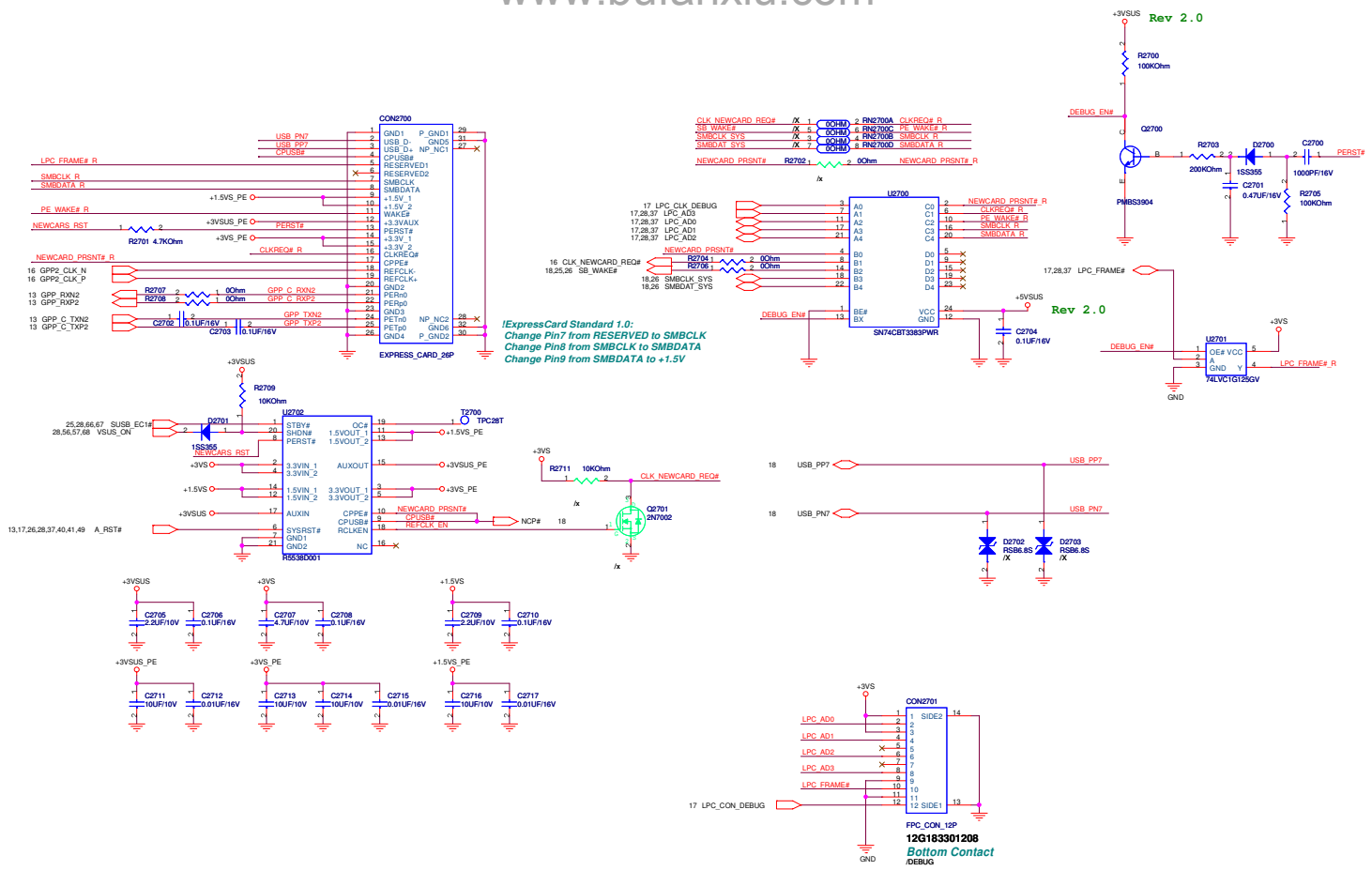
ASUS Title: A7K
 ASUSTECH CO. LTD. Engineer: Endy Zhang
 Size: Custom Project Name: CRT And TV Connector Rev: 2.0
 Date: 2007.11.14.2007 Sheet: 23 of 69

<< Kennedy_Zhang >>



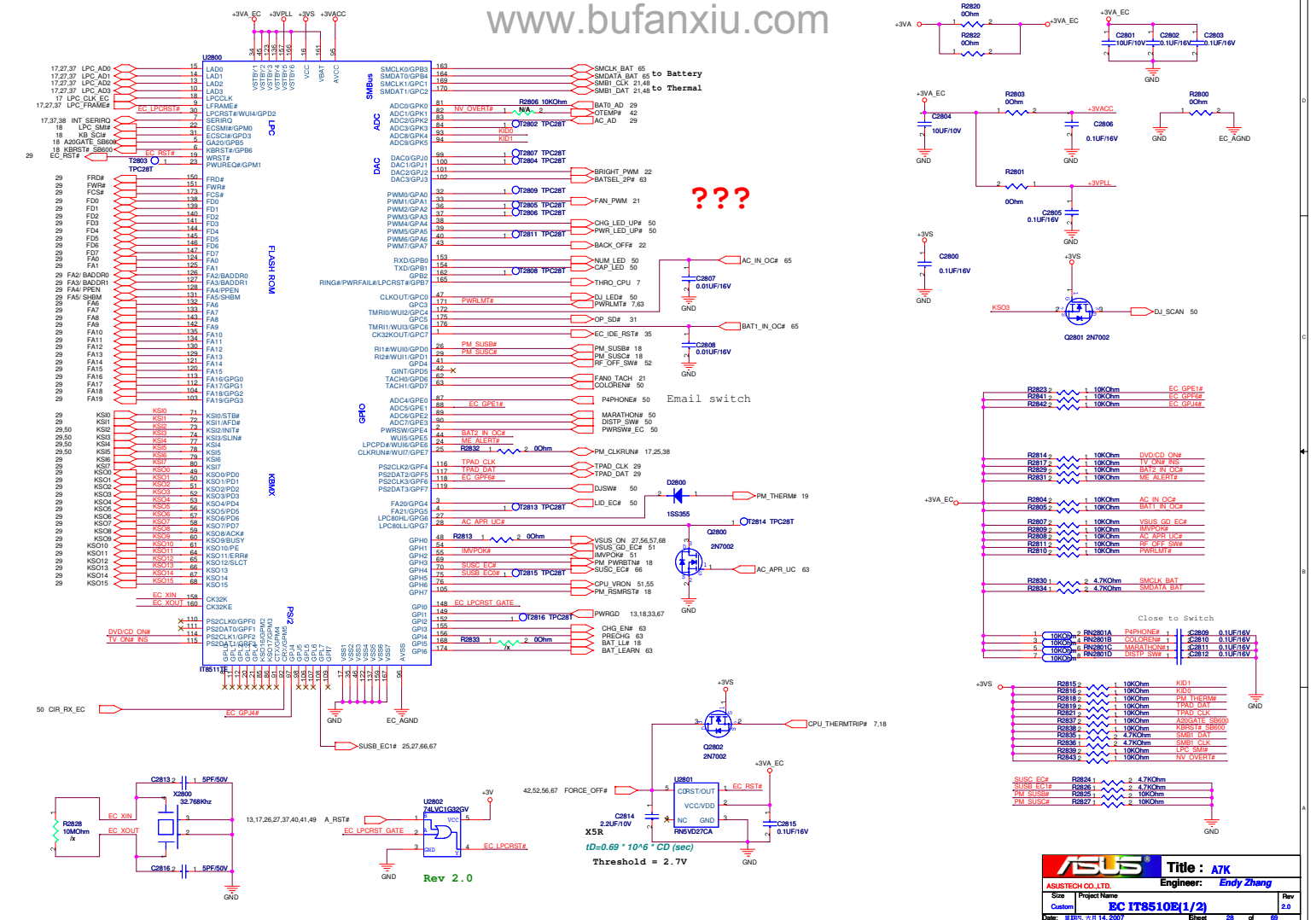
ASUS		Title : ATK	
ASUSTECH CO.,LTD.		Engineer: <i>Endy Zhang</i>	
Size	Project Name	Rev	
Custom	DVI	2.0	
Date: 2007.12.14.2007		Sheet	24 of 29

<< Kennedy_Zhang >>



ASUS		Title : A7K
ASUSTECH CO. LTD.		Engineer: Endy Zhang
Size: Custom	Project Name: New Card	Rev: 2.0
Date: 2007.11.14.2007	Sheet: 27	of 69

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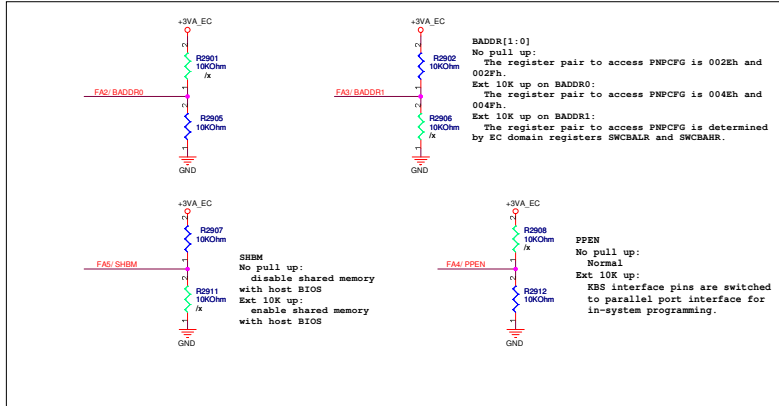
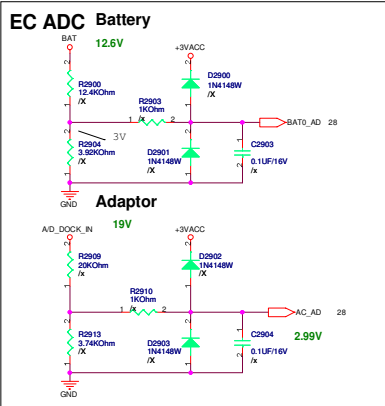
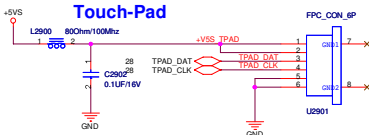
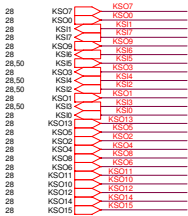
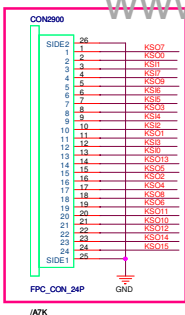
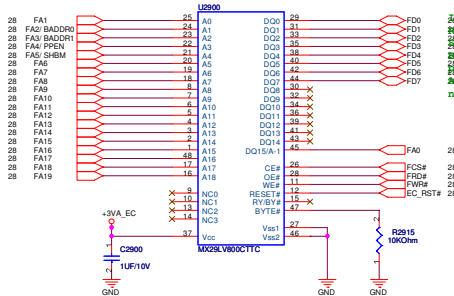


<< Kennedy_Zhang >>

ISA ROM (8Mbits)

SST-PLCC32 4Mbits Flash ROM
PN:05G001014110
(FLASH SST SST39VF040-70-4C-NHE
4M-70 PLCC-32)

If need to use 8Mbits ISA ROM, could choose SST39LF080. But it does not have PLCC32 package. ASUS does not have part number yet.



EC Hardware Strap

strap value sampled after VSTBY power up reset

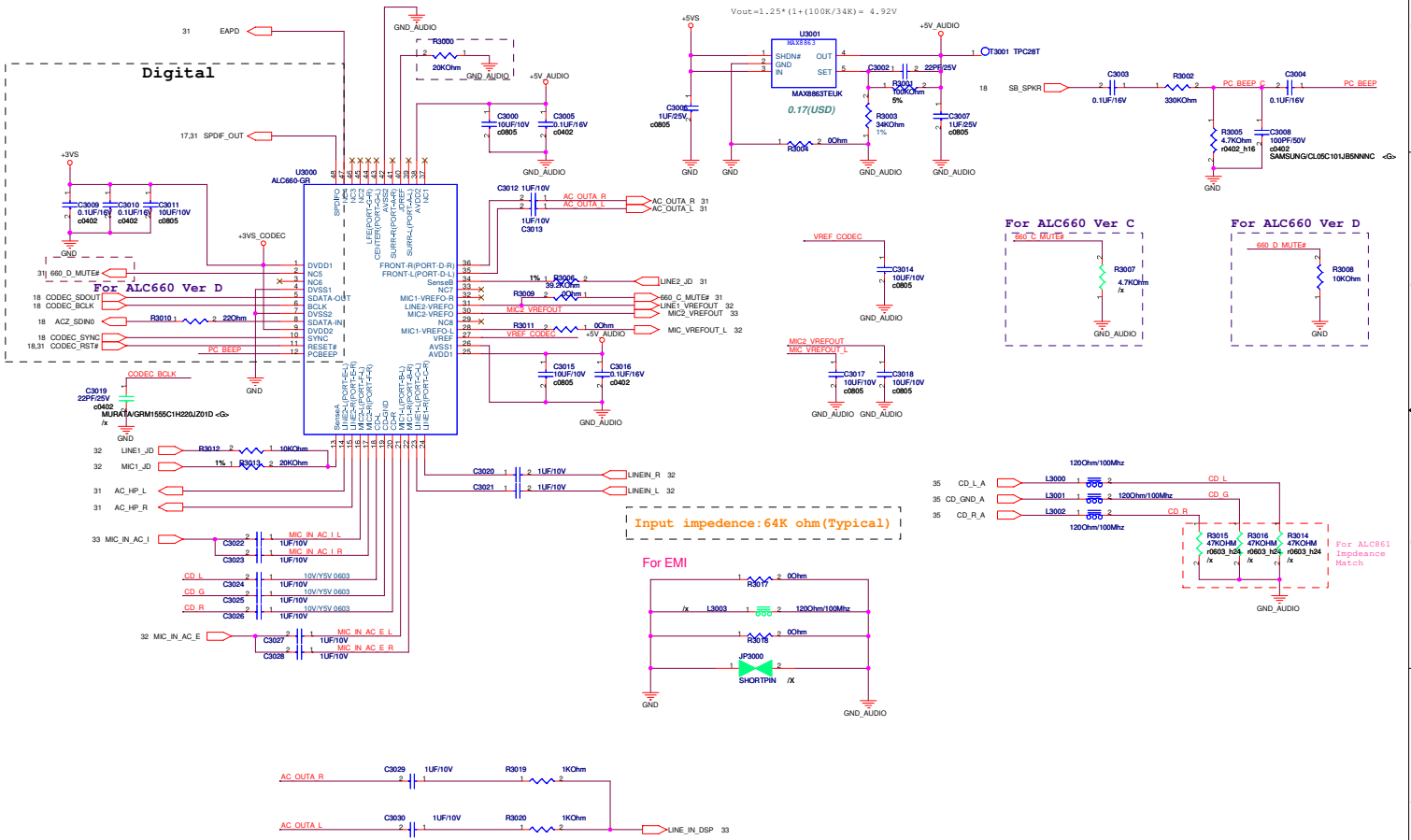
BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

SBMM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

PPEN
No pull up:
Normal
Ext 10K up:
EEP interface pins are switched to parallel port interface for in-system programming.

ASUS		Title : A7K	
ASUSTECH CO.,LTD.		Engineer: <i>Endy Zhang</i>	
Size	Project Name	Rev	
Custom	EC IT8510E(2/2)	2.0	
Date: 2008-12-14 2007	Sheet	20	of 20

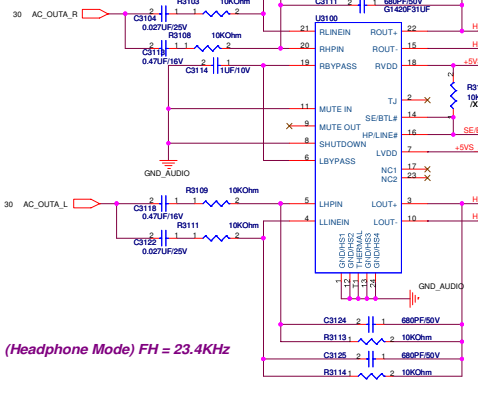
<< Kennedy_Zhang >>



ASUS		Title : A7K
ASUSTECH CO. LTD.		Engineer: Endy Zhang
Size: Custom	Project Name: ALC660	Rev: 2.0
Date: 2007.11.14	Sheet: 30	of 69

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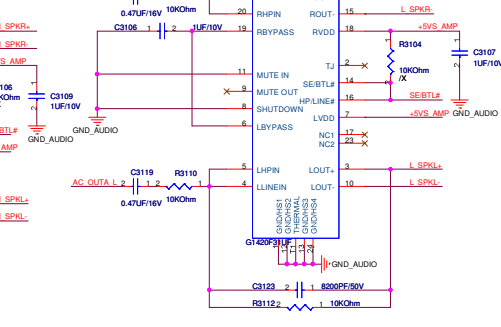
Headphone & Middle/High Range Frequency Amplifier (Tweeter)
FL = 590 Hz
FH = 23.4KHz



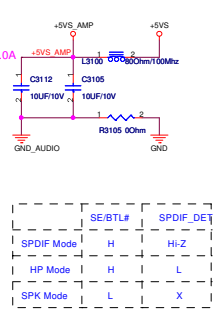
(Headphone Mode) FH = 23.4KHz

Low Range Frequency Amplifier (Woofer)

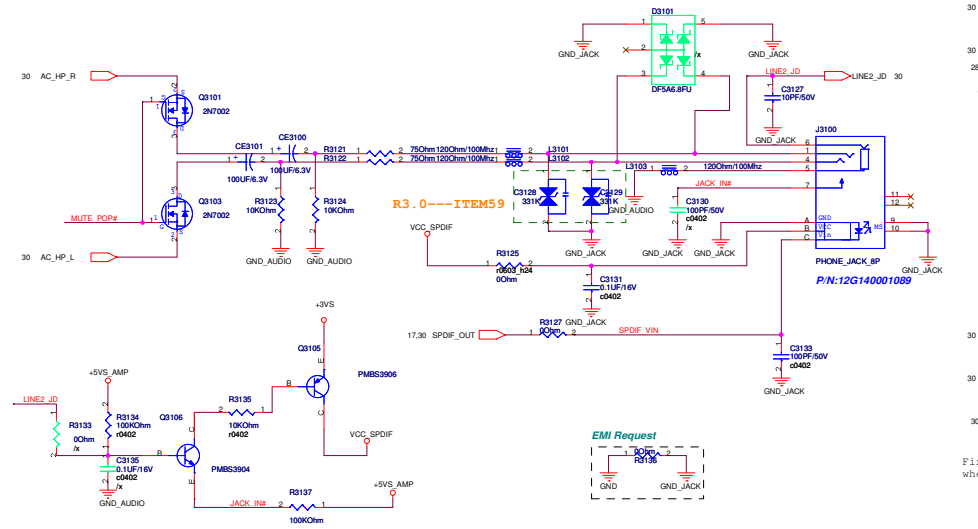
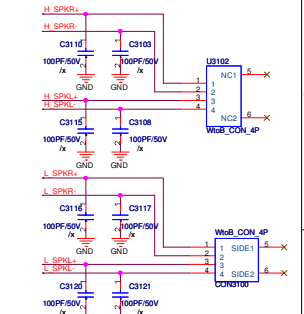
FL = 33.9 Hz
FH = 1.942 KHz



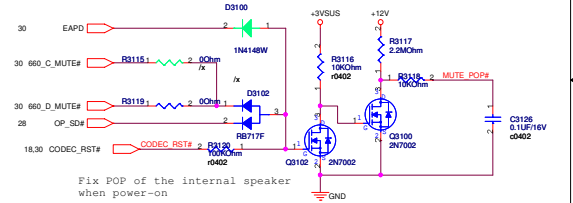
Max: 1.0A



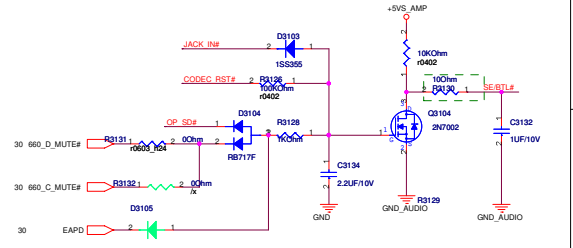
SEBTLP	SPODF_DE	
SPDIF Mode	H	H-Z
HP Mode	L	L
SPK Mode	L	X



EMI Request

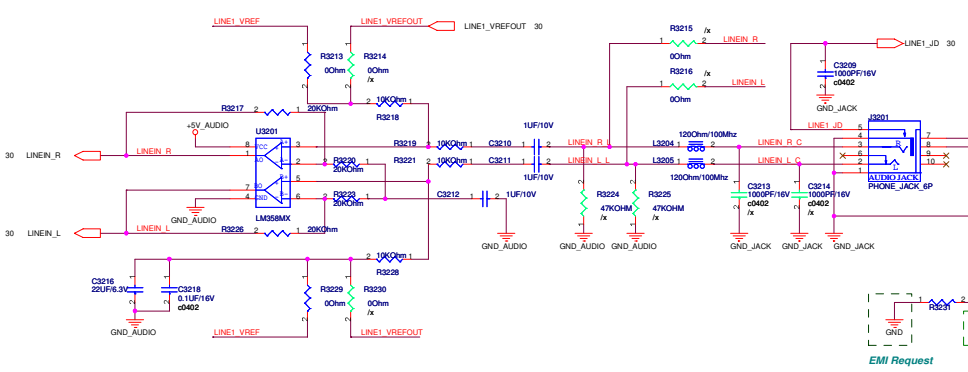
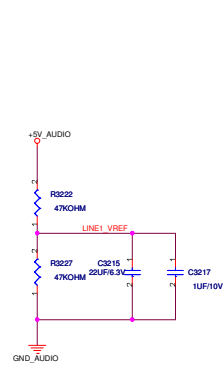
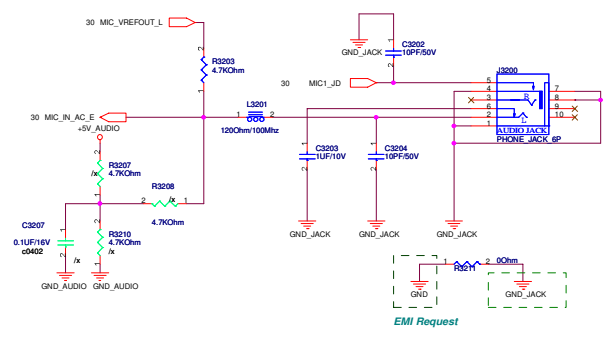


Fix POP of the internal speaker when power-on



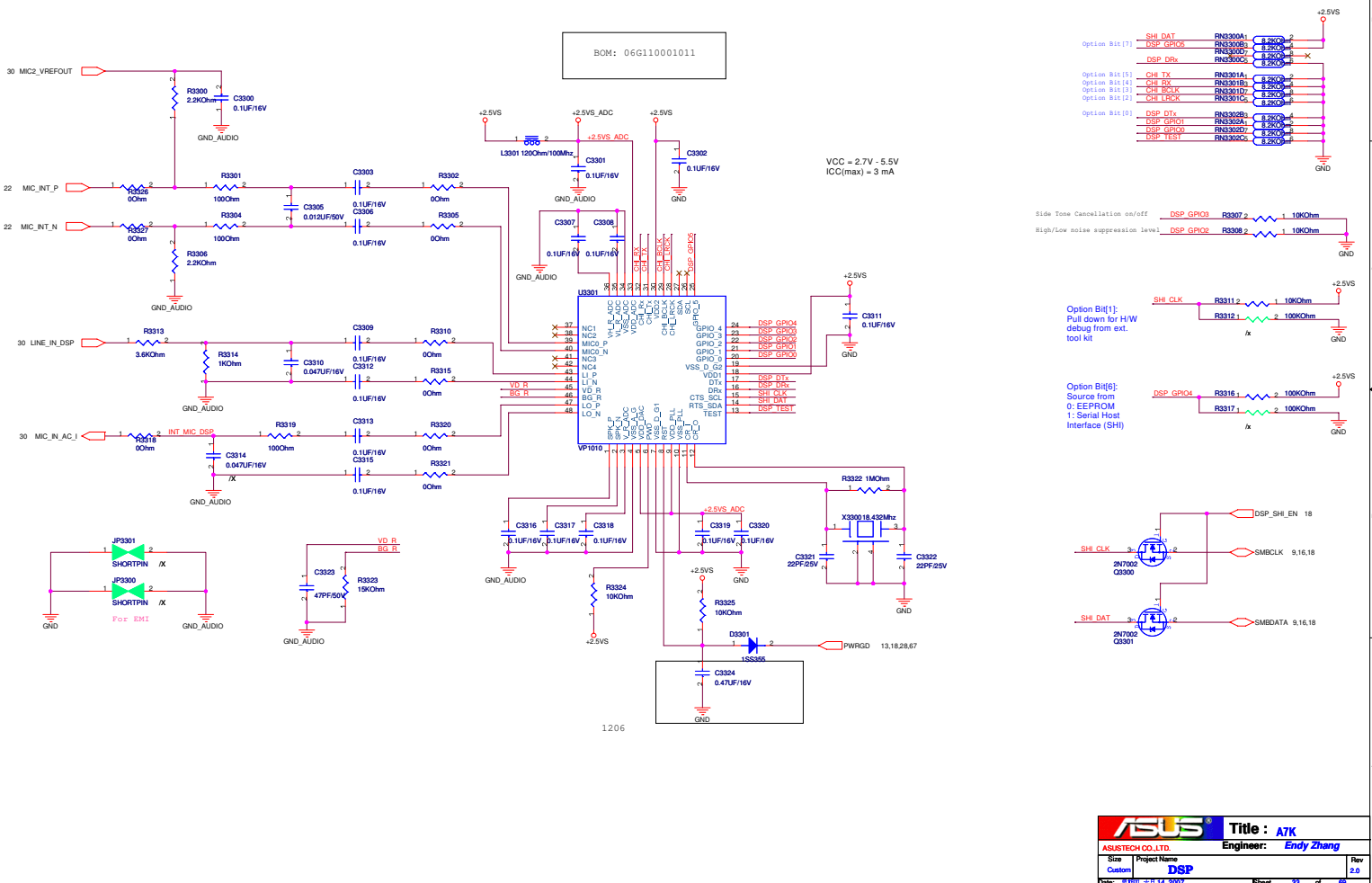
Fix POP of the internal speaker when power-off

<< Kennedy_Zhang >>



ASUS		Title : A7K
ASUSTECH CO.,LTD.		Engineer: Endy Zhang
Size	Project Name	Rev
Custom	MIC And Line in	2.0
Date: 2007.7.14	Sheet	32 of 69

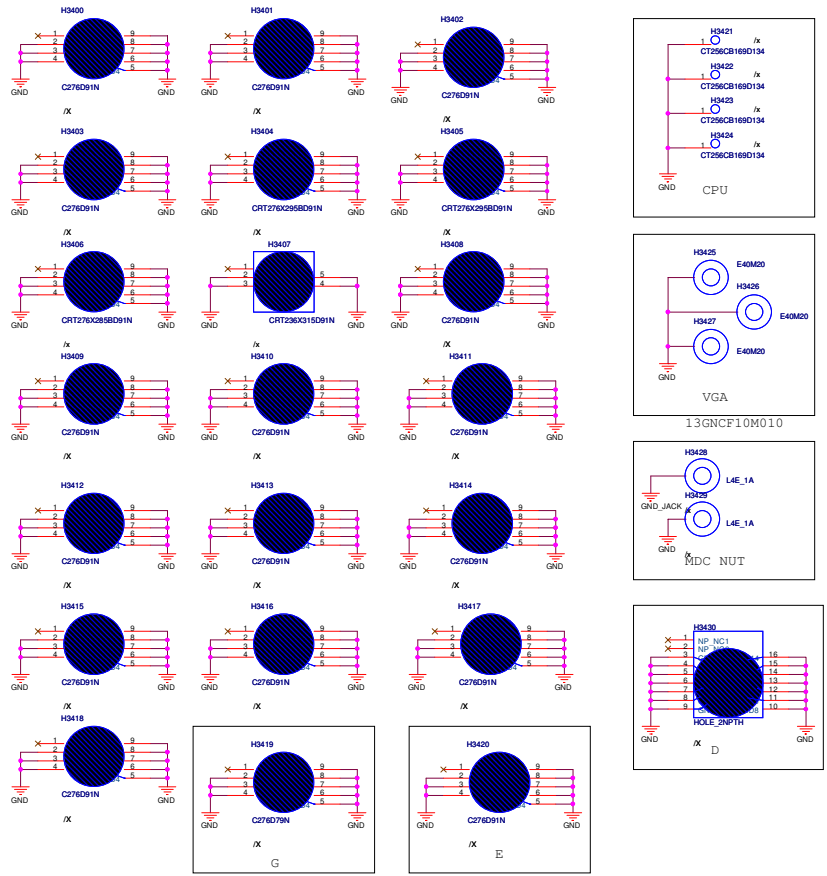
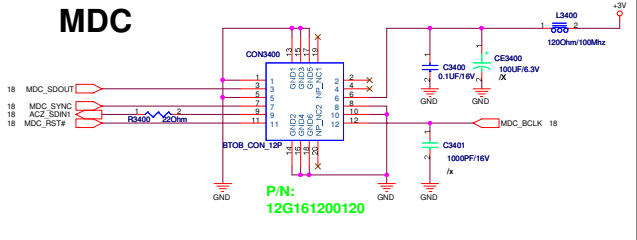
<< Kennedy_Zhang >>



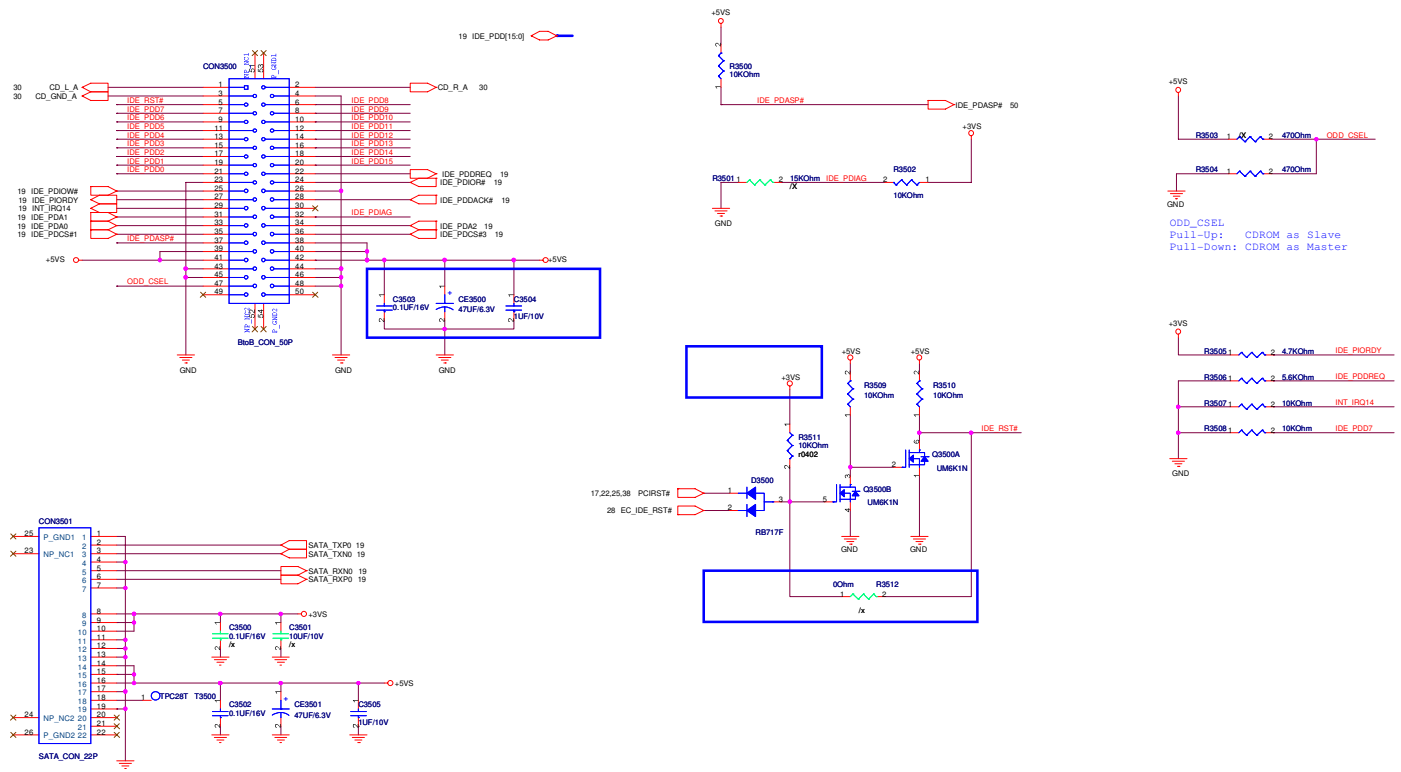
ASUS		Title : A7K
ASUSTECH CO. LTD.		Engineer: Endy Zhang
Size	Project Name	Rev
Custom	DSP	2.0
Date: 2007.11.14.2007	Sheet	33 of 69

<< Kennedy_Zhang >>

MDC

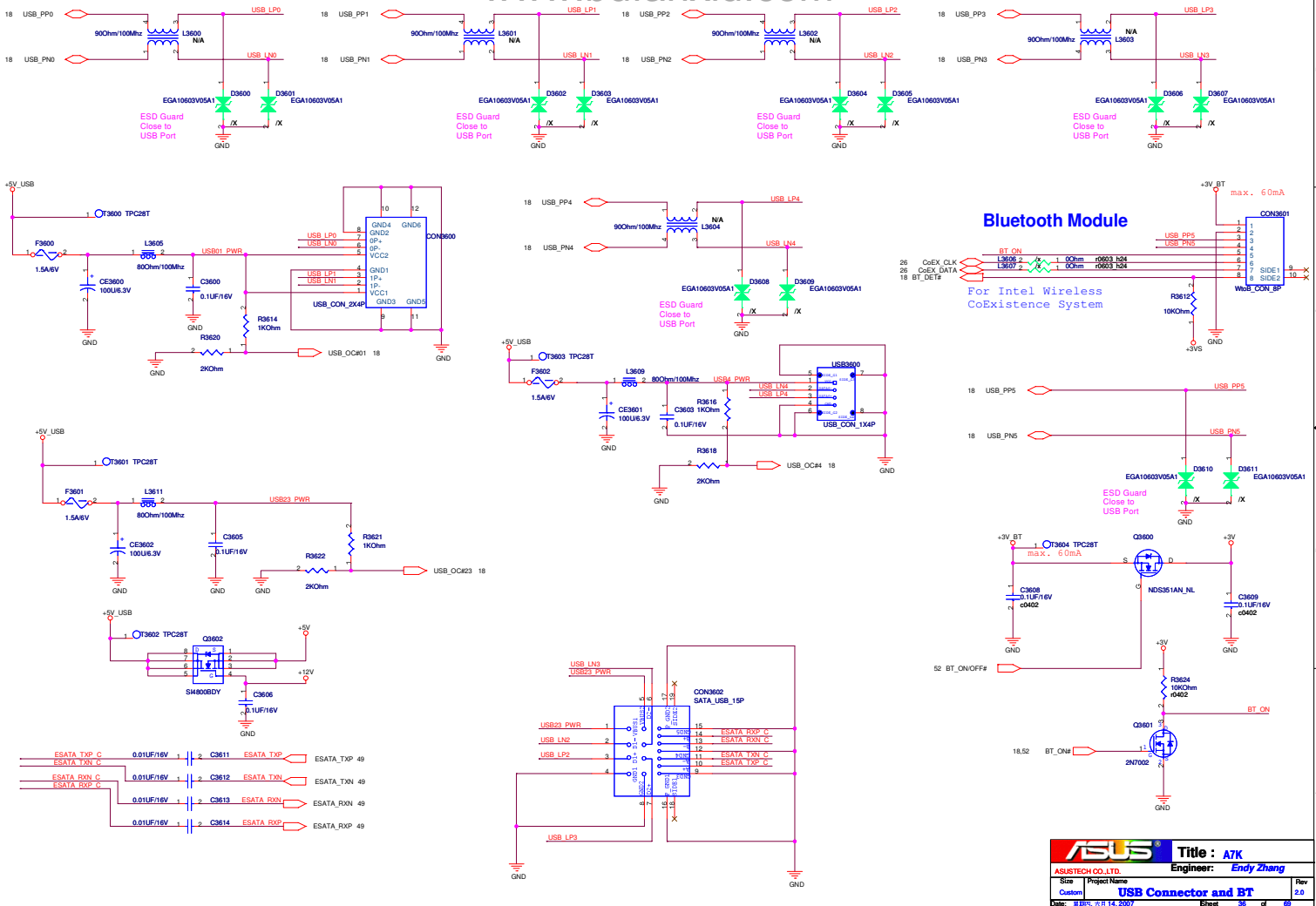


<< Kennedy_Zhang >>



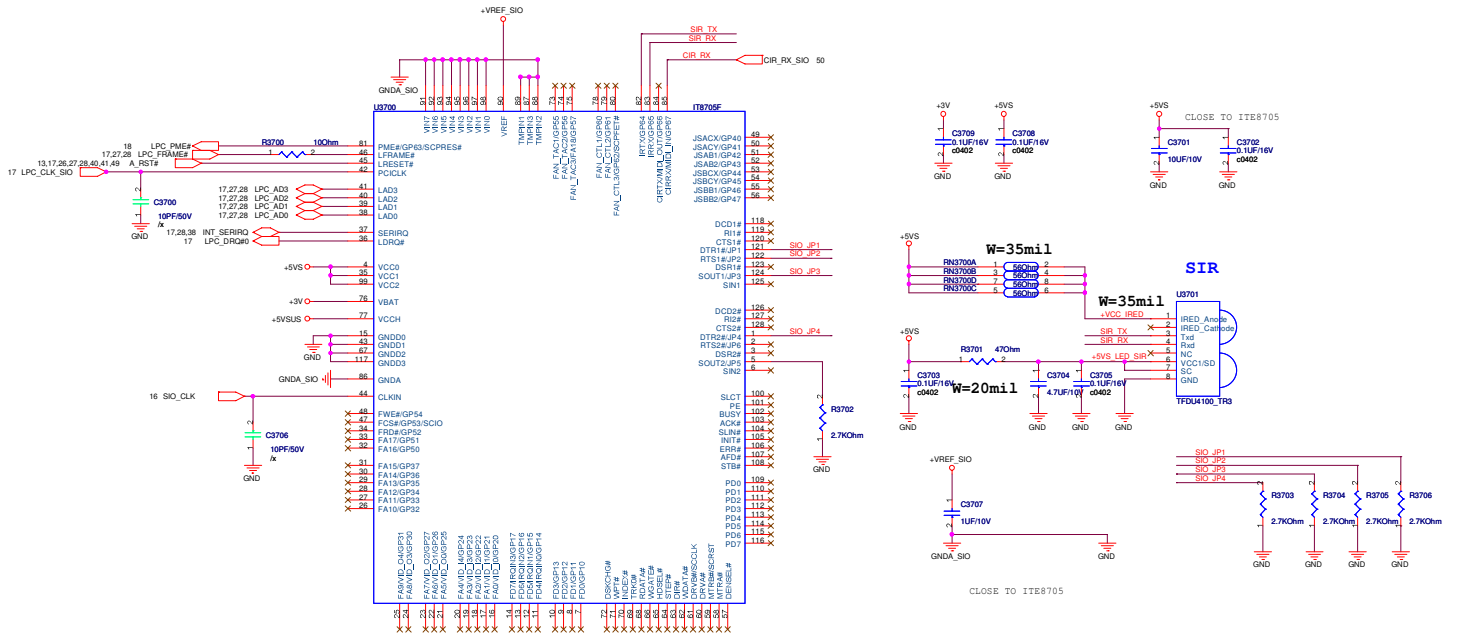
ASUS		Title : A7K
ASUSTECH CO. LTD.		Engineer: Endy Zhang
Size	Project Name	Rev
Custom	HDD And ODD	2.0
Date: 2007.11.14.2007	Sheet	35 of 69

<< Kennedy_Zhang >>



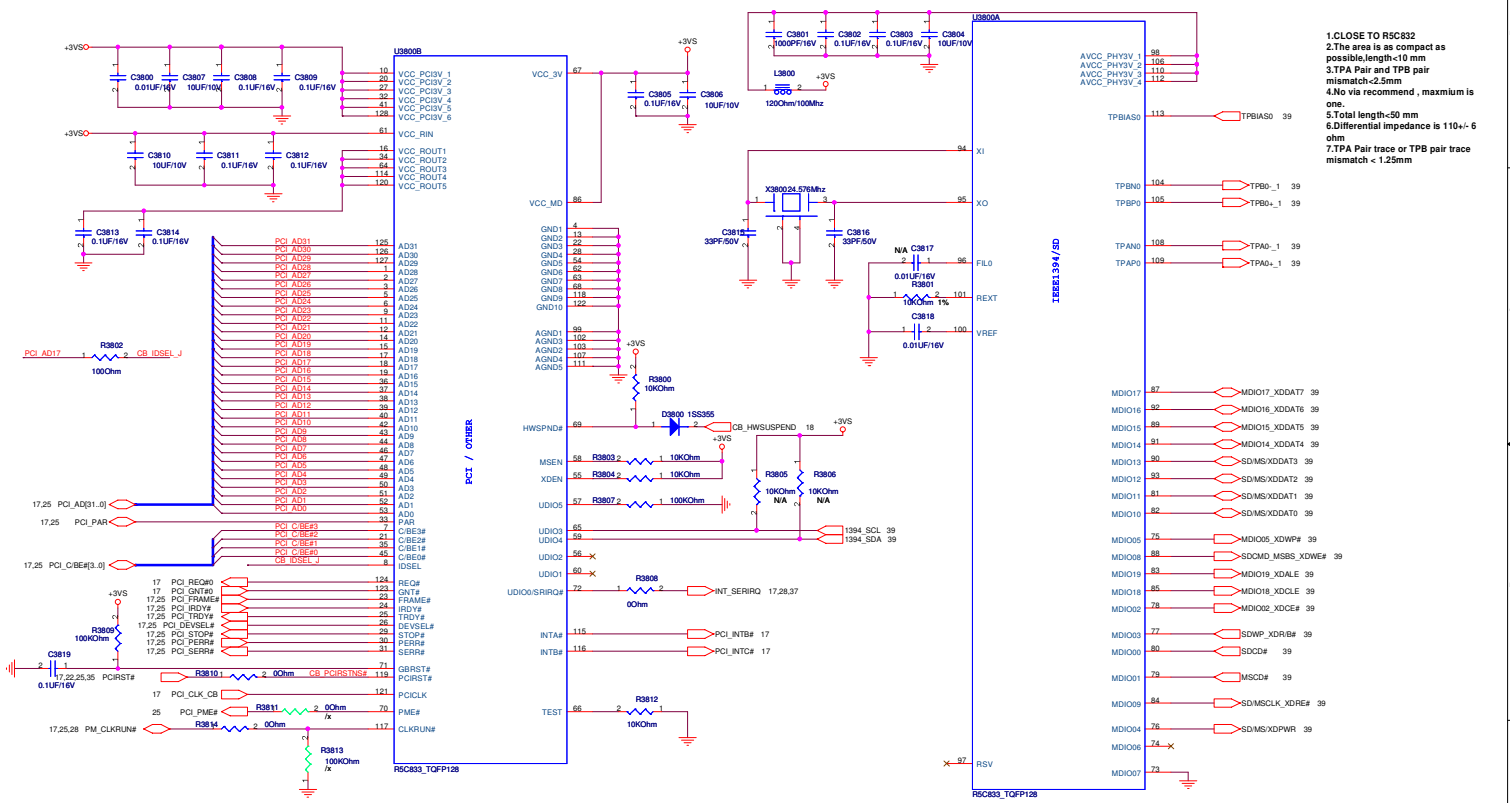
ASUS		Title : A7K	
ASUSTECH CO.,LTD.		Engineer: <i>Endy Zhang</i>	
Size	Project Name	Rev	
Custom	USB Connector and BT	2.0	
Date: 2008-11-14 2007	Sheet	36	39

<< Kennedy_Zhang >>



ASUS		Title : ATK	
ASUSTECH CO., LTD.		Engineer: Endy Zhang	
Size	Project Name	Rev	
Custom	SIO and SIR	2.0	
Date: 2007.12.14.2007		Sheet	37 of 39

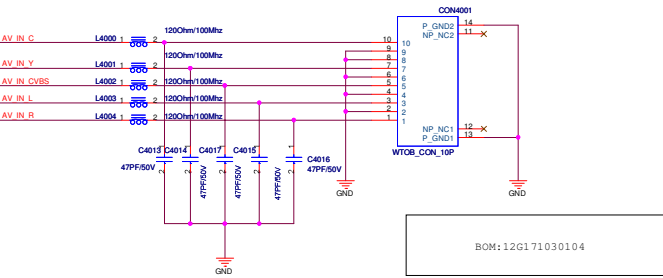
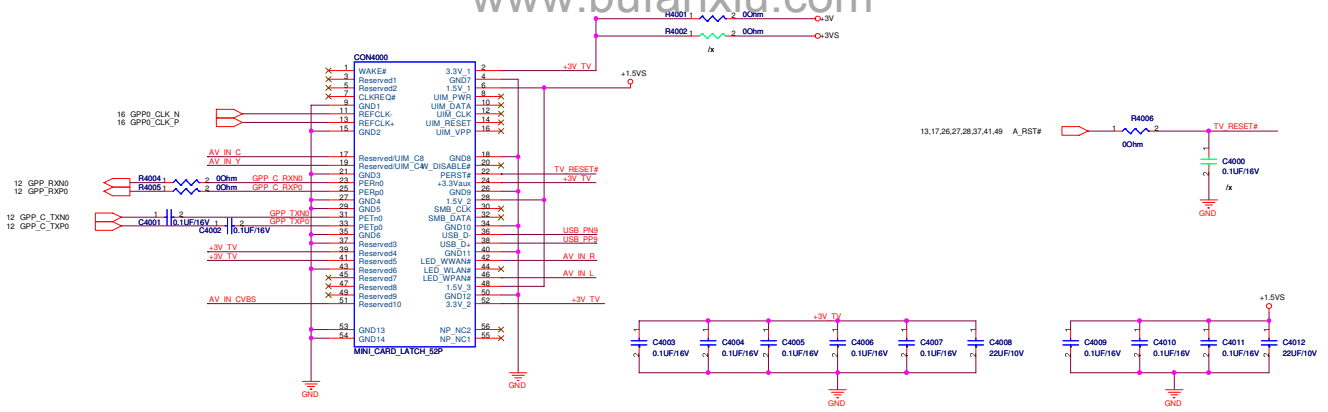
<< Kennedy_Zhang >>



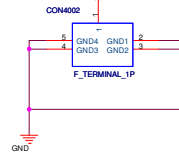
- 1. CLOSE TO R5C832
- 2. The area is as compact as possible, length < 10 mm
- 3. TPA Pair and TPB pair mismatch < 2.5mm
- 4. No via recommend, maximum is one.
- 5. Total length < 90 mm
- 6. Differential impedance is 110 ± 6 ohm
- 7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

ASUS		Title : A7K	
ASUSTECH CO., LTD.		Engineer: Endy Zhang	
Size	Project Name	Rev	
Custom	Card Bus R5C832	2.0	
Date: 2007.07.14.2007	Sheet	38	of 69

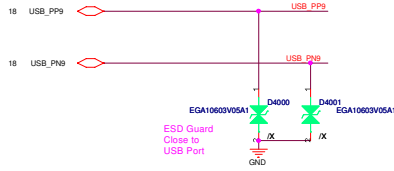
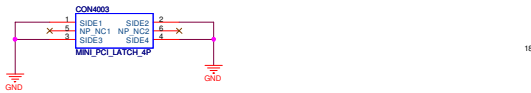
<< Kennedy_Zhang >>



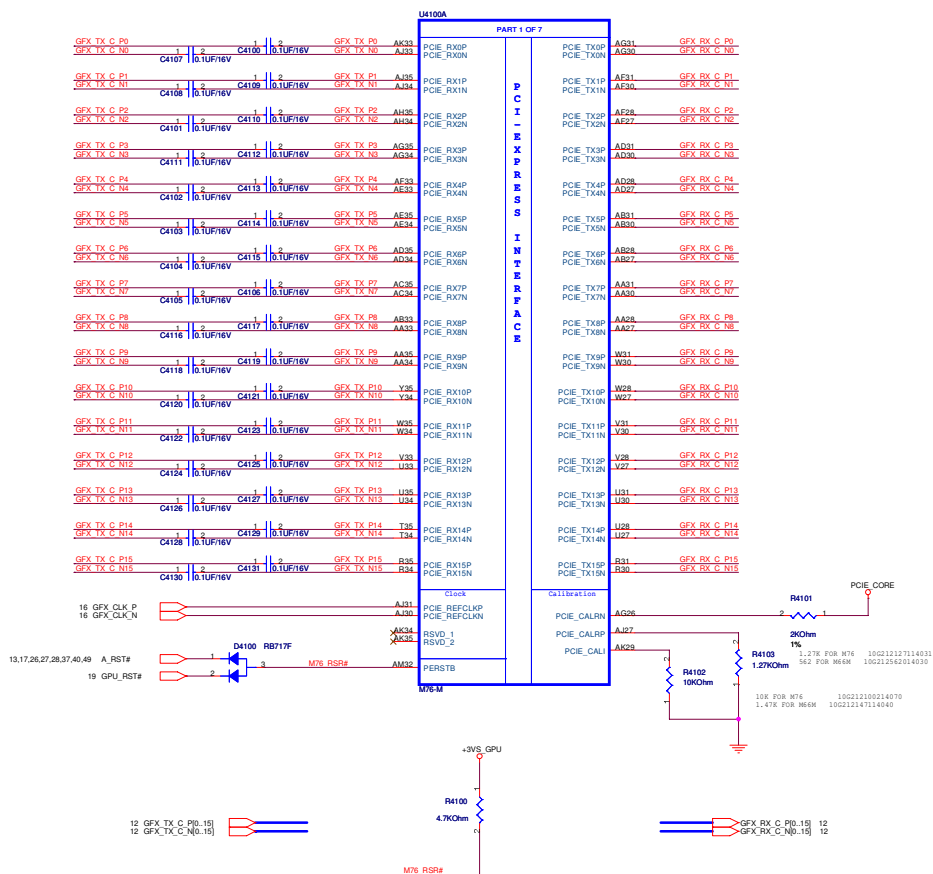
ATV_DTV_FM Antenna



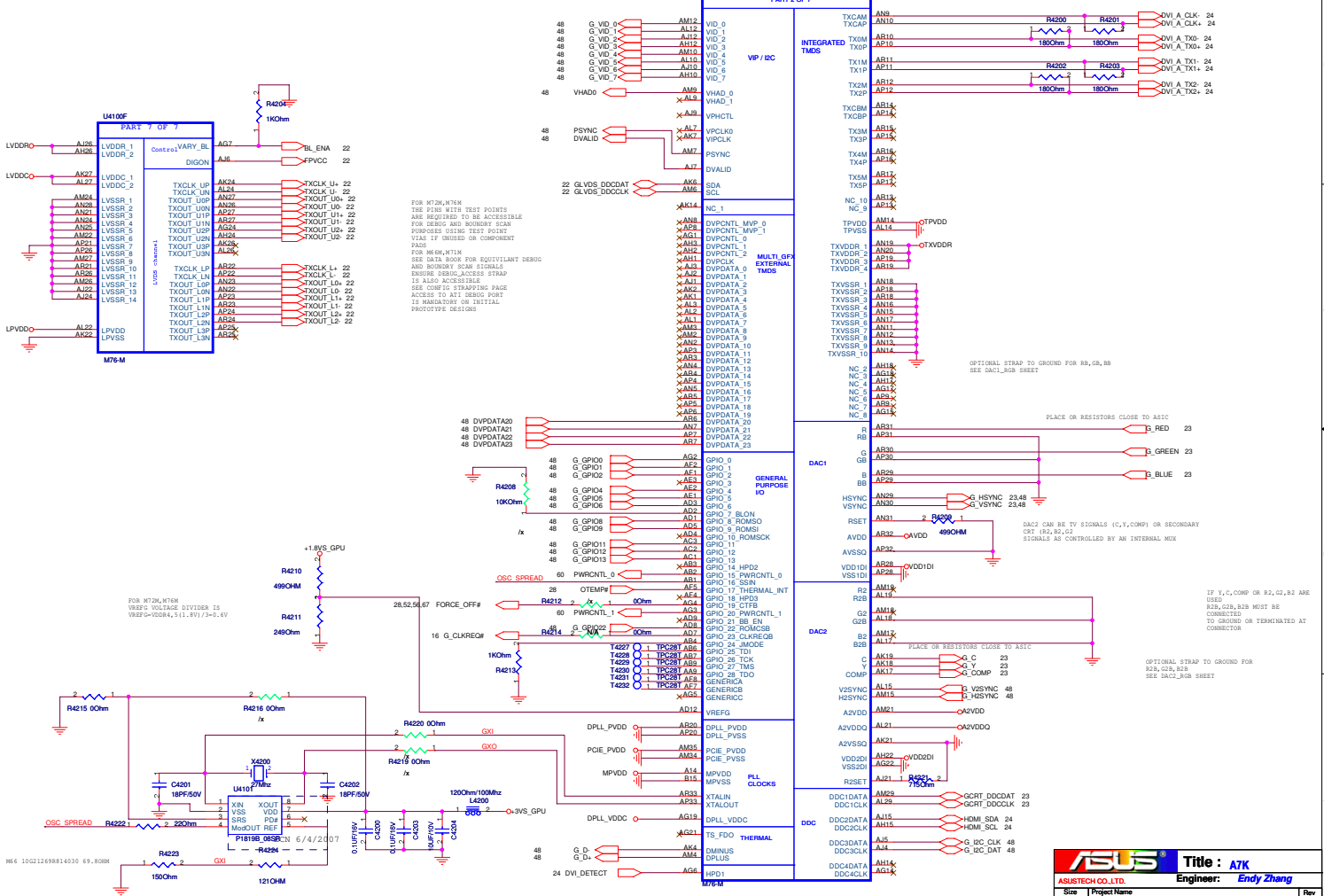
14G152075000



<< Kennedy_Zhang >>

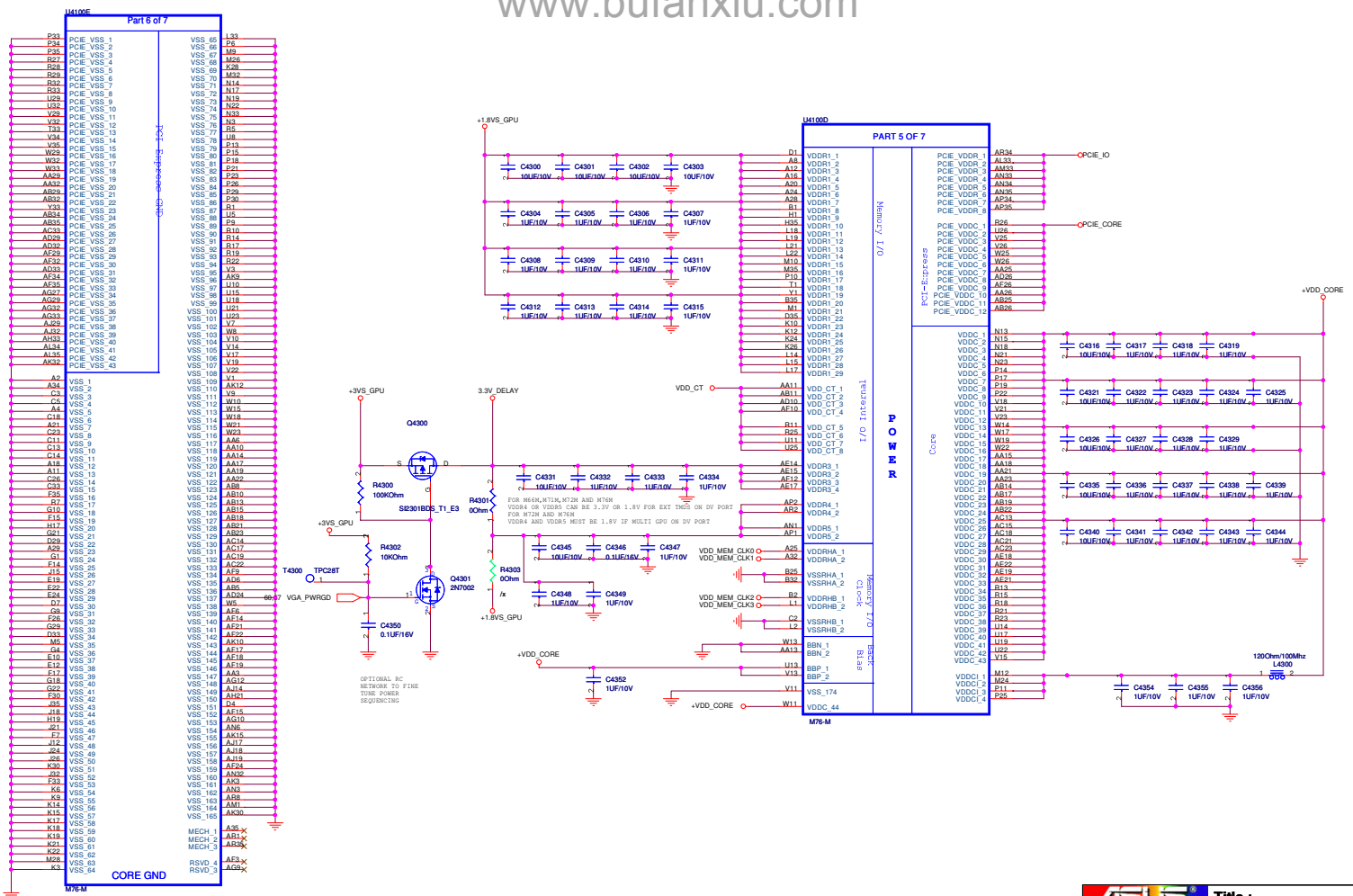


<< Kennedy_Zhang >>




<< Kennedy_Zhang >>

ASUSTECH CO. LTD.		Title : A7K	
Size	Project Name	Engineer:	Endy Zhang
Custom	M76Q2/5DVI DAC DDC VID	Date:	11/14/2007
		Sheet	42 of 69

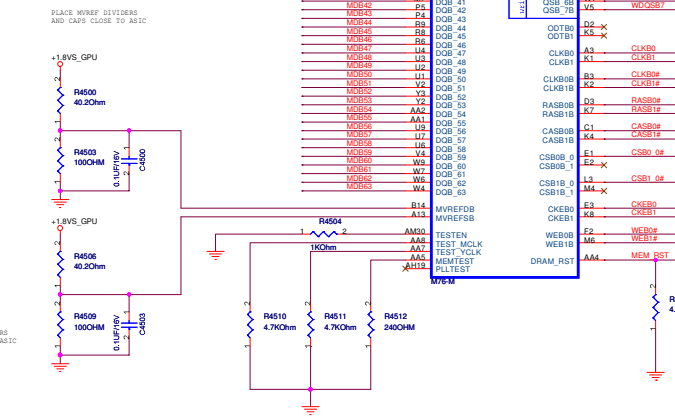
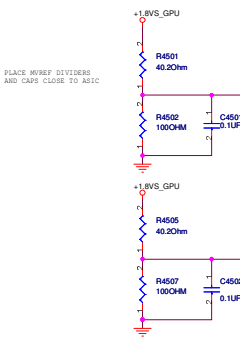
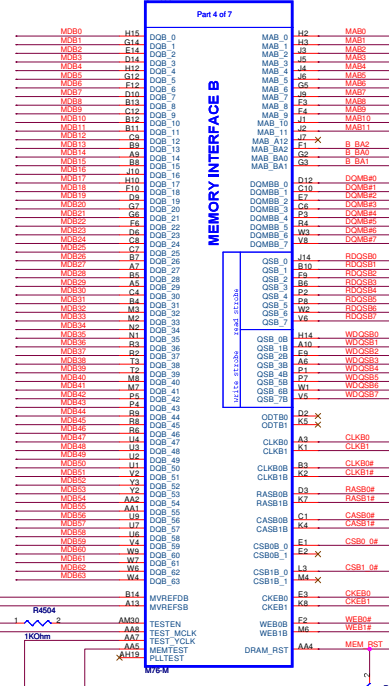
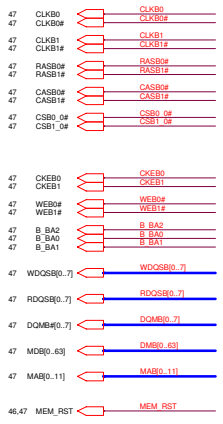
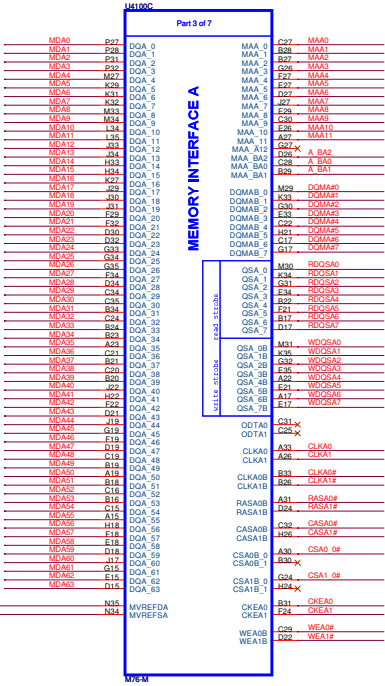
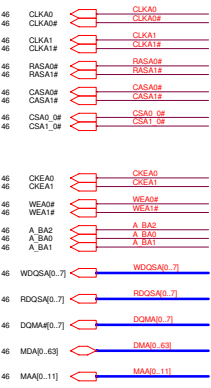


ASUS		Title : A7K
ASUSTECH CO. LTD.		Engineer: Endy Zhang
Size: Custom	Project Name: M76(3/5)Power	Rev: 2.0
Date: 2008.11.14.2007	Sheet: 43	of 69

<< Kennedy_Zhang >>

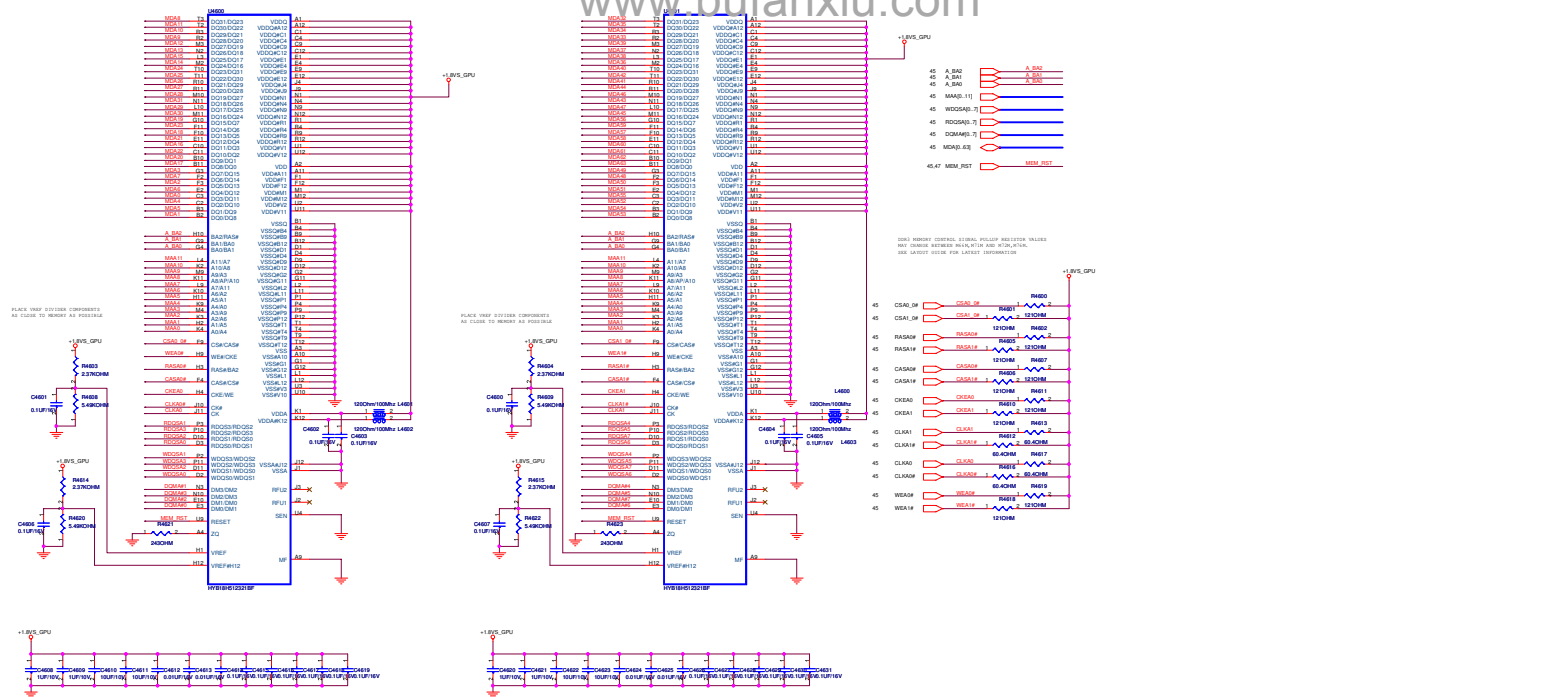
		Title : A7K
ASUSTECH CO., LTD.		Engineer: <i>Andy Zhang</i>
Size	Project Name	Rev
Custom	<Doc>	2.0
Date: 2007.11.14		Sheet 44 of 69

<< Kennedy_Zhang >>

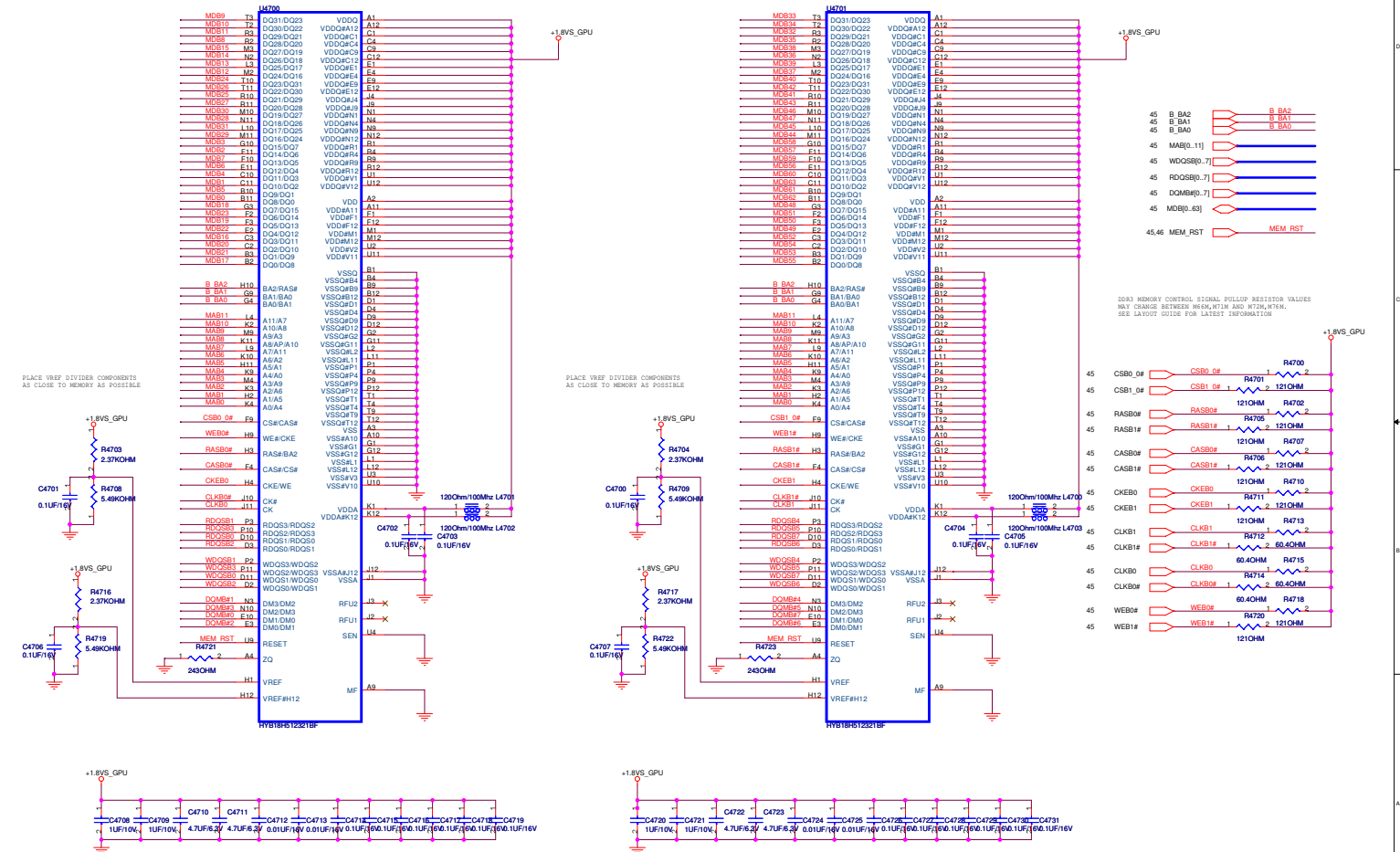


ASUS Title: **A7K**
 ASUSTECH CO., LTD. Engineer: **Endy Zhang**
 Size: **Project Name**
 Custom: **M7G(5)Memory 1/F** Rev: **2.0**
 Date: **8/20/2007 14:20:07** Sheet **25** of **26**

<< Kennedy_Zhang >>

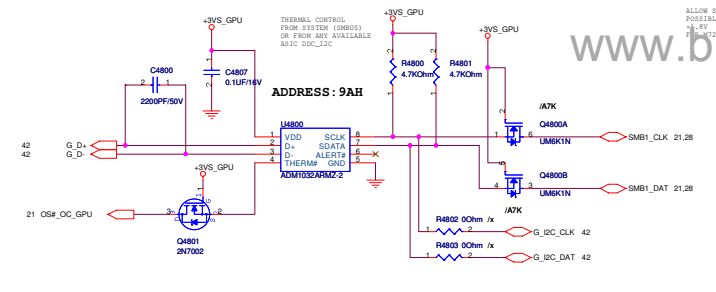


<< Kennedy_Zhang >>



ASUS		Title : A7K	
ASUSTECH CO., LTD.		Engineer: <i>Endy Zhang</i>	
Size	Project Name	Rev	
Custom	GDDR3 Memory(2/2)	2.0	
Date: 2007.11.14.2007	Sheet	47	of 69

<< Kennedy_Zhang >>



NTM2M AND NTM6M HAVE INTERNAL TEMP SENSORS AND AN EXTERNAL SENSOR CHIP IS NOT REQUIRED

AT11 RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

VIO1 VIO2 VIO4 VIO6 VIO7 RSTNC VBEAD GPIO2 GPIO3 GPIO8 DVALID

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TO_GENERIC GPIO21_B8_EN GPIO20_23_CLRREQ (DRIVES LOW DURING RESET) V2STNC R2STNC

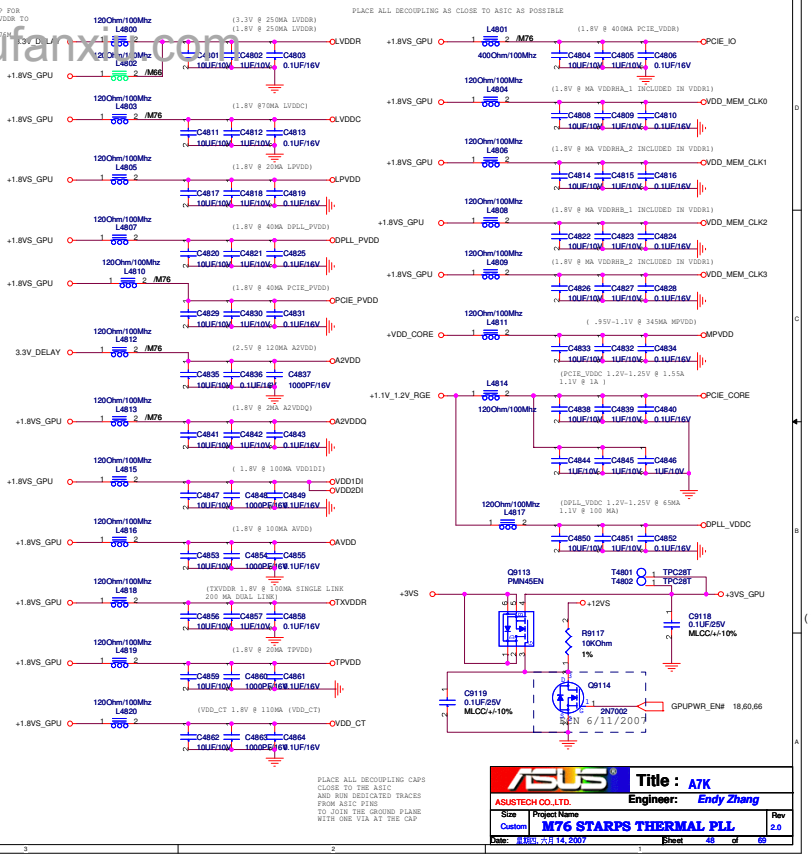
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS

0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = RESISTOR DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS
BIF_MSI_DIS	VIO1	0 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO2	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO3	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO4	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO5	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO6	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO7	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO8	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO9	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO10	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO11	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO12	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO13	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO14	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO15	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO16	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO17	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO18	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO19	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO20	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO21	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO22	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO23	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO24	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO25	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO26	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO27	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO28	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO29	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO30	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO31	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO32	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO33	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO34	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO35	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO36	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO37	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO38	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO39	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO40	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO41	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO42	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO43	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO44	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO45	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO46	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO47	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO48	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO49	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO50	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO51	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO52	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO53	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO54	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO55	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO56	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO57	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO58	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO59	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO60	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO61	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO62	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO63	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO64	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO65	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO66	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO67	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO68	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO69	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO70	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO71	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO72	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO73	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO74	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO75	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO76	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO77	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO78	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO79	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO80	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO81	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO82	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO83	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO84	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO85	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO86	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO87	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO88	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO89	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO90	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO91	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO92	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO93	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO94	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO95	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO96	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO97	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO98	0 MESSAGE SIGNAL INTERRUPT DISABLED
MSI_FORCE_ENABLE	VIO99	1 MESSAGE SIGNAL INTERRUPT ENABLED
MSI_FORCE_DISABLE	VIO100	0 MESSAGE SIGNAL INTERRUPT DISABLED



ASUS Title: **A7K**

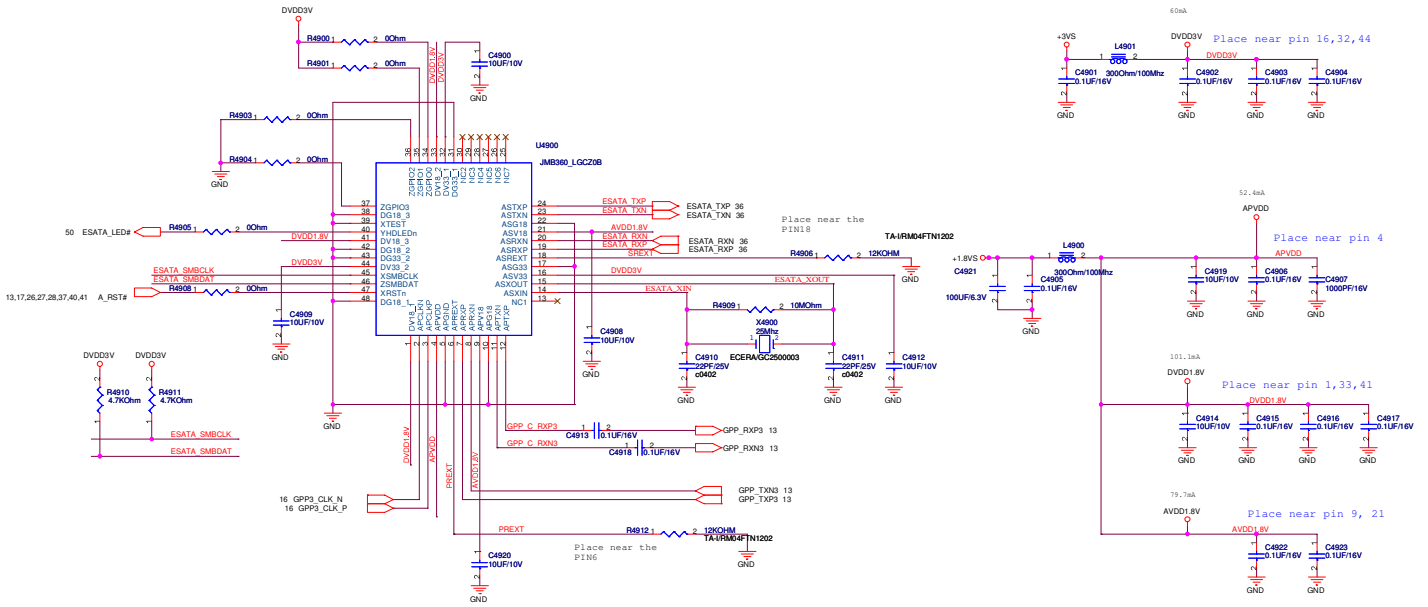
ASUSTECH CO., LTD. Engineer: **Endy Zhang**

Size: Project Name: **M76 STARPS THERMAL PLL**

Custom: Rev: 2.0

Date: 11/14/2007 Sheet: 45 of 49

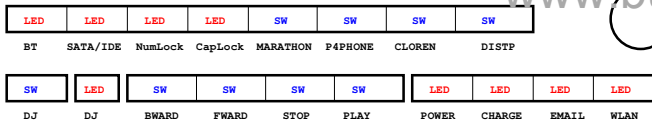
<< Kennedy_Zhang >>



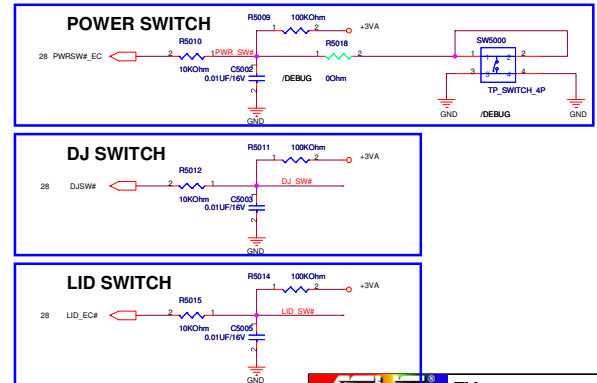
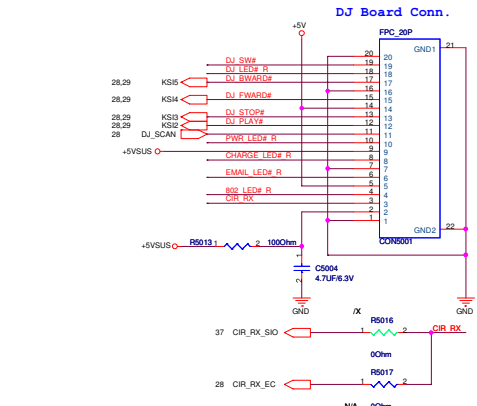
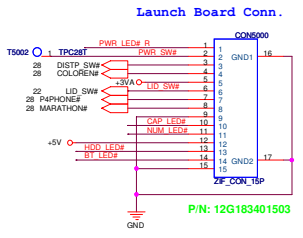
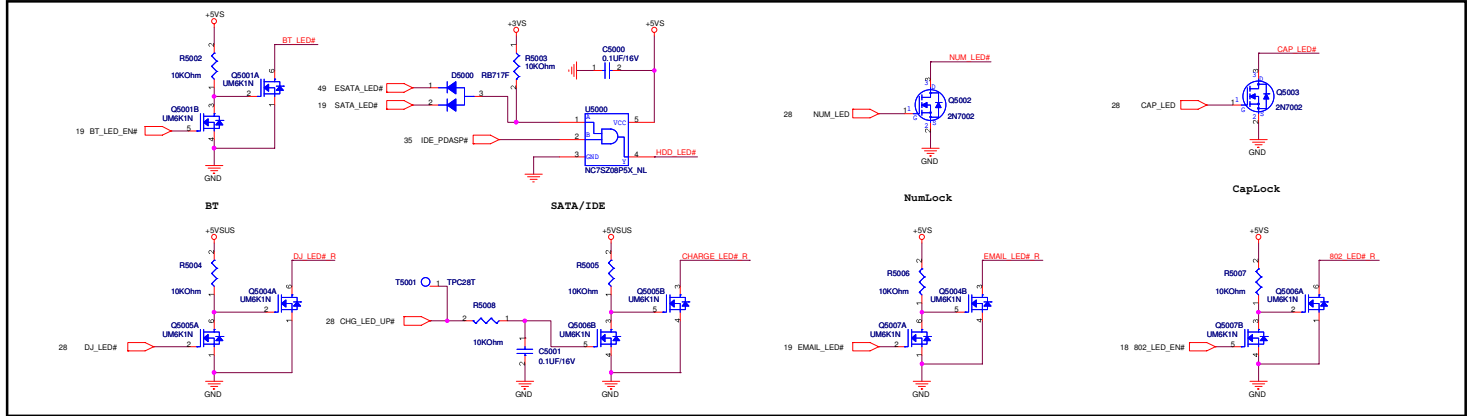
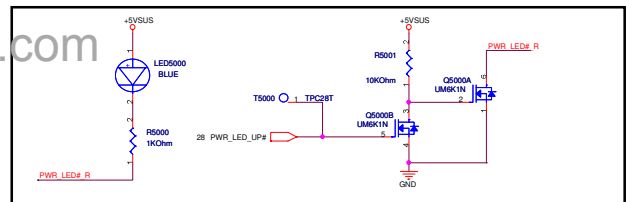
ASUS		Title : A7K
ASUSTECH CO., LTD.		Engineer: Endy Zhang
Size	Project Name	Rev
Custom	E-SATA	2.0
Date: 2007.11.14.2007	Sheet	49 of 69

<< Kennedy_Zhang >>

A7K TOP VIEW

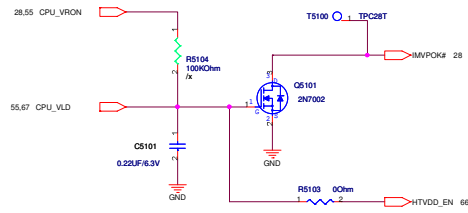
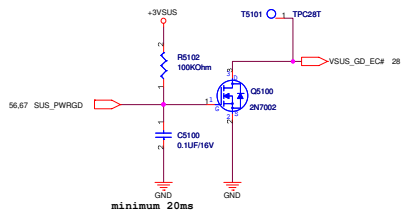


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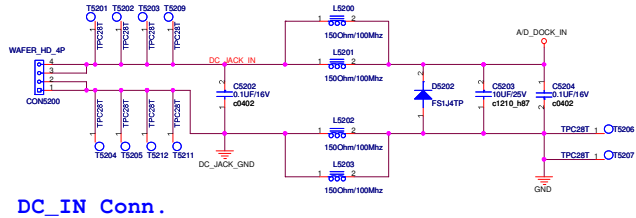
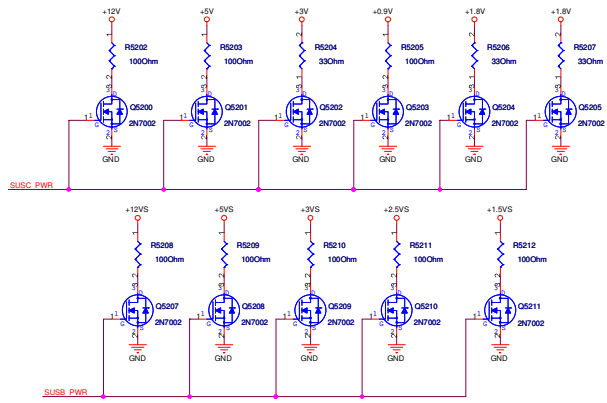
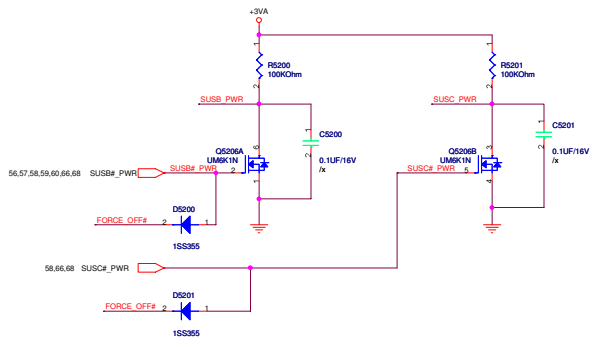
ASUS Title: **A7K**
 ASUSTECH CO., LTD. Engineer: **Endy Zhang**
 Size Project Name
 Custom **Function Key** Rev
 Date: 0.000_2014.14.2007 Sheet 50 of 59

<< Kennedy_Zhang >>

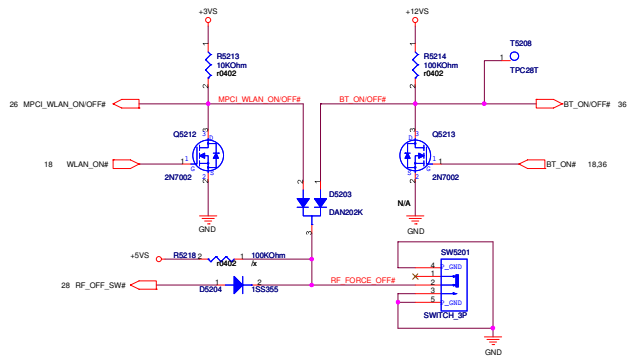
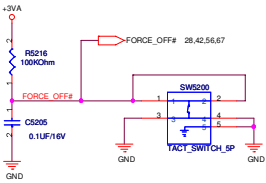


ASUS		Title : ATK	
ASUSTECH CO.,LTD.		Engineer: <i>Andy Zhang</i>	
Size	Project Name	Rev	
Custom	Power Sequence	2.0	
Date: 2007.12.14.2007	Sheet	01	of 09

<< Kennedy_Zhang >>



DC_IN Conn.



ASUS		Title : ATK	
ASUSTECH CO.,LTD.	Engineer: Endy Zhang		Rev
Size	Project Name	Custom	
Date: 2008-11-14 2007		Sheet 32 of 39	

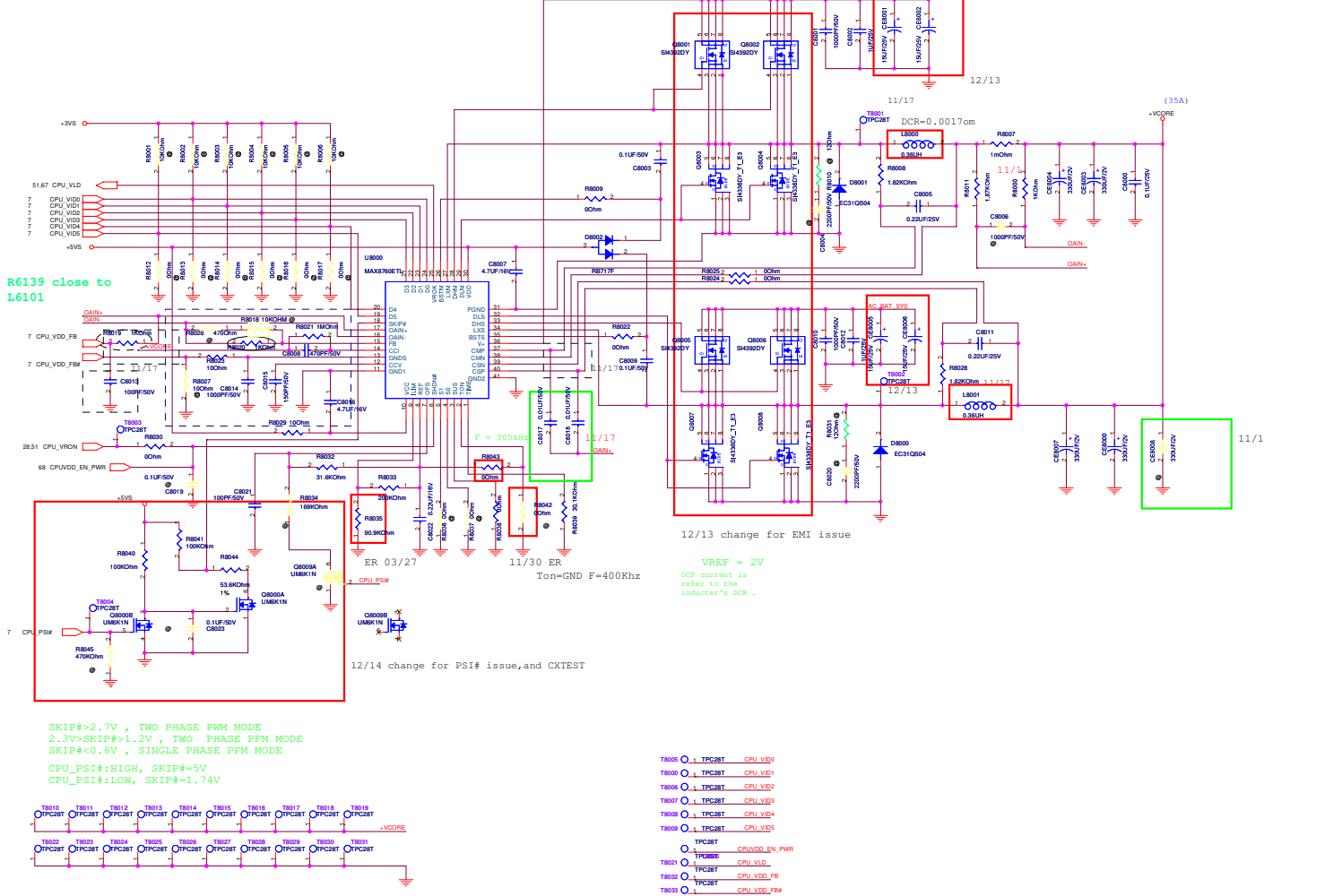
<< Kennedy_Zhang >>

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ASUSTECH CO.,LTD.		Engineer: Endy Zhang	
Size	Project Name	Rev	
Custom	BLANK	2.0	
Date: 2014.14.2007	Sheet 03 of 09		

<< Kennedy_Zhang >>

		Title : A7K	
ASUSTECH CO.,LTD.		Engineer: Andy Zhang	
Size	Project Name	Rev	
Custom	BLANK	2.0	
Date: 2014.14.2007	Sheet 04 of 09		

<< Kennedy_Zhang >>



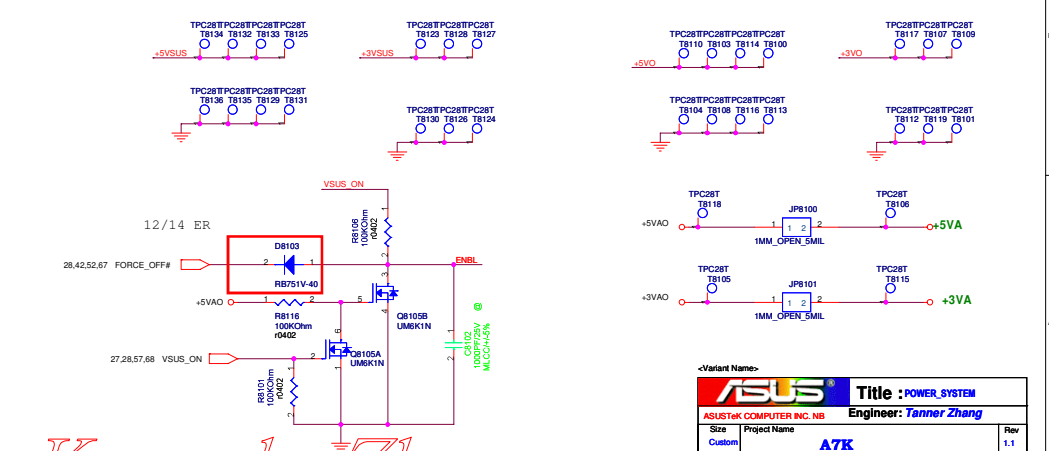
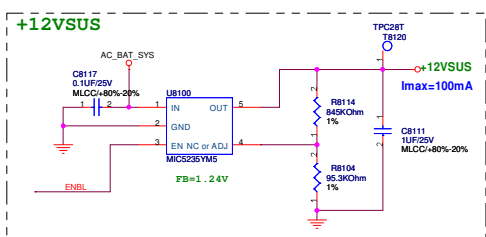
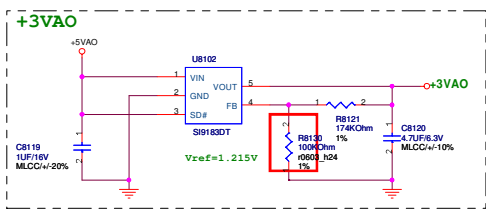
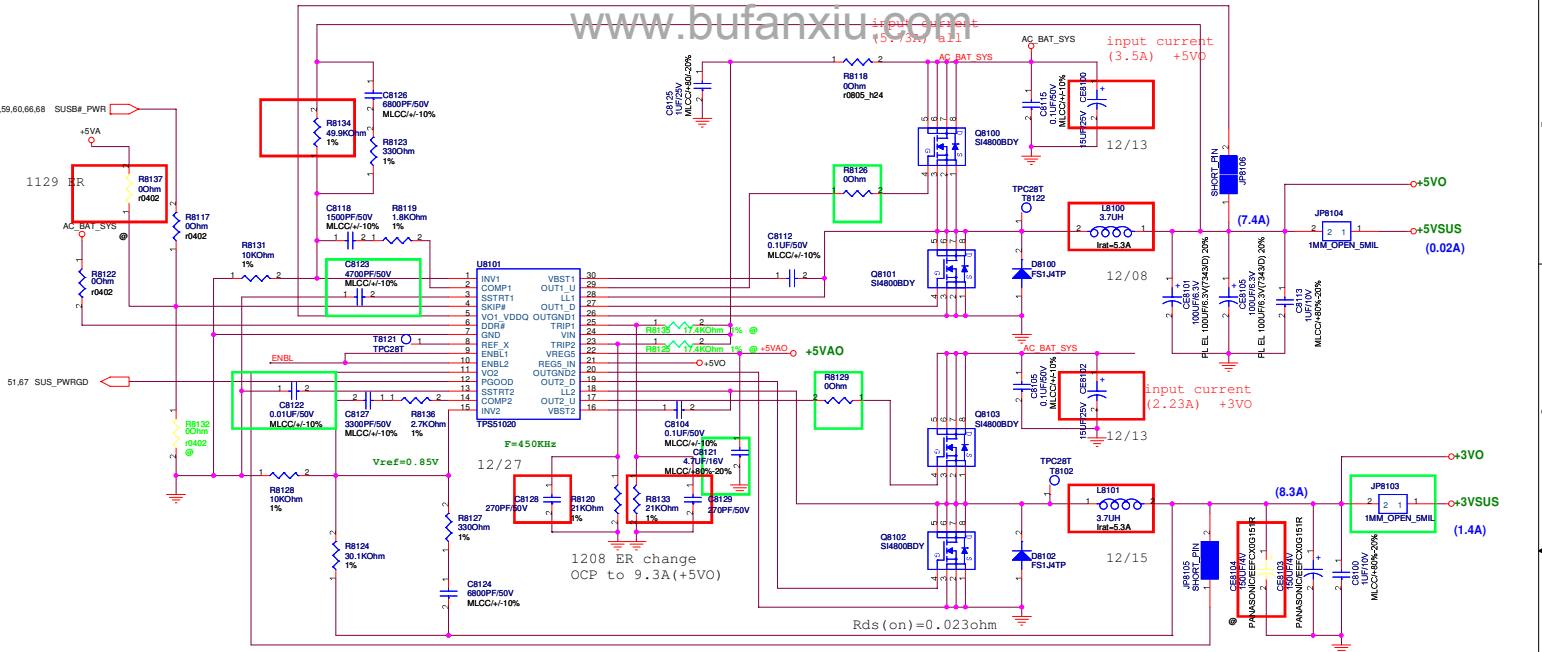
R6139 close to L6101

SKIP#>2.7V , TWO PHASE PWM MODE
 2.3V>SKIP#>1.2V , TWO PHASE PFM MODE
 SKIP#<0.8V , SINGLE PHASE PFM MODE
 CPU_PSI# : HIGH , SKIP# = 5V
 CPU_PSI# : LOW , SKIP# = 1.74V

- T8005 ○ L TPC28T CPU_VDD0
- T8006 ○ L TPC28T CPU_VDD1
- T8008 ○ L TPC28T CPU_VDD2
- T8007 ○ L TPC28T CPU_VDD4
- T8008 ○ L TPC28T CPU_VDD4
- T8009 ○ L TPC28T CPU_VDD5
- L TPC28T CPU_VDD0EN_PWR
- L TPC28T CPU_VDD
- T8021 ○ TPC28T CPU_VDD_FB
- T8035 ○ TPC28T CPU_VDD_FB
- T8035 ○ L TPC28T CPU_VDD_FB#

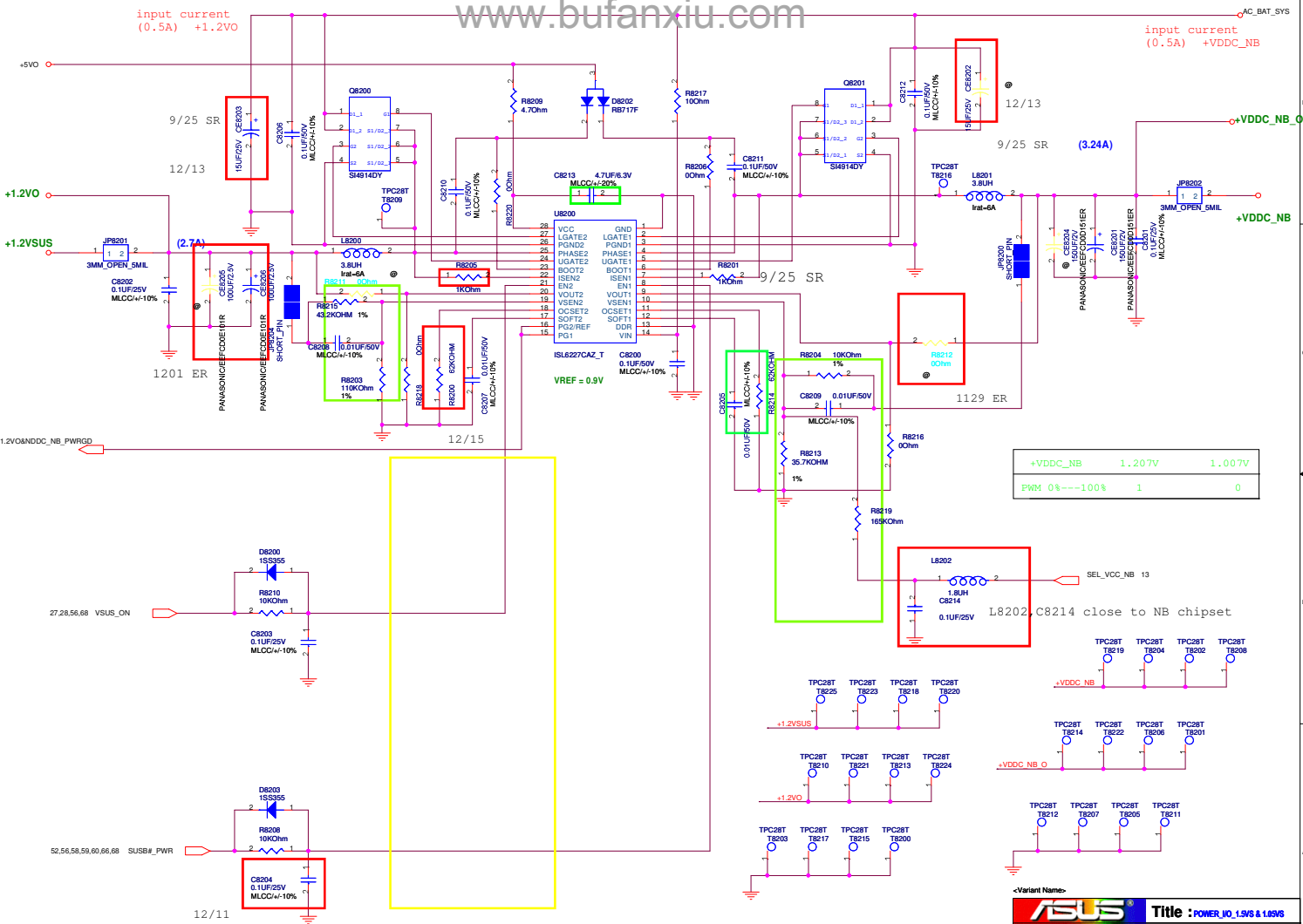
<< Kennedy_Zhang >>

ASUS		Title : POWER_VCORE	
Size	Project Name	Engineer	Tanner Zhang
C	ATK		
Date	2014-12-15-2007	Sheet	55 of 69



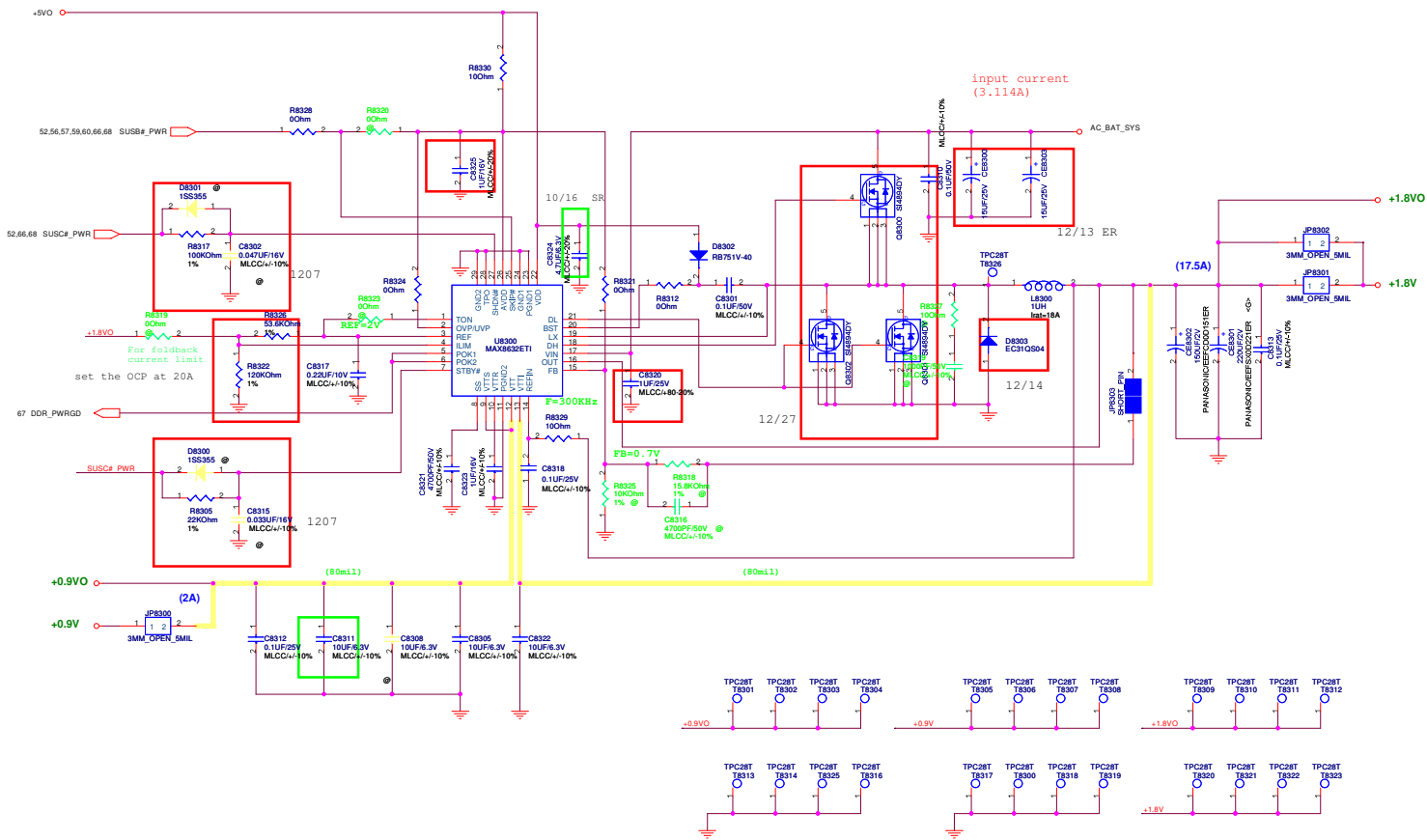
ASUS		Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB		Engineer: Tanner Zhang
Size	Project Name	Rev
Custom	A7K	1-1
Date: 8/26/2007 14:20:07	Sheet	56 of 60

« Kennedy_Zhang »



ASUS		Title : POWER_IO_L9V6 & L6V6	
-<OrigName>		Engineer:	
Size	Project Name	Rev	
Custom	ATK	1.1	
Date: 8/15/2007	7:14.2007	Sheet	57 of 88

<< Kennedy_Zhang >>



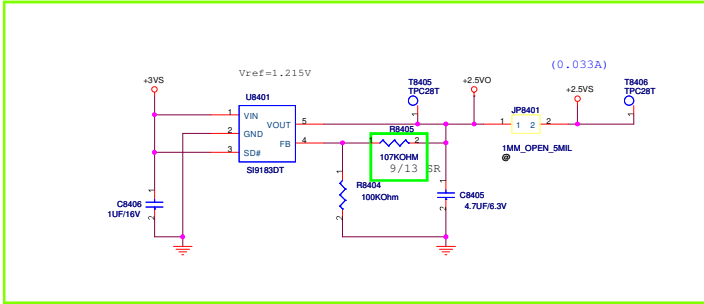
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ASUS		Title : POWER_IO_DDR & VTT
ASUSTeK COMPUTER INC. NB		Engineer: Tanner Zhang
Size	Project Name	Rev
Custom	ATK	1.0
Date: 11/04/2007 14:00	Sheet	88 of 89

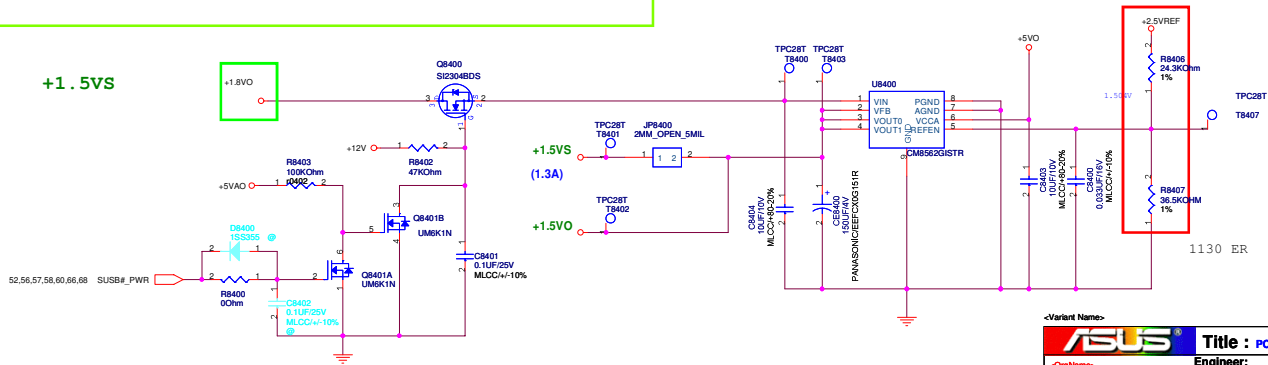
<< Kennedy_Zhang >>



+2.5VS

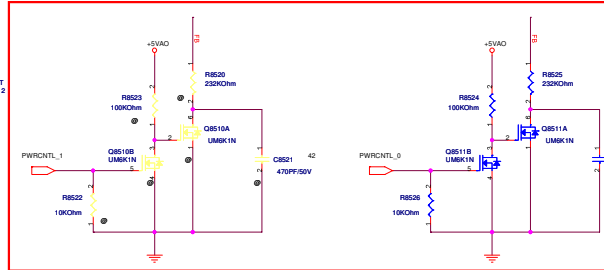
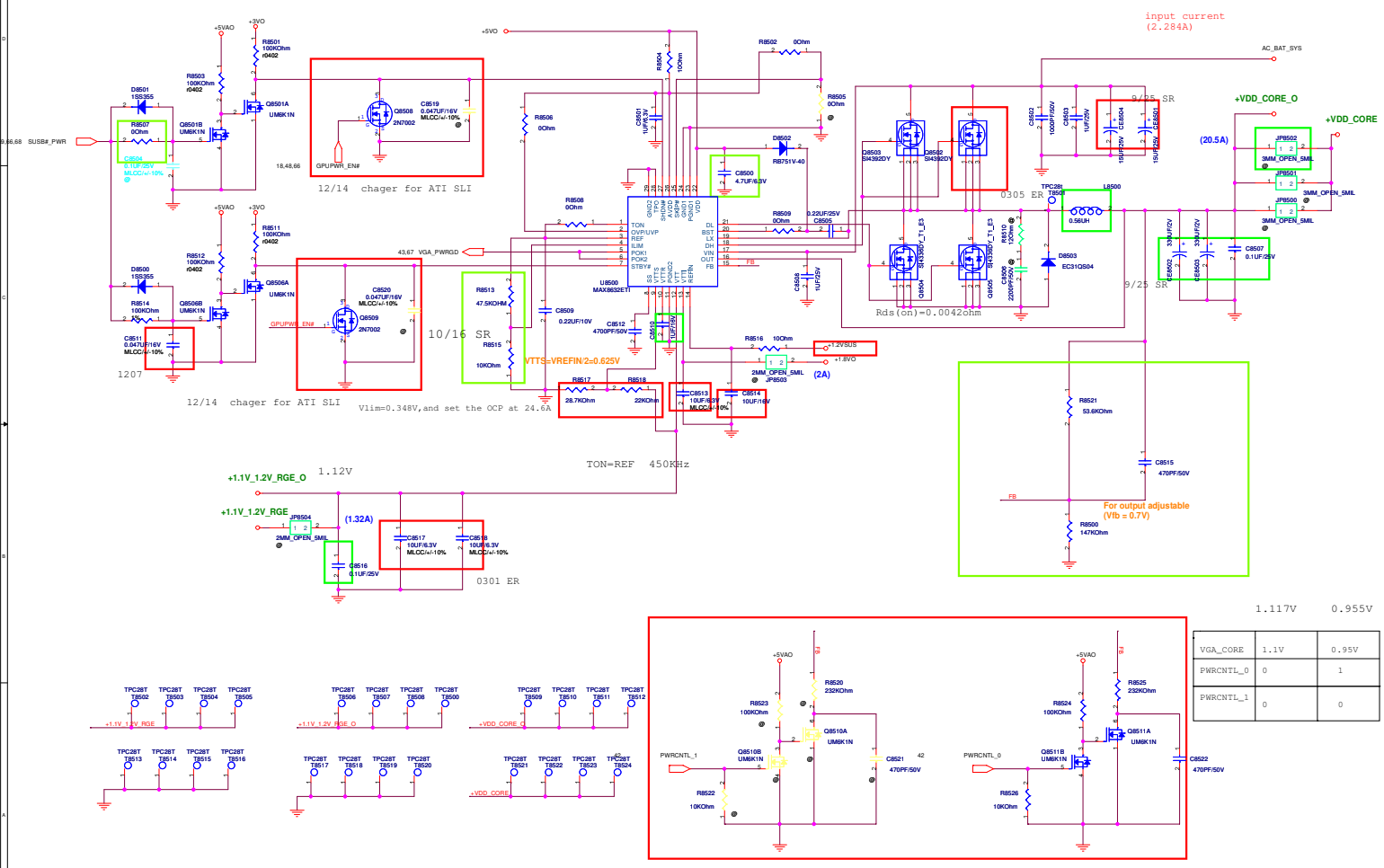


+1.5VS



ASUS		Title : POWER_U0_+3VA & +2.5V
Engineer:		
Size	Project Name	Rev
Custom	A7K	1.1
Date: 8/24/2007	Sheet 99	of 99


« Kennedy_Zhang »




VGA_CORE	1.1V	0.95V
PWRCTRL_0	0	1
PWRCTRL_1	0	0

ASUS		Title : POWER_VGACORE_1.V0
ASUSTECH	Project Name	Engineer: Tanner Zhang
C	Project Name	Rev
	ATK	2.0
Date: 2014.12.14.2007	Sheet	85 of 89

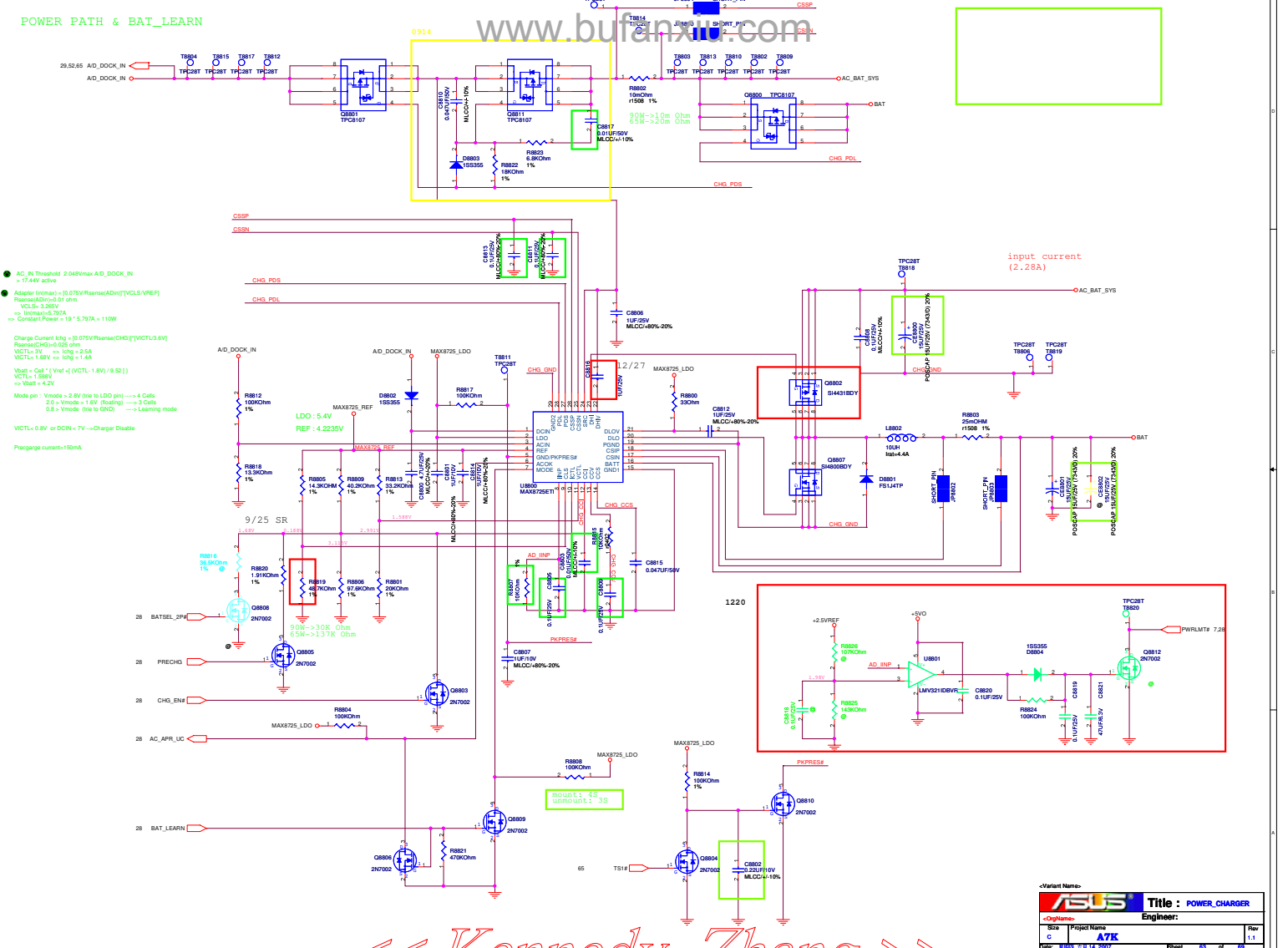
« Kennedy_Zhang »

<-Variant Name->		
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Engineer:		
Size	Project Name	Rev
B	A7K	1.1
Date: 2008.7.14.2007		Sheet 61 of 69

<< Kennedy_Zhang >>

<Variant Name>			
		Title : POWER_SHUTDOWN#	
<OrigName>		Engineer:	
Site	Project Name		Rev
Custom	ATK		1.1
Date: 8/18/2007 7:14:2007		Sheet 82 of 88	

« Kennedy_Zhang »



● AC_IN_Threshold > 2.048Vmax AD_DOCK_IN > 17.44V active
 ● Adapter (In/ma) = [0.075V/Rsense(ADIN)]*(VCL5-VREF)
 Resense(ADIN) = 0.01ohm
 VCL5 = 3.25V
 => In/ma = 5.737A
 => Constant Power = 19 * 5.737A = 110W

 Charge Current Ichg = [0.075V/Rsense(CHG)]*(VCTL3-V5)
 Resense(CHG) = 0.02ohm
 VCTL3 = 5V => Ichg = 2.5A
 VCTL1 = 5.58V => Ichg = 1.4A


 Vbat = Cell1 + (Vbat - (VCTL1 - 1.5V)) / 9.521
 VCTL1 = 5.58V
 => Vbat = 4.2V

 Mode pin: Vinode > 2.5V (96 to LDO pin) => 4 Cells
 2.0 > Vinode > 1.8V (Booting) => 3 Cells
 0.8 > Vinode (96 to DCIN) => Learning mode
 VCTL = 0.8V or DCIN = 7V => Charger Disable

 Precharge current = 150mA

-Variant Name-		Title : POWER_CHARGER	
ASUS			
Design	Project Name	Engineer:	
C	A7K		Rev 1.1
Date: 2014.12.14.2017	Sheet: 65	of	69

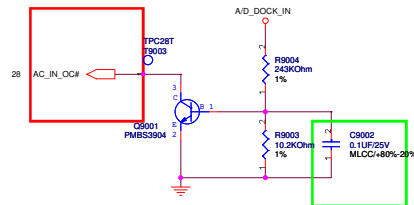
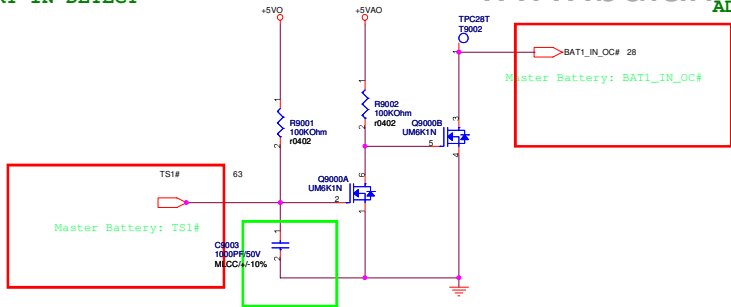
« Kennedy_Zhang »

<Variant Name>			
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<OrigName>		Engineer:	
Site	Project Name		Rev
Custom	ATK		1.1
Date: 8/15/2007 7:14:2007		Sheet 64 of 88	

« Kennedy_Zhang »

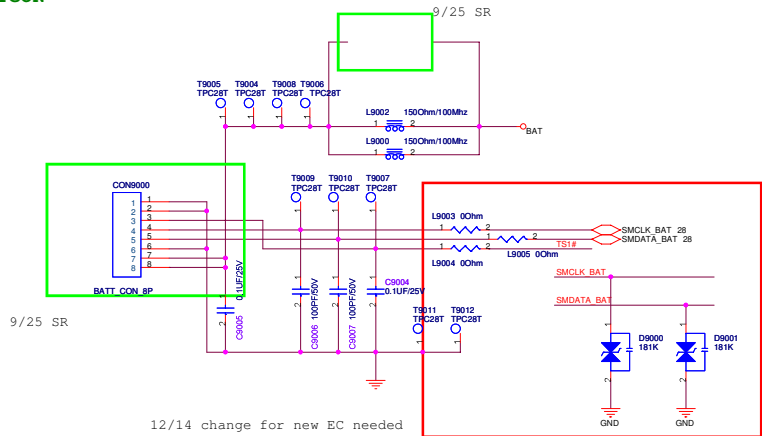
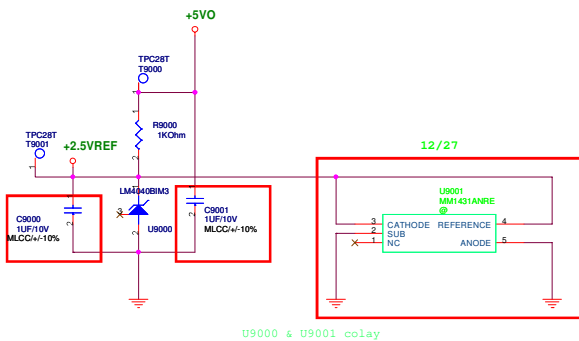
BATTERY IN DETECT

ADAPTER IN DETECT



+2.5VREF

BATCON



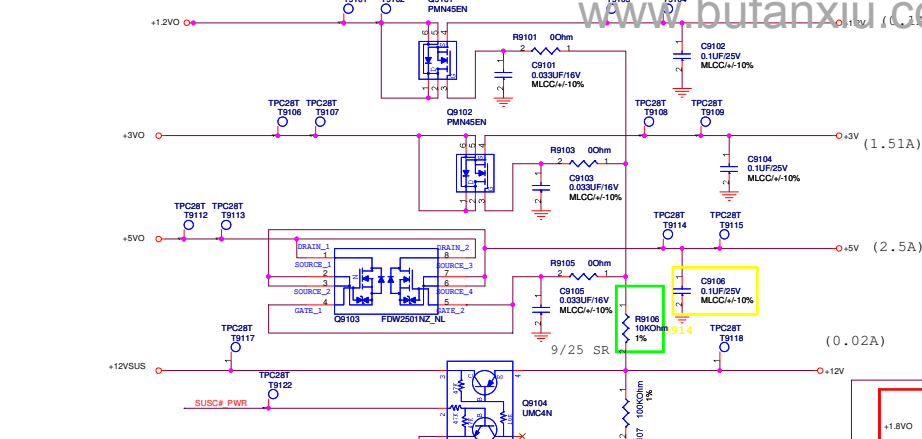
U9000 & U9001 colaly

12/14 change for new EC needed

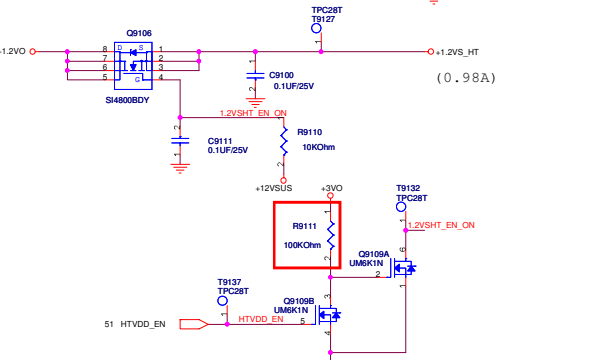
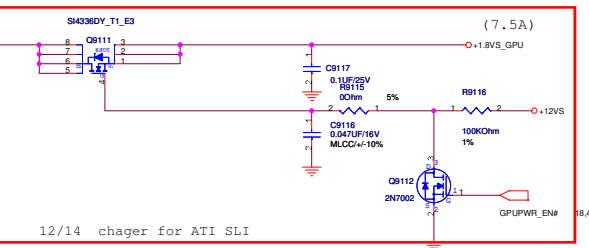
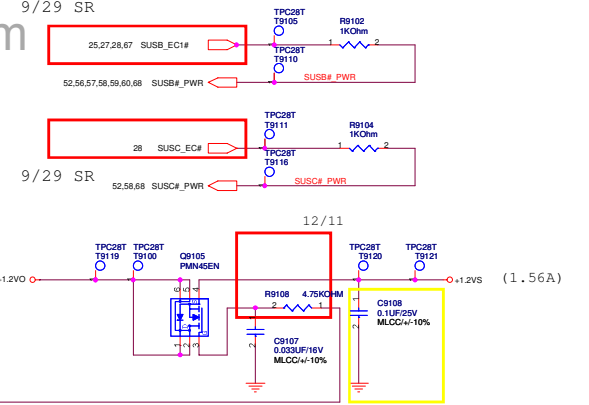
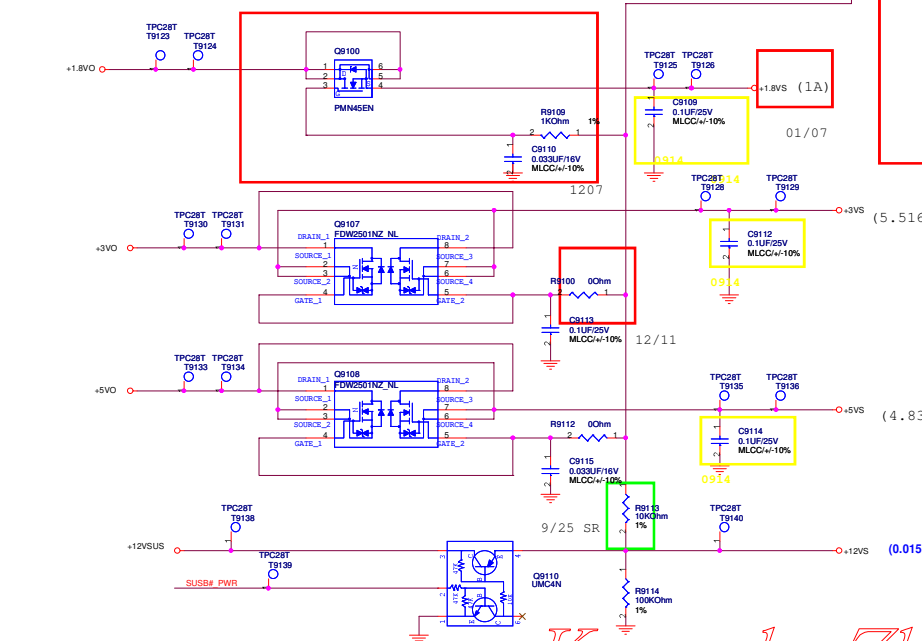
ASUS		Title : POWER_DETECT
Engineer: Tanner Zhang		Rev
Size	Project Name	1.1
Custom	ATK	
Date: 8/10/14 7:14:2007	Sheet	65 of 88

« Kennedy_Zhang »

SUSC#_STAGE POWER



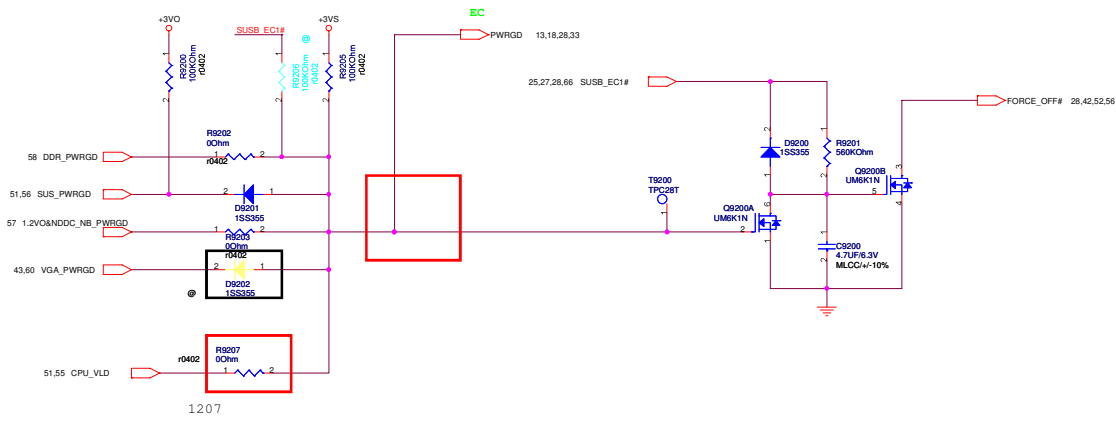
SUSB#_PWR POWER



ASUS		Title : POWER_LOAD_SWITCH	
Engineer:		Rev	
Size	Project Name	Rev	1.1
Custom	ATK	Date: 8/18/2007 7:14:2007	Sheet 86 of 88

« Kennedy_Zhang »

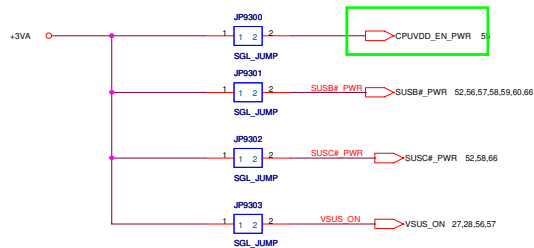
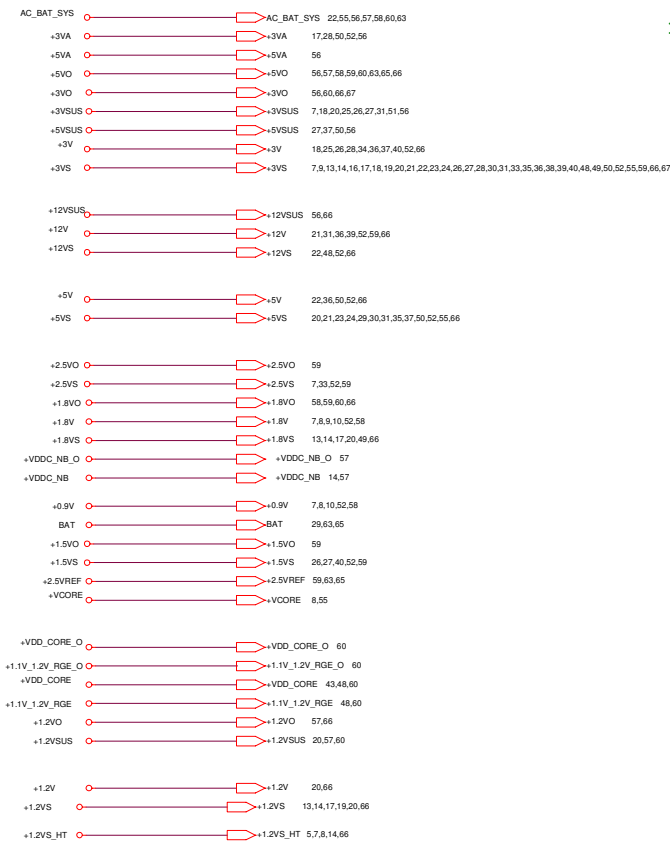
POWER GOOD DETECTER



<Variant Name>		ASUS		Title : POWER_PROTECT	
<OrigName>		Engineer:			
Site	Project Name			Rev	
Custom	ATK			1.1	
Date:	8/18/2007 7:14:2007	Sheet	67	of	88

« Kennedy_Zhang »

FOR POWER TEST



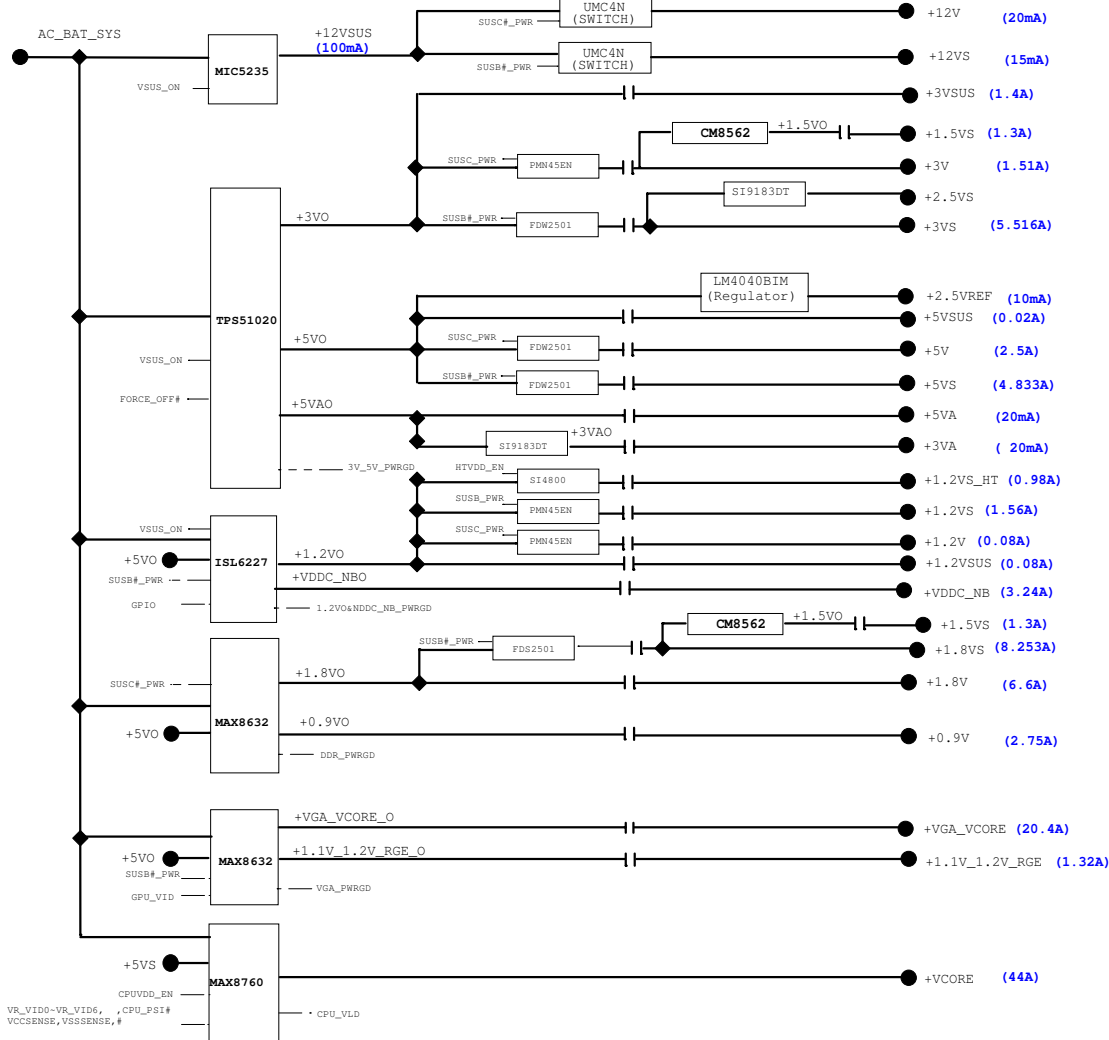
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ASUS Title : POWER_SIGNAL

Engineer:

Site	Project Name	Rev
Custom	ATK	1.1
Date: 8/18/2007 7:14:2007	Sheet 68 of 88	

« Kennedy_Zhang »



<< Kennedy_Zhang >>