

A8T/M SCHEMATIC R2.1

PAGE	Content	PAGE	Content
SYSTEM PAGE REF.		POWER PAGE REF.	
4	AMD S1 CPU--HT	61	POWER_VCORE
5	AMD S1 CPU--CNIL	62	POWER_SYSTEM
6	AMD S1 CPU--DDR2	63	POWER_I/O_1.2VO & 1.0VO
7	AMD S1 CPU--PWR/GND	64	POWER_I/O_LDO
8	DDR2 SO-DIMM_0	65	POWER_I/O_DDR2
9	DDR2 SO-DIMM_1	66	POWER_VGA_CORE (Empty)
10	DDR2 ADDRESS TERMINATION	67	POWER_LOAD_SYSTEM
11	C51M--HT TO CPU	68	POWER_CHARGER
12	C51M--HT TO MCP	69	POWER_PIC
13	C51M--PCI-E	70	POWER_PROTECT
14	C51M--CRT & LVDS	71	POWER_SWITCH_+5VLCM
15	C51M--PWR/GND	72	POWER_DIAGRAM
16	VGA CONN		
17	LVDS & INVERTER CONN		
18	CRT & TV_OUT		
19	MCP51--HT		
20	MCP51--PCI		
21	MCP51--IDE		
22	MCP51--USB & HDA & GPIO		
23	MCP51--PWR/GND		
24	HDD & CD-ROM CONN		
25	USB PORTS		
26	SUPER I/O LPC47N217		
27	BIOS & FIR		
28	KBC 38857		
29	SM BUS & POWER PORT		
30	PCI-E--MINI CARD		
31	PCI-E--NEW CARD		
32	PCI--LAN RTL8110CL		
33	RJ45 & RJ11		
34	PCI--1394, CardReader R5C832		
35	PCI--4 IN1 CON		
36	AUDIO CODEC ALC660		
37	AUDIO AMP G1420		
38	MDC,B/T,TPM & DISCHG,HOLE		
39	DVI CONN		
40	ACIN, BAT, FAN, I/O PORT		
41	SW & LED & TP		
42	POWER-ON SEQUENCE		
43	HISTORY		
44	I/O PORT		

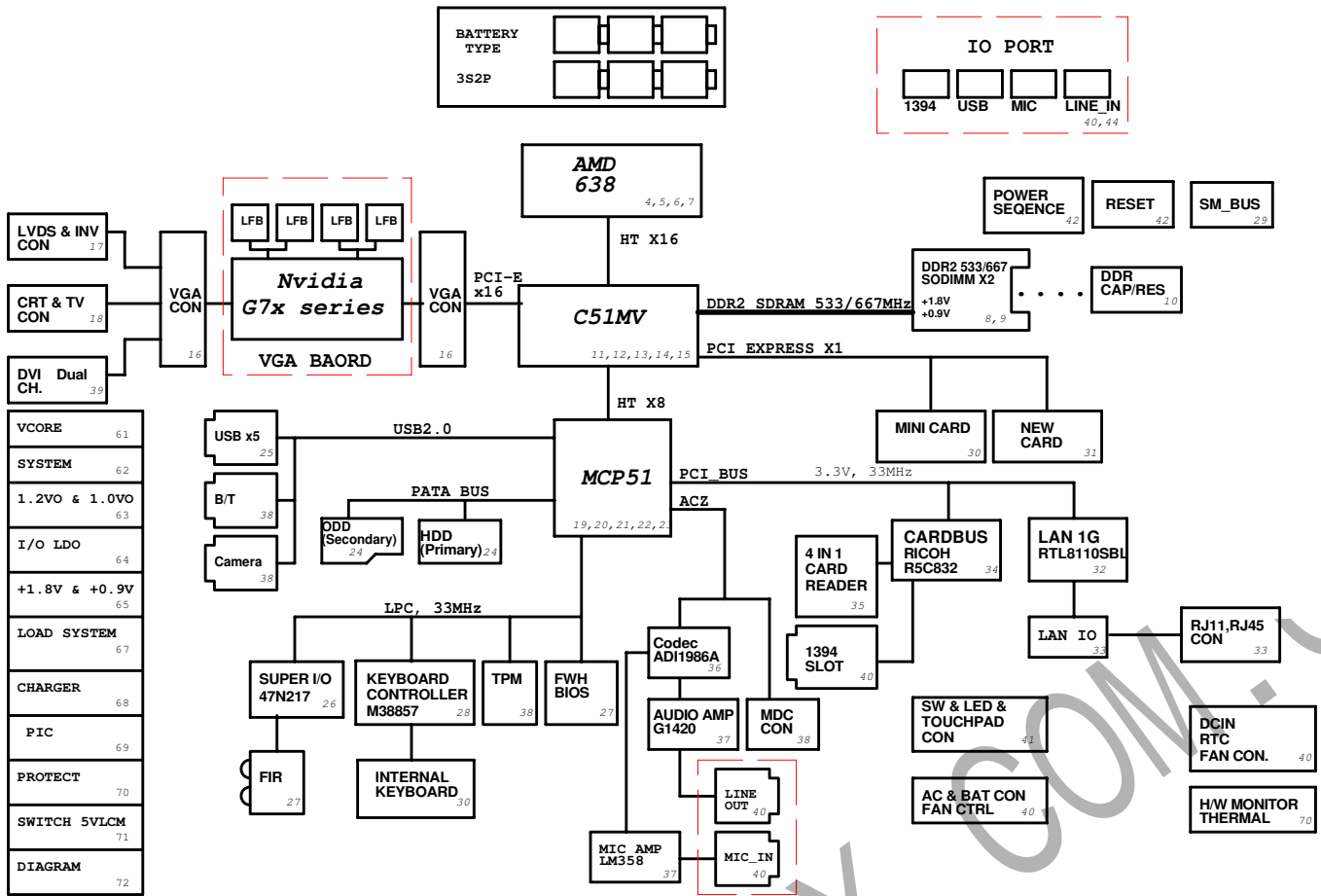
Core Design

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: PAGE REF.	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 1 OF 55		RELEASE DATE:	

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A8T/M AMD S1/C51MV BLOCK DIAGRAM



Core Designs

	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
			SHEET: 2 OF 55		RELEASE DATE: _____	

<< Kennedy_Zhang >>

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PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
 DDR_SODIMM0 = 1010000x (A0h)
 DDR_SODIMM1 = 1010001x (A2h)

MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWR_LMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CR_VID2)	+3VSUS
GPIO_11[16]		(CPD_VID[0:5])	+3VSUS
GPIO_17		(LID#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDINO_AUD	+3VSUS
GPIO_23		ACZ_SDIN1_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	STO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(R3#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERMTRIP#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_F)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

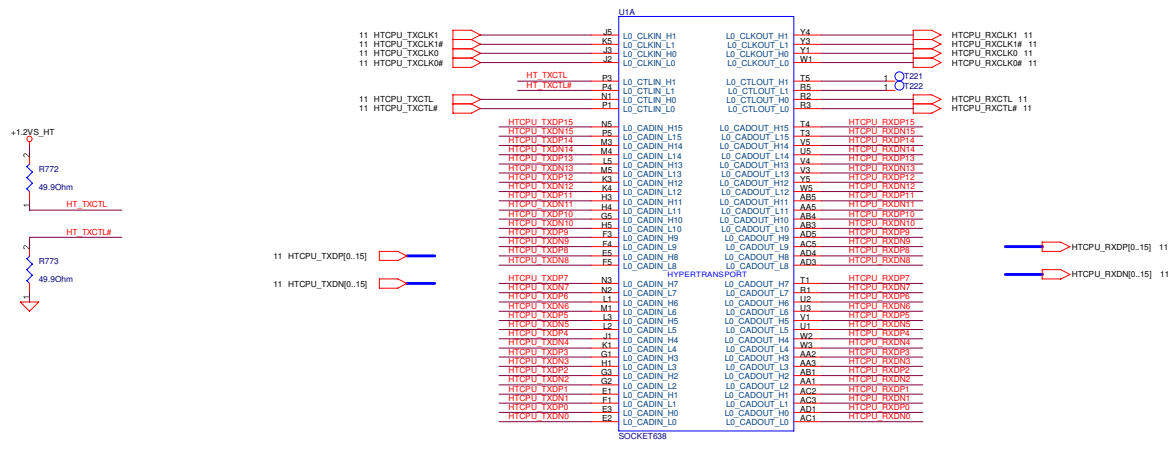
M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDT0	+3V
P53	GPO	KBDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPI	SMD_BAT	+3V
P77	GPI	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PGIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

Core Design:

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SCHEMATICS REF.	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 3 OF 55		RELEASE DATE:	

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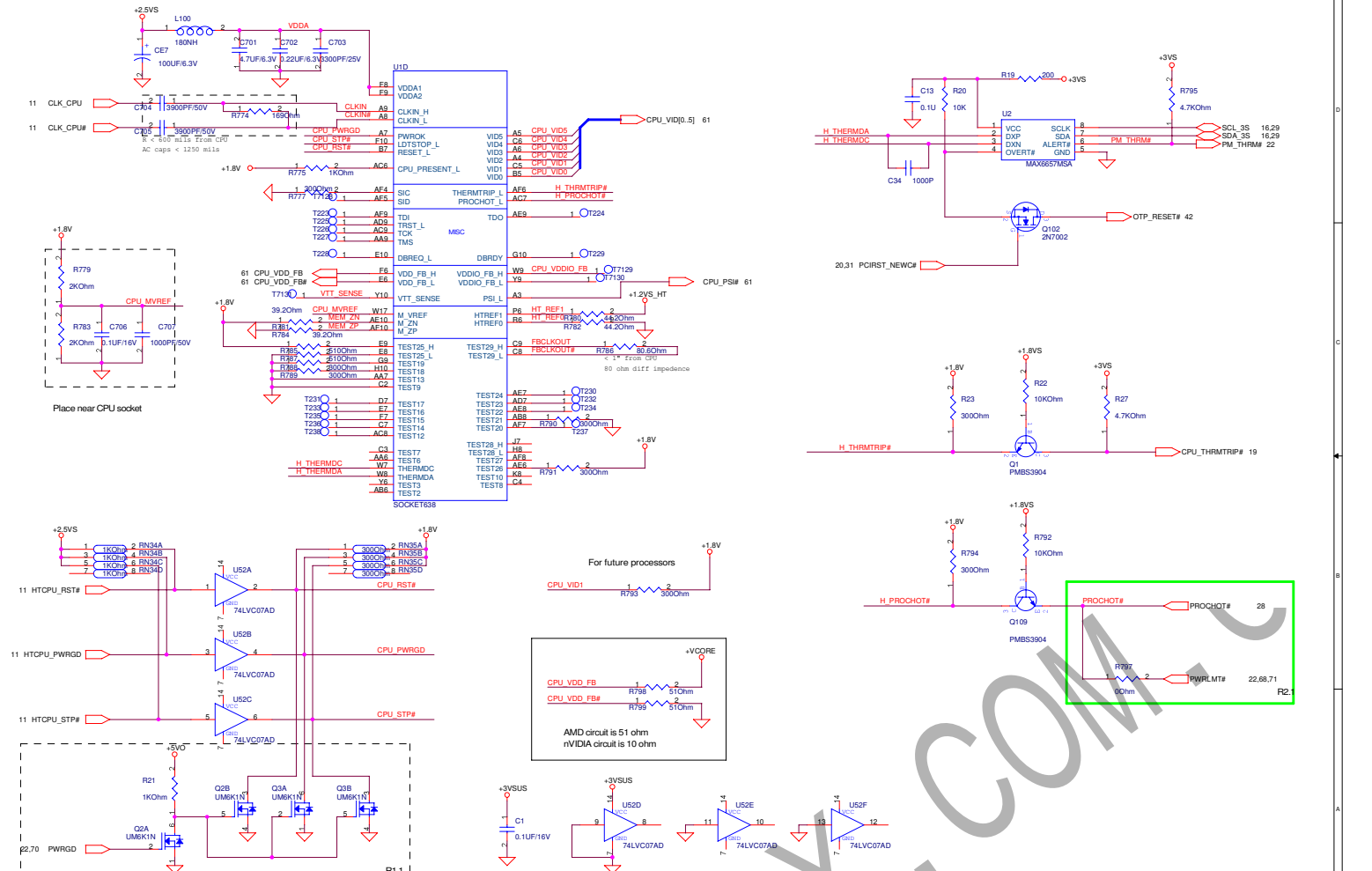
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ASUS Core Designs	PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU HT	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET 4 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

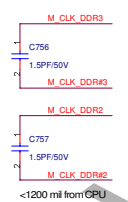
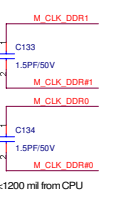
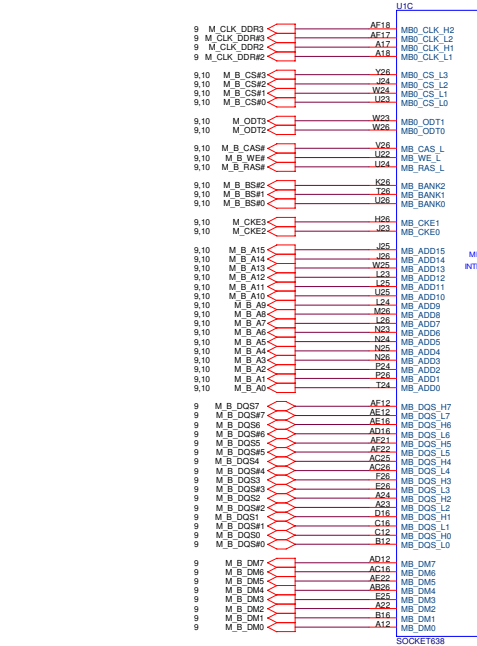
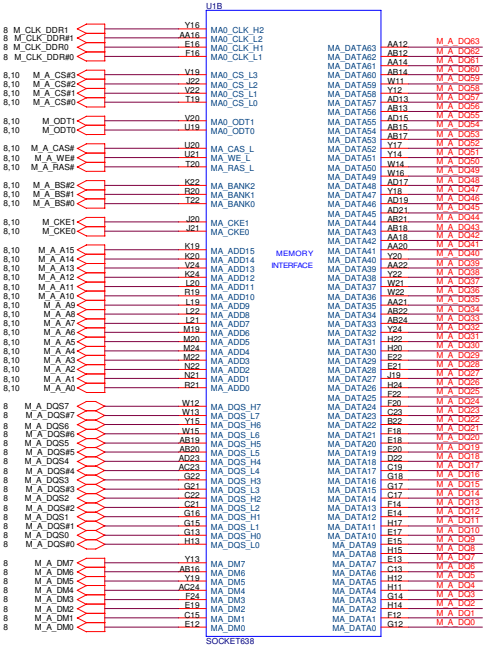
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ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU CNTL	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 5	OF: 55	RELEASE DATE:	

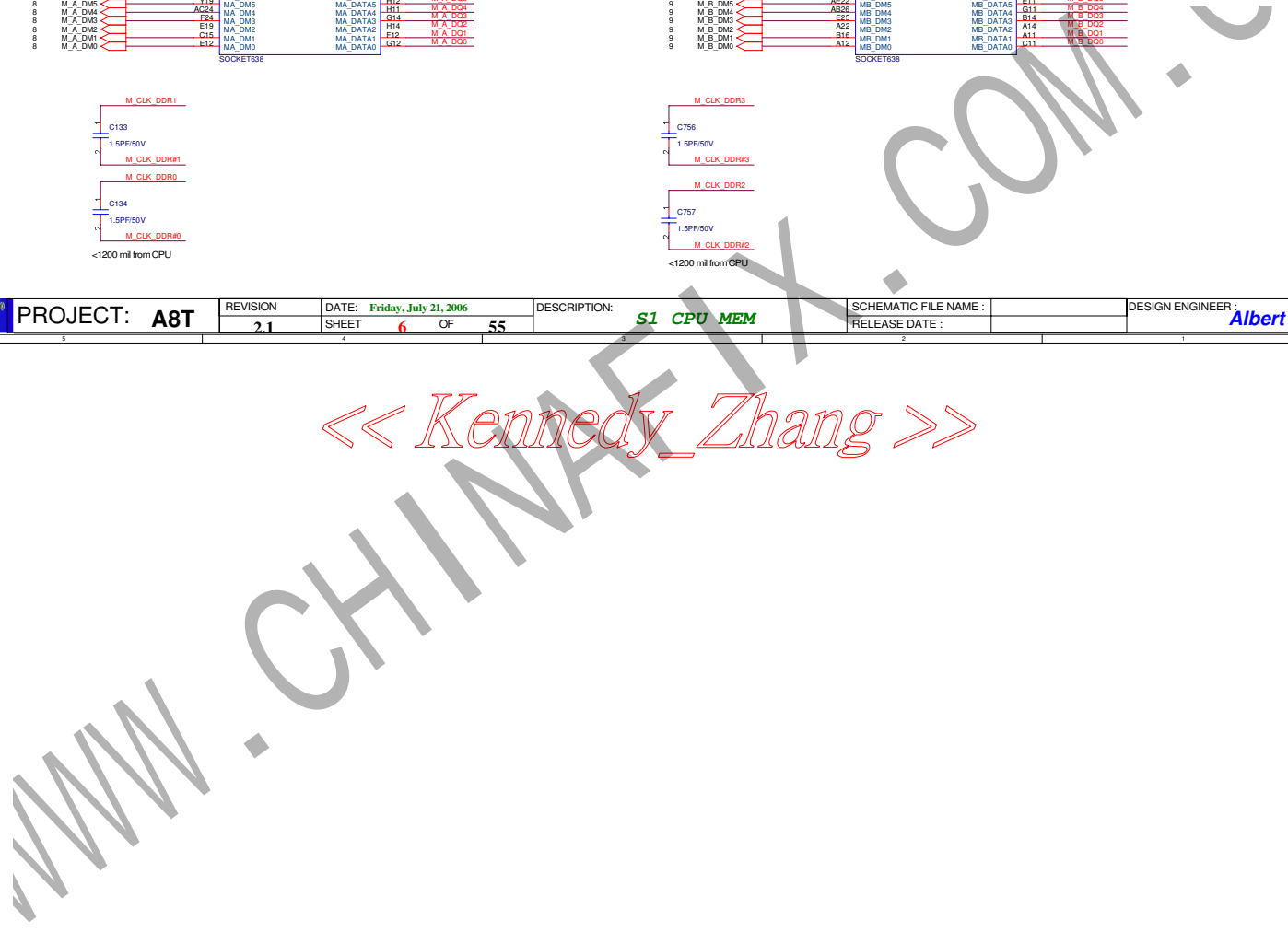
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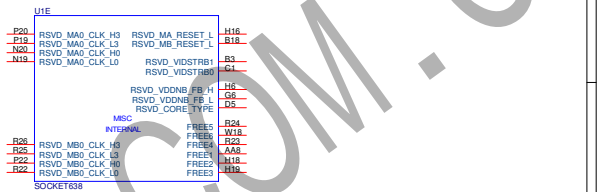
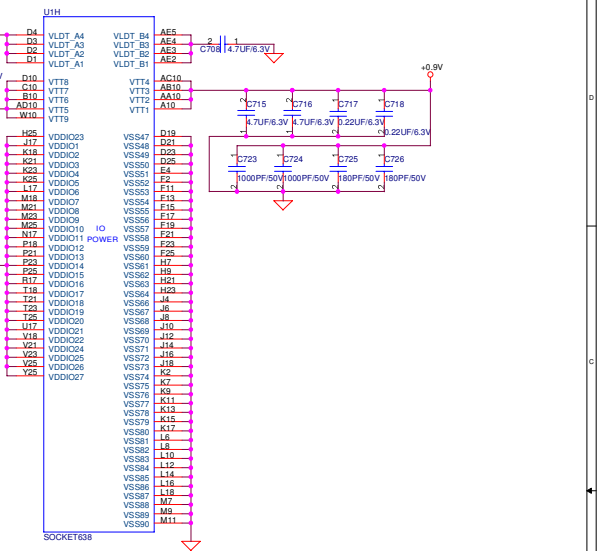
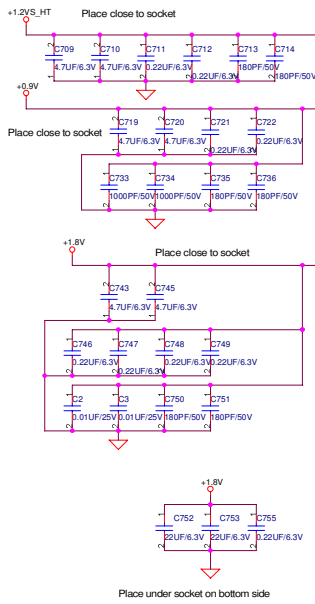
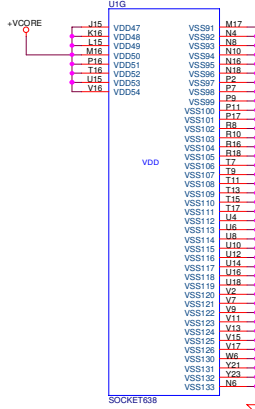
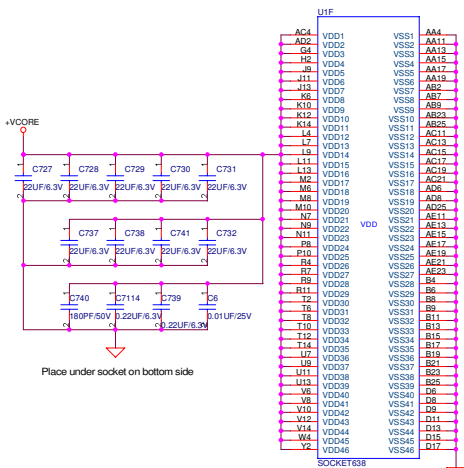
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ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU MEM	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 6	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>





Core Designs

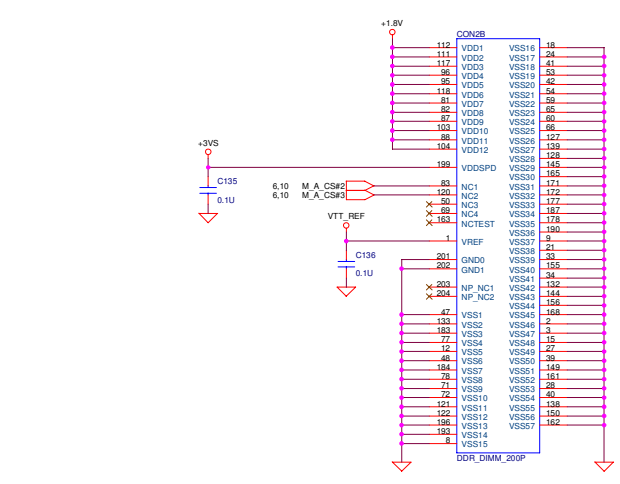
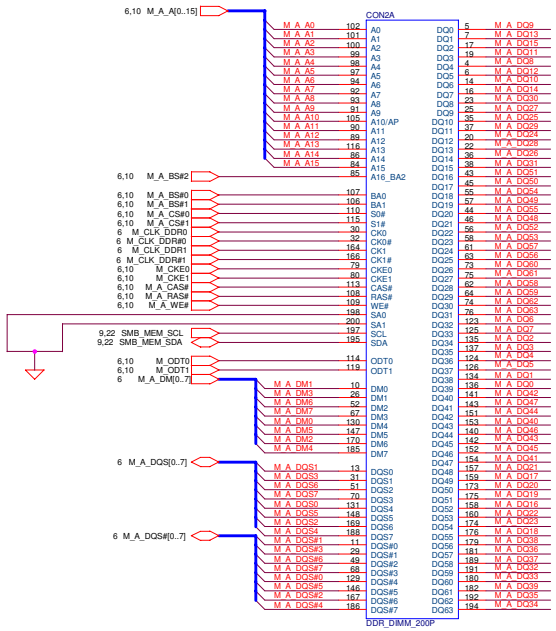
	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU PWR/GND	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
			SHEET 7 OF 55		RELEASE DATE: _____	

<< Kennedy_Zhang >>

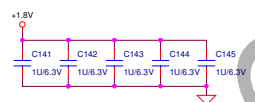
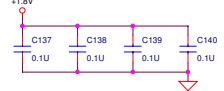
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6 M_A_DQ[0..63] M_A_DQ[0..63]

+1.8V 5.7,9,10,38,65
+3VS 5.8,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,34,36,38,39,41,46,61,70

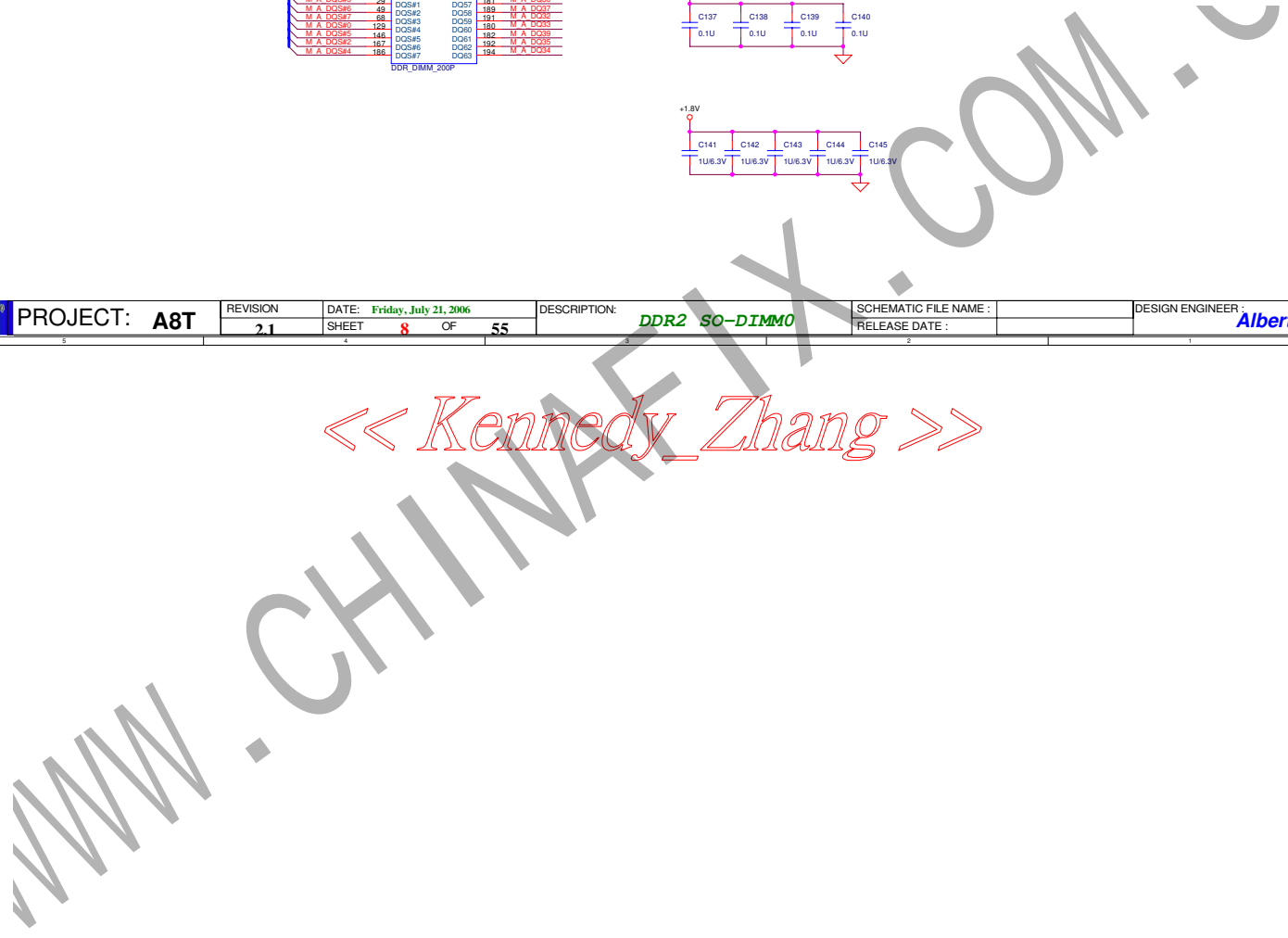


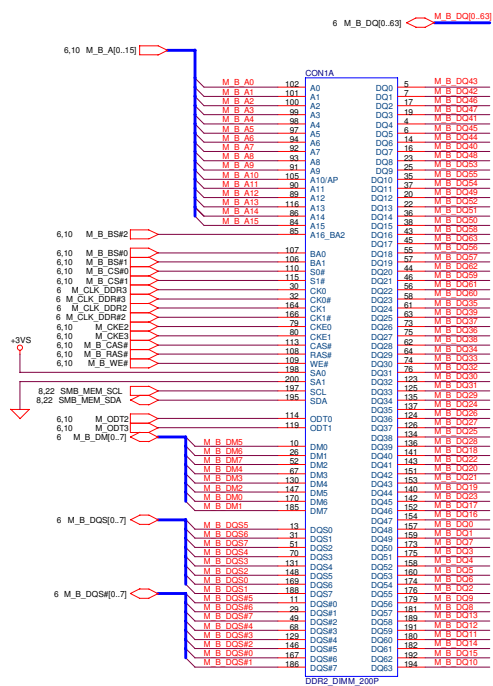
Layout Note: Place these Caps near SO DIMM 0



ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 SO-DIMM0	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 8 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

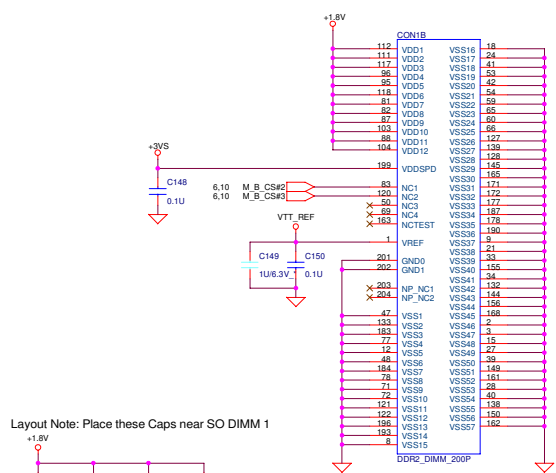




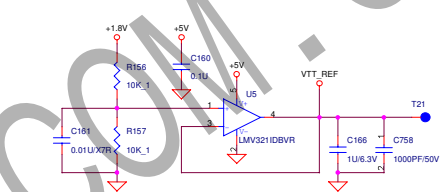
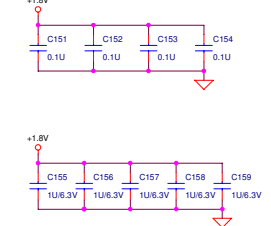
+1.8V
+3VS
+5V

+1.8V
+3VS
+5V

5,7,8,10,38,65
5,8,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,34,36,38,39,41,48,61,70
16,18,25,28,31,38,40,41



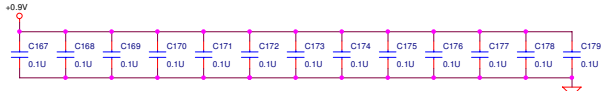
Layout Note: Place these Caps near SO DIMM 1



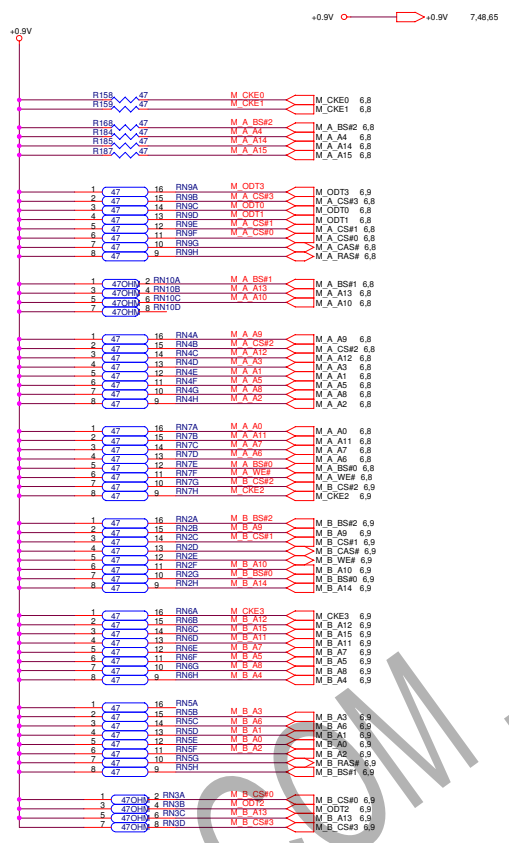
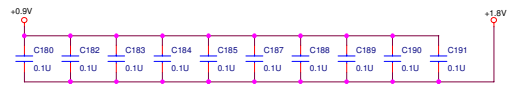
ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 SO-DIMM1	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 9	OF: 55	RELEASE DATE:	

<< Kennedy_Zhang >>





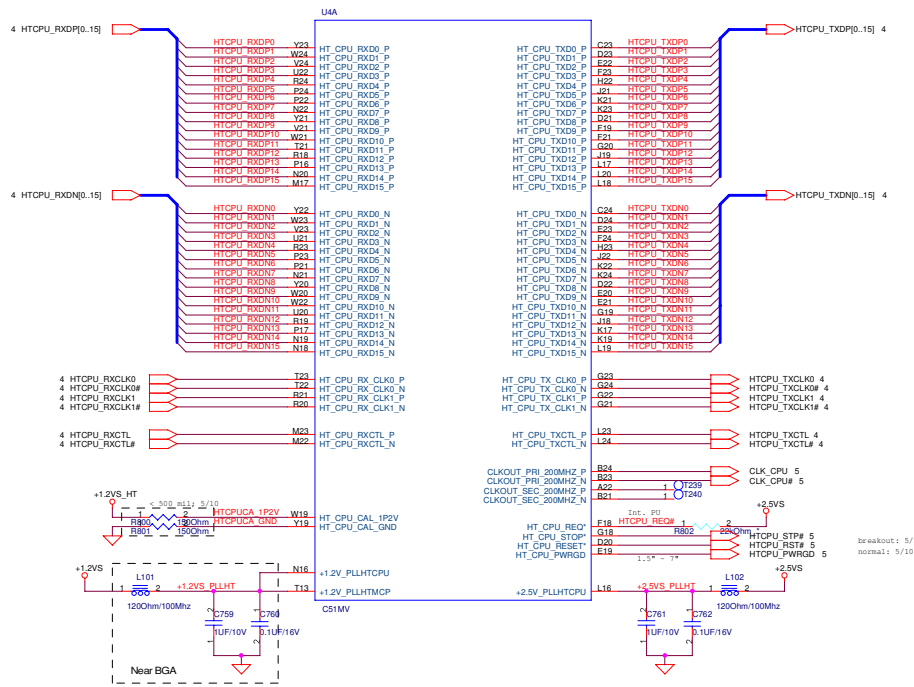
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



ASUS PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 10 OF 55			RELEASE DATE:	

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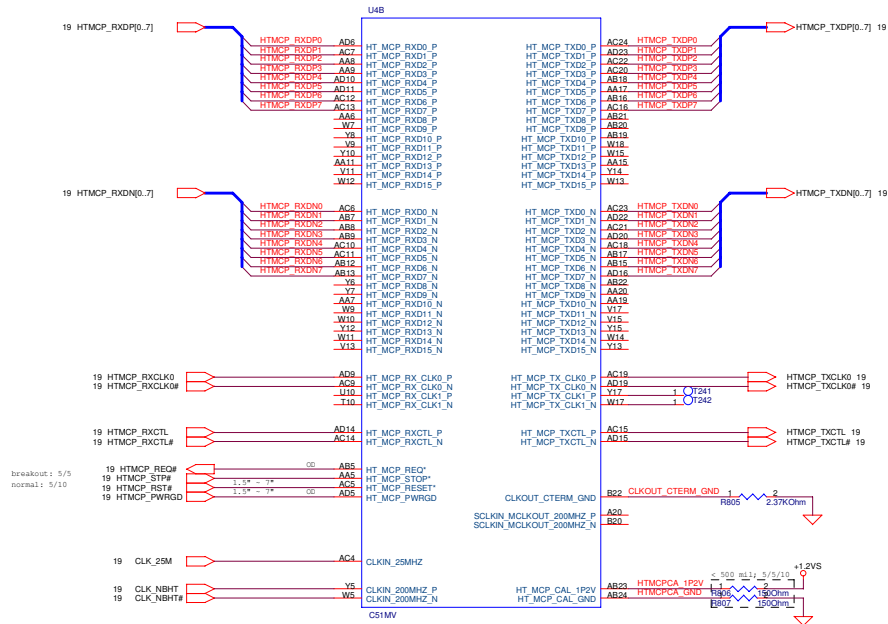
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DESIGN ENGINEER: Albert Su

ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET 11 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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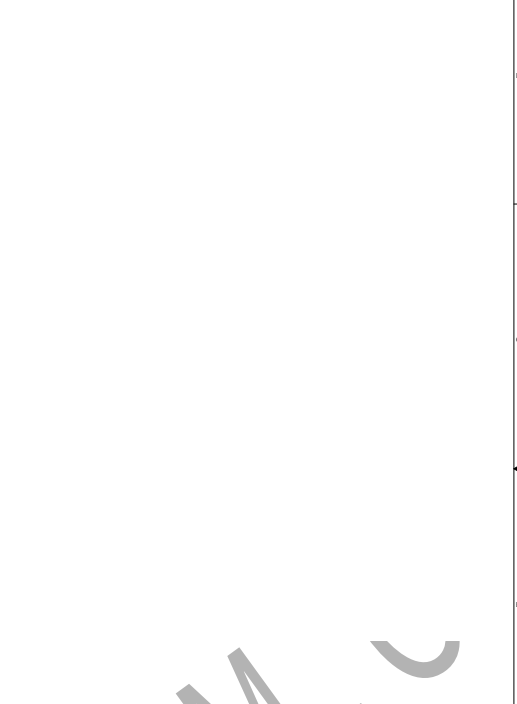
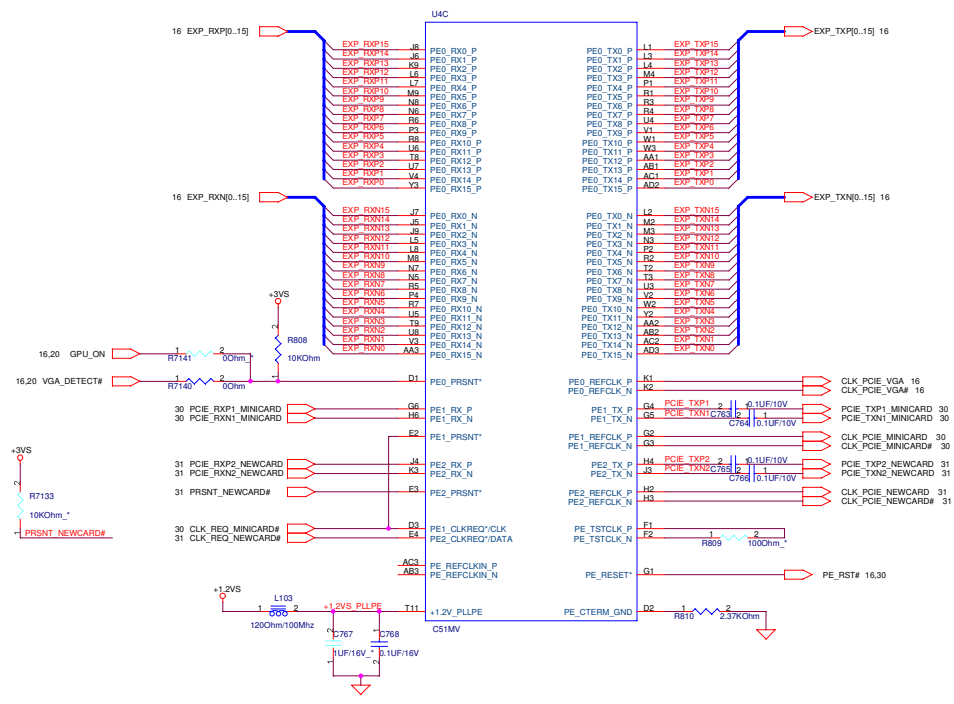
breakout: 5/5
normal: 5/10

Core Designs

ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME:	DESIGN ENGINEER:
		2.1	SHEET 12 OF 55	C51M HT TO MCP	RELEASE DATE:	Albert Su

<< Kennedy_Zhang >>

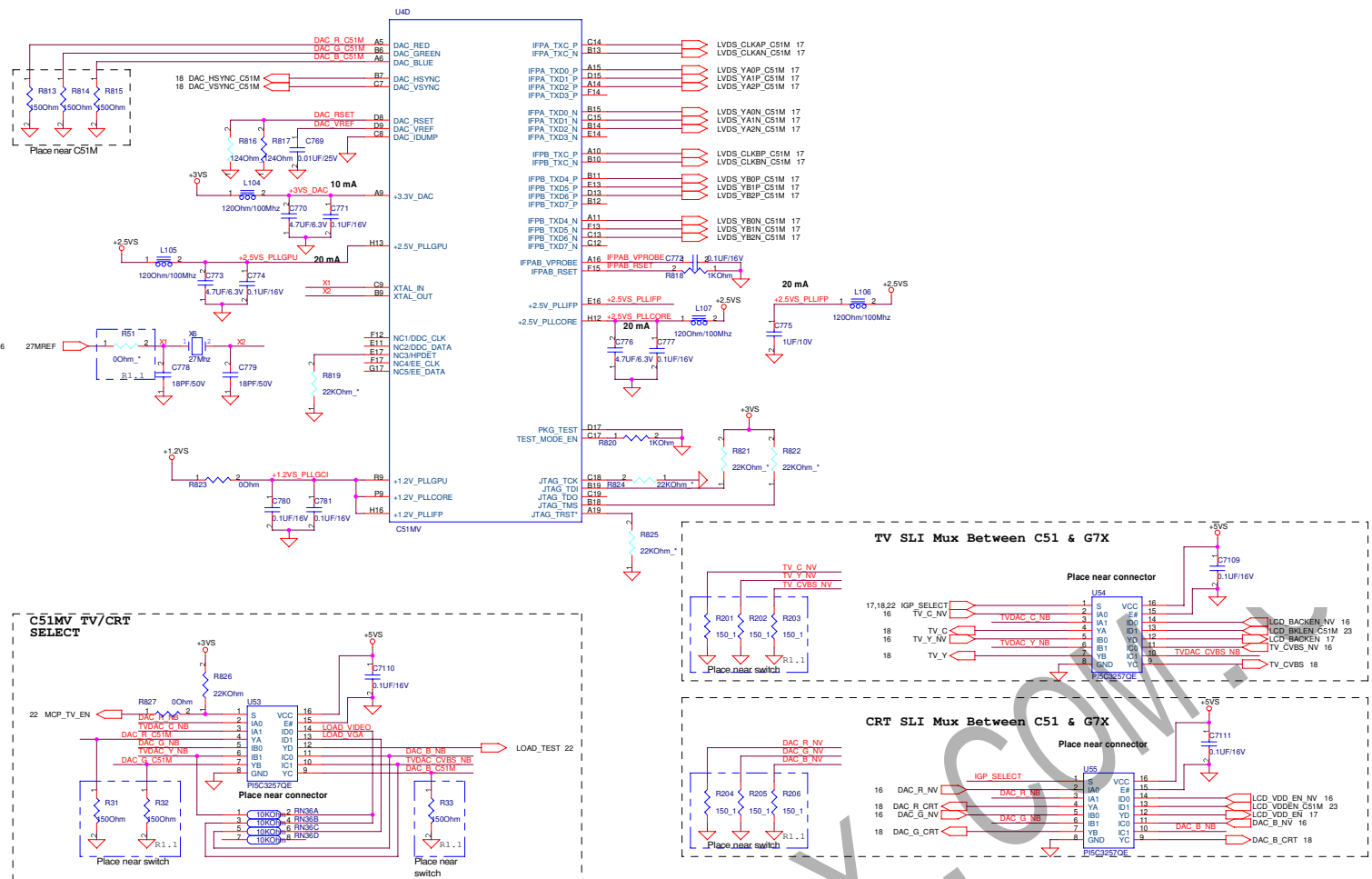
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ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PCI-E	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 13 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

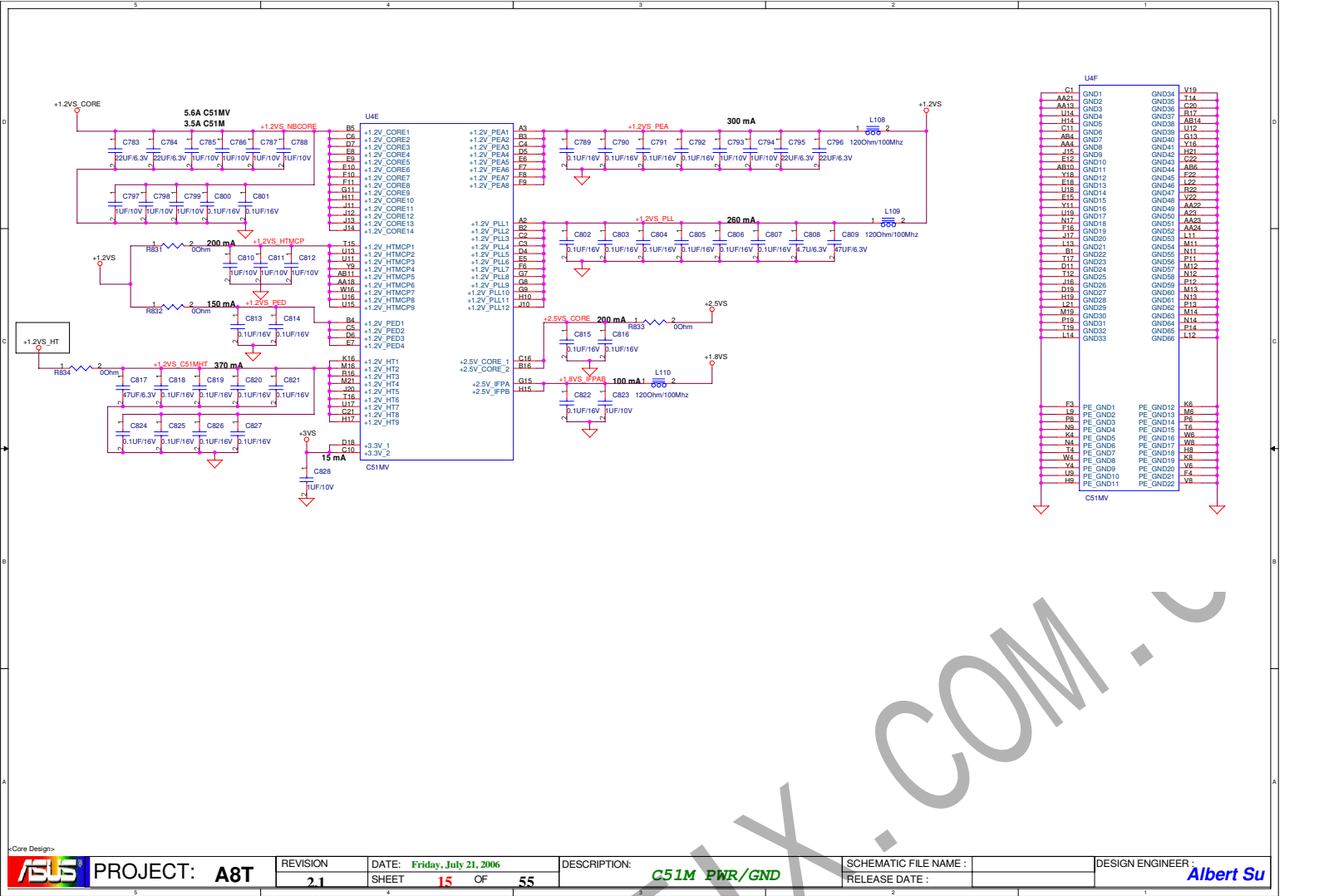
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ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M CRT&LVDS	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 14	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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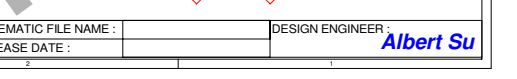
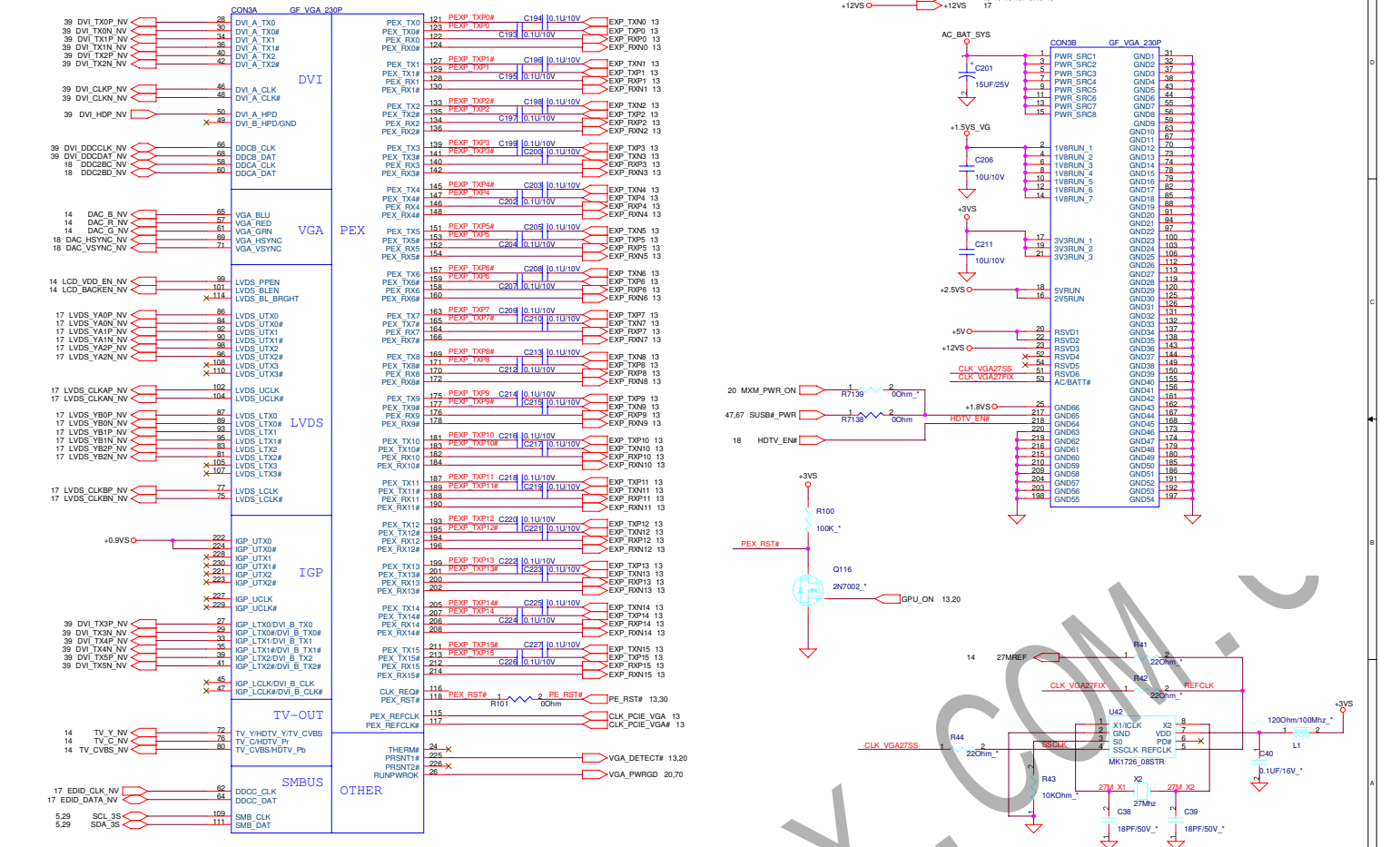
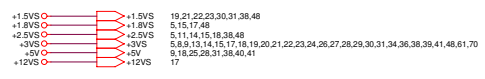
U4F			
G1	GND1	GND34	V19
AA21	GND2	GND35	T14
AA33	GND3	GND36	C20
U44	GND4	GND37	R17
H14	GND5	GND38	AB14
C11	GND6	GND39	U12
GND6		GND40	G13
AB4	GND7	GND41	Y16
AA4	GND8	GND42	H21
J15	GND9	GND43	AB6
GND9		GND44	C22
AB10	GND10	GND45	AB8
E12	GND11	GND46	L22
Y18	GND12	GND47	P22
E18	GND13	GND48	Y22
U18	GND14	GND49	AA22
E12	GND15	GND50	AA3
Y11	GND16	GND51	AA23
U19	GND17	GND52	AA24
N17	GND18	GND53	AA25
F16	GND19	GND54	M11
J17	GND20	GND55	L11
L13	GND21	GND56	P11
BL	GND22	GND57	M12
T17	GND23	GND58	P12
D11	GND24	GND59	M13
T12	GND25	GND60	P13
N16	GND26	GND61	M14
D19	GND27	GND62	P14
M19	GND28	GND63	M15
L21	GND29	GND64	P15
M18	GND30	GND65	M16
F18	GND31	GND66	L12
L14	GND32		
L14	GND33		

ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: G51M PWR/GND	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 15	OF: 55		RELEASE DATE:	

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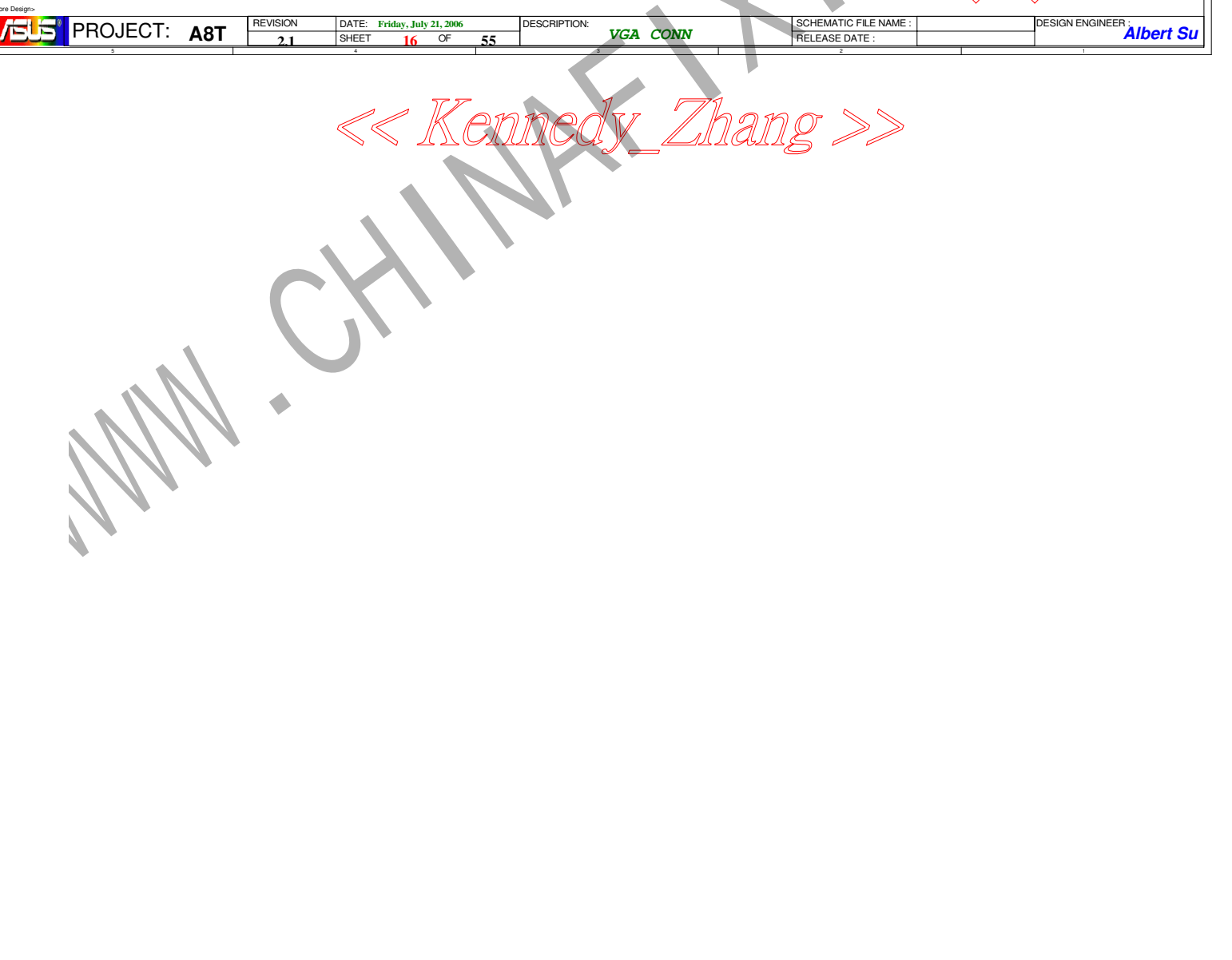
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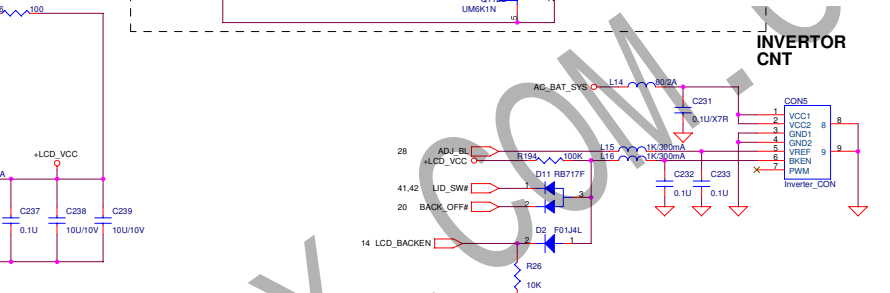
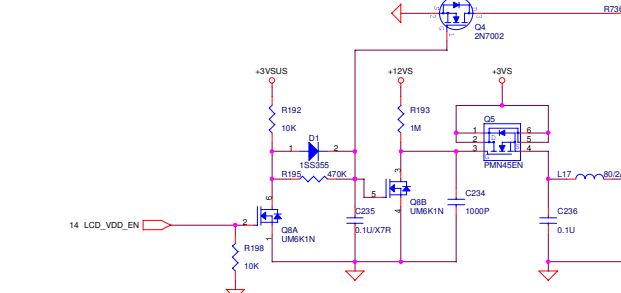
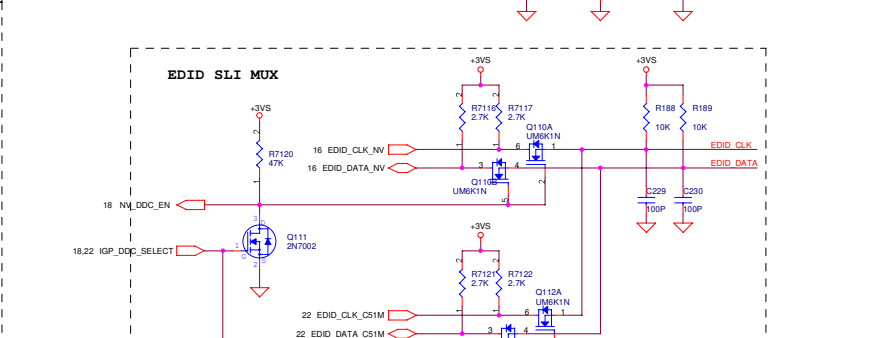
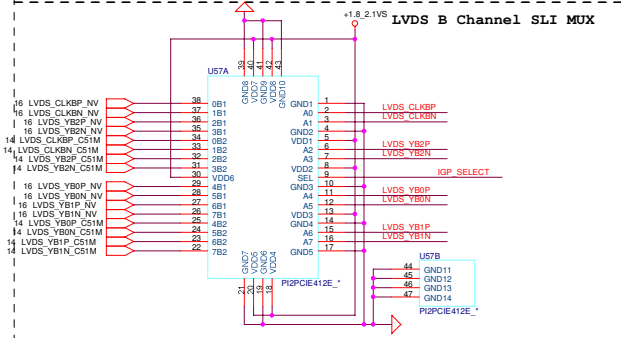
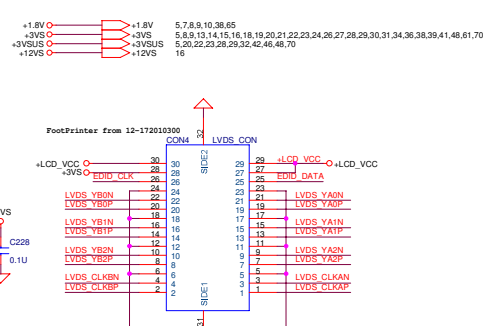
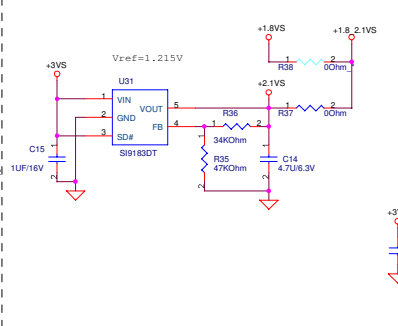
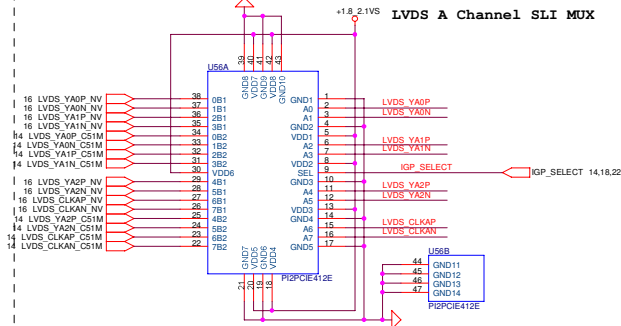
Parity Inversion:
PEXP_TXP0, 1, 2, 4, 5,
6, 8, 14



ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: VGA CONN	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	SHEET 16 OF 55			RELEASE DATE:	

<< Kennedy_Zhang >>

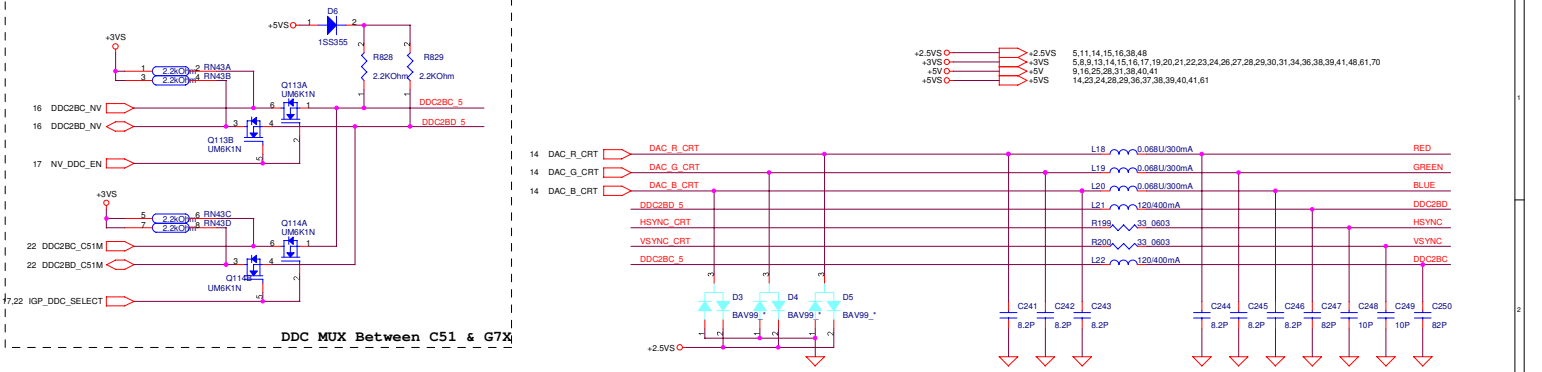




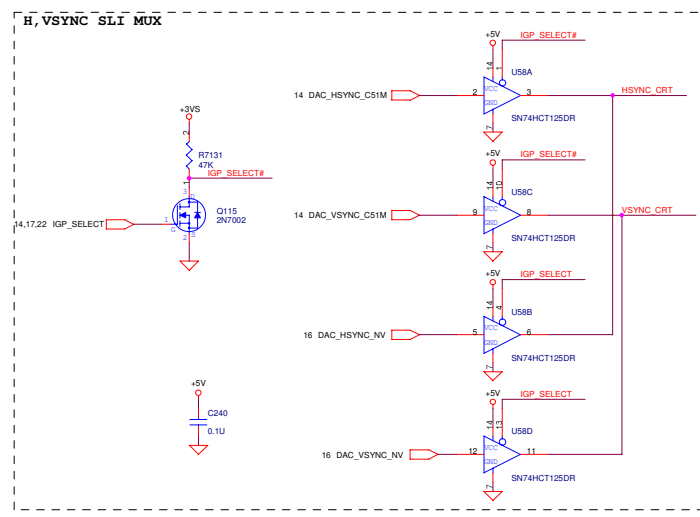
ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: LVDS, INVERTER CONN	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
	SHEET: 17	OF: 55	RELEASE DATE: _____		

<< Kennedy_Zhang >>

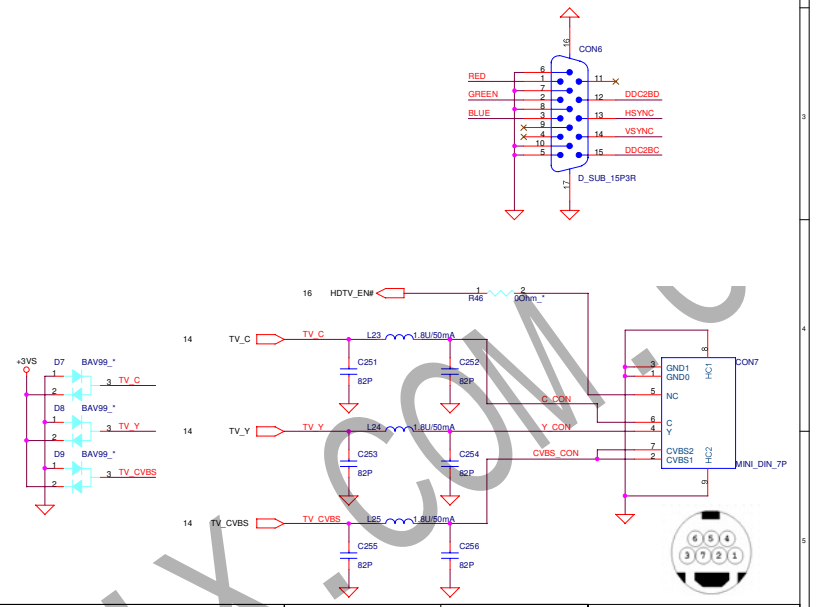
WWW.CHINAHELP.COM



DDC MUX Between C51 & G7X



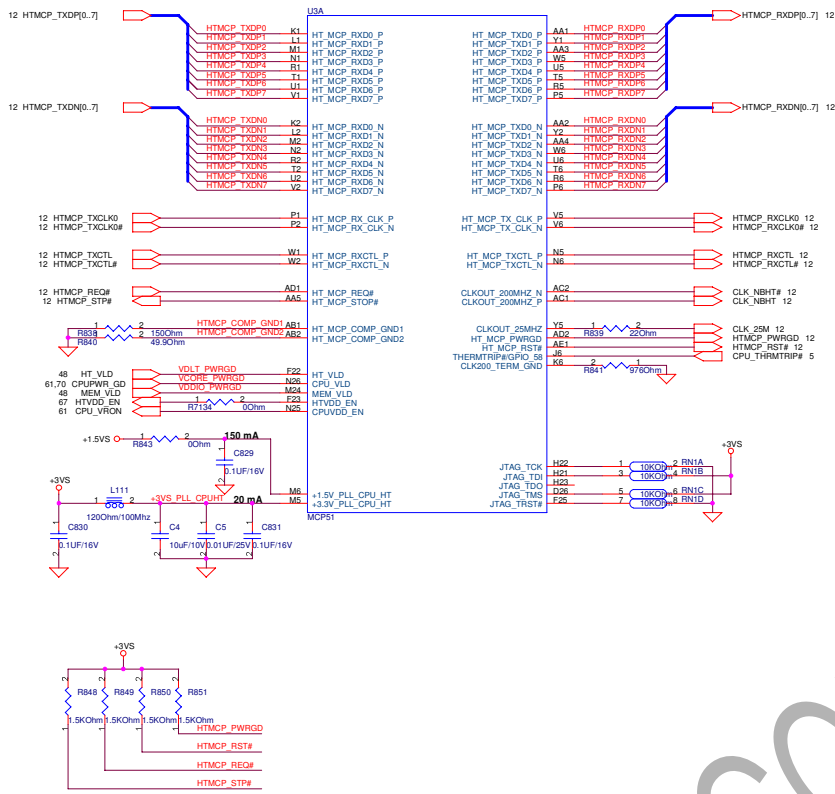
H_VSYNC SLI MUX



ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		2.1	SHEET 18 OF 55	CRT & TV OUT	RELEASE DATE :	Albert Su

<< Kennedy_Zhang >>

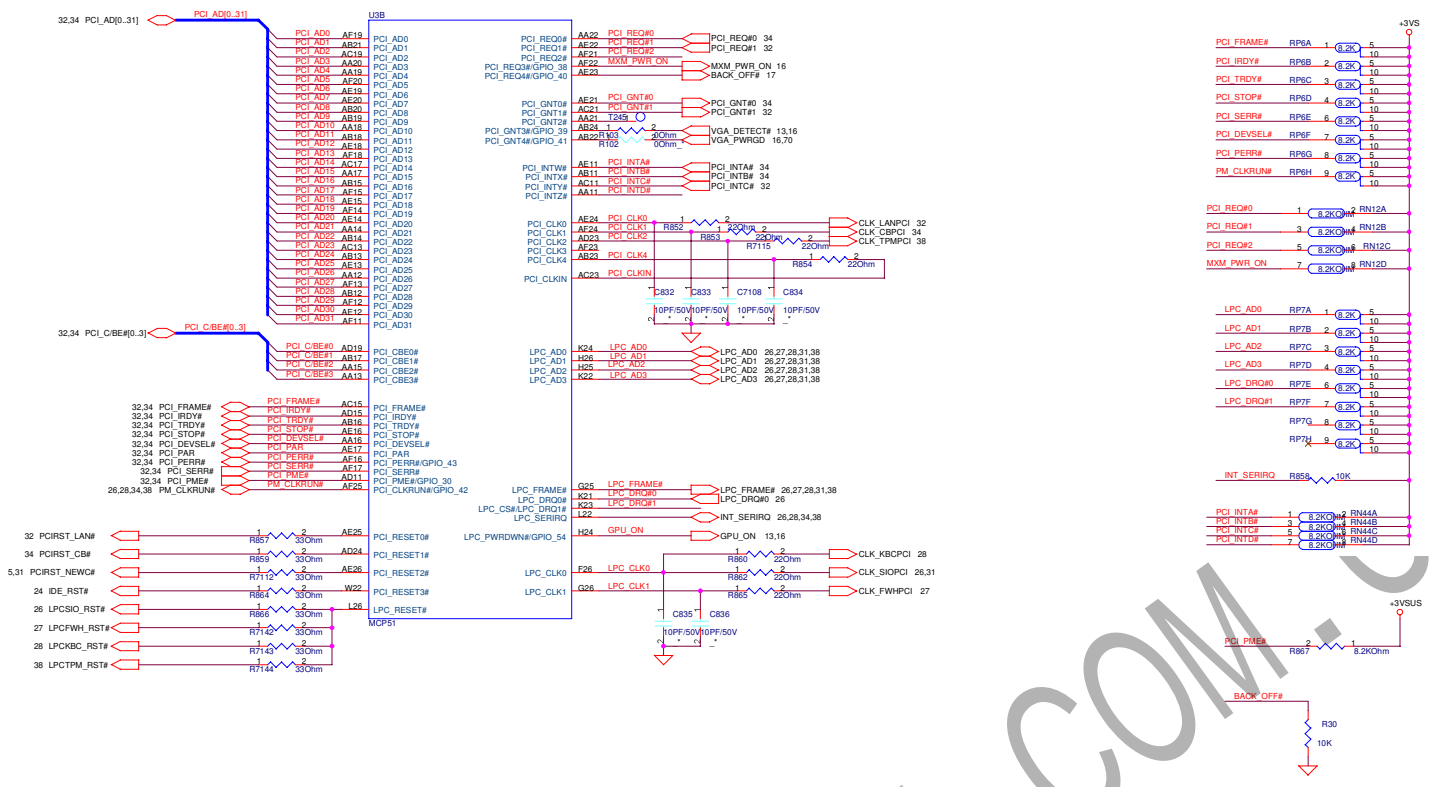
WWW.CHINAFAIR.COM



ASUS PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 HT I/F	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 19	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>

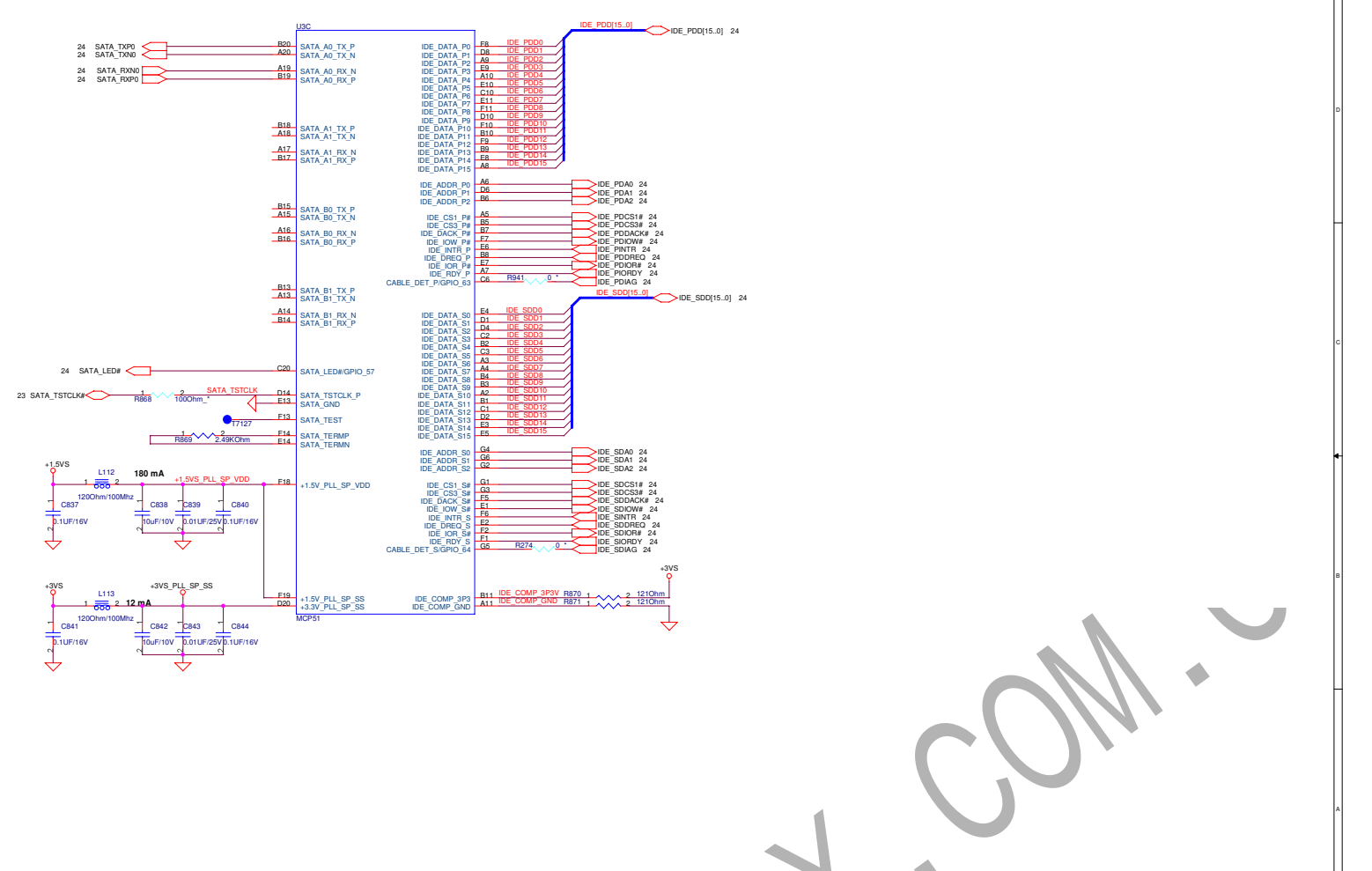
WWW.CHINAFAIRY.COM.CN



ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PCI	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 20	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>

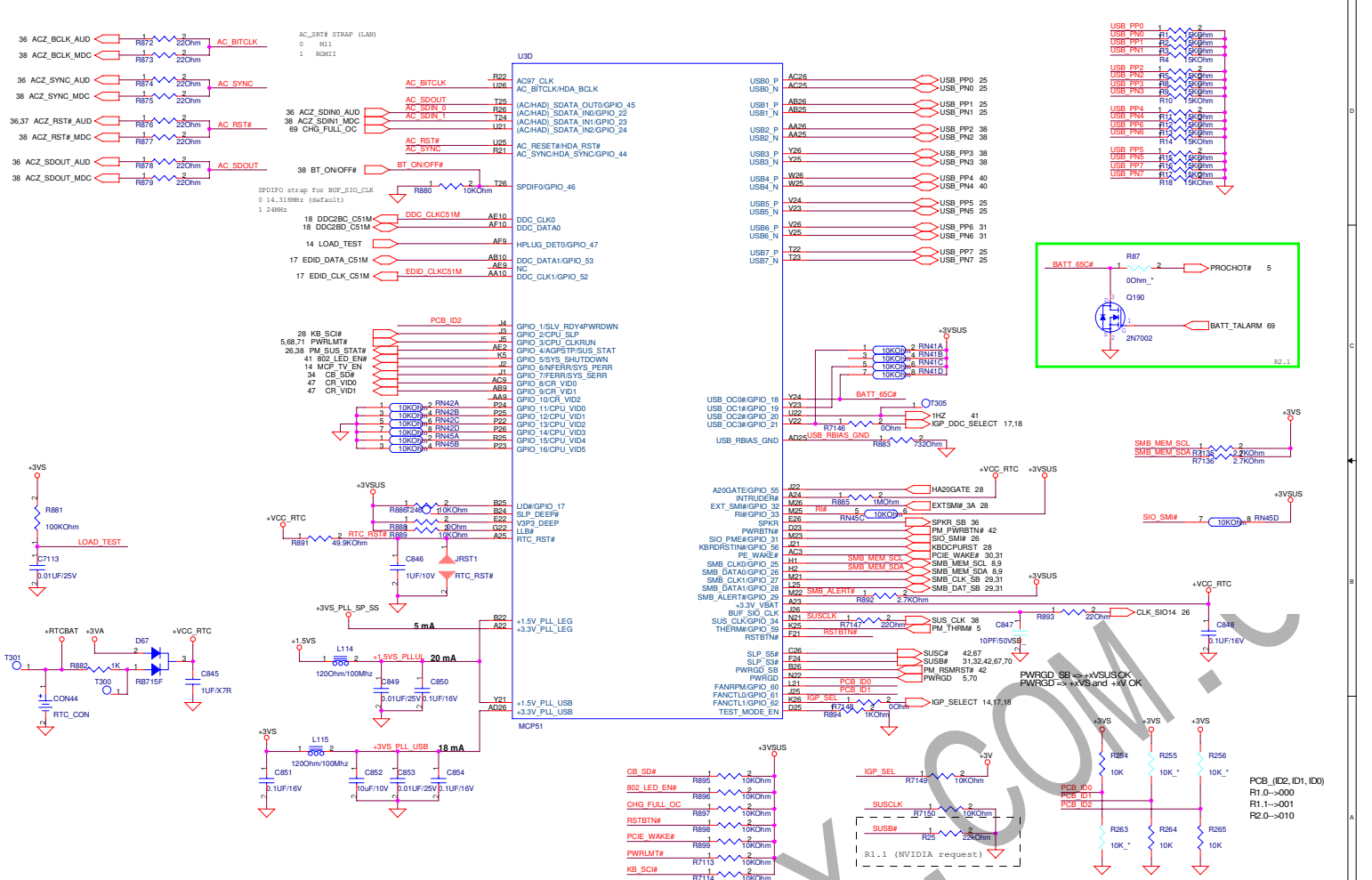
WWW.CHINAPEIX.COM



ASUS PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 IDE	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET 21	OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

WWW.CHINAFIX.COM.CN

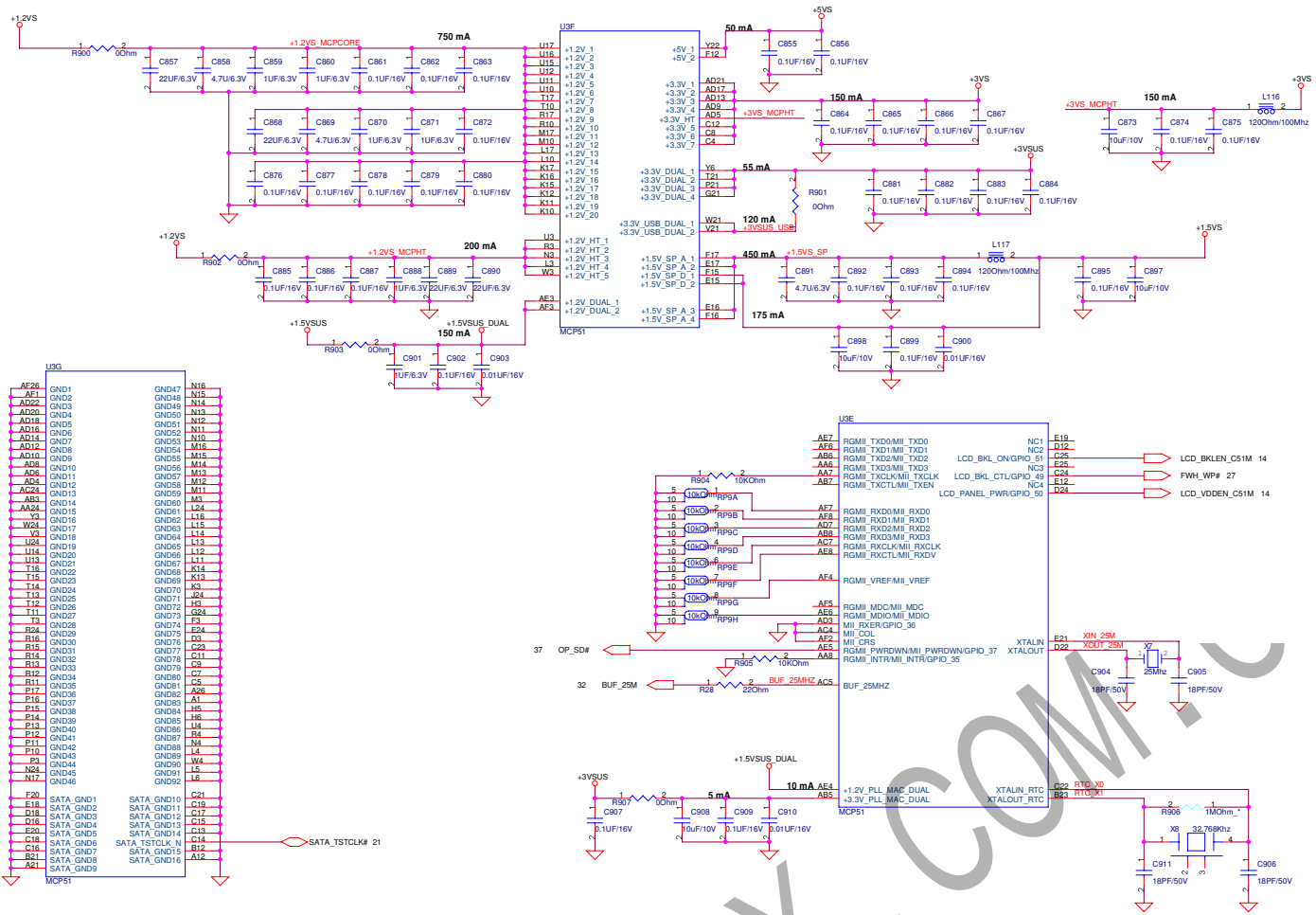


REVISION	DATE	DESCRIPTION	SCHEMATIC FILE NAME	DESIGN ENGINEER
2.1	Friday, July 21, 2006	MCP51 USB/HDA		Albert Su

PROJECT	SHEET	OF	RELEASE DATE
A8T	22	55	

« Kennedy_Zhang »

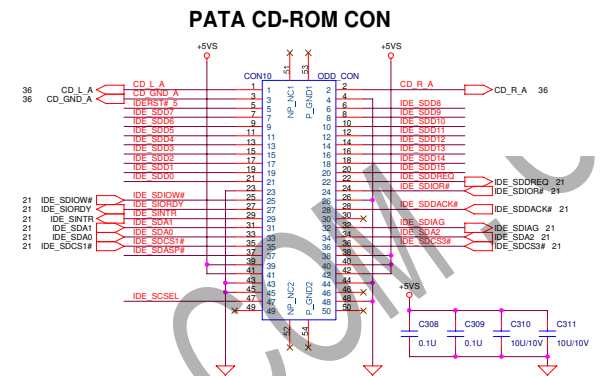
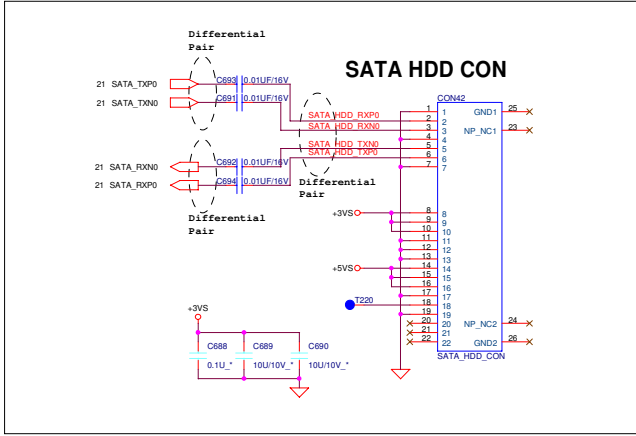
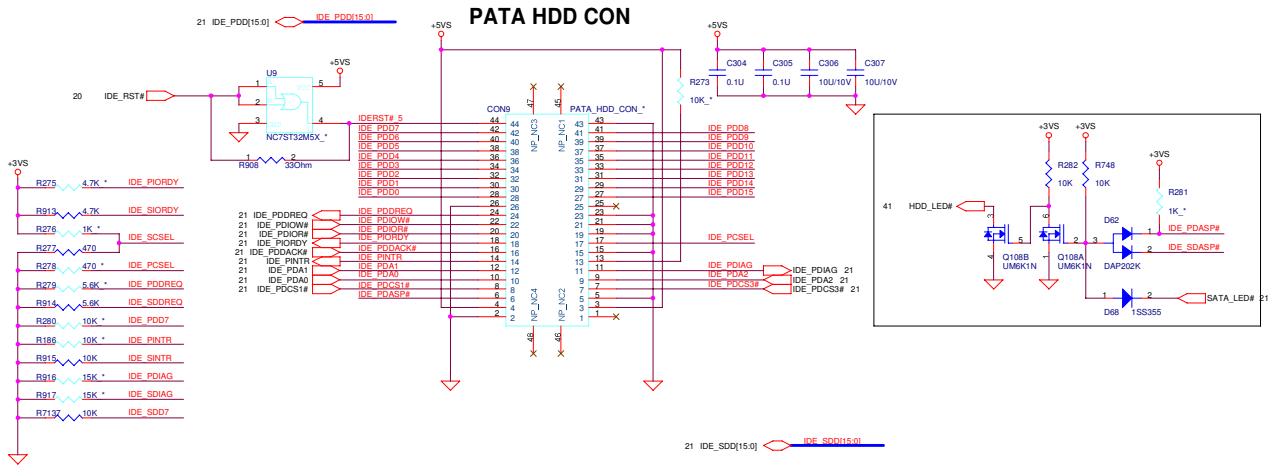
WWW.CHINAFAIRWAY.COM



ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PWR/GND	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
	SHEET: 23 OF 55		RELEASE DATE: _____		

<< Kennedy_Zhang >>

WWW.CHINAKEY.COM

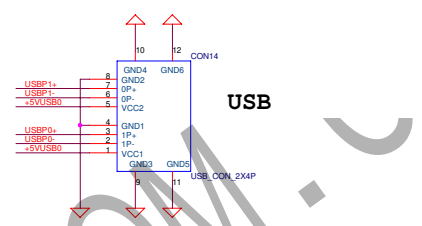
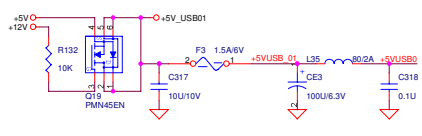
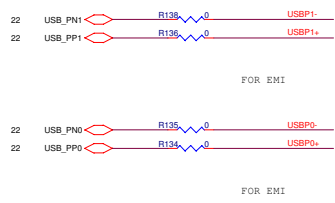
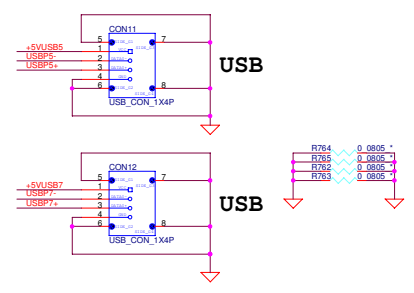
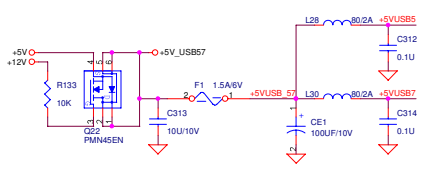
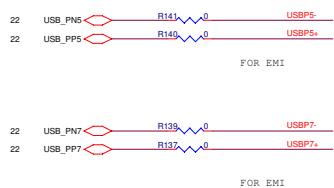


+3VS ○ → +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30,31,34,36,38,39,41,48,61,70
 +5VS ○ → +5VS 14,16,23,28,29,36,37,38,39,40,41,61
 +5V ○ → +5V 9,16,18,25,28,31,38,40,41

ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: HDD & CD-ROM CONN	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	2.1	SHEET 24 OF 55	RELEASE DATE:		

<< Kennedy_Zhang >>





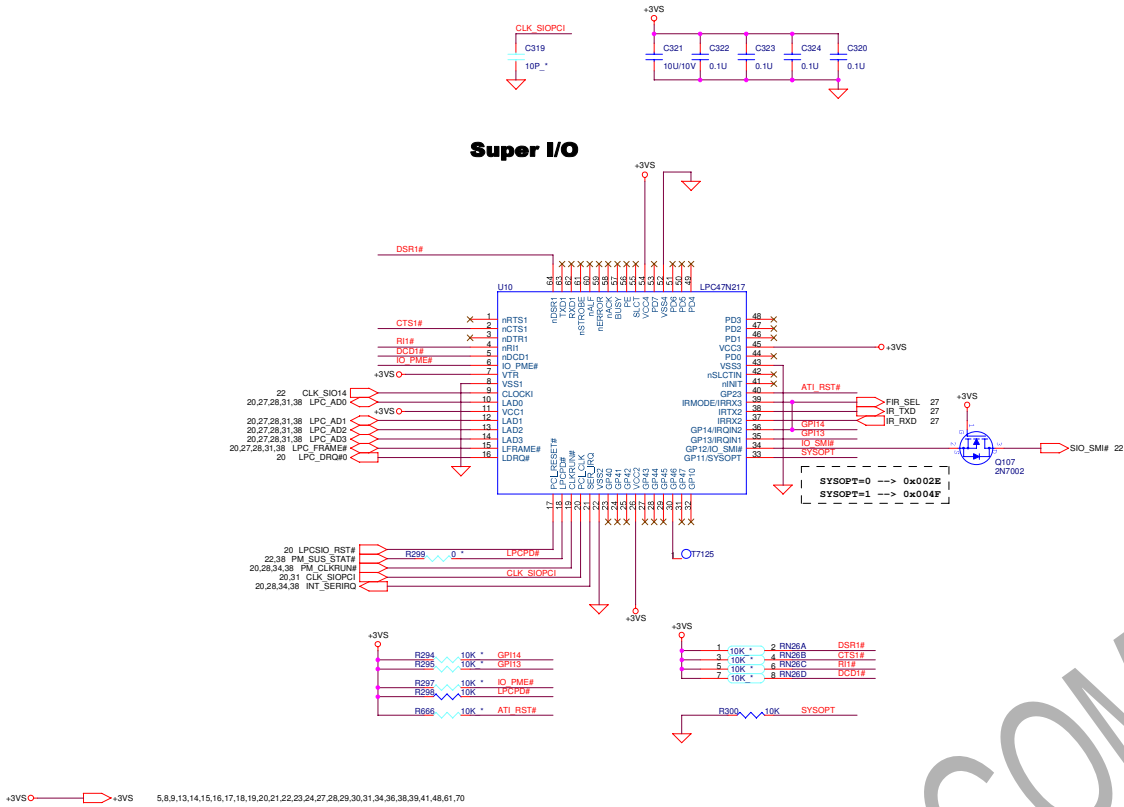
+5V \rightarrow +5V 9,16,18,28,31,38,40,41

ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: USB PORTS	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 25 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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Super I/O

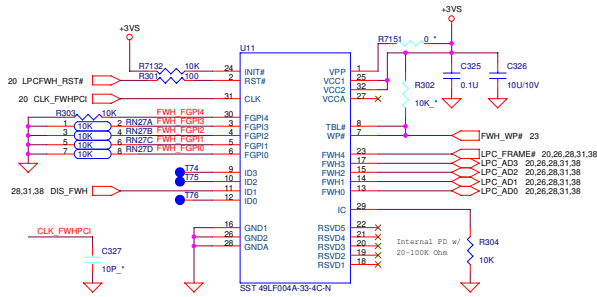


+3VS \rightarrow +3VS 5,6,8,13,14,15,16,17,18,19,20,21,22,23,24,27,28,29,30,31,34,36,38,39,41,48,61,70

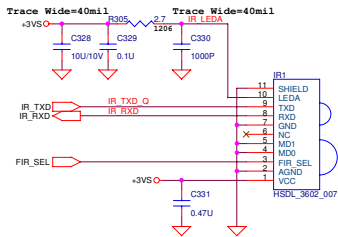
ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SUPER IO LPC47N217	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	2.1	SHEET 26 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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PLCC32 Socket Part Number :
12G043400324
Graphics from:
05-001005111



+3VS → +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,30,31,34,36,38,39,41,48,61,70

Core Design

ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: BIOS, IR	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 27 OF 55		RELEASE DATE:	

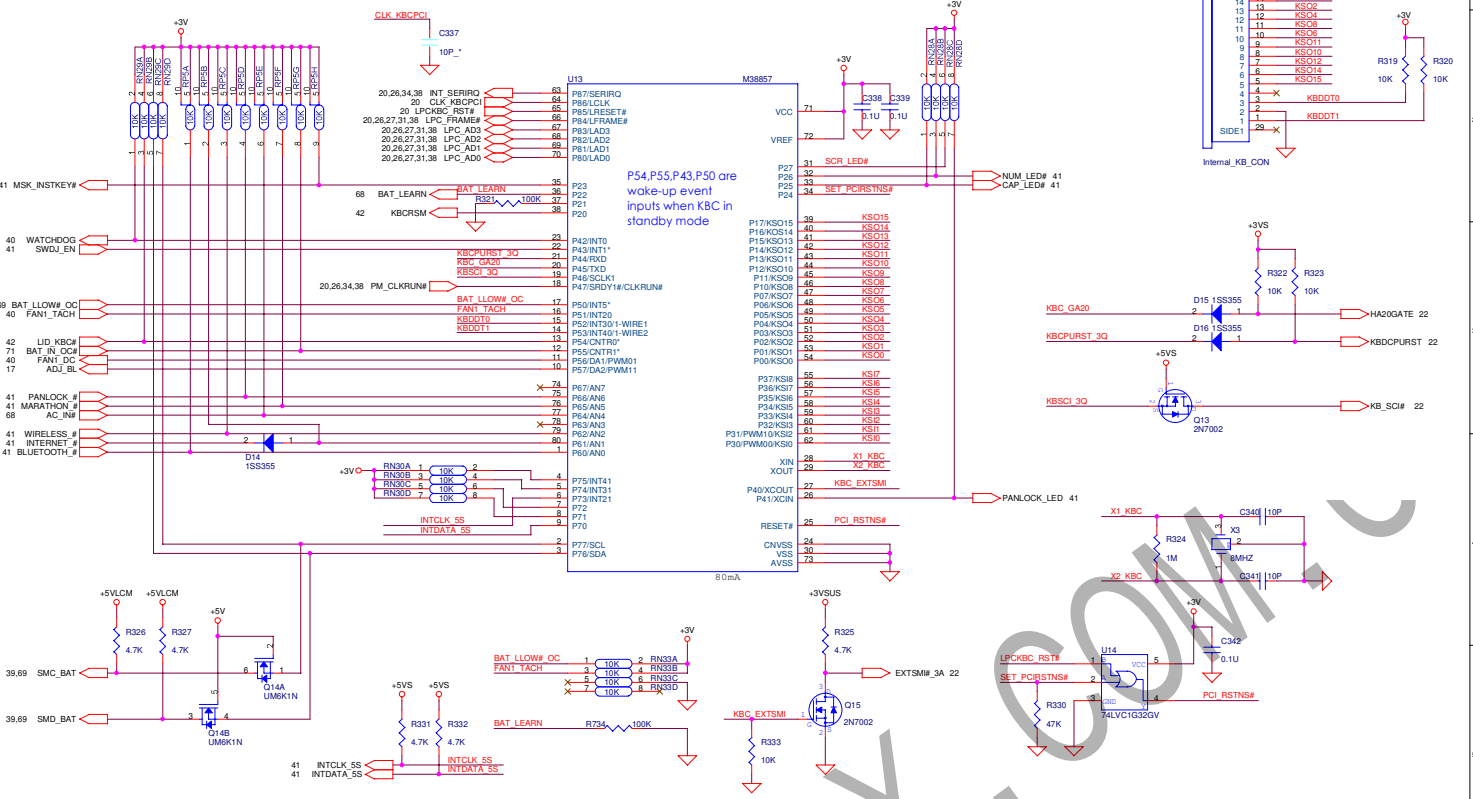
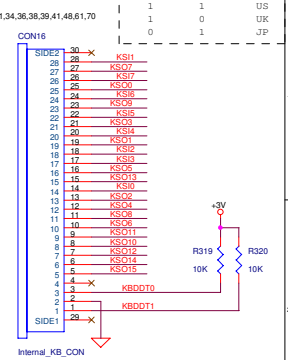
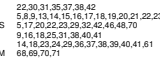
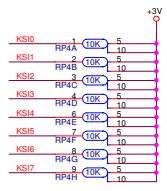
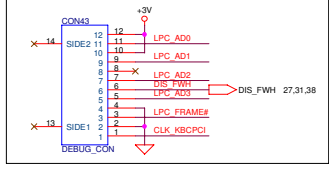
<< Kennedy_Zhang >>

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage

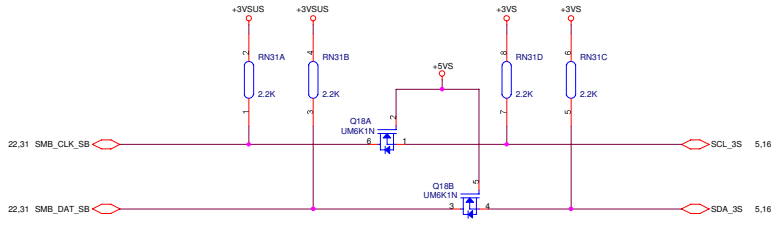


ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: KBC 38857	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 28	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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MCP51



Terminal Sensor,
TPM

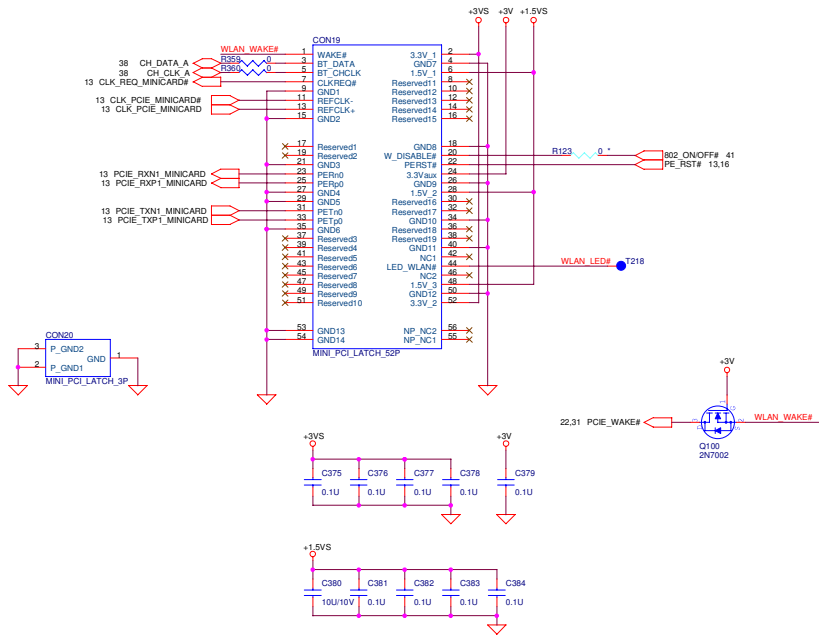
+3VA	→	+3VA	22,38,41,42,48,71
+3VSUS	→	+3VSUS	5,17,20,22,23,28,32,42,46,48,70
+0.9VS	→	+0.9VS	16
+1.5VS	→	+1.5VS	19,21,22,23,30,31,38,48
+2.5VSC	→	+2.5VSC	5,11,14,15,16,18,38,48
+3VS	→	+3VS	5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,34,38,39,39,41,48,61,70
+5VS	→	+5VS	14,18,23,24,28,36,37,38,39,40,41,61
+12VS	→	+12VS	16,17
+1.8V	→	+1.8V	5,7,8,9,10,38,65
+3V	→	+3V	22,28,30,31,35,37,38,42
+5V	→	+5V	9,18,19,25,28,31,38,40,41
+12V	→	+12V	25,40
+VCORE	→	+VCORE	5,7,61
+5VLCM	→	+5VLCM	28,68,69,70,71

Core Design

ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SM BUS & POWER PORT	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 29 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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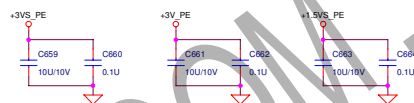
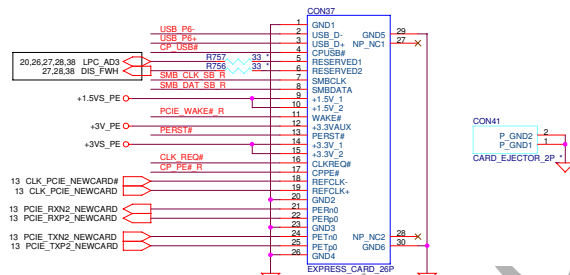
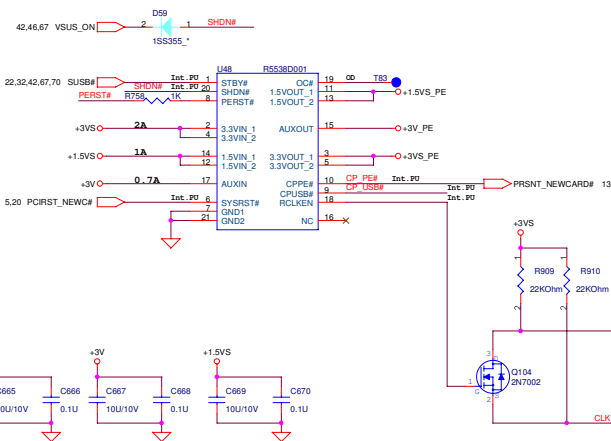
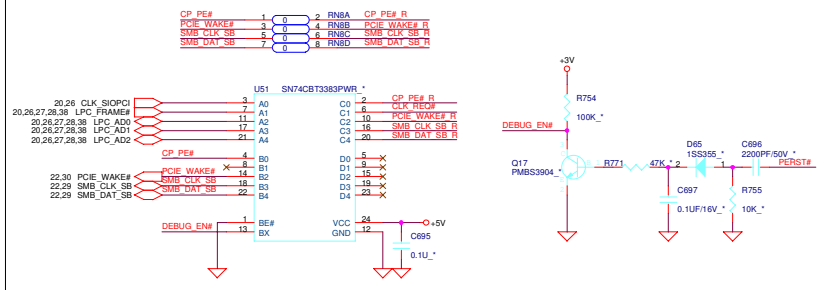
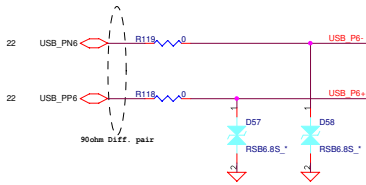
+1.5VS → +1.5VS 19,21,22,23,31,38,48
 +3V → +3V 22,28,31,35,37,38,42
 +3VS → +3VS 5,6,8,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,31,34,36,38,39,41,48,61,70

Core Designs

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: MINI CARD	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		2.1	SHEET 30 OF 55		RELEASE DATE :	

<< Kennedy_Zhang >>

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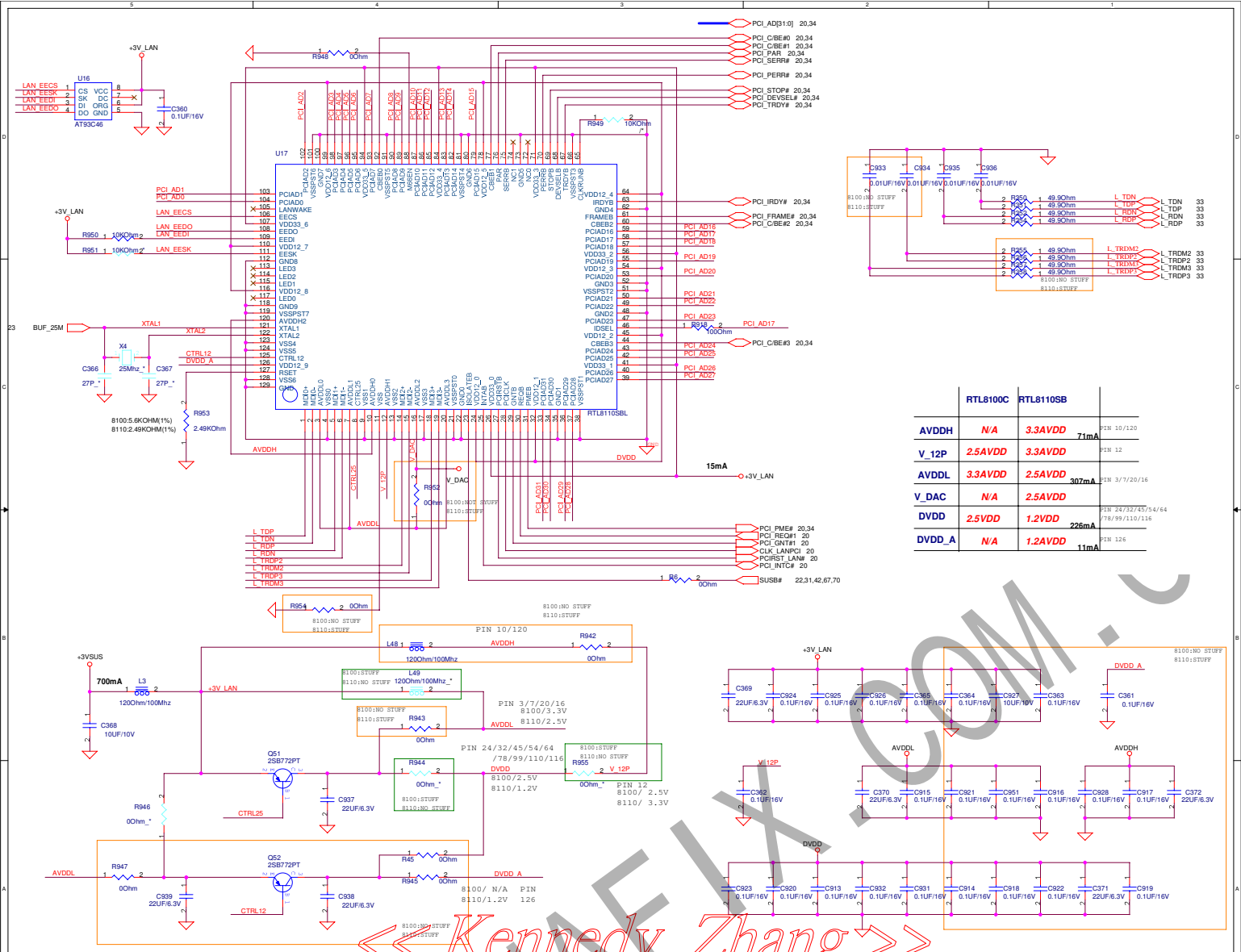
+1.5V C 19,21,22,23,30,38,48
 +3V C 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,34,36,38,39,41,48,61,70
 +3V C 22,28,30,35,37,38,42

Core Designs


ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: NEW_CARD	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
	SHEET 31 OF 55			RELEASE DATE: _____	

<< Kennedy_Zhang >>

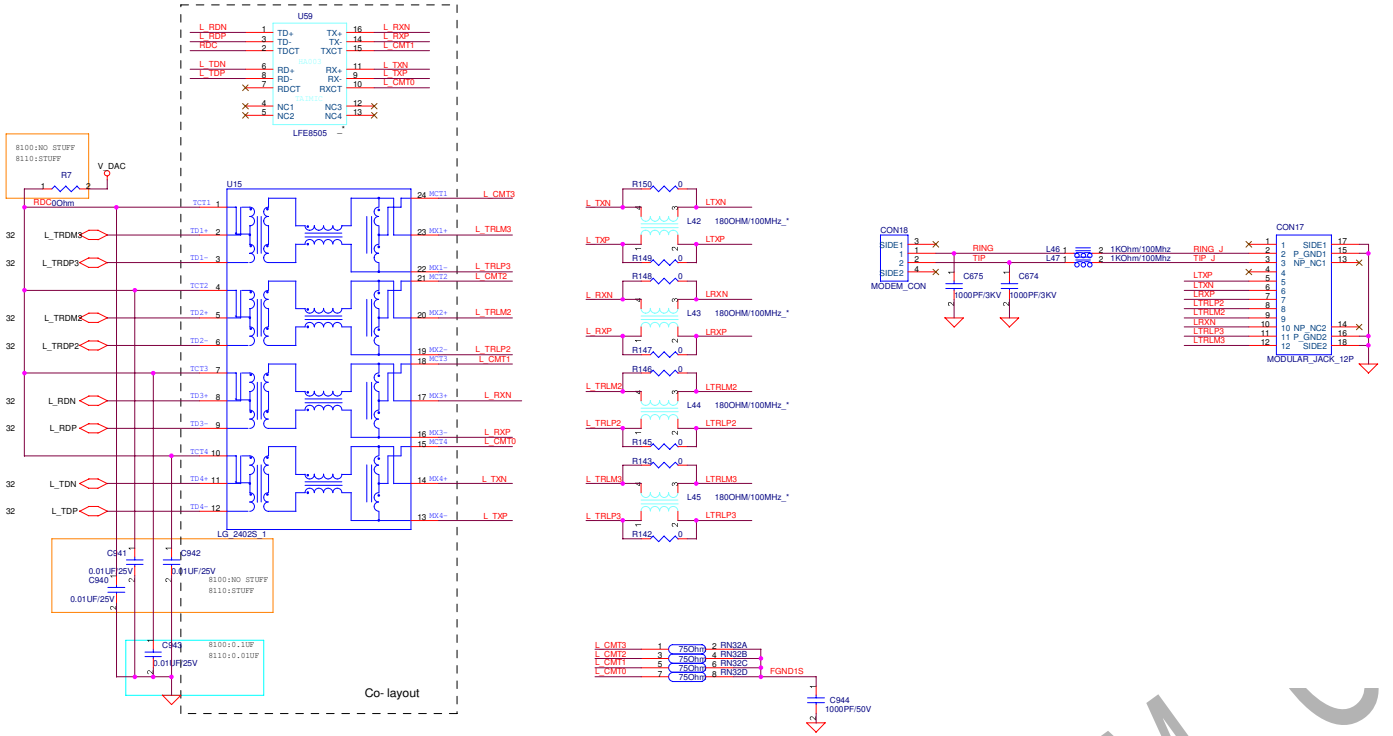
WWW.CHINAFFIX.COM



Kennedy Zhang

 PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: LAN -- RTL8100CL	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	SHEET 32 OF 55			RELEASE DATE:	

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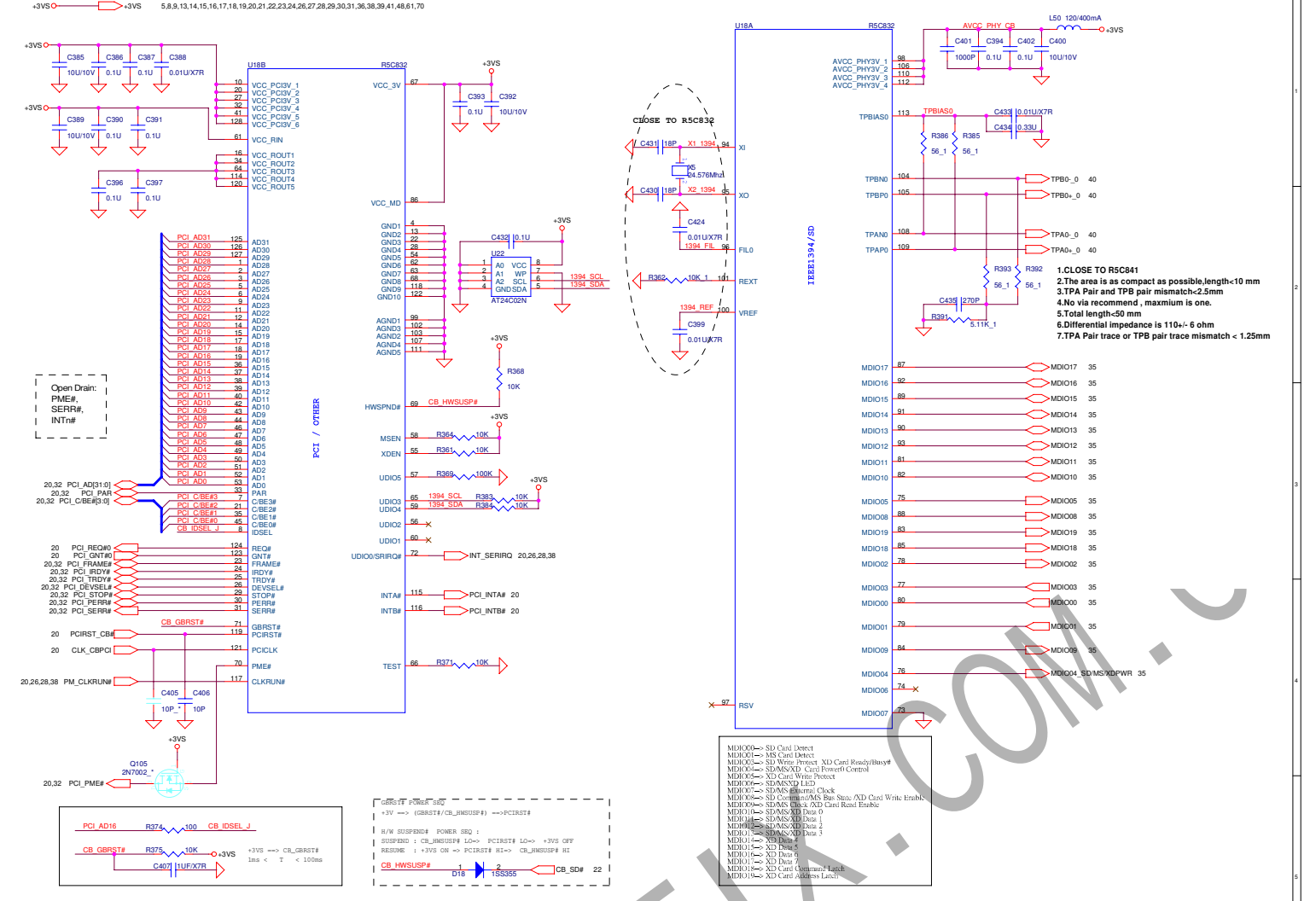


Core Design

	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 33 OF 55		RELEASE DATE:	

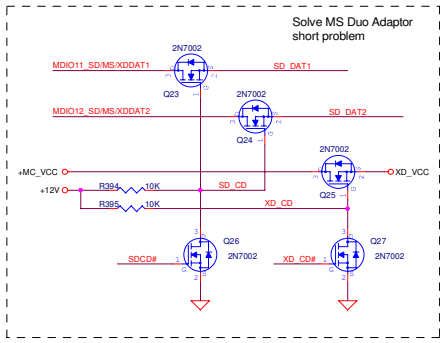
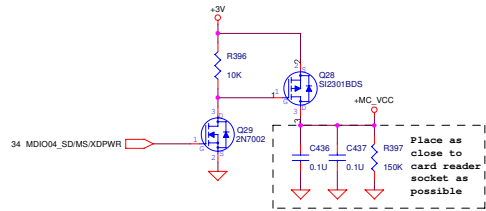
<< Kennedy_Zhang >>

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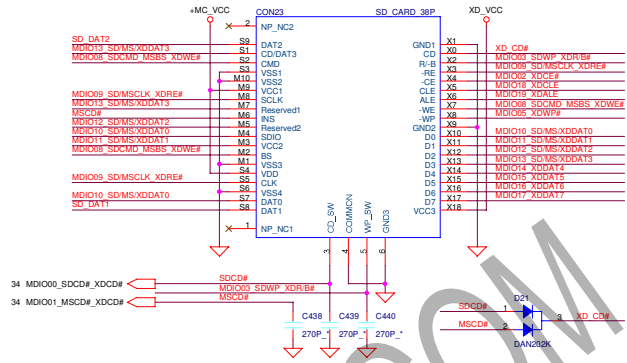


« Kennedy Zhang »

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+3V O → +3V 22.28,30.31,37.38,42
 +12V O → +12V 25.37,40.67

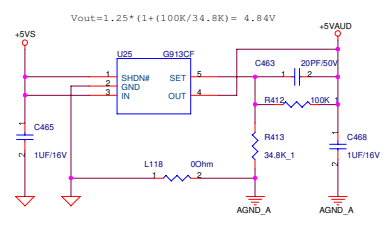
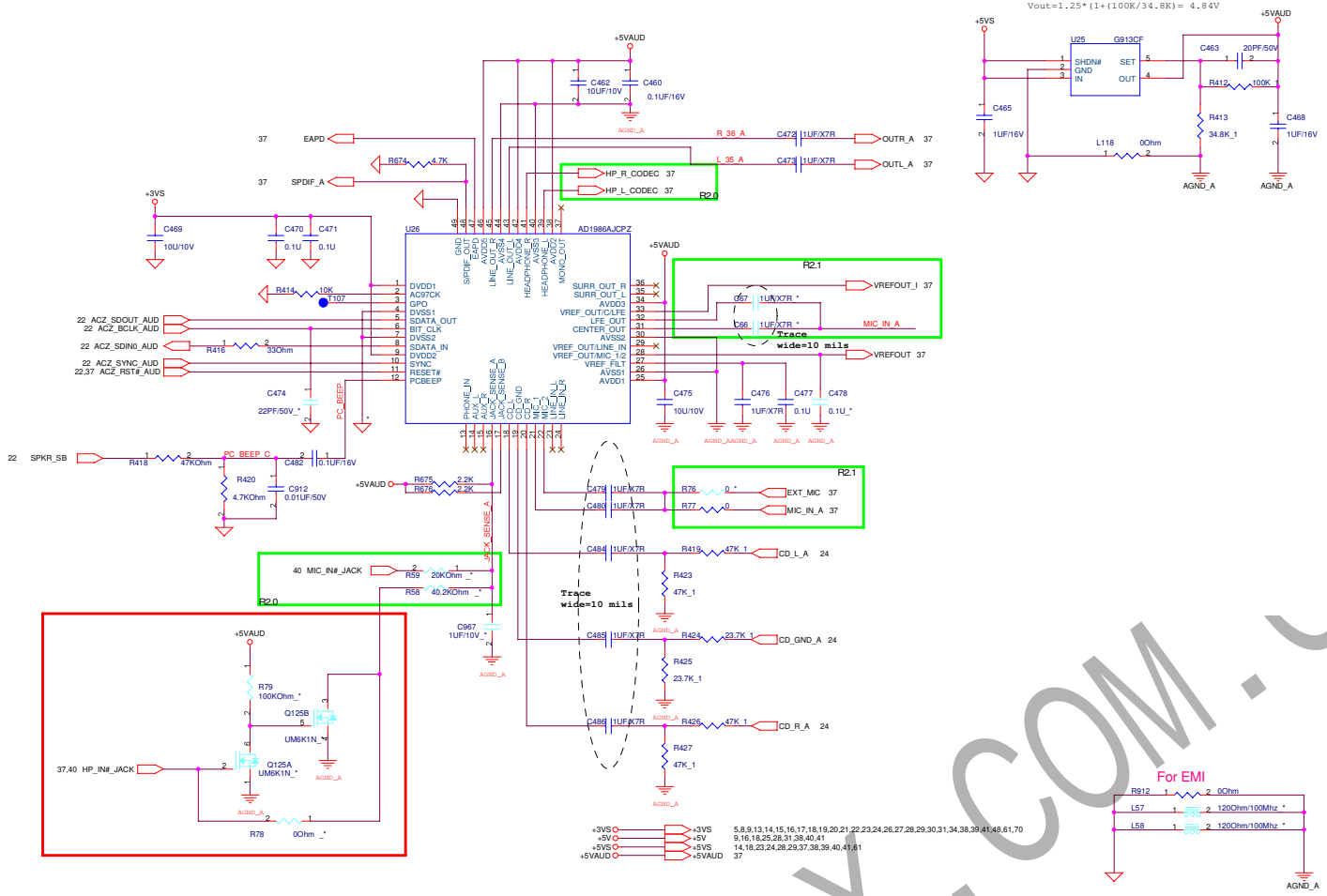


<Core Design>

	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: 4 IN 1 CONN	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET 35 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

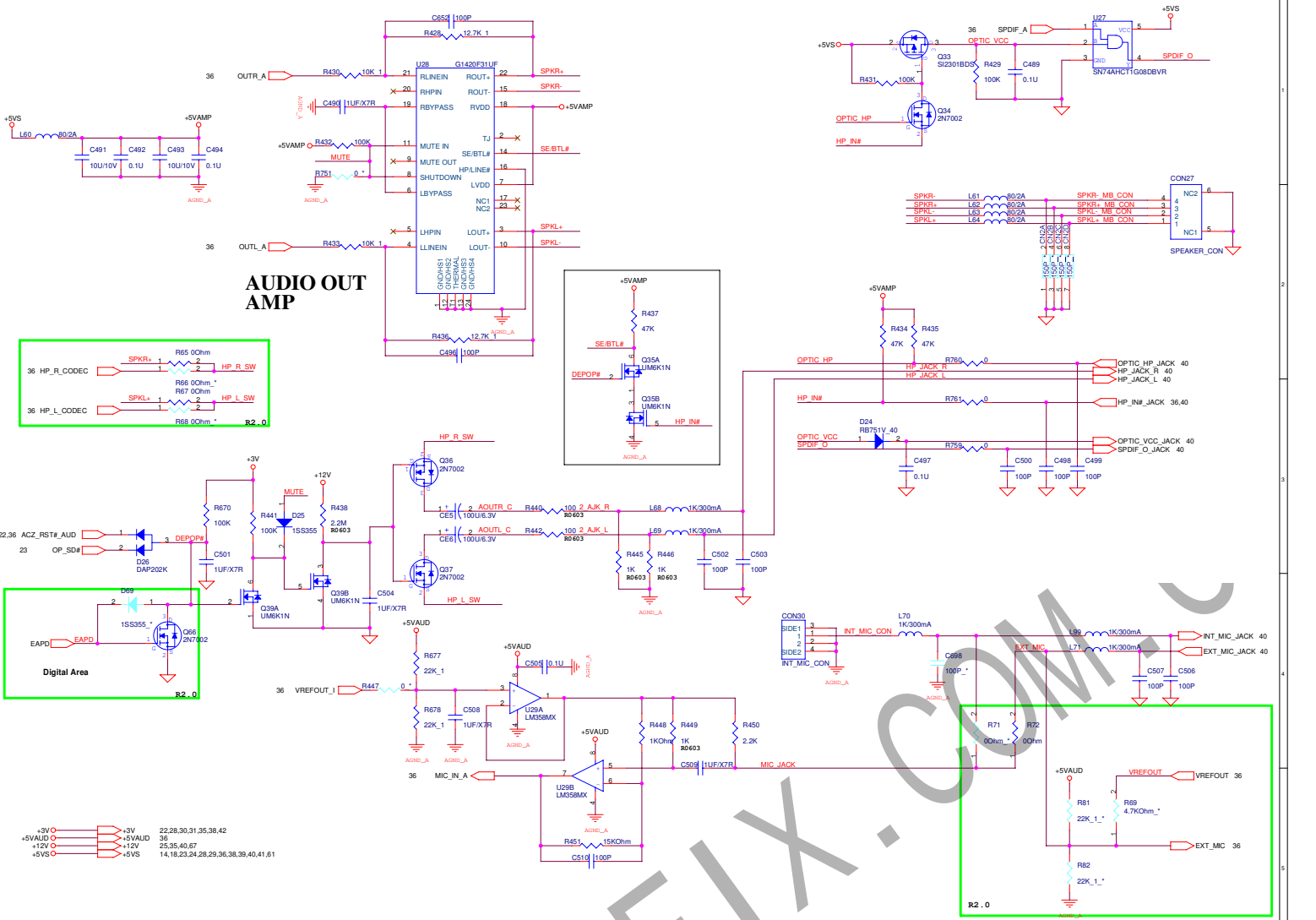
WWW.CHINAHELPX.COM



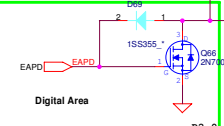
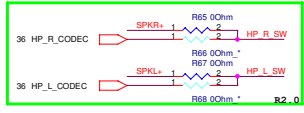
Core Design:		ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 36 OF 55			RELEASE DATE:	

<< Kennedy_Zhang >>

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AUDIO OUT AMP

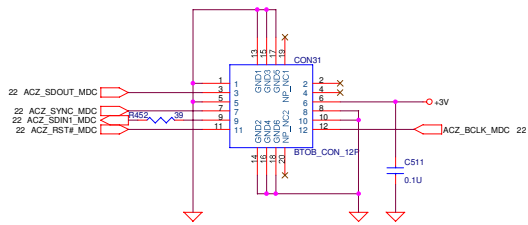


+3V	22,28,30,31,35,38,42
+5VAUD	36
+12V	23,35,40,67
+5VS	14,18,23,24,28,29,36,38,39,40,41,61

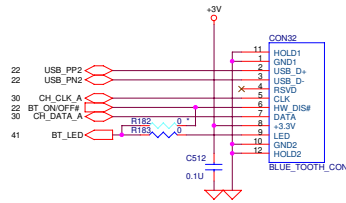
ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: AUDIO AMP (G1420)	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
SHEET: 37 OF 55		RELEASE DATE:			

Kennedy Zhang

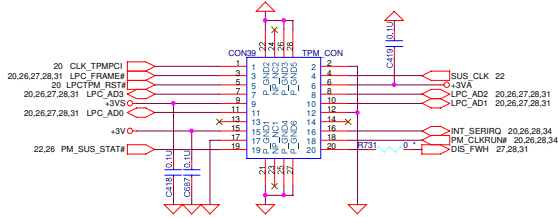
WWW.CHINAELIX.COM



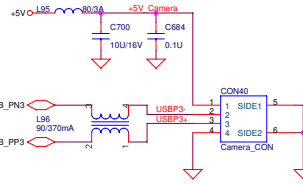
Azalia MDC MODEM CON



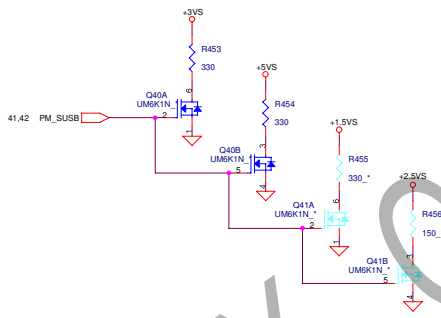
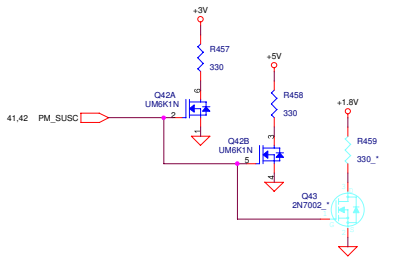
Bluetooth Module CON



TPM Module CON



Camera Module CON



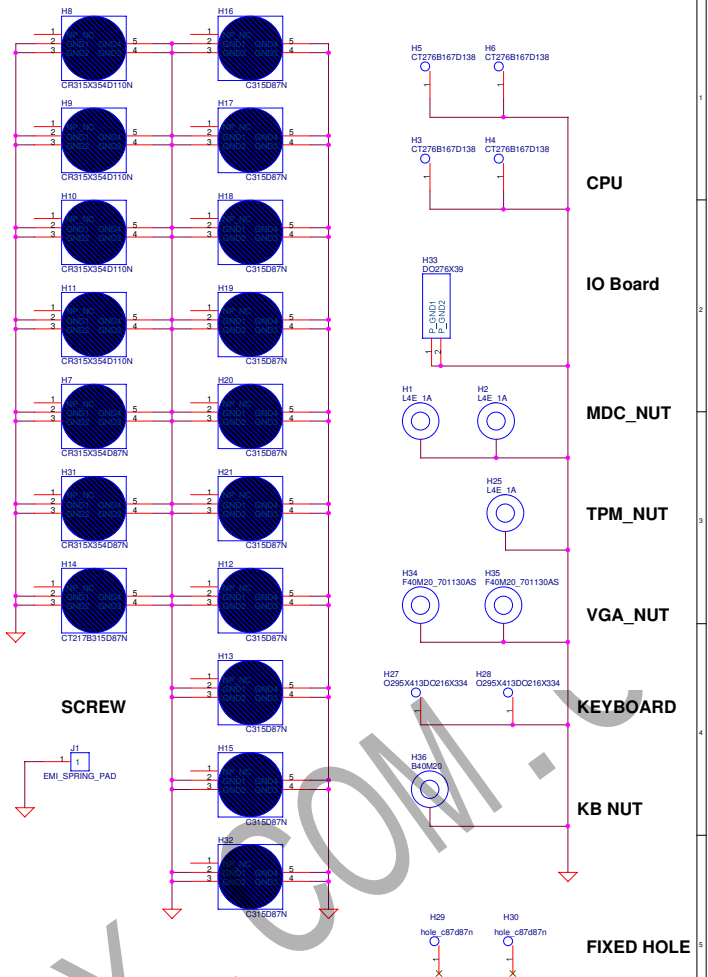
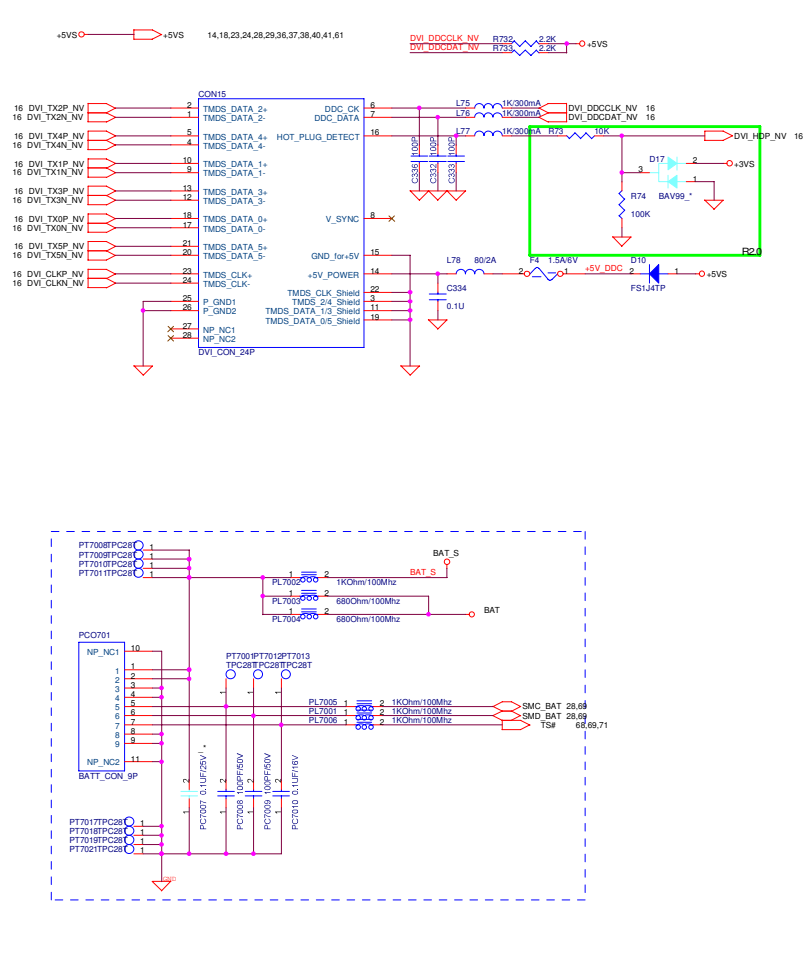
+1.5V	+1.5V	19,21,22,23,30,31,48
+1.8V	+1.8V	5,7,8,9,10,65
+2.5V	+2.5V	5,11,14,15,16,18,48
+3V	+3V	22,29,30,31,35,37,42
+3VS	+3VS	5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,34,36,39,41,48,61,70
+5V	+5V	3,16,18,25,28,31,40,41
+5VS	+5VS	14,18,23,24,28,29,36,37,39,40,41,61

Core Design

	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MDC, B/T, TPM, Camera & DISCHG	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
			SHEET: 38 OF 55		RELEASE DATE: _____	

<< Kennedy_Zhang >>

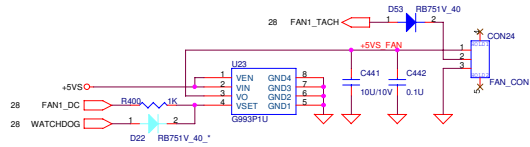
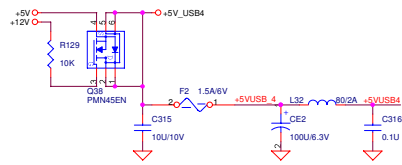
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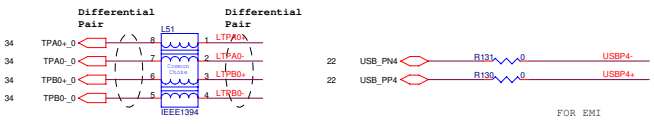
ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DVI CONN & HOLE	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 39 OF 55			RELEASE DATE:	

<< Kennedy_Zhang >>

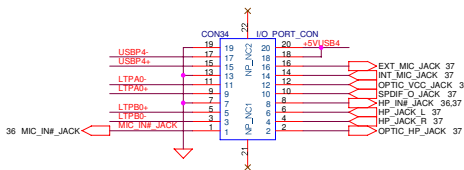
WWW.CHINAKEY.COM



FAN CONTROL

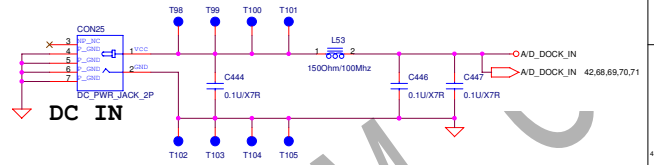


FOR EMI



I/O PORT

+5V 9,16,18,25,28,31,38,41
+5VS 14,18,23,24,28,29,36,37,38,39,41,61

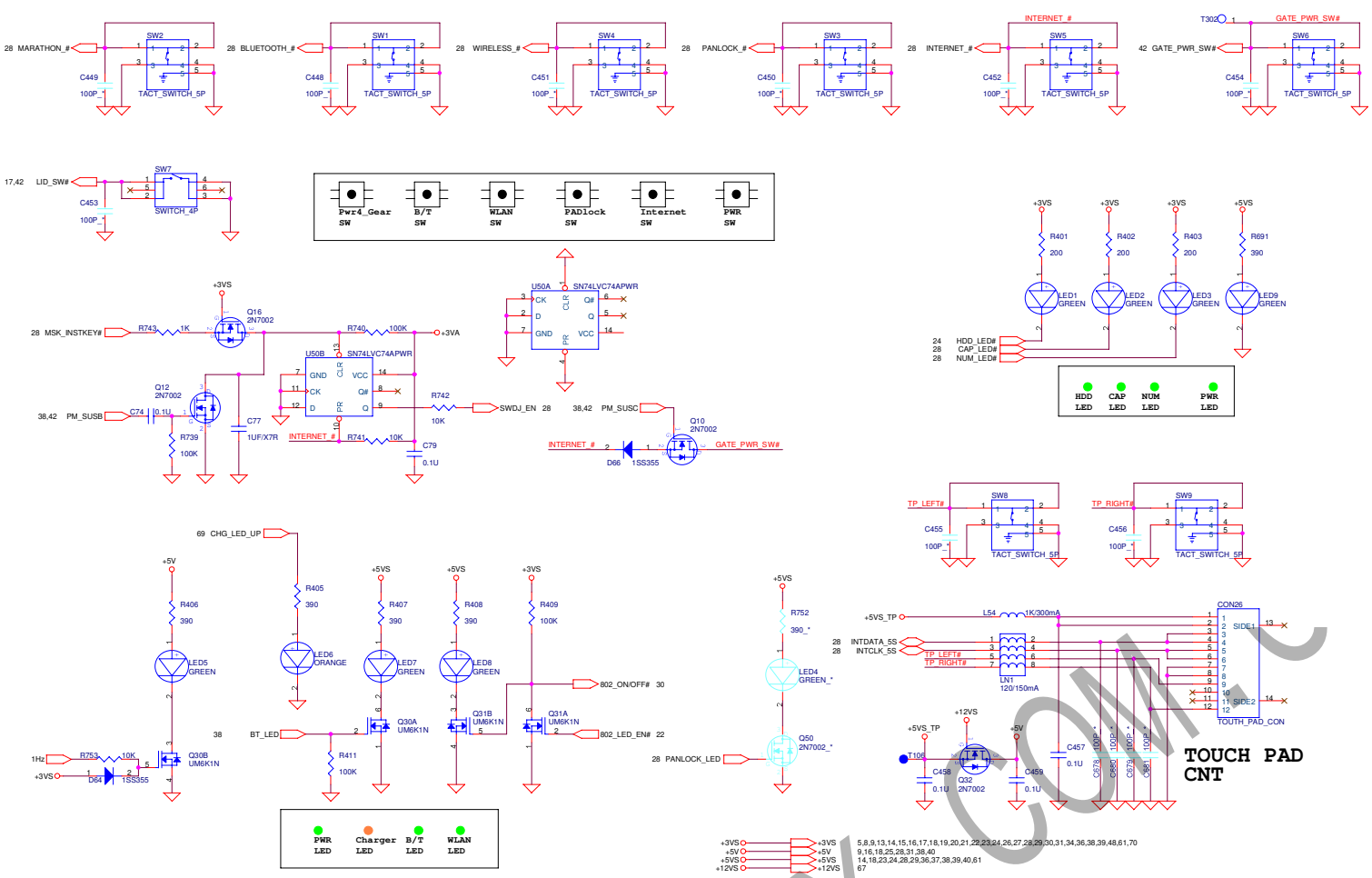


ACIN_CONN

ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: FAN_CTRL & ACIN	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 40 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

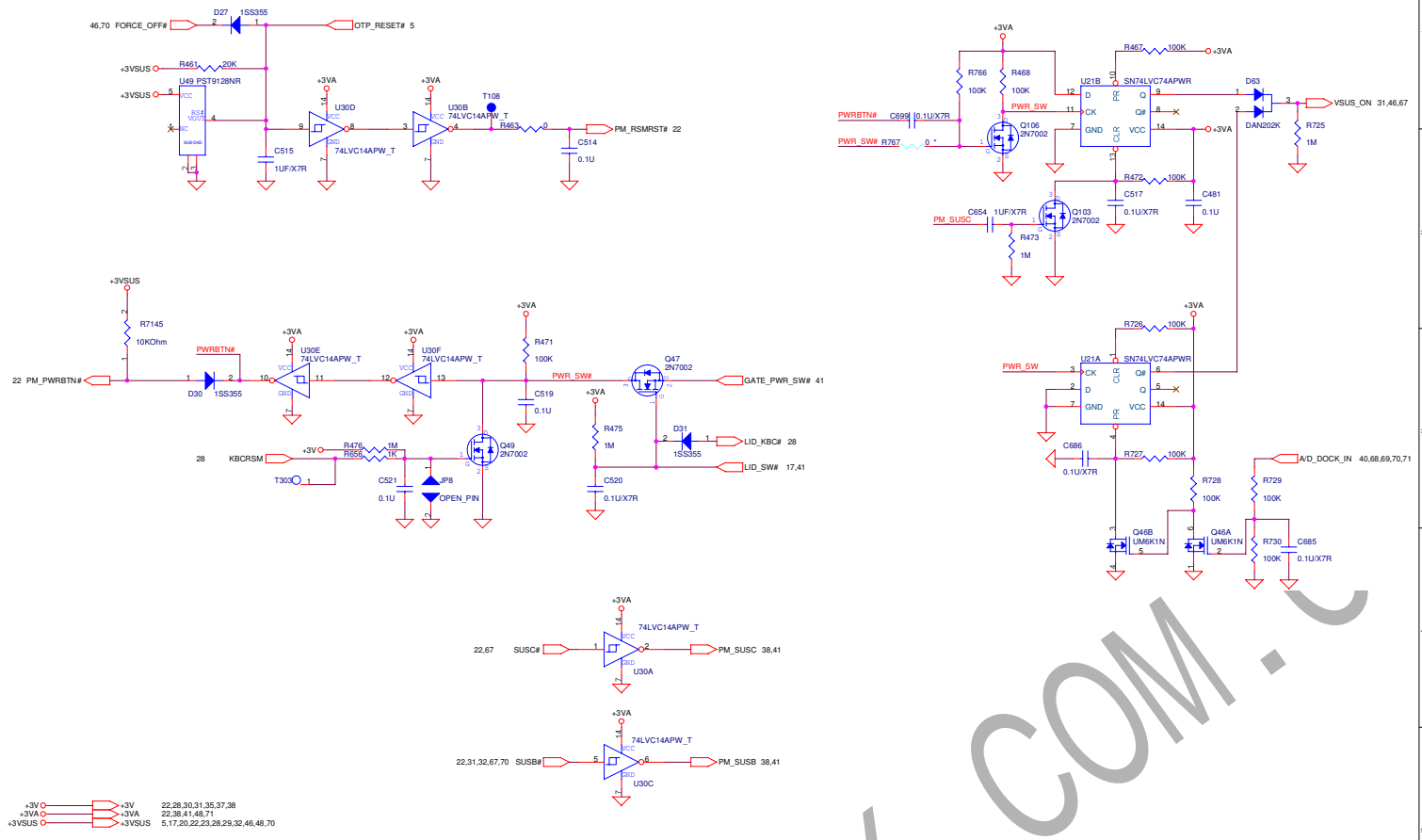
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ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SW & LED & TP	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 41	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 42 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

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Revision History

Power:

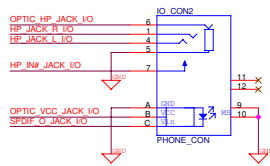
System:

Core Design:

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: HISTORY	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 43 OF 55		RELEASE DATE:	

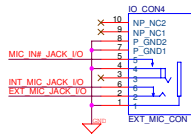
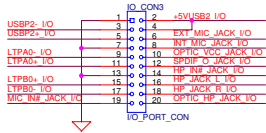
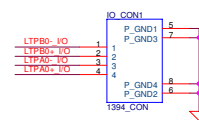
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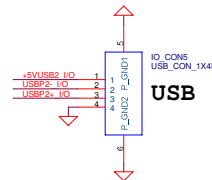


**LINE_OUT
SPDIF**

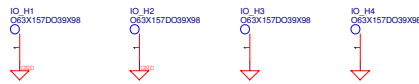
1394A



MIC



USB

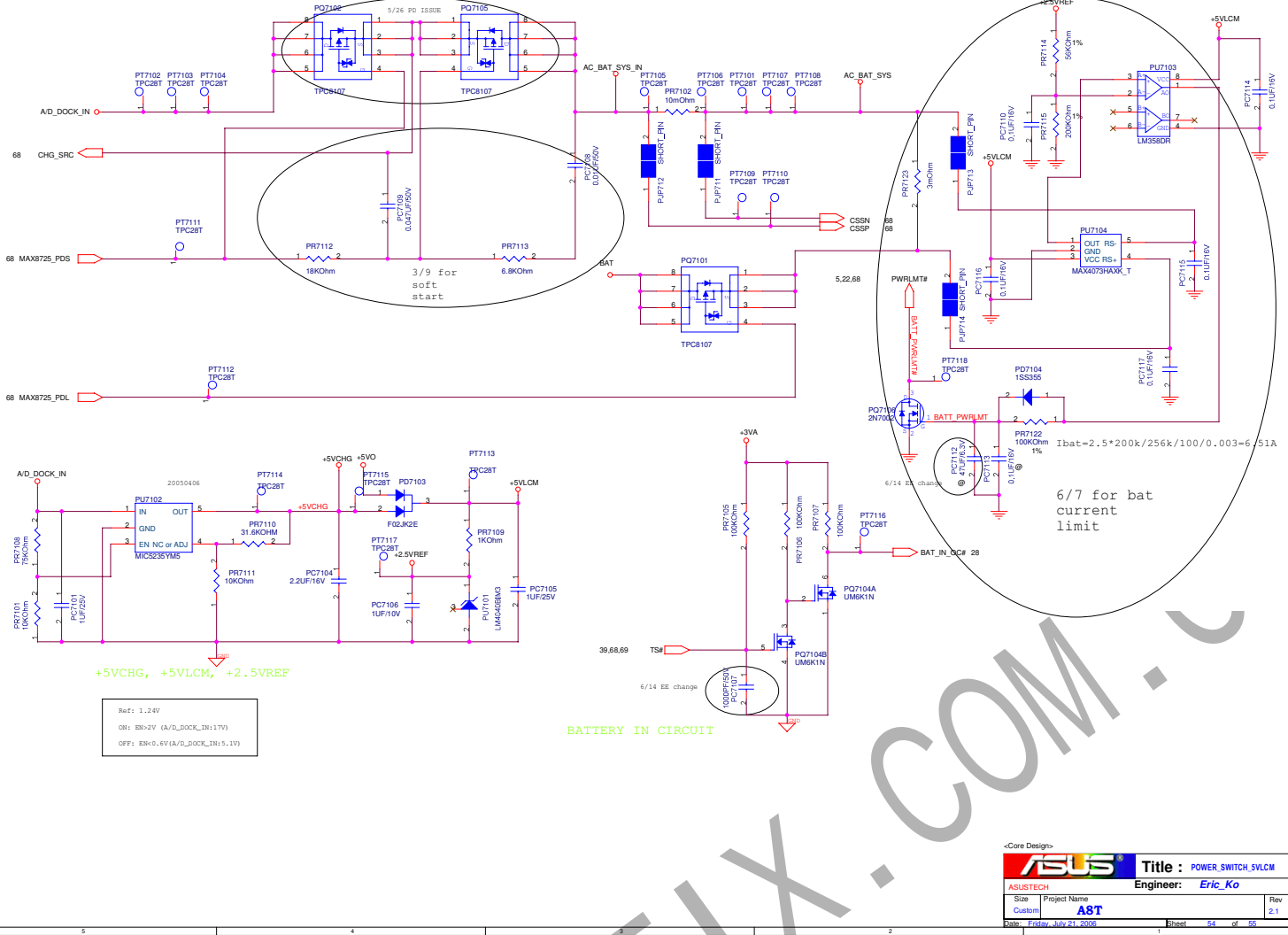


Core Designs

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: I/O PORT	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 44 OF 55		RELEASE DATE:	

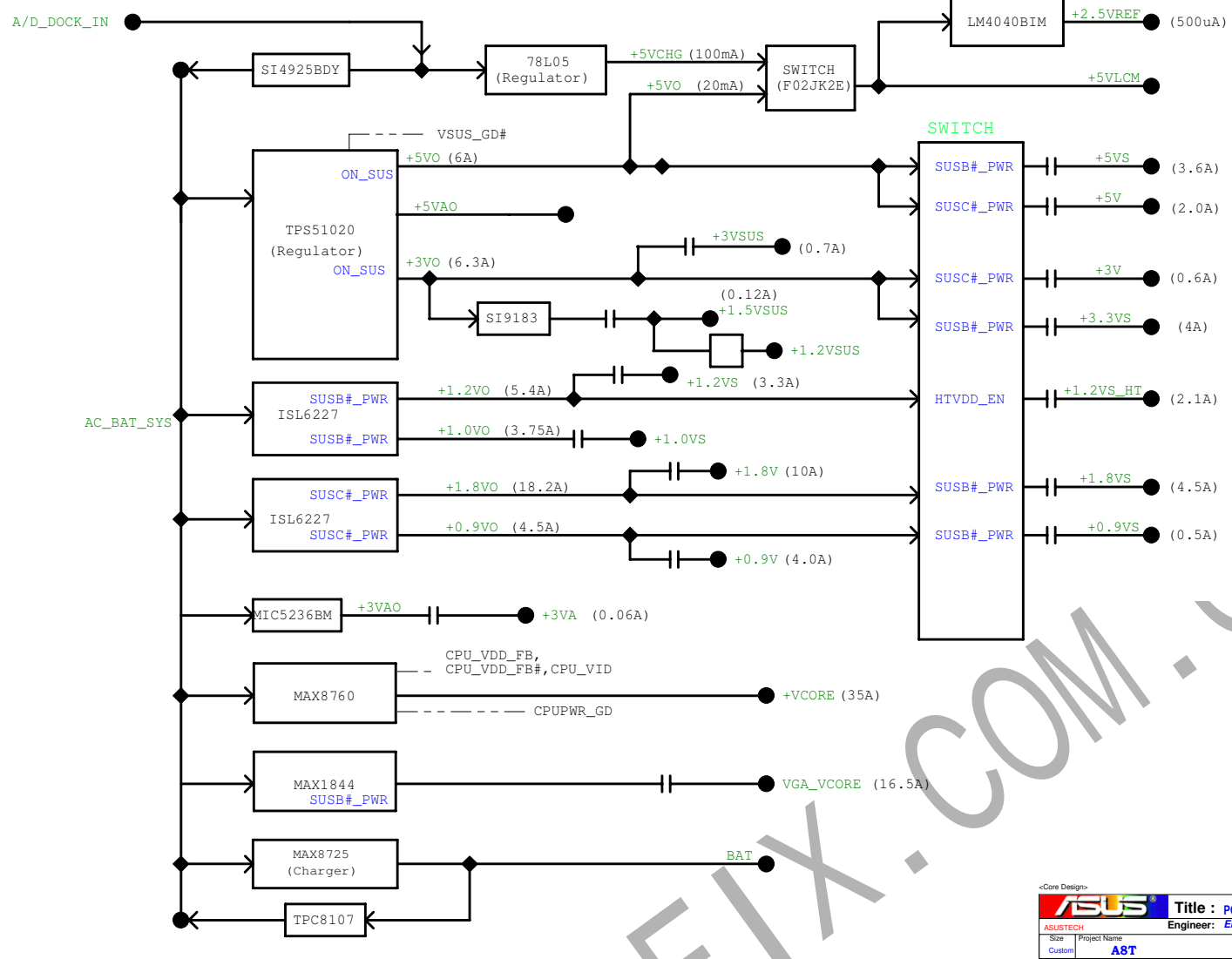
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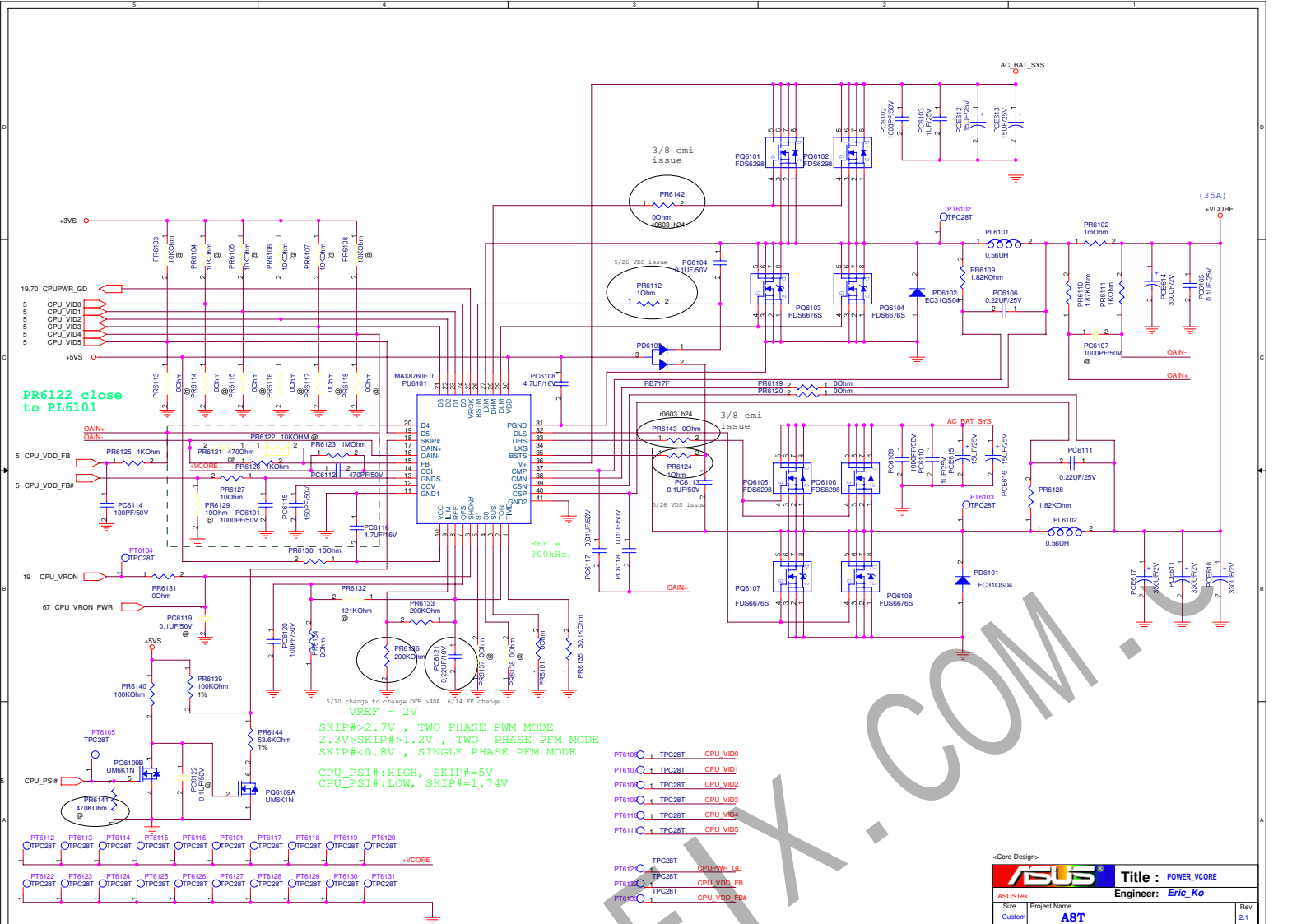


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		Title : POWER DIAGRAM	
ASUSTECH	Project Name	Engineer: Eric_Ko	Rev
Custom	ABT		2.1
Date: Friday, July 21, 2006		Sheet 66	of 66

<< Kennedy_Zhang >>

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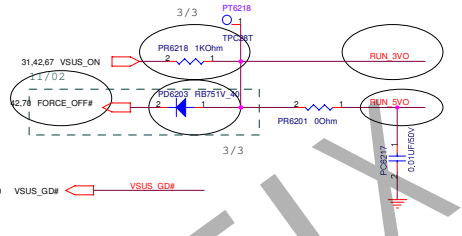
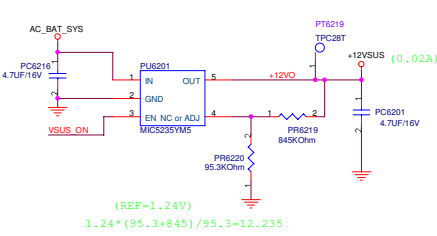
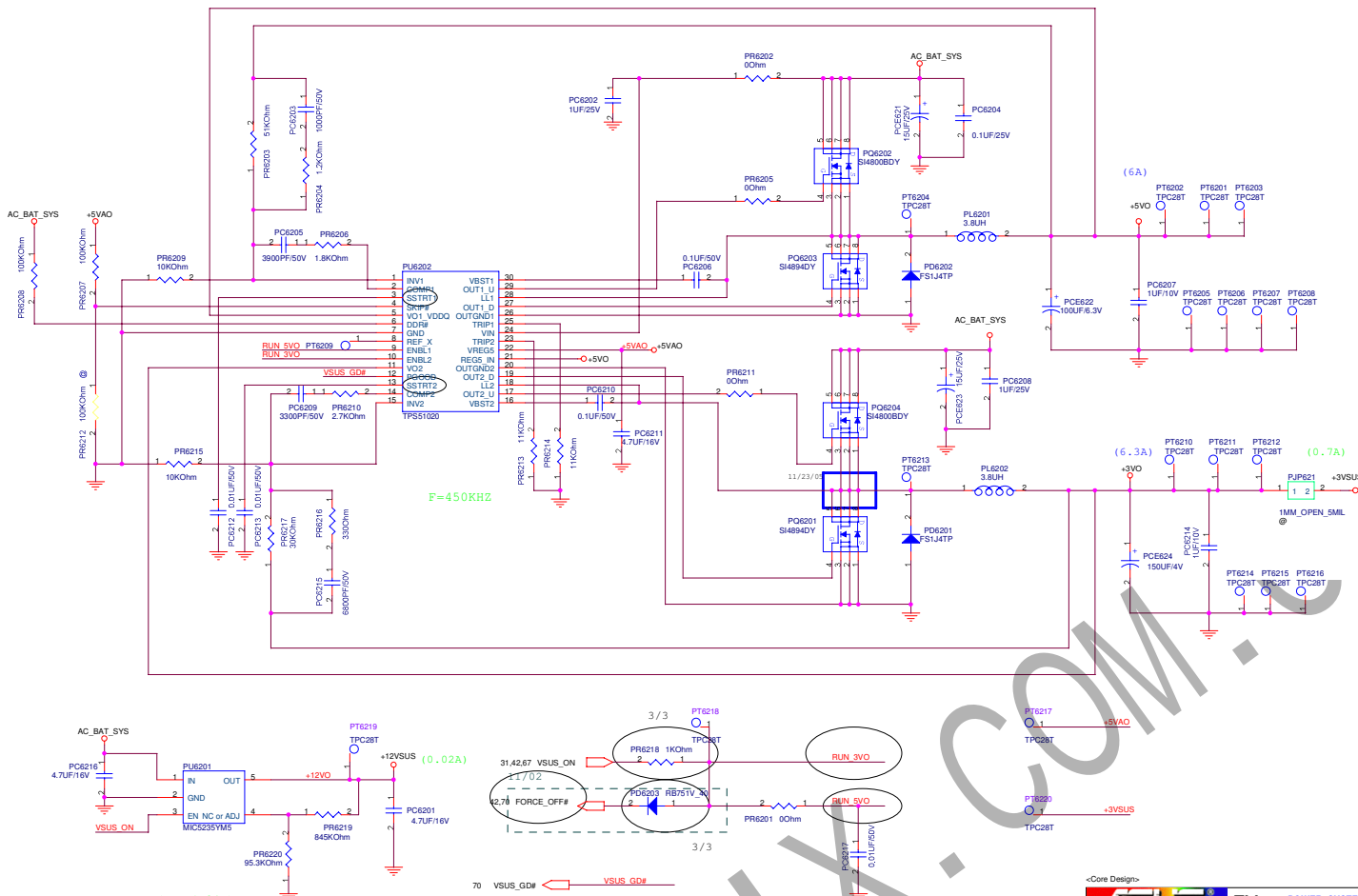


- PT6100 1 TPC28T CPU VID0
- PT6100 1 TPC28T CPU VID1
- PT6100 1 TPC28T CPU VID2
- PT6100 1 TPC28T CPU VID3
- PT6110 1 TPC28T CPU VID4
- PT6111 1 TPC28T CPU VID5

- PT612 1 TPC28T CPUVRRN_GD
- PT6102 1 TPC28T CPU_VDD_FB
- PT6105 1 TPC28T CPU_VDD_FWB

ASUSTek		Title: POWER_VCORE	
Size	Project Name	Engineer: Eric_Ko	Rev
Custom	ABT		2.1
Date: Friday, July 21, 2006	Sheet	61	of 66

<< Kennedy_Zhang >>

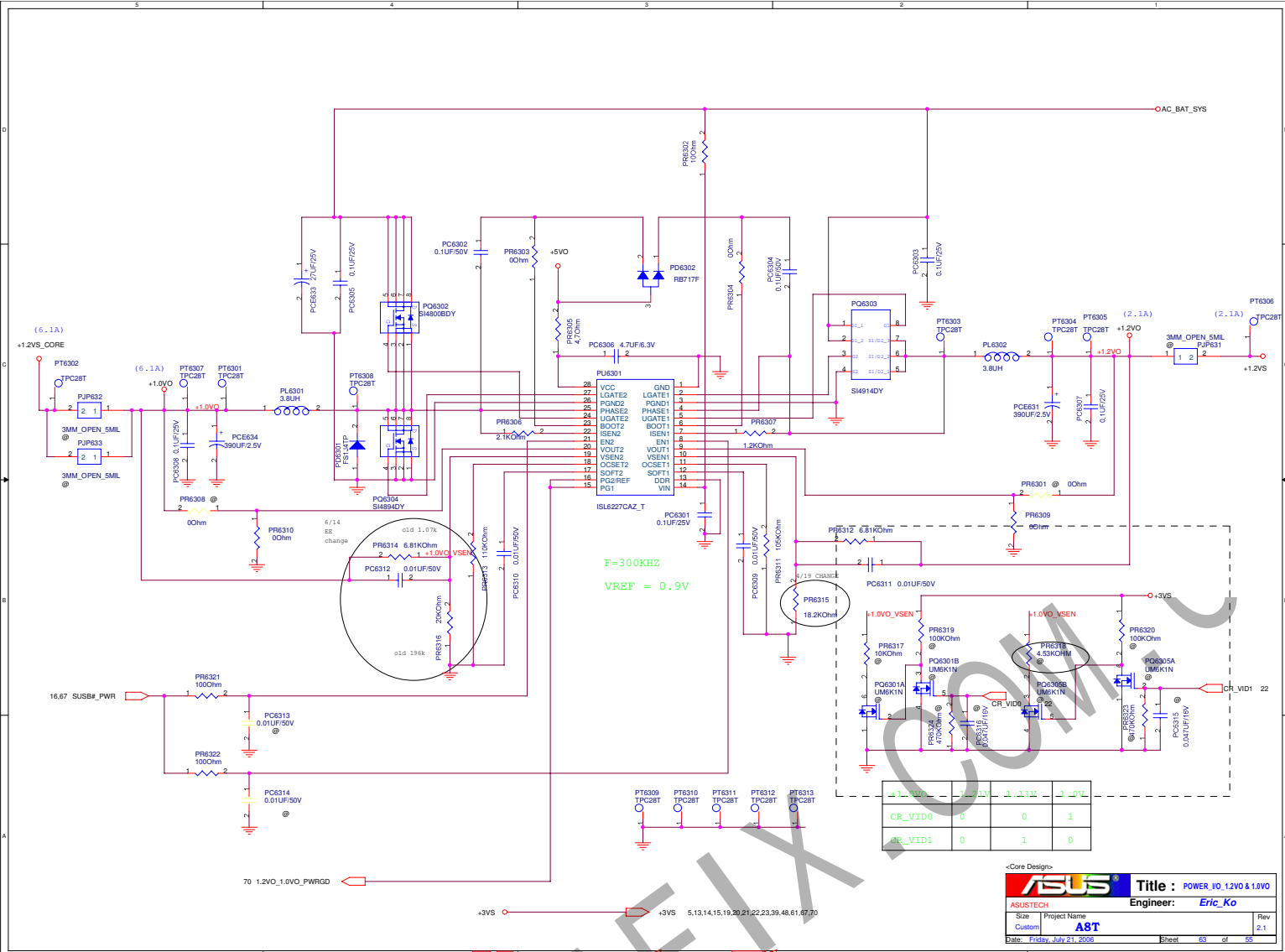


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ASUS		Title : POWER_SYSTEM
ASUSTECH	Project Name	Engineer: Eric_Ko
Size	Custom	ABT
Date: Friday, July 21, 2006	Sheet	62 of 95

<< Kennedy_Zhang >>

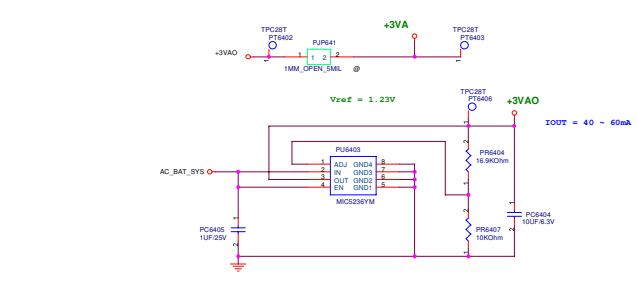
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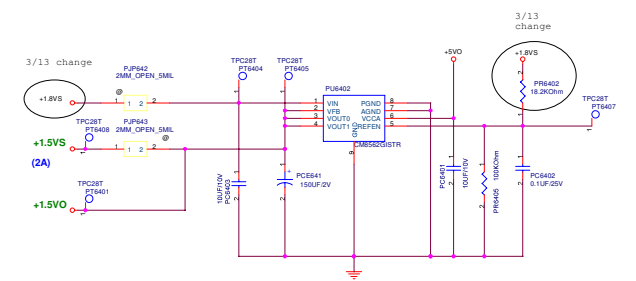
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ASUS Title: POWER_IO_1.2V0 & 1.0V0
 ASUSTECH Engineer: Eric_Ko
 Size: Custom Project Name: AST Rev: 2.1
 Date: Friday, July 21, 2006 Sheet: 63 of 69

<< Kennedy_Zhang >>

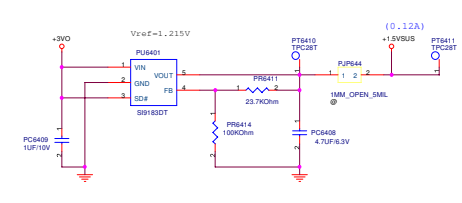
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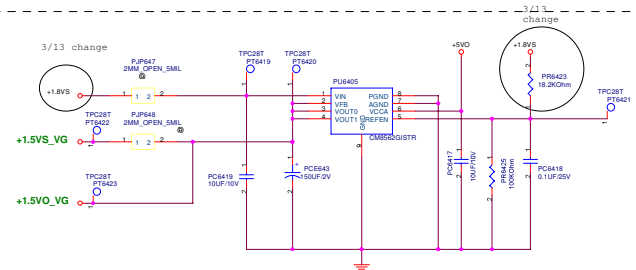
+3VA



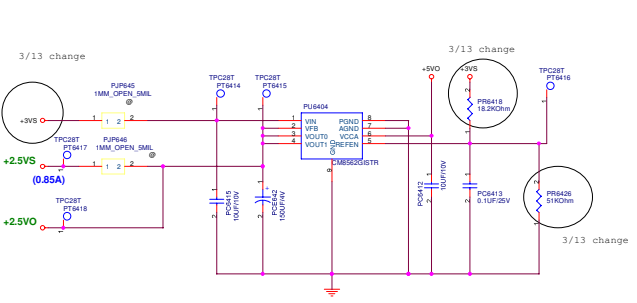
+1.5VS



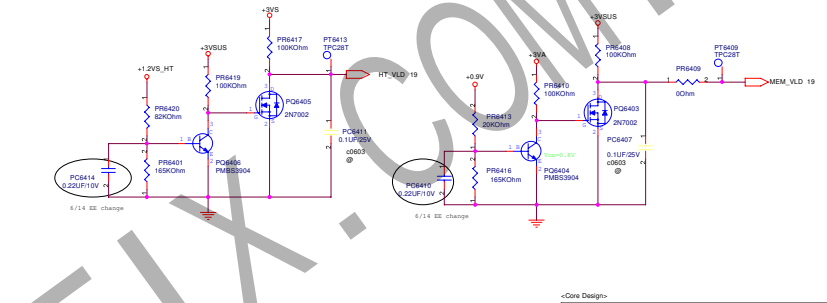
+1.5VSUS



+1.5VS_VG



+2.5VS

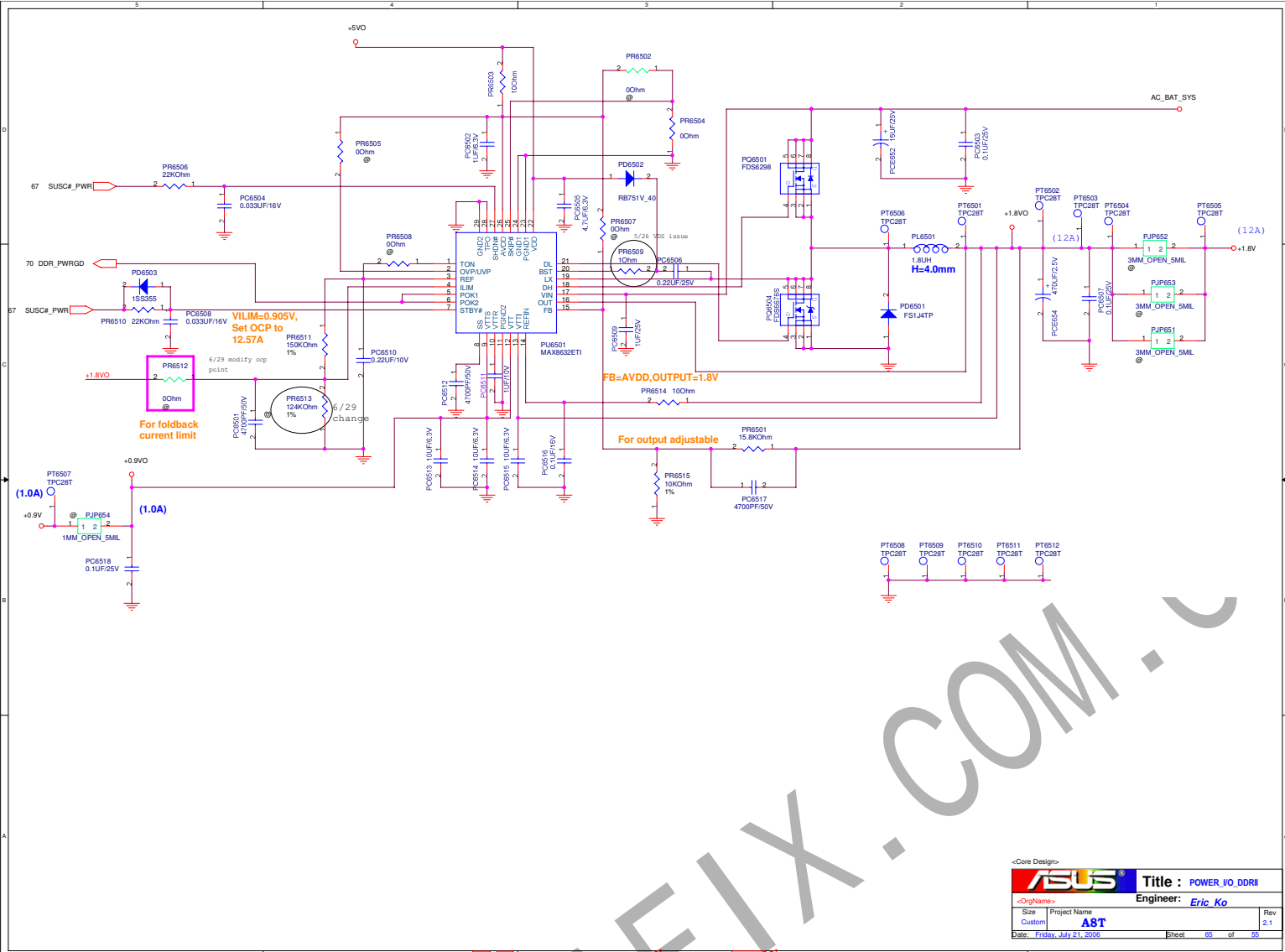


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ASUS		Title : POWER_IO_LDO	
ASUSTECH	Project Name	Engineer: Eric_Ko	
Rev	0	0.1UF/25V	2/1
Rev	1	0.1UF/25V	2/1

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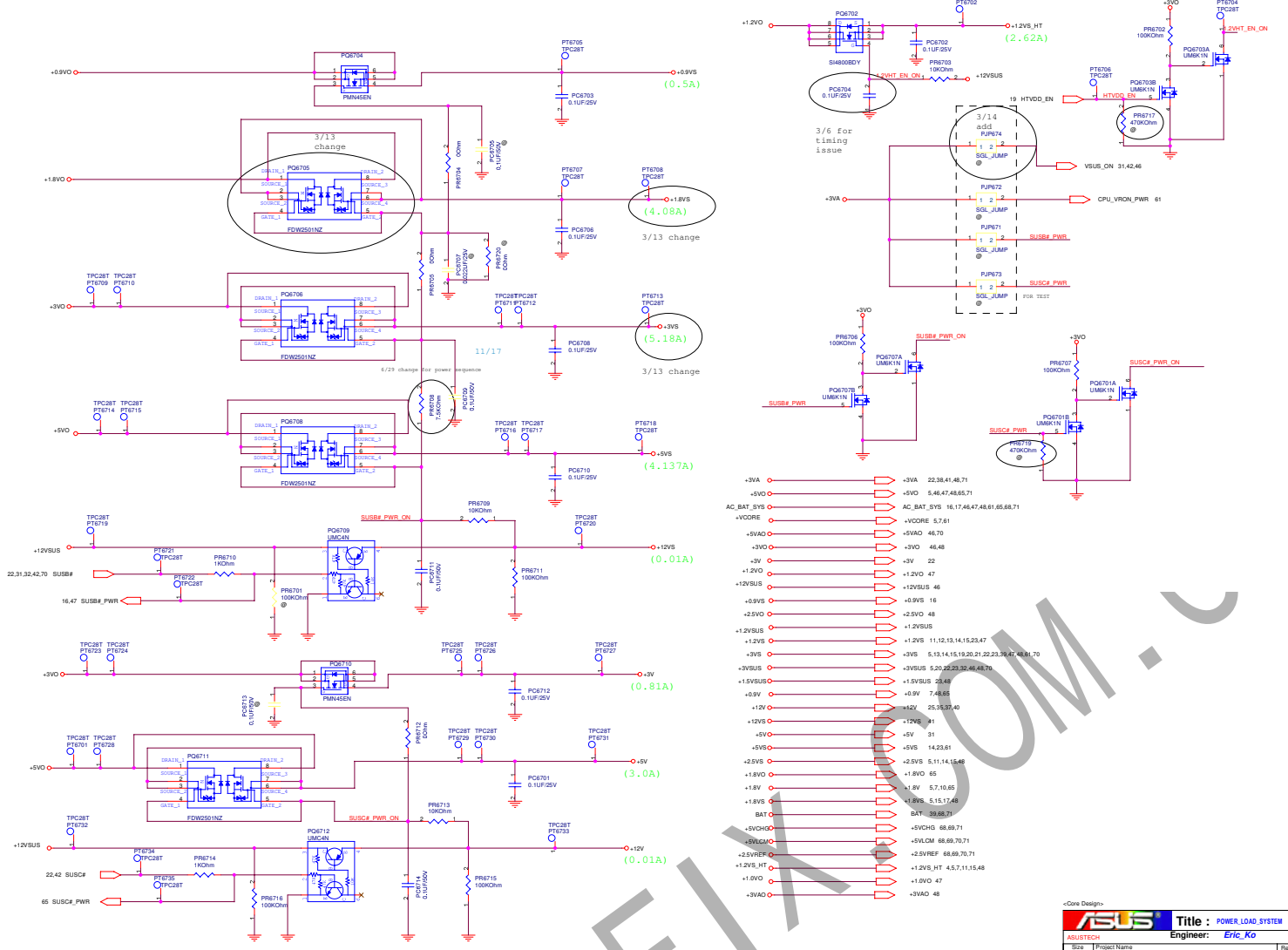


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ASUS		Title : POWER_IO_DDR1
Engineer: Eric Ko		
<OrigName>	Project Name	Rev
Size	Custom	ABT
Date: Friday, July 21, 2006	Sheet	65 of 65

<< Kennedy_Zhang >>

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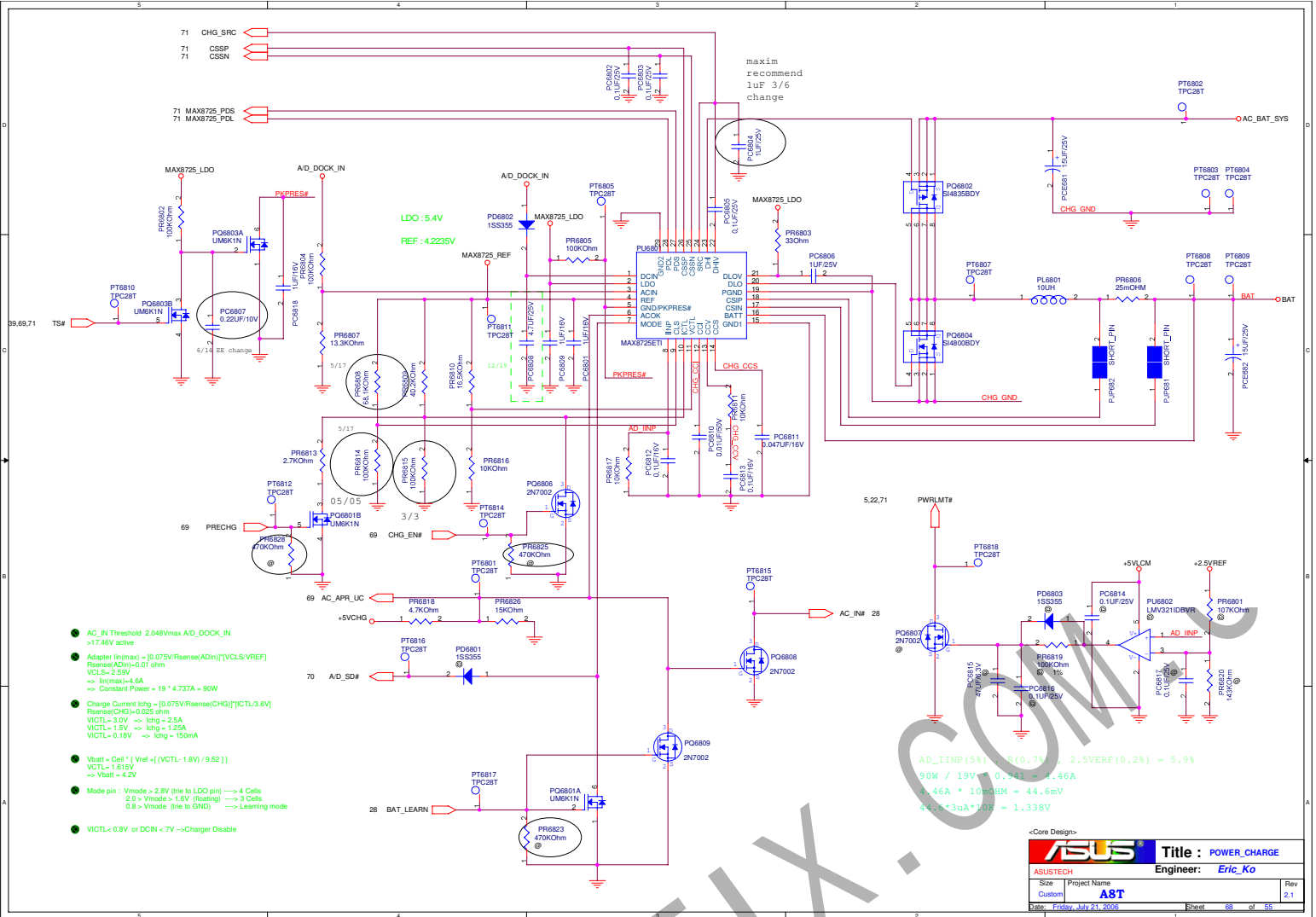


+3VA	22.38,41,48,71
+5V0	5.46,47,48,65,71
AC_BAT_SYS	16,17,46,47,48,61,65,68,71
+VDDREF	5,761
+3V0	46,70
+5V0	46,48
+3V	22
+12V0	47
+12VSUS	48
+0.9V	15
+2.5V0	48
+1.2VSUS	11,12,13,14,15,23,47
+3V	5,13,14,15,16,20,21,22,23,30,47,48,64,70
+3VSUS	5,20,22,23,32,46,48,70
+1.5VSUS	28,49
+0.9V	7,48,65
+12V	25,35,37,40
+12V#	41
+5V	31
+5V	14,23,61
+2.5V	5,11,14,15,48
+1.8V0	65
+1.8V	5,7,10,65
+1.8V#	5,15,17,49
BAT#	39,68,71
+5VCHG0	68,69,71
+5VLC0	68,69,70,71
+2.5VREF	68,69,70,71
+1.2V#_HT	4,5,7,11,15,48
+1.2V0	47
+3VAD	48

ASUS		Title: POWER_LOAD_SYSTEM
ASUSTeK	Project Name:	Engineer: Eric_Ko
Custom	ASBT	Rev: 2.1
Date: Friday, July 21, 2006	EScan: 87	of 88

« Kennedy_Zhang »

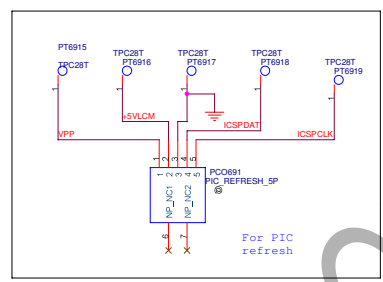
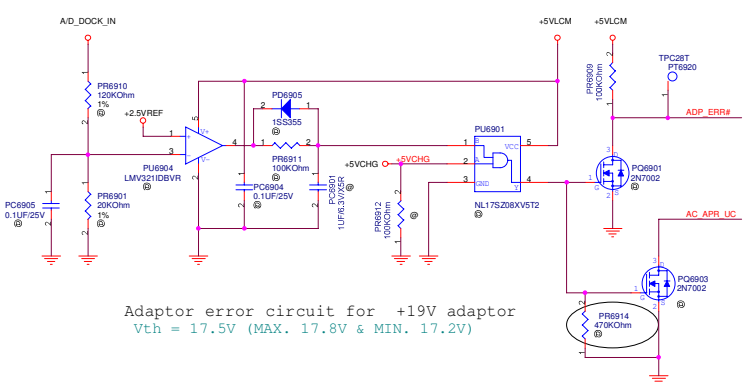
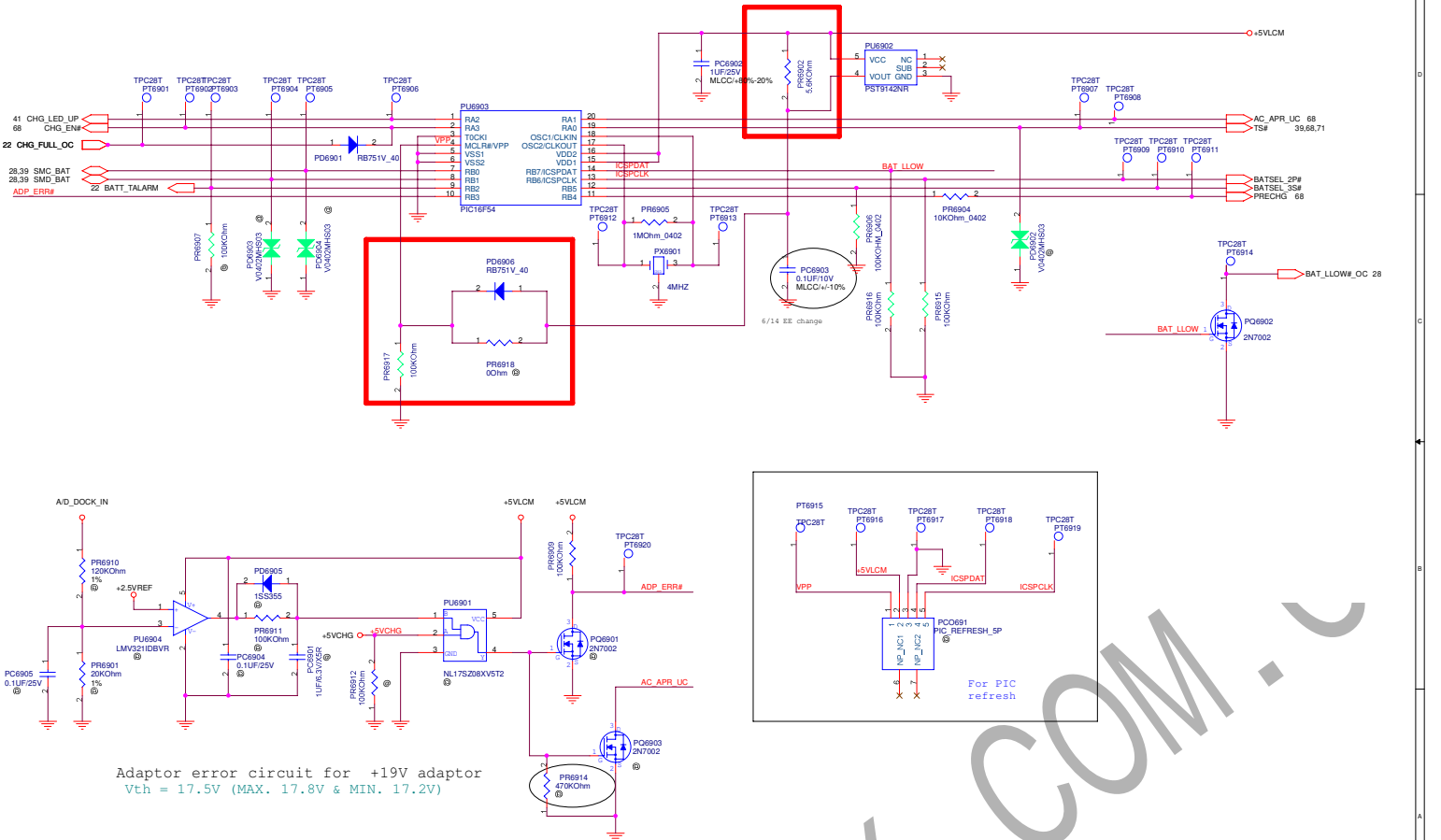
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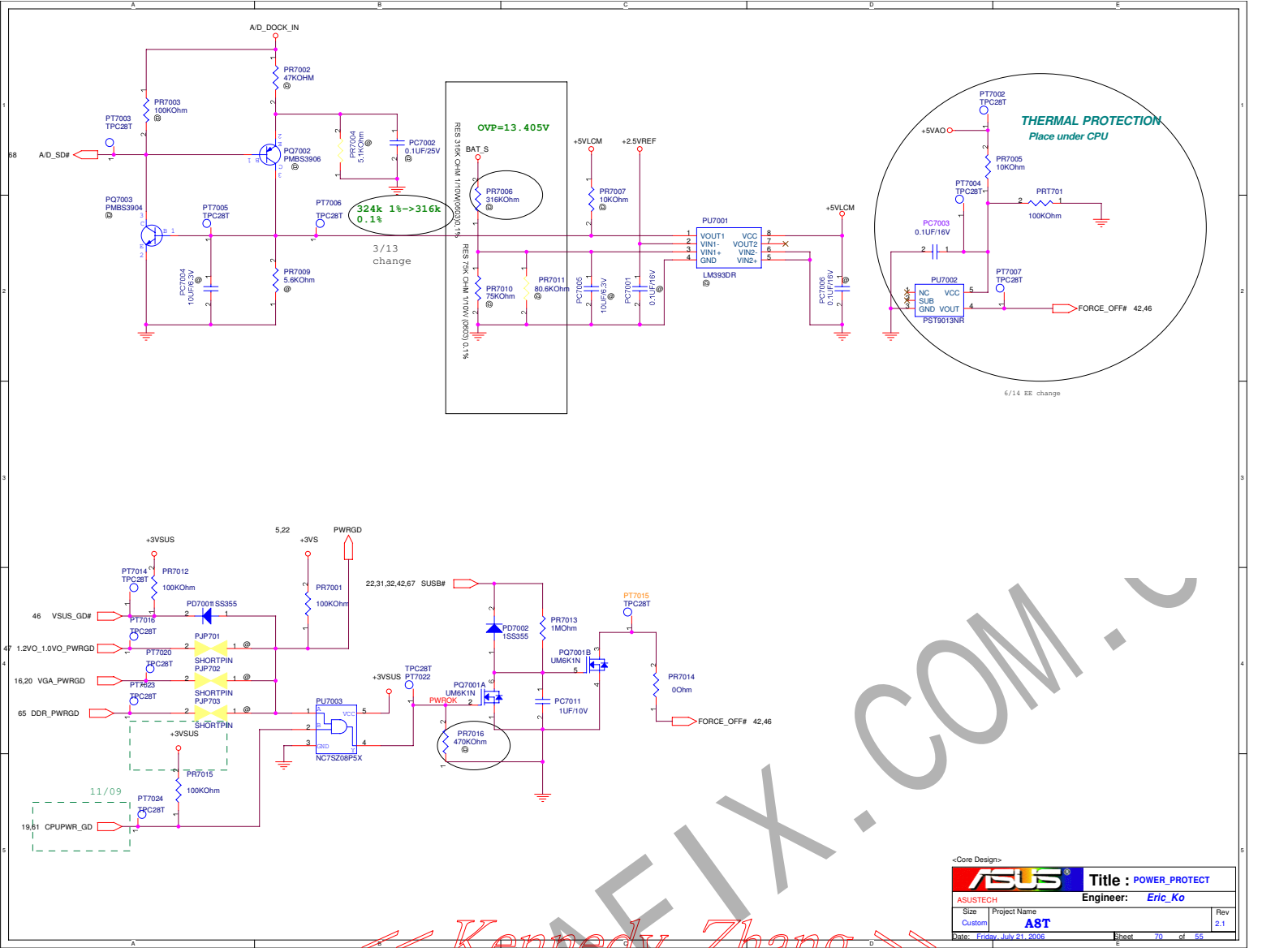


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		Title : POWER PIC	
<OrigName>		Engineer: Eric_Ko	
Size	Project Name		Rev
Custom	ABT		2.1
Date: Friday, July 23, 2006	Sheet	69	of 95

<< Kennedy_Zhang >>

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-Core Design-

ASUS		Title : POWER_PROTECT
ASUSTECH	Project Name	Engineer: Eric_Ko
Size	Custom	Rev 2.1
Date: Friday, July 21, 2006	Sheet 70	of 55