A8T/M SCHEMATIC R2.1

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5	AMD S1 CPU--CNTL
6	AMD S1 CPU--DDR2
7	AMD S1 CPU--PWR/GND
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9	DDR2 SO-DIMM_1
10	DDR2 ADDRESS TERMINATION
11	C51M--HT TO CPU
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13	C51M--PCI-E
14	C51M--CRT & LVDS
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18	CRT & TV_OUT
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20	MCP51--PCI
21	MCP51--IDE
22	MCP51--USB & HDA & GPIO
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25	USB PORTS
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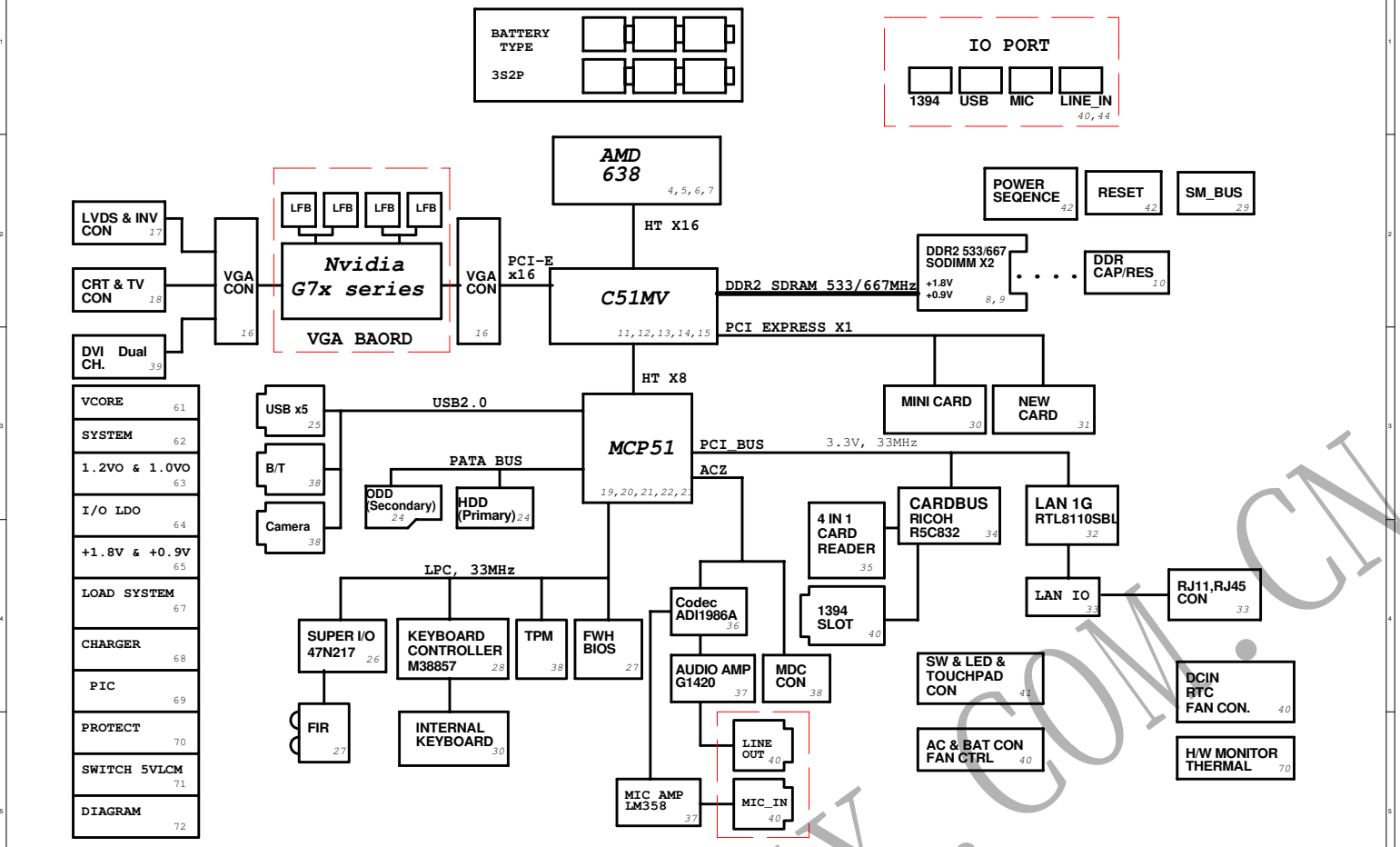
<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: PAGE REF.	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 1 OF 55		RELEASE DATE :	Albert Su

A8T/M AMD S1/C51MV BLOCK DIAGRAM



<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
	2.1	SHEET 2 OF 55		RELEASE DATE :	

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010001x (A2h)

MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWRLMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CR_VID2)	+3VSUS
GPIO_[11:16]		(CPU_VID[0:5])	+3VSUS
GPIO_17		(LFD#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDIN0_AUD	+3VSUS
GPIO_23		ACZ_SDIN1_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	SIO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(RI#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

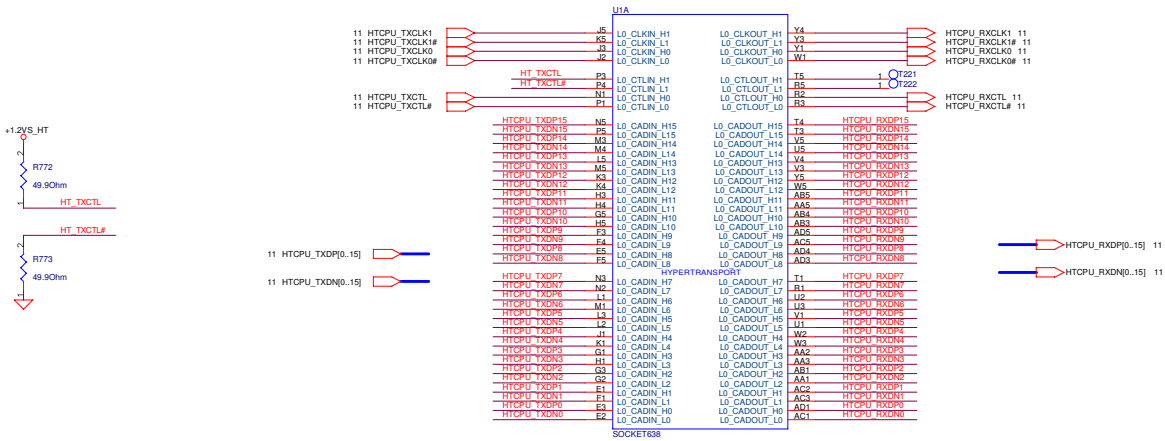
MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERM#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_F)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SCHEMATICS REF.	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 3 OF 55		RELEASE DATE :	



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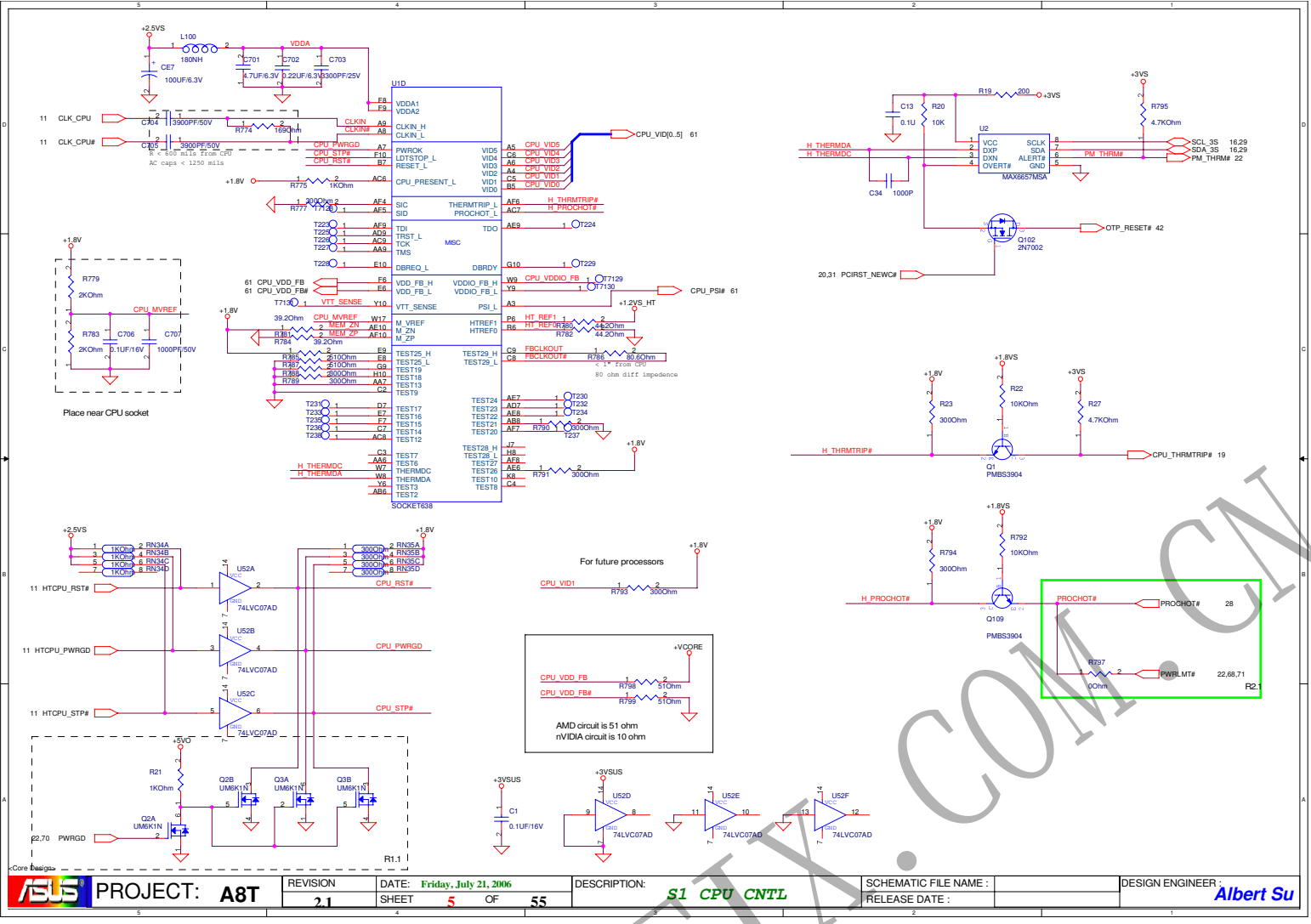
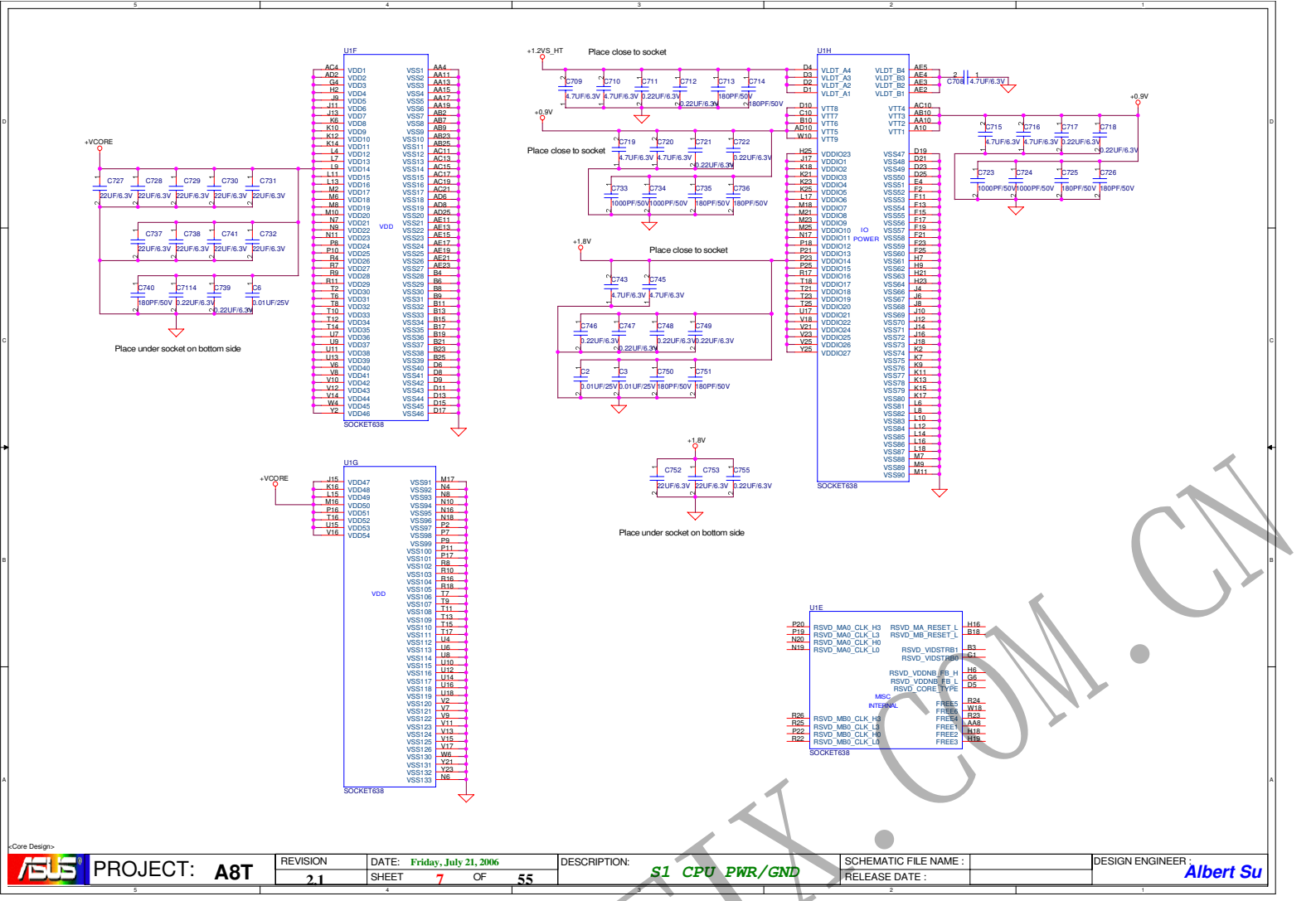
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU HT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 4 OF 55		RELEASE DATE :	



PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU CNTL	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 5 OF 55		RELEASE DATE :		

<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU MEM	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 6 OF 55		RELEASE DATE :	Albert Su



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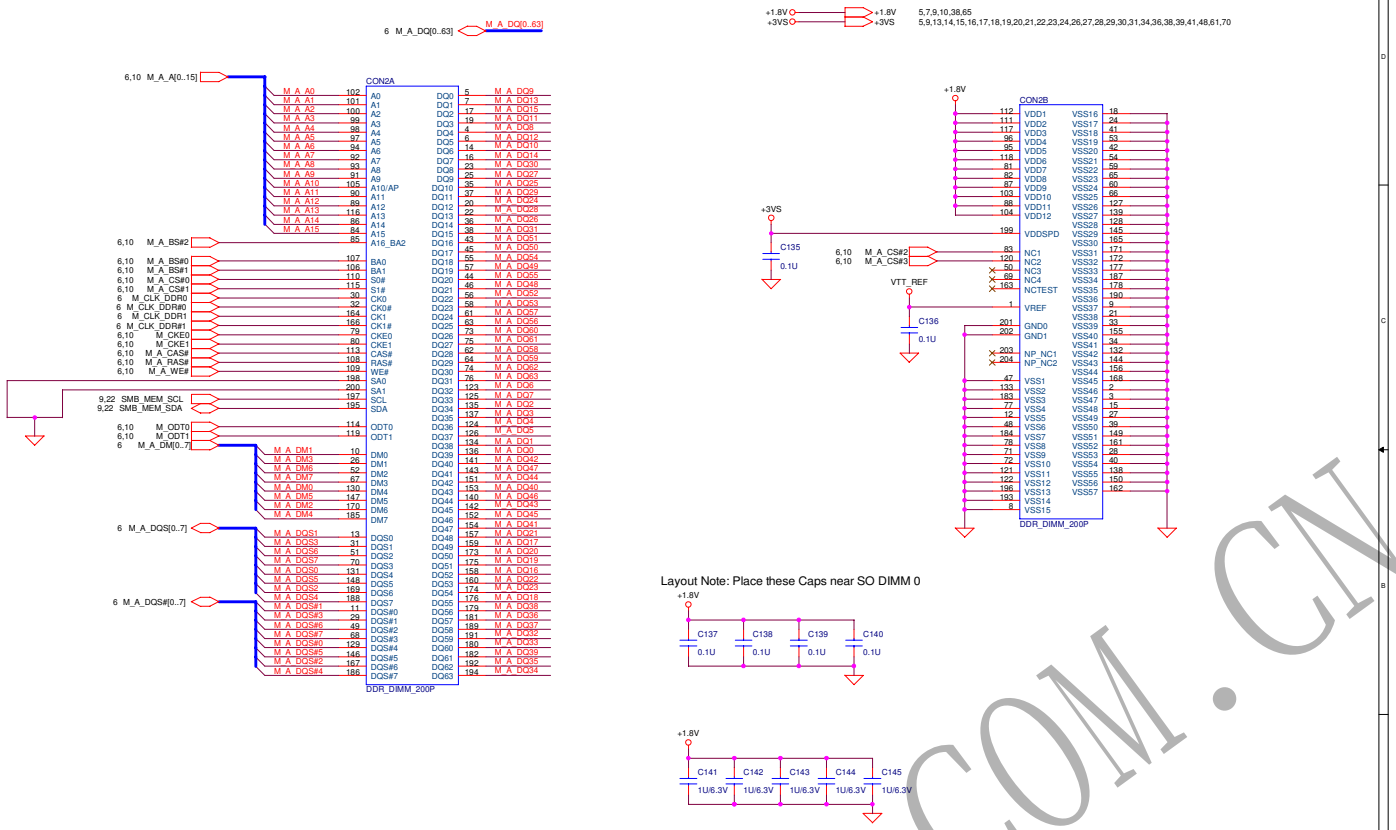
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 7 OF 55	DESCRIPTION: S1 CPU PWR/GND	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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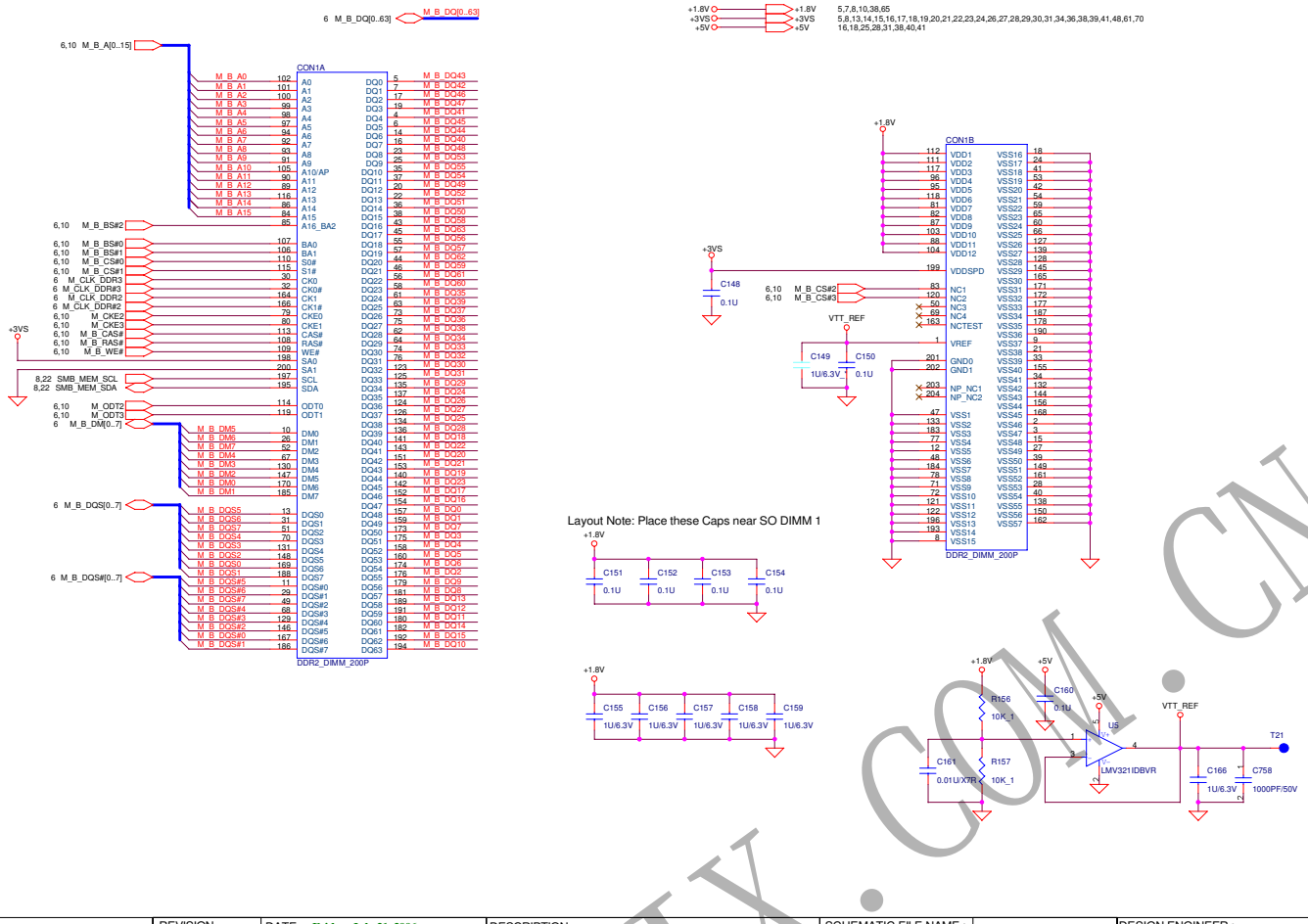
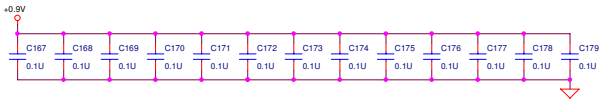
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 8 OF 55	DESCRIPTION: DDR2 SO-DIMM0	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

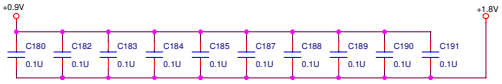


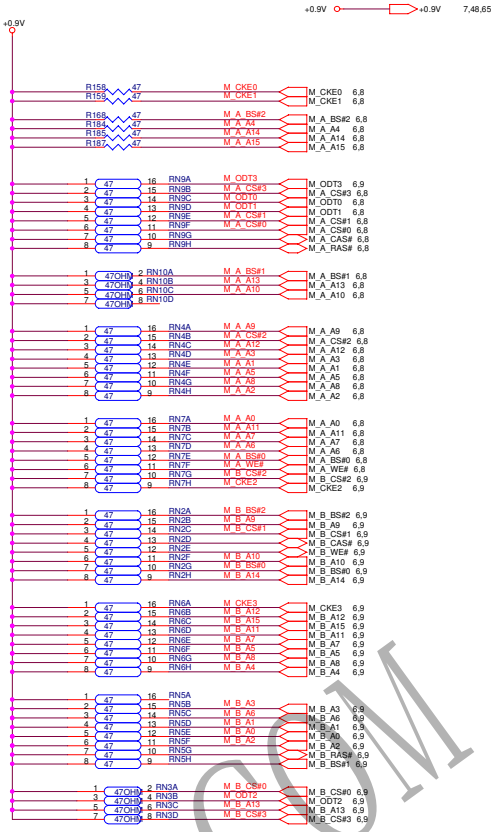
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 9 OF 55	DESCRIPTION: DDR2 SO-DIMM1	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V





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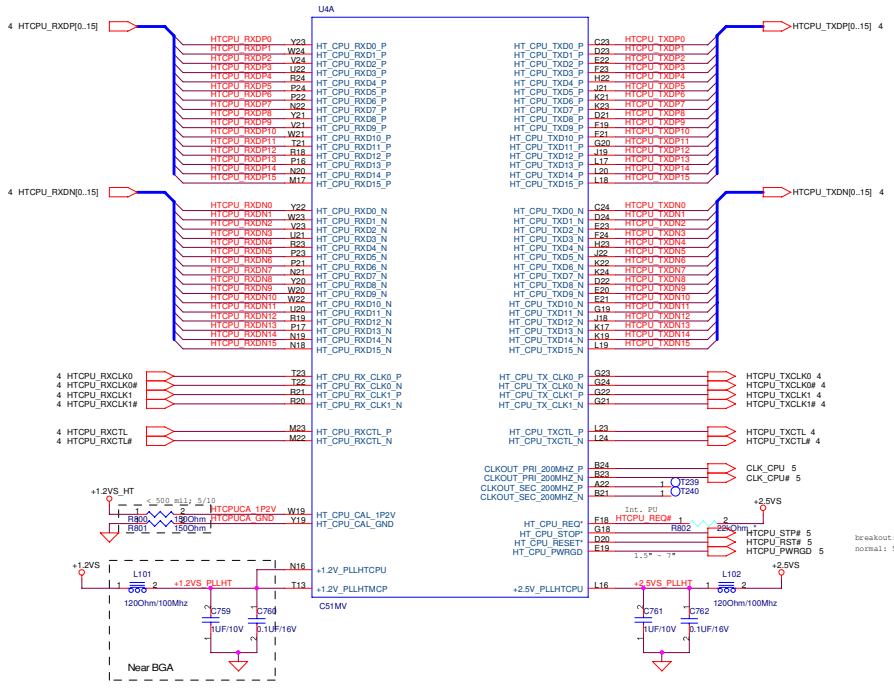
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 10 OF 55	DDR2 ADDRESS TERMINATION	RELEASE DATE :	Albert Su



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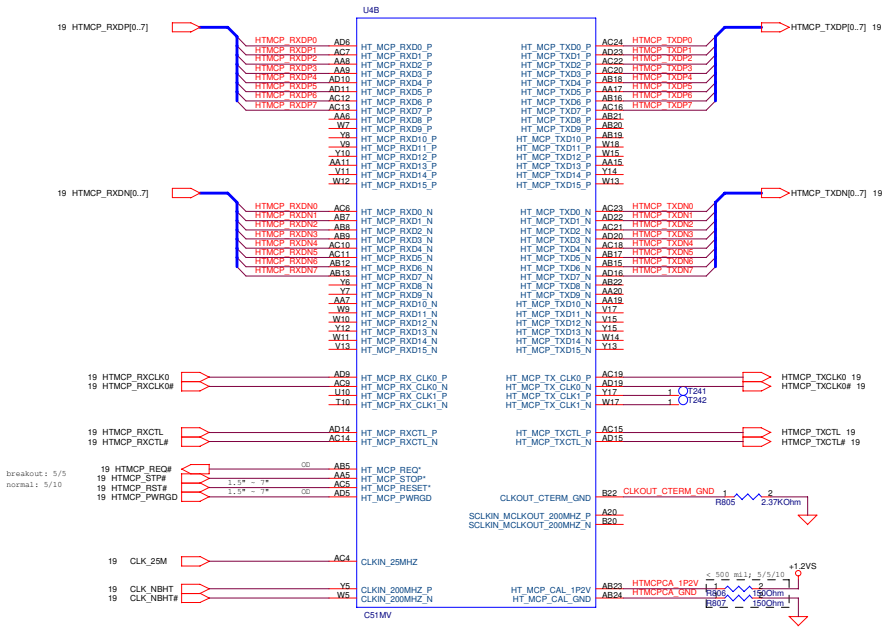
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 11 OF 55	DESCRIPTION: C51M_HT	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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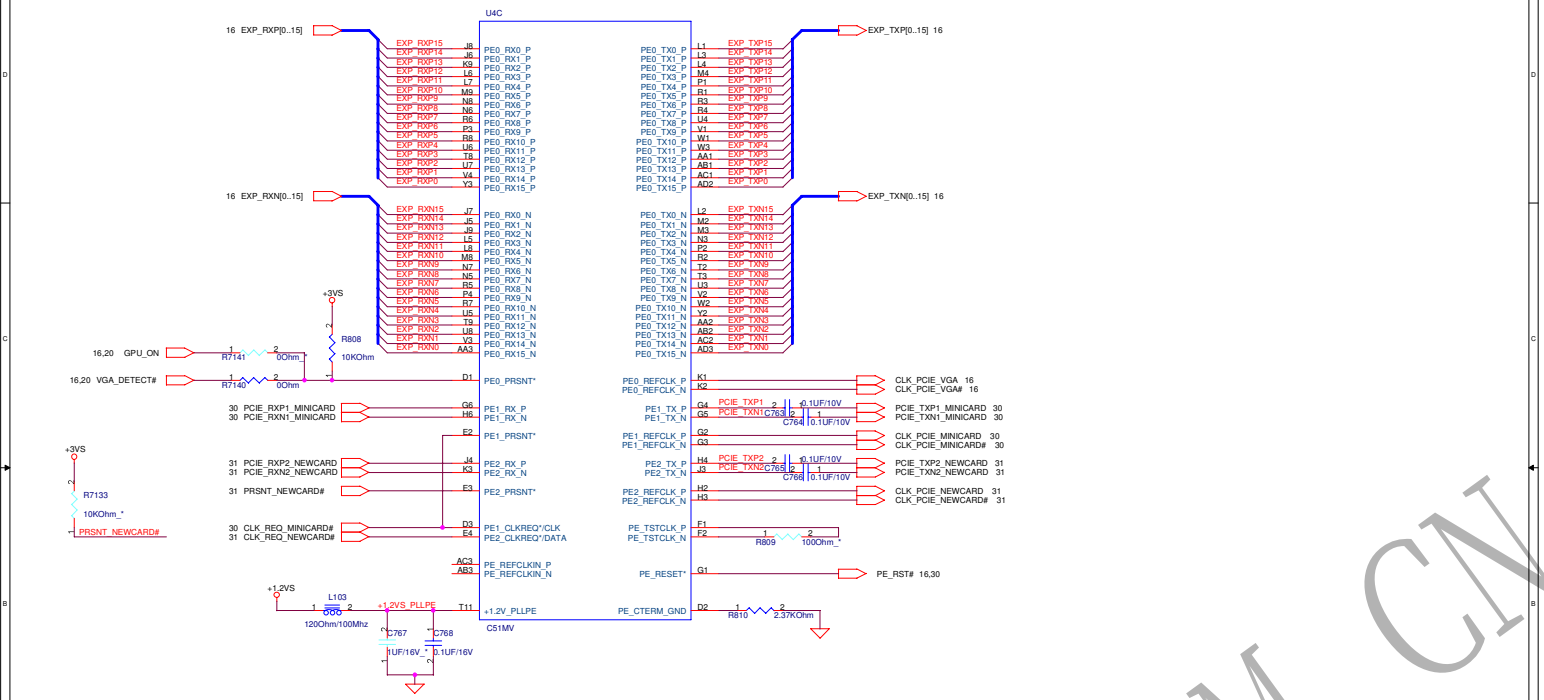
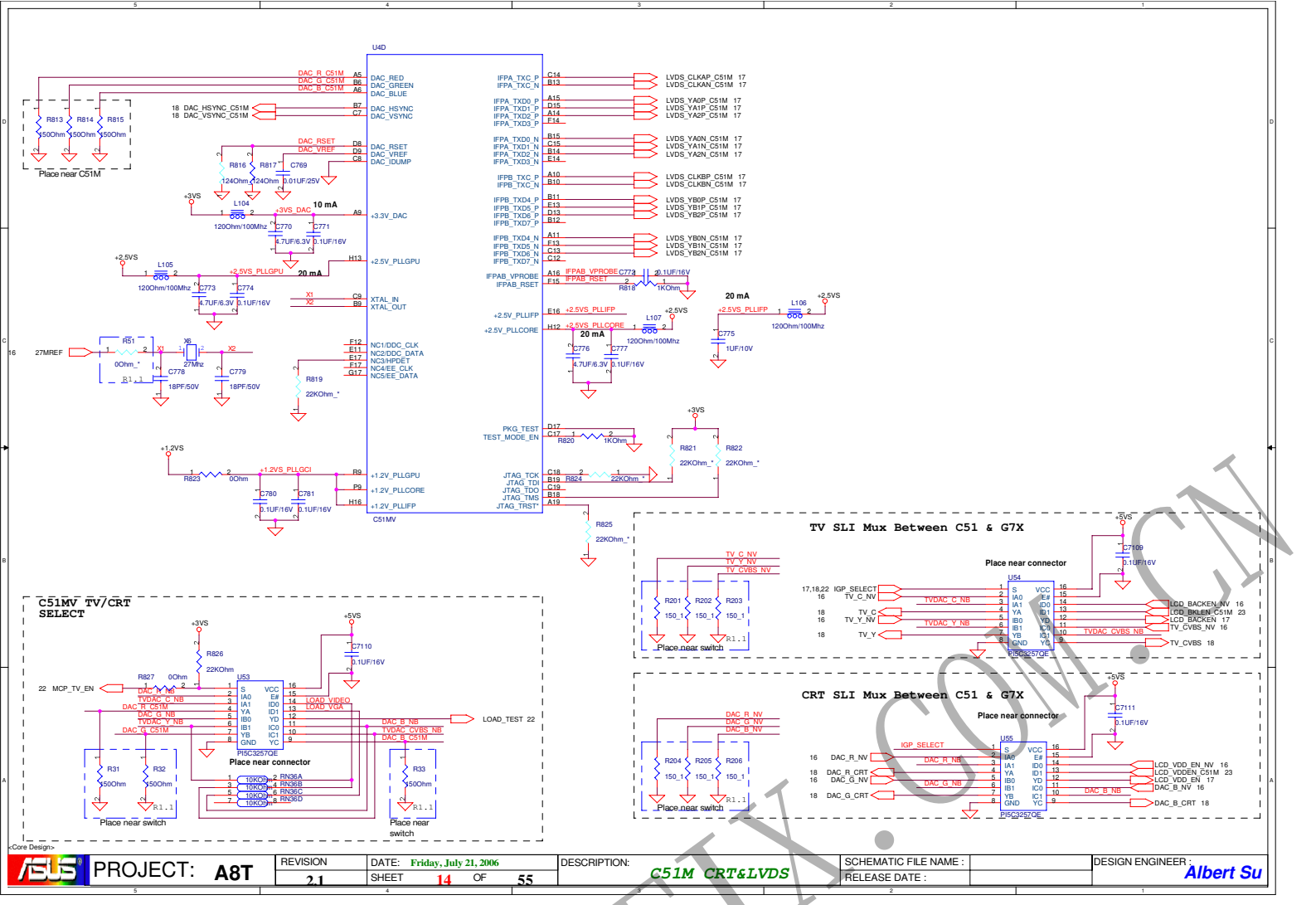
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT TO MCP	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
	2.1	SHEET 12 OF 55		RELEASE DATE :	

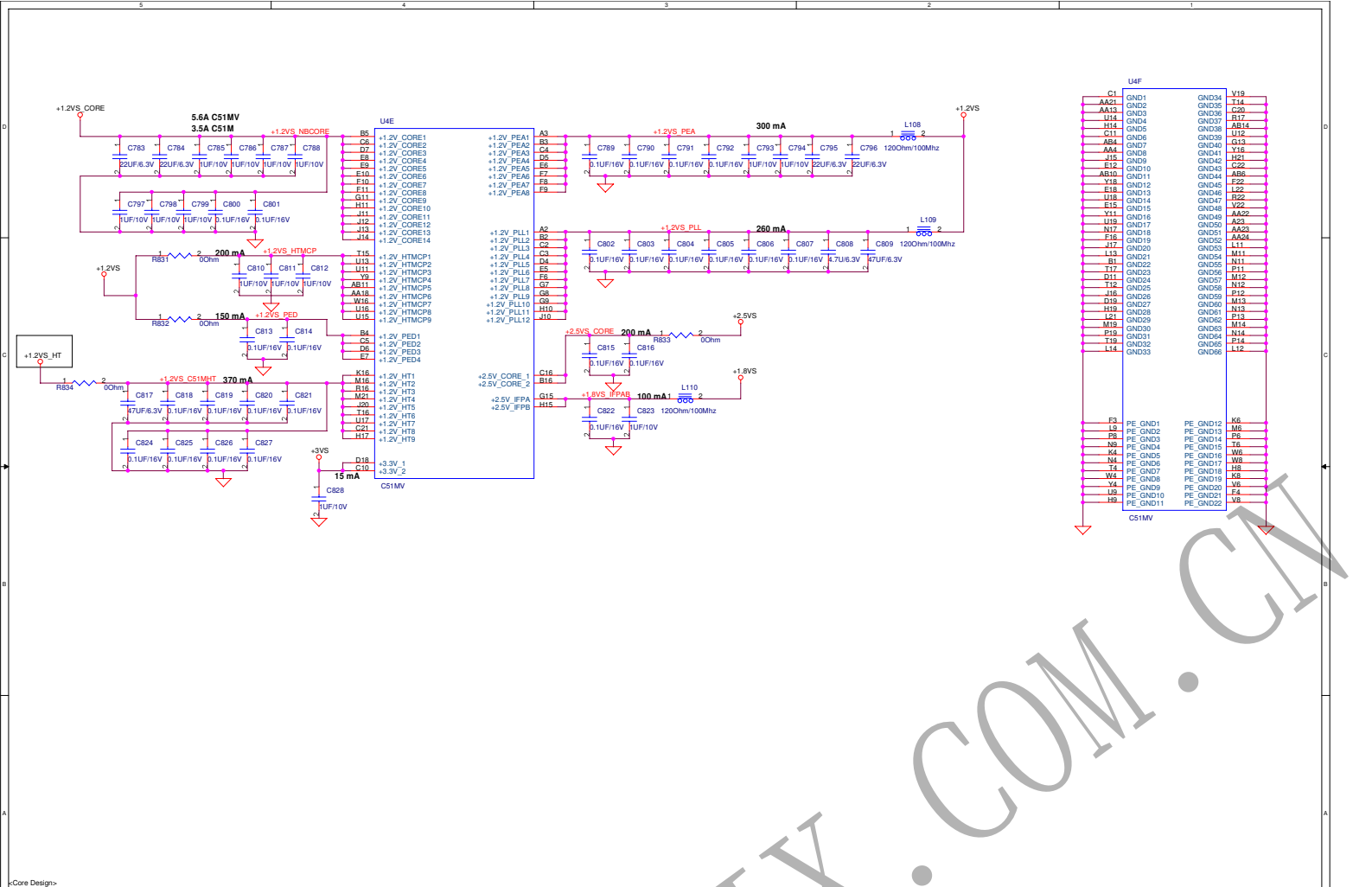


<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 13 OF 55	DESCRIPTION: C51M PCI-E	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 14 OF 55	DESCRIPTION: C51M CRT&LVDS	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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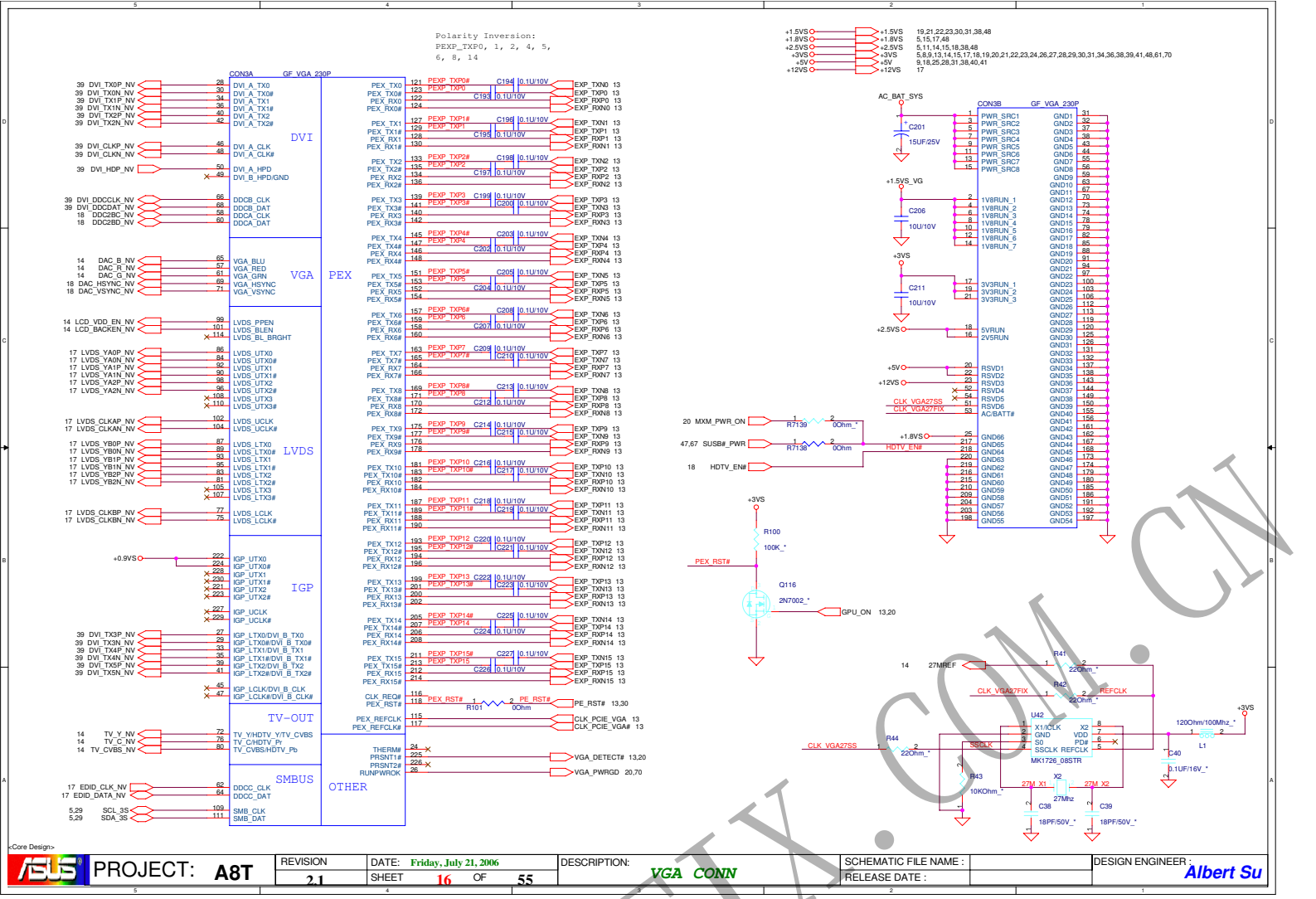
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 15 OF 55	DESCRIPTION: C51M PWR/GND	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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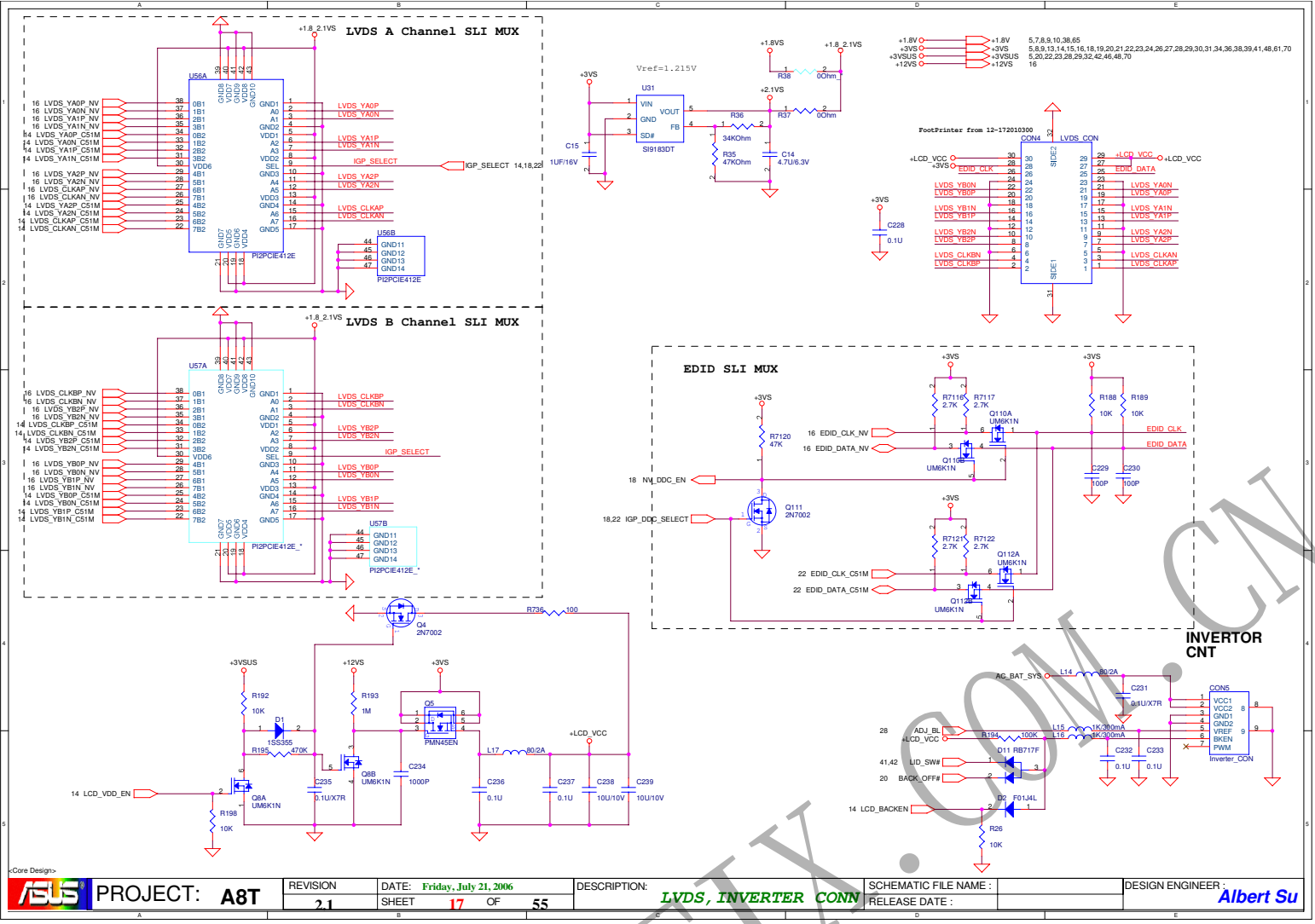
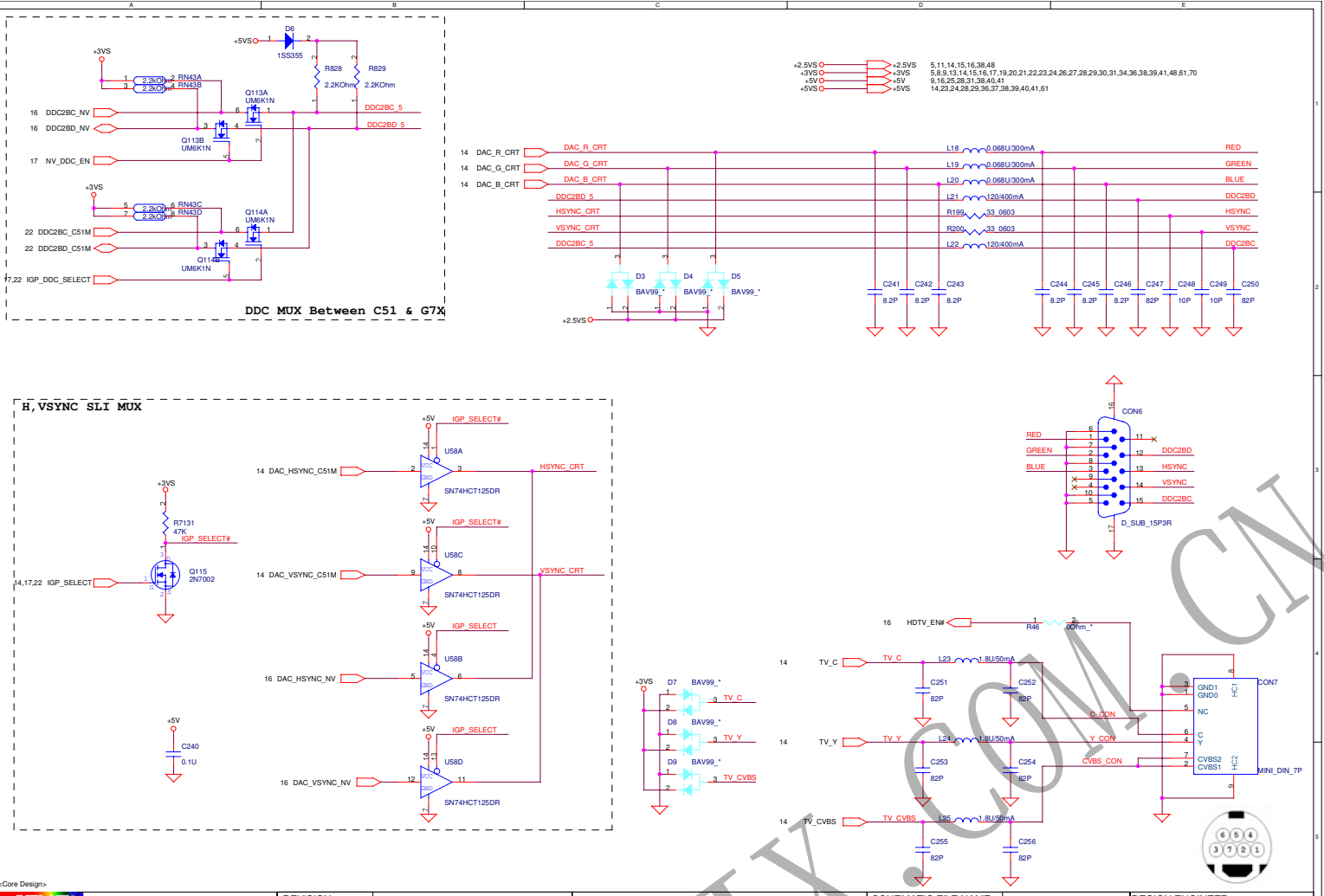
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 16 OF 55	DESCRIPTION: VGA CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

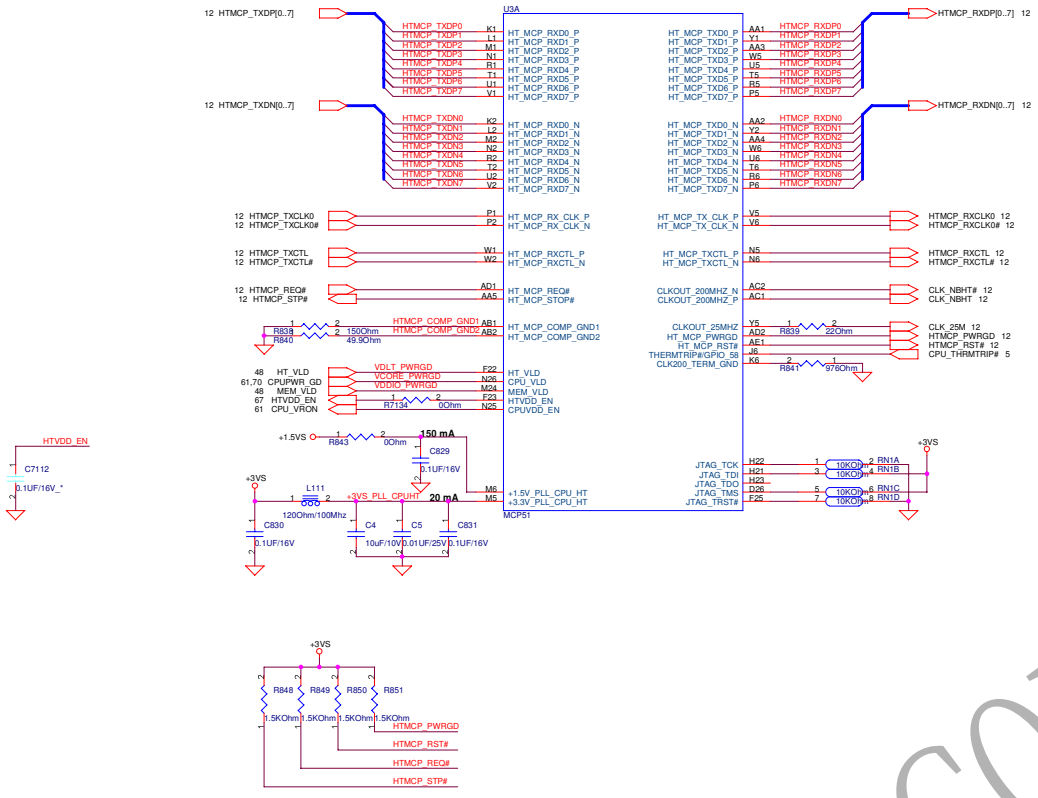


PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: LVDS, INVERTER CONN	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 17 OF 55		RELEASE DATE :	



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 18 OF 55	DESCRIPTION: CRT & TV OUT	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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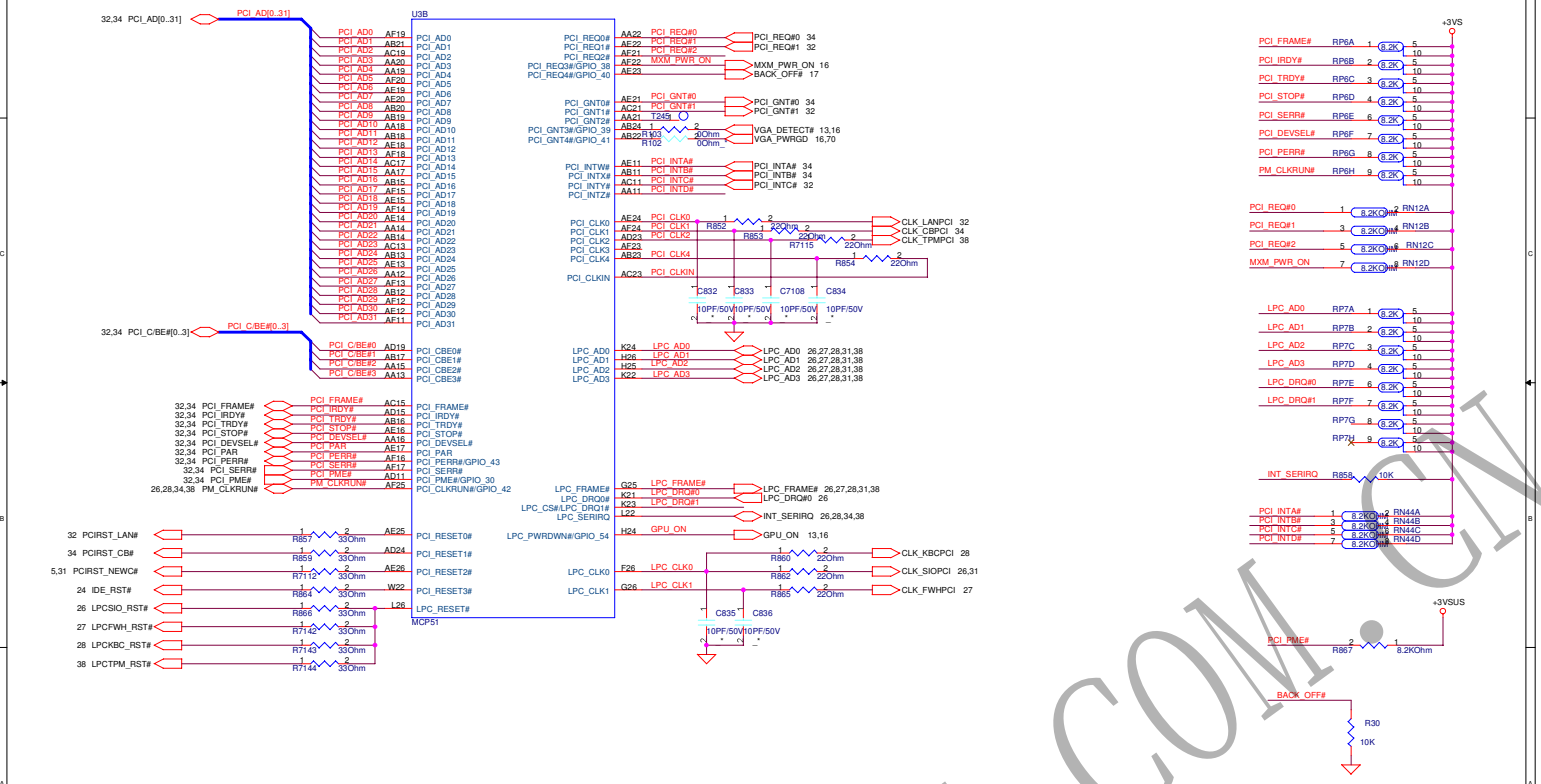
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 HT I/F	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 19 OF 55		RELEASE DATE :	Albert Su



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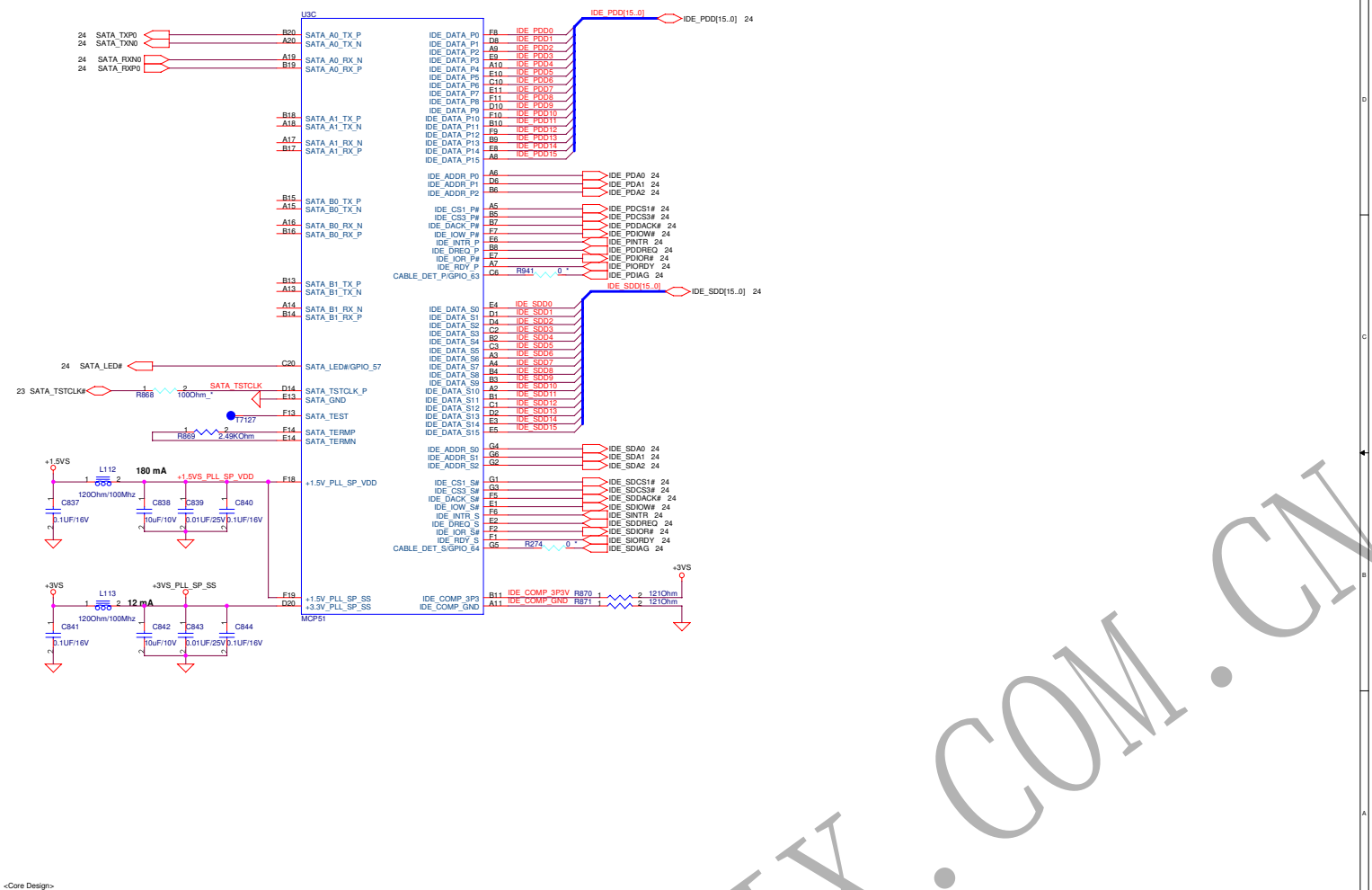
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 20 OF 55	DESCRIPTION: MCP51 PCI	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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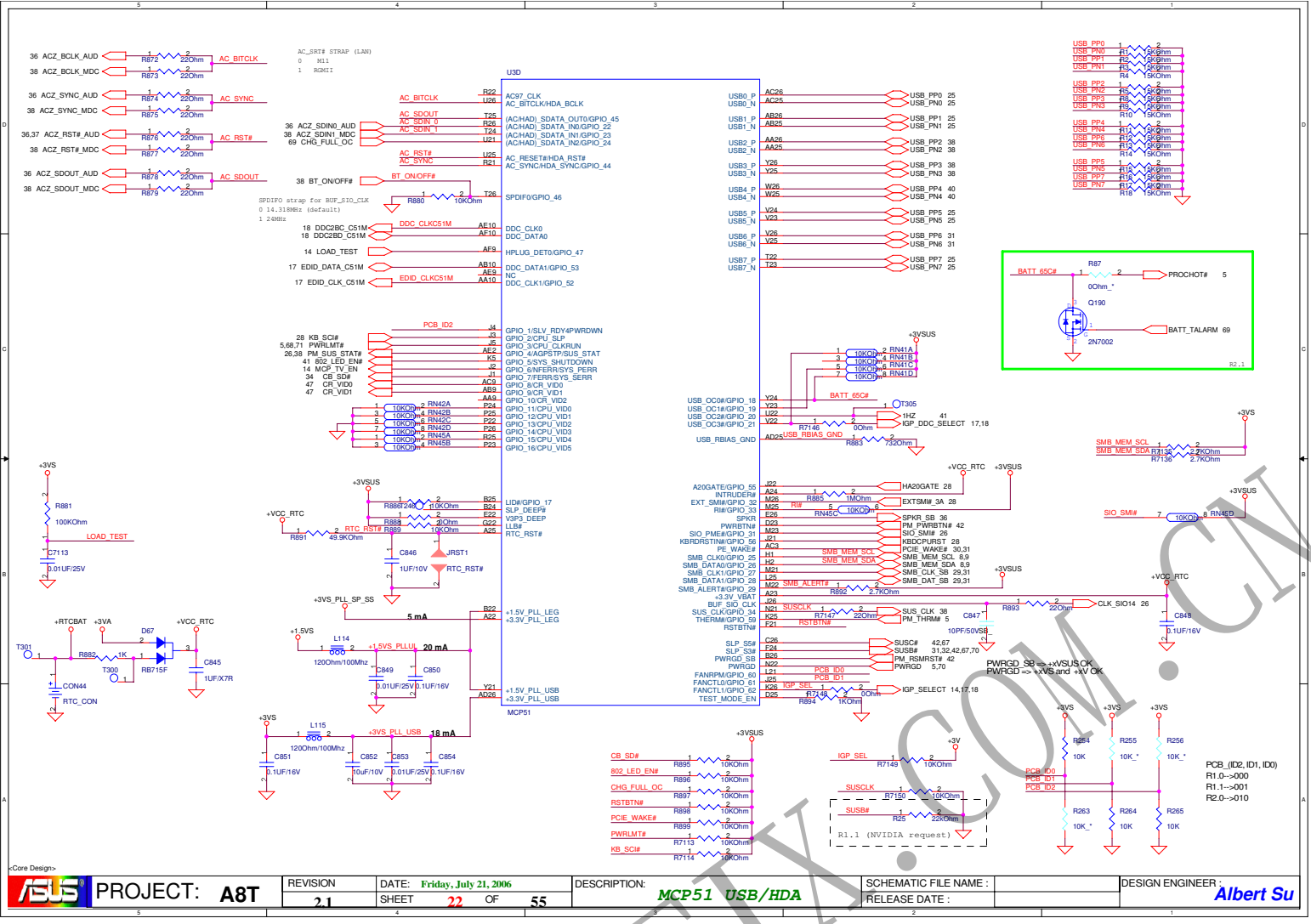
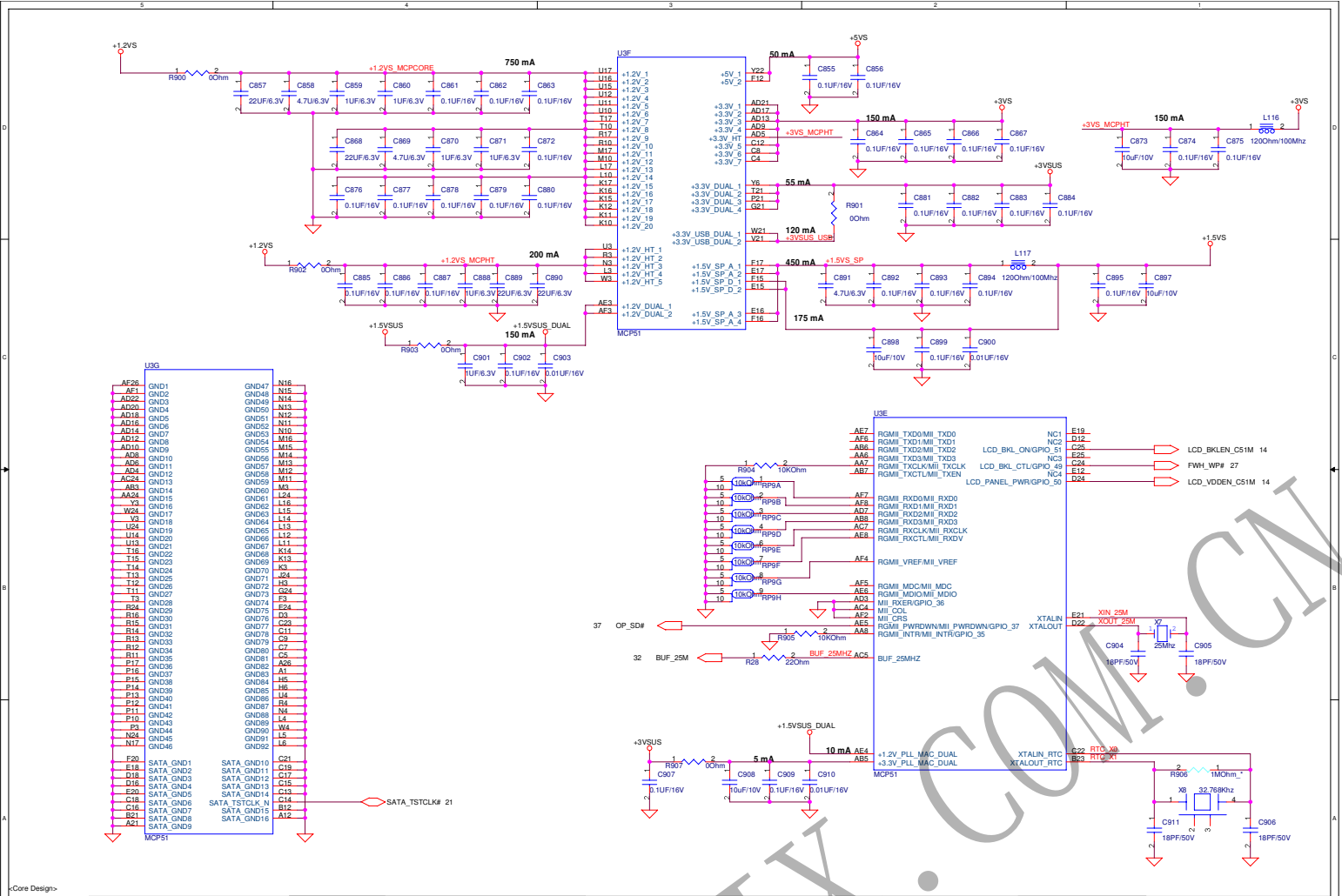
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 IDE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 21 OF 55		RELEASE DATE :	



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 22 OF 55	DESCRIPTION: MCP51 USB/HDA	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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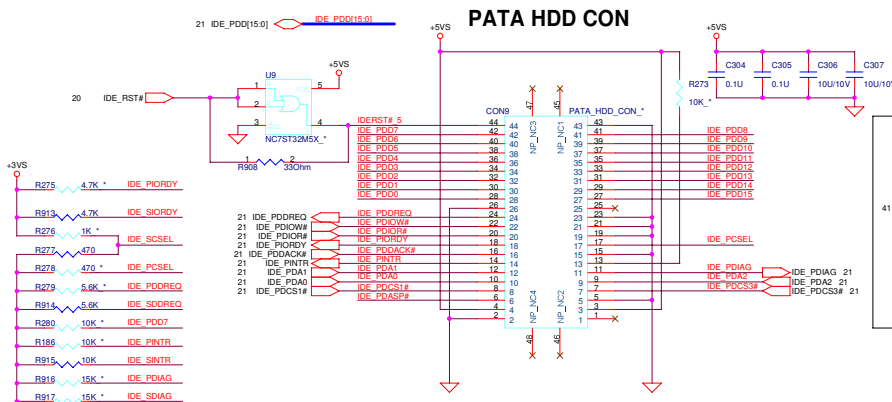
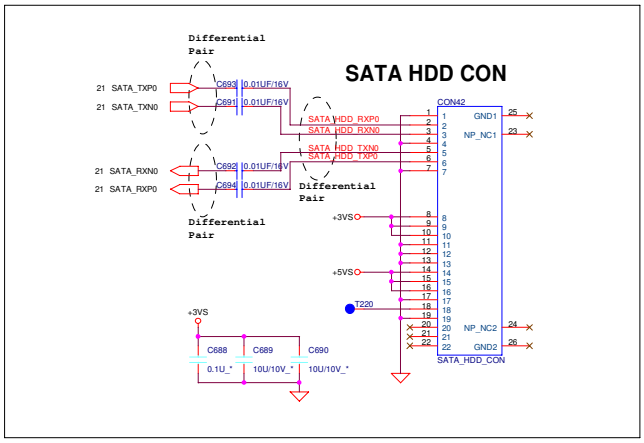
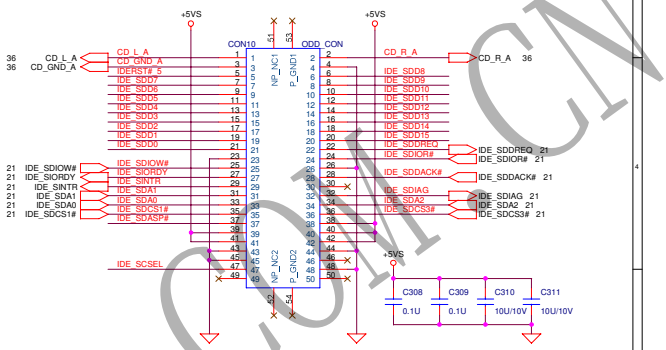
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 23 OF 55		RELEASE DATE :	



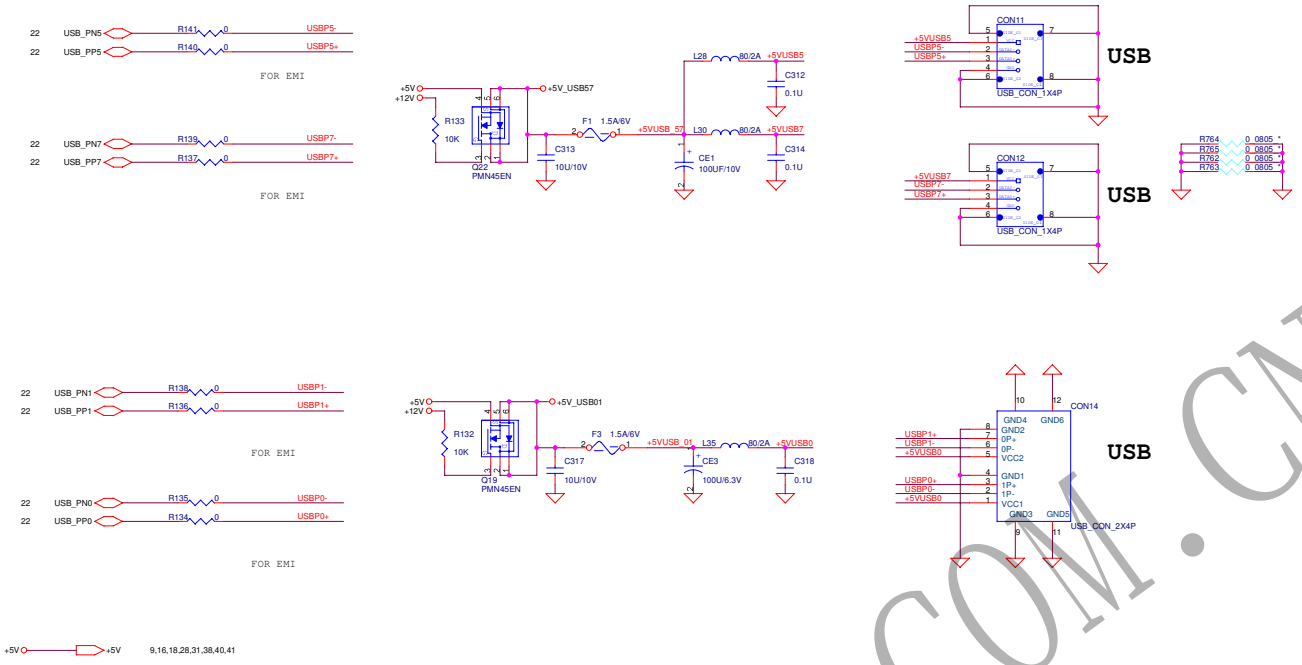




+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30,31,34,36,38,39,41,48,61,70
+5VS +5VS 14,18,23,28,29,36,37,38,39,40,41,61
+5V +5V 9,16,18,25,28,31,38,40,41

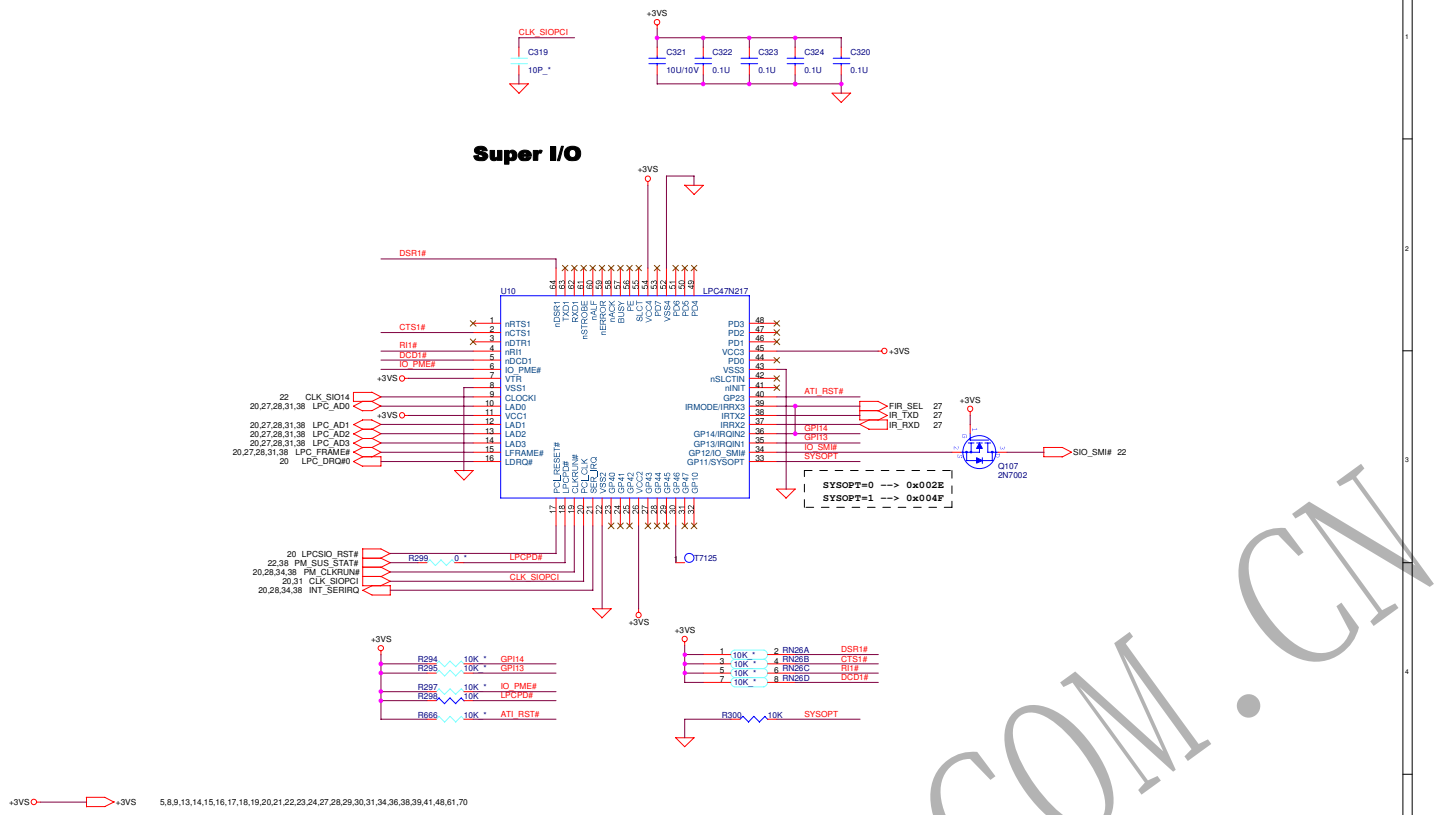
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 24 OF 55	DESCRIPTION: HDD & CD-ROM CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



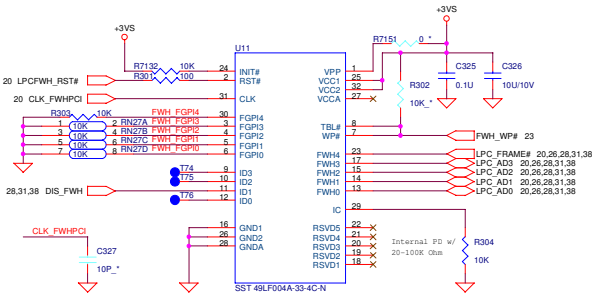
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 25 OF 55	DESCRIPTION: USB PORTS	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SUPER IO LPC47N217	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 26 OF 55		RELEASE DATE :	Albert Su



PLCC32 Socket Part Number :
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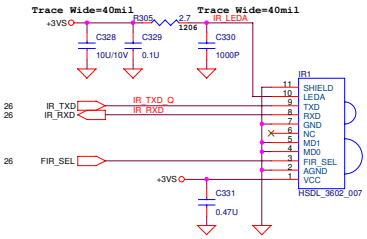
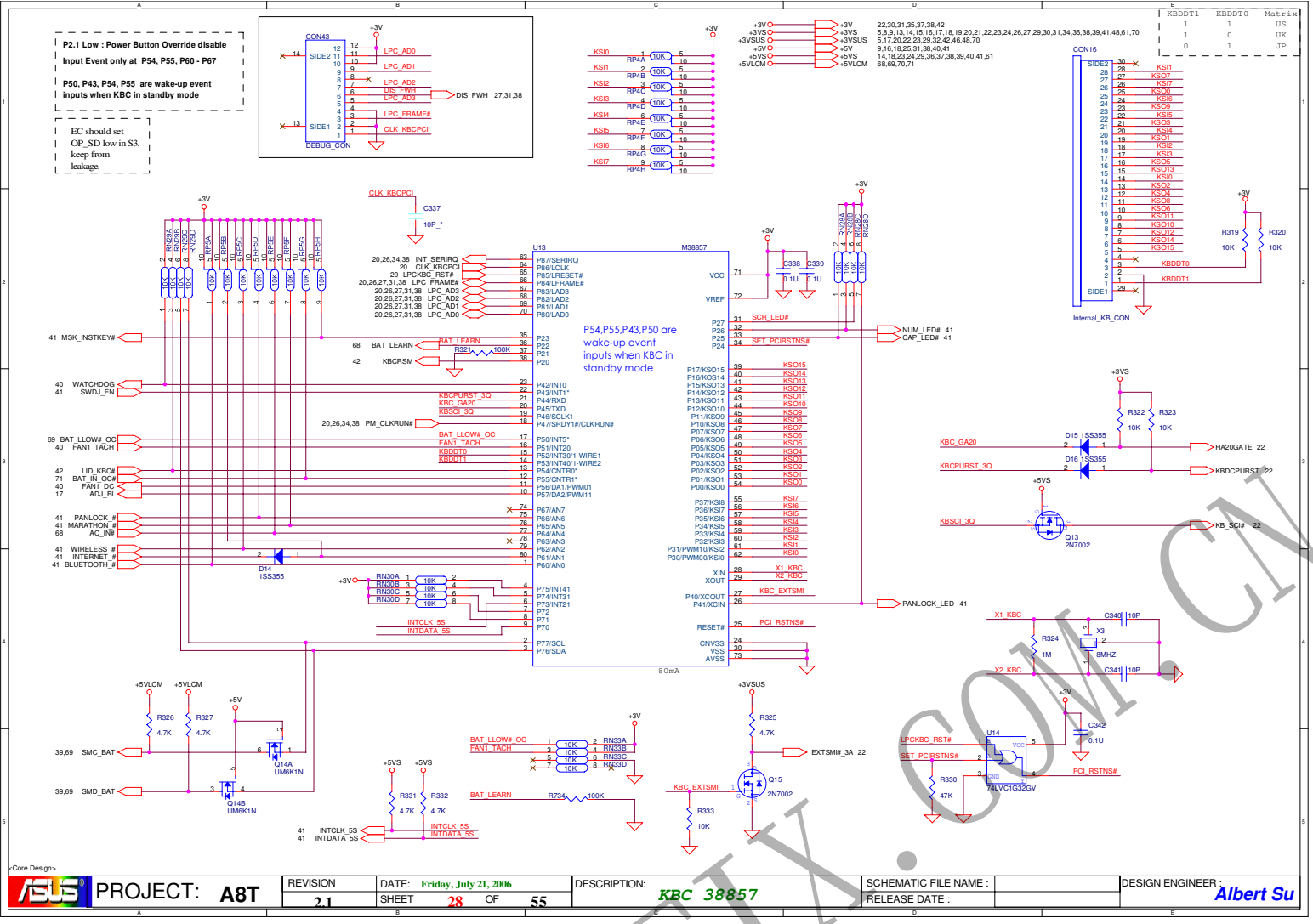
Graphics from:
05-001005111



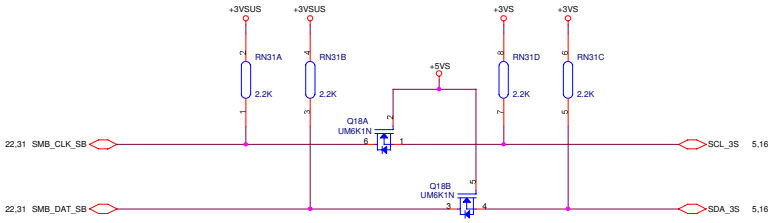
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,30,31,34,36,38,39,41,48,61,70

<Core Design>

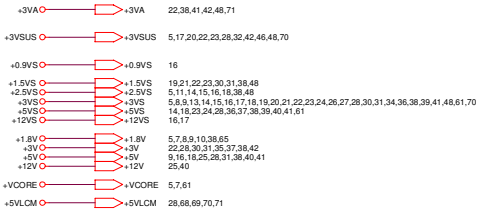
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: BIOS , IR	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
	2.1	SHEET 27 OF 55		RELEASE DATE :	



MCP51



Termal Sensor,
TPM



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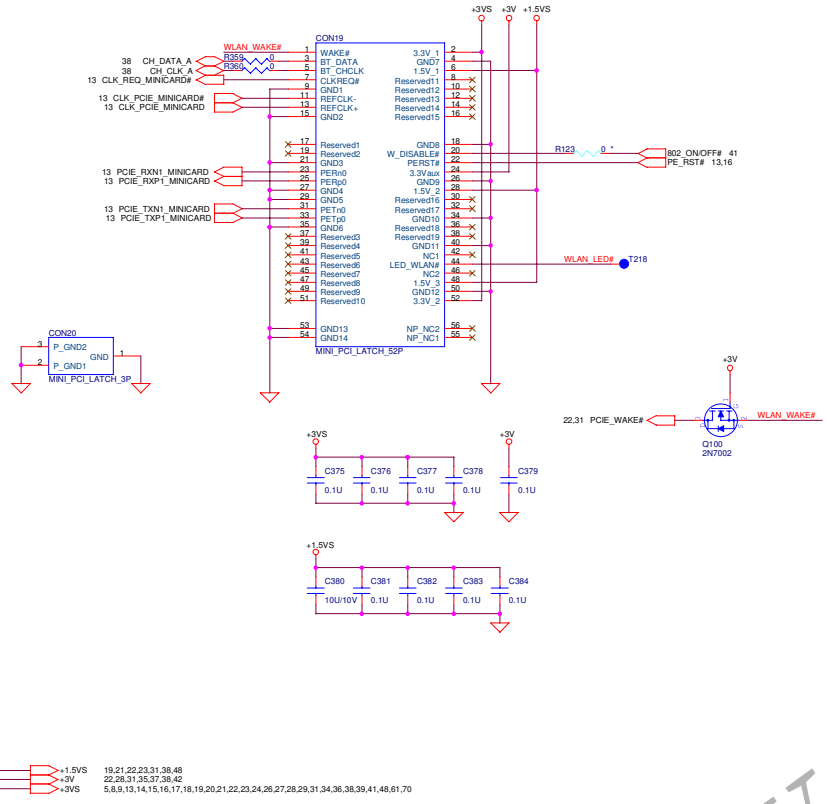
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SM BUS & POWER PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 29 OF 55		RELEASE DATE :	



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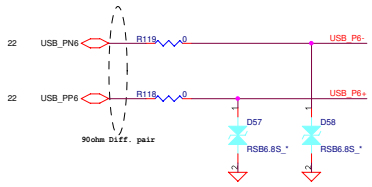
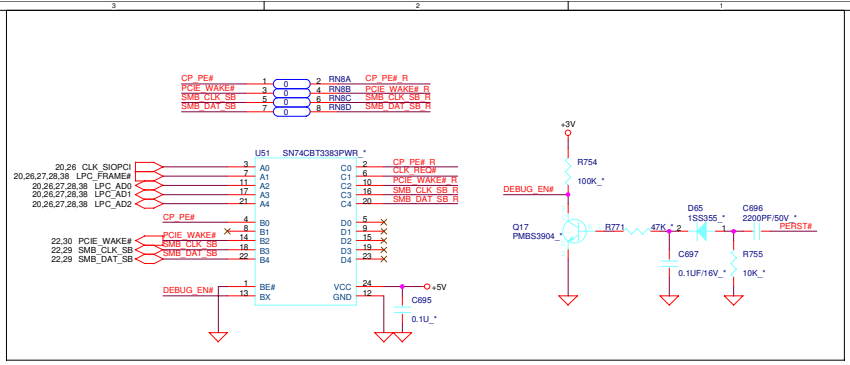
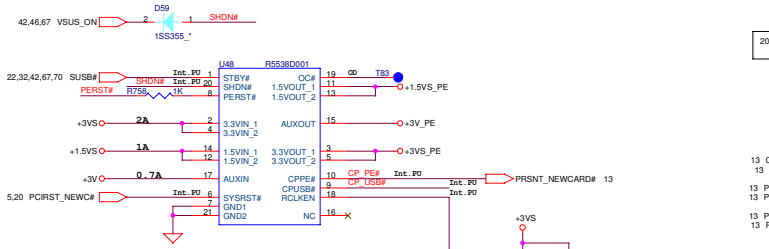
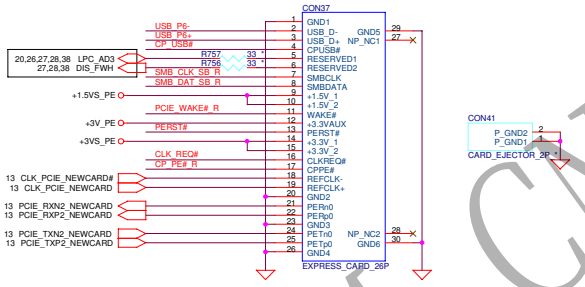
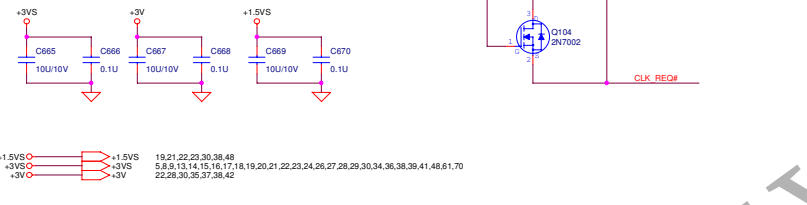
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MINI CARD	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 30 OF 55		RELEASE DATE :	

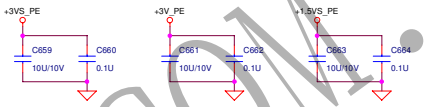












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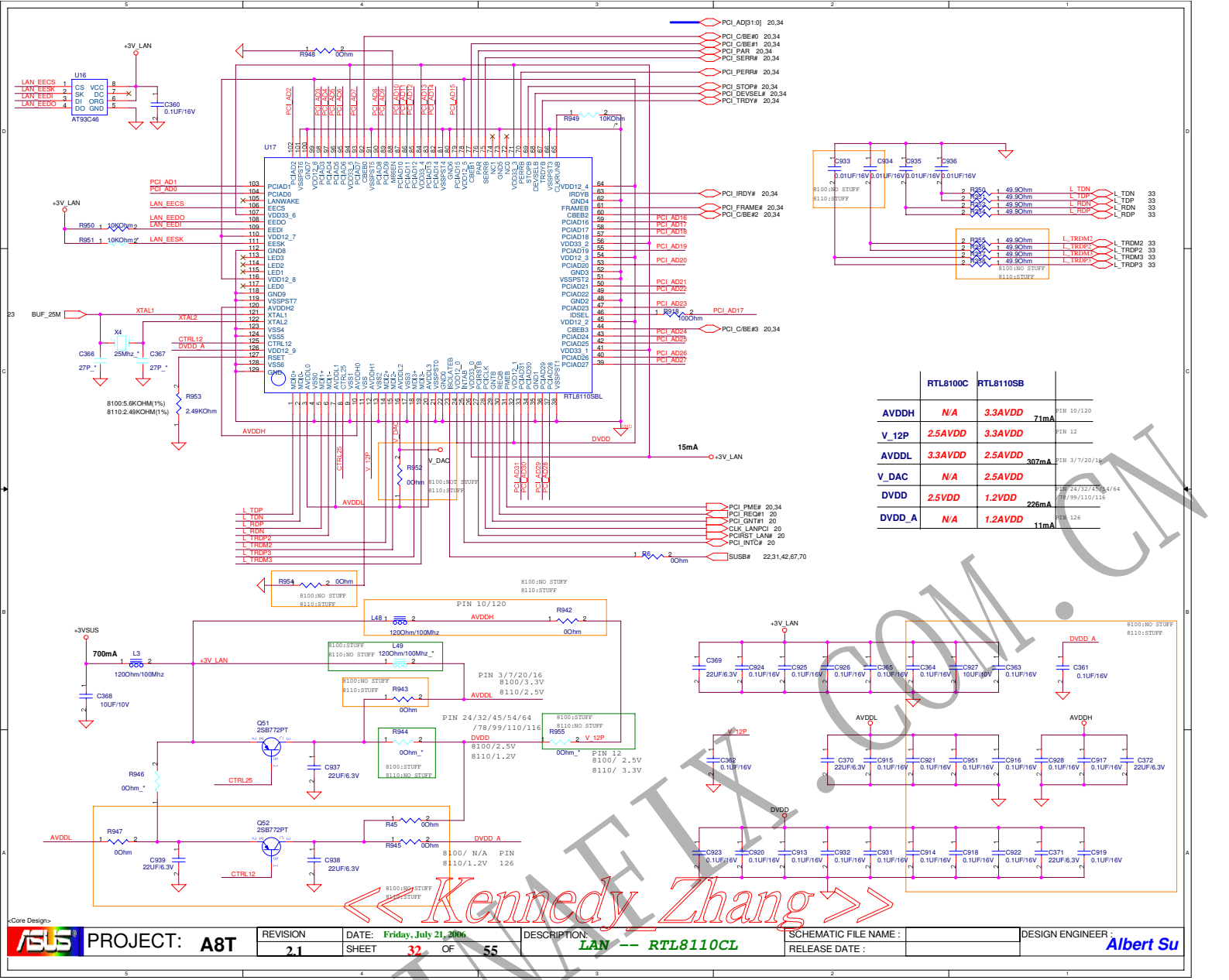
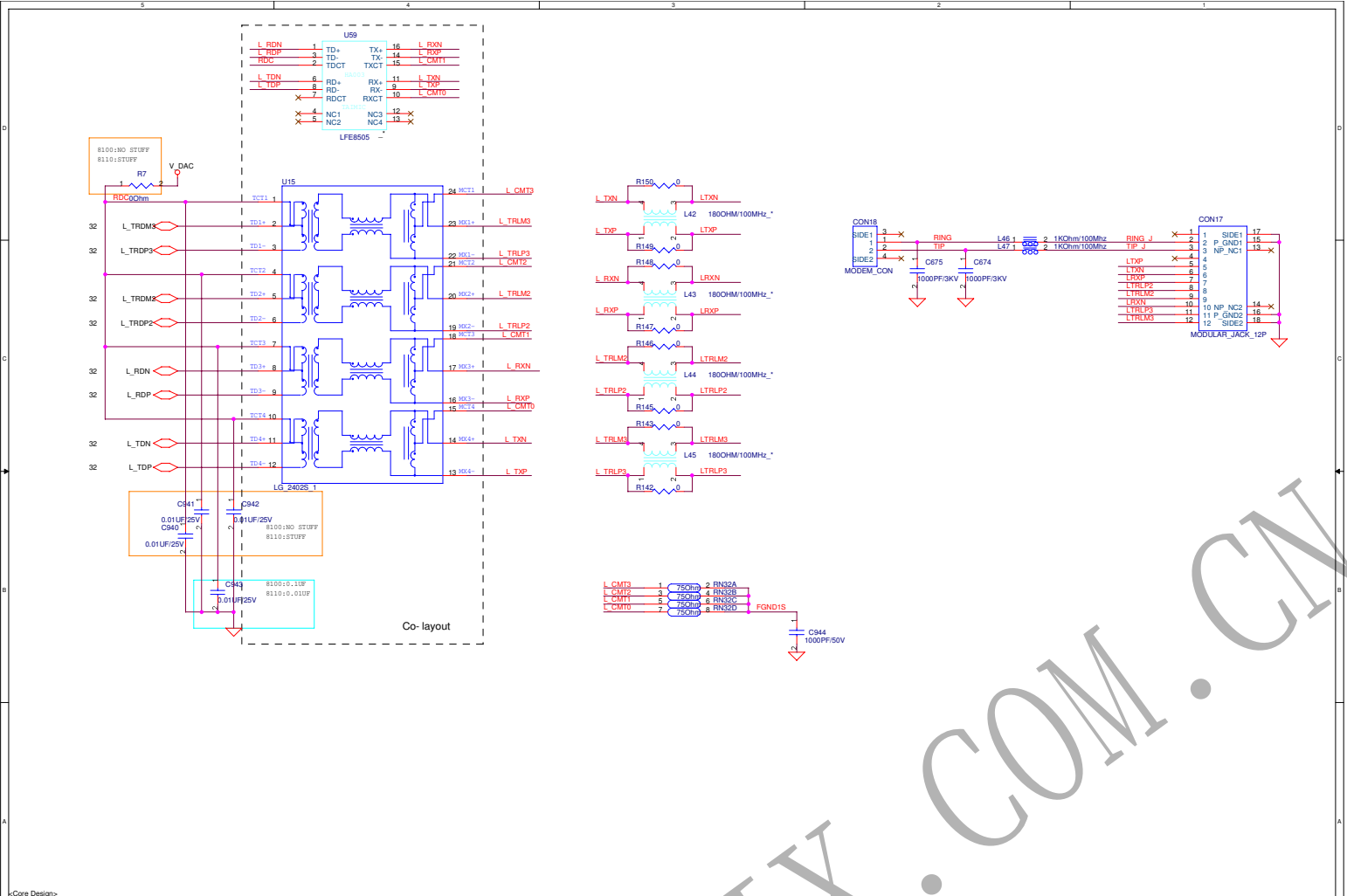
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 31 OF 55	NEW CARD	RELEASE DATE :	Albert Su



	RTL8100C	RTL8110SB	
AVDDH	N/A	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD	2.5VDD	1.2VDD	PIN 126
DVDD_A	N/A	1.2AVDD	

71mA
307mA
226mA
11mA

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: LAN -- RTL8110CL	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 32 OF 55		RELEASE DATE :	



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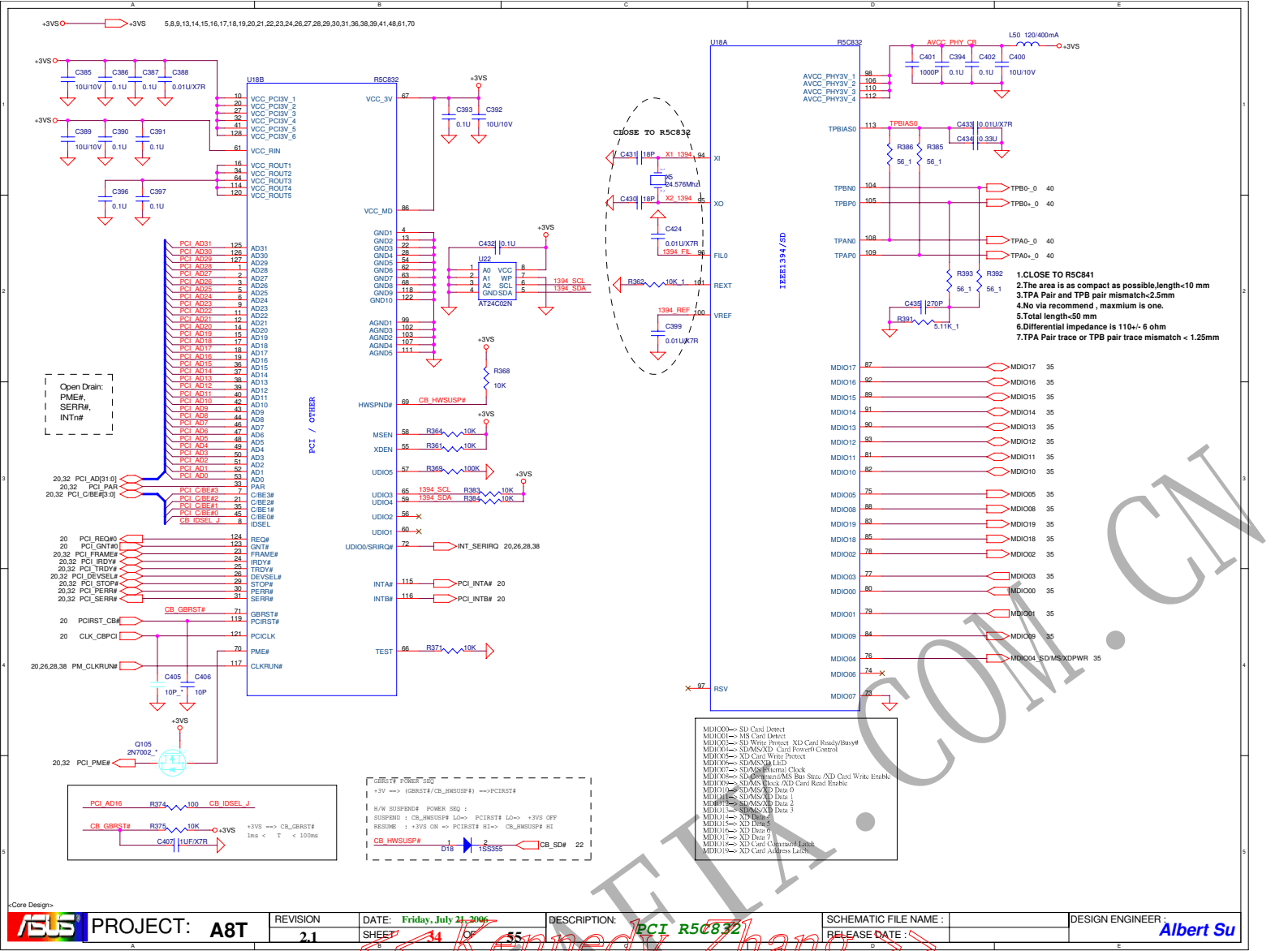
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 33 OF 55	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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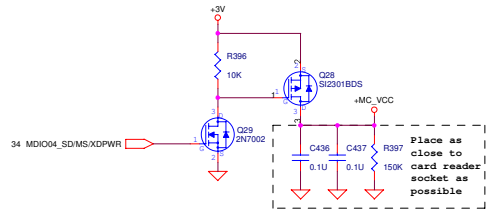
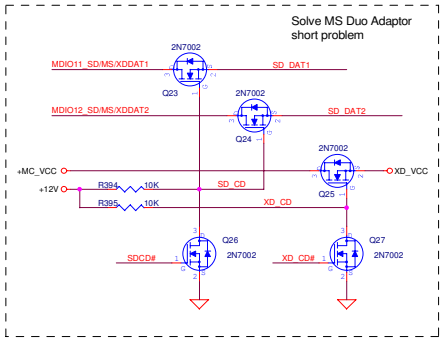
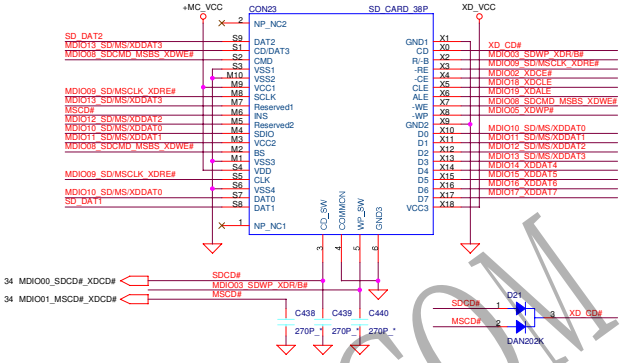
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 44 OF 55	DESCRIPTION: PCI R5C832	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su







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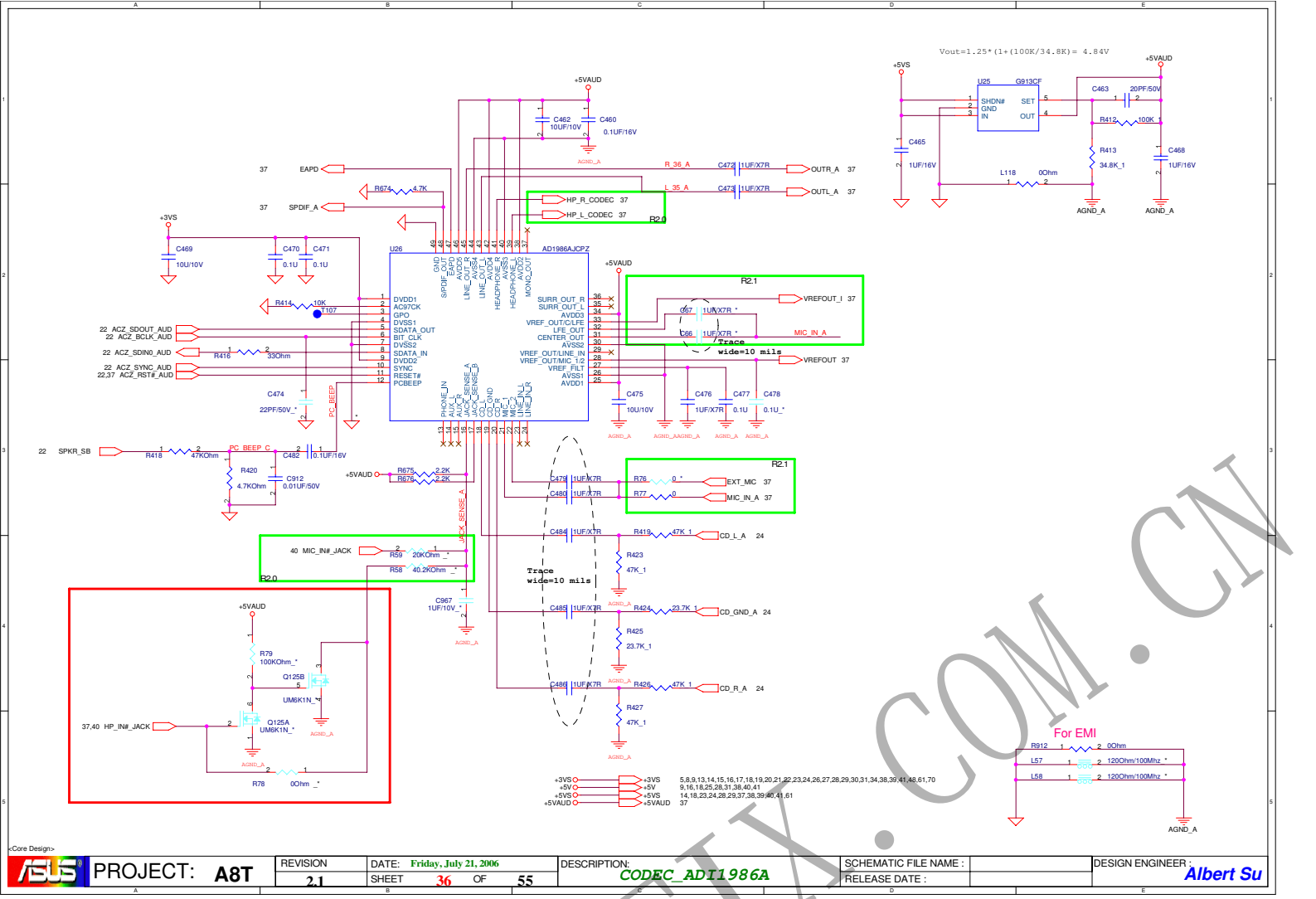
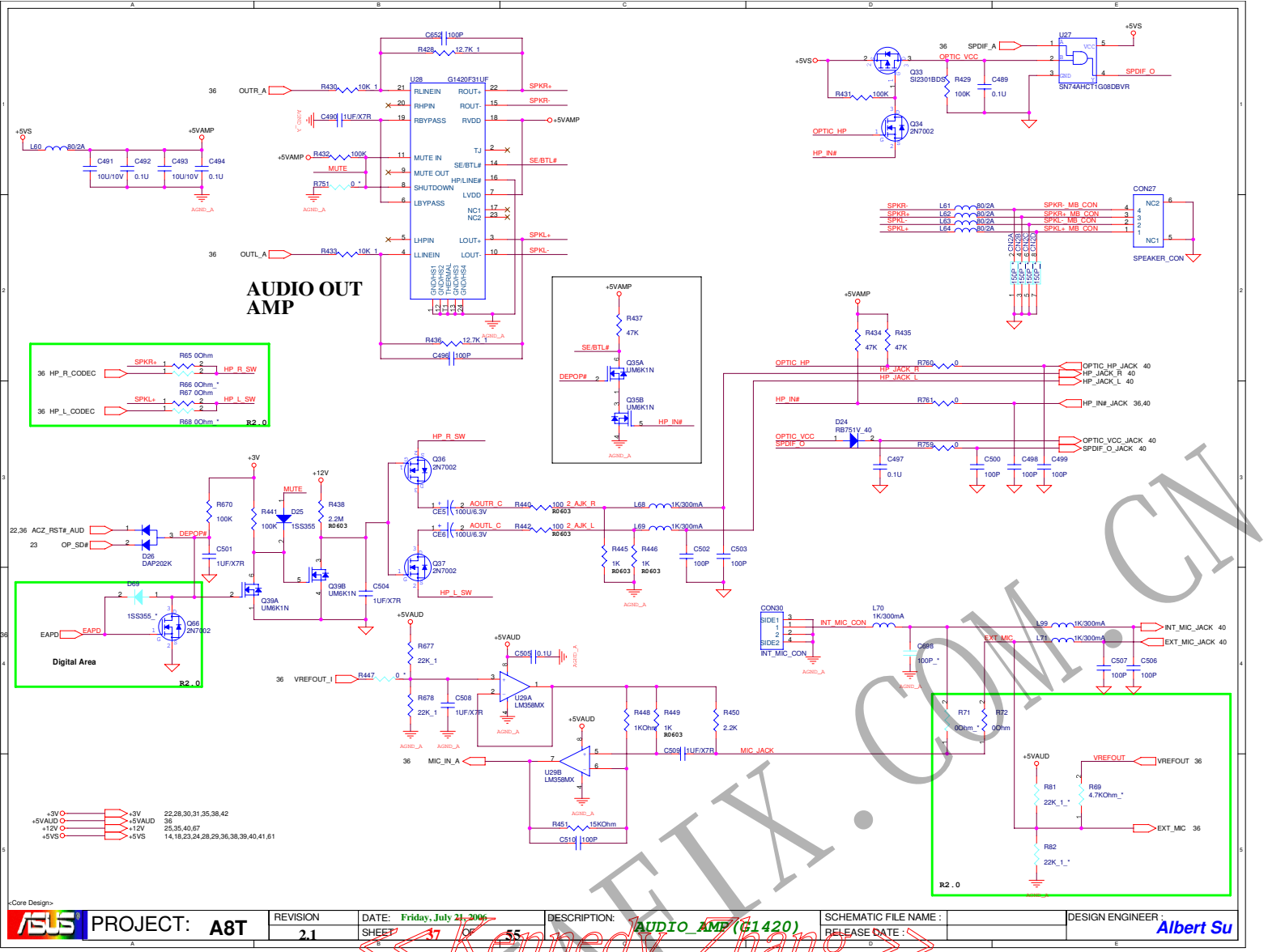
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 35 OF 55	DESCRIPTION: 4 IN 1 CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

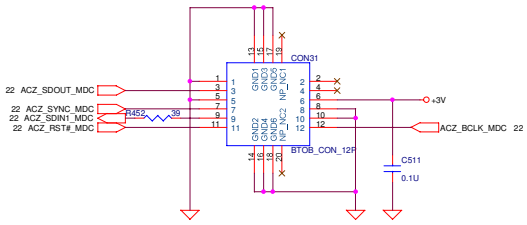


<Core Design>

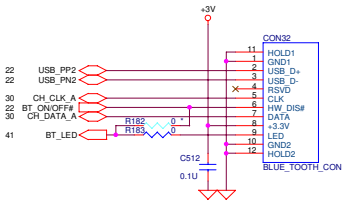
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 36 OF 55		RELEASE DATE :		



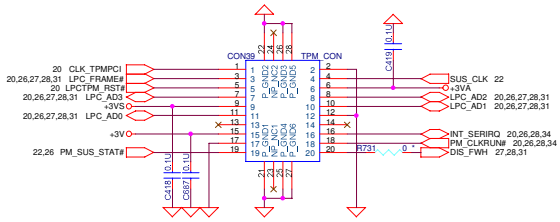
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: AUDIO_AMP (G1420)	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 37 OF 55		RELEASE DATE :		



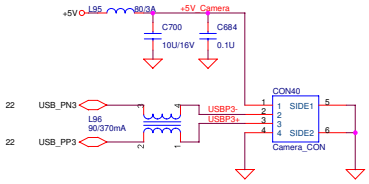
Azalia MDC MODEM CON



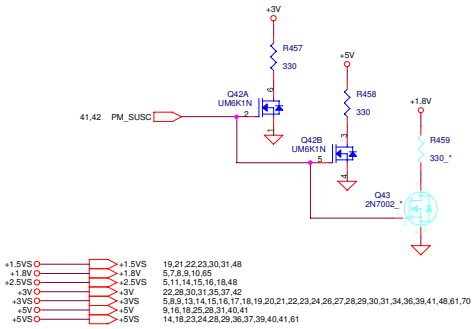
Bluetooth Module CON

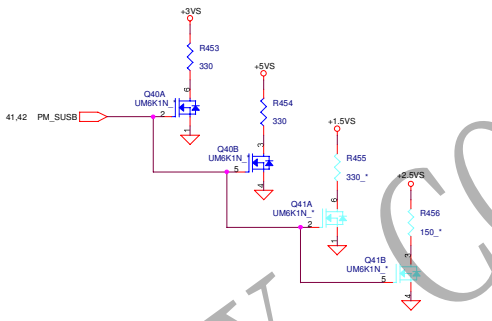


TPM Module CON



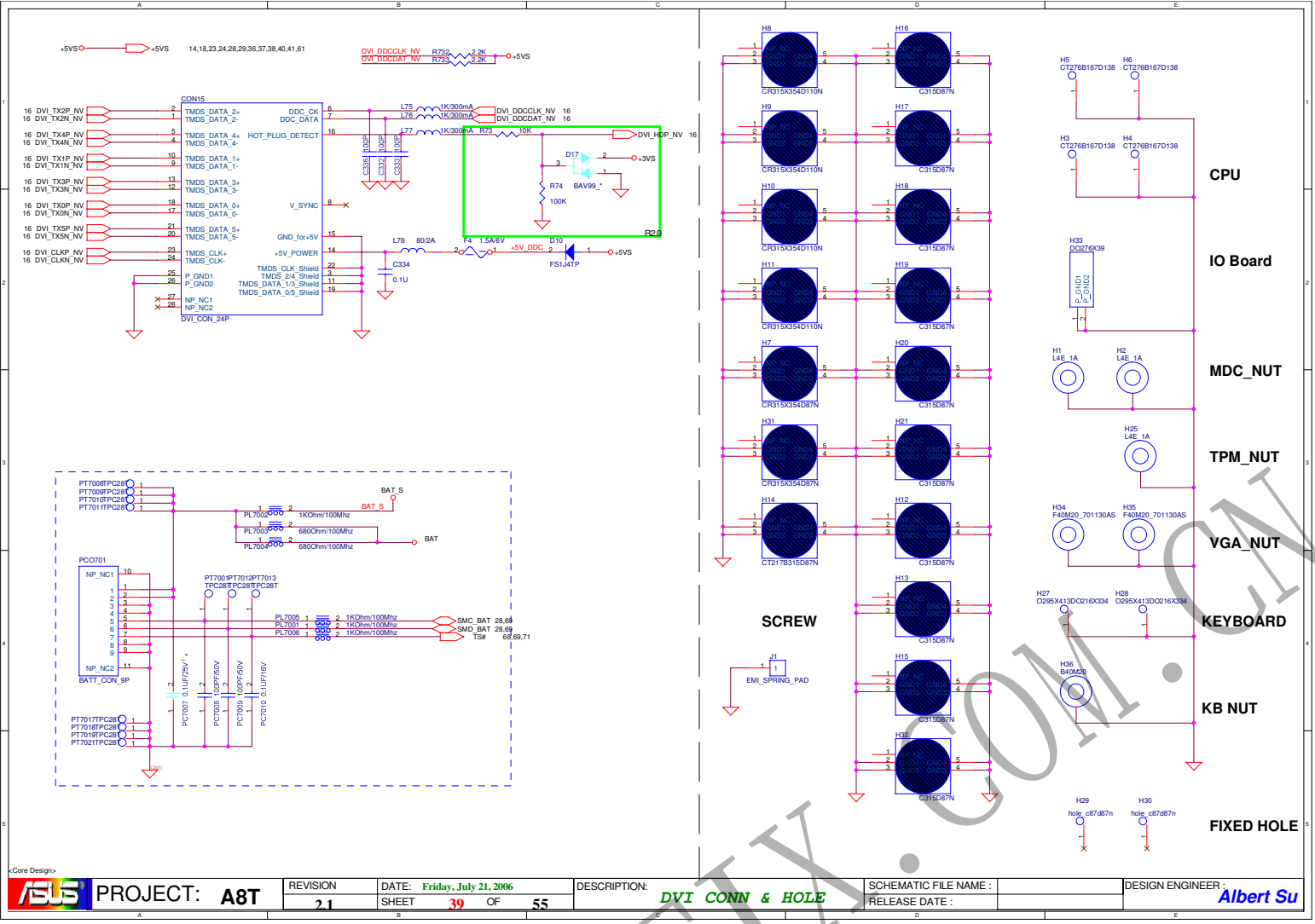
Camera Module CON





<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 38 OF 55	DESCRIPTION: MDC, B/T, TPM, Camera & DISCHG	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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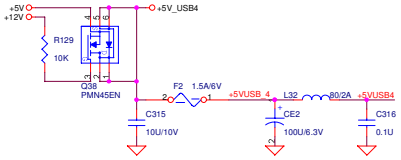
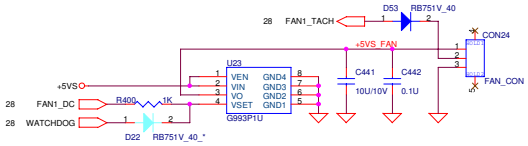
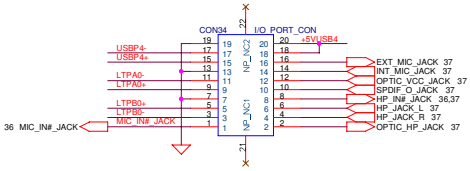
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DVI CONN & HOLE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 39 OF 55		RELEASE DATE :	

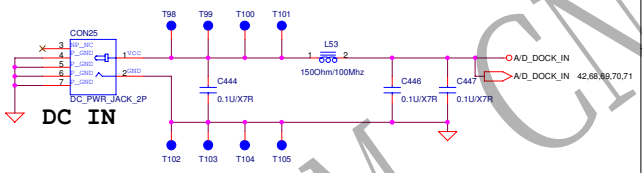




FAN CONTROL



I/O PORT

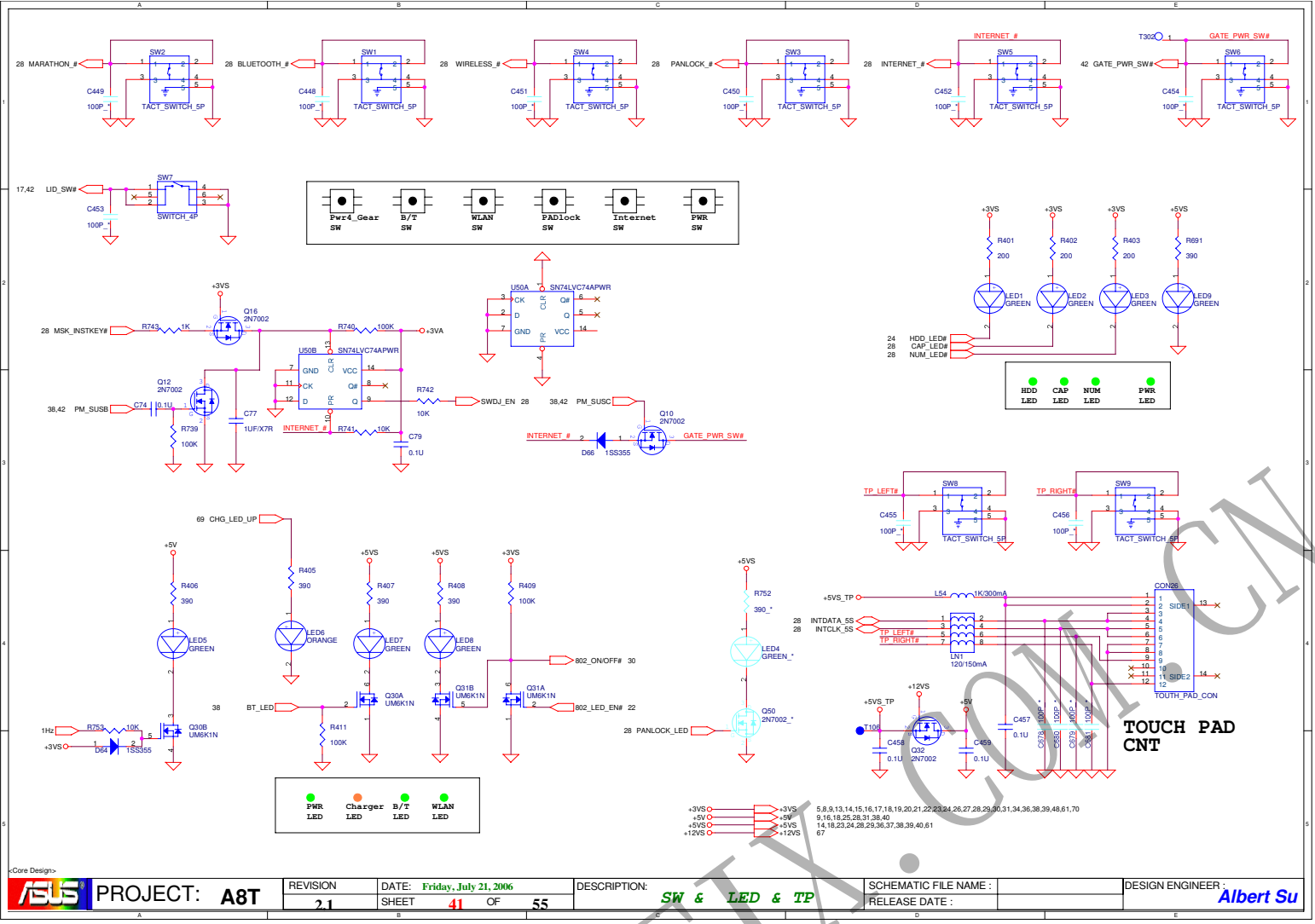


DC IN

ACIN_CONN

<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 40 OF 55	FAN_CTRL & ACIN	RELEASE DATE :	Albert Su



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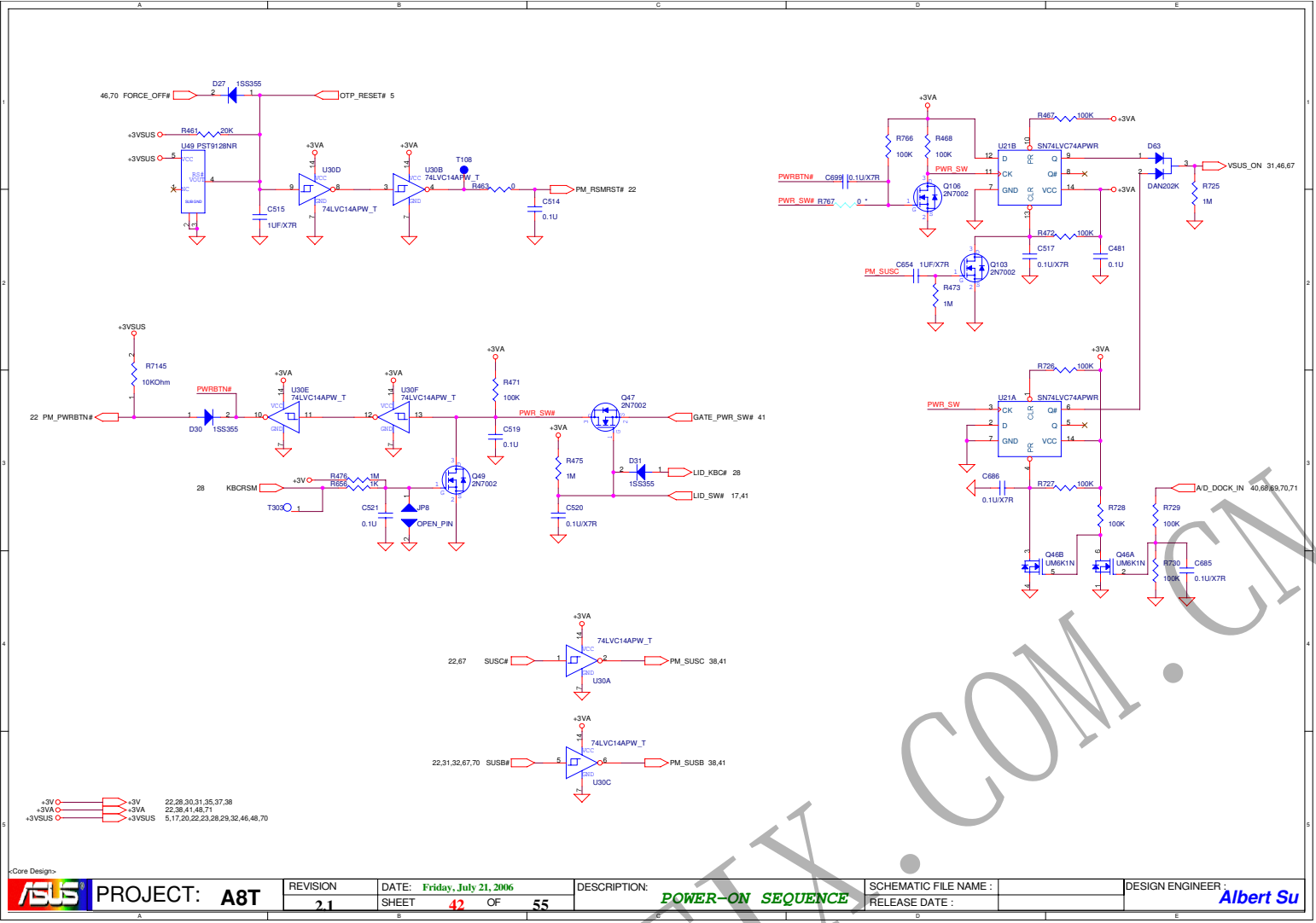
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 41 OF 55	DESCRIPTION: SW & LED & TP	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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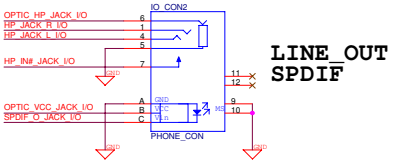
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 42 OF 55		RELEASE DATE :	

Revision History

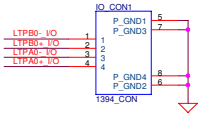
Power:

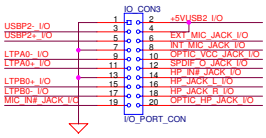
System:

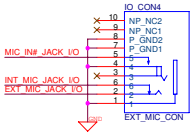


LINE_OUT
SPDIF

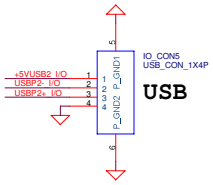
1394A



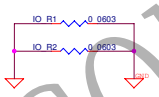




MIC



USB



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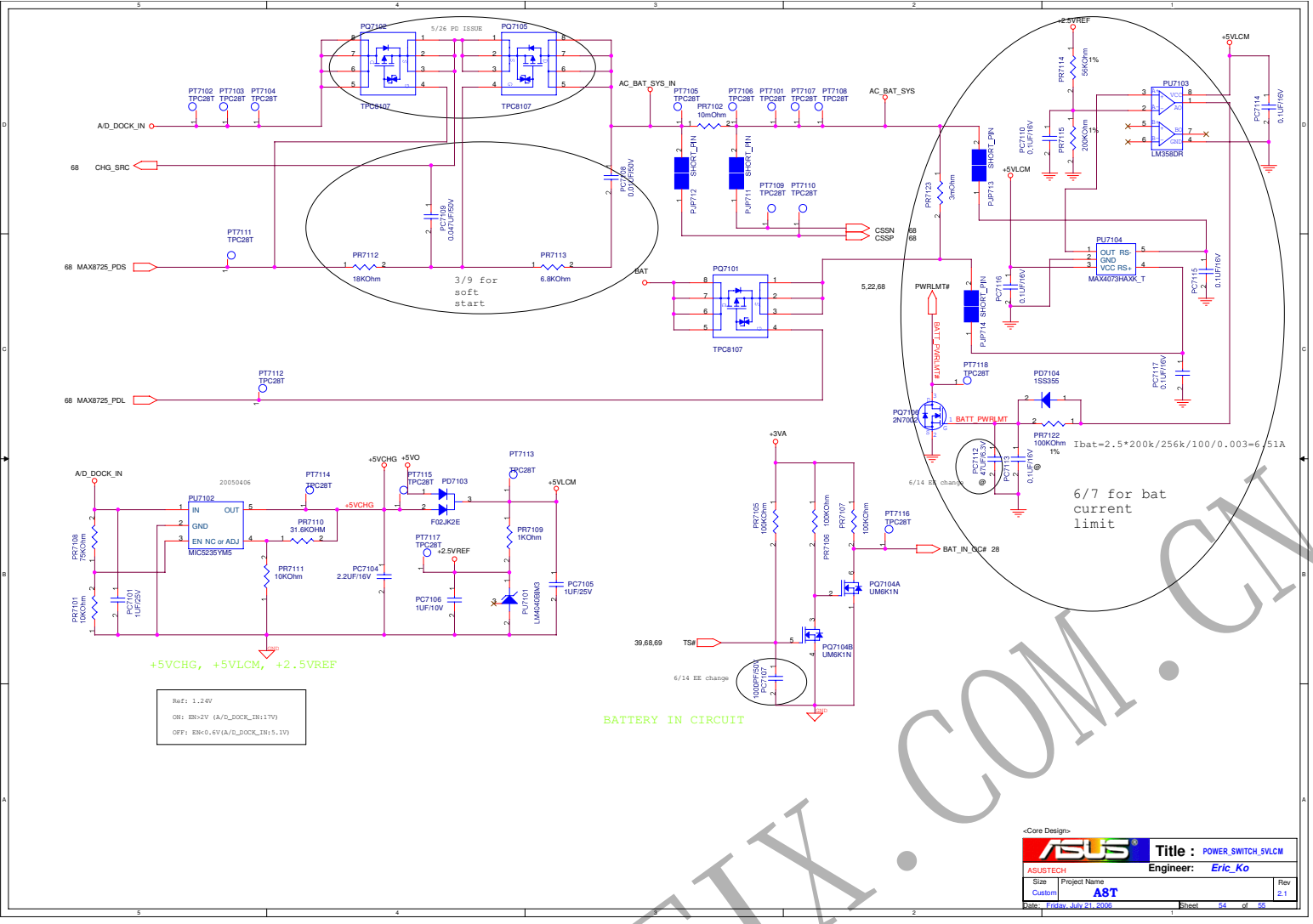
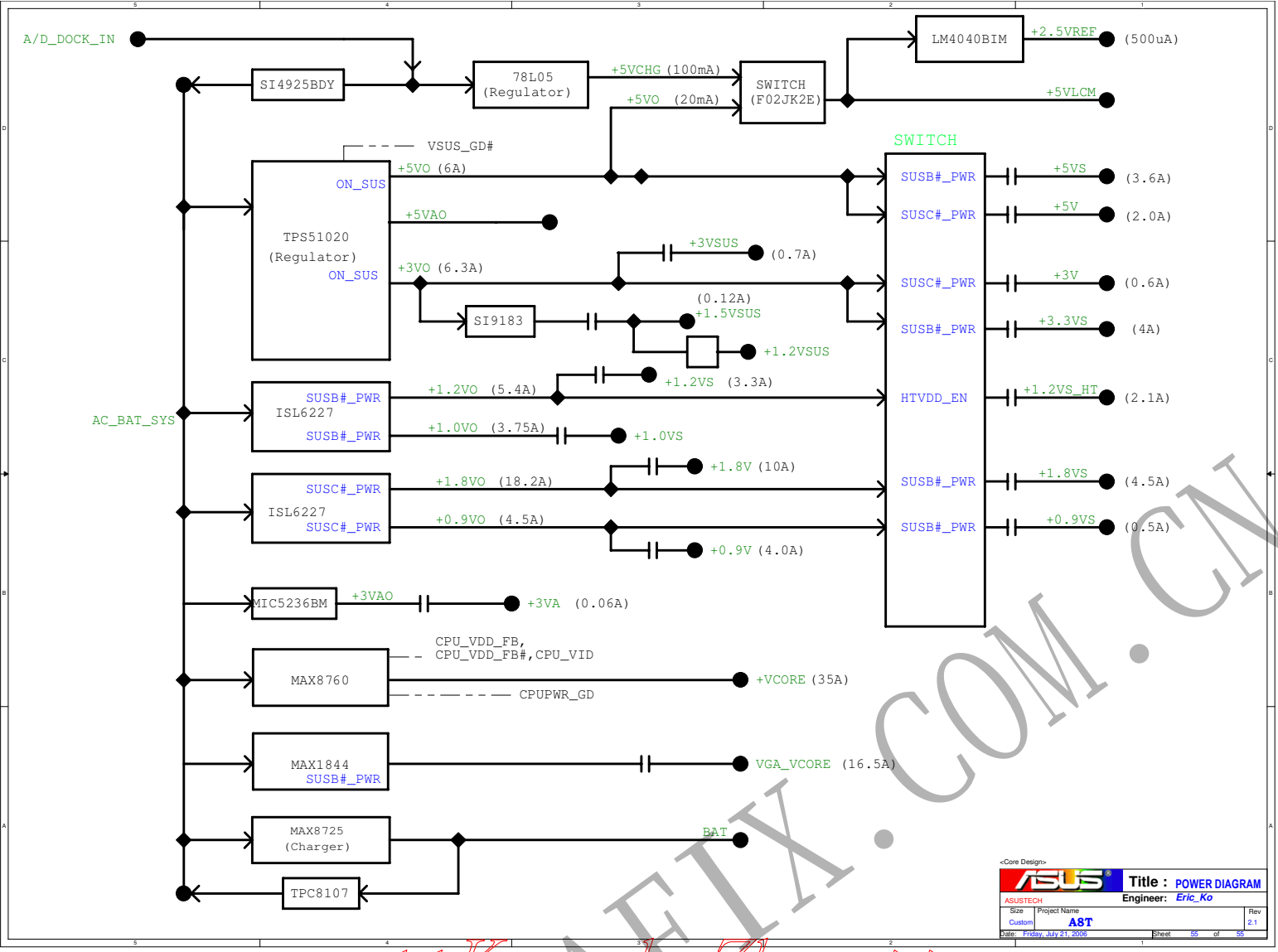
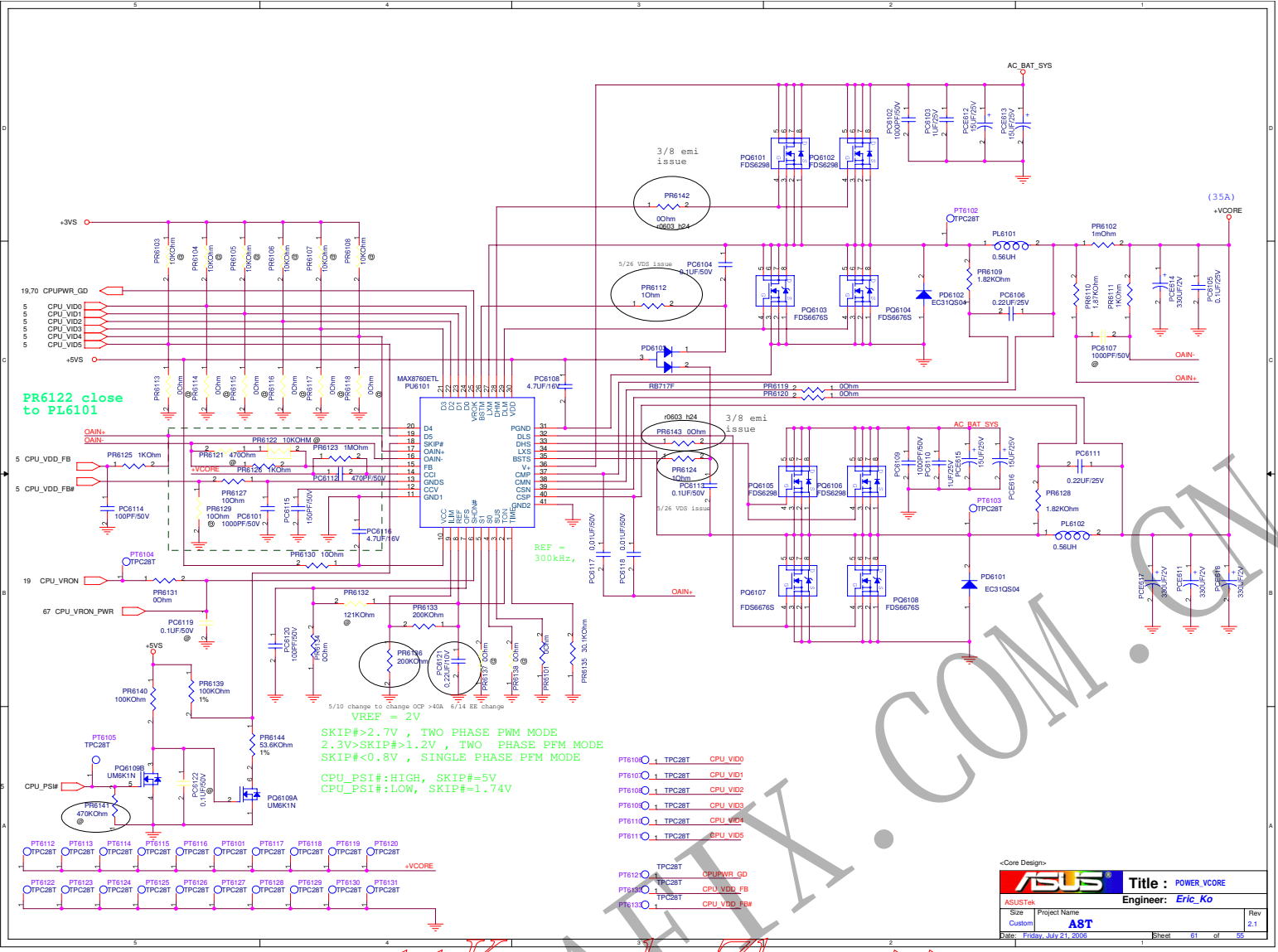
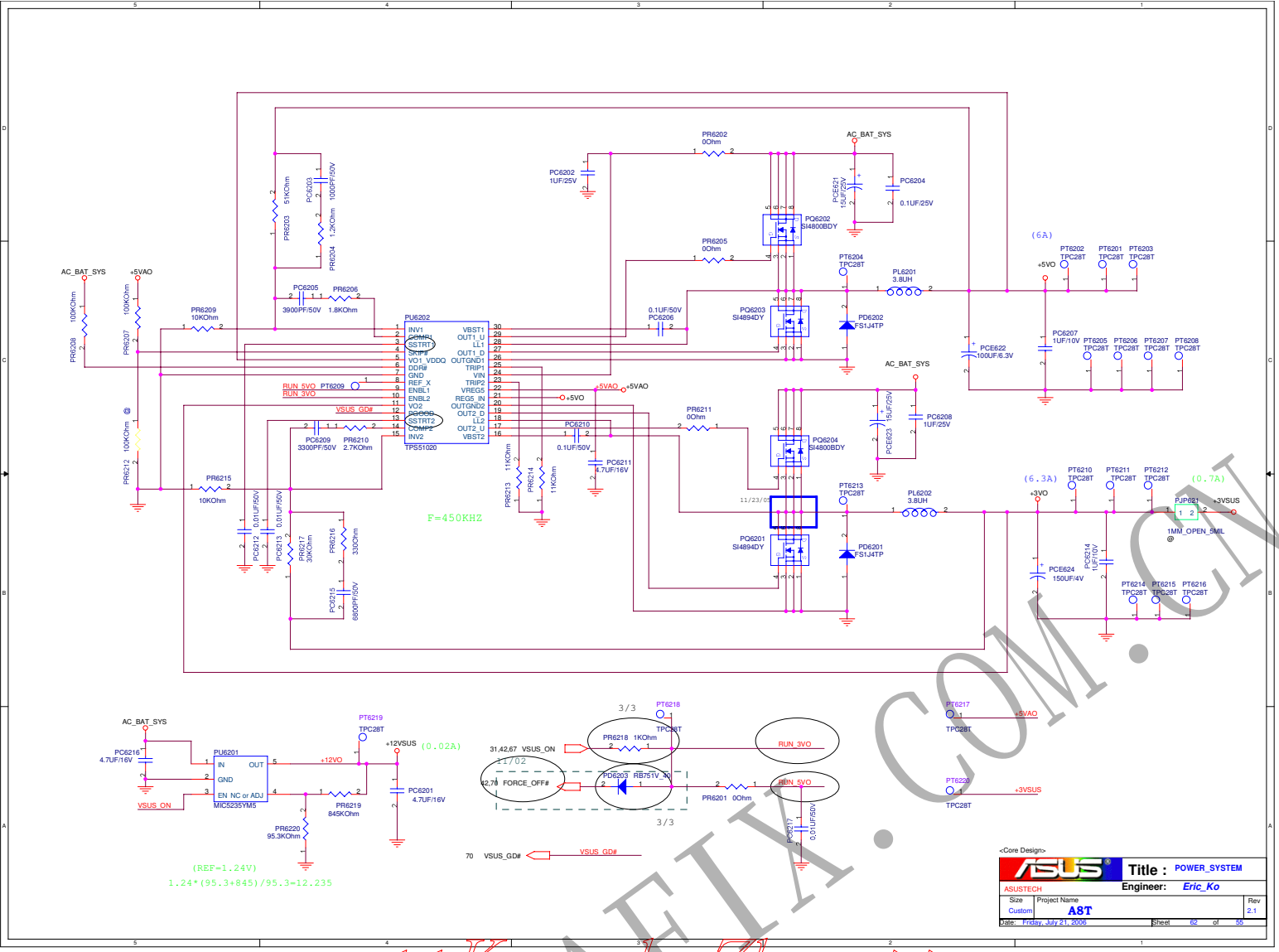
PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: I/O PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 44 OF 55		RELEASE DATE :	Albert Su

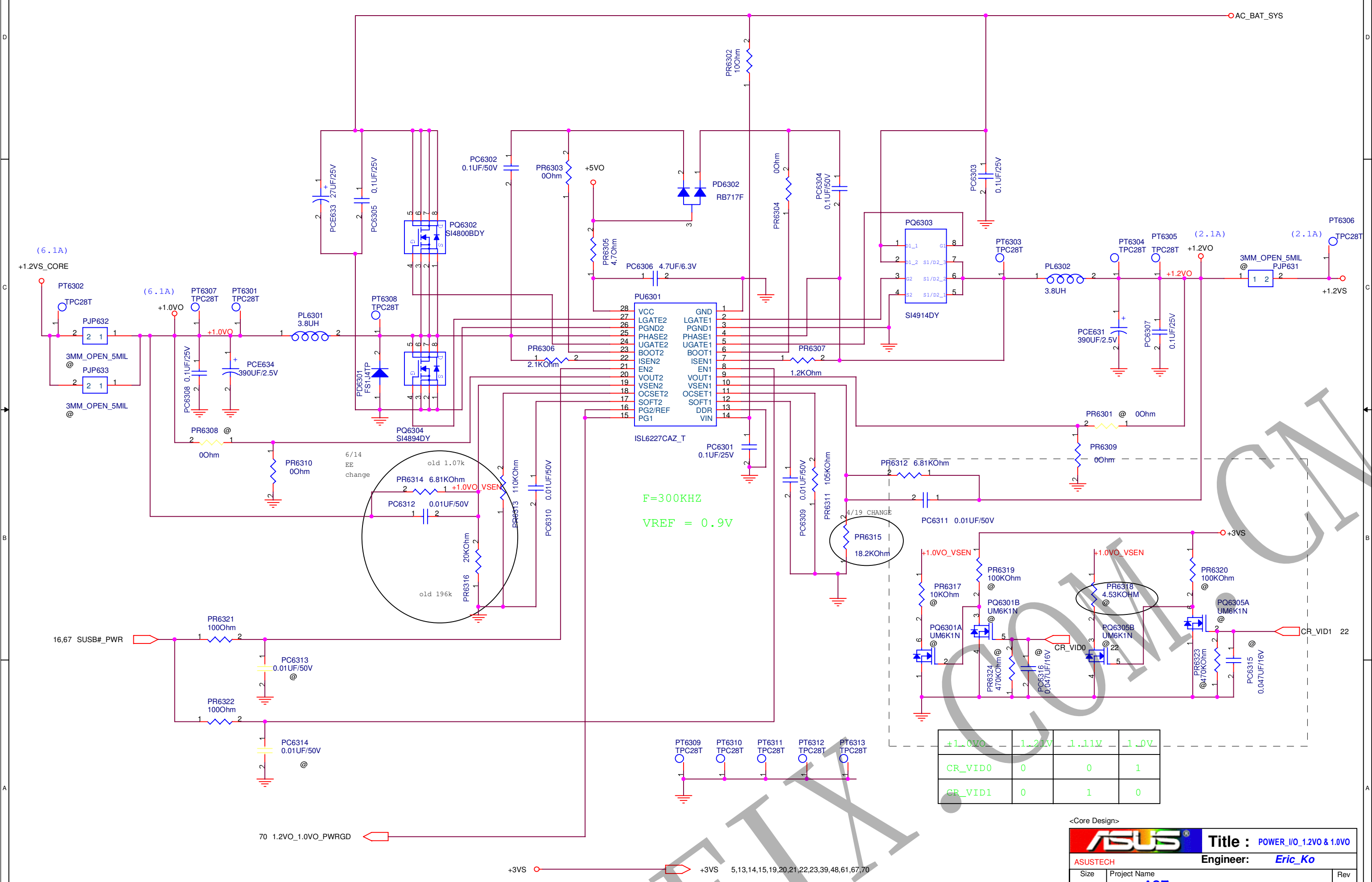


<< Kennedy Zhang >>









+1.0VO	1.21V	1.11V	1.0V
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CR_VID1	0	1	0

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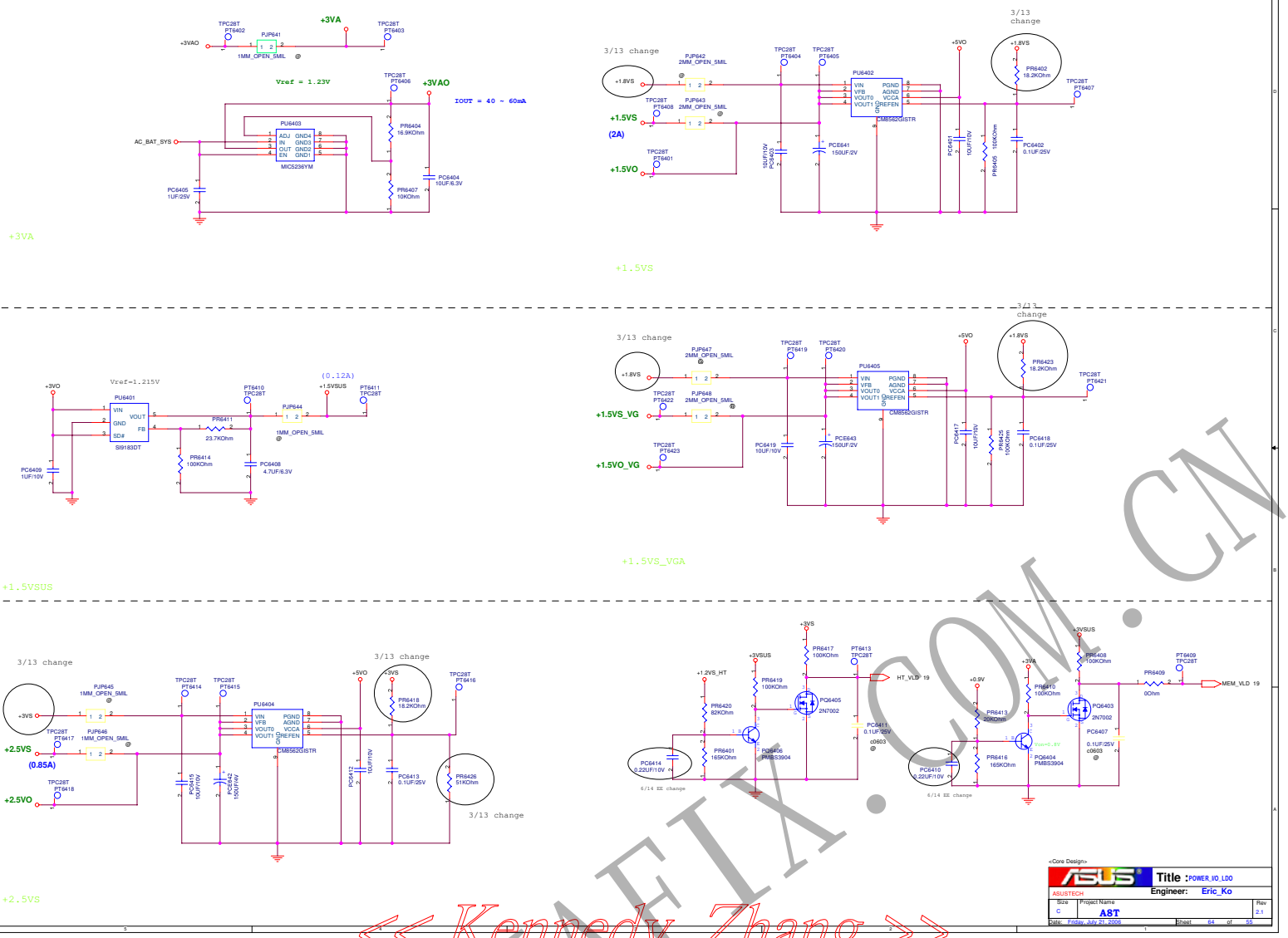
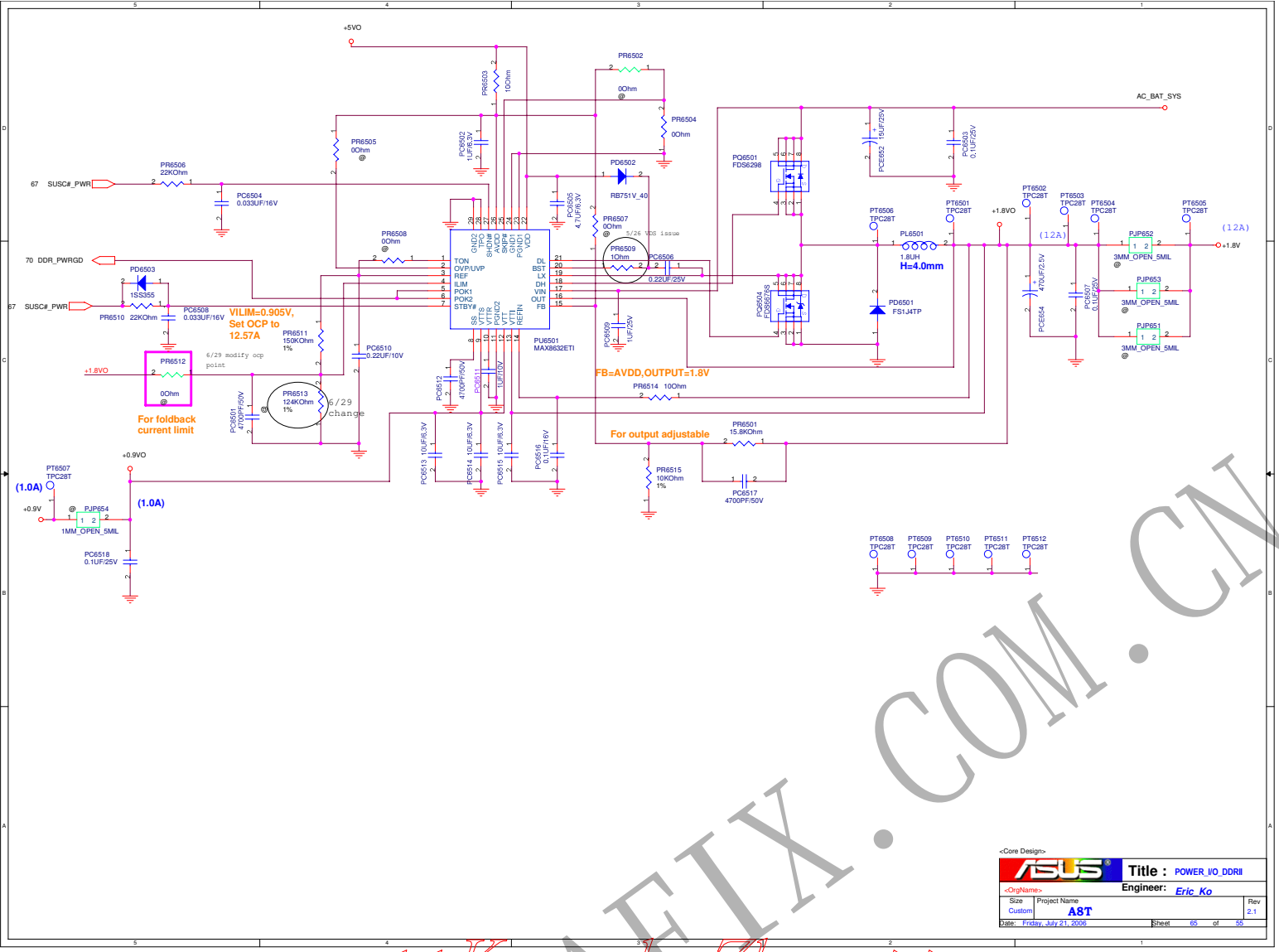
ASUSTECH	Title : POWER_I/O_1.2VO & 1.0VO	
	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 63 of 55	





<Core Design>

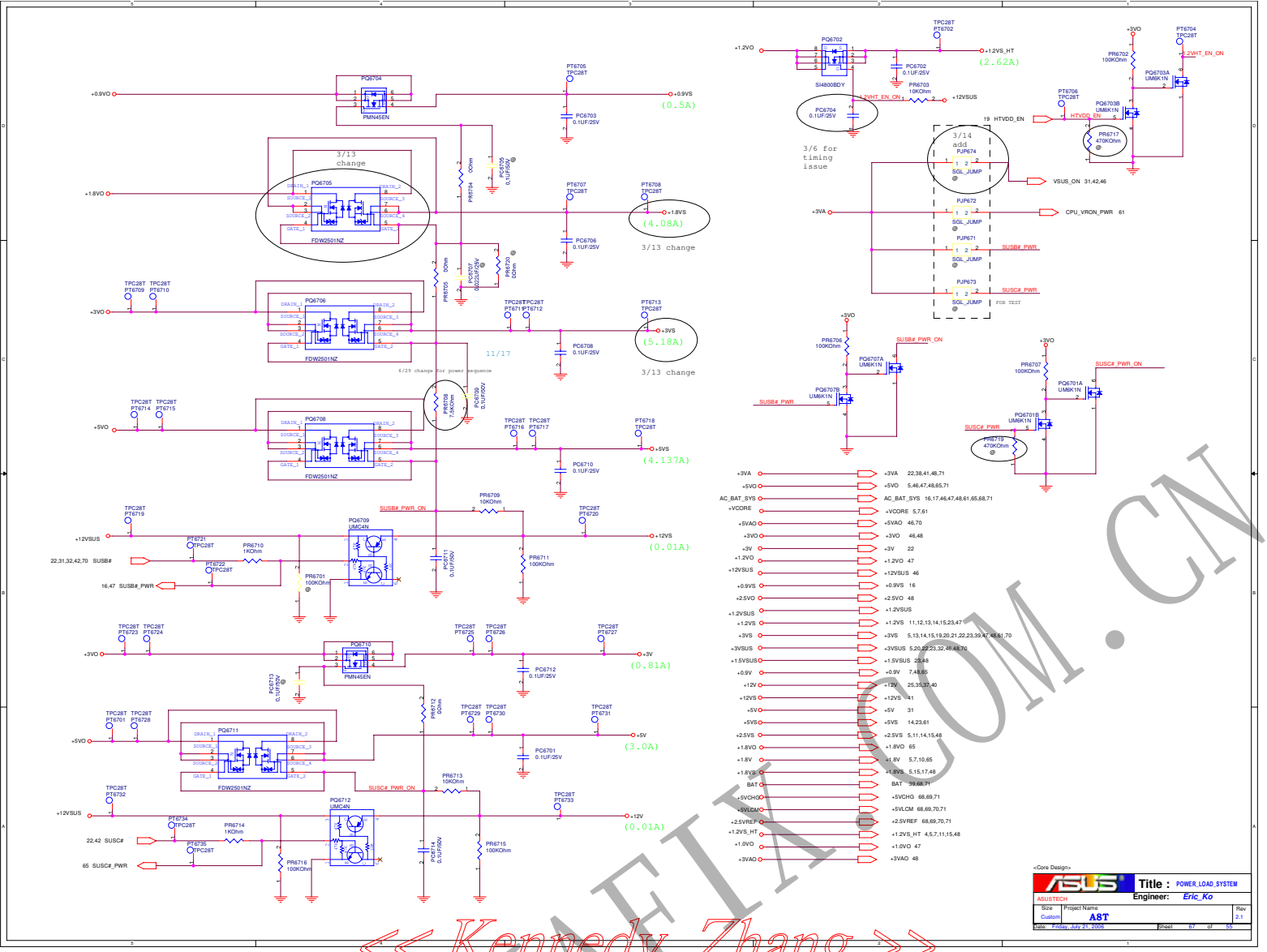
Title : POWER_I/O_DDRII

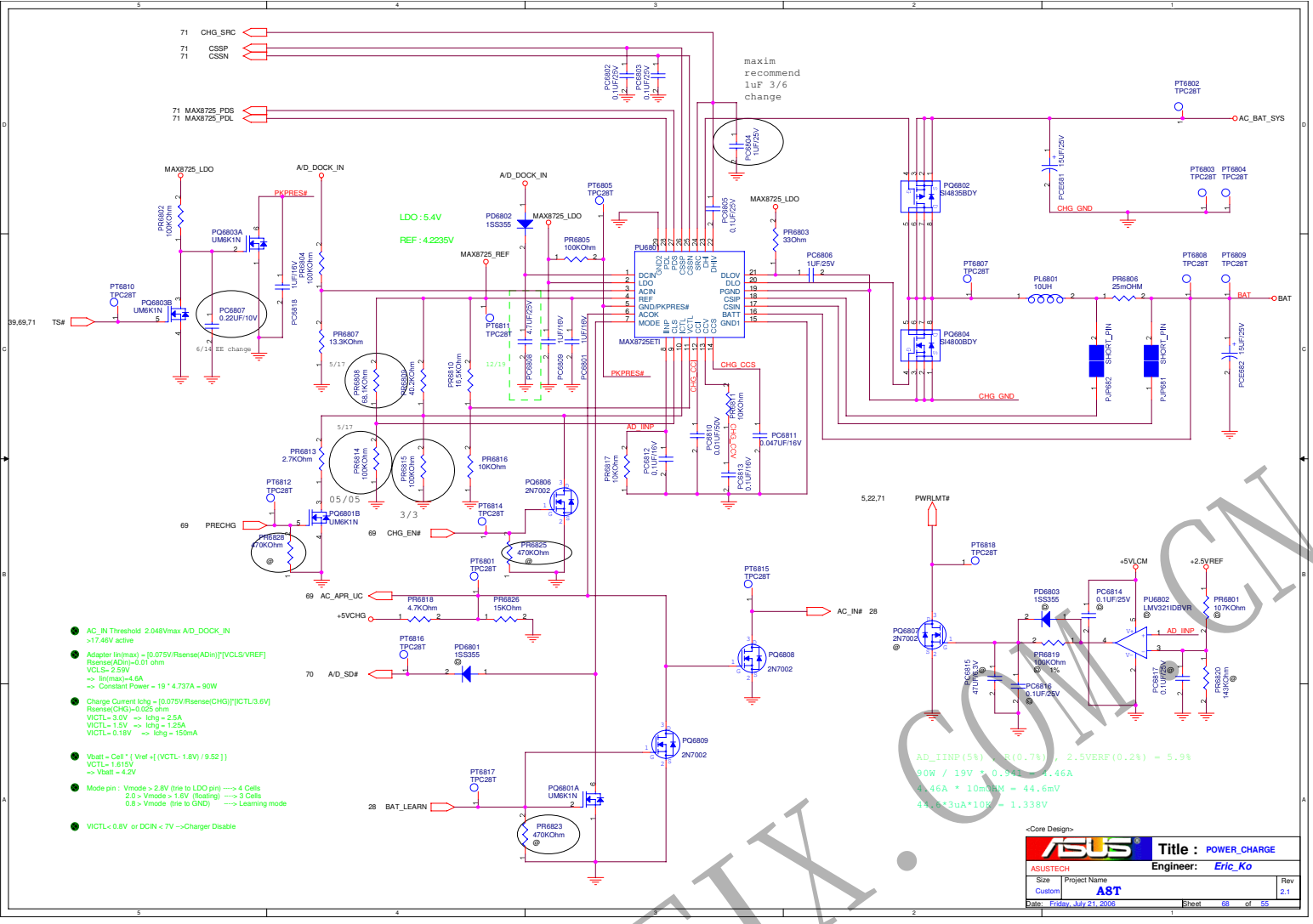
<OrgName>

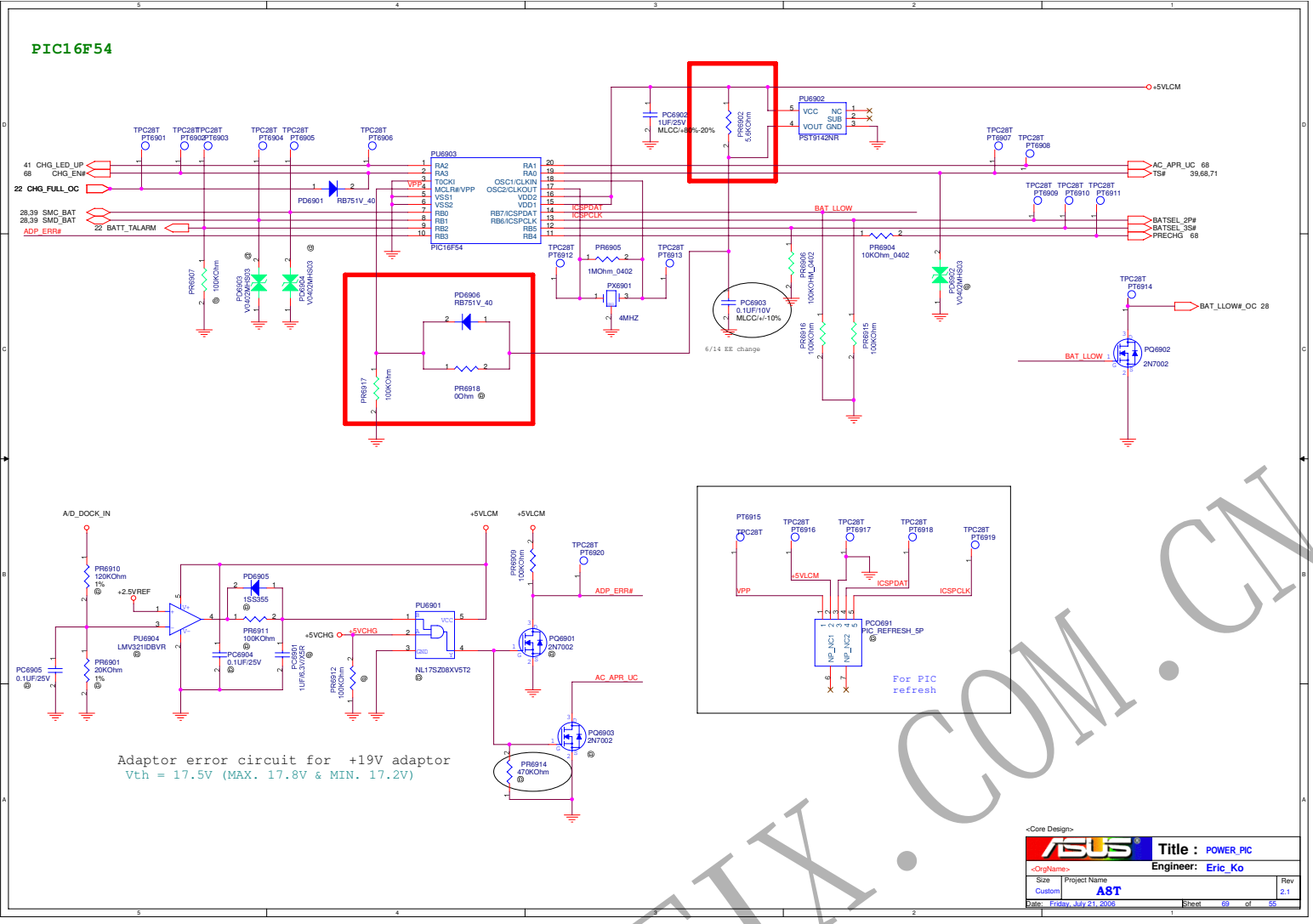
Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

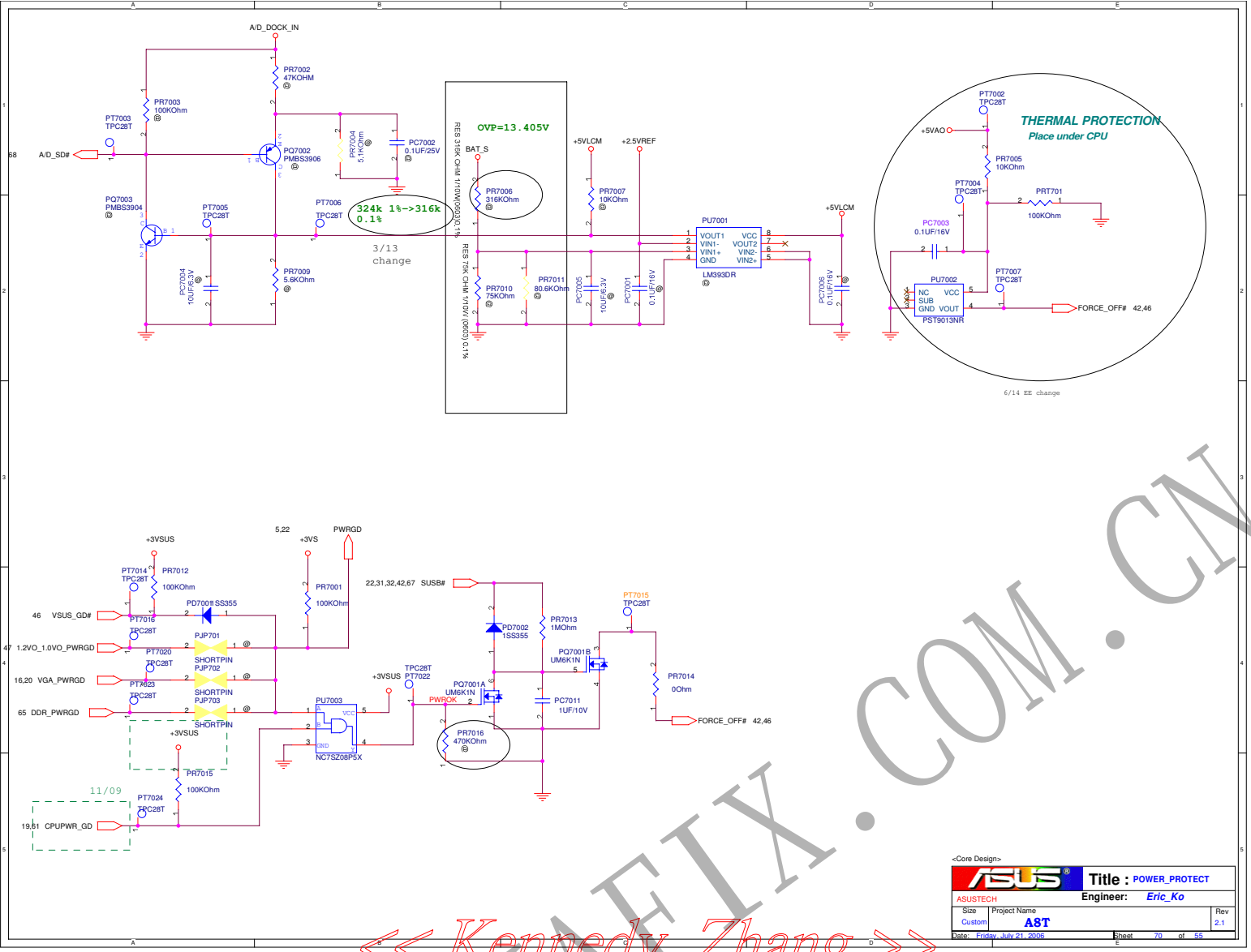
Date: Friday, July 21, 2006 Sheet 65 of 55







<< Kennedy_Zhang >>



<Core Design>

ASUSTECH

Title : POWER_PROTECT

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

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