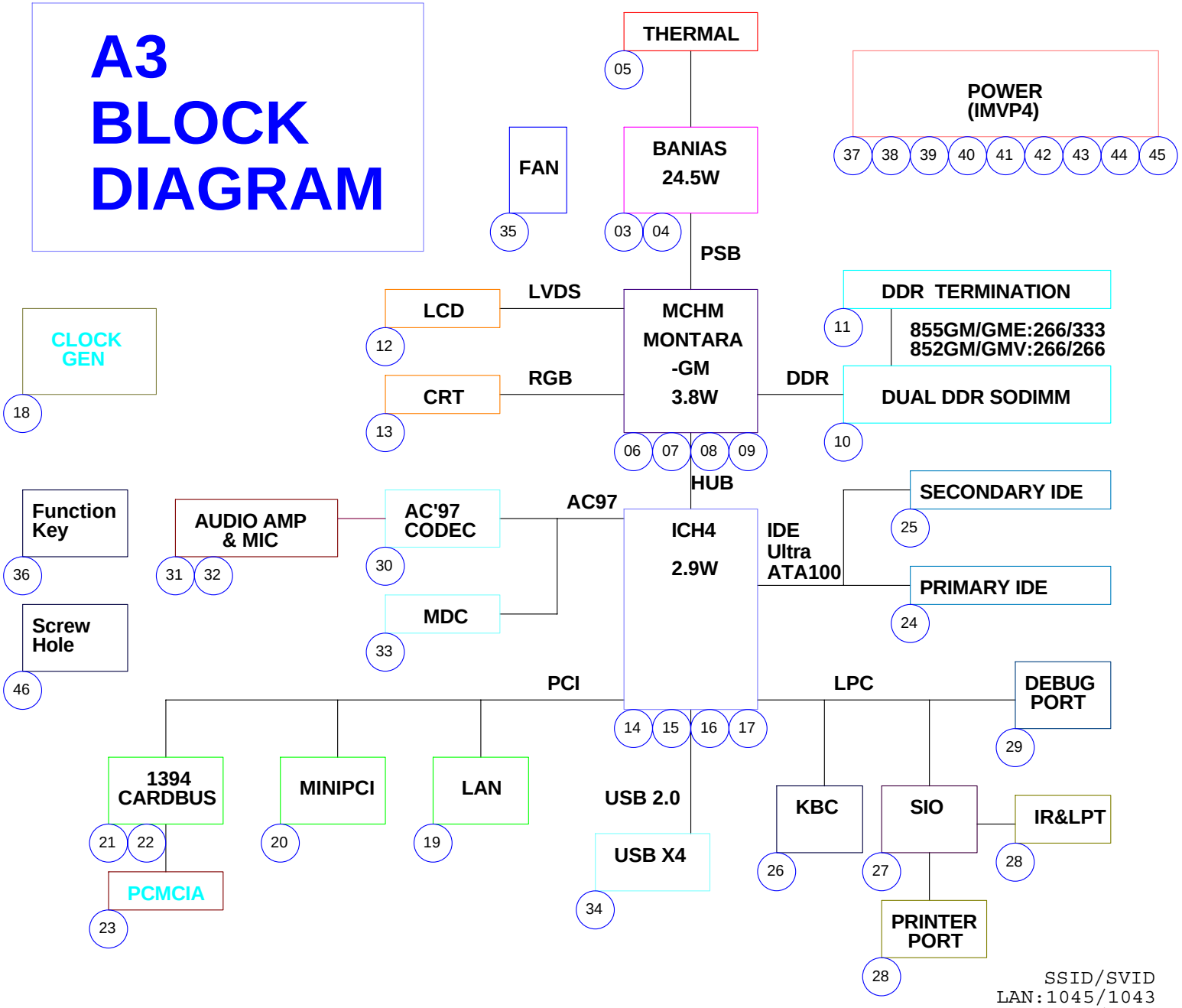
A3 BLOCK DIAGRAM



SSID/SVID
LAN:1045/1043
MDC:1826/1043
CardBUS:1894/1043
1394:1897/1043

FILE LIST

01

ASUSTek COMPUTER INC. NB1

Title : BLOCK DIAGRAM

Engineer: John Hung

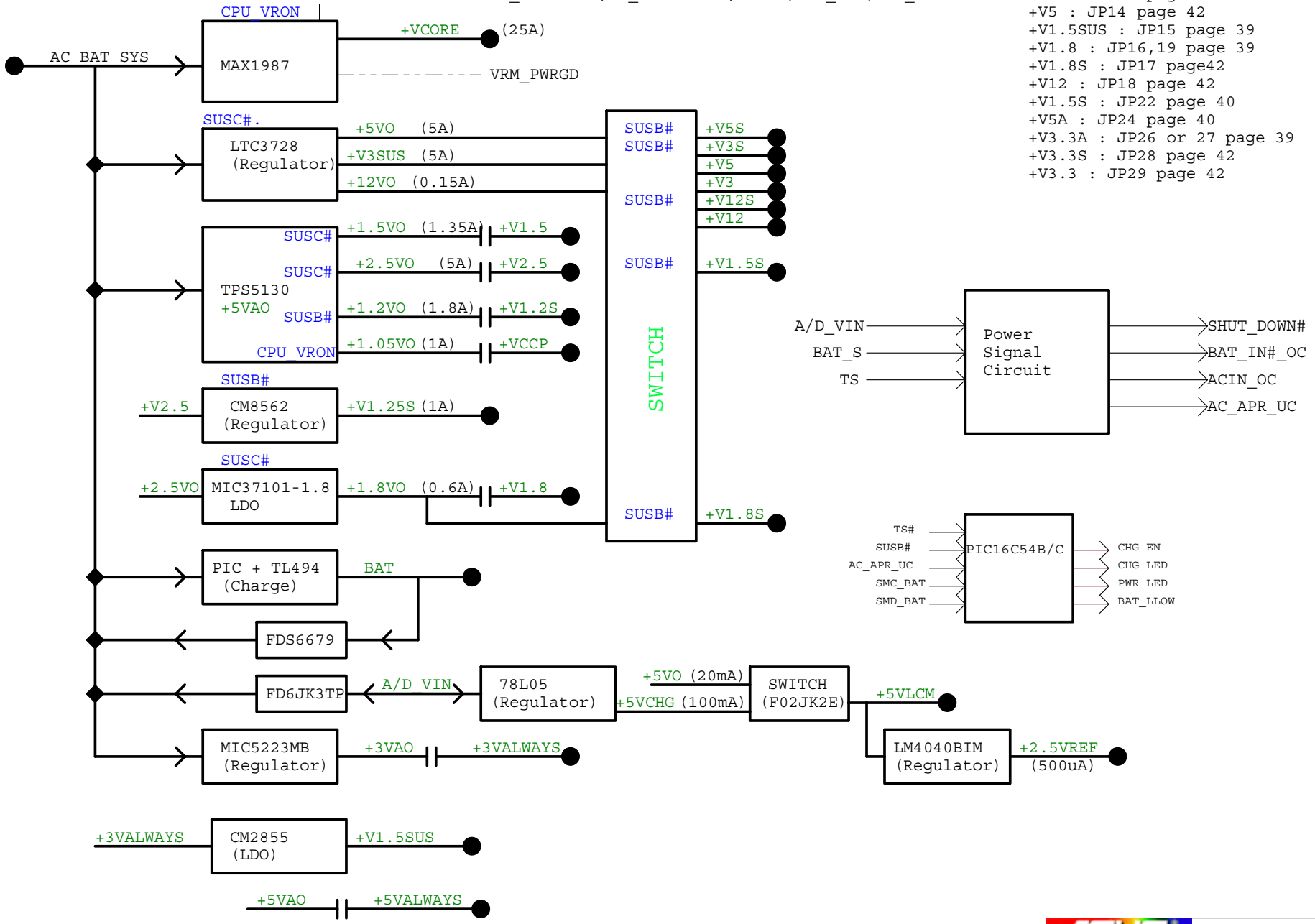
Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 1 of 49

System work voltage
Adapter in : 19.5 ~18.5 V
Battery in : 16.8 ~ 11.6V

VR_VID0-VR_VID5
PM_STPCPU#.,PM_DPRSLPVR.,PCI#.,MCH_OK.,CLK_EN#

+V1.25S : JP4,5 page 39
+V2.5 : JP6 page 40
+V1.2S : JP7 page 40
+VCCP : JP9 page 40
+V5S : JP13 page 42
+V5 : JP14 page 42
+V1.5SUS : JP15 page 39
+V1.8 : JP16,19 page 39
+V1.8S : JP17 page42
+V12 : JP18 page 42
+V1.5S : JP22 page 40
+V5A : JP24 page 40
+V3.3A : JP26 or 27 page 39
+V3.3S : JP28 page 42
+V3.3 : JP29 page 42



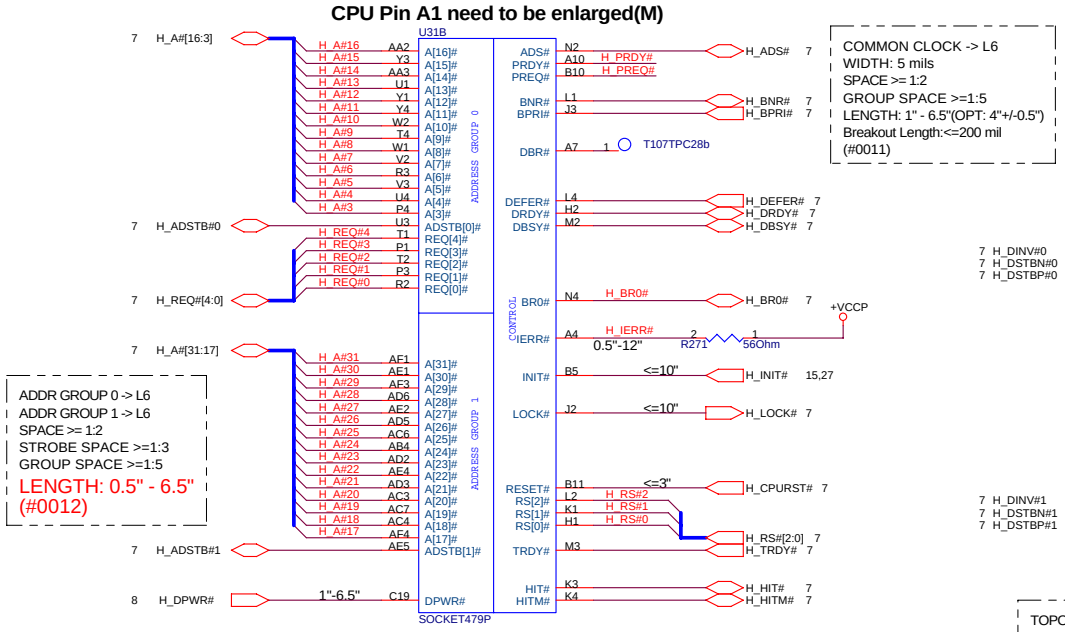
ASUSTek COMPUTER INC. NB1

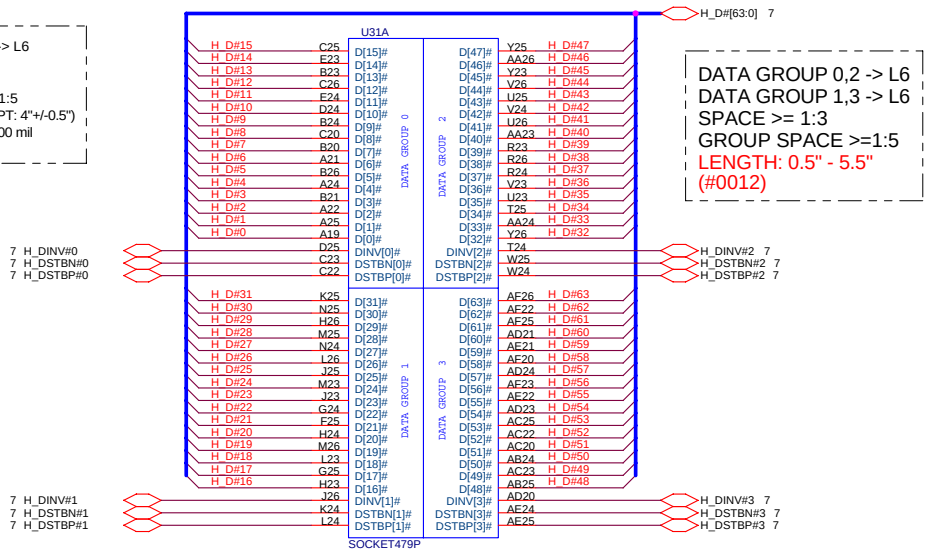
Title : POWER DIAGRAM
Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 2 of 49

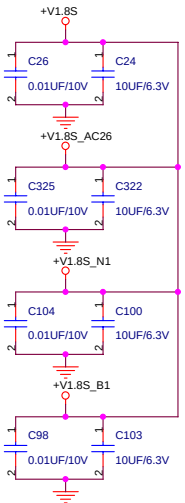
CPU Pin A1 need to be enlarged(M)

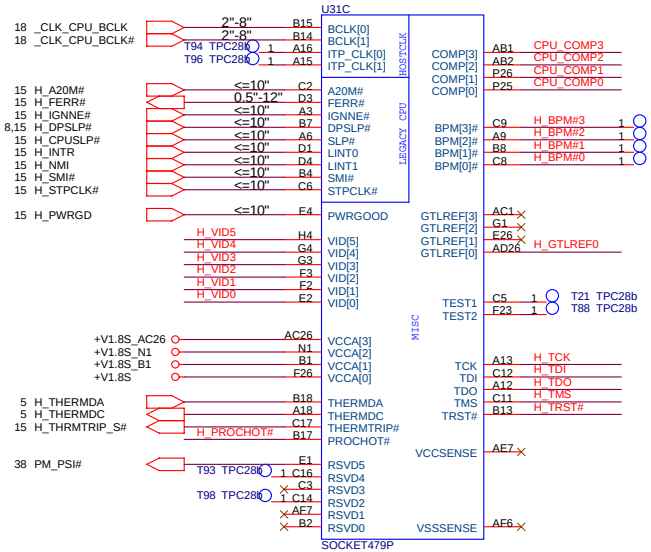


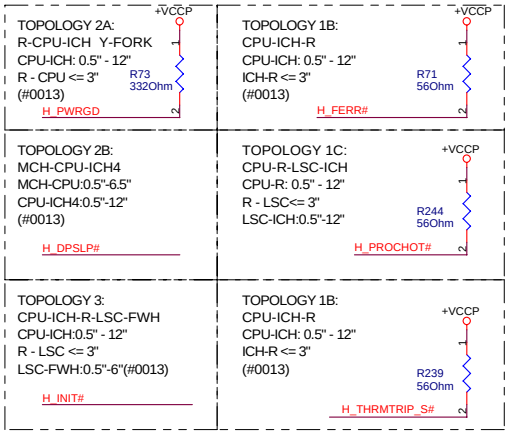


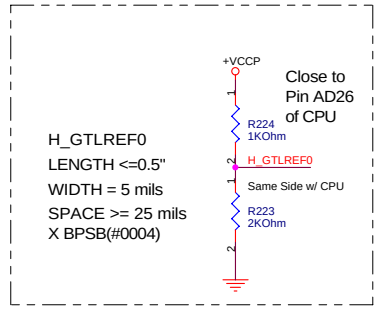
CPU PLL CIRCUITS

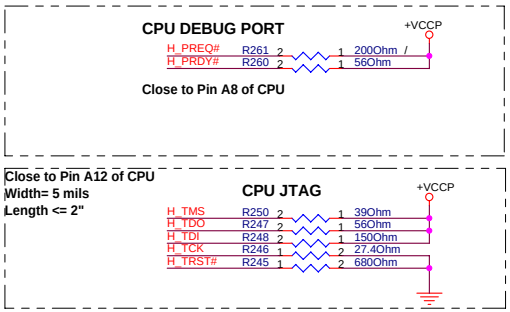
1.71V - 1.89V(+/- 5%)
S0-S1M: 0.3A

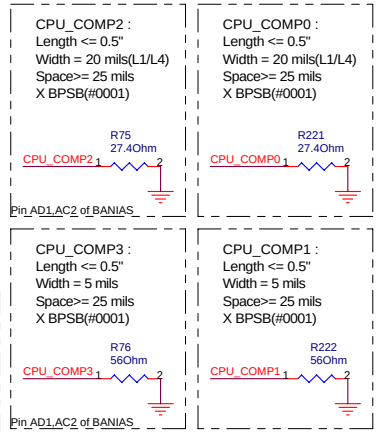










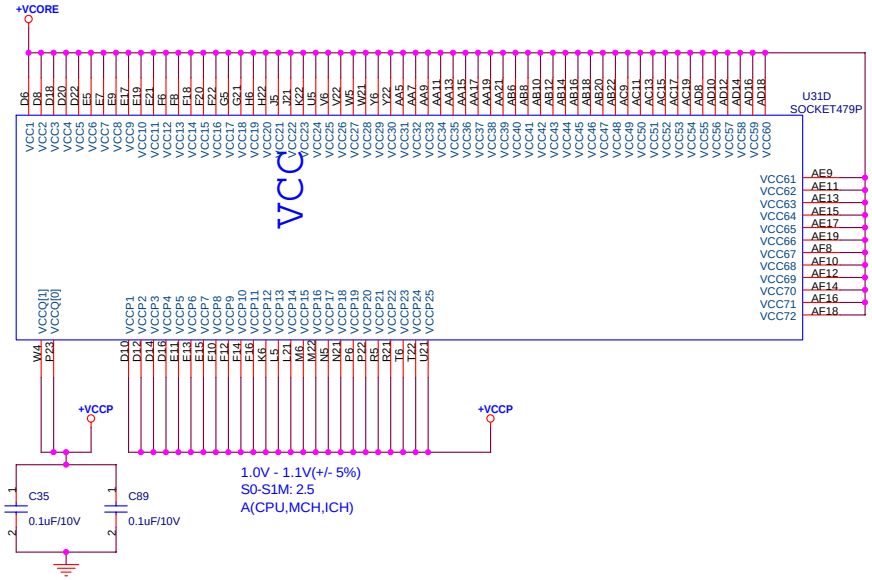


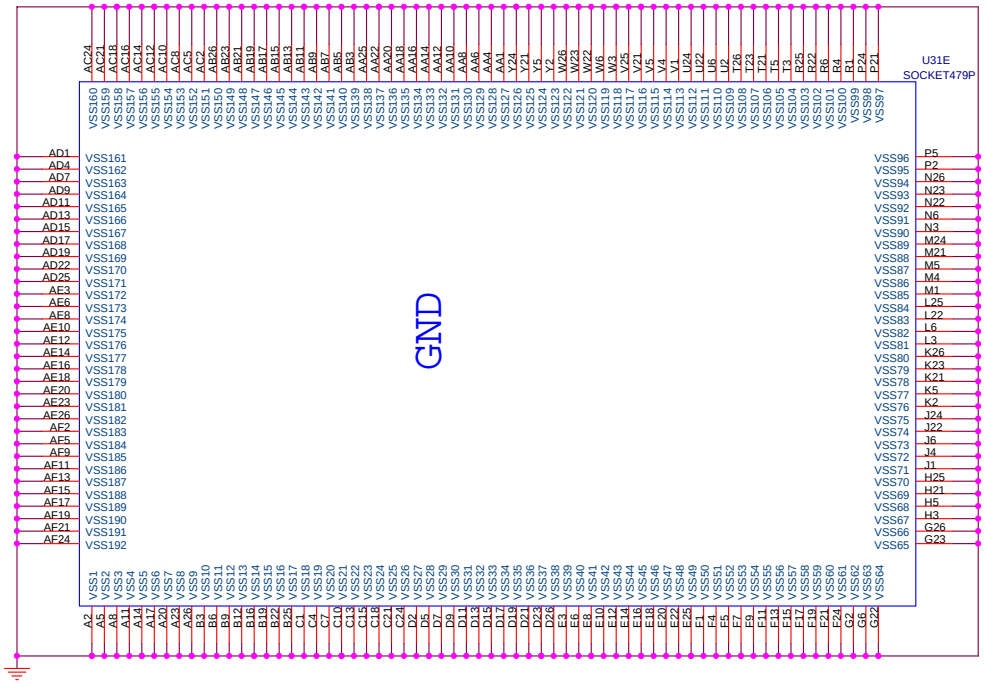
2025

ASUSTek COMPUTER INC. NB1	Title : CPU-BANIAS(HOST)	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 3 of 49	

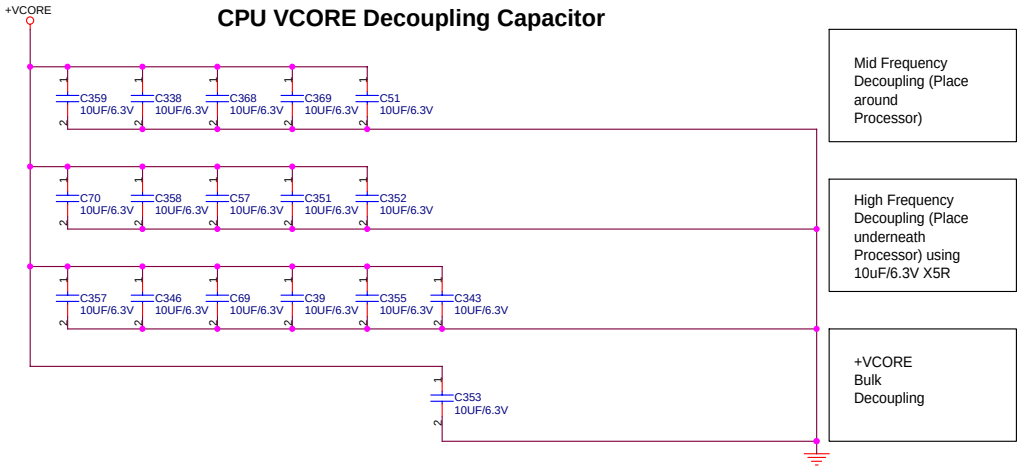
HFM(1.3GHz-1.7GHz): 1.468V
LFM(600MHz): 0.956V

0.745V - 1.356V(+/- 1.5%)
C0: 25 A
C3: 7.59A
C4: 0.9A





CPU VCORE Decoupling Capacitor

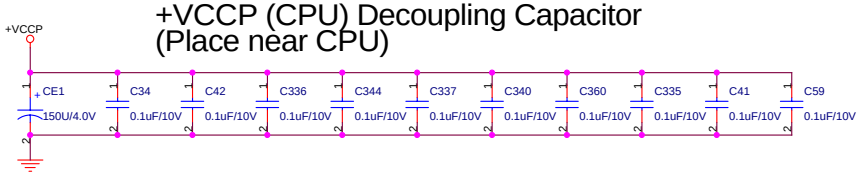


Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

+VCCP (CPU) Decoupling Capacitor (Place near CPU)



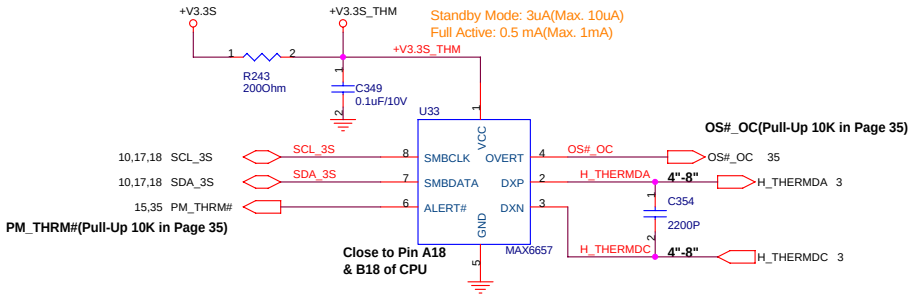
M3N : Four 200 uF are located in IMVP4
A3N : Delete 10uF/6.3V from 35pcs to 17pcs

ASUSTek COMPUTER INC. NB1	Title : CPU-BANIAS(PWR)	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 4 of 49	

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



ASUSTek COMPUTER INC. NB1	Title : THERMAL	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 5 of 49	

3.8W

Thermal Power: ~ 3.8W

LxWxH=37.5x37.5x2.58

U32B

DDR SYSTEM MEMORY

RG82855GM

20A3L

1107

Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.

1.23125V-1.26875V
S0-S1M:Max. 80 mA
S3: 0 mA

(MCH-Sighting041)
M-GM system memory interface generates single pulse CKE events which may cause Intermittent hangs and display corruptions when using Micron and Infineon S0-DIMMs.

Route for COMMAND
1. DDR_AA[12:6],DDR_AA3,DDR_AA0
2. DDR_WE#
3. DDR_RAS#
4. DDR_CAS#
5. DDR_BS0#,DDR_BS1#

Route for CPC
1. DDR_AA[5:4],DDR_AA[2:1]

Route for CPC
1. DDR_AB[5:4],DDR_AB[2:1]

Route for CONTROL
1. DDR_CKE[1:0],DDR_CS[1:0]#

Route for CONTROL
DDR_CKE[3:2],DDR_CS[3:2]#

Route for CLOCK
1. CLK_DDR[2:0],CLK_DDR[2:0]#

Route for CLOCK
CLK_DDR[5:3],CLK_DDR[5:3]#

Title : NB-MCHM(DDR)			
ASUSTek COMPUTER INC. NB1	Engineer: John Hung		
Size: Custom	Project Name: A3N		Rev: 2.0
Date: Friday, April 23, 2004	Sheet 6 of 49		

MCH_HLZCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)

MCH_HLZCOMP

MCH_HYRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)

MCH_HYRCOMP — R235 27.4Ohm

MCH_HXRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)

MCH_HXRCOMP — R226 27.4Ohm

MCH_HYSWING :
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%

MCH_HYSWING — R240 301Ohm — R241 150Ohm — C345 0.1uF/10V
Close to Pin H28

MCH_HXSWING :
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%

MCH_HXSWING — R225 301Ohm — R228 150Ohm — C328 0.1uF/10V
Close to Pin B20

3 H_A#[31:3] — H_A#3 … H_A#31 — P23, T25, T28, R27, U23, U24, R24, U28, V28, U27, T27, V27, U25, V26, Y24, V25, V23, W25, Y25, AA27, W24, W23, W27, Y27, AA28, W28, AB27, Y26, AB28

3 H_REQ#[4:0] — H_REQ#0 … H_REQ#4 — R28, P25, R23, R25, T23

3 H_ADSTB#0 — T26
3 H_ADSTB#1 — AA26

18 _CLK_MCH_BCLK# — AD29
18 _CLK_MCH_BCLK — AE29

MCH_HYRCOMP — H28
MCH_HYSWING — K28
MCH_HXRCOMP — B20
MCH_HXSWING — B18

3 H_DSTBN#0 — J28
3 H_DSTBN#1 — C27
3 H_DSTBN#2 — E22
3 H_DSTBN#3 — D18
3 H_DSTBP#0 — K27
3 H_DSTBP#1 — D26
3 H_DSTBP#2 — E21
3 H_DSTBP#3 — E18
3 H_DINV#0 — J25
3 H_DINV#1 — E25
3 H_DINV#2 — B25
3 H_DINV#3 — G19

3 H_CPURST# — F15

MCH_HDVREF — K21
J21
MCH_HCCVREF — J17
MCH_HAVREF — Y28
Y22

14 HUB_PD[10:0] — HUB_PD0 … HUB_PD10 — <=6" U7, U4, U3, V3, W2, W6, V6, W7, T3, V5, V4

14 HUB_PSTRB — W3
14 HUB_PSTRB# — V2
MCH_HLZCOMP — T2
U2
W1

+V1.2S_GMCH_HI — R249 27.4Ohm

+VCCP — R49 56Ohm / H_CPURST#

+V1.2S_GMCH_HI — R251 49.9Ohm — 0.8V +/- 2% — R253 100Ohm — HUB_VSWING_MCH — C356 0.1uF/10V

0.343V- 0.357V(Typ. 0.35V)
HUB_VREF_MCH — C362 0.01UF/10V — C363 0.1uF/10V — R262 100Ohm
+V1.2S_GMCH_HI — R252 240Ohm

U32A
LXWxH=37.5x37.5x2.58
HOST
HUB I/F
RG82855GM
20A3L
2025

HA#3 … HA#31
HD#0 … HD#63

H_D#[63:0] 3

H_ADS# 3
H_TRDY# 3
H_DRDY# 3
H_DEFER# 3
H_HITM# 3
H_HIT# 3
H_LOCK# 3
H_BR0# 3
H_BNR# 3
H_BPRI# 3
H_DBSY# 3
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] 3

MCH_HAVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)

+VCCP — 2/3(+VCCP) +/- 2% — R67 49.9Ohm — MCH_HAVREF — C81 0.1uF/10V — C79 1uF/6.3V — R66 100Ohm

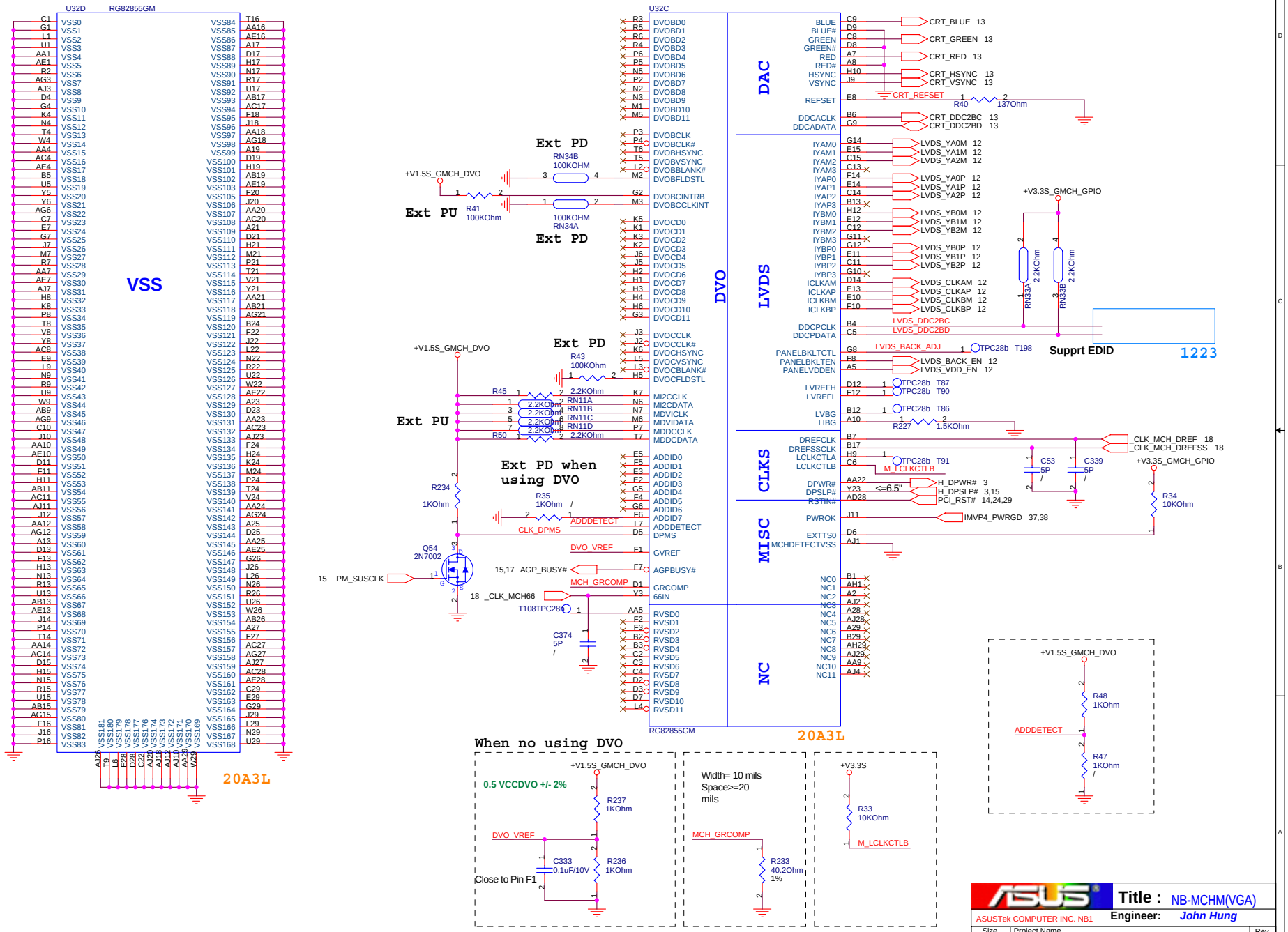
MCH_HCCVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)

+VCCP — 2/3(+VCCP) +/- 2% — R270 49.9Ohm — MCH_HCCVREF — C376 0.1uF/10V — C377 1uF/6.3V — R269 100Ohm

MCH_HDVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)

+VCCP — 2/3(+VCCP) +/- 2% — R44 49.9Ohm — MCH_HDVREF — C48 0.1uF/10V — C44 0.1uF/10V — C46 0.1uF/10V — C52 1uF/6.3V — R46 100Ohm

ASUSTek COMPUTER INC. NB1
Title : NB-MCHM(HOST)
Engineer: John Hung
Size: Custom | Project Name: A3N | Rev: 2.0
Date: Friday, April 23, 2004 | Sheet 7 of 49



ASUSTek COMPUTER INC. NB1	Title : NB-MCHM(VGA)		
	Engineer: John Hung		
Size: Custom	Project Name: A3N		Rev: 2.0
Date: Friday, April 23, 2004	Sheet 8 of 49		

(MCH-Sighting041)
The core supply (1.2V) should be powered up a minimum of 1ms before the DVO and GPIO IO (1.5V and 3.3V) voltage rails.

LxWxH=37.5x37.5x2.58

U32E

RG82855GM

20A3L

POWER

+V1.2S 1.14V - 1.26V(+/- 5%) S0-S1M:Max. 1.4 A

+V1.2S_GMCH_CORE

+V1.2S_GMCH_HI 1.14V - 1.26V(+/- 5%) S0-S1M:Max. 90 mA

+V1.2S_GMCH_DPLLA 1.14V - 1.26V(+/- 5%) S0-S1M: 0.3 A

+V1.2S_GMCH_DPLLB 1.14V - 1.26V(+/- 5%) S0-S1M: 0.3 A

+V1.5S 1.425V - 1.575V(+/- 5%) S0-S1M: Max. 90 mA

+V1.5S_GMCH_DVO 1.425V - 1.575V(+/- 5%)

+V1.5S_GMCH_ADAC 1.425V - 1.575V(+/- 5%)

+V1.5S_GMCH_ALVDS 1.425V - 1.575V(+/- 5%) S0-S1M: Max. 70 mA

+V1.5S_GMCH_DLVDS 1.425V - 1.575V(+/- 5%) S0-S1M: Max. 70 mA

+V2.5 2.375V - 2.625V(+/- 5%) S0-S3: Max. 50 mA

+V2.5_GMCH_TXLVDS

+V3.3S

+V3.3S_GMCH_GPIO 3.135V - 3.465V(+/- 5%)

+VCCP 1.0V - 1.1V(+/- 5%) S0-S1M: 2.5 A(CPU,MCH,ICH) S0-S1M: Max. 0.72A

M_PWR_VTTF0 M_PWR_VTTF1 M_PWR_VTTF2 M_PWR_VTTF3 M_PWR_VTTF4 2.375V - 2.625V(+/- 5%) S0-S1M: Max. 2.07A S3: Max. 25 mA

+V2.5_GMCH_SM +V2.5

+V2.5_GMCHQSM +V2.5_GMCH_SM

+V1.2S_GMCH_ASM L42 +V1.2S_GMCH_HI 1.14V - 1.26V(+/- 5%) S0-S1M: 0.4 A

Caution: L2 be placed between Pin U9 ans U13

Caution: There is no vias between Pin B8 and C99,C100 (It means C99,C100 must be in same layer with MCHM)

Caution: There is no vias between Pin B11 and C106,C107 (It means C106, C107 must be in same layer with MCHM)

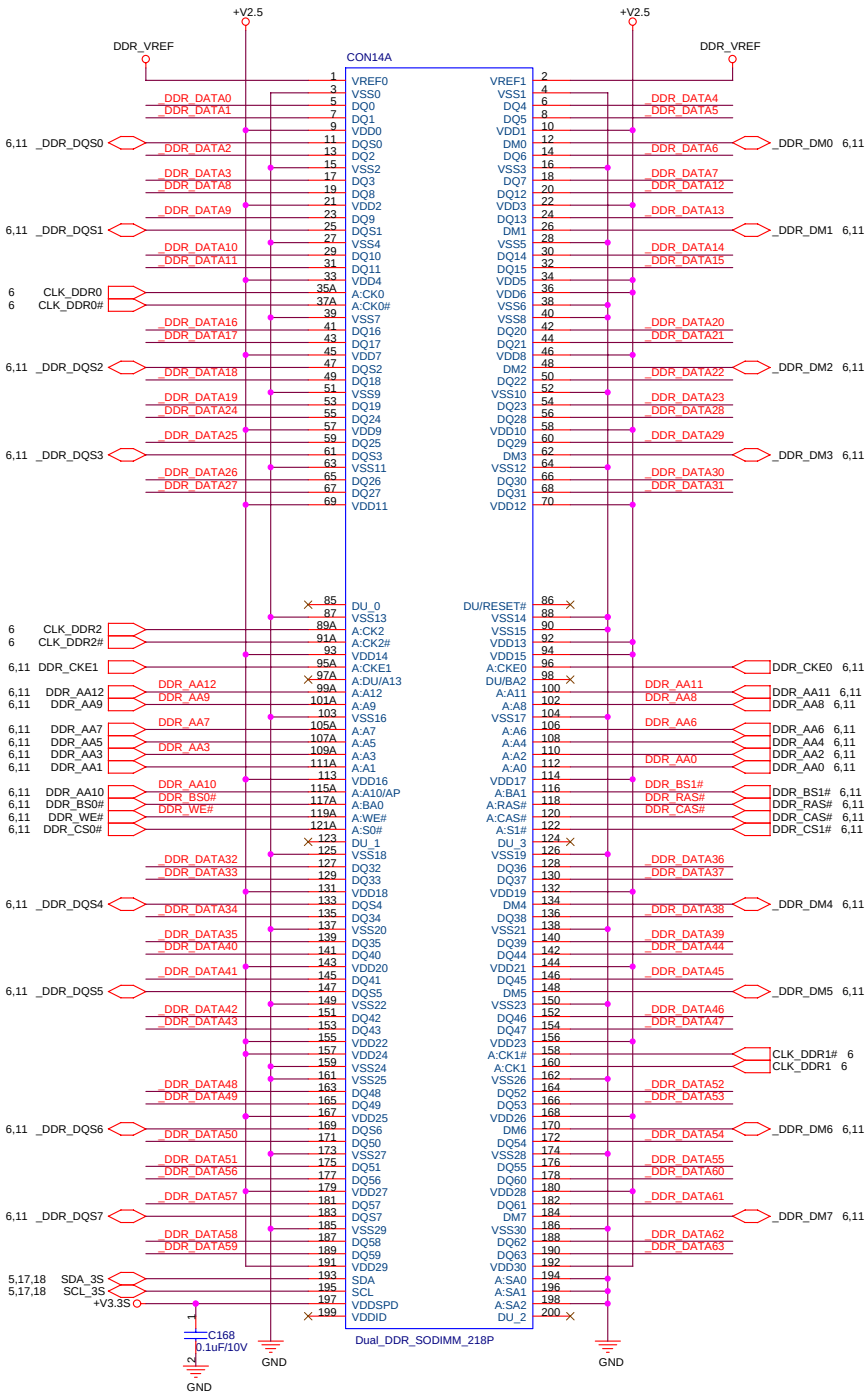
2025

2025

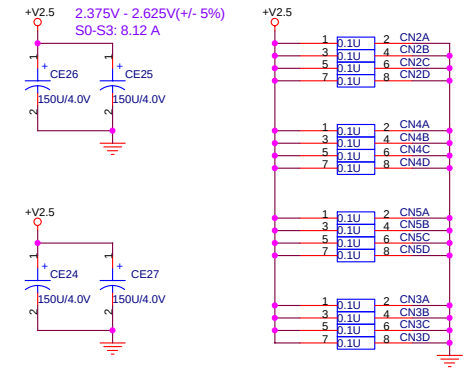
VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB
855GME: 1.35V
855GM: 1.2V
852GM,GME,GMV: 1.5V

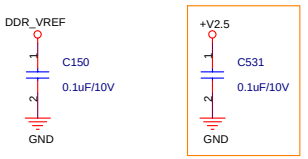
Title :	NB-MCHM(PWR)		
ASUSTek COMPUTER INC. NB1	Engineer:	John Hung	
Size: Custom	Project Name: A3N		Rev: 2.0
Date: Friday, April 23, 2004	Sheet 9 of 49		

6,11 _DDR_DATA[63:0]

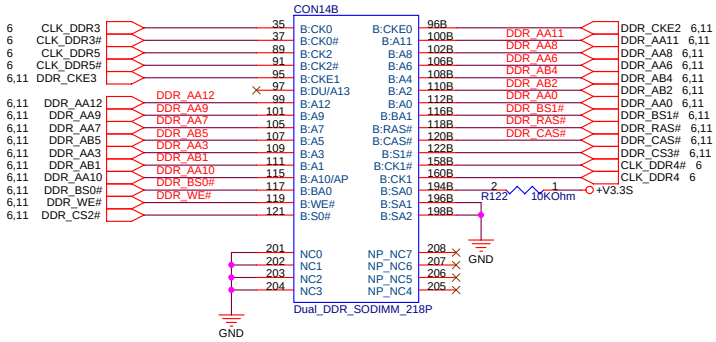


FOR +V2.5 DECOUPLING





2024
EMI : Close to DDR socket power plane of +V2.5



ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 10 of 49	

Title : DUAL DDR SODIMM

DDR TERMINATION

6,10 _DDR_DATA[63:0]
6,10 _DDR_DM[8:0]
6,10 _DDR_DQS[8:0]
6,10 DDR_AA[12:0]
6,10 DDR_AB[2:1]
6,10 DDR_AB[5:4]

+V1.25S

DDR_DATA0 6 56Ohm 11 RN58F
DDR_DATA4 8 56Ohm 9 RN58H
DDR_DATA1 5 56Ohm 12 RN58E
DDR_DATA5 7 56Ohm 10 RN58G
DDR_DQS0 4 56Ohm 13 RN58D
DDR_DM0 3 56Ohm 14 RN58C
DDR_DATA6 8 56Ohm 9 RN57H
DDR_DATA2 2 56Ohm 15 RN58B

DDR_DATA3 1 56Ohm 16 RN58A
DDR_DATA7 7 56Ohm 10 RN57G
DDR_DATA8 6 56Ohm 11 RN57F
DDR_DATA12 5 56Ohm 12 RN57E
DDR_DATA9 3 56Ohm 14 RN57C
DDR_DATA13 4 56Ohm 13 RN57D
DDR_DQS1 2 56Ohm 15 RN57B
DDR_DM1 1 56Ohm 16 RN57A

DDR_DATA10 6 56Ohm 11 RN56F
DDR_DATA14 8 56Ohm 9 RN56H
DDR_DATA11 5 56Ohm 12 RN56E
DDR_DATA15 7 56Ohm 10 RN56G
DDR_DATA16 4 56Ohm 13 RN56D
DDR_DATA20 3 56Ohm 14 RN56C
DDR_DATA17 2 56Ohm 15 RN56B
DDR_DATA21 1 56Ohm 16 RN56A

DDR_DQS2 8 56Ohm 9 RN55H
DDR_DM2 7 56Ohm 10 RN55G
DDR_DATA18 5 56Ohm 12 RN55E
DDR_DATA22 6 56Ohm 11 RN55F
DDR_DATA19 4 56Ohm 13 RN55D
DDR_DATA23 3 56Ohm 14 RN55C
DDR_DATA24 2 56Ohm 15 RN55B
DDR_DATA28 8 56Ohm 9 RN54H

DDR_DATA25 1 56Ohm 16 RN55A
DDR_DATA29 7 56Ohm 10 RN54G
DDR_DQS3 6 56Ohm 11 RN54F
DDR_DM3 5 56Ohm 12 RN54E
DDR_DATA26 4 56Ohm 13 RN54D
DDR_DATA30 3 56Ohm 14 RN54C
DDR_DATA27 1 56Ohm 16 RN54A
DDR_DATA31 2 56Ohm 15 RN54B

6,10 DDR_CKE1
6,10 DDR_CKE2
6,10 DDR_CKE0
6,10 DDR_CKE3

DDR_CKE1 6 56Ohm 11 RN53F
DDR_CKE2 5 56Ohm 12 RN63E
DDR_CKE0 6 56Ohm 11 RN63F
DDR_CKE3 1 56Ohm 16 RN63A
DDR_AA12 8 56Ohm 9 RN53H
DDR_AA11 3 56Ohm 14 RN63C
DDR_AA9 7 56Ohm 10 RN53G
DDR_AA8 4 56Ohm 13 RN63D

DDR_AA7 5 56Ohm 12 RN53E
DDR_AA6 7 56Ohm 10 RN62G
DDR_AA5 2 56Ohm 15 RN63B
DDR_AB5 4 56Ohm 13 RN53D
DDR_AA4 7 56Ohm 10 RN63G
DDR_AB4 4 56Ohm 13 RN52D
DDR_AA3 3 56Ohm 14 RN53C
DDR_AA2 8 56Ohm 9 RN63H

+V1.25S

DDR_AB2 1 56Ohm 16 RN53A
DDR_AA1 8 56Ohm 9 RN62H
DDR_AB1 2 56Ohm 15 RN53B
DDR_AA0 5 56Ohm 12 RN52E
DDR_AA10 4 56Ohm 13 RN62D
DDR_BS1# 7 56Ohm 10 RN52G
DDR_BS0# 3 56Ohm 14 RN62C
DDR_RAS# 6 56Ohm 11 RN52F

6,10 DDR_BS1#
6,10 DDR_BS0#
6,10 DDR_RAS#

DDR_WE# 2 56Ohm 15 RN62B
DDR_CAS# 5 56Ohm 12 RN62E
DDR_CS0# 6 56Ohm 11 RN62F
DDR_CS2# 8 56Ohm 9 RN52H
DDR_CS1# 3 56Ohm 14 RN52C
DDR_CS3# 1 56Ohm 16 RN62A
DDR_DATA32 8 56Ohm 9 RN61H
DDR_DATA36 2 56Ohm 15 RN52B

6,10 DDR_WE#
6,10 DDR_CAS#
6,10 DDR_CS0#
6,10 DDR_CS2#
6,10 DDR_CS1#
6,10 DDR_CS3#

DDR_DATA33 7 56Ohm 10 RN61G
DDR_DATA37 1 56Ohm 16 RN52A
DDR_DQS4 6 56Ohm 11 RN61F
DDR_DM4 5 56Ohm 12 RN61E
DDR_DATA34 4 56Ohm 13 RN61D
DDR_DATA38 3 56Ohm 14 RN61C
DDR_DATA35 1 56Ohm 16 RN61A
DDR_DATA39 2 56Ohm 15 RN61B

DDR_DATA40 6 56Ohm 11 RN51F
DDR_DATA44 7 56Ohm 10 RN51G
DDR_DATA41 5 56Ohm 12 RN51E
DDR_DATA45 8 56Ohm 9 RN51H
DDR_DQS5 4 56Ohm 13 RN51D
DDR_DM5 3 56Ohm 14 RN51C
DDR_DATA42 2 56Ohm 15 RN51B
DDR_DATA46 1 56Ohm 16 RN51A

DDR_DATA43 8 56Ohm 9 RN60H
DDR_DATA47 7 56Ohm 10 RN60G
DDR_DATA48 6 56Ohm 11 RN60F
DDR_DATA52 4 56Ohm 13 RN60D
DDR_DATA49 5 56Ohm 12 RN60E
DDR_DATA53 3 56Ohm 14 RN60C
DDR_DQS6 2 56Ohm 15 RN60B
DDR_DM6 1 56Ohm 16 RN60A

DDR_DATA50 8 56Ohm 9 RN50H
DDR_DATA54 6 56Ohm 11 RN50F
DDR_DATA51 7 56Ohm 10 RN50G
DDR_DATA55 5 56Ohm 12 RN50E
DDR_DATA56 4 56Ohm 13 RN50D
DDR_DATA60 3 56Ohm 14 RN50C
DDR_DATA57 2 56Ohm 15 RN50B
DDR_DATA61 1 56Ohm 16 RN50A

DDR_DQS7 6 56Ohm 11 RN59F
DDR_DM7 5 56Ohm 12 RN59E
DDR_DATA58 2 56Ohm 15 RN59B
DDR_DATA62 4 56Ohm 13 RN59D
DDR_DATA59 1 56Ohm 16 RN59A
DDR_DATA63 3 56Ohm 14 RN59C
7 56Ohm 10 RN59G
8 56Ohm 9 RN59H

FOR +V1.25S DECOUPLING

+V1.25S

1 0.1U 2 CN24A
5 0.1U 6 CN24C
1 0.1U 2 CN19A
5 0.1U 6 CN19C
1 0.1U 2 CN22A
5 0.1U 6 CN22C
1 0.1U 2 CN23A
5 0.1U 6 CN23C
1 0.1U 2 CN27A
5 0.1U 6 CN27C
1 0.1U 2 CN26A
5 0.1U 6 CN26C
1 0.1U 2 CN25A
5 0.1U 6 CN25C
1 0.1U 2 CN20A
5 0.1U 6 CN20C
1 0.1U 2 CN28A
5 0.1U 6 CN28C
1 0.1U 2 CN21A
5 0.1U 6 CN21C
1 0.1U 2 CN16A
5 0.1U 6 CN16C
1 0.1U 2 CN17A
5 0.1U 6 CN17C
1 0.1U 2 CN18A
5 0.1U 6 CN18C
1 0.1U 2 CN15A
5 0.1U 6 CN15C
1 0.1U 2 CN14A
5 0.1U 6 CN14C

+V1.25S

3 0.1U 4 CN24B
7 0.1U 8 CN24D
3 0.1U 4 CN19B
7 0.1U 8 CN19D
3 0.1U 4 CN22B
7 0.1U 8 CN22D
3 0.1U 4 CN23B
7 0.1U 8 CN23D
3 0.1U 4 CN27B
7 0.1U 8 CN27D
3 0.1U 4 CN26B
7 0.1U 8 CN26D
3 0.1U 4 CN25B
7 0.1U 8 CN25D
3 0.1U 4 CN20B
7 0.1U 8 CN20D
3 0.1U 4 CN28B
7 0.1U 8 CN28D
3 0.1U 4 CN21B
7 0.1U 8 CN21D
3 0.1U 4 CN16B
7 0.1U 8 CN16D
3 0.1U 4 CN17B
7 0.1U 8 CN17D
3 0.1U 4 CN18B
7 0.1U 8 CN18D
3 0.1U 4 CN15B
7 0.1U 8 CN15D
3 0.1U 4 CN14B
7 0.1U 8 CN14D

ASUSTek COMPUTER INC. NB1

Title : DDR TERMINATION

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 11 of 49

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output D/A signal (adjust voltage level) to adjust Back light.

A3N use D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

USB PORT 3 for CAMERA

USB PORT 5 for WLAN

LCD	CABLE ID:	PID3	PID2	PID1	PID0
14.1	XGA	1	1	1	1
15.1	XGA	1	1	0	1
15.1	SXGA+	1	0	1	1

RN86A,B: page 20

LCD Power

SI3865: US$0.22

3-3.6V
S0-S1M:410 mA(500 mA Max.)

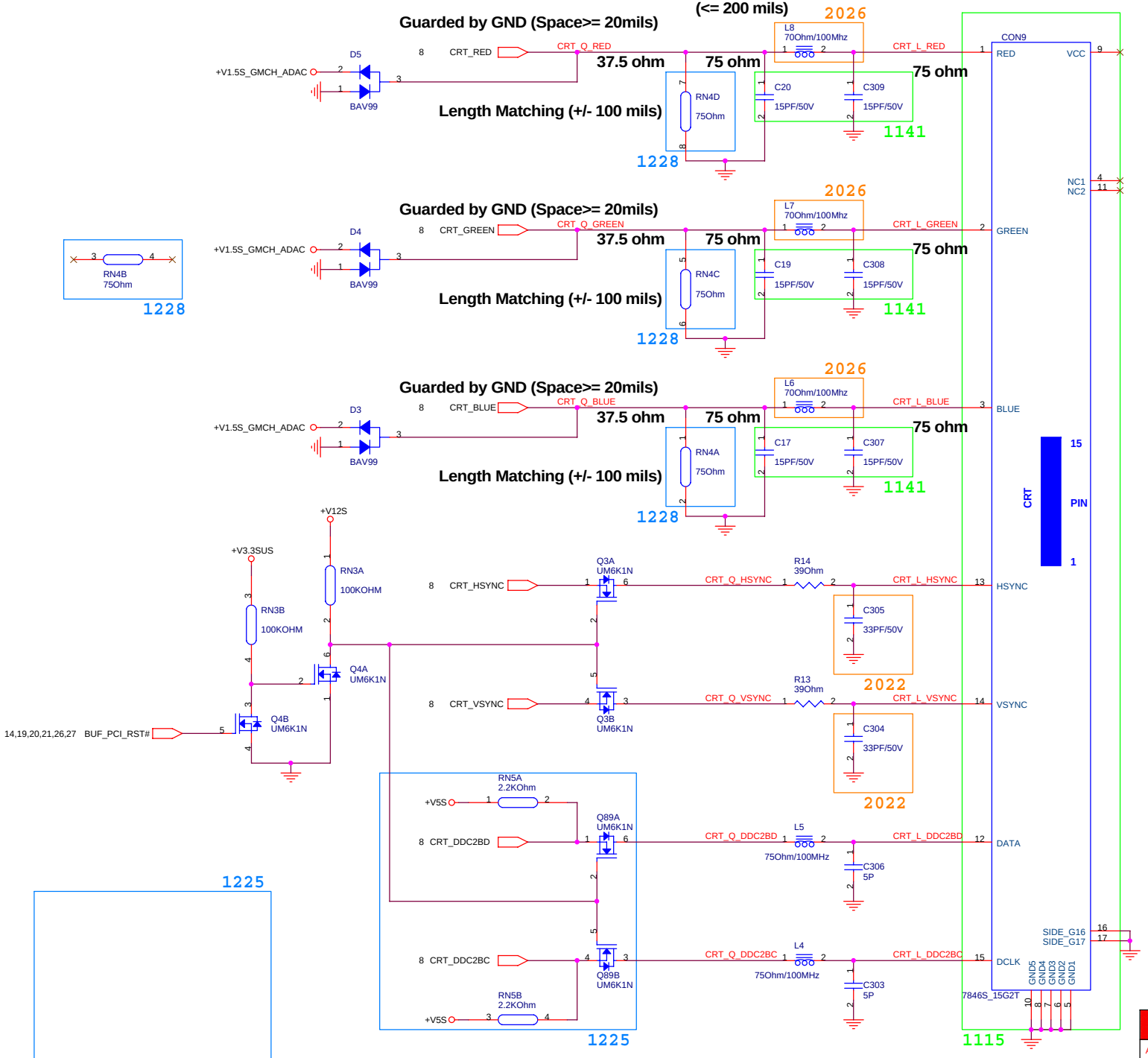
Caution:
Must tune R369 & C270 to meet Panel Spec

Title :	LVDS & BACKLIGHT
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 12 of 49

Place Pi-Filter close to CRT
(<= 200 mils)

Guarded by GND (Space>= 20mils)

Length Matching (+/- 100 mils)



ASUSTek COMPUTER INC. NB1	Title : CRT CONNECTOR	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 13 of 49	

Use Daisy-Chain Topology

PCI_REQ#	PCI_REQ#?
CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL	PCI_AD?
CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

LxWxH=31x31x2.38

U20A

19,20,21,22 PCI_AD[31:0]

PCI_AD0 H5 AD0
PCI_AD1 J3 AD1
PCI_AD2 H3 AD2
PCI_AD3 K1 AD3
PCI_AD4 G5 AD4
PCI_AD5 J4 AD5
PCI_AD6 H4 AD6
PCI_AD7 J5 AD7
PCI_AD8 K2 AD8
PCI_AD9 G2 AD9
PCI_AD10 L1 AD10
PCI_AD11 G4 AD11
PCI_AD12 L2 AD12
PCI_AD13 H2 AD13
PCI_AD14 L3 AD14
PCI_AD15 F5 AD15
PCI_AD16 F4 AD16
PCI_AD17 N1 AD17
PCI_AD18 E5 AD18
PCI_AD19 N2 AD19
PCI_AD20 E3 AD20
PCI_AD21 N3 AD21
PCI_AD22 E4 AD22
PCI_AD23 M5 AD23
PCI_AD24 E2 AD24
PCI_AD25 P1 AD25
PCI_AD26 E1 AD26
PCI_AD27 P2 AD27
PCI_AD28 D3 AD28
PCI_AD29 R1 AD29
PCI_AD30 D2 AD30
PCI_AD31 P4 AD31

HI0 L19 HUB_PD0 <=6"
HI1 L20 HUB_PD1 <=6"
HI2 M19 HUB_PD2 <=6"
HI3 M21 HUB_PD3 <=6"
HI4 P19 HUB_PD4 <=6"
HI5 R19 HUB_PD5 <=6"
HI6 T20 HUB_PD6 <=6"
HI7 R20 HUB_PD7 <=6"
HI8 P23 HUB_PD8 <=8"
HI9 L22 HUB_PD9 <=8"
HI10 N22 HUB_PD10 <=8"
HI11 K21 HUB_PD11

HUB_PD[10:0] 7

R314 56Ohm

HI_STB#/HI_STBF N20 HUB_PSTRB# 7
HI_STB/HI_STBS P21 HUB_PSTRB 7
HICOMP R23 HUB_RCOMP_ICH4
HI_VSWING R22 HUB_VSWING_ICH4

EE_CS D10
EE_DIN D11
EE_DOUT A8
EE_SHCLK C12

LAD0/FWH0 T2 LPC_AD0 20,26,27
LAD1/FWH1 R4 LPC_AD1 20,26,27
LAD2/FWH2 T4 LPC_AD2 20,26,27
LAD3/FWH3 U2 LPC_AD3 20,26,27
LFRAME#/FWH4 T5 LPC_FRAME# 20,26,27
LDRQ1# U4 T48 TPC28b
LDRQ0# U3 LPC_DRQ#0 27

19,20,21 PCI_C/BE#0 J2 C/BE0#
19,20,21 PCI_C/BE#1 K4 C/BE1#
19,20,21 PCI_C/BE#2 M4 C/BE2#
19,20,21 PCI_C/BE#3 N4 C/BE3#

DEVSEL# M3 PCI_DEVSEL# 17,19,20,21
FRAME# F1 PCI_FRAME# 17,19,20,21
IRDY# L5 PCI_IRDY# 17,19,20,21
TRDY# F2 PCI_TRDY# 17,19,20,21
STOP# F3 PCI_STOP# 17,19,20,21
PAR G1 PCI_PAR 19,20,21
PERR# L4 PCI_PERR# 17,19,20,21

SERR# K5 PME_SB# PCI_SERR# 17,19,20,21
PME# W2
PLOCK# M2 PCI_LOCK# 17
PCIRST# U5 PCI_RST# 8,24,29
PCICLK P5 4"-8.5" CLK_ICHPCI 18
CLKRUN#/GPIO24 AC2 PM_CLKRUN# 20,21,26

17,21 PCI_REQ#0 B1 REQ0#
17,20 PCI_REQ#1 A2 REQ1#
17,19 PCI_REQ#2 B3 REQ2#
17 PCI_REQ#3 C7 REQ3#
17 PCI_REQ#4 B6 REQ4#
A6 REQB#/REQ5#/GPIO1
B5 REQA#/GPIO0

21 PCI_GNT#0 C1 GNT0#
20 PCI_GNT#1 E6 GNT1#
19 PCI_GNT#2 A7 GNT2#
B7 GNT3#
D6 GNT4#
C5 GNTB#/GNT5#/GPIO17
E8 GNTA#/GPIO16

T43 TPC28b
T49 TPC28b
T46 TPC28b
T150 TPC28b

FW82801DBM

+V3.3S

RN28A 1 10KOhm 2
RN28B 3 10KOhm 4

C455 5P /

ICH4 pin E8

Strap Option

Default: Pull-High 20K
Pull-Down for BIOS
TOP-BLOCK SWAP

5 10KOhm 6 RN30C

+V3.3S

RN30D 10KOhm

+V3.3

C178 0.1uF/10V

PCI_RST#

U17 NC7SZ08P5X

BUF_PCI_RST# 13,19,20,21,26,27

Meet LPC reset >= 60 us
(Add Buffer)

+V3.3

+V3.3

RN30A 10KOhm

RN30B 10KOhm

Q36 PMBS3904

20,21,27 PCI_PME#

PME_SB#

19 PME_SB#

pull up to VccSus3_3 by internal pull-up resistor

Strap Option

Default: Pull-Down
Pull-High for Hub
Interface 1.5
Buffer Mode

ICH4 USE

+V1.5S_ICH

R310 48.7Ohm

HUB_RCOMP_ICH4

1109

R-ICH4 <= 0.5"

+V1.5S_ICH

0.8V +/- 2% ICH4(R22)<=3"

R132 130Ohm

HUB_VSWING_ICH4

C436 0.01UF/10V

C439 0.1uF/10V

R133 150Ohm

2025

Caution:
The VREF of HUB interface is 0.35V
The VSWING of HUB interace is 0.8V
But in Intel CRB, their naming convention will make people confused.

Title :	ICH4-M(HUBPCI)		
ASUSTek COMPUTER INC. NB1	Engineer:	John Hung	
Size: Custom	Project Name: A3N		Rev: 2.0
Date: Friday, April 23, 2004	Sheet 14 of 49		

USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Pair Width/Space: 7/10 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils

LxWxH=31x31x2.38

U20C

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBRBIAS USBRBIAS# OC0# OC1# OC2# OC3# OC4# OC5# AGPBUSY#/GPIO6 C3_STAT#/GPIO21 CPUPERF#/GPIO22 DPRSLPVR LAN_RST# PWRBTN# PWROK RI# RSMRST# SLP_S1#/GPIO19 SLP_S3# SLP_S4# SLP_S5# STP_PCI#/GPIO18 STP_CPU#/GPIO20 SSMUXSEL/GPIO23 SUSCLK SUS_STAT#/LPCPD# SYS_RESET# THRM# THRMTRIP# VGATE/VRMPWRGD

GPIO7 GPIO8 GPIO12 GPIO13 GPIO25 GPIO27 GPIO28 GPIO32 GPIO33 GPIO34 GPIO35 GPIO36 GPIO37 GPIO38 GPIO39 GPIO40 GPIO41 GPIO42 GPIO43 A20GATE A20M# CPUPWRGD CPUSLP# DPSLP# FERR# IGNNE# INIT# INTR NMI SMI# STPCLK# RCIN#

FW82801DBM

USBRBIAS:
W/S: 5/5 mils
Length: <= 0.5"

R138 18.2Ohm <=0.5"

RN31C 10KOhm

1201

T50 TPC28b T138TPC28b T51 TPC28b T166TPC28b

R313 56Ohm <=3"

R383 1KOhm

R156 180KOhm

C212 1UF/10V

C213 0.1uF/10V

C225 0.047UF/10V

R170 10MOhm

R166 10MOhm

C216 18P

C220 18P

X2 32.768KHZ +/-20ppm/12.5PF

RTC CIRCUITRY

RTC Circuits:
RTC_RST#, RTC_VBIAS, RTC_X1, RTC_X2
Width= 5 mils
Length<=1"
Need GND Guard

Measure duty-cycle of SUSCLK
(Pin AA4) must be in 30-70%

1215

G3: 5 uA

RC time delay should be 10-20 ms

GPIO[32:43] default:
Output High
ICH4 EDS R:1.0 page 10-94
10.10.8, 10.10.9

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils

1104 1219 2021 1212

LxWxH=31x31x2.38

U20B

IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15

IDE_SDD0 IDE_SDD1 IDE_SDD2 IDE_SDD3 IDE_SDD4 IDE_SDD5 IDE_SDD6 IDE_SDD7 IDE_SDD8 IDE_SDD9 IDE_SDD10 IDE_SDD11 IDE_SDD12 IDE_SDD13 IDE_SDD14 IDE_SDD15

IDE_SDA0 IDE_SDA1 IDE_SDA2 IDE_SDCS1# IDE_SDCS3# IDE_SIORDY IDE_SDIOW# IDE_SDIOR# IDE_SDDACK# IDE_SDDREQ

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils

AC97 SDOUT & SYNC

ICH4 — T — R2 — AMC
R1
AC97

Outer Layer: 5 mils
W/S= 1:1
ICH4-(T): 1"- 8"
R1-(T): 0.1"- 0.4"
AC97-R1: <=5.6"
R2-(T): 0.1"- 0.4"
AMC-R2: 0.9"-5.6"

AC97_SYNC R143 33Ohm AC97_SYNC_MDC
R141 33Ohm AC97_SYNC_CODEC
AC97_SDOUT R144 33Ohm AC97_SDOUT_MDC
R142 33Ohm AC97_SDOUT_CODEC

1 to 8 inches | 0.1 to 0.4 inches | 0.9 to 5.6 inches

T type routing, place R at branch point.

AC97 SDIN

ICH4 — R2 — AMC AC97

Outer Layer: 5 mils
W/S= 1:1
ICH4-R2: 0.9"- 13.6"
AC97-R2: 0.1"-0.4"
(#0013)

AC97_SDIN0
AC97_SDIN1

INTEL REQUEST

U38 NC7SZ08P5X

PM_SLP_S3# SLP_S1# C472 0.1uF/10V PM_SLP_S1# 18,35

Strap Option — Default: Pull-Down 20K
Pull-High for CPU SAFE_MODE

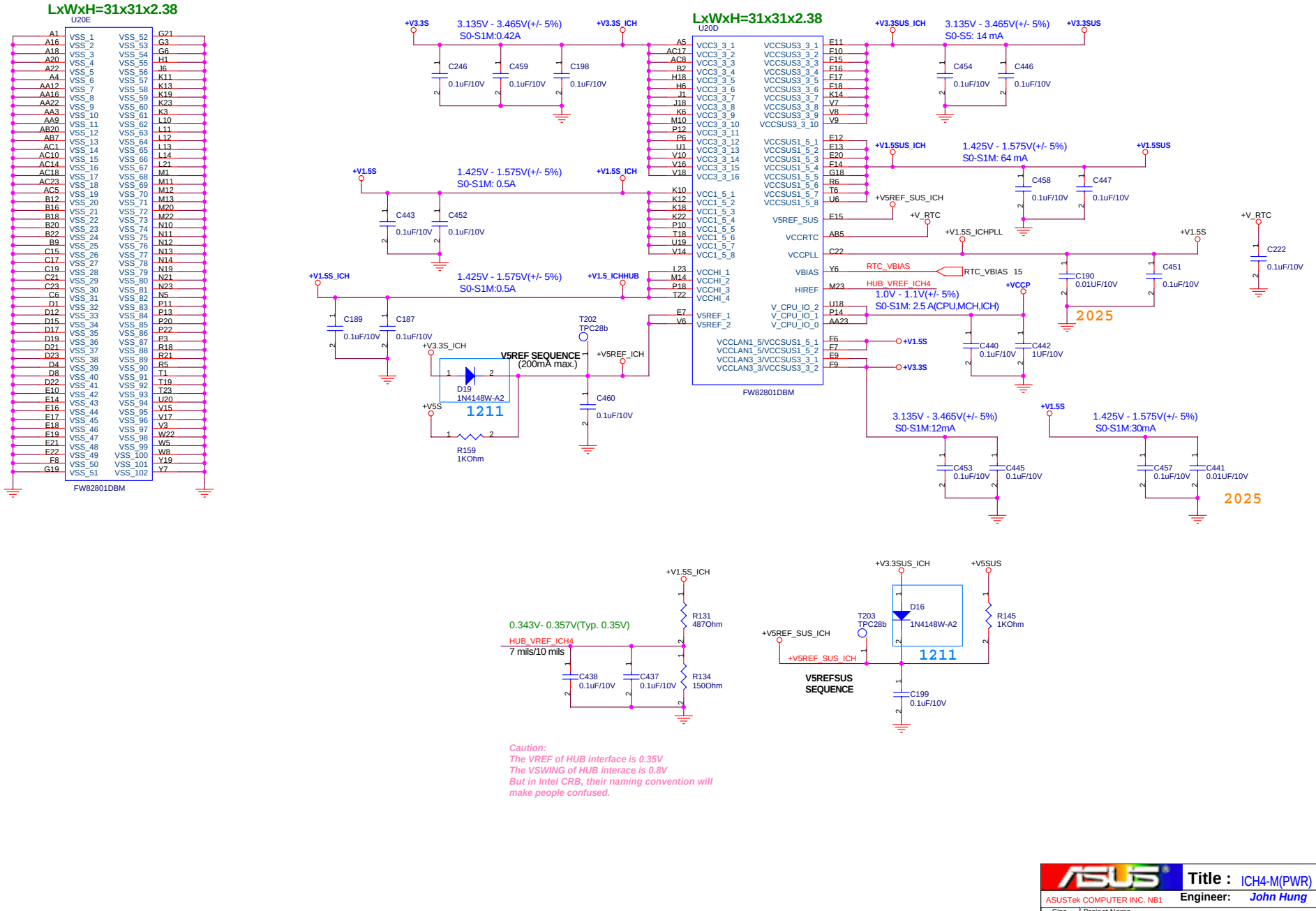
Strap Option — Default: Pull-Down 20K
Pull-High for Not Supported
PM_DPRSLPVR 38

PID_0_ICH4 PID_1_ICH4 PID_2_ICH4 PID_3_ICH4
RN89B RN89A RN89C RN89D 2.2KOhm
PID_0 PID_1 PID_2 PID_3

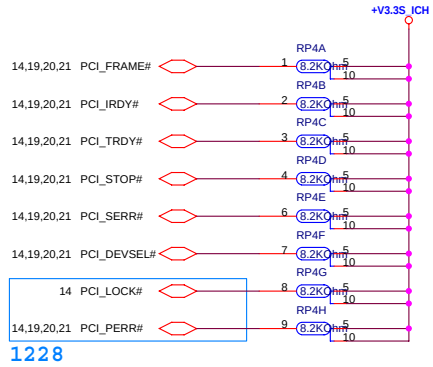
2021

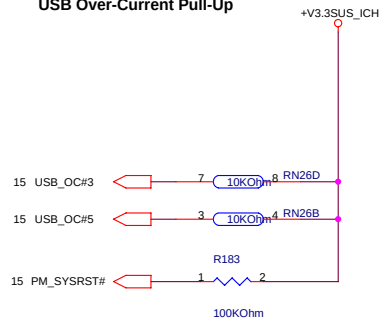
AC97 AC97_SDIN0 MDC AC97_SDIN1

Title :	ICH4-M(H_U_IDE_PM)
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 15 of 49

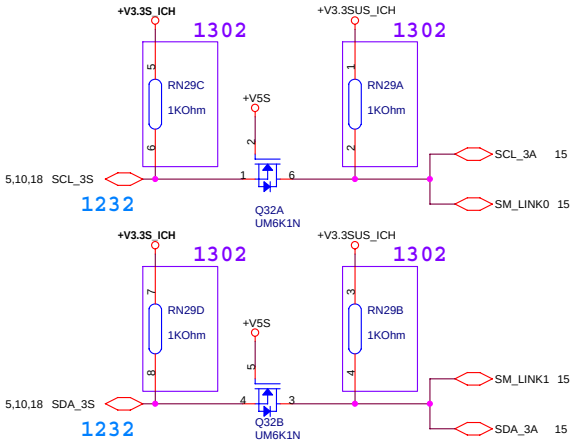


Title :	ICH4-M(PWR)
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 16 of 49

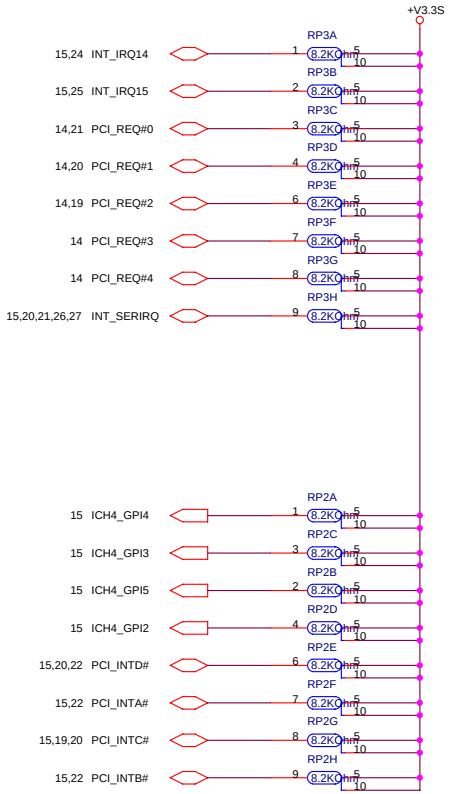


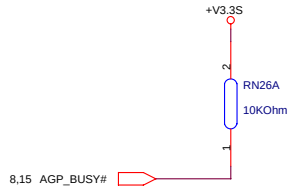


ICH4 SMLink & SMbus must be tied together



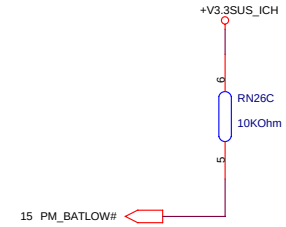
Can Swap





BATTERY LOW

ICH4



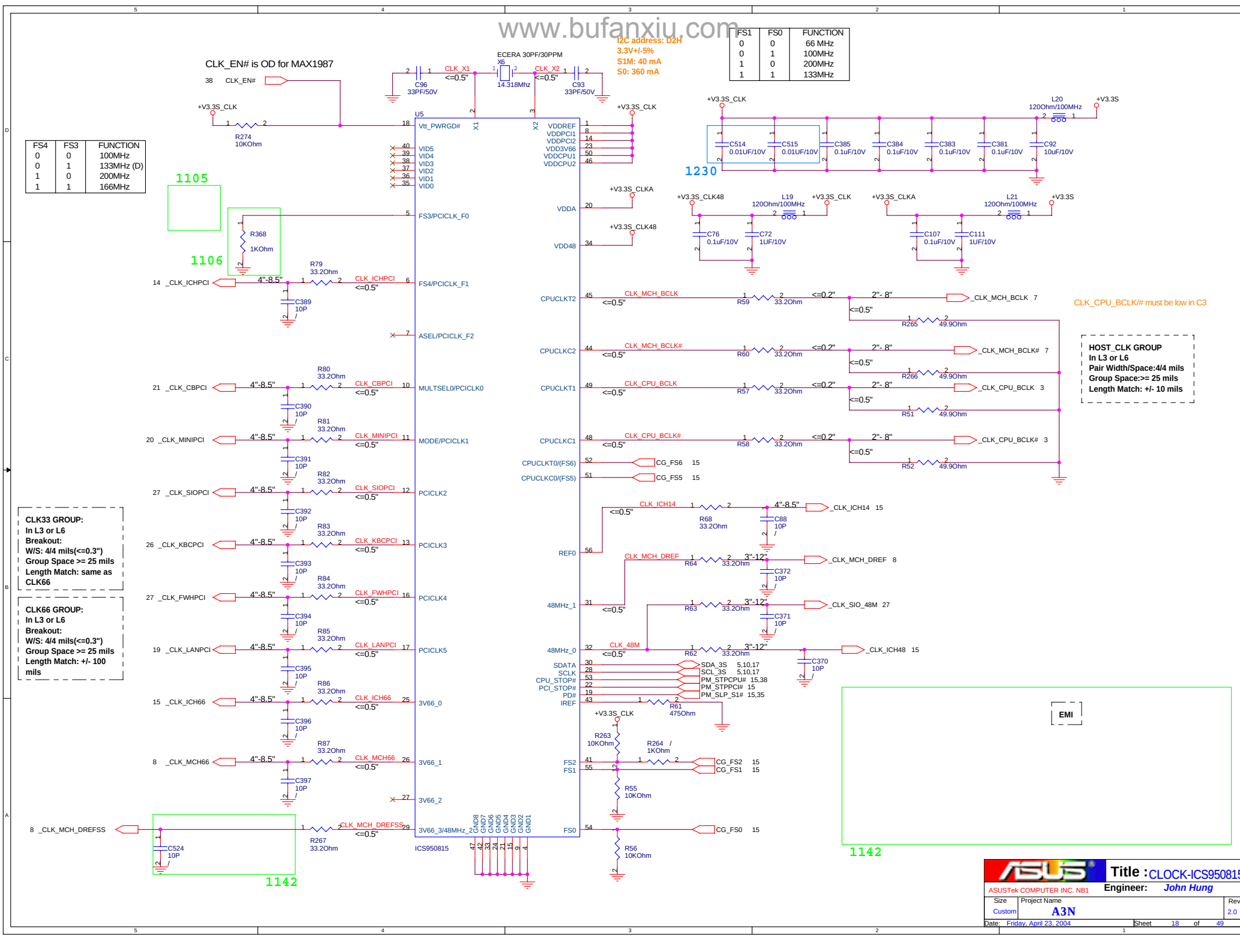
ASUSTek COMPUTER INC. NB1

Title : ICH4-M(PULLUP)

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

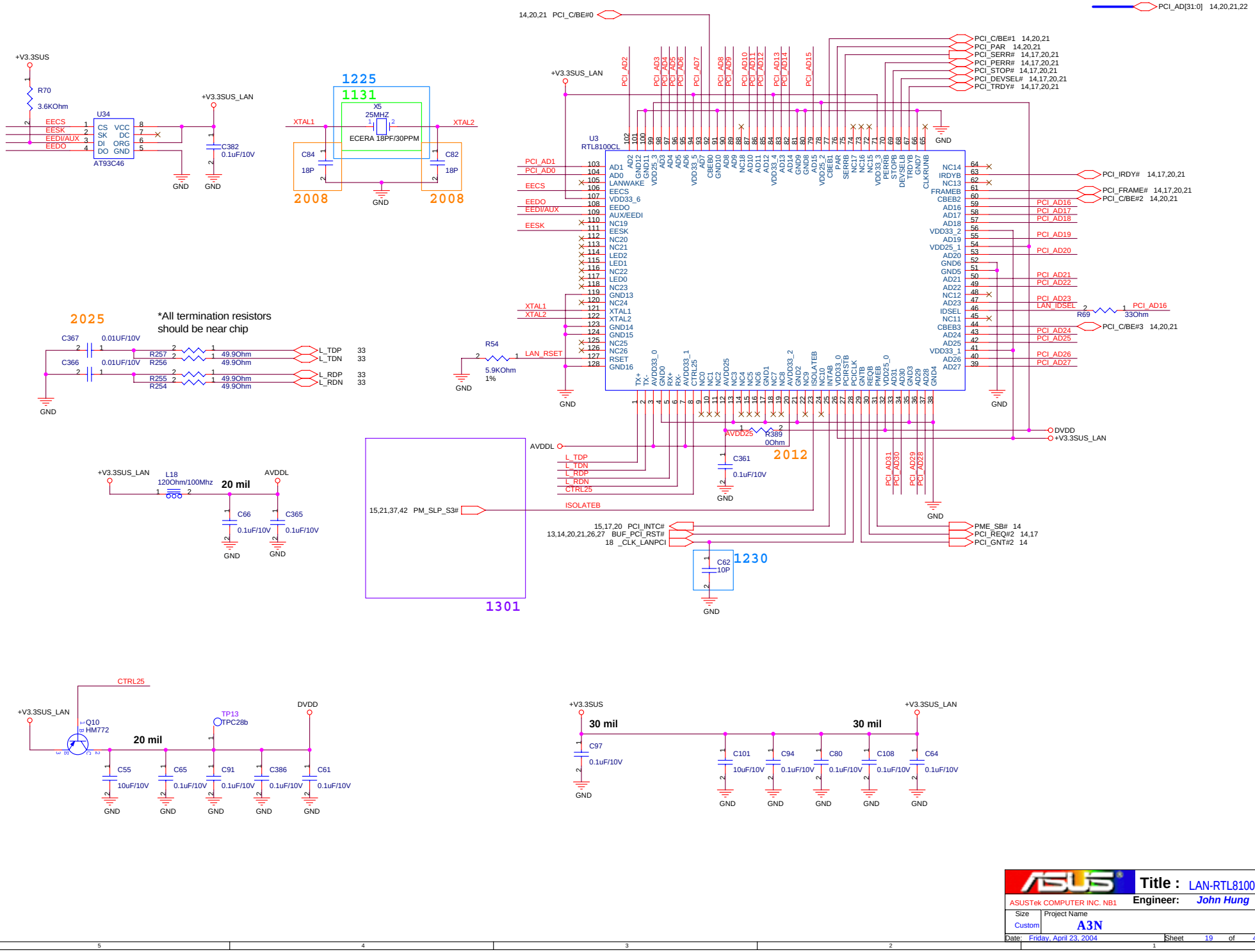
Date: Friday, April 23, 2004 Sheet 17 of 49



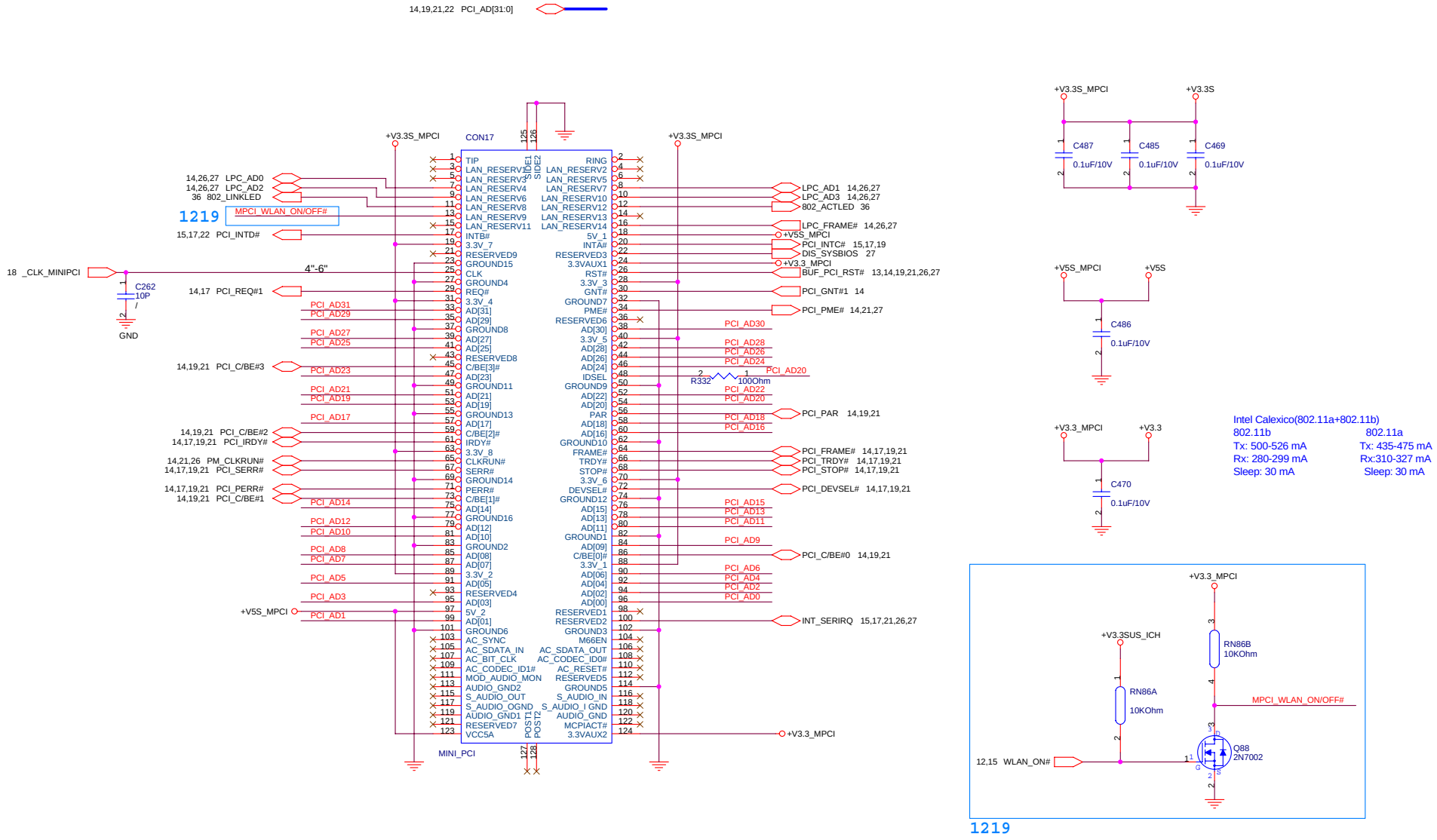
FS1	FS0	FUNCTION
0	0	66 MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz

FS4	FS3	FUNCTION
0	0	100MHz
0	1	133MHz (D)
1	0	200MHz
1	1	166MHz

Title :	CLOCK-ICS950815
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 18 of 49



ASUSTek COMPUTER INC. NB1	Title : LAN-RTL8100CL	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 19 of 49	



Intel Calexico(802.11a+802.11b)

802.11b	802.11a
Tx: 500-526 mA	Tx: 435-475 mA
Rx: 280-299 mA	Rx:310-327 mA
Sleep: 30 mA	Sleep: 30 mA

1219

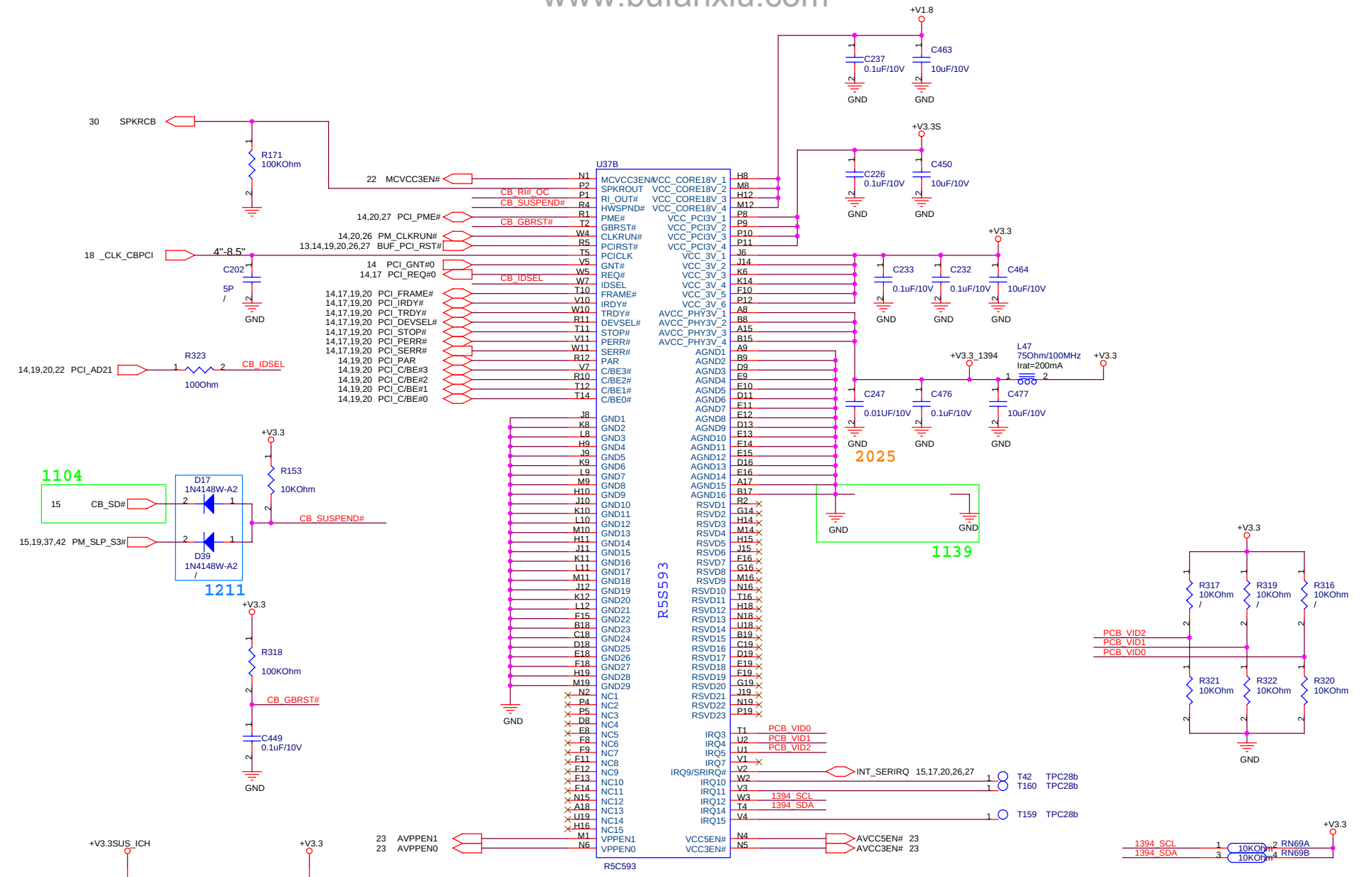
ASUSTek COMPUTER INC. NB1

Title : MINIPCI

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 20 of 49



<Variant Name>

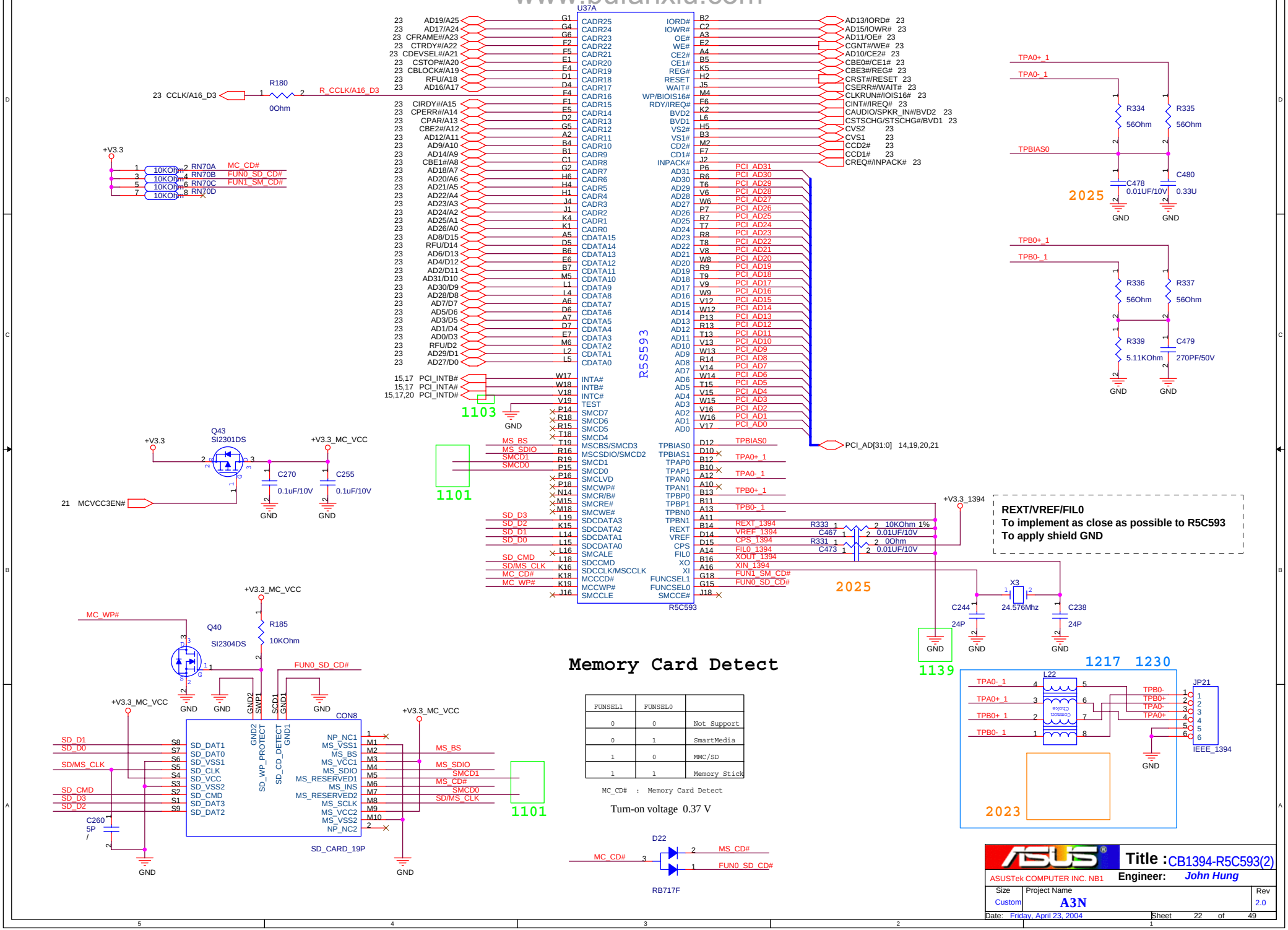
ASUSTek COMPUTER INC. NB1

Title : CB1394-R5C593(1)

Engineer: John Hung

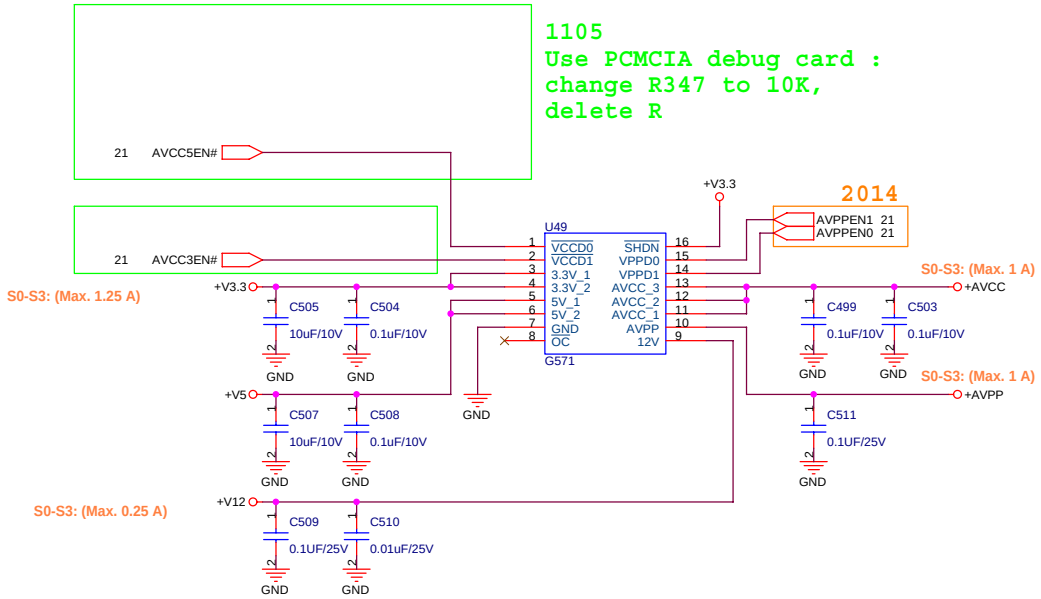
Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 21 of 49

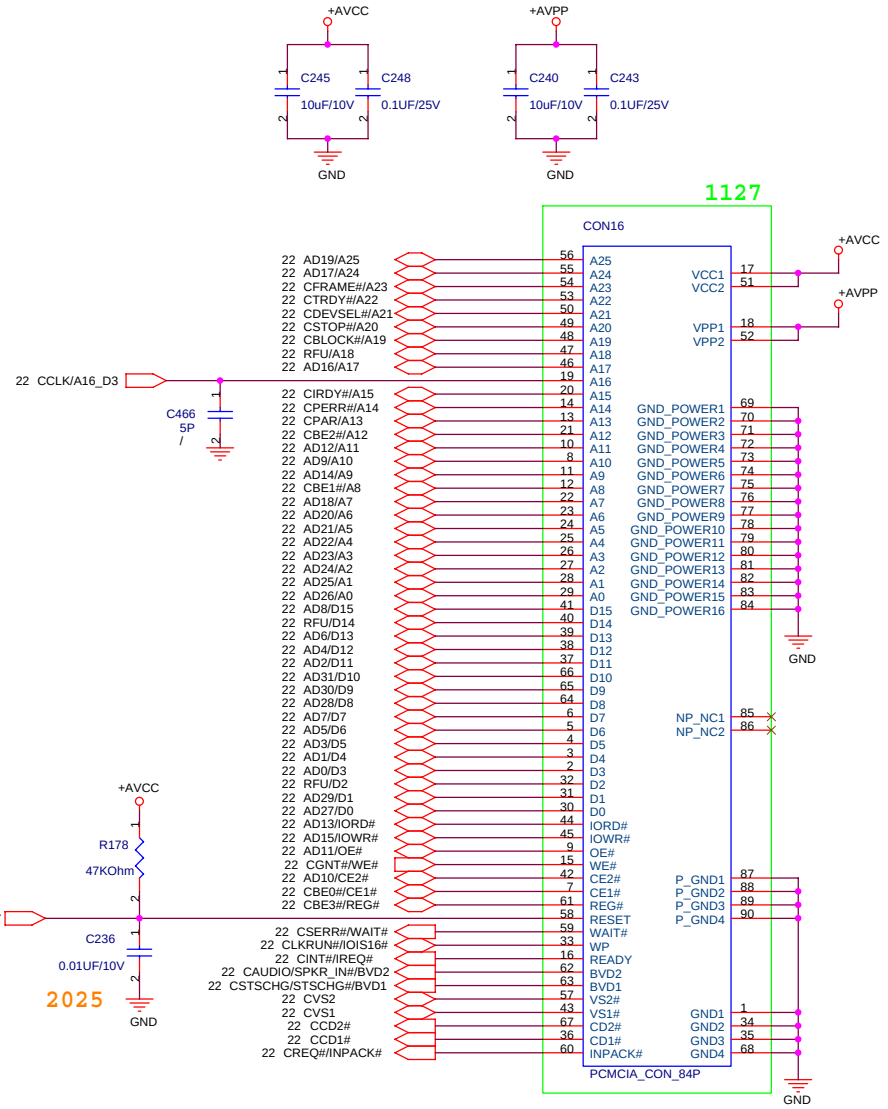


CB POWER SWITCH

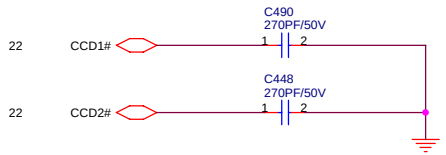
1105
Use PCMCIA debug card :
change R347 to 10K,
delete R



CB SOCKET



CB DE-BOUNCE



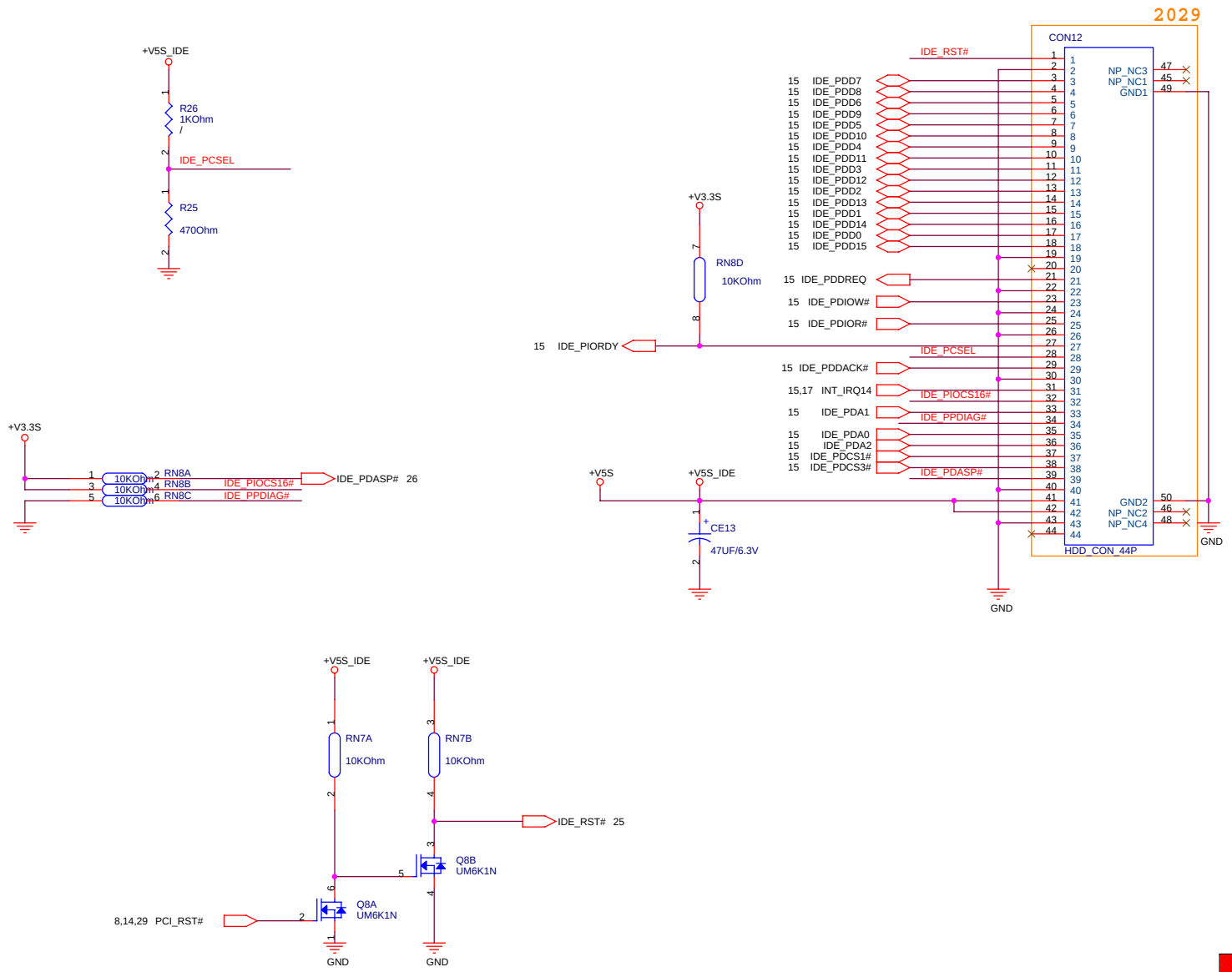
<Variant Name>

Title : PCMCIA SOCKET

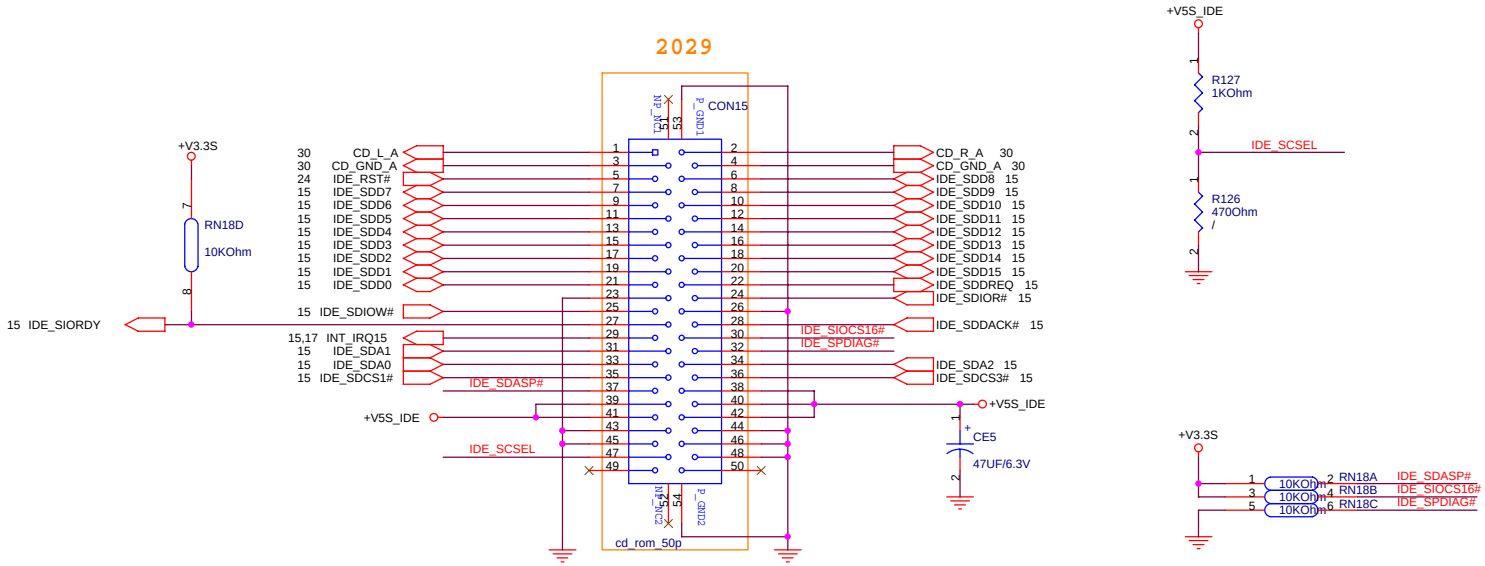
ASUSTek COMPUTER INC. NB1 Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 23 of 49



ASUSTek COMPUTER INC. NB1	Title : HDD Connector	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 24 of 49	



ASUSTek COMPUTER INC. NB1	Title : ODD Connector	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 25 of 49	

S0-S3: (2.5 mA Typ, 7 mA Max.)

LxWxH=14x14x1.7

U16

M38857

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

Audio DJ pin depends on Keyboard Matrix.

Follow M6N

A3N follow M6N Keyboard Matrix

P21: Power button overwrite disable. Only can be pulled down as default value than can be used as a input.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

ZIF_CON_28P

K/B	US	UK	JP
KEYDETECT1	H	L	L
KEYDETECT2	H	H	L

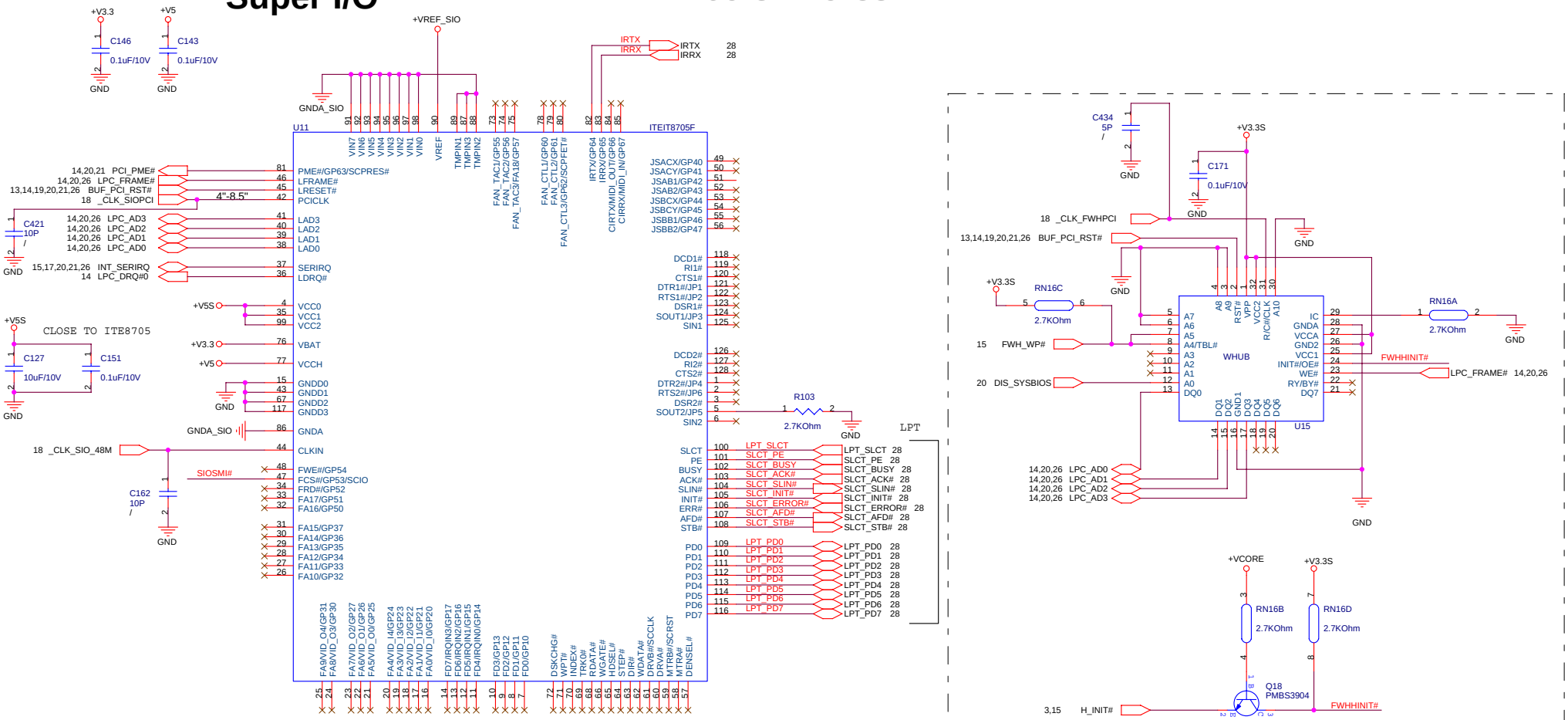
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell

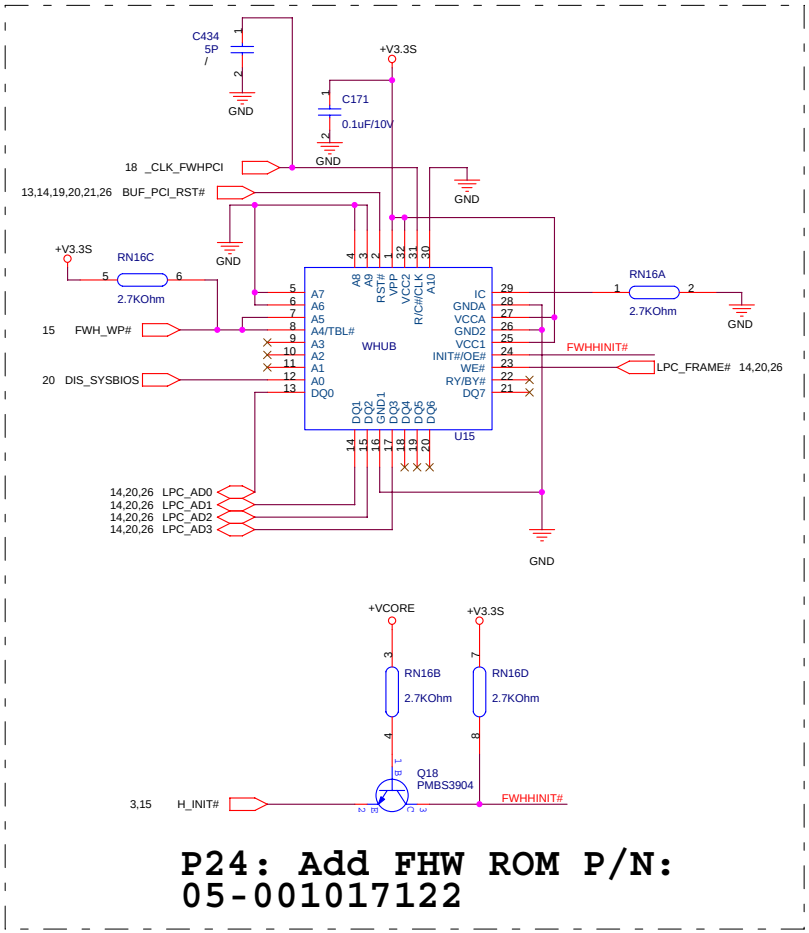
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU throttling 50%

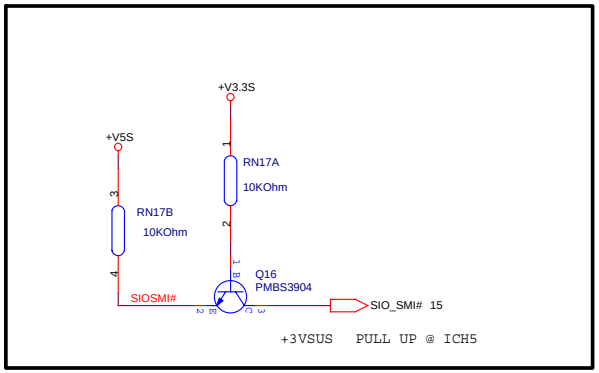
IDE NUM CAP SCR

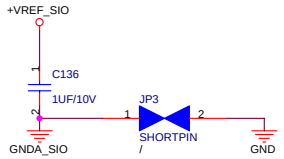
Title :	KBC-M38857
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 26 of 49

Super I/O





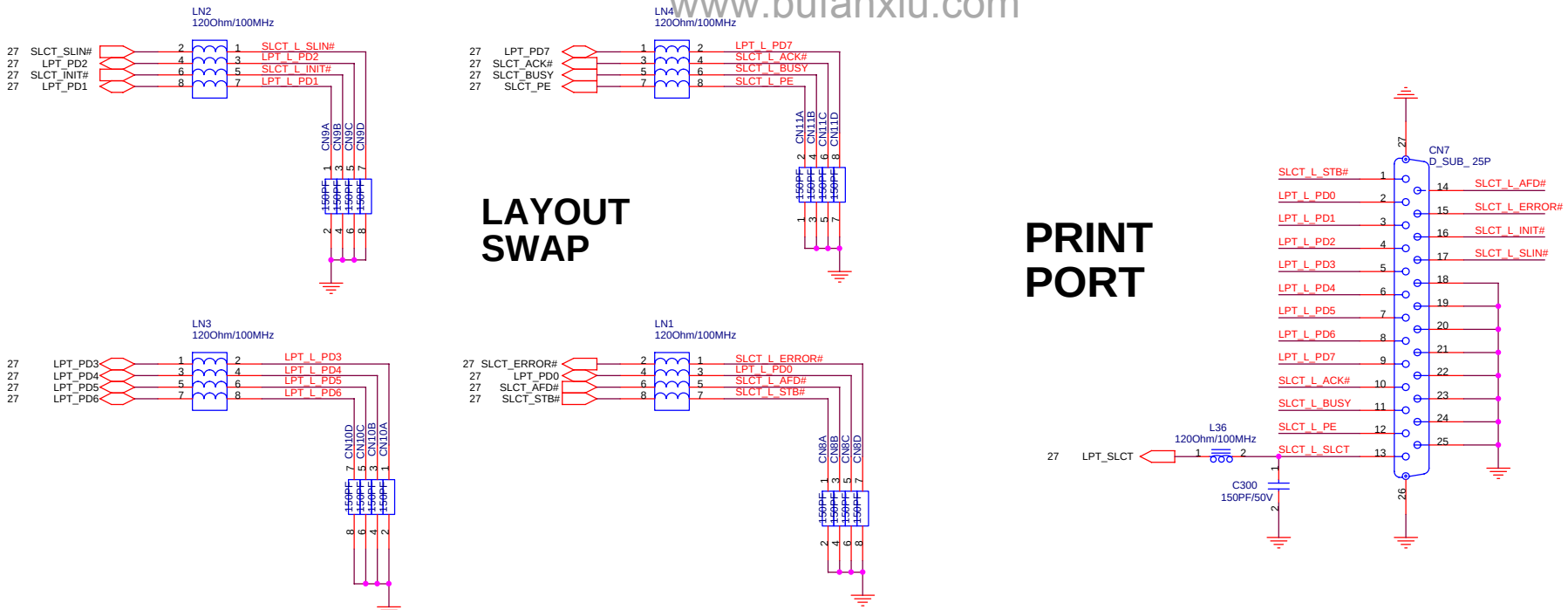


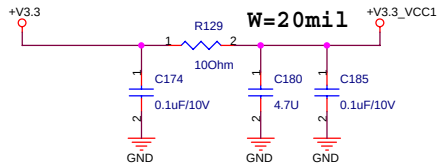


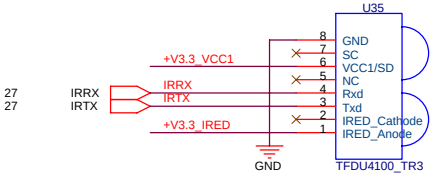
CLOSE TO ITE8705

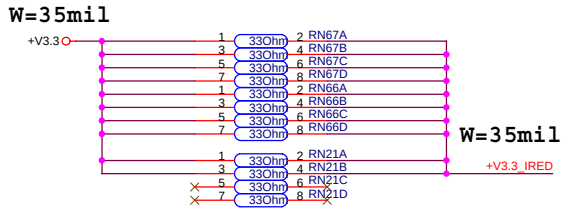
<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : SIO-ITE8705	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 27 of 49	









ASUSTek COMPUTER INC. NB1

Title :

Engineer: John Hung

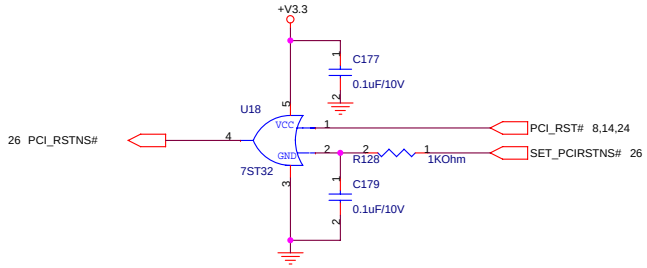
Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 28 of 49

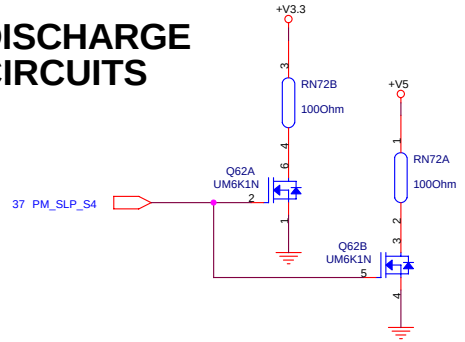
PCMCIA DEBUG Card

1105

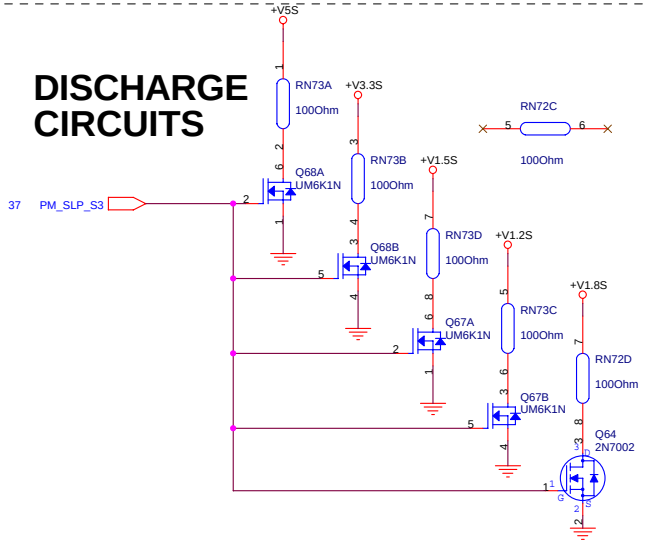
PCI_RSTNS# Gen Circuit



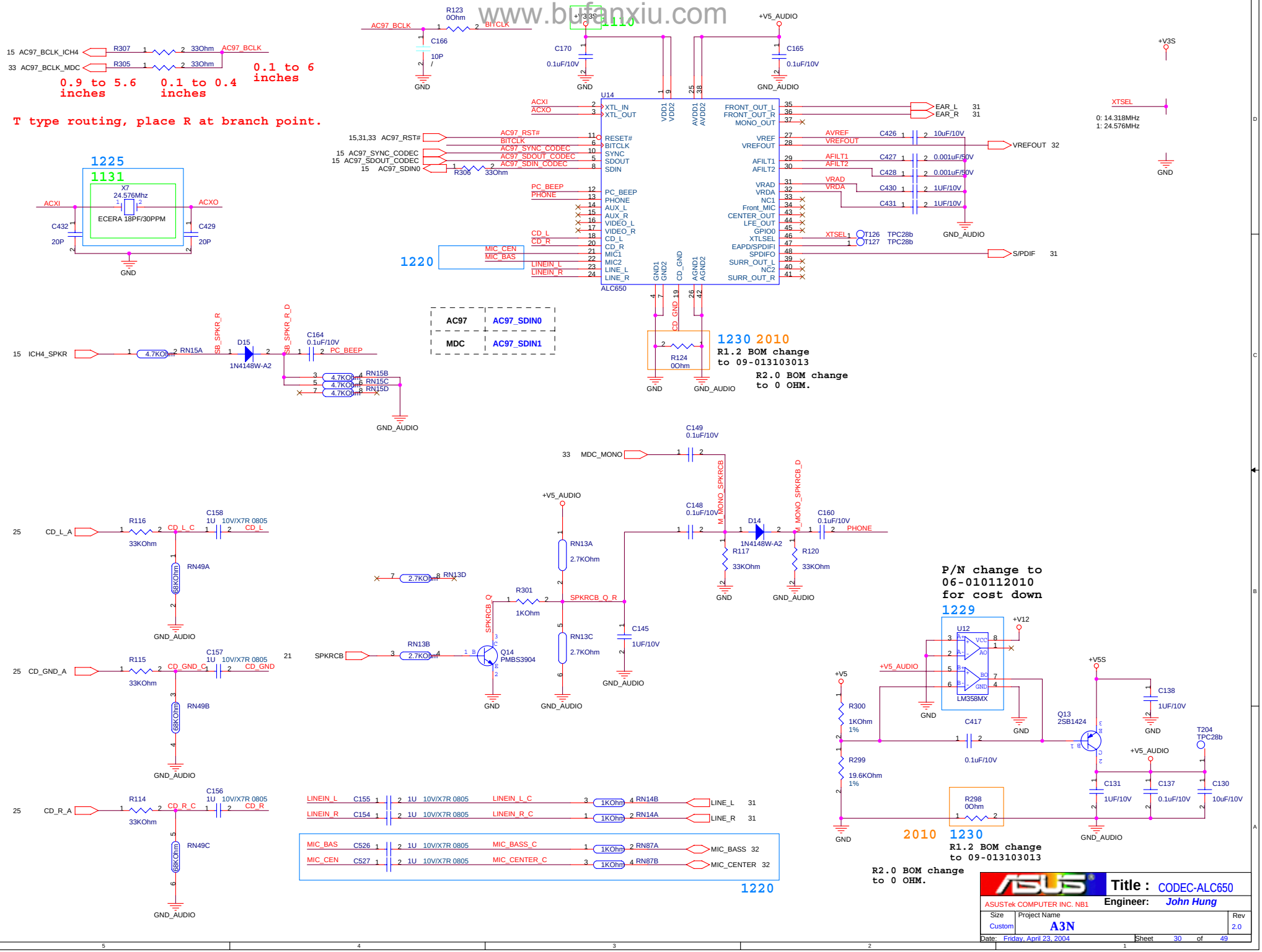
DISCHARGE CIRCUITS



DISCHARGE CIRCUITS



ASUSTek COMPUTER INC. NB1	Title : Discharge circuit	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 29 of 49	



2024 R104 0Ohm
R2.0 BOM change to 09-013103013

2010 R285 0Ohm
R2.0 BOM change to 0 OHM.

R304 0Ohm /

R1.2 BOM change 1230 to 09-013103013

$$f(highpass) = \frac{1}{2*3.14*R*C} = \frac{1}{\text{----------}} = 73$$

R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.

1202 1207 1230

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.

2018 D54 DAP202K

2018 D53 1N4148W-A2 SN74LV14 U52F U52E

For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.

2018 D49 DAP202K Q85A UM6K1N

1207

$$f(highpass) = \frac{1}{2*3.14*C(IL)*R(IL)} = \frac{1}{\text{----------}} = 500$$

$$f(lowpass) = \frac{1}{2*3.14*C(150P)*R(10K)} = \frac{1}{\text{----------}} = 106K$$

$$BTL\ Gain = -2\frac{R(FL)}{R(IL)} = -2\frac{10K}{10K} = -2$$

$$Speaker\ W = \frac{V*V}{R} = \frac{2*2}{4ohm} = 1W$$

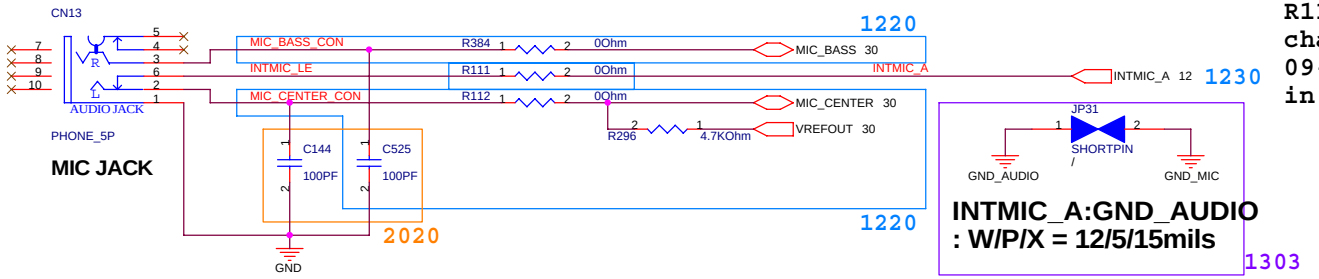
Can use 1W(4ohm) speaker

Title :	AUDIO AMP
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 31 of 49

1220

MIC OP CIRCUIT

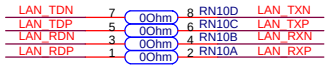
MIC JACK

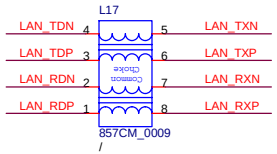


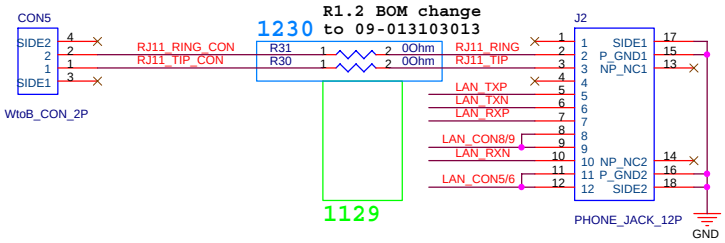
R111 & R112
change to
09-013103013
in R1.2 BOM

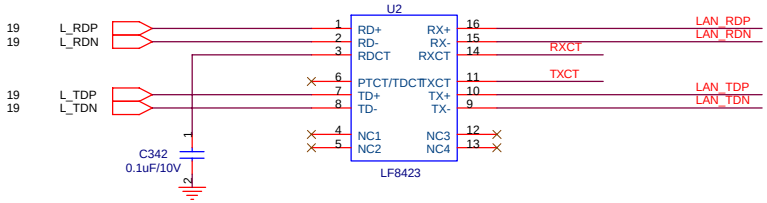
ASUSTek COMPUTER INC. NB1	Title :	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 32 of 49	

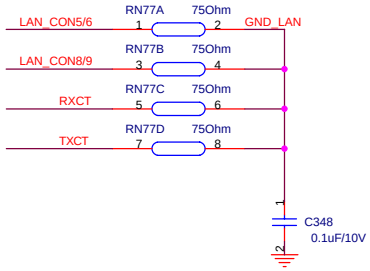
OP: FOR EMI



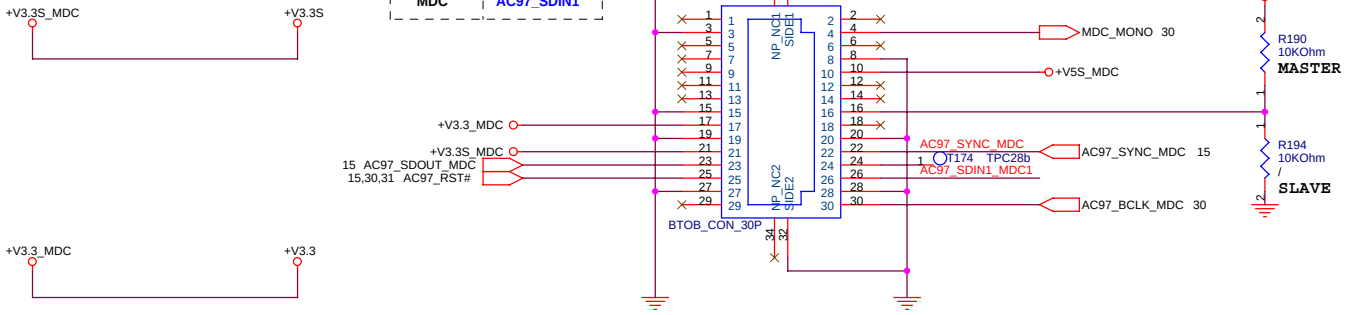


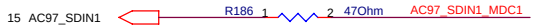






MDC





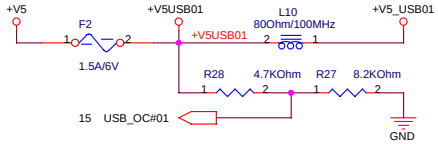
MDC

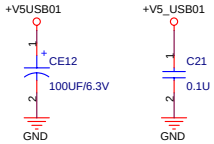
ASUSTek COMPUTER INC. NB1 Engineer: John Hung

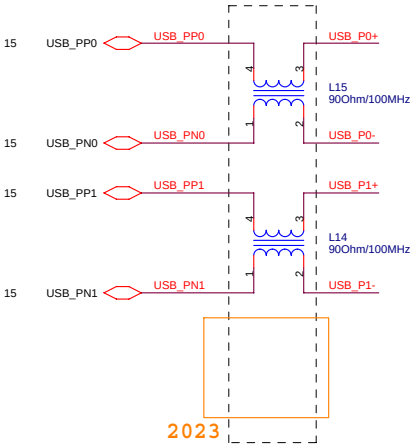
Title :

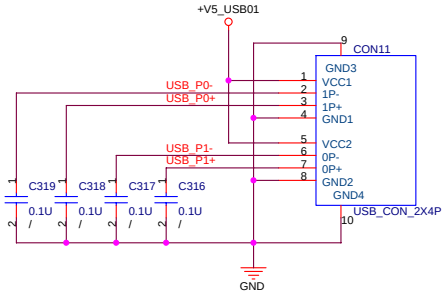
Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 33 of 49









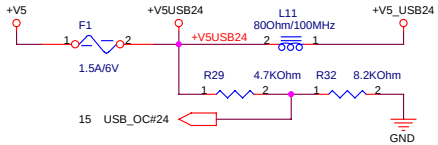
2023

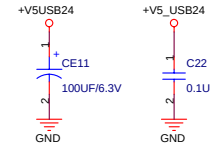
R & L Co-Lay

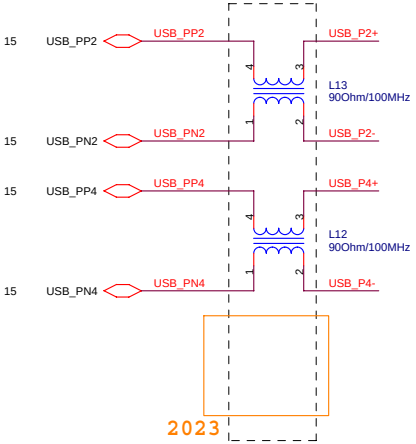
USB PORT 0 & PORT 1

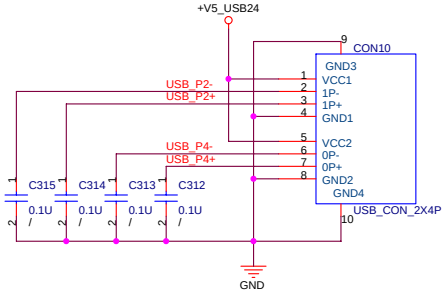
1128

USB PORT 3 for CAMERA
Change to page 12









2023

R & L Co-Lay

USB PORT 2 & PORT 4

1128

USB PORT 5 for WLAN
Change to page 12

ASUSTek COMPUTER INC. NB1

Title : USB

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

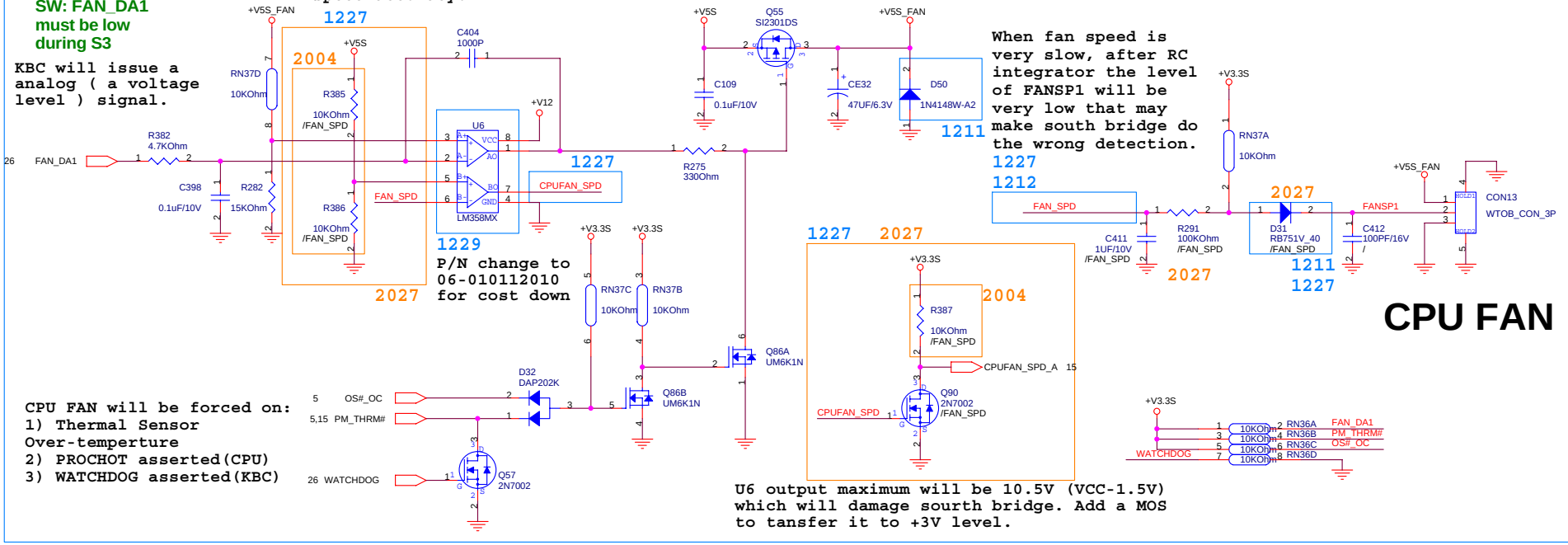
Date: Friday, April 23, 2004 Sheet 34 of 49

Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.

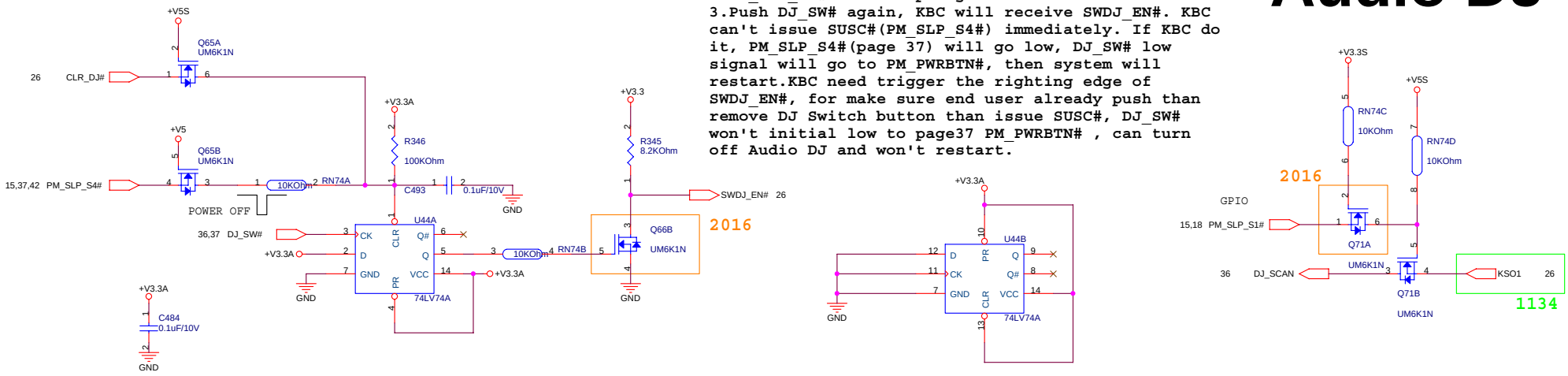


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

Audio DJ

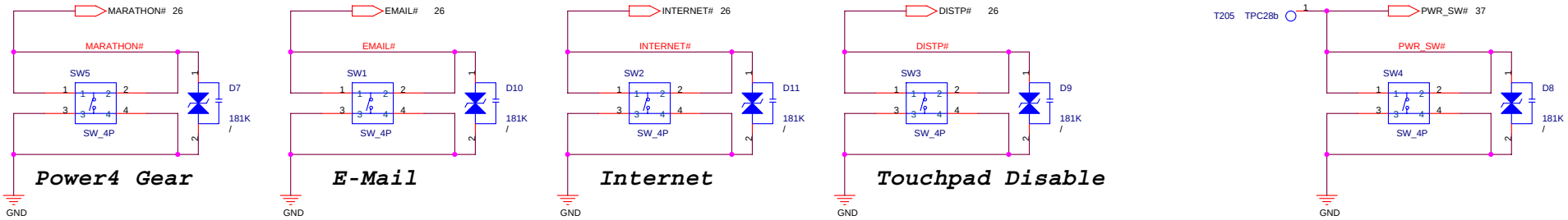
SWDJ_EN# function :
1.Push DJ_SW#, turn on Audio DJ.
2.PM_SLP_S4# will keep high.
3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.

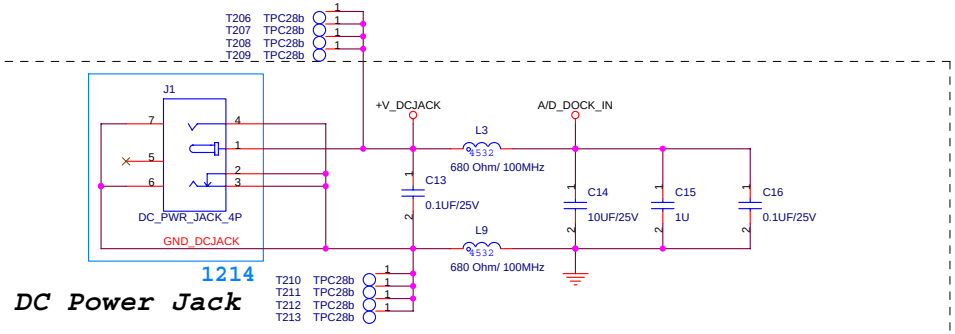


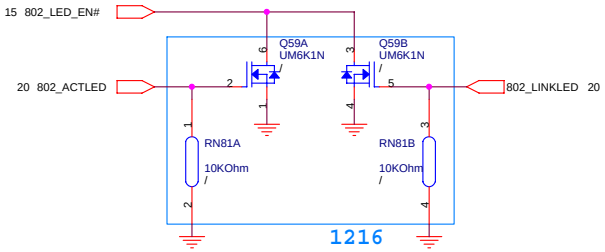
When power on, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D42 to Enable AudioDJ in OS.
Use D42 to Turn off AudioDJ when system be turned on in DJ mode.

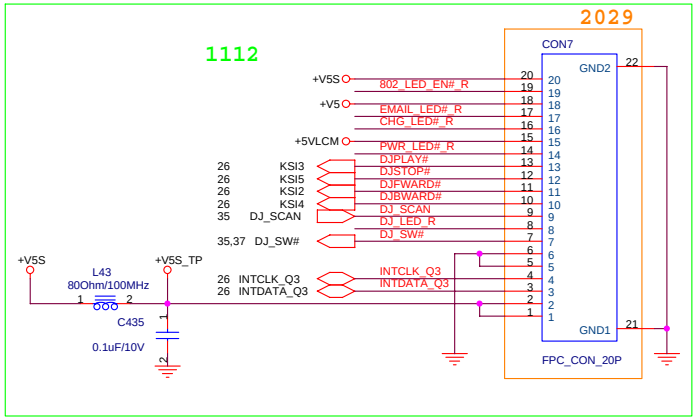
<Variant Name>

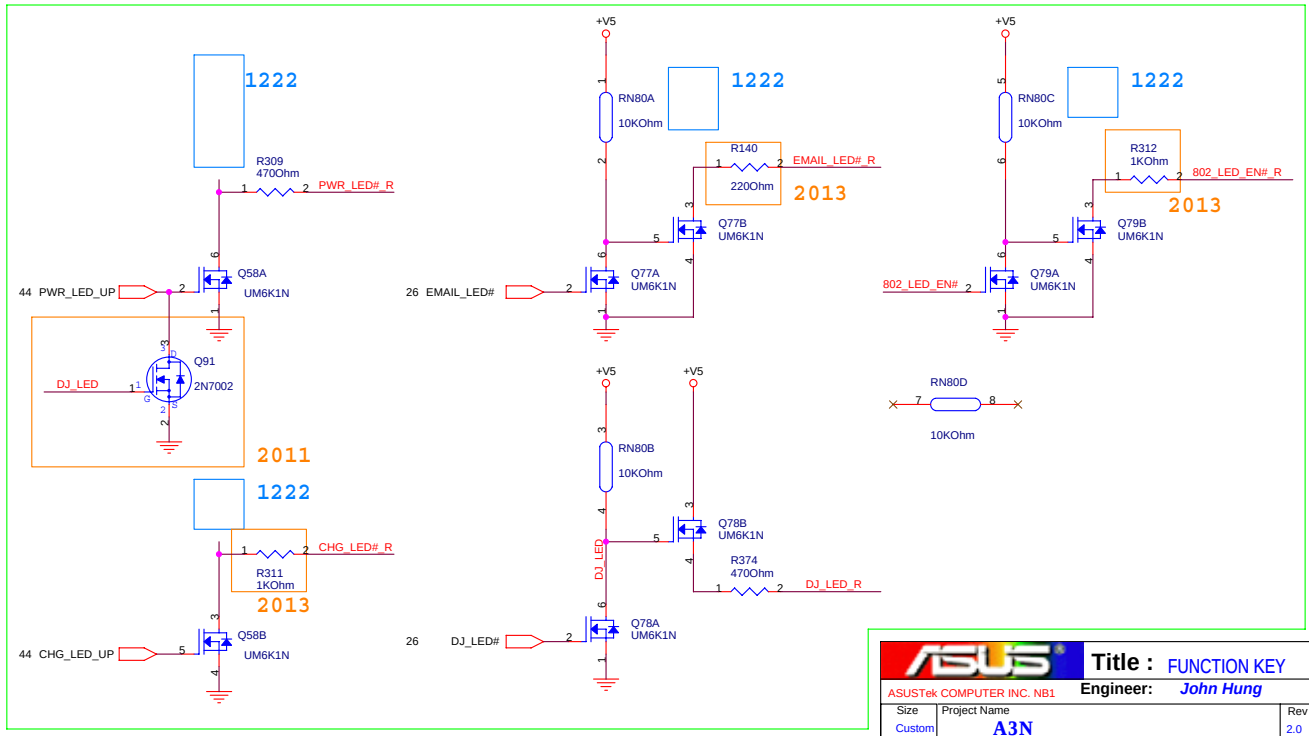
ASUSTek COMPUTER INC. NB1	Title : FAN&Audio DJ	
	Engineer: John Hung	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 35 of 49	











ASUSTek COMPUTER INC. NB1

Title : FUNCTION KEY

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 36 of 49

POWER ON/OFF SEQUENCE

System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.8VSUS>
RSMRST#->SLPS4#->SLPS3#->VCCLAN->LANPWROK
->V5REF->VCC->VCORE->PWROK->VGATE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+V1.8S
NB : +V1.2S, +V1.5S, +2.5V, +VCCP
SB :+V1.5SUS, +V3.3SUS, +VCCP, +V1.5S, +V3.3S
DDR :+V2.5, +V1.25,+V1.25S

(Set FORCE_OFF# as Force System Off function)

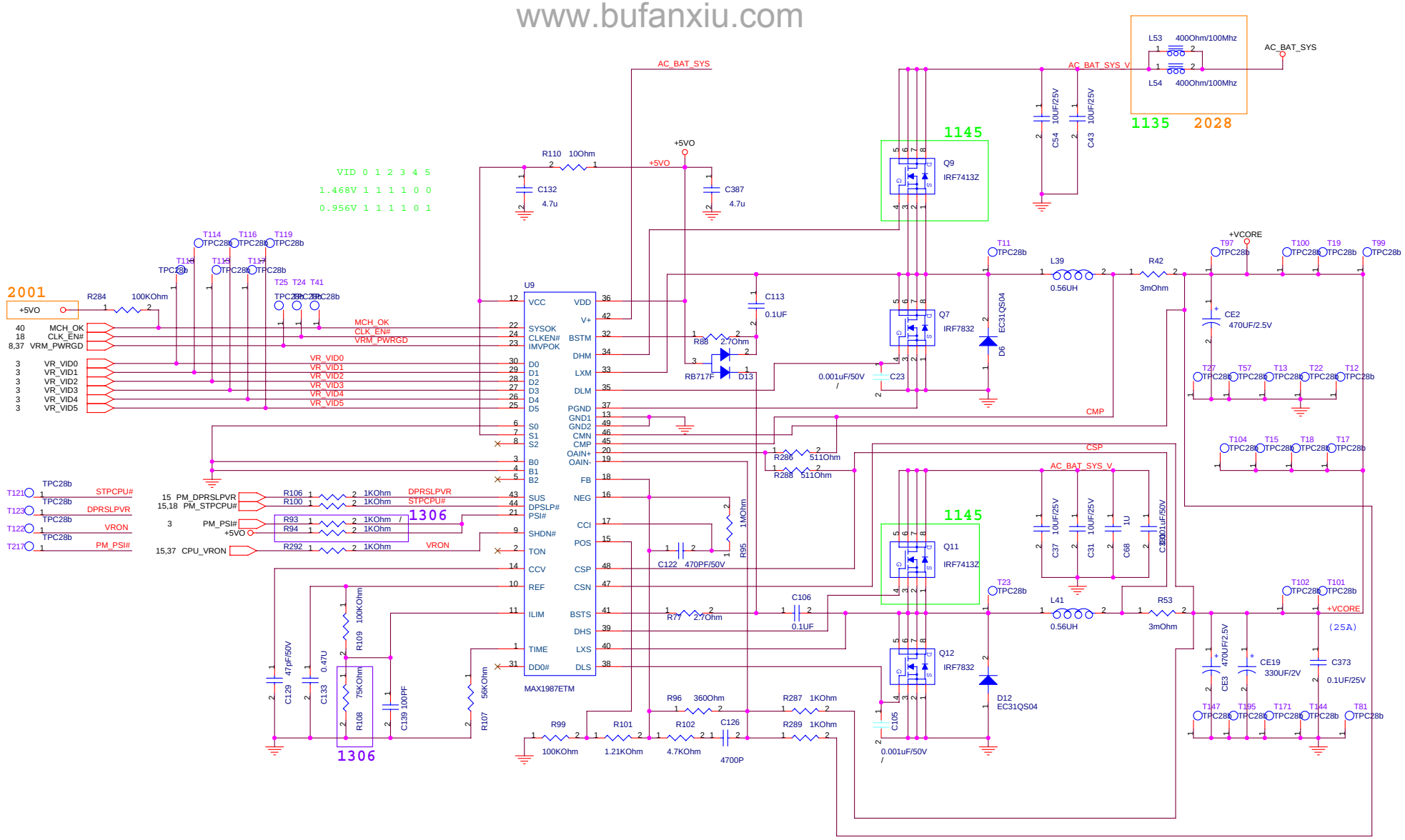
To Discharge circuits

To Discharge circuits

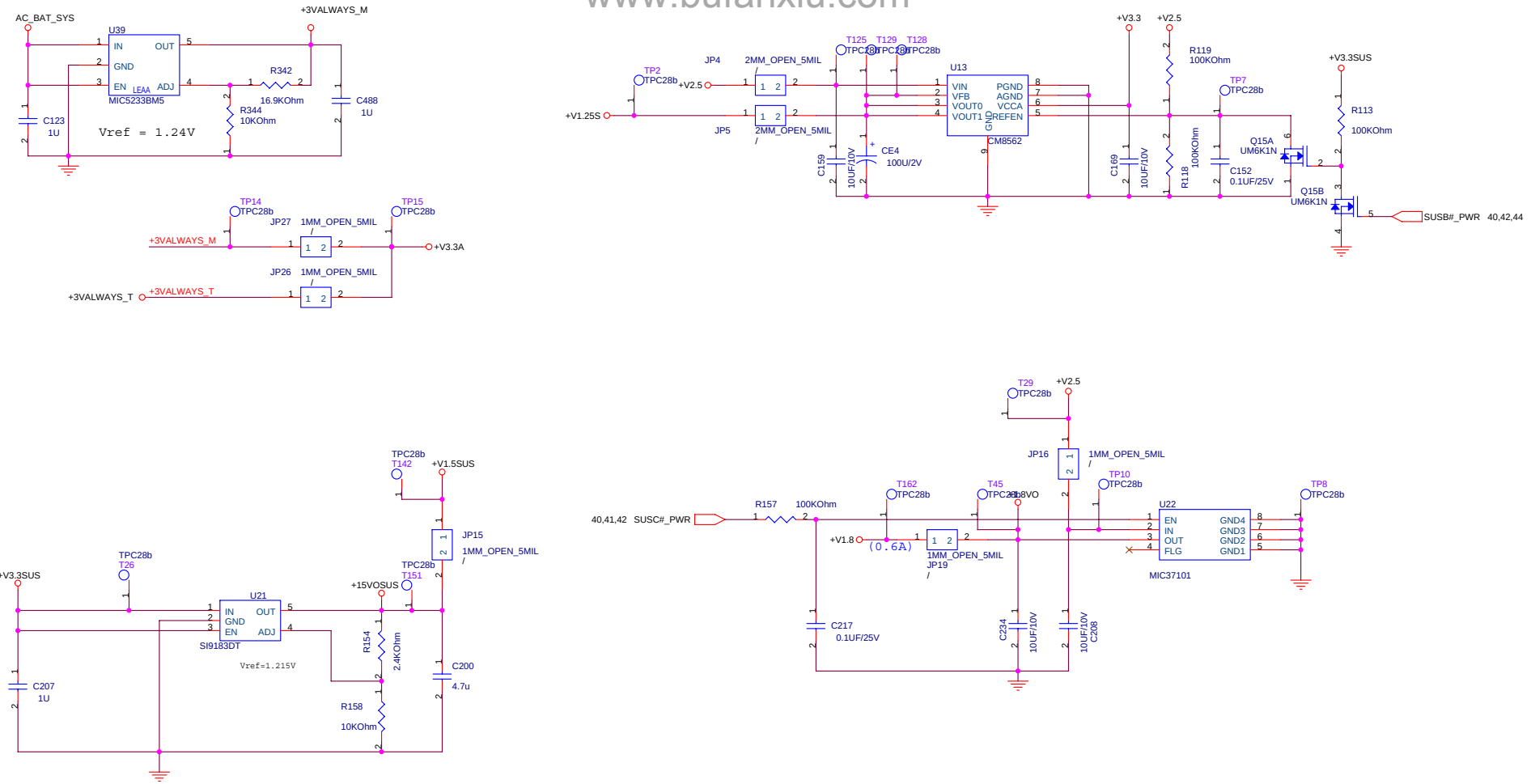
To POWER

LID SWITCH

Title :	PWR & RESET SEQ
ASUSTek COMPUTER INC. NB1	Engineer: John Hung
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 37 of 49



Title :	Vcore
ASUSTek COMPUTER INC. NB1	Engineer: Adams Lin
Size: Custom	Project Name: A3N
Rev: 2.0	
Date: Friday, April 23, 2004	Sheet 38 of 49



<Variant Name>

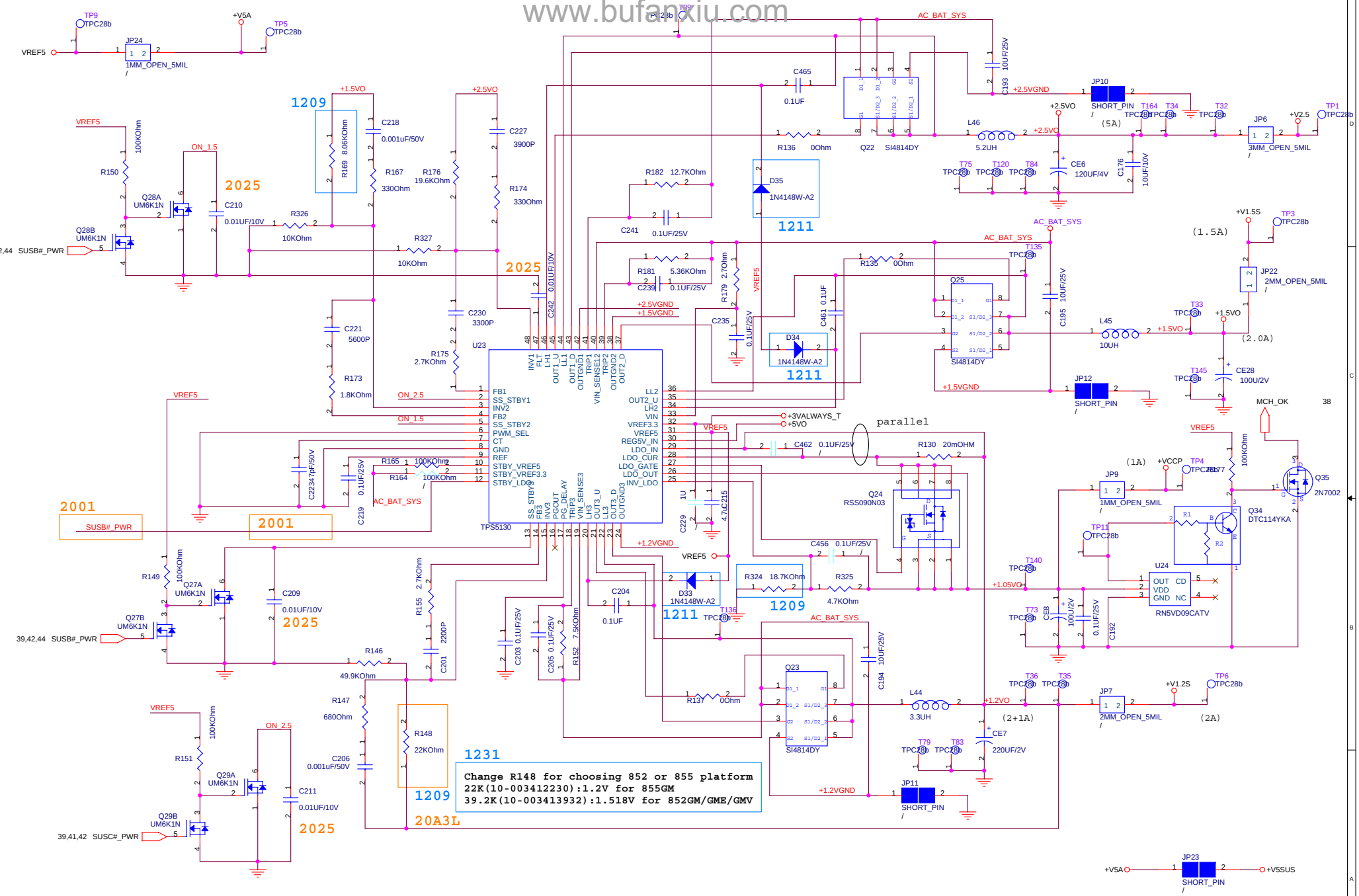
Title : 1.25V&1.8V

ASUSTek COMPUTER INC. NB1

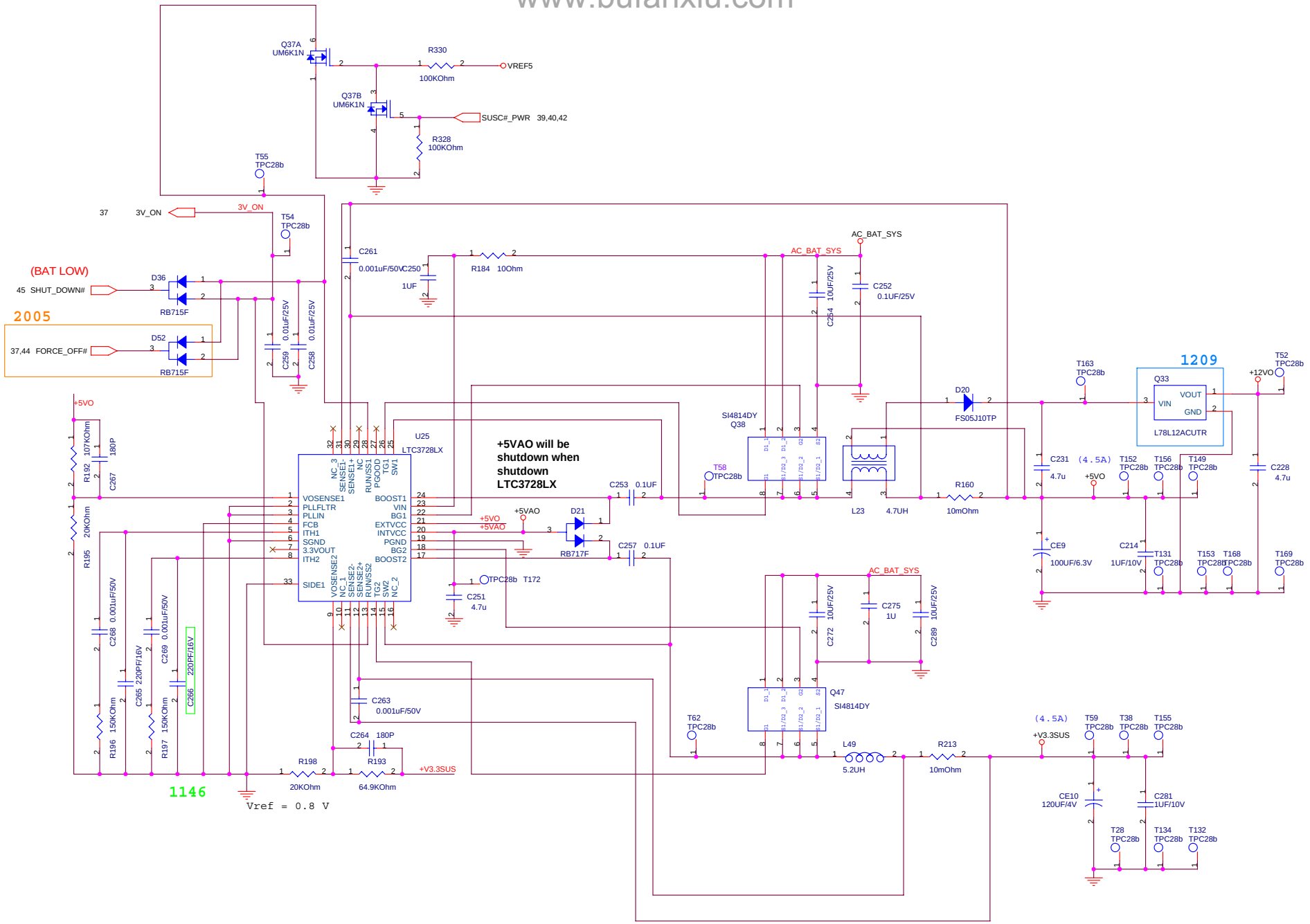
Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 39 of 49



Title	2.5V&1.5V&1.2V&1.05V
Engineer	Adams Lin
ASUSTek COMPUTER INC. NB1	
Size	Custom
Project Name	A3N
Rev	2.0
Date	Friday, April 23, 2004
Sheet	40 of 49



<Variant Name>

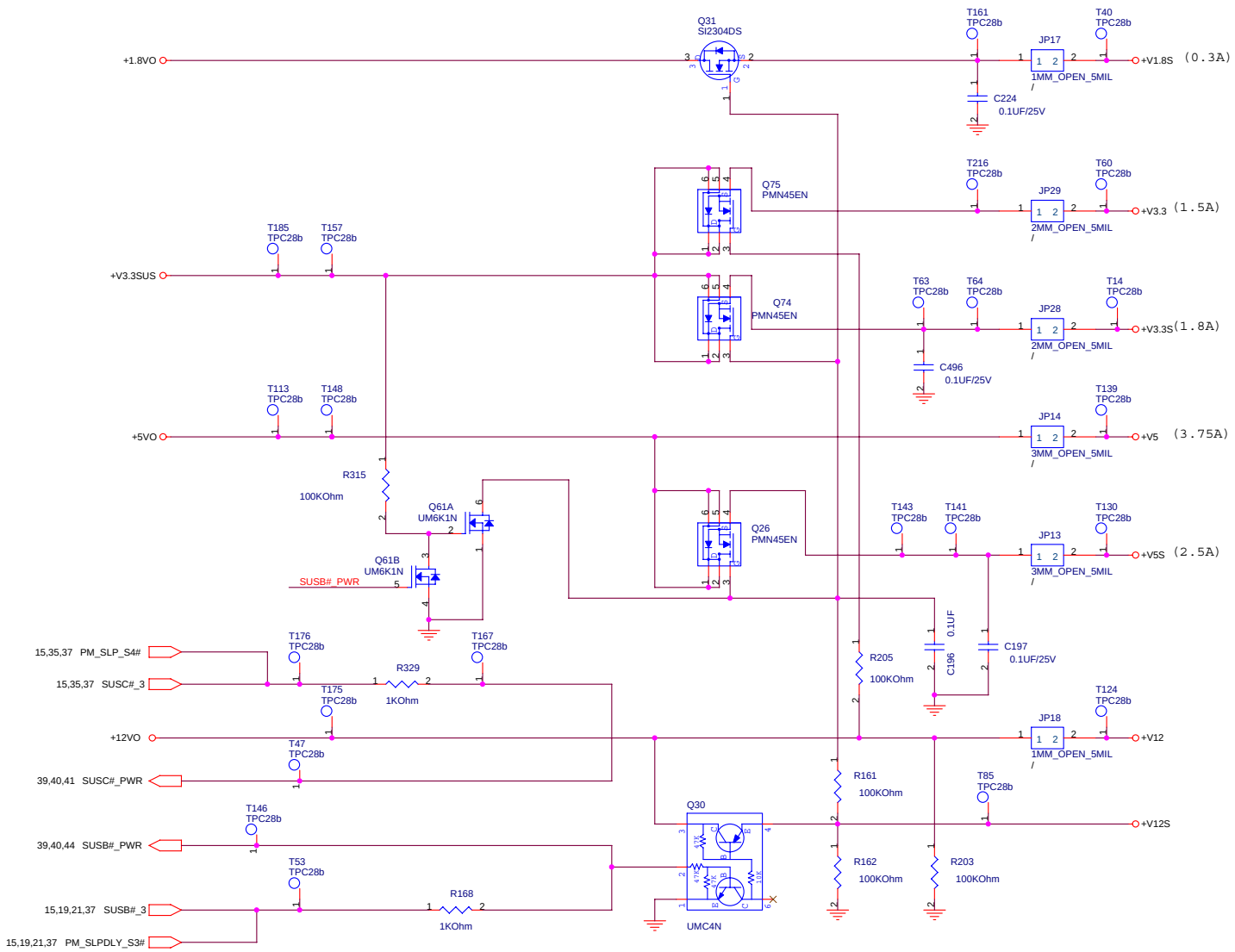
ASUSTek COMPUTER INC. NB1

Title : SYSTEM

Engineer: Adams Lin

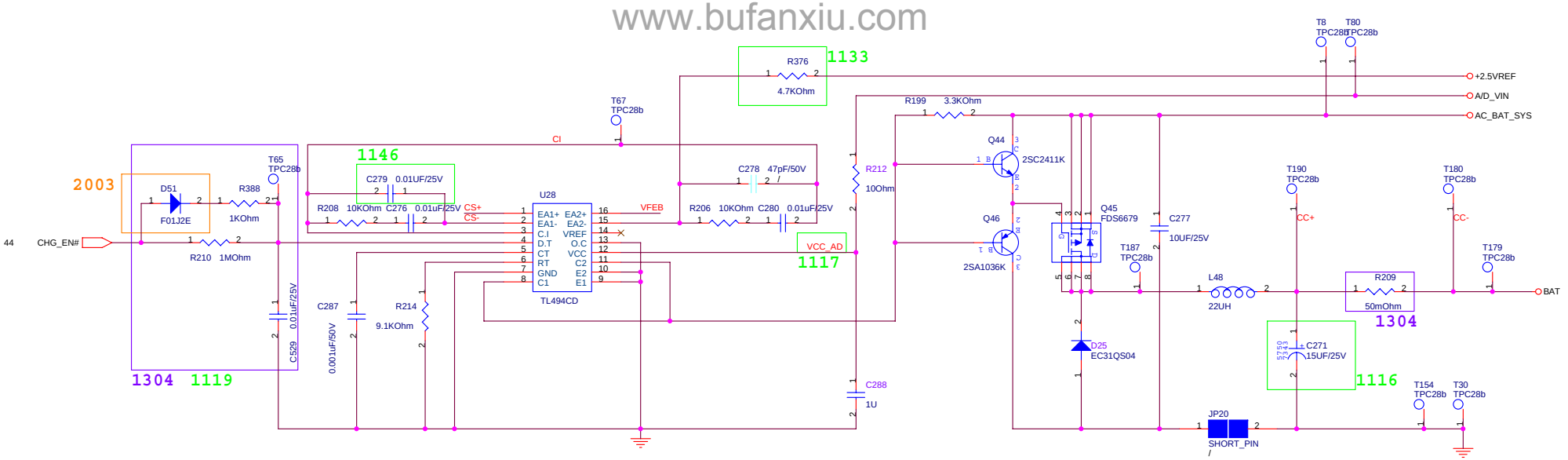
Size	Project Name	Rev
Custom	A3N	2.0

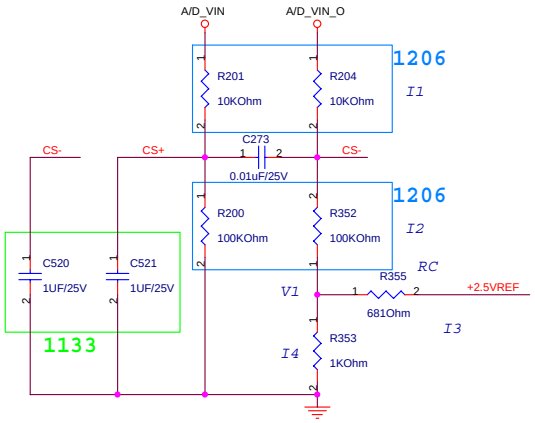
Date: Friday, April 23, 2004 Sheet 41 of 49

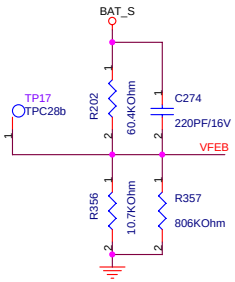


<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : LOAD SYWITCH	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3N	Rev: 2.0
Date: Friday, April 23, 2004	Sheet 42 of 49	

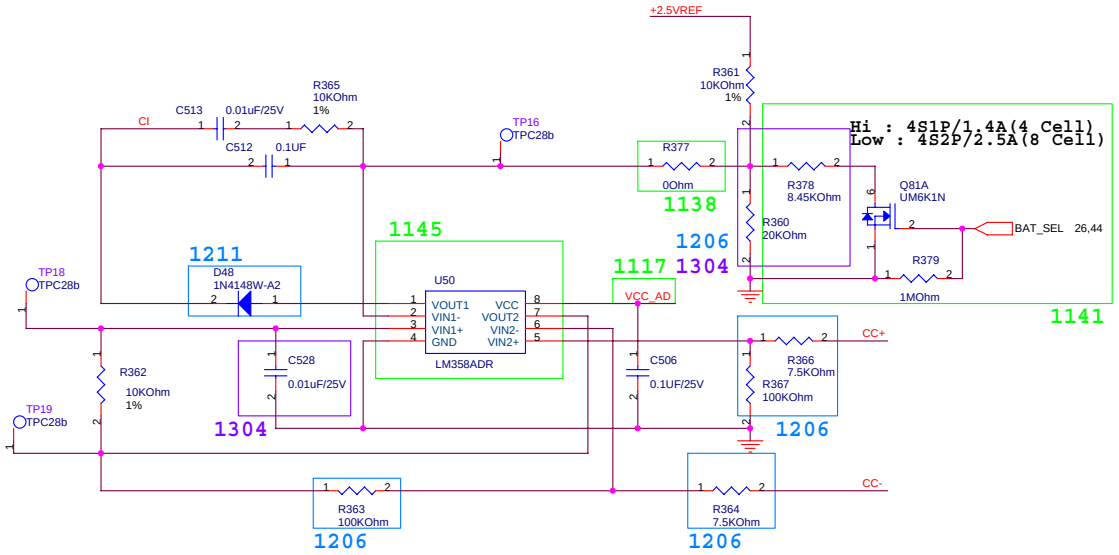






Current sharing = 3.1A

A/D_VIN=19V A/D_VIN_O=19V-3.1A*50mohm=18.845V
CS+=CS-=19*(100/110)=17.272727V
I1=(18.845V-17.272727V)/10K=0.15723mA
V1=17.272727V-(0.15723mA*100K)=1.5497V
I4=1.5497V/1K=1.5497mA
I3=1.5497mA-0.15723mA=1.39247mA
RC=(2.5V-1.5497V)/1.39247mA=681 ohm



<Variant Name>

ASUSTek COMPUTER INC. NB1

Title : CHARGER

Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3N	2.0

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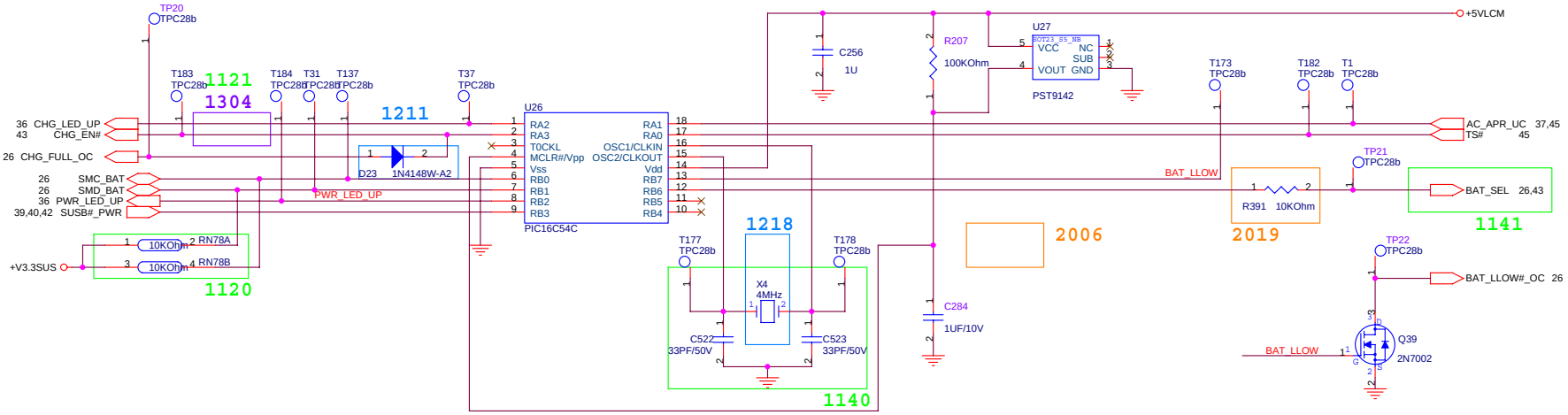

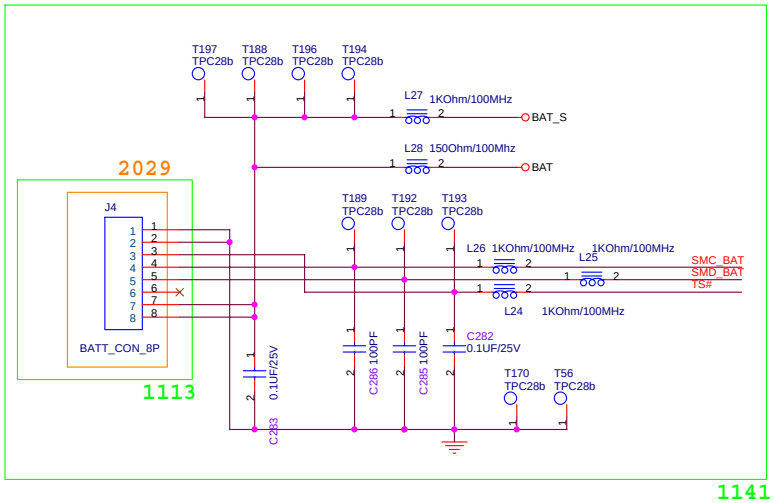

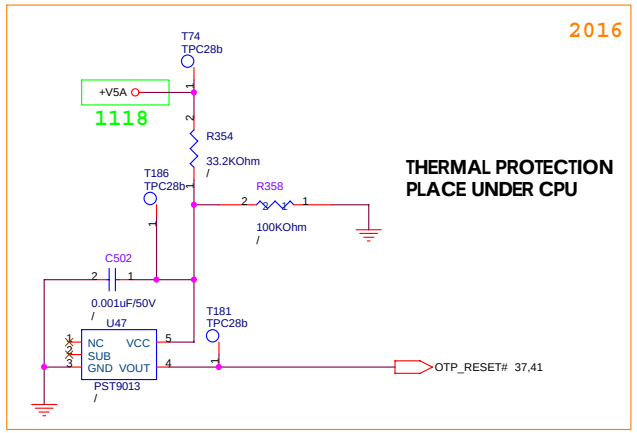

<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : PIC16C54	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3N	Rev: 2.0
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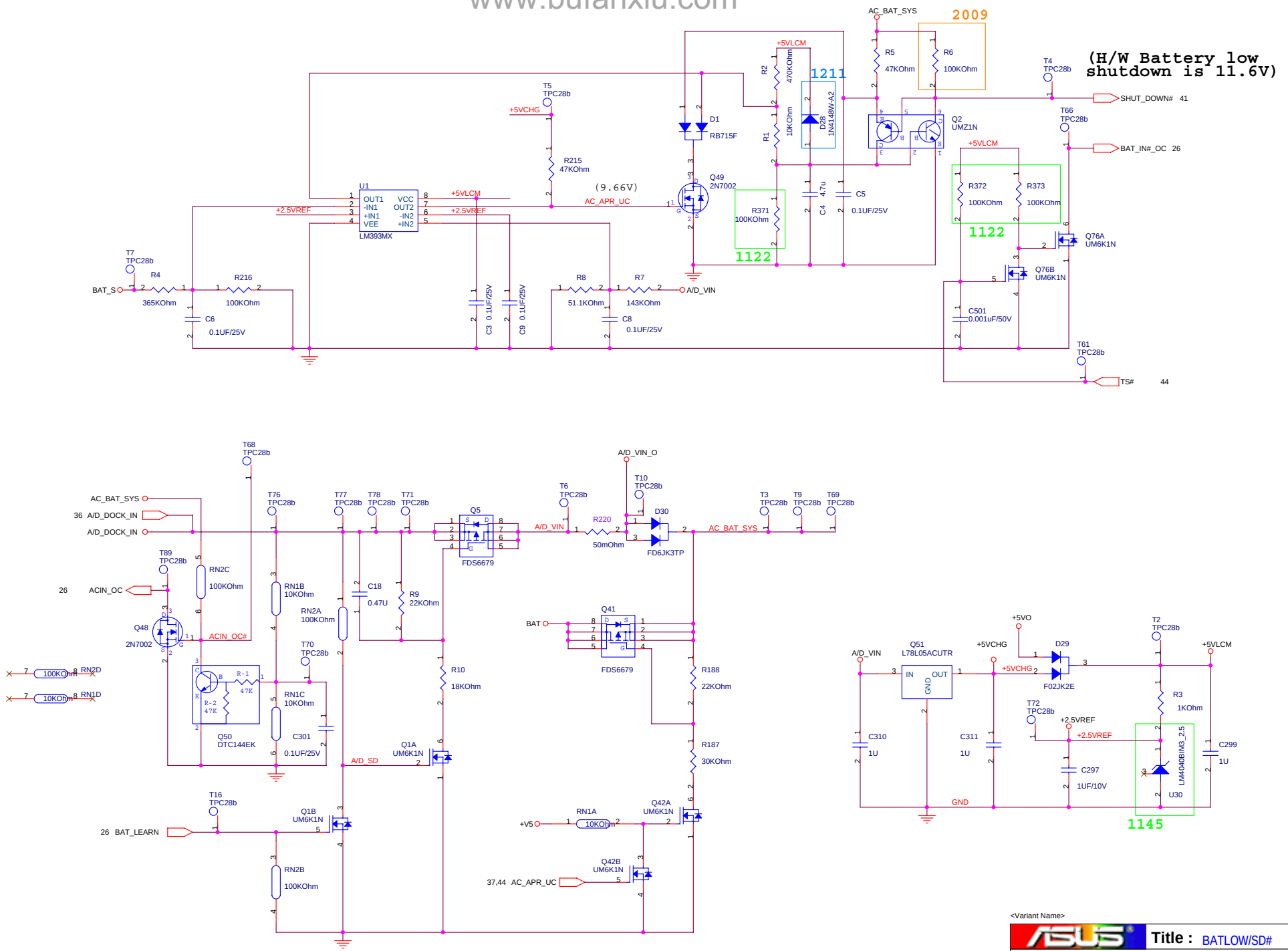

<Variant Name>

Title : BATLOW/SD#

ASUSTek COMPUTER INC. NB1 Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3N	2.0

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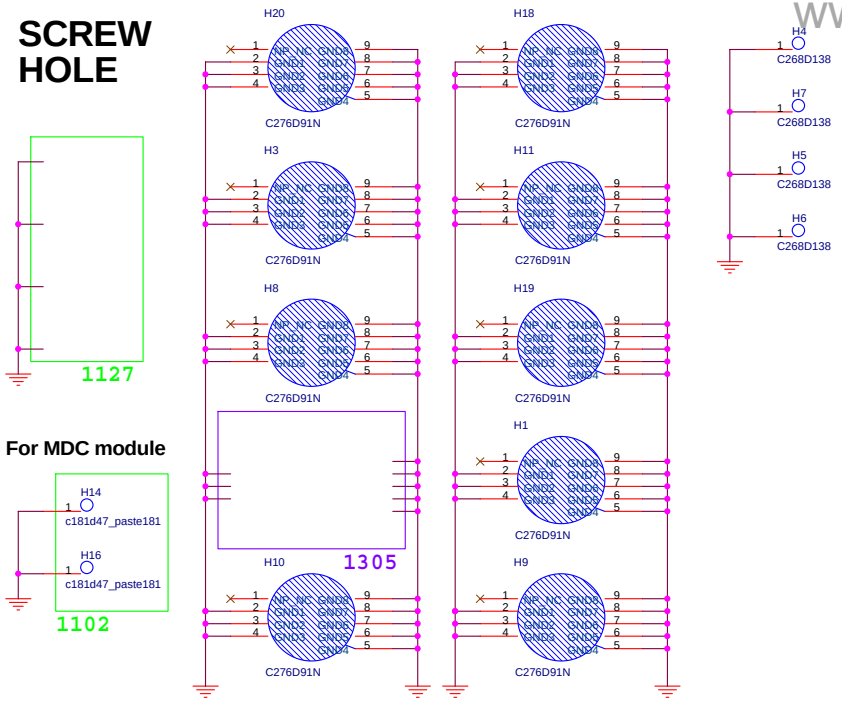
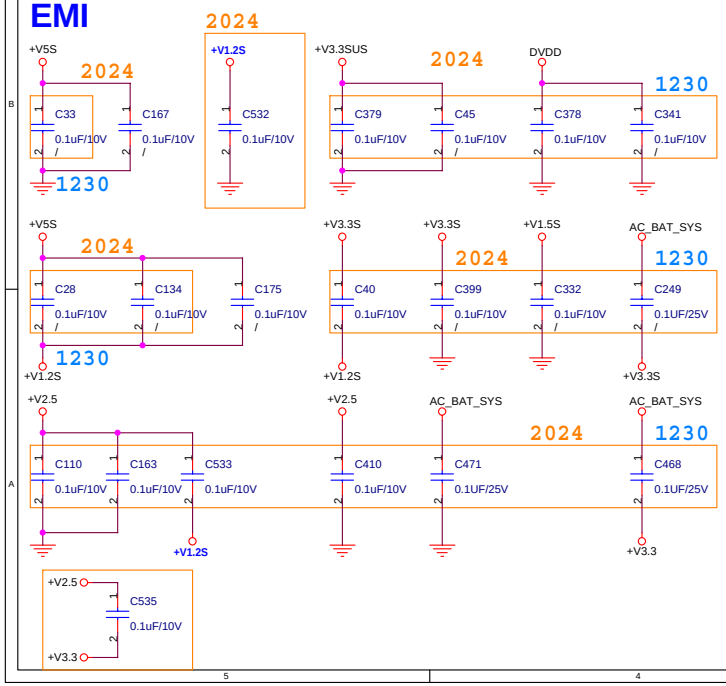
SCREW HOLE



CPU Throttling(BIOS setting): 90 degree C.
System shutdown(BIOS setting) : 100 degree C.
H/W shutdown(page 44, U47 , no load) : 105 degree C.

EMI



Short Pad location:
Page39: JP4,5,15,16,19,26,27
Page40: JP6,7,9,22,24
Page42: JP13,14,17,18,28,29

Don't Short Pad: JP26

JP4:+V2.5 --Power In
JP5:+V1.25S
JP6:+V2.5
JP7:+V1.2S
JP9:+VCCP
JP13:+V5S
JP14:+V5
JP15:+V1.5SUS
JP16:+V2.5 --Power IN
JP17:+V1.8S
JP18:+V12
JP19:+V1.8
JP22:+V1.5S
JP24: VREF5-->+V5A
JP26:+3VALWAYS_T-->+V3.3A(open)
JP27:+3VALWAYS_M-->+V3.3A(short)
JP28:+V3.3S
JP29:+V3.3

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	20 mils

37.5 OHM	WIDTH
TOP/BOT	12 mils

42 OHM	WIDTH
TOP/BOT	10 mils

55 OHM	WIDTH
TOP/BOT	5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	7 mils/ 10 mils

100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#

CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

<Variant Name>

Title : SCREW HOLE
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size: Custom | Project Name: A3N | Rev: 2.0
Date: Friday, April 23, 2004 | Sheet 46 of 49

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

ASUSTek COMPUTER INC. NB1

Title : SECOND SOURCE

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 47 of 49

Rev	Date	Description
R1.00	03/12/19	1. Initial release.
R1.1 Green Block	04/02/03	1. Connect SDD0,SDD1 for RICOH request. Page 22. 2. Add MDC screw hole P/N & footprint. Page 46. 3. Connect CardBus chip INTC to PCI_INTD#. page 22. 4. Change CB_SD# location from KBC to ICH4 GPIO25. page 15,21,26. 5. Delete PCMCIA debug card function. page 18,23,29. 6. Host clock frequency select failed.Add a pull-down R to FS3 so that FS[4:3]=00 and Host clock frequency=100MHz. page18. 7. Load wrong value. Change RN39~RN48 from 56Ohm to 10Ohm. page 6. 8. Load wrong value. Change pull-up RN . page 37. 9. The value in M3N schematic is wrong. Change HUB_RCOMP_ICH4 pull-up R from 48.7KOhm to 48.7Ohm. page 14. 10. Modify +V3S to +V3.3S. page 30. 11. Can not boot in battery mode.Remove C497. page 37. 12. Modify 20-pin connector pin define and add DJ_LED function for new touchpad. page 26,36. 13. Due to height limitation, change BATT CONN. page 44. 14. Remove the pull-up RN75B because AC_APR_UC has been pulled-up in page 45. page 37. 15. Change CRT CONN because the original one was reversed. page 12. 16. C271 change form 10UF/25V/X5R to 15UF/25V/POSCAP. page 43. 17. U50 VCC change from +5VLCM to VCC_AD(19V). page 43. 18. For wrong connection, change R354 pull-up power plane from +5VO to +5VA. page 44. 19. Change R210 from 47K to 470K/0402. page 43. 20. Add RN78 to pull high SMC_BAT and SMD_BAT, and add UM6K1N to prevent leakage current into KBC. page 26,44. 21. For Power RD request, add R370 to CHG_EN#. page 44. 22. Replace RN32 with 3 single 100K resistor. page 45. 23. Change KB CONN pin definition because R1.0 was reversed. page 26. 24. Remove INVTER_A from KBC and load L33 because BIOS RD decide to use NB to control the pannel backlight. page 12,26. 25. Because P67/AN8 of KBC38857 cannot receive PWM signal, move CPUFAN_SPD_A to P57/DA2/PWM11 of KBC38857. page 26. 26. Change LEDs' power to 5V level. page 36. 27. Modify PCMCIA socket footprint. page 23,46. 28. Combine connector : Change CON1,delete CON3,CON4. page 12, 34. 29. Swap LAN connection(J2 pin5~12) for wrong connecting. page 33. 30. Modify PM_RSMRST# circuit. page 37. 31. For cost down, change X5,X7. page 19,30. 32. Combine two NC7SZ14P5 into one SN74LV14APWR for cost down.page 37. 33. To reduce jitter when charging, add R376,C520&C521. page 43. 34. For M6N R1.1 wrong connection, change Audio DJ DJ_SCAN pin from KSO4 to KSO1. page 26,35. 35. For Power RD request, add two beads L53&L54 at Vin Side. page 38. 36. Modify EDID and panel ID optional circuit. page 12. 37. Change CLR_DJ# to P53 because P54 of M38857 cannot be configured as output. page 26. 38. Add R377 for Power RD request. page 43. 39. Based on Ricoh's suggestion, remove CB_AGND and connect all AGND to generic GND. page 21,22. 40. For cost down, change X4. page 44. 41. Modify for battery 4S2P and 4S1P application. page 26,43,44. 42. For EMI RD request, change Cap of CRT Pi-filter from 3.3pF to 15pF. page 13. 43. Delete spread spectrum IC ICS91718 circuit because few model use it and not easy to buy. page 18. 44. Change C172 & C173 from 22pF to 5pF and unload R125 to obtain more accurate 8MHz frequency. page 26. 45. For cost down, Power RD request to change Q9&Q11 to 07-005198012, U30 to 06-006002411, and U50 to 06-010112010. page 38,43,45.

Rev	Date	Description
R1.1	04/02/10	46. For Power RD request, change , C266 from 33pF to 220pF, C279 from 0.1uF to 0.01uF. page 41,43. 47. Change U29 P/N for ME. page 31.
R1.2 Blue Block	04/02/19	1. LAN_RST# changes to 10K Ohm pull-down to GND. Page 15. 2. To be able to hear low frequency in headphone mode, change C423 & C424 from 10uF/10V to CE30,CE31 47uF/6.3V. Page 31. 3. Pull high BAT_IN#_OC, whose OC means Open Collector, to +V3.3 at KBC. Page 26. 4. There is only one SS0540 in A3N, change to 1SS355. page 35. 5. The power of LCD EEPROM connect to +V3.3S_LCD. When BIOS want to read EEPROM data, the EEPROM is still OFF,because +V3.3S_LCD is not enabled at this moment. Change EEPROM power to +V3.3S. page 12. 6. Change R360,R363,R364,R366,R367,R378 value for charger at C.C. mode and change R200,R201,R204,R352 at C.S. mode to get more accurate current limit value. page 43. 7. Add de-POP(reduce pop noise) circuit. page 31. 8. Change Fan control function from PWM mode to DC mode. page 35. 9. Based on Power RD's request, change Q33,R169,R148,R324. page 40,41. 10. S5N can not turn on some panels since its diodes in inverter circuit have higher forward voltage. Follow S5N, change DAP202K and 1SS35 in inverter circuit to Schottky diode RB717F and RB751V-40 respectively. page 12. 11. Electrical characteristics of diode 1SS35 and 1N4148-A2 can be compatible, but 1N4148-A2 has lower price. For cost down, change 1SS355 to 1N4148-A2. page 12,16,21,35,37,40,43,44,45. 12. Change "Back light adjust" function from North Bridge to KBC. Change "CUPFAN_SPD_A" from KBC to ICH4 for BIOS request. page 8,12,26,35. 13. For cost down, change audio AMP from APA2020A to G1420. page 31. 14. A3N R1.1 uses the same AC_IN jack as L3F, which was found easy to be damaged. Change it to solider one used on A2. page 36. 15. Follow M6N and W1N to modify RTC circuit. page 15. 16. Un-mount Q59 and RN81 to control WLAN led directly from SB's GPIO pin: 802_LED_EN#. page 36. 17. Swap 1394 TPB0+/-,TPA0+/- for smoother layout. page 22. 18. X4 is dip type and at top side which may be lost in SMT IR re-flow for bottom side. Change X4 to SMD type. page 44. 19. Add mini-PCI and USB WLAN hardware disable circuit page 12,15,20. 20. QT report a bug: The "Center/Subwoofer Speaker Out" is invalid after setting "Number of Speakers" to 6-channel mode for 5.1 speaker output and then executed "Speaker Test". Modify relative circuit. page 30,32. 21. Fine tune audio amp low-pass frequency. page 31. 22. Delete RN79 because after experiment we find it can be un-mounted. page 36. 23. Remove LCD EDID relative circuit. page 8,12. 24. Combin R191,R308,R380 and R381 into 4R8P RN88. page 26. 25. Follow S5N to modify CRT_DDC circuit to prevent current leakage. page 13. 26. Although crystal DIP type is cheaper than SMD type, but costs more manpower. Change X5 and X7 back to SMD type. page 19,30. 27. Improve accuracy of reading fan speed. page 35. 28. Swap RN4 and pin8,9 of RP4 for smoother layout. page 13,17. 29. For cost down, change U6 and U12 NS LM358MX (06-010008000) to TI LM358ADR (06-010112010). page 30,35. 30. For EMI RD's request to modify BOM. page 18,19,22,30,31,32,33,46. 31. Add description of choosing 855GM or 852GM/GME/GMV platform by changing R148. page 40. **32. Debug code will stop at "A0" or "06". Modify SMBus layout: 1. Daisy chain routing. 2.Don't cross power plane when the trace refer to power plane. Page 17.**

ASUSTek COMPUTER INC. NB1

Title : REVISION(1)

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

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Rev	Date	Description
R1.00	03/12/19	1. Initial release.
R1.3 Purple Block	04/03/11	1. Pin23, ISOLATEB, of LAN 8100CL need to be low in S3. Follow MB P4PE-X to connect it with PM_SLP_S3#. page 19. **2. Debug Code will stop at "13". Change SMBus Pull-High RN29 from 4.7KOhm(0402) to 1KOhm(0603). page 17.** 3. Improve MIC layout. page 12,32. 4. For Power RD's request to modify charger circuit. page 43,44. 5. Delete screw hole H2, to prevent CN7 short with H2. Layout engineer create a new screw hole. page 46. 6. For Power RD's request to modify BOM. Change R108 from 100K to 75K for OCP, un-mount R93 and mount R94 to meet Intel CPU spec. page 38.
R2.0 Orange Block	04/04/15	1. Sometimes Debug Code will stop at "00" in ON/OFF test. Modify power sequence circuit , delete R163. page 38,40. 2. Based on request came from factory to update all testpoints' symbol because all testpins are changed from 75mil to 68mil. All pages that include test points. 3. Power team request, cost down D51 part. page43. 4. Fine-tune R385,R386 and R387 to get more accurate level of fan ON/OFF detection. page35. 5. When system with battery only. System can't be power on after push Force OFF button SW6. Because SW6 connect to SHUT_DOWN#, but this signal will be latch low(power design: when battery low, page 46 : battery low detect circuit will issue low than latch it.) when it is at low state. Don't connect SHUT_DOWN# to SW6 at page 37.(SHUT_DOWN# already connected to 3V_ON at page 41. Connect SW6 to U25, and change D40 to 1N4148(delete at item 2015). Page 37. 6. Because A3N use SW6 as "Force OFF" button ,not "Reset" button. We don't need connect SW6 to PIC16C54C. Delete D24.page37,44. 7. Can't turn on Audio DJ when system only with battery and no adapter. Because +V3.3SUS will be turn off when system only with battery. Need turn on +V3.3SUS by connect DJ_SW# to 3V_ON. Change D45 to DAP202K. Page 37. 8. LAN crystal accurate is 39.2ppm, it can't meet spec. +/-30ppm). Change from 15pF to 18pF to meet spec. page 19. 9. Some system can't boot by battery only. Because signal "SHUTDOWN#" be latch at low state. Change R6 value from 470K to 100K. Page 45. 10.QT bug : Noise occur from headphone via speaker out jack. Change R124,R298,R285 from Bead to 0 ohm. Page 30,31. 11.The Power LED should not be bright when enabled Audio DJ in power off mode. Page 36. 12.The inductor will cause the 2.5V power control loop unstable. Change L40 to R389 Page 19. 13. Balance the LED Brightness. Fine tune R value,R140 470-->220,R311,R312 470-->1K. Page 36. 14. G571(U49) 593 Control Signal(U37) VPPD0 : VPPEN1 VPPD1 : VPPEN0 Otherwise, CardBus Card may be destroyed. Page 23. 15. When issue OTP_RESET#, system can't be turn off & display white screen. Because LTC3728 can't be shutdown by only put low 3V_ON. Need shutdown +V3.3SUS & +5VO at the same time. Delete D40. Page 37. 16. Change Q63,Q66,Q71 and no load Q63,R338,C482,R354,R358,C502,U47 for cost down. page 35,37,44. 17. Add test point for Taipei Factory request. page 6,12,15,16,19,30,36,37,38,39,42,43,44 18. QT bug: Pop noise can be heard via headphone when system boot, restart and resume from S3. Modify De-Pop circuit. page 31,37. 19. Taipei factory request : Add R391 for different battery charge current test at 8 cells and 4 cells. Page44. 20. EMI request, load C144, C525. page 32.

Rev	Date	Description
R1.00	03/12/19	1. Initial release.
R2.0 Orange Block	04/04/15	21. ICH4 GPIO [24:43] , default state is output high, if PID_[0:3] be connected to GND by LCD cable, these GPIO will issue +V3.3(default output high) short to GND during system power on. Add R=2.2K to prevent this kind of situration. Page 15. 22. Measurement team Problem: VGA EA fail below items 1,V-SYNC:under shoot over 30% of high level voltage range. 2,H-SYNC:over shoot over 30% of high level voltage range, under shoot over 30% of high level voltage range. Change Change C304, C305 from 5pF to 33pF. Page 13. 23. EMI request use Choke on USB & 1394 ports. Delete option R, don't co-layout. Page 22,34. 24. EMI request : Add C531,C532,C533,C535. Delete C147,C433. Change C110,C163 connection. Change C410 location. Change C378,C379,C410,C163,C110 to 0.1uF/10V. Change C471,C468 to 0.1uF/25V. Change C45,C33,C28,C134,C332,C399,C341 to 0.1uF/10V and don't load. Change C40 to 0.1uF/10V. Change C249 to 0.1uF/25V and don't load.Page 10,46. Change R104 from 0 ohm to bead. Page 31. 25. Change C26,C98,C104,C325(page3), C362(page7), C324,C329(page9), C436(page14), C190,C441(page16), C366,C367(page19), C247(page21), C467,C473,C478(page22), C236(page23), C209,C210,C211,C242(page40), from 0.01uF/25V to 0.01uF/10V. Use 10V is OK. 26. Measurement team Problem: VGA EA fail in rise time and fall time of RGB signal at resolution 1024X768 at 60Hz. Change L6,L7,L8 from 75Ohm/100MHz to 70Ohm/100MHz. Page 13. 27. Load FAN on/off component : /FAN_SPD. page 35. 28. Change L53,L54 from 09-012400000 to 09-012400001 for cost down. page38. 29. CON1,CON7,CON12,CON15 and J4 change to formal P/N. page 12,24,25,36,44. A3L. For A3L platform : change U32 to 852GM P/N:02-010185200,R148. page 6,7,8,9,40.

ASUSTek COMPUTER INC. NB1

Title : REVISION(2)

Engineer: John Hung

Size	Project Name	Rev
Custom	A3N	2.0

Date: Friday, April 23, 2004 Sheet 49 of 49