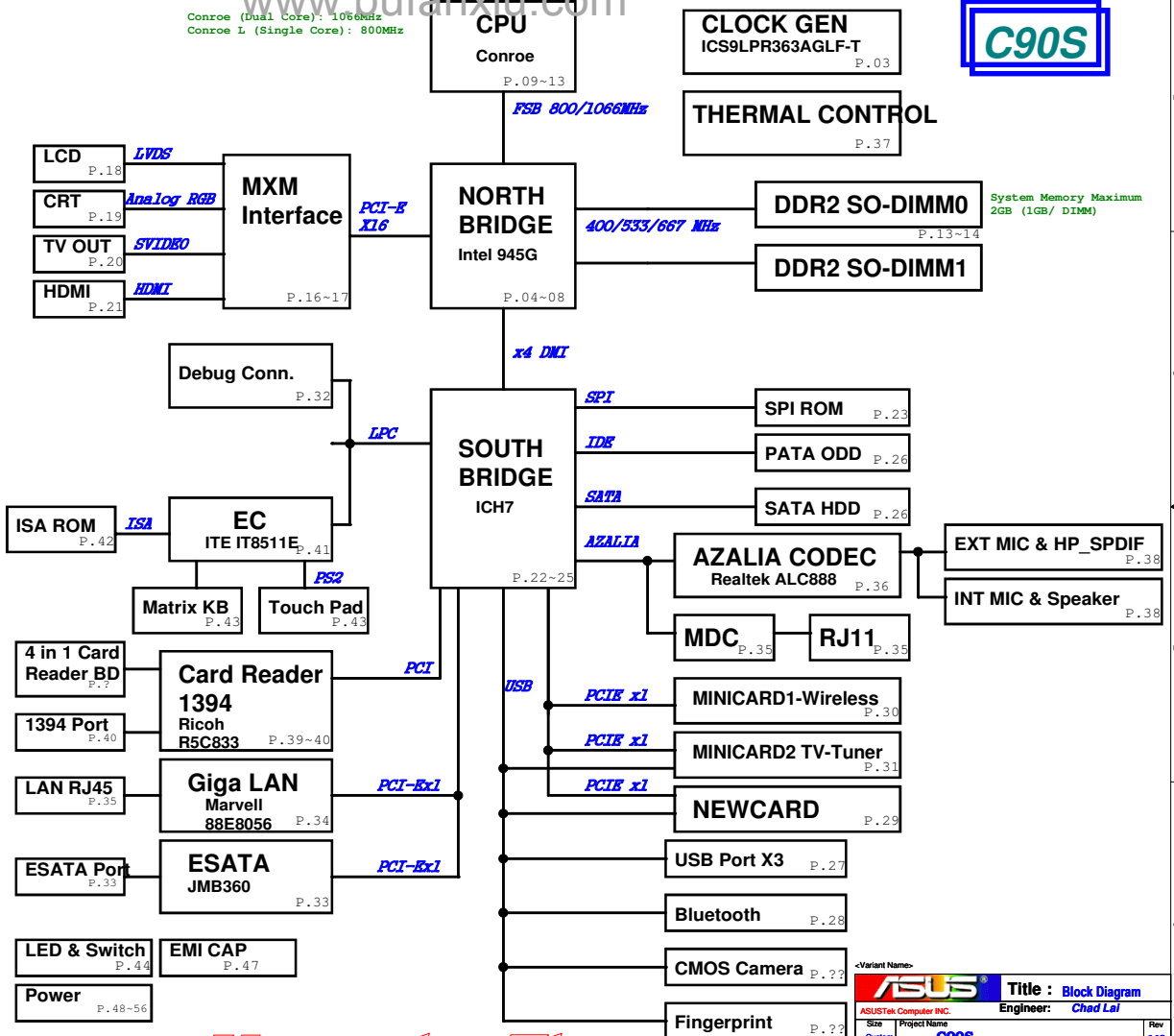




1 BLOCK Diagram
 2 HISTORY
 3 Power Sequence
 4 CLKGEN-ICS9LPR364AGLF-T
 5 NB-945_1
 6 NB-945_2
 7 NB-945_3
 8 NB-945_4
 9 NB-945_5
 10 LGA775-1
 11 LGA775-2
 12 LGA775-3
 13 LGA775-4
 14 DDRII_1-DIMMs
 15 DDRII_2-Termination
 16 MXM Interface
 17 MXM Power & GND
 18 NBIO_1-LVDS & Inverter
 19 NBIO_2-CRT
 20 NBIO_3-SVIDEO
 21 NBIO_4-HDMI Connector
 22 SB-ICH7-1
 23 SB-ICH7-2
 24 SB-ICH7-3
 25 SB-ICH7-4
 26 SBIO_1-SATA_HDD & IDE_ODD
 27 SBIO_2-USB & DAUGHTER
 28 SBIO_3-Bluetooth & G-Sensor
 29 SBIO_4-EXPRESS CARD
 30 SBIO_5-Mini Card1-Wireless
 31 SBIO_6-Mini Card2-MINICARD
 32 SBIO_7-TPM/Debug/I2C_GPIO
 33 PCIE-ESATA-JMB360
 34 PCIE-GLAN-Marvell 88E8056
 35 MDC&RJ45/RJ11
 36 Audio_1-Realtek ALC888
 37 Audio_2-Speaker / MicA
 38 Audio_3-Phone Jack
 39 PCI-Reader-R5C833
 40 PCI-Reader-Connector
 41 EC-IT8511E
 42 ECIO_1-ISA ROM & KB & TP
 43 ECIO_2-FAN
 44 LED & SW
 45 DC IN & BAT IN & Discharge
 46 Screw Hole & Nut
 47 EMI CAP
 48 POWER_FLOWCHART
 49 POWER_CHARGER
 50 POWER_SYSTEM
 51 POWER_VCORE
 52 POWER_I/O_DDR & VTT
 53 POWER_I/O_+3VA
 54 POWER_GOOD_DETECTOR
 55 POWER_LOAD SWITCH



ASUS Title : Block Diagram
 Engineer: Chad Lei
 Project Name: C90S
 Date: 01/30/2007
 Sheet 1 of 55

<< Kennedy_Zhang >>

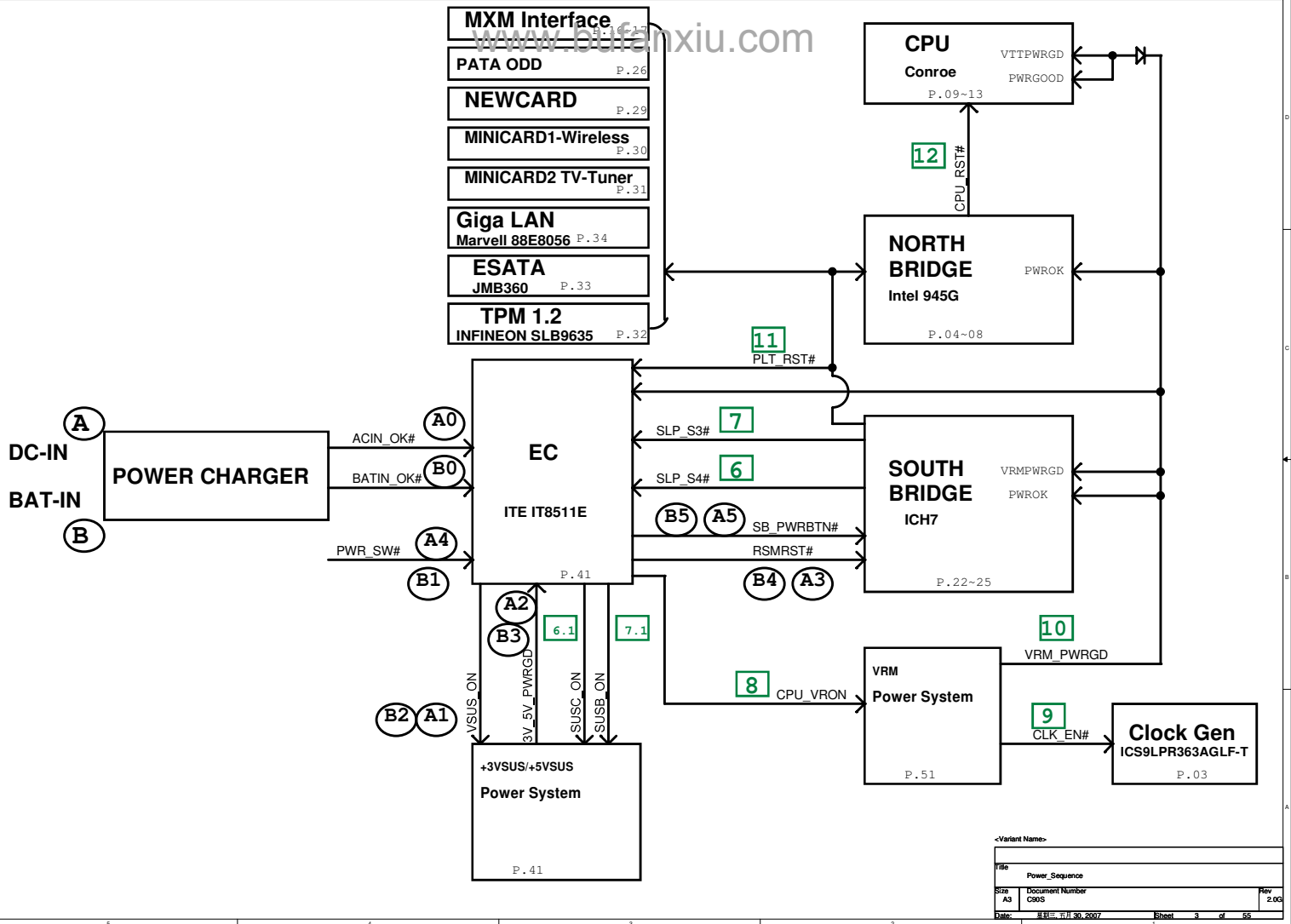
Rev	Date	Description
1.0	04/10/06	1. Initial release.(From Z84F)
1.1	08/08/06	1. Change Audio Codec from AD1988B to ALC888(Page 35) 2. Change AJ2, AJ3 to Azalia type 3. Correct RN2 Connection 4. Add PR5312, PR5313 to fix NANYA DIMM S3 fail issue(Page 62) 5. MXM_PWROK : remove R80(Page 19, Page 28) 6. PR5308 change to 1.2K 1% 0603(Page 62) 7. Change Inverter Connector type (12pin) & Pin define CON7(Page 22) 8. Remove : AR1, AR6, AR7, AR8, AR13, AR14, AR15, AR18, AR19, AR21, AR22, AR34, AC1, AC2, AC4, AC5, AC7, AC8, AC11, AC13, AC23, AC25, AC26, AC27, AU2, AQ6, AQ7, AQ9, AQ12 Add : AC81-AC85, AR71, ARN3, AD3, AD4, AL16
	08/10/06	1. Remove T100-T118(Page 41) 2. Add PU5901, PC5905, PC5906 for CIR Power(Page 64) 3. PR5308 change to 150K 1% 0603, PC5312 change to 1500PF 0603(Page 62) 4. Add PR5060, PR5061(Page 61) 5. PR5114 change to 27K 1% 0603(Page 60) 6. PR5722 change to 22K 1% 0603, Stuff PR5721(Page 59) 7. R77 change to 4.7K, Pull to +5VCHG for AC_OK(Page 20) 8. Change connection of L23, L24 9. Change CON18 P/N 10. Add D30, D31, D32, C175, C176, R136(Page 28)
	08/11/06	1. Add Audio Amp. AU100, AR100-AR103, AC100-AC107, non-stuff AC41(Page 36) 2. AC82 change to 1uF 0603, Add AU2, AC23, AC86, AC87, AR72, AR73, AJP1, AJP2, Remove AC12 3. Change MXM SMBus connection to EC, SMB1_CLK, SMB1_DAT(Page 28, Page19) 1. Change eSATA Controller from SiI3531 to JMB360(Page 31)
1.2	08/29/06	
1.0G	11/03/2006	1. C90 1.0G Gerber out
1.1G	11/03/2006	ME modify 1. <P46>MB_PAD1 change to None PTH type 2. <P42>Fingerprint & TouchPad Connector change to 12G18340120F 3. <P27>DAUGHTER change to 40PIN 12G171010404 4. <P18>LVDS change to 30PIN 12G17001030P

Rev	Date	Description

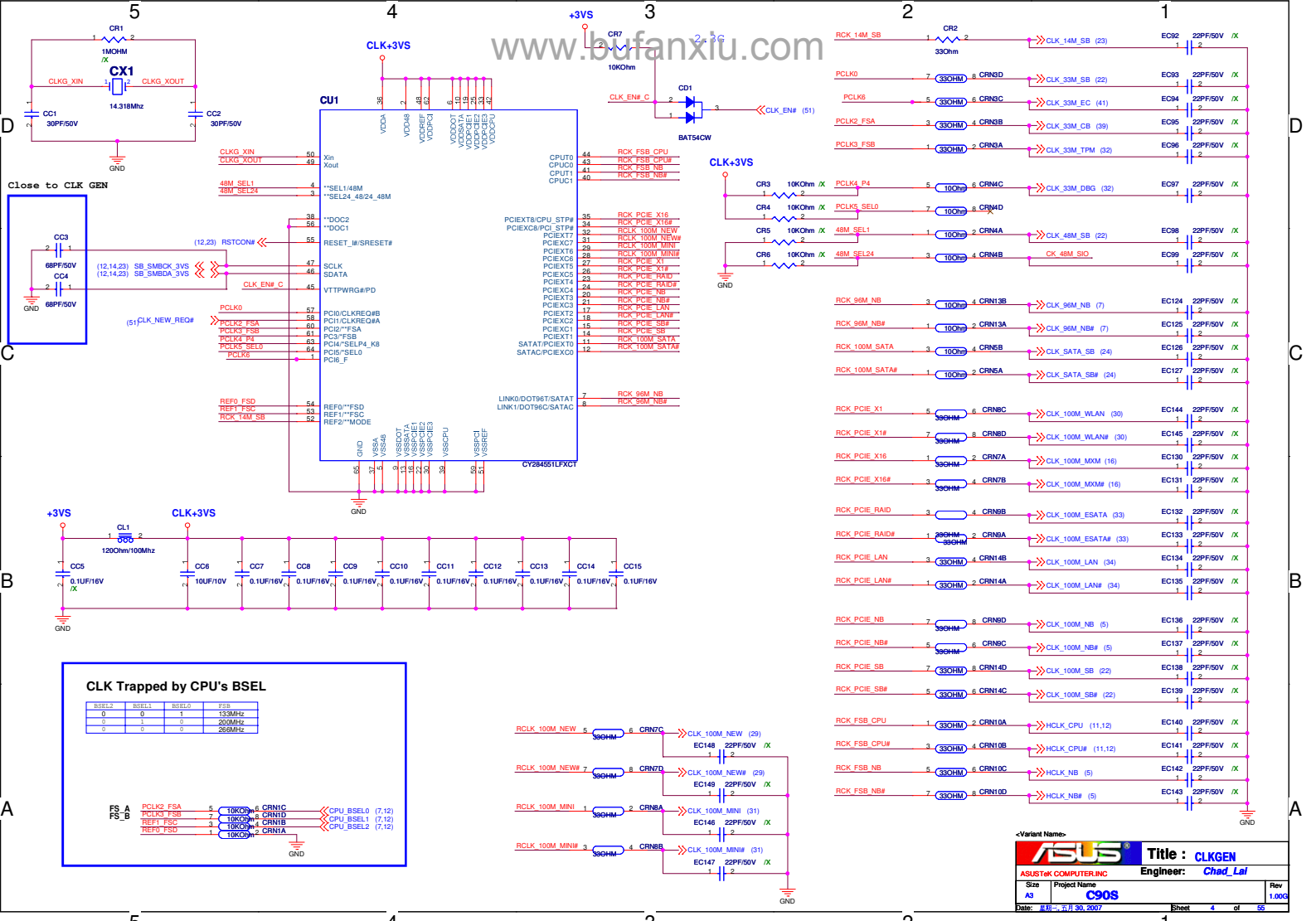
<Variant Name>

		Title : History	
ASUSTek Computer INC.		Engineer: Chad Lal	
Site	Project Name	Rev	
Custom	C90S	2.00	
Date: 8/8/2007		Sheet 2	of 55

<< Kennedy_Zhang >>

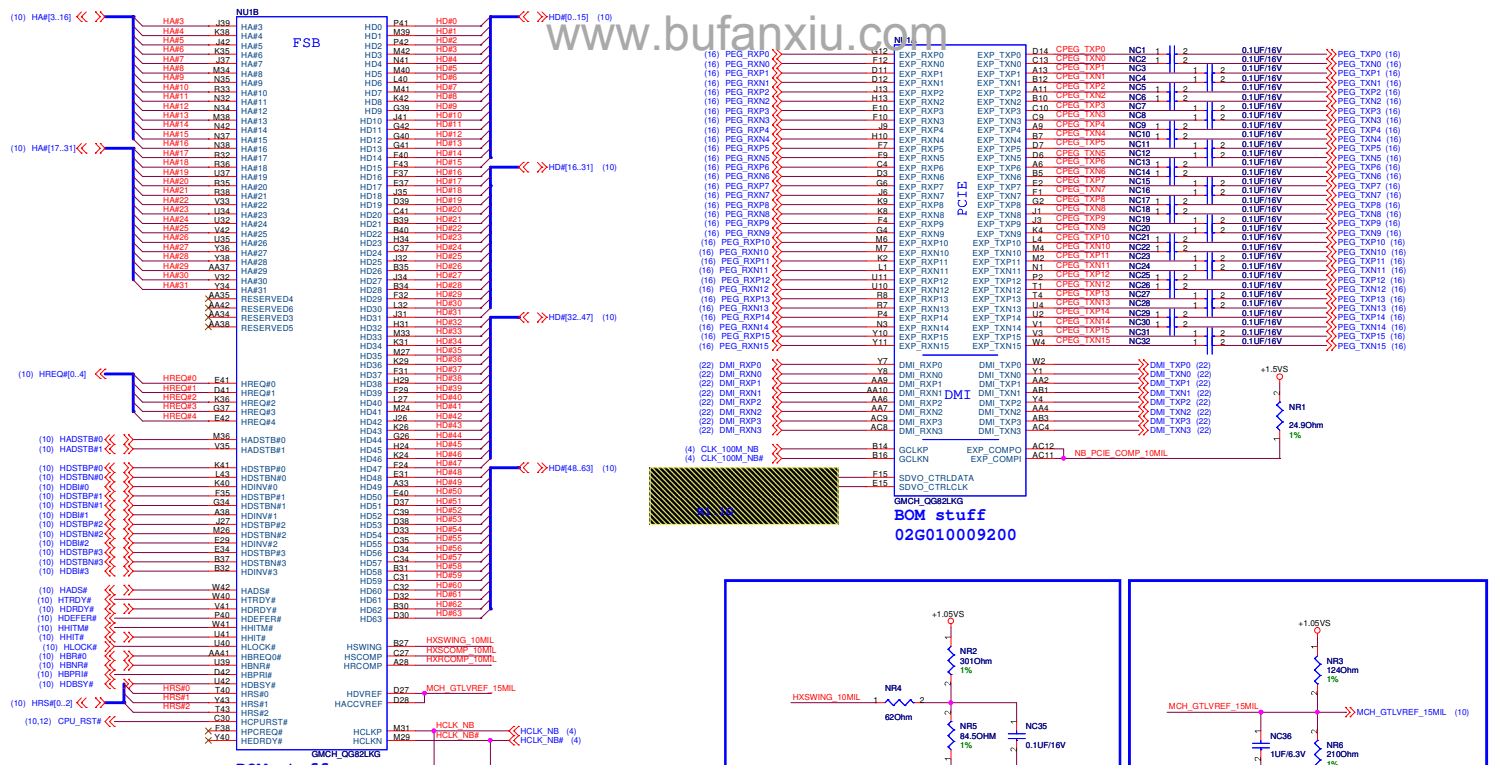


<< Kennedy_Zhang >>



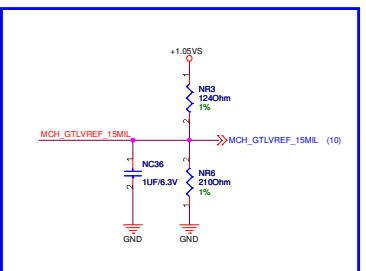
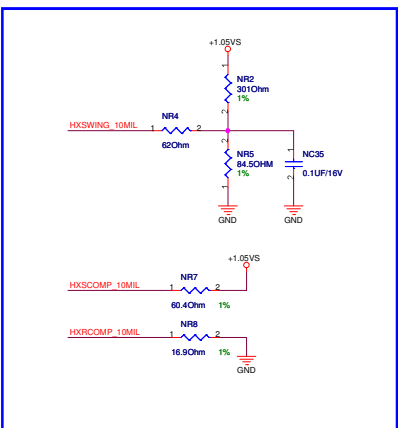
<< Kennedy_Zhang >>

ASUS Title: CLKGEN
 ASUSTek COMPUTER INC Engineer: Chad Lai
 Size A3 Project Name C90S Rev 1.000
 Date: 08/30/2007 Sheet 4 of 55



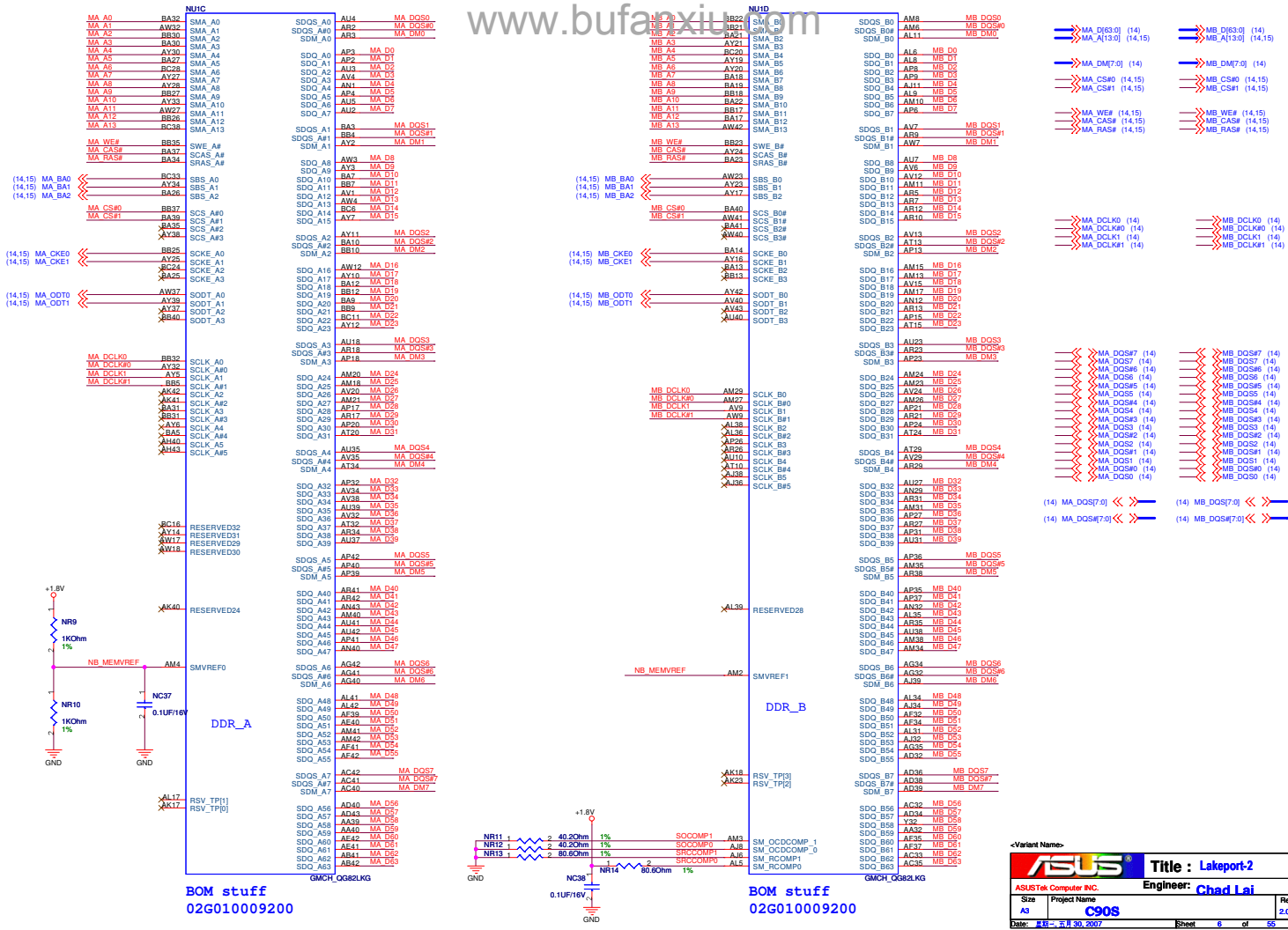
BOM stuff
02G01009200

BOM stuff
02G01009200



ASUS
ASUSTek Computer Inc.
Title: Lakeport-1
Engineer: Chad Lai
Size A3 Project Name C90S
Rev 2.00
Date: 03/30/2007 Sheet 6 of 55

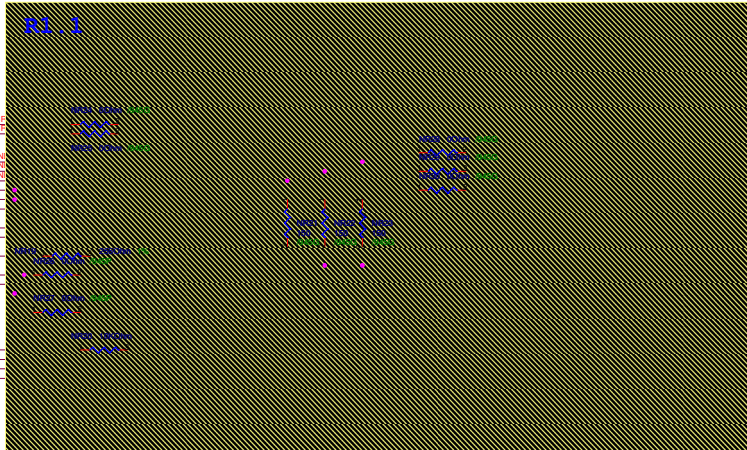
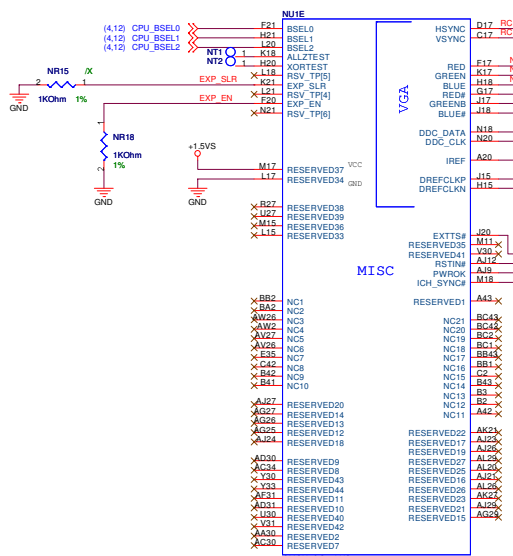
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

ASUS Lakeport-2
 Title: Lakeport-2
 Engineer: Chad Lai
 Project Name: C90S
 Rev: 2.00
 Date: 08/30/2007
 Sheet: 6 of 55

* EXP_SLR : PCIEX16 Lane Reversal Strap Selection
 0 : Reverse
 1 : Normal (IPU)

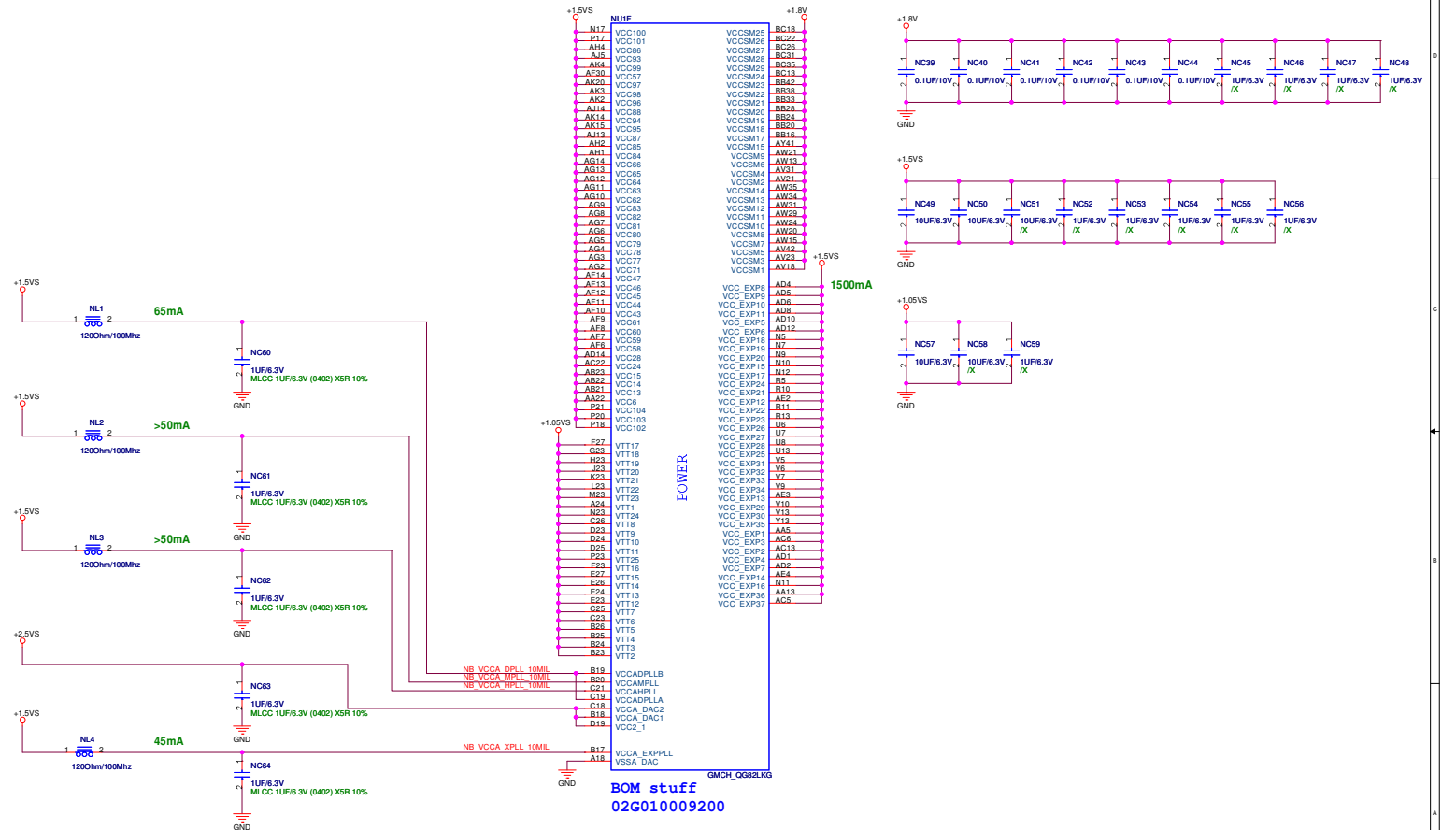


BOM stuff
 02G010009200

-Variant Name-

ASUS		Title : Lakeport-3
ASUSTek Computer INC.		Engineer: Chad Lai
Size A3	Project Name C90S	Rev 2.00
Date: 08/30/2007	Sheet 7	of 55

<< Kennedy_Zhang >>



<Variant Name>

ASUS		Title : Lakeport-4
ASUSTek Computer INC.		Engineer: Chad Lai
Size	Project Name	Rev
A3	C90S	2.00
Date: RE: W 11 30, 2007	Sheet	8 of 55

<< Kennedy_Zhang >>

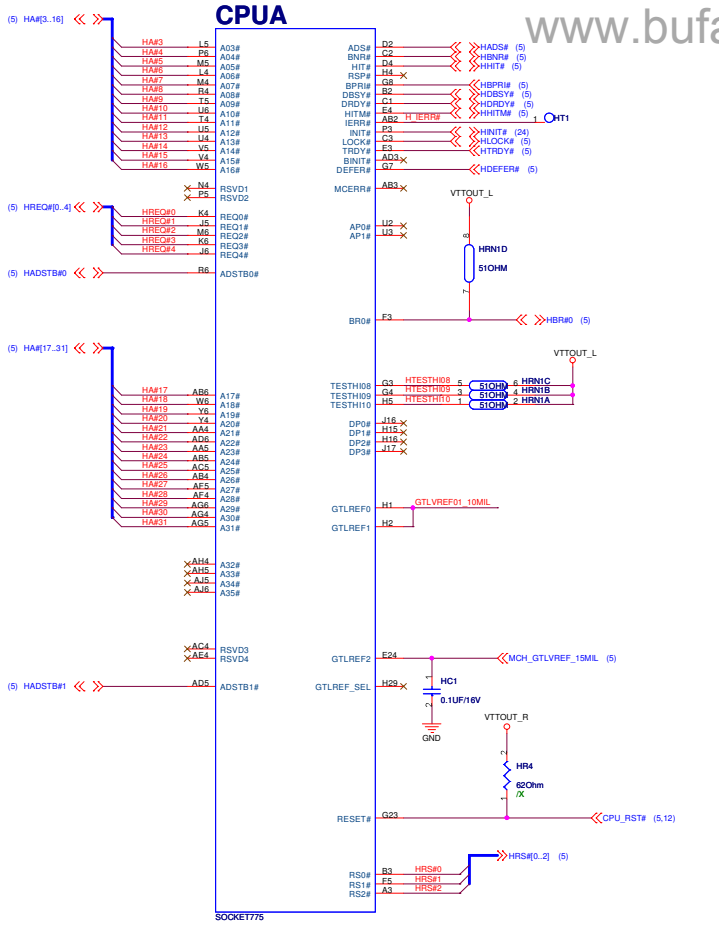


GMCH_QG82LKG
BOM stuff
 02G010009200

BOM stuff
 02G010009200

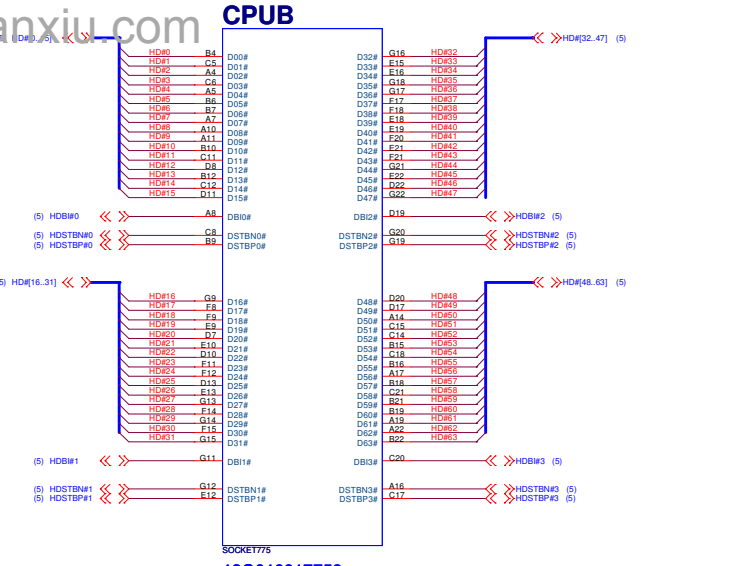
<-Variant Name-
 **Title : Lakeport-5**
 ASUSTek Computer INC. **Engineer: Chad Lai**
 Size Project Name
 A3 C90S
 Date: **08-30-2007** Sheet **6** of **55**
 Rev **2.00**

<< Kennedy_Zhang >>

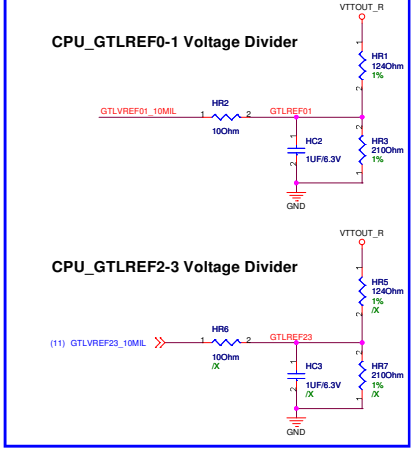


12G010917758

CPU SOCKET目前料號是:12G010917758
CPU SOCKET料號:12G010917758 change to 12G01090775N

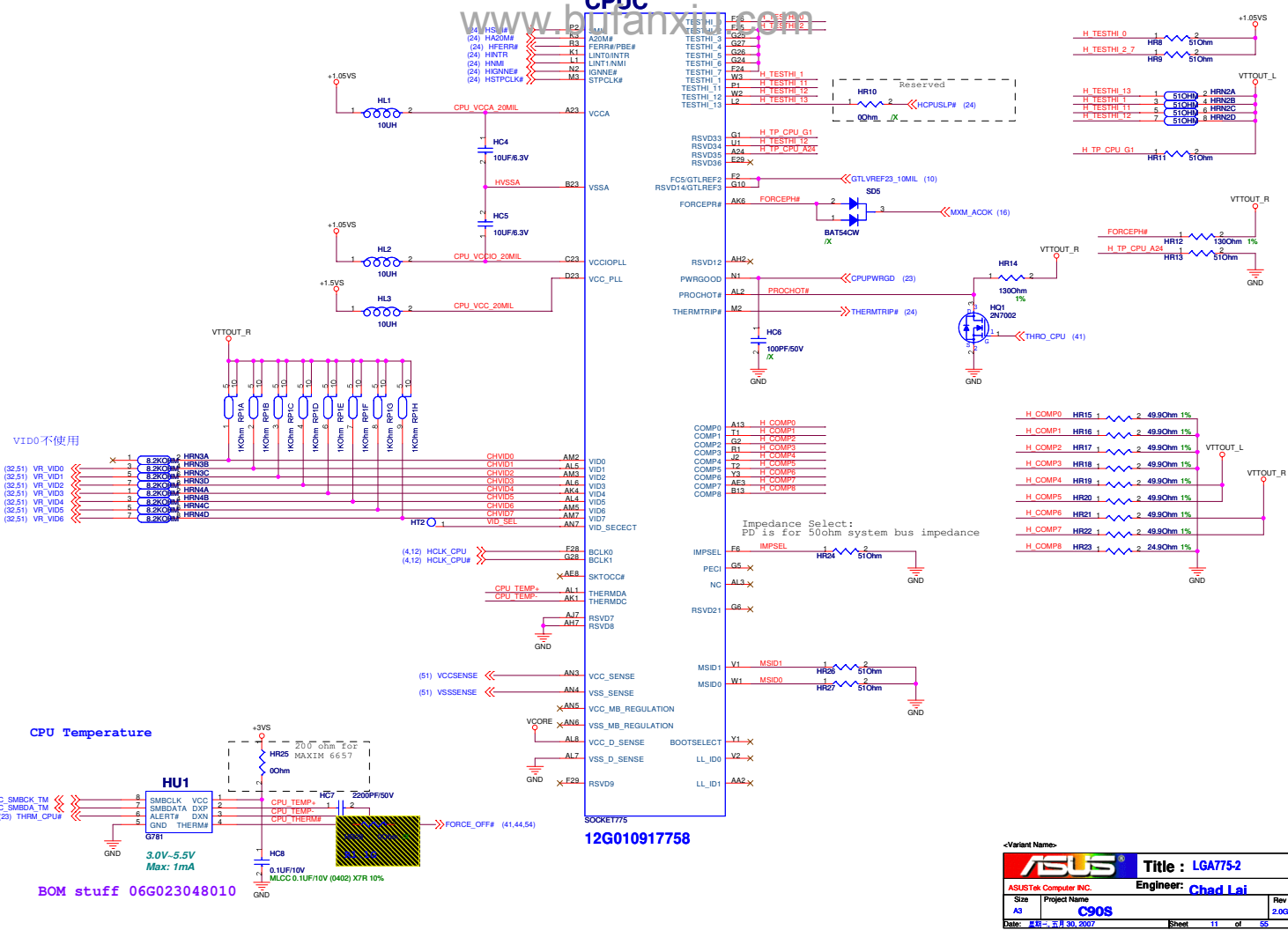


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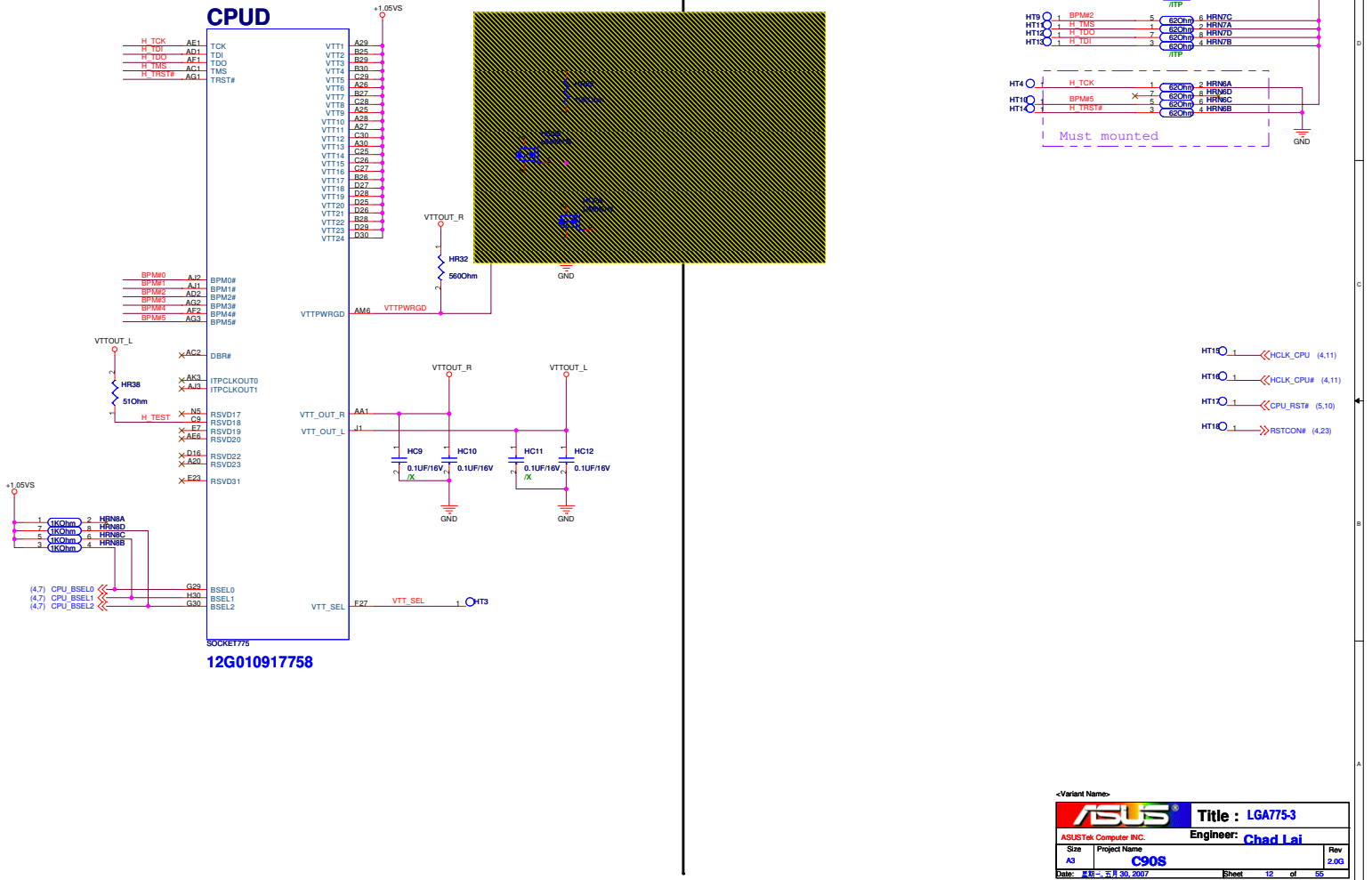


ASUS Title: LGA775-1
 ASUSTek Computer INC. Engineer: Chad Lai
 Size A3 Project Name C90S
 Date: 08-30-2007 Sheet 10 of 55

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



-Variant Name-

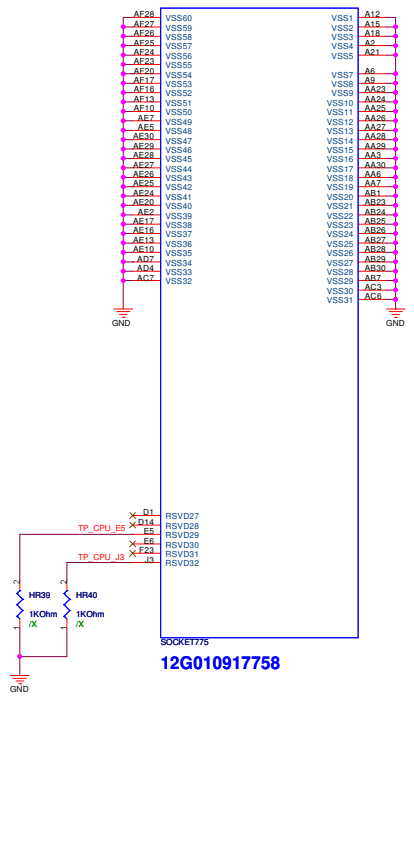
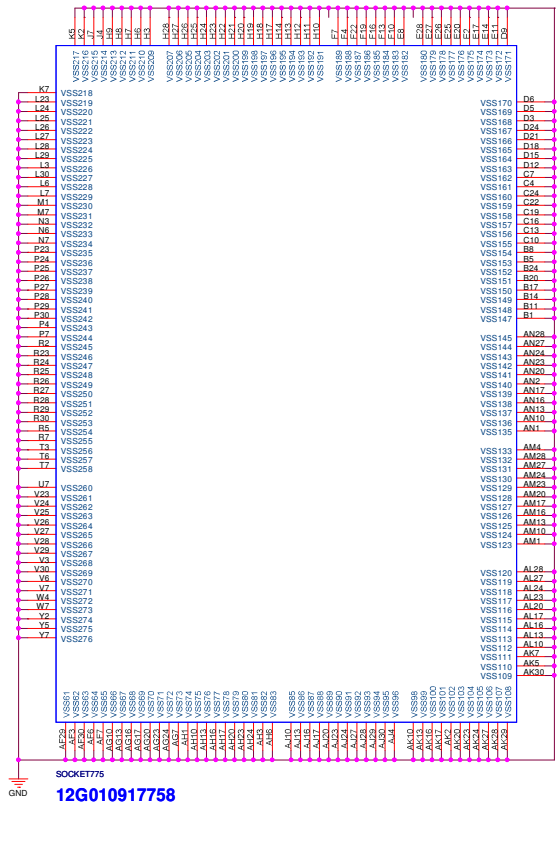
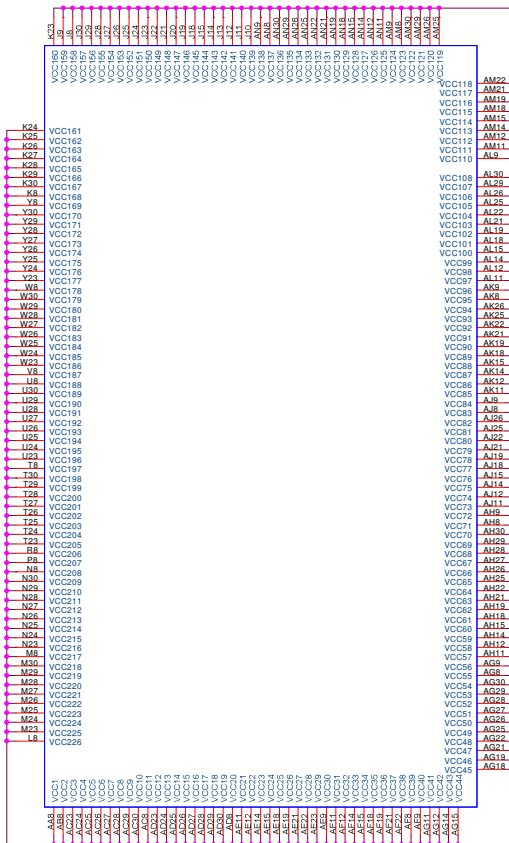
ASUS		Title : LGA775-3
ASUSTek Computer INC.		Engineer: Chad Lai
Size	Project Name	Rev
A3	C90S	2.00
Date: 08/30/2007	Sheet	12 of 50

<< Kennedy_Zhang >>

CPU_E

CPU_G

CPU_F



SOCKET775
12G010917758

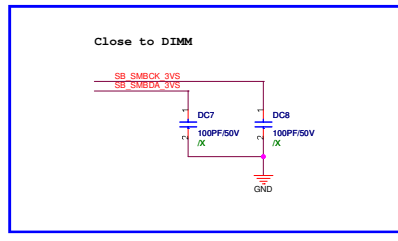
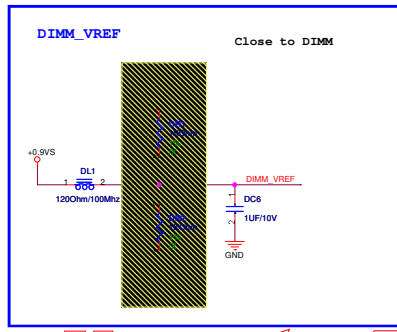
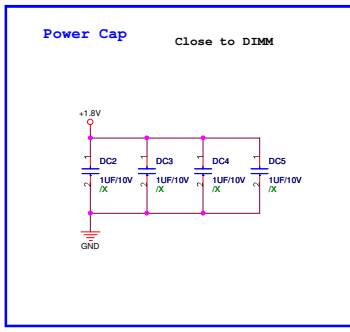
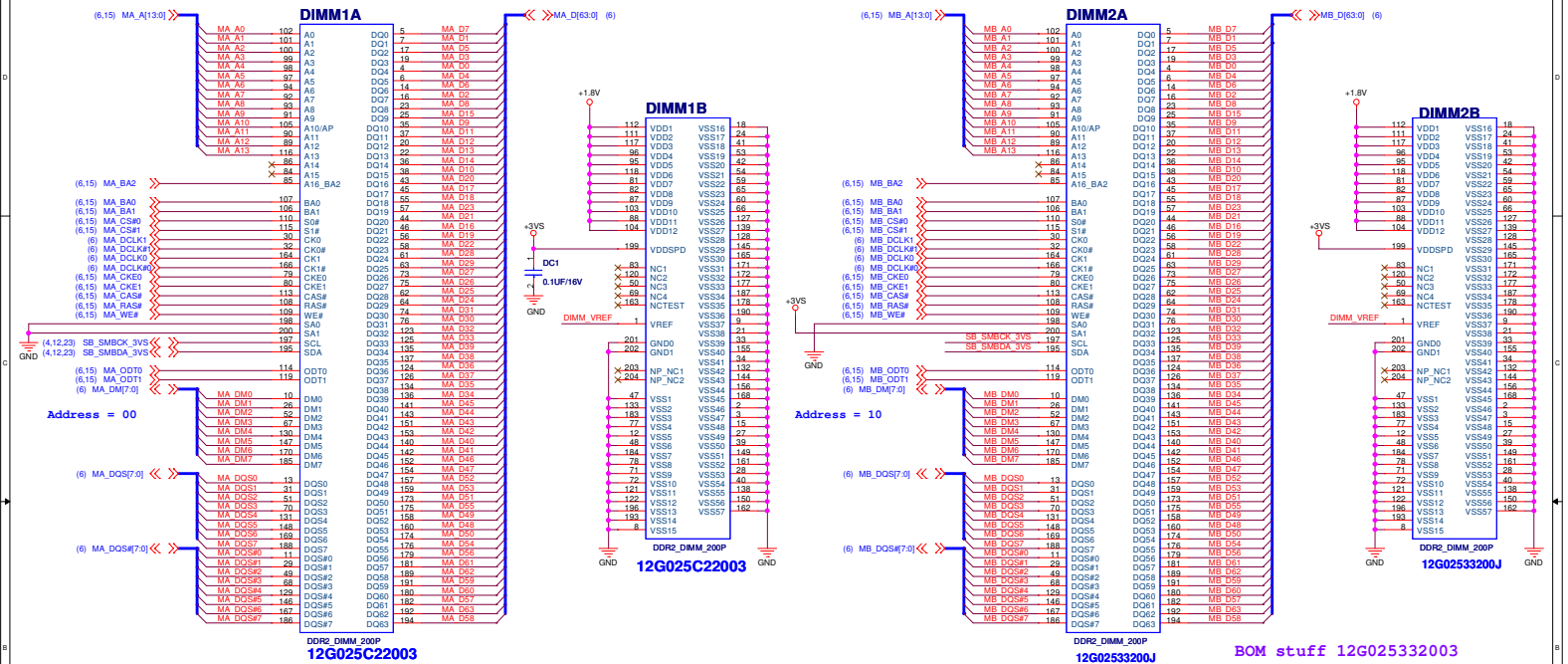
SOCKET775
12G010917758

SOCKET775
12G010917758

-Variant Name-

ASUS		Title : LGA775-4	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size	Project Name	Rev	
A3	C90S	2.0G	
Date: #B# - #M# - #Y#	Sheet	13	of 55

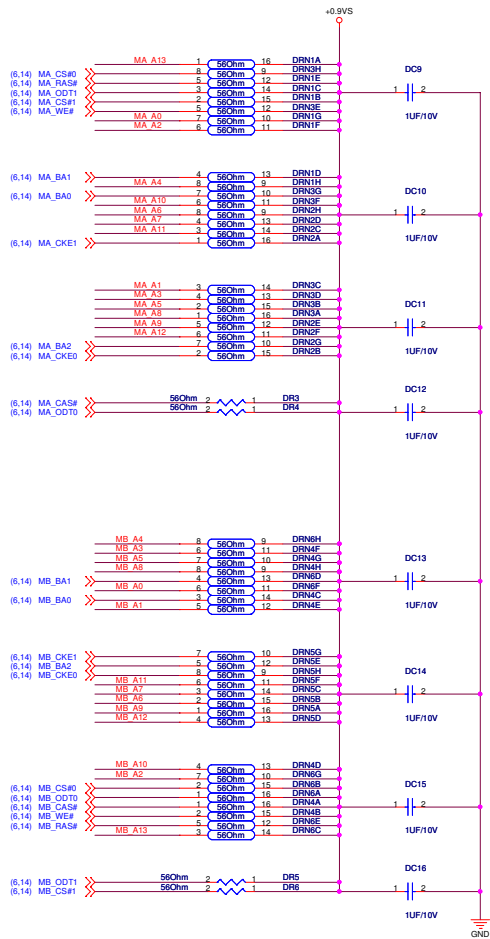
<< Kennedy_Zhang >>



ASUS Title : DDR2 SO-DIMMs
 ASUS/STek Computer INC. Engineer: Chad Lei
 Custom C90S
 Date: #18 - 11/30/2007 Sheet 14 of 55

« Kennedy_Zhang »

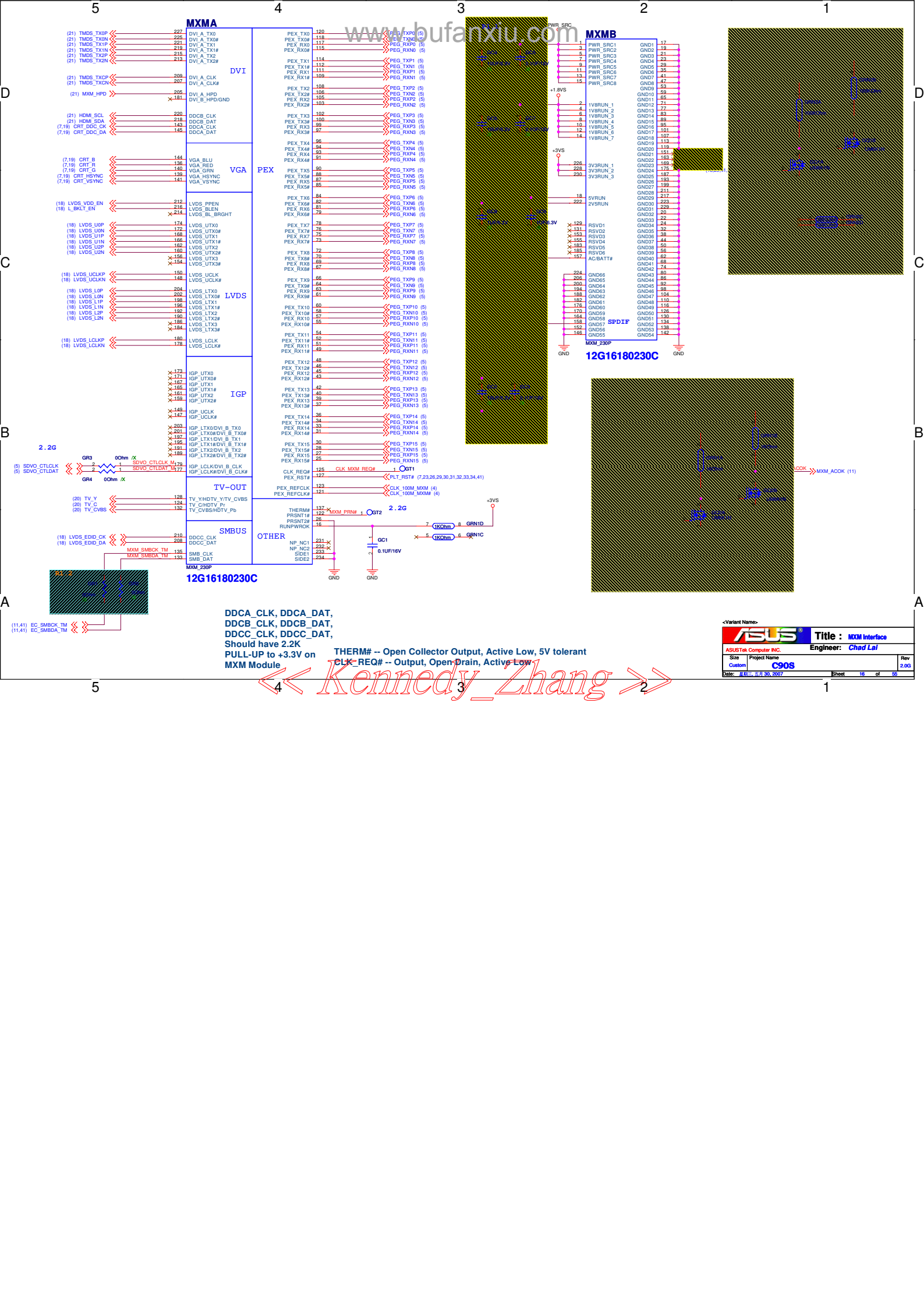
(6.14) MA_A13# >>>
(6.14) MB_A13# >>>



<Variant Name>

ASUS Title : DDR2 TERMINATION
 ASUSTek Computer INC. Engineer: Chad Lai
 Size | Project Name | Rev
 Custom | C90S | 2.0G
 Date: 8/11 - 11/30, 2007 | Sheet 15 of 55

<< Kennedy_Zhang >>



DDCA_CLK, DDCA_DAT,
DDCB_CLK, DDCB_DAT,
DDCC_CLK, DDCC_DAT,
Should have 2.2K
PULL-UP to +3.3V on
MXM Module

THERM# -- Open Collector Output, Active Low, 5V tolerant
CLK_REQ# -- Output, Open-Drain, Active Low

« Kennedy_Zhang »

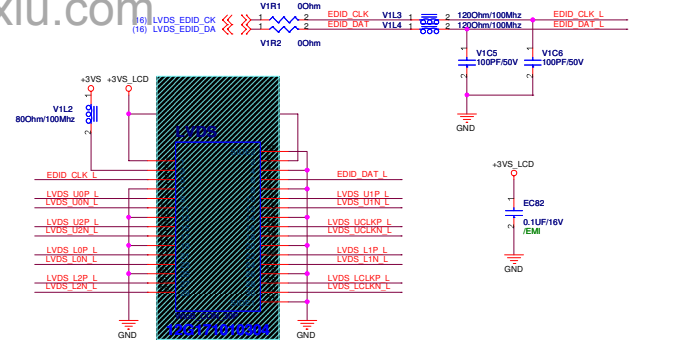
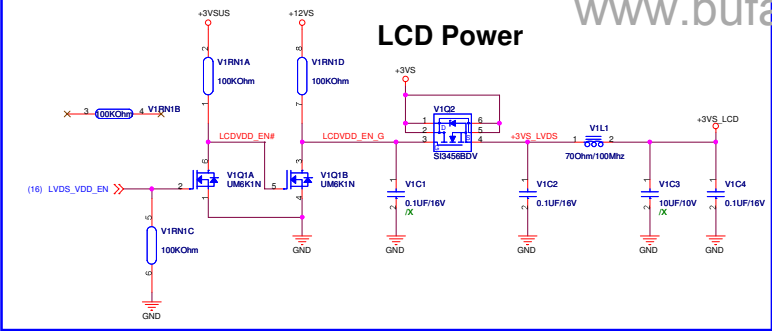
ASUS		Title : MXM Interface	
ASUSTek Computer INC.		Engineer : Chad Lal	
Size	Project Name	Rev	
Custom	C90S	2.03	
Date: 2007-11-20		Sheet	16 of 55

MXM Connector Pin Definition

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	PWR_SRC	2	1V8RUN	111	PEX_RX1	112	PEX_TX1#	221	DVI_A_TX1	222	2V5RUN
3	PWR_SRC	4	1V8RUN	113	GND	114	PEX_TX1	223	GND	224	GND
5	PWR_SRC	6	1V8RUN	115	PEX_RX0#	116	GND	225	DVI_A_TX0#	226	3V3RUN
7	PWR_SRC	8	1V8RUN	117	PEX_RX0	118	PEX_TX0#	227	DVI_A_TX0	228	3V3RUN
9	PWR_SRC	10	1V8RUN	119	GND	120	PEX_TX0	229	GND	230	3V3RUN
11	PWR_SRC	12	1V8RUN	121	PEX_REFCLK#	122	PRSNT1#				
13	PWR_SRC	14	1V8RUN	123	PEX_REFCLK	124	TV_C/HDTV_Pr				
15	PWR_SRC	16	RUNPWROK	125	CLK_REQ#	126	GND				
17	GND	18	5VRUN	127	PEX_RST#	128	TV_Y/HDTV_Y/TV_CVBS				
19	GND	20	GND	129	RSVD	130	GND				
21	GND	22	GND	131	RSVD	132	TV_CVBS/HDTV_Pb				
23	GND	24	GND	133	SMB_DAT	134	GND				
25	PEX_RX15#	26	PRSNT2#	135	SMB_CLK	136	VGA_RED				
27	PEX_RX15	28	PEX_TX15#	137	THERM#	138	GND				
29	GND	30	PEX_TX15	139	VGA_HSYNC	140	VGA_GRN				
31	PEX_RX14#	32	GND	141	VGA_VSYNC	142	GND				
33	PEX_RX14	34	PEX_TX14#	143	DDCA_CLK	144	VGA_BLU				
35	GND	36	PEX_TX14	145	DDCA_DAT	146	GND				
37	PEX_RX13#	38	GND	147	IGP_RSVD	148	LVDS_UCLK#				
39	PEX_RX13	40	PEX_TX13#	149	IGP_RSVD	150	LVDS_UCLK				
41	GND	42	PEX_TX13	151	IGP_RSVD	152	GND				
43	PEX_RX12#	44	GND	153	IGP_RSVD	154	LVDS_UTX3#				
45	PEX_RX12	46	PEX_TX12#	155	IGP_RSVD	156	LVDS_UTX3				
47	GND	48	PEX_TX12	157	AC/BATT#	158	SPDIF				
49	PEX_RX11#	50	GND	159	IGP_RSVD	160	LVDS_UTX2#/DVI_C_TX5#				
51	PEX_RX11	52	PEX_TX11#	161	IGP_RSVD	162	LVDS_UTX2/DVI_C_TX5				
53	GND	54	PEX_TX11	163	IGP_RSVD	164	GND				
55	PEX_RX10#	56	GND	165	IGP_RSVD	166	LVDS_UTX1#/DVI_C_TX4#				
57	PEX_RX10	58	PEX_TX10#	167	IGP_RSVD	168	LVDS_UTX1/DVI_C_TX4				
59	GND	60	PEX_TX10	169	IGP_RSVD	170	GND				
61	PEX_RX9#	62	GND	171	IGP_RSVD	172	LVDS_UTX0#/DVI_C_TX3#				
63	PEX_RX9	64	PEX_TX9#	173	IGP_RSVD	174	LVDS_UTX0/DVI_C_TX3				
65	GND	66	PEX_TX9	175	GND	176	GND				
67	PEX_RX8#	68	GND	177	IGP/DVI_B_CLK#	178	LVDS_LCLK#/DVI_C_TXC#				
69	PEX_RX8	70	PEX_TX8#	179	IGP/DVI_B_CLK	180	LVDS_LCLK/DVI_C_TXC				
71	GND	72	PEX_TX8	181	DVI_B_HPD/GND	182	GND				
73	PEX_RX7#	74	GND	183	RSVD	184	LVDS_LTX3#				
75	PEX_RX7	76	PEX_TX7#	185	RSVD	186	LVDS_LTX3				
77	GND	78	PEX_TX7	187	GND	188	GND				
79	PEX_RX6#	80	GND	189	IGP/DVI_B_TX2#	190	LVDS_LTX2#/DVI_C_TX2#				
81	PEX_RX6	82	PEX_TX6#	191	IGP/DVI_B_TX2	192	LVDS_LTX2/DVI_C_TX2				
83	GND	84	PEX_TX6	193	GND	194	GND				
85	PEX_RX5#	86	GND	195	IGP/DVI_B_TX1#	196	LVDS_LTX1#/DVI_C_TX1#				
87	PEX_RX5	88	PEX_TX5#	197	IGP/DVI_B_TX1	198	LVDS_LTX1/DVI_C_TX1				
89	GND	90	PEX_TX5	199	GND	200	GND				
91	PEX_RX4#	92	GND	201	IGP/DVI_B_TX0#	202	LVDS_LTX0#/DVI_C_TX0#				
93	PEX_RX4	94	PEX_TX4#	203	IGP/DVI_B_TX0	204	LVDS_LTX0/DVI_C_TX0				
95	GND	96	PEX_TX4	205	DVI_A_HPD	206	GND				
97	PEX_RX3#	98	GND	207	DVI_A_CLK#	208	DDCC_DAT				
99	PEX_RX3	100	PEX_TX3#	209	DVI_A_CLK	210	DDCC_CLK				
101	GND	102	PEX_TX3	211	GND	212	LVDS_PPEN				
103	PEX_RX2#	104	GND	213	DVI_A_TX2#	214	LVDS_BL_BRGHT				
105	PEX_RX2	106	PEX_TX2#	215	DVI_A_TX2	216	LVDS_BLEN				
107	GND	108	PEX_TX2	217	GND	218	DDCB_DAT				
109	PEX_RX1#	110	GND	219	DVI_A_TX1#	220	DDCB_CLK				

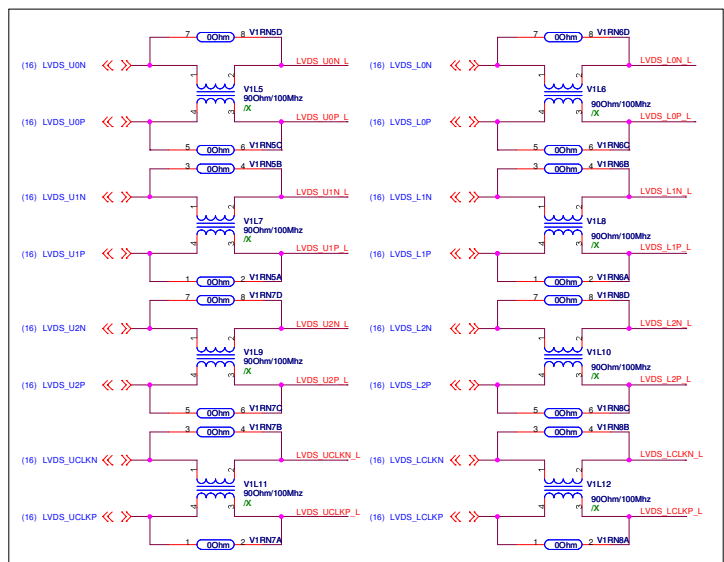
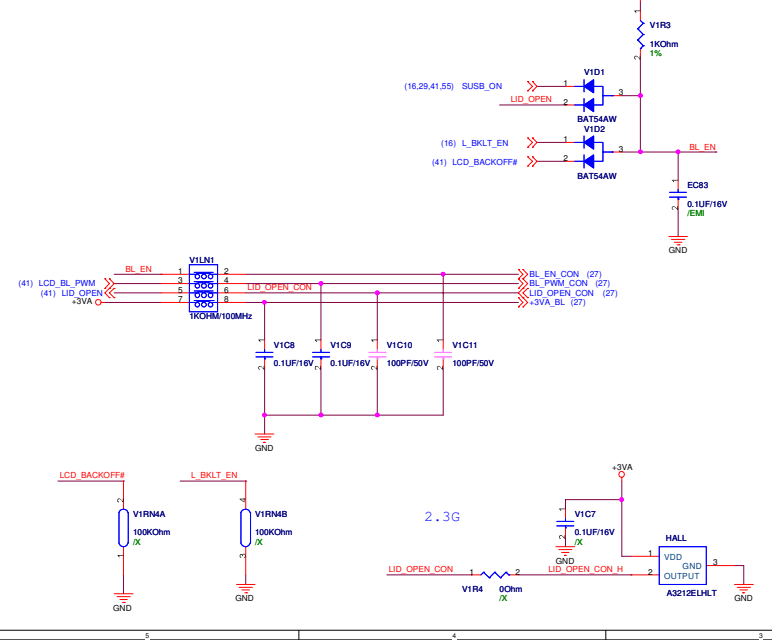
Kennedy_Zhang

ASUS		Title : MXM PWR & GND	
<small>ASUSTek Computer INC.</small>		Engineer : Chad Lai	
<small>Size</small>	<small>Project Name</small>	<small>Rev</small>	
Custom	C90S	2.03	
<small>Date : 8/13, 2007</small>		<small>Sheet 17 of 55</small>	



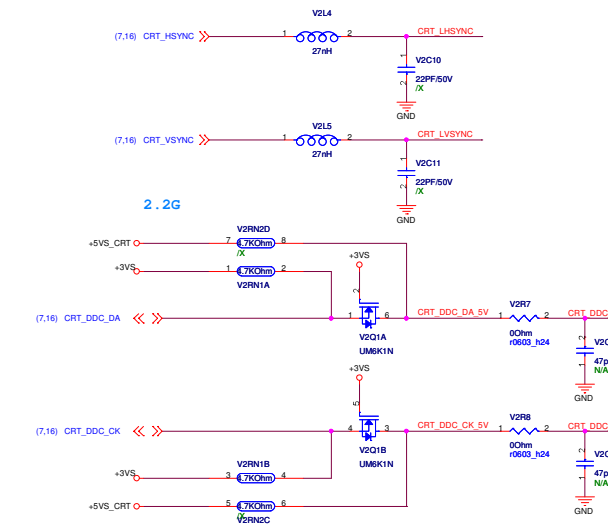
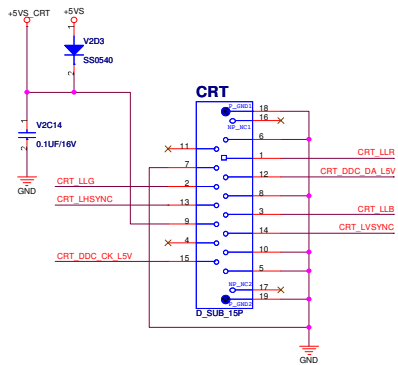
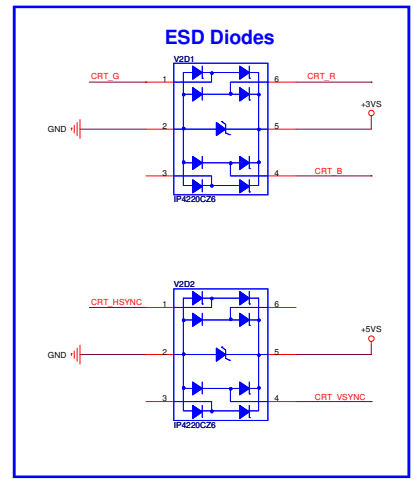
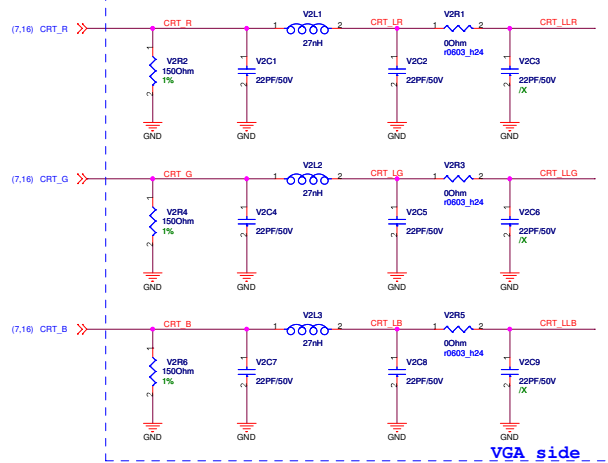
BIOS
BACK_OFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050
 PANEL ID1 = 0 : WXGA 1280x800
 PANEL ID0 RESERVE FOR VENDOR



ASUS		Title : LVDS & INVERTER
ASUSTek Computer INC.		Engineer: Chad Lai
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 08-15-07	Sheet: 18	of 55

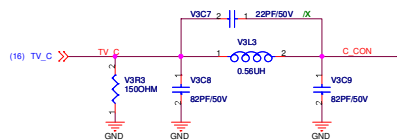
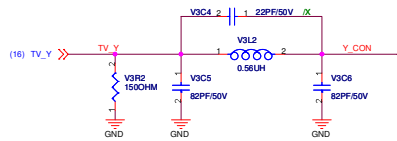
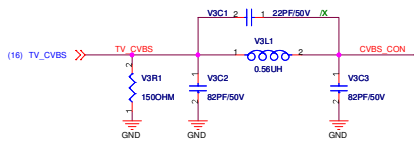
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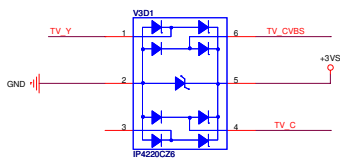
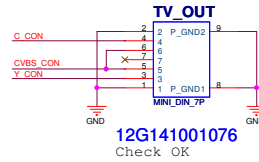
<Variant Name>

		Title : CRT	
ASUSTek Computer INC.		Engineer: Chad Lal	
Size	Project Name		Rev
A3	C90S		2.0G
Date: 8/10/2007		Sheet	19 of 59

<< Kennedy_Zhang >>



TV OUT Connector

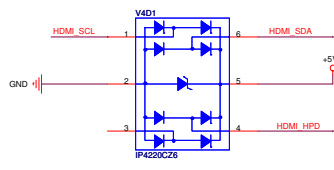
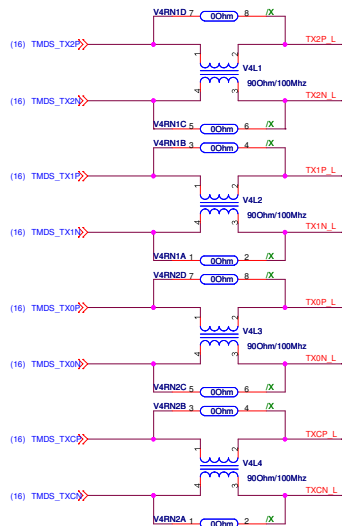


ESD Diode, Place close to Connector

ASUS		Title : TV-OUT Connector	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	C90S	2.00	
Date: 8/11/2007		Sheet	20 of 55

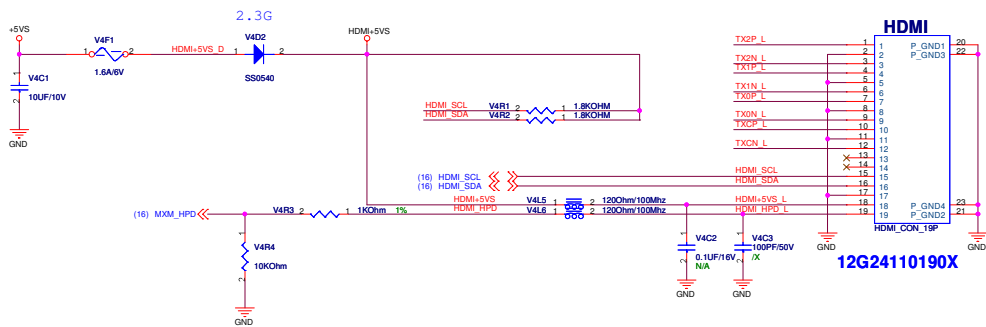
« Kennedy_Zhang »

Choke : TDK ACM2012 preferred



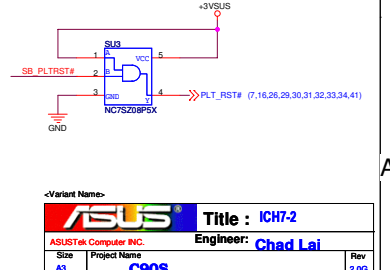
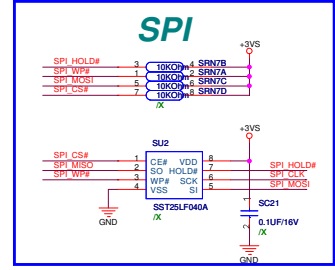
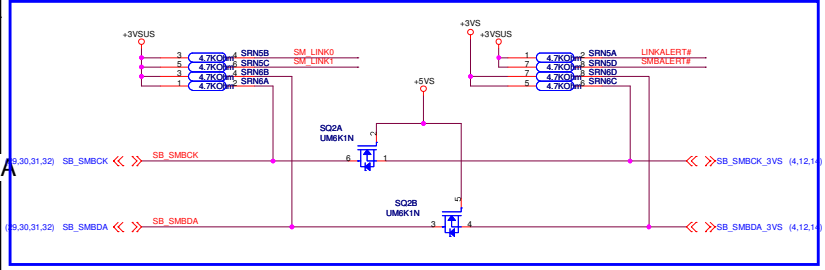
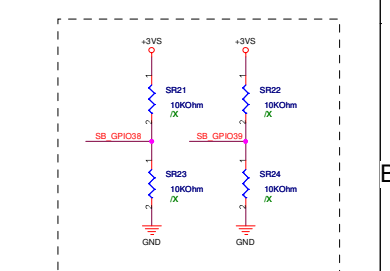
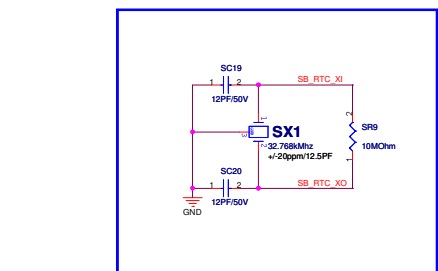
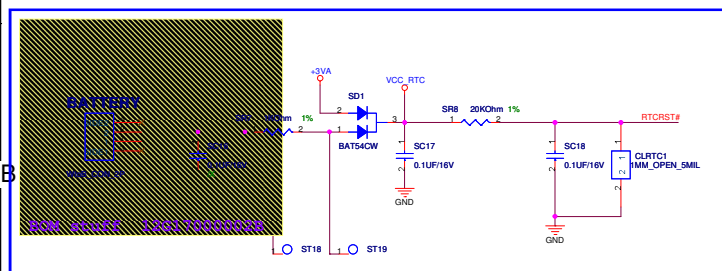
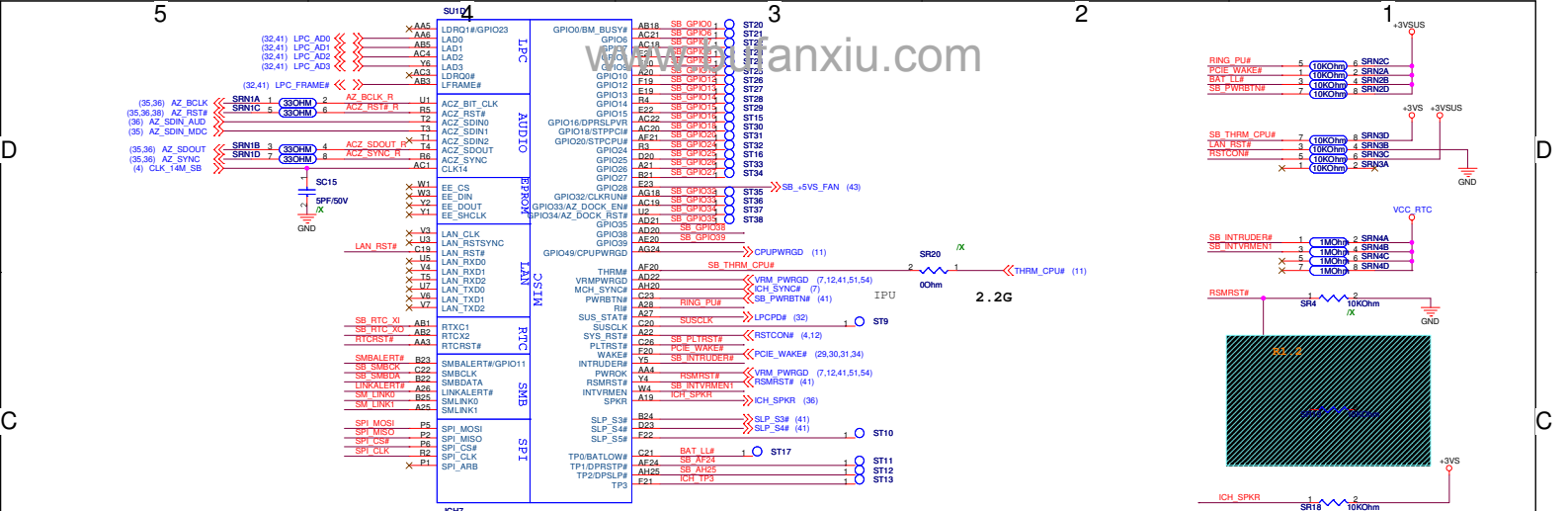
ESD Diode, Place close to Connector

HDMI Connector



ASUS		Title : HDMI Connector	
ASUSTek Computer INC.		Engineer: Chad Lal	
Size	Project Name	Rev	
Custom	C90S	2.03	
Date: 8/23, 2007	Sheet	21	of 55

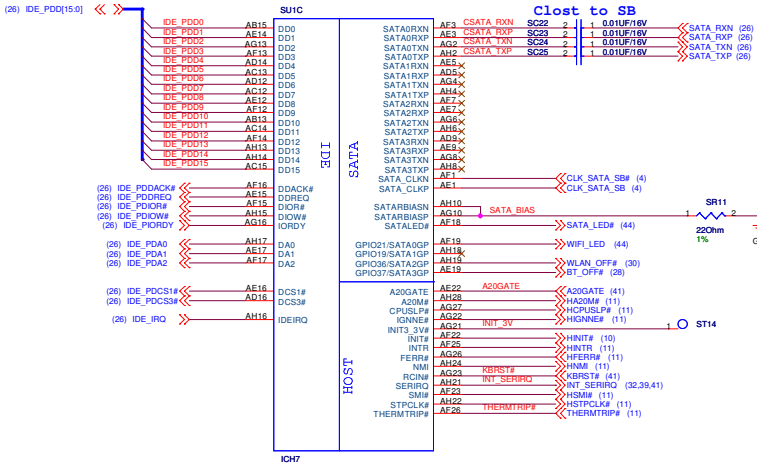
« Kennedy_Zhang »



ASUS Title: ICH7-2
 ASUSTek Computer INC. Engineer: Chad Lai
 Size: A3 Project Name: C90S Rev: 2.0G
 Date: 11/20/2007 Sheet: 29 of 35

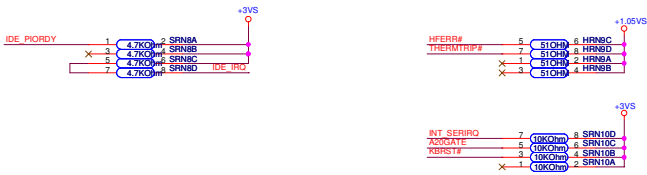
<< Kennedy_Zhang >>

(HDA_SDOUT, HDA_SYNC)
(11) = LANE1-4 as a PCIeX4 port
(00) = LANE1-4 as 4 PCIeX1 ports (* default internal PD)
others = reserved
(GNT3#)
1 = Normal (* internal PU)
0 = Top-block swap for FWH



(SB_GPIO20)
1 = reserved
0 = Intel recommend (* internal PD)
(GNT1#)
1 = Desktop/Mobile (* internal PU)
0 = Server

(ICH_TP3)
1 = PCIe Strap (* default internal PU)
0 = XOR chan test mode



(INTVRMEN, LAN100_SLP)
1 = Enabled internal VRMs for VccSus1_05, 1_5 and VccCLL1_5, 1_05 and VccLAN1_05 (*)
0 = Disabled internal VRMs

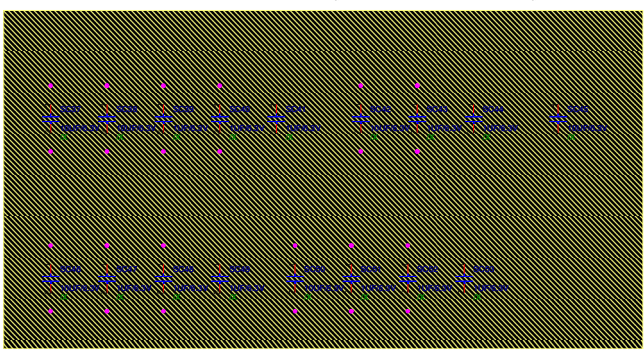
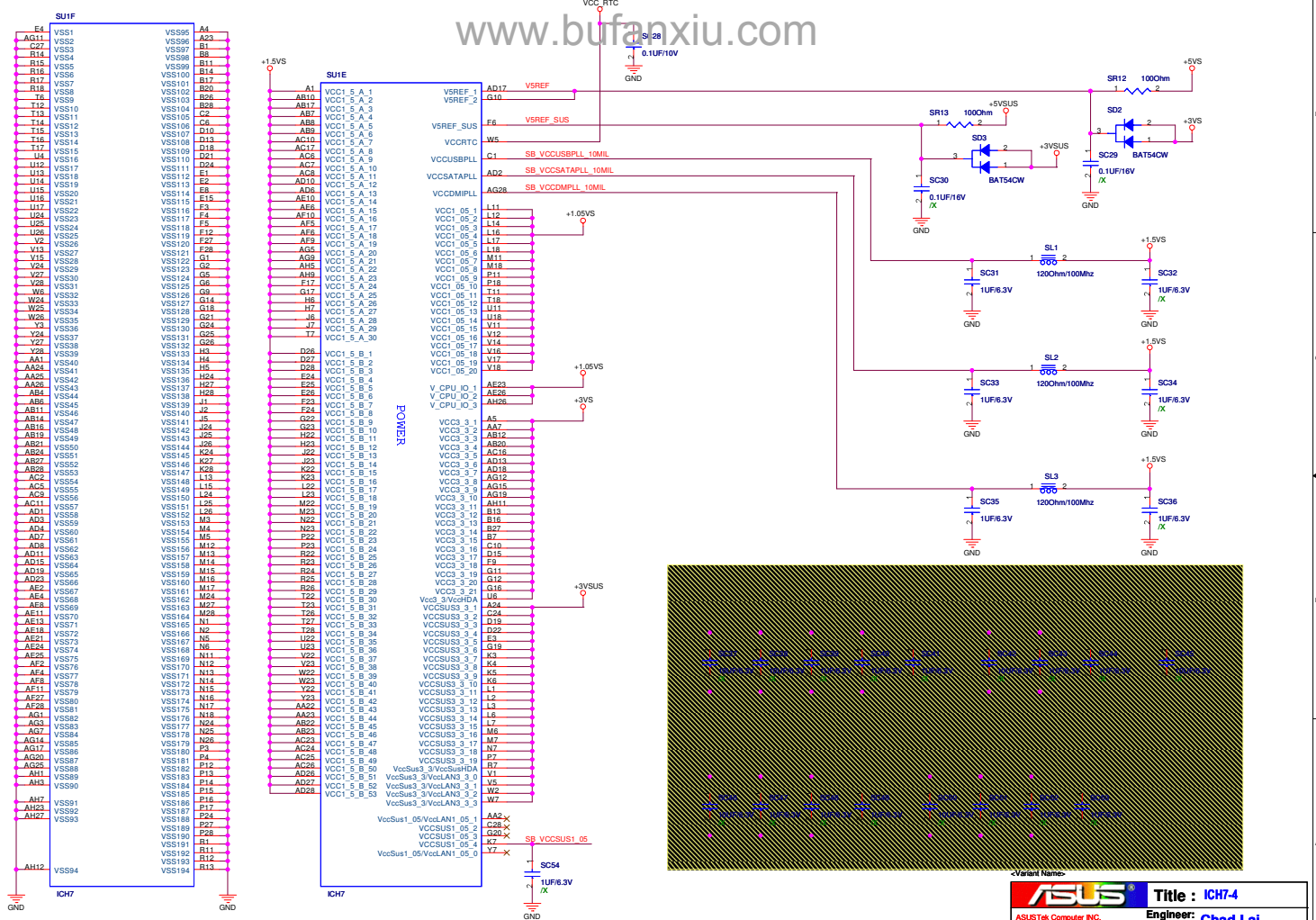
(ICH_SATALED#)
1 = LANE1-4 normal (* internal PU)
0 = LANE1-4 reverse

(SPKR)
1 = Disabled TCO Reboot
0 = Enabled TCO Reboot
(* internal PD)
(TP_GPIO33) : Not used for ICHRM
1 = Enabled Descriptor Security (* internal PU)
0 = Disabled Descriptor Security

<Variant Name>

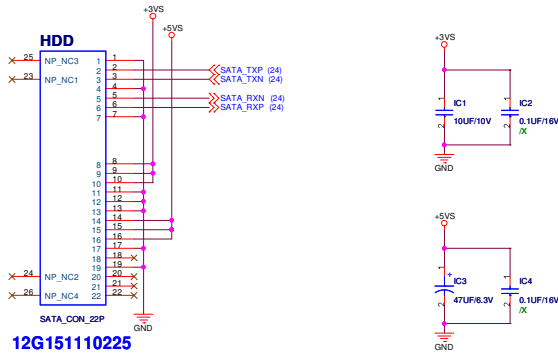
ASUS		Title: ICH7-3	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: Z.0G	
Date: 08.02.2007		Sheet: 31	of 35

<< Kennedy_Zhang >>

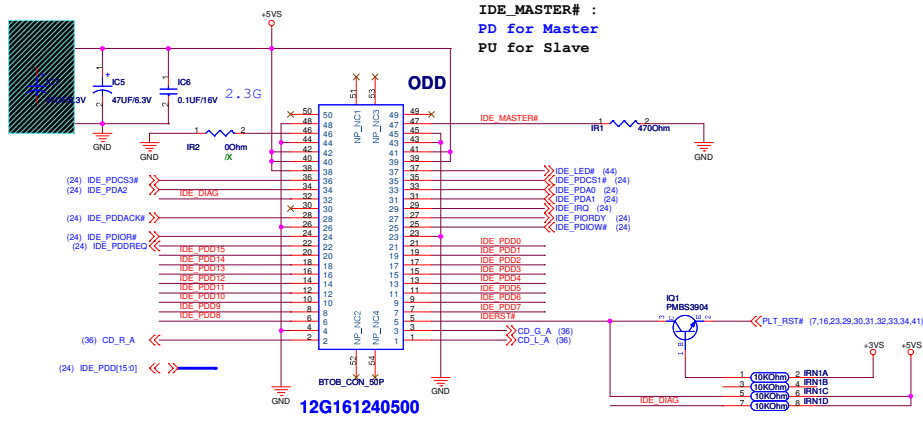


ASUS Title: ICH7-4
 ASUSTek Computer INC. Engineer: Chad Lai
 Size: A3 Project Name: C90S Rev: 2.00
 Date: 08/30/2007 Sheet: 26 of 55

<< Kennedy_Zhang >>



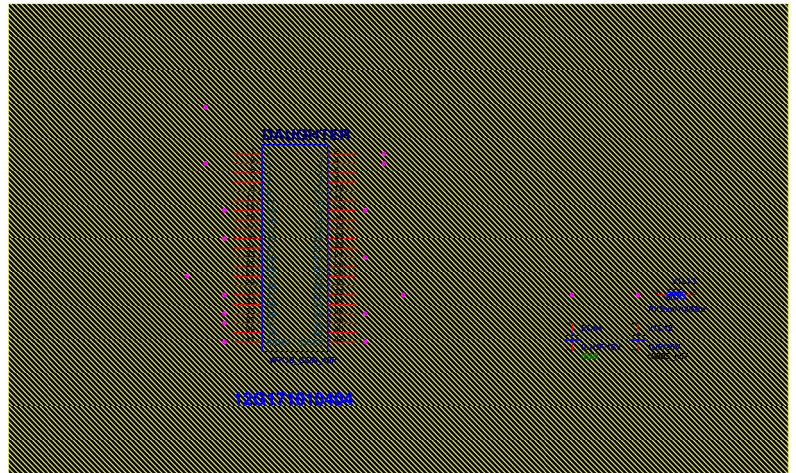
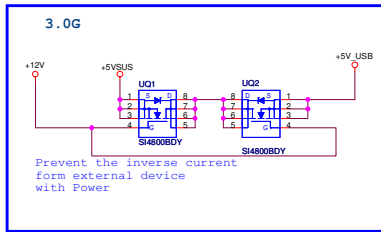
ODD



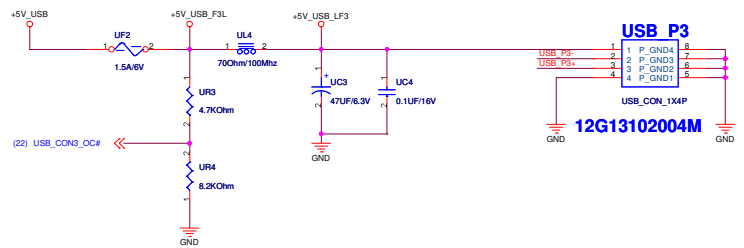
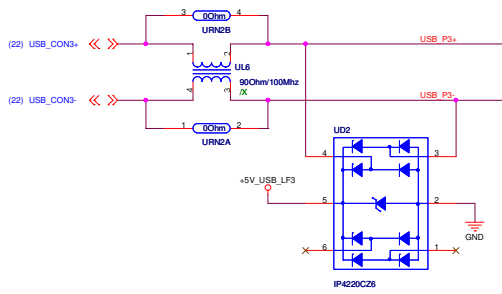
<Variant Name>

ASUS		Title : SATA-HDD & ODD
ASUSTek Computer INC.		Engineer: Chad Lai
Size	Project Name	Rev
Custom	C90S	2.00
Date: 8/8 - 11/30/2007	Sheet	26 of 55

« Kennedy_Zhang »



All close to USB connectors

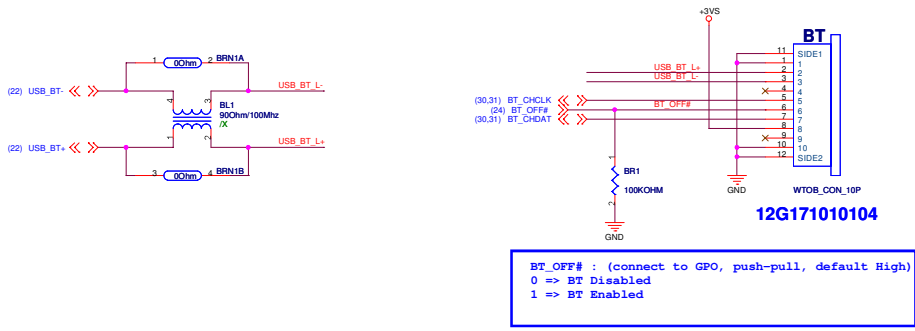


<Variant Name>

ASUS		Title : USB CONN
ASUSTek Computer INC.		Engineer: Chad Lai
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 11/13/2007	Sheet: 27	of 55

<< Kennedy_Zhang >>

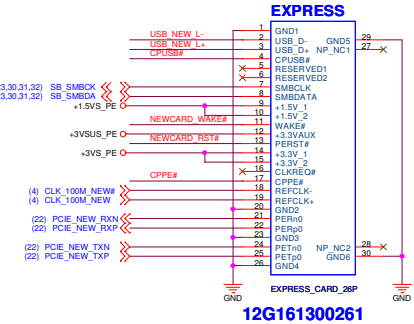
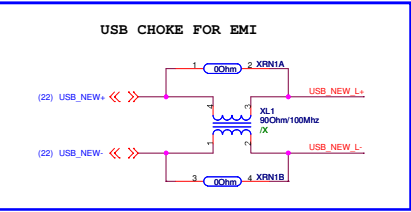
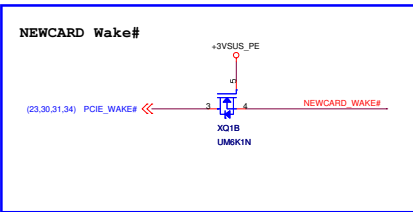
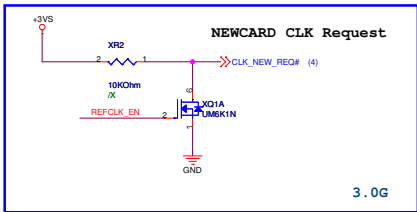
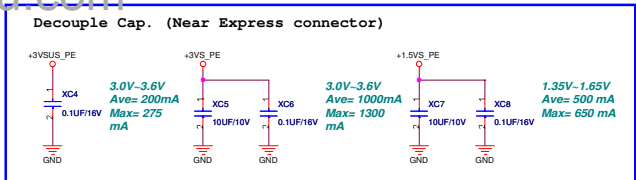
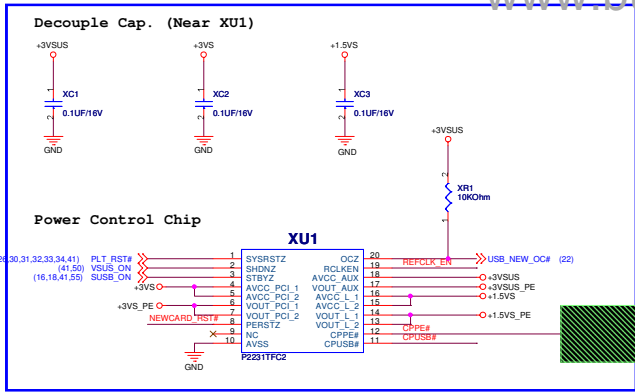
Bluetooth Connector



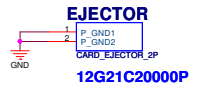
G-Sensor

3.0G

« Kennedy_Zhang »

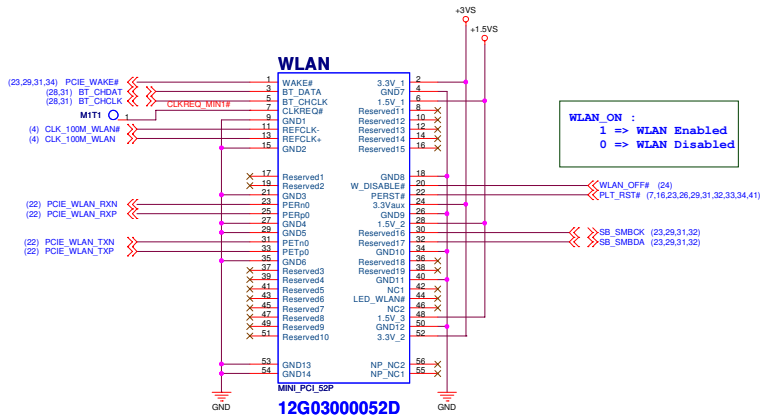
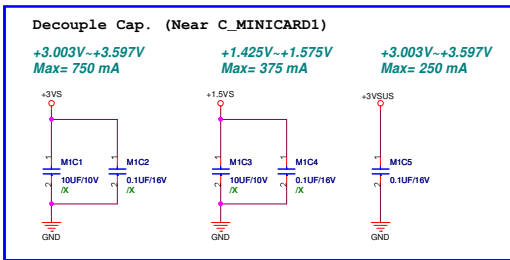


!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V



ASUS		Title : NEWCARD	
ASUSTek Computer INC.		Engineer: Chad Lai	
Site	Project Name	Rev	
Custom	C90S	2.00	
Date: 08-11-2007	Sheet	28	of 55

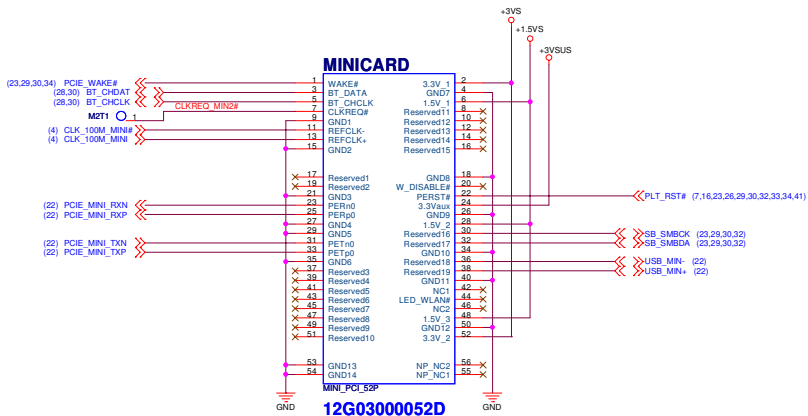
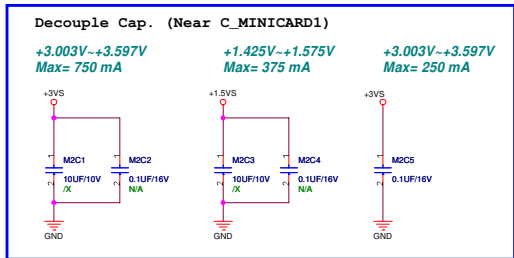
« Kennedy_Zhang »



<Variant Name>

ASUS		Title : MINI CARD
ASUSTek Computer INC.		Engineer: Chad Lai
Size	Project Name	Rev
Custom	C90S	2.00
Date: 2007年5月30日	Sheet	30 of 55

« Kennedy_Zhang »

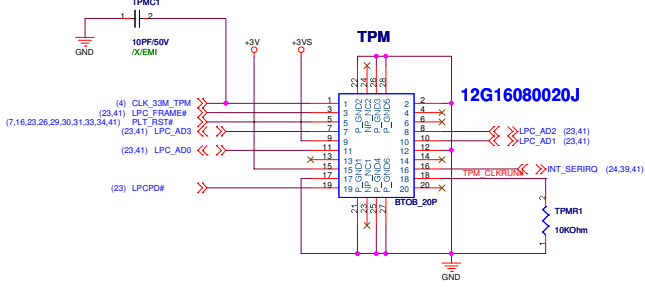


<Variant Name>

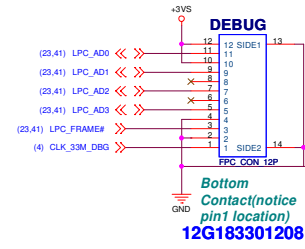
ASUS		Title : MINI CARD
ASUSTek Computer INC.		Engineer: Chad Lai
Size	Project Name	Rev
Custom	C90S	2.00
Date: 2007年5月30日	Sheet	31 of 55

« Kennedy_Zhang »

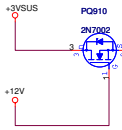
TPM Connector



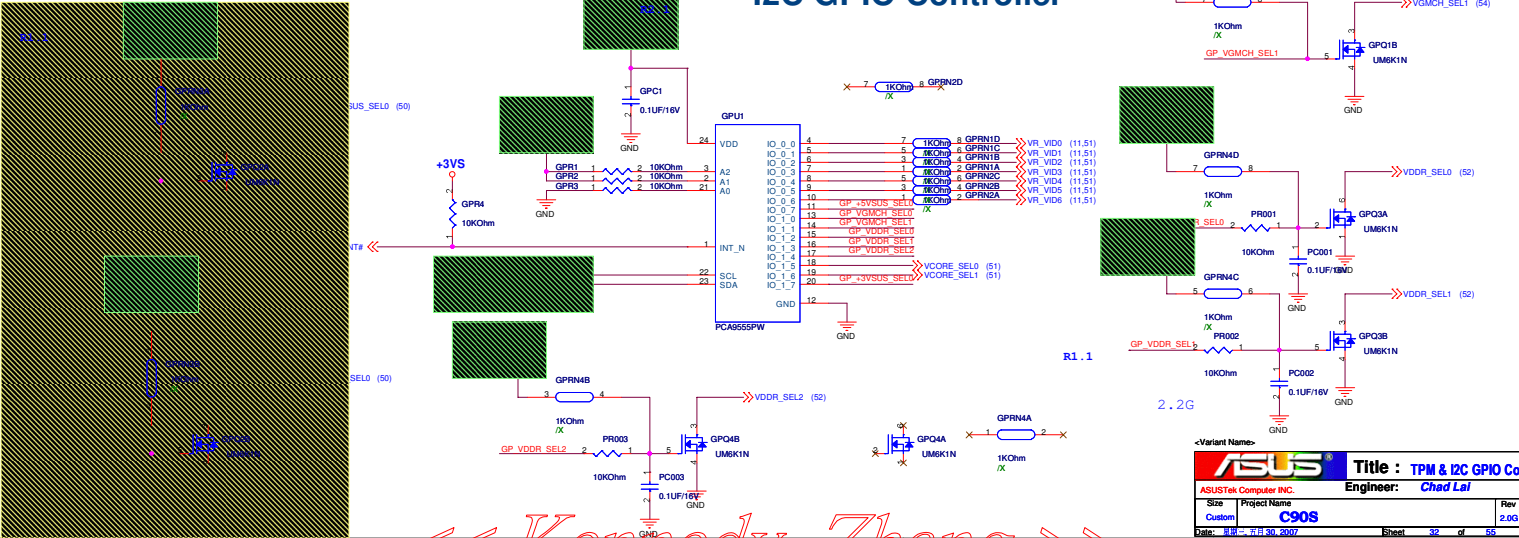
Debug Connector



FOR +3V POWER TPM_LED PWR_LED

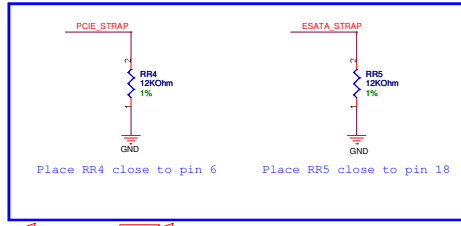
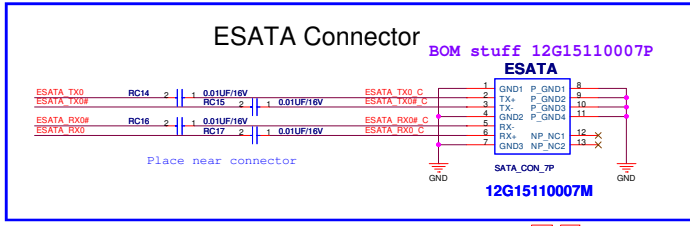
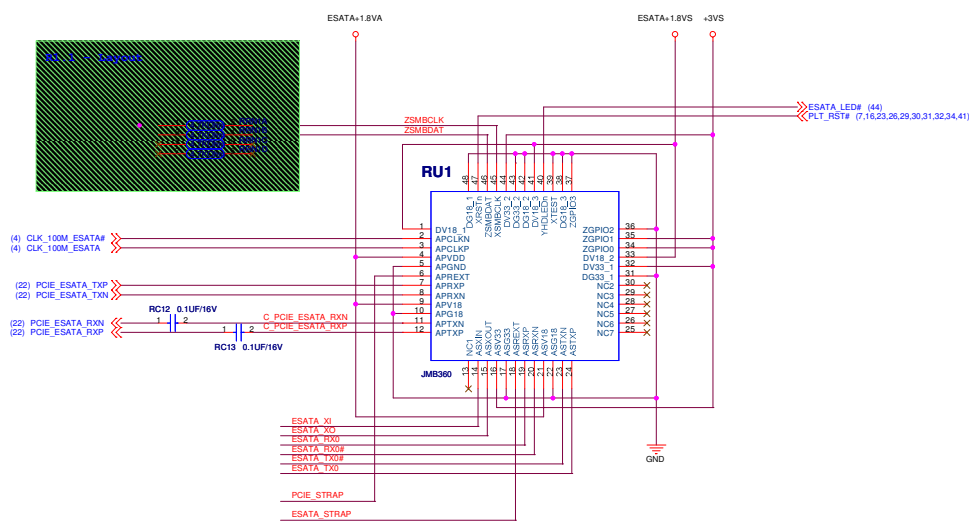
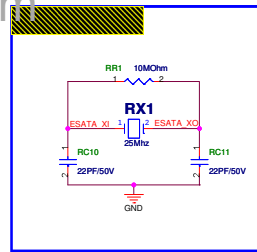
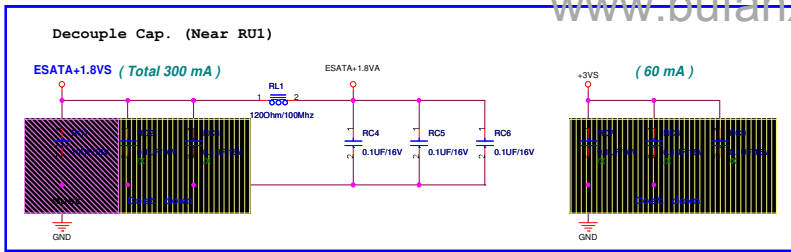


I2C GPIO Controller



ASUS		Title : TPM & I2C GPIO Control	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	C90S	2.0G	
Date: 8/8	T/H 30, 2007	Sheet	32 of 55

« Kennedy_Zhang »



ASUS Logo

ASUSTek Computer INC. Title: ESATA-JMB360
 Engineer: Chad Lal

Size	Project Name	Rev
Custom	C90S	2.0G
Date: R1E1: R# 30, 2007	Sheet 38	of 56

« Kennedy_Zhang »

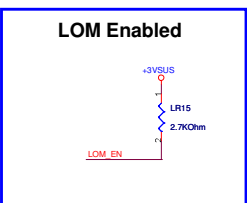
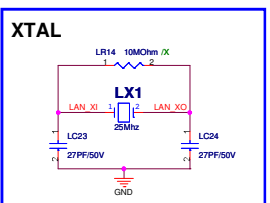
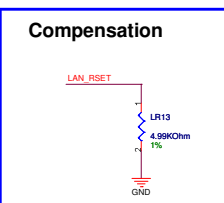
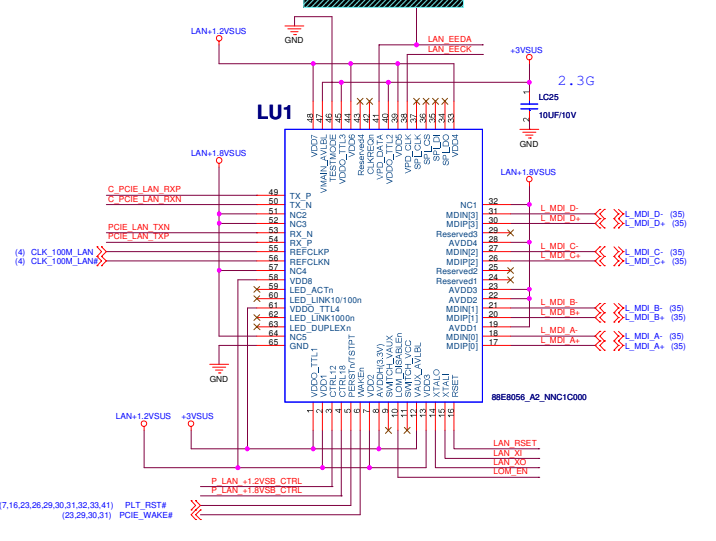
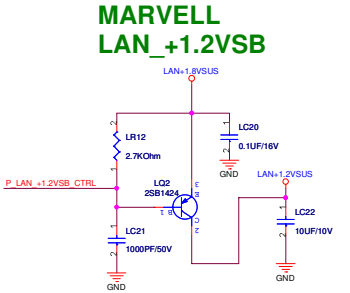
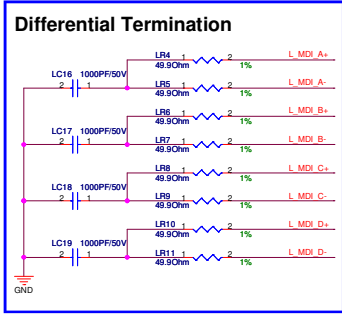
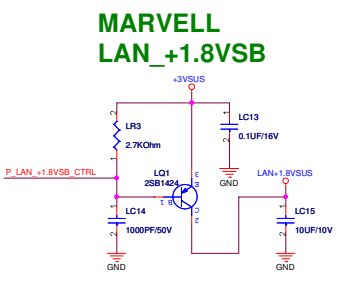
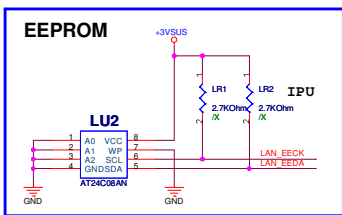
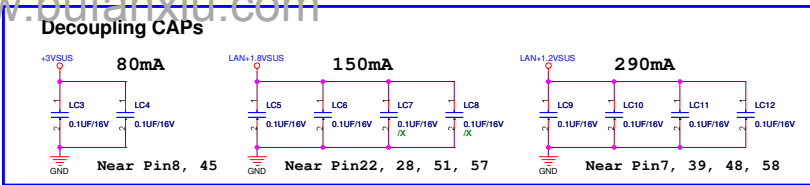
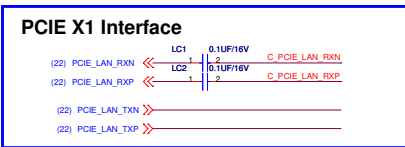
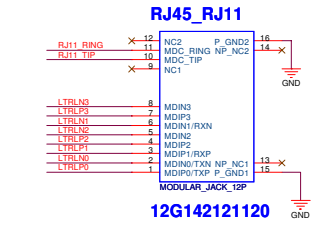
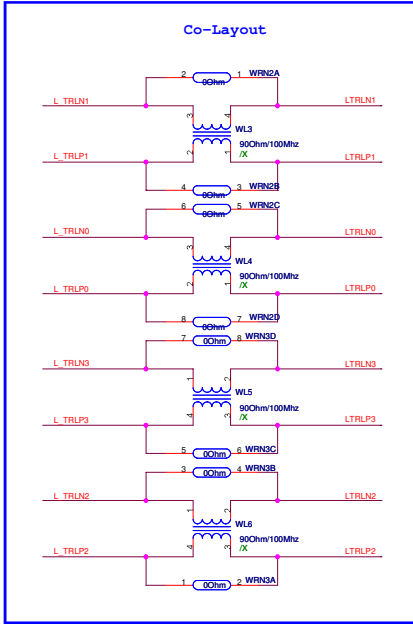
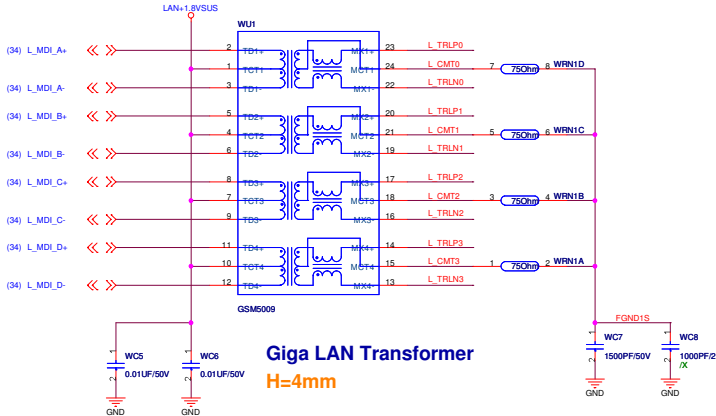
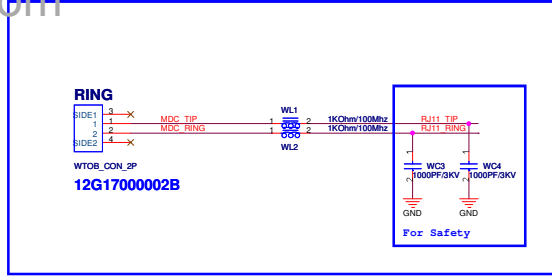
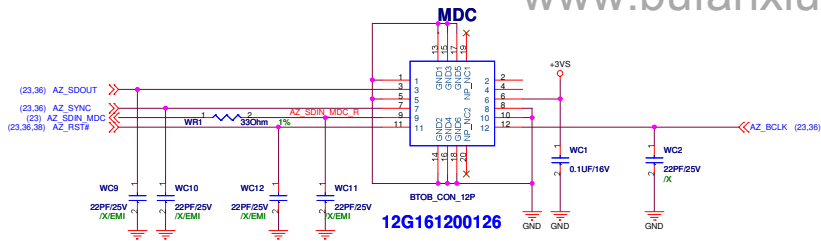


Table 30: Media Dependent Interface Pin Mapping

Pin	MDIX	100BASE-T	100BASE-TX	100BASE-T	100BASE-TX	100BASE-T	100BASE-TX
MDI[0]	TX_0	TX_0	TX_0	TX_0	TX_0	TX_0	TX_0
MDI[1]	TX_1	TX_1	TX_1	TX_1	TX_1	TX_1	TX_1
MDI[2]	TX_2	TX_2	TX_2	TX_2	TX_2	TX_2	TX_2
MDI[3]	TX_3	TX_3	TX_3	TX_3	TX_3	TX_3	TX_3
MDI[4]	TX_4	TX_4	TX_4	TX_4	TX_4	TX_4	TX_4
MDI[5]	TX_5	TX_5	TX_5	TX_5	TX_5	TX_5	TX_5

ASUS Title: Marvell 88E8056
 ASUSTek Computer INC. Engineer: Chad Lai
 Size: A3 Project Name: C90S Rev: 2.0G
 Date: 08-30-2007 Sheet: 34 of 55

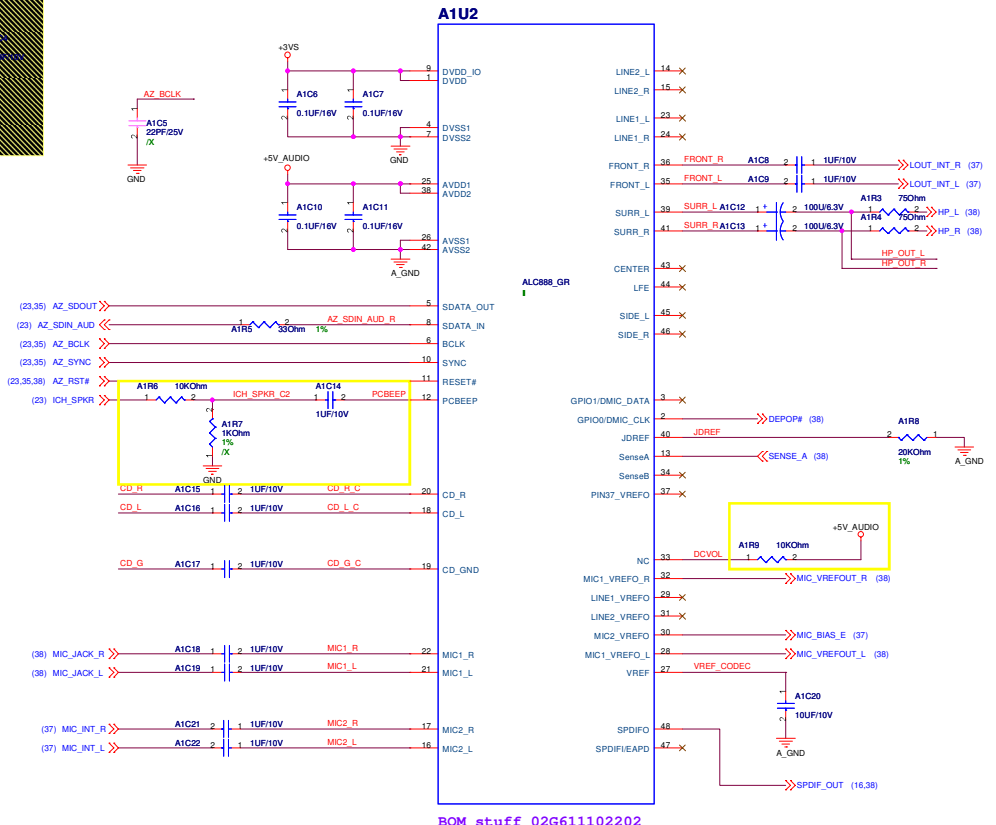
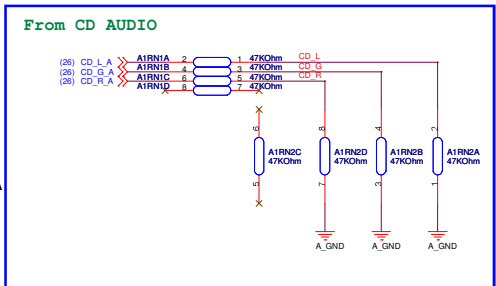
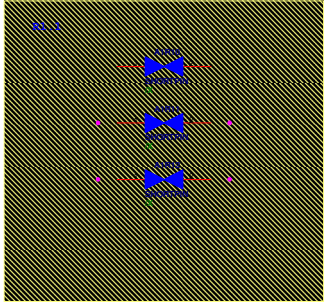
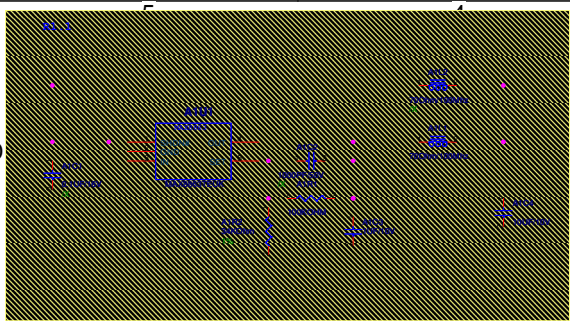
<< Kennedy_Zhang >>



<Variant Name>

ASUS		Title : MDC / RJ45
ASUSTek Computer Inc.		Engineer: Chad Lai
Size: A3	Project Name: C90S	Rev: 2.0G
Date: #18- 7/130_2007	Sheet: 35	of 35

<< Kennedy_Zhang >>

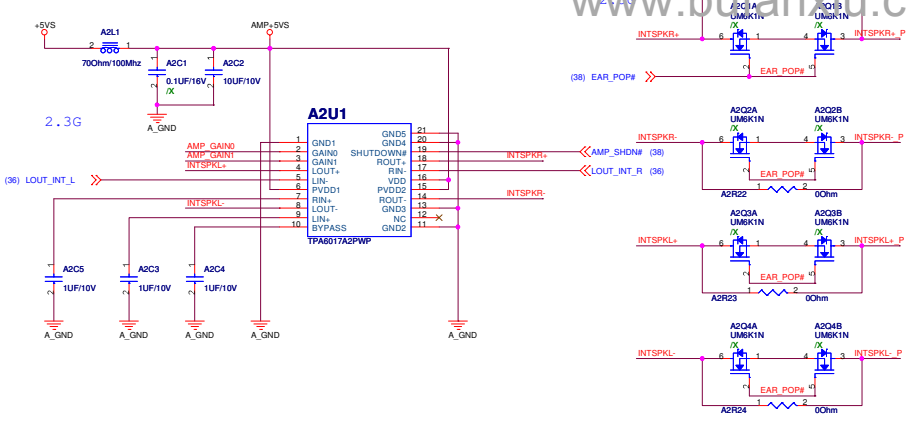


BOM stuff 02G611102202

ASUS		Title : <Title>	
ASUSTek Computer INC.		Engineer: Chad Lal	
Size A3	Project Name C90S	Rev 2.00	
Date: 08/11/2007	Sheet 36	of 55	

<< Kennedy_Zhang >>

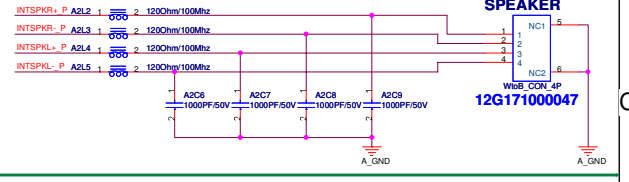
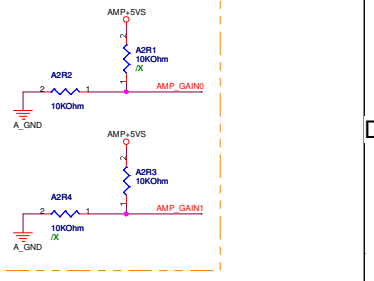
Audio Amp.



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GAIN Setting

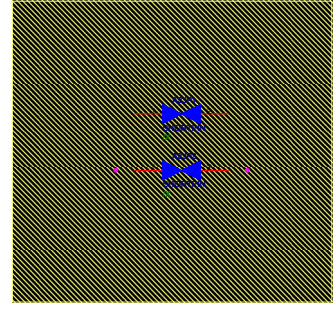
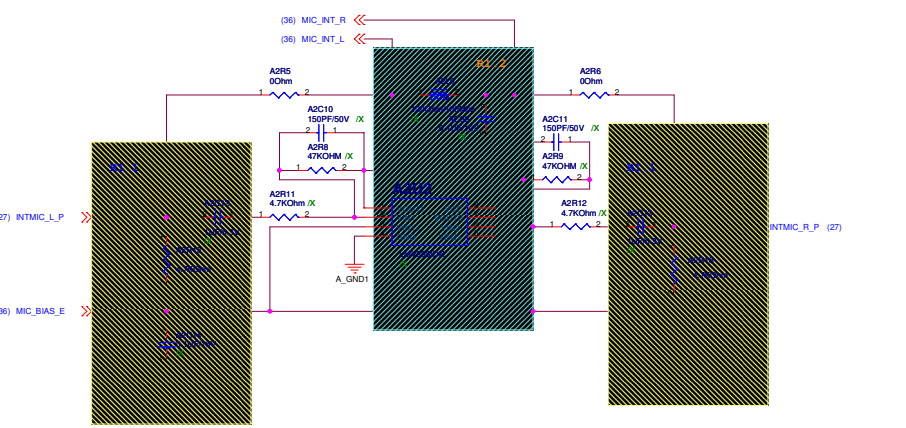
GAIN0	GAIN1	Av (inV)	Input Impedance
0	0	6dB	90k ohm
0	1	10dB	70k ohm
1	0	15.6dB	45k ohm
1	1	21.6dB	25k ohm



Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz

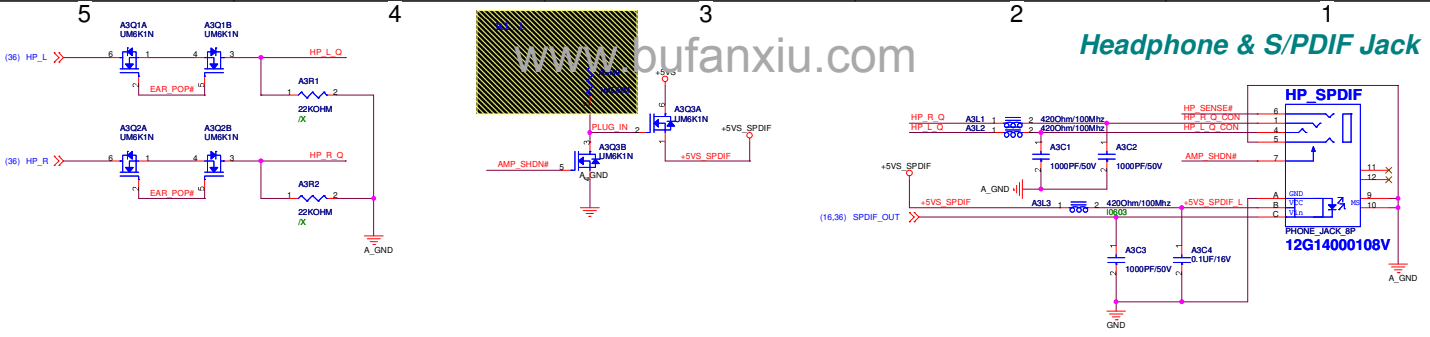
Place Near INTMIC Connector



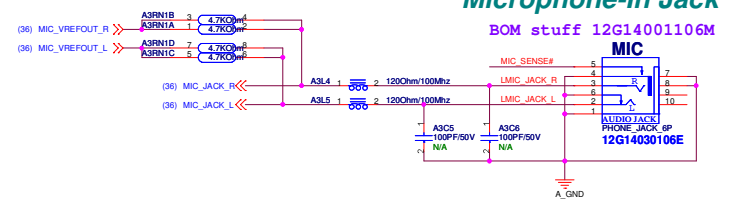
ASUS Title: SCH page name
 Engineer: Chad Lal
 Project Name: C90S
 Date: 08/30/2007 Sheet 37 of 55

<< Kennedy_Zhang >>

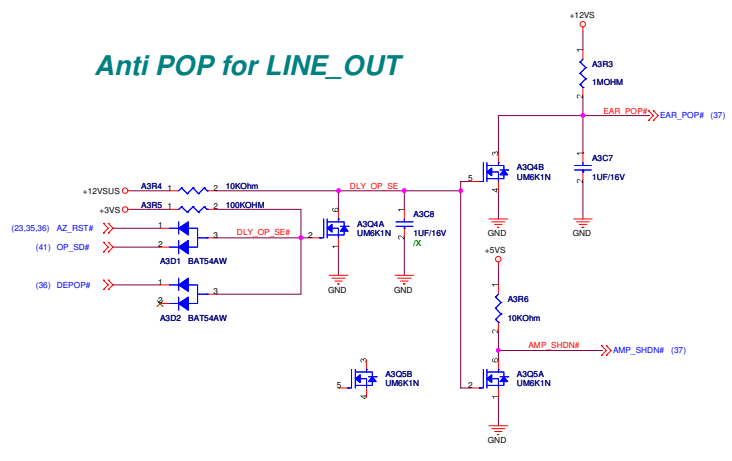
Headphone & S/PDIF Jack



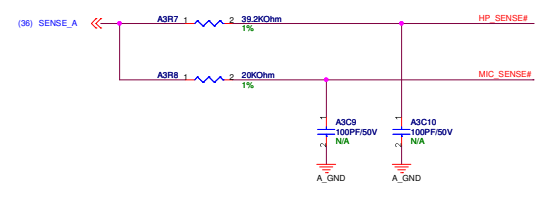
Microphone-In Jack



Anti POP for LINE_OUT

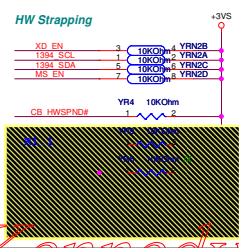
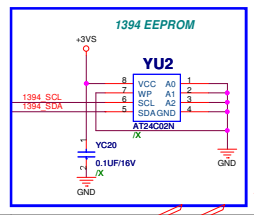
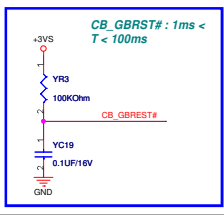
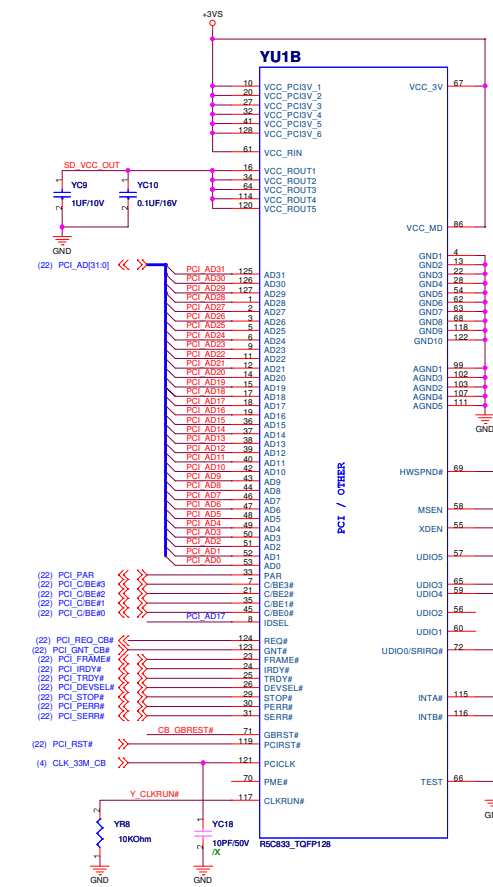
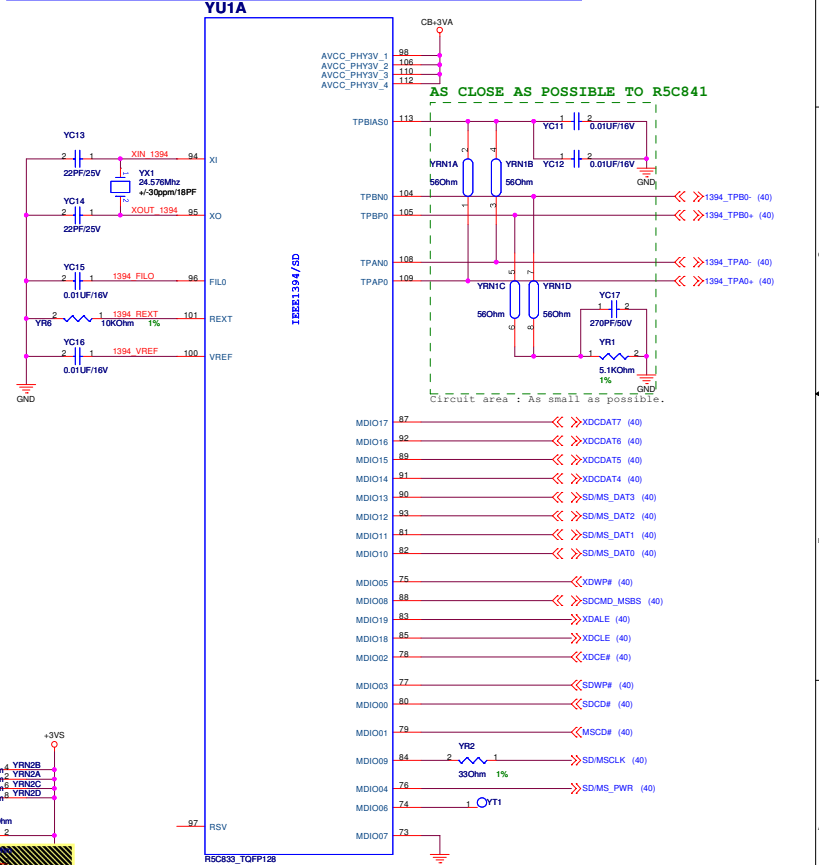
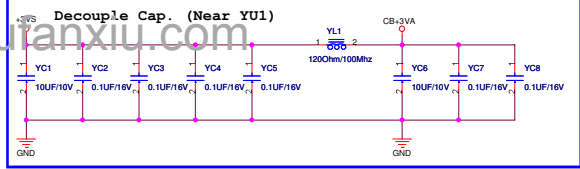


Jack Plug-in Detection



ASUS		Title: SCH page name	
ASUSTek Computer INC.		Engineer: Chad Lal	
Size: A3	Project Name: C90S	Date: 08/30/2007	Rev: 2.00
Date: 08/30/2007		Sheet: 38	of: 55

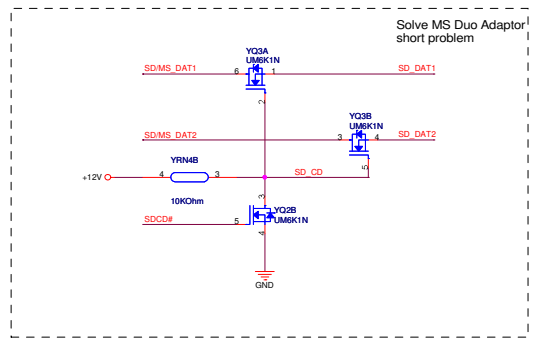
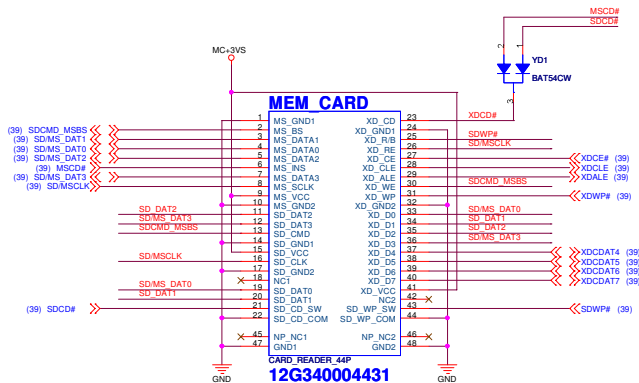
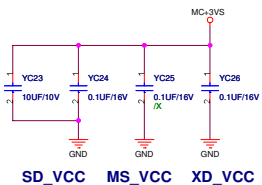
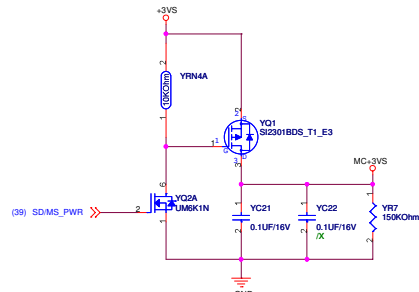
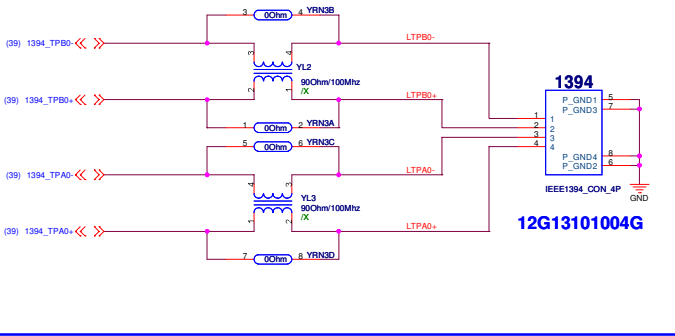
<< Kennedy_Zhang >>



ASUS		Title : CARD1394-R5C832(1)	
ASUSTek Computer INC.		Engineer: Chad Lal	
Size	Project Name	Rev	
Custom	C90S	2.0G	
Date: 8/18	11/30/2007	Sheet	39 of 55

« Kennedy_Zhang »

1394



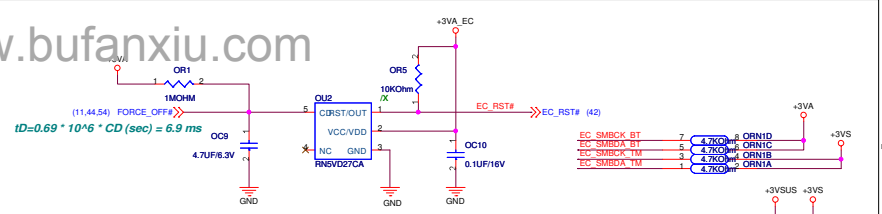
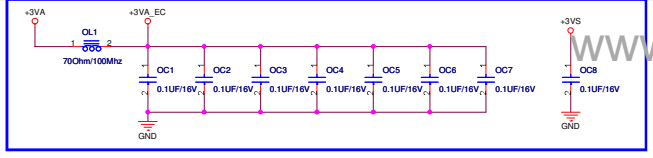
ASUS Title 1394 CON

ASUSTek Computer INC. Engineer: Chad Lal

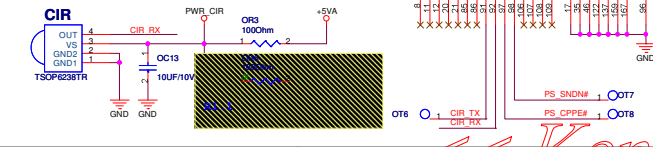
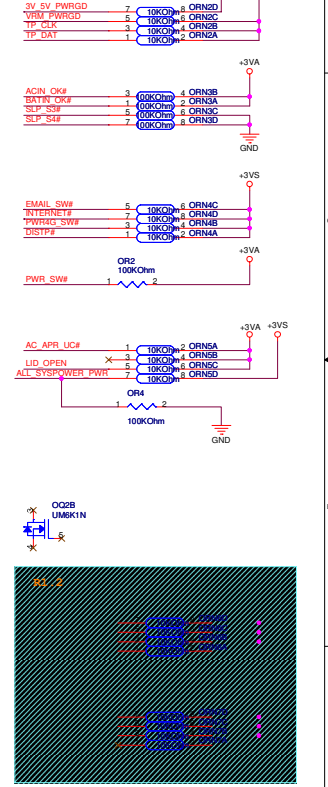
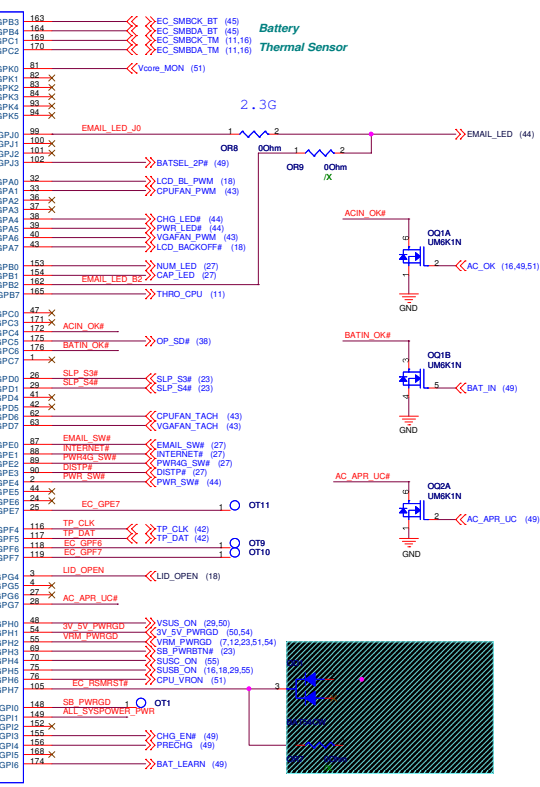
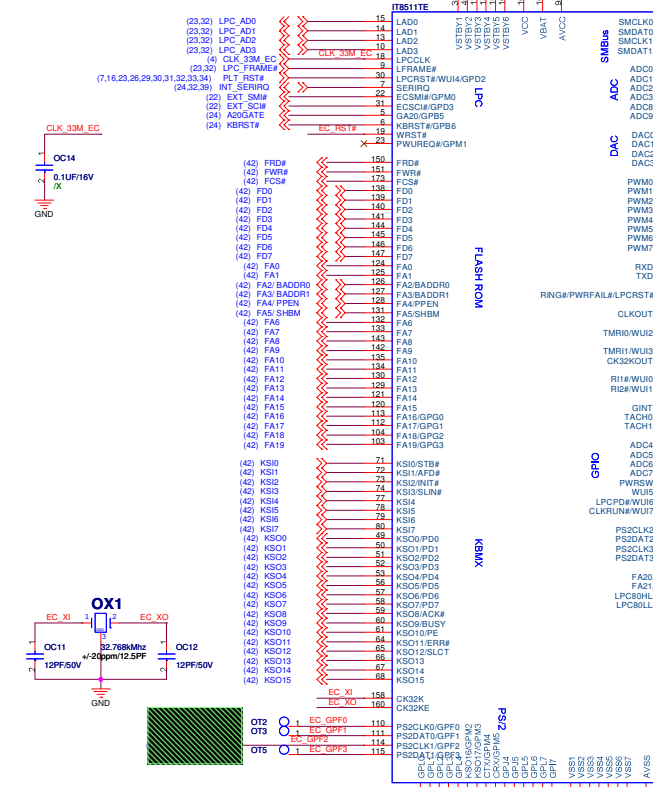
Size A3 Project Name C90S Rev 2.0G

Date: 8/10/2007 Sheet 40 of 52

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Check LPC PU in SB



BOM stuff 06G042012011

ASUS logo and project information: Title: EC IT8511E, Engineer: Chad Lai, Project Name: C90S, Date: 08-18-2007, Sheet: 41 of 55.

<< Kennedy_Zhang >>

[FA3/ BADDR1 : FA2/ BADDR0]

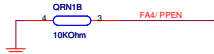
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 01: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 10: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

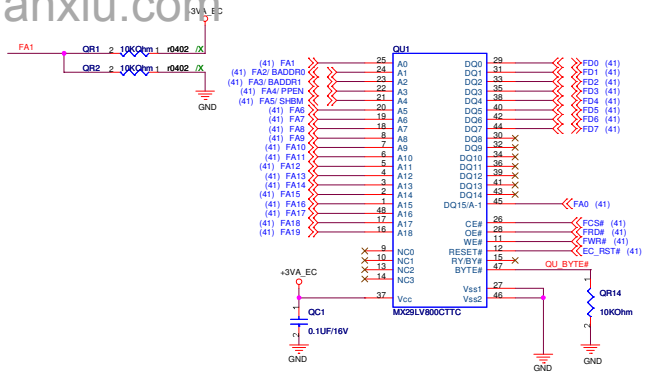
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



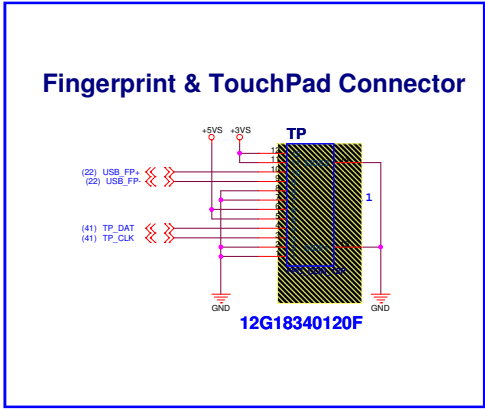
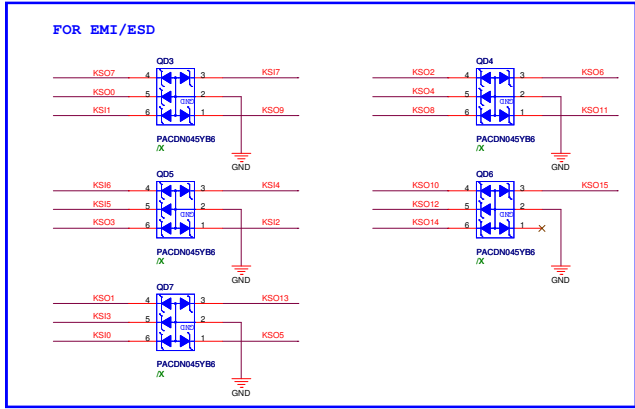
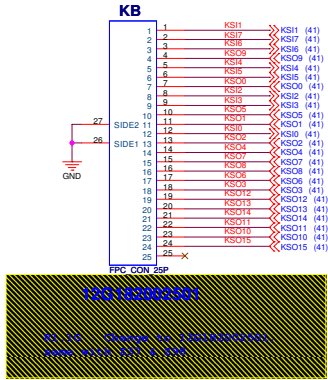
FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS



BIOS : 05G001204043

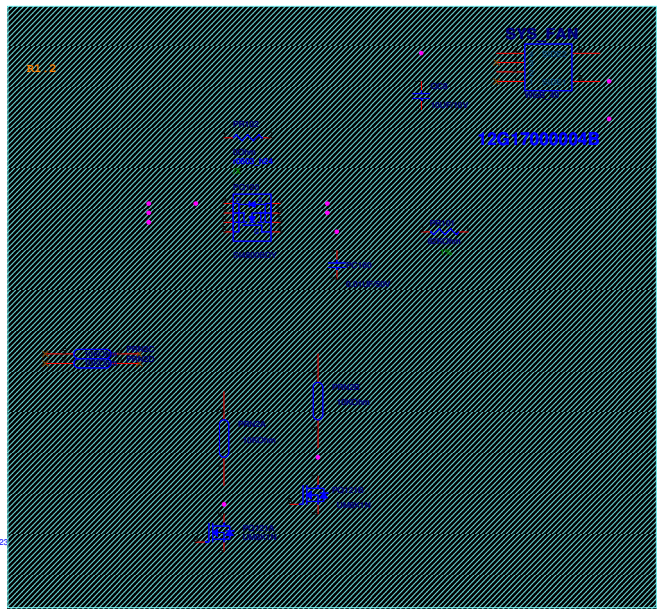
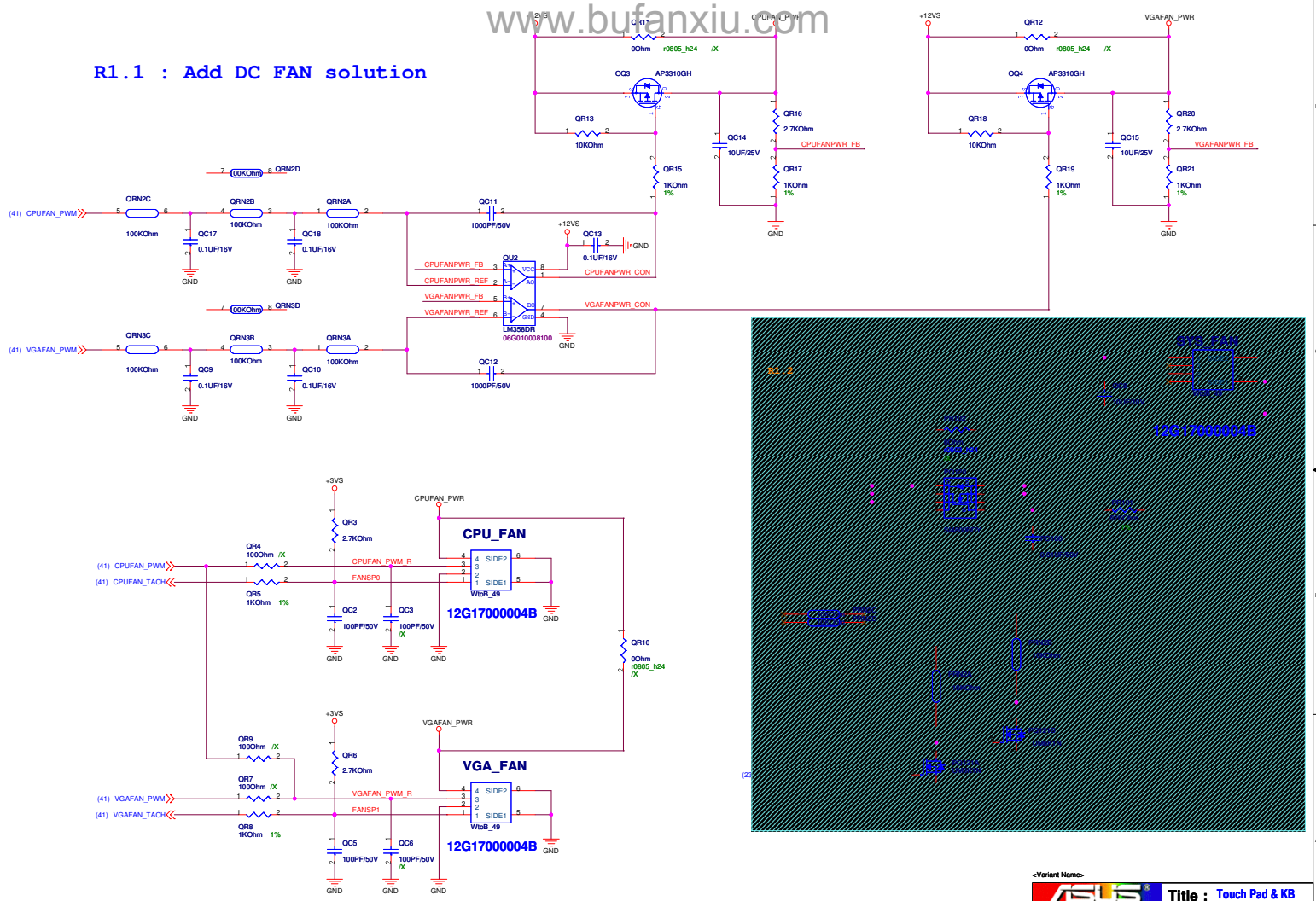
Keyboard Connector



-Variant Name-		ASUS		Title : ISA FLASH ROM	
ASUSTek Computer INC.		Engineer: Chad Lai		Rev: 2.00	
Site: Custom	Project Name: C90S	Date: 05-30-2007		Sheet: 42 of 55	

« Kennedy_Zhang »

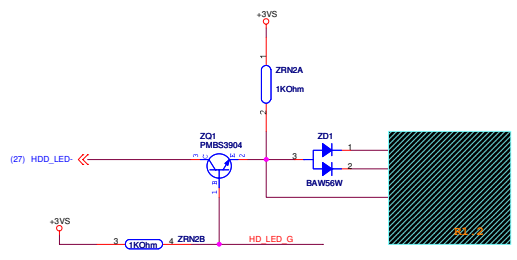
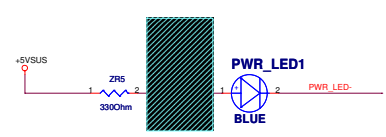
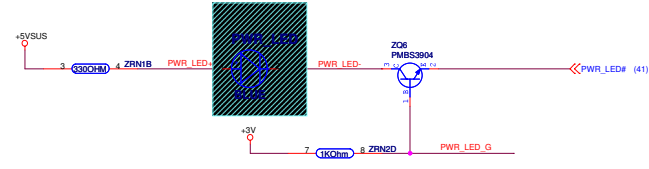
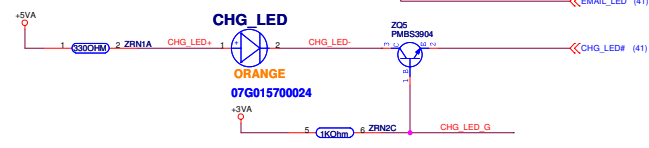
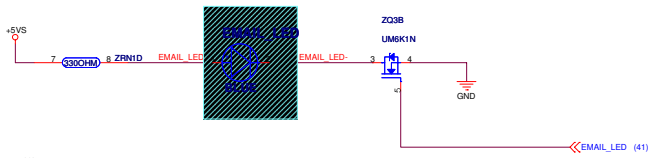
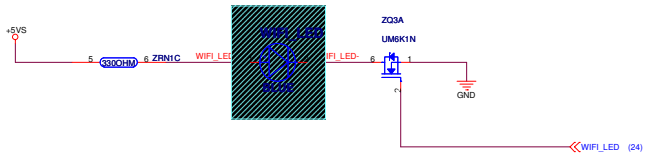
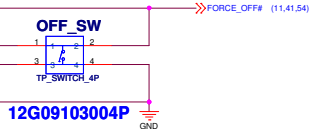
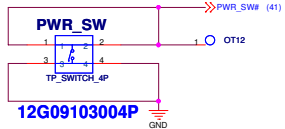
R1.1 : Add DC FAN solution



<Variant Name>

ASUS		Title : Touch Pad & KB	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	C90S	2.0G	
Date: 11/13/2007		Sheet 43	of 55

« Kennedy_Zhang »

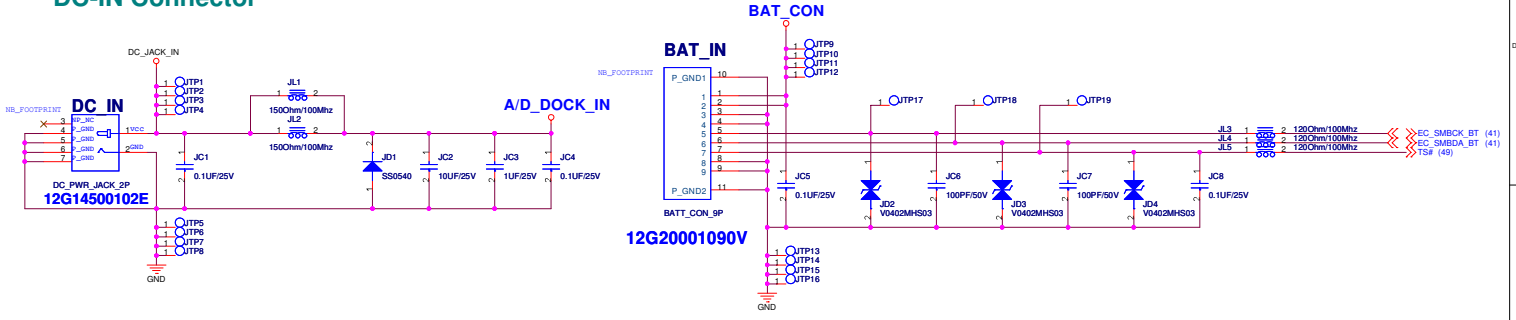


<Variant Name>

ASUS		Title : LED & SW
ASUSTek Computer INC.		Engineer: Chad Lai
Size	Project Name	Rev
Custom	C90S	2.0G
Date: 05/30/2007	Sheet	44 of 55

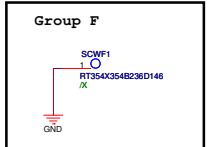
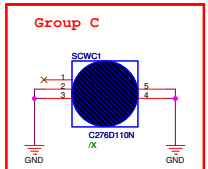
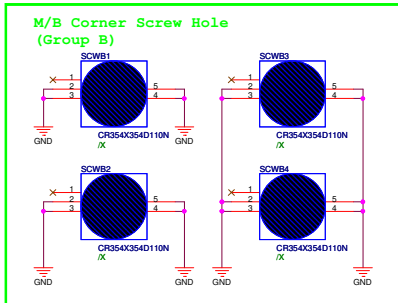
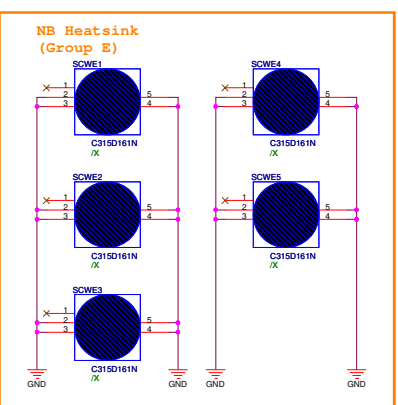
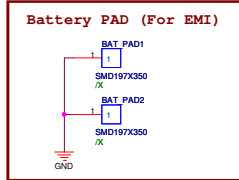
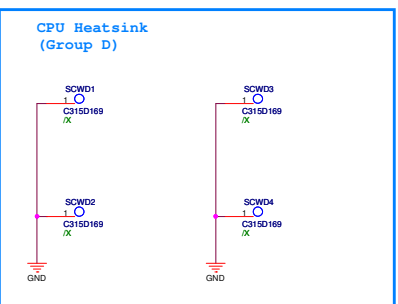
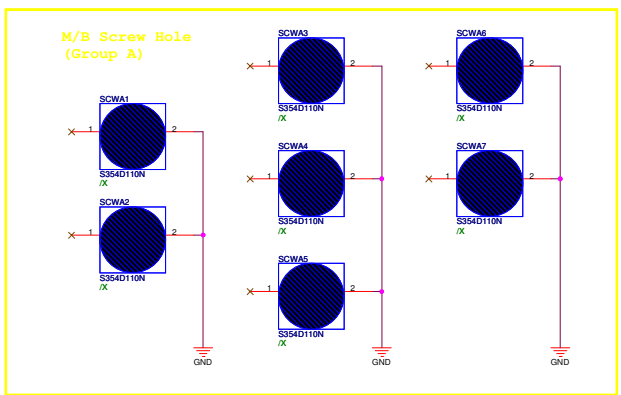
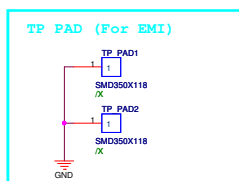
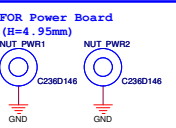
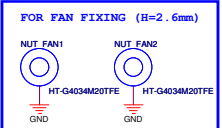
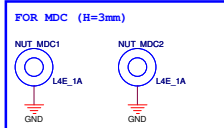
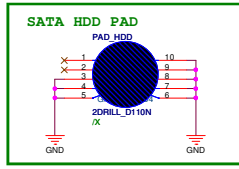
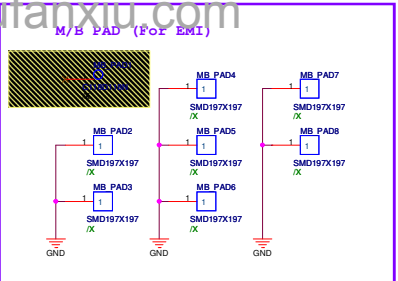
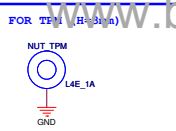
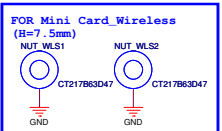
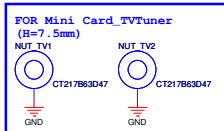
« Kennedy_Zhang »

DC-IN Connector



ASUS		Title : DC IN & BAT IN	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size	Project Name		Rev
Custom	C90S		2.00
Date: 8/11/2007		Sheet	45 of 55

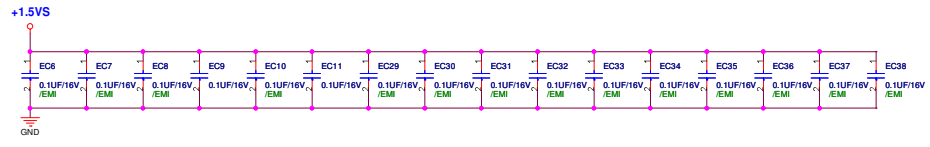
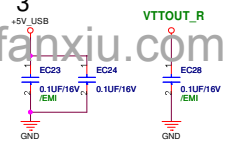
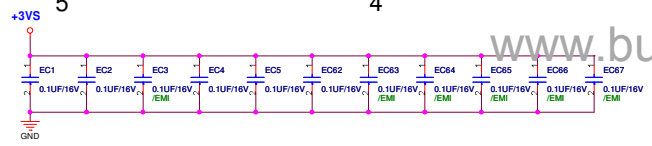
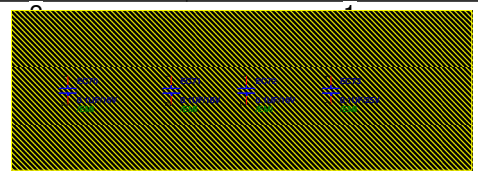
« Kennedy_Zhang »



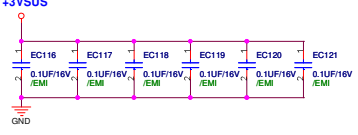
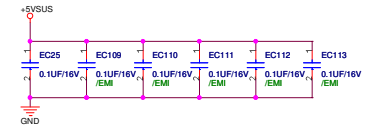
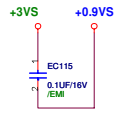
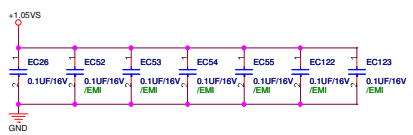
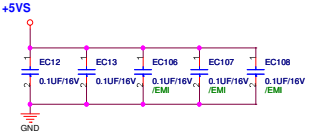
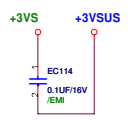
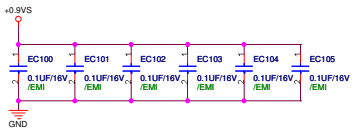
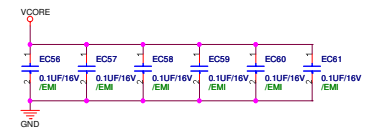
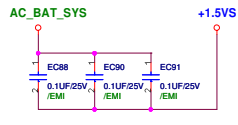
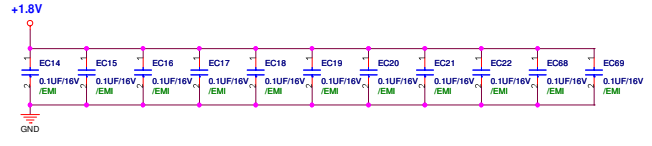
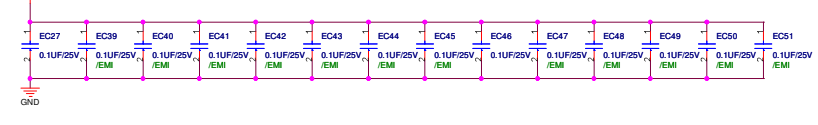
<Variant Name>

ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	C90S	2.00	
Date: 8/11/2007		Sheet: 46	of 55

« Kennedy_Zhang »



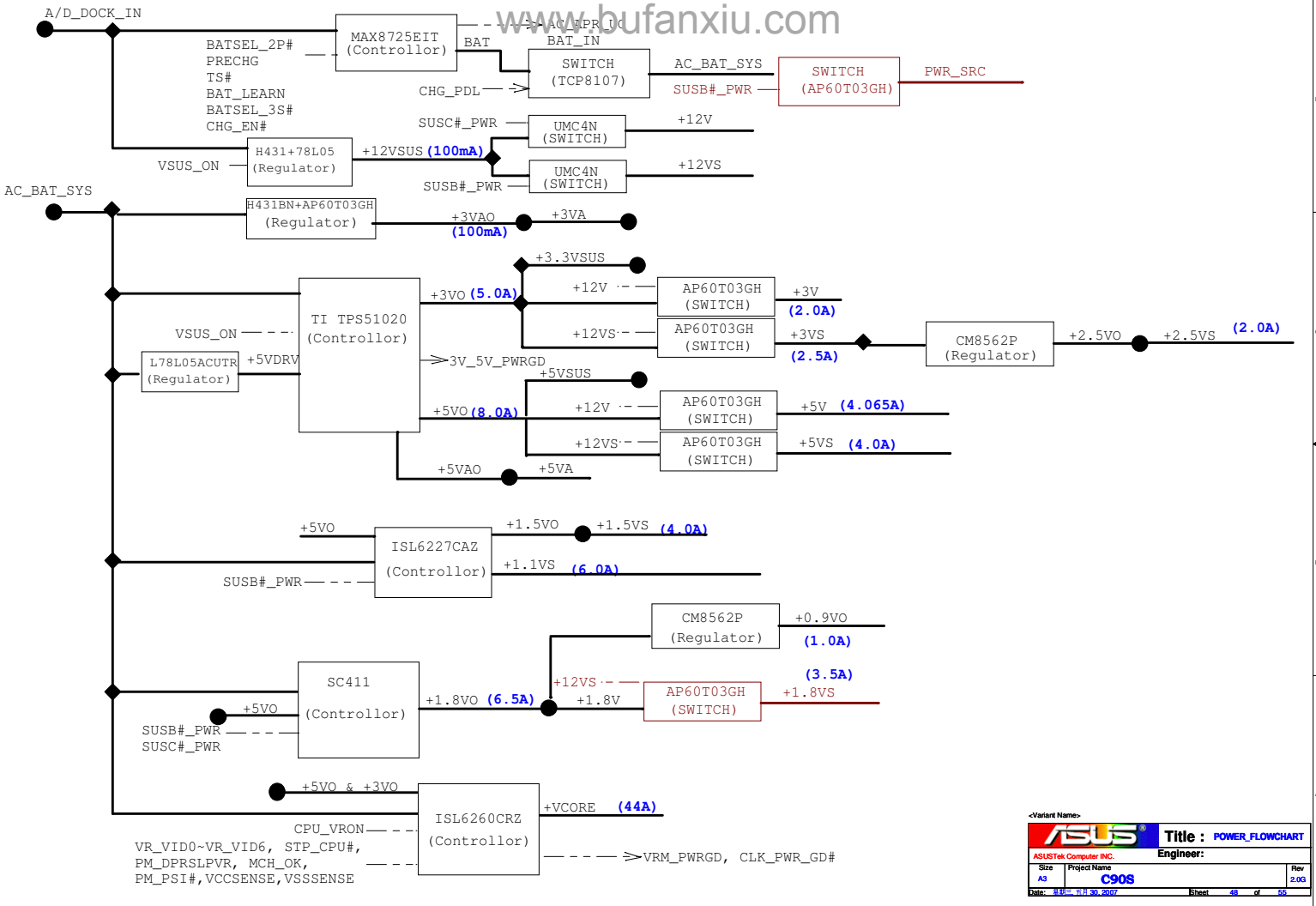
AC_BAT_SYS



-Variant Name-

		Title : EMI CAP	
ASUSTek Computer INC.		Engineer: Chad Lal	
Size	Project Name		Rev
Custom	C90S		2.03
Date: 2007.11.30		Sheet	47 of 55

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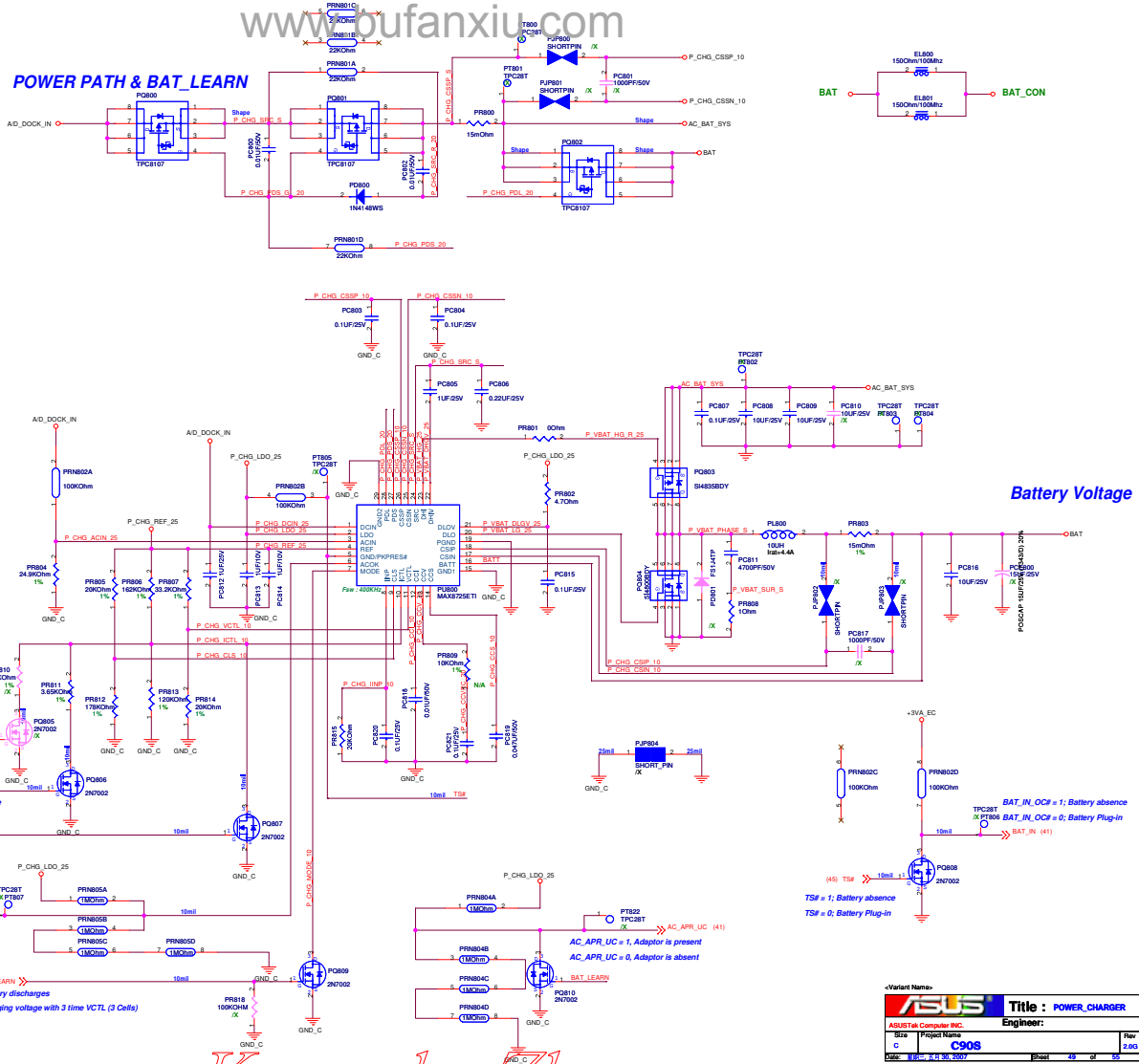


<Variant Name>

ASUS		Title : POWER_FLOWCHART	
ASUSTek Computer INC.		Engineer:	
Site	Project Name	Rev	
AS	C90S	2.00	
Date: 8/18/2007	Sheet	48	of 55

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POWER PATH & BAT_LEARN



Setting the Adapter Input Current Limit

Adapter I_{lim}(max) = [0.075V/Rsense(AD_{IN})] * [VCL5/VREF]
 VCL5 = 2.865V
Adaptor Max. Current :
 PR807 = 20K PR812 = 178K; I_{limit} = 4.5A; 81W
 PR807 = 27K PR812 = 47K; I_{limit} = 3.175A; 60W

Setting the Charge Voltage

V_{batt} = Cell * (V_{ref} + [(VCTL - 1.8V) / 9.52])
 VCTL = 1.588V ⇒ V_{batt} = 4.2V

Setting the Charge Current

Charge Current I_{chg} = [0.075V/Rsense(CHG)] * [VICTL3.6V]
 Rsense(CHG) = 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA
 V_{icl} = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; V_{icl} = 2.084V
 ⇒ I_{charge} = 1.6933A
 BATSEL_2P# = 0, 6 or 9 Cells; V_{icl} = 2.111V
 ⇒ I_{charge} = 2.9329A
 PR814 = 120K PR813 = 120K; I_{charge} = 2.9329A

Mode pin : V_{mode} > 2.8V (try to LDO pin) ⇒ 4 Cells
 2.0 > V_{mode} > 1.6V (floating) ⇒ 3 Cells
 0.8 > V_{mode} (try to GND) ⇒ Learning mode
 VICTL < 0.8V or DCIN < 7V ⇒ Charger Disable

MAX8725_REF : 4.2235V
 MAX8725_LDO : 5.4V

(4) BATSEL_2P#
 BATSEL_2P# = 1, 3 Cells
 BATSEL_2P# = 0, 6 or 9 Cells

(4) PRECHG
 PRECHG = 1, Pre-Charging Mode
 Charging Current = 156mA

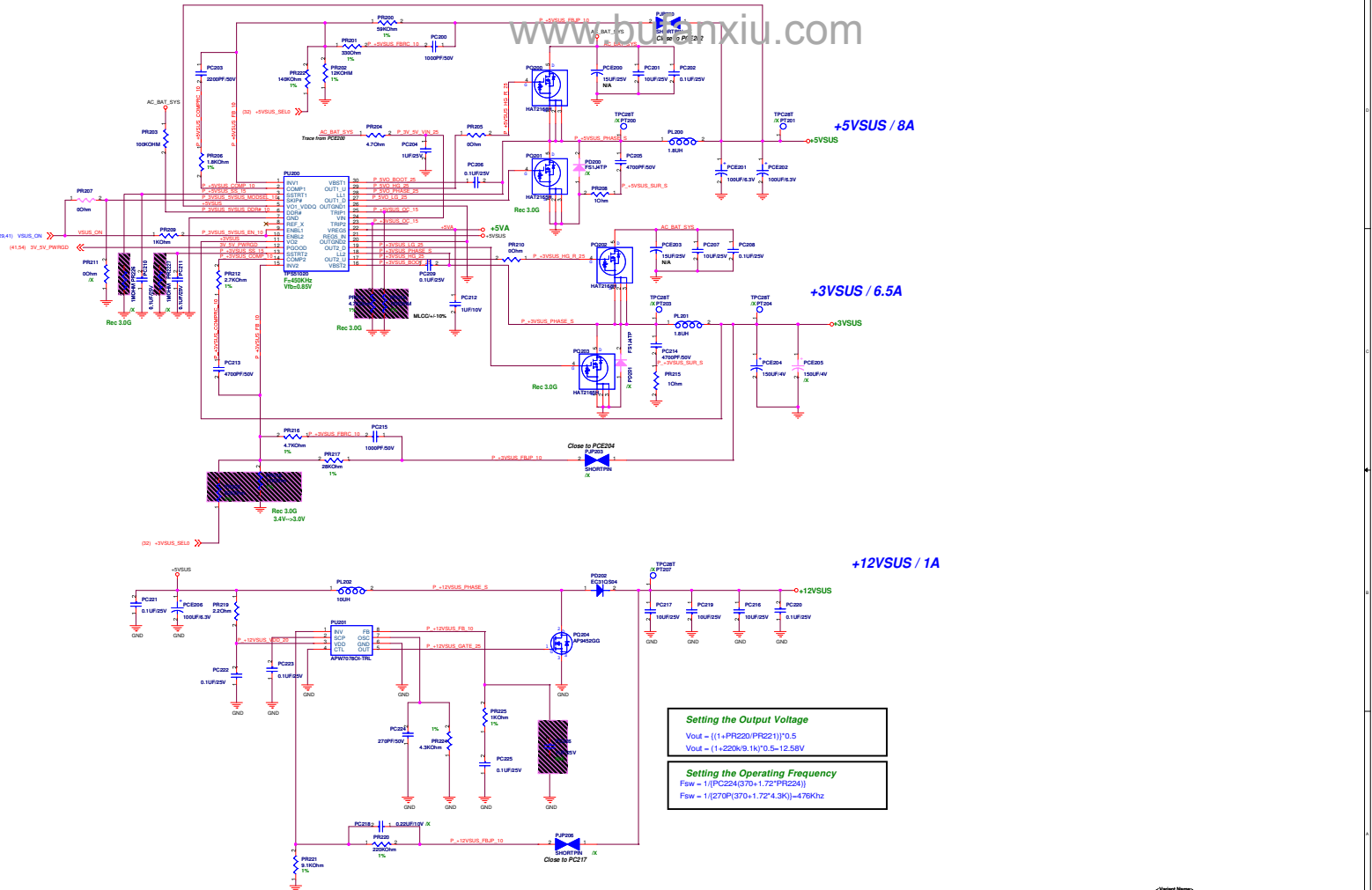
(4) CHG_EN#
 CHG_EN# = 1, Charger Disabled
 CHG_EN# = 0, Charger Enabled

(16:41:51) AC_OK
 AC_OK = 1, Adaptor is present
 AC_OK = 0, Adaptor is absent

(4) BAT_LEARN
 BAT_LEARN = 1, Battery discharges
 BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

ASUS		Title : POWER_CHARGER	
ASUSTek Computer INC.	Engineer:		
Sz2	Project Name	Rev	
C	C908	2/03	
Date: 2013-10-20 20:07		Sheet	49 of 50

« Kennedy_Zhang »

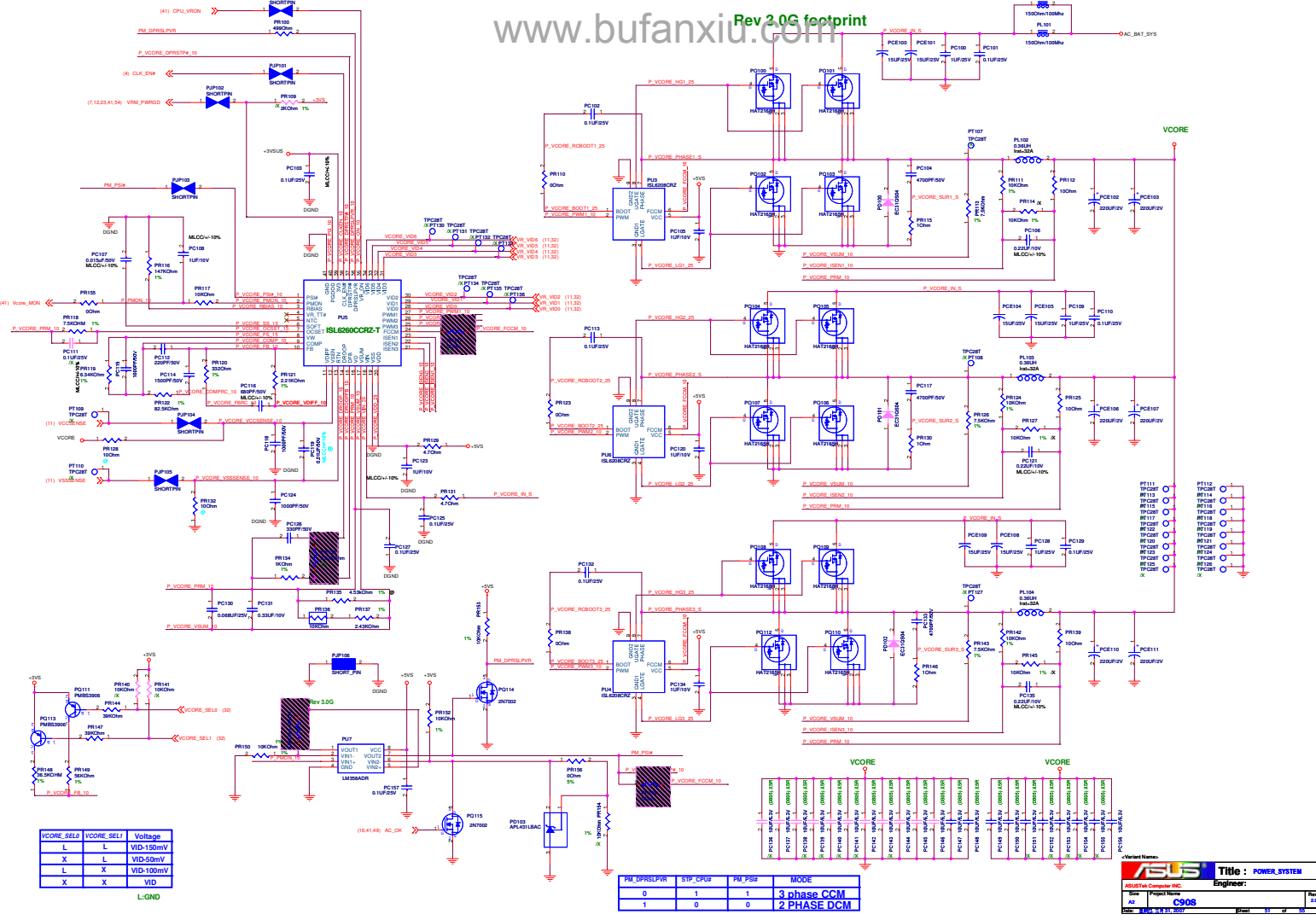


Setting the Output Voltage
 $V_{out} = ((1 + PR220/PR221)) * 0.5$
 $V_{out} = (1 + 220k/9.1k) * 0.5 = 12.58V$

Setting the Operating Frequency
 $F_{sw} = 1 / (2 * 70P(370 + 1.72 * 4.3K)) = 476KHz$

ASUS		Title : POWER_SYSTEM
ASUSTek Computer INC	Engineer:	
Size	Project Name	Rev
A0	C908	2.00
Date	2012-11-28	Page 2 of 2

<< Kennedy_Zhang >>



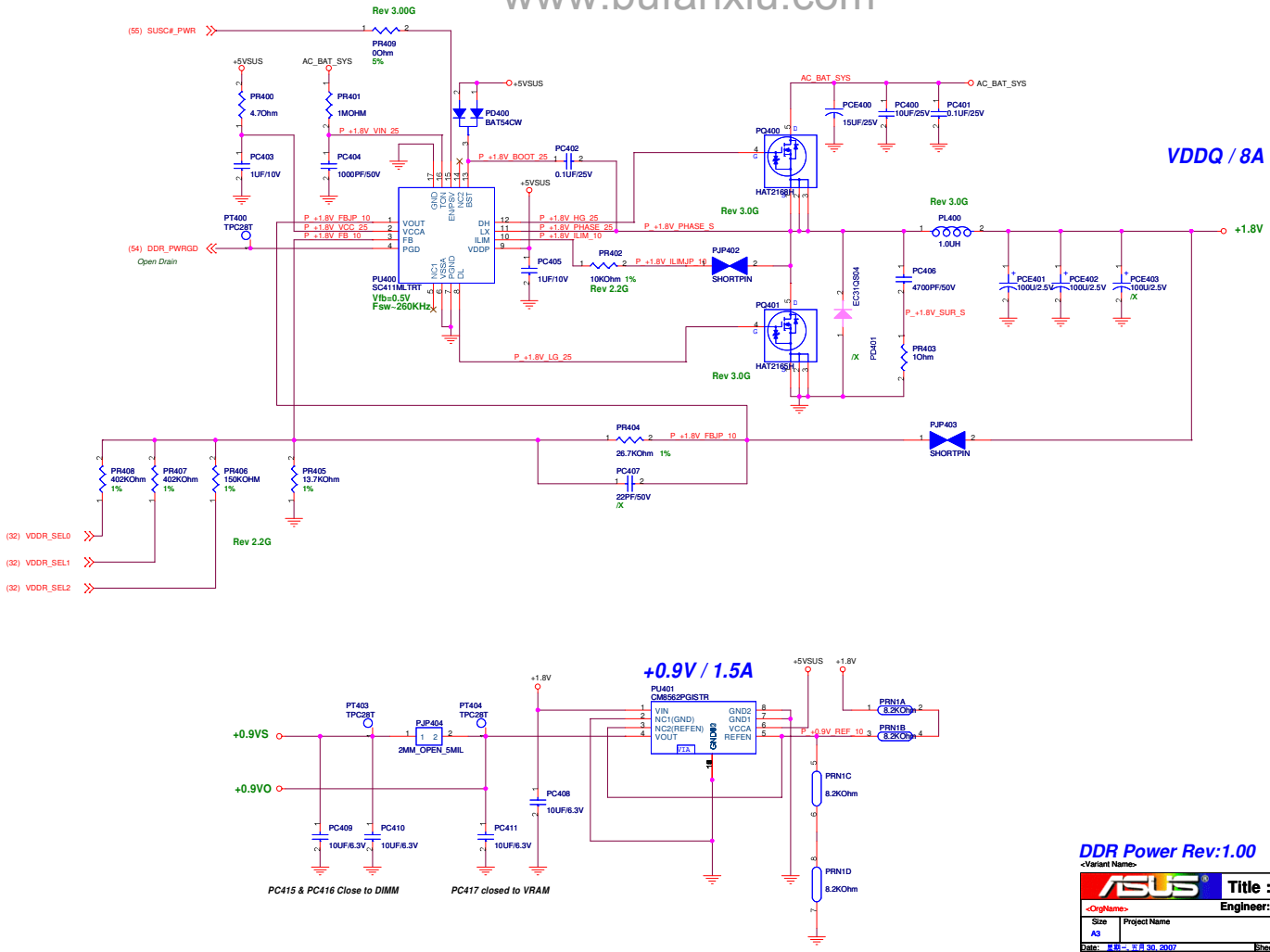
Vcore_sel0	Vcore_sel1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID

L-GND

PM_DPRSLFVR	STP_CRP	PM_PSR	MODE
0	1	1	3 phase CCM
1	0	0	2 PHASE DCM

ASUS Title: POWER_SYSTEM
 Engineer:
 C908
 Rev: 1.0

<< Kennedy_Zhang >>

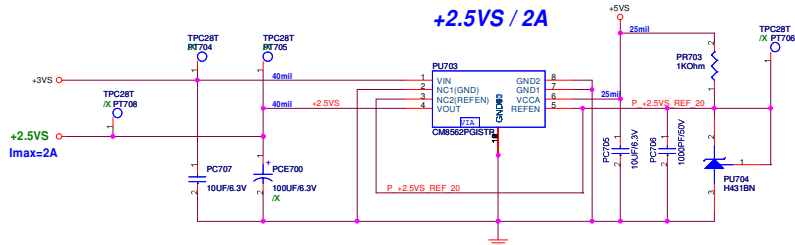
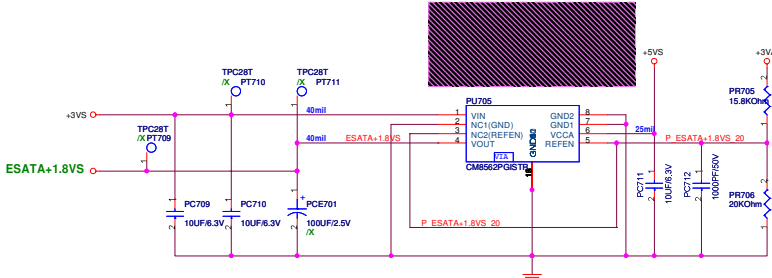
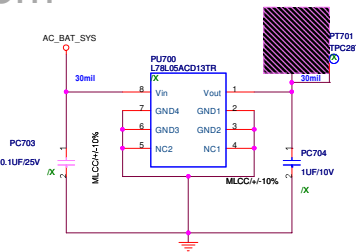
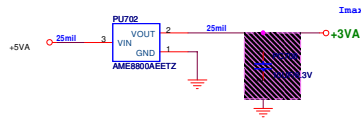
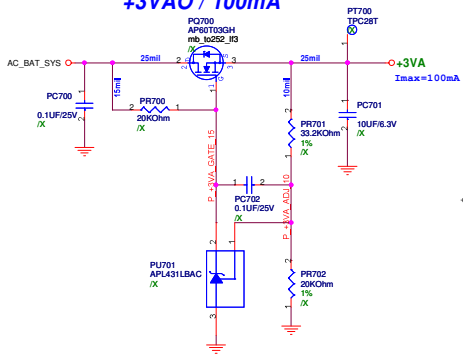


DDR Power Rev:1.00

ASUS		Title :
-<OrigName>		Engineer:
Size	Project Name	Rev
A3		2.0G
Date:	## - ## 30, 2007	Sheet 62 of 69

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+3VAO / 100mA

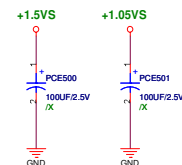
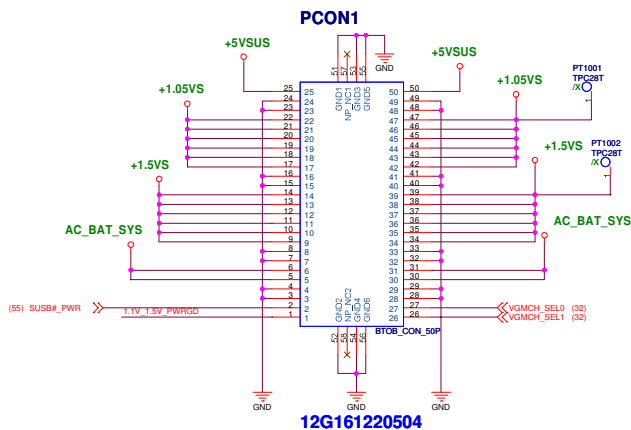
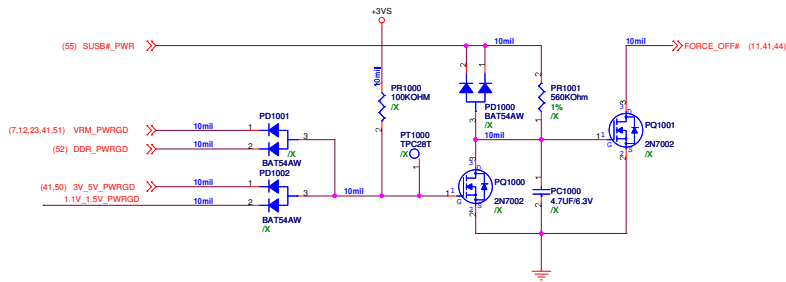


<Variant Name>

ASUS		Title : POWER_IO_+3VA & +2.5V	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	C90S	2.00	
Date: 8/21/2007		Sheet 53	of 53

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Power Good Detector



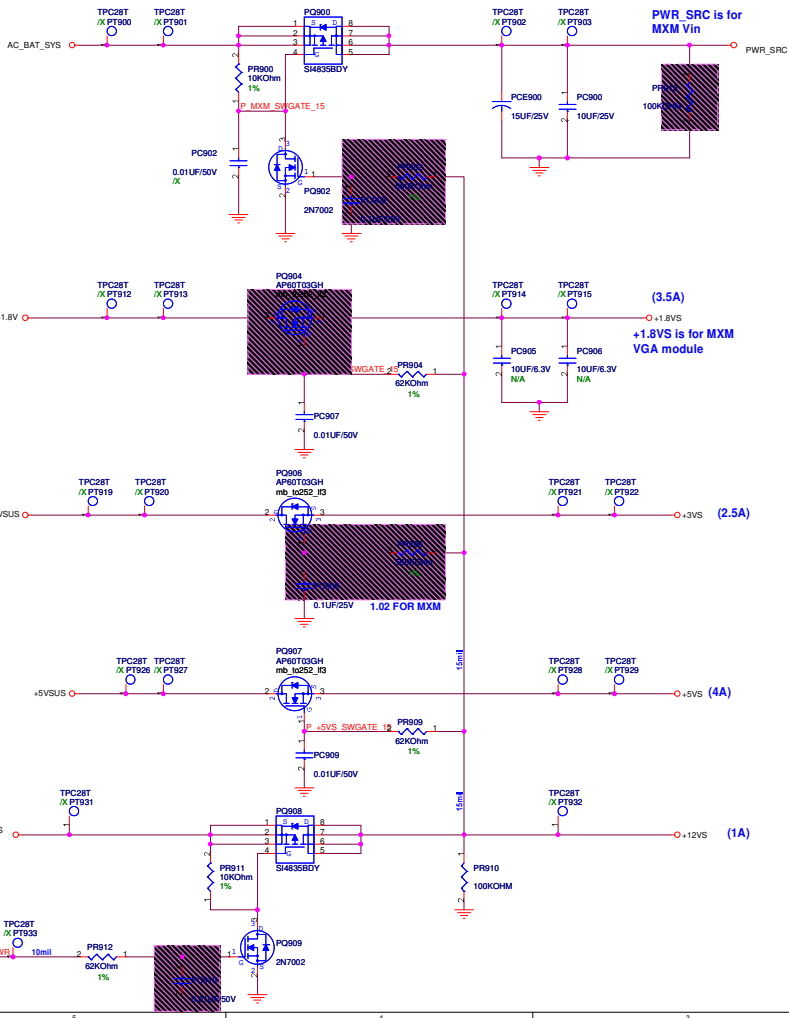
Near NB & SB

<Variant Name>

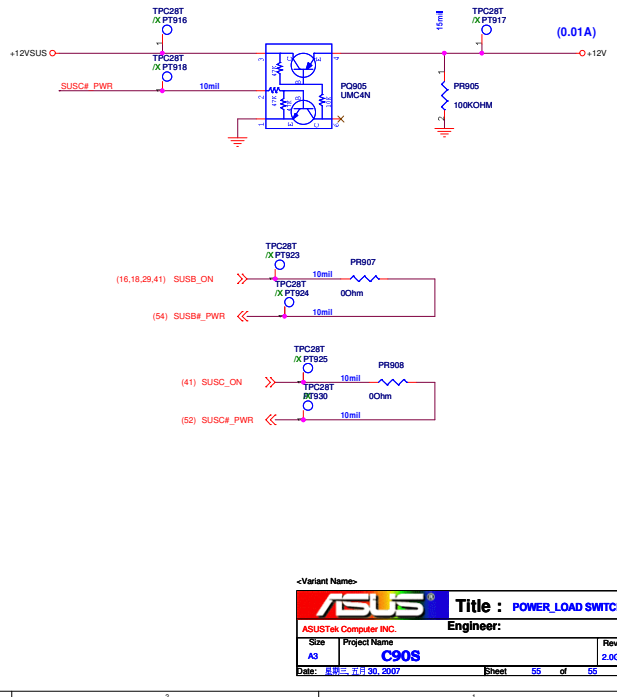
ASUS		Title : POWER_PROTECT	
ASUSTek Computer INC.		Engineer:	
Site	Project Name	Rev	
Custom	C90S	2.00	
Date: 2007.05.30	2007	Sheet	54 of 55

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SUSB#_PWR POWER



SUSC#_PWR POWER



<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
ASUSTek Computer INC.			
Engineer:			
Site	Project Name	Rev	
A3	C90S	2.0G	
Date: 五月 30, 2007	Sheet		55 of 55

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