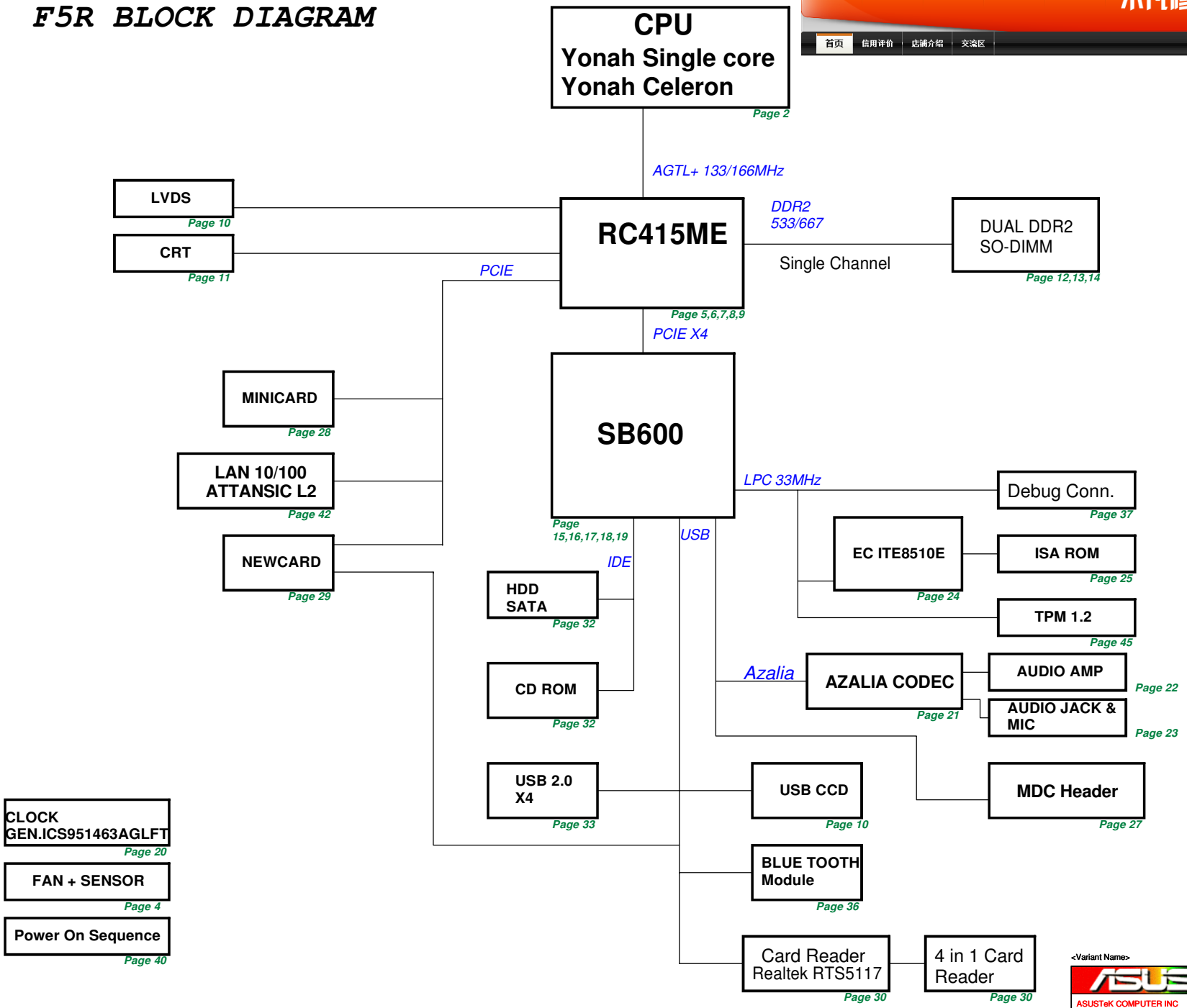
F5R BLOCK DIAGRAM



<Variant Name>

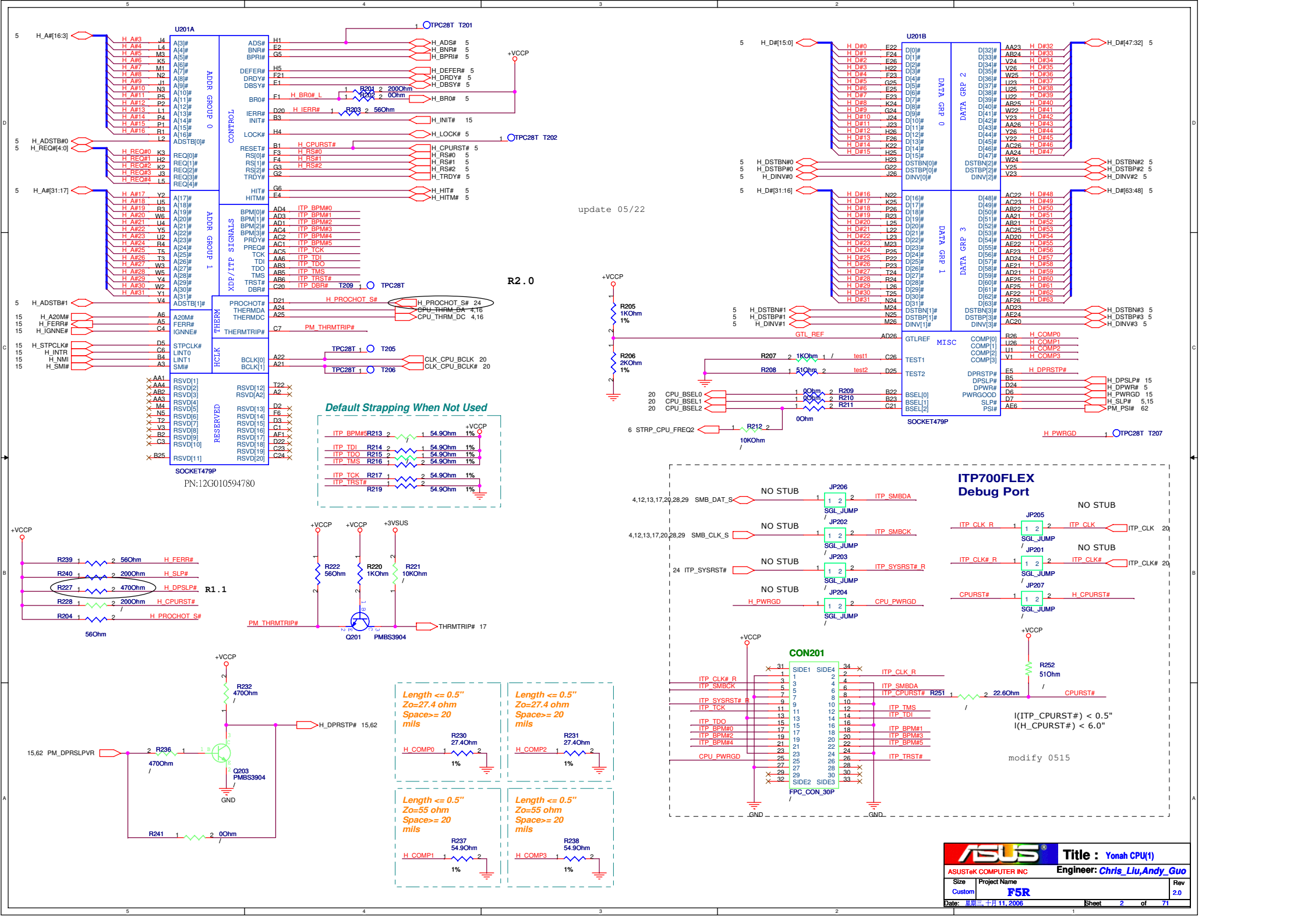
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

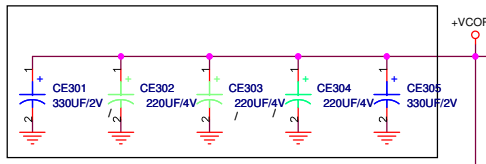
Engineer: Chris_Liu,Andy_Guo

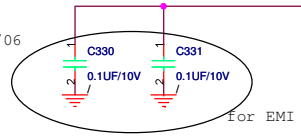
Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 1 of 71

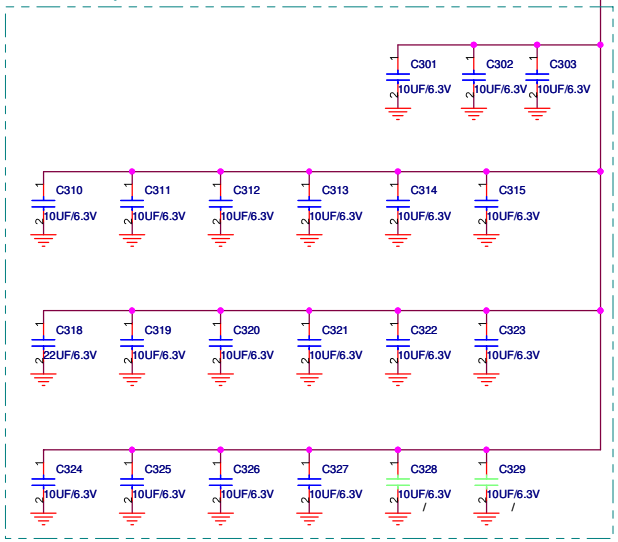

U201A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
SOCKET479P
PN:12G010594780
R2.0
update 05/22
U201B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET479P
Default Strapping When Not Used
R1.1
Q201 PMBS3904
Q203 PMBS3904
ITP700FLEX
Debug Port
CON201
FPC_CON_30P
NO STUB
SGL_JUMP
I(ITP_CPURST#) < 0.5"
I(H_CPURST#) < 6.0"
modify 0515
Length <= 0.5" Zo=27.4 ohm Space>= 20 mils
Length <= 0.5" Zo=55 ohm Space>= 20 mils
Title : Yonah CPU(1)
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Size: Custom
Project Name: F5R
Rev: 2.0
Date: 星期三, 十月 11, 2006
Sheet 2 of 71

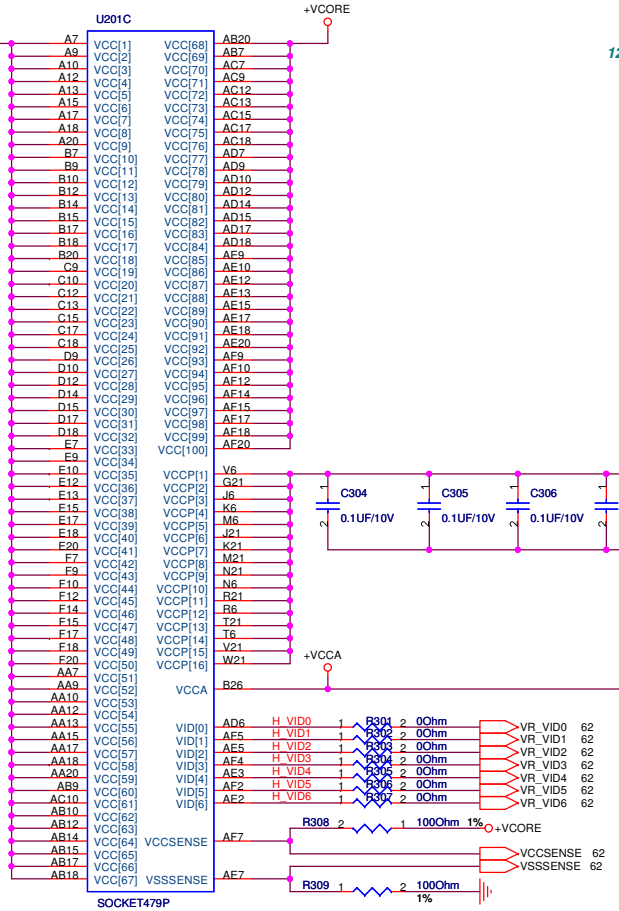
R1.1

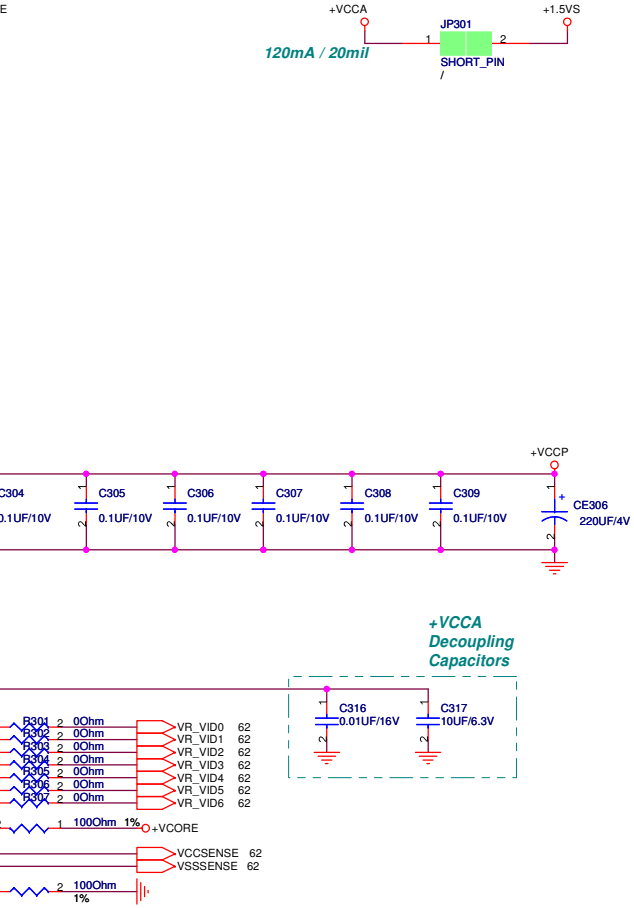




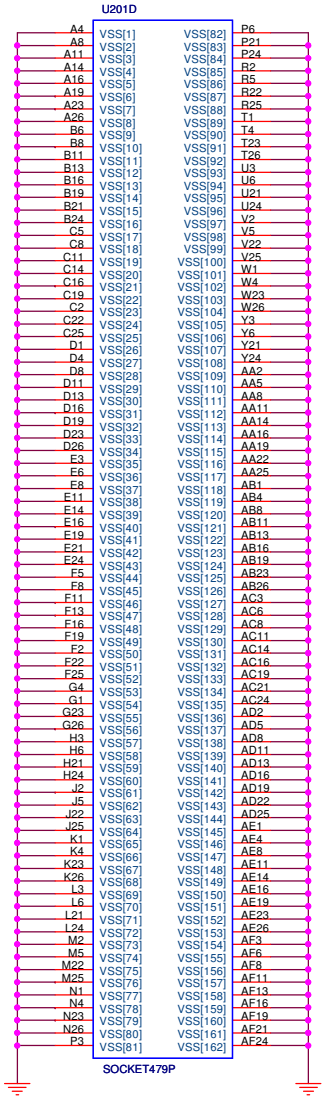
CPU +VCORE Mid-Frequency Capacitors







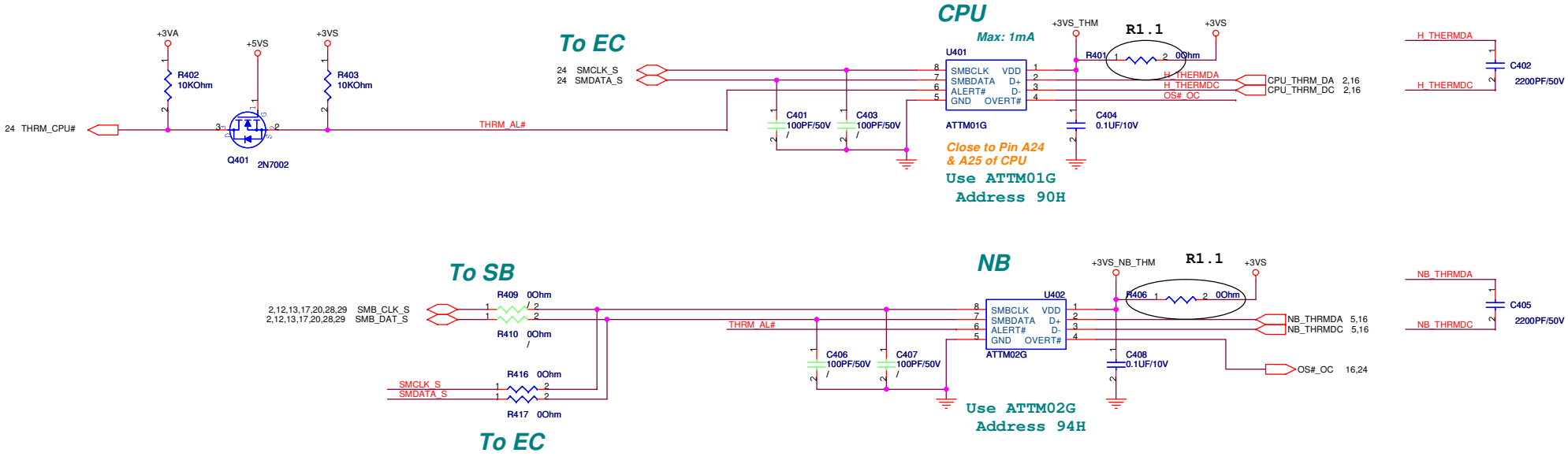
+VCCA Decoupling Capacitors



+VCORE Low-Freq Capacitor
Intel: 330UF *6
ATI: 330UF *6
R1F: 330UF *4
A7J: 330UF *5
F5X: 330UF *5
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
ATI: 10UF *26
R1F: 22UF *16
A7J: 22UF*29 use 19
A6RF: 22UF*21 use 21
F5X: 10UF *21 use 19
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4
A7J: 220UF *1, 0,1UF *6
A6RF: 220UF *1, 0,1UF *6
F5X: 220UF *1, 0.1UF *6

ASUSTeK COMPUTER INC	Title : Yonah CPU(2)	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 3 of 71	

Thermal Sensor

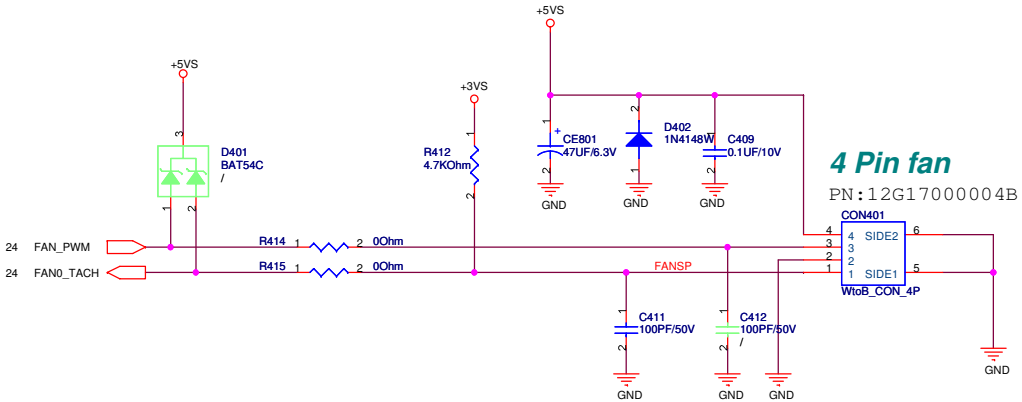


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

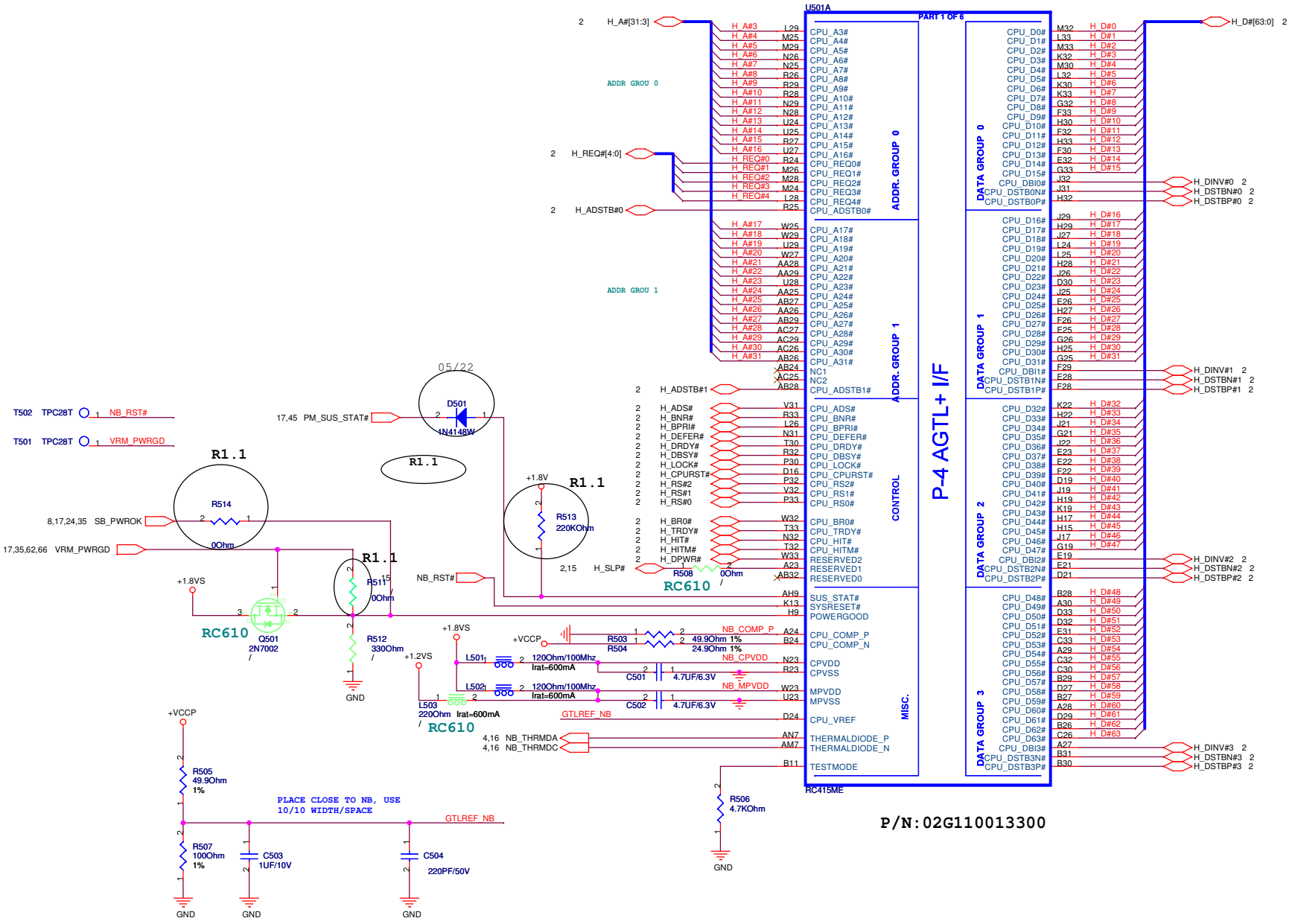
Avoid FSB,Power

DC FAN Control



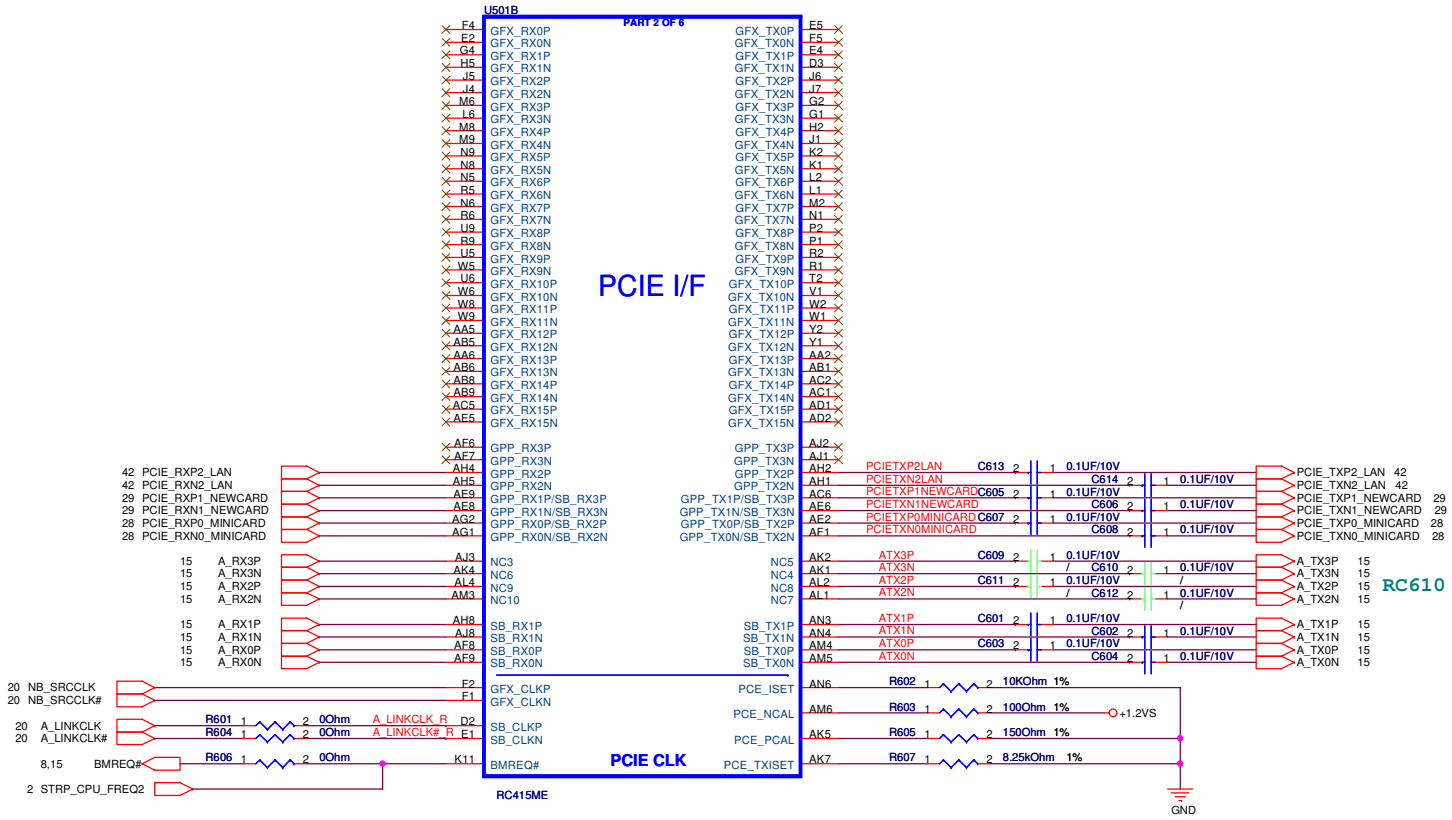
<Variant Name>

ASUSTeK COMPUTER INC	Title : THER SENSOR & FAN	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 4 of 71	



<Variant Name>

ASUSTeK COMPUTER INC	Title : RC415M(HOST)	
	Engineer: Chris_liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 5 of 71	



<Variant Name>

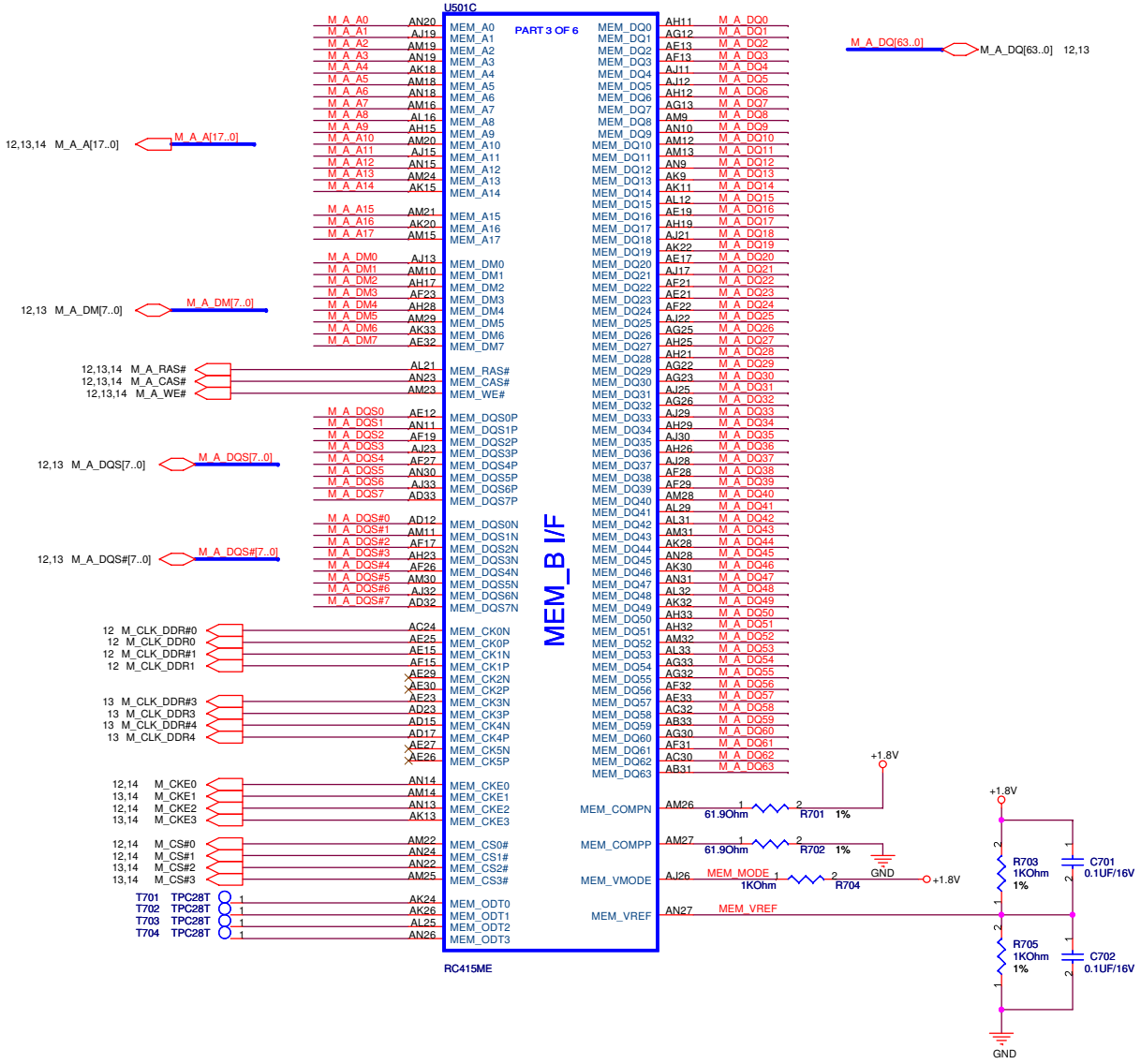
Title : RC415M(2)

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 6 of 71



<Variant Name>

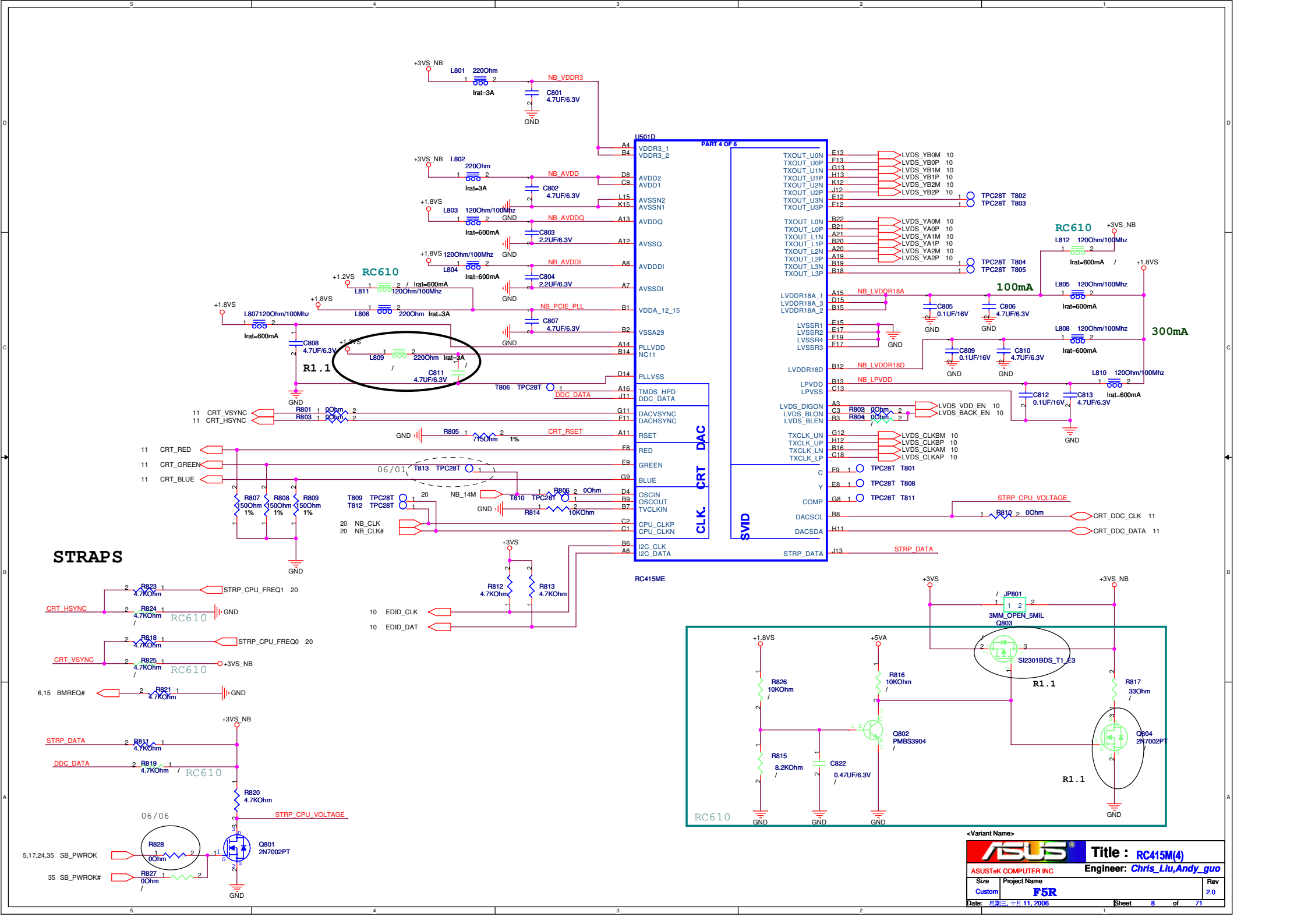
Title : RC415M(3)

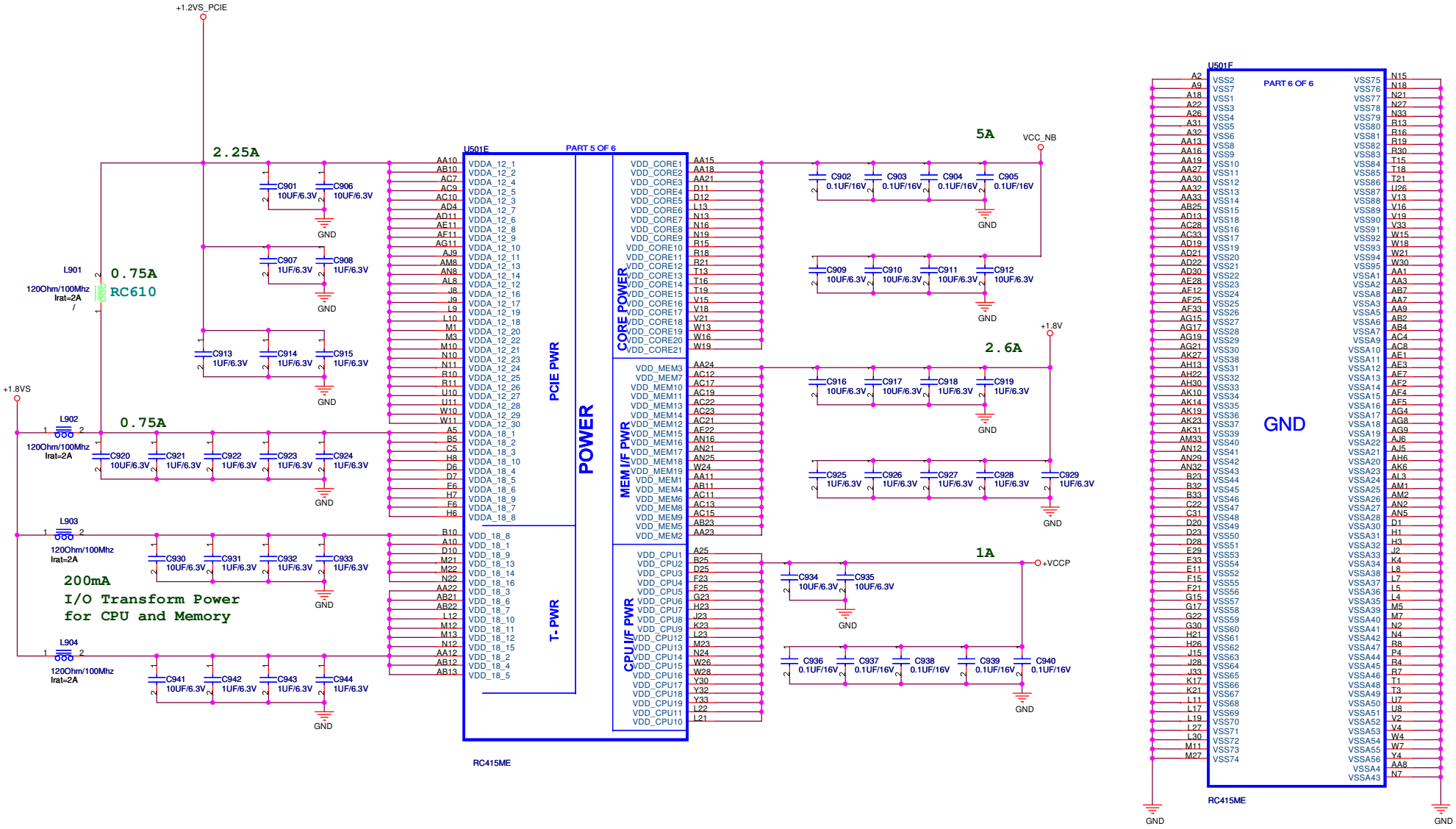
ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 7 of 71


STRAPS
U501D
PART 4 OF 6
RC415ME
RC610
100mA
300mA
R1.1
06/01
06/06
Title : RC415M(4)
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_guo
Size Custom
Project Name F5R
Rev 2.0
Date: 星期三, 十月 11, 2006
Sheet 8 of 71
<Variant Name>



<Variant Name>

ASUSTeK COMPUTER INC

Title : RC415M(5)

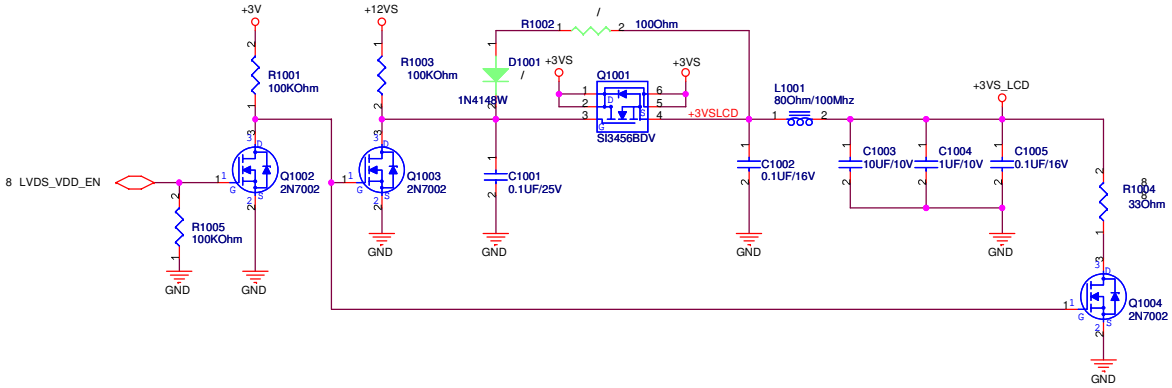
Engineer: Chris_liu,Andy_guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 9 of 71

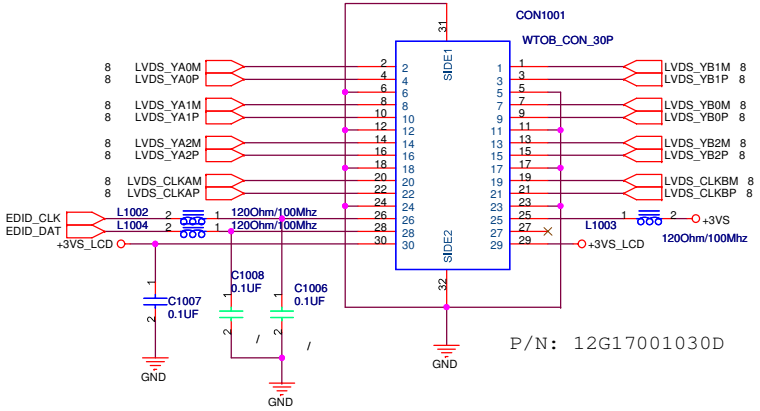
LCD Backlight Control

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

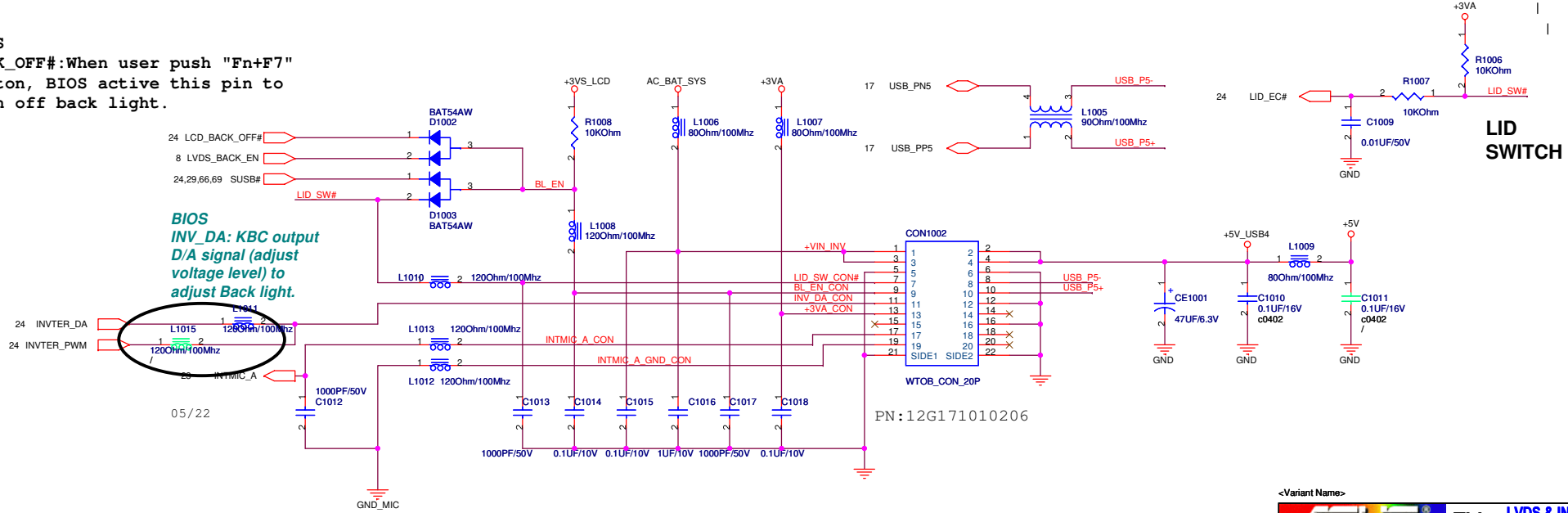
LCD LVDS Interface



P/N: 12G17001030D

INVERTER Interface

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



PN:12G171010206

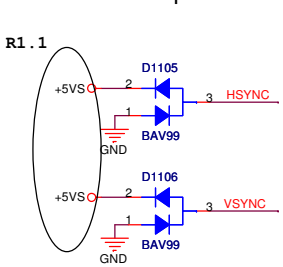
<Variant Name>

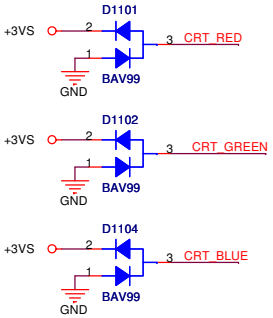
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 10 of 71	

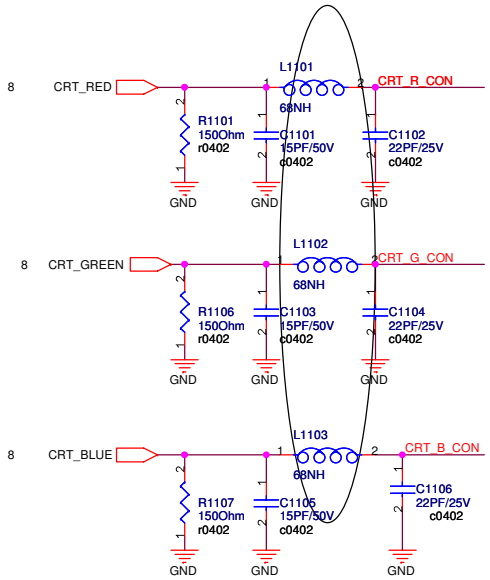
R2.0

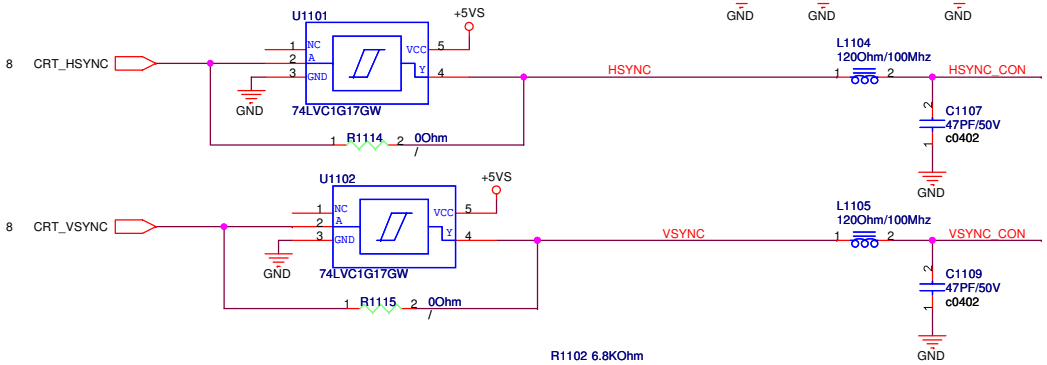
PLACE ESD Diodes near
VGA port

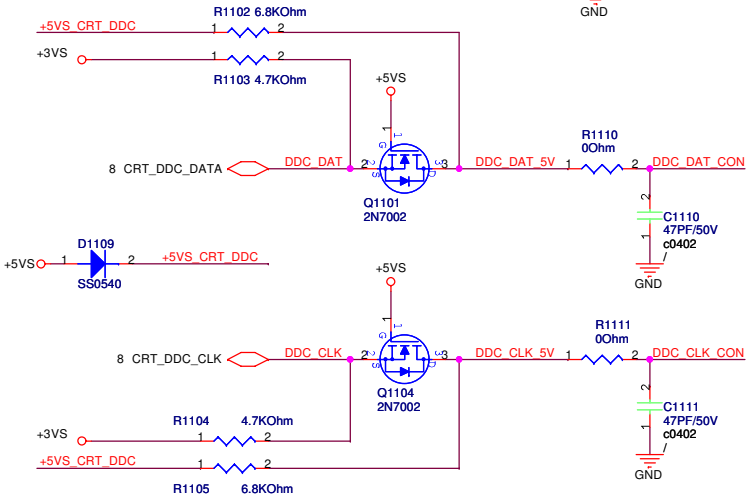
R1.1

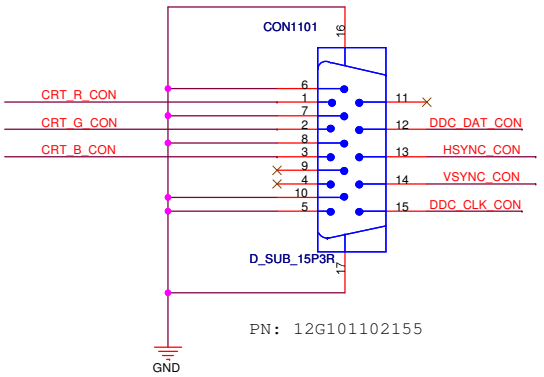












PN: 12G101102155

<Variant Name>

ASUSTeK COMPUTER INC

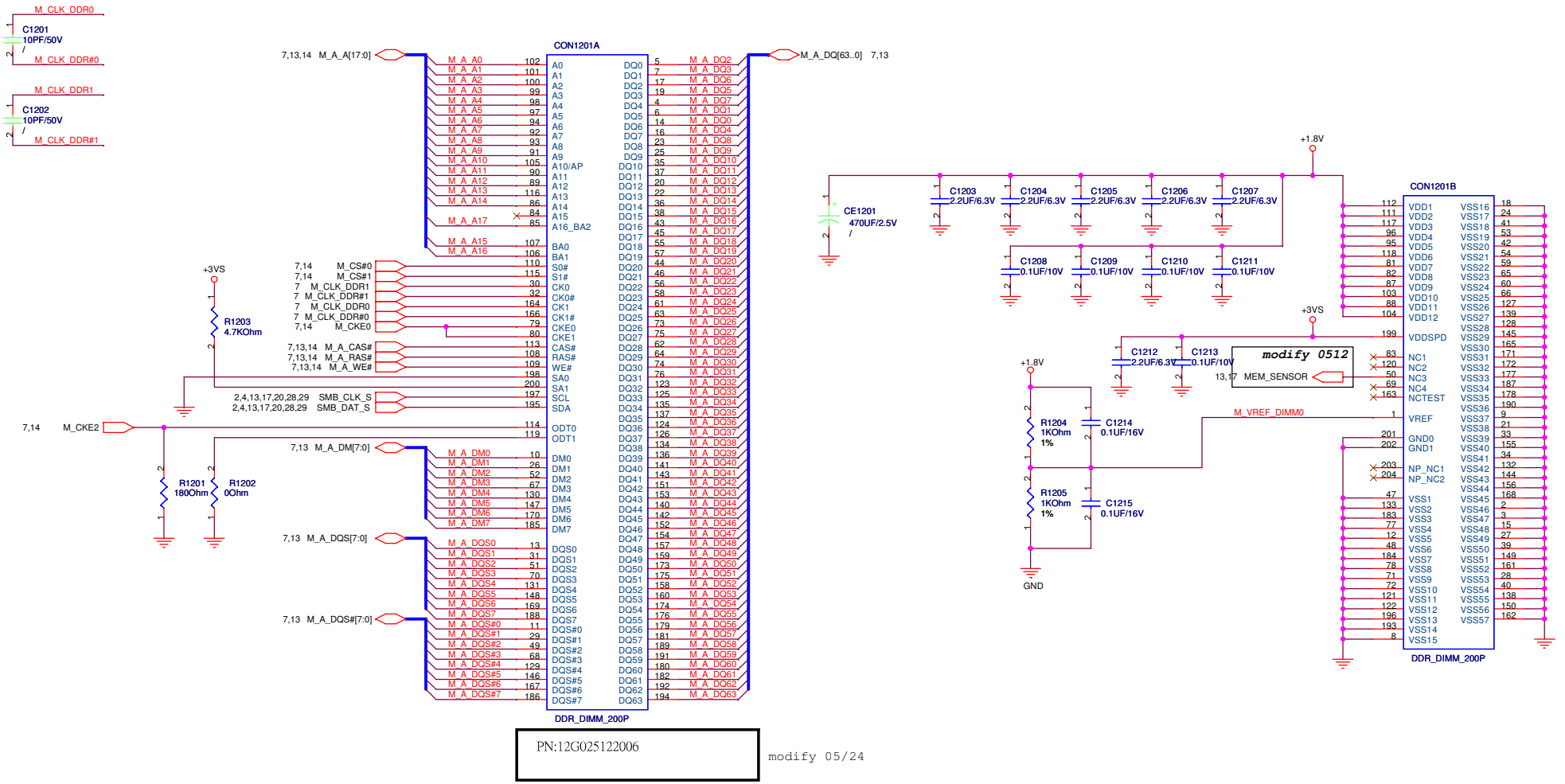
Title : CRT

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 11 of 71

TOP

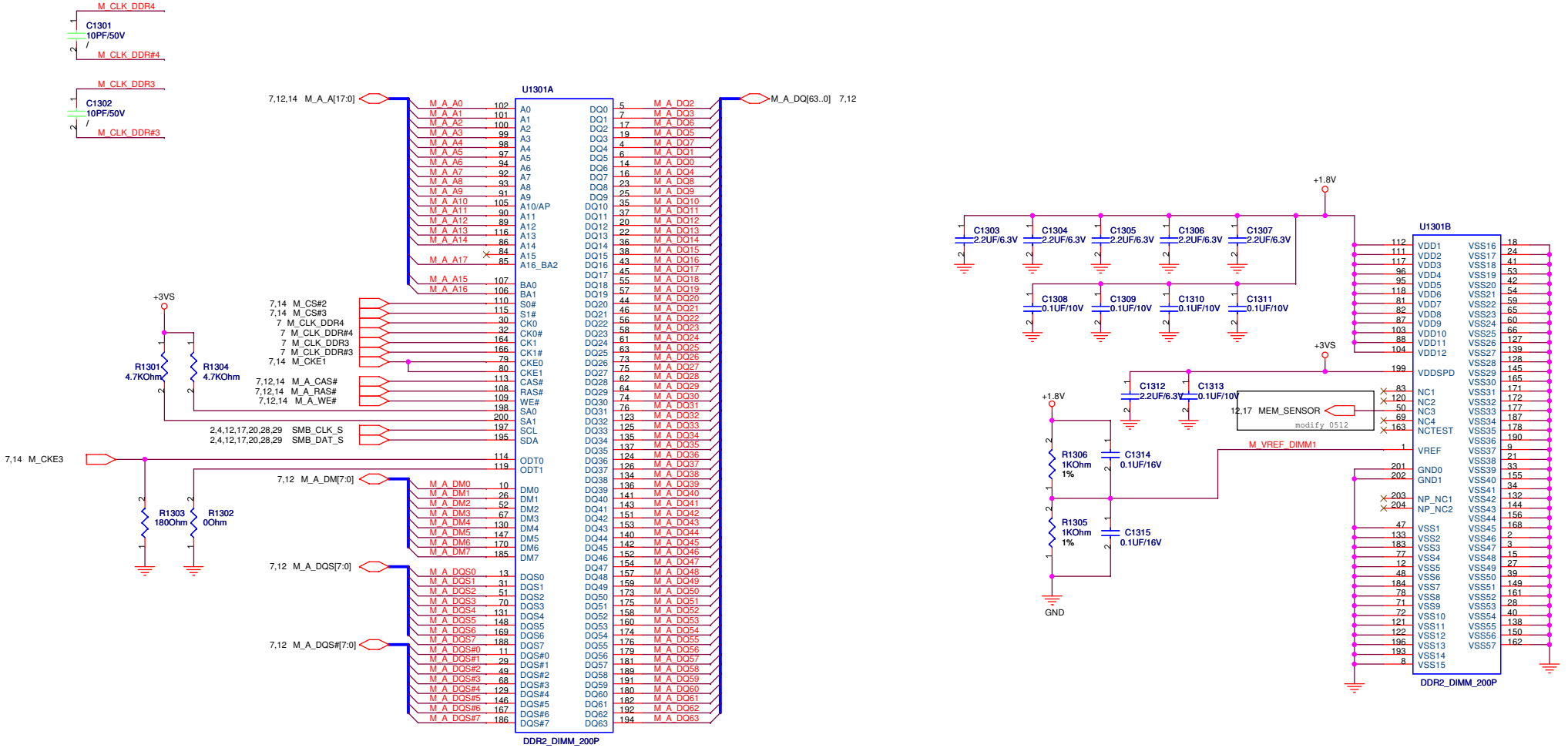


PN:12G025122006

modify 05/24

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM1	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 12 of 71	



PN:12G025C22002 REV.

<Variant Name>

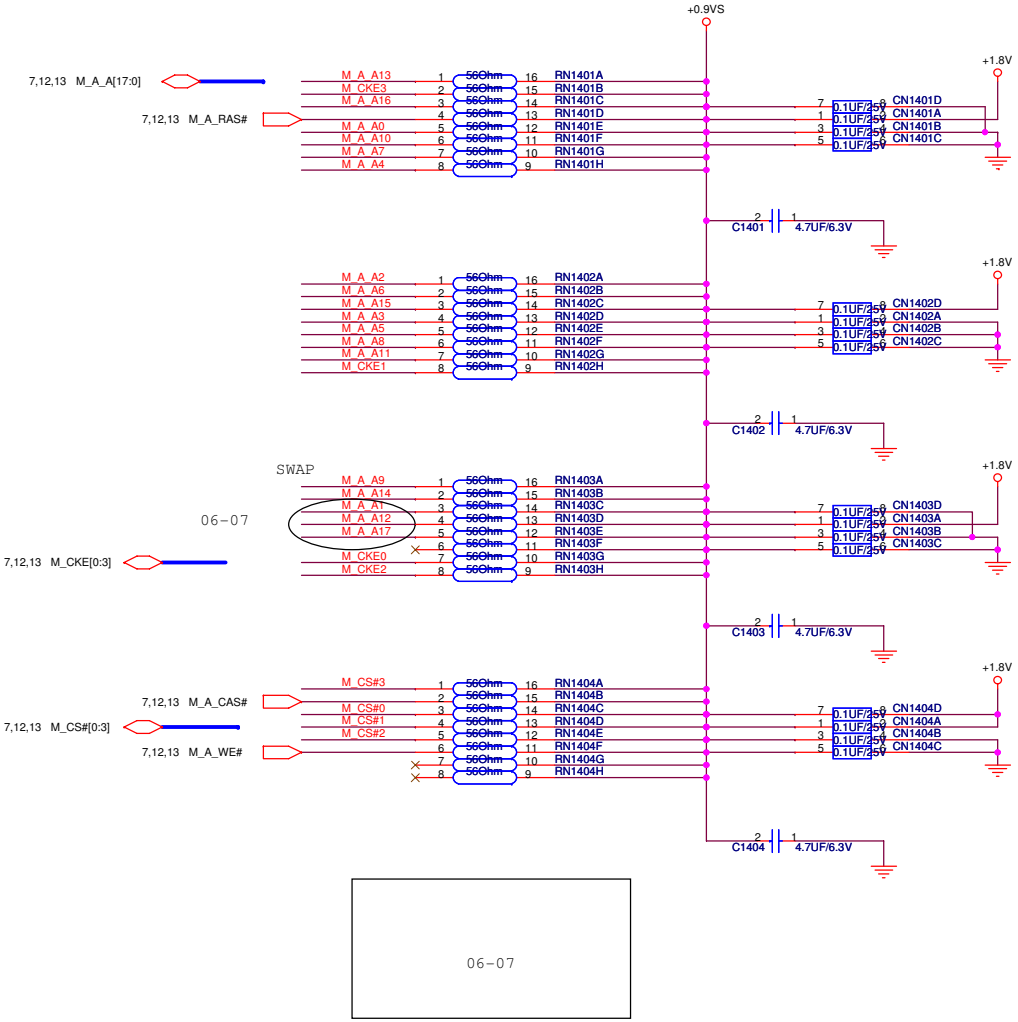
ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM1

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 13 of 71



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 TERMINATION

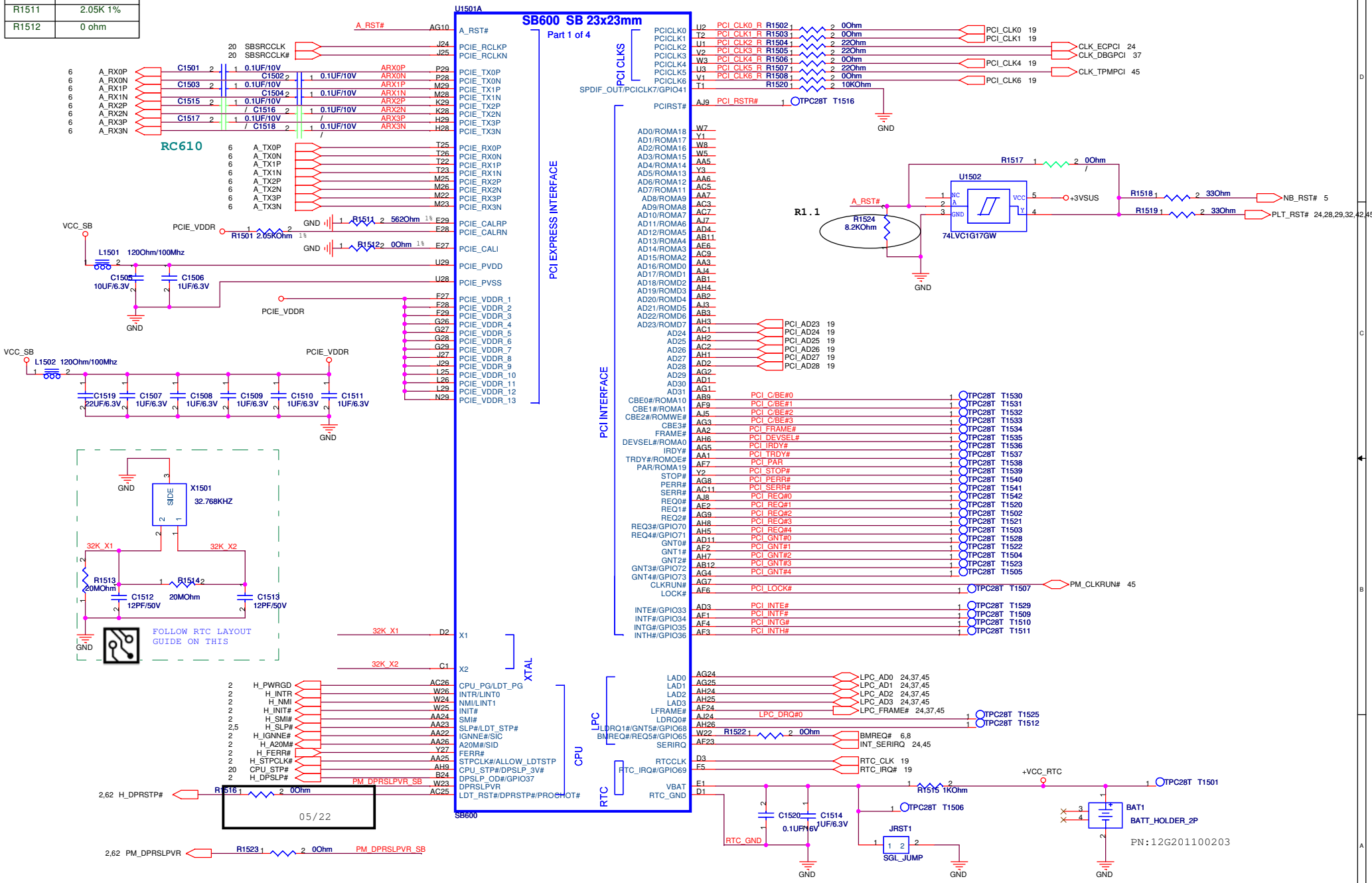
Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

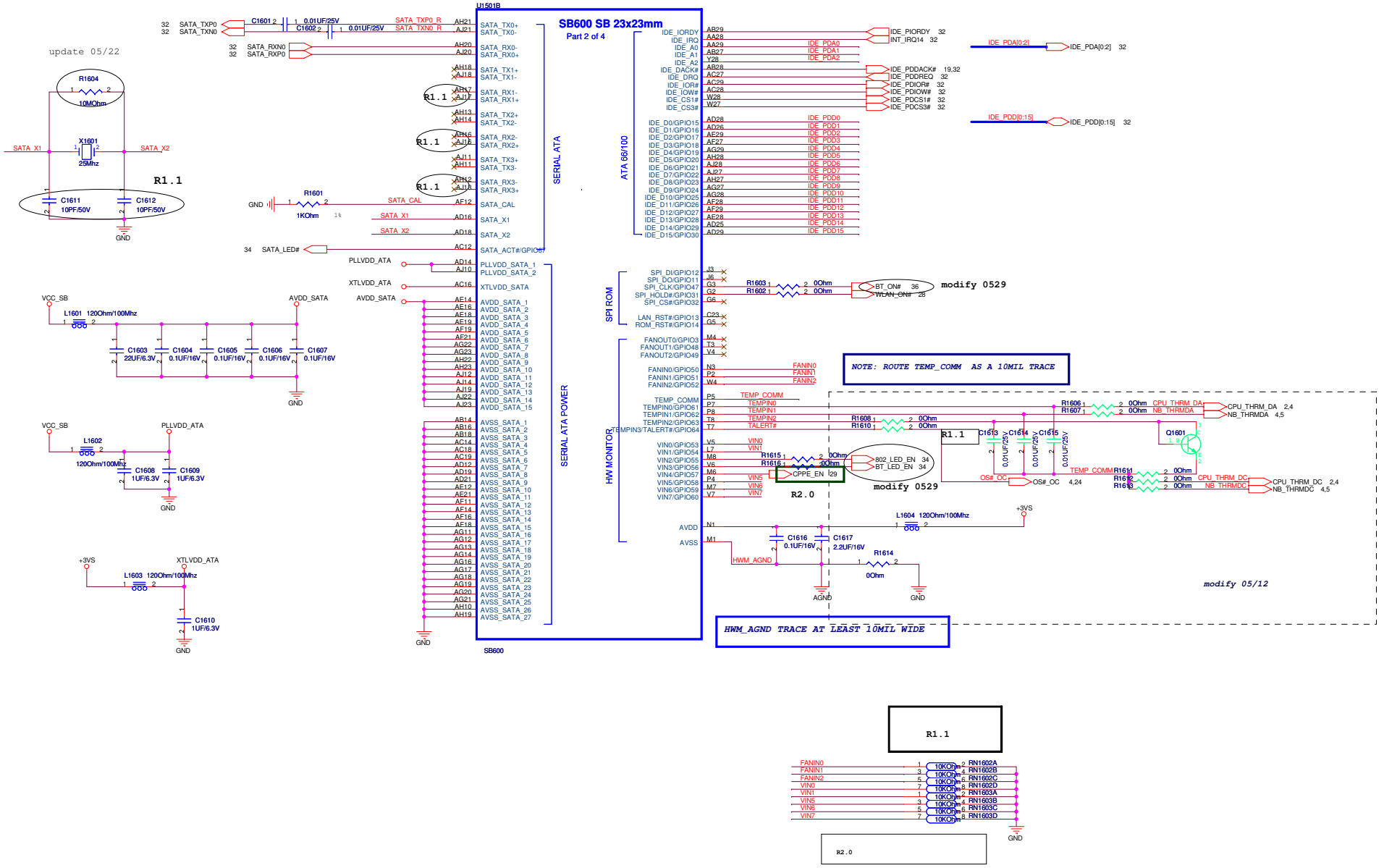
Date: 星期三, 十月 11, 2006 Sheet 14 of 71

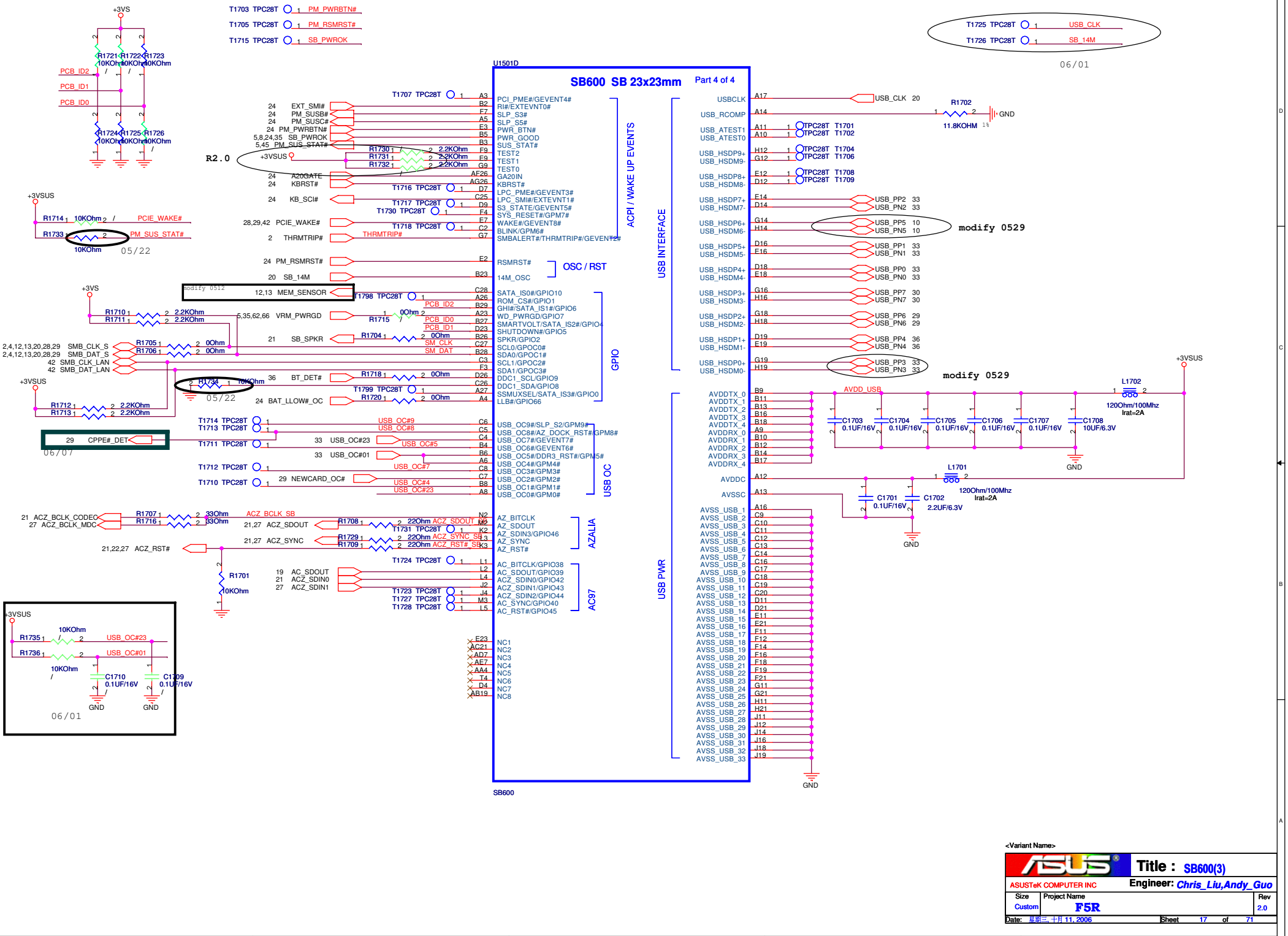
SB CALIBRATION RESISITOR VALUE

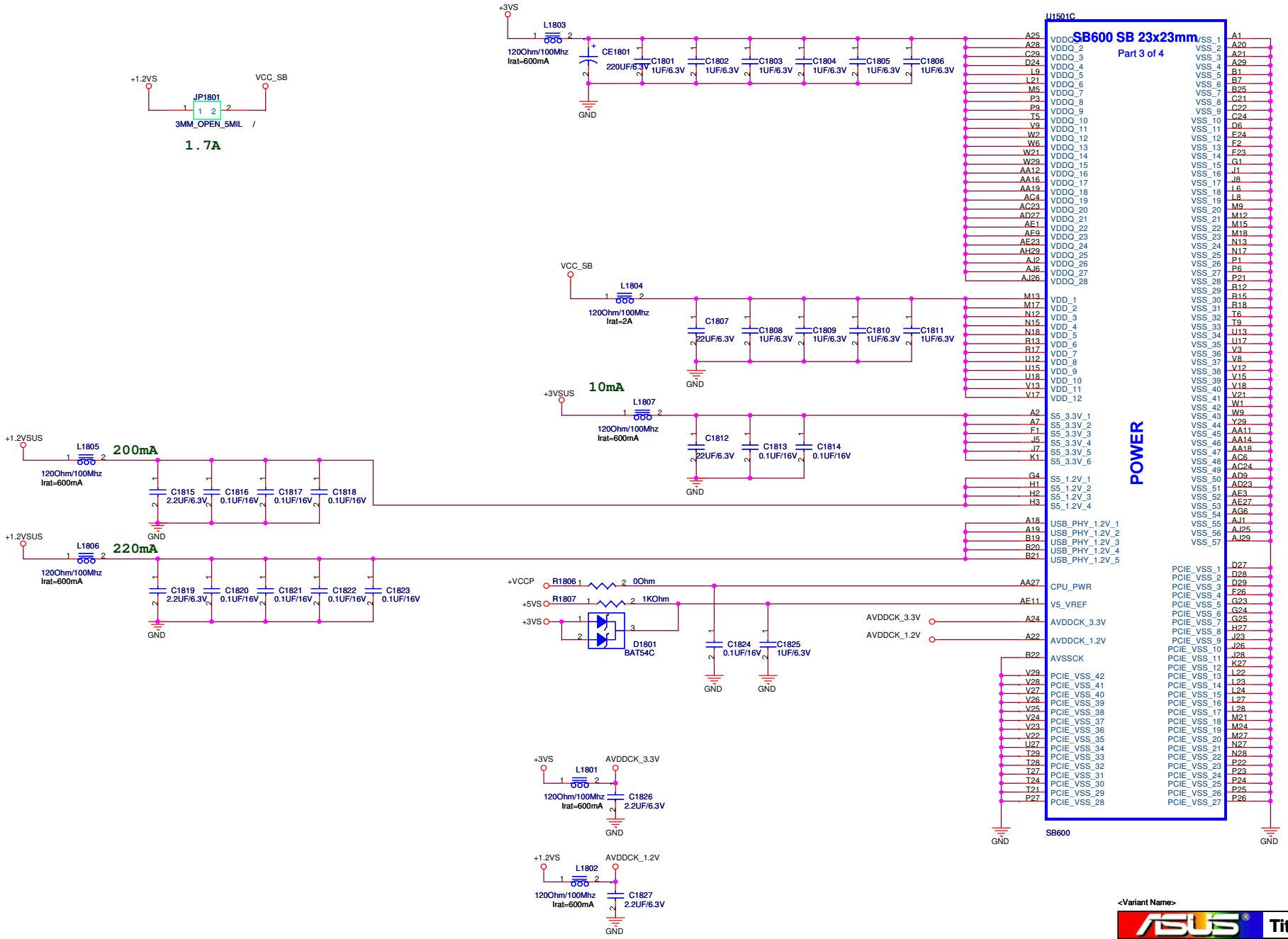
	SB600
R1501	562 OHM 1%
R1511	2.05K 1%
R1512	0 ohm



ASUSTeK COMPUTER INC	Title : SB600(1)		
	Engineer: Chris_Liu,Andy_Guo		
Size: Custom	Project Name: F5R		Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 15 of 71		


U1501B
SB600 SB 23x23mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SB600
update 05/22
R1.1
modify 0529
modify 05/12
NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE
HWM_AGND TRACE AT LEAST 10MIL WIDE
R2.0


SB600 SB 23x23mm
Part 4 of 4
U1501D
SB600
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
R2.0
modify 0529
modify 0512
05/22
06/07
06/01
T1703 TPC28T PM_PWRBTN#
T1705 TPC28T PM_RSMRST#
T1715 TPC28T SB_PWROK
T1725 TPC28T USB_CLK
T1726 TPC28T SB_14M
PCB_ID2
PCB_ID1
PCB_ID0
PCIE_WAKE#
PM_SUS_STAT#
SB_PWROK
EXT_SMI#
PM_SUSB#
PM_SUSC#
PM_PWRBTN#
SUS_STAT#
A20GATE
KBRST#
KB_SCI#
THRMTRIP#
PM_RSMRST#
SB_14M
MEM_SENSOR
VRM_PWRGD
SB_SPKR
BT_DET#
BAT_LLOW#_OC
CPPE#_DET
NEWCARD_OC#
SMB_CLK_S
SMB_DAT_S
SMB_CLK_LAN
SMB_DAT_LAN
ACZ_BCLK_CODEC
ACZ_BCLK_MDC
ACZ_BCLK_SB
ACZ_SDOUT
ACZ_SYNC
ACZ_RST#
AC_SDOUT
AC_SDIN0
AC_SDIN1
USB_OC#23
USB_OC#01
USB_OC#9
USB_OC#8
USB_OC#5
USB_OC#7
USB_OC#4
USB_OC#23
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN
KBRST#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
RSMRST#
14M_OSC
SATA_IS0#/GPIO10
ROM_CS#/GPIO1
GHI#/SATA_IS1#/GPIO6
WD_PWRGD/GPIO7
SMARTVOLT/SATA_IS2#/GPIO4
SHUTDOWN#/GPIO5
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
SSMUXSEL/SATA_IS3#/GPIO0
LLB#/GPIO66
USB_OC9#/SLP_S2/GPM9#
USB_OC8#/AZ_DOCK_RST#/GPM8#
USB_OC7#/GEVENT7#
USB_OC6#/GEVENT6#
USB_OC5#/DDR3_RST#/GPM5#
USB_OC4#/GPM4#
USB_OC3#/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AC_BITCLK/GPIO38
AC_SDOUT/GPIO39
ACZ_SDIN0/GPIO42
ACZ_SDIN1/GPIO43
ACZ_SDIN2/GPIO44
AC_SYNC/GPIO40
AC_RST#/GPIO45
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
USBCLK
USB_RCOMP
USB_ATEST1
USB_ATEST0
USB_HSDP9+
USB_HSDM9-
USB_HSDP8+
USB_HSDM8-
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
AVDDC
AVSSC
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
AVSS_USB_25
AVSS_USB_26
AVSS_USB_27
AVSS_USB_28
AVSS_USB_29
AVSS_USB_30
AVSS_USB_31
AVSS_USB_32
AVSS_USB_33
AVDD_USB
120Ohm/100Mhz Irat=2A
2.2UF/6.3V
10UF/6.3V
0.1UF/16V
11.8KOHM 1%
GND
+3VS
+3VSUS
<Variant Name>
Title : SB600(3)
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Size Custom
Project Name F5R
Rev 2.0
Date: 星期三, 十月 11, 2006
Sheet 17 of 71



<Variant Name>

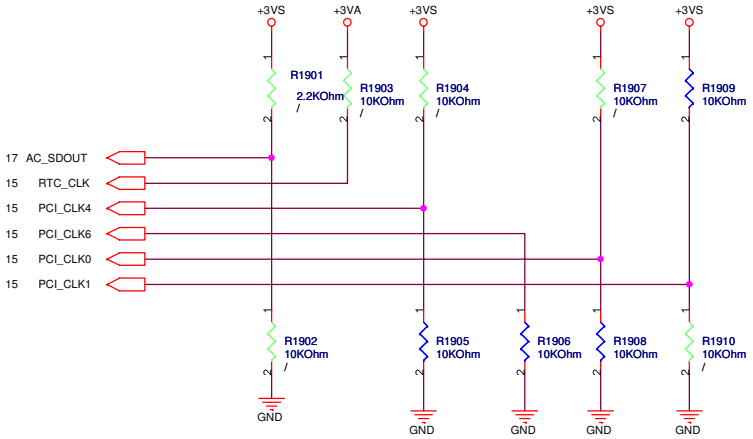
Title : SB600(PWR)

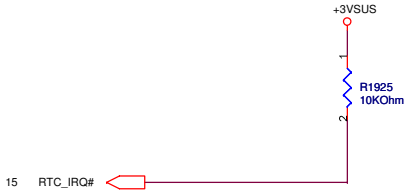
ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 18 of 71

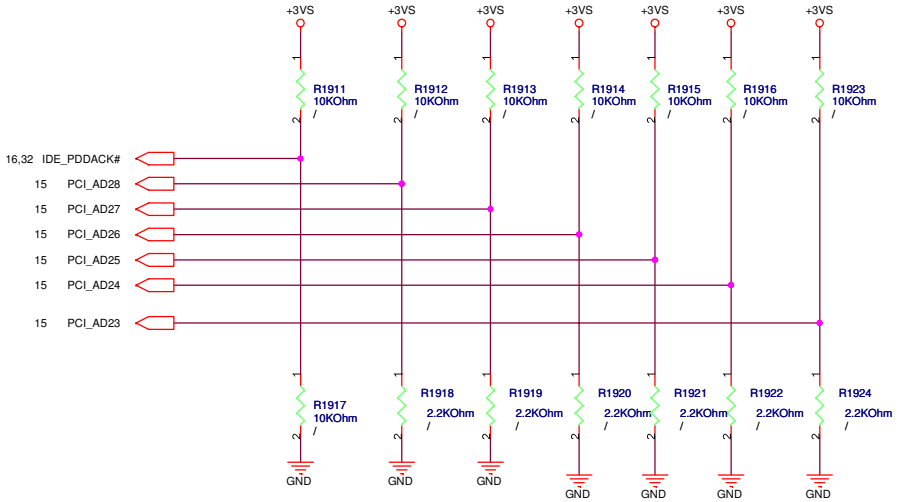




NOTE: R1925 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TOKEEP THE INPUT FROM FLOATING.

REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	SB600 PCI_CLK0 PCI_CLK1	SB460 PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM DEFAULT L, H = LPC II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT		



DEBUG STRAPS

	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED
	SB460 ONLY	SB600 ONLY					SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

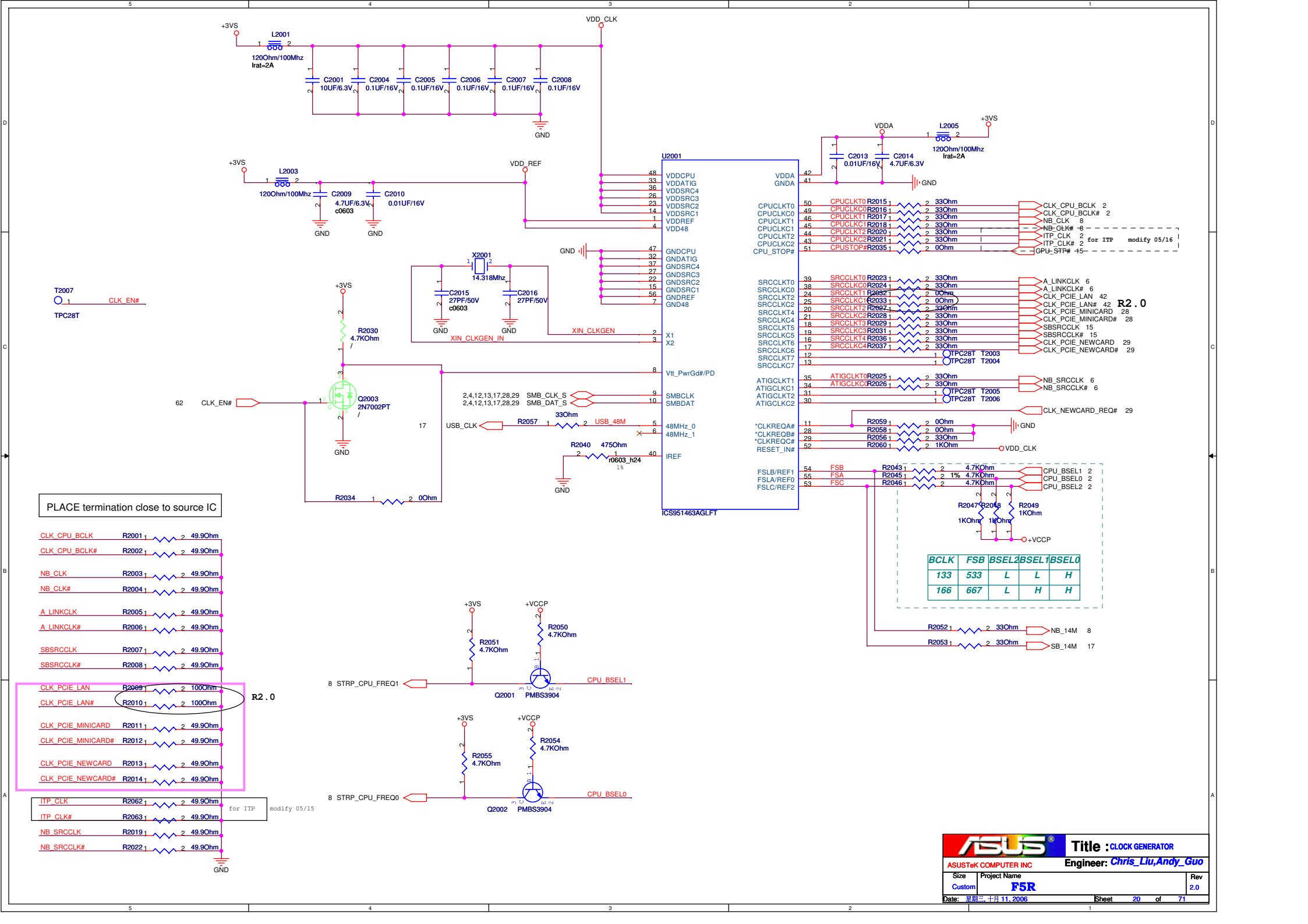
ASUSTeK COMPUTER INC

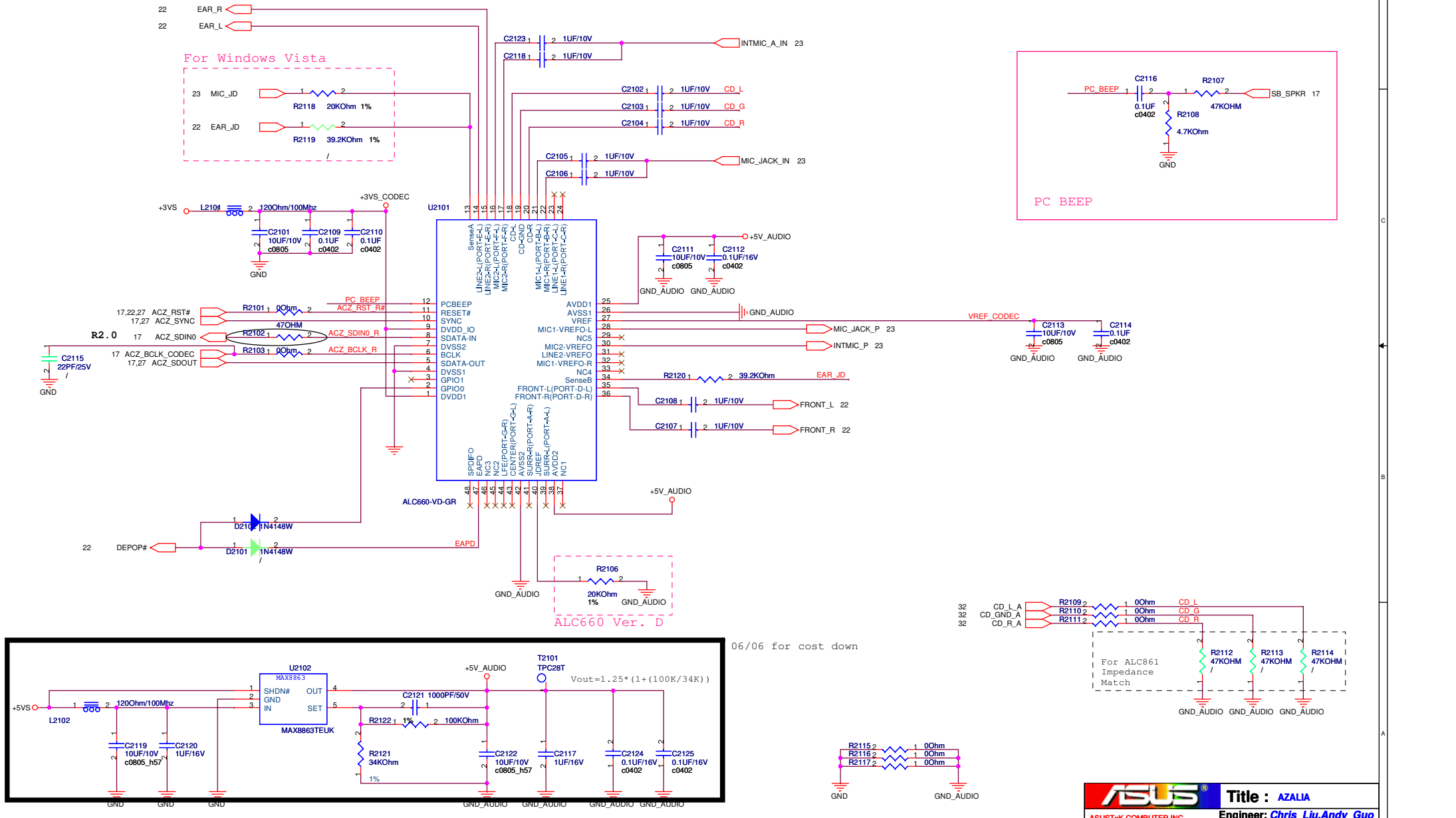
Title : SB600(5)

Engineer: <Enginner Name>

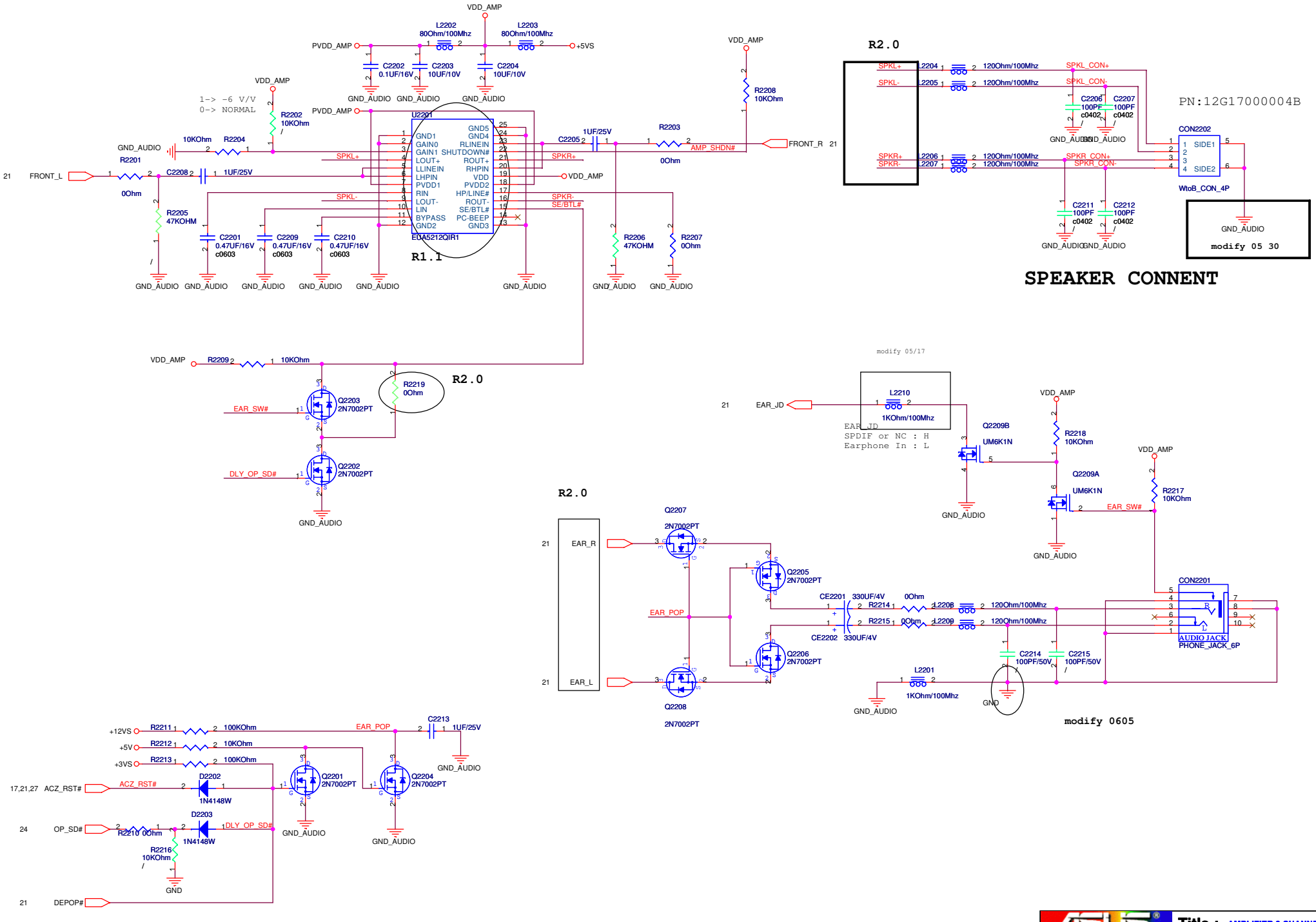
Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 19 of 71

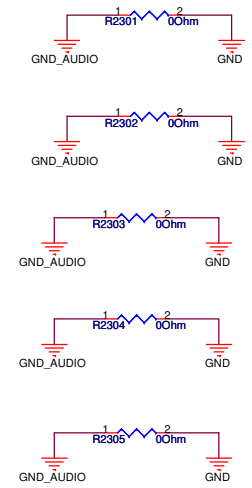

+3VS
L2001
120Ohm/100Mhz
Irat=2A
C2001 10UF/6.3V
C2004 0.1UF/16V
C2005 0.1UF/16V
C2006 0.1UF/16V
C2007 0.1UF/16V
C2008 0.1UF/16V
GND
VDD_CLK
+3VS
L2003
120Ohm/100Mhz
C2009 4.7UF/6.3V c0603
C2010 0.01UF/16V
GND
GND
VDD_REF
U2001
VDDCPU
VDDATIG
VDDSRC4
VDDSRC3
VDDSRC2
VDDSRC1
VDDREF
VDD48
GNDCPU
GNDATIG
GNDSRC4
GNDSRC3
GNDSRC2
GNDSRC1
GNDREF
GND48
X2001
14.318Mhz
C2015 27PF/50V c0603
C2016 27PF/50V
XIN_CLKGEN
XIN_CLKGEN_IN
X1
X2
Vtt_PwrGd#/PD
SMBCLK
SMBDAT
48MHz_0
48MHz_1
IREF
R2040 475Ohm r0603_h24 1%
ICS951463AGLFT
VDDA
GNDA
L2005
120Ohm/100Mhz
Irat=2A
C2013 0.01UF/16V
C2014 4.7UF/6.3V
CPUCLKT0
CPUCLKC0
CPUCLKT1
CPUCLKC1
CPUCLKT2
CPUCLKC2
CPU_STOP#
SRCCLKT0
SRCCLKC0
SRCCLKT1
SRCCLKC1
SRCCLKT2
SRCCLKC2
SRCCLKT4
SRCCLKC4
SRCCLKT3
SRCCLKC3
SRCCLKT5
SRCCLKC5
SRCCLKT6
SRCCLKC6
SRCCLKT7
SRCCLKC7
ATIGCLKT0
ATIGCLKC0
ATIGCLKT1
ATIGCLKC1
ATIGCLKT2
ATIGCLKC2
*CLKREQA#
*CLKREQB#
*CLKREQC#
RESET_IN#
FSLB/REF1
FSLA/REF0
FSLC/REF2
FSB
FSA
FSC
R2043 4.7KOhm
R2045 4.7KOhm
R2046 4.7KOhm
R2047 1KOhm
R2048 1KOhm
R2049 1KOhm
+VCCP
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
R2052 33Ohm
R2053 33Ohm
NB_14M
SB_14M
T2007
CLK_EN#
TPC28T
+3VS
R2030 4.7KOhm
Q2003 2N7002PT
62 CLK_EN#
17
USB_CLK
R2057 33Ohm
USB_48M
R2034 0Ohm
2,4,12,13,17,28,29 SMB_CLK_S
2,4,12,13,17,28,29 SMB_DAT_S
R2059 0Ohm
R2058 0Ohm
R2056 33Ohm
R2060 1KOhm
CLK_NEWCARD_REQ#
R2033 0Ohm
R2023 33Ohm
R2024 33Ohm
R2027 0Ohm
R2032 33Ohm
R2028 33Ohm
R2029 33Ohm
R2031 33Ohm
R2036 33Ohm
R2037 33Ohm
R2025 33Ohm
R2026 33Ohm
R2015 33Ohm
R2016 33Ohm
R2017 33Ohm
R2018 33Ohm
R2020 33Ohm
R2021 33Ohm
R2035 0Ohm
ITP_CLK 2 for ITP modify 05/16
GPU_STP# 15
R2.0
PLACE termination close to source IC
CLK_CPU_BCLK R2001 49.9Ohm
CLK_CPU_BCLK# R2002 49.9Ohm
NB_CLK R2003 49.9Ohm
NB_CLK# R2004 49.9Ohm
A_LINKCLK R2005 49.9Ohm
A_LINKCLK# R2006 49.9Ohm
SBSRCCLK R2007 49.9Ohm
SBSRCCLK# R2008 49.9Ohm
CLK_PCIE_LAN R2009 100Ohm
CLK_PCIE_LAN# R2010 100Ohm
CLK_PCIE_MINICARD R2011 49.9Ohm
CLK_PCIE_MINICARD# R2012 49.9Ohm
CLK_PCIE_NEWCARD R2013 49.9Ohm
CLK_PCIE_NEWCARD# R2014 49.9Ohm
ITP_CLK R2062 49.9Ohm
ITP_CLK# R2063 49.9Ohm
for ITP modify 05/15
NB_SRCCLK R2019 49.9Ohm
NB_SRCCLK# R2022 49.9Ohm
R2.0
8 STRP_CPU_FREQ1
R2051 4.7KOhm
R2050 4.7KOhm
Q2001 PMBS3904
CPU_BSEL1
8 STRP_CPU_FREQ0
R2055 4.7KOhm
R2054 4.7KOhm
Q2002 PMBS3904
CPU_BSEL0
CLK_CPU_BCLK 2
CLK_CPU_BCLK# 2
NB_CLK 8
NB_CLK# 8
ITP_CLK 2
ITP_CLK# 2
A_LINKCLK 6
A_LINKCLK# 6
CLK_PCIE_LAN 42
CLK_PCIE_LAN# 42
CLK_PCIE_MINICARD 28
CLK_PCIE_MINICARD# 28
SBSRCCLK 15
SBSRCCLK# 15
CLK_PCIE_NEWCARD 29
CLK_PCIE_NEWCARD# 29
NB_SRCCLK 6
NB_SRCCLK# 6
CPU_BSEL1 2
CPU_BSEL0 2
CPU_BSEL2 2
Title : CLOCK GENERATOR
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Size Custom
Project Name F5R
Rev 2.0
Date: 星期三, 十月 11, 2006
Sheet 20 of 71



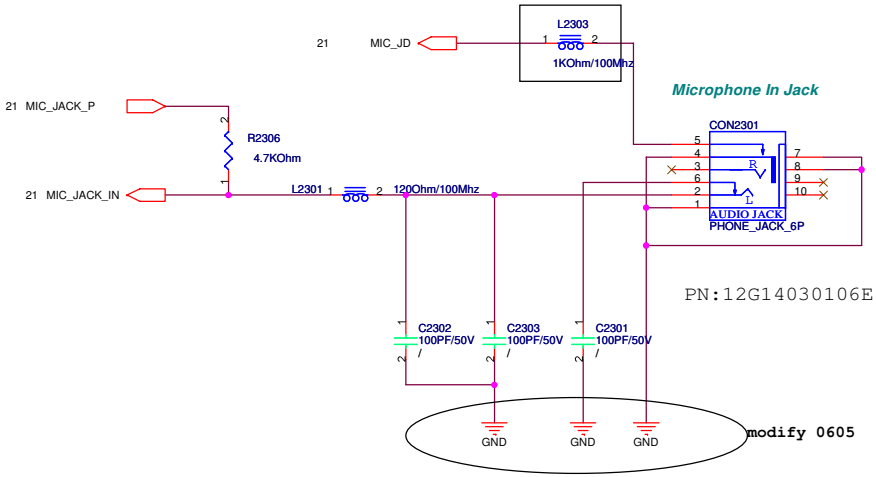
Title :	AZALIA
ASUSTeK COMPUTER INC	Engineer: Chris_Liu,Andy_Guo
Size: Custom	Project Name: F5R
Rev: 2.0	
Date: 星期三, 十月 11, 2006	Sheet 21 of 71



ASUSTeK COMPUTER INC	Title : AMPLIFIER 2 CHANNEL		
	Engineer: Chris_Liu,Andy_Guo		
Size: Custom	Project Name: F5R		Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 22 of 71		

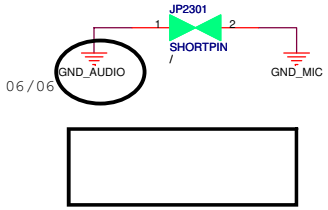


modify 05/17



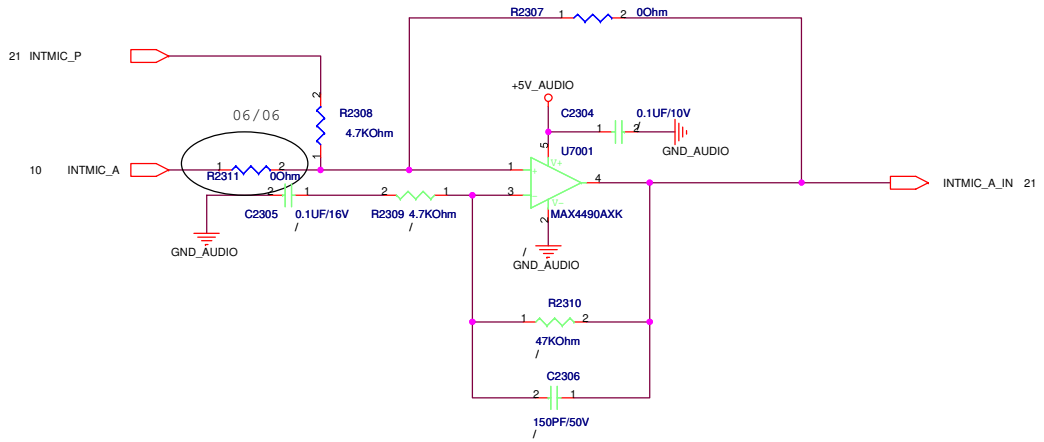
PN:12G14030106E

INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



modify 0605

Pre-AMP For Test Function



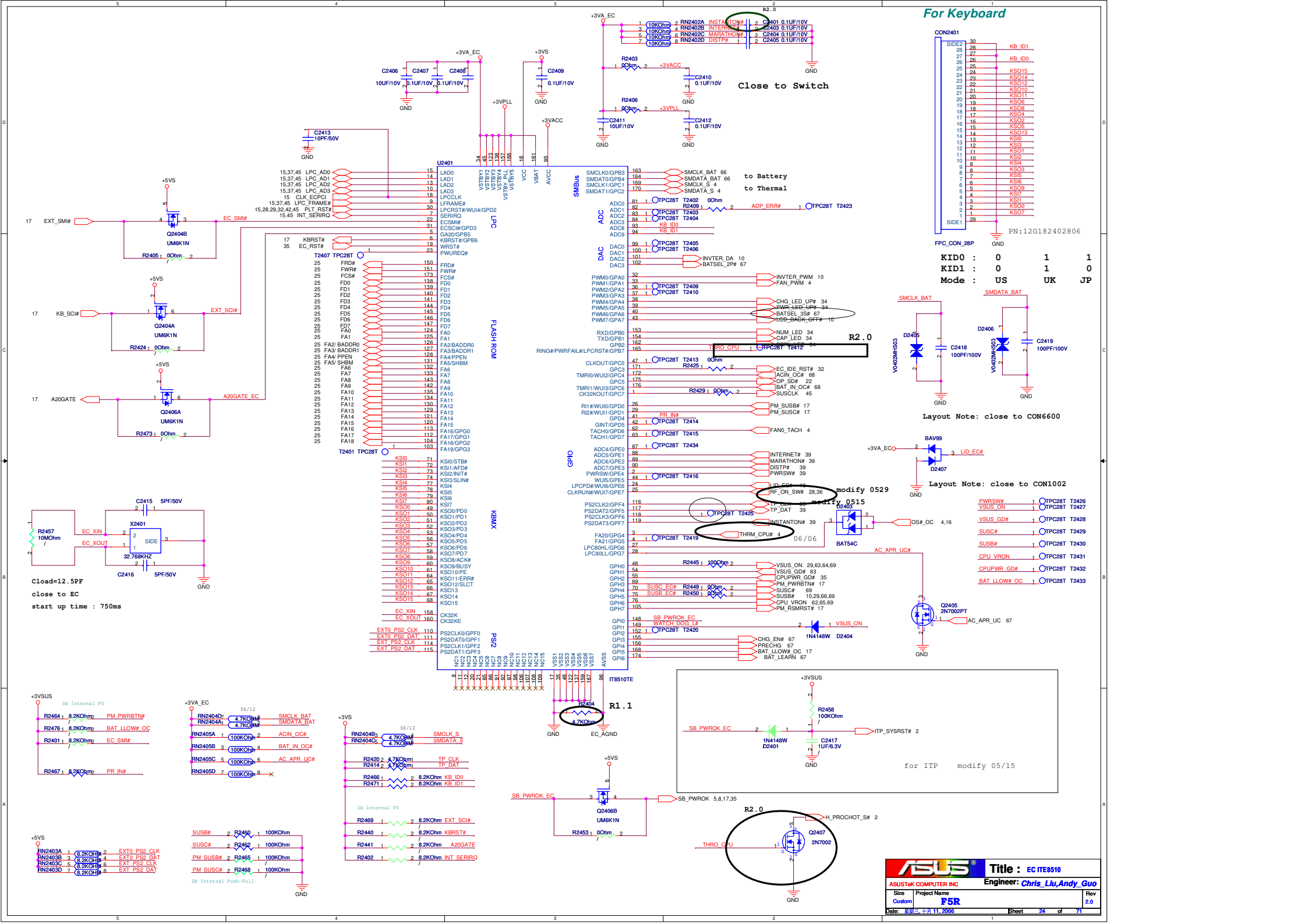
ASUSTeK COMPUTER INC

Title : MIC JACK

Engineer: *Chris_Liu,Andy_Guo*

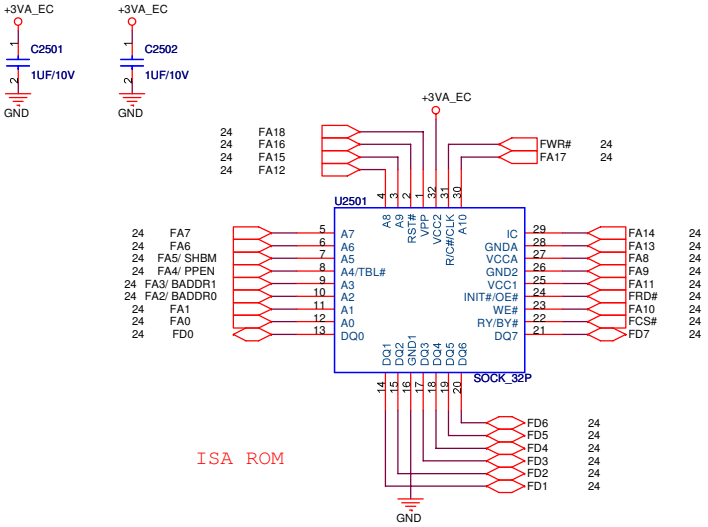
Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 23 of 71


For Keyboard
Close to Switch
to Battery
to Thermal
R2.0
modify 0529
modify 0515
06/06
Layout Note: close to CON6600
Layout Note: close to CON1002
Cload=12.5PF
close to EC
start up time : 750ms
R1.1
for ITP modify 05/15
KID0 : 0 1 1
KID1 : 0 1 0
Mode : US UK JP
PN:12G182402806
Title : EC ITE8510
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Project Name F5R
Rev 2.0
Sheet 24 of 71

EC Hardware Strapping

PLCC32 Socket **SST-PLCC32 4Mbits Flash ROM**
PN:12G04300032F **PN:05G001027221**



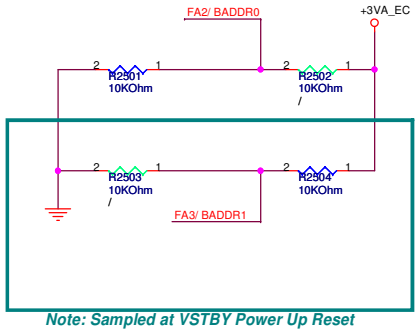
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

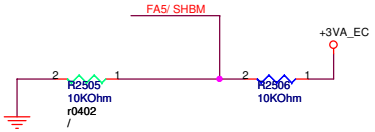


Note: Sampled at VSTBY Power Up Reset

FA5/ SHBM

0: Disable Shared Memory with Host BIOS

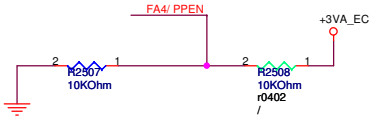
1: Enable Shared Memory with Host BIOS



FA4/ PPEN

0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 25 of 71	

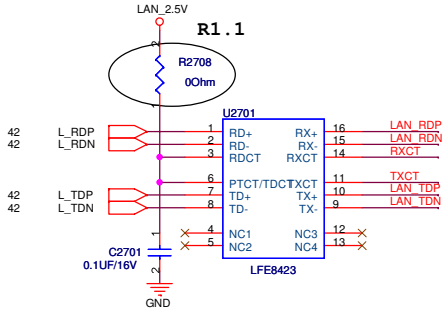
Title : *

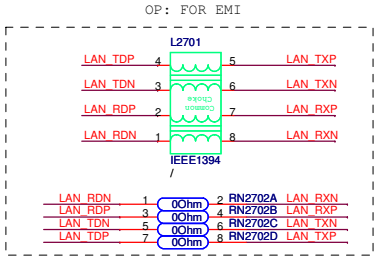
ASUSTeK COMPUTER INC

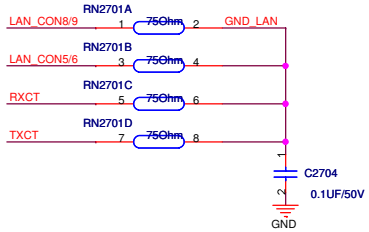
Engineer: Chris_Liu,Andy_Guo

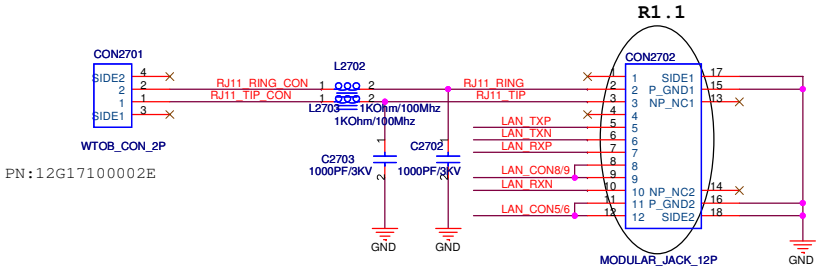
Size	Project Name	Rev
Custom	F5R	2.0

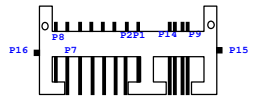
Date: 星期三, 十月 11, 2006 Sheet 26 of 71







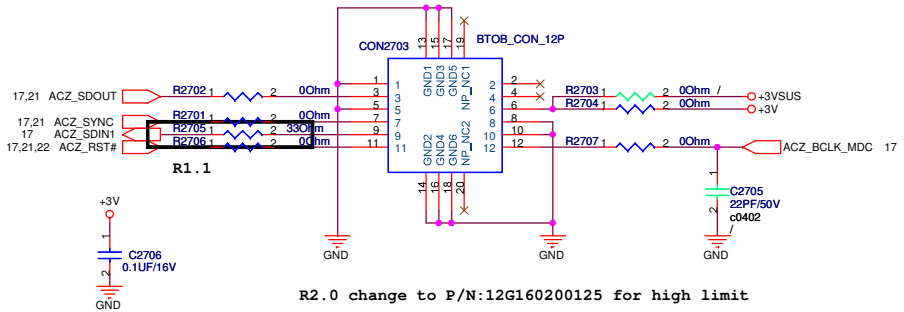




LAN PORT

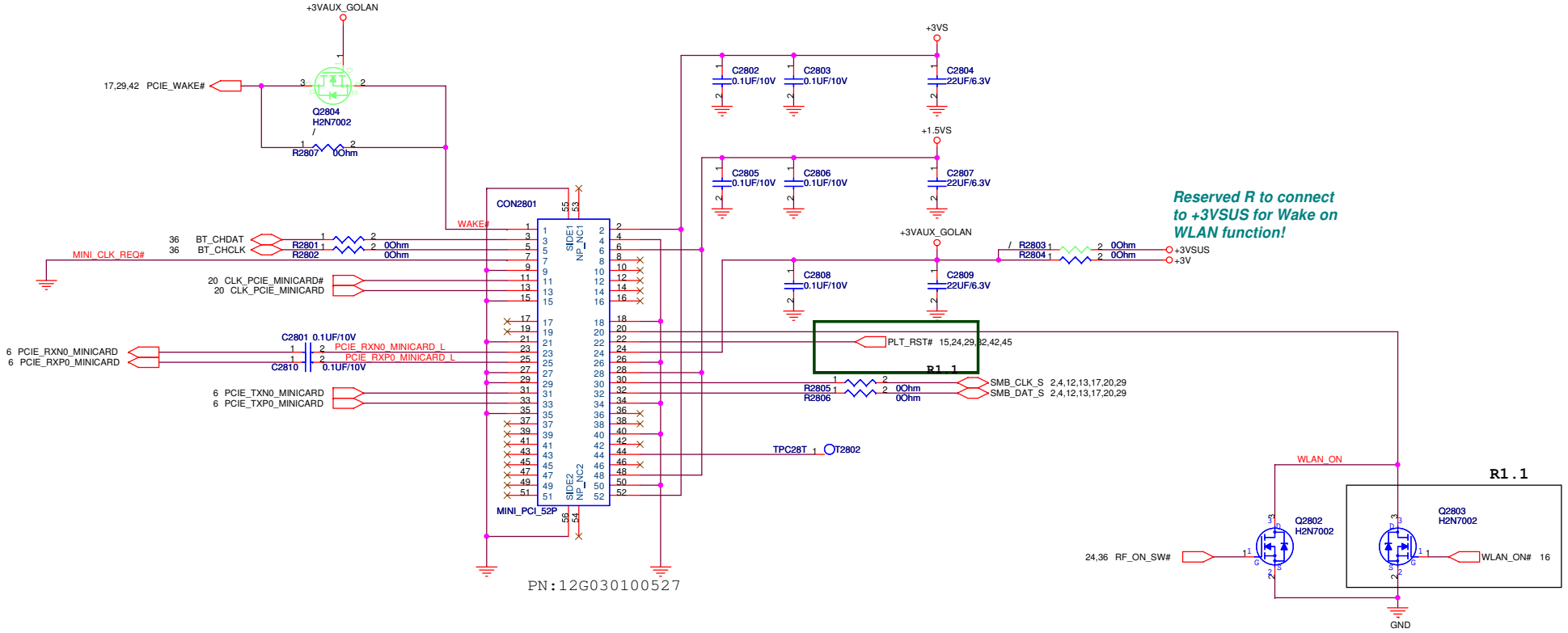
MDC

MDC



R2.0 change to P/N:12G160200125 for high limit

ASUSTeK COMPUTER INC	Title : RJ11+45 & MDC		
	Engineer: Chris_Liu,Andy_Guo		
Size: Custom	Project Name: F5R		Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 27 of 71		



PN:12G030100527

<Variant Name>

ASUSTeK COMPUTER INC	Title : MINICARD	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 28 of 71	

FOR SWAP

modify 0607

17 USB_PP6 — L2901 90Ohm/100Mhz — USB_P6+

17 USB_PN6 — USB_P6-

D2902 RSB6.8S / D2903 RSB6.8S /

06/07

SB600 GPO57

16 CPPE_EN — R2902 0Ohm — 10,24,66,69 SUSB#

SB600 GPM8

17 CPPE#_DET — D2904 1N4148W — CPUSB#

D2905 1N4148W

24,63,64,69 VSUS_ON — D2901 1N4148W — 0Ohm R2905 — NEWCARS_RST

06/06

U2901 R5538D001

STBY# SHDN# PERST# — OC# 1.5VOUT_1 1.5VOUT_2 — NEWCARD_OC# 17, +1.5VS_PE

3.3VIN_1 3.3VIN_2 — AUXOUT — +3VSUS_PE

1.5VIN_1 1.5VIN_2 — 3.3VOUT_1 3.3VOUT_2 — +3VS_PE

AUXIN — CPPE# CPUSB# RCLKEN — CPUSB# REFCLK_EN

SYSRST# GND1 GND2 — NC

+1.5VS +3VSUS +3VS

15,24,28,32,42,45 PLT_RST#

R1.1

!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

CON2901 EXPRESS_CARD_26P

USB_P6- USB_P6+ CPUSB#

GND1 USB_D- USB_D+ CPUSB# RESERVED1 RESERVED2 SMBCLK SMBDATA +1.5V_1 +1.5V_2 WAKE# +3.3VAUX PERST# +3.3V_1 +3.3V_2 CLKREQ# CPPE# REFCLK- REFCLK+ GND2 PERn0 PERp0 GND3 PETn0 PETp0 GND4 — GND5 NP_NC1 NP_NC2 GND6

2,4,12,13,17,20,28 SMB_CLK_S

2,4,12,13,17,20,28 SMB_DAT_S

+1.5VS_PE PCIE_WAKE# C +3VSUS_PE PERST# +3VS_PE

NEWCARS_RST — R2901 0Ohm

20 CLK_PCIE_NEWCARD#

20 CLK_PCIE_NEWCARD

6 PCIE_RXN1_NEWCARD — C2902 0.1UF/10V — PCIE_RXN1_NEWCARD_L

6 PCIE_RXP1_NEWCARD — C2903 0.1UF/10V — PCIE_RXP1_NEWCARD_L

6 PCIE_TXN1_NEWCARD

6 PCIE_TXP1_NEWCARD

PN:12G161300261

06/07

CLK_NEWCARD_REQ# 20

REFCLK_EN — Q2901 2N7002

+3VSUS_PE — R2904 10KOhm

17,28,42 PCIE_WAKE# — Q2902 H2N7002 — PCIE_WAKE# C

R2903 0Ohm

U2902 CARD_EJECTOR_2P

P_GND1 P_GND2

PN:12G21C102604

+3VSUS: C2901 2.2UF/6.3V, C2904 0.1UF/10V

+3VS: C2905 4.7UF/10V, C2906 0.1UF/10V

+1.5VS: C2907 2.2UF/6.3V, C2908 0.1UF/10V

+3VSUS_PE: C2909 10UF/10V, C2910 0.01UF/16V

+3VS_PE: C2911 10UF/10V, C2912 10UF/10V, C2913 0.01UF/16V

+1.5VS_PE: C2914 10UF/10V, C2915 0.01UF/16V

<Variant Name>

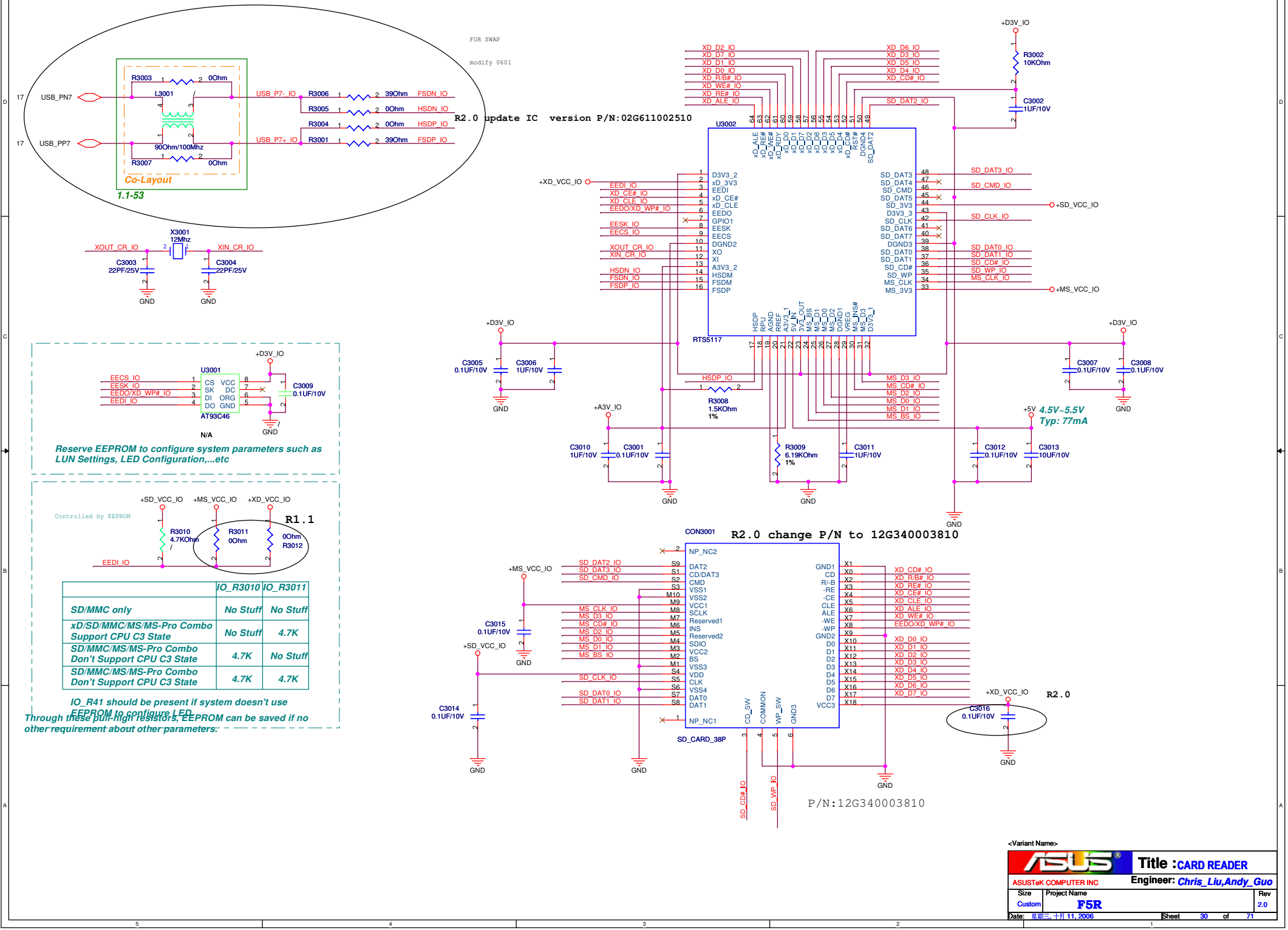
ASUSTeK COMPUTER INC

Title : NEWCARD

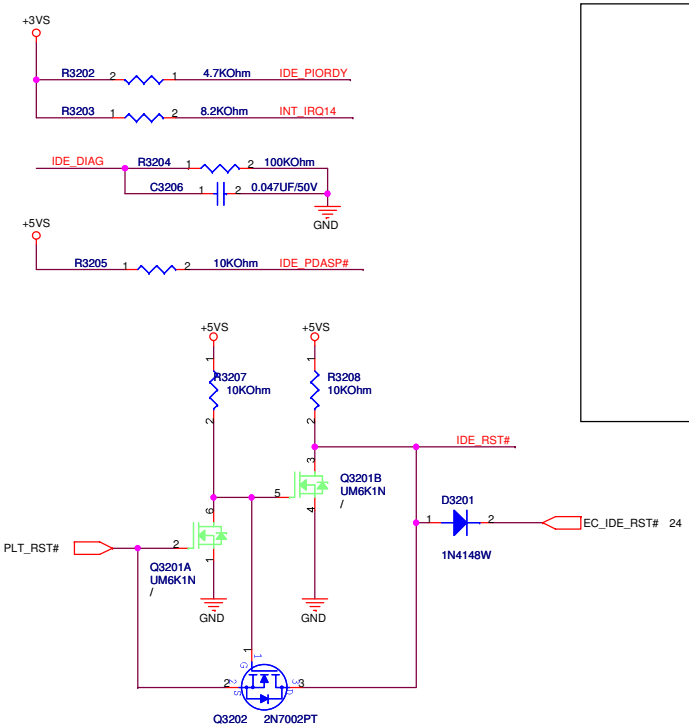
Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

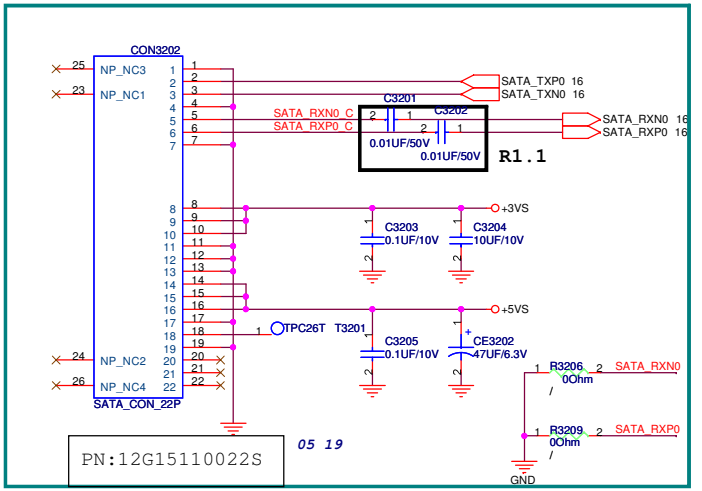
Date: 星期三, 十月 11, 2006 Sheet 29 of 71



	IO_R3010	IO_R3011
SD/MMC only	No Stuff	No Stuff
xD/SD/MMC/MS/MS-Pro Combo Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	No Stuff
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	4.7K



modify 0512

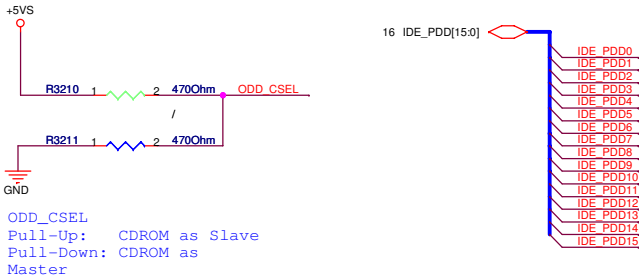


Dafult

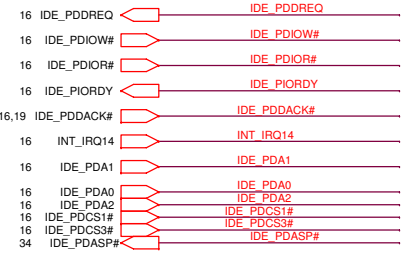
PATA

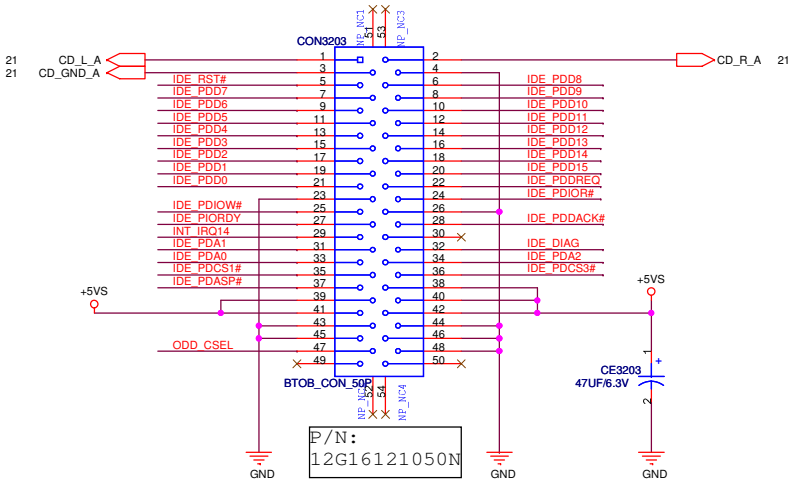
SATA

CD-ROM



ODD_CSEL
Pull-Up: CDROM as Slave
Pull-Down: CDROM as Master





update 05 18

<Variant Name>

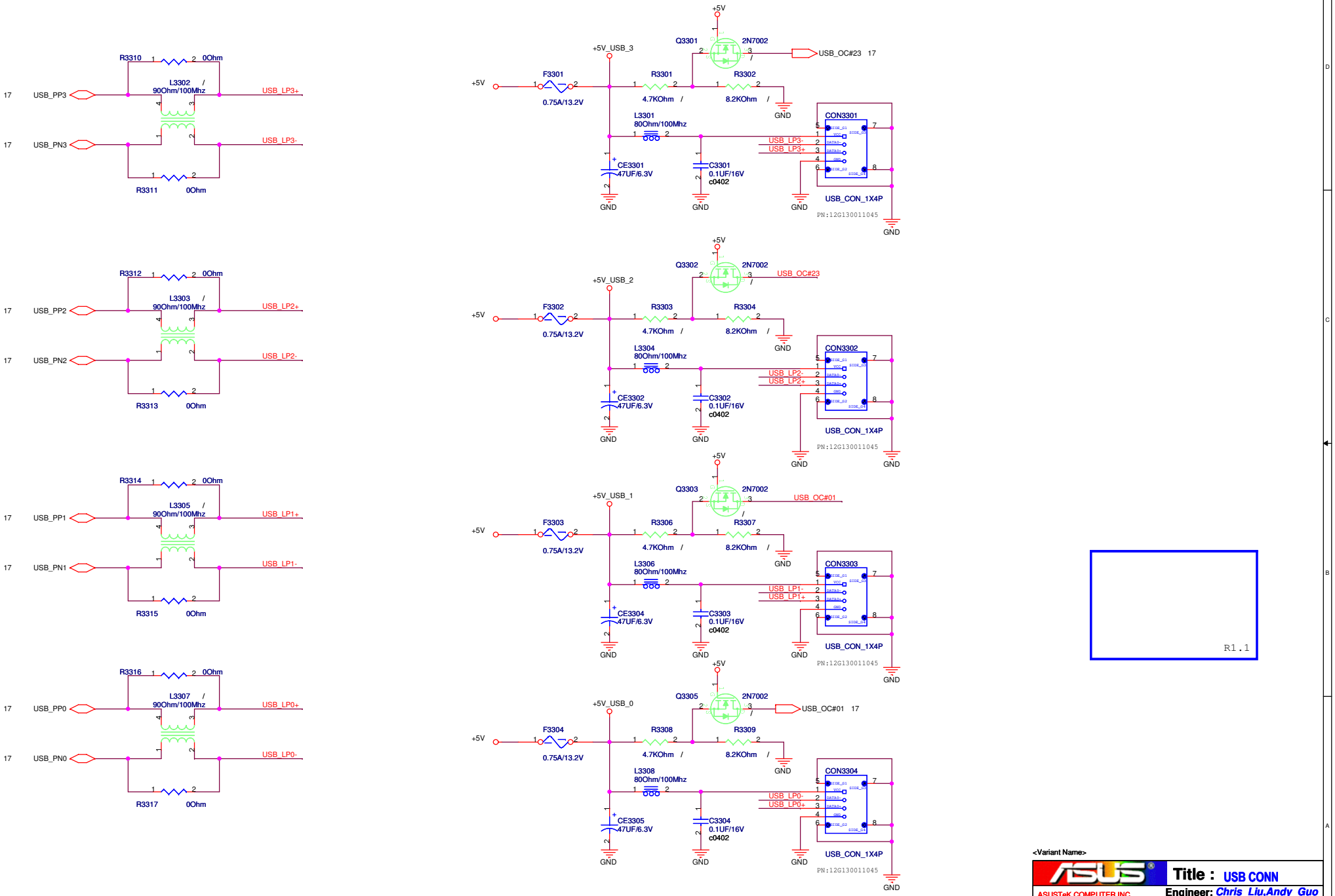
ASUSTeK COMPUTER INC

Title : HDD & CD-ROM

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 32 of 71



<Variant Name>

ASUSTeK COMPUTER INC

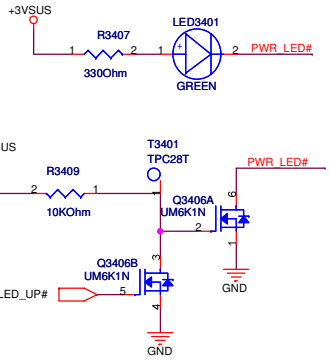
Title : USB CONN

Engineer: Chris_Liu,Andy_Guo

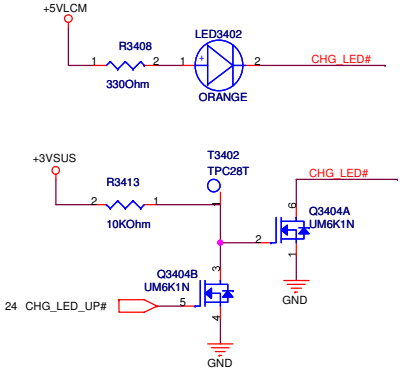
Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 33 of 71

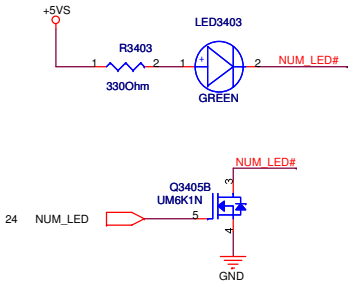
For POWER LED



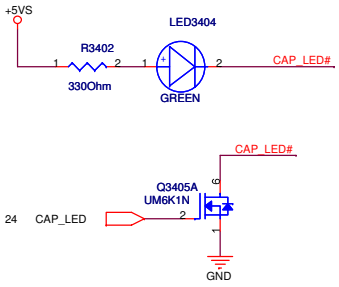
BATTERY LED



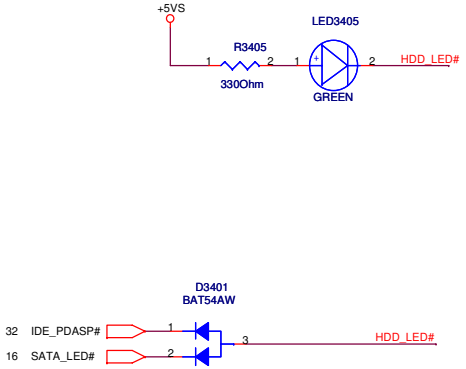
Num Lock



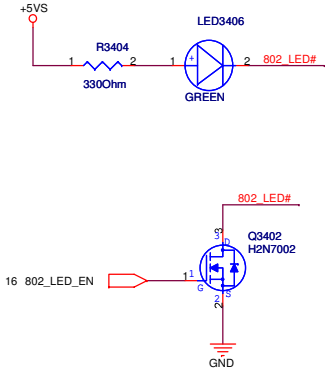
Cap Lock



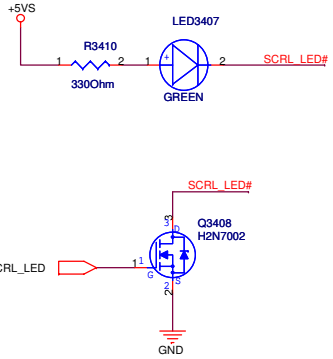
SATA/IDE LED



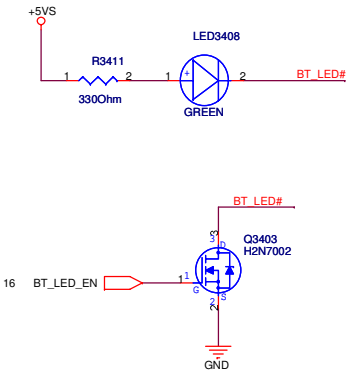
WireLess LED



Scroll Lock



BT LED



<Variant Name>

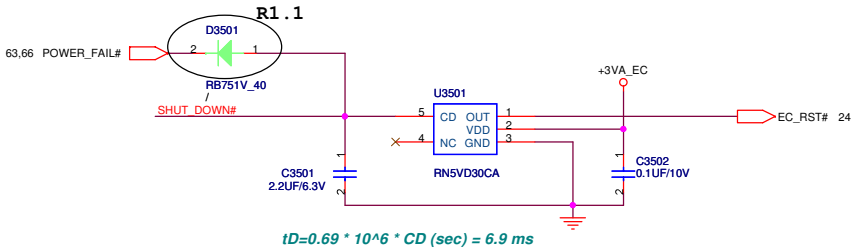
ASUSTeK COMPUTER INC

Title : LED

Engineer: Chris_Liu,Andy_Guo

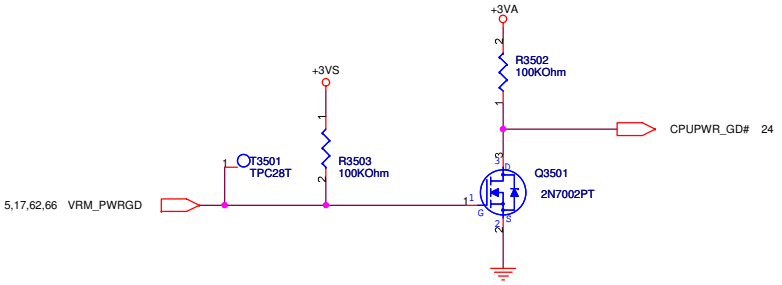
Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 34 of 71

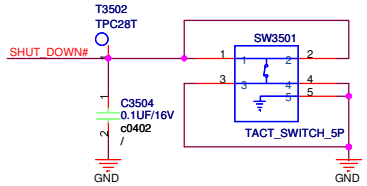


*tD=0.69 * 10^6 * CD (sec) = 6.9 ms*

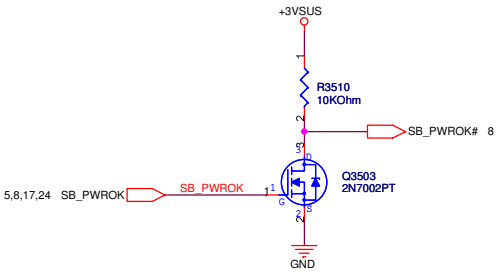
tD=0.69*10^6*CD pin sec Change threshold = 2.9V



RESET SW.



P/N: 12G091030050



<Variant Name>

ASUSTeK COMPUTER INC

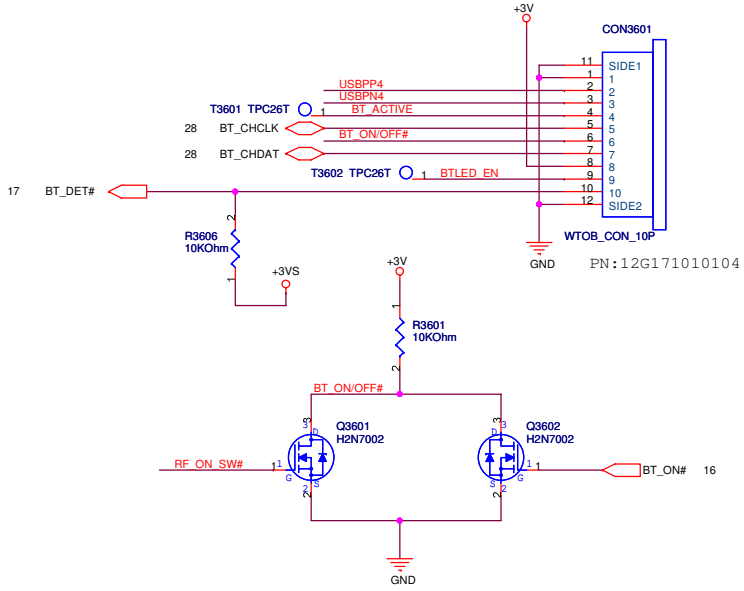
Title : RST

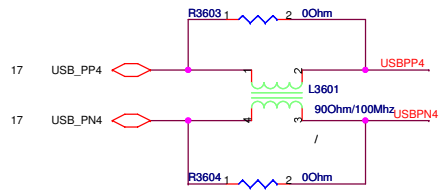
Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

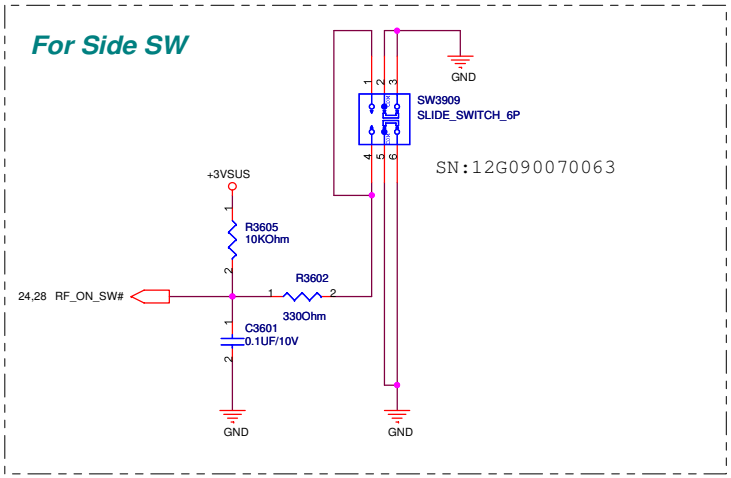
Date: 星期三, 十月 11, 2006 Sheet 35 of 71

For Bluetooth



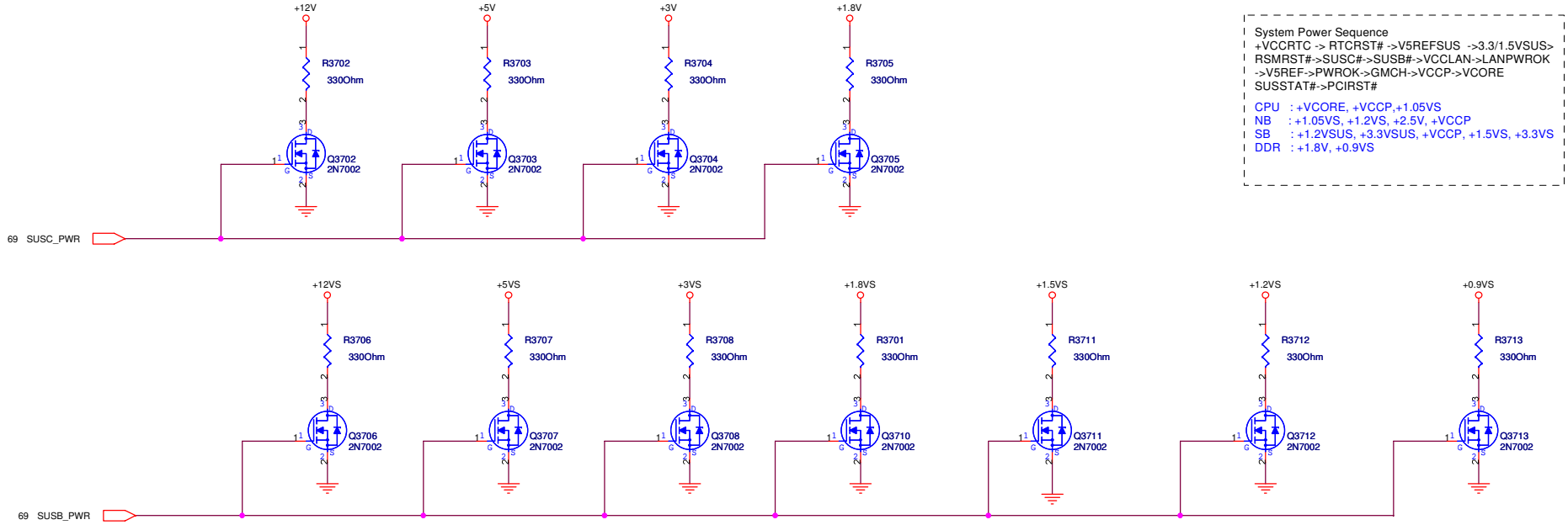


For Side SW



<Variant Name>

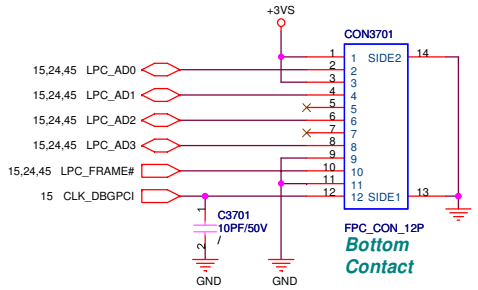
ASUSTeK COMPUTER INC	Title : BlueTooth	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 36 of 71	



System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#

CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.2VS, +2.5V, +VCCP
SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS

Debug Port



<Variant Name>

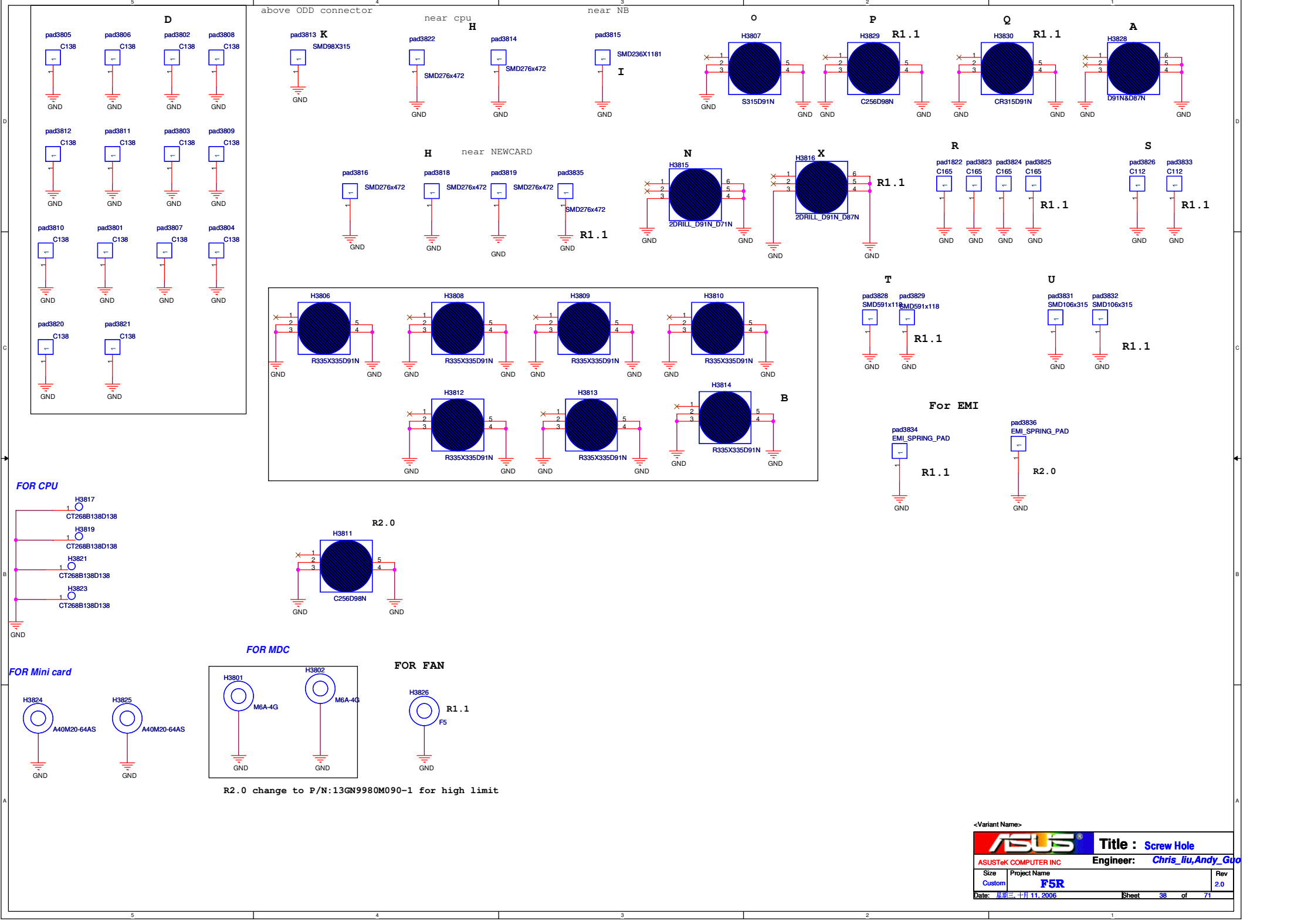
Title : DISCHARGE CKT

ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 37 of 71



<Variant Name>

ASUSTeK COMPUTER INC

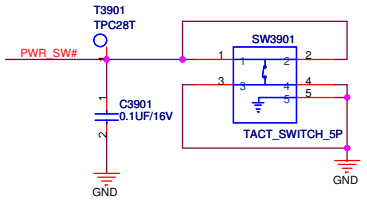
Title : Screw Hole

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

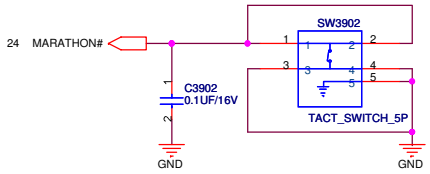
Date: 星期三, 十月 11, 2006 Sheet 38 of 71

Power SW.

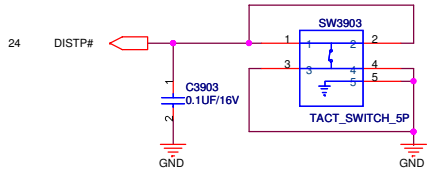


P/N: 12G091030050

Marathon SW.

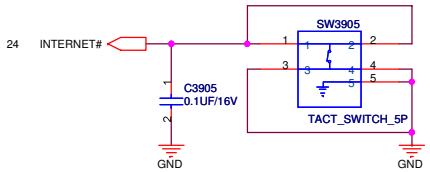


Disable Touch Pad SW.

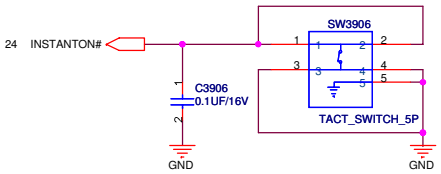


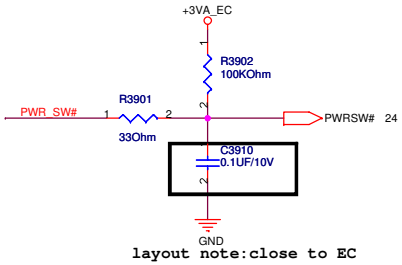
Internet SW.

modify 05/17



IstantON SW.

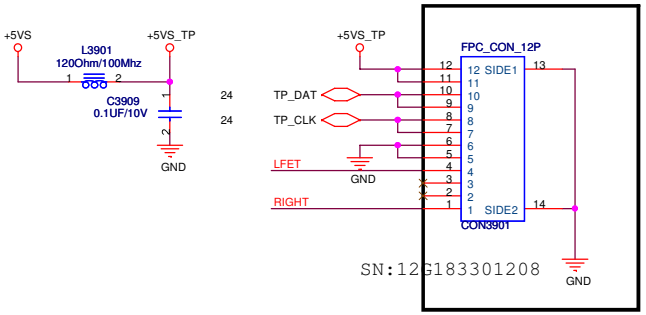


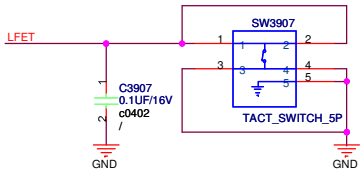


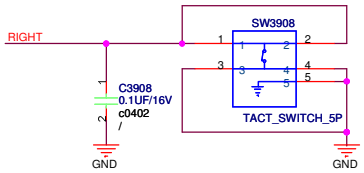
layout note:close to EC

Touch-Pad

R1.1

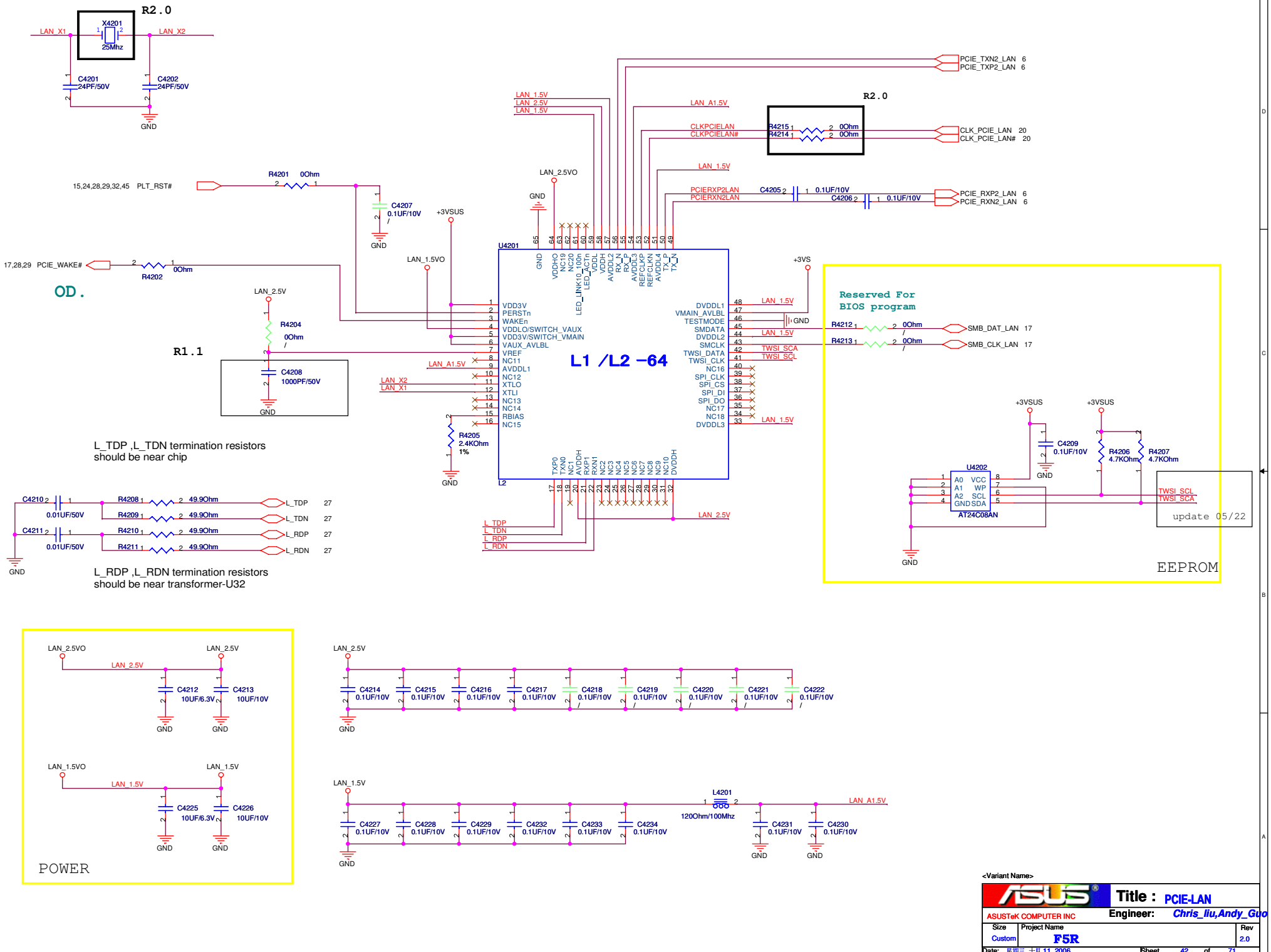






<Variant Name>

ASUSTeK COMPUTER INC	Title : SWITCH & TP	
	Engineer: Chris_liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 39 of 71	



<Variant Name>

ASUSTeK COMPUTER INC

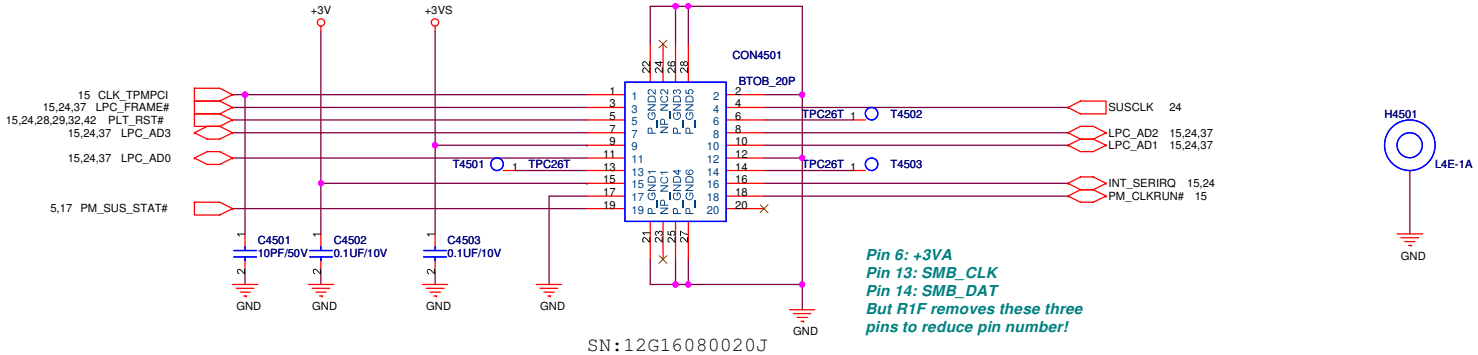
Title : PCIE-LAN

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	2.0

Date: 星期三, 十月 11, 2006 Sheet 42 of 71

For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

SN:12G16080020J

<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Chris_liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 45 of 71	

change list:

06-05-12

1. page16, add another thermal sensor schematic according to ATI demo schematic.
2.page32. delete PATA HDD connector according to ME request
3. page 12.13.17.add mem_sensor according to ATI demo schematic

06-05-15

1.Add the ITP function on page 2,20,24.
2.Page 24 delete the PWRLIMIT# net (power part has delete the power limit function)

06-05-16

1.connect BATSEL_3S# to EC pin 40

05-06-17

1.pag39 delete sw3904 according to markeeting spec
2. page 22 add L2210 for layout request
3.add L2303 for layout request

06-05-18

1.page 32 update ODD connector CON3203 P/N
2.PAGE 29 modify NEWCARD connector U2902 P/N

06-05-19

1.page 32 update SATA connector CON3202 P/N

06-05-22

1. page 5 change R510 to D501 according to F5X
2.page5 ADD R513 according to F5X
3.page 8 Remove L809,C811 according to ATI demo schematic
4. page10 mount L1011,unmount L1015 due to using the D/A inverter
5. page 15 remove R1524 due to SB600 (for Yonah)do not support H_PROCHOT
6. page 16 mount R1604 according to ATI suggestion
7.Page 17 add R1733,R1733 according to ATI suggestion
8.Page 30mount U3001,C3009 according to F5X
9.Page 38 add screw hole and pad
10.Page 42 exchange TWSI_SCA and TWSI_SCL

06-05-23

1.Page27 Add R2708 pull up resistor for Attansic request
2.Page27 change C2702,C2703 to close to CON2702

06-05-24

1.page12 modify CON1201 P/N

06-05-25

1.Page38 add H3826 for lock fan
2. delete some screw hole and add pad3820,pad3821

06-05-26

1.page 38 add screw hole H3815 H3816

06-05-29

1.page 17 exchange net USB_PP5 and USB_PP3,exchange net USB_PN5 and USB_PN3
2.page 24 connect RF_ON_SW# to EC pin 25
3.page16 connect net BT_ON# to SB600 GPIO47
4.page 16connect net 802_LED_EN to GPIO55
5.page 16 connect net BT_LED_EN to GPIO56

06-05-30

1.page 22 connect con2202 pin 5,pin6 to GND_AUDIO

06-06-01

1.Page 29 swap USB_PP6 and USB_PN6
2.Page 30 swap USB_PP7 and USB_PN7
3.Page 17 add pull up resistor R1735 and R1736,decoupling capacitor C1709 and C1710 on the USB_OC#01,USB_OC#23
4.Page17 add test point T1725,T1726
5.Page8 add test point T813

06-06-05

1.page38 change H3807 P/N
2.page22 delete net GND JACK
3.page23 delete net GND JACK and JP2302

06-06-06

Page 5 Add resistor R514 accordintg to Frank's suggestion
Page 8 Add resistor R828 accordintg to Frank's suggestion
Page 23 Add resistor R2311 for EMI request
Page 23 change GND to GND_AUDIO for EMI request
Page 3 Add C330 and C331 for EMI suggestion
Page 65 connect PR6507 pin 2 to +12VS
Page 24 delete Q2407 for repeat
Page 29 Add R2905,unmout d2901 for cost down
Page 21 change U2102 for cost down
Page 20 change U2001 for thermal request

06-06-07

Page 29 Modify the CON2901 schematic
Page 14 delete RN1405,CN1405
Page 16 connect VIN4 to R2902 for newcard shut down
Page 17 connect USB_OC#8 to D2904,D2905 FOR NEW CARD DETECT
Page 29 ADD R2902, D2904,D2905
page 38 change pad3819 connect to GND for EMI request
Page 29 swap USB_PP6 and USB_PN6

06-08

page4 change CE401 P/N for hight limit

R1.1

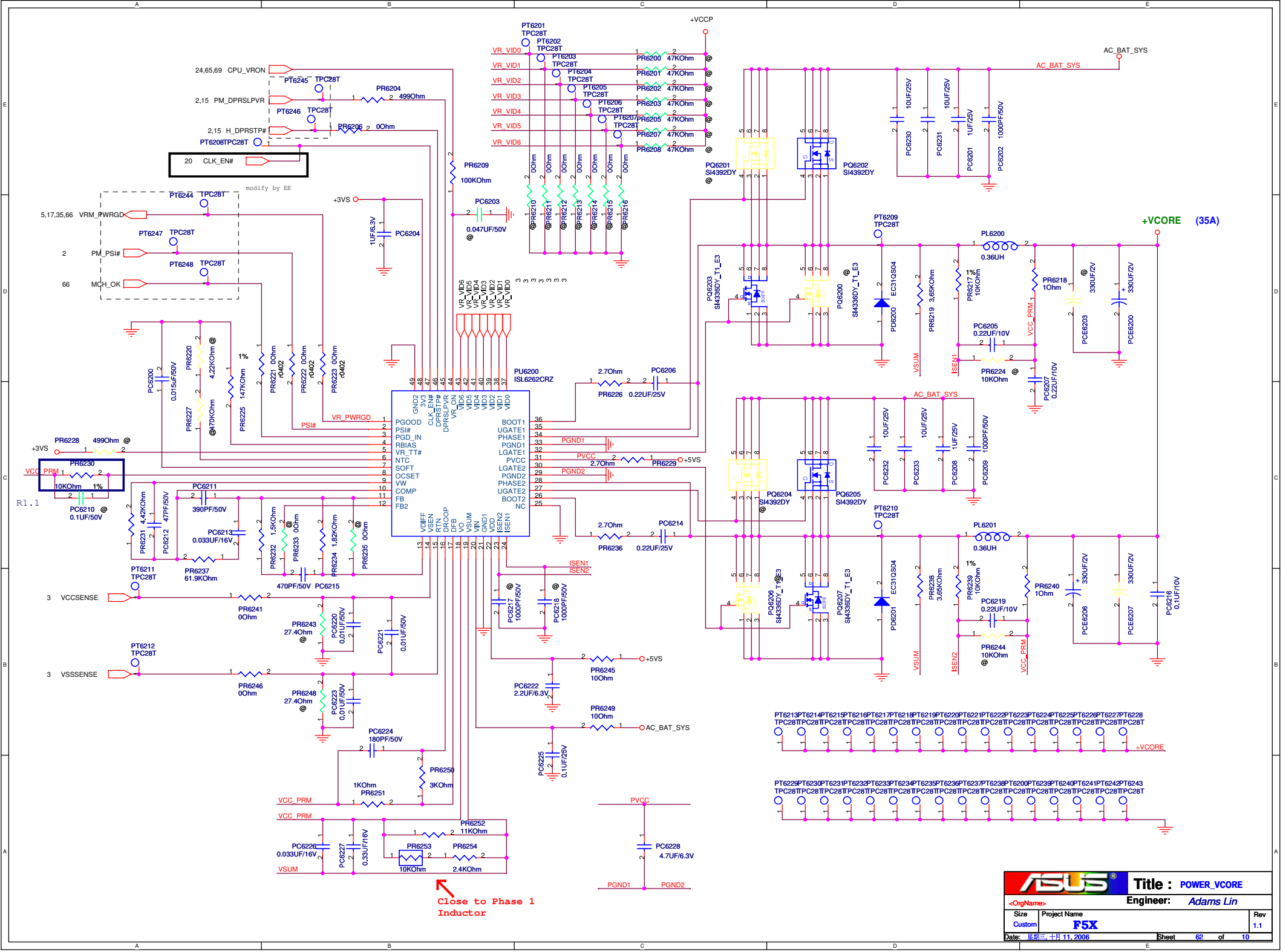
Page3 DNI CE301,CE302,CE303,CE304,CE305
Page4 R401,R406 change to 0 ohm
Page5 R513 cahnge to 220K ohm,Mount R514, DNI R511
Page8 add (L809 and C811)DNI for RC610
Page16 X1601 change to PN:07G010Q02501 for cost
Page22 R2201,R2203 change to 0ohm DNI R2205,R2206 chenge U2201 P/N for cost down
page 24 R2404 change to 4.7Kohm
Page27 R2708 change to 0 ohm,change CON2702 P/N
Page28 Mount Q2803 for BIOS request
Page30 R3011,R3012 change to 0 ohm according to attansic demo schematic
Page32 C3201,C3202 change to 0.01u
Page39 Reverse CON3901 pin definition for ME request
Page42 X4201 change to PN:07G010Q02501 for cost down
Page 2 change R227 pull-up resistor from 200 ohm resistor to 470 ohm resistor according ATI suggestion
Page 5 remove D502 (for SB600,it is no need)
Page 8 chang Q803 from N-MOS to P-MOS,add Q804 for correction
Page11 correct HSYNC YSYNC the ESD prodection diodes connect to +5VS instead of +3vs.
page 15 add 8.2Kohm 5% pull-down resistor on A_RST# to ensure a logic low at initial power-on.
Page 16 Please leave pin SATA_RX1/2/3+/- unconnected, do not connected them to ground according to ATI suggestion
Page 16 remove R1609,RN1601according to ATI suggestion
Page 17 change R1730,R1731,R1732 pull-up resistor to +3.3VSUS
page 38 add EMI finger
page 16 change C1611,C1612 from 24pf to 10pf

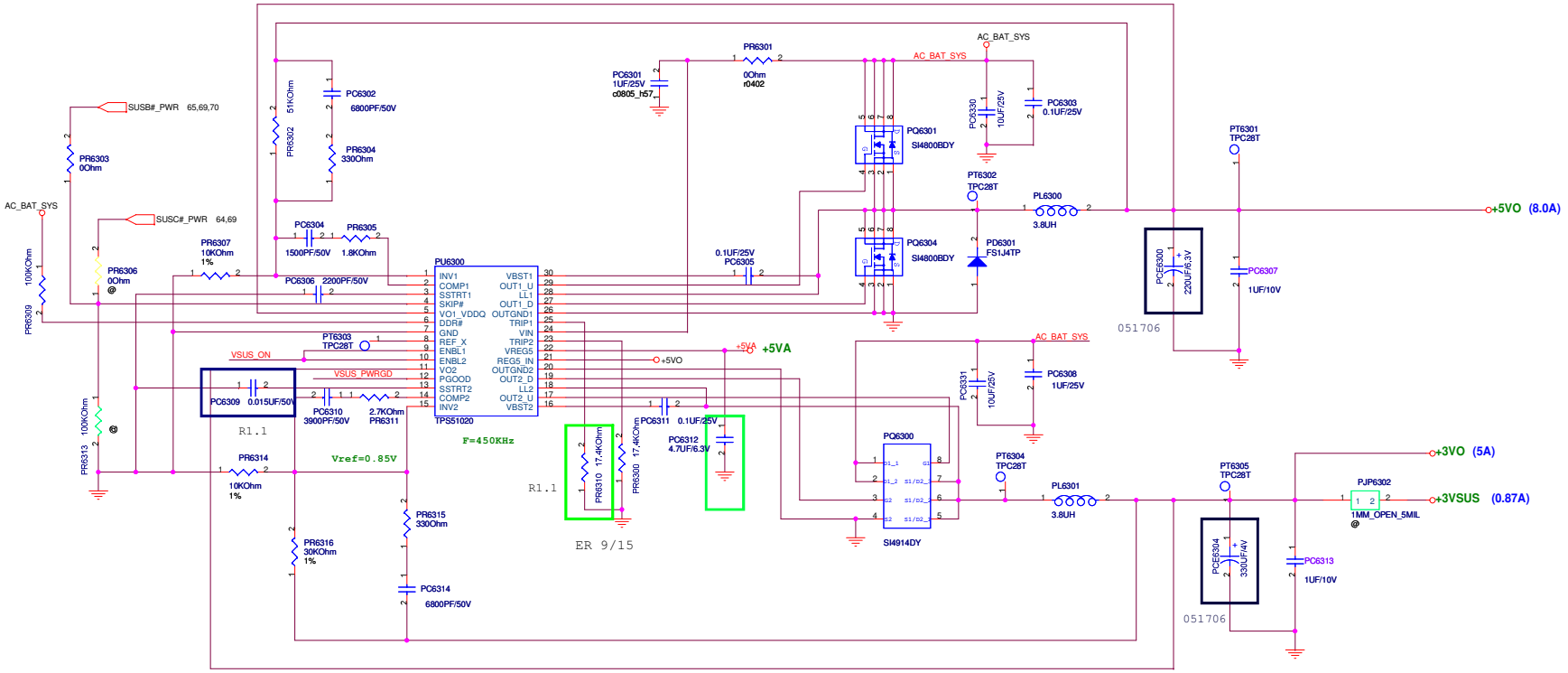
R2.0

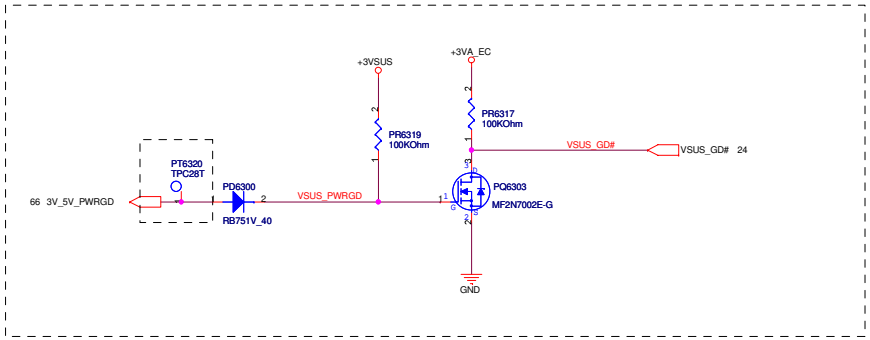
page 2 ,24 add CPU throttle function for power team request (add Q2407)
page16 delete change net name CPPE_EN,and delete its pull down resistor RN1604
page17 change net name CPPE_DET#, unmount R1730,R1731,R1732 for fix bug :cannot find ODD
page 22 exchange SPKL+ SPKL-,SPKR+ SPKR-,EAR_R EAR_L for correction, add R2219 for vista option
Modify CON3001,CON2801,CON2703,H3801,H3802 P/N
Modify R2102 value from 33ohm to 47ohm for correcting AC_SDIN0 slew rate.
Modify L1101,L1102,L1103 from bead to inductor 68nH for correction R G B signal rise time falling time and amplitude

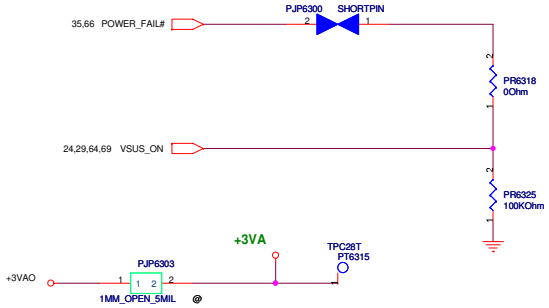
<Variant Name>

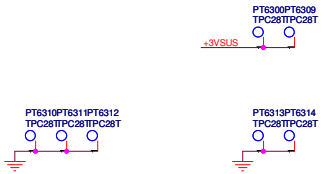
ASUSTeK COMPUTER INC	Title : change list	
	Engineer: Chris_liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 2.0
Date: 星期三, 十月 11, 2006	Sheet 46 of 71	

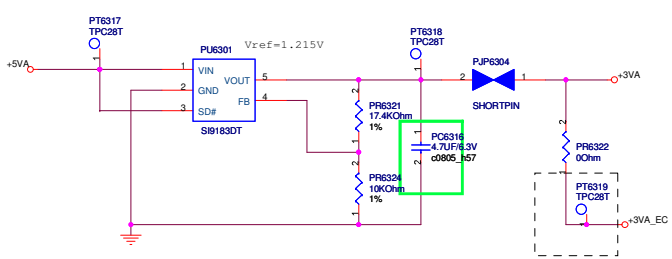

+VCCP
AC_BAT_SYS
+VCORE (35A)
PU6200
ISL6262CRZ
PQ6201 SI4392DY
PQ6202 SI4392DY
PQ6203 SI4336DY_T1_E3
PQ6200 SI4336DY_T1_E3
PQ6204 SI4392DY
PQ6205 SI4392DY
PQ6206 SI4336DY_T1_E3
PQ6207 SI4336DY_T1_E3
PD6200 EC31QS04
PD6201 EC31QS04
PL6200 0.36UH
PL6201 0.36UH
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
CPU_VRON
PM_DPRSLPVR
H_DPRSTP#
CLK_EN#
VRM_PWRGD
PM_PSI#
MCH_OK
VCCSENSE
VSSSENSE
VCC_PRM
VSUM
ISEN1
ISEN2
PVCC
PGND1
PGND2
+3VS
+5VS
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer: Adams Lin
Project Name F5X
Size Custom
Rev 1.1
Date: 星期三, 十月 11, 2006
Sheet 62 of 10

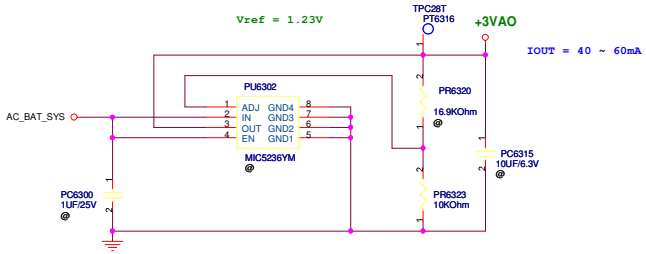




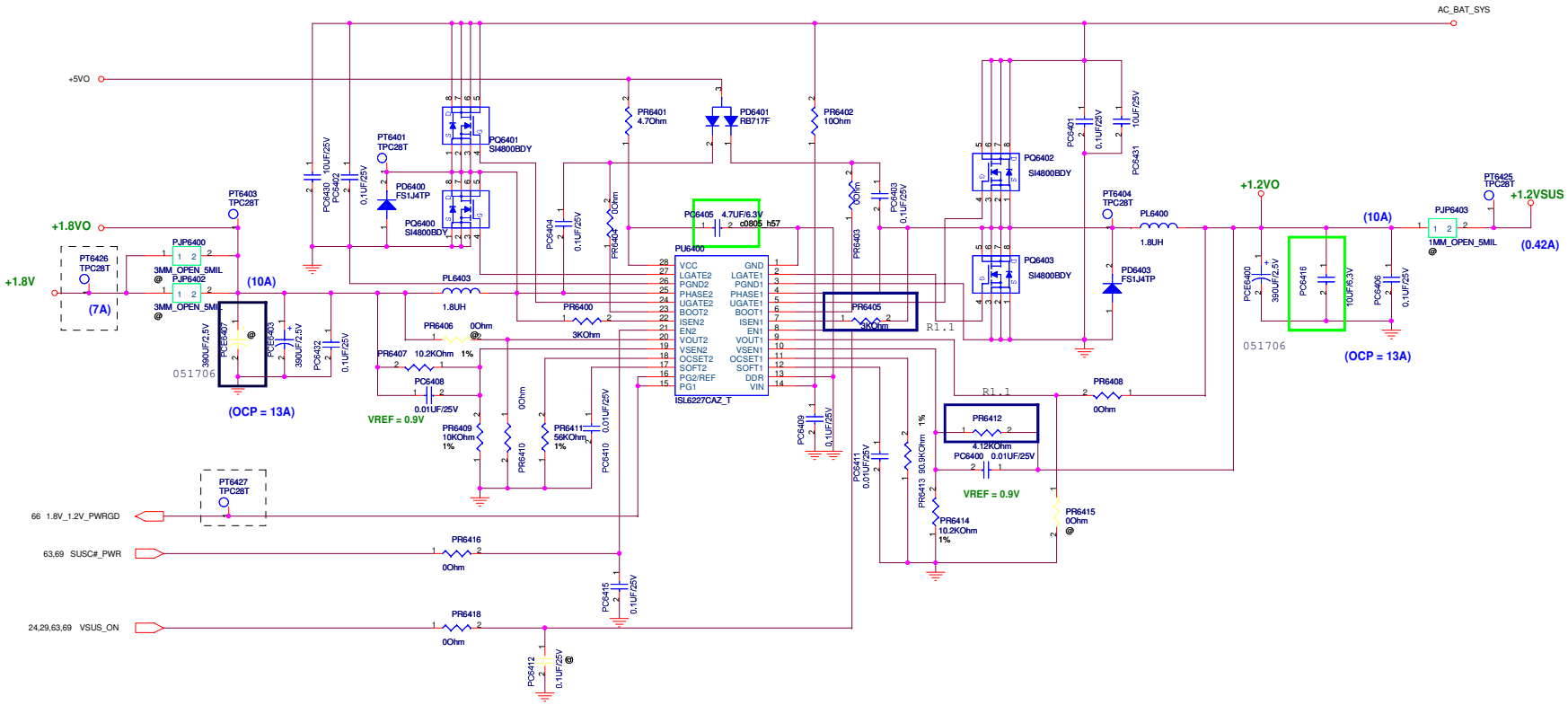


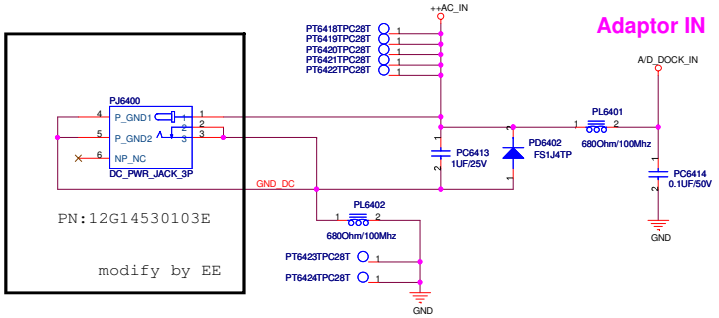




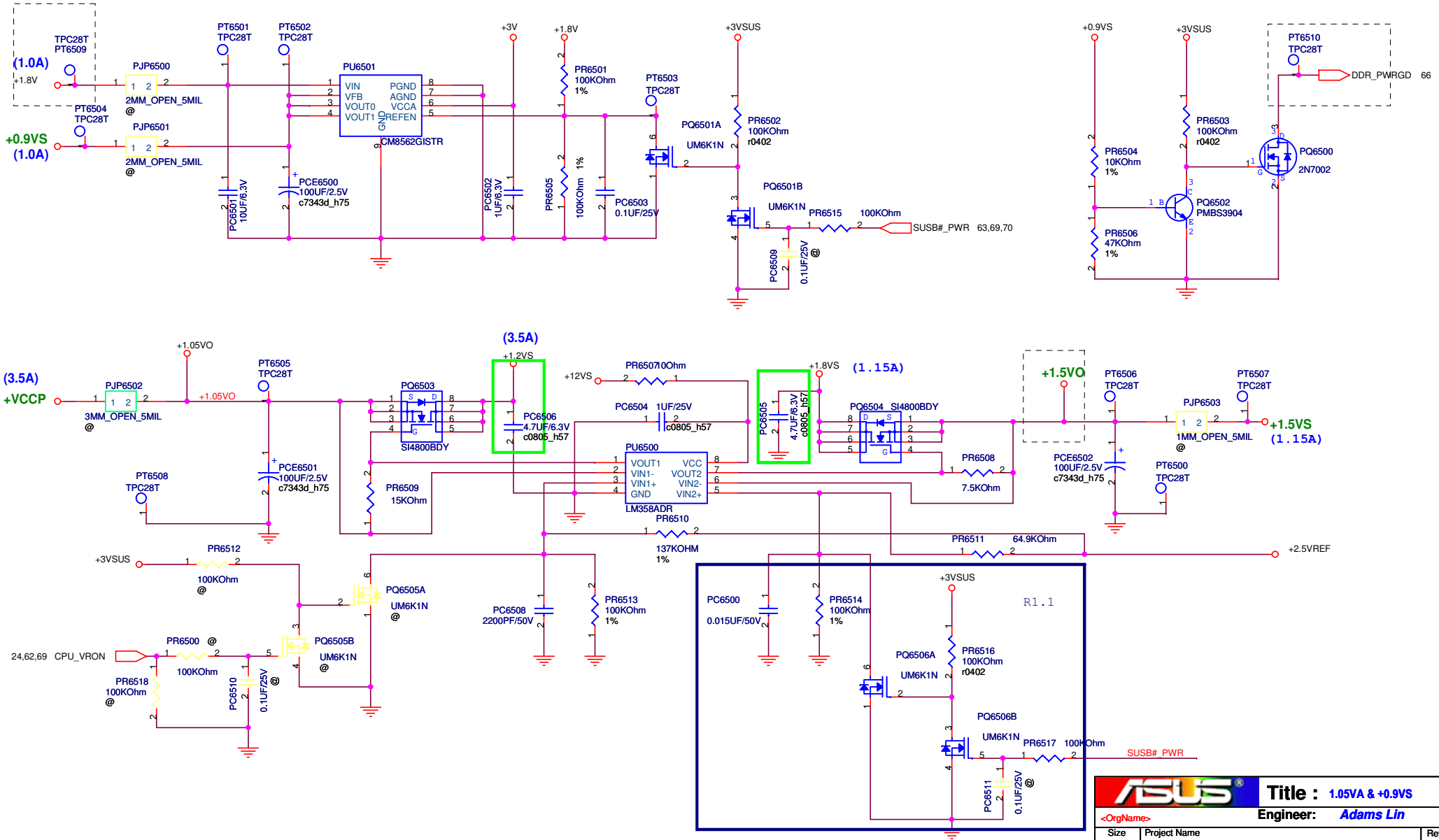


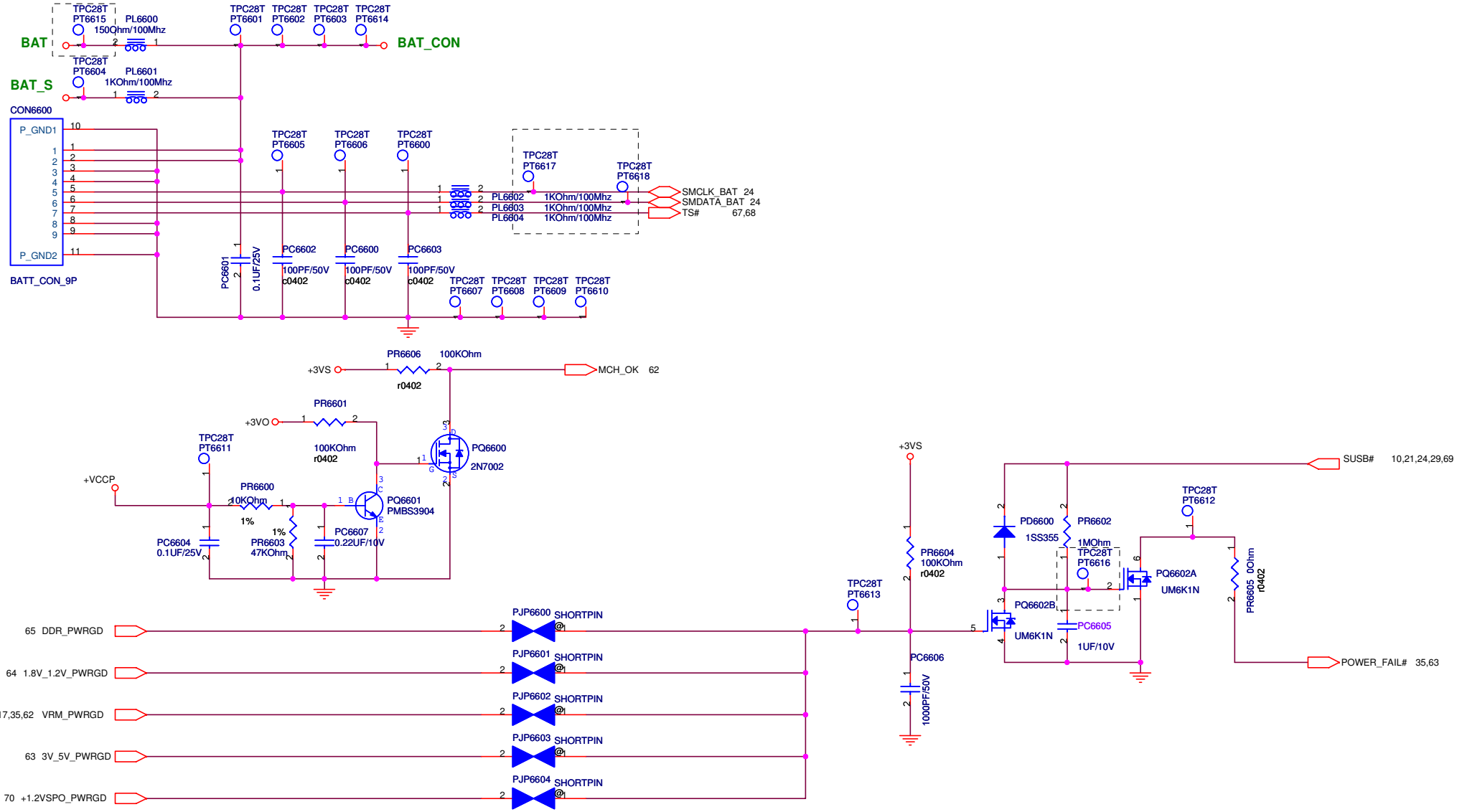
ASUS	Title : SYSTEM_+5VA & +3VA	
<OrgName>	Engineer: Adams Lin	
Size: C	Project Name: F5X	Rev: 1.1
Date: 星期三, 十月 11, 2006	Sheet 63 of 10	



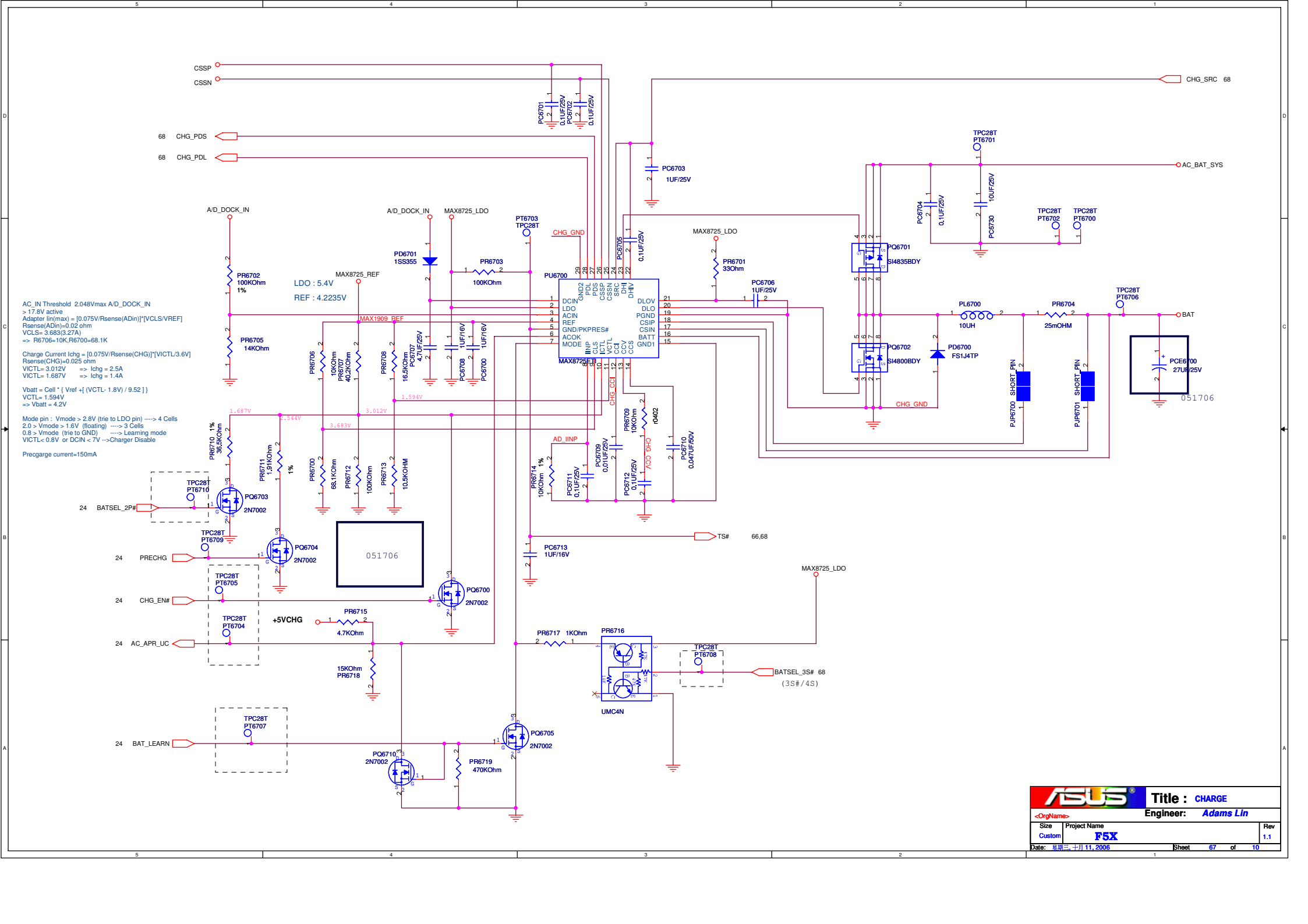


Title : 1.8V&1.2VS		
<OrgName>	Engineer: Adams Lin	
Size: C	Project Name: F5X	Rev: 1.1
Date: 星期三, 十月 11, 2006	Sheet 64 of 10	

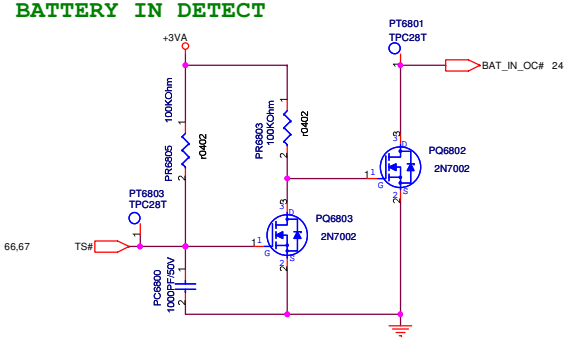

(1.0A)
+1.8V
TPC28T PT6509
PJP6500
2MM_OPEN_5MIL
@
PT6504 TPC28T
+0.9VS
(1.0A)
PJP6501
2MM_OPEN_5MIL
@
PT6501 TPC28T
PT6502 TPC28T
PU6501
VIN PGND
VFB AGND
VOUT0 VCCA
VOUT1 VREFEN
GND
CM8562GISTR
PC6501 10UF/6.3V
PCE6500 100UF/2.5V c7343d_h75
PC6502 1UF/6.3V
+3V
+1.8V
PR6501 100KOhm 1%
PR6505 100KOhm 1%
PC6503 0.1UF/25V
PT6503 TPC28T
PQ6501A UM6K1N
+3VSUS
PR6502 100KOhm r0402
PQ6501B UM6K1N
PR6515 100KOhm
SUSB#_PWR 63,69,70
PC6509 0.1UF/25V @
+0.9VS
PR6504 10KOhm 1%
PR6506 47KOhm 1%
PR6503 100KOhm r0402
PQ6502 PMBS3904
PQ6500 2N7002
PT6510 TPC28T
DDR_PWRGD 66
(3.5A)
+VCCP
PJP6502
3MM_OPEN_5MIL
@
+1.05VO
PT6505 TPC28T
PCE6501 100UF/2.5V c7343d_h75
PT6508 TPC28T
PQ6503 SI4800BDY
PR6509 15KOhm
(3.5A)
+1.2VS
PC6506 4.7UF/6.3V c0805_h57
+12VS
PR6507 10Ohm
PC6504 1UF/25V c0805_h57
PU6500
VOUT1 VCC
VIN1- VOUT2
VIN1+ VIN2-
GND VIN2+
LM358ADR
PC6505 4.7UF/6.3V c0805_h57
+1.8VS
(1.15A)
PQ6504 SI4800BDY
PR6508 7.5KOhm
PR6510 137KOHM 1%
PR6511 64.9KOhm
+2.5VREF
+1.5VO
PT6506 TPC28T
PCE6502 100UF/2.5V c7343d_h75
PT6500 TPC28T
PJP6503
1MM_OPEN_5MIL
@
PT6507 TPC28T
+1.5VS
(1.15A)
+3VSUS
PR6512 100KOhm @
PQ6505A UM6K1N @
PQ6505B UM6K1N @
PR6500 @ 100KOhm
24,62,69 CPU_VRON
PR6518 100KOhm @
PC6510 0.1UF/25V @
PC6508 2200PF/50V
PR6513 100KOhm 1%
PC6500 0.015UF/50V
PR6514 100KOhm 1%
R1.1
PQ6506A UM6K1N
PR6516 100KOhm r0402
PQ6506B UM6K1N
PR6517 100KOhm
SUSB#_PWR
PC6511 0.1UF/25V @
Title : 1.05VA & +0.9VS
<OrgName>
Engineer: Adams Lin
Size B
Project Name F5X
Rev 1.1
Date: 星期三, 十月 11, 2006
Sheet 65 of 10

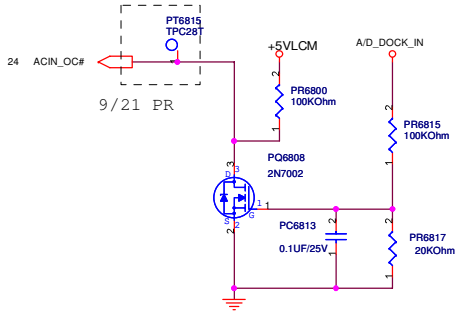


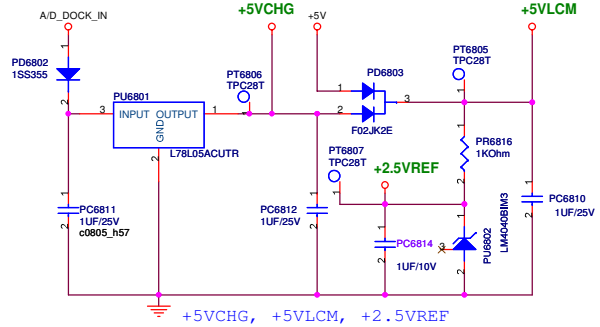
Title : BAT CON/PWOK		
<OrgName>	Engineer: Adams Lin	
Size: B	Project Name: F5X	Rev: 1.1
Date: 星期三, 十月 11, 2006	Sheet 66 of 10	

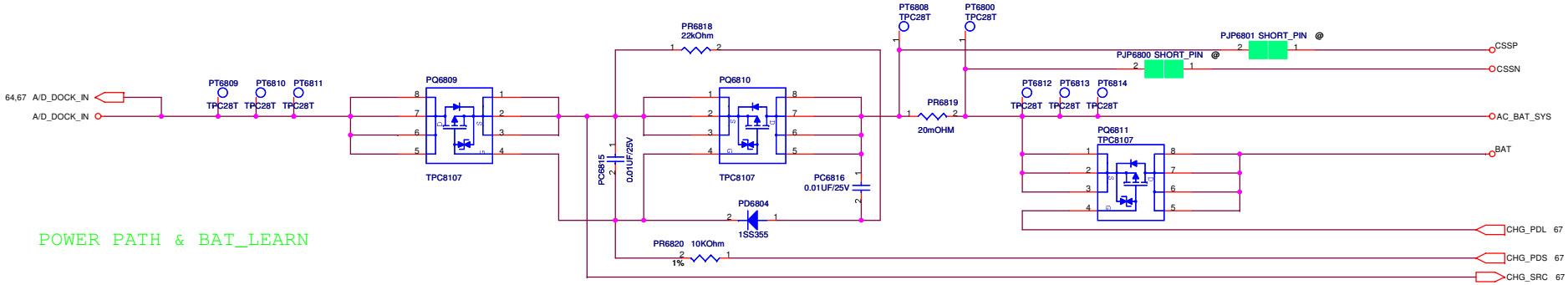

CSSP
CSSN
CHG_SRC 68
68 CHG_PDS
68 CHG_PDL
AC_BAT_SYS
BAT
A/D_DOCK_IN
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
MAX1909_REF
CHG_GND
PU6700
MAX8725EUI
PT6703 TPC28T
PC6703 1UF/25V
PD6701 1SS355
PR6703 100KOhm
PR6701 33Ohm
PC6706 1UF/25V
PR6702 100KOhm 1%
PR6705 14KOhm
PR6706
PR6707 10KOhm 40.2KOhm
PR6708 16.5KOhm
PC6707 4.7UF/25V
PC6708 1UF/16V
PC6700 1UF/16V
PC6705 0.1UF/25V
PC6701 0.1UF/25V
PC6702 0.1UF/25V
PC6704 0.1UF/25V
PC6730 10UF/25V
TPC28T PT6701
TPC28T PT6702
TPC28T PT6700
TPC28T PT6706
PQ6701 SI4835BDY
PQ6702 SI4800BDY
PD6700 FS1J4TP
PL6700 10UH
PR6704 25mOHM
PJP6700 SHORT_PIN
PJP6701 SHORT_PIN
PCE6700 27UF/25V
051706
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.8V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.683(3.27A)
=> R6706=10K,R6700=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.012V => Ichg = 2.5A
VICTL= 1.687V => Ichg = 1.4A
Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.594V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
1.687V
2.544V
3.012V
3.683V
1.594V
PR6710 1% 36.5KOhm
PR6711 1.91KOhm 1%
PR6700 68.1KOhm
PR6712 100KOhm
PR6713 10.5KOHM
TPC28T PT6710
PQ6703 2N7002
24 BATSEL_2P#
TPC28T PT6709
PQ6704 2N7002
24 PRECHG
TPC28T PT6705
24 CHG_EN#
PQ6700 2N7002
TPC28T PT6704
+5VCHG
PR6715 4.7KOhm
24 AC_APR_UC
15KOhm PR6718
TPC28T PT6707
24 BAT_LEARN
PQ6710 2N7002
PR6719 470KOhm
PQ6705 2N7002
AD_IINP
PR6714 10KOhm 1%
PC6711 0.1UF/25V
PC6709 0.01UF/25V
PR6709 10KOhm
R402
CHG_CCV
PC6712 0.1UF/25V
PC6710 0.047UF/50V
CHG_CCI
TS# 66,68
PC6713 1UF/16V
PR6717 1KOhm
PR6716
UMC4N
TPC28T PT6708
BATSEL_3S# 68
(3S#/4S)
Title : CHARGE
Engineer: Adams Lin
<OrgName>
Size Custom
Project Name F5X
Rev 1.1
Date: 星期三, 十月 11, 2006
Sheet 67 of 10

BATTERY IN DETECT

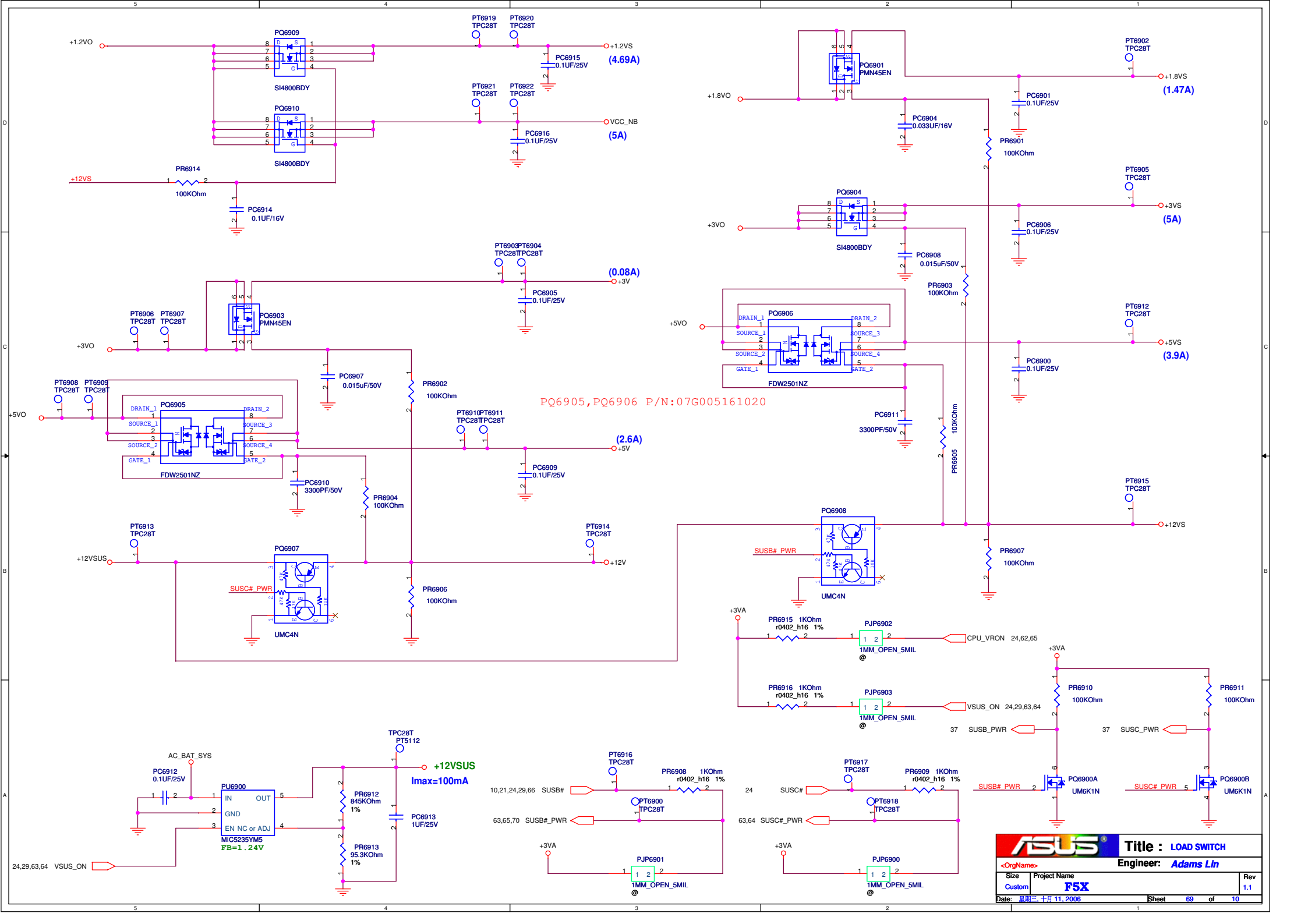








ASUS	Title : PROTECTION/SD#	
<OrgName>	Engineer: Adams Lin	
Size: Custom	Project Name: F5X	Rev: 1.1
Date: 星期三, 十月 11, 2006	Sheet 68 of 10	



ASUS

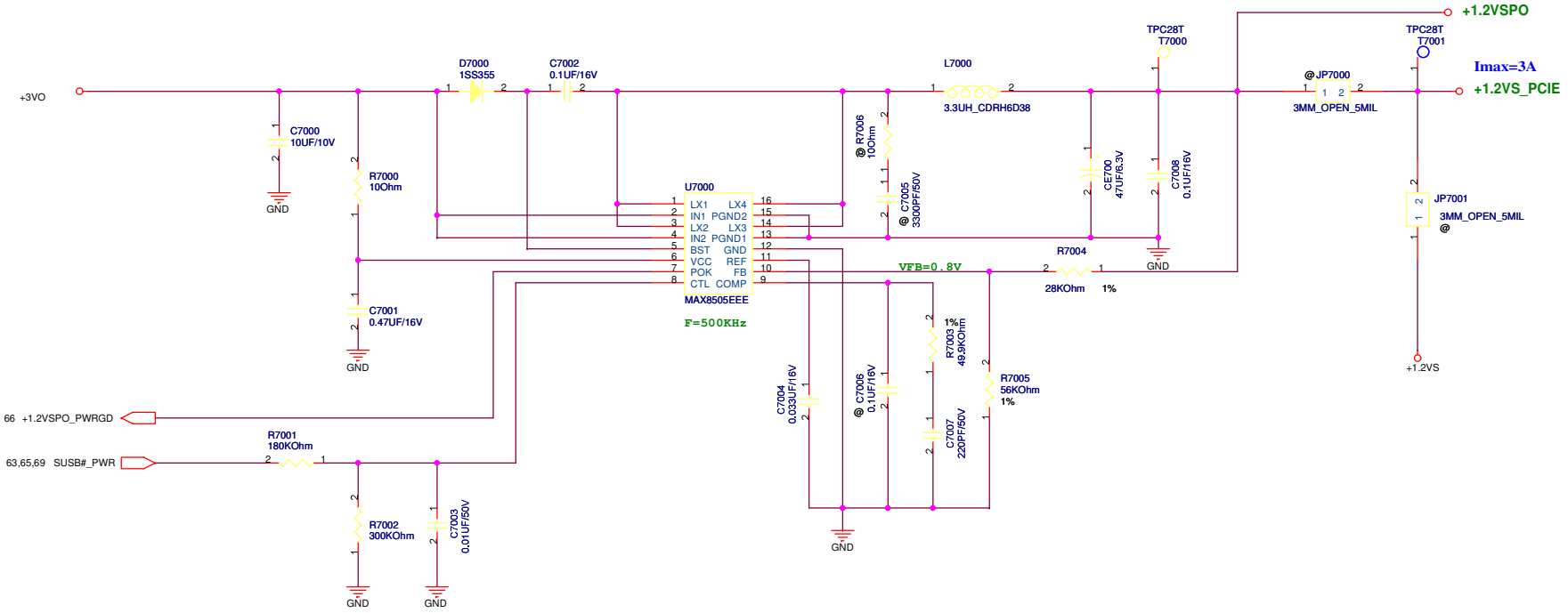
Title : LOAD SWITCH

<OrgName>

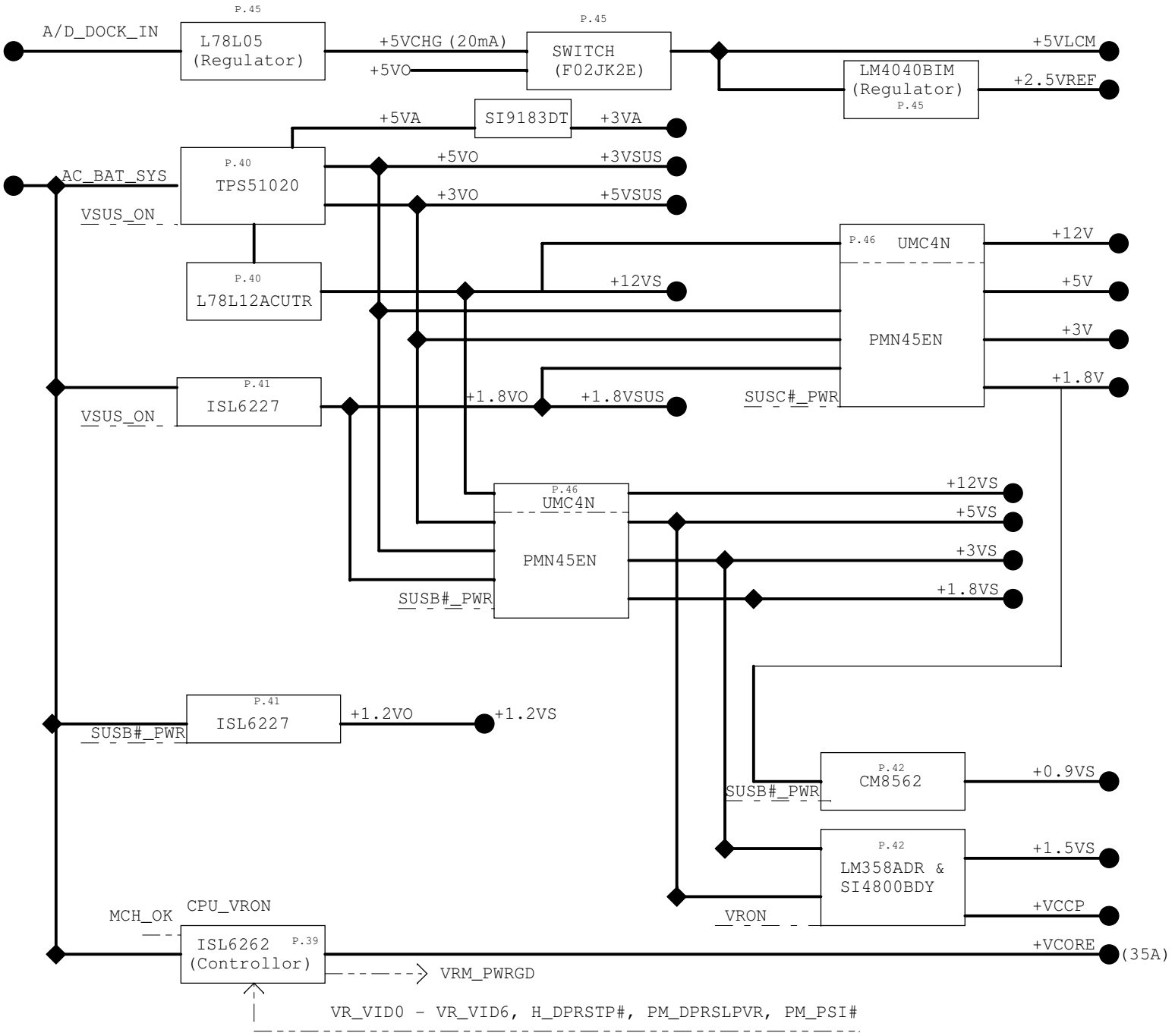
Engineer: Adams Lin

Size	Project Name	Rev
Custom	F5X	1.1

Date: 星期二, 十月 11, 2006 Sheet 69 of 10



ASUS	Title : POWER_1.2VS_PCIE	
<OrgName>	Engineer:	
Size: Custom	Project Name: F5X	Rev: 1.1
Date: 星期三, 十月 11, 2006	Sheet 70 of 10	


A/D_DOCK_IN
P.45
L78L05
(Regulator)
+5VCHG (20mA)
+5VO
P.45
SWITCH
(F02JK2E)
+5VLCM
LM4040BIM
(Regulator)
P.45
+2.5VREF
+5VA
SI9183DT
+3VA
P.40
TPS51020
+5VO
+3VSUS
AC_BAT_SYS
+3VO
+5VSUS
VSUS_ON
P.46
UMC4N
+12V
P.40
L78L12ACUTR
+12VS
+5V
PMN45EN
+3V
+1.8V
P.41
ISL6227
+1.8VO
+1.8VSUS
SUSC#_PWR
VSUS_ON
P.46
UMC4N
+12VS
+5VS
PMN45EN
+3VS
+1.8VS
SUSB#_PWR
P.41
ISL6227
+1.2VO
+1.2VS
SUSB#_PWR
P.42
CM8562
+0.9VS
SUSB#_PWR
P.42
LM358ADR &
SI4800BDY
+1.5VS
+VCCP
VRON
MCH_OK
CPU_VRON
ISL6262
(Controllor)
P.39
+VCORE
(35A)
VRM_PWRGD
VR_VID0 - VR_VID6, H_DPRSTP#, PM_DPRSLPVR, PM_PSI#