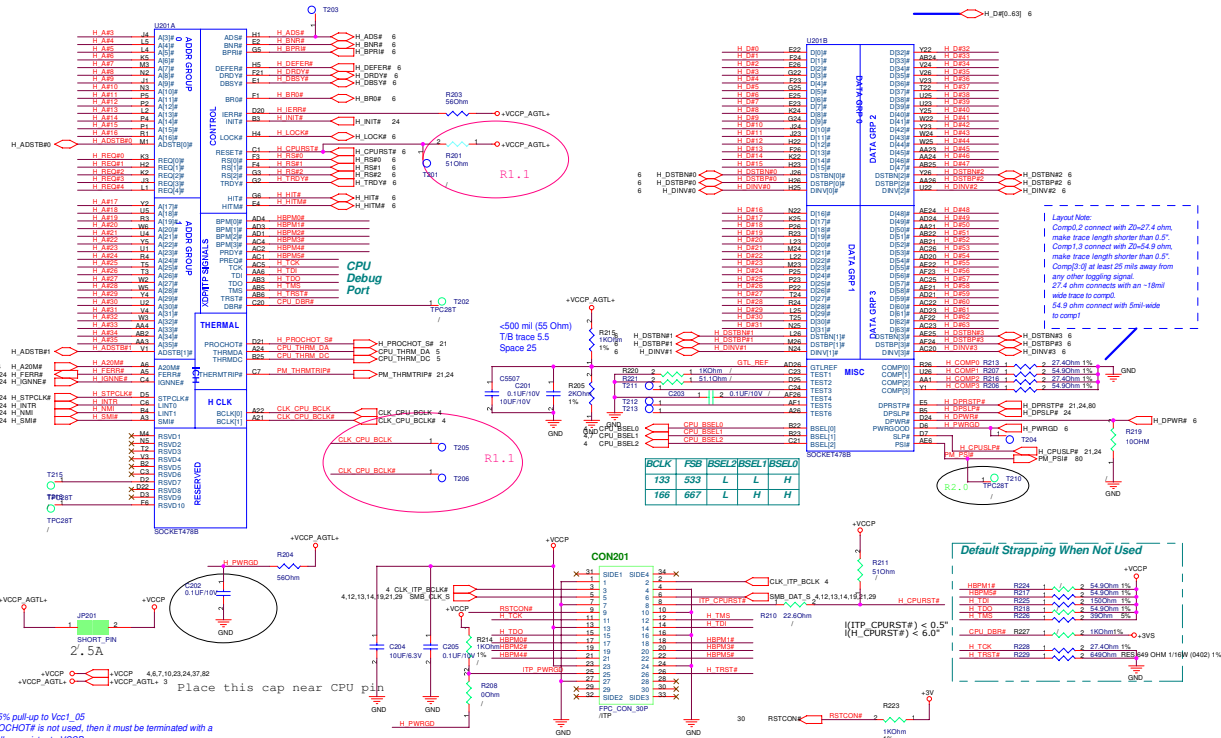
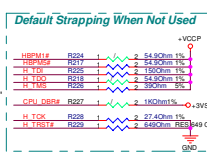


ASUS		Title : Block Diagram	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
B	FSV		1.0
Date: #B#	#B# 23 2007	Sheet	1 of 94

<< Kennedy_Zhang >>



Layout Note:
 Comp2.2 connect with Z0-27.4 ohm,
 make trace length shorter than 0.5".
 Comp1.5 connect with Z0-4.8 ohm,
 make trace length shorter than 0.5".
 Comp3.0 at least 20 mils away from
 any other logging signal.
 27.4 ohm connects with an -18mil
 wide trace to comp1.
 54.8 ohm connect with 5mil wide
 to comp1.



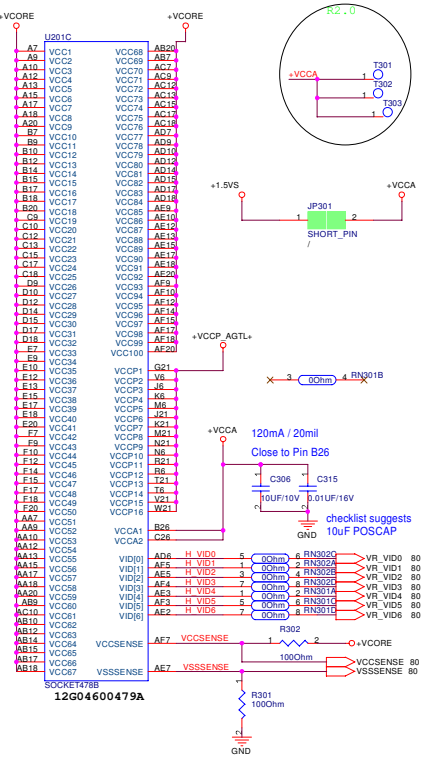
68 ± 5% pull-up to Vcc1_05
 If PROCHOT# is not used, then it must be terminated with a
 56 pull-up resistor to VCCP.
 If PROCHOT# is routed between CPU, IMVP and MCH,
 pull-up resistor has to be 75 Ohm ± 5%.



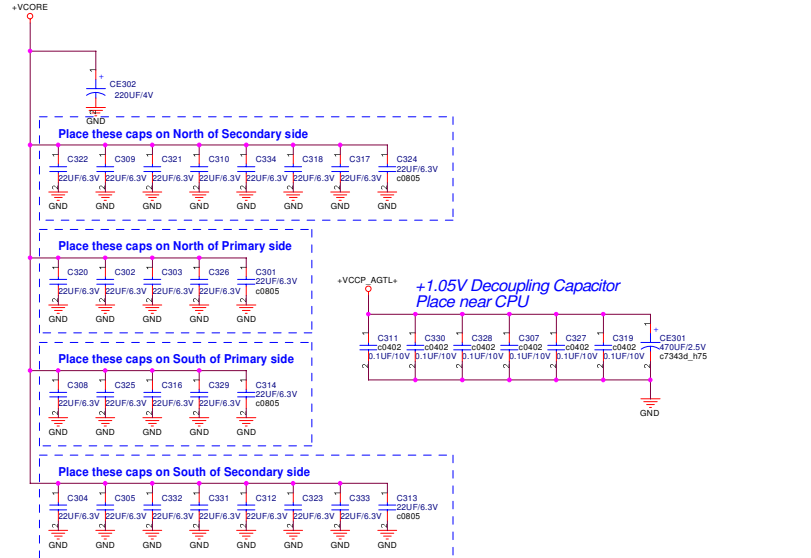
« Kennedy_Zhang »

YUNAH FSB667			
LFM	TYP	HFV	
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

YUNAH FSB667			
VCCP	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
ICCP	Min	Typ	Max
ICCP			2.5A



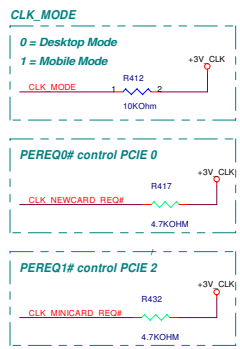
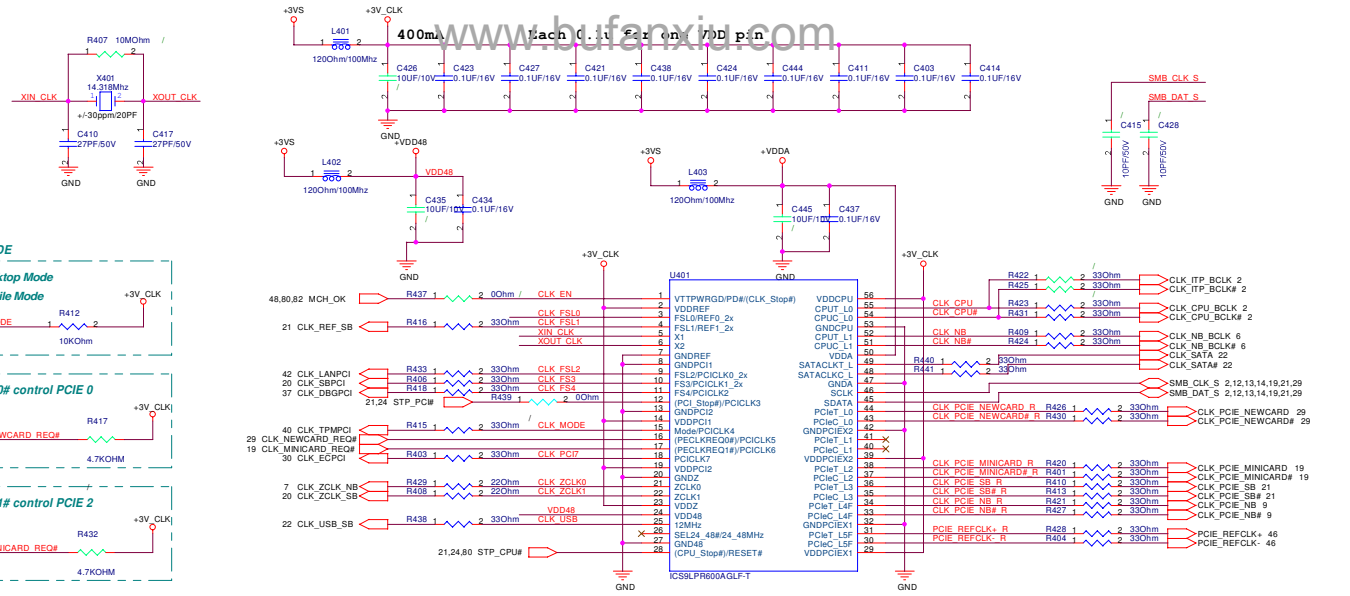
J201D			
A4	VSS1	VSS83	P21
A8	VSS3	VSS85	P23
A11	VSS5	VSS87	P25
A14	VSS7	VSS89	P27
A16	VSS9	VSS91	P29
A19	VSS11	VSS93	P31
A23	VSS13	VSS95	P35
A26	VSS15	VSS97	P38
A29	VSS17	VSS99	P41
B6	VSS19	VSS101	P44
B8	VSS21	VSS103	P46
B11	VSS23	VSS105	P49
B14	VSS25	VSS107	P51
B16	VSS27	VSS109	P53
B19	VSS29	VSS111	P55
B21	VSS31	VSS113	P57
B24	VSS33	VSS115	P59
B27	VSS35	VSS117	P61
B29	VSS37	VSS119	P63
C4	VSS39	VSS121	P65
C5	VSS41	VSS123	P67
C8	VSS43	VSS125	P69
C11	VSS45	VSS127	P71
C14	VSS47	VSS129	P73
C17	VSS49	VSS131	P75
C19	VSS51	VSS133	P77
C22	VSS53	VSS135	P79
C25	VSS55	VSS137	P81
C28	VSS57	VSS139	P83
D1	VSS59	VSS141	P85
D4	VSS61	VSS143	P87
D6	VSS63	VSS145	P89
D11	VSS65	VSS147	P91
D16	VSS67	VSS149	P93
D19	VSS69	VSS151	P95
D24	VSS71	VSS153	P97
D29	VSS73	VSS155	P99
E2	VSS75	VSS157	P101
E4	VSS77	VSS159	P103
E6	VSS79	VSS161	P105
E8	VSS81	VSS163	P107
E9	VSS83	VSS165	P109
E11	VSS85	VSS167	P111
E14	VSS87	VSS169	P113
E16	VSS89	VSS171	P115
E19	VSS91	VSS173	P117
E21	VSS93	VSS175	P119
E24	VSS95	VSS177	P121
E26	VSS97	VSS179	P123
E29	VSS99	VSS181	P125
F4	VSS101	VSS183	P127
F6	VSS103	VSS185	P129
F8	VSS105	VSS187	P131
F11	VSS107	VSS189	P133
F14	VSS109	VSS191	P135
F16	VSS111	VSS193	P137
F19	VSS113	VSS195	P139
F21	VSS115	VSS197	P141
F24	VSS117	VSS199	P143
F26	VSS119	VSS201	P145
F29	VSS121	VSS203	P147
G2	VSS123	VSS205	P149
G4	VSS125	VSS207	P151
G11	VSS127	VSS209	P153
G16	VSS129	VSS211	P155
G21	VSS131	VSS213	P157
G26	VSS133	VSS215	P159
G31	VSS135	VSS217	P161
G36	VSS137	VSS219	P163
H4	VSS139	VSS221	P165
H6	VSS141	VSS223	P167
H8	VSS143	VSS225	P169
H11	VSS145	VSS227	P171
H14	VSS147	VSS229	P173
H16	VSS149	VSS231	P175
H19	VSS151	VSS233	P177
H21	VSS153	VSS235	P179
H24	VSS155	VSS237	P181
J2	VSS157	VSS239	P183
J4	VSS159	VSS241	P185
J6	VSS161	VSS243	P187
J8	VSS163	VSS245	P189
J11	VSS165	VSS247	P191
J14	VSS167	VSS249	P193
J16	VSS169	VSS251	P195
J19	VSS171	VSS253	P197
J21	VSS173	VSS255	P199
J24	VSS175	VSS257	P201
J26	VSS177	VSS259	P203
J29	VSS179	VSS261	P205
K1	VSS181	VSS263	P207
K4	VSS183	VSS265	P209
K6	VSS185	VSS267	P211
K11	VSS187	VSS269	P213
K16	VSS189	VSS271	P215
K21	VSS191	VSS273	P217
K26	VSS193	VSS275	P219
L4	VSS195	VSS277	P221
L6	VSS197	VSS279	P223
L11	VSS199	VSS281	P225
L14	VSS201	VSS283	P227
L16	VSS203	VSS285	P229
L19	VSS205	VSS287	P231
L21	VSS207	VSS289	P233
L24	VSS209	VSS291	P235
M2	VSS211	VSS293	P237
M5	VSS213	VSS295	P239
M6	VSS215	VSS297	P241
M11	VSS217	VSS299	P243
M16	VSS219	VSS301	P245
M21	VSS221	VSS303	P247
N1	VSS223	VSS305	P249
N4	VSS225	VSS307	P251
N6	VSS227	VSS309	P253
N11	VSS229	VSS311	P255
N16	VSS231	VSS313	P257
N21	VSS233	VSS315	P259
N26	VSS235	VSS317	P261
P4	VSS237	VSS319	P263
P9	VSS239	VSS321	P265



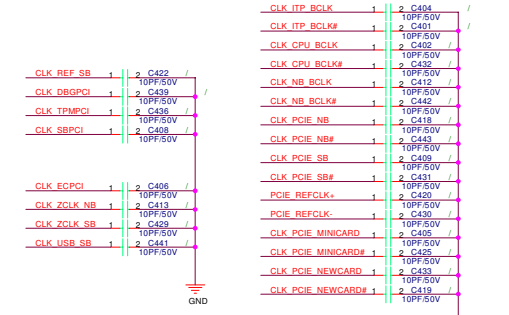
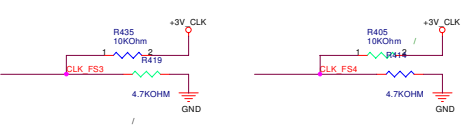
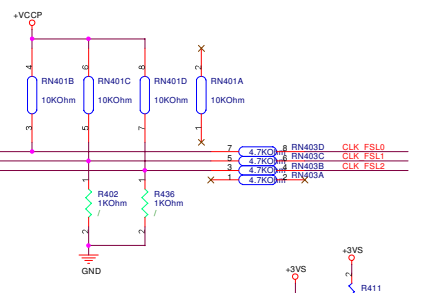
Layout Note:
 VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils with 7 mils spacing, with trace impedance of 20±2.4 Ohm.
 The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
 These resistors should be placed within 2 inch of the CPU.

ASUS		Title : Yonah CPU (2)	
ASUSTeK COMPUTER INC. Engineer: Hawk Zhu			
Size	Project Name	Rev	
A3	FSV	1.0	
Date: 08/11/03	11/11/03	Sheet	9 of 94

<< Kennedy_Zhang >>



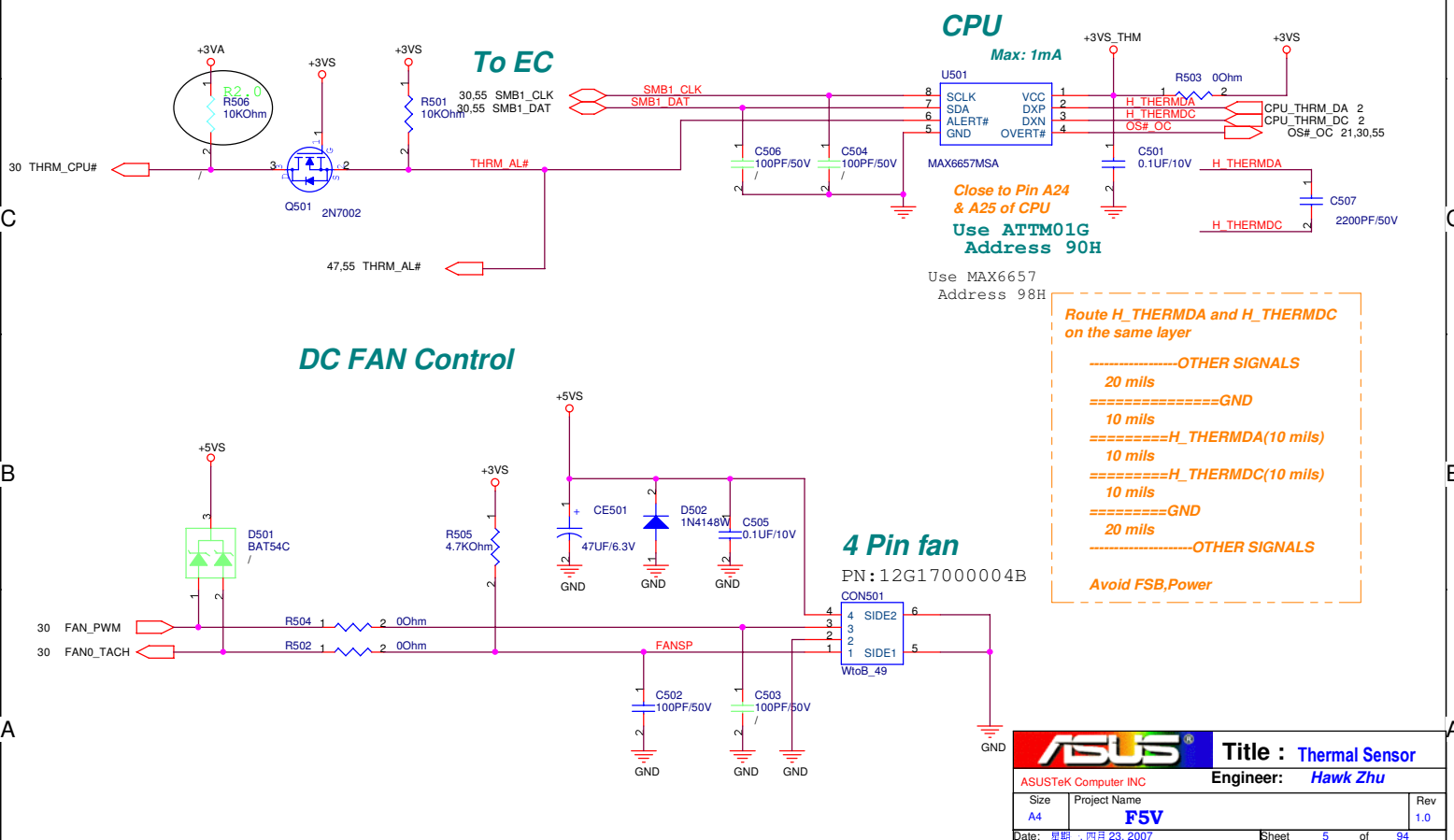
FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



ASUS Title : Clock GEN
 ASUSTek Computer INC Engineer: Hawk Zhu
 Size Project Name
 A3 FSV
 Date: 11/18/23, 2007 Sheet 4 of 34

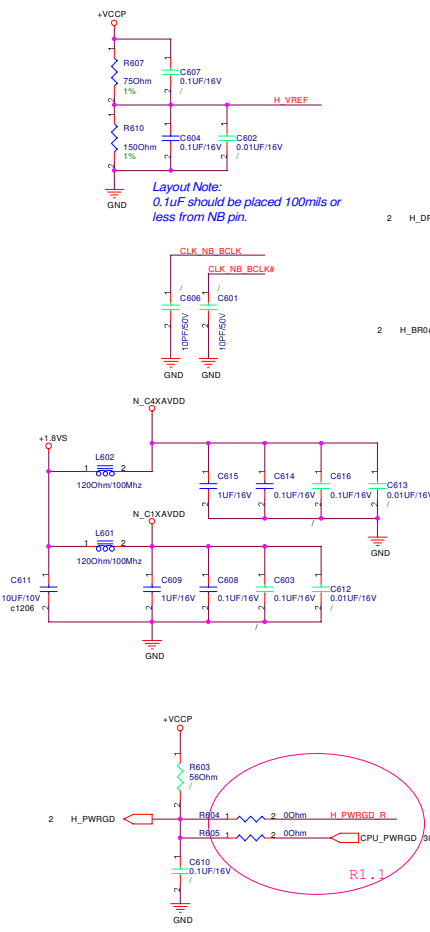
<< Kennedy_Zhang >>

Thermal Sensor



ASUS		Title : Thermal Sensor
ASUSTeK Computer INC		Engineer: Hawk Zhu
Size A4	Project Name F5V	Rev 1.0
Date: 星期四, 四月 23, 2007		Sheet 5 of 94

<< Kennedy_Zhang >>



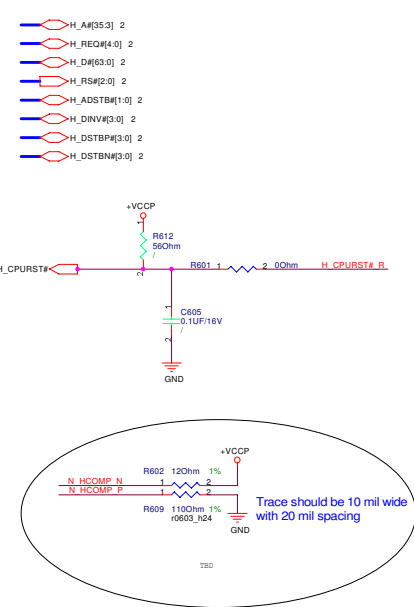
N_C1XAVDD 25mA

N_C1XAVSS 25mA

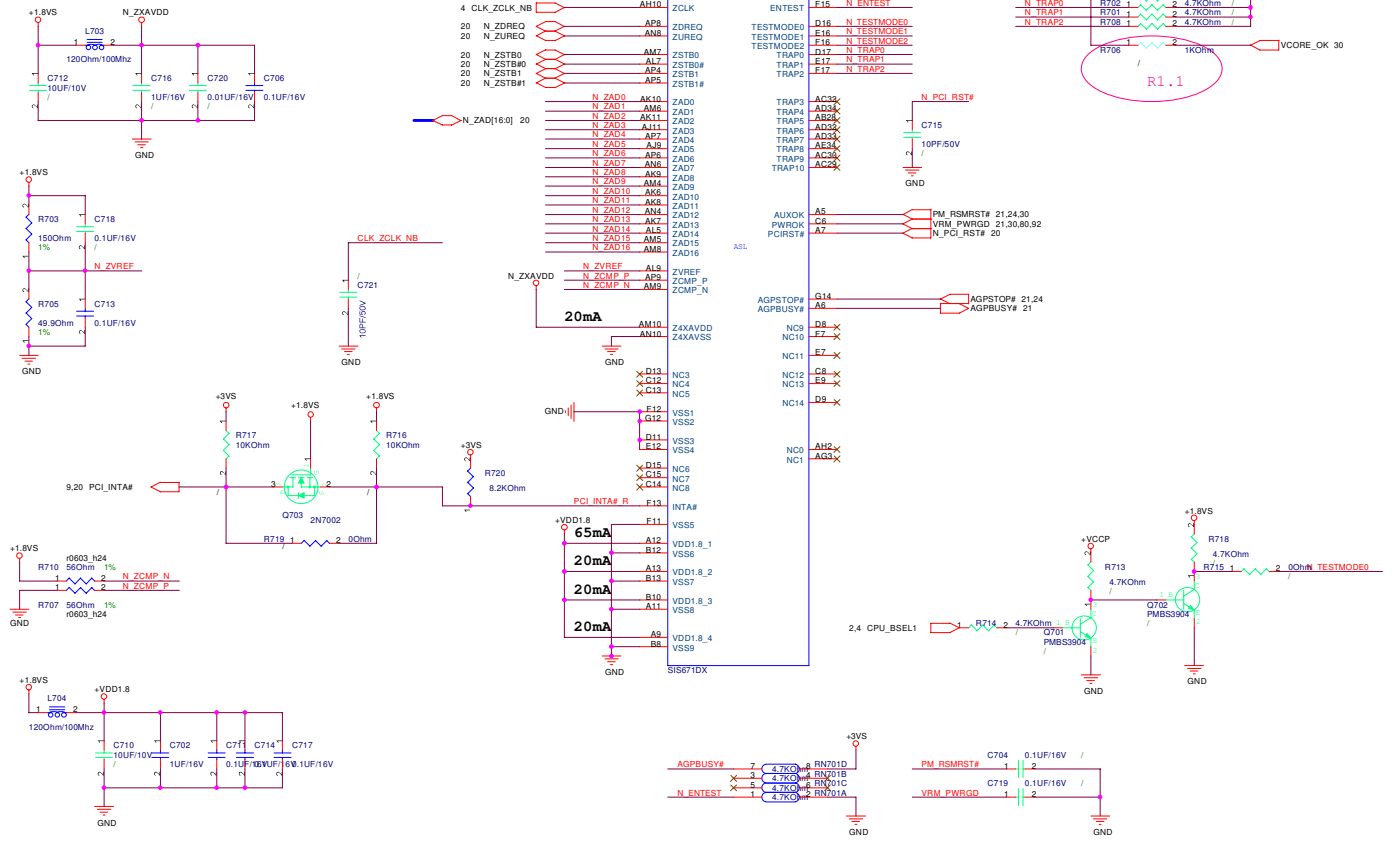
HD00#	N29	H_D40
HD01#	M28	H_D42
HD02#	L30	H_D43
HD03#	K28	H_D45
HD04#	J30	H_D47
HD05#	H31	H_D48
HD06#	G34	H_D49
HD07#	F33	H_D410
HD08#	E32	H_D411
HD09#	D32	H_D412
HD10#	C33	H_D413
HD11#	B33	H_D414
HD12#	A33	H_D415
HD13#	J30	H_D416
HD14#	H31	H_D417
HD15#	G34	H_D418
HD16#	F33	H_D419
HD17#	E32	H_D420
HD18#	D32	H_D421
HD19#	C33	H_D422
HD20#	B33	H_D423
HD21#	A33	H_D424
HD22#	J30	H_D425
HD23#	H31	H_D426
HD24#	G34	H_D427
HD25#	F33	H_D428
HD26#	E32	H_D429
HD27#	D32	H_D430
HD28#	C33	H_D431
HD29#	B33	H_D432
HD30#	A33	H_D433
HD31#	J30	H_D434
HD32#	H31	H_D435
HD33#	G34	H_D436
HD34#	F33	H_D437
HD35#	E32	H_D438
HD36#	D32	H_D439
HD37#	C33	H_D440
HD38#	B33	H_D441
HD39#	A33	H_D442
HD40#	J30	H_D443
HD41#	H31	H_D444
HD42#	G34	H_D445
HD43#	F33	H_D446
HD44#	E32	H_D447
HD45#	D32	H_D448
HD46#	C33	H_D449
HD47#	B33	H_D450
HD48#	A33	H_D451
HD49#	J30	H_D452
HD50#	H31	H_D453
HD51#	G34	H_D454
HD52#	F33	H_D455
HD53#	E32	H_D456
HD54#	D32	H_D457
HD55#	C33	H_D458
HD56#	B33	H_D459
HD57#	A33	H_D460
HD58#	J30	H_D461
HD59#	H31	H_D462
HD60#	G34	H_D463
HD61#	F33	H_D464
HD62#	E32	H_D465
HD63#	D32	H_D466
DB00#	A32	H_D467
DB01#	E32	H_D468
DB02#	F27	H_D469
DB03#	E23	H_D470
DB04#	H33	H_D471
DB05#	E31	H_D472
DB06#	B28	H_D473
DB07#	D04	H_D474
DB08#	H34	H_D475
DB09#	D32	H_D476
DB10#	A28	H_D477
DB11#	A28	H_D478
DB12#	E04	H_D479
DB13#	E04	H_D480
DB14#	A21	H_D481
DB15#	C21	H_D482

Host

SIS671DX



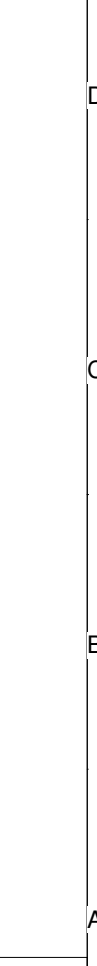
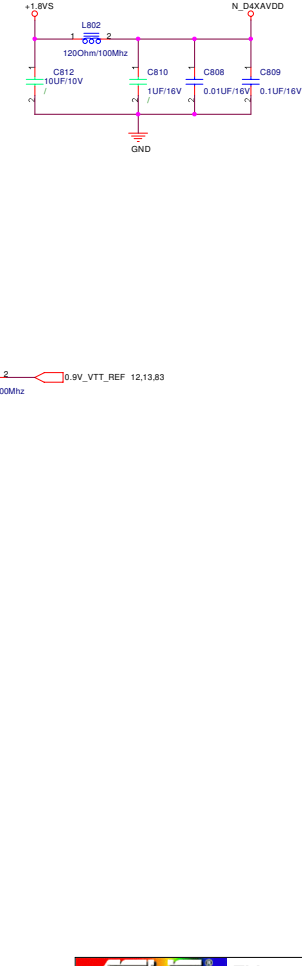
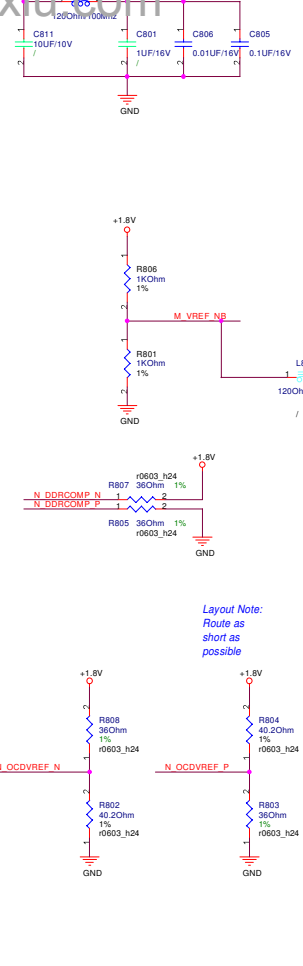
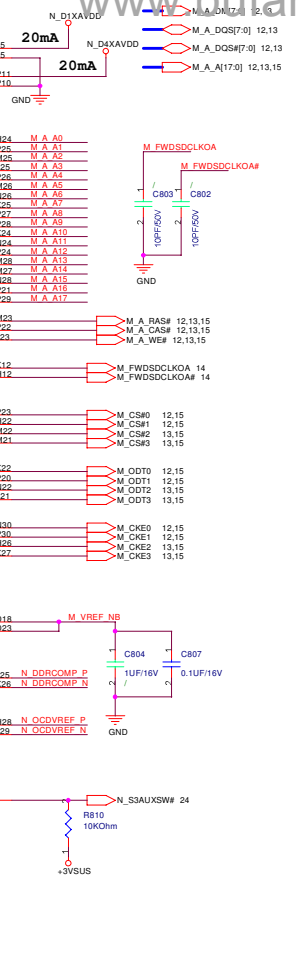
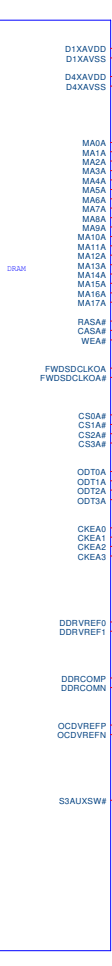
<< Kennedy_Zhang >>



ASUS		Title M671DX(MuTIOL&VGA)	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
A3	FSV		1.0
Date: 2007-10-23		Sheet 7 of 94	

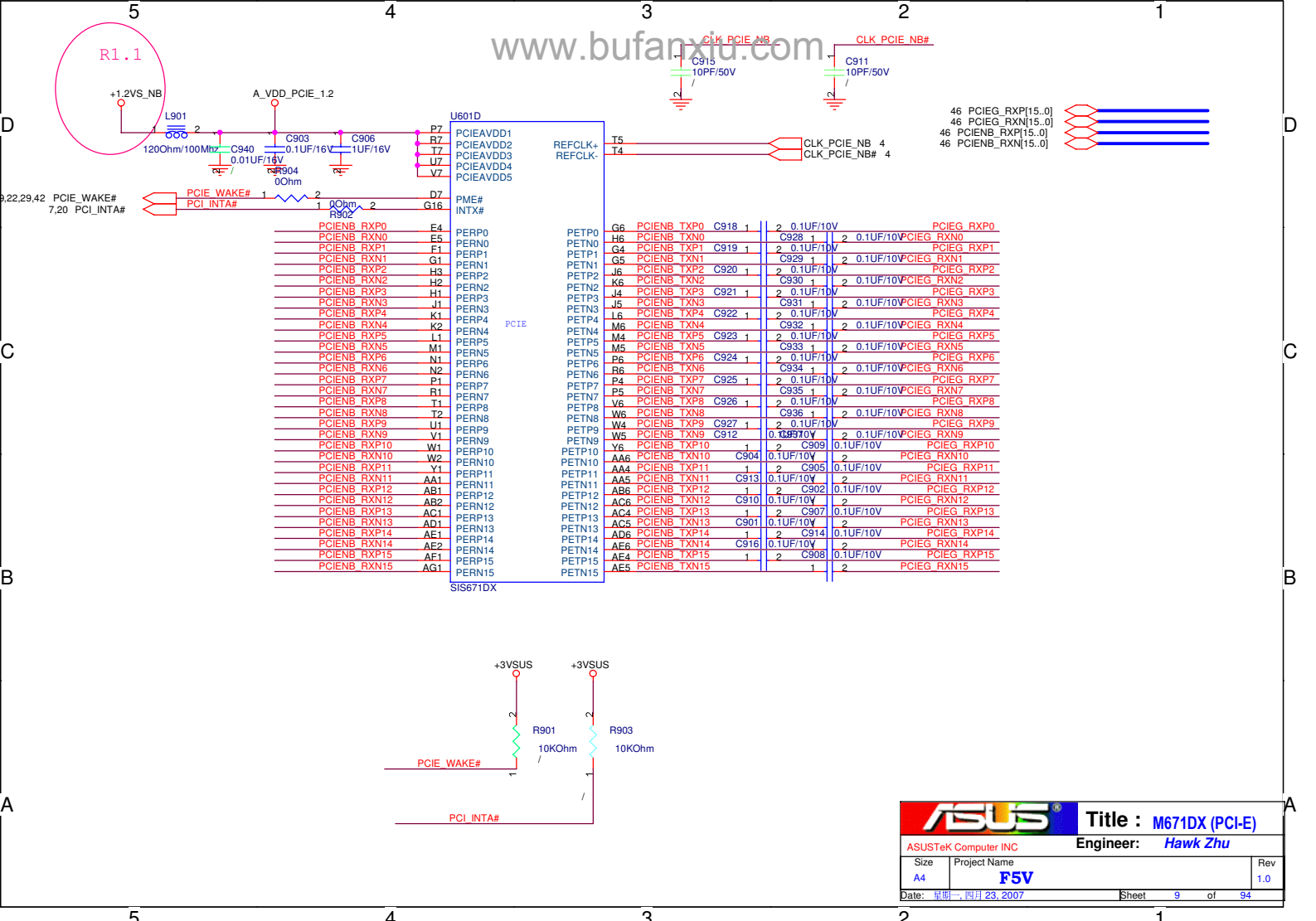
<< Kennedy_Zhang >>

M_A_DQ00	AD30	MD0A
M_A_DQ01	AD30	MD1A
M_A_DQ02	AG34	MD2A
M_A_DQ03	AE29	MD3A
M_A_DQ04	AE32	MD4A
M_A_DQ05	AE32	MD5A
M_A_DQ06	AE31	MD6A
M_A_DQ07	AE30	MD7A
M_A_DQ08	AD28	DM0A
M_A_DQ09	AE32	DM1A
M_A_DQ09A	AE33	DG50A#
M_A_DQ09	AE34	DG50A#
M_A_DQ09	AE34	MD8A
M_A_DQ10	AH31	MD10A
M_A_DQ11	AG30	MD11A
M_A_DQ12	AG30	MD12A
M_A_DQ13	AG32	MD13A
M_A_DQ14	AG32	MD14A
M_A_DQ15	AJ31	MD15A
M_A_DQ16	AH34	DM1A
M_A_DQ17	AH32	DM2A
M_A_DQ18	AH33	DG51A#
M_A_DQ18	AK34	MD18A
M_A_DQ19	AL32	MD19A
M_A_DQ20	AK32	MD20A
M_A_DQ21	AG29	MD21A
M_A_DQ22	AM34	MD22A
M_A_DQ23	AL31	MD23A
M_A_DQ24	AK31	DM2A
M_A_DQ25	AK33	DG52A#
M_A_DQ25	AL34	DG52A#
M_A_DQ26	AM32	MD24A
M_A_DQ27	AP31	MD25A
M_A_DQ28	AM30	MD26A
M_A_DQ29	AK30	MD27A
M_A_DQ30	AK29	MD28A
M_A_DQ31	AK28	MD29A
M_A_DQ32	AK27	MD30A
M_A_DQ33	AM30	DM3A
M_A_DQ34	AM31	DG53A#
M_A_DQ34	AK20	MD32A
M_A_DQ35	AM19	MD33A
M_A_DQ36	AH18	MD34A
M_A_DQ37	AN20	MD35A
M_A_DQ38	AJ21	MD36A
M_A_DQ39	AP18	MD37A
M_A_DQ40	AP19	MD38A
M_A_DQ41	AP17	MD39A
M_A_DQ42	AM18	DM4A
M_A_DQ43	AK19	DG54A
M_A_DQ44	AK18	DG54A#
M_A_DQ45	AJ17	MD40A
M_A_DQ46	AK17	MD41A
M_A_DQ47	AP16	MD42A
M_A_DQ48	AP18	MD43A
M_A_DQ49	AN18	MD44A
M_A_DQ50	AN18	MD45A
M_A_DQ51	AL17	DM5A
M_A_DQ52	AM17	DG55A#
M_A_DQ53	AM16	DG55A#
M_A_DQ54	AK16	MD48A
M_A_DQ55	AN14	MD49A
M_A_DQ56	AJ15	MD50A
M_A_DQ57	AP15	MD51A
M_A_DQ58	AM16	MD52A
M_A_DQ59	AK15	MD53A
M_A_DQ60	AP14	MD54A
M_A_DQ61	AH15	MD55A
M_A_DQ62	AL15	DM6A
M_A_DQ63	AM15	DG56A#
M_A_DQ64	AL13	MD56A
M_A_DQ65	AM13	MD57A
M_A_DQ66	AK12	MD58A
M_A_DQ67	AJ14	MD59A
M_A_DQ68	AK14	MD60A
M_A_DQ69	AK12	MD61A
M_A_DQ70	AH14	MD62A
M_A_DQ71	AK13	MD63A
M_A_DQ72	AP12	DM7A
M_A_DQ73	AP13	DG57A#



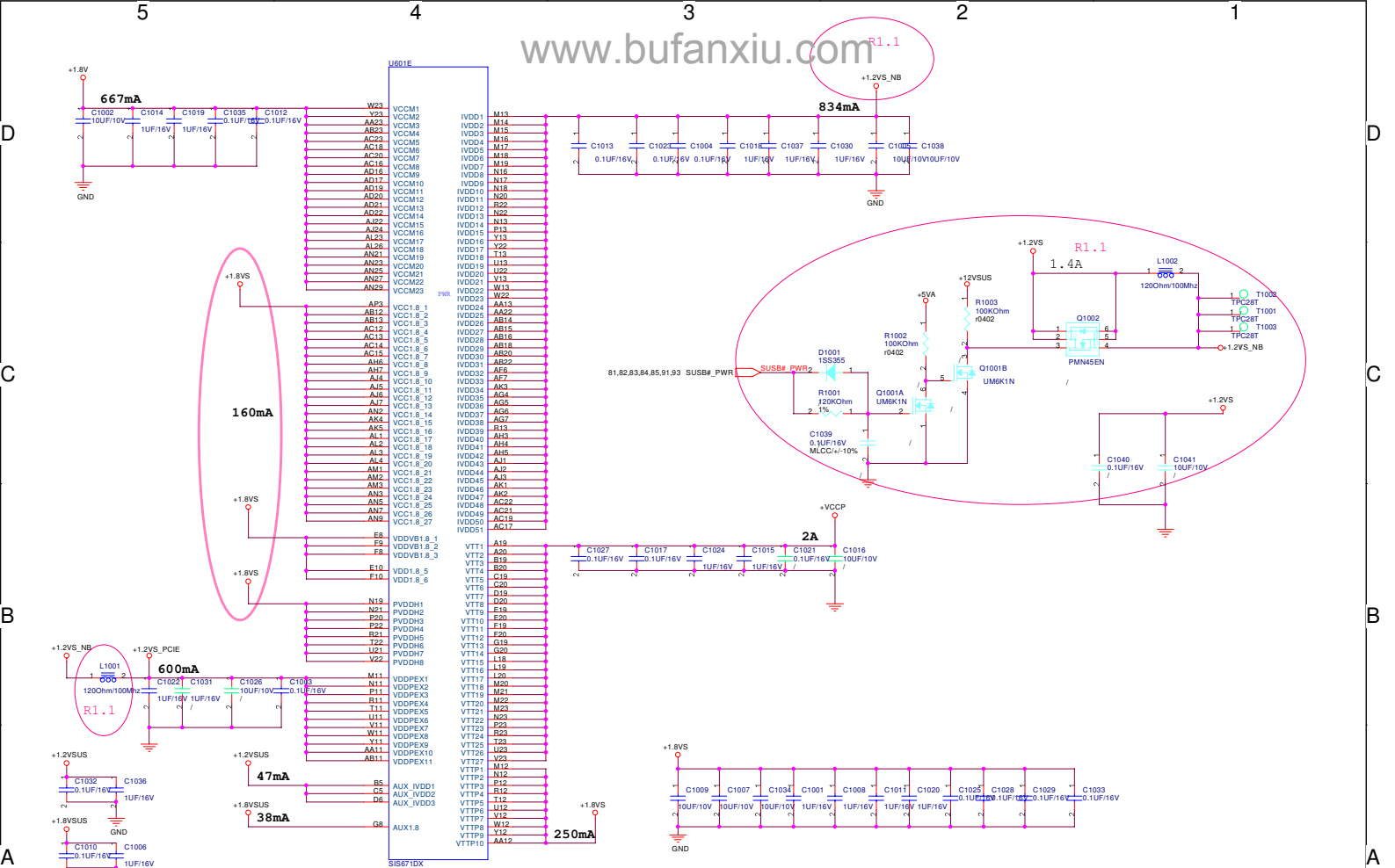
ASUS		Title : M671DX (DDR2)	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size	A3	Project Name	F5V
Date:	Rev	Sheet	8 of 94

<< Kennedy_Zhang >>



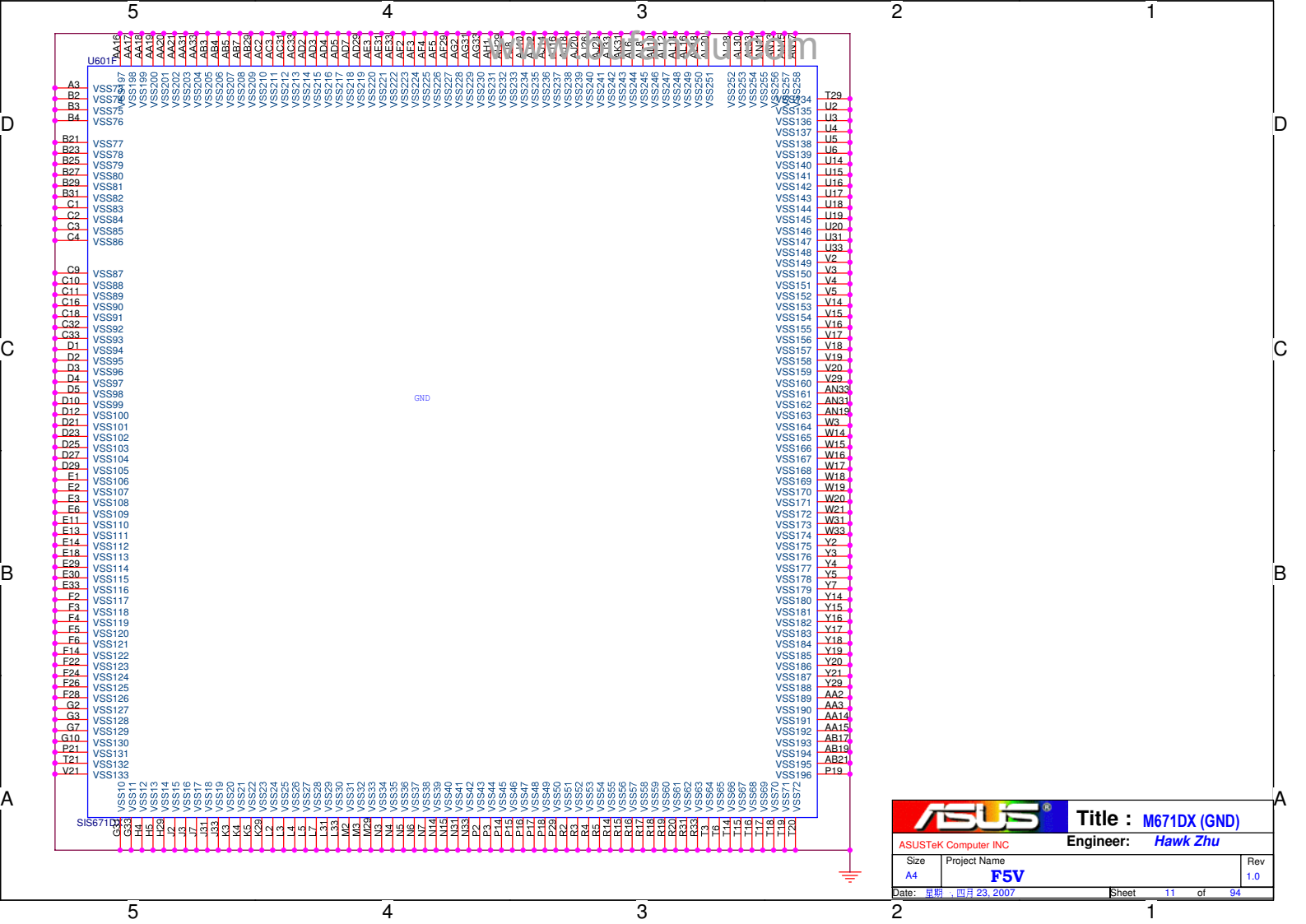
ASUS Title : M671DX (PCI-E)
 ASUSTeK Computer INC Engineer: Hawk Zhu
 Size Project Name Rev
 A4 F5V 1.0
 Date: 星期一, 四月 23, 2007 Sheet 9 of 94

<< Kennedy_Zhang >>



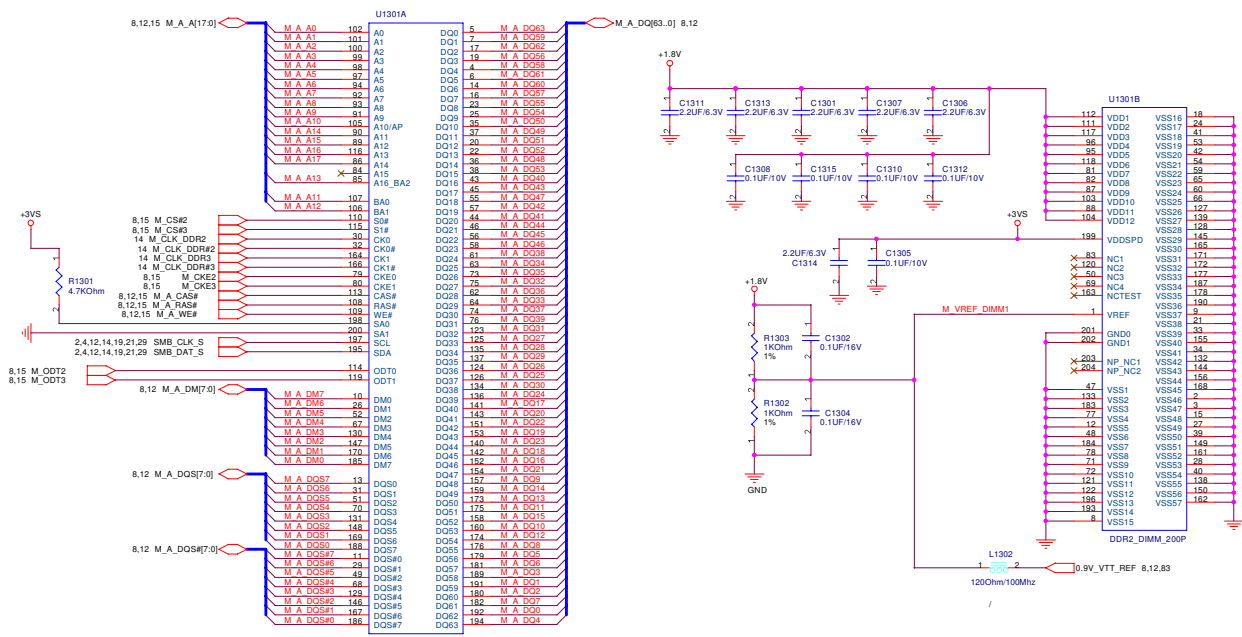
ASUS		Title : M671DX (PWR)	
ASUSTek Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A3	Project Name F5V	Rev 1.0	
Date: 2007-11-23-2007	Sheet 10	of 94	

<< Kennedy_Zhang >>



		Title : M671DX (GND)	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size A4	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet 11 of 94	

<< Kennedy_Zhang >>

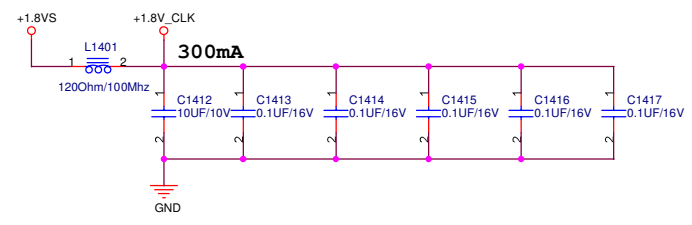
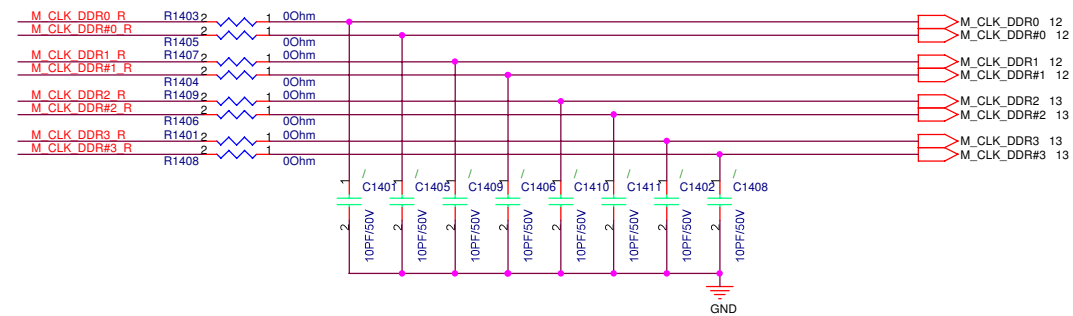
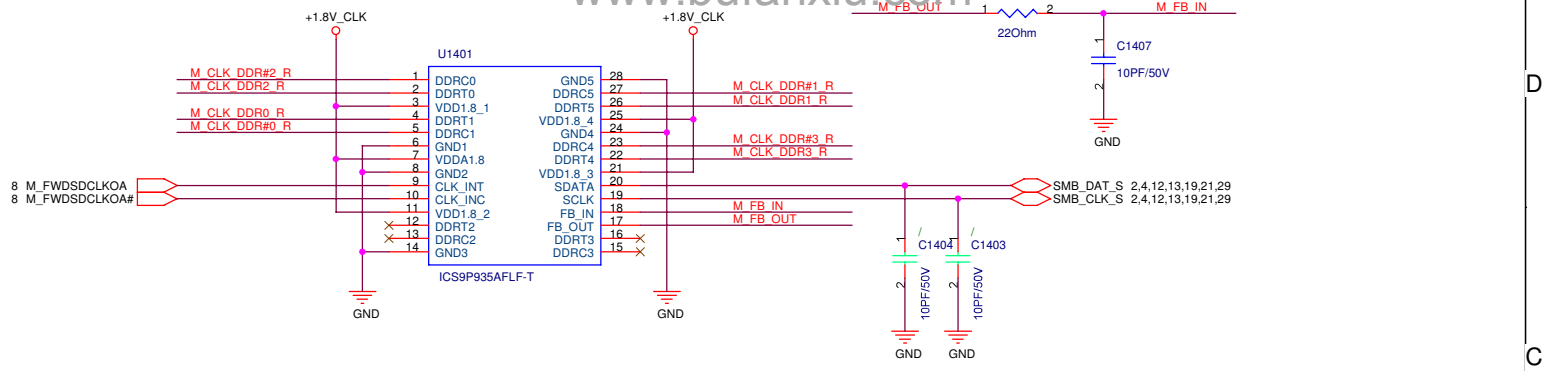


DDR2_DIMM_200P
 PN:12G025C22002

- M_CLK_DDR2
- C1303 10PF/50V
- M_CLK_DDR#2
- M_CLK_DDR3
- C1309 10PF/50V
- M_CLK_DDR#3

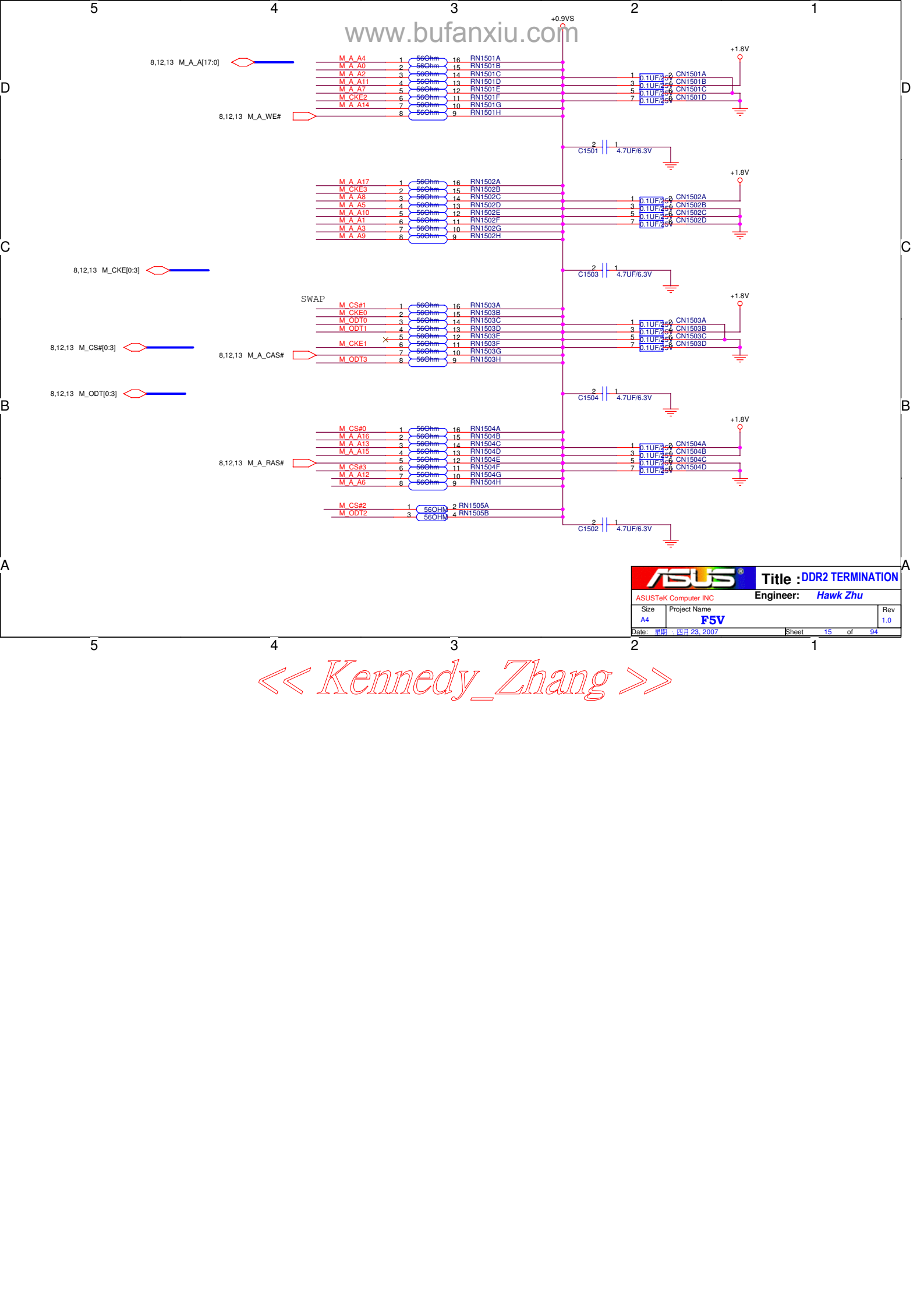
ASUS		Title : DDR2 SO-DIMM2
ASUSTek Computer INC		Engineer: Hawk Zhu
Size	Project Name	Rev
A3	FSV	1.0
Date: 08/11/23/2007	Sheet 19	of 34

<< Kennedy_Zhang >>




		Title : DDR2 BUFFER	
ASUSTeK Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A4	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet	14 of 94

<< Kennedy_Zhang >>



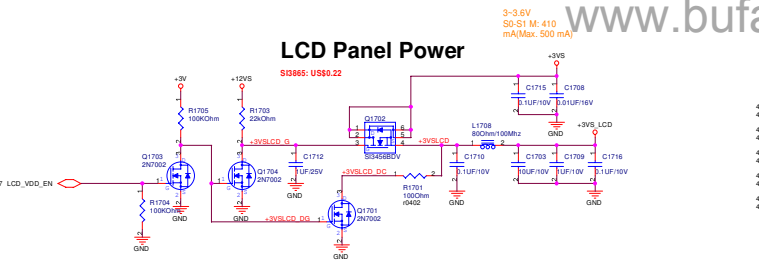
		Title :DDR2 TERMINATION	
ASUSTeK Computer INC		Engineer: <i>Hawk Zhu</i>	
Size A4	Project Name F5V	Rev 1.0	
Date: 星期四, 四月 23, 2007		Sheet 15 of 94	

<< Kennedy_Zhang >>

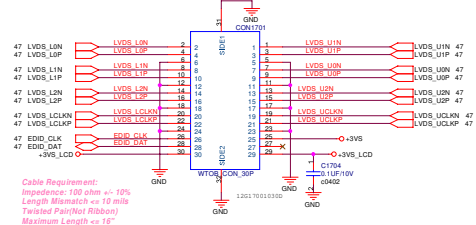
		Title : SIS	
ASUSTek Computer Inc.		Engineer: Hawk Zhu	
Size	Project Name	Rev	
C	FSV		1.0
Date: 2011-01-25 2:07		Sheet: 16	of 24

« Kennedy_Zhang »

LCD Panel Power



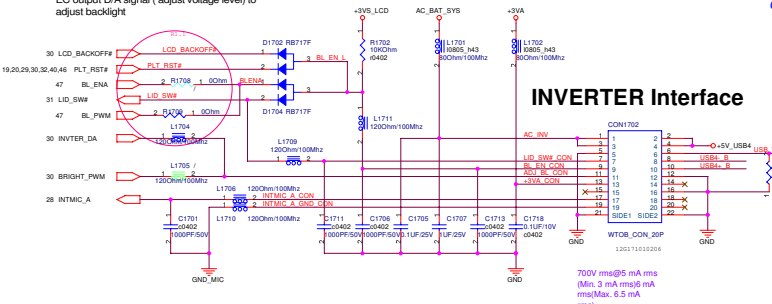
LCD LVDS Interface



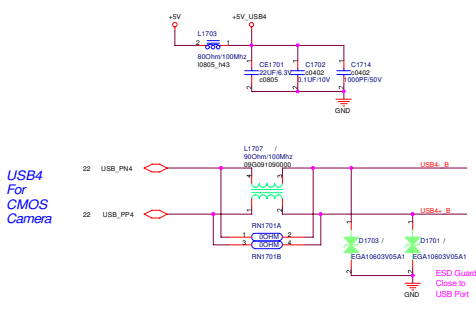
Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 18"

LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "F7+F7" button
BIOS active this pin to turn
On/Off backlight
EC
INVERTER_DA
EC output D/A signal (adjust voltage level) to
adjust backlight



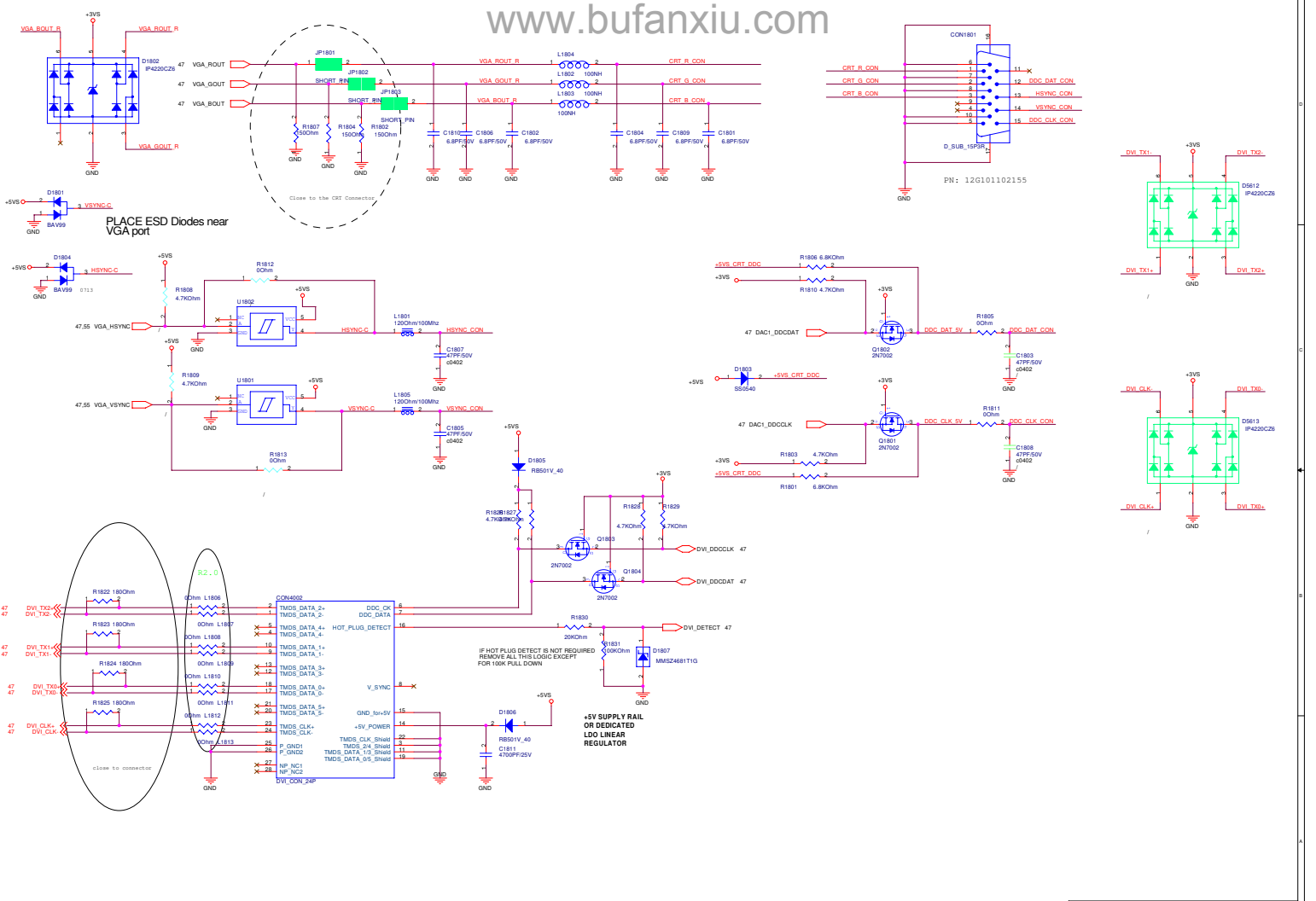
INVERTER Interface



USB4
For
CMOS
Camera

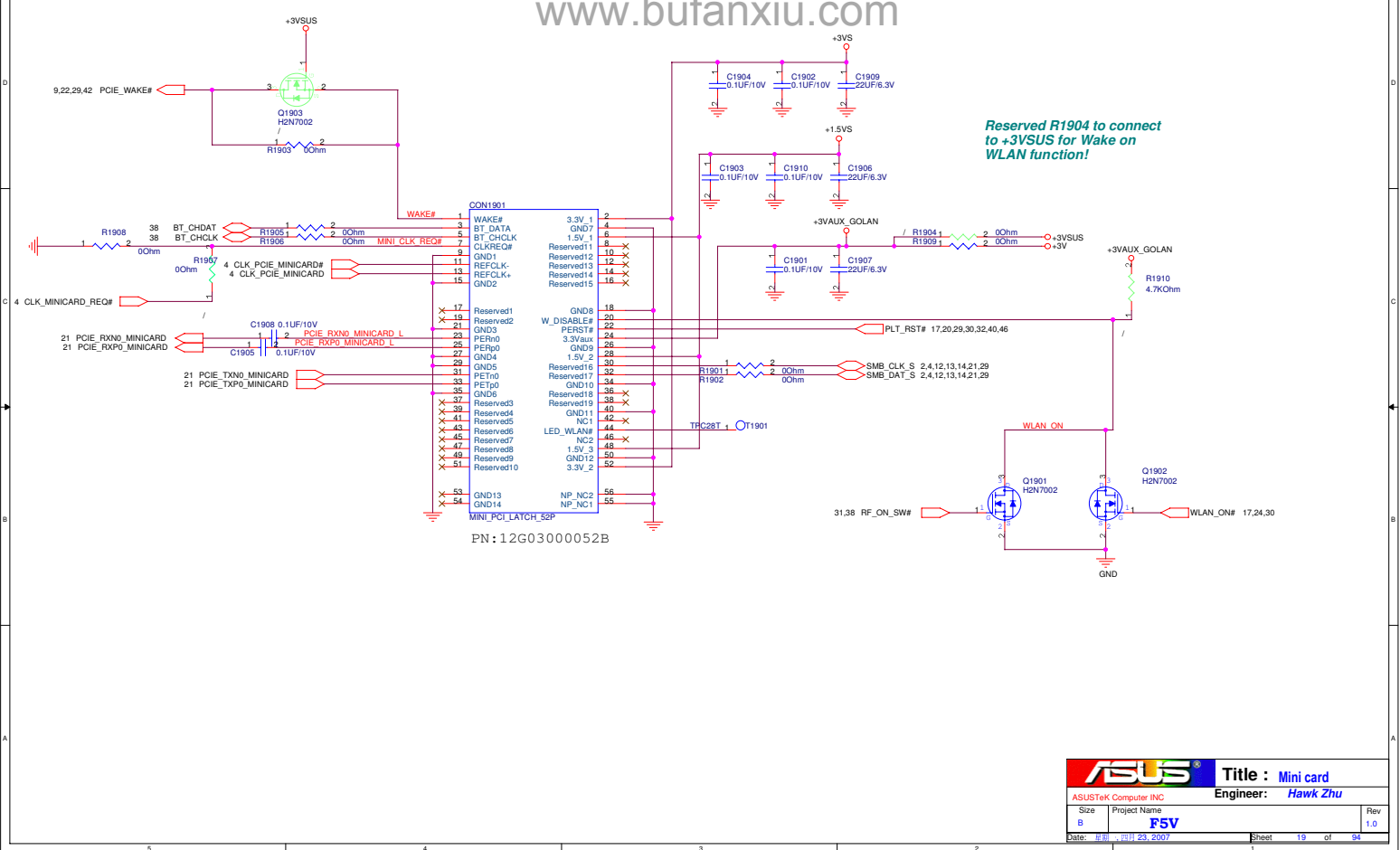
ASUS		Title : LVDS	
ASUSTek Computer Inc.		Engineer: Hawk Zhu	
BSZ	Project Name		Rev
C	FSV		1.0
Date: 2011-01-25-2007	Sheet: 17	of	24

<< Kennedy_Zhang >>



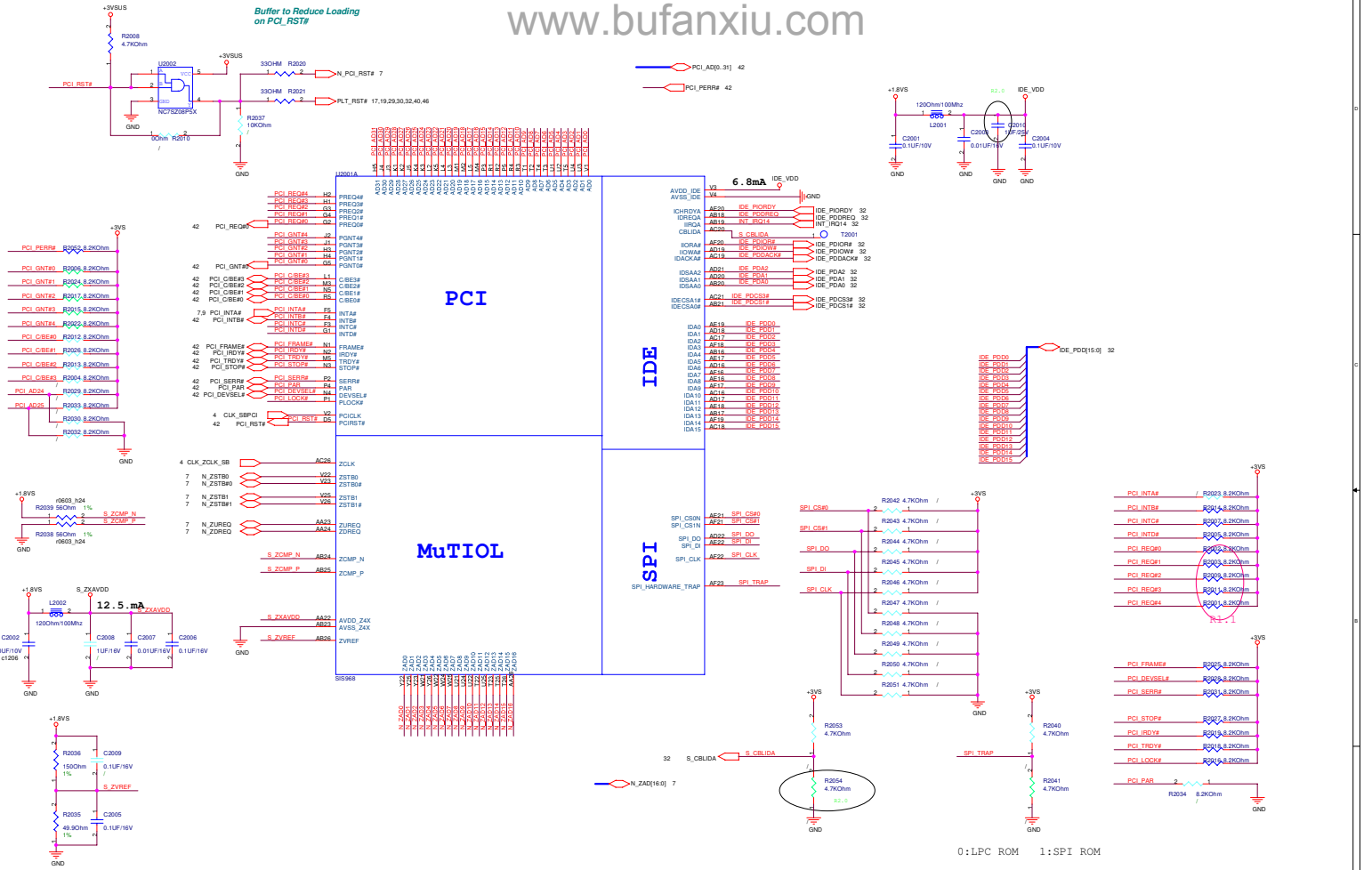
ASUS		Title : CRT&DVI	
ASUSTek Computer INC.		Engineer: Hawk Zhu	
Ver	Project Name	Rev	Rev
1.0	F5V	1.0	1.0
Date: 08-10-2007	Sheet: 18	of	24

« Kennedy_Zhang »

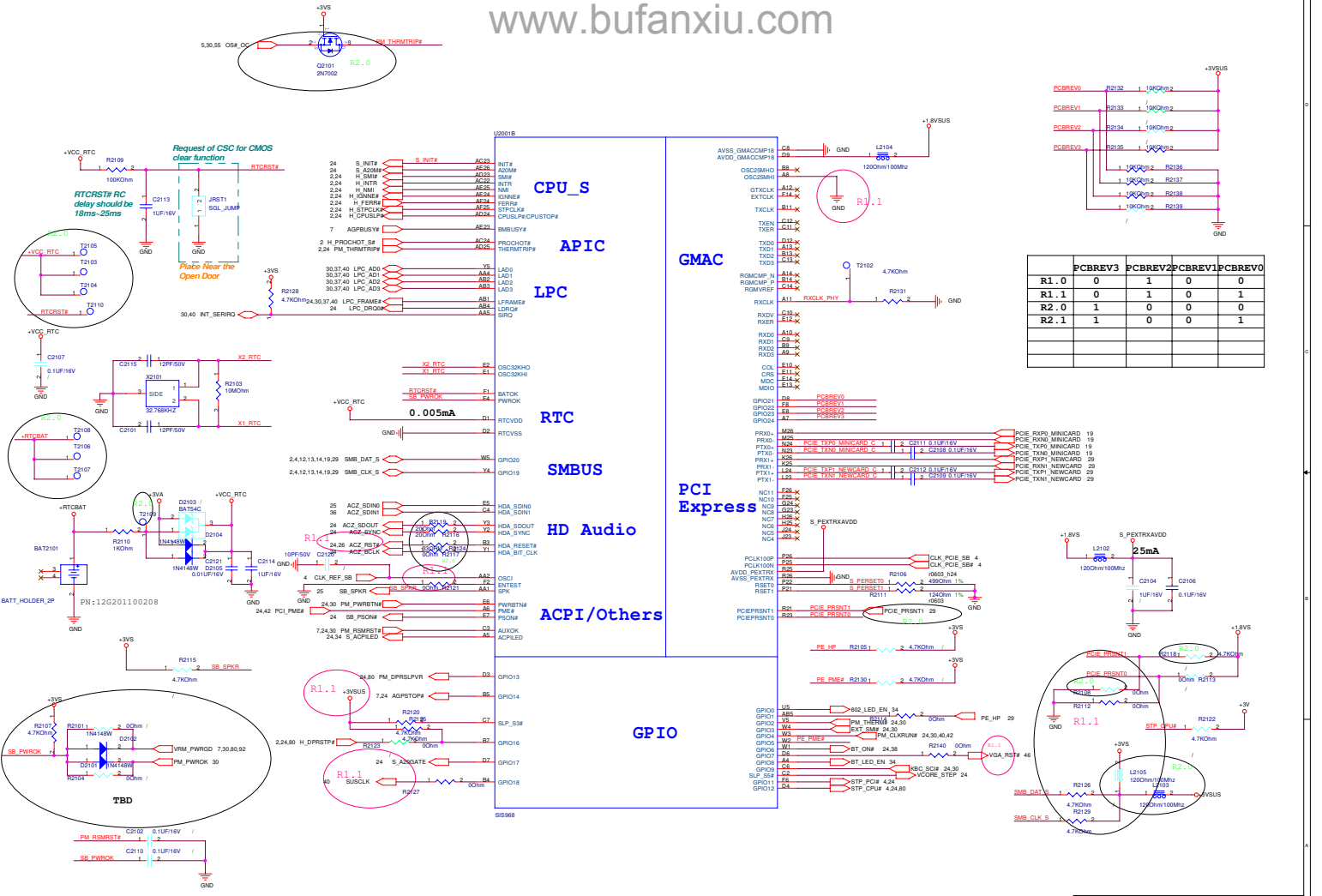


ASUS		Title : Mini card	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
B	FSV		1.0
Date: #B#	#B# 23 2007	Sheet	19 of 94

<< Kennedy_Zhang >>



« Kennedy_Zhang »



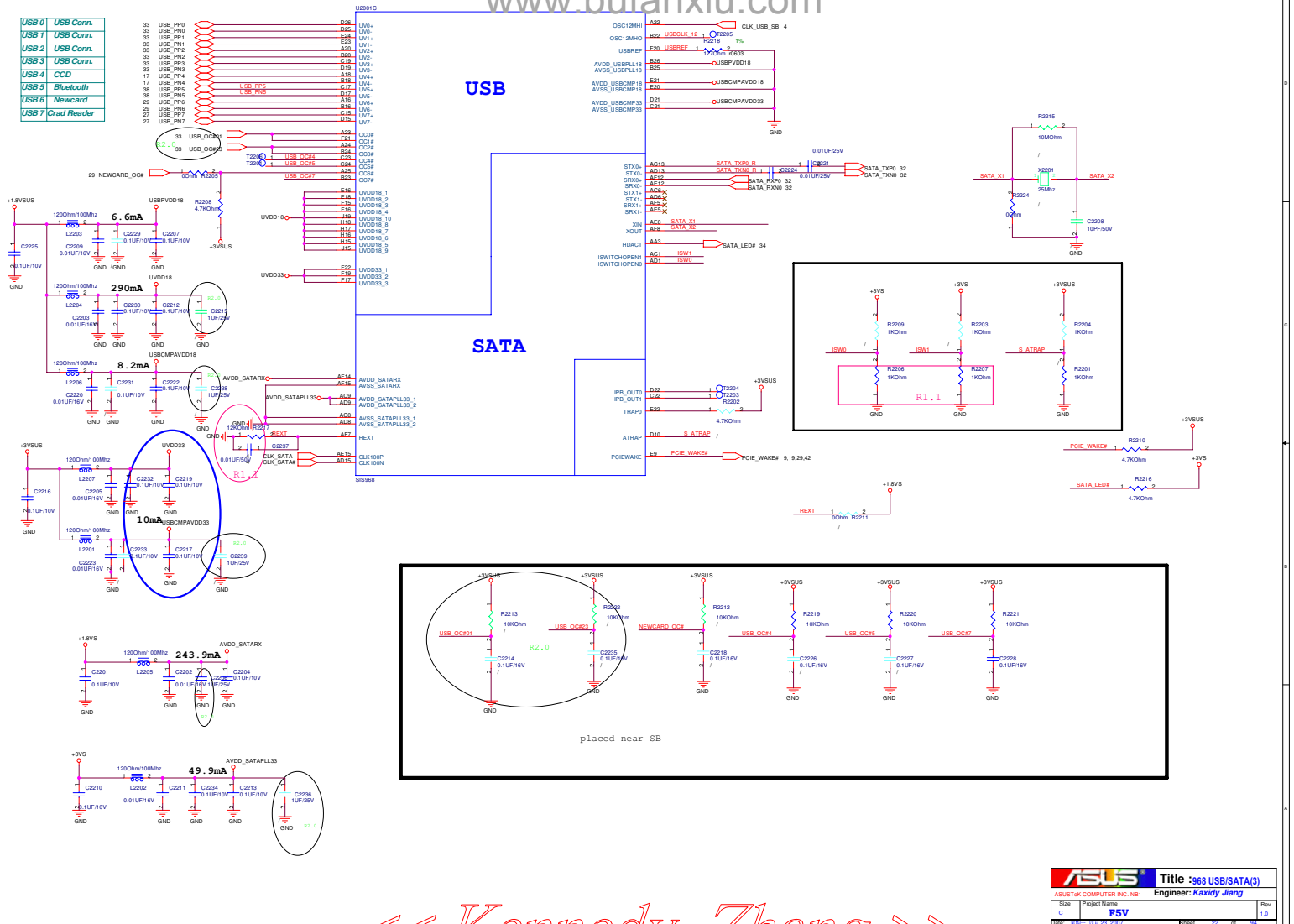
	PCBREV3	PCBREV2	PCBREV1	PCBREV0
R1.0	0	1	0	1
R2.0	1	0	0	0
R2.1	1	0	0	1

ASUS 8-Pin (AUDIO/ACPI/GPIO2) Header

ASUSTeK COMPUTER INC. NET
 Sira Project Name Engineer: Kaxidy Jjiang
F5V
 Date: 08/16/07 EScan: 21 of 24

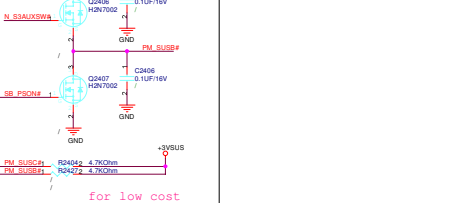
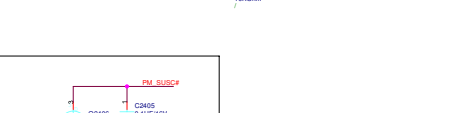
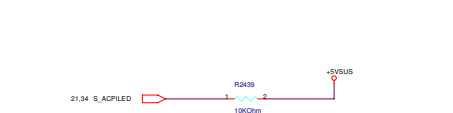
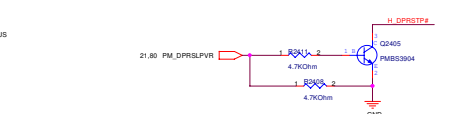
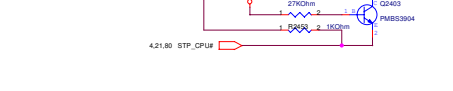
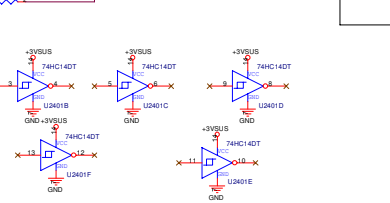
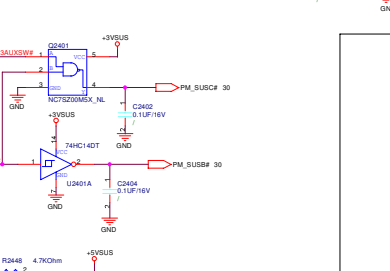
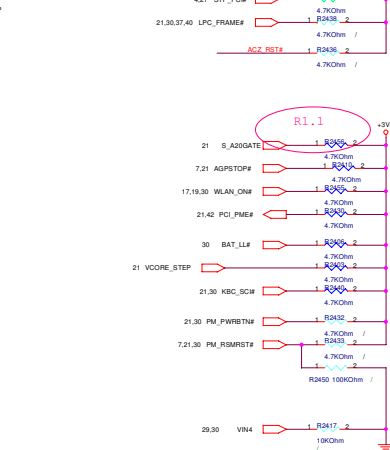
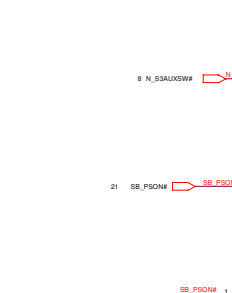
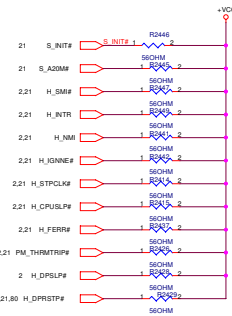
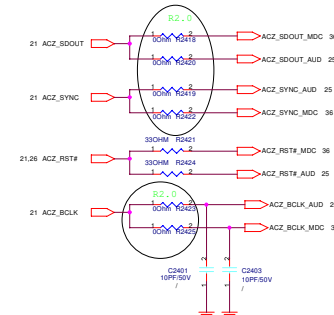
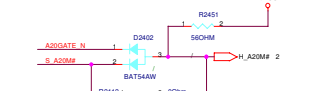
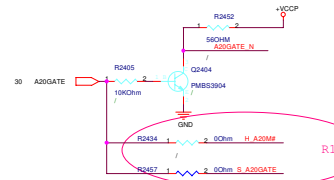
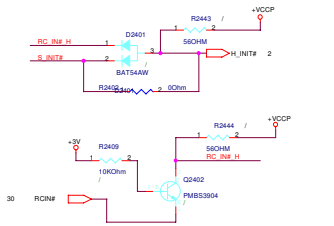
« Kennedy_Zhang »

- USB 0 USB Conn.
- USB 1 USB Conn.
- USB 2 USB Conn.
- USB 3 USB Conn.
- USB 4 CCD
- USB 5 Bluetooth
- USB 6 Newcard
- USB 7 Crad Reader



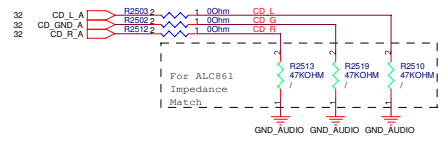
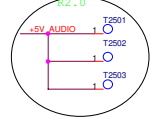
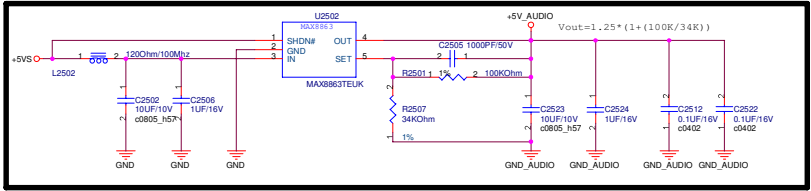
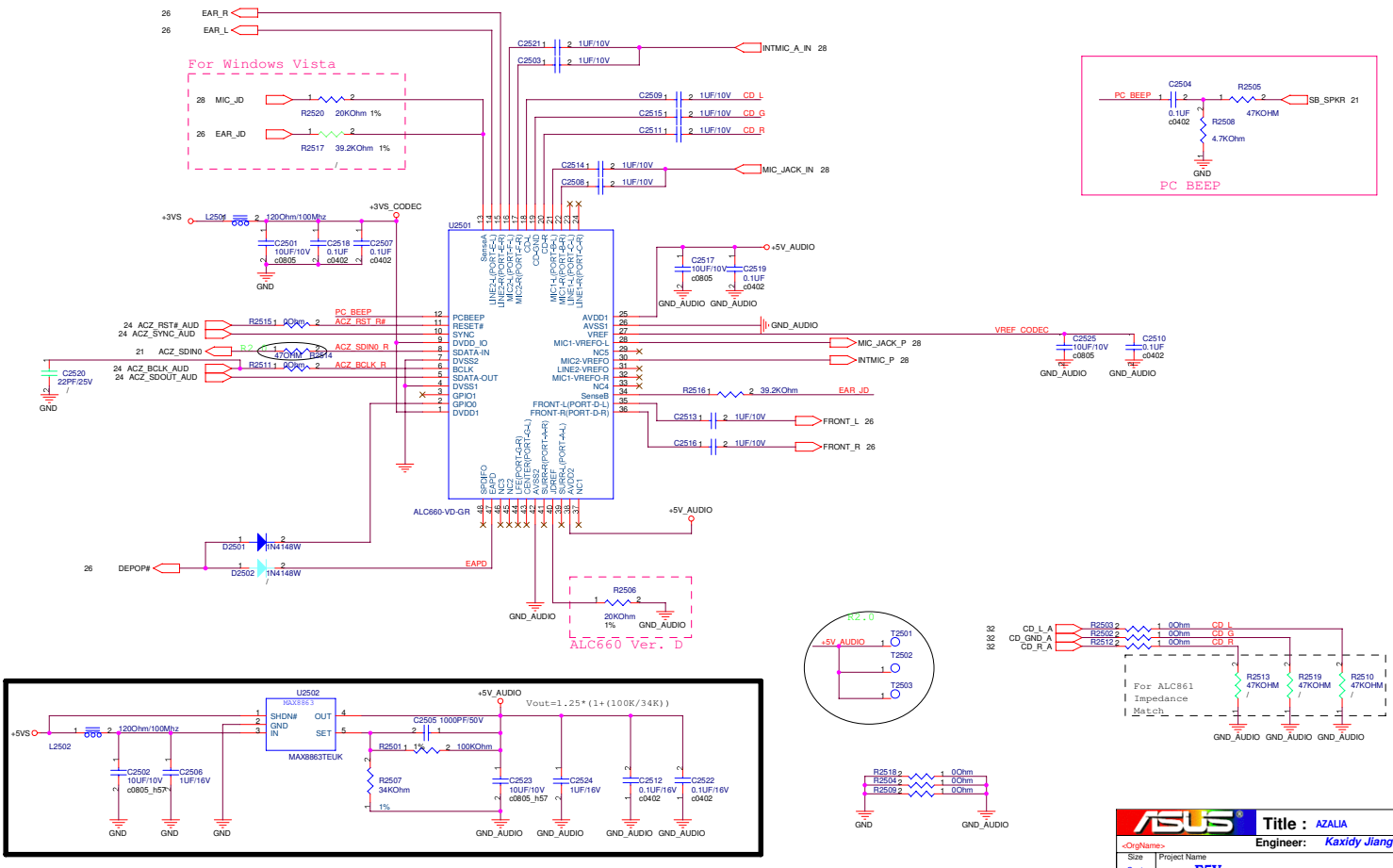
ASUS		Title : 968 USB/SATA(3)	
ASUSTeK COMPUTER INC. (CN)		Engineer: Kaxidy Jiang	
Src	Project Name	Rev	
C	FSV	1.0	
Date:	1/11/2015	Drawn:	CS

« Kennedy_Zhang »



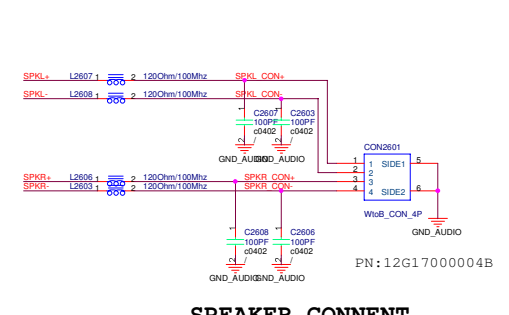
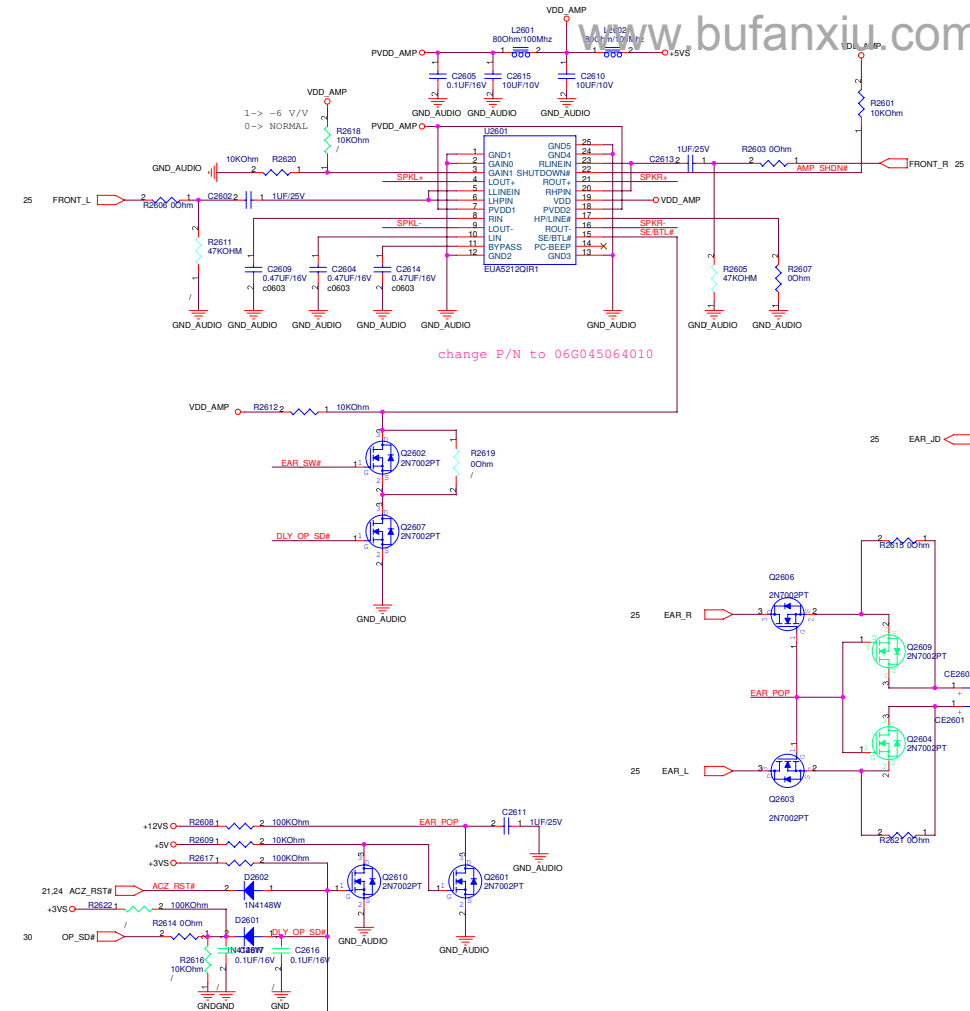
ASUS Title: 968 Strap(5)
ASUSTeK COMPUTER INC. NE1 Engineer: Kaxidy Jiang
Size: C Project Name: FSV Rev: 1.0
Date: 11/11/2011 Page: 24 of 24

« Kennedy_Zhang »

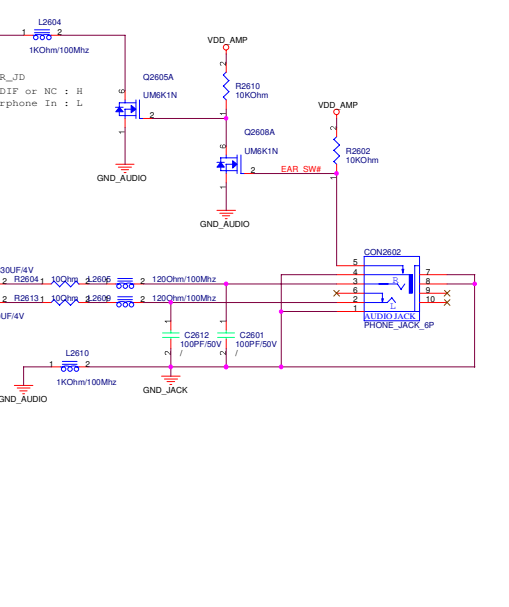
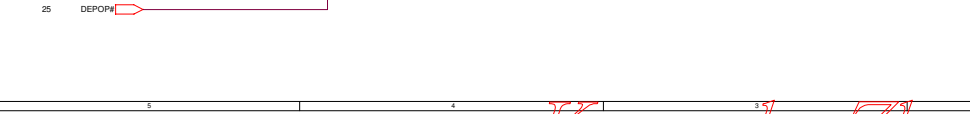


ASUS		Title : AZALIA	
<OrigName>	Project Name	Engineer:	Kaxidy Jiang
Size	Custom	Project Name	F5V
Date:	11/19/2007	Sheet	25 of 94
		Rev	1.0

<< Kennedy_Zhang >>

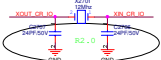
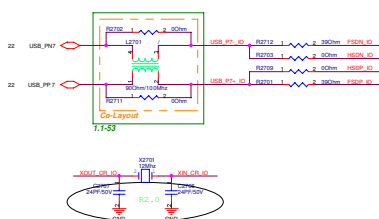


SPEAKER CONNET



ASUS		Title : AMPLIFIER 2 CHANNEL	
<OrigName>	Project Name	Engineer: Kaxidy Jiang	Rev
Size	Custom	F5V	1.0
Date: 11/13/2007	Sheet	26	of 34

<< Kennedy_Zhang >>



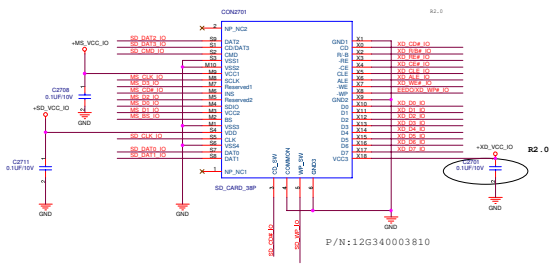
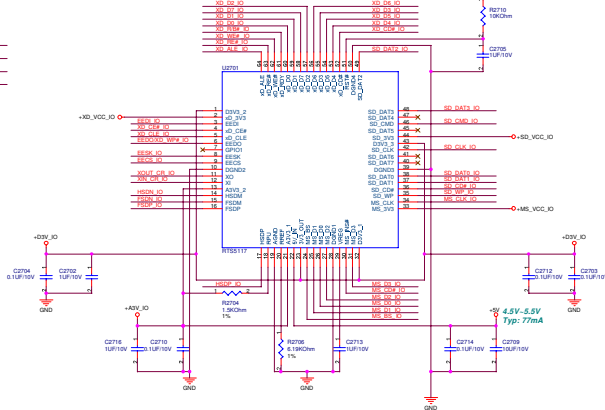
Reserve EEPROM to configure system parameters such as LUN Settings, LED Configuration, etc

Controlled by EEPROM

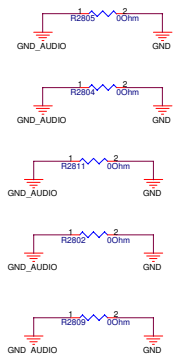
IO_R2708 PO_R2705	
SD/MMC only	No Stuff No Stuff
SD/MMC/MS/MS-Pro Combo	No Stuff 4.7K
Support CPU C3 State	4.7K No Stuff
SD/MMC/MS/MS-Pro Combo	4.7K No Stuff
Don't Support CPU C3 State	4.7K No Stuff
SD/MMC/MS/MS-Pro Combo	4.7K 4.7K
Don't Support CPU C3 State	4.7K 4.7K

IO_R41 should be present if system doesn't use EEPROM to configure LED.

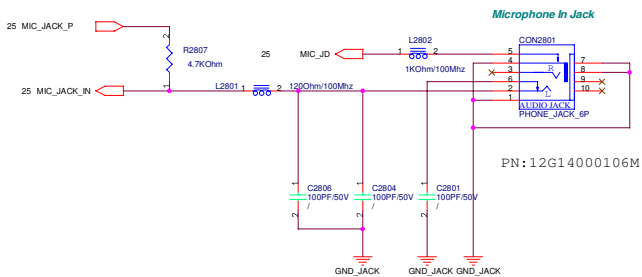
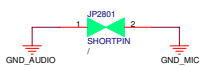
Through these pull-up resistors, EEPROM can be saved if no other requirement about other parameters.



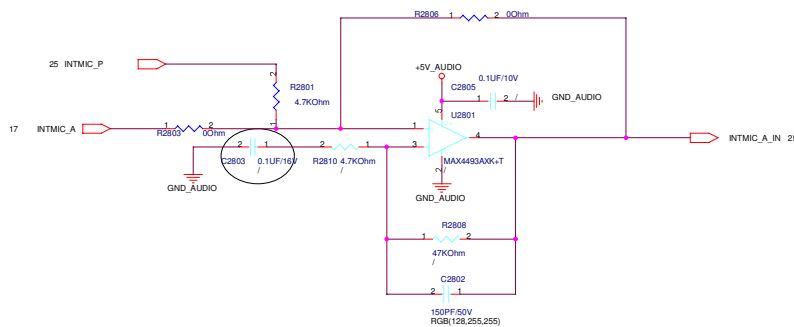
<< Kennedy_Zhang >>



INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



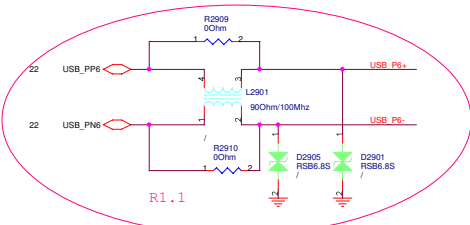
Pre-AMP For Test Function



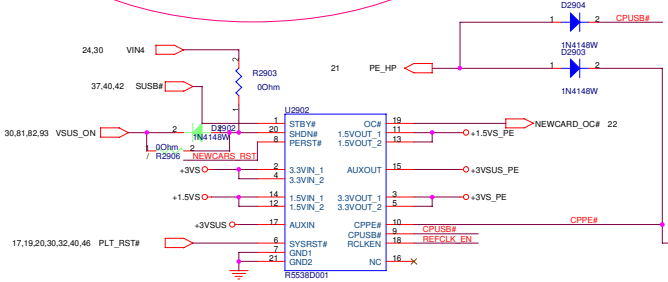
ASUS		Title : MIC.LINE-IN JACK	
-<OrigName>		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 11/19/2007		Sheet 28	of 94

<< Kennedy_Zhang >>

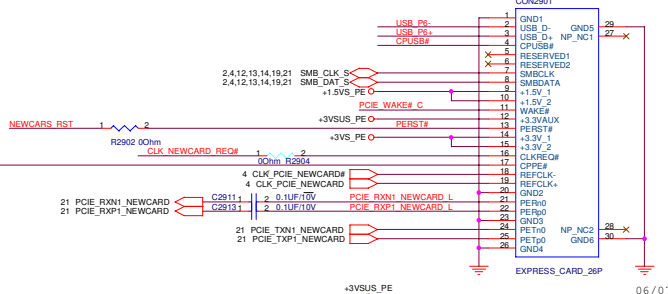
FOR SWAP



R1.1

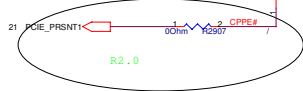
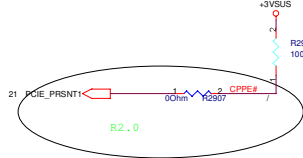
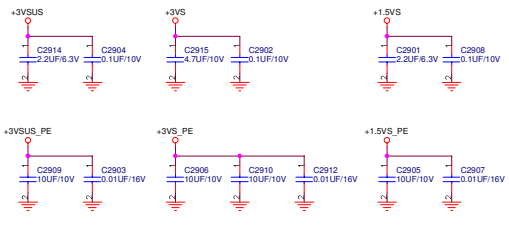
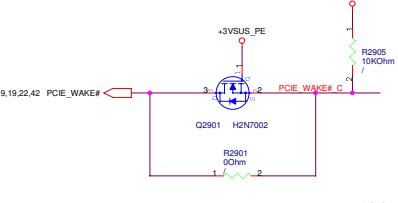
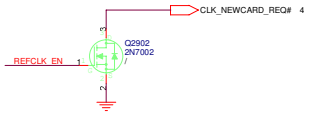


!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



PN:12G161300261 06/07

PN:12G21C102604

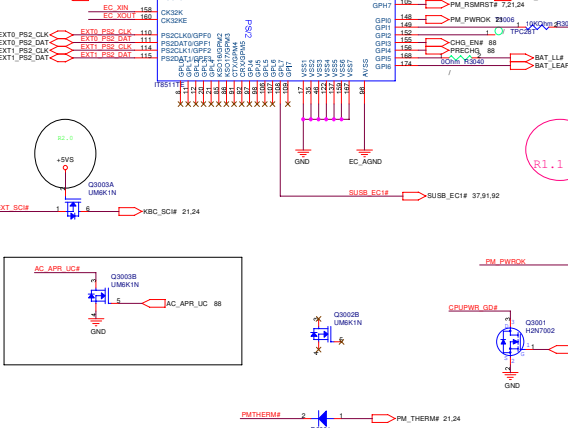
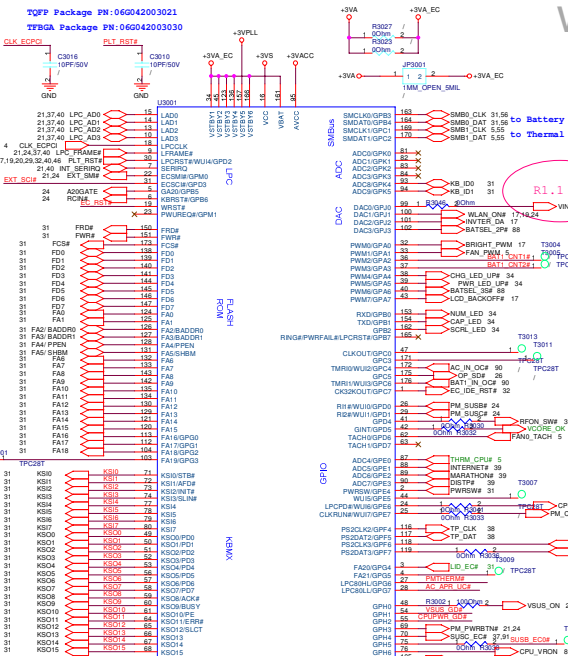


<Variant Name>

ASUS		Title : NEWCARD	
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/11/2007	Sheet	29	of 34

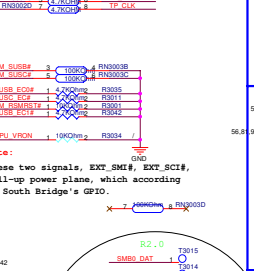
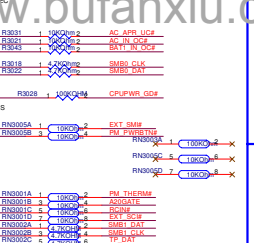
<< Kennedy_Zhang >>

For IT8510 Core IC



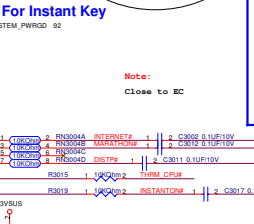
www.butanfaniu.com

For Pill-up/Pull-down



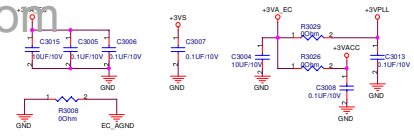
Note: These two signals, EXT_SMI#, EXT_SCI#, pull-up power plane, which according to South Bridge's GP0.

For Instant Key

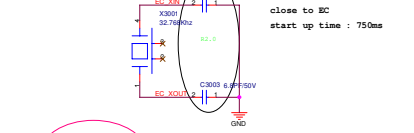


Note: Close to EC

For IT8510 Power

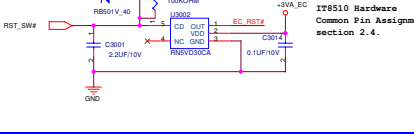


For Xtal



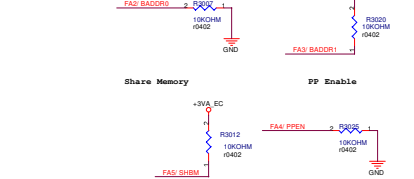
Note: Load=12.5PF close to EC start up time : 750ms

For EC reset

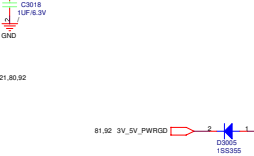


Note: The reset timing of IT8510 : Refer to IT8510 Hardware Common Pin Assignment section 2.4.

For EC Hardware Strap



For Pull-up/Pull-down



Note: Close to EC

« Kennedy_Zhang »

For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
don't connect to Battery
Connector.

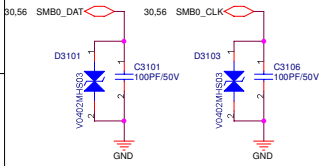
Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
must connect to Battery
Connector.

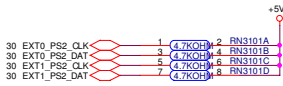
Note:

When we plug in or plug out the
battery, it may cause a spike to
damage the EC and gas gauge. It
needed to add these varistors to
protect those pins.

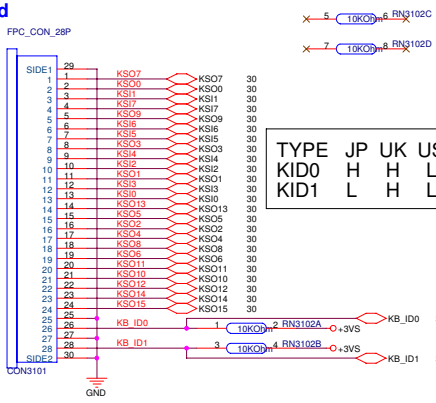
close to connector



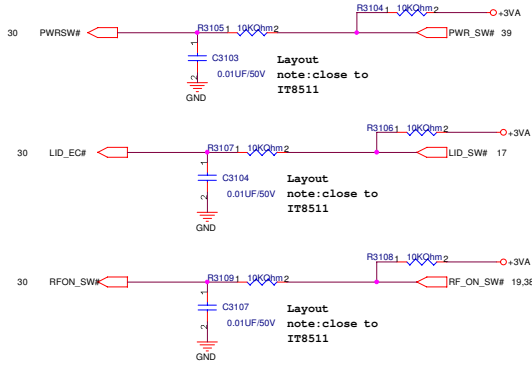
For External PS/2 I/F



For Keyboard



For Switch



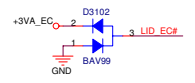
Note:

PWR SWITCH

This LID_EC# is a signal
from inverter board, it is
easy to cause high voltage
damage when plugging
inverter board connector to
M/B with AC present. It
needed to add bidirectional
diode to protect this pin.

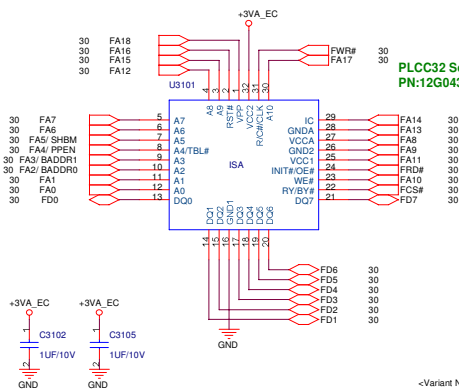
LID SWITCH

RF SWITCH



Layout
note: close to
connector

For 4M bits ISA ROM



Note:

If you use 8M bits ROM, you need
to connect FA19 to EC side.

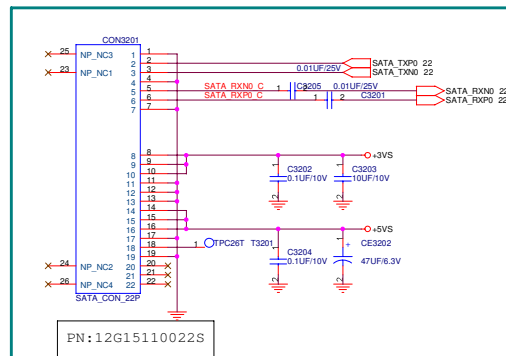
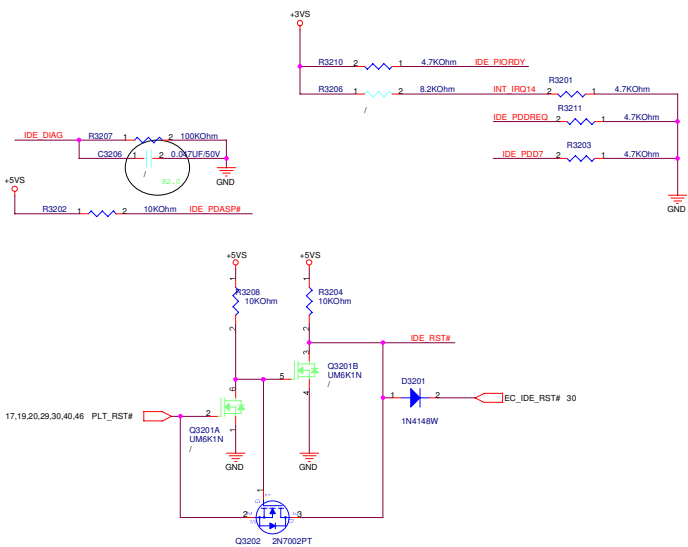
PLCC32 Socket
PN:12G04300032F

SST-PLCC32 4Mbits Flash ROM
PN:05G001027221

-Variant Name-

ASUS		Title :KB&ISA ROM	
ASUSTek COMPUTER INC. NBI		Engineer: Kaxidy Jiang	
Size	Project Name	Rev	
Custom	F5V	1.0	
Date:	2007-10-23	Sheet	31 of 94

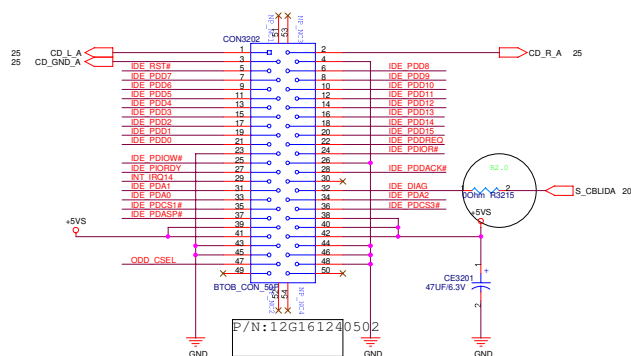
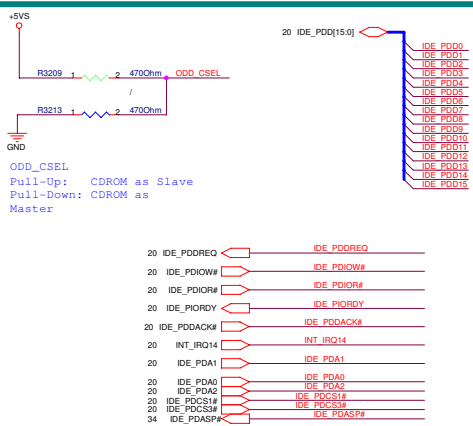
« Kennedy_Zhang »



Default

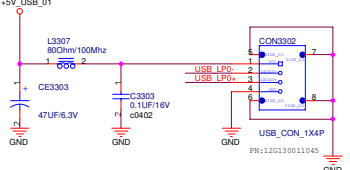
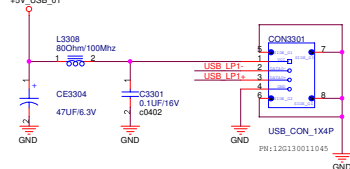
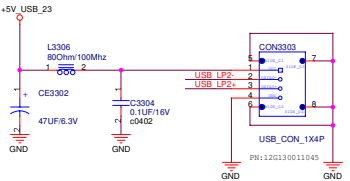
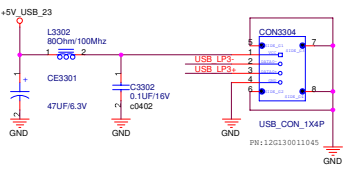
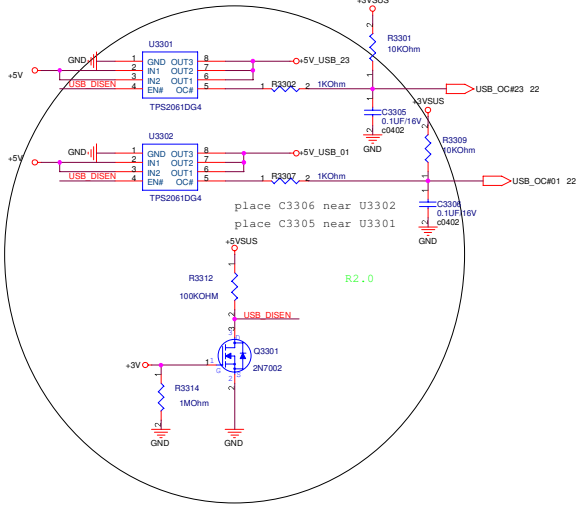
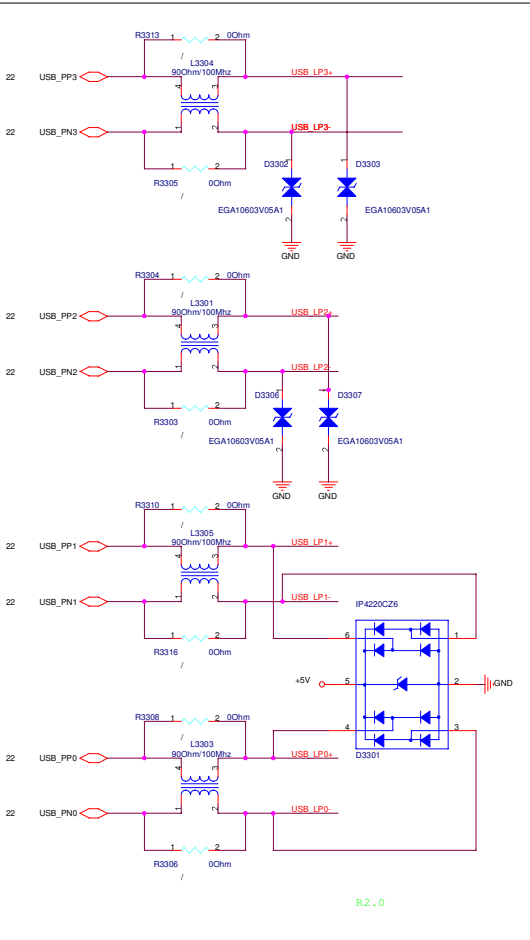
SATA

CD-ROM



ASUS
ASUSTeK COMPUTER INC. Title : HDD & CD-ROM
Engineer: Kazidy Jjiang
Project Name: FSV
Date: 11/11/2007
Sheet 10 of 94

<< Kennedy_Zhang >>

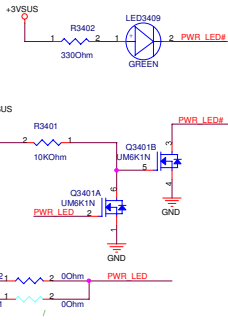


<Variant Name>

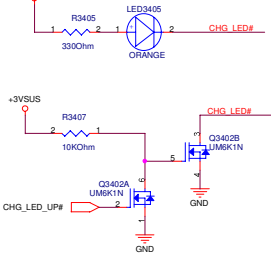
ASUS		Title : USB CONN	
ASUSTAK COMPUTER INC. NBI		Engineer: Kaxidy Jiang	
Size	Project Name		Rev
Custom	F5V		1.0
Date: #B1-10/23/2007		Sheet	33 of 84

<< Kennedy_Zhang >>

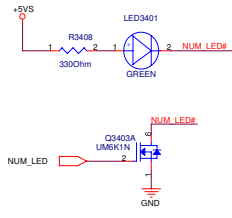
For POWER LED



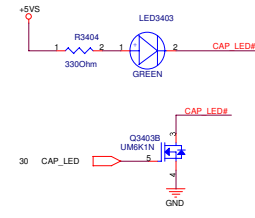
BATTERY LED



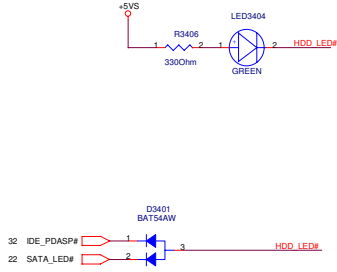
Num Lock



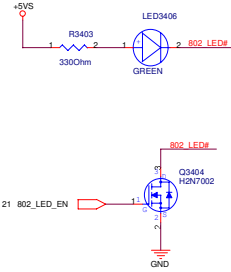
Cap Lock



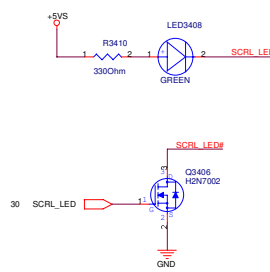
SATA/IDE LED



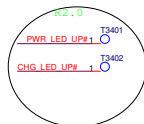
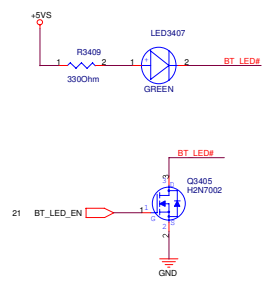
Wireless LED



Scroll Lock




BT LED



<Variant Name>

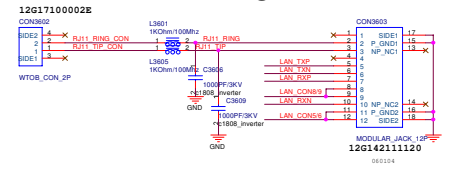
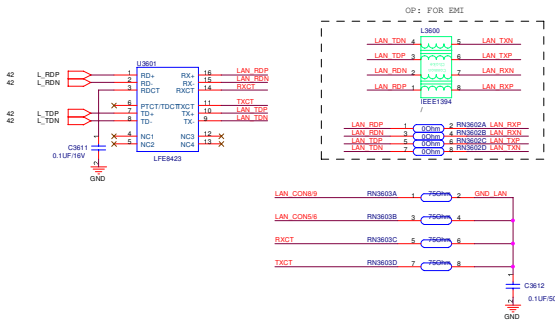
ASUS		Title : LED	
ASUSTeK COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
Custom	FSV		1.0
Date: 2007-11-23	Sheet: 34	of 34	

<< Kennedy_Zhang >>

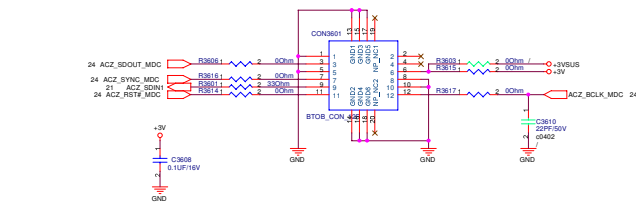
		Title : BLANK	
ASUSTeK Computer INC		Engineer: Hawk Zhu	
Size	Project Name		Rev
B	FSV		1.0
Date: # [0] [0] 23 2007		Sheet 35 of 94	

<< *Kennedy_Zhang* >>

LAN PORT

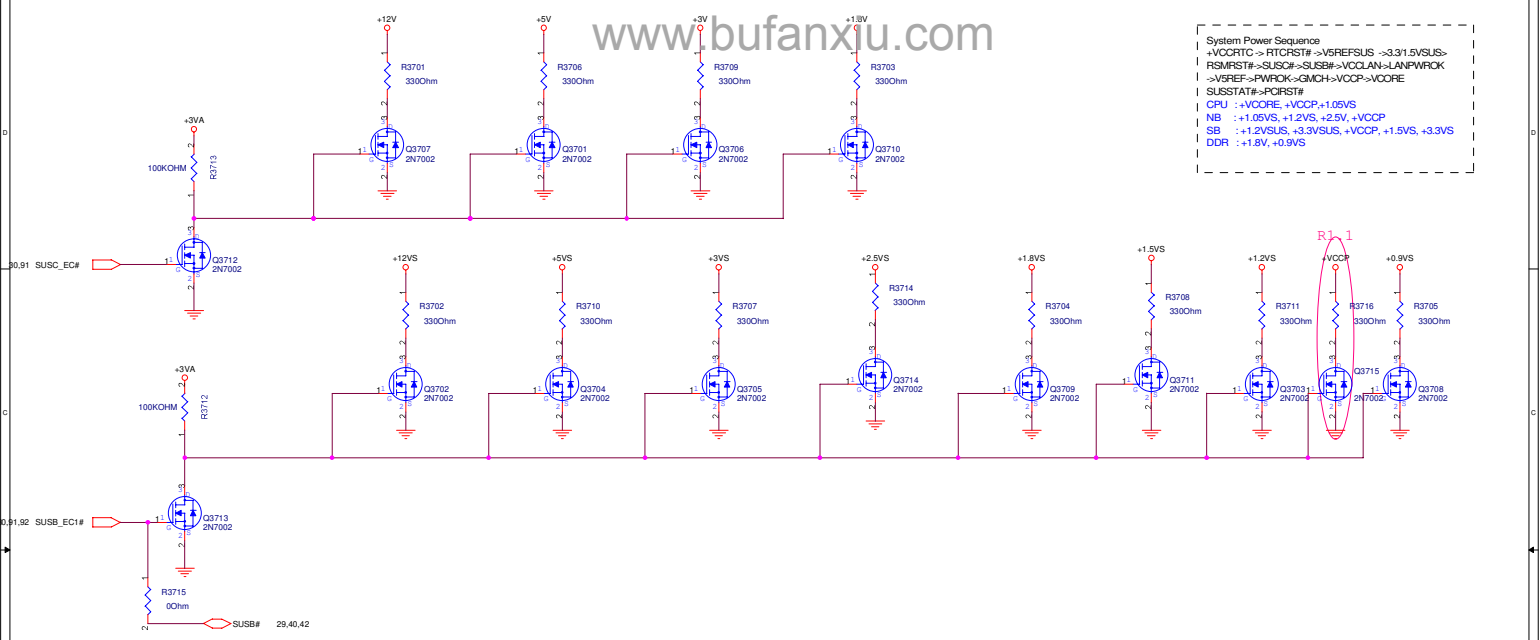


MDC

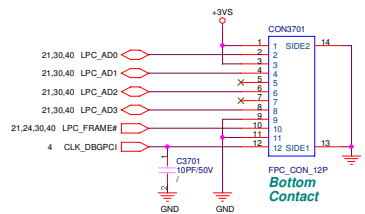


<< Kennedy_Zhang >>

System Power Sequence
 +VCCRTC->RTCRST#->V5REFSUS->+3.1.5VSUS->
 RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWCK->
 ->V5REF->PWCK->GMCH->VCCP->VCCRE
 SUSSTAT#->PCRST#
 CPU : +VCCRE +VCCP +1.05VS
 NB : +1.05VS, +1.2VS, +2.5V, +VCCP
 SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS



Debug Port



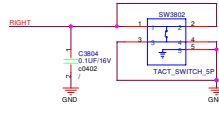
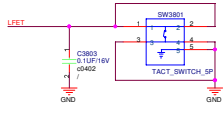
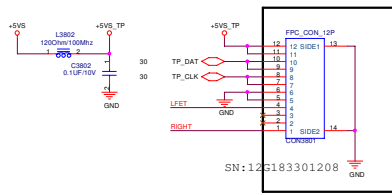
<Variant Names>

ASUS		Title : DISCHARGE CKT	
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/11/2007	Sheet	37	of 34

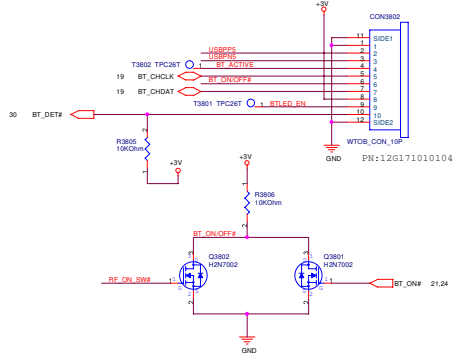
<< Kennedy_Zhang >>

Touch-Pad

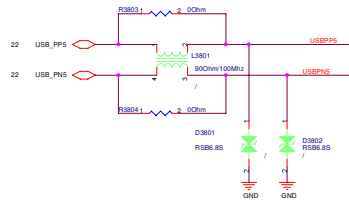
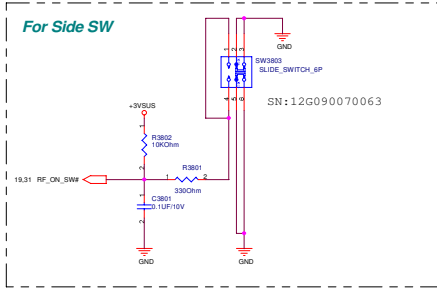
R1.1



For Bluetooth



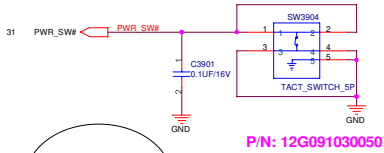
For Side SW



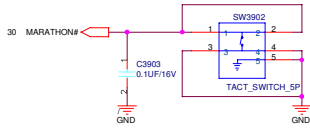
-Variant Name-		Title :BT&TP	
ASUS		Engineer:Kaidy Jiang	
Sra	Project Name	Rev	
C	F5V	1.0	
Doc No	10138-8007	ESD	38 of 34

« Kennedy_Zhang »

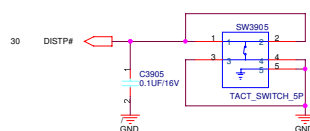
Power SW.



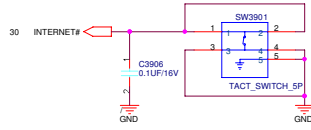
Marathon SW.



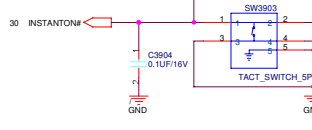
Disable Touch Pad SW.



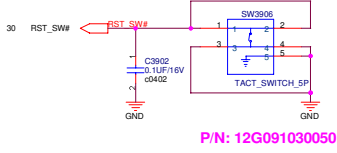
Internet SW.



IstantON SW.



RESET SW.

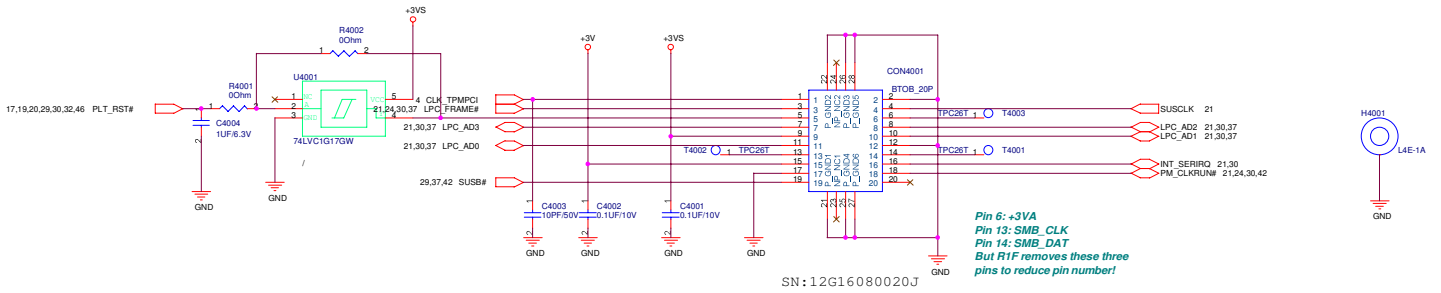


<Variant Name>

ASUS		Title : SWITCH
ASUSTeK COMPUTER INC.		Engineer: <i>Kaxidy jiang</i>
Size: Custom	Project Name: FSV	Rev: 1.0
Date: 2007.11.23	Sheet: 39	of 94

<< Kennedy_Zhang >>

For TPM Module



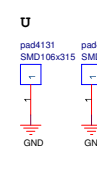
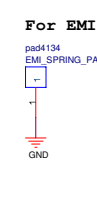
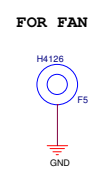
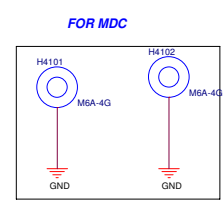
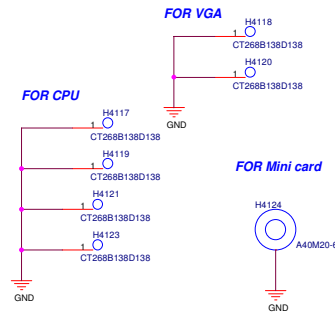
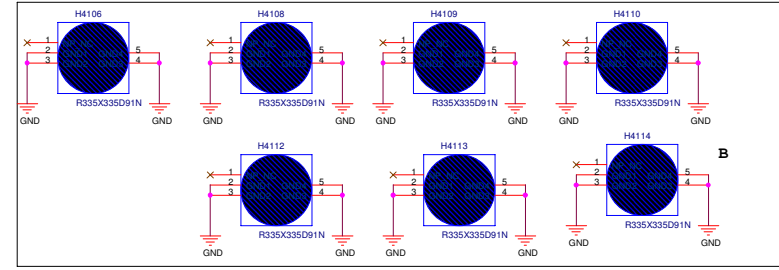
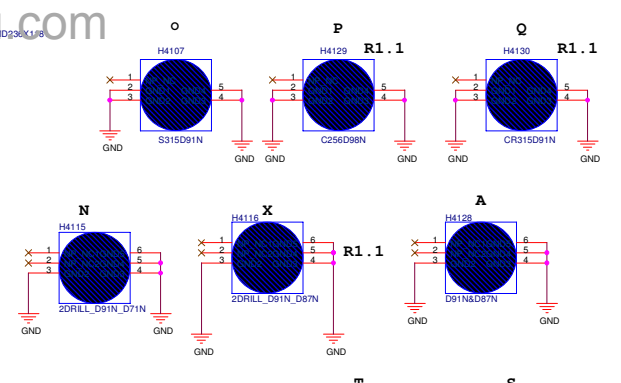
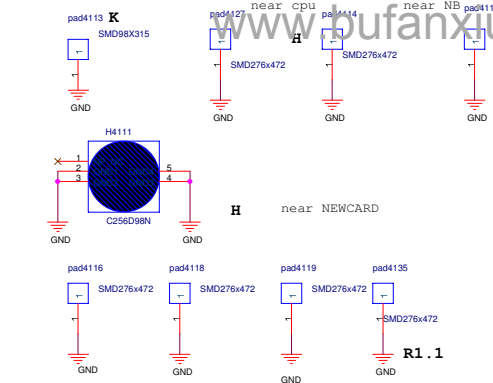
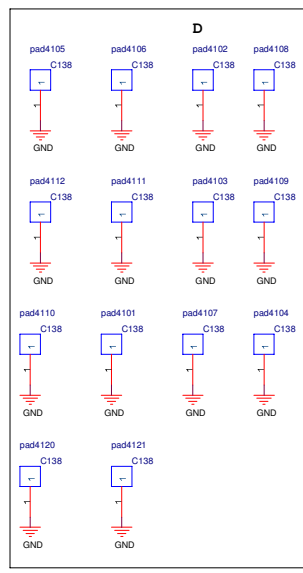
<Variant Name>

ASUS		Title : TPM
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy Jiang</i>
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 11/11/2007	Sheet: 40	of 94

<< Kennedy_Zhang >>

above ODD connector

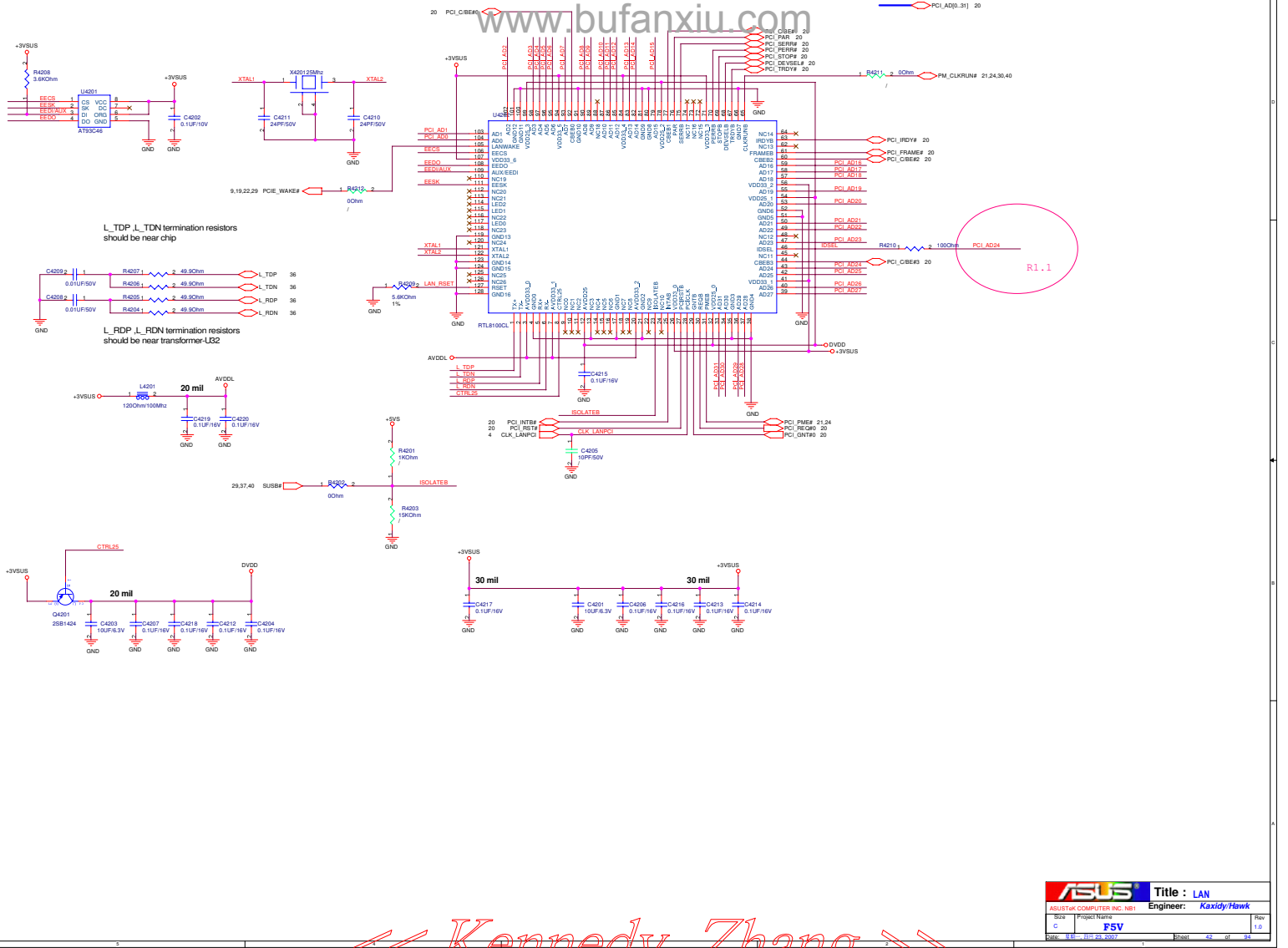
www.bufofanxju.com



R2.0 change to P/N:13GN9980M090-1 for high limit

ASUS [®]		Title : Screw hole	
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk	
Size	Project Name		Rev
B	F5V		1.0
Date: # [] [] [] 23 2007		Sheet	41 of 94

<< Kennedy_Zhang >>




ASUS		Title : LAN	
ASUSTeK COMPUTER INC. (NET)		Engineer: KaxidyHawk	
Size	Project Name	Rev	1.0
C	FSV		
Date: 08-10-25-2007	Sheet: 41	of	48

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 43 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 44 of 94

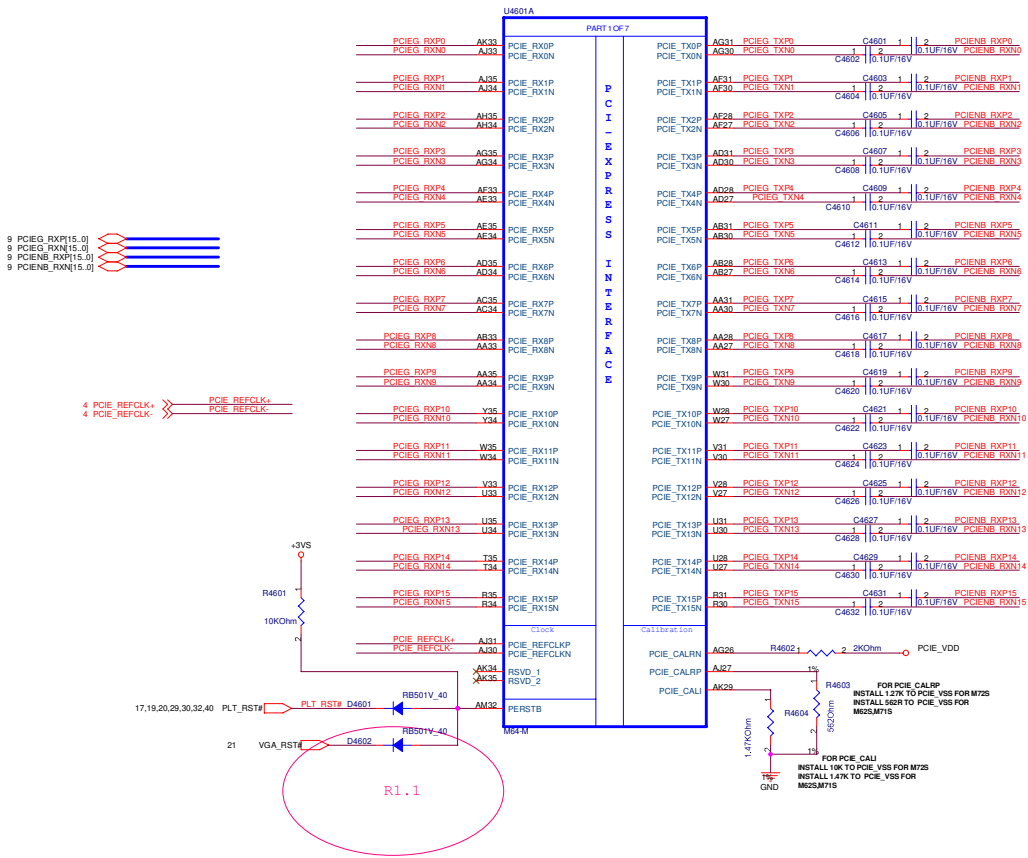
<< Kennedy_Zhang >>

D
C
B
A

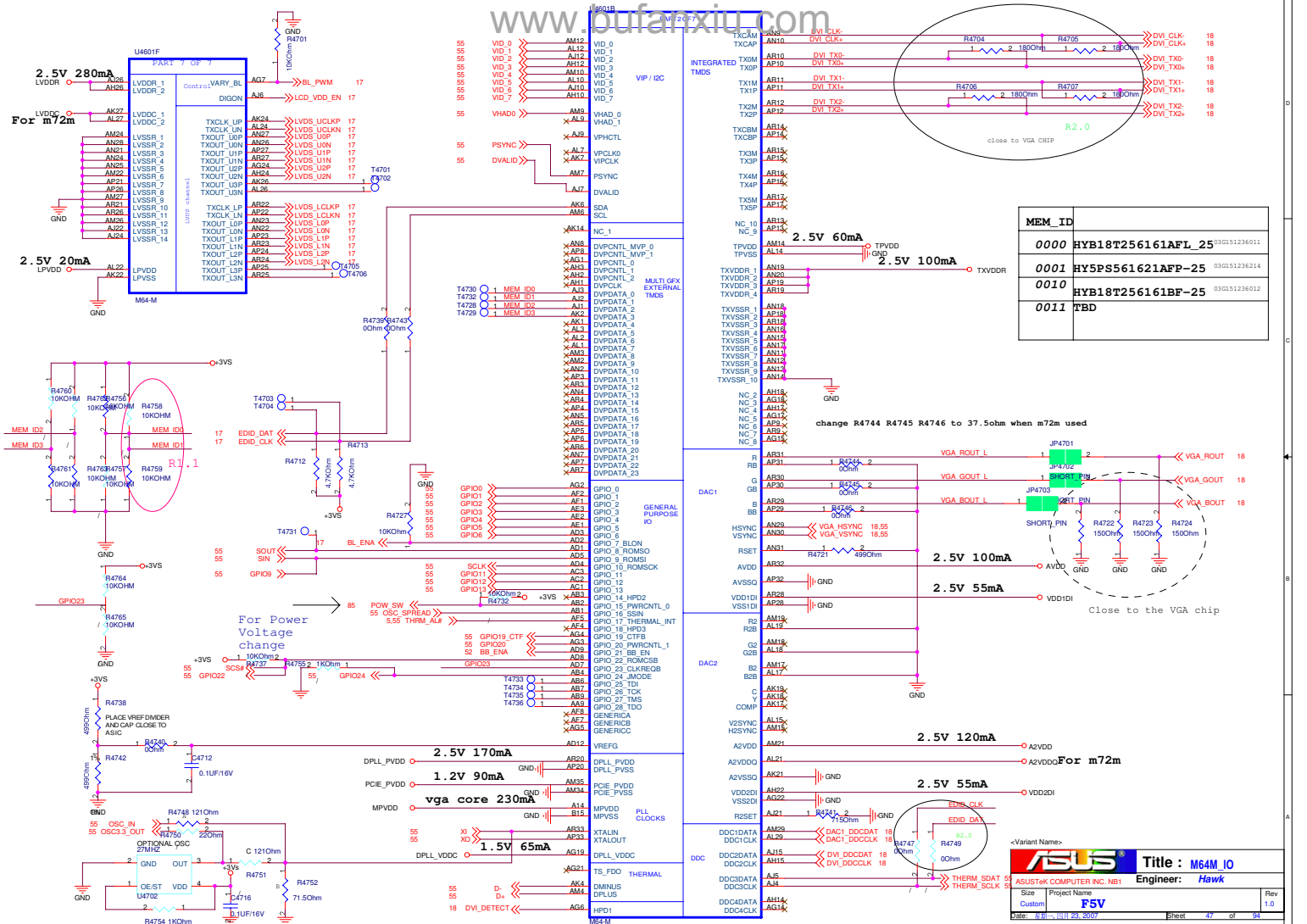
D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 45 of 94

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

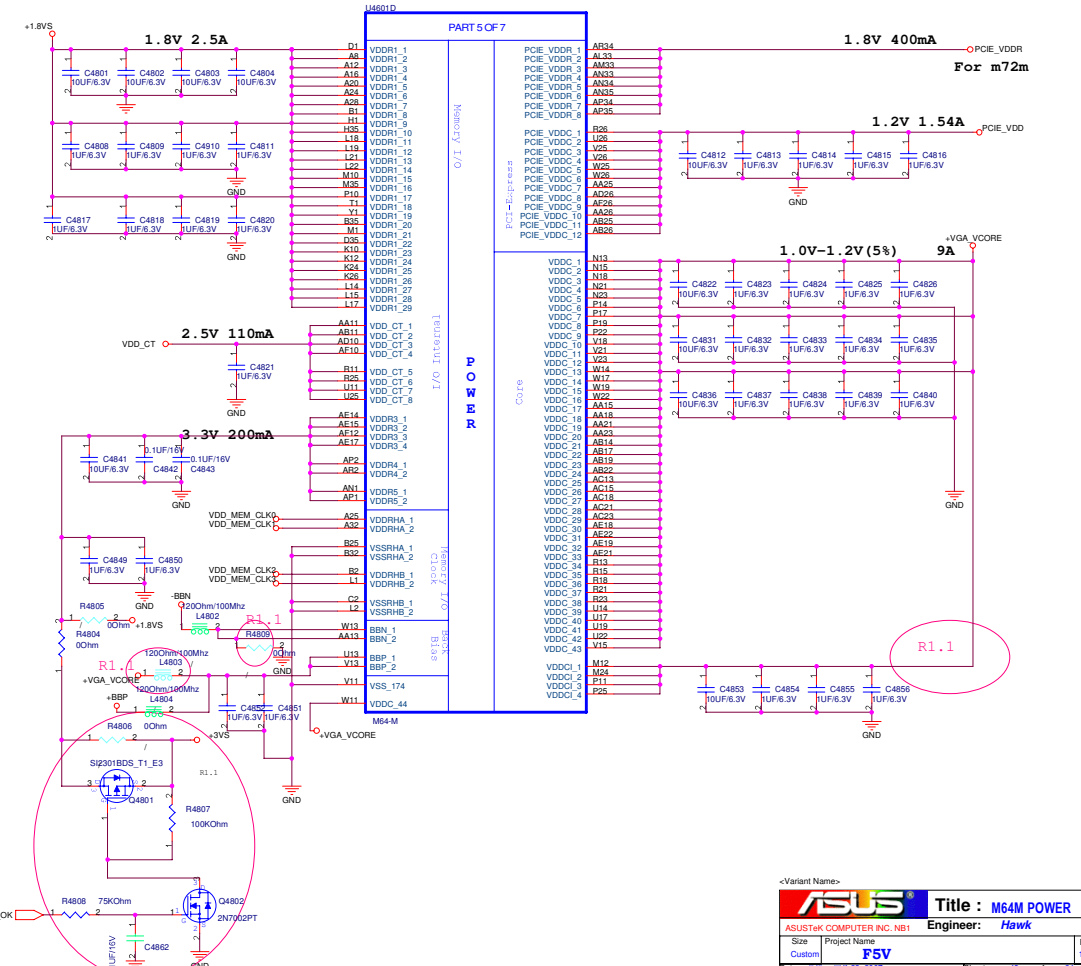


MEM ID	
0000	HYB18T256161AFL-25 03G151236011
0001	HY5PS561621AFP-25 03G151236214
0010	HYB18T256161BF-25 03G151236012
0011	TBD

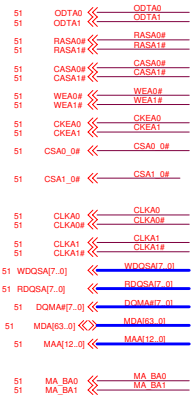
ASUS		Title : M64M IO	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 2007-11-23	Sheet	47	of 94

<< Kennedy_Zhang >>

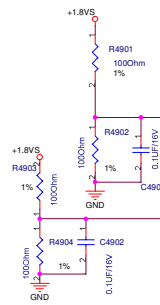
H4601E			H4601D			
Part 6 of 7			PART 5 OF 7			
P34	PCI0_VSS_1	VSS_65	L33	VDDR1_1	AR34	PCI0_VDDR_1
P35	PCI0_VSS_2	VSS_66	M3	VDDR1_2	AL33	PCI0_VDDR_2
R27	PCI0_VSS_3	VSS_67	M8	VDDR1_3	AN33	PCI0_VDDR_3
R28	PCI0_VSS_4	VSS_68	K28	VDDR1_4	AN33	PCI0_VDDR_4
R29	PCI0_VSS_5	VSS_69	M2	VDDR1_5	AN34	PCI0_VDDR_5
R30	PCI0_VSS_6	VSS_70	N14	VDDR1_6	AN35	PCI0_VDDR_6
R31	PCI0_VSS_7	VSS_71	N17	VDDR1_7	AP34	PCI0_VDDR_7
R32	PCI0_VSS_8	VSS_72	N19	VDDR1_8	AP34	PCI0_VDDR_8
L29	PCI0_VSS_9	VSS_73	N22	VDDR1_9		
L30	PCI0_VSS_10	VSS_74	N25	VDDR1_10		
L31	PCI0_VSS_11	VSS_75	N3	VDDR1_11		
L32	PCI0_VSS_12	VSS_76	N6	VDDR1_12		
V34	PCI0_VSS_13	VSS_77	R5	VDDR1_13		
V35	PCI0_VSS_14	VSS_78	U8	VDDR1_14		
V36	PCI0_VSS_15	VSS_79	P13	VDDR1_15		
V37	PCI0_VSS_16	VSS_80	E14	VDDR1_16		
V38	PCI0_VSS_17	VSS_81	E15	VDDR1_17		
V39	PCI0_VSS_18	VSS_82	E23	VDDR1_18		
V40	PCI0_VSS_19	VSS_83	E24	VDDR1_19		
V41	PCI0_VSS_20	VSS_84	F29	VDDR1_20		
V42	PCI0_VSS_21	VSS_85	F30	VDDR1_21		
V43	PCI0_VSS_22	VSS_86	F30	VDDR1_22		
V44	PCI0_VSS_23	VSS_87	G8	VDDR1_23		
V45	PCI0_VSS_24	VSS_88	G9	VDDR1_24		
V46	PCI0_VSS_25	VSS_89	H10	VDDR1_25		
V47	PCI0_VSS_26	VSS_90	H11	VDDR1_26		
V48	PCI0_VSS_27	VSS_91	H14	VDDR1_27		
V49	PCI0_VSS_28	VSS_92	H17	VDDR1_28		
V50	PCI0_VSS_29	VSS_93	H22	VDDR1_29		
V51	PCI0_VSS_30	VSS_94	I3	VDDR1_30		
V52	PCI0_VSS_31	VSS_95	I4	VDDR1_31		
V53	PCI0_VSS_32	VSS_96	I5	VDDR1_32		
V54	PCI0_VSS_33	VSS_97	I6	VDDR1_33		
V55	PCI0_VSS_34	VSS_98	I7	VDDR1_34		
V56	PCI0_VSS_35	VSS_99	I8	VDDR1_35		
V57	PCI0_VSS_36	VSS_100	I9	VDDR1_36		
V58	PCI0_VSS_37	VSS_101	I10	VDDR1_37		
V59	PCI0_VSS_38	VSS_102	I11	VDDR1_38		
V60	PCI0_VSS_39	VSS_103	I12	VDDR1_39		
V61	PCI0_VSS_40	VSS_104	I13	VDDR1_40		
V62	PCI0_VSS_41	VSS_105	I14	VDDR1_41		
V63	PCI0_VSS_42	VSS_106	I15	VDDR1_42		
V64	PCI0_VSS_43	VSS_107	I16	VDDR1_43		
V65	PCI0_VSS_44	VSS_108	I17	VDDR1_44		
V66	PCI0_VSS_45	VSS_109	I18	VDDR1_45		
A2	VSS_1	VSS_110	AK12	VDDR1_46		
A3	VSS_2	VSS_111	AK12	VDDR1_47		
A4	VSS_3	VSS_112	AK12	VDDR1_48		
A5	VSS_4	VSS_113	AK12	VDDR1_49		
A6	VSS_5	VSS_114	AK12	VDDR1_50		
A7	VSS_6	VSS_115	AK12	VDDR1_51		
A8	VSS_7	VSS_116	AK12	VDDR1_52		
A9	VSS_8	VSS_117	AK12	VDDR1_53		
A10	VSS_9	VSS_118	AK12	VDDR1_54		
A11	VSS_10	VSS_119	AK12	VDDR1_55		
A12	VSS_11	VSS_120	AK12	VDDR1_56		
A13	VSS_12	VSS_121	AK12	VDDR1_57		
A14	VSS_13	VSS_122	AK12	VDDR1_58		
A15	VSS_14	VSS_123	AK12	VDDR1_59		
A16	VSS_15	VSS_124	AK12	VDDR1_60		
A17	VSS_16	VSS_125	AK12	VDDR1_61		
A18	VSS_17	VSS_126	AK12	VDDR1_62		
A19	VSS_18	VSS_127	AK12	VDDR1_63		
A20	VSS_19	VSS_128	AK12	VDDR1_64		
A21	VSS_20	VSS_129	AK12	VDDR1_65		
A22	VSS_21	VSS_130	AK12	VDDR1_66		
A23	VSS_22	VSS_131	AK12	VDDR1_67		
A24	VSS_23	VSS_132	AK12	VDDR1_68		
A25	VSS_24	VSS_133	AK12	VDDR1_69		
A26	VSS_25	VSS_134	AK12	VDDR1_70		
A27	VSS_26	VSS_135	AK12	VDDR1_71		
A28	VSS_27	VSS_136	AK12	VDDR1_72		
A29	VSS_28	VSS_137	AK12	VDDR1_73		
A30	VSS_29	VSS_138	AK12	VDDR1_74		
A31	VSS_30	VSS_139	AK12	VDDR1_75		
A32	VSS_31	VSS_140	AK12	VDDR1_76		
A33	VSS_32	VSS_141	AK12	VDDR1_77		
A34	VSS_33	VSS_142	AK12	VDDR1_78		
A35	VSS_34	VSS_143	AK12	VDDR1_79		
A36	VSS_35	VSS_144	AK12	VDDR1_80		
A37	VSS_36	VSS_145	AK12	VDDR1_81		
A38	VSS_37	VSS_146	AK12	VDDR1_82		
A39	VSS_38	VSS_147	AK12	VDDR1_83		
A40	VSS_39	VSS_148	AK12	VDDR1_84		
A41	VSS_40	VSS_149	AK12	VDDR1_85		
A42	VSS_41	VSS_150	AK12	VDDR1_86		
A43	VSS_42	VSS_151	AK12	VDDR1_87		
A44	VSS_43	VSS_152	AK12	VDDR1_88		
A45	VSS_44	VSS_153	AK12	VDDR1_89		
A46	VSS_45	VSS_154	AK12	VDDR1_90		
A47	VSS_46	VSS_155	AK12	VDDR1_91		
A48	VSS_47	VSS_156	AK12	VDDR1_92		
A49	VSS_48	VSS_157	AK12	VDDR1_93		
A50	VSS_49	VSS_158	AK12	VDDR1_94		
A51	VSS_50	VSS_159	AK12	VDDR1_95		
A52	VSS_51	VSS_160	AK12	VDDR1_96		
A53	VSS_52	VSS_161	AK12	VDDR1_97		
A54	VSS_53	VSS_162	AK12	VDDR1_98		
A55	VSS_54	VSS_163	AK12	VDDR1_99		
A56	VSS_55	VSS_164	AK12	VDDR1_100		
A57	VSS_56	VSS_165	AK12	VDDR1_101		
A58	VSS_57					
A59	VSS_58					
A60	VSS_59					
A61	VSS_60					
A62	VSS_61					
A63	VSS_62					
A64	VSS_63					
A65	VSS_64					



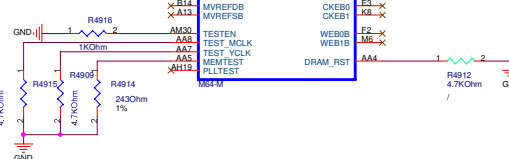
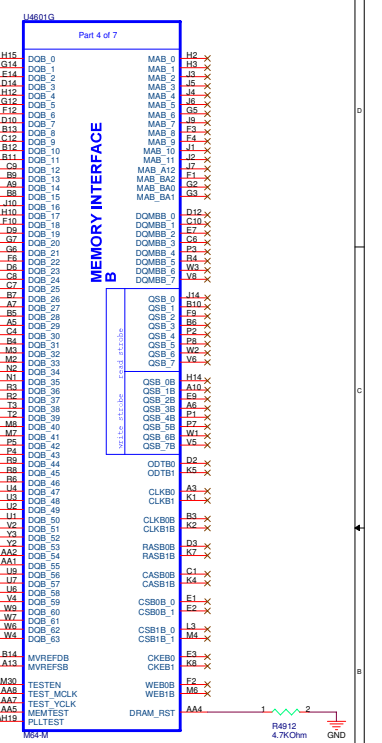
<< Kennedy_Zhang >>



PLACE MVREF DIVIDERS
AND CAPS CLOSE TO
ASIC




MEMORY INTERFACE														
MDA0	P27	DQA 0	MMA 0	C27	MAA0	MAB 0	H12	X						
MDA1	P28	DQA 1	MMA 1	B08	MAA1	MAB 1	H13	X						
MDA2	P31	DQA 2	MMA 2	B07	MAA2	MAB 2	H14	X						
MDA3	P32	DQA 3	MMA 3	G06	MAA3	MAB 3	H15	X						
MDA4	M27	DQA 4	MMA 4	F07	MAA4	MAB 4	H16	X						
MDA5	K29	DQA 5	MMA 5	E07	MAA5	MAB 5	H17	X						
MDA6	R31	DQA 6	MMA 6	D07	MAA6	MAB 6	H18	X						
MDA7	K32	DQA 7	MMA 7	J07	MAA7	MAB 7	H19	X						
MDA8	M33	DQA 8	MMA 8	E08	MAA8	MAB 8	H20	X						
MDA9	M34	DQA 9	MMA 9	C30	MAA9	MAB 9	H21	X						
MDA10	L34	DQA 10	MMA 10	E08	MAA10	MAB 10	H22	X						
MDA11	L35	DQA 11	MMA 11	A07	MAA11	MAB 11	H23	X						
MDA12	L33	DQA 12	MMA 12	G07	MAA12	MAB 12	H24	X						
MDA13	L34	DQA 13	MMA 13	D08	X	MAB 13	H25	X						
MDA14	H33	DQA 14	MMA 14	D08	X	MAB 14	H26	X						
MDA15	H34	DQA 15	MMA 15	MA_BA0		MAB 15	H27	X						
MDA16	K27	DQA 16	MMA 16	MA_BA1		MAB 16	H28	X						
MDA17	J29	DQA 17	DOMA0_0	M09	DOMA00	MAB 17	H29	X						
MDA18	H31	DQA 18	DOMA0_1	G30	DOMA01	MAB 18	H30	X						
MDA19	F29	DQA 19	DOMA0_2	F30	DOMA02	MAB 19	H31	X						
MDA20	E32	DQA 20	DOMA0_3	C30	DOMA03	MAB 20	H32	X						
MDA21	E32	DQA 21	DOMA0_4	G32	DOMA04	MAB 21	H33	X						
MDA22	D00	DQA 22	DOMA0_5	H01	DOMA05	MAB 22	H34	X						
MDA23	R32	DQA 23	DOMA0_6	C17	DOMA06	MAB 23	H35	X						
MDA24	G33	DQA 24	DOMA0_7	G17	DOMA07	MAB 24	H36	X						
MDA25	G34	DQA 25	OSA 0	M30	RDS0A0	MAB 25	H37	X						
MDA26	G35	DQA 26	OSA 1	K34	RDS0A1	MAB 26	H38	X						
MDA27	F34	DQA 27	OSA 2	C31	RDS0A2	MAB 27	H39	X						
MDA28	G34	DQA 28	OSA 3	E34	RDS0A3	MAB 28	H40	X						
MDA29	G34	DQA 29	OSA 4	R22	RDS0A4	MAB 29	H41	X						
MDA30	G35	DQA 30	OSA 5	F21	RDS0A5	MAB 30	H42	X						
MDA31	B34	DQA 31	OSA 6	D17	RDS0A6	MAB 31	H43	X						
MDA32	G34	DQA 32	OSA 7	D17	RDS0A7	MAB 32	H44	X						
MDA33	B34	DQA 33	OSA 8B	M31	WDQSA0	MAB 33	H45	X						
MDA34	B34	DQA 34	OSA 1B	K35	WDQSA1	MAB 34	H46	X						
MDA35	B34	DQA 35	OSA 2B	G32	WDQSA2	MAB 35	H47	X						
MDA36	C30	DQA 36	OSA 3B	E35	WDQSA3	MAB 36	H48	X						
MDA37	R31	DQA 37	OSA 4B	R22	WDQSA4	MAB 37	H49	X						
MDA38	C30	DQA 38	OSA 5B	E21	WDQSA5	MAB 38	H50	X						
MDA39	J22	DQA 39	OSA 6B	A17	WDQSA6	MAB 39	H51	X						
MDA40	J22	DQA 40	OSA 7B	E17	WDQSA7	MAB 40	H52	X						
MDA41	H22	DQA 41	ODTA0	C31	ODTA0	MAB 41	H53	X						
MDA42	F22	DQA 42	ODTA1	C25	ODTA1	MAB 42	H54	X						
MDA43	D21	DQA 43	CLKA0	A33	CLKA0	MAB 43	H55	X						
MDA44	H19	DQA 44	CLKA1	A36	CLKA1	MAB 44	H56	X						
MDA45	G19	DQA 45	CLKA2	A36	CLKA2	MAB 45	H57	X						
MDA46	F18	DQA 46	CLKA0B	B33	CLKA0B	MAB 46	H58	X						
MDA47	D18	DQA 47	CLKA1B	B36	CLKA1B	MAB 47	H59	X						
MDA48	C18	DQA 48	CLKA2B	B36	CLKA2B	MAB 48	H60	X						
MDA49	B19	DQA 49	RAS0A	A31	RAS0A	MAB 49	H61	X						
MDA50	A19	DQA 50	RAS0B	D34	RAS0B	MAB 50	H62	X						
MDA51	B18	DQA 51	RAS0C	C18	RAS0C	MAB 51	H63	X						
MDA52	C18	DQA 52	CAS0A	C32	CAS0A	MAB 52	H64	X						
MDA53	B18	DQA 53	CAS0B	H08	CAS0B	MAB 53	H65	X						
MDA54	C18	DQA 54	CAS0C	H08	CAS0C	MAB 54	H66	X						
MDA55	A18	DQA 55	CAS0A0_0	A30	CAS0A0_0	MAB 55	H67	X						
MDA56	B18	DQA 56	CAS0A0_1	S30	X	MAB 56	H68	X						
MDA57	F18	DQA 57	CAS0B_0	G34	CAS0B_0	MAB 57	H69	X						
MDA58	F18	DQA 58	CAS0B_1	G34	CAS0B_1	MAB 58	H70	X						
MDA59	D18	DQA 59	CSA0B_0	G34	CSA0B_0	MAB 59	H71	X						
MDA60	A17	DQA 60	CSA0B_1	G34	CSA0B_1	MAB 60	H72	X						
MDA61	G15	DQA 61	CSA1B_0	G34	CSA1B_0	MAB 61	H73	X						
MDA62	E15	DQA 62	CSA1B_1	G34	CSA1B_1	MAB 62	H74	X						
MDA63	H15	DQA 63	CKEA0	B31	CKEA0	MAB 63	H75	X						
			CKEA1	F24	CKEA1	MAB 64	H76	X						
			WEA0A	C29	WEA0A	MAB 65	H77	X						
			WEA1B	D22	WEA1B	MAB 66	H78	X						
						MAB 67	H79	X						
						MAB 68	H80	X						
						MAB 69	H81	X						
						MAB 70	H82	X						
						MAB 71	H83	X						
						MAB 72	H84	X						
						MAB 73	H85	X						
						MAB 74	H86	X						
						MAB 75	H87	X						
						MAB 76	H88	X						
						MAB 77	H89	X						
						MAB 78	H90	X						
						MAB 79	H91	X						
						MAB 80	H92	X						
						MAB 81	H93	X						
						MAB 82	H94	X						
						MAB 83	H95	X						
						MAB 84	H96	X						
						MAB 85	H97	X						
						MAB 86	H98	X						
						MAB 87	H99	X						
						MAB 88	H100	X						
						MAB 89	H101	X						
						MAB 90	H102	X						
						MAB 91	H103	X						
						MAB 92	H104	X						
						MAB 93	H105	X						
						MAB 94	H106	X						
						MAB 95	H107	X						
						MAB 96	H108	X						
						MAB 97	H109	X						
						MAB 98	H110	X						
						MAB 99	H111	X						
						MAB 100	H112	X						

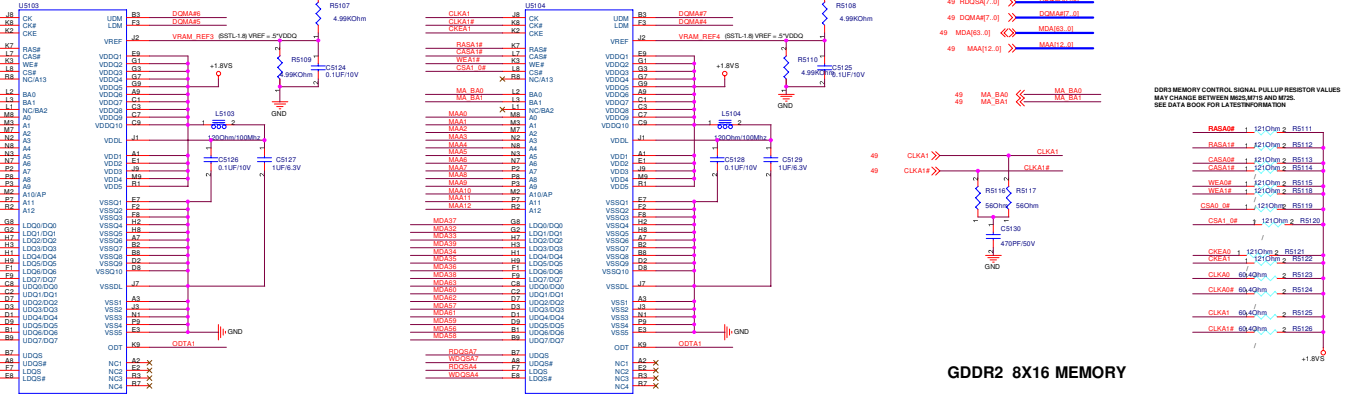
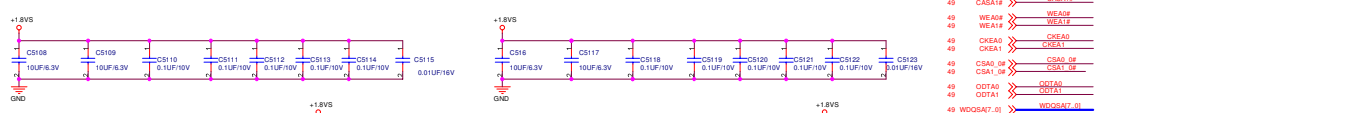
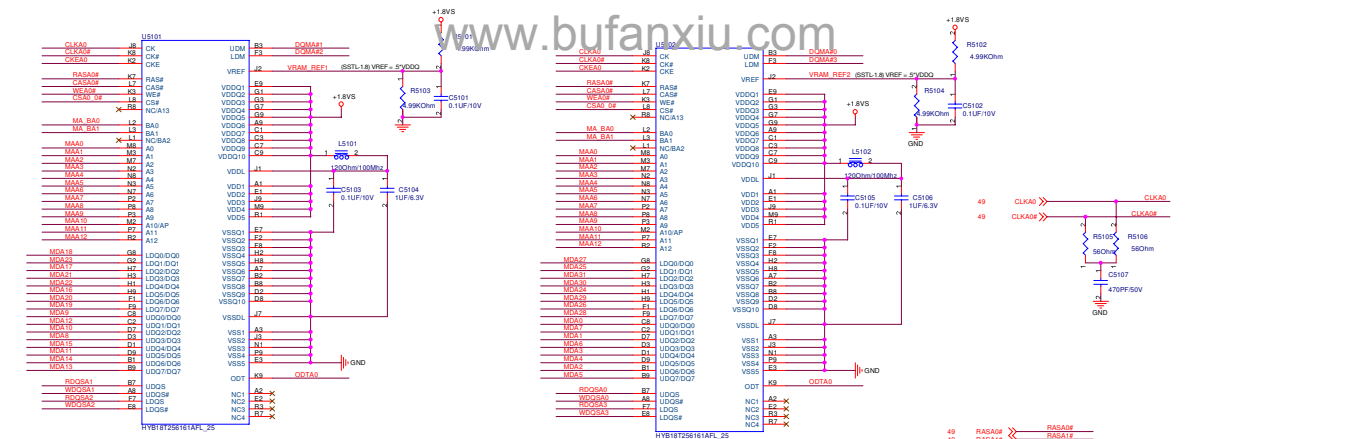


<< Kennedy_Zhang >>

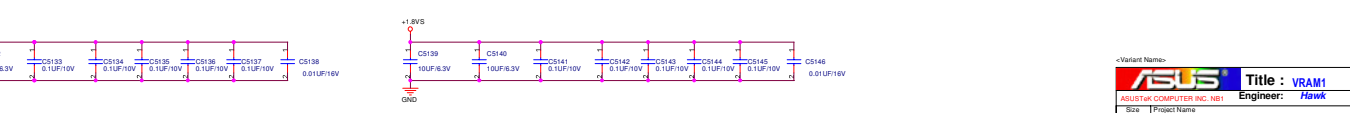


		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期一, 四月 23, 2007		Sheet 50 of 94

<< Kennedy_Zhang >>



GDDR2 8X16 MEMORY



ASUS Title: VRAM
 Engineer: f5w
 F5V
 Rev 1.0

« Kennedy_Zhang »

**COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED**

BB_ENA = 0V FOR BACK BIASING DISABLED

MAX1673 SHUTDOWN

-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND

N FET A = OFF, P FET B = OFF, N FET C = ON

+BBP = VDD_CORE

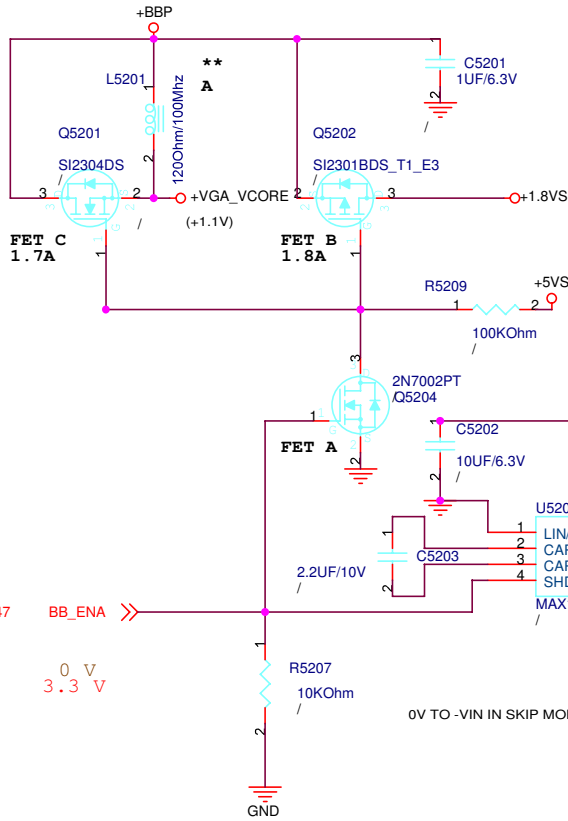
BB_ENA = +3.3V FOR BACK BIASING ENABLED

MAX1673 ENABLED

-BBN = -.5V

N FET A = ON, P FET B = ON, N FET C = OFF

+BBP = +1.5V



**** FOR NO BACK BIASING
DO NOT INSTALL FETS OR REGULATOR LOGIC
AND INSTALL BEAD A AND RESISTOR A**

ASUS		Title : BACK BIAS
ASUSTek COMPUTER INC. NB1		Engineer: Hawk
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 52 of 94

<< Kennedy_Zhang >>

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

www.bufanxiu.com

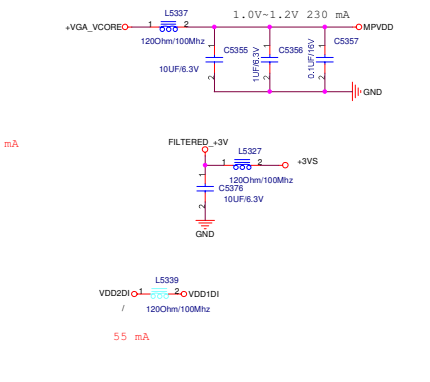
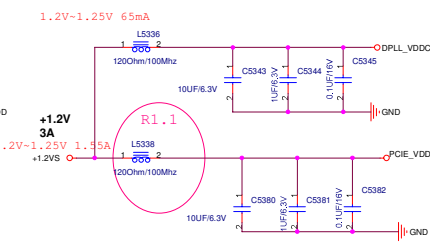
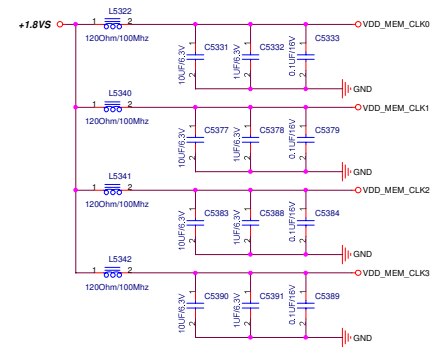
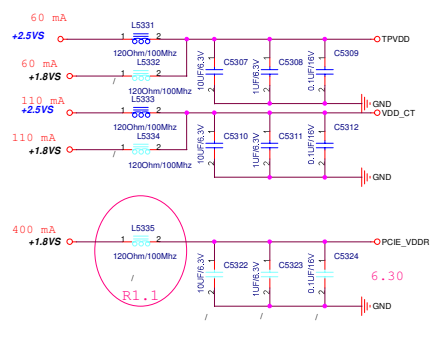
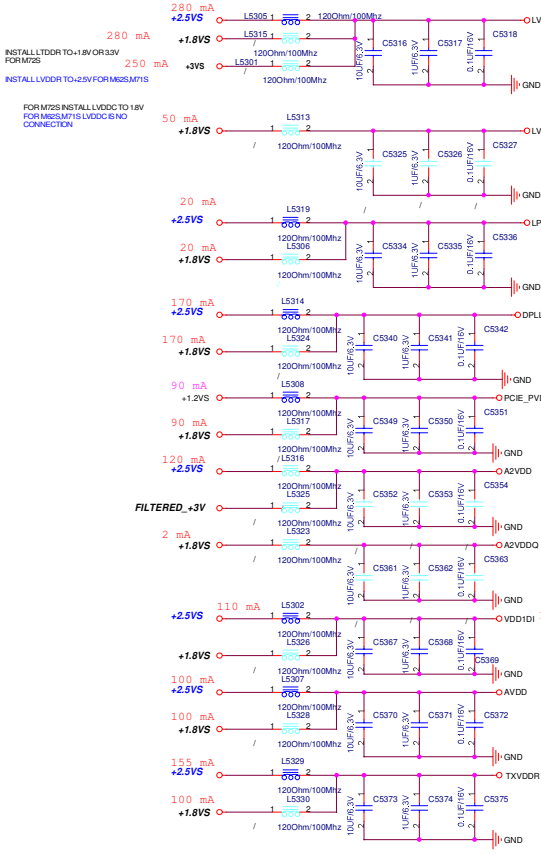
LTPVSS18 DVSSDI TPVSS MPVSS
* PCIE_PVSS PVSS A2VSSQ AVSSQ

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP

280 mA
+2.5VS
INSTALL LTPDDR TO +1.8V OR 3.3V FOR M2S

250 mA
+1.8VS
INSTALL LVDDR TO +2.5V FOR M2S/M7S


FOR M7S2S INSTALL LVDDC TO 1.8V FOR M2S/M7S LVDDC IS NO CONNECTION



ASUS		Title : IO capacitor	
ASUSTek COMPUTER INC. N81		Engineer: Hawk	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/23/2007	Sheet: 53	of	94

<< Kennedy_Zhang >>

<Variant Name>

		Title : VRAN2
ASUSTEK COMPUTERS INC. NET		Engineer: HAWK
Size	Project Name	Rev
C	FSV	1.0
Code: 001-10138-0007	ESpec	04 of 04

« Kennedy_Zhang »

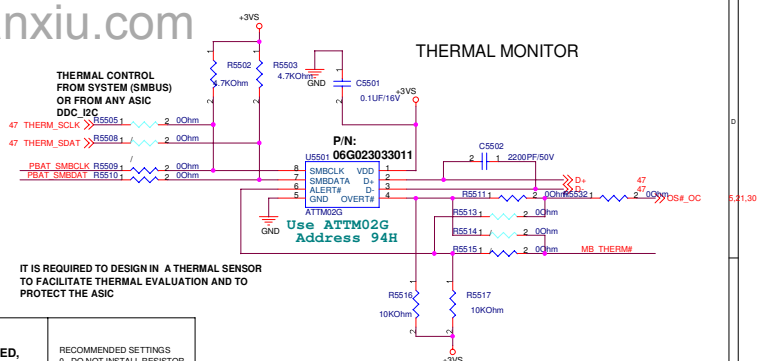
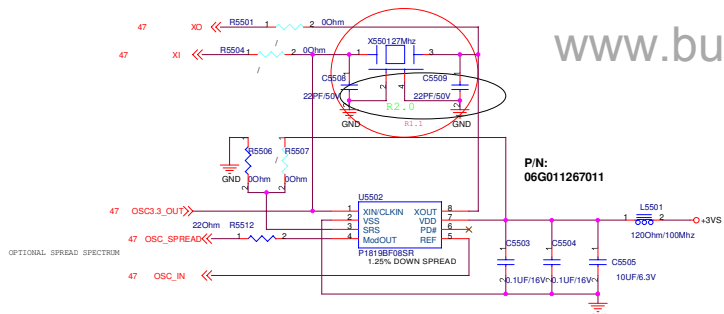
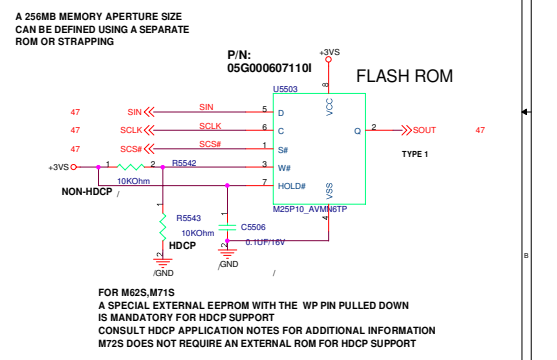
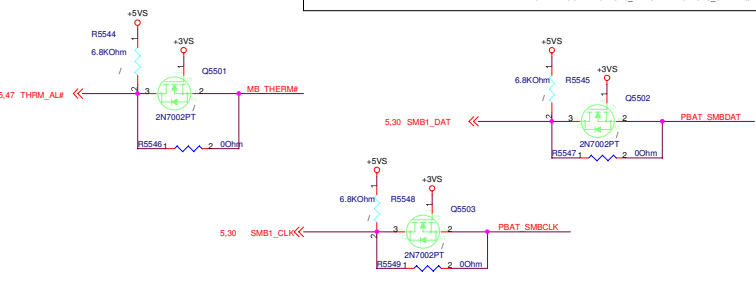


Table listing configuration straps for various GPIOs. Each row includes a pin number (e.g., 47), a strap name (e.g., GPIO0), a resistor value (e.g., 2 10KOhm), and a color-coded line.

CONFIGURATION STRAPS table with columns: STRAPS, PIN, DESCRIPTION OF DEFAULT SETTINGS, M62S M71S, and M72S. It lists settings for BIF_MSI_DIS, BIF_64BAR_EN_A, TX_PWRS_ENB, TX_DEEMPH_EN, BIF_DEBUG_ACCESS, PLL_BIAS_RD_1.0, BIOS_ROM_EN, ROMIDCFG(3:0), VIP_DEVICE_STRAP_ENA, BIF_VGA_DIS, and MEM_TYPE.

ATI RESERVED CONFIGURATION STRAPS table with columns: STRAPS, PIN, DESCRIPTION OF DEFAULT SETTINGS, M62S M71S, and M72S. It lists settings for VID0, VID2, VID3, VID4, VID5, VID7, HSYNC, GPIO8, DVALID, GPIO2, and GPIO3.

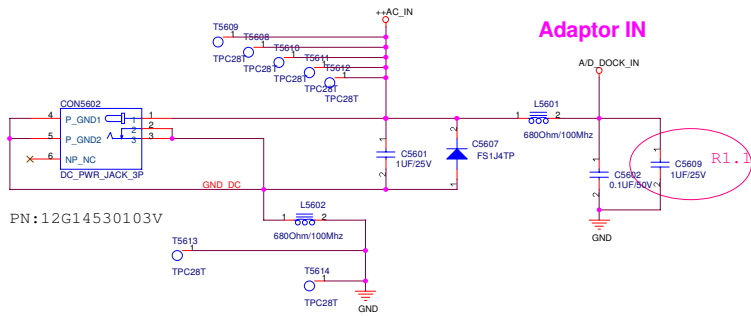
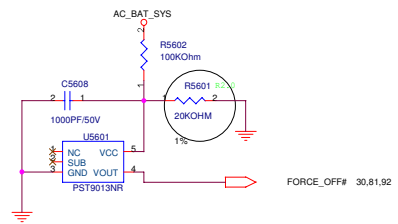
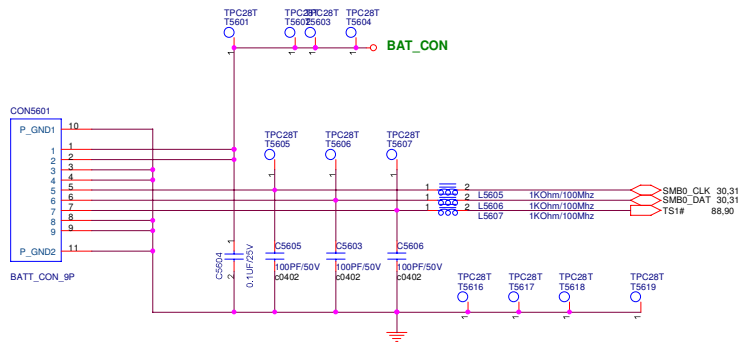
Only populate the required straps, see table and databook



COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

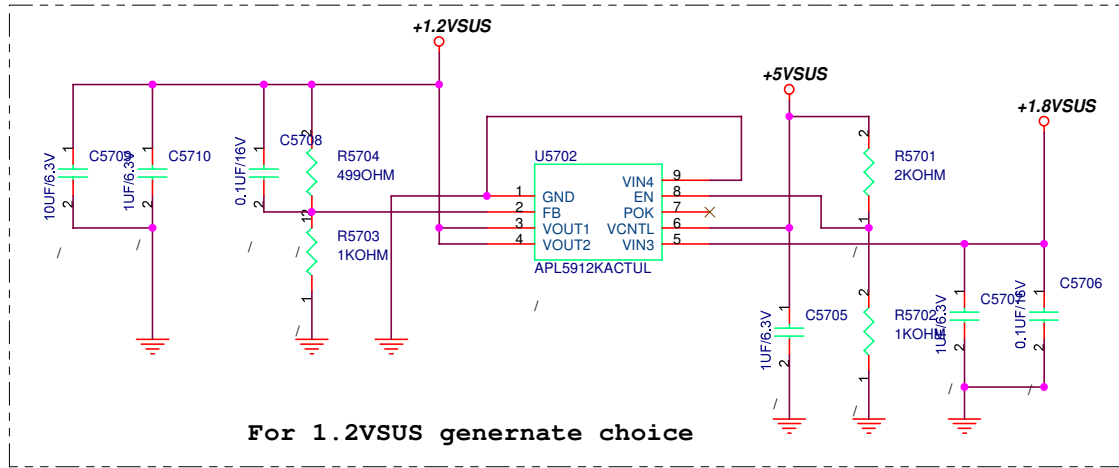
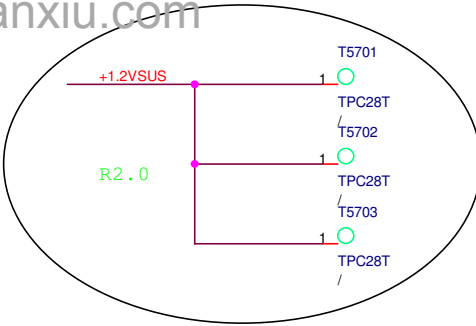
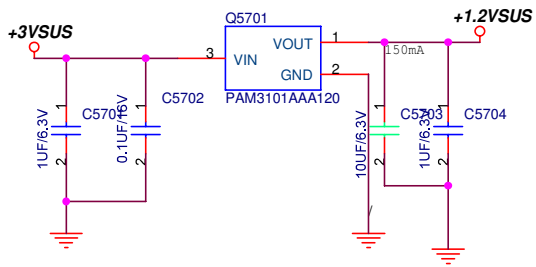
ASUS Title: SS STRAPS table with fields for Project Name (FSV), Engineer (Hawk Kazidy), Date (11/11/23/2007), and Sheet (55 of 94).

<< Kennedy_Zhang >>



ASUS		Title : AC/BAT JACK	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk	
Size	Project Name		Rev
B	F5V		1.0
Date: # [] [] [] 23 2007		Sheet	56 of 94

<< Kennedy_Zhang >>




For 1.2VSUS generate choice

ASUS		Title : +1.2VSUS
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007	Sheet 57 of 94	

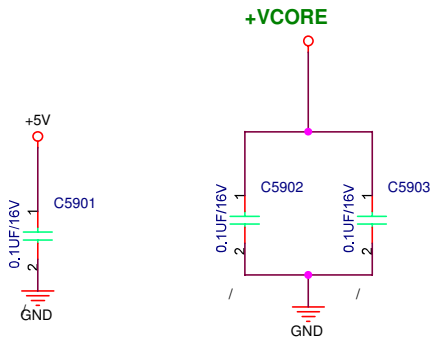
<< Kennedy_Zhang >>

D
C
B
A

D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 58 of 94

<< Kennedy_Zhang >>



		Title : EMI
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 59 of 94

<< Kennedy_Zhang >>

- 1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.
- 2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#
- 3. P7 unmount R706
- 4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]
- 5. P21 change R2121 to 00hm
add R2124(330hm) for ACZ_RST# according to 968 ACT.
add R2108/R2112(00hm) for PCIEPRSNTO/1 according to sis ACT.
ADD GMAC OSC25MHZ to GND according to sis ACT.
unmount L2103, mount L2105 according to spec.
unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
change GPIO17 from VIN4 to S_A20GATE, add R2127(00hm) for reserve SUSCLK
- 6. P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage
- 7. P22 change R2217 to 12KOhm, add C2237(22pF) for SATA REXT according to 968 ACT.
- 8. P24 add R2434 for A20GATE to H_A20M#, add R2457 for A20GATE to S_A20GATE, add R2456 to PU S_A20GATE
- 9. P29 add R2909/R2910(00hm), unmount L2901 for EMI.
- 10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .
delete D3004 for DDR power are not SUS power,
add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,
Add R3019 for INSTANTON#
- 11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost
- 12. P37 mount R3716/Q3715 for +VCCP discharge
- 13. P42 change IDSEL to PCI_AD24
- 14. P46 add D4602 for VGA_RST#
- 15. P48 unmount L4803/R4809, delete L4801
unmount R4806, mount Q4801/R4807/Q4802/R4808
- 16. P53 change L5335/L5338 to match the current.
- 17. P55 change X5501 to +-10ppm to follow spec, add C5508/C5509 to match X5501
- 18. P56 add C5609 for over current damaging charge IC.
- 19. P4 Change C440 from 0.1UF to 0.22UF
- 20. P10 change L1001 to 2A to match the current,, Add +1.2VS delay circuit.
- 21. P21 Add VGA_RST# to GPIO7, add R2140 for VGA_RST#.
- 22. P47 Unmount R4759, mount R4758 for Vram changed from 03G151236011 to 03G151236012.


- R2.0
- 1. P29 mount R2907, connect PCIE_PRSNT1 to CPEP#
 - 2. P21 unmount R2109, mount R2119, change R2118 from 00hm to 4.7KOhm but unmount R2118
 - 2. P27 change R2708 to 00hm and mount it to not support C3 mode
 - 3. P33422 add two TPS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply
 - 4. P21 add R2141 to connect OS#_OC to PM_THERMTRIP#, change R2141 to Q2101
 - 5. P30 change C3009/C3003 to 6.8pF
 - 6. P27 change C2706/C2707 to 24pF
 - 7. P55 change C5508/C5509 to 22pF
 - 8. P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301
 - 9. P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3
 - 10. P30 change Q3003 PU from +5V to +5VS
 - 11. P5 unmount R506
 - 12. P56 change R5601 to 20KOhm
 - 13. P20 unmount R2054, add and mount C2010
 - P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206
 - 14. P27 change 4in1 cardreader
 - 15. P47 mount R4704/R4705/R4706/R4707
P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839, change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813
 - 16. P21 Unmount L2105, mount L2103
 - 17. P21 change R2116 from 330hm to 200hm, change R2117 from 330hm to 00hm, change R2119 from 330hm to 200hm
 - P24 change R2418 from 330hm to 00hm, change R2420 from 330hm to 00hm, change R2419 from 330hm to 00hm, change R2422 from 330hm to 00hm, change R2423 from 330hm to 00hm, change R2425 from 330hm to 00hm
P25 change R2514 from 330hm to 470hm

		Title : BLANK	
ASUSTek COMPUTER INC. H&I		Engineer: Kaxidy/Hawk	
Ver	Project Name	Rev	
1.0	F5VL	1.0	
Date: 2011-05-20		Sheet: 65	of 65

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 61 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 62 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 63 of 94

<< Kennedy_Zhang >>


D
C
B
A

D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 64 of 94

<< Kennedy_Zhang >>




		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 65 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 66 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 67 of 94

<< Kennedy_Zhang >>


D
C
B
A

D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 68 of 94

<< Kennedy_Zhang >>




		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 69 of 94

<< Kennedy_Zhang >>


D
C
B
A

D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 70 of 94

<< Kennedy_Zhang >>




		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 71 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 72 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 73 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 74 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 75 of 94

<< Kennedy_Zhang >>

D
C
B
A


D
C
B
A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 76 of 94

<< Kennedy_Zhang >>


D
C
B
A

D
C
B
A

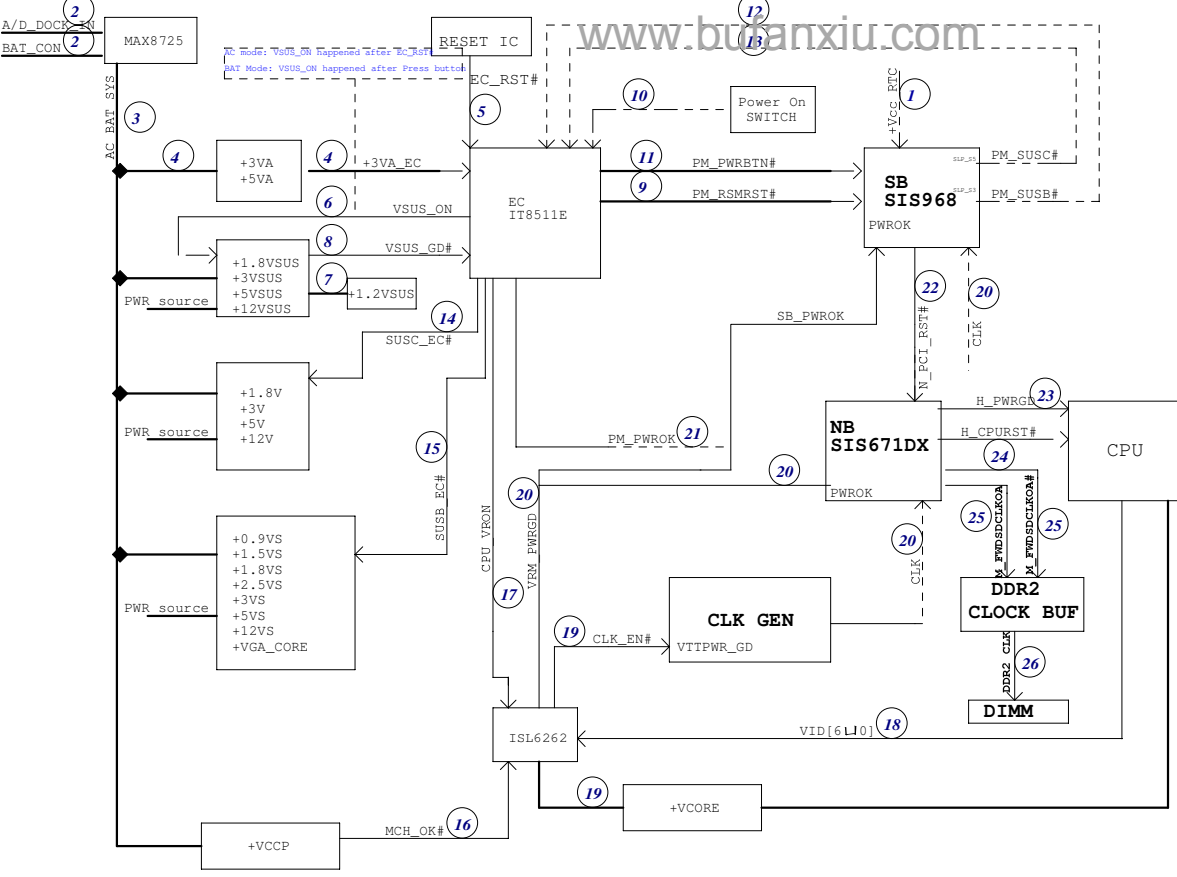
		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 77 of 94

<< Kennedy_Zhang >>



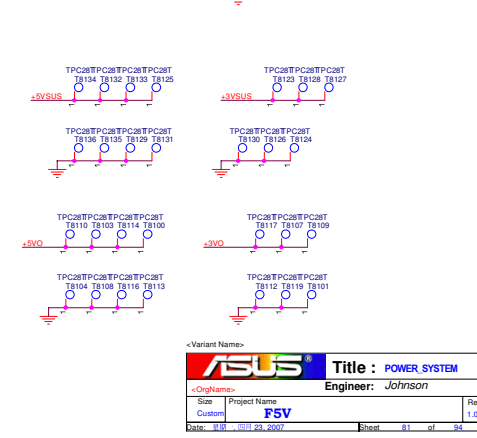
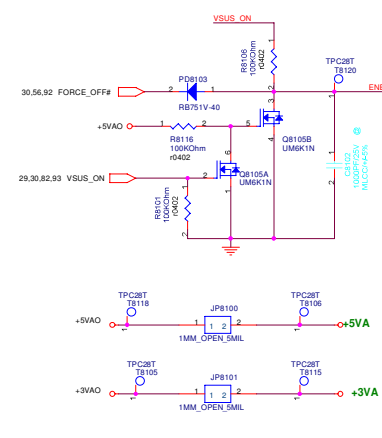
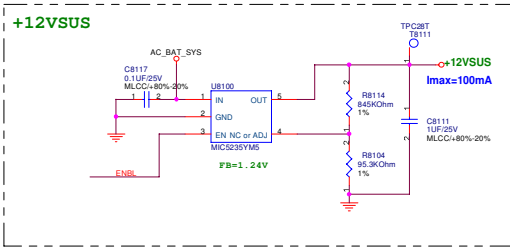
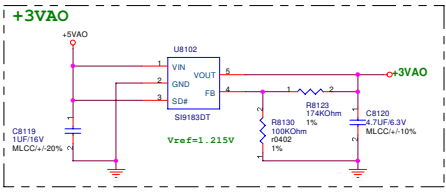
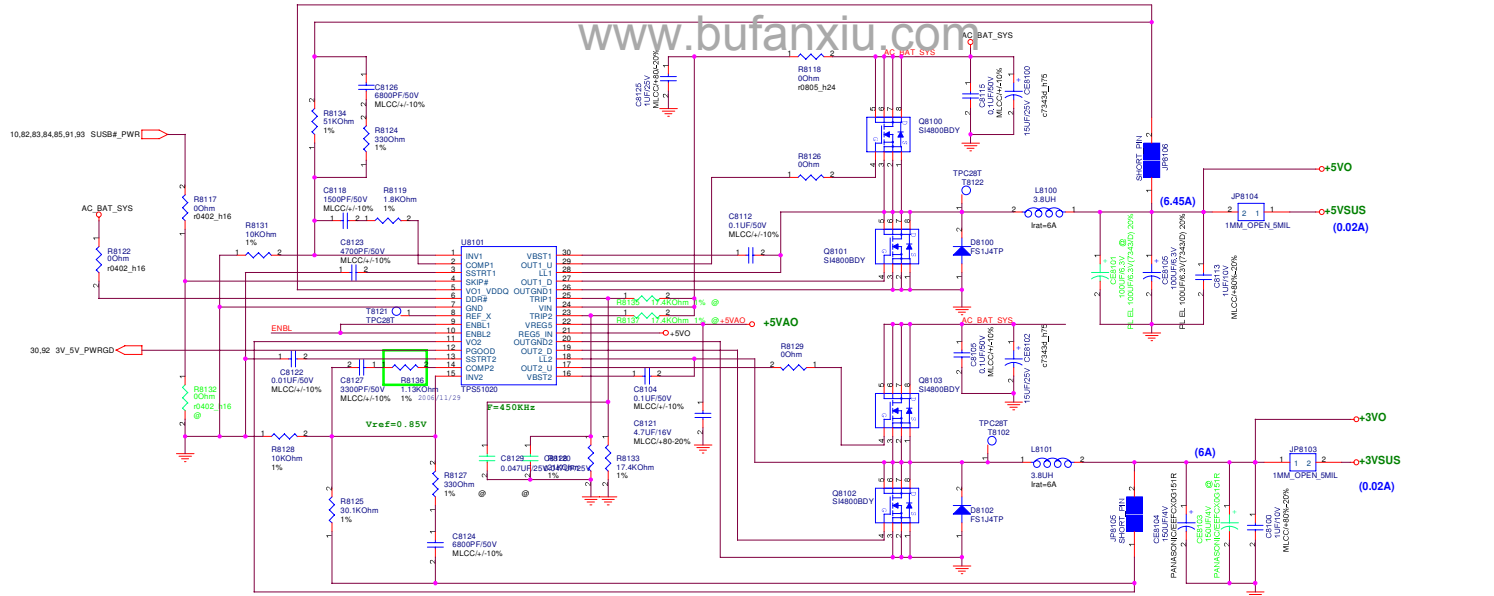
		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	Rev
A	F5V	1.0
Date: 星期一, 四月 23, 2007		Sheet 78 of 94

<< Kennedy_Zhang >>



Power On Sequence
 1 -----> 26

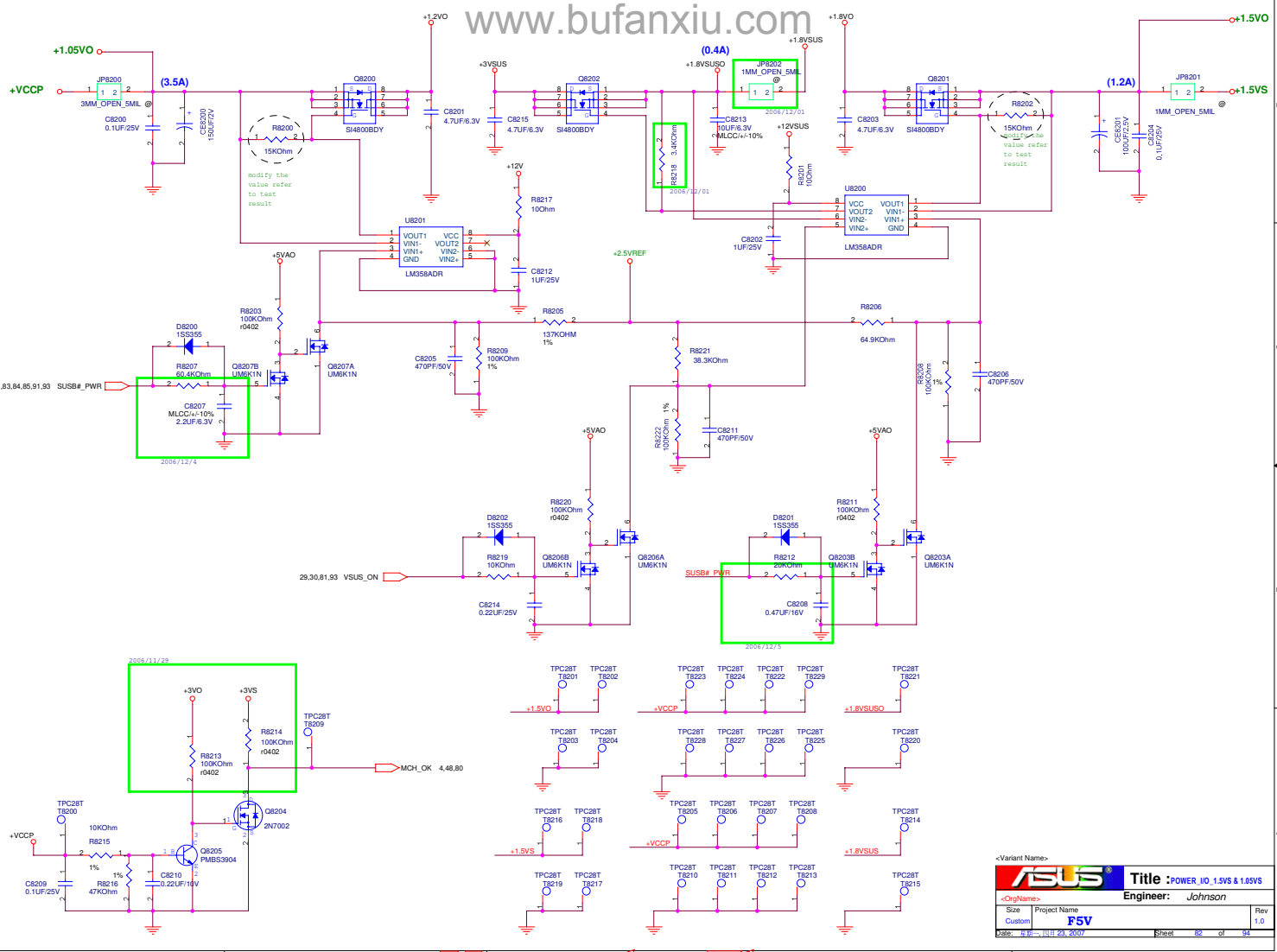
<< Kennedy_Zhang >>



<Variant Name>

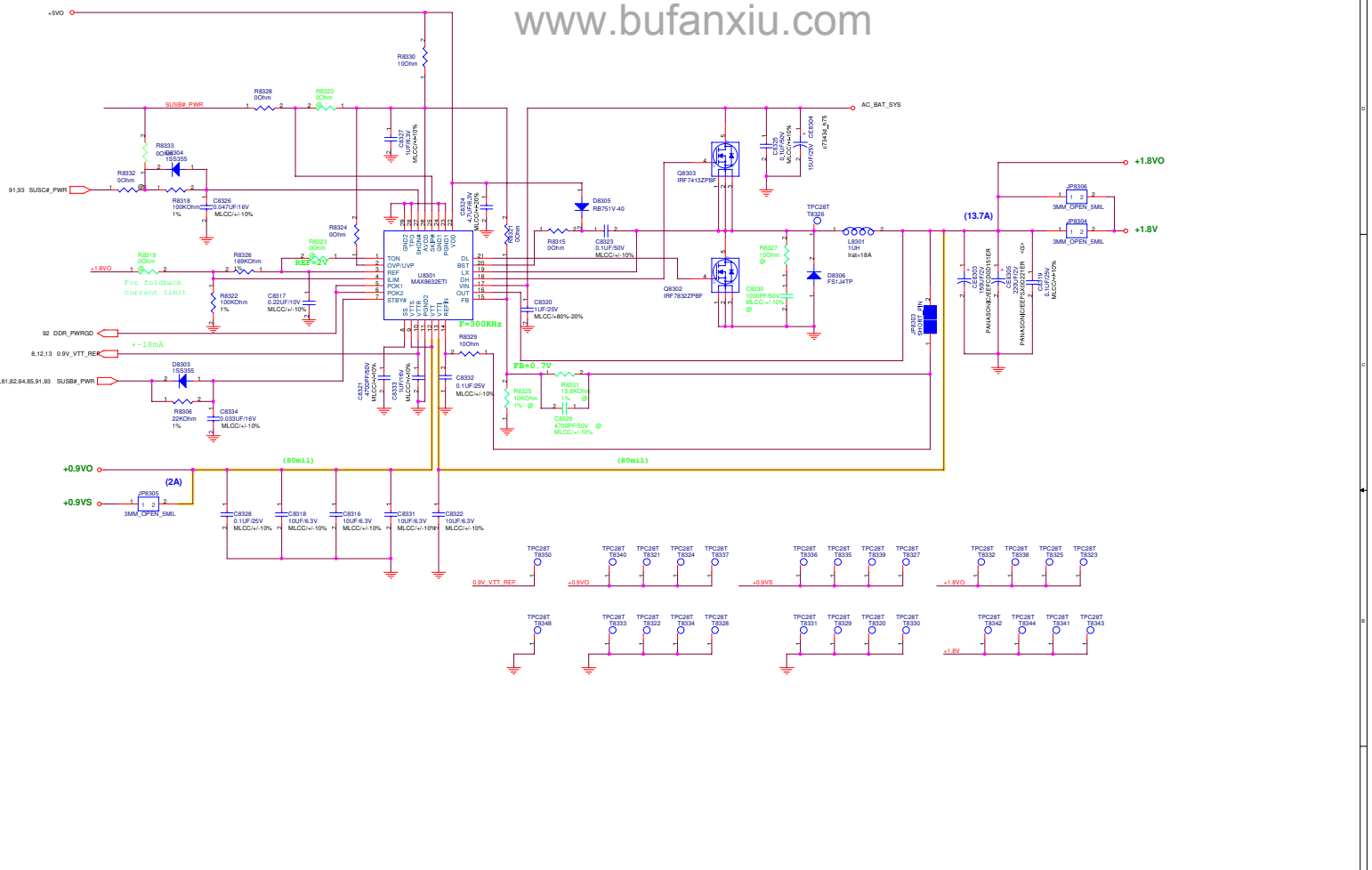
ASUS		Title : POWER SYSTEM	
<OrigName>	Project Name	Engineer:	Johnson
Size	Custom	F5V	Rev 1.0
Date: 3/18/2007 09:29:2007		Sheet 81	of 94

<< Kennedy_Zhang >>



-Variant Name-		Title :POWER_IIO_1.5VS & 1.5VS	
ASUS		Engineer: Johnson	
Size	Project Name	Rev	1.0
Custom	F5V		
Date: 11/23/2007	Sheet	62	of 84

<< Kennedy_Zhang >>

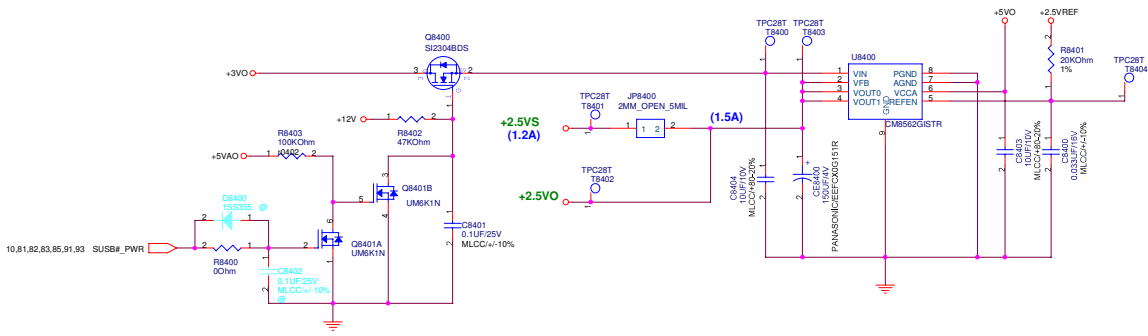


-Variant Name-

		Title : POWER_IO_DDR & VTT	
-Originals-		Engineer: Johnson	
Size	Project Name	Rev	
C	F5V	1.0	
DATE: 10/23/2007	ESDN	81	of 84

« Kennedy_Zhang »

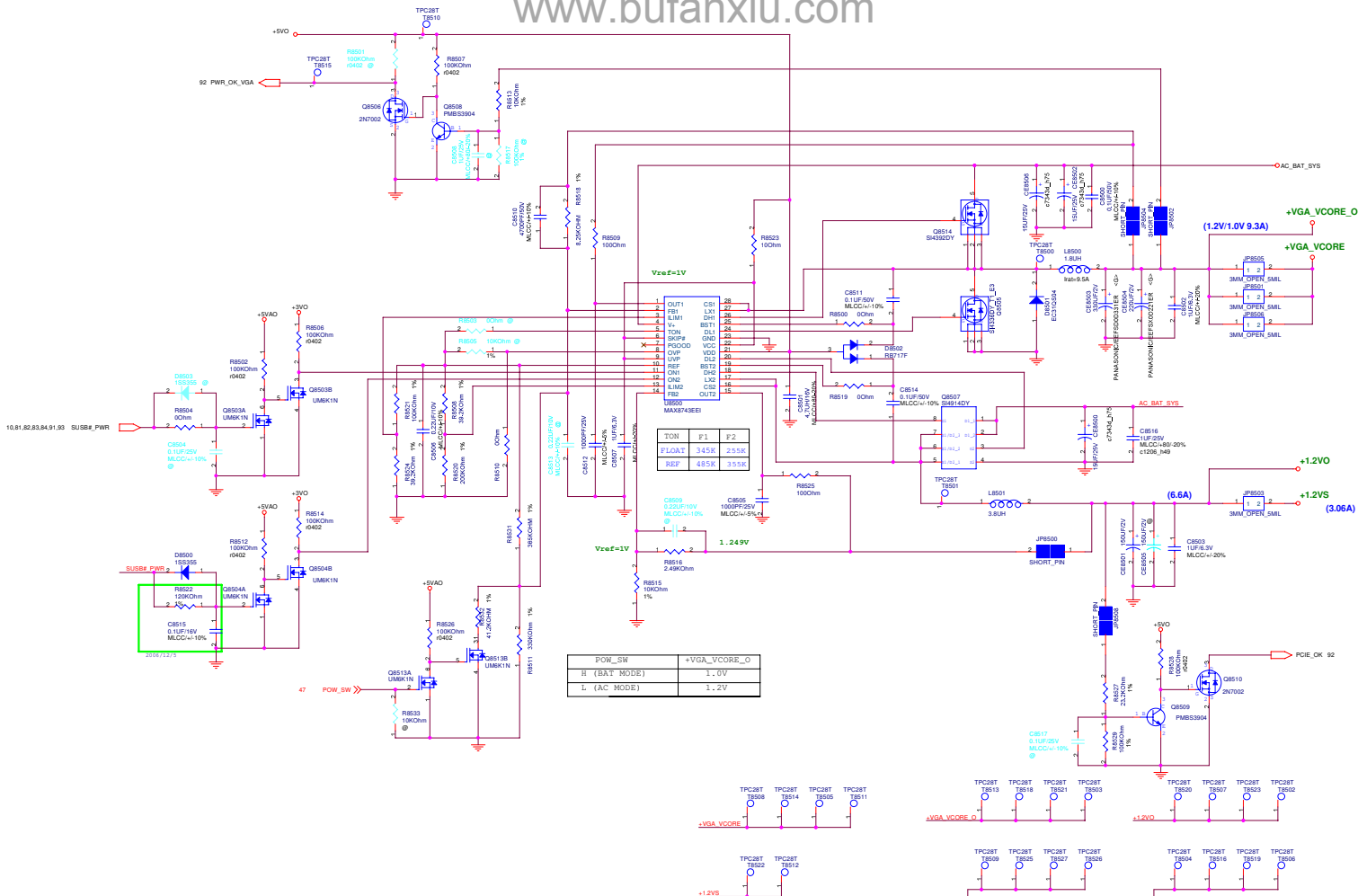
+2.5VS



<Variant Names>

		Title : POWER_IO_+3VA & +2.5V
Engineer: Johnson		
<OrigName>	Project Name	Rev
Size	Custom	F5V
Date: 11/11/2007	Sheet 84	of 94


<< Kennedy_Zhang >>




<Variant Name>

		Title : POWER VGA CORE & RAM
-> Designer :		Engineer : Johnson
Size :	Project Name :	Rev :
C :	F5V	1.0
Date : 08/11/2007	FileNo :	85 of 84

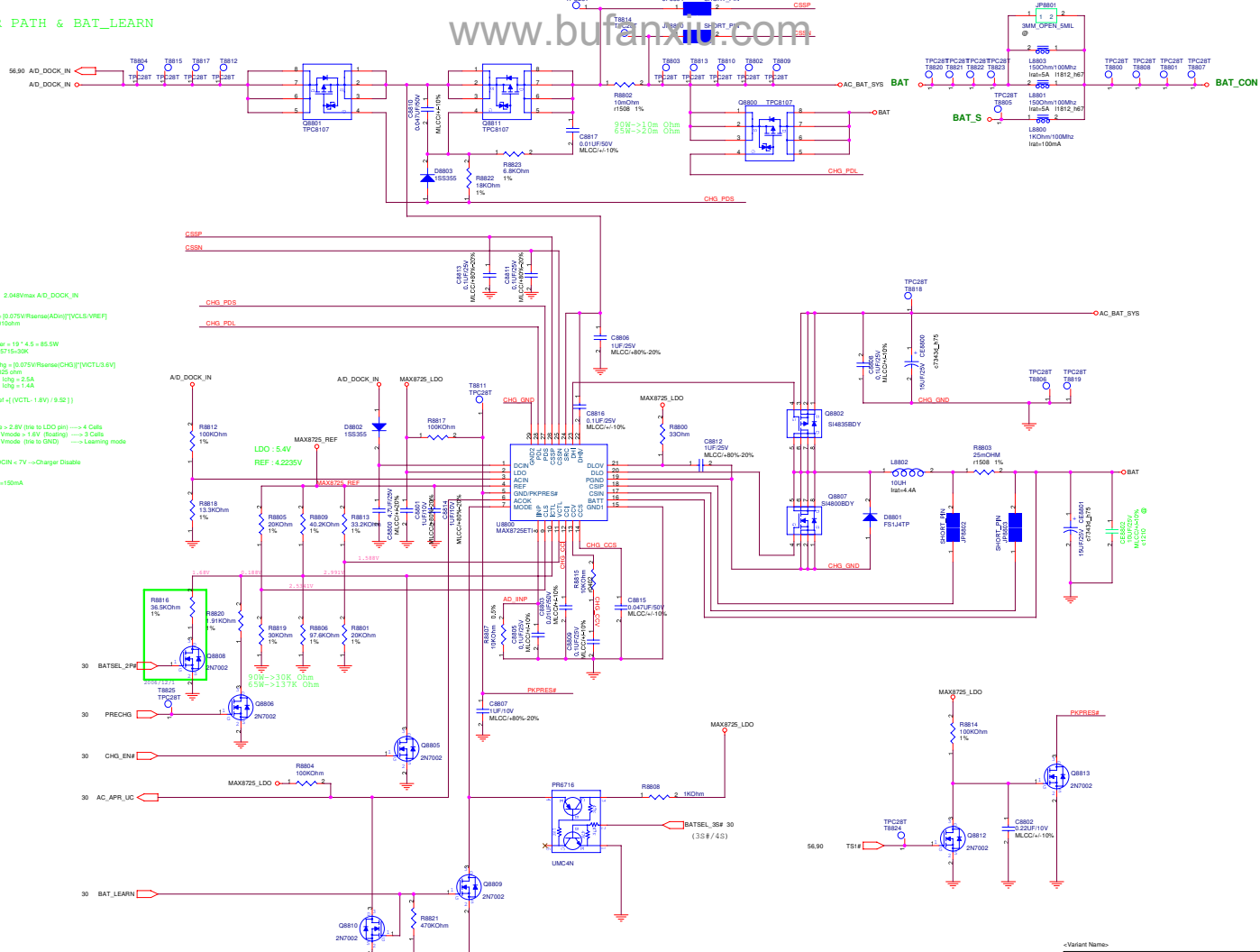
<< Kennedy_Zhang >>

<Variant Name>		Title : NA	
		Engineer: <i>Johnson</i>	
Size	Project Name		Rev
B	FSV		1.0
Date:	# 01	11/11/23, 2007	Sheet 86 of 94

<< *Kennedy_Zhang* >>

<Variant Name>					Title : N/A	
<OrigName>			Engineer: Johnson			
Size	Project Name			Rev		
Custom	FSV			1.0		
Date: 2007-11-23			Sheet 87 of 94			

<< Kennedy_Zhang >>




VC_N Threshold > 0.048Vmax AD_DOCK_IN
 > 17.44V active
 Adapter In(max) = [0.075V/Rsense/Adm][VCL5 VREF]
 Resense/Adm=0.000m
 VCL5=2.534V
 => In(max)=4.5A
 => Constant Power = 13.145 + 85.5W
 => RST to 200mA/57.1530k
 Charge Current Ichg = [0.075V/Rsense/CHG][VCTL3.6V]
 Resense/CHG=0.0020m
 VCTL=3V => Ichg = 2.5A
 VCTL=1.588V => Ichg = 1.4A
 Mode pin: Vinode > 2.8V (pin to LDO pin) => 4 Cells
 2.0 < Vinode < 1.8V (Booting) => 3 Cells
 0.8 < Vinode (pin to DND) => Learning mode
 VICT=0.8V or DCIN = 7V => Charger Disable
 Precharge current=150mA

-Variant Name-

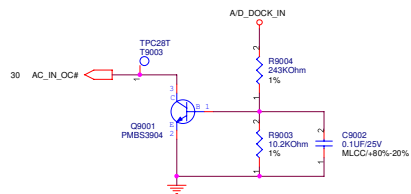
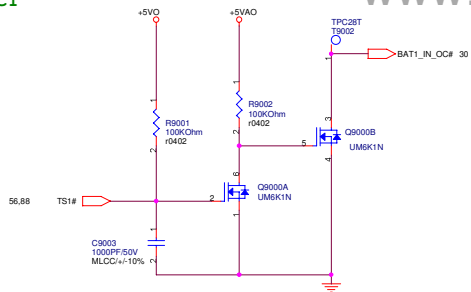
ASUS		Title :POWER CHARGER
-Original-		Engineer: Johnson
Size	Project Name	Rev
C	F5V	1.0
Doc. No.:	10133-2007	ESch: 88 of 84

« Kennedy_Zhang »

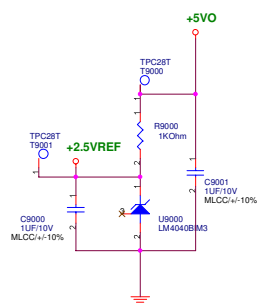
<Variant Name>					Title : N/A	
<OrigName>			Engineer: Johnson			
Size	Project Name				Rev	
Custom	FSV				1.0	
Date: 11/11/2007					Sheet 89 of 94	

<< Kennedy_Zhang >>

BATTERY IN DETECT



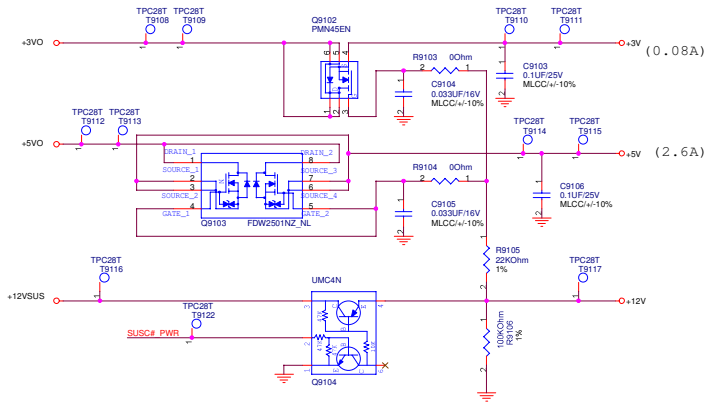
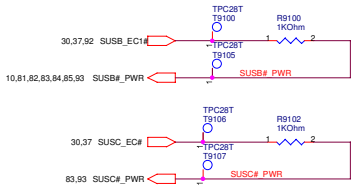
+2.5VREF



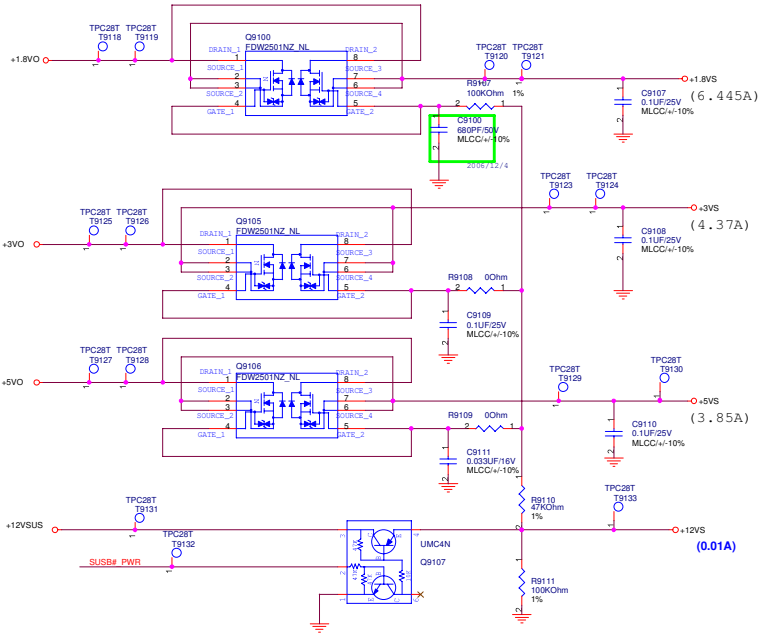
<Variant Name>

		Title :POWER_DETECT	
<OrigName>		Engineer: Johnson	
Size	Project Name		Rev
Custom	FSV		1.0
Date: 2007-11-23	2007	Sheet	90 of 94

<< Kennedy_Zhang >>



SUSB#_PWR POWER

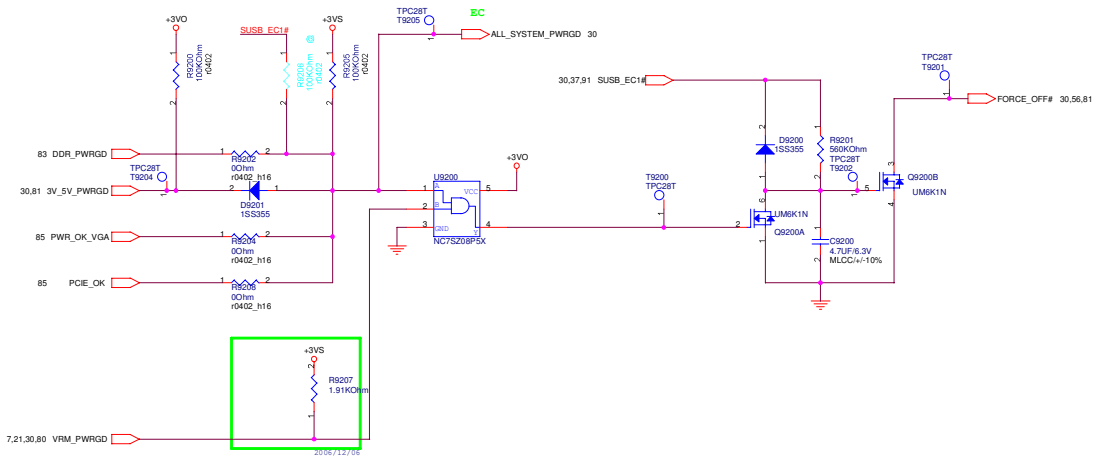


<Variant Name>


ASUS		Title :POWER_LOAD_SWITCH	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 2007-11-23 2007	Sheet	BT	of 94

<< Kennedy_Zhang >>

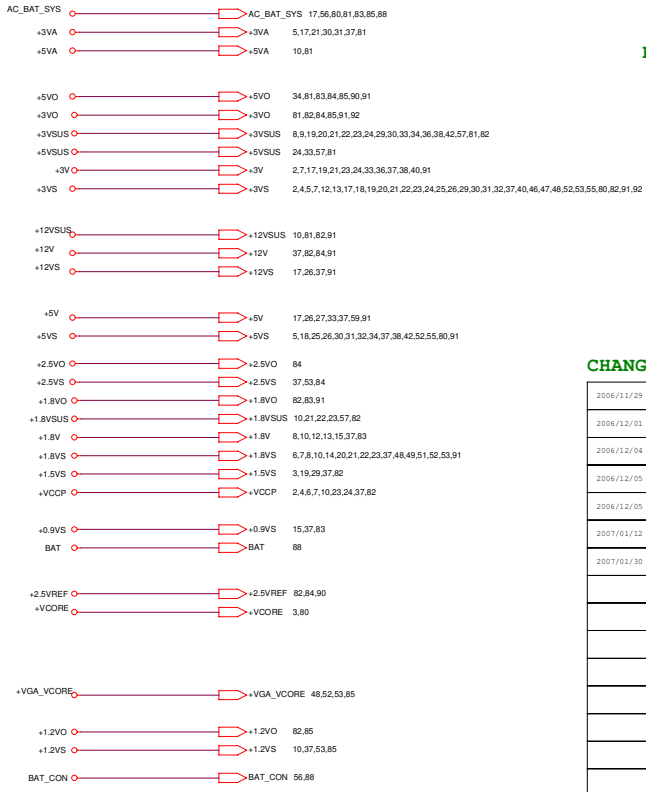
POWER GOOD DETECTOR



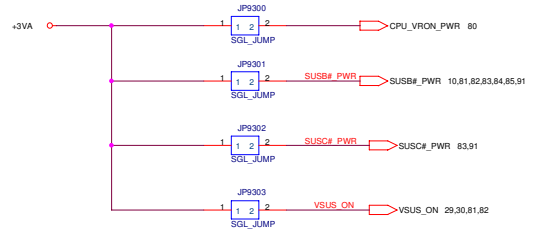
<Variant Name>

		Title :POWER_PROTECT	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	F5V	1.0	
Date: 2007-11-11 11:23:2007	Sheet	62	of 94

<< Kennedy_Zhang >>



FOR POWER TEST



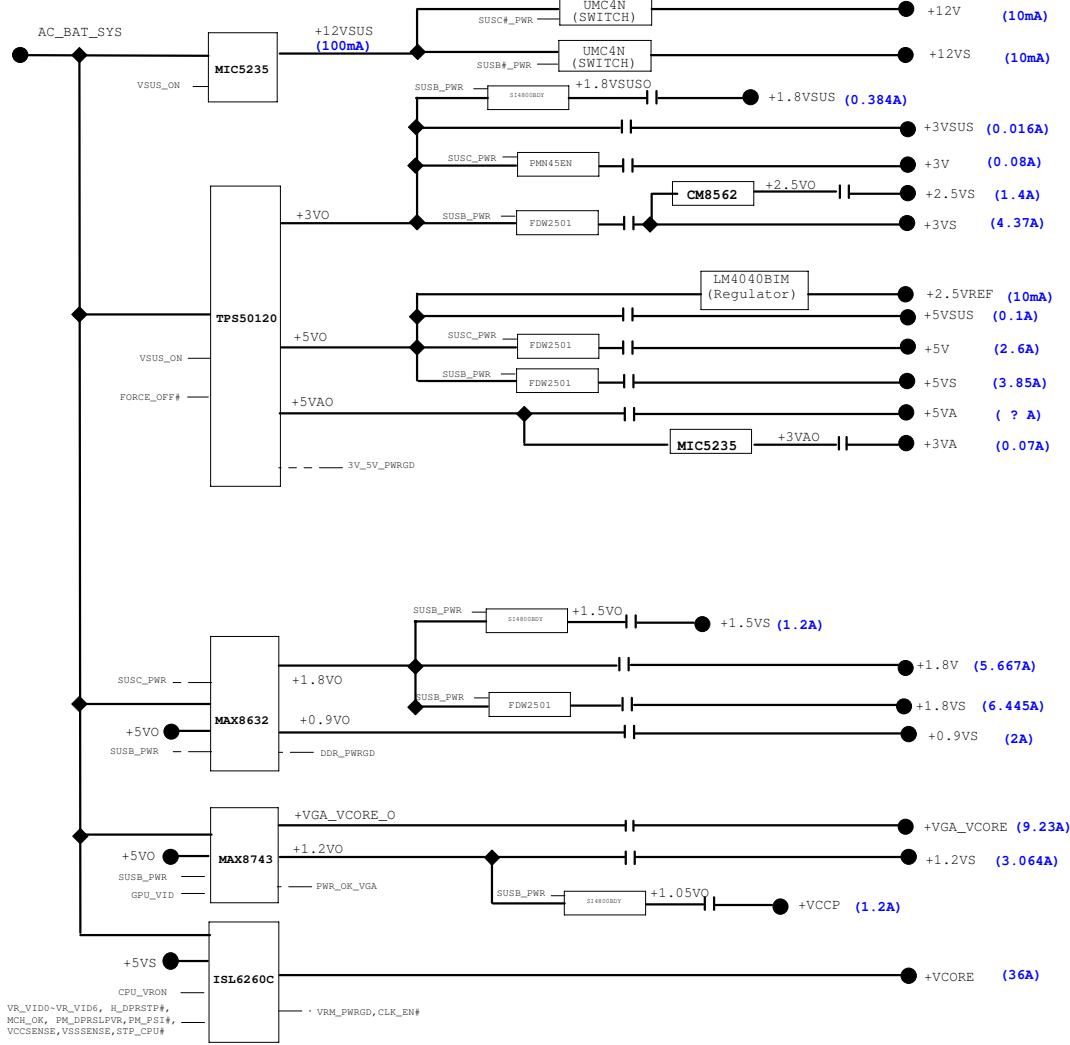
CHANGE LIST

2006/11/29	1. Pull high R8213 to +3V0 , 2. change C8334 to 0.1uF, 3.change R8136 to 1.13KOhm
2006/12/01	1. change R8218 to 3.4KOhm, 2. add JP8202, 3. delete R8055, 4.add Q8808 & R8816
2006/12/04	1. change C8207 to 2.2uF & R8207 to 60.4KOhm , 2. delete R8055, 3.change C9910 to 680pF
2006/12/05	1. change C8208 to 0.47uF & R8212 to 20KOhm, 2. change C8515 to 0.1uF & R8522 to 120KOhm.
2006/12/05	1.change R9207 to 1.91KOhm
2007/01/12	1. change input cap footprint, 2. add necessary TP.
2007/01/30	1. C8207 to 2.2uF/6.3V

-Variant Name-

ASUS		Title :POWER_SIGNAL
-OrigName-	Engineer : Johnson	
Size	Project Name	Rev
Custom	FSV	1.0
Date: 11/23/2007	Sheet 93	of 94

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

ASUS		Title :POWER_FLOWCHART	
Engineer: Johnson			
Rev	Project Name	Date	Rev
1.0	FSV	11/02/2007	1.0
1	1	1	1