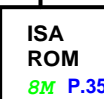
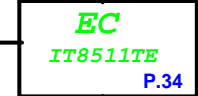
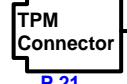
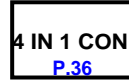
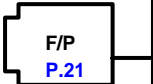
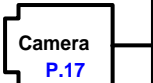
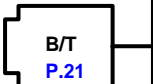
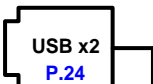
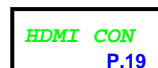
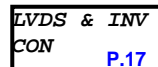
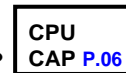
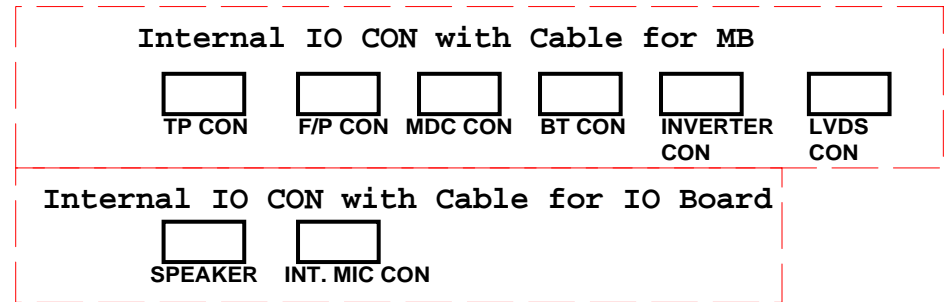
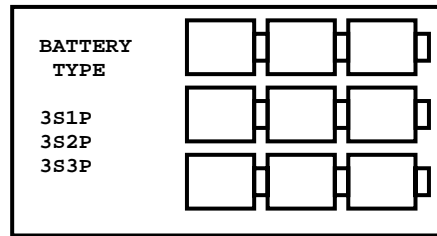


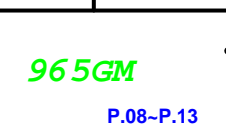
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ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size Custom	Project Name F6E	Rev 1.10	
Date: Tuesday, August 21, 2007		Sheet 1 of 94	

F6E BLOCK DIAGRAM

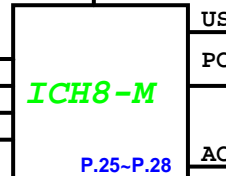
www.bufoanxi.com



AGTL 1.468V, 200MHZ



DDR2 SDRAM 533/667MHZ



ACZ

USB2.0

PATA BUS

SATA BUS

LPC, 33MHZ

ACZ

USB2.0

PCI EXPRESS X1

ACZ

USB x1

LAN 1000

MINI CARD WLAN

HOST BUS

DDR2 SDRAM 533/667MHZ

DDR2 533/667 SODIMM X2

+1.8V +0.9VS P.14~P.15

DDR CAP/RES P.16

DCIN RTC FAN CON.

THERMAL SENSOR (MAX6657) P.06

USB2.0

PCI EXPRESS X1

ACZ

USB x1

LAN 1000 RTL8111B P.29

MINI CARD WLAN P.20

NEWCARD P.33

ESATA P.31

AC & BAT CON P.47

ACZ

USB2.0

PCI EXPRESS X1

ACZ

USB x1

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NEWCARD P.33

ESATA P.31

AC & BAT CON P.47

ACZ

USB2.0

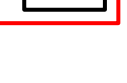
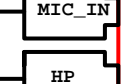
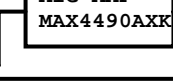
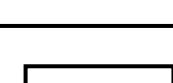
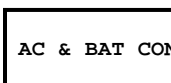
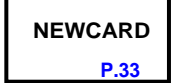
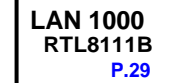
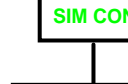
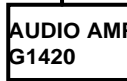
PCI EXPRESS X1

ACZ

USB x1

LAN 1000

Daughter Board



<Variant Name>

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	PWRLIMIT#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	I
31	ECSC#/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FANO_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/O
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPIO	ICH8_PWROK	O
149	GP1	ALL_SYS_PWRGD	I
152	GP2	BAT1_CNT2#	O
155	GP3	CHG_EN#	O
156	GP4	PRECHG	O
168	GP5	EC_CLK_EN	O
174	GP6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

ICH8M_GPIO

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i 0	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i H-Z	GPI	PCI_INT[H:E]#	+3VS	IRQ[H:E]#
GPIO 06	i 0	GPO	BIOS_REC_?_(TP)	+3VS	TACH2
GPIO 07	i 0	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i	GPI	EXTSM#	+3VSUS	N/A
GPIO 09	i H-Z	GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i H-Z	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SC#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i H-Z	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat	Native	STP_PC#	+3VSUS	STP_PC# , No GPIO in Mobile
GPIO 16	Nat	Native	PM DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i 1	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O freq	GPO	N/A	+3VS	N/A
GPIO 19	i H-Z	GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O 1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat	Native	N/A	+3VS	LDRO1#
GPIO 24	O H-Z	GPO	MSK_PCIRST	+3VSUS	ELGPIO0(MEM_LED) , Not Cleared by CF9h RST event.
GPIO 25	Nat	Native	STP_CPU#	+3VS	STP_CPU# , No GPIO in Mobile
GPIO 26	Nat	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O 0	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O 0	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O 0	Native	PM_CLKRUN#	+3VS	CLKRUN# , No GPIO in Mobile
GPIO 33	O 1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O 0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O 0	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i 0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 39	i	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a	N/A	N/A	N/A	No implement
GPIO 48	i 1	Native	N/A	+3VS	SDATAOUT1
GPIO 49	Nat	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat	Native	PCI_GNT3#	+3VS	GNT3#

<Variant Name>

		Title :Schematic Info.	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	Rev	
Custom	F6E	1.10	
Date: Tuesday, August 21, 2007		Sheet	3 of 94

<Variant Name>



Title : MEROM CPU (2)

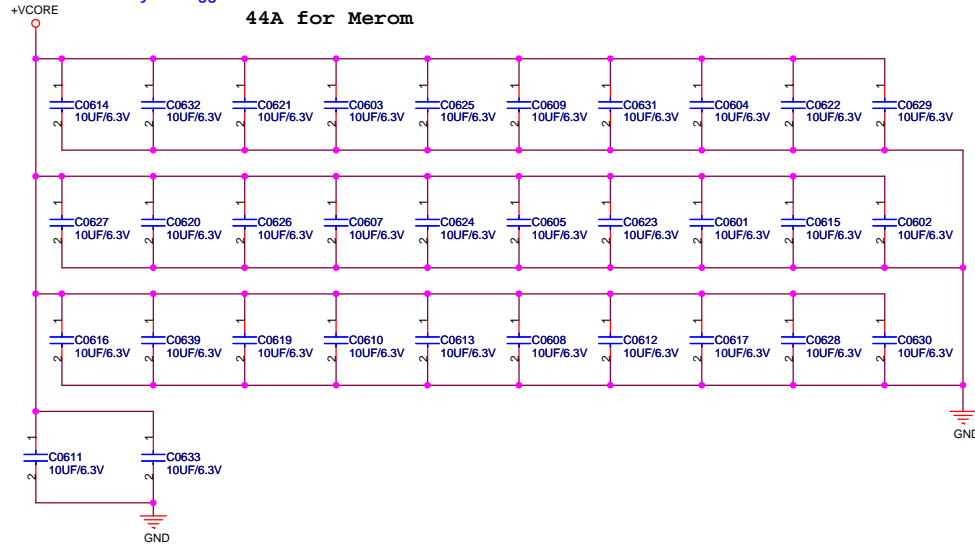
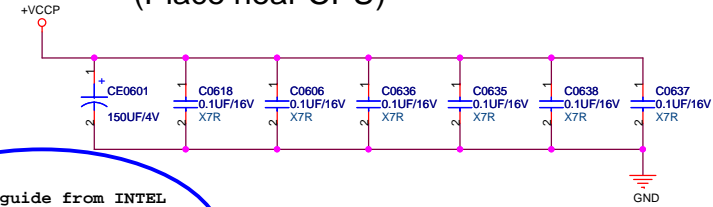
Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 5 of 94

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom

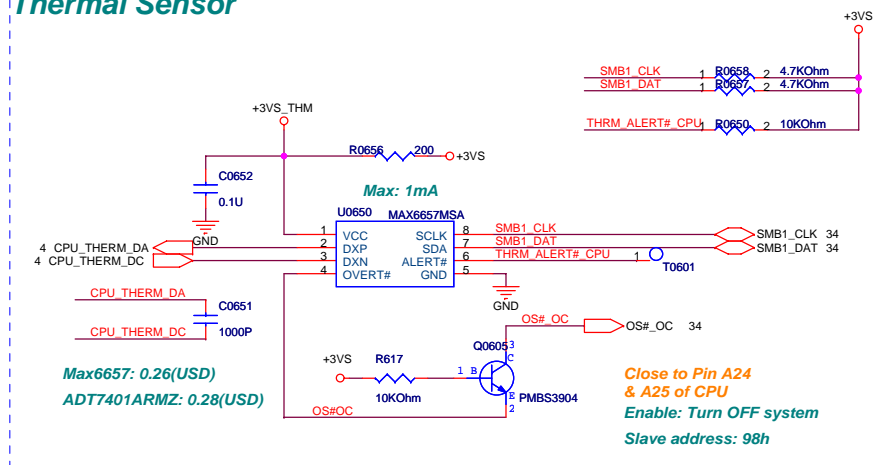
+VCCP Decoupling Capacitor
(Place near CPU)

Decoupling guide from INTEL

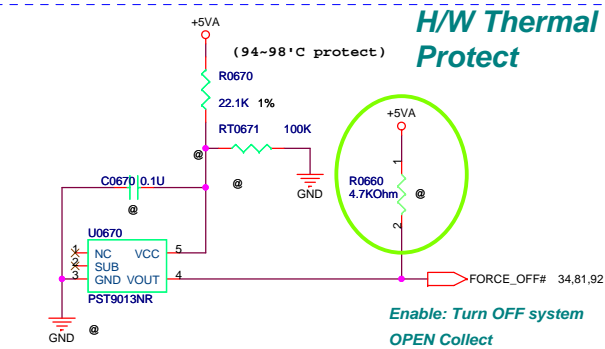
VCCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it ! _0907

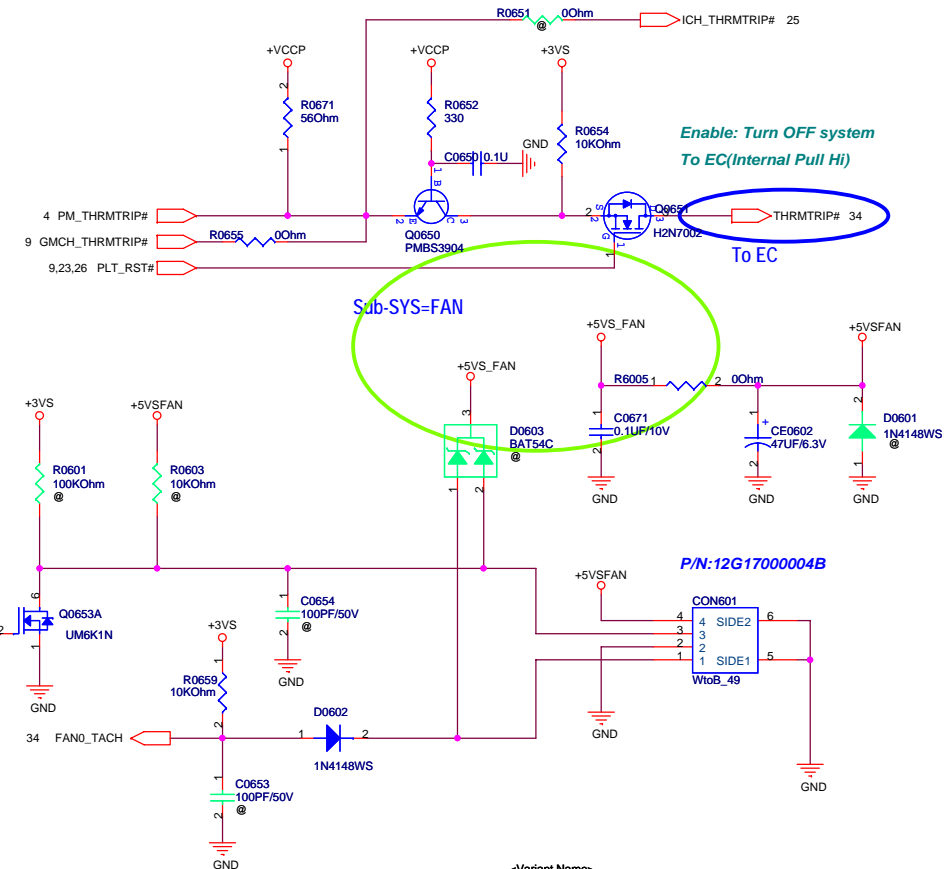
Thermal Sensor



H/W Thermal Protect



Sub-SYS=CPU



<Variant Name>

CPU CAP, Thermal Sensor

ASUSTeK COMPUTER INC

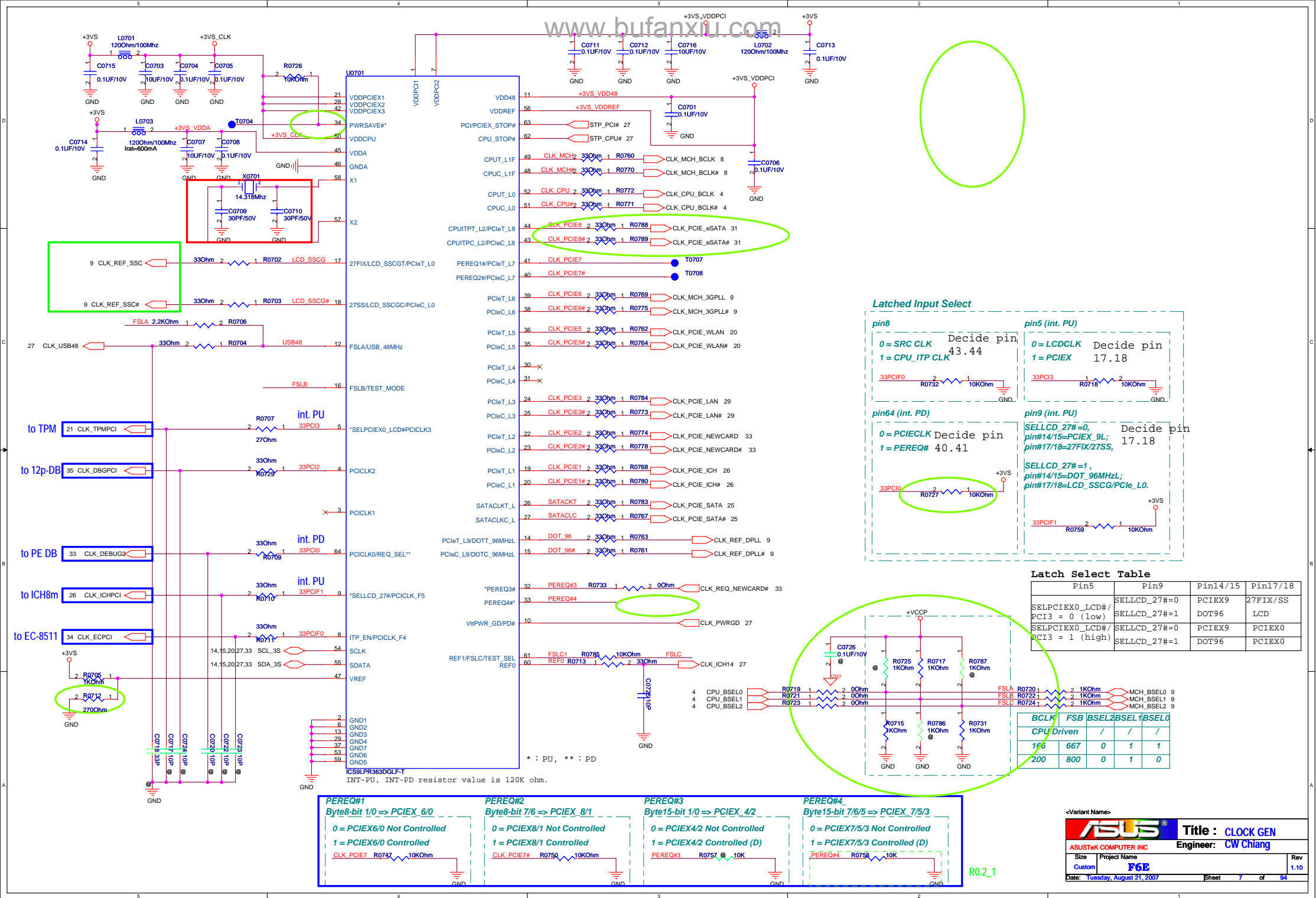
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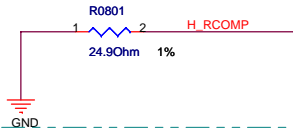
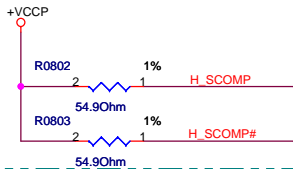
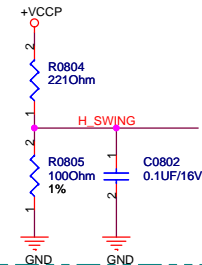
Engineer: CW Chiang

Size
CustomProject Name
F6ERev
1.10

Date: Tuesday, August 21, 2007

Sheet 6 of 94



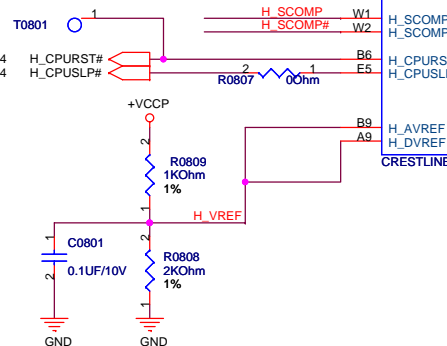
4 H_D#[63:0]  H_D#[63:0]4 H_A#[35:3]  H_A#[35:3]**RCOMP***For Calibrating the FSB I/O Buffer***SCOMP***For Slew Rate Compensation on the FSB***Voltage Swing***For Providing a Reference Voltage to The FSB RCOMP circuits*

U0801A

H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G7	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	Y8	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	N5	H_D#_21
H_D#22	N3	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD9	H_D#_34
H_D#35	AC9	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AB2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	Y3	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AG3	H_D#_47
H_D#48	AJ9	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AJ6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ7	H_D#_58
H_D#59	AJ2	H_D#_59
H_D#60	AE5	H_D#_60
H_D#61	AJ3	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

ISOH_SWING B3
H_RCOMP C2H_SCOMP W1
H_SCOMP# W2H_CPURST# B6
H_CPUSLP# E5H_AVREF B9
H_DVREF A9

CRESTLINE_965GM



H_A#_3	J13	H_A#3
H_A#_4	B11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	F16	H_A#8
H_A#_9	L13	H_A#9
H_A#_10	C17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	K16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L16	H_A#14
H_A#_15	J17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	R17	H_A#19
H_A#_20	B16	H_A#20
H_A#_21	H20	H_A#21
H_A#_22	L19	H_A#22
H_A#_23	D17	H_A#23
H_A#_24	M17	H_A#24
H_A#_25	N16	H_A#25
H_A#_26	J19	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	E19	H_A#28
H_A#_29	B17	H_A#29
H_A#_30	B15	H_A#30
H_A#_31	E17	H_A#31
H_A#_32	C18	H_A#32
H_A#_33	A19	H_A#33
H_A#_34	B19	H_A#34
H_A#_35	N19	H_A#35

H_ADS#	G12	H_ADS#	H_ADS# 4
H_ADSTB#_0	H17	H_ADSTB#0	H_ADSTB#0 4
H_ADSTB#_1	G20	H_ADSTB#1	H_ADSTB#1 4
H_BNR#	C8	H_BNR#	H_BNR# 4
H_BPRI#	E8	H_BPRI#	H_BPRI# 4
H_BREQ#	F12	H_BREQ#0	H_BREQ#0 4
H_DEFER#	D6	H_DEFER#	H_DEFER# 4
H_DBSY#	C10	H_DBSY#	H_DBSY# 4
HPLL_CLK	AM5	CLK_MCH_BCLK	CLK_MCH_BCLK 7
HPLL_CLK#	H8	H_DPWR#	CLK_MCH_BCLK# 7
H_DPWR#	K7	H_DRDY#	H_DPWR# 4
H_DRDY#	E4	H_HIT#	H_DRDY# 4
H_HIT#	C6	H_HITM#	H_HIT# 4
H_HITM#	G10	H_LOCK#	H_HITM# 4
H_LOCK#	B7	H_TRDY#	H_LOCK# 4
H_TRDY#			

H_DINV#_0	K5	H_DINV#0	H_DINV#0 4
H_DINV#_1	L2	H_DINV#1	H_DINV#1 4
H_DINV#_2	AD13	H_DINV#2	H_DINV#2 4
H_DINV#_3	AE13	H_DINV#3	H_DINV#3 4

H_DSTBN#_0	M7	H_DSTBN#0	H_DSTBN#0 4
H_DSTBN#_1	K3	H_DSTBN#1	H_DSTBN#1 4
H_DSTBN#_2	AD2	H_DSTBN#2	H_DSTBN#2 4
H_DSTBN#_3	AH11	H_DSTBN#3	H_DSTBN#3 4

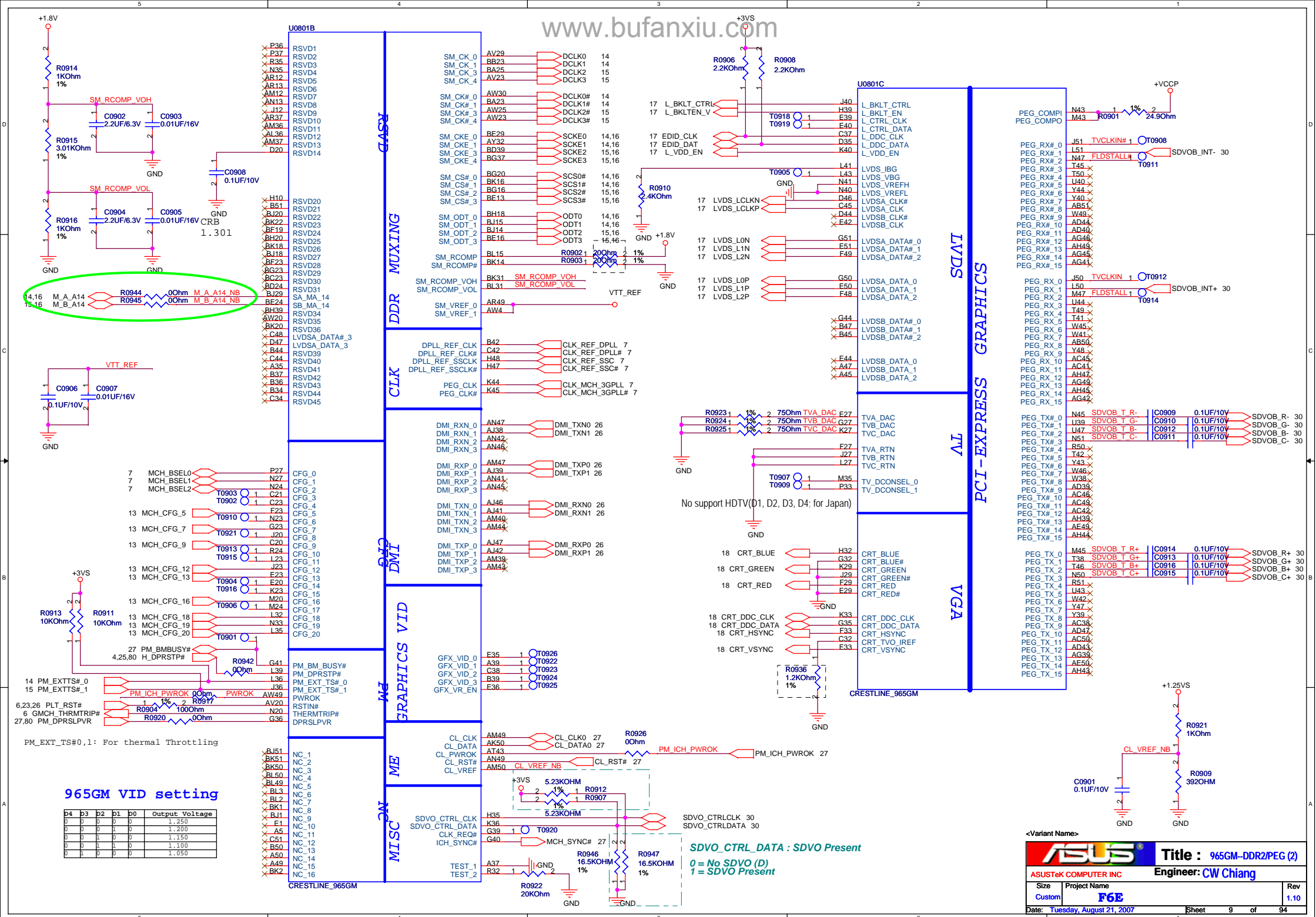
H_DSTBP#_0	L7	H_DSTBP#0	H_DSTBP#0 4
H_DSTBP#_1	K2	H_DSTBP#1	H_DSTBP#1 4
H_DSTBP#_2	AC2	H_DSTBP#2	H_DSTBP#2 4
H_DSTBP#_3	AJ10	H_DSTBP#3	H_DSTBP#3 4

H_REQ#_0	M14	H_REQ#0	
H_REQ#_1	E13	H_REQ#1	
H_REQ#_2	A11	H_REQ#2	
H_REQ#_3	H13	H_REQ#3	
H_REQ#_4	B12	H_REQ#4	

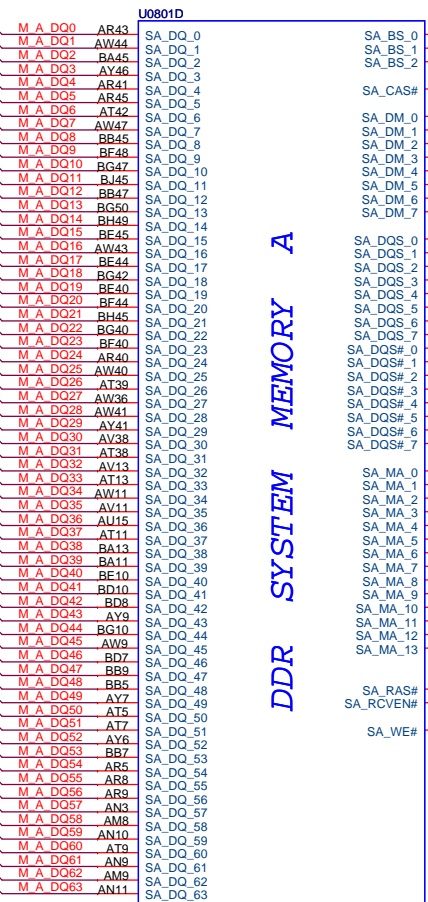
H_RS#_0	E12	H_RS#0	H_RS#0 4
H_RS#_1	D7	H_RS#1	H_RS#1 4
H_RS#_2	D8	H_RS#2	H_RS#2 4

4 H_REQ#[4:0]  H_REQ#[4:0]

<Variant Name>



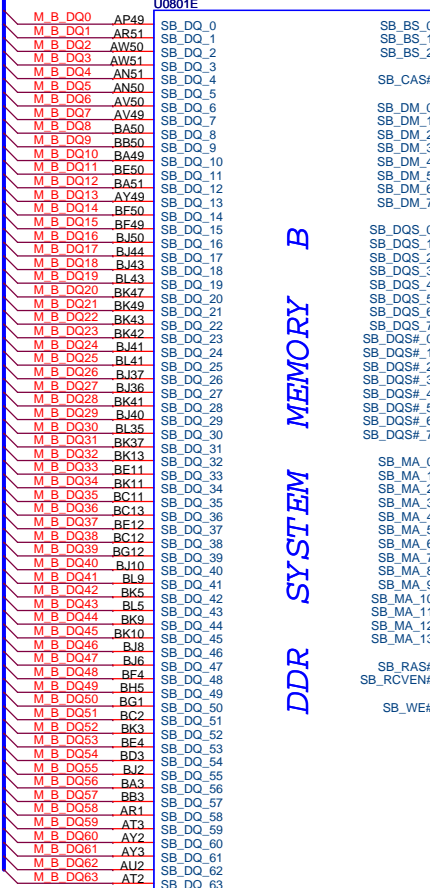
14 M_A_DQ[0:63]



CRESTLINE_965GM

DDR SYSTEM MEMORY A

15 M_B_DQ[0:63]



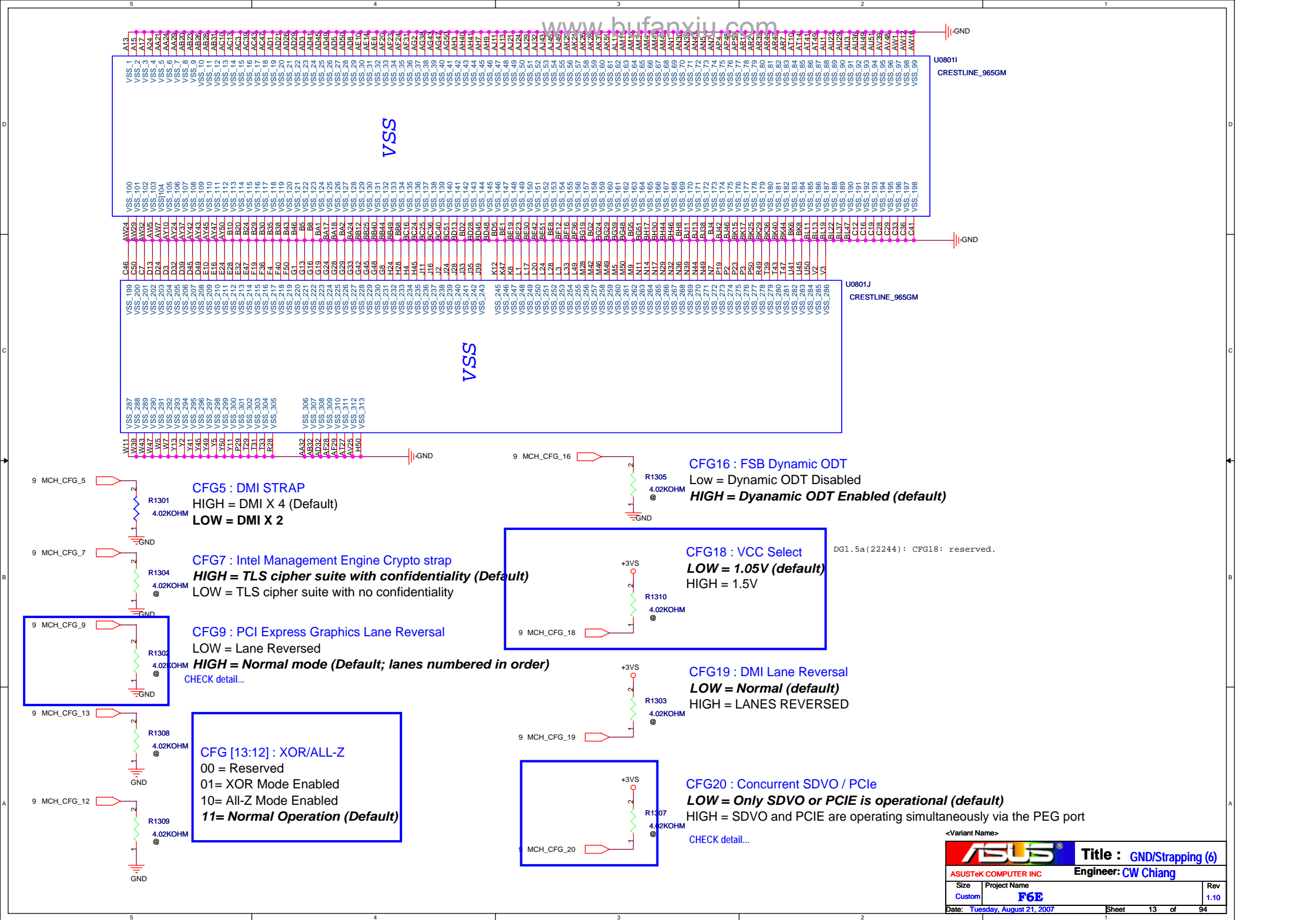
CRESTLINE_965GM

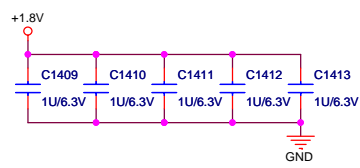
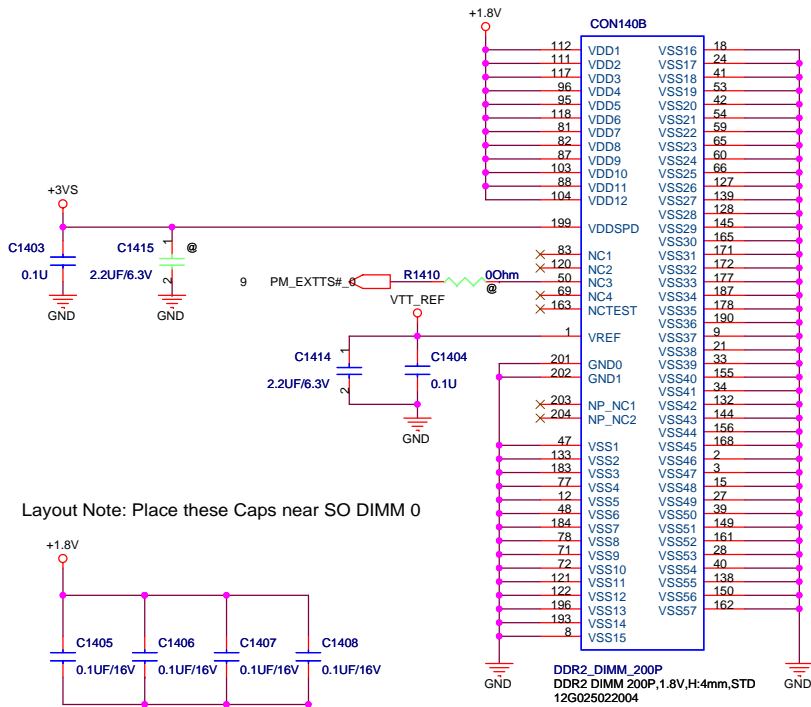
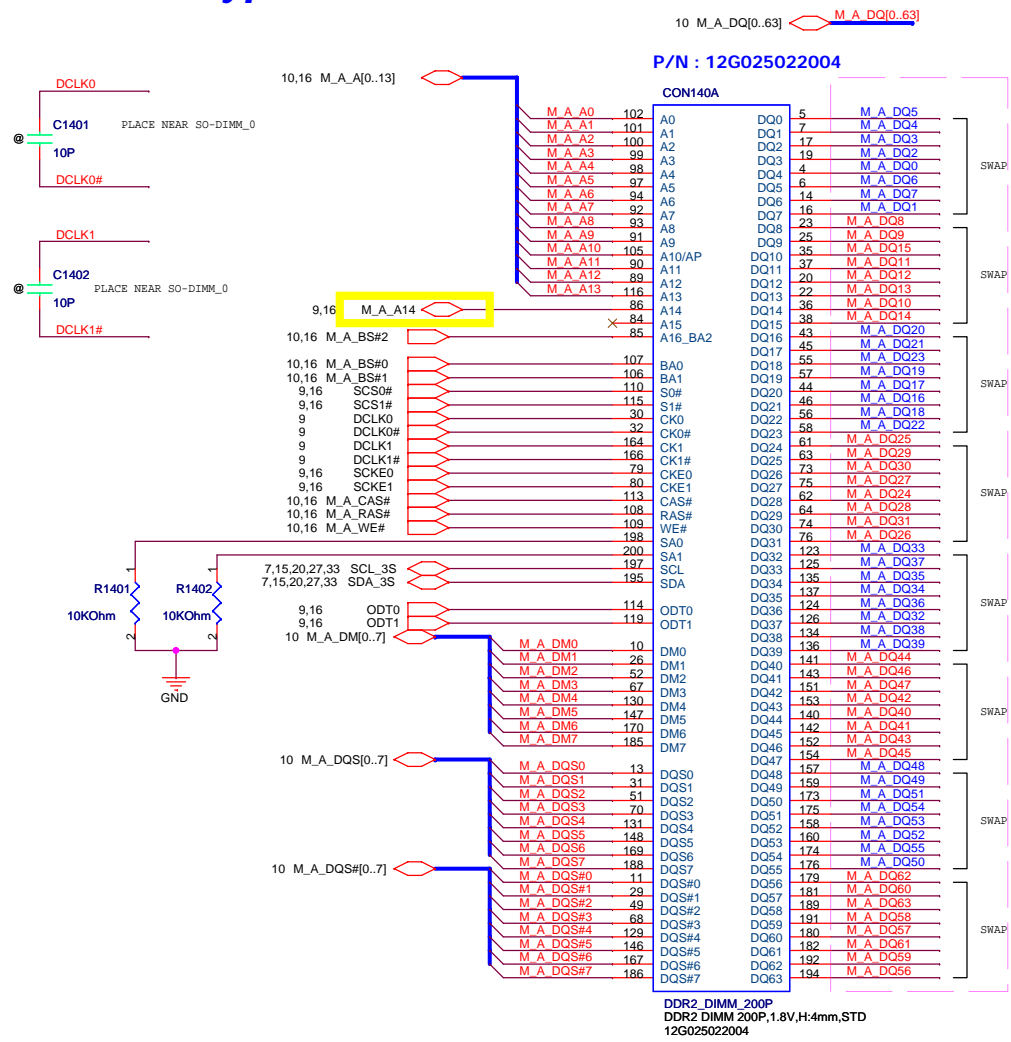
DDR SYSTEM MEMORY B

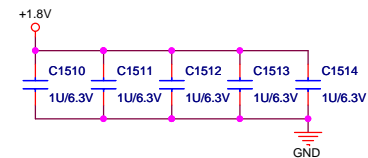
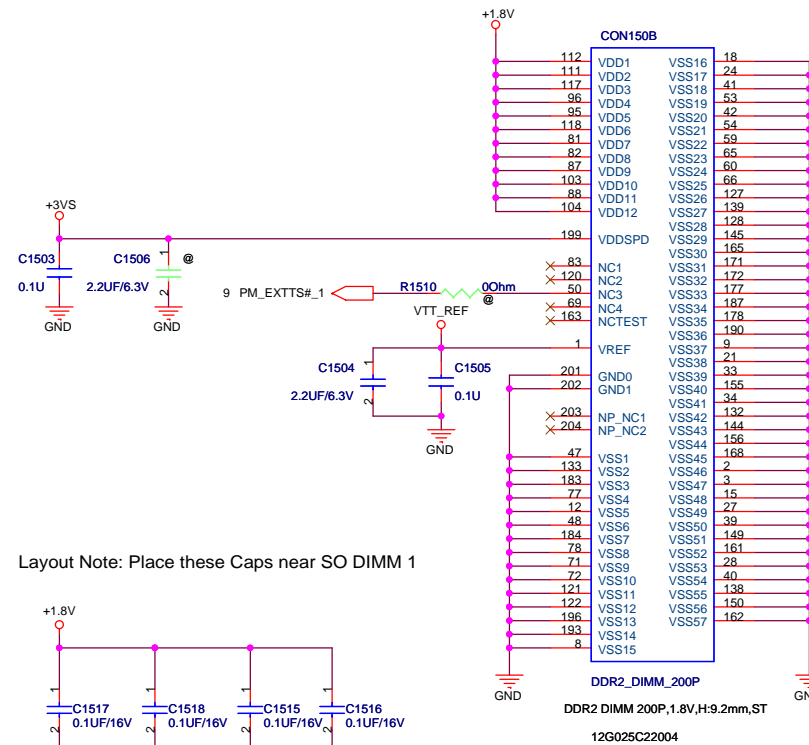
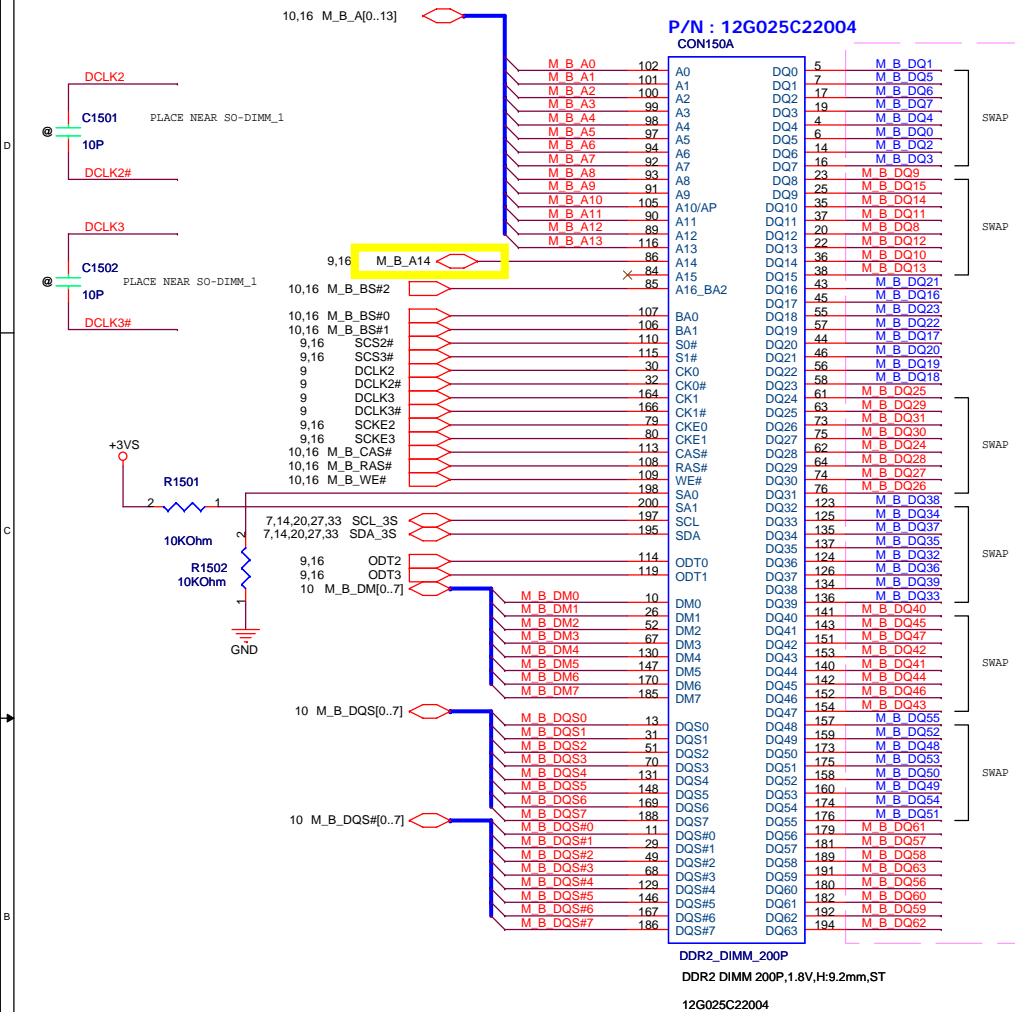
<Variant Name>

ASUS		Title : 965GM-DDR2 bus (3)	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	Rev	
Custom	F6E	1.10	
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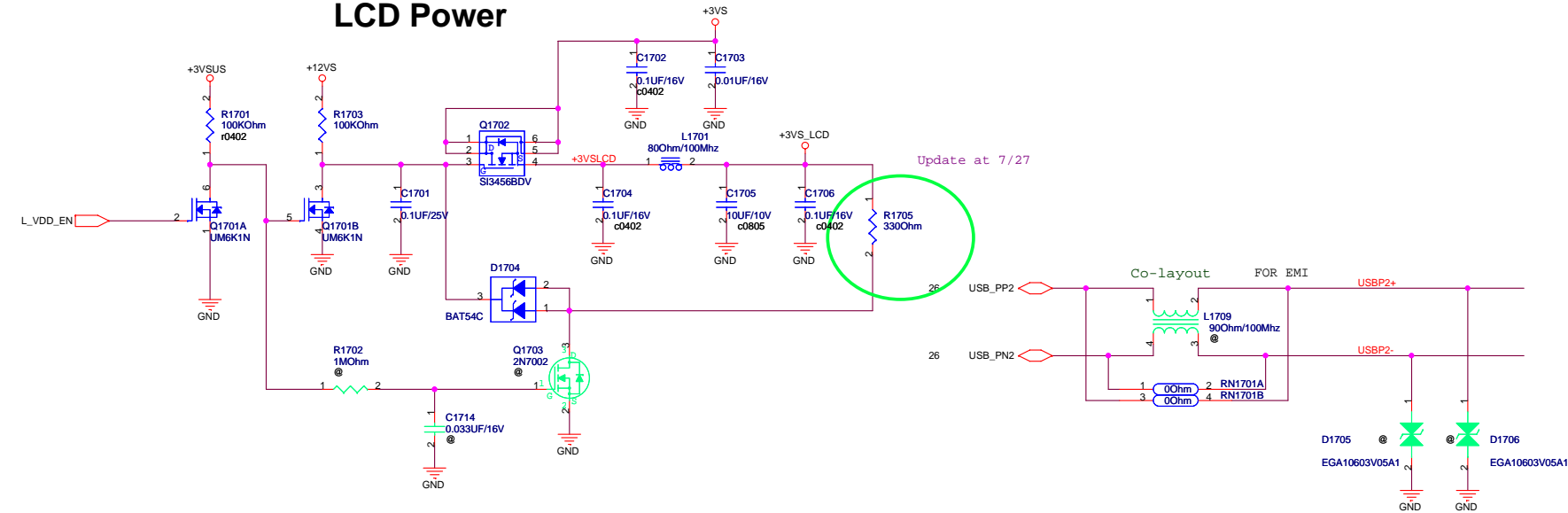






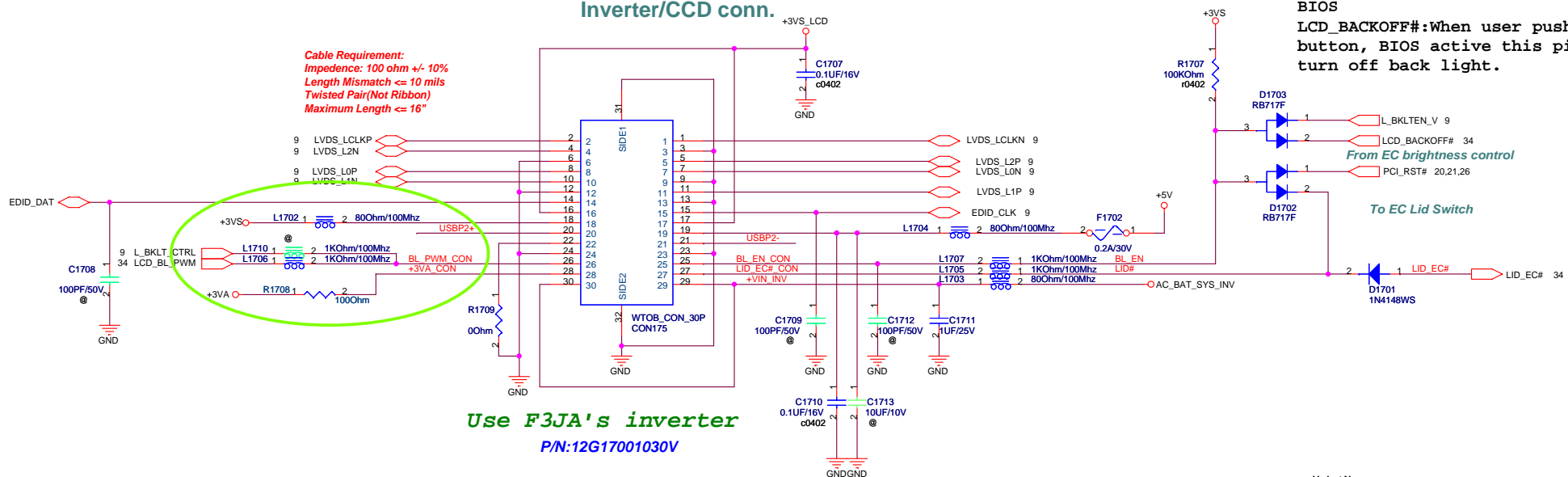
<Variant Name>

LCD Power



Inverter/CCD conn.

Cable Requirement:
 Impedence: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"



BIOS
 LCD_BACKOFF#: When user push "Fn+F7"
 button, BIOS active this pin to
 turn off back light.

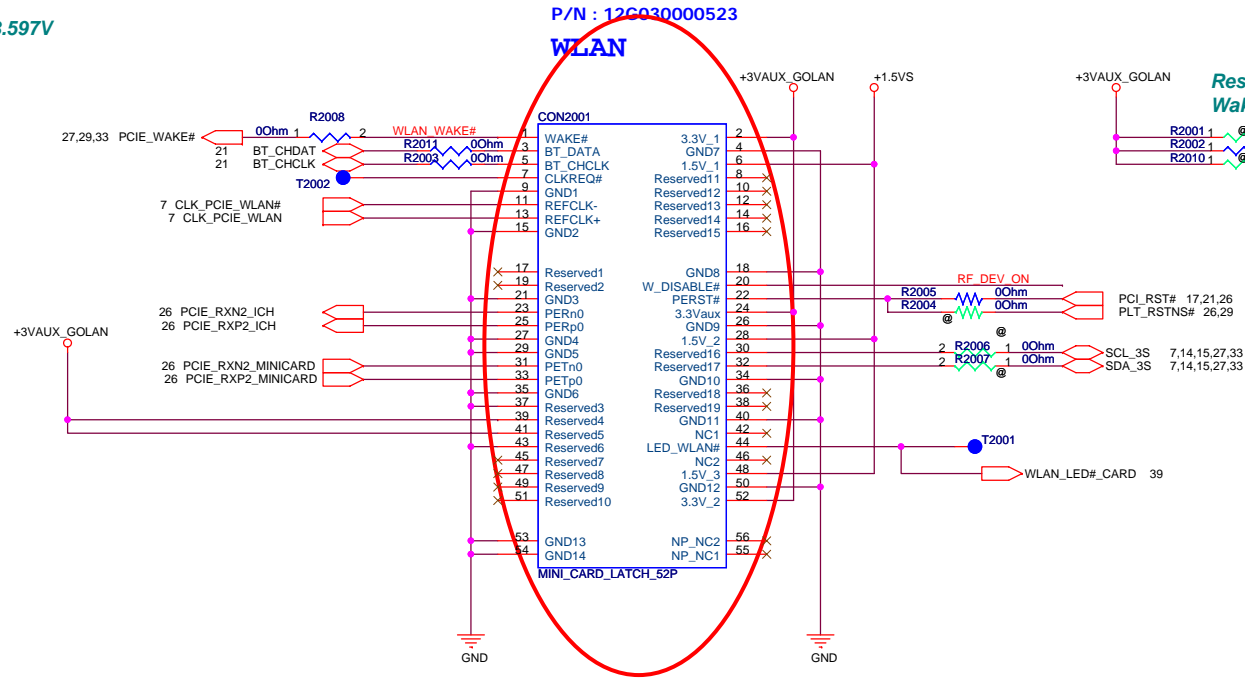
From EC brightness control

To EC Lid Switch

<Variant Name>

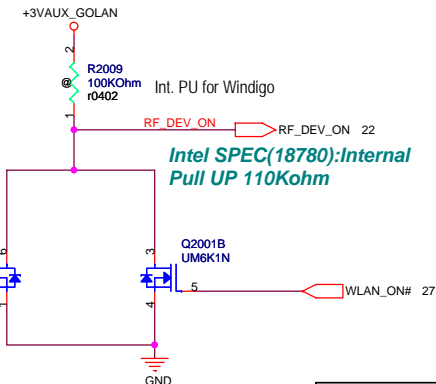
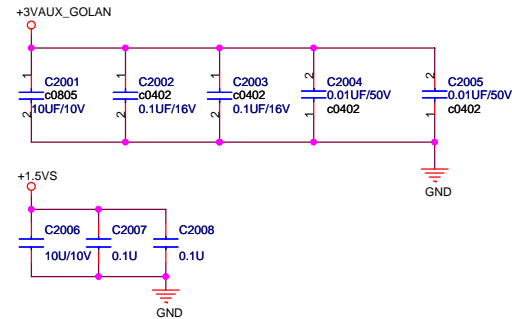
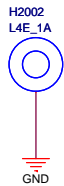
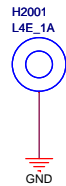
+3VAUX_GOLAN: +3.003V~+3.597V
Max= 1100 mA

+1.5VS: +1.425V~+1.575V
Max= 375 mA

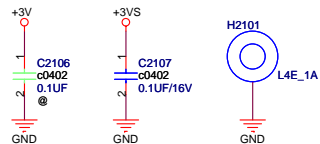
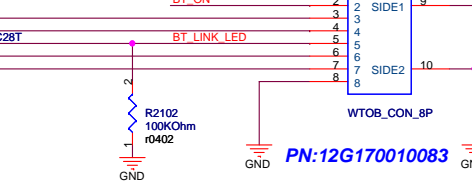


Reserved R to +3VSUS for Wake on WLAN function!

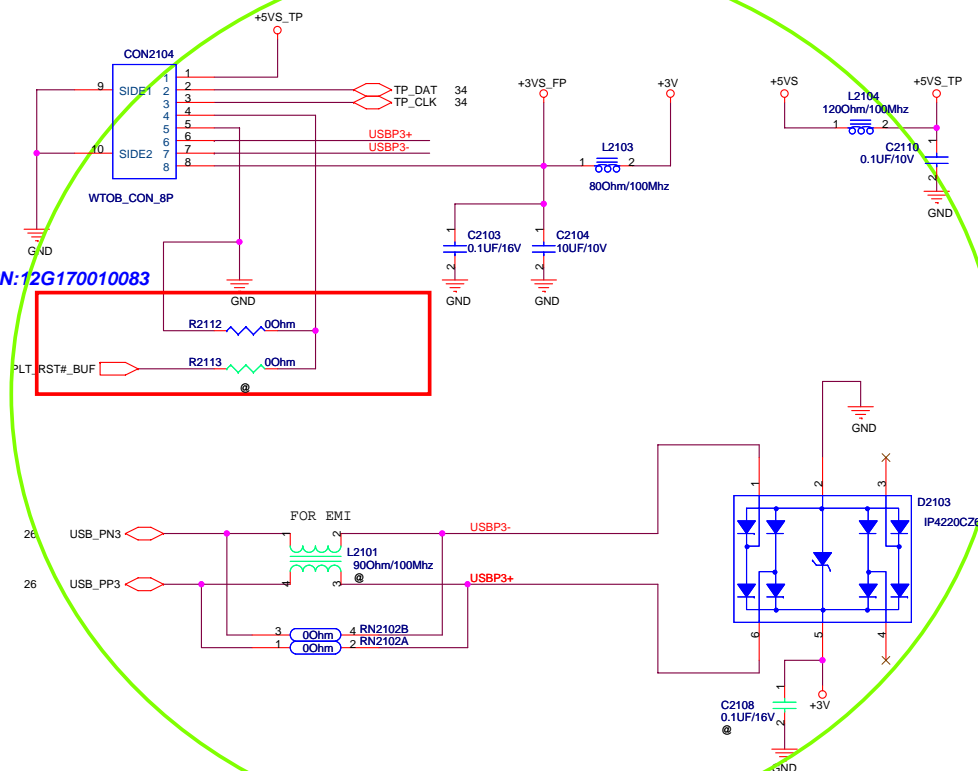
+1.5VS 5,12,25,28,33,37,82
 +3V 19,21,22,26,33,35,37,91
 +3VS 6,7,9,12,13,14,15,17,18,19,21,22,23,25,27,28,29,30,31,33,34,37,38,39,80,91,92



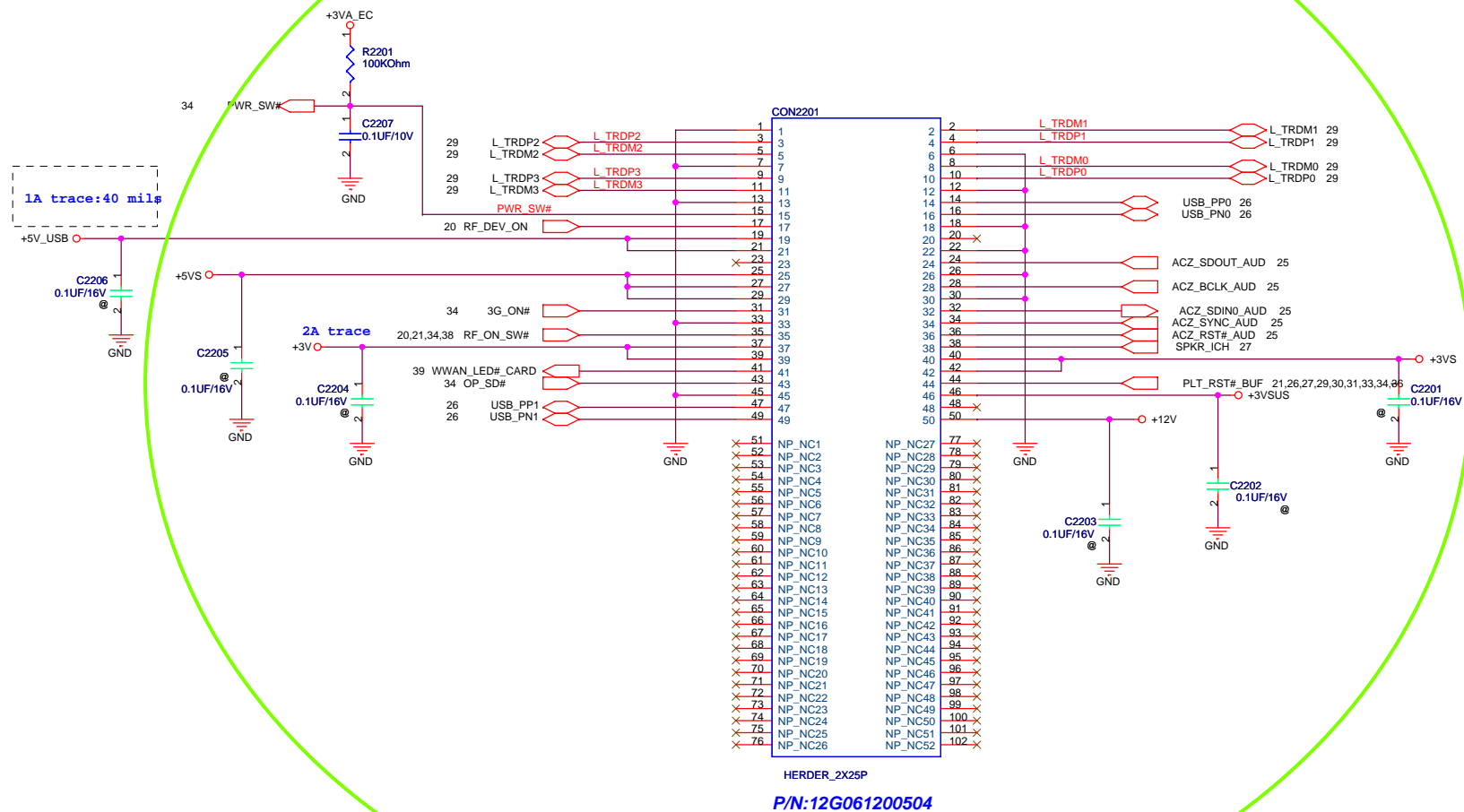
For Intel Wireless
CoExistence System



PN:12G170010083



<Variant Name>





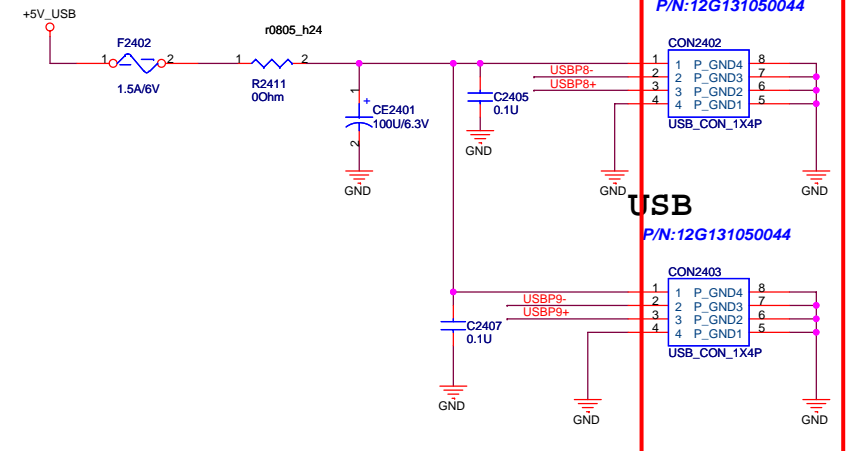
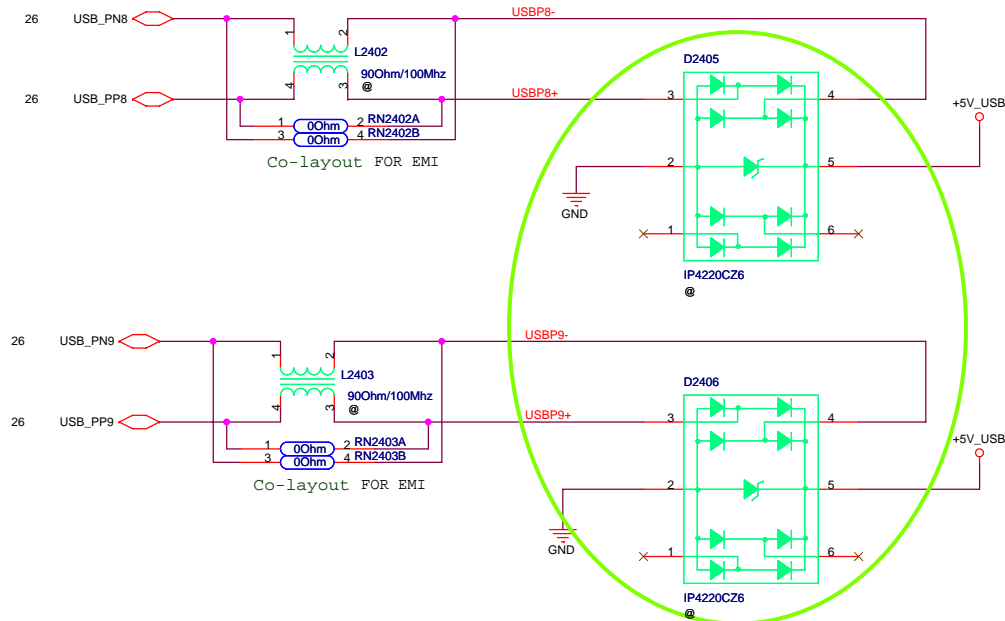
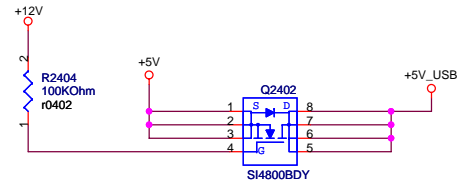
Engineer: CW Chiang

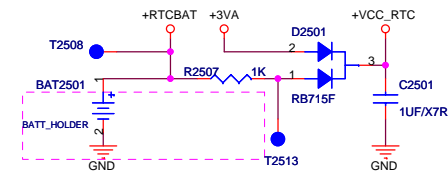
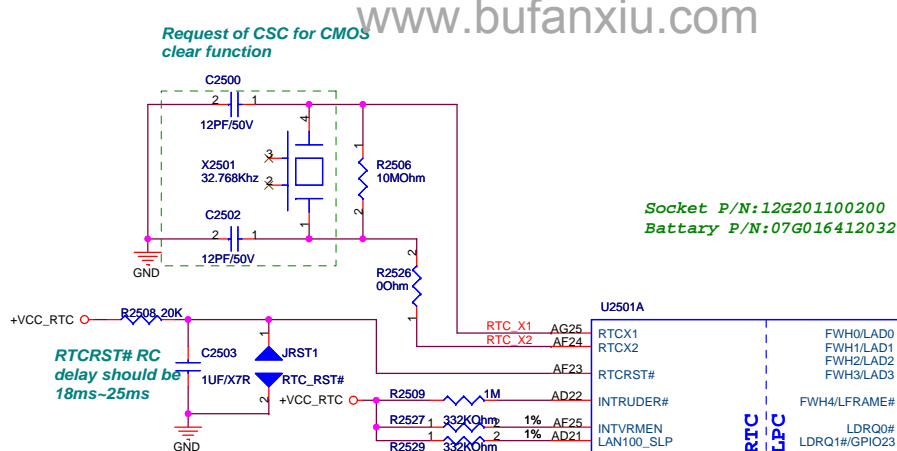
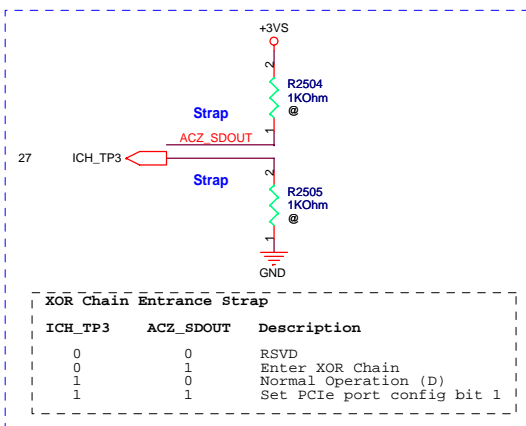
Rev	
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1.

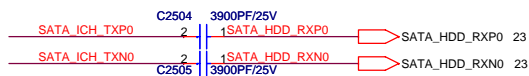
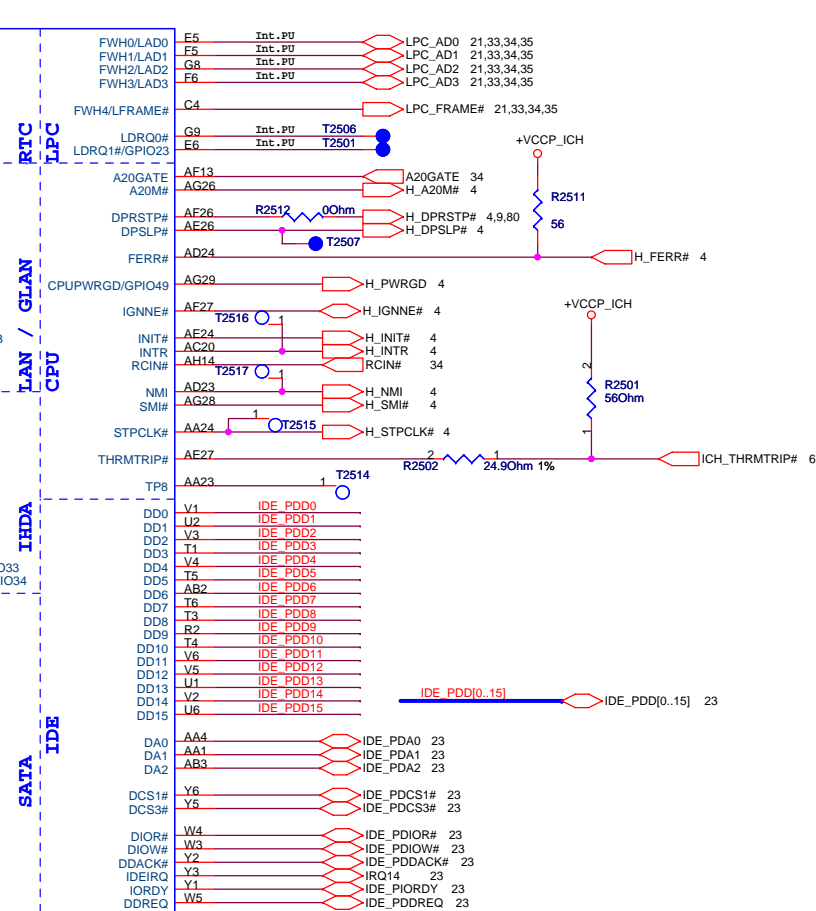
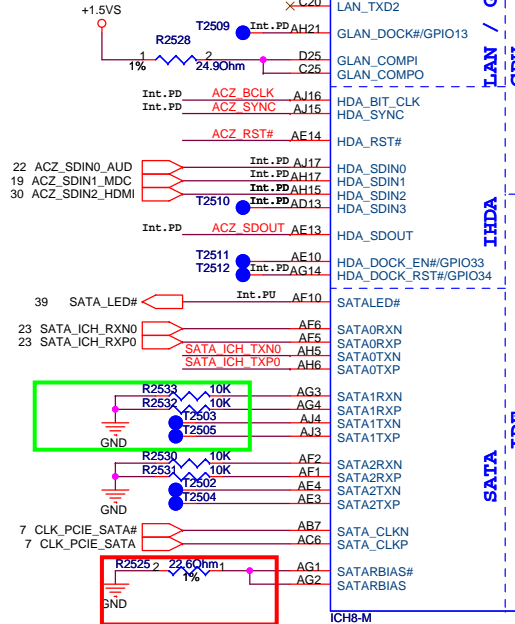
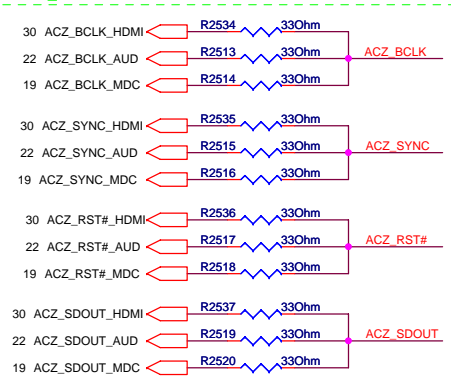
Sheet 23 of 94

<Variant Name>



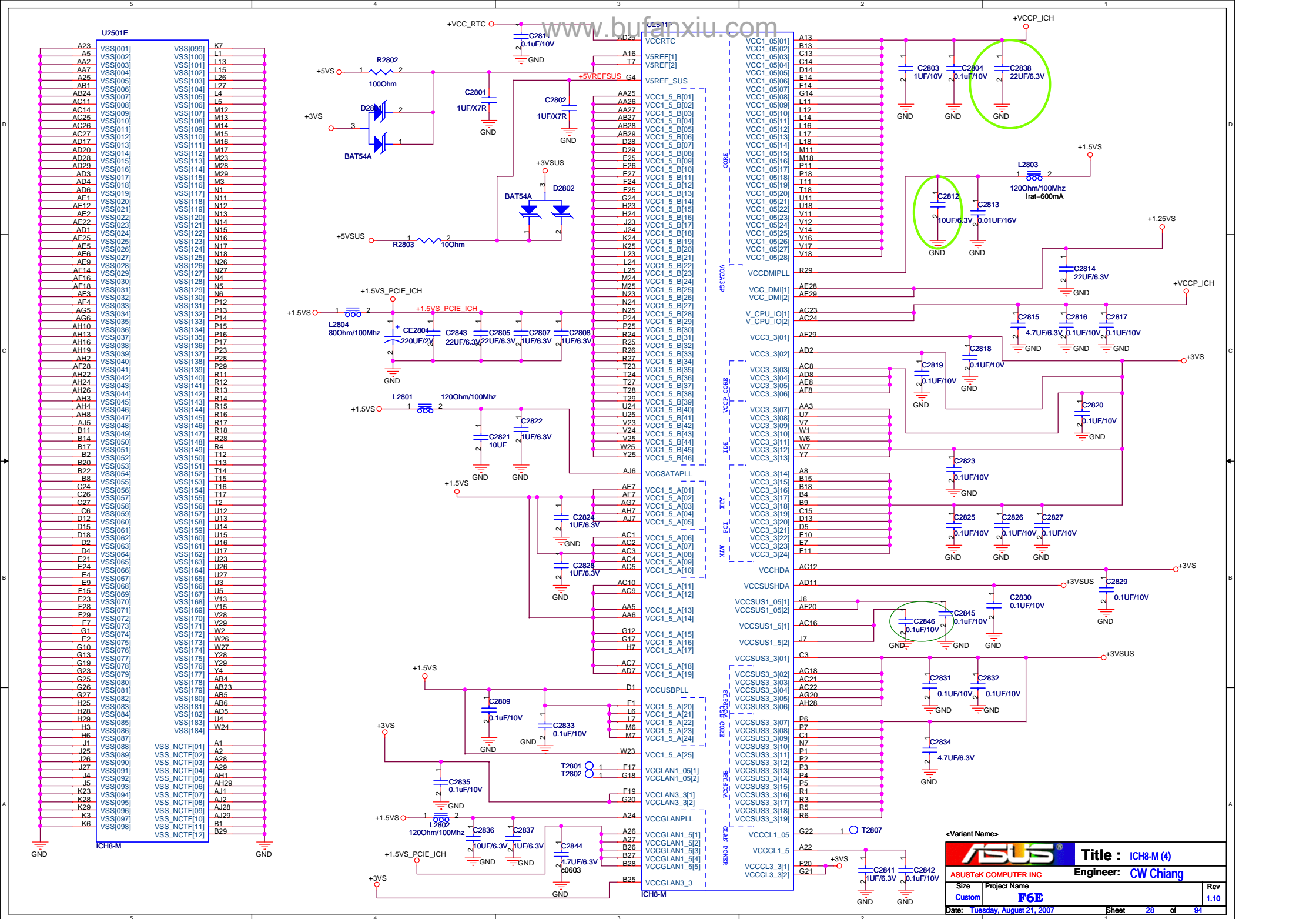


R0.2_4



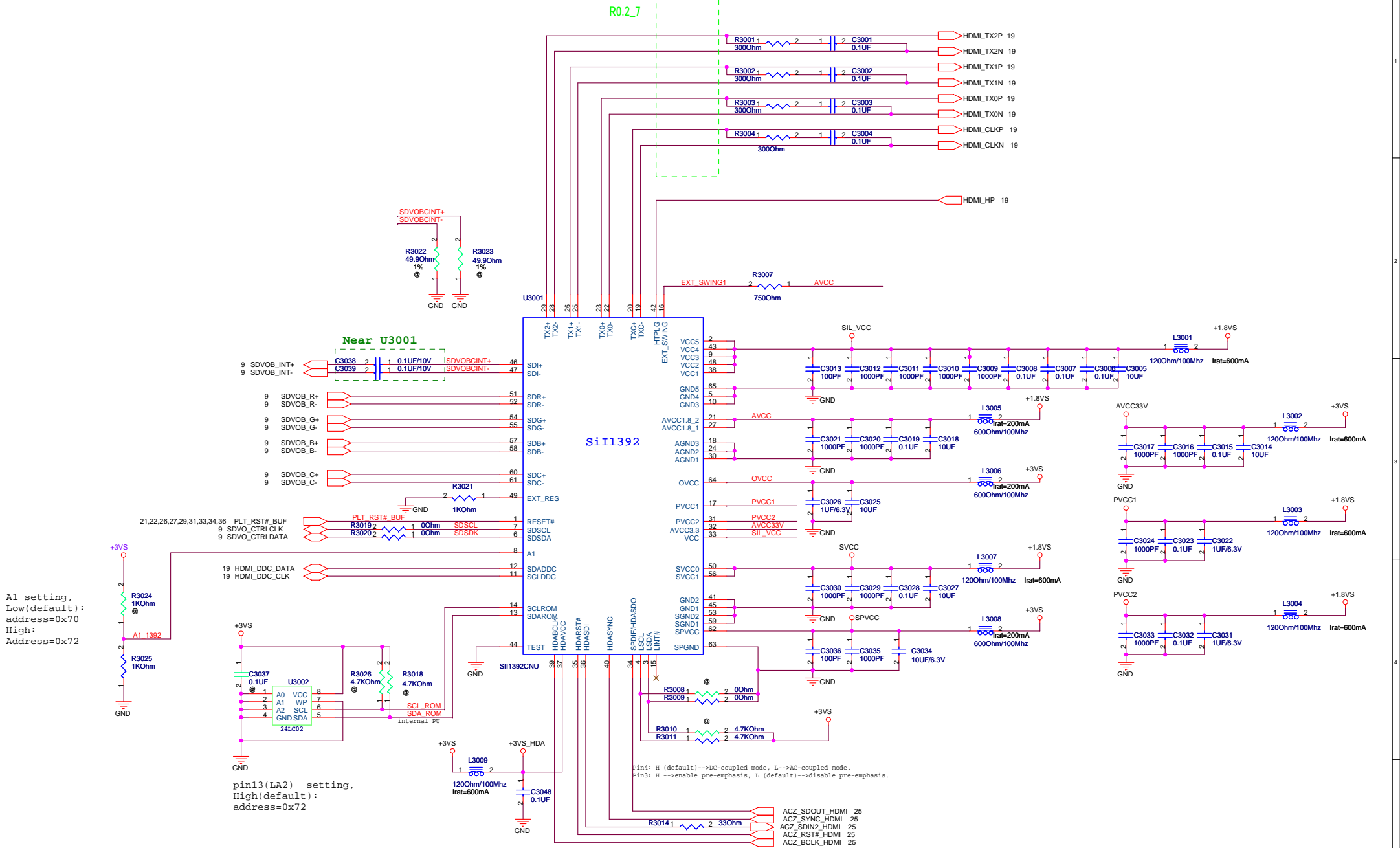
<=> SATA HDD

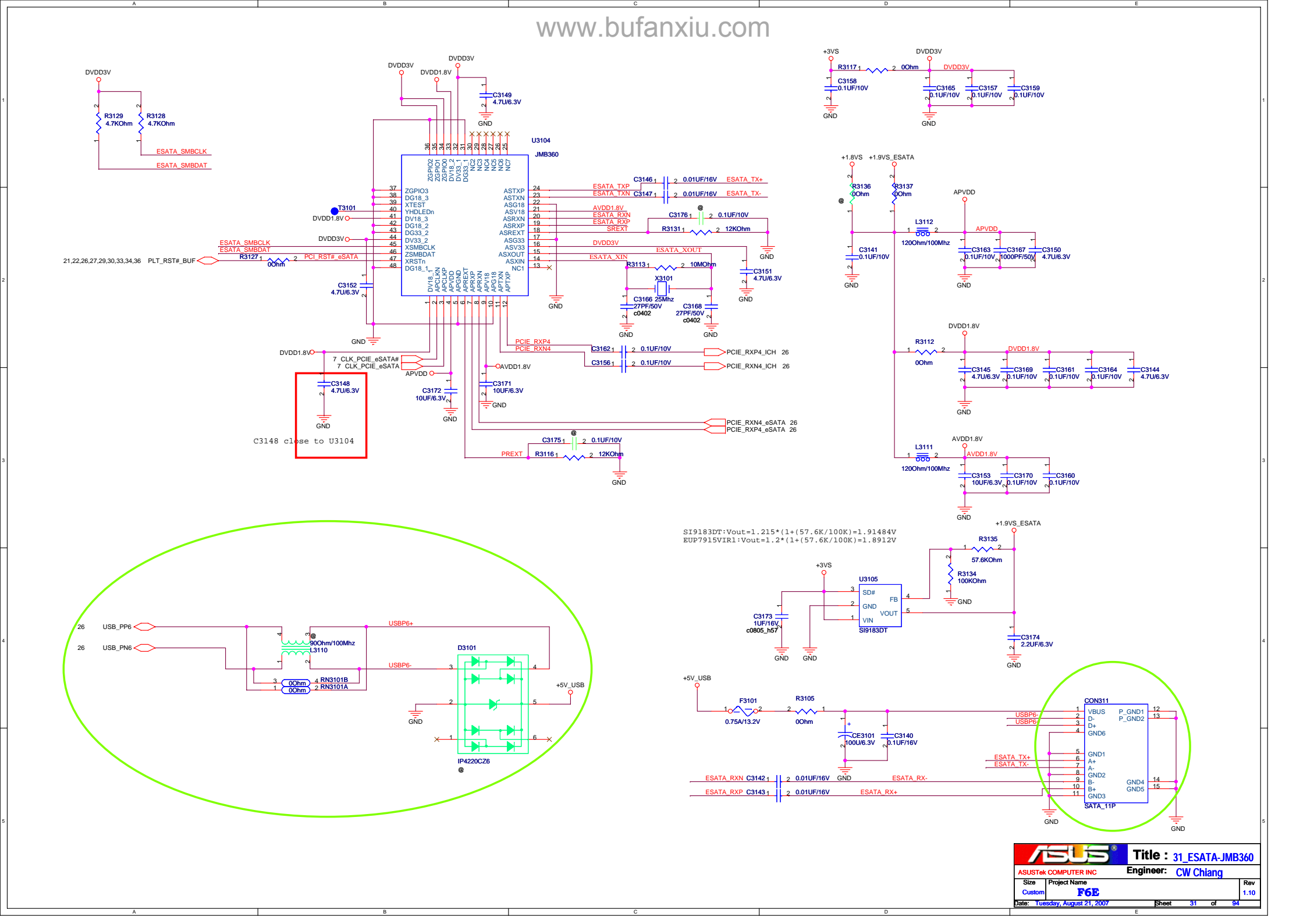
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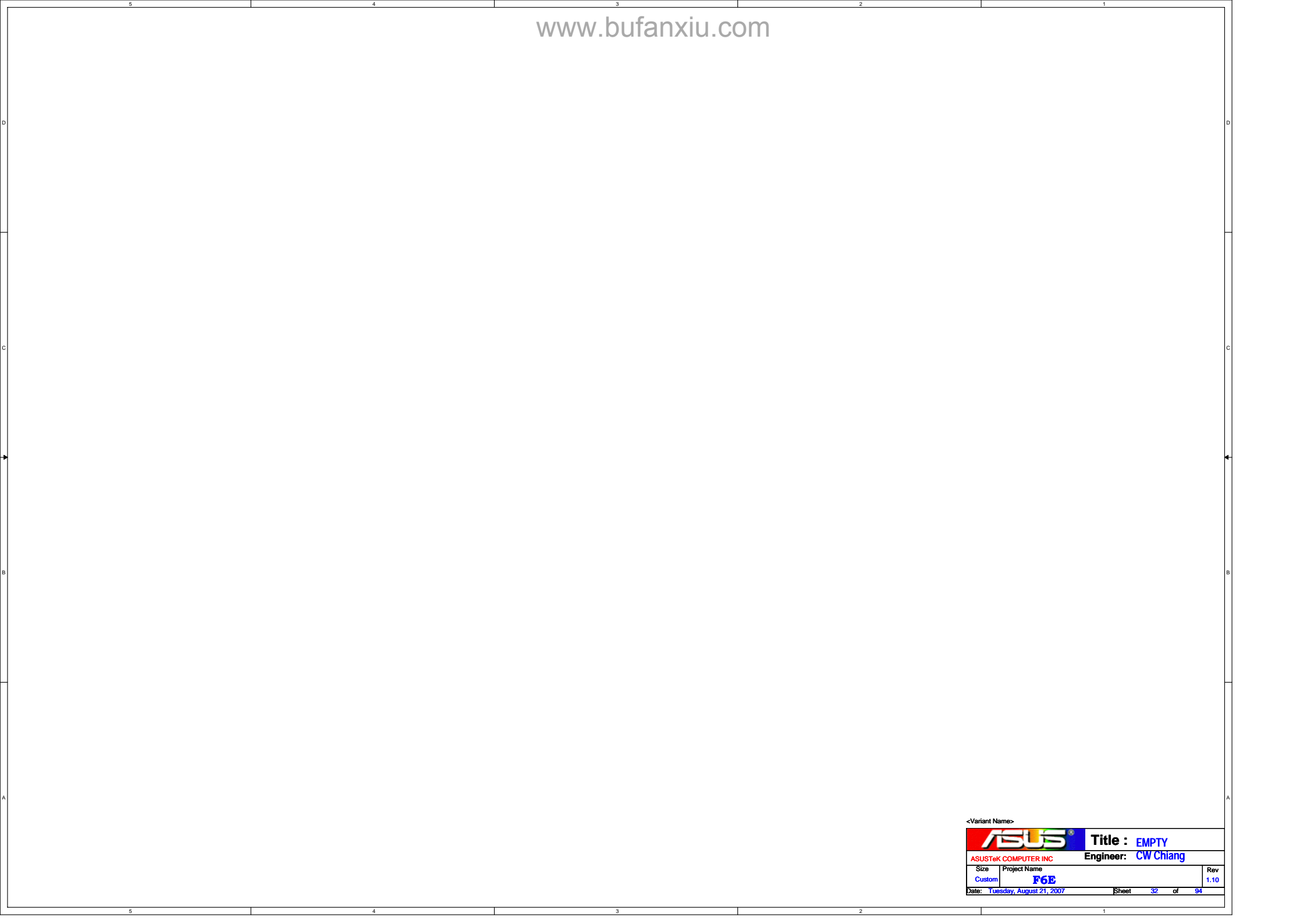




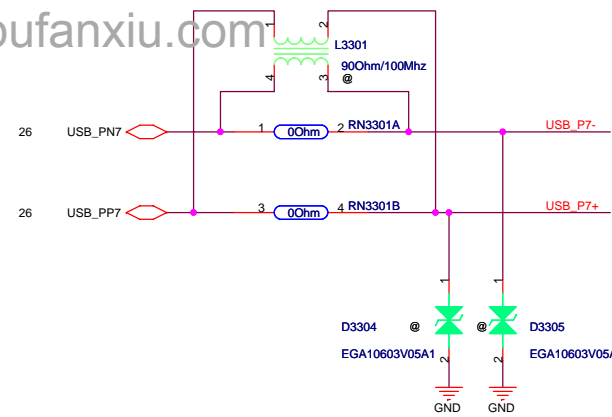
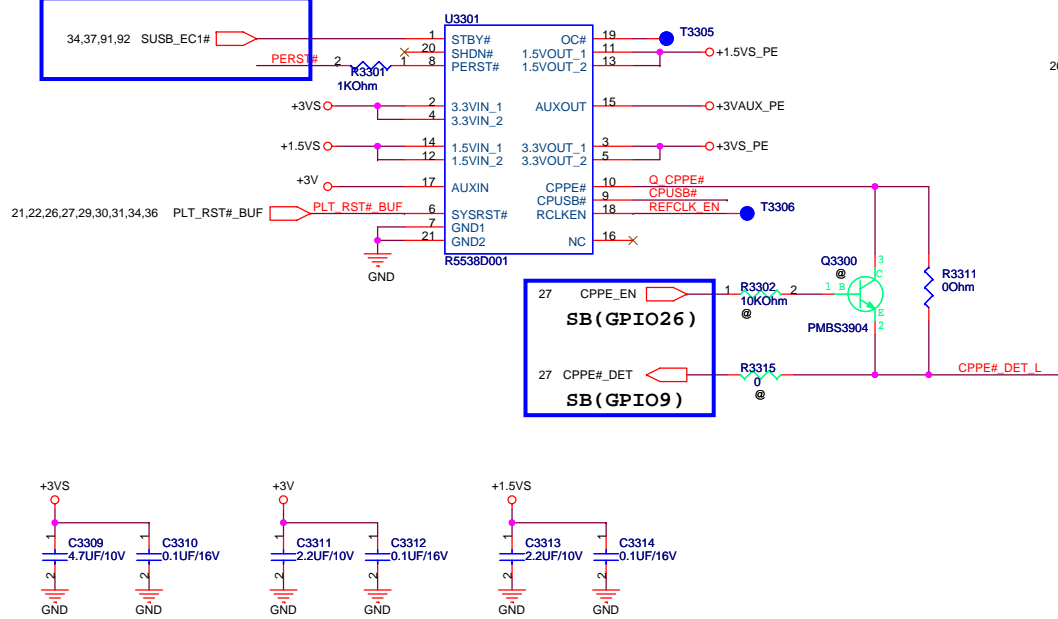
R0.2.7



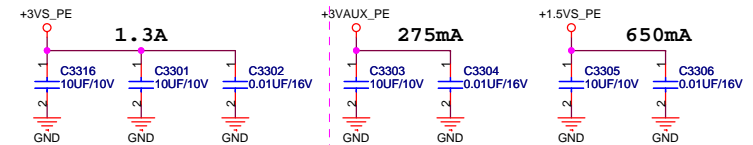
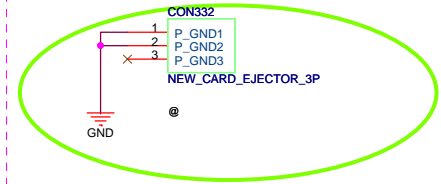
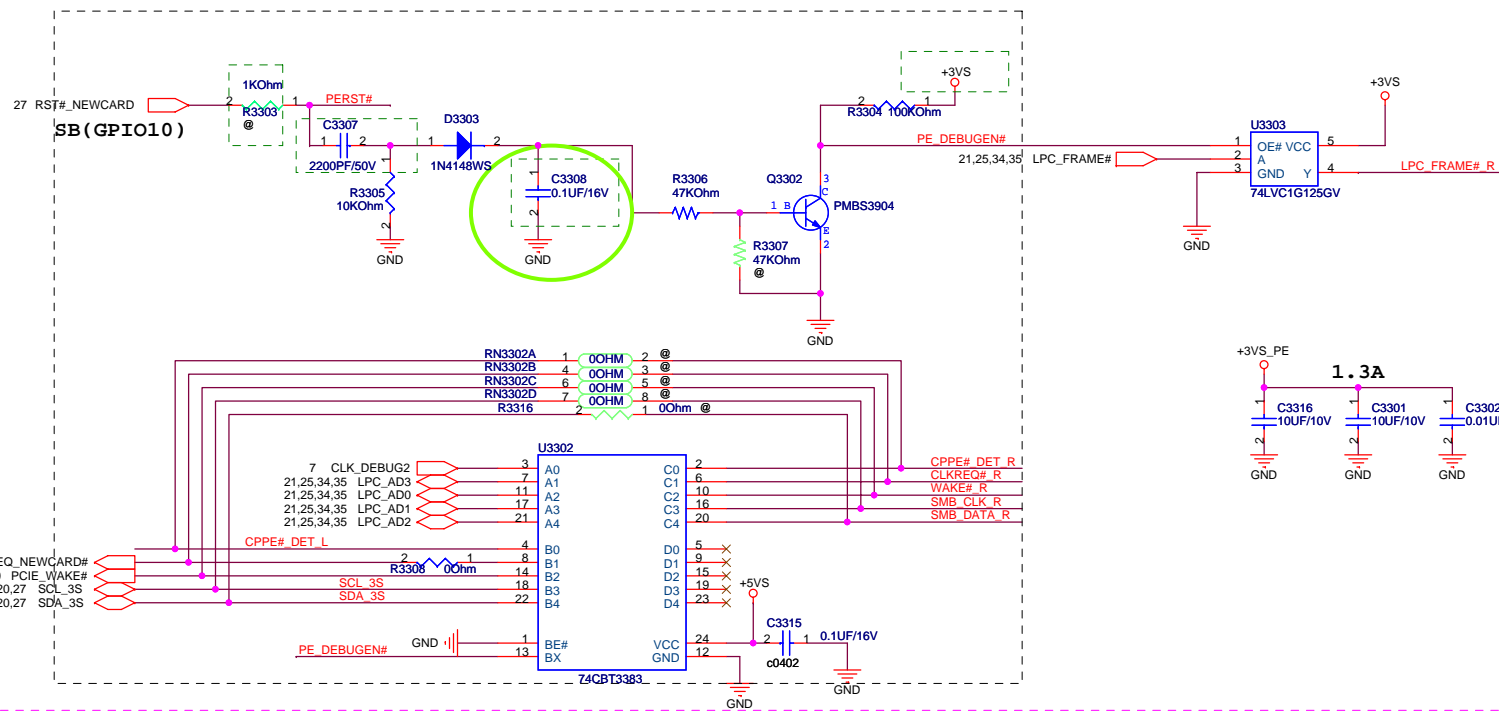
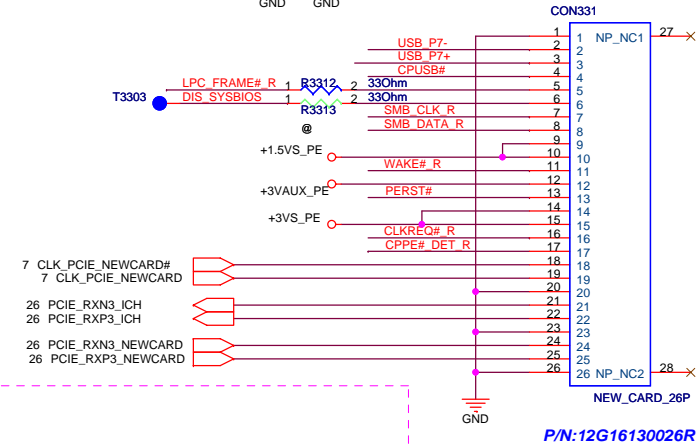




New EC pin to avoid the re-recognize when resume from S3/S4...



NewCard Header

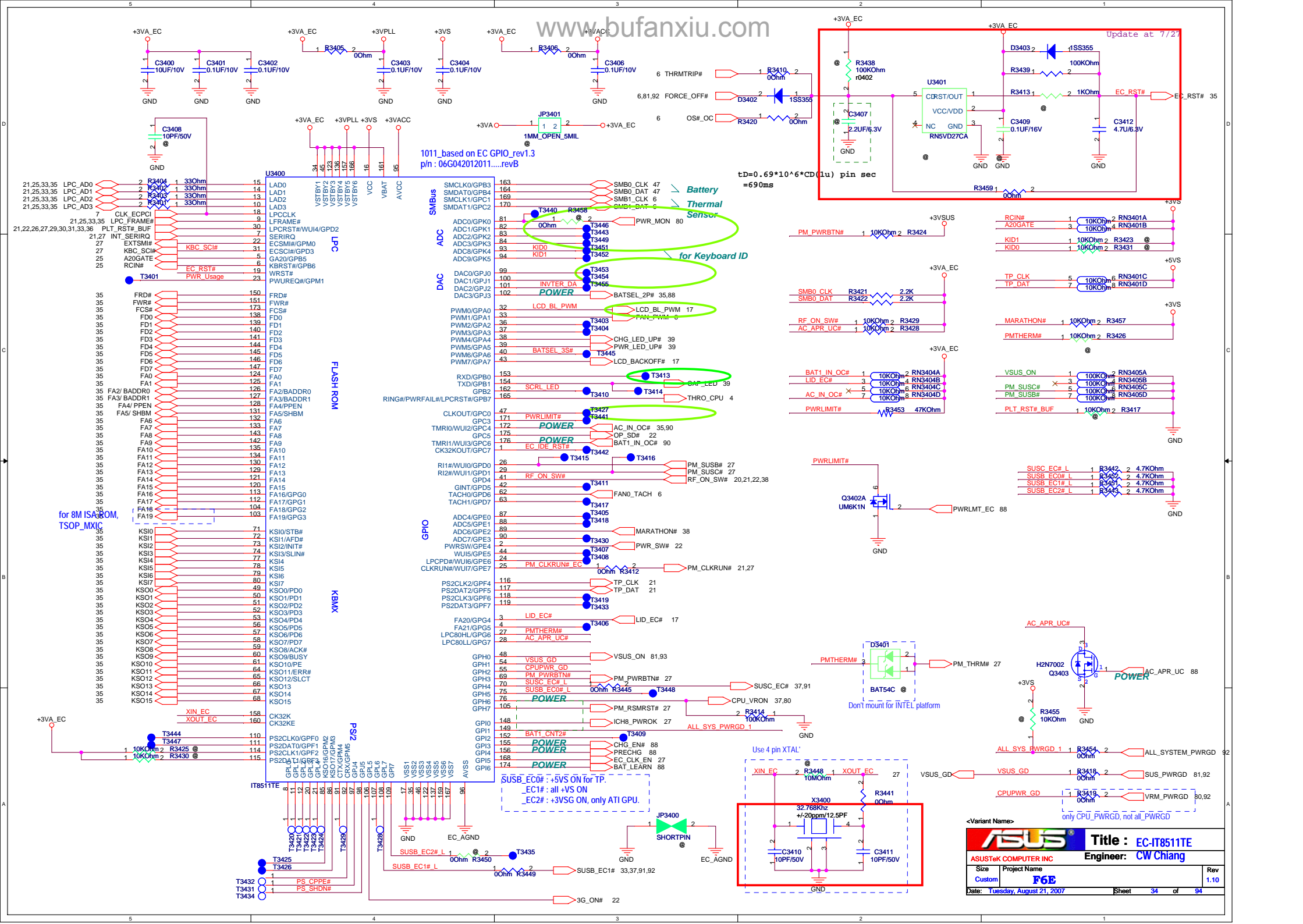


ASUSTek COMPUTER INC.

Li-Ts Rd., Peitou, Taipei, Taiwan, ROC



Title			NEW CARD		CW Chiang	
Size	Custom	Document Number	F6E		Rev	1.10
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EC Hardware Strapping

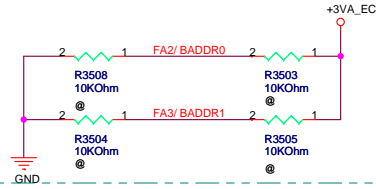
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

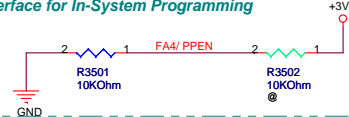


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

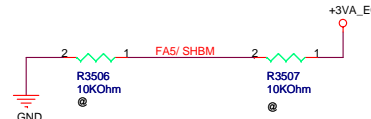
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

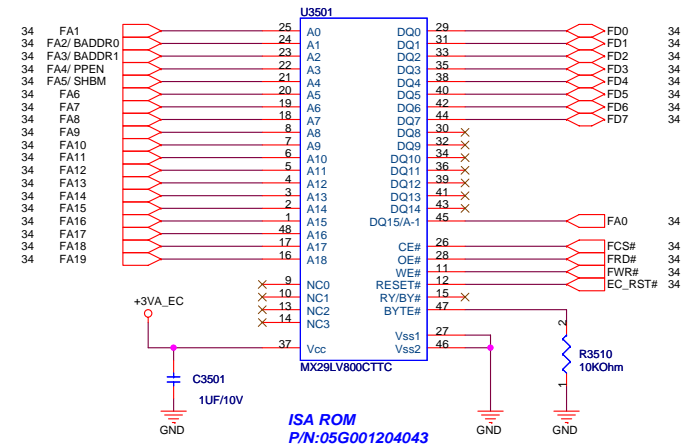
0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



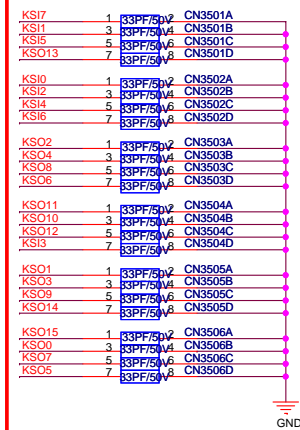
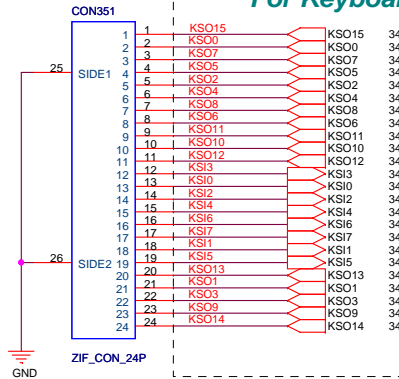
ISA ROM TSOP

8M TSOP _ MXIC

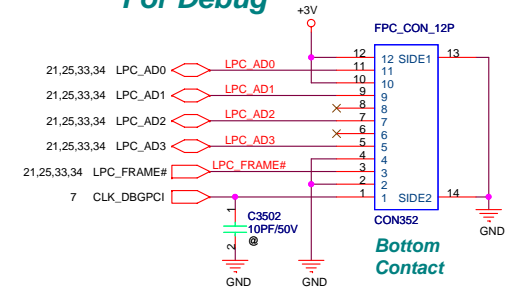


P/N: 12G182402404

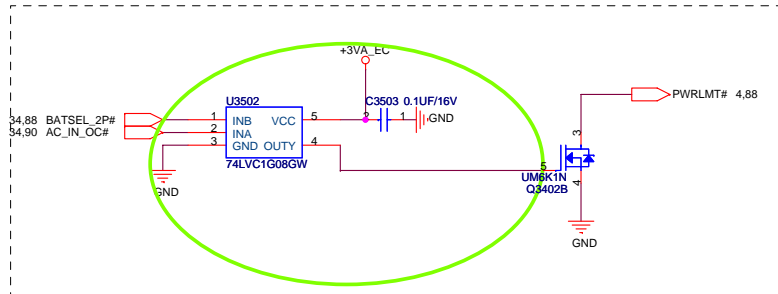
For Keyboard



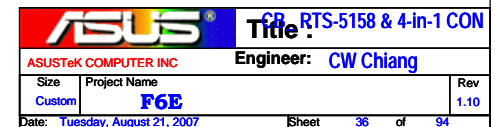
For Debug

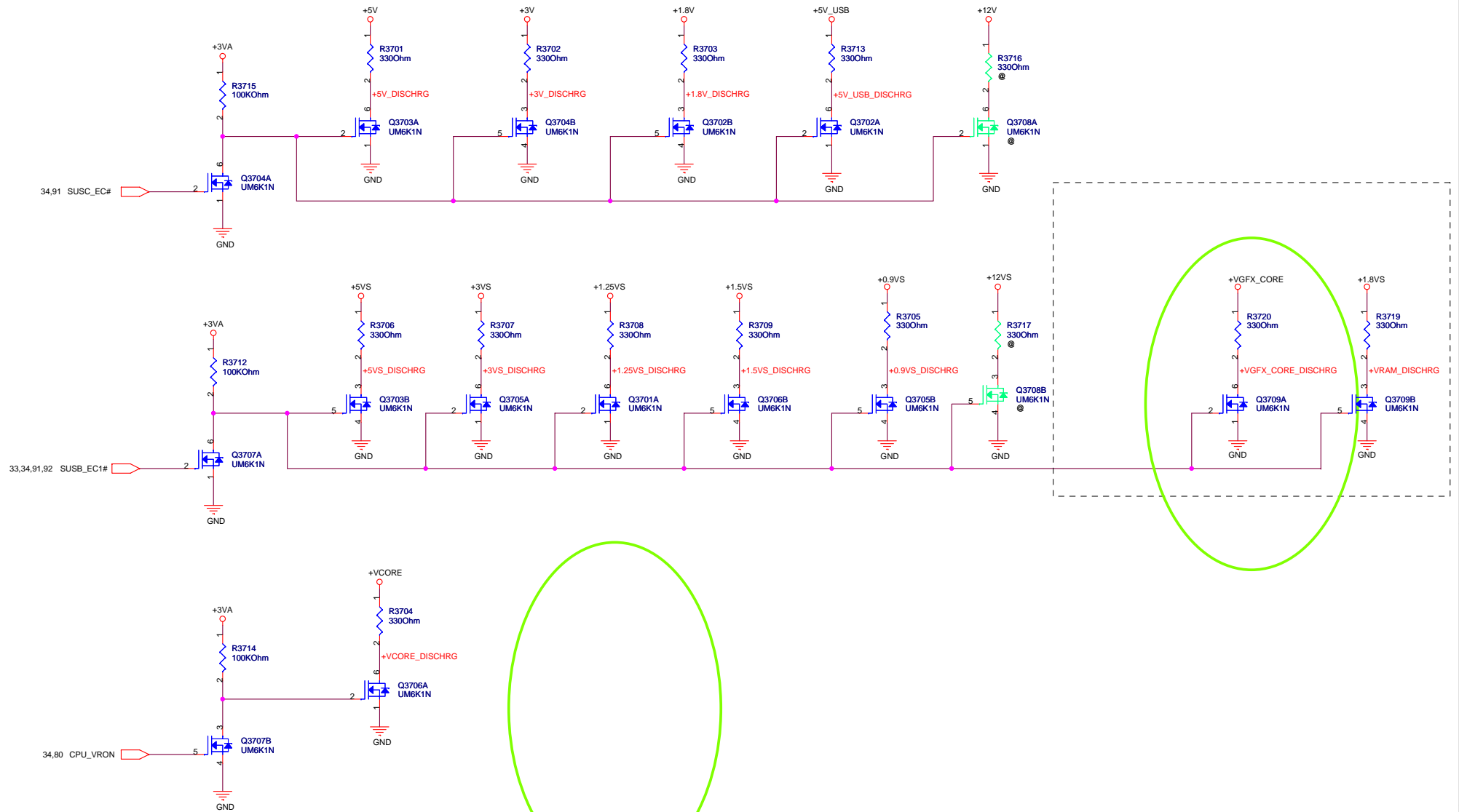


PWRLMT Circuit: For 65W adaptor.



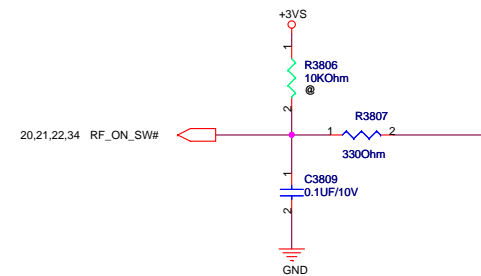
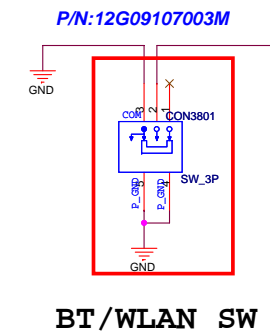
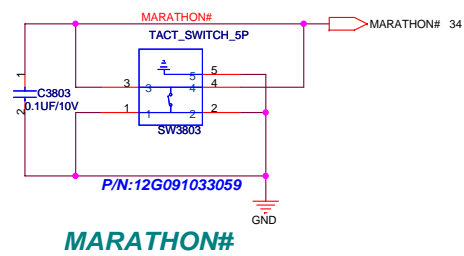
<Variant Name>





<Variant Name>

		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	Rev	
Custom	F6E	1.10	
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<Variant Name>

www.bufanxiu.com

PWR LED

Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

For BATTERY LED

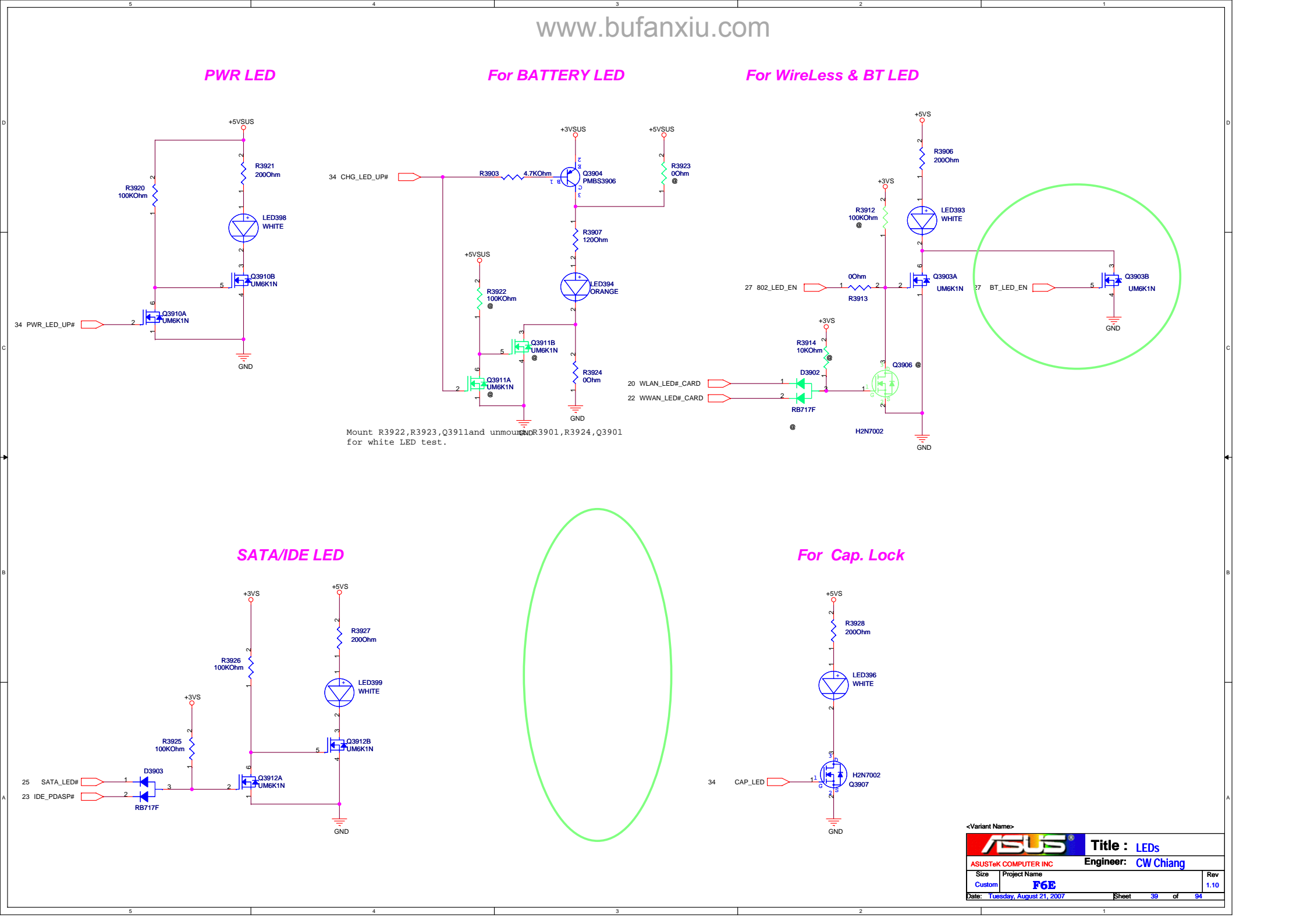
Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

For WireLess & BT LED

SATA/IDE LED

For Cap. Lock

<Variant Name>		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size Custom	Project Name F6E	Date: Tuesday, August 21, 2007	Rev 1.10
		Sheet 39	of 94



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PWR LED

For BATTERY LED

Mount R3922, R3923, Q3911 and unmount R3901, R3924, Q3901 for white LED test.

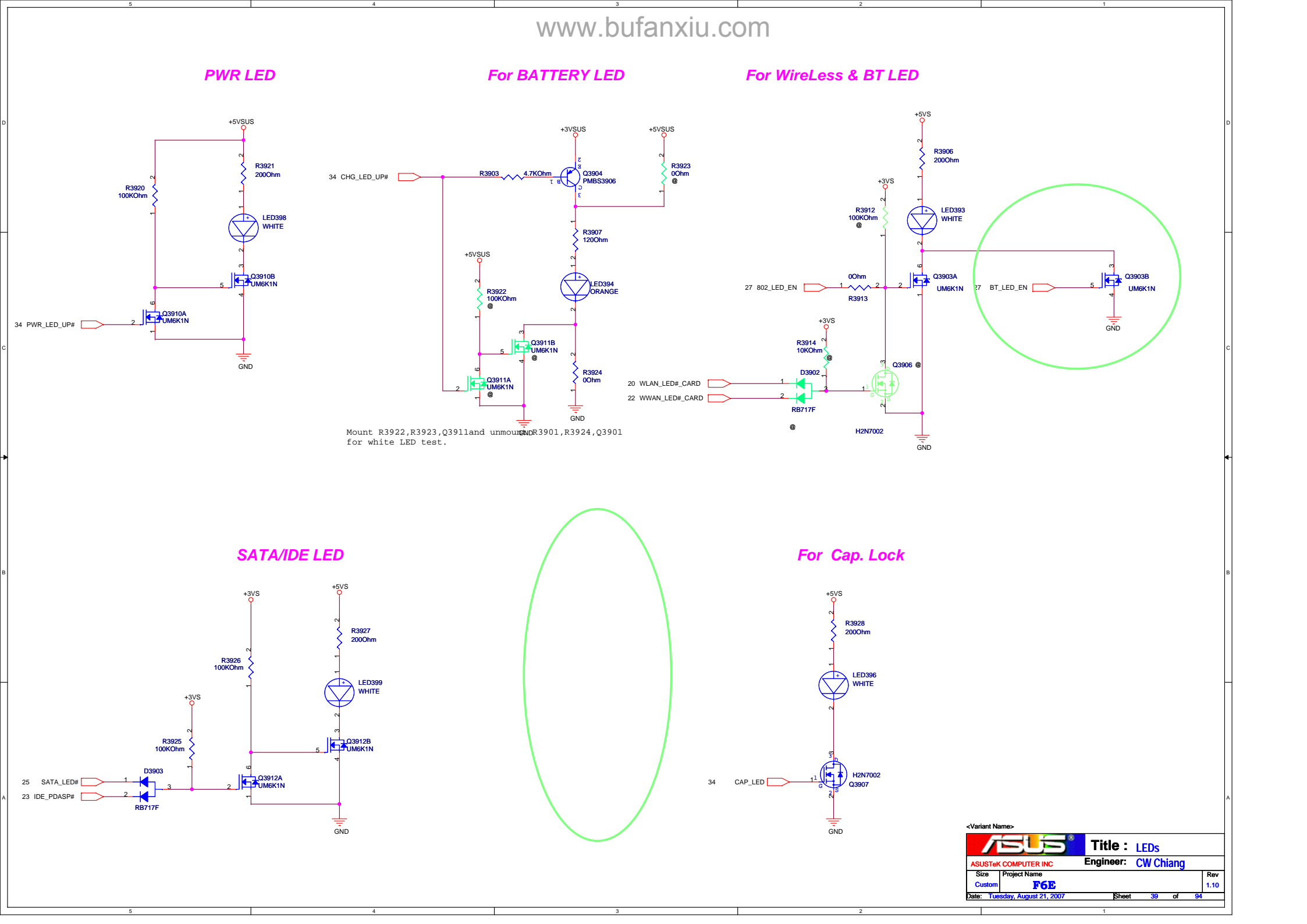
For WireLess & BT LED

SATA/IDE LED

For Cap. Lock

<Variant Name>

ASUS		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name		Rev
Custom	F6E		1.10
Date: Tuesday, August 21, 2007		Sheet 39 of 94	



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PWR LED

Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

For BATTERY LED

Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

For WireLess & BT LED

SATA/IDE LED

For Cap. Lock

<Variant Name>		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	F6E	Rev
Custom			1.10
Date: Tuesday, August 21, 2007	Sheet	39	of 94

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PWR LED

For BATTERY LED

Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

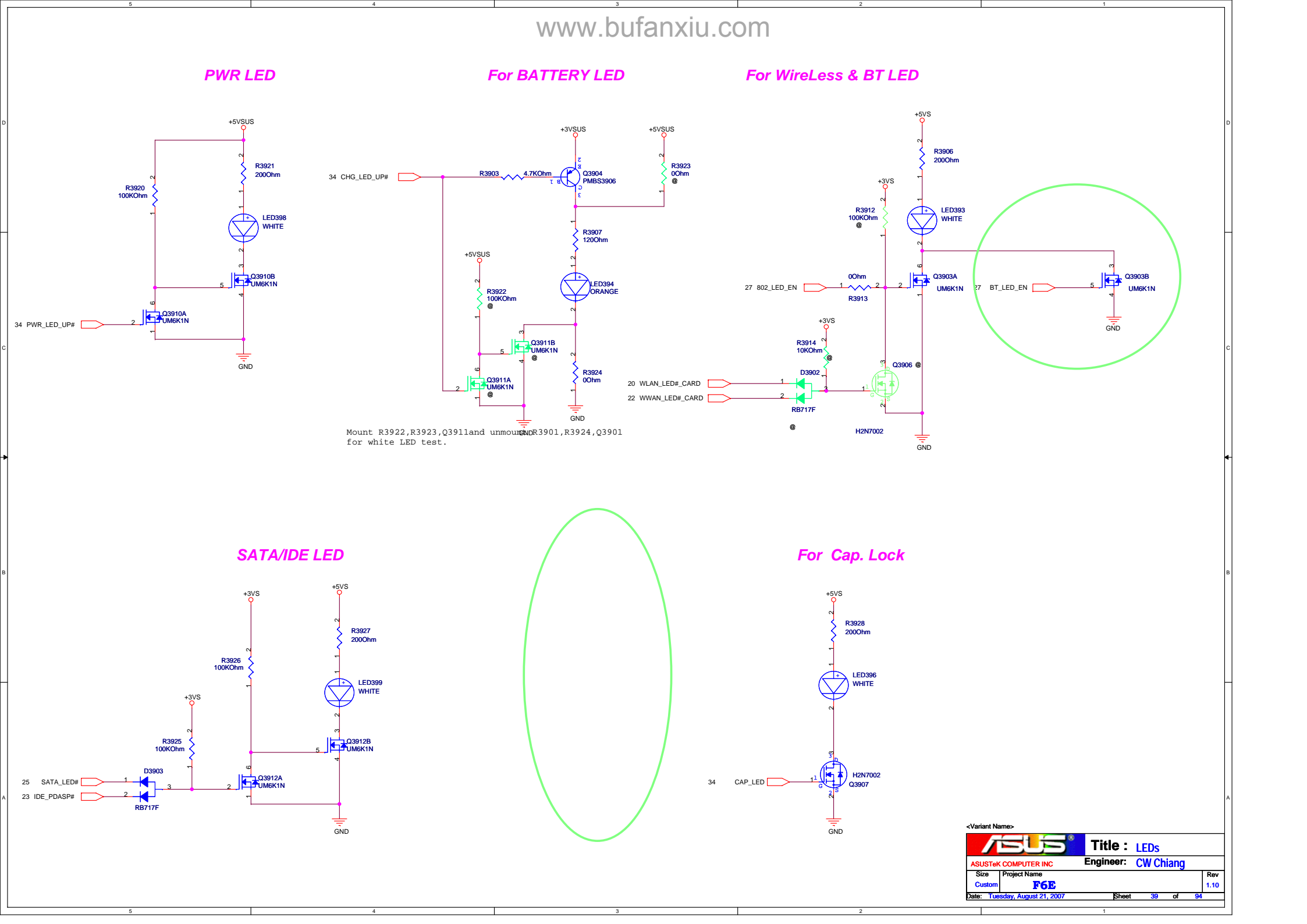
For WireLess & BT LED

SATA/IDE LED

For Cap. Lock

<Variant Name>

ASUS		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name		Rev
Custom	F6E		1.10
Date: Tuesday, August 21, 2007		Sheet 39 of 94	



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PWR LED

Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

For BATTERY LED

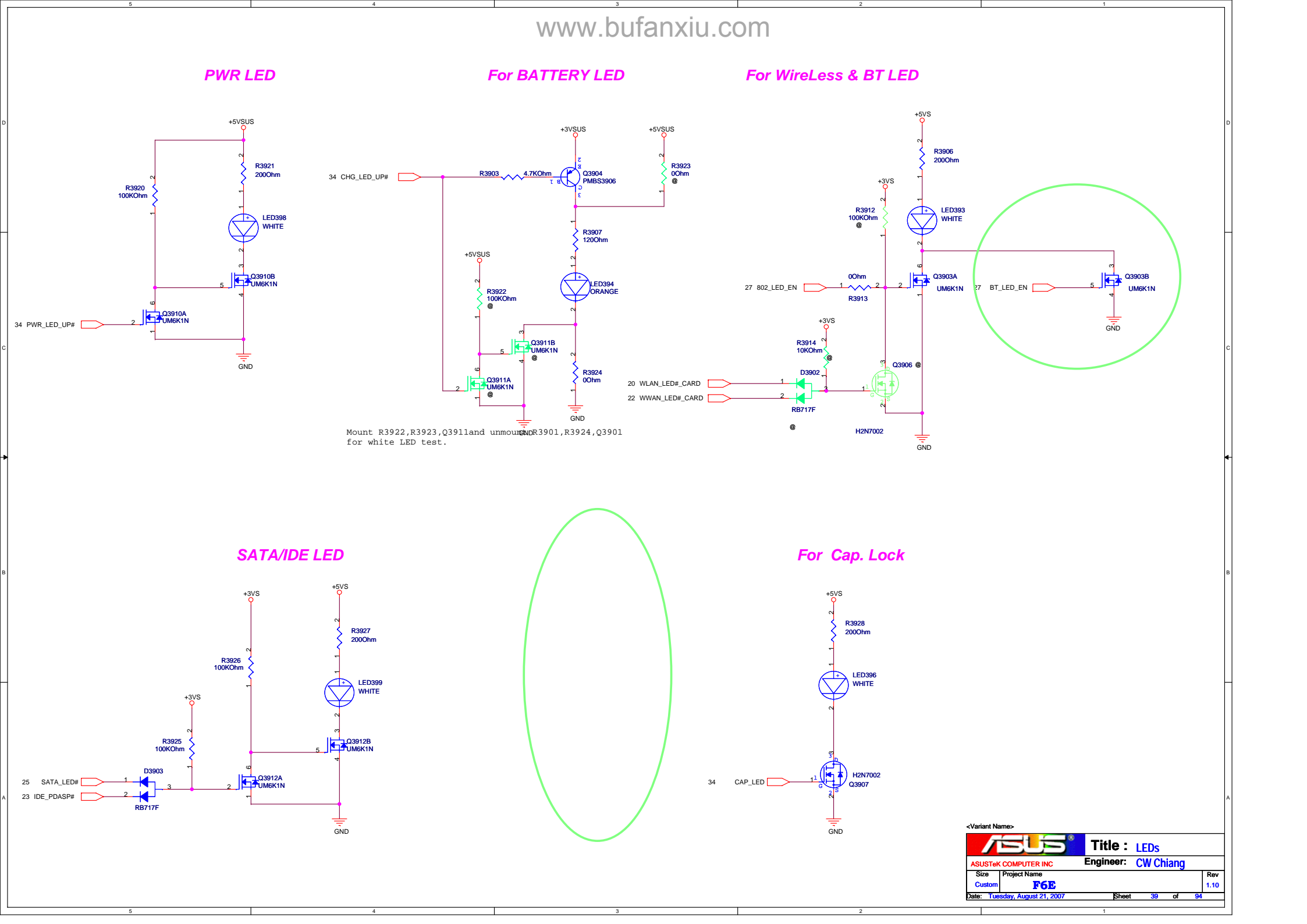
Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

For WireLess & BT LED

SATA/IDE LED

For Cap. Lock

<Variant Name>		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	F6E	Rev
Custom			1.10
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PWR LED

For BATTERY LED

Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

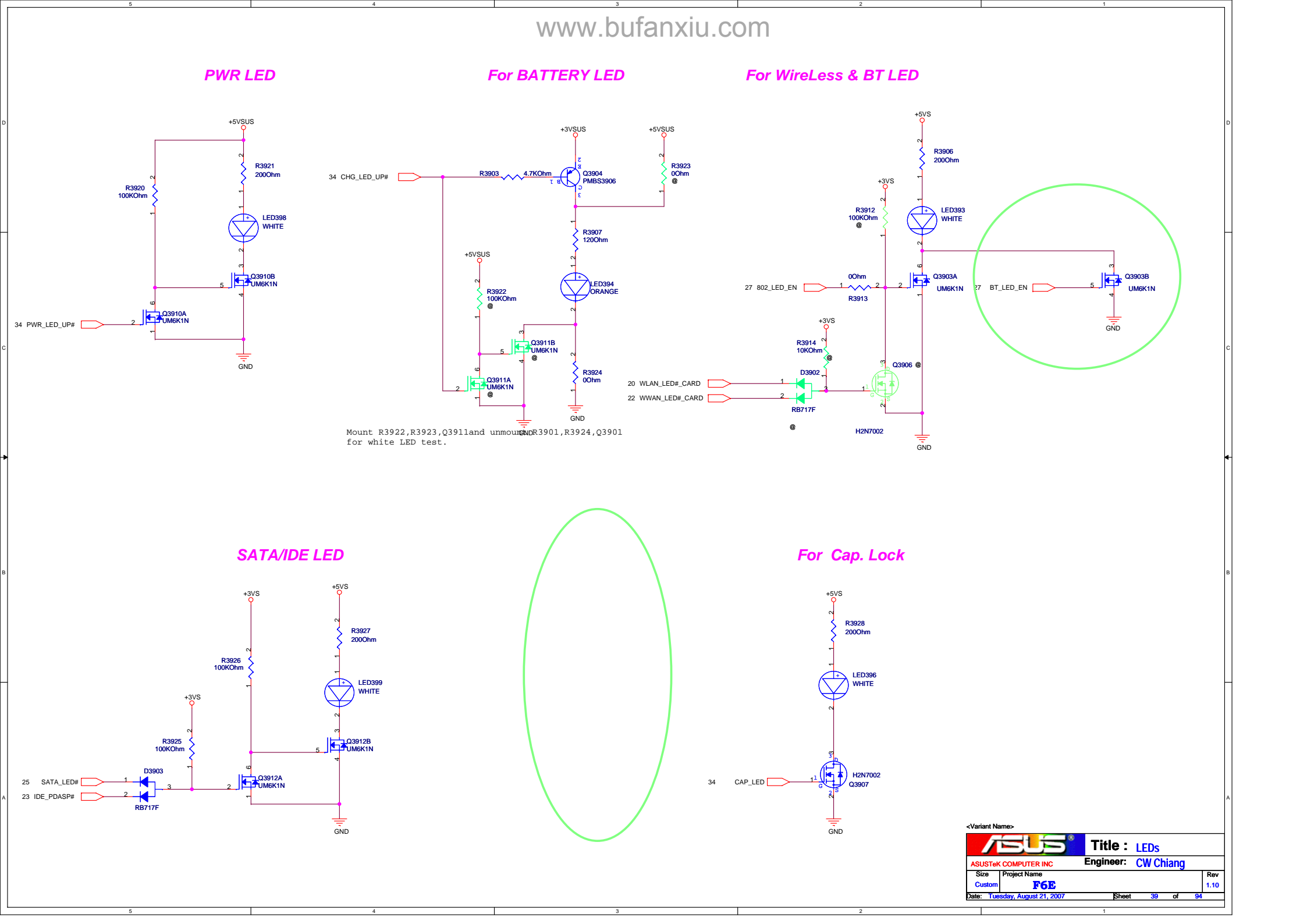
For WireLess & BT LED

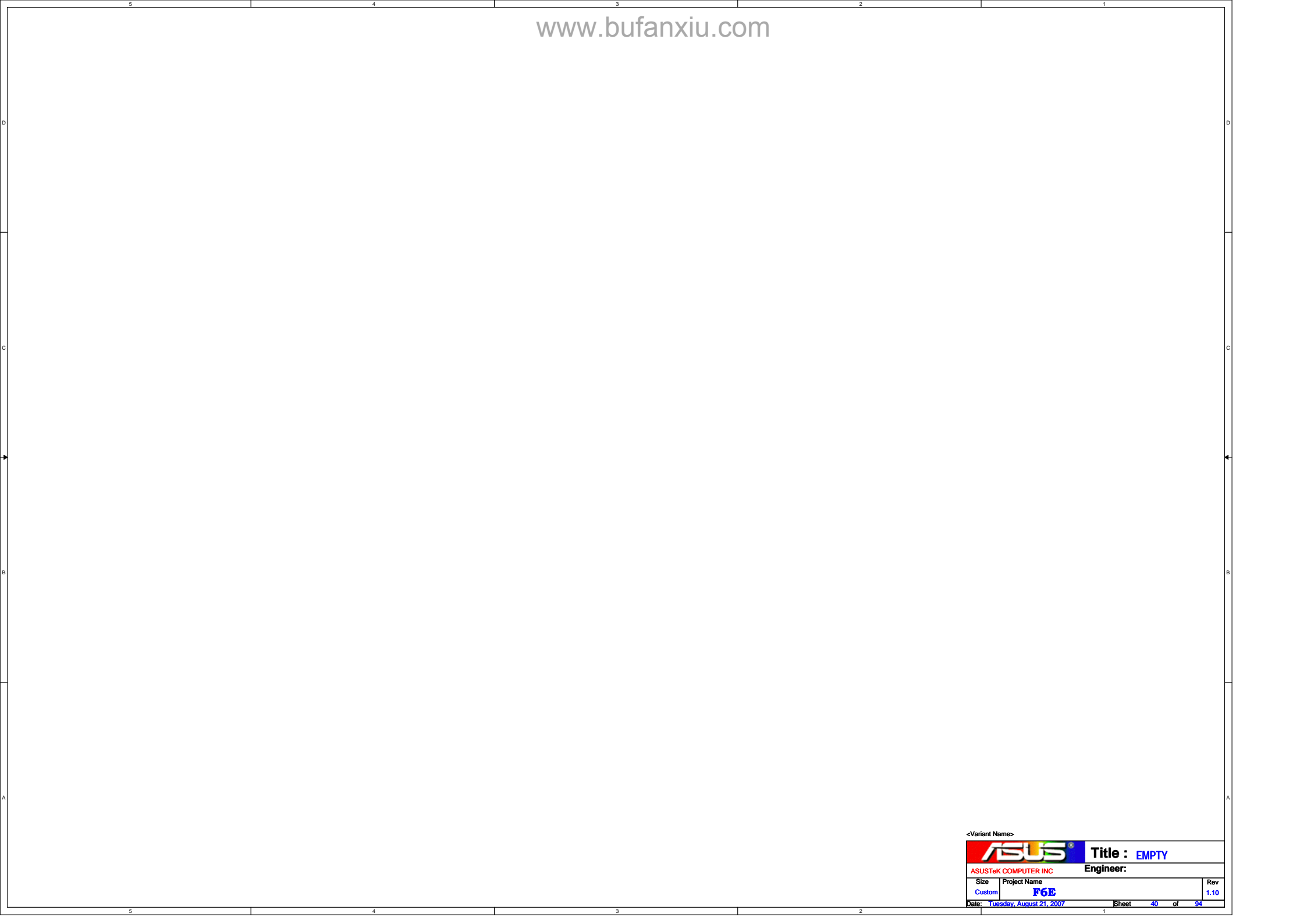
SATA/IDE LED

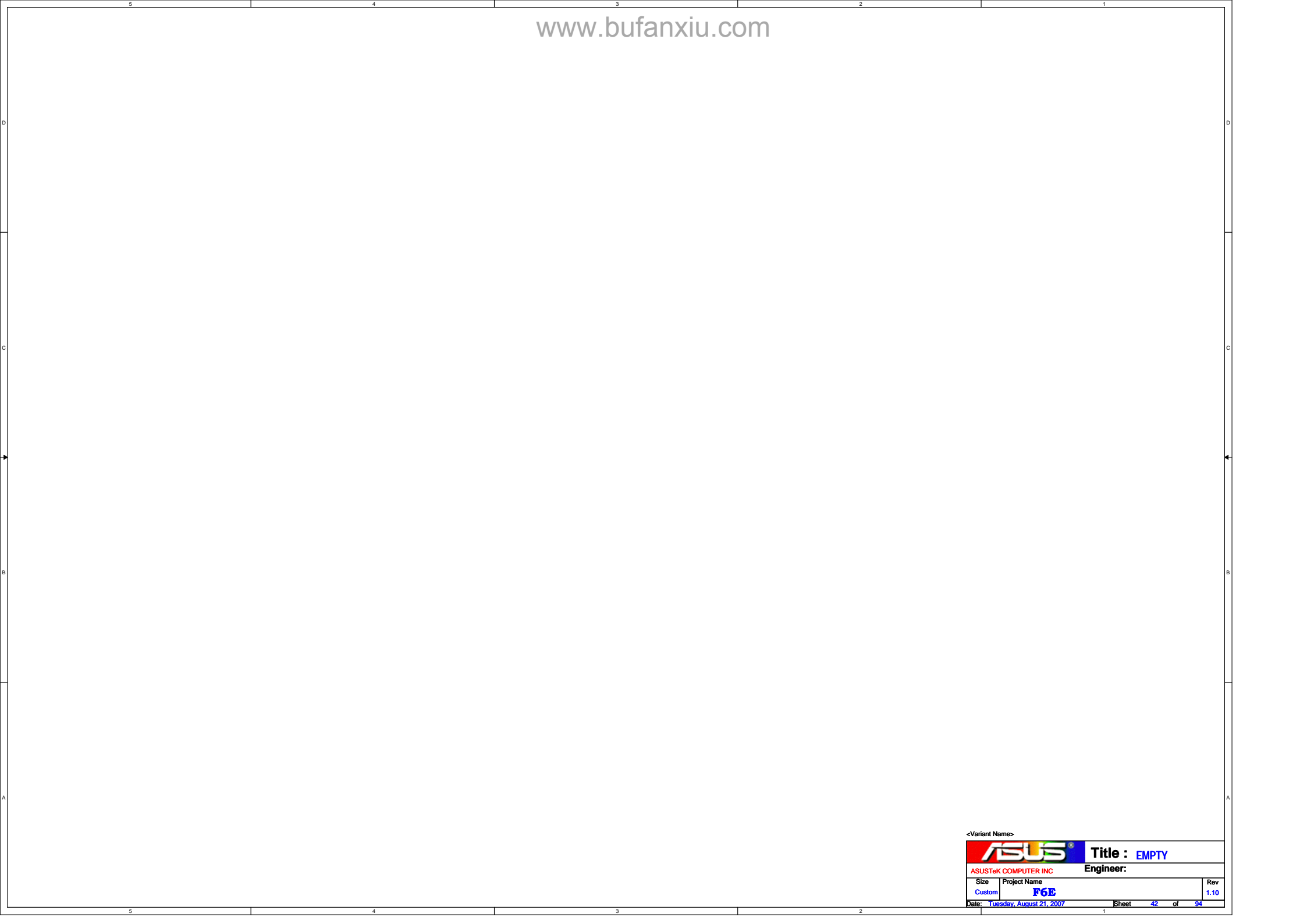
For Cap. Lock

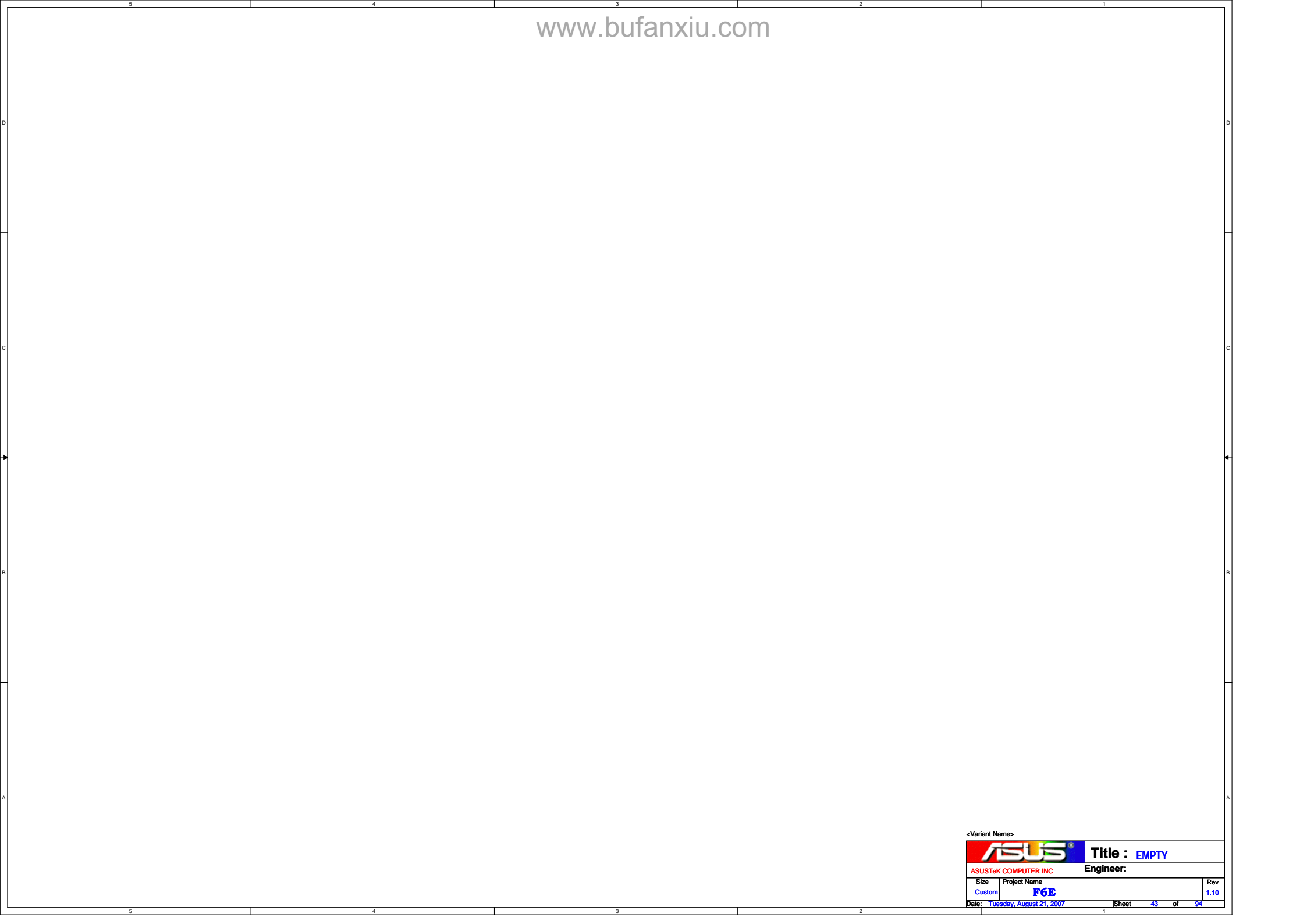
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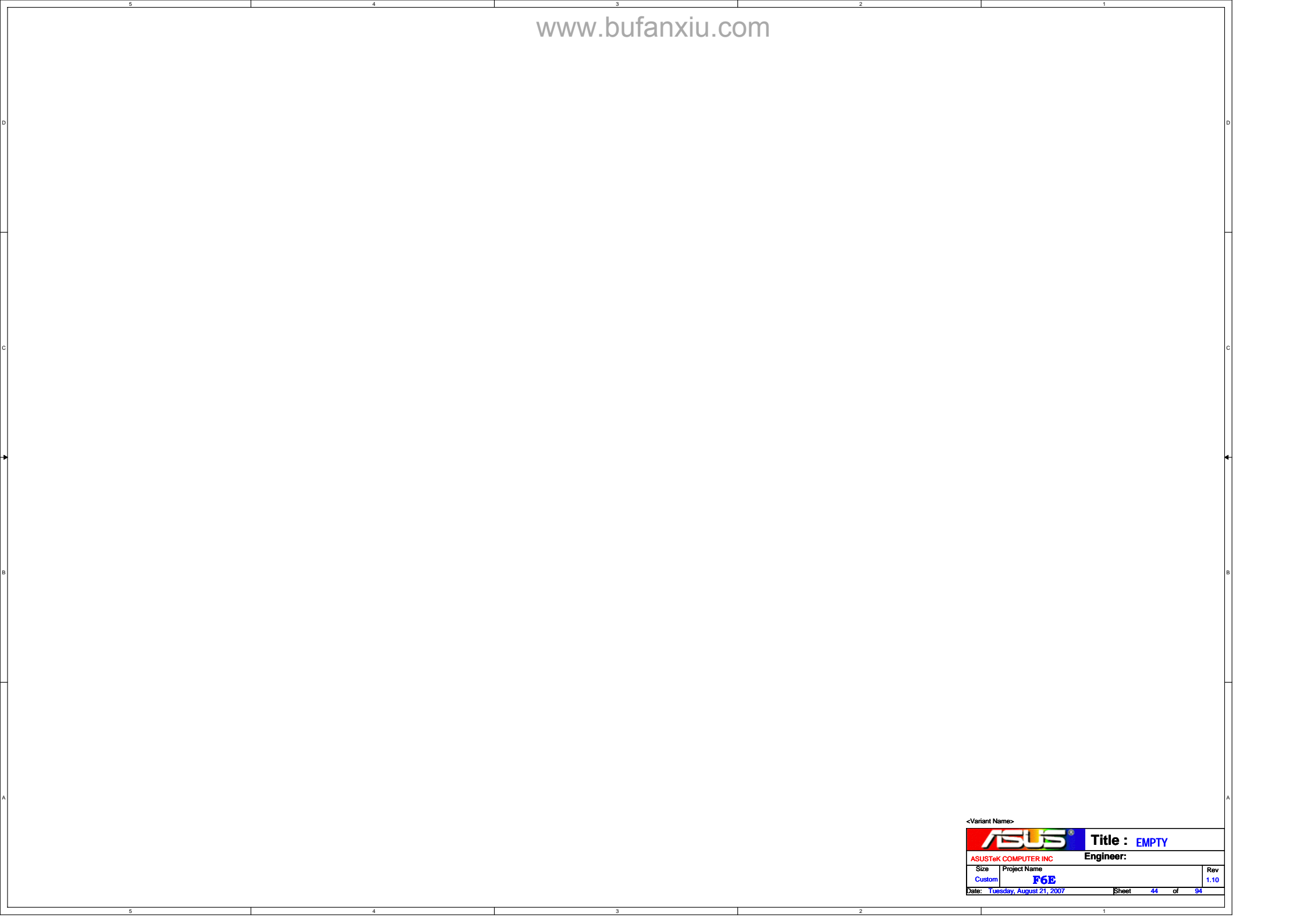
ASUS		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name		Rev
Custom	F6E		1.10
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<Variant Name>



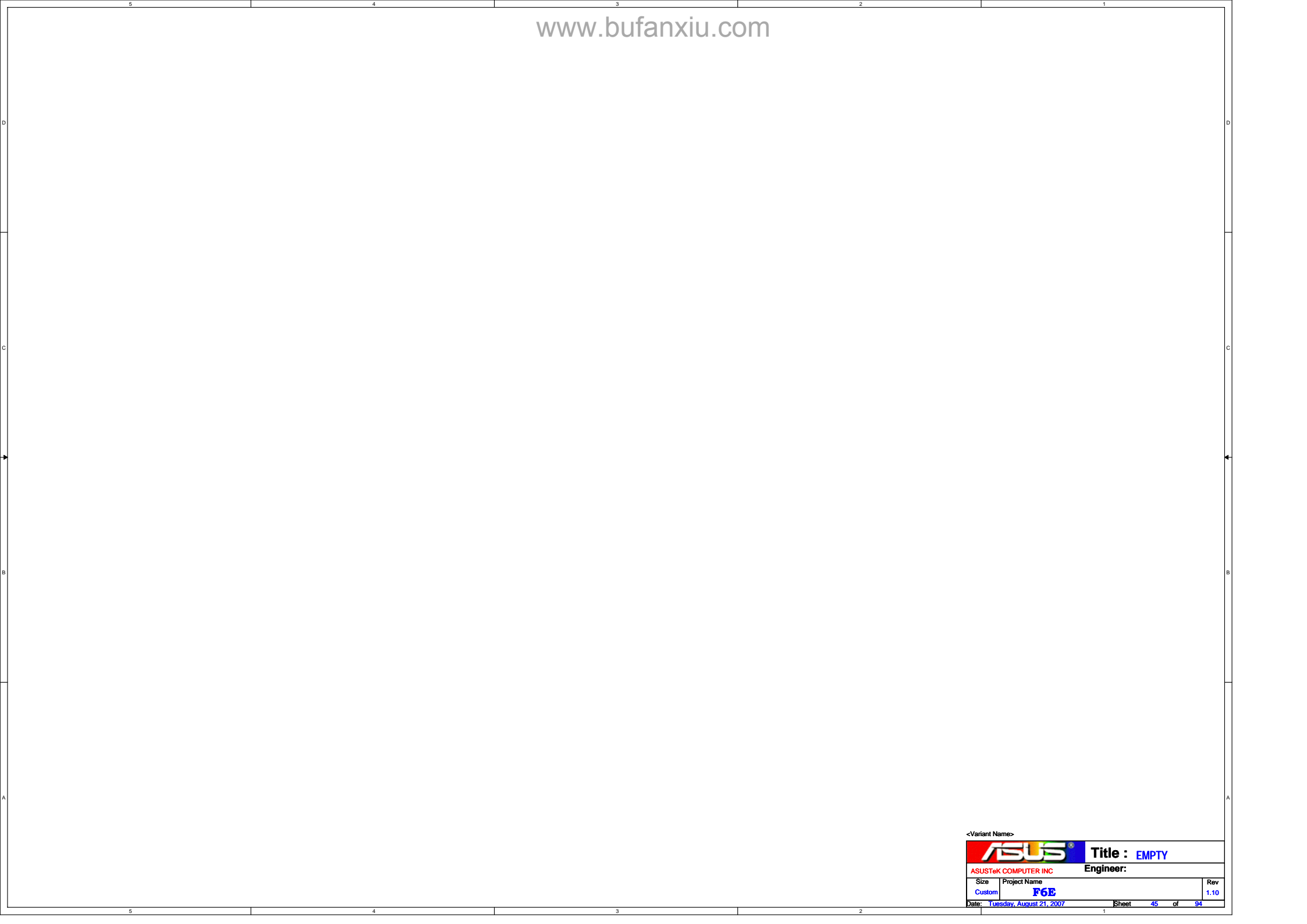
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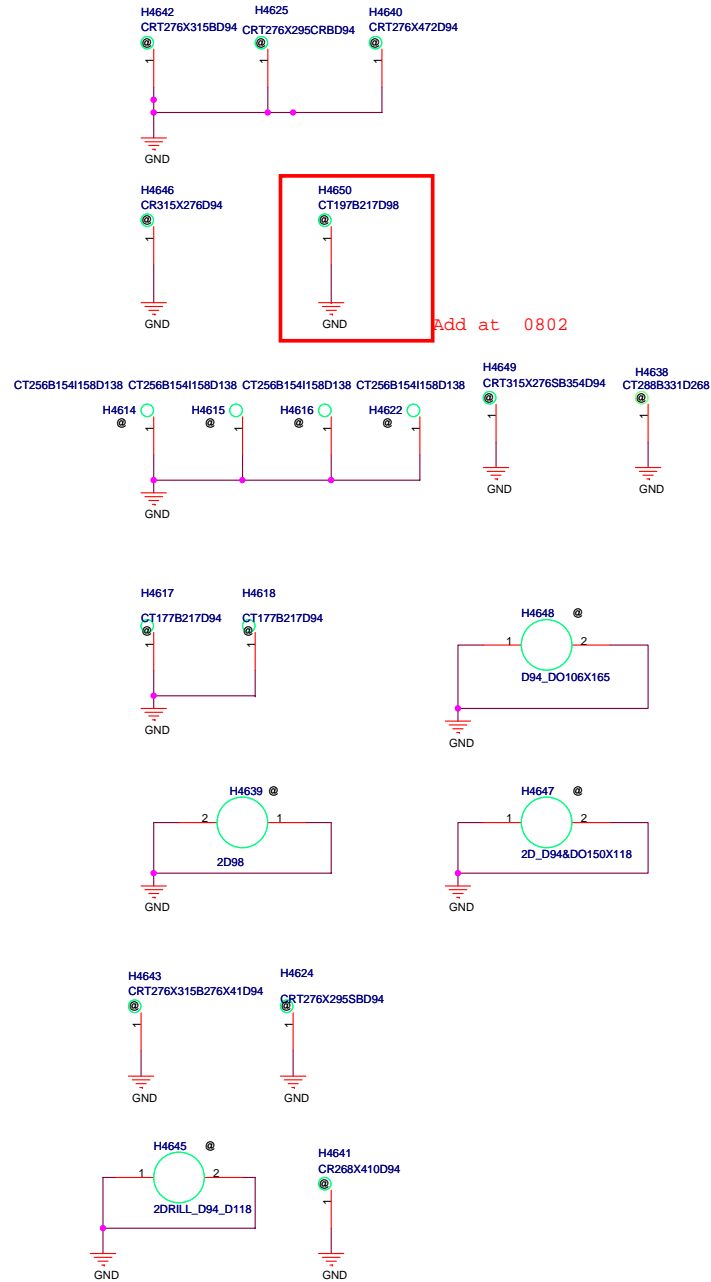
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

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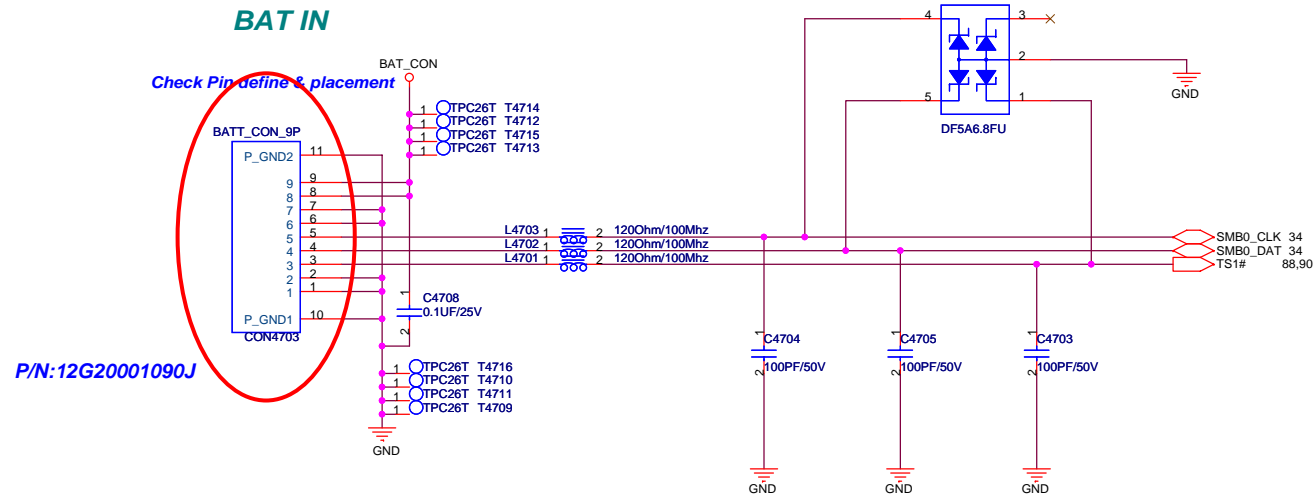
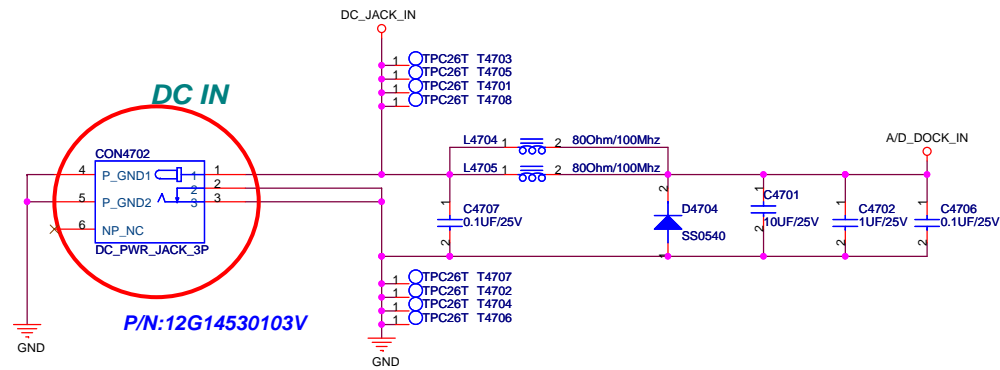




Add at 0802

<Variant Name>

ASUS		Title : SCREW HOLE	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	Rev	
Custom	F6E	1.10	
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<Variant Name>

ASUS		Title : DC & BAT IN	
ASUSTeK COMPUTER INC		Engineer: CW Chiang	
Size	Project Name	Rev	
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Rev0.3(Change List from R0.2 to R0.3)

- 1.Page 35: Add C3504-C3527 for EMI Requirement
- 2.Page 29 and 36: Add PLT_RSTNS# Connect to Lan and Card Reader Reset Pin
- 3.Page 34: Add EC Reset Circuit
- 4.Page 81: Change L8100 and L8101 from height = 4.5mm to 4.0mm
- 5.Page 46: Add H4638 for Antenna
- 6.Page 22: Change CON2201(BtoB Conn) Pin Define(Follow IO Board)
- 7.Page 19: Swap Signal Between CON1902 (HDMI Connector) and CHOKE
- 8.Page 86: Remove VGA Vcore Circuit
- 9.Page 11: Remove JP1102 and JP1103
- 10.Page 31: Swap D3101
- 11.Page 34: Add R3458
- 12.Page 11: Add CE1103 for VGFX_CORE

Rev0.4(Change List from R0.3 to R0.4)

- 13.Page 36: Remove C3619
- 14.Page 31: Swap L3110 RN3101 D3101
- 15.Page 38: Change SW3803 to 12G091033059
- 16.Page 92 Page 93: Remove GFX_PWRGD, +VCCFX_CORE
- 17.Page 27: Modify SM BUS Signal
- 18.Page 06: Remove Q9201
- 19.Page 22: R3803 rename to R2201,C3805 rename to C2207
- 20.Page 38: CON4707 rename to CON3801
- 21.Page 35: Change C3504 - C3527 to CN3501 - CN3506
- 22.Page 47: Change Batt Connector From 12G200010901 to 12G20001090J
- 23.Page 81 Page82: Power remove CE8101 CE8103 CE8204


Rev0.5(Change List from R0.4 to R0.5)

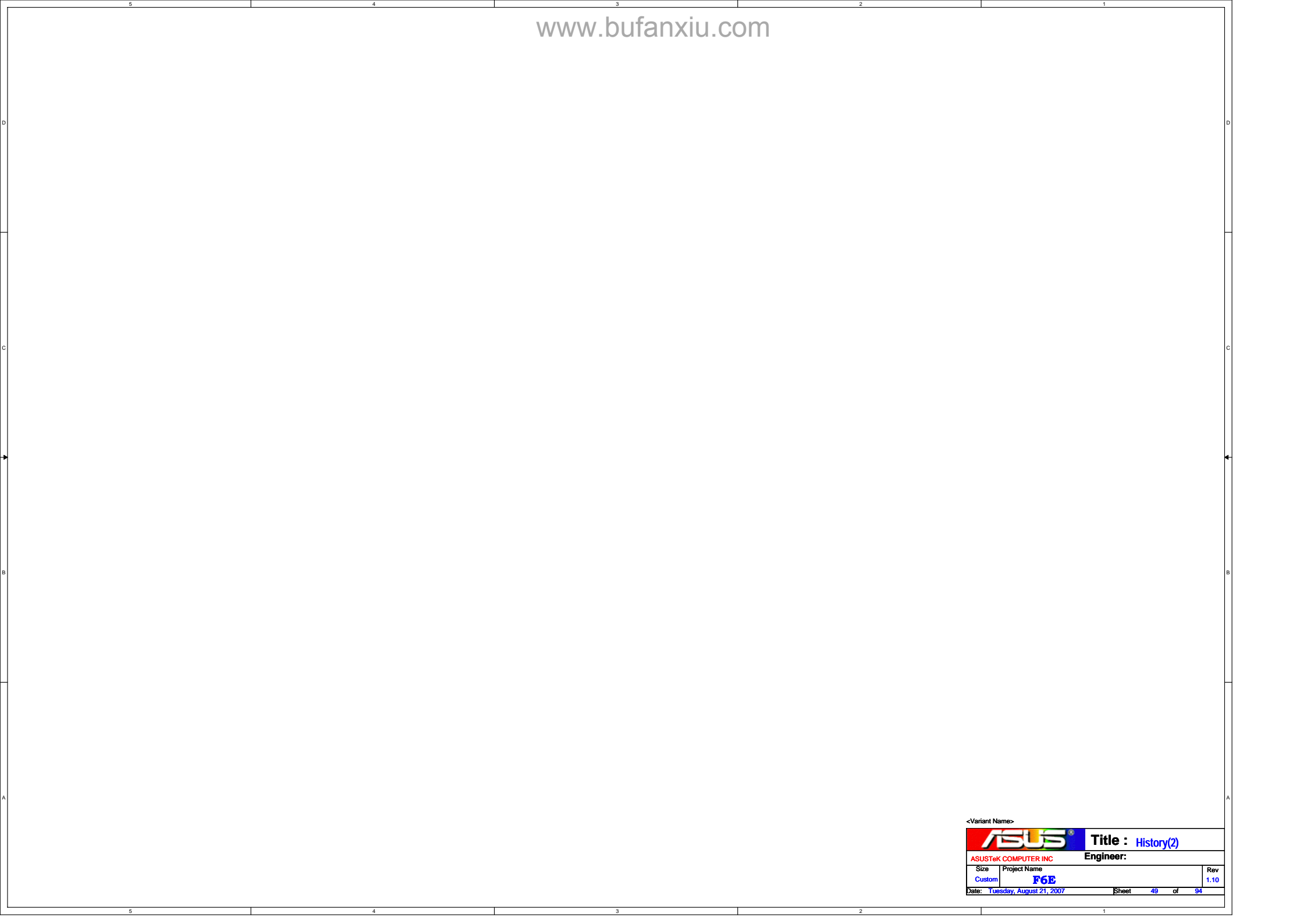
- 24.Page 07: Remove Q0701
- 25.Page 38: CON3801 Pin1 Pin2 swap
- 26.Page 17: Change L1708 to R1708 (0603 100ohm)
- 27.Page 82: Remove JP8202 JP8206
- 28.Page 26: Change U2603 to 06G004603219 for cost down
- 29.Page 26 35: Change U2602 U3502 to 06G004092010 for cost down
- 30.Page 07 20: Remove CLK_REQ_MINICARD and R0734
- 31.Page 28: Change C2812 to 11G235210615320 for cost down
- 32.Page 28: Add C2838 for VCCP_ICH
- 33.Page 06: Add R0671 for PM_THRMTRIP# Pull Up.
- 34.Page 16: Add C1602 C1603 for VTT_REF +0.9VS
- 35.Page 27: Modify ICH8_PWROK circuit for Leakage issue(ADD R2754 D2702)
- 36.Page 24: Change R2411 from 0603 to 0805
- 37.Page 17: Add R1709 for CCD
- 38.Page 26 27: Change USB_OC# Pull High Circuit and Add R2615 R2616 R2757 R2758
- 39.Page 31: Add C3175 C3176 for eSATA(JMicron suggested)
- 40.Page 35: Remove R3509
- 41.Page 34: Add T3449
- 42.Page 19: Change R1903~R1910 to RN1901~RN1904
- 43.Page 37: Remove +VCCP Discharge Circuit
- 44.Page 34: Remove R3432 R3433
- 45.Page 27: Add D2703 for Leakage Issue
- 46.Page 24: Change ESD Diode D2401 D2402 to D2405, D2403 D2404 to D2406 for cost
- 47.~~Page 33: Change C3308 from 0603 to 0402~~

Rev0.6(Change List from R0.5 to R1.0)

- 48.Page 39: Remove R3907 R3909 LED394 LED395 Q3905 Add Q3907 for 5 LED Lights
- 49.Page 47: Change ESD Diode D4701 D4702 D4703 to D4705
- 50.Page 31: Change eSATA Connector to 12G142001110
- 51.Page 35: Change Debug Connector to 12G183301208
- 52.Page 28: Change JP2802
- 53.Page 39: Modify LED Circuits for White LED
- 54.Page 46: Update Screw Hold
- 55.Page 17 19 24 31 33: Change Co-lay resistance from 0402 to 0603
- 56.Page 6 Rename +5VS to +5VS_FAN for FAN Power(Power request)
- 57.Page 28: Change C2801 C2802 0.1uF (0402) to 1uF (0603)
- 58.Page 46: Remove JP4601
- 59.Page 39: Change R3926 connect to +3VS
- 60.Page 36: Change RST5158 Reset Pin Connect to PLT_RST#_BUF
- 61.Page 27: Remove D2702 D2701 due to the ITE 8511 set the GPIO to OPEN-DRAIN
- 62.Page 34: Remove D3404 and Unmount Reset IC (EC_RST# By RC)
- 63.Page 29: Add C2941 for +1.8V_LAN
- 64.Page 17: Change R1705 to 330 ohm for LCD Power Sequence
- 65.Page 29: Change R2903 from 2.49K ohm to 2.21K ohm for GigaLan eye pattern
- 66.Page 24: Change USB Connector CON2402 CON2403 to 12G131050044
- 67.Page38: Change Slide Switch CON3801 to 12G09107003M
- 68.Page17: Change LVDS Connector CON175 to 12G17001030V
- 69.Page 29: Change R2903 from 2.21K ohm to 2.49K ohm
- 70.Page 25: Change R2525 from 24.9 ohm to 22.6 ohm for SATA
- 71.Page 21: Add R2111 R2112 (PLT_RST#_BUF) Connected to CON2104 for Finger Printer Issue
- 72.Page 29: Del C2924 Change C2841 to 22UF/10V
- 73.Page 28: Change JP2802 to 2MM size
- 74.Page 27: Add D2701 D2702 R2759 R2760 for ICH8_PWROK PM_RSMRST# Leakage Issue.
- 75.Page 31: Add C3148 4.7uF/6.3V for DVDD1.8V
- 76.Page 31: Remove Extra eSATA Reset Circuit (Remove U3103 R3115 C3155 C3154)
- 77.Page 34: Add R3459 for EC_RST#
- 78.Page 28: Change JP2802 to JP8206(+VCCP change to +1.05VO)
- 79.Page 29: Change L2903 L2905 L2906 to R2929 R2930 R2931
- 80.Page 31: Change R3135 to 57.6K ohm

<Variant Name>

		Title : History(1)	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name F6E		Rev 1.10
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FOR LAYOUT
PLACEMENT

(44A)
+VCORE

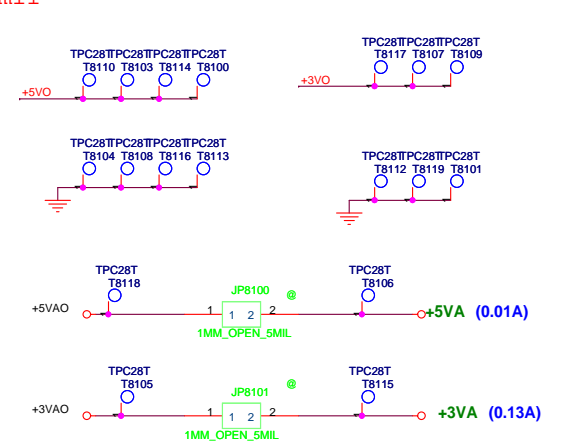
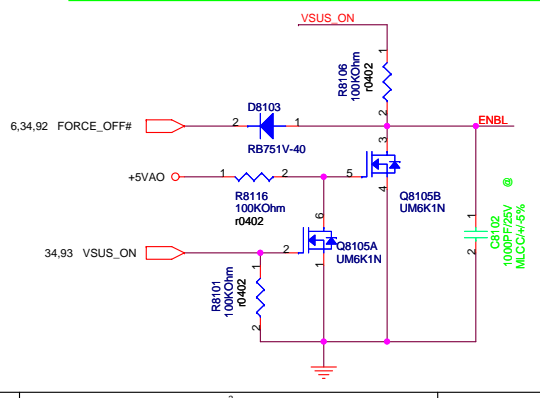
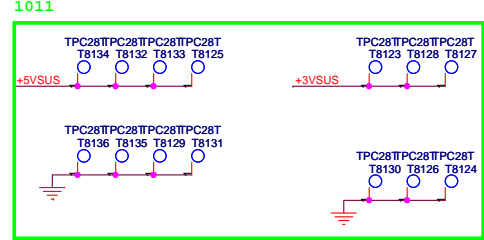
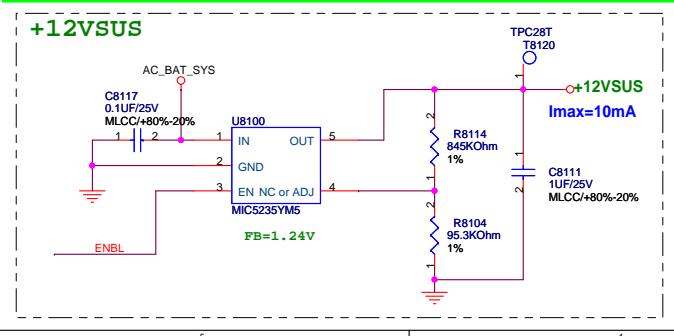
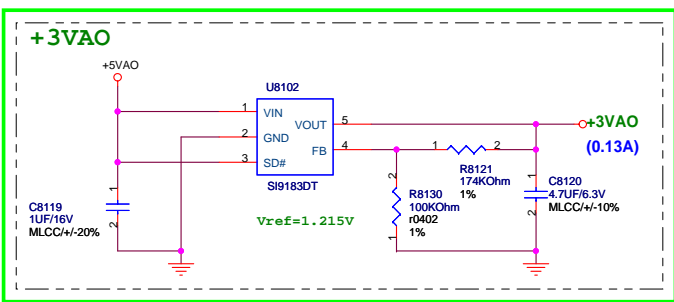
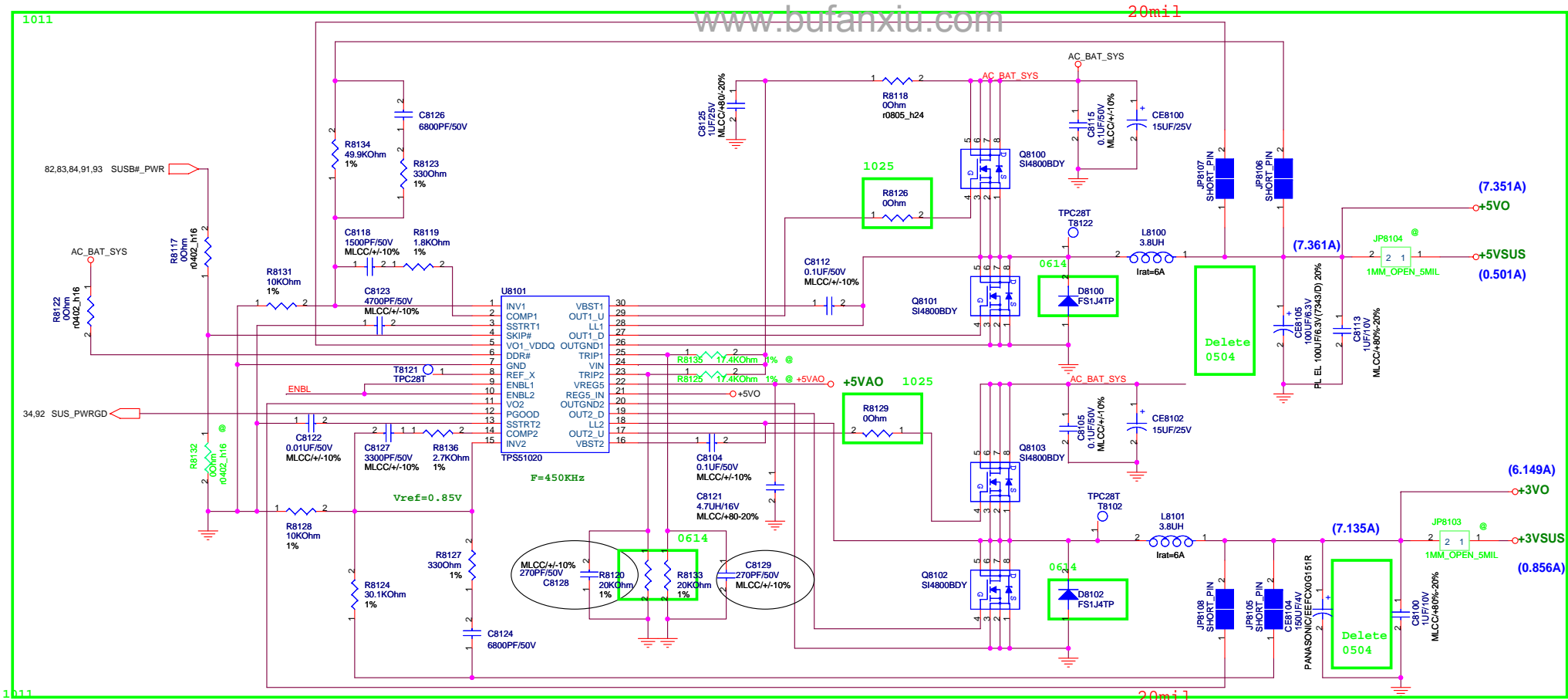
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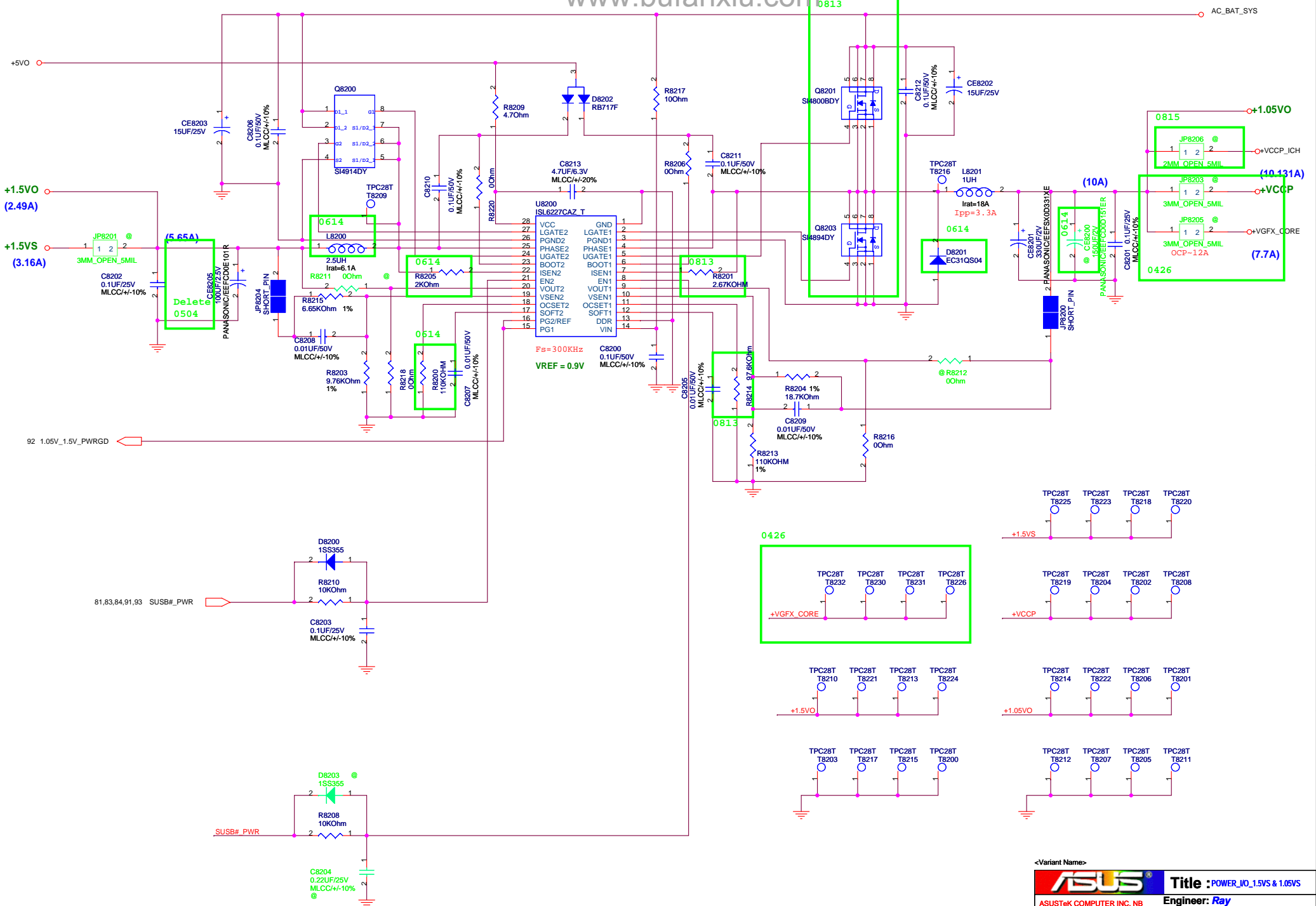
for current
balance

Close to Pin 18

Close to Phase 1
Inductor

C8021 & C8018 for transient response





<Variant Name>



Title : POWER_UO_1.5VS & 1.05VS

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size

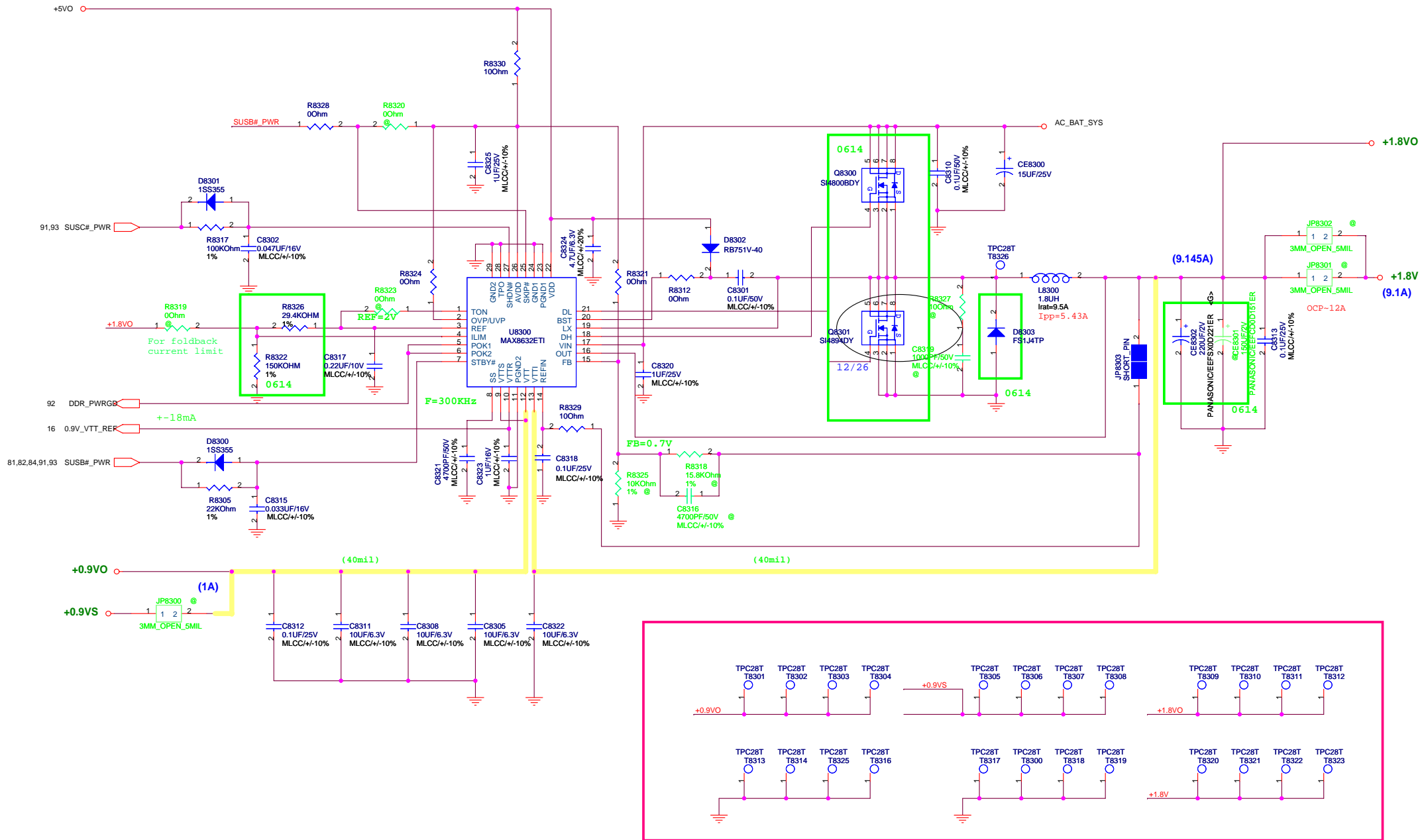
Custom

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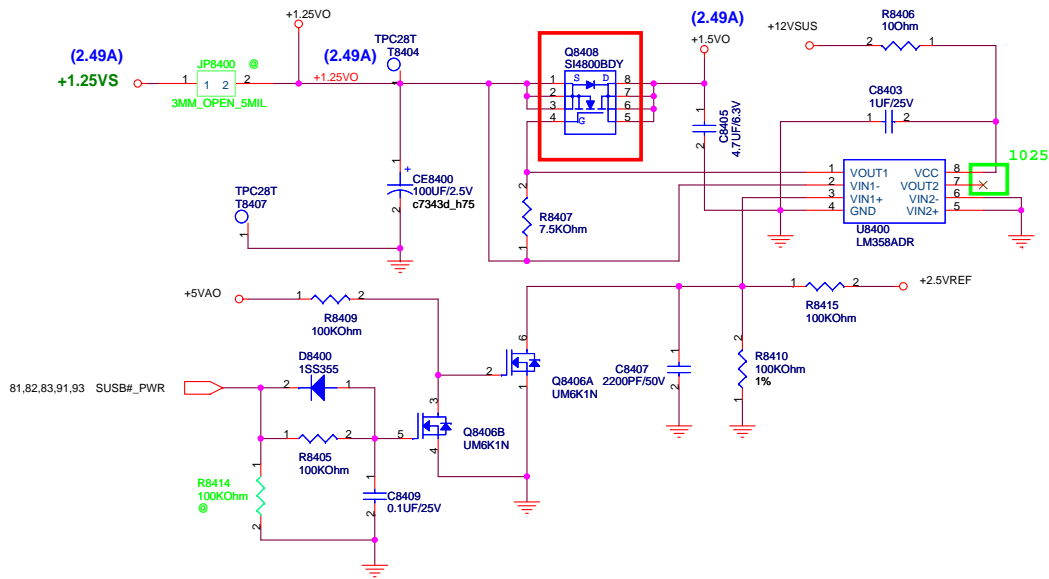
Rev 1.10

F6E



<Variant Name>

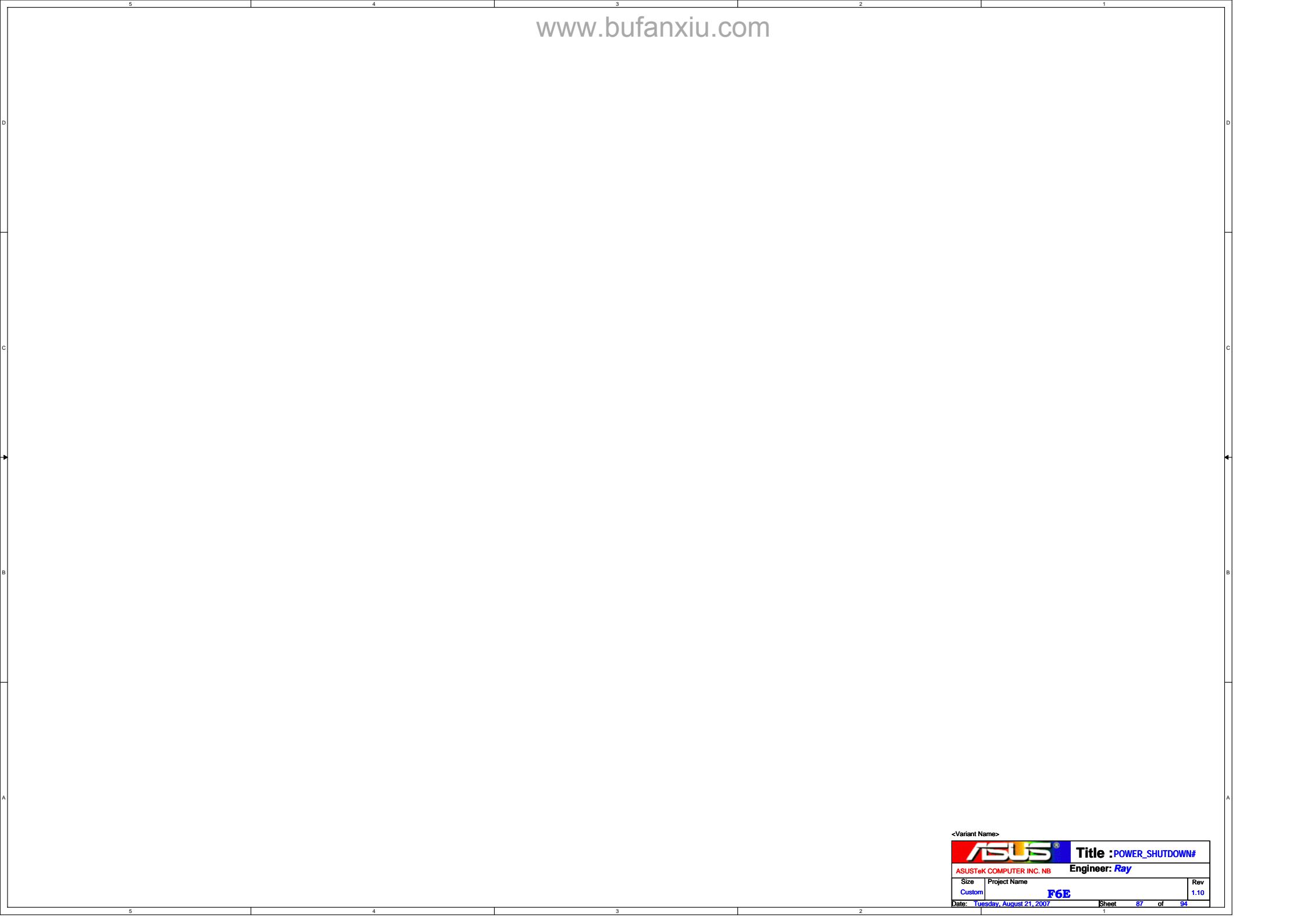
+1.25VS



delete +VRAM &VGA_core

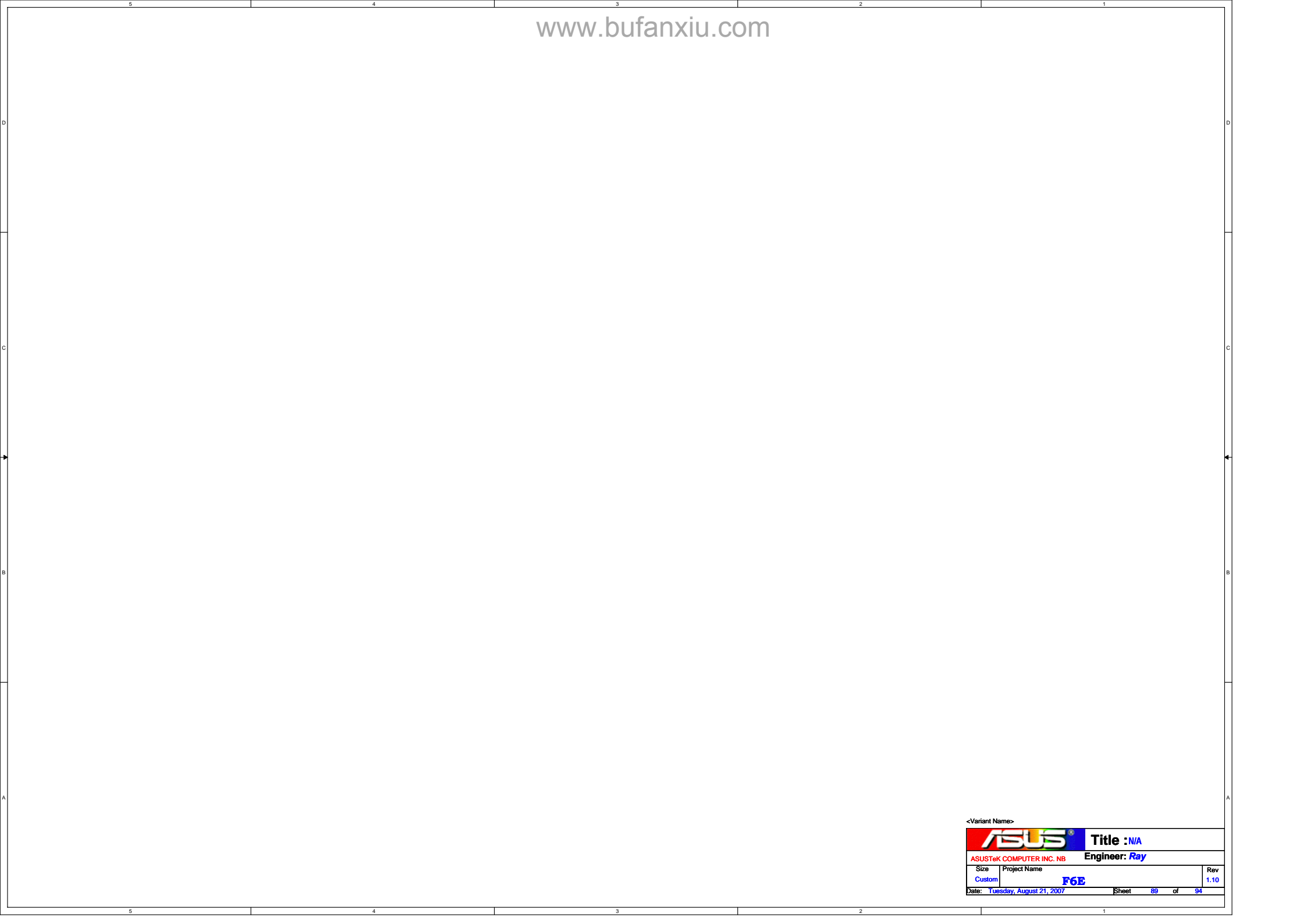
<Variant Name>

		Title : POWER_+VCCFX_CORE	
ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size	Project Name		Rev
B	F6E		1.10
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<Variant Name>

**ASUS**[®]

Title :*N/A*

ASUSTeK COMPUTER INC. NBEngineer: *Ray*

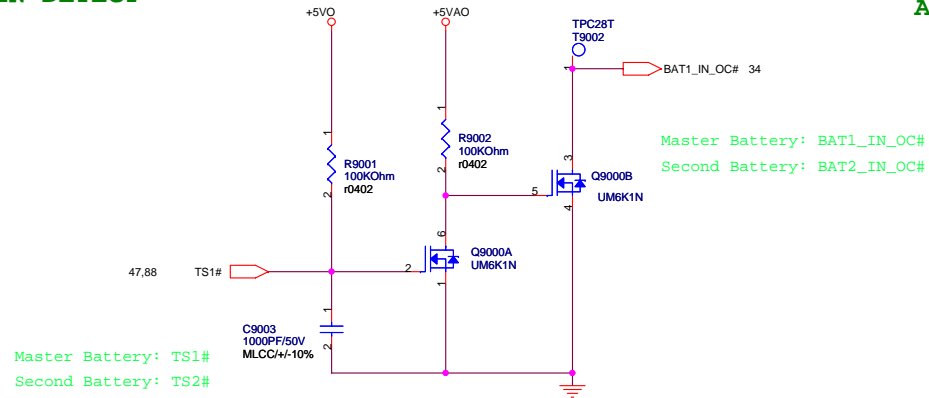
Size
Custom

Project Name
F6E

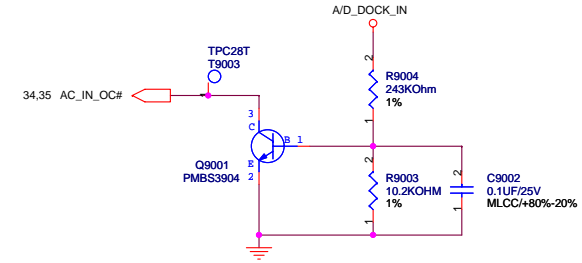
Rev
1.10

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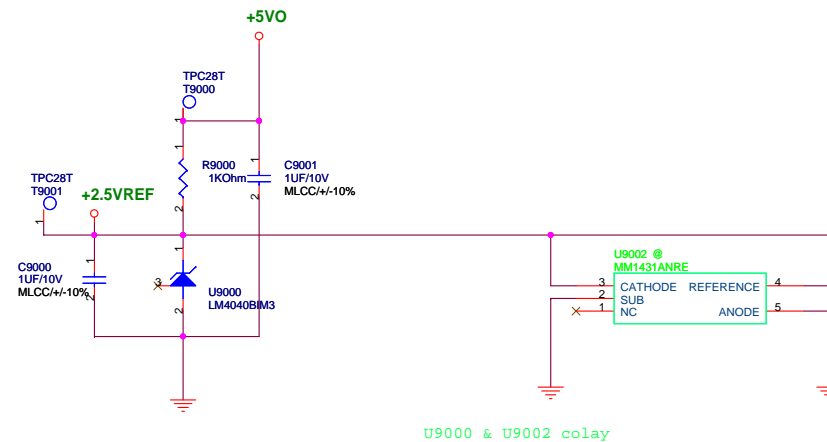
BATTERY IN DETECT



ADAPTER IN DETECT



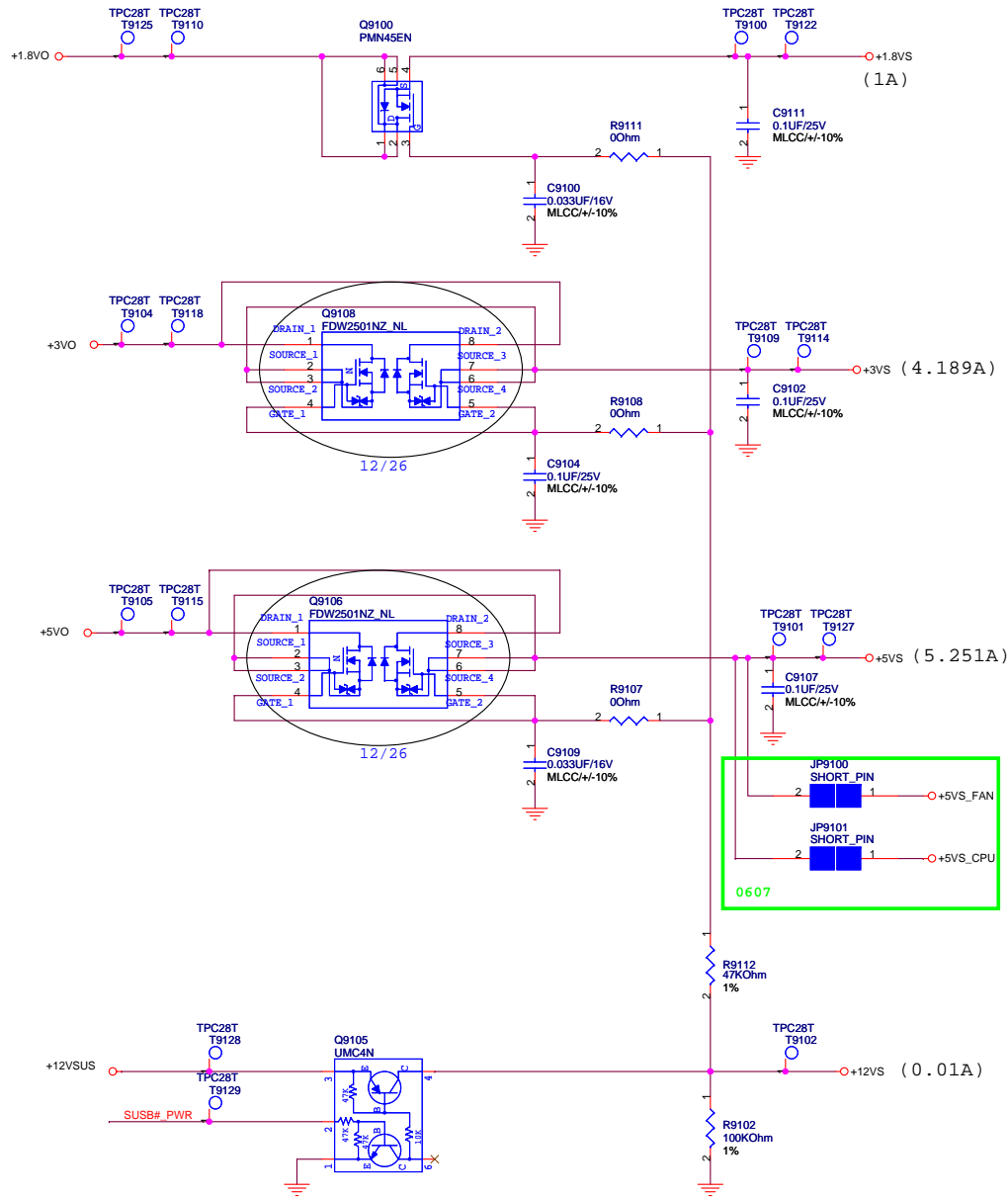
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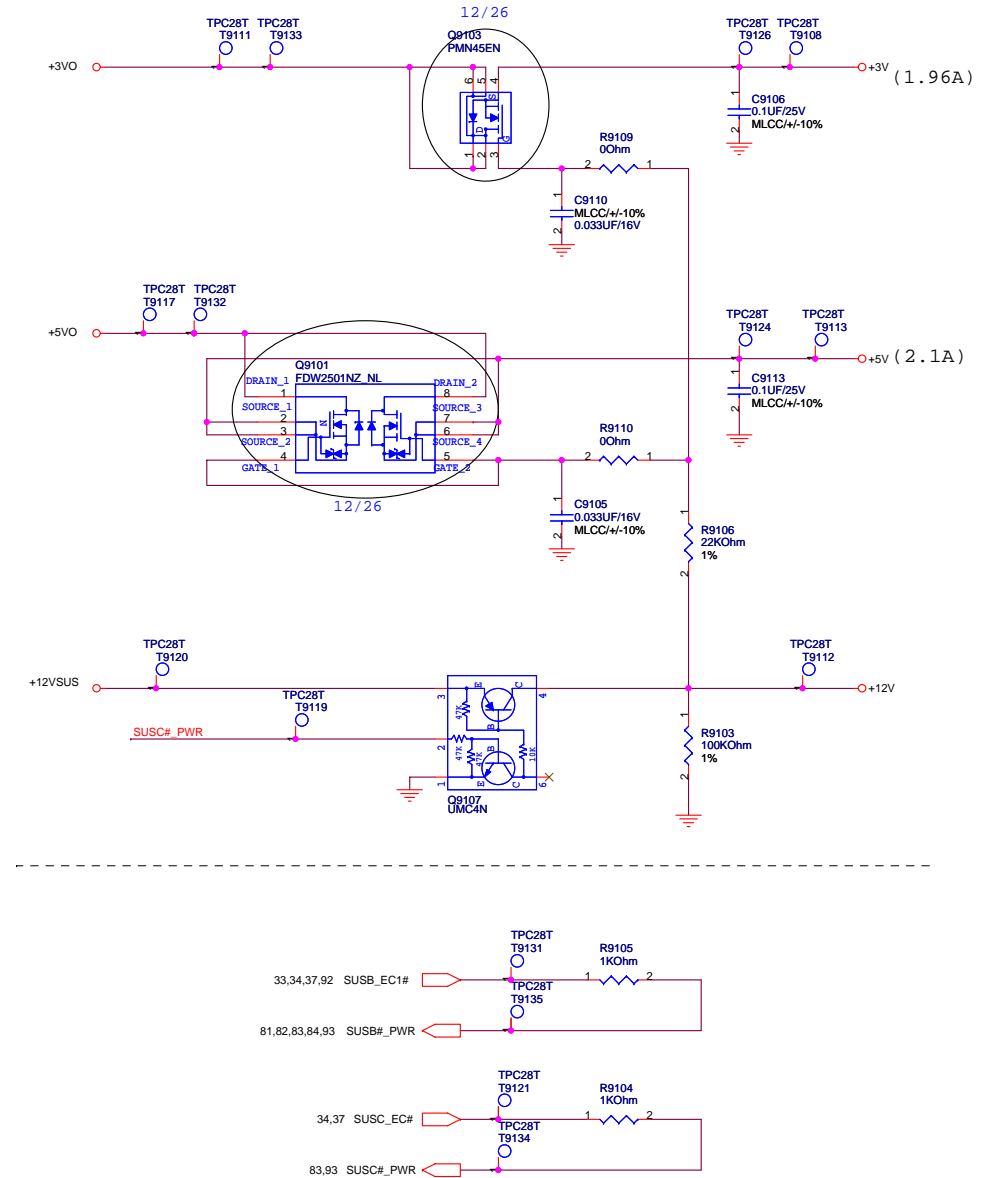
<Variant Name>

ASUS		Title :POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size Custom	Project Name F6E	Rev 1.10	
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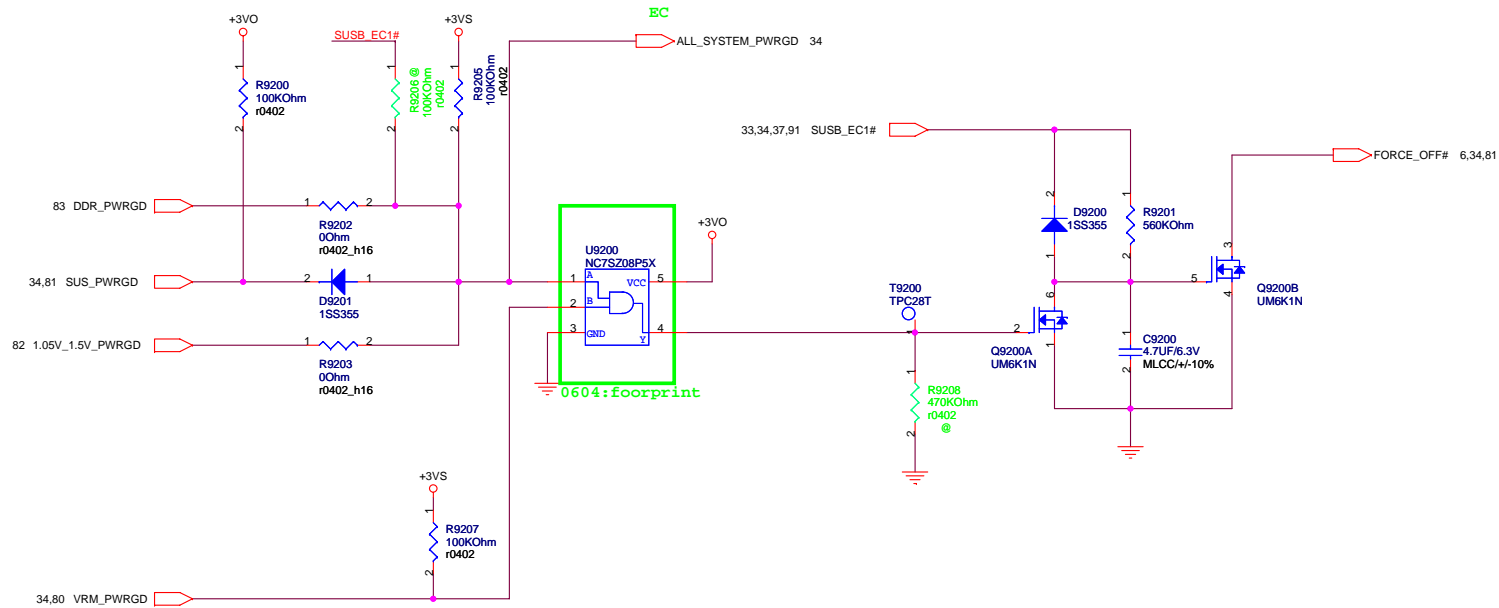
SUSB#_PWR POWER



SUSC#_PWR POWER



POWER GOOD DETECTOR



<Variant Name>



Title :POWER_PROTECT

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size
Custom

Project Name

F6E

Rev

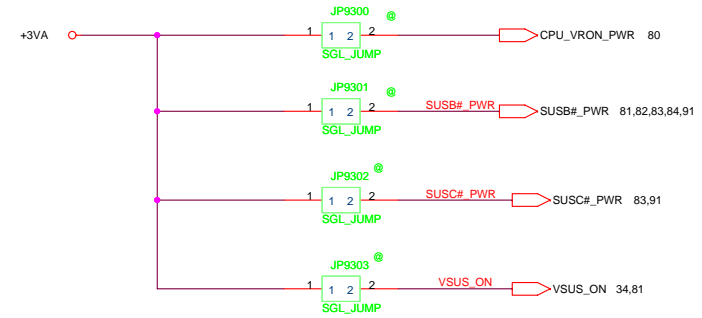
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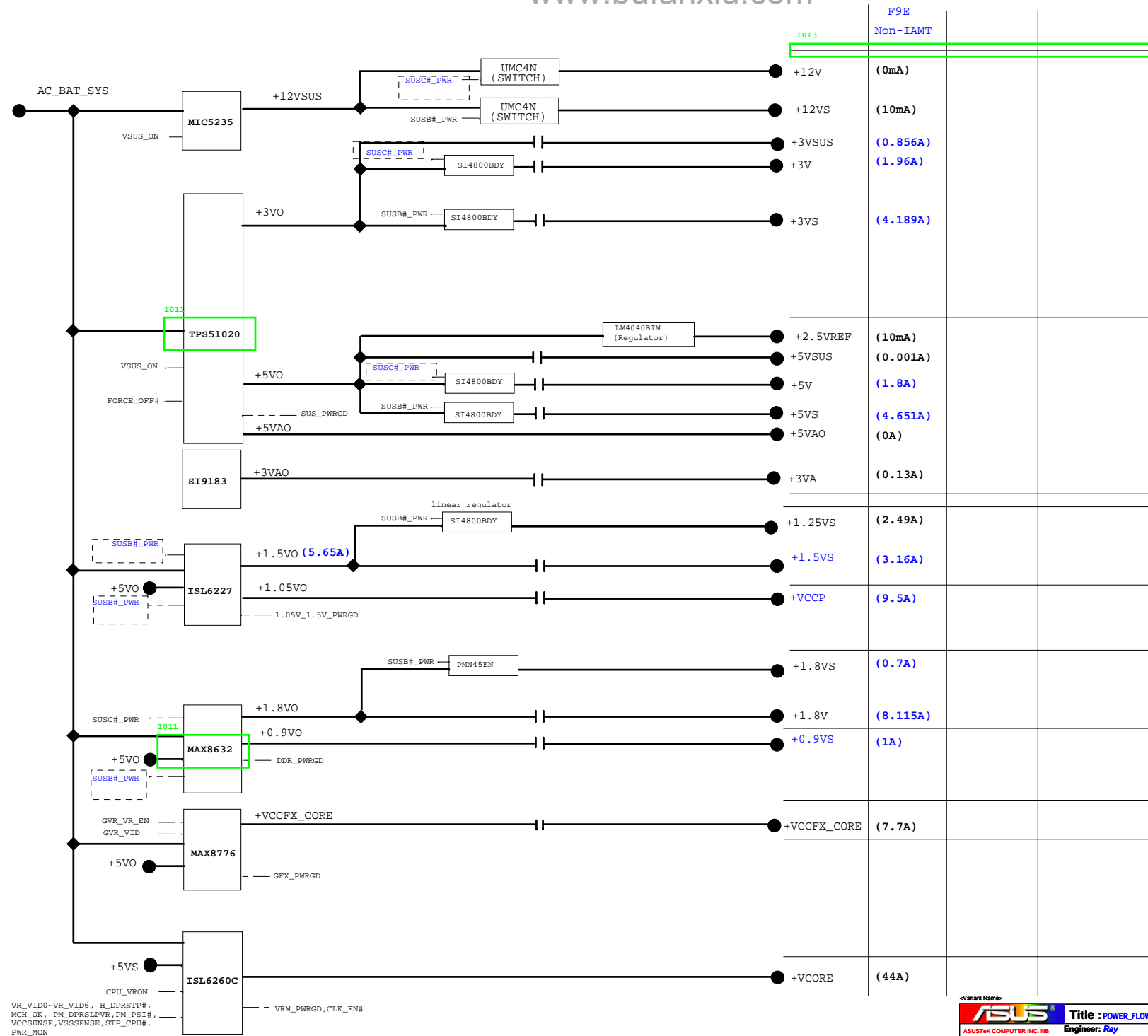
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FOR POWER TEST





<Variant Name>