


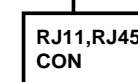
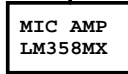
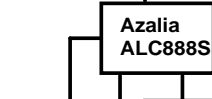
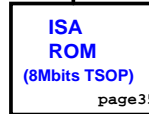
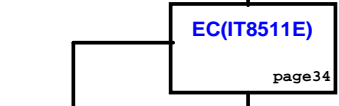
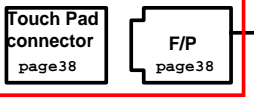
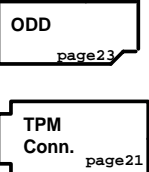
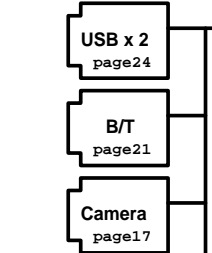
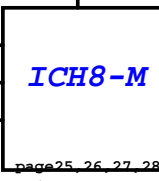
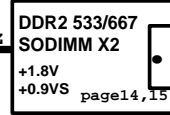
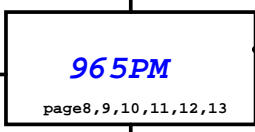
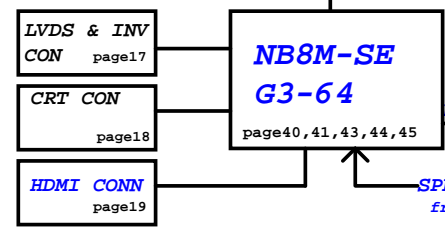
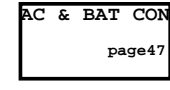
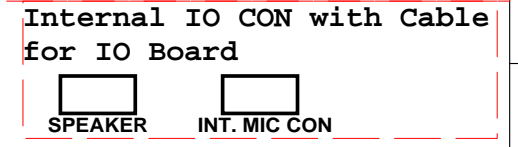
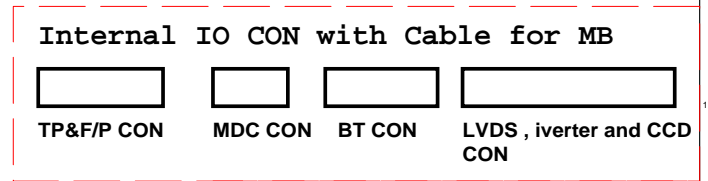
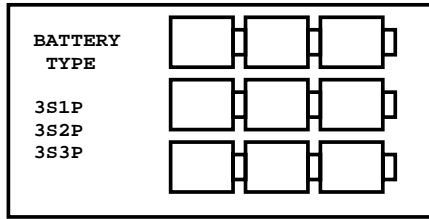
F6S SCHEMATIC Revision 1.1

PAGE	Content	PAGE	Content
SYSTEM PAGE REF.		POWER PAGE REF.	
4	CPU-MEROM(1)	47	DC & BAT IN
5	CPU-MEROM(2)	48	History(1)
6	CPU CAP, Thermal Senor	49	History(2)
7	CLOCK GEN._ICS9LPR363CGLF		
8	NB_-965PM--CPU (1)		
9	NB_-965PM--DDR2/PEG (2)		
10	NB_-965PM--DDR2 bus (3)		
11	NB_-965PM--POWER (4)		
12	NB_-965PM--POWER (5)	80_POWER_VCORE	
13	NB_-965PM--GND/Strapping (6)	81_POWER_SYSTEM	
14	DDR2 SO-DIMM_0	82_POWER_I/O_1.5VS & 1.05VS	
15	DDR2 SO-DIMM_1	83_POWER_I/O_DDR & VTT	
16	DDR2 ADDRESS TERMINATION	84_POWER_I/O_+2.5VS	
17	LVDS & INVERTER CONN	85_POWER_VGA_CORE & +1.25VO	
18	CRT conn.	86_POWER_VCCFGX (Empty)	
19	MDC,HDMI conn.	87_POWER_SHUTDOWN#	
20	PCI-E--MINI CARD--(2)_WWAN	88_POWER_CHARGER	
21	B/T,F/P& TPM	89_POWER_PIC(Empty)	
22	B TO B CONN(M)	90_POWER_PROTECT	
23	HDD & CD-ROM CONN	91_POWER_LOAD SWITCH	
24	USB PORT	92_POWER_PROTECT	
25	SB_-ICH8M--(1)-CPU, IDE, AUDIO	93_POWER_SIGNAL	
26	SB_-ICH8M--(2)-PCI, PCI-E, USB	94_POWER_FLOWCHART	
27	SB_-ICH8M--(3)-GPIO		
28	SB_-ICH8M--(4)-PWR/GND		
29	PCI-E--LAN_RTL8111B		
30	eSATA-JMB360		
31	EMPTY		
32	EMPTY		
33	NEWCARD		
34	EC-IT8511		
35	ISA ROM & KB		
36	CARD READER_RTS5158		
37	DISCHARGE		
38	Instant Key & Touch Pad		
39	LEDs		
40	NB8M-SE--PCIE (1)		
41	NB8M-SE--FB (2)		
42	NB8M-SE--VRAM (3)		
43	NB8M-SE--RGB/LCD/ROM/GPIO(4)		
44	NB8M-SE--MIOB/CRYSTAL/TMDS(5)		
45	NB8M-SE--VRAM_TERMINATOR(6)		
46	SREW HOLE		

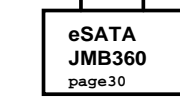
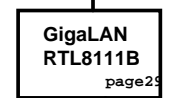
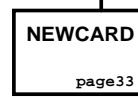
<Variant Name>

			Title : PAGE REF.	
ASUSTek COMPUTER INC			Engineer:	
Size Custom	Project Name F6S			Rev 1.1
Date: Tuesday, August 21, 2007		Sheet 1 of 94		

F6S BLOCK DIAGRAM



Daughter Board



EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	PWRLIMIT#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	
31	ECSC#/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	GIN7/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/O
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APPR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPIO	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

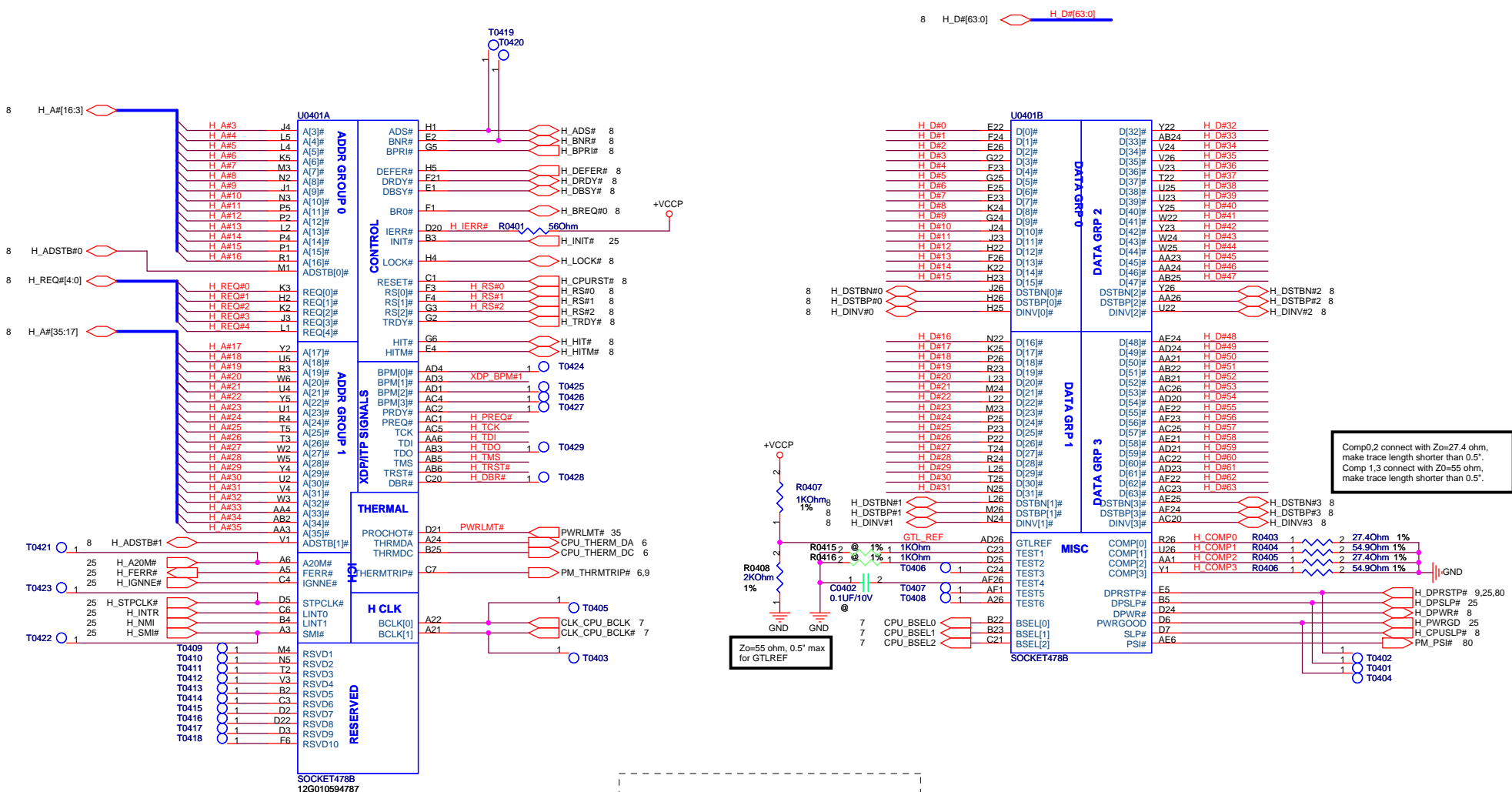
ICH8M_GPIO

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	GPI	BT_DET#	+3VS	FACH1
GPIO [5:2]	i ^{HZ}	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	GPO	BIOS_REC_?(TP)	+3VS	FACH2
GPIO 07	i	GPO	802_LED_EN	+3VS	FACH3
GPIO 08	i	GPI	EXTSM#	+3VSUS	N/A
GPIO 09	i ^{HZ}	GPO	LAN_WOL_EN_?(TP)	+3VSUS	WOL_EN
GPIO 10	i ^{HZ}	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat ^{HZ}	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SC#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i ^{HZ}	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat ¹	Native	STP_PC#	+3VSUS	STP_PC# , No-GPIO in Mobile
GPIO 16	Nat ⁰	Native	PM DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	GPO	WLAN_ON#	+3VS	FACH0
GPIO 18	O	GPO	N/A	+3VS	N/A
GPIO 19	i	GPO	CPU_SELECT	+3VS	SATA0P
GPIO 20	O	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat	Native	N/A	+3VS	LDRQ#
GPIO 24	O	GPO	MSK_PCIRST	+3VSUS	CLGP00(MEM_LED) , Not Cleared by CF9h RST event.
GPIO 25	Nat ¹	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO in Mobile
GPIO 26	Nat	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	GPO	CB_SD#_?(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO in Mobile
GPIO 33	O	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	GPO	SATACLKREQ#_?(TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_?(TP)	+3VS	SATA2GP
GPIO 37	i	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

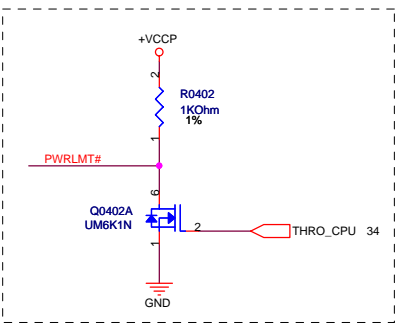
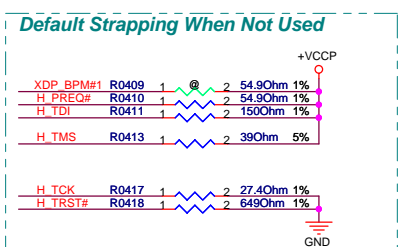
Pin	Default	Use As	Signal Name	Power	Mux
GPIO 39	i	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a	N/A	N/A	N/A	No implement
GPIO 48	i	Native		+3VS	SDATAOUT1
GPIO 49	Nat	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat ¹	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat ¹	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat ¹	Native	PCI_GNT3#	+3VS	GNT3#

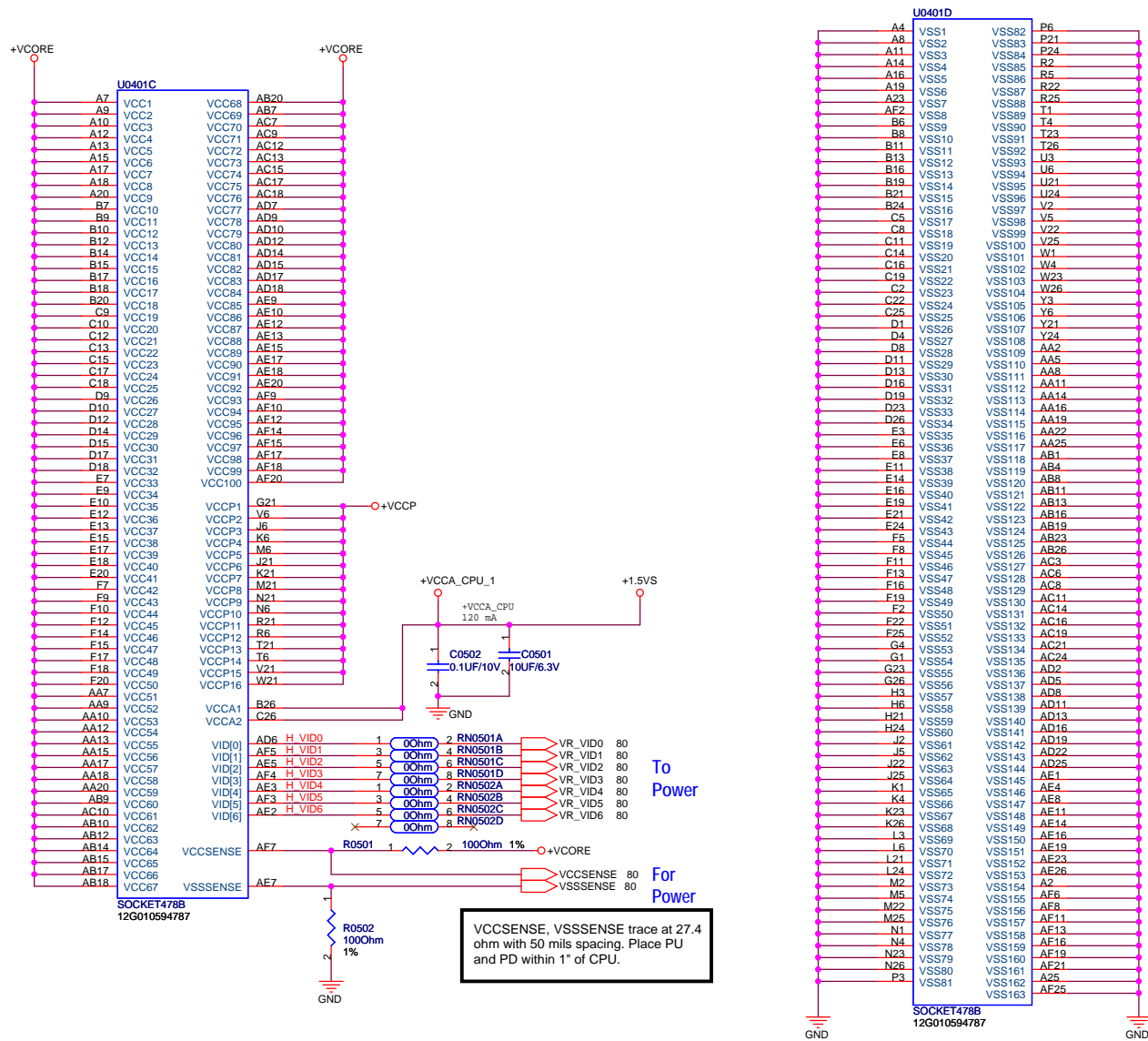
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ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007	Sheet	3	of 94



Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp 1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".





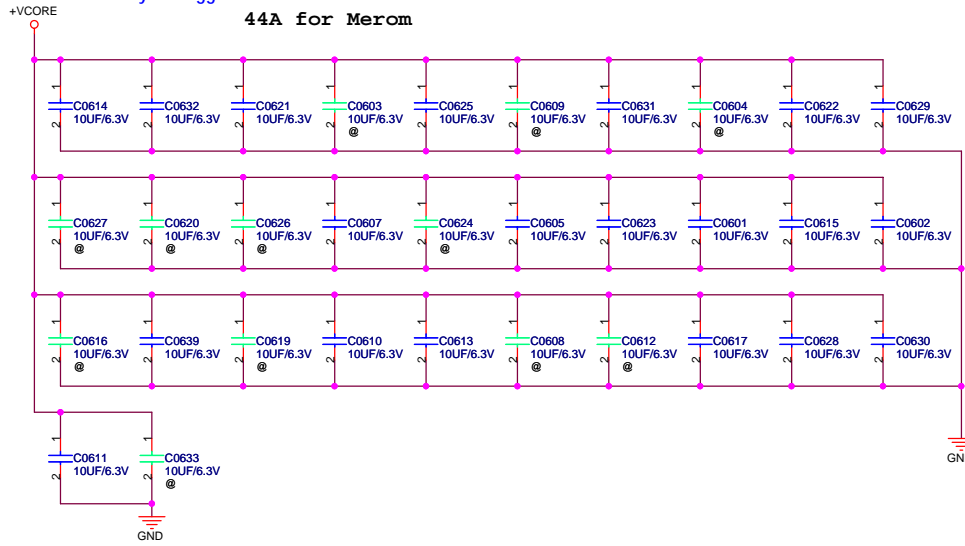
VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

<Variant Name>

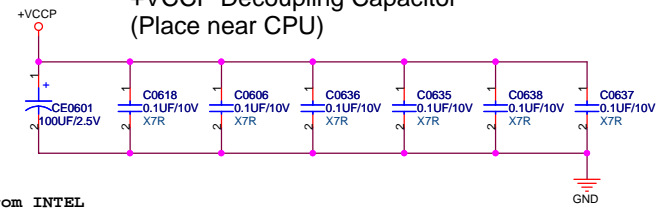
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ASUSTek COMPUTER INC		Engineer: <OrgAddr>	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet 5 of 94	

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom

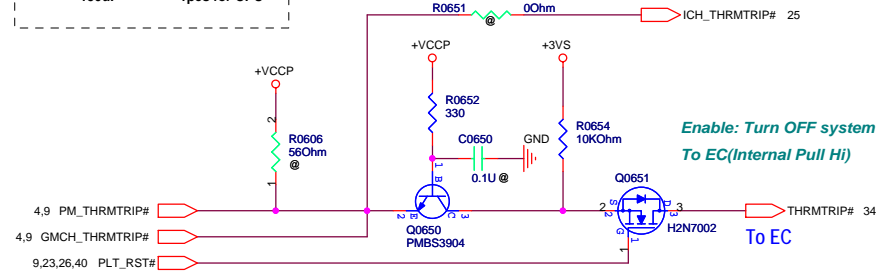


+VCCP Decoupling Capacitor (Place near CPU)

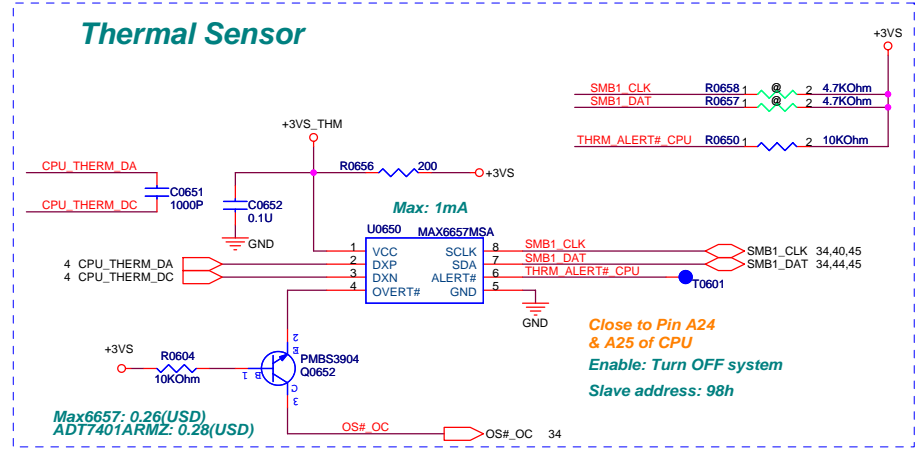


Decoupling guide from INTEL

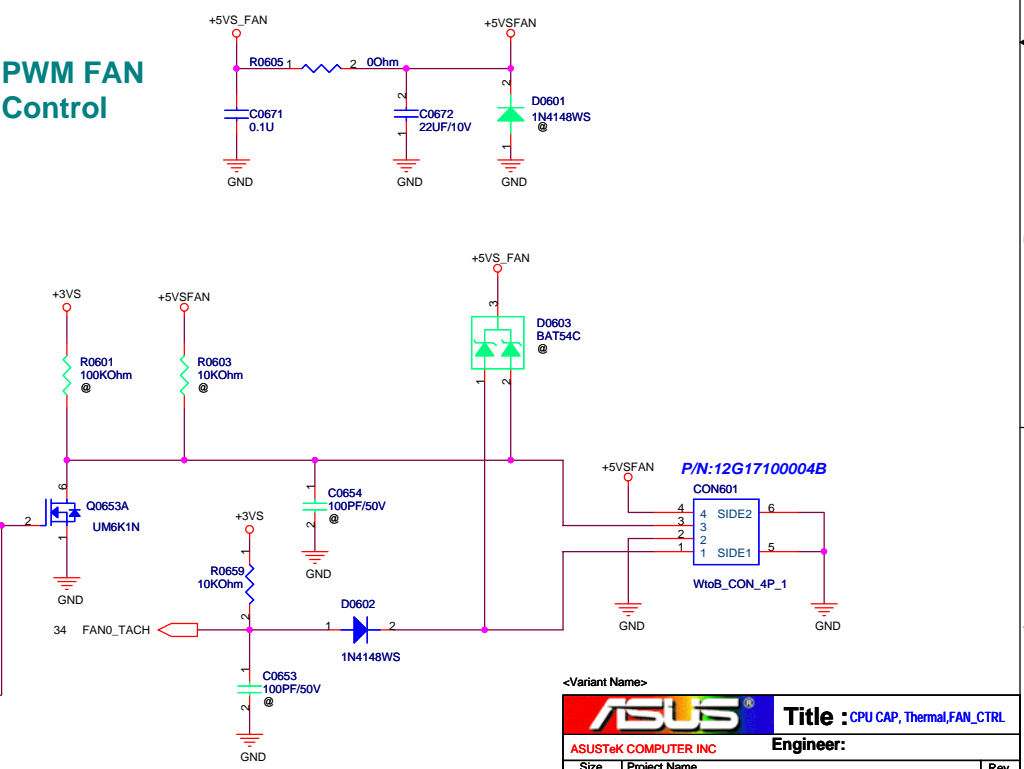
- VCCORE 22uF/10V * 32pcs
- 330uF/2V * 6pcs
- VCCP 0.1uF * 6pcs for CPU
- 150uF * 1pcs for CPU



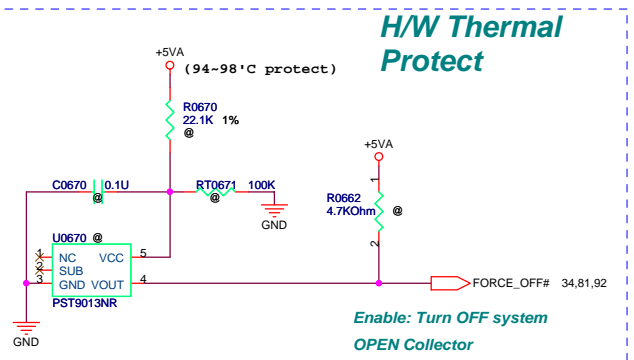
Thermal Sensor

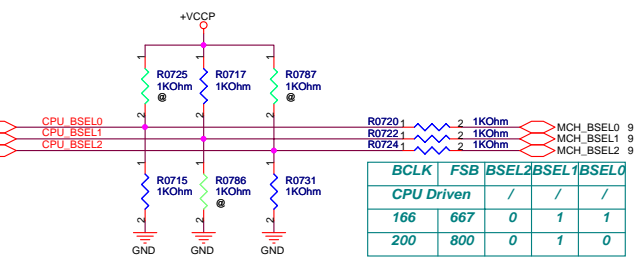
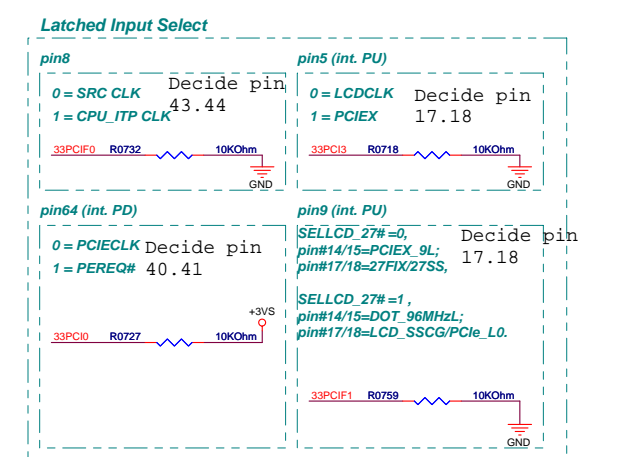
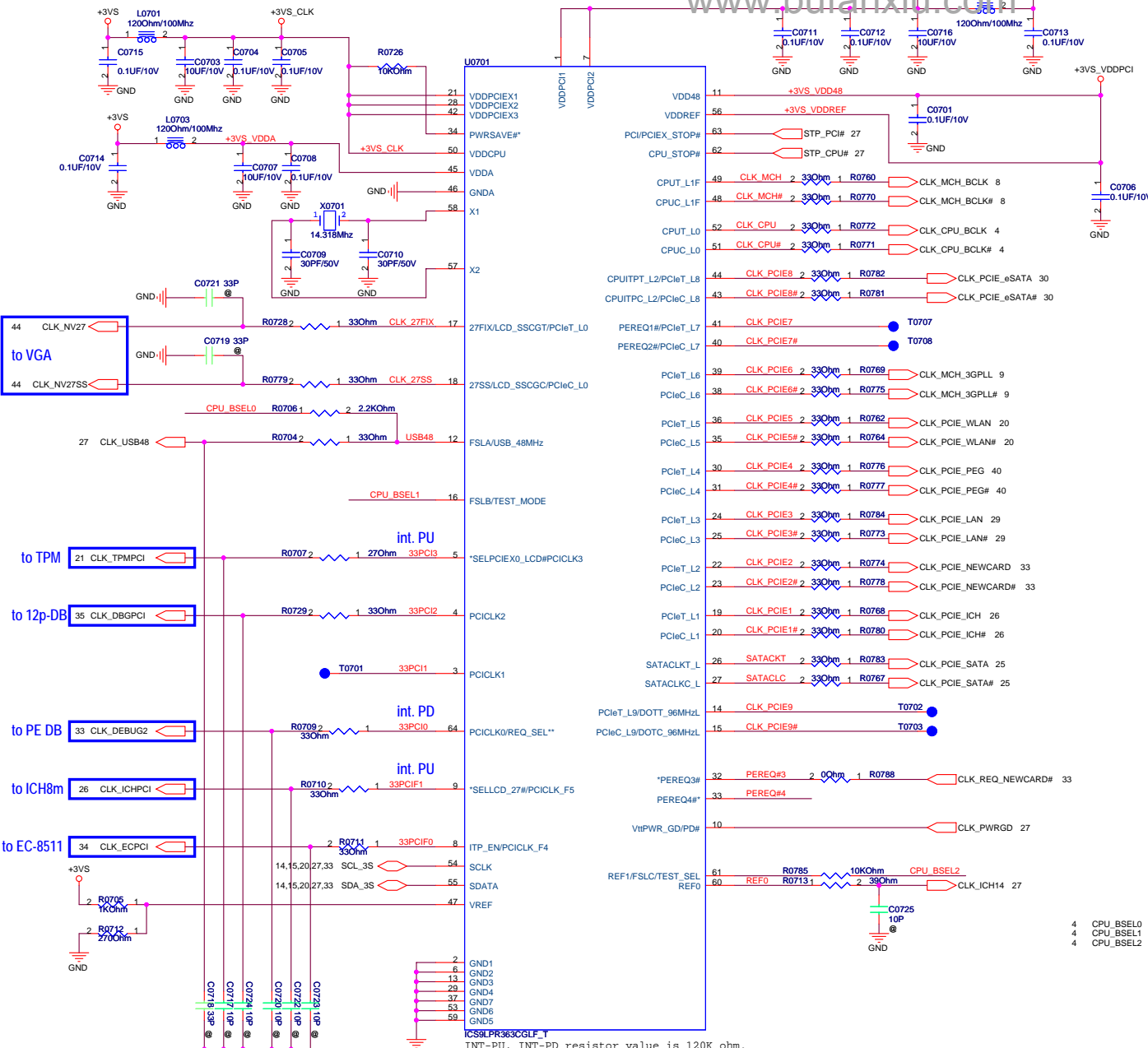


PWM FAN Control

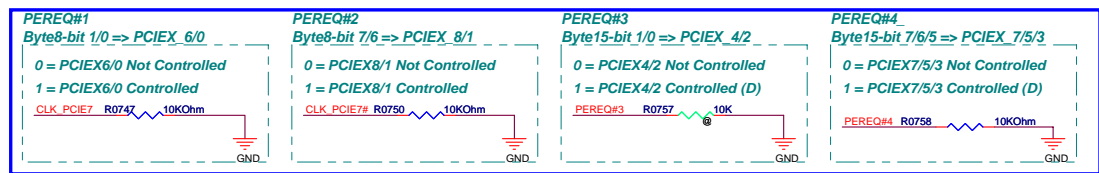


H/W Thermal Protect





BCLK	FSB	BSEL2	BSEL1	BSEL0
CPU Driven	/	/	/	/
166	667	0	1	1
200	800	0	1	0



<Variant Name>

ASUS Title: **CLOCK GEN**

ASUSTek COMPUTER INC Engineer: <OrgAddr1>

Size Project Name: **F6S**

Custom

Date: Tuesday, August 21, 2007 Sheet 7 of 94

4 H_D#[63:0] H_D#[63:0]

4 H_A#[35:3] H_A#[35:3]

U0801A

H_D#0	E2	H_D#_0	H_A#_3
H_D#1	G2	H_D#_1	B11 H_A#4
H_D#2	G7	H_D#_2	C11 H_A#5
H_D#3	M6	H_D#_3	M11 H_A#6
H_D#4	H7	H_D#_4	H_A#_7
H_D#5	H3	H_D#_5	F16 H_A#8
H_D#6	G4	H_D#_6	L13 H_A#9
H_D#7	F3	H_D#_7	G17 H_A#10
H_D#8	N8	H_D#_8	C14 H_A#11
H_D#9	H2	H_D#_9	H_A#_10
H_D#10	M10	H_D#_10	H_A#_11
H_D#11	N9	H_D#_11	H_A#_12
H_D#12	N12	H_D#_12	K16 H_A#12
H_D#13	H5	H_D#_13	H_A#_13
H_D#14	P13	H_D#_14	B13 H_A#13
H_D#15	K9	H_D#_15	L16 H_A#14
H_D#16	M2	H_D#_16	H_A#_15
H_D#17	W10	H_D#_17	H_A#_16
H_D#18	Y4	H_D#_18	B14 H_A#16
H_D#19	V4	H_D#_19	K19 H_A#17
H_D#20	M3	H_D#_20	H_A#_17
H_D#21	J1	H_D#_21	P15 H_A#18
H_D#22	N5	H_D#_22	H_A#_18
H_D#23	N3	H_D#_23	R17 H_A#19
H_D#24	W6	H_D#_24	B16 H_A#20
H_D#25	W9	H_D#_25	H20 H_A#21
H_D#26	Y7	H_D#_26	L19 H_A#22
H_D#27	Y7	H_D#_27	D17 H_A#23
H_D#28	Y9	H_D#_28	H_A#_23
H_D#29	P4	H_D#_29	M17 H_A#24
H_D#30	W3	H_D#_30	H_A#_24
H_D#31	N1	H_D#_31	N16 H_A#25
H_D#32	AD12	H_D#_32	H_A#_25
H_D#33	AE3	H_D#_33	J19 H_A#26
H_D#34	AD9	H_D#_34	B18 H_A#27
H_D#35	AC9	H_D#_35	E19 H_A#28
H_D#36	AC7	H_D#_36	H_A#_28
H_D#37	AC14	H_D#_37	B17 H_A#30
H_D#38	AD11	H_D#_38	E17 H_A#31
H_D#39	AC11	H_D#_39	C18 H_A#32
H_D#40	AB2	H_D#_40	A19 H_A#33
H_D#41	AD7	H_D#_41	B19 H_A#34
H_D#42	AB1	H_D#_42	N19 H_A#35
H_D#43	Y3	H_D#_43	
H_D#44	AC6	H_D#_44	
H_D#45	AC5	H_D#_45	
H_D#46	AG3	H_D#_46	
H_D#47	AJ9	H_D#_47	
H_D#48	AJ9	H_D#_48	
H_D#49	AH8	H_D#_49	
H_D#50	AJ14	H_D#_50	
H_D#51	AE9	H_D#_51	
H_D#52	AH11	H_D#_52	
H_D#53	AH12	H_D#_53	
H_D#54	AJ5	H_D#_54	
H_D#55	AH5	H_D#_55	
H_D#56	AJ6	H_D#_56	
H_D#57	AE7	H_D#_57	
H_D#58	AJ7	H_D#_58	
H_D#59	AJ2	H_D#_59	
H_D#60	AE5	H_D#_60	
H_D#61	AJ3	H_D#_61	
H_D#62	AH2	H_D#_62	
H_D#63	AH13	H_D#_63	

HOST

H_ADS#	G12	H_ADS#	H_ADS#_4
H_ADSTB#_0	H17	H_ADSTB#0	H_ADSTB#0_4
H_ADSTB#_1	G20	H_ADSTB#1	H_ADSTB#1_4
H_BNR#	C8	H_BNR#	H_BNR#_4
H_BPRI#	E8	H_BPRI#	H_BPRI#_4
H_BREQ#	F12	H_BREQ#0	H_BREQ#0_4
H_DEFER#	D6	H_DEFER#	H_DEFER#_4
H_DBSY#	C10	H_DBSY#	H_DBSY#_4
H_DPWR#	AM5	H_DPWR#	CLK_MCH_BCLK#_7
H_DRDY#	AM7	H_DRDY#	CLK_MCH_BCLK#_7
H_HIT#	H8	H_HIT#	H_HIT#_4
H_HITM#	K7	H_HITM#	H_HITM#_4
H_LOCK#	E4	H_LOCK#	H_LOCK#_4
H_TRDY#	G10	H_TRDY#	H_TRDY#_4
	B7		

H_DIN#_0	K5	H_DIN#0	H_DIN#0_4
H_DIN#_1	L2	H_DIN#1	H_DIN#1_4
H_DIN#_2	AD13	H_DIN#2	H_DIN#2_4
H_DIN#_3	AE13	H_DIN#3	H_DIN#3_4

H_DSTBN#_0	M7	H_DSTBN#0	H_DSTBN#0_4
H_DSTBN#_1	K3	H_DSTBN#1	H_DSTBN#1_4
H_DSTBN#_2	AD2	H_DSTBN#2	H_DSTBN#2_4
H_DSTBN#_3	AH11	H_DSTBN#3	H_DSTBN#3_4

H_DSTBP#_0	L7	H_DSTBP#0	H_DSTBP#0_4
H_DSTBP#_1	K2	H_DSTBP#1	H_DSTBP#1_4
H_DSTBP#_2	AC2	H_DSTBP#2	H_DSTBP#2_4
H_DSTBP#_3	AJ10	H_DSTBP#3	H_DSTBP#3_4

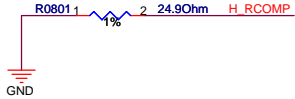
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H_REQ#_1	E13	H_REQ#1	
H_REQ#_2	A11	H_REQ#2	
H_REQ#_3	H13	H_REQ#3	
H_REQ#_4	B12	H_REQ#4	

H_RS#_0	E12	H_RS#0	H_RS#0_4
H_RS#_1	D7	H_RS#1	H_RS#1_4
H_RS#_2	D8	H_RS#2	H_RS#2_4

4 H_REQ#[4:0] H_REQ#[4:0]

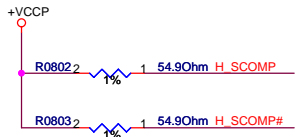
RCOMP

For Calibrating the FSB I/O Buffer



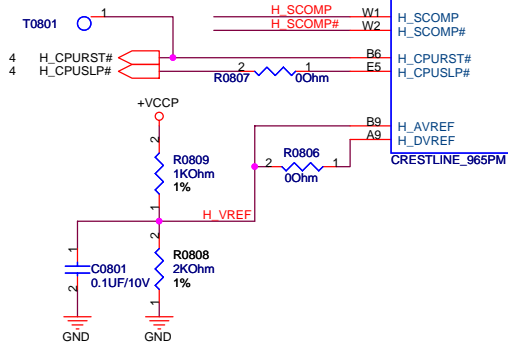
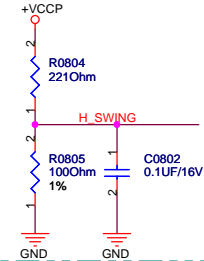
SCOMP

For Slew Rate Compensation on the FSB



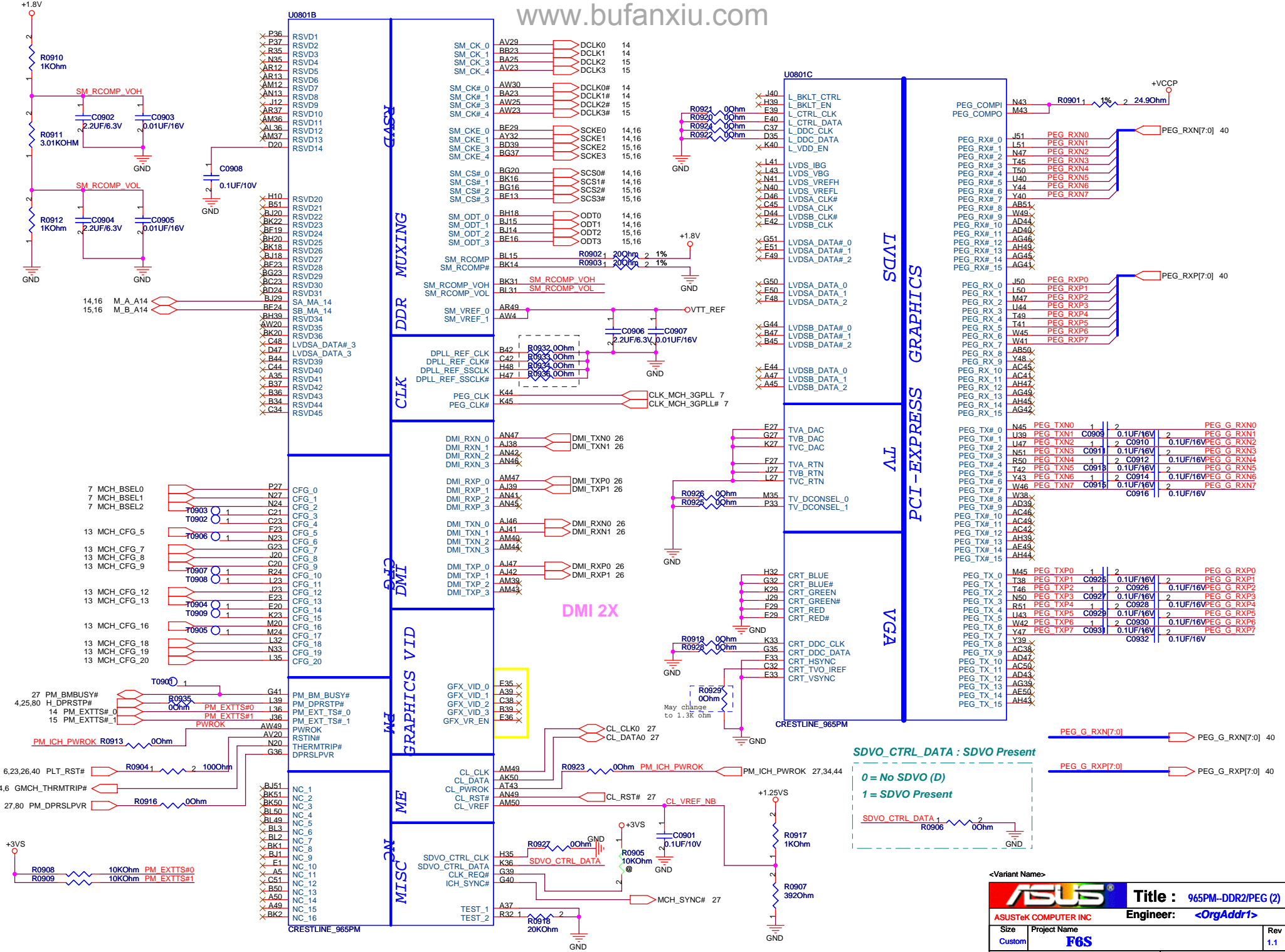
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



<Variant Name>

ASUS Title : 965PM -- CPU (1)
 ASUSTeK COMPUTER INC Engineer: <OrgAddrt>
 Size Project Name
 Custom F6S
 Date: Tuesday, August 21, 2007 Sheet 8 of 94 Rev 1.1



ASUS Title : 965PM-DDR2/PEG (2)
 ASUSTek COMPUTER INC Engineer: <OrgAddr1>
 Size: Custom Project Name: F6S
 Date: Tuesday, August 21, 2007 Sheet 9 of 94 Rev 1.1

14 M_A_DQ[0:63]

U0801D

M_A_DQ0	AR43	SA_DQ_0
M_A_DQ1	AW44	SA_DQ_1
M_A_DQ2	BA45	SA_DQ_2
M_A_DQ3	AY46	SA_DQ_3
M_A_DQ4	AR41	SA_DQ_4
M_A_DQ5	AR45	SA_DQ_5
M_A_DQ6	AW47	SA_DQ_6
M_A_DQ7	AT42	SA_DQ_7
M_A_DQ8	BR45	SA_DQ_8
M_A_DQ9	BF48	SA_DQ_9
M_A_DQ10	BG47	SA_DQ_10
M_A_DQ11	BJ45	SA_DQ_11
M_A_DQ12	BA47	SA_DQ_12
M_A_DQ13	BG50	SA_DQ_13
M_A_DQ14	BJ49	SA_DQ_14
M_A_DQ15	BE45	SA_DQ_15
M_A_DQ16	AW43	SA_DQ_16
M_A_DQ17	BE44	SA_DQ_17
M_A_DQ18	BG42	SA_DQ_18
M_A_DQ19	BE40	SA_DQ_19
M_A_DQ20	BF44	SA_DQ_20
M_A_DQ21	BJ45	SA_DQ_21
M_A_DQ22	BG40	SA_DQ_22
M_A_DQ23	BE40	SA_DQ_23
M_A_DQ24	AR40	SA_DQ_24
M_A_DQ25	AW40	SA_DQ_25
M_A_DQ26	AT39	SA_DQ_26
M_A_DQ27	AV36	SA_DQ_27
M_A_DQ28	AW41	SA_DQ_28
M_A_DQ29	AY41	SA_DQ_29
M_A_DQ30	AV38	SA_DQ_30
M_A_DQ31	AT38	SA_DQ_31
M_A_DQ32	AV13	SA_DQ_32
M_A_DQ33	AT13	SA_DQ_33
M_A_DQ34	AW11	SA_DQ_34
M_A_DQ35	AV11	SA_DQ_35
M_A_DQ36	AU15	SA_DQ_36
M_A_DQ37	AT11	SA_DQ_37
M_A_DQ38	BA13	SA_DQ_38
M_A_DQ39	BA11	SA_DQ_39
M_A_DQ40	BE10	SA_DQ_40
M_A_DQ41	BD10	SA_DQ_41
M_A_DQ42	BD8	SA_DQ_42
M_A_DQ43	AY9	SA_DQ_43
M_A_DQ44	BG10	SA_DQ_44
M_A_DQ45	AW9	SA_DQ_45
M_A_DQ46	BD7	SA_DQ_46
M_A_DQ47	BB9	SA_DQ_47
M_A_DQ48	BB5	SA_DQ_48
M_A_DQ49	AY7	SA_DQ_49
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M_A_DQ51	AT7	SA_DQ_51
M_A_DQ52	AY6	SA_DQ_52
M_A_DQ53	BB7	SA_DQ_53
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M_A_DQ56	AR9	SA_DQ_56
M_A_DQ57	AN3	SA_DQ_57
M_A_DQ58	AM8	SA_DQ_58
M_A_DQ59	AN10	SA_DQ_59
M_A_DQ60	AT9	SA_DQ_60
M_A_DQ61	AN9	SA_DQ_61
M_A_DQ62	AM9	SA_DQ_62
M_A_DQ63	AN11	SA_DQ_63

CRESTLINE_965PM

DDR SYSTEM MEMORY A

SA_BS_0	BB19	M_A_BS#0 14,16
SA_BS_1	BK19	M_A_BS#1 14,16
SA_BS_2	BF29	M_A_BS#2 14,16
SA_CAS#	BL17	M_A_CAS# 14,16
SA_DM_0	AT45	M_A_DM0
SA_DM_1	BD44	M_A_DM1
SA_DM_2	BD42	M_A_DM2
SA_DM_3	AW38	M_A_DM3
SA_DM_4	AW13	M_A_DM4
SA_DM_5	BG8	M_A_DM5
SA_DM_6	AY5	M_A_DM6
SA_DM_7	AN6	M_A_DM7
SA_DQS_0	AT46	M_A_DQS0
SA_DQS_1	BE48	M_A_DQS1
SA_DQS_2	BB43	M_A_DQS2
SA_DQS_3	BC37	M_A_DQS3
SA_DQS_4	BB16	M_A_DQS4
SA_DQS_5	BB6	M_A_DQS5
SA_DQS_6	BB2	M_A_DQS6
SA_DQS_7	AP3	M_A_DQS7
SA_DQS#_0	AT47	M_A_DQS#0
SA_DQS#_1	BD47	M_A_DQS#1
SA_DQS#_2	BC41	M_A_DQS#2
SA_DQS#_3	BA37	M_A_DQS#3
SA_DQS#_4	BA16	M_A_DQS#4
SA_DQS#_5	BH7	M_A_DQS#5
SA_DQS#_6	BC1	M_A_DQS#6
SA_DQS#_7	AP2	M_A_DQS#7
SA_MA_0	BJ19	M_A_A0
SA_MA_1	BD20	M_A_A1
SA_MA_2	BK27	M_A_A2
SA_MA_3	BH28	M_A_A3
SA_MA_4	BL24	M_A_A4
SA_MA_5	BK28	M_A_A5
SA_MA_6	BJ27	M_A_A6
SA_MA_7	BJ25	M_A_A7
SA_MA_8	BL28	M_A_A8
SA_MA_9	BA28	M_A_A9
SA_MA_10	BC19	M_A_A10
SA_MA_11	BE28	M_A_A11
SA_MA_12	BG30	M_A_A12
SA_MA_13	BJ16	M_A_A13
SA_RAS#	BE18	M_A_RAS# 14,16
SA_RCVEN#	AY20	M_A_RAS# 14,16
SA_WE#	BA19	M_A_WE# 14,16

15 M_B_DQ[0:63]

U0801E

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M_B_DQ5	AN50	SB_DQ_5
M_B_DQ6	AV50	SB_DQ_6
M_B_DQ7	AV49	SB_DQ_7
M_B_DQ8	BA50	SB_DQ_8
M_B_DQ9	BB50	SB_DQ_9
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M_B_DQ11	BE50	SB_DQ_11
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M_B_DQ13	AY49	SB_DQ_13
M_B_DQ14	BE50	SB_DQ_14
M_B_DQ15	BF49	SB_DQ_15
M_B_DQ16	BJ50	SB_DQ_16
M_B_DQ17	BJ44	SB_DQ_17
M_B_DQ18	BJ43	SB_DQ_18
M_B_DQ19	BL43	SB_DQ_19
M_B_DQ20	BK47	SB_DQ_20
M_B_DQ21	BK49	SB_DQ_21
M_B_DQ22	BK43	SB_DQ_22
M_B_DQ23	BK42	SB_DQ_23
M_B_DQ24	BJ41	SB_DQ_24
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M_B_DQ27	BJ36	SB_DQ_27
M_B_DQ28	BK41	SB_DQ_28
M_B_DQ29	BJ40	SB_DQ_29
M_B_DQ30	BL35	SB_DQ_30
M_B_DQ31	BK37	SB_DQ_31
M_B_DQ32	BK13	SB_DQ_32
M_B_DQ33	BE11	SB_DQ_33
M_B_DQ34	BK11	SB_DQ_34
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M_B_DQ41	BL9	SB_DQ_41
M_B_DQ42	BK5	SB_DQ_42
M_B_DQ43	BL5	SB_DQ_43
M_B_DQ44	BK9	SB_DQ_44
M_B_DQ45	BK10	SB_DQ_45
M_B_DQ46	BJ6	SB_DQ_46
M_B_DQ47	BJ6	SB_DQ_47
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M_B_DQ51	BC2	SB_DQ_51
M_B_DQ52	BK3	SB_DQ_52
M_B_DQ53	BF4	SB_DQ_53
M_B_DQ54	BD3	SB_DQ_54
M_B_DQ55	BJ2	SB_DQ_55
M_B_DQ56	BA3	SB_DQ_56
M_B_DQ57	BB3	SB_DQ_57
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M_B_DQ60	AY2	SB_DQ_60
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M_B_DQ63	AT2	SB_DQ_63

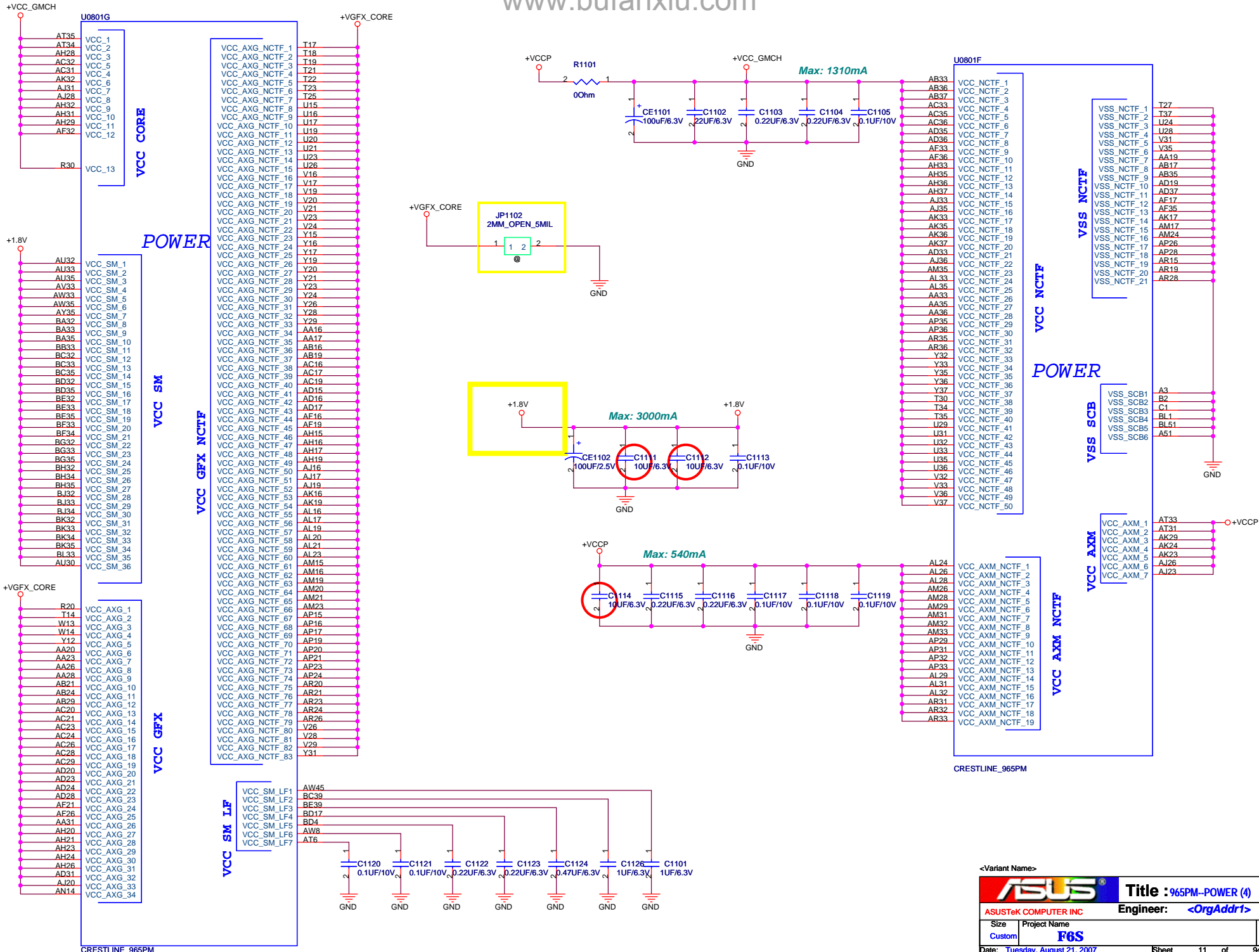
CRESTLINE_965PM

DDR SYSTEM MEMORY B

SB_BS_0	AY17	M_B_BS#0 15,16
SB_BS_1	BG18	M_B_BS#1 15,16
SB_BS_2	BG36	M_B_BS#2 15,16
SB_CAS#	BE17	M_B_CAS# 15,16
SB_DM_0	AR50	M_B_DM0
SB_DM_1	BD49	M_B_DM1
SB_DM_2	BK45	M_B_DM2
SB_DM_3	BL39	M_B_DM3
SB_DM_4	BH12	M_B_DM4
SB_DM_5	BJ7	M_B_DM5
SB_DM_6	BE3	M_B_DM6
SB_DM_7	AW2	M_B_DM7
SB_DQS_0	AT50	M_B_DQS0
SB_DQS_1	BD50	M_B_DQS1
SB_DQS_2	BK46	M_B_DQS2
SB_DQS_3	BK39	M_B_DQS3
SB_DQS_4	BL12	M_B_DQS4
SB_DQS_5	BL7	M_B_DQS5
SB_DQS_6	BE2	M_B_DQS6
SB_DQS_7	AV2	M_B_DQS7
SB_DQS#_0	AU50	M_B_DQS#0
SB_DQS#_1	BC50	M_B_DQS#1
SB_DQS#_2	BL45	M_B_DQS#2
SB_DQS#_3	BK38	M_B_DQS#3
SB_DQS#_4	BK12	M_B_DQS#4
SB_DQS#_5	BK7	M_B_DQS#5
SB_DQS#_6	BE2	M_B_DQS#6
SB_DQS#_7	AV3	M_B_DQS#7
SB_MA_0	BC18	M_B_A0
SB_MA_1	BG28	M_B_A1
SB_MA_2	BG25	M_B_A2
SB_MA_3	AW17	M_B_A3
SB_MA_4	BE25	M_B_A4
SB_MA_5	BE25	M_B_A5
SB_MA_6	BA29	M_B_A6
SB_MA_7	RC28	M_B_A7
SB_MA_8	AY28	M_B_A8
SB_MA_9	BD37	M_B_A9
SB_MA_10	BG17	M_B_A10
SB_MA_11	BE37	M_B_A11
SB_MA_12	BA39	M_B_A12
SB_MA_13	BG13	M_B_A13
SB_RAS#	AV16	M_B_RAS# 15,16
SB_RCVEN#	AY18	M_B_RAS# 15,16
SB_WE#	BC17	M_B_WE# 15,16

<Variant Name>

		Title : 965PM-DDR2 bus (3)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007	Sheet	10	of 94



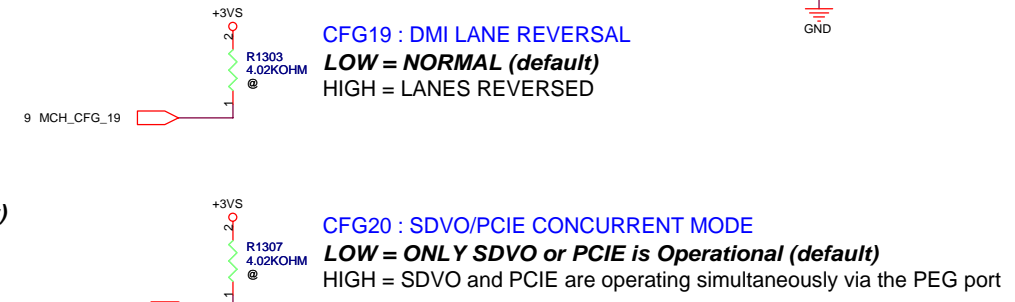
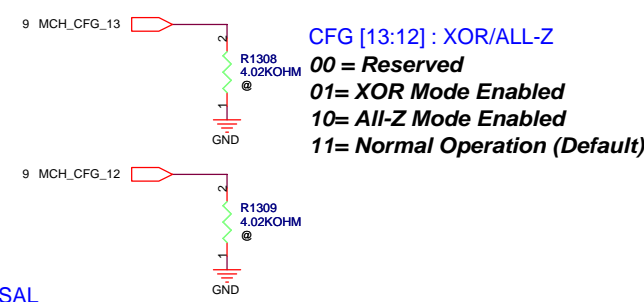
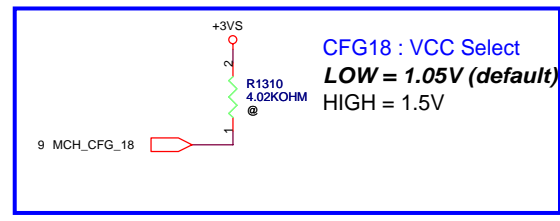
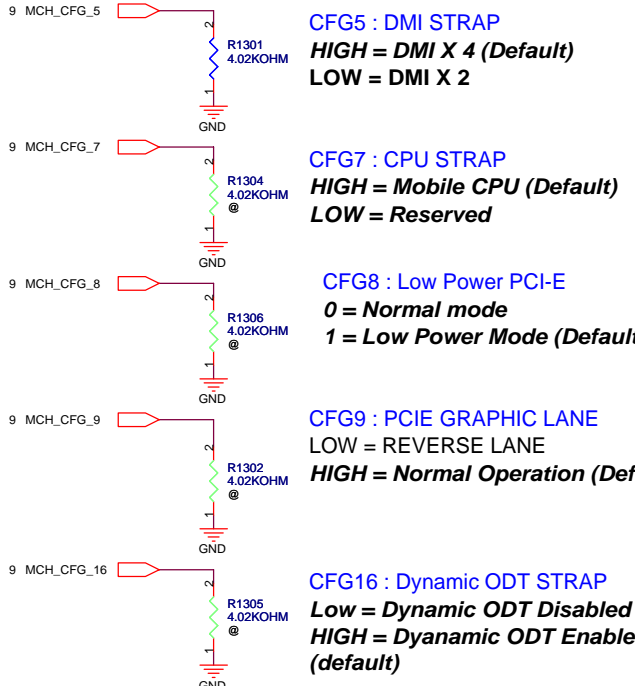
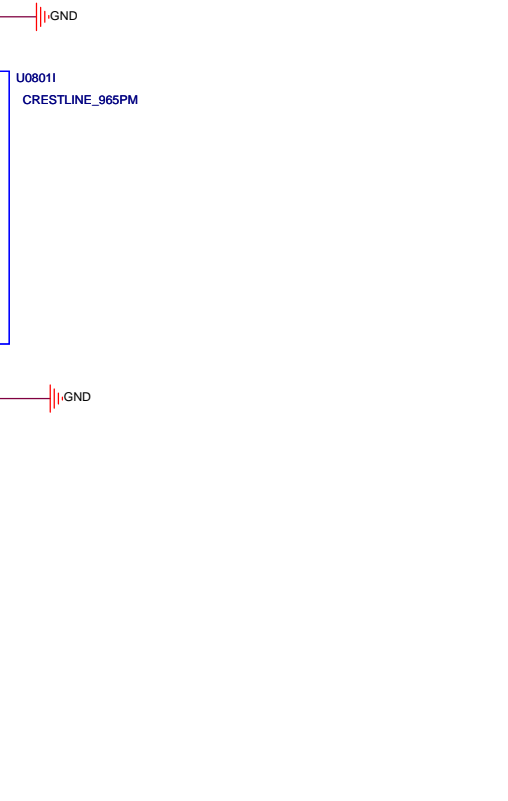
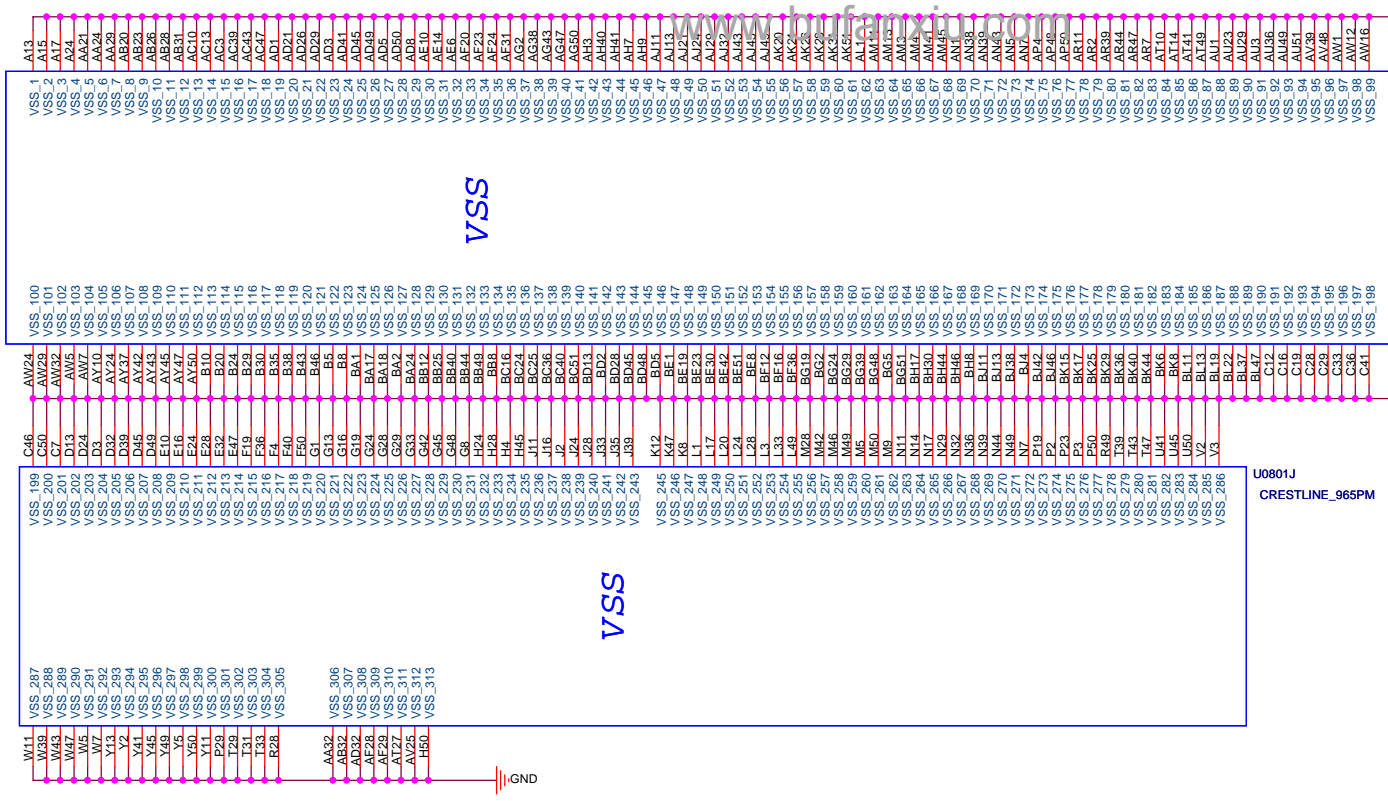
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ASUS Title : 965PM-POWER (4)

ASUSTeK COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F6S	1.1

Date: Tuesday, August 21, 2007 Sheet 11 of 94



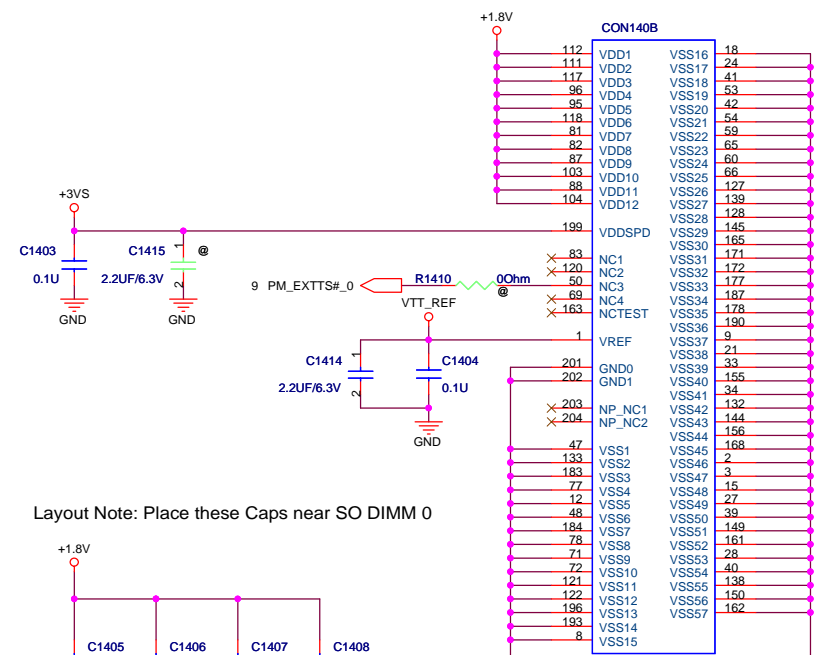
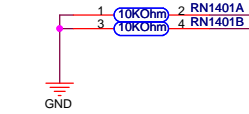
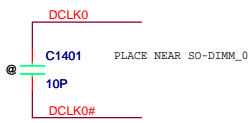
10 M_A_DQ[0..63] M_A DQ[0..63]

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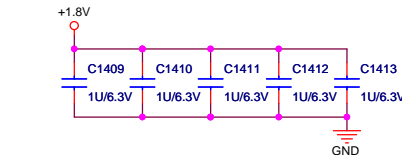
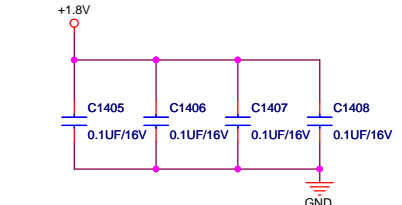
CON140A

A0	102	5	M_A DQ4
A1	101	7	M_A DQ0
A2	100	17	M_A DQ2
A3	99	19	M_A DQ1
A4	97	4	M_A DQ5
A5	94	6	M_A DQ6
A6	94	14	M_A DQ3
A7	92	16	M_A DQ7
A8	93	23	M_A DQ15
A9	91	25	M_A DQ11
A10/AP	105	35	M_A DQ9
A11	90	37	M_A DQ10
A12	89	20	M_A DQ12
A13	116	22	M_A DQ8
A14	86	36	M_A DQ13
A15	84	38	M_A DQ14
A16_BA2	85	43	M_A DQ21
BA0	107	45	M_A DQ18
BA1	106	55	M_A DQ22
SA0	110	57	M_A DQ23
SA1	110	44	M_A DQ17
CK0	115	46	M_A DQ20
CK1	30	56	M_A DQ16
CKE0	92	58	M_A DQ19
CKE1	164	61	M_A DQ28
CAS#	113	63	M_A DQ29
RAS#	108	73	M_A DQ25
WE#	109	75	M_A DQ26
SA0	198	62	M_A DQ24
SA1	200	64	M_A DQ27
SDA	197	74	M_A DQ31
SDA_3S	195	76	M_A DQ30
ODT0	114	123	M_A DQ32
ODT1	119	125	M_A DQ36
DM0	10	135	M_A DQ34
DM1	26	137	M_A DQ37
DM2	52	124	M_A DQ38
DM3	67	126	M_A DQ33
DM4	130	134	M_A DQ35
DM5	147	136	M_A DQ39
DM6	170	141	M_A DQ44
DM7	185	143	M_A DQ45
DQS0	13	151	M_A DQ46
DQS1	31	153	M_A DQ43
DQS2	51	140	M_A DQ47
DQS3	70	142	M_A DQ41
DQS4	131	152	M_A DQ40
DQS5	148	154	M_A DQ42
DQS6	169	157	M_A DQ49
DQS7	188	159	M_A DQ54
DQS#0	11	173	M_A DQ51
DQS#1	29	175	M_A DQ50
DQS#2	49	158	M_A DQ48
DQS#3	68	160	M_A DQ53
DQS#4	129	174	M_A DQ52
DQS#5	146	176	M_A DQ55
DQS#6	167	179	M_A DQ61
DQS#7	186	181	M_A DQ56
DQ62		188	M_A DQ58
DQ63		191	M_A DQ59
		180	M_A DQ60
		182	M_A DQ57
		192	M_A DQ62
		194	M_A DQ63

DDR2_DIMM_200P
DDR2 DIMM 200P,1.8V,H:4mm,STD
12G025022004



Layout Note: Place these Caps near SO DIMM 0



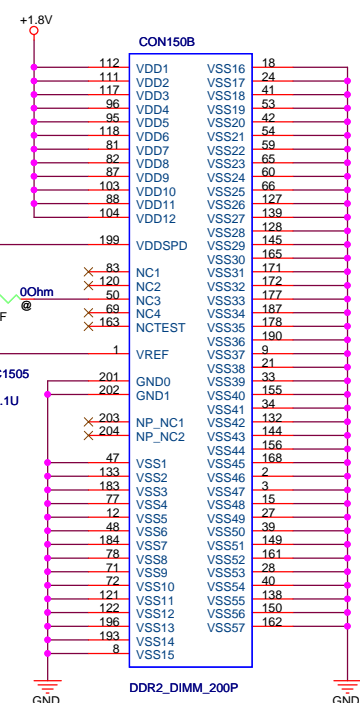
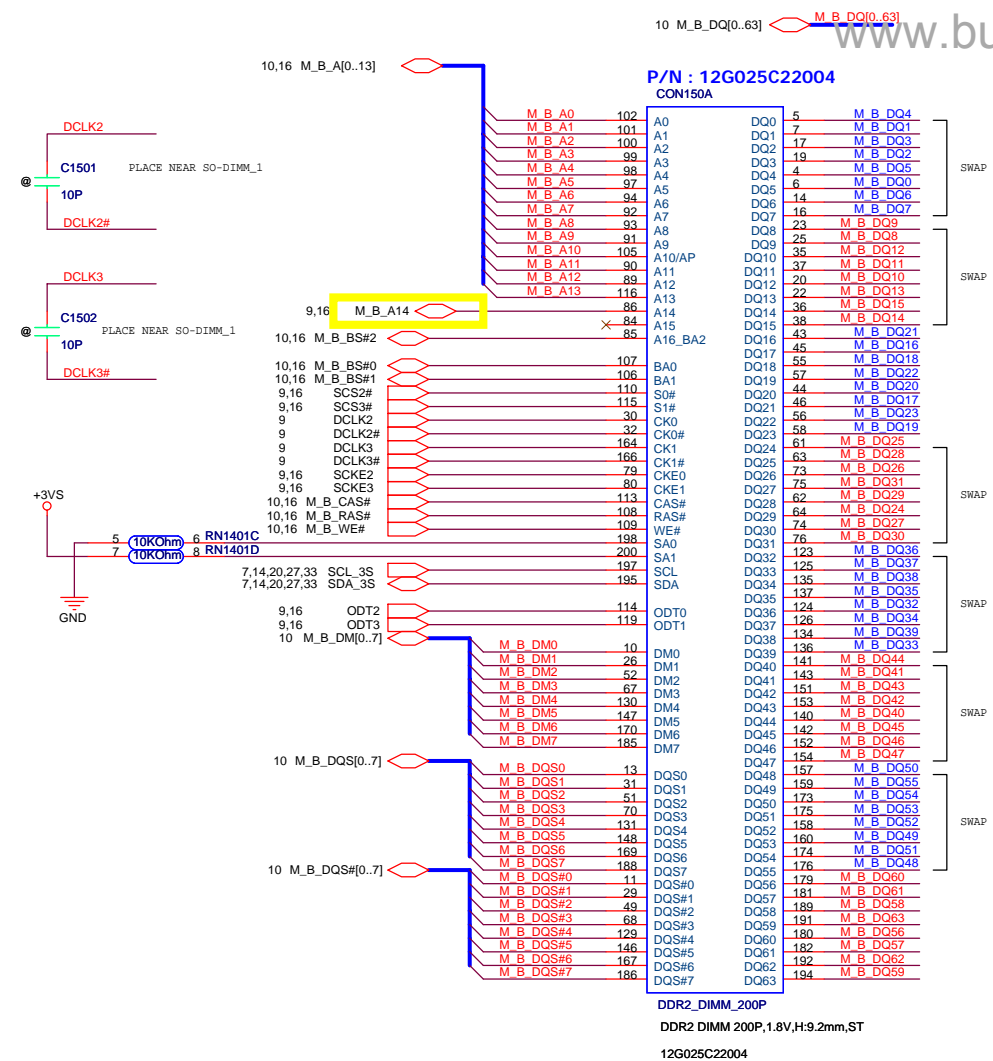
<Variant Name>

ASUS Title : DDR SO-DIMM 0

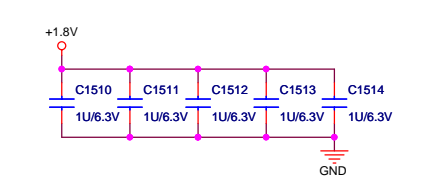
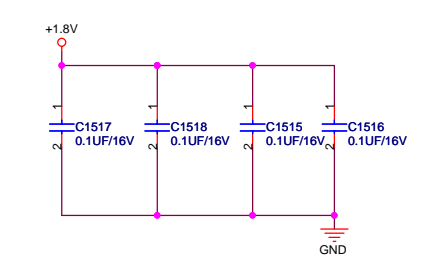
ASUSTek COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F6S	1.1

Date: Tuesday, August 21, 2007 Sheet 14 of 94



Layout Note: Place these Caps near SO DIMM 1



DDR2_DIMM_200P
DDR2 DIMM 200P,1.8V,H:9.2mm,ST
12G025C22004

<Variant Name>

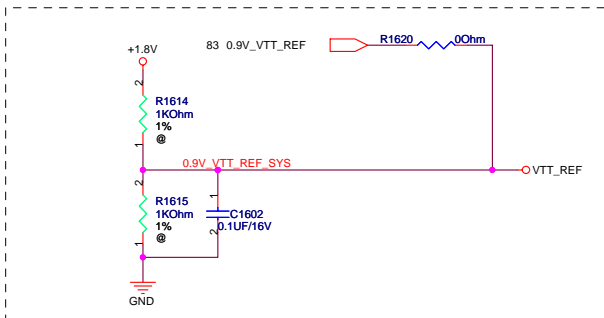
ASUS Title : **DDR SO-DIMM_1**

ASUSTek COMPUTER INC Engineer: <OrgAddr1>

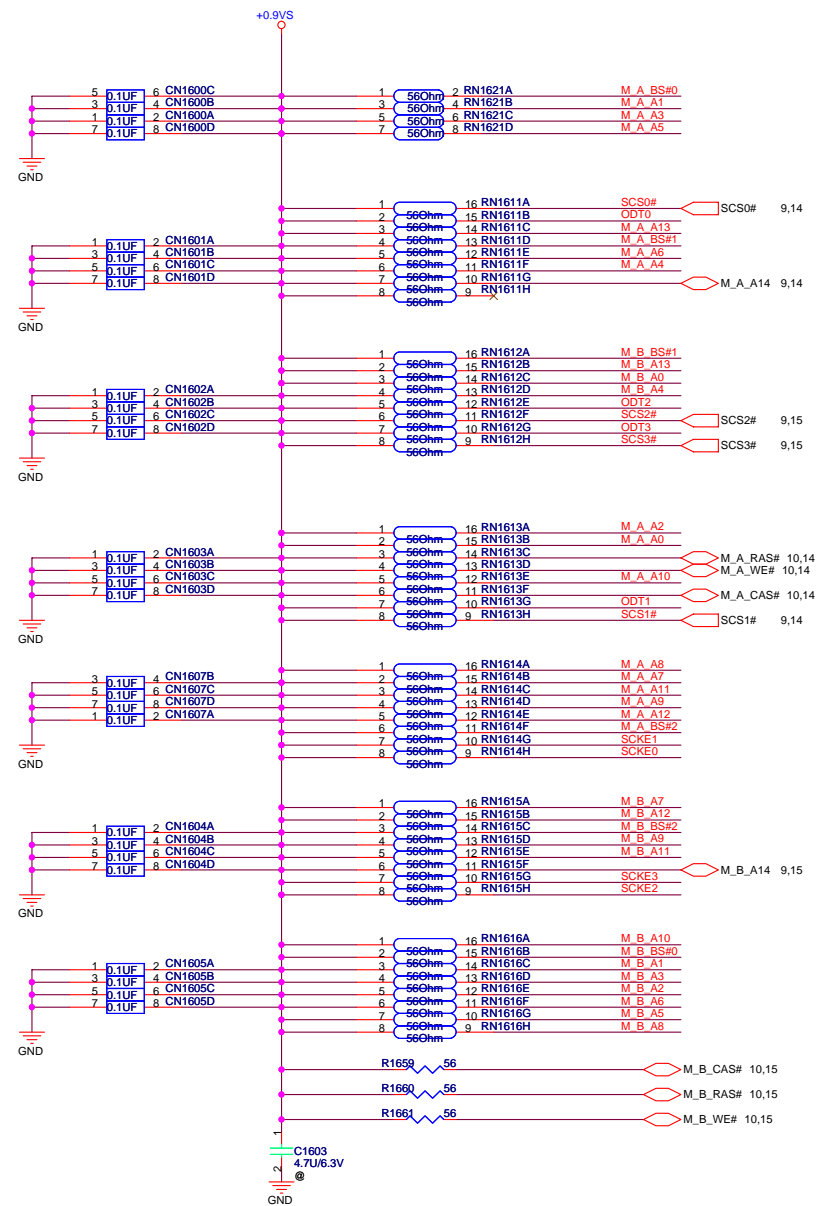
Size	Project Name	Rev
Custom	F6S	1.1

Date: Tuesday, August 21, 2007 Sheet 15 of 94

SWAPPED



- M_A_A[0..13] 10,14
- M_A_BS#[0..2] 10,14
- M_B_A[0..13] 10,15
- M_B_BS#[0..2] 10,15
- SCKE[0:3] 9,14,15
- ODT[0:3] 9,14,15

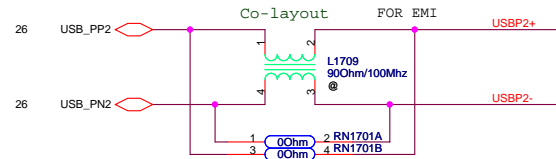
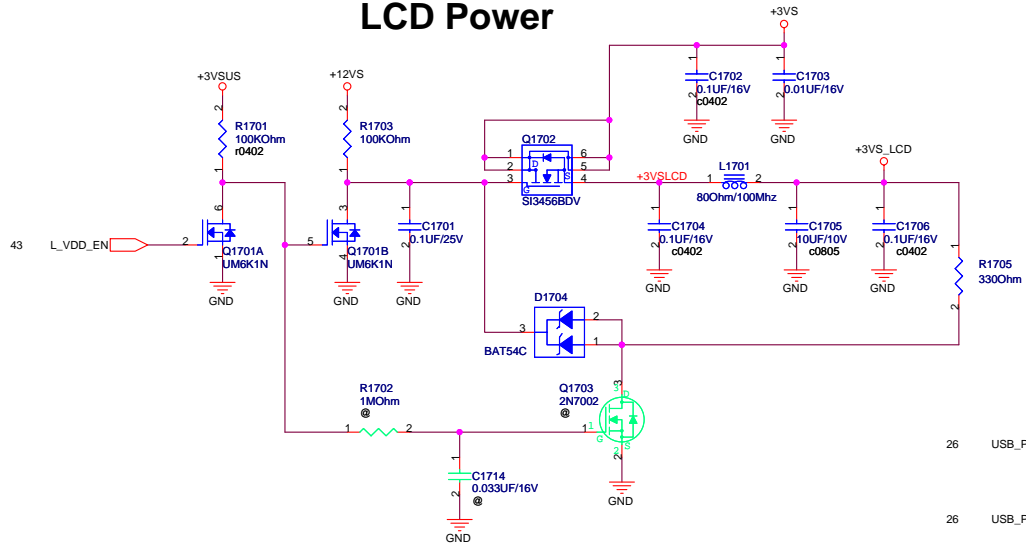


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

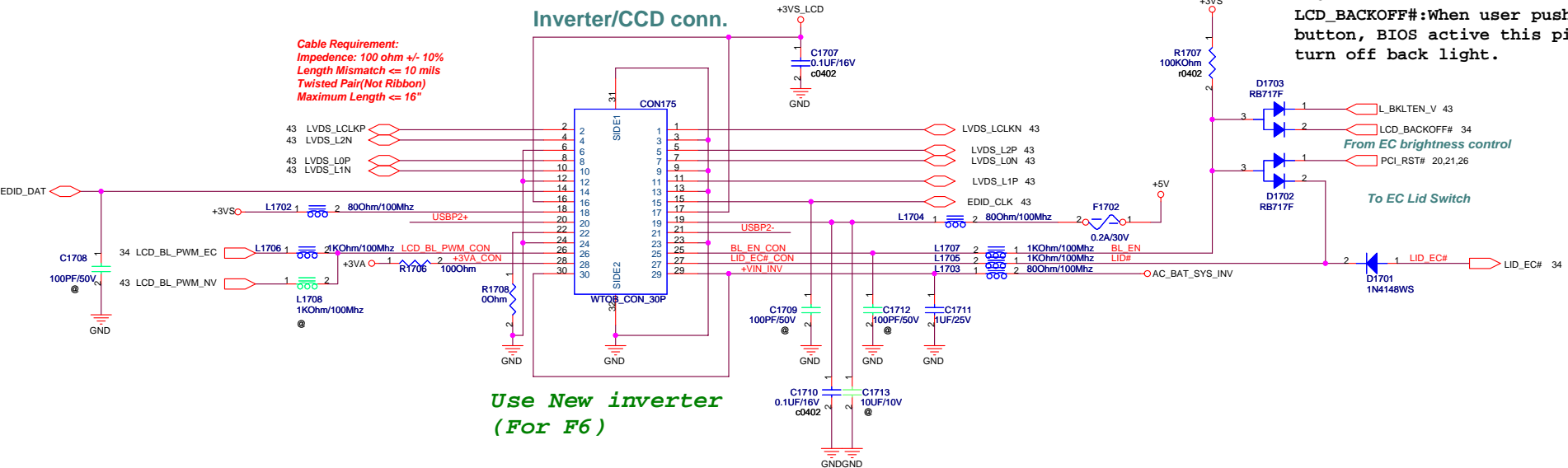
ASUS		Title : DDR2 ADDR TERM
ASUSTek COMPUTER INC		Engineer: <OrgAddr>
Size Custom	Project Name F6S	Rev 1.1
Date: Tuesday, August 21, 2007	Sheet 16	of 94

LCD Power



Cable Requirement:
 Impedence: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

Inverter/CCD conn.



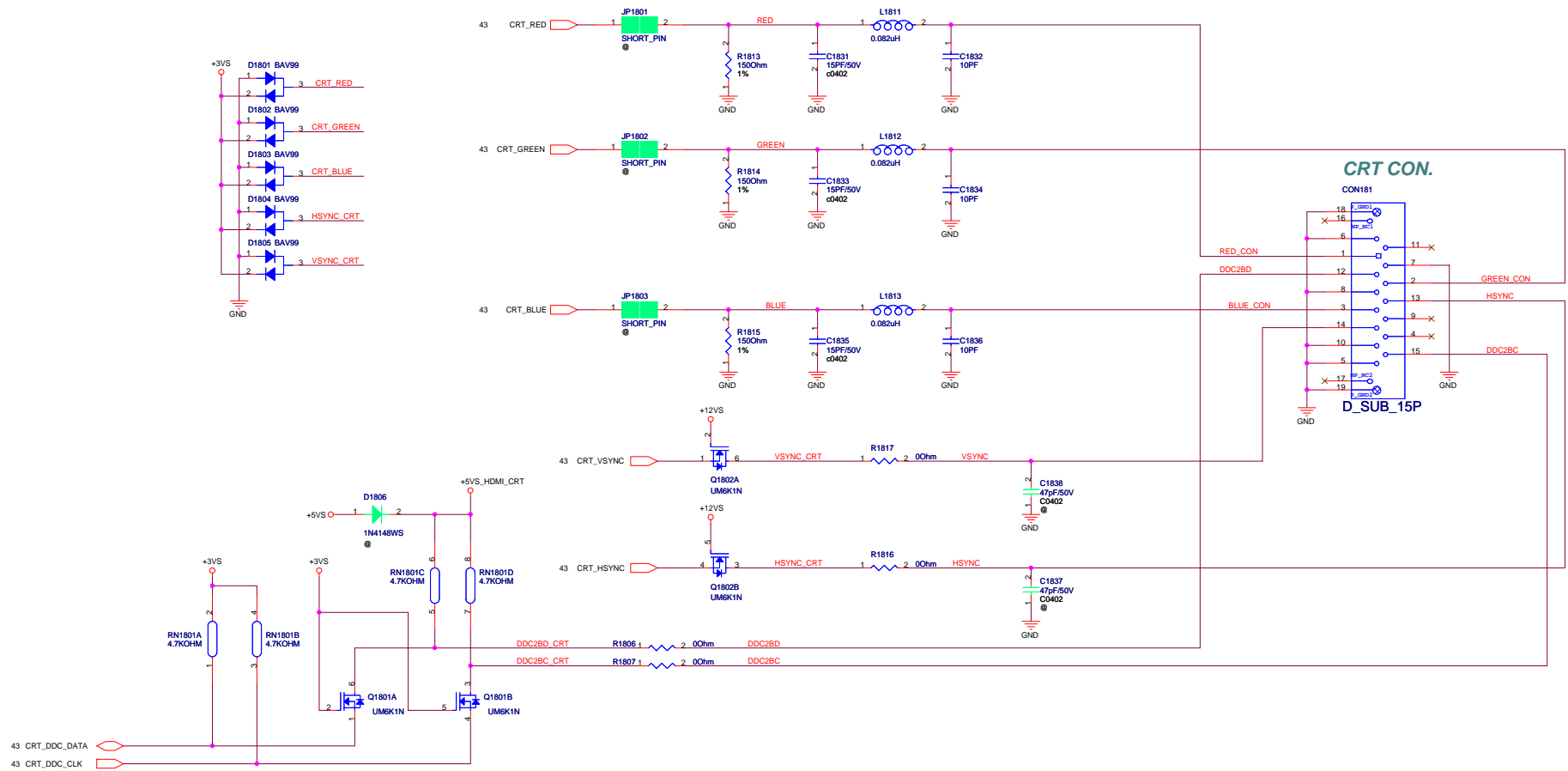
**Use New inverter
 (For F6)**

BIOS
 LCD_BACKOFF#:When user push "Fn+F7"
 button, BIOS active this pin to
 turn off back light.

From EC brightness control
 L_BKLTEN_V 43
 LCD_BACKOFF# 34
 PCI_RST# 20,21,26

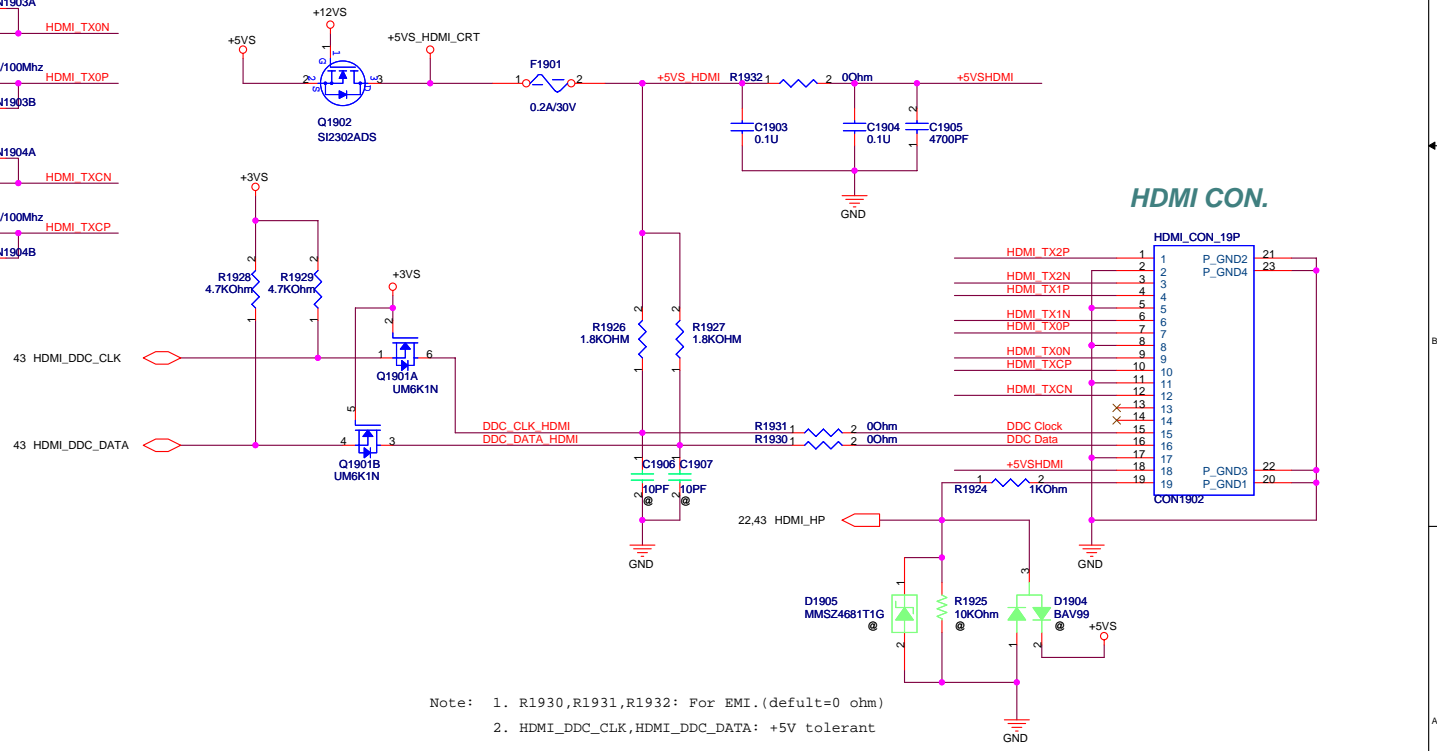
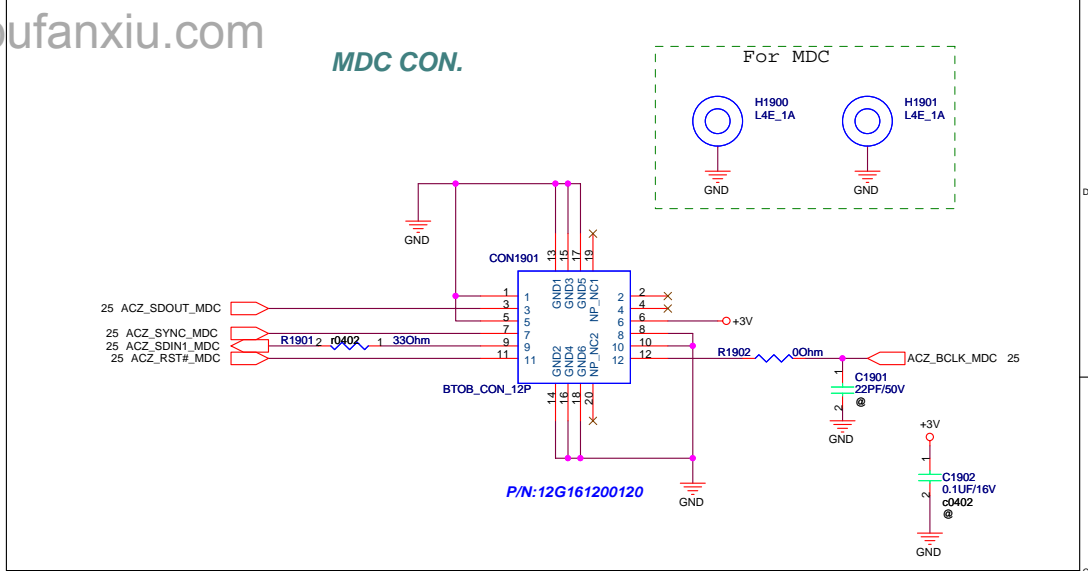
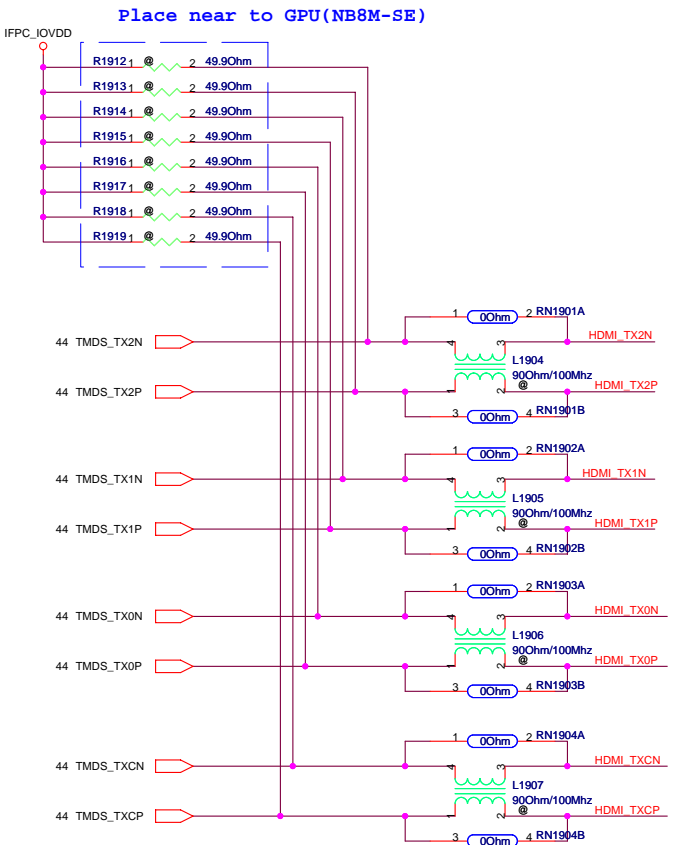
To EC Lid Switch
 LID_EC# 34

ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007	Sheet 17	of 94	



<Variant Name>

ASUS		Title : CRT
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
C	F6S	1.1
Date: Tuesday, August 21, 2007		Sheet 18 of 94



Note: 1. R1930,R1931,R1932: For EMI.(default=0 ohm)
 2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant

<Variant Name>

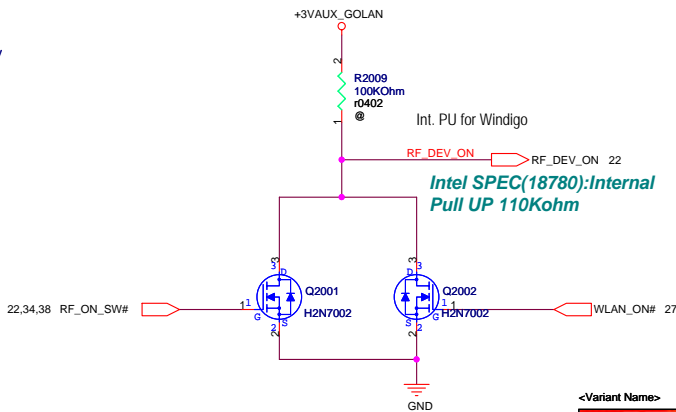
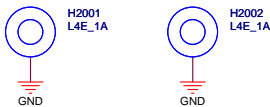
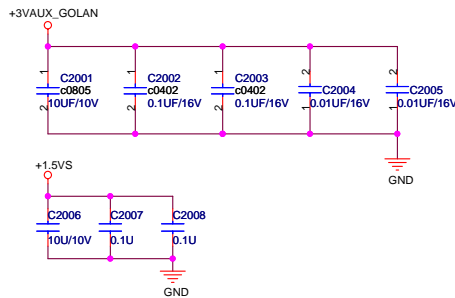
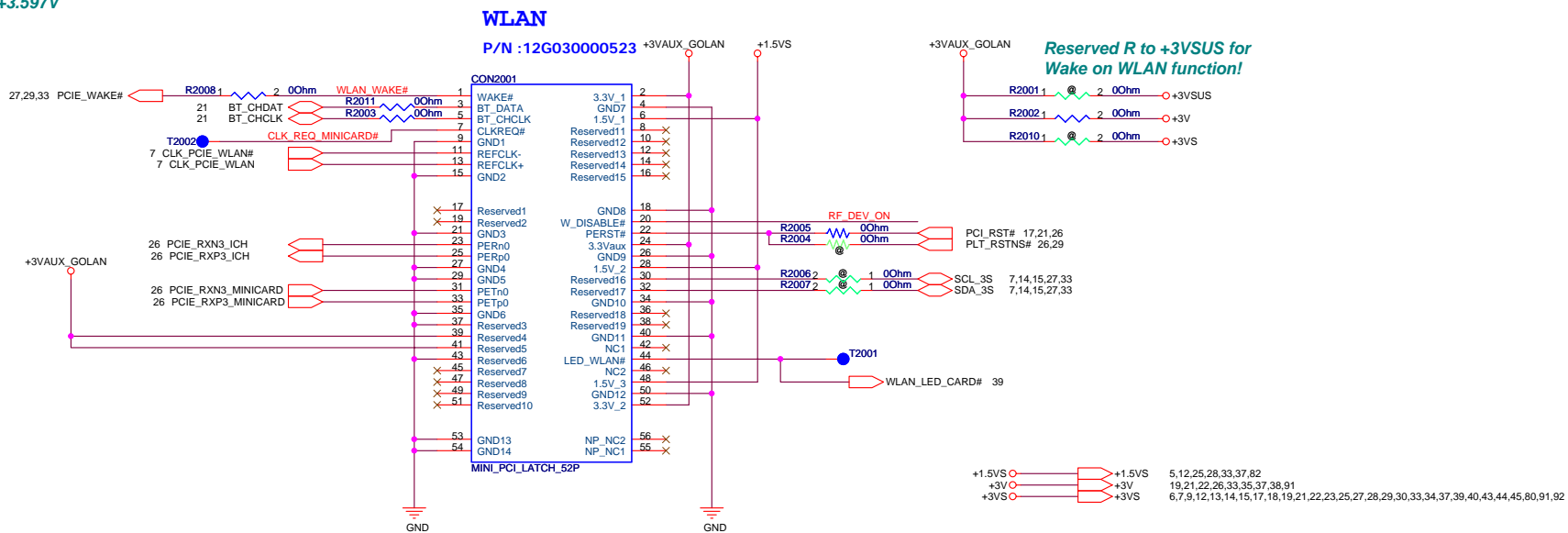
ASUS Title : MDC,HDMI CON

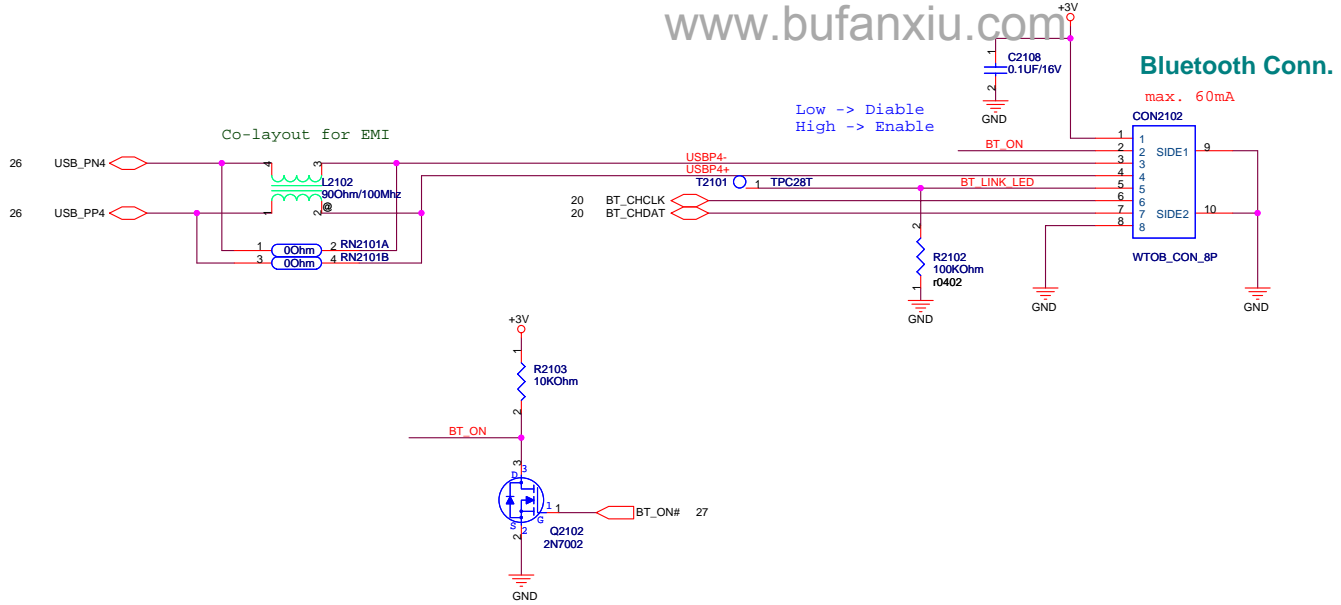
ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F6S	1.1

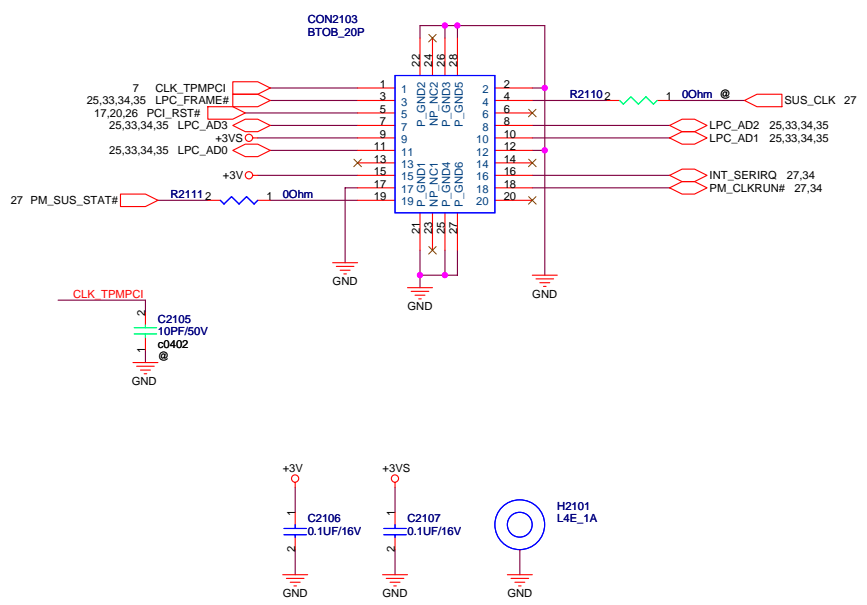
Date: Tuesday, August 21, 2007 Sheet 19 of 94

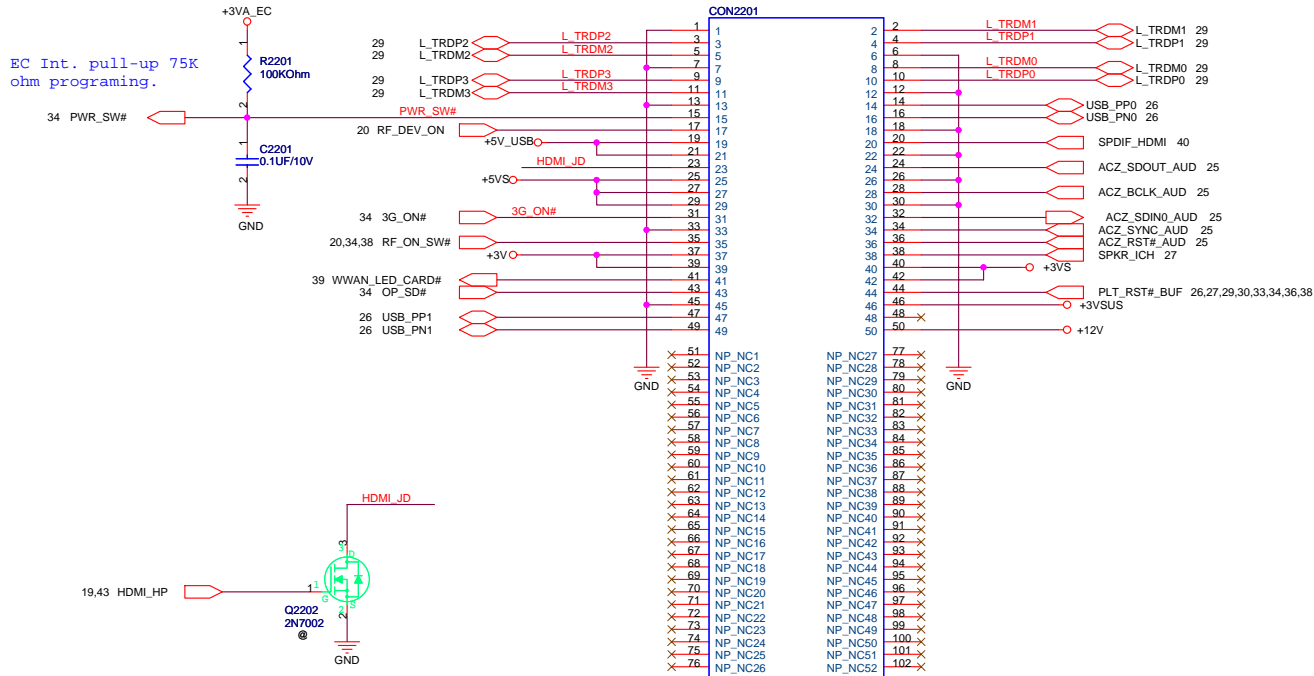
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA



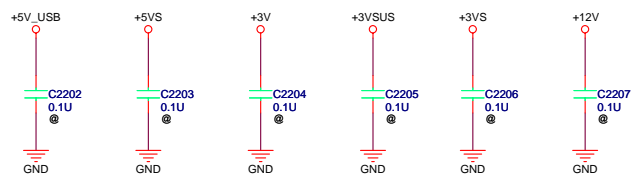


TPM Module Conn.

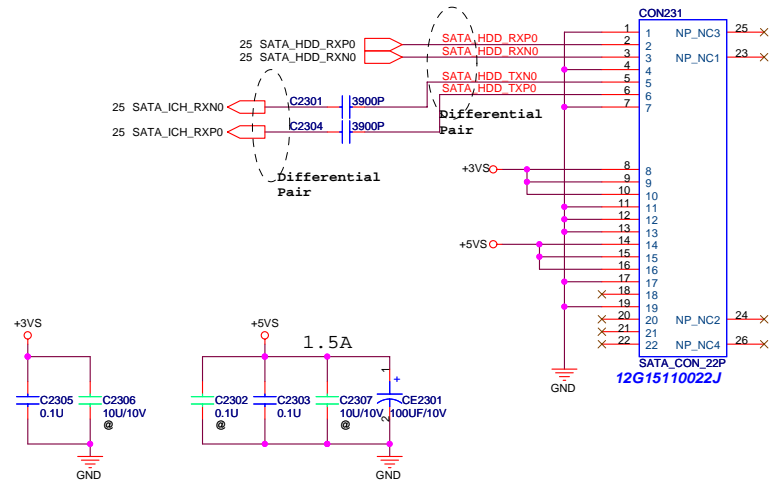




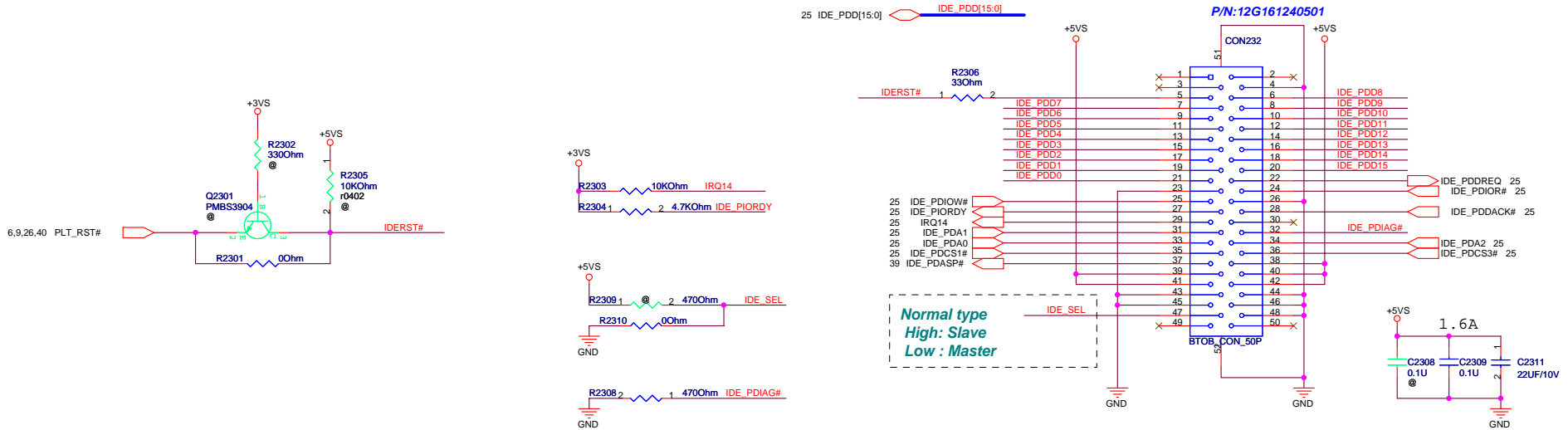
HERDER_2X25P

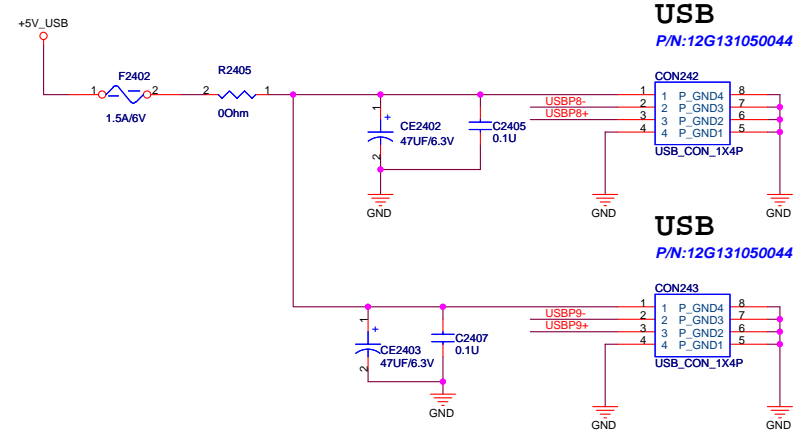
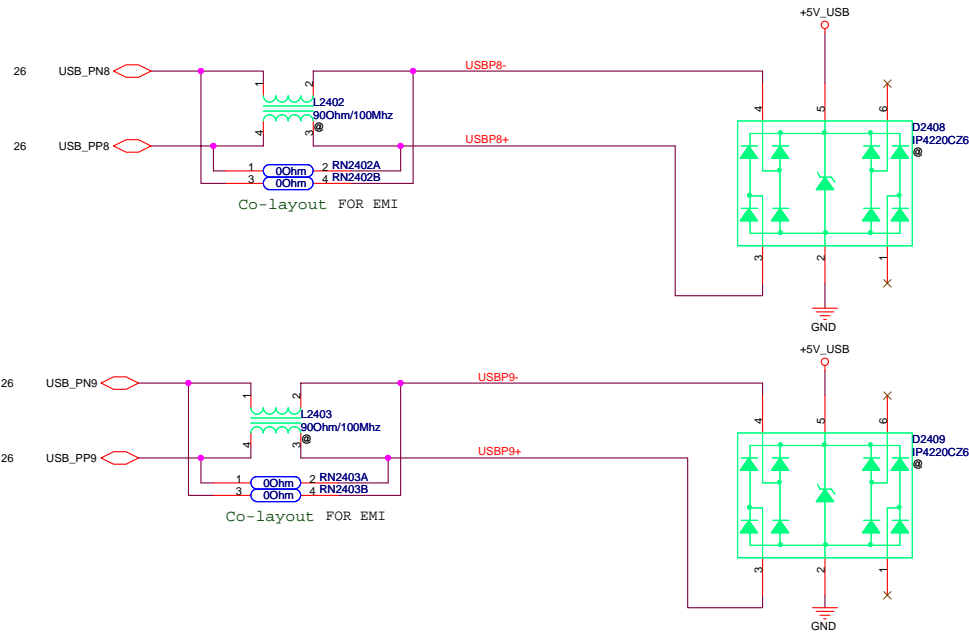
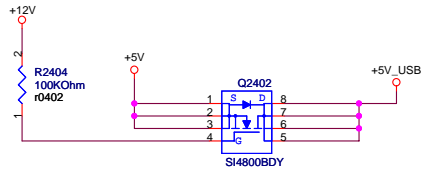


SATA HDD CON



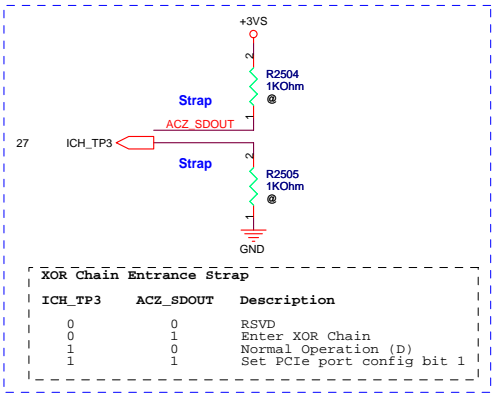
PATA CD-ROM CON





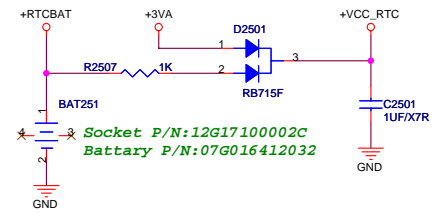
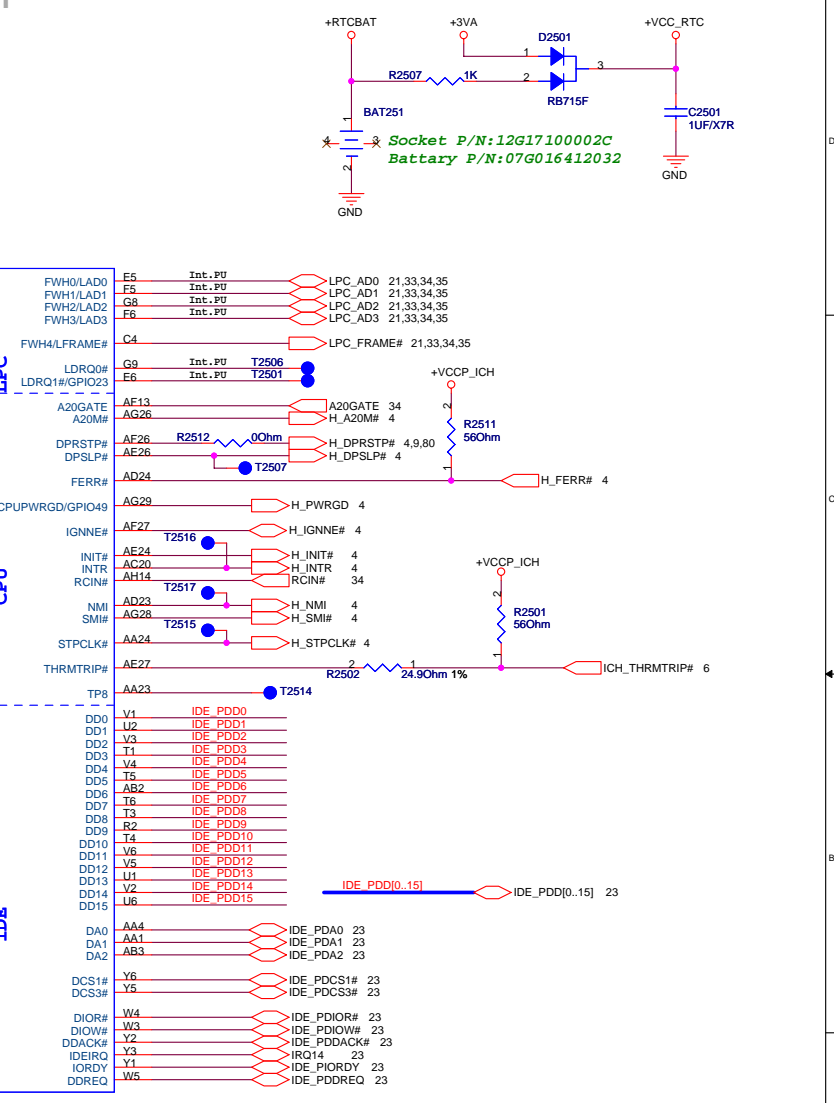
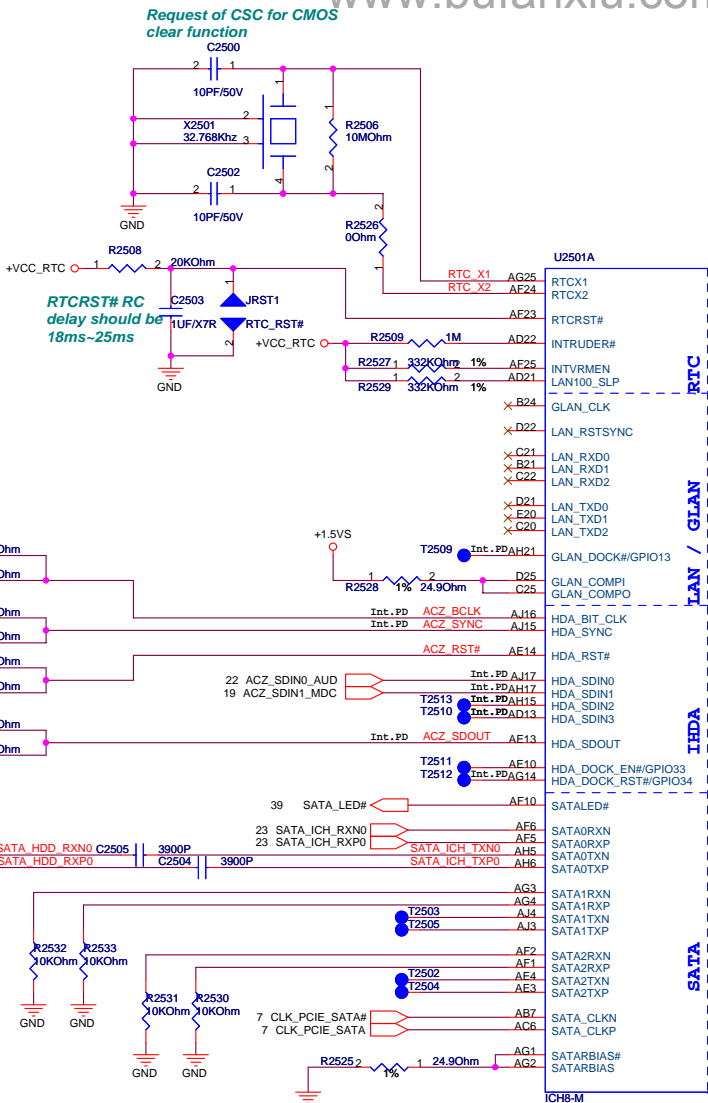
<Variant Name>

ASUS		Title : USB PORTS	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	24 of 94



XOR Chain Entrance Strap

ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (D)
1	1	Set PCIe port config bit 1



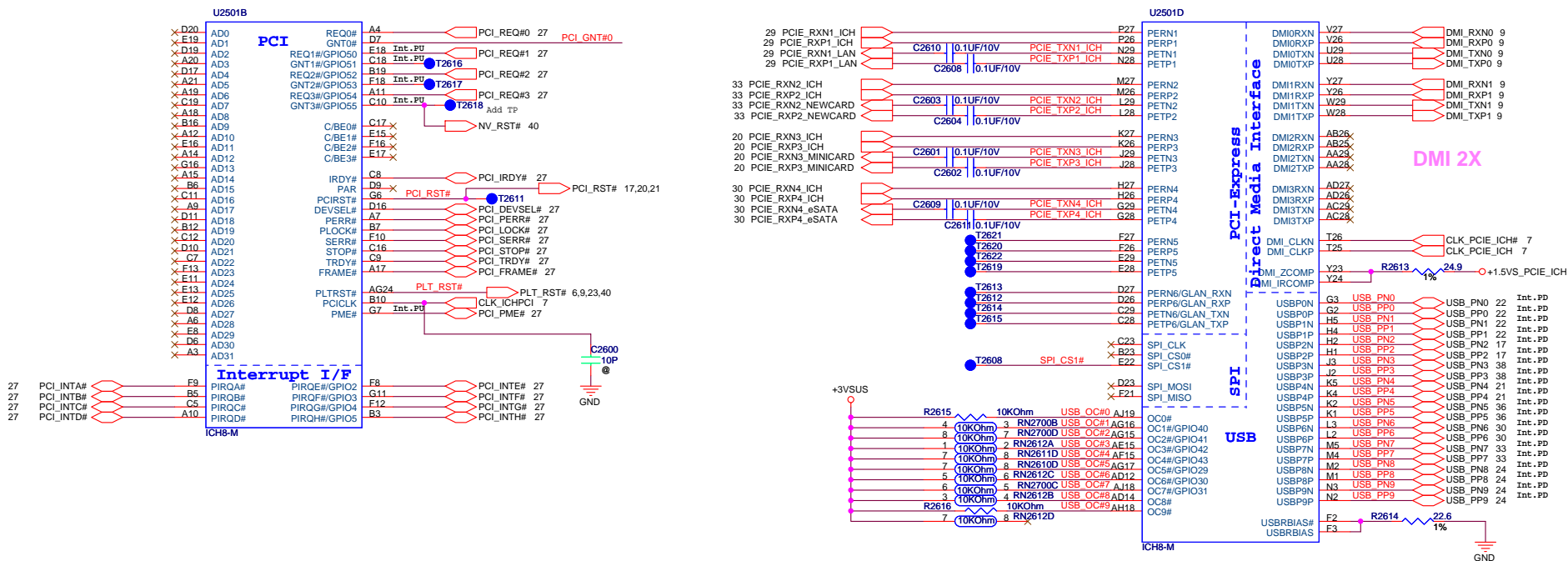
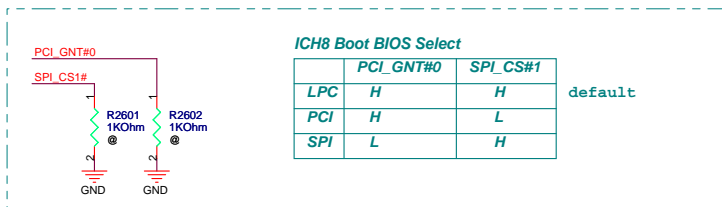
SATA HDD <=>



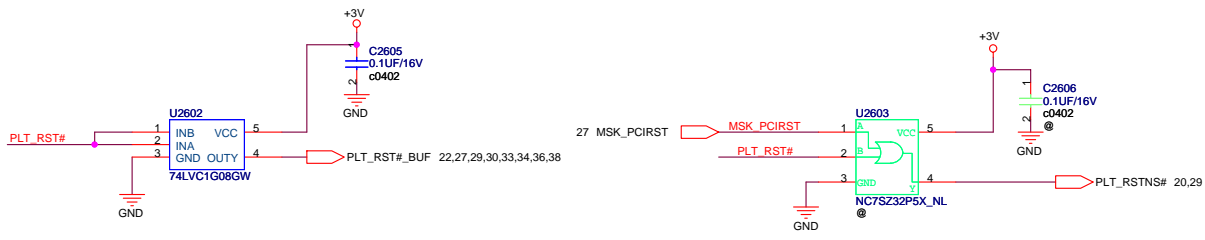
+3VA <=> +3VA 17,27,34,37,46,81,93
 +VCCP <=> +VCCP 4,5,6,7,8,9,11,12,28,37,85

<Variant Name>

ASUS		Title : ICH8-M (1)	
ASUSTek COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	25 of 94



USB 0	USB Conn.
USB 1	WWAN
USB 2	Camera
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	Card Reader
USB 6	USB Conn.
USB 7	Newcard
USB 8	USB Conn.
USB 9	USB Conn.



<Variant Name>

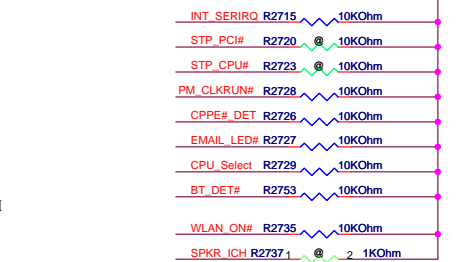
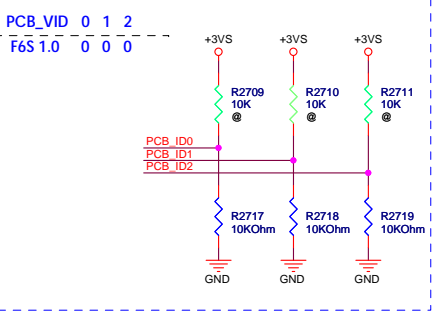
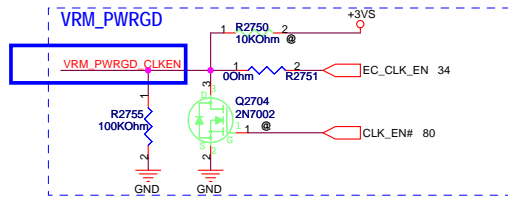
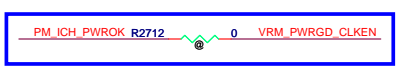
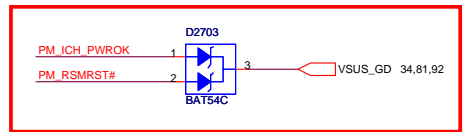
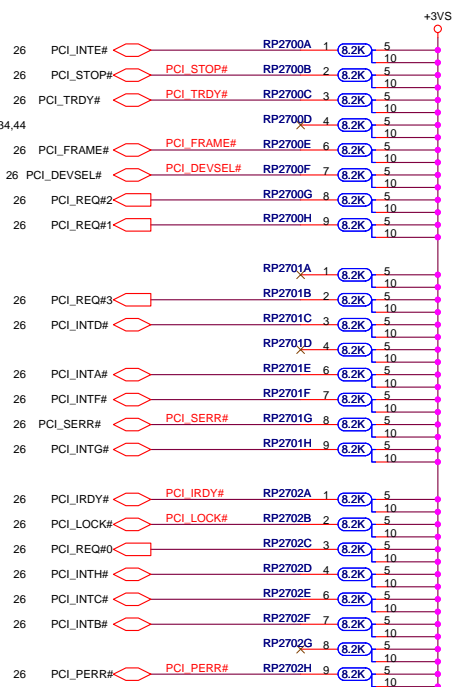
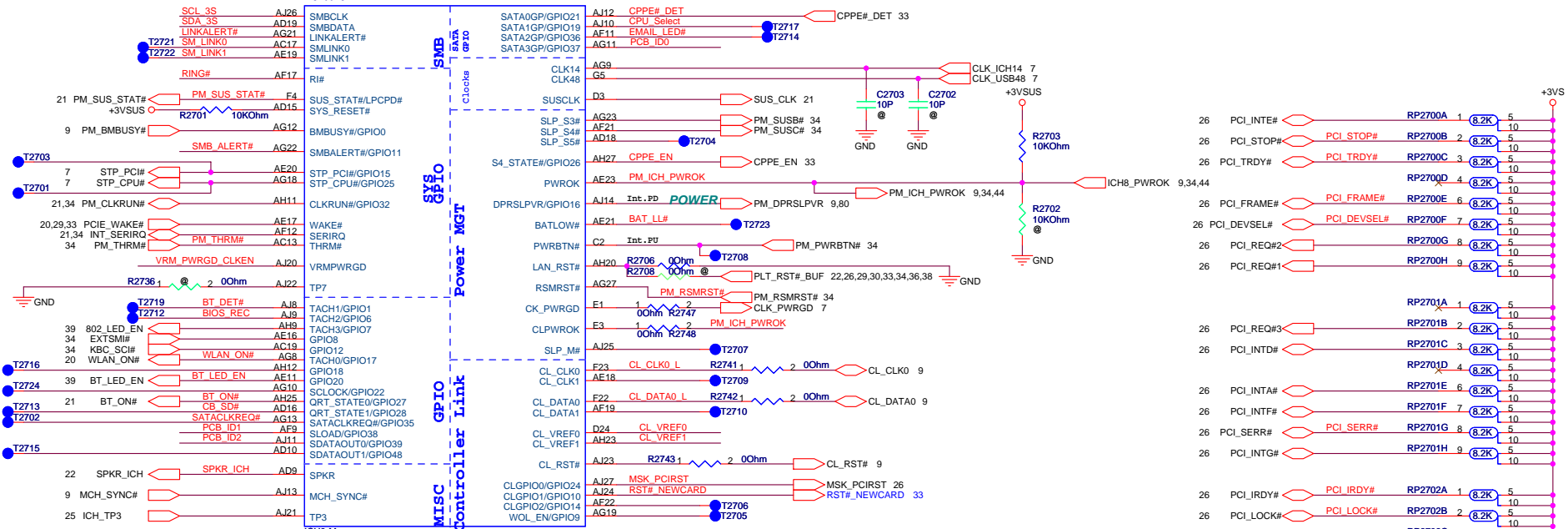
ASUS Title : ICH8-M (2)

ASUSTek COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F6S	1.1

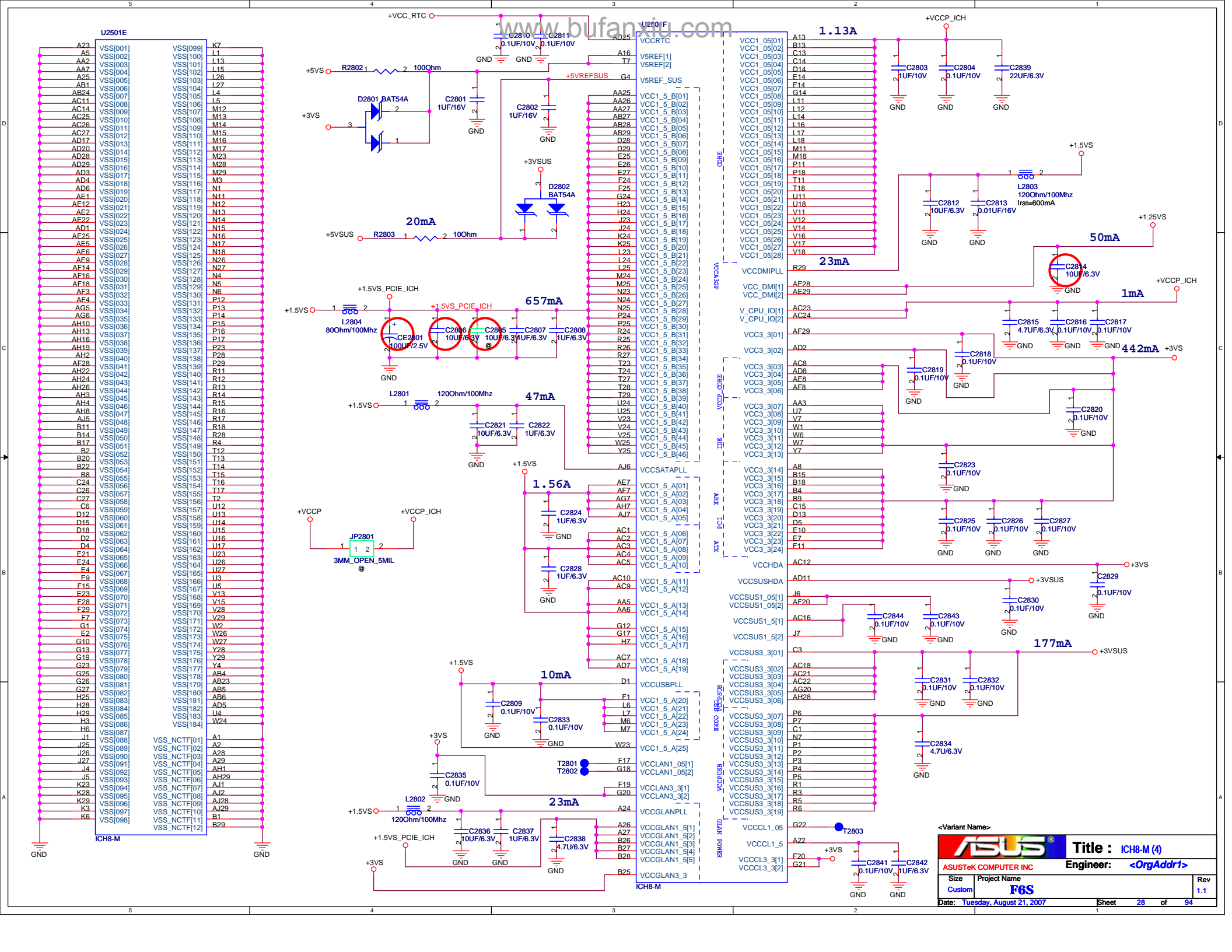
Date: Tuesday, August 21, 2007 Sheet 26 of 94

U2501C



<Variant Name>

ASUS		Title : ICH8-M (3)	
ASUSTek COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007	Sheet	27	of 94



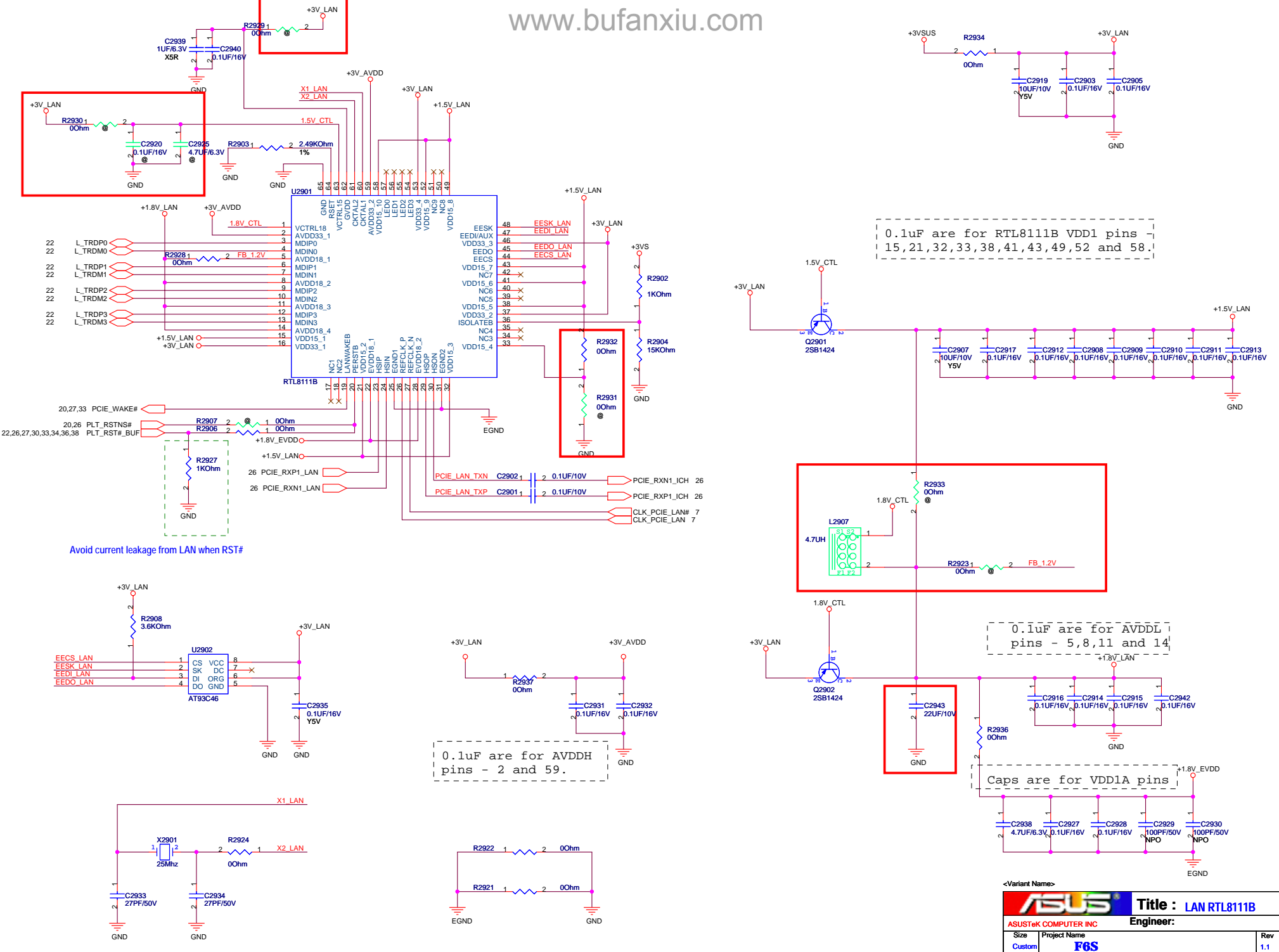
<Variant Name>

ASUS Title : ICH8-M (4)

ASUSTek COMPUTER INC Engineer: <OrgAddr>

Size	Project Name	Rev
Custom	F6S	1.1

Date: Tuesday, August 21, 2007 Sheet 28 of 94



Avoid current leakage from LAN when RST#

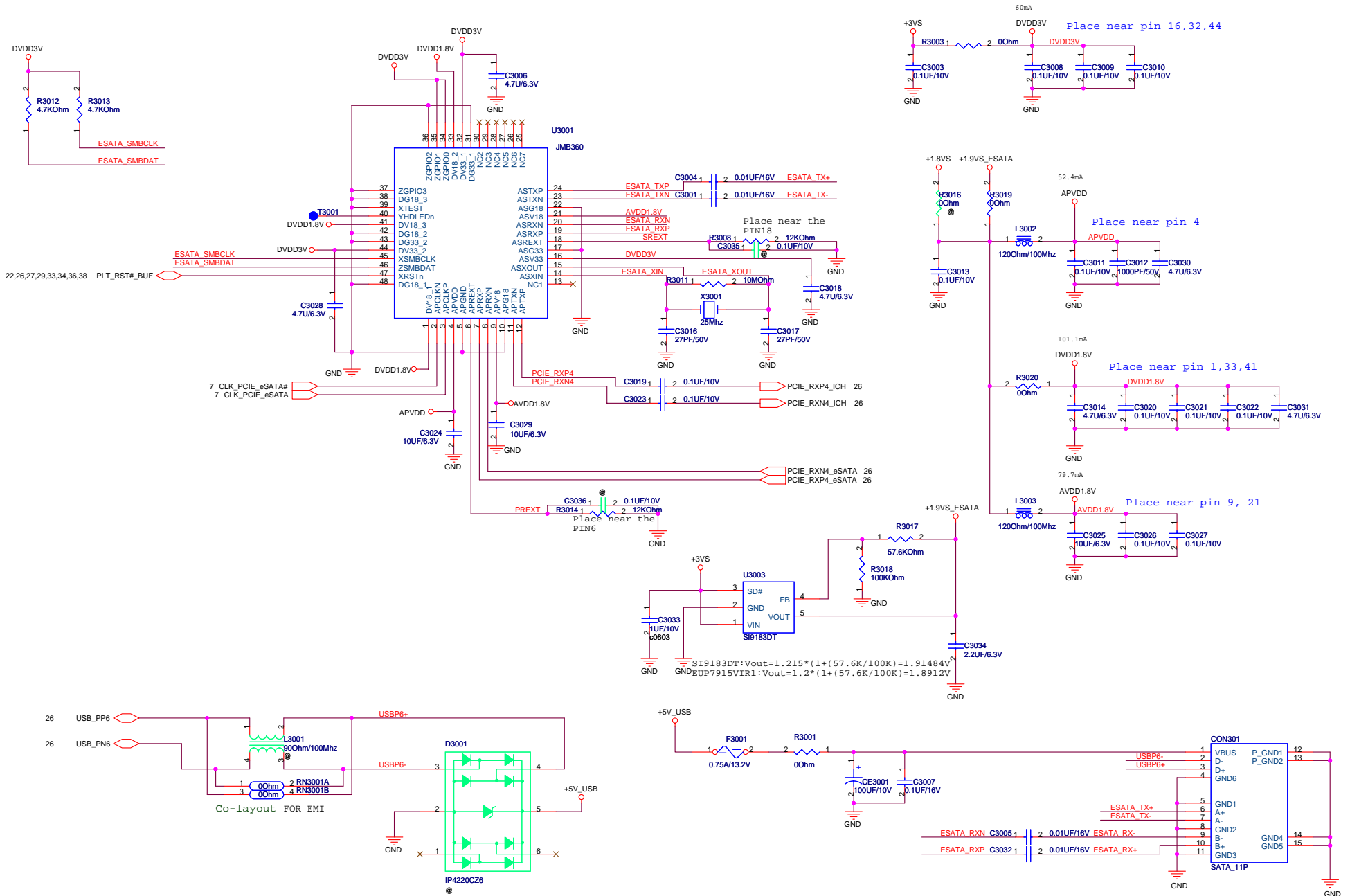
<Variant Name>

ASUS Title : LAN RTL8111B

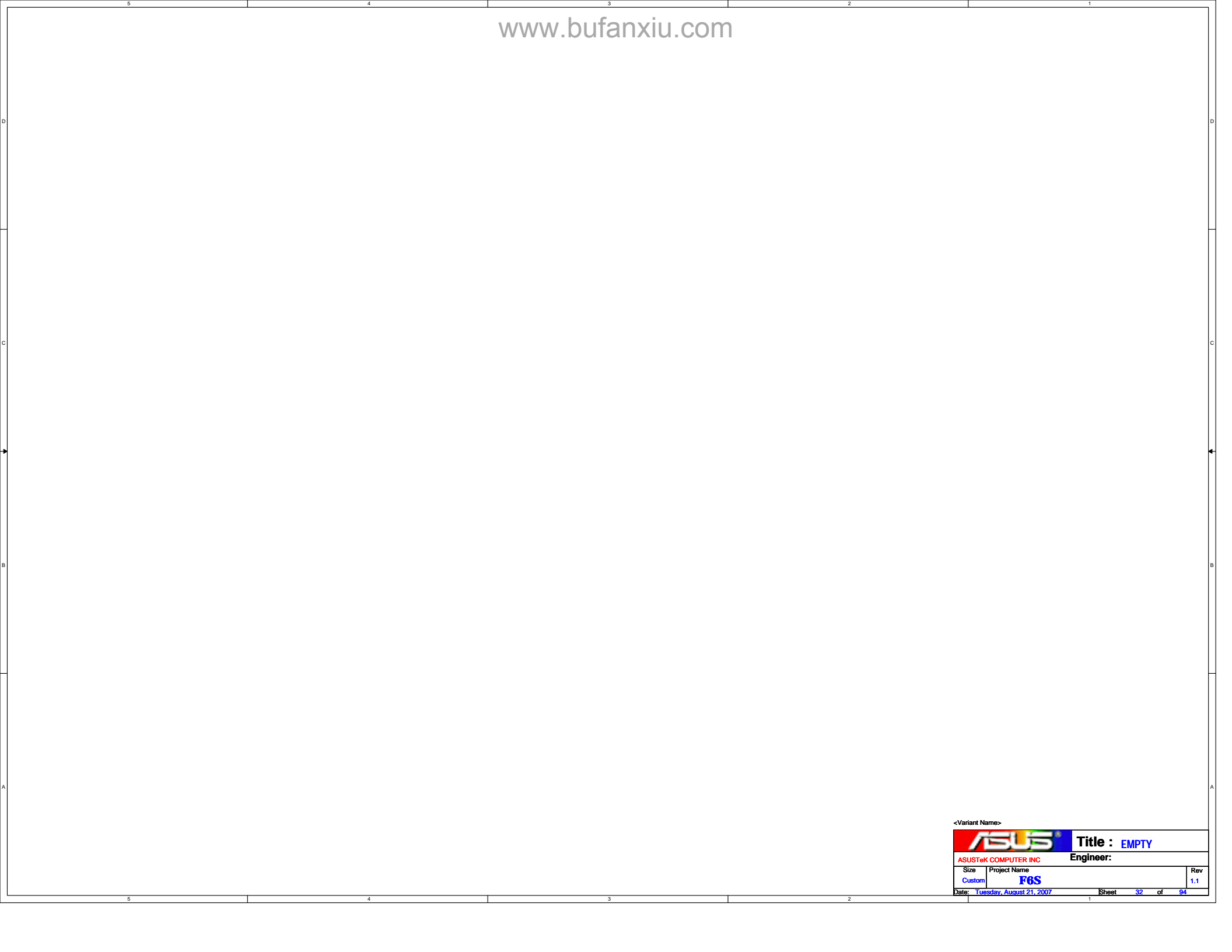
ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F6S	1.1


Date: Tuesday, August 21, 2007 Sheet 29 of 94



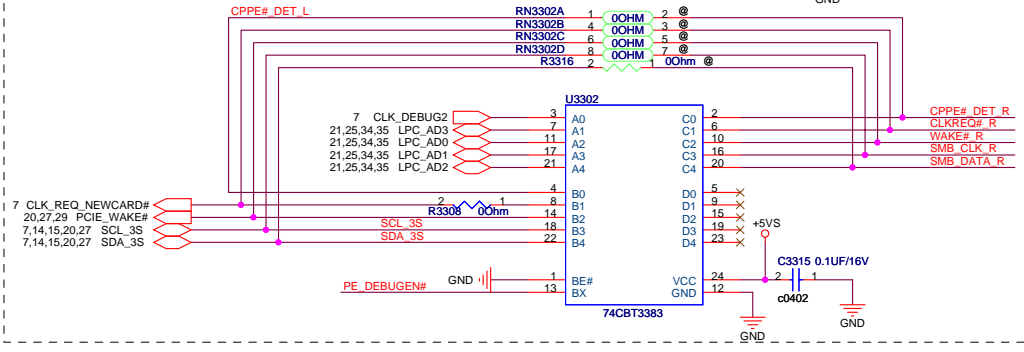
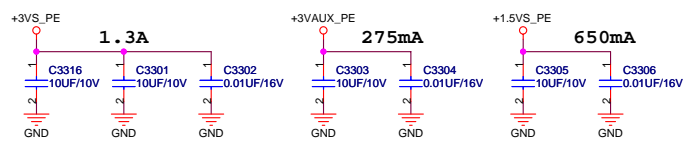
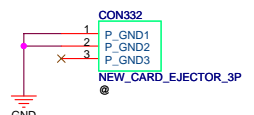
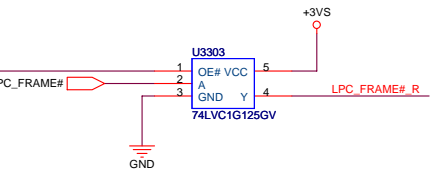
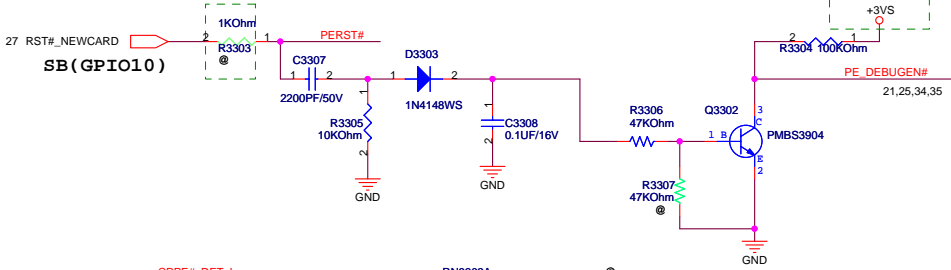
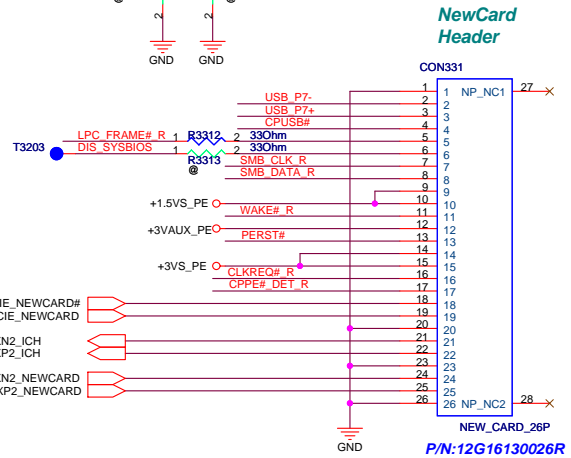
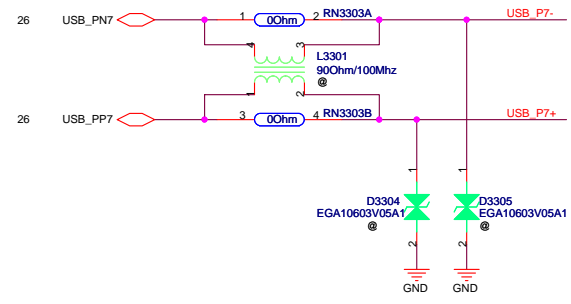
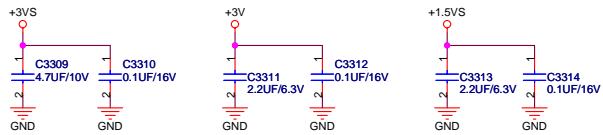
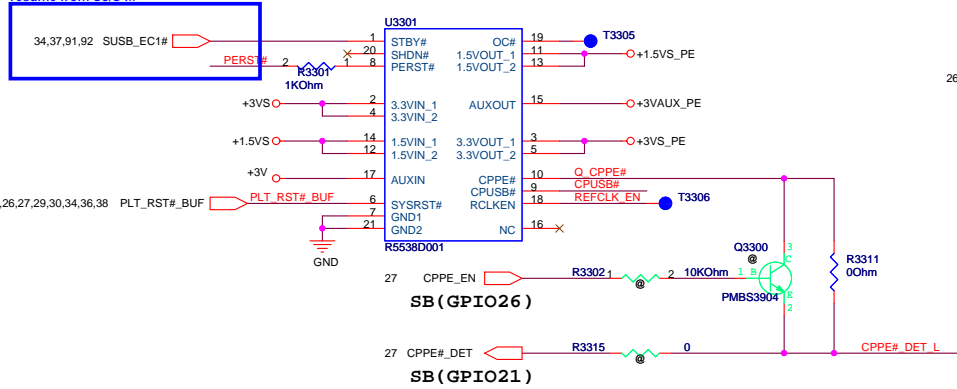
		Title : EMPTY	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	FGS		1.1
Date: Tuesday, August 21, 2007		Sheet	31 of 94

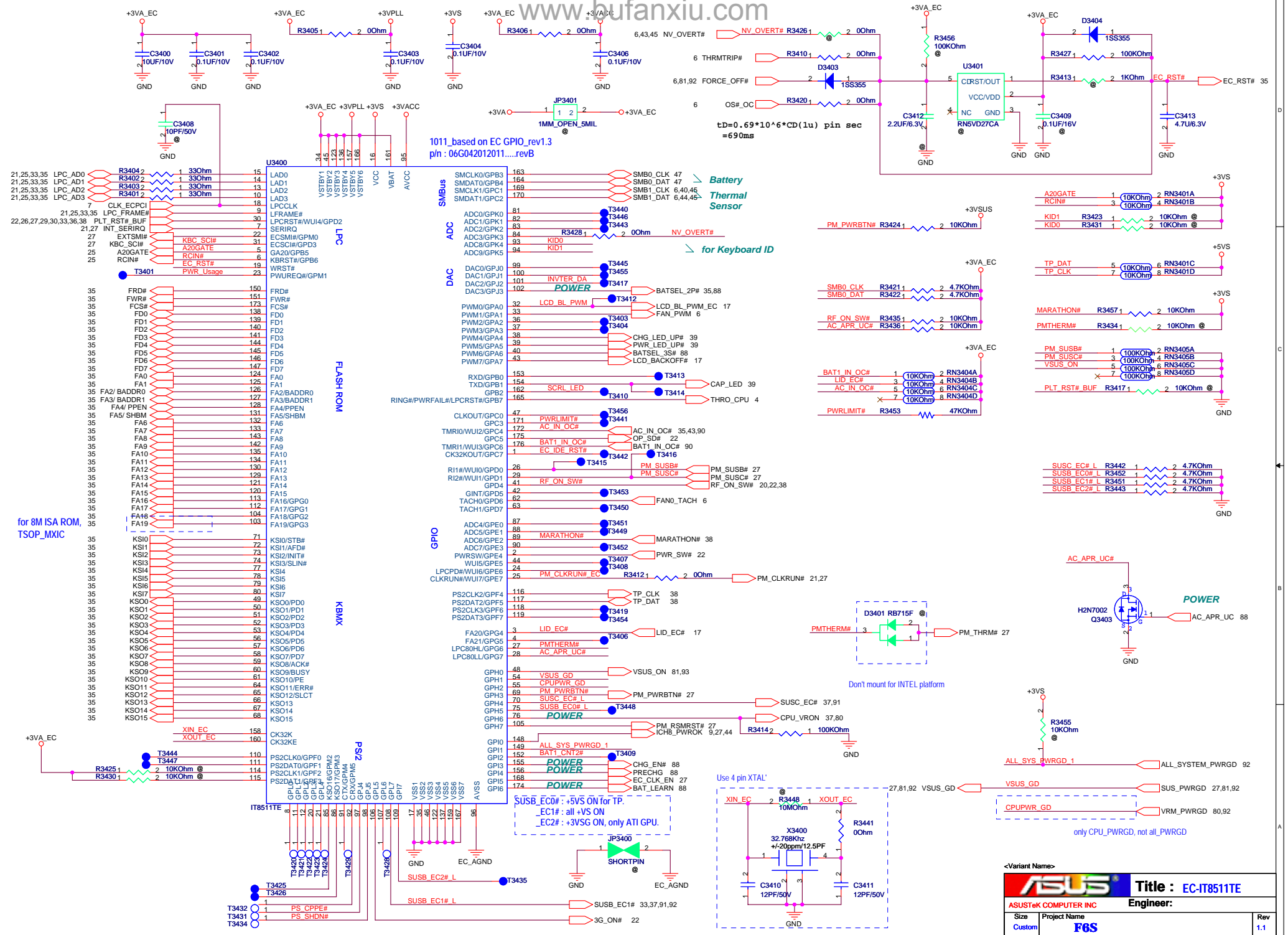


<Variant Name>

		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F6S		1.1
Date:	Tuesday, August 21, 2007	Sheet	32 of 94

New EC pin to avoid the re-recognize when resume from S3/S4.





<Variant Name>

ASUS Title : EC-IT8511TE

ASUSTek COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F6S	1.1

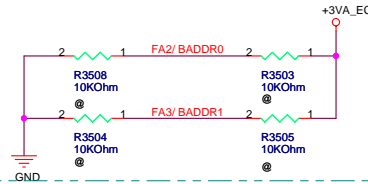
Date: Tuesday, August 21, 2007 Sheet 34 of 94

ISA ROM_TSOP

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

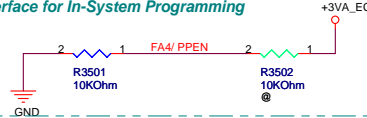
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

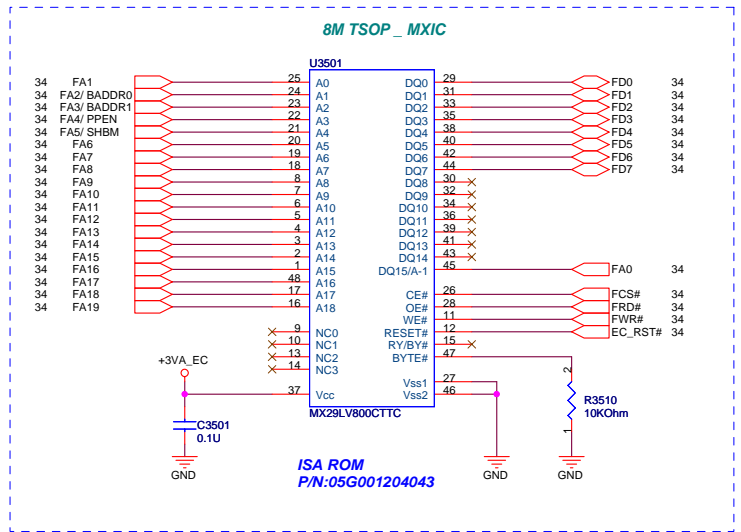
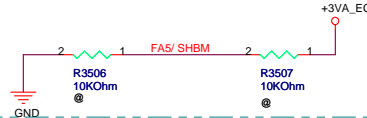
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



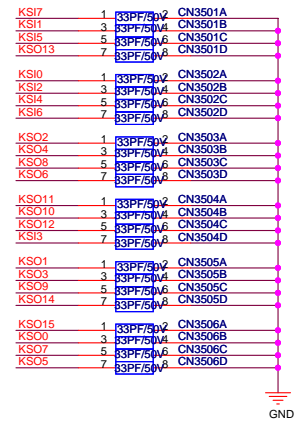
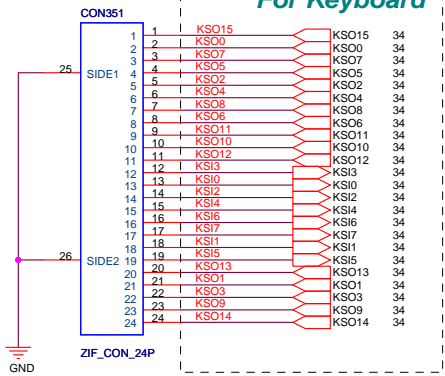
FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

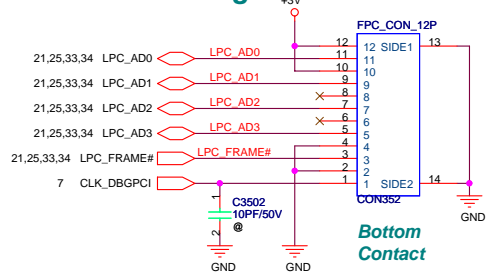


P/N:12G182402404

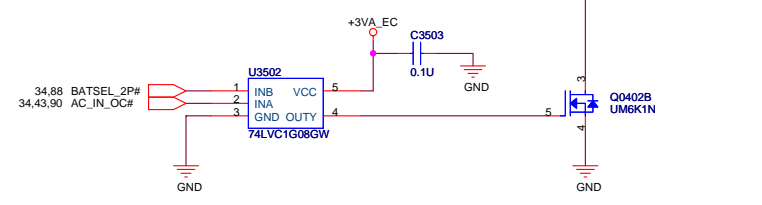
For Keyboard

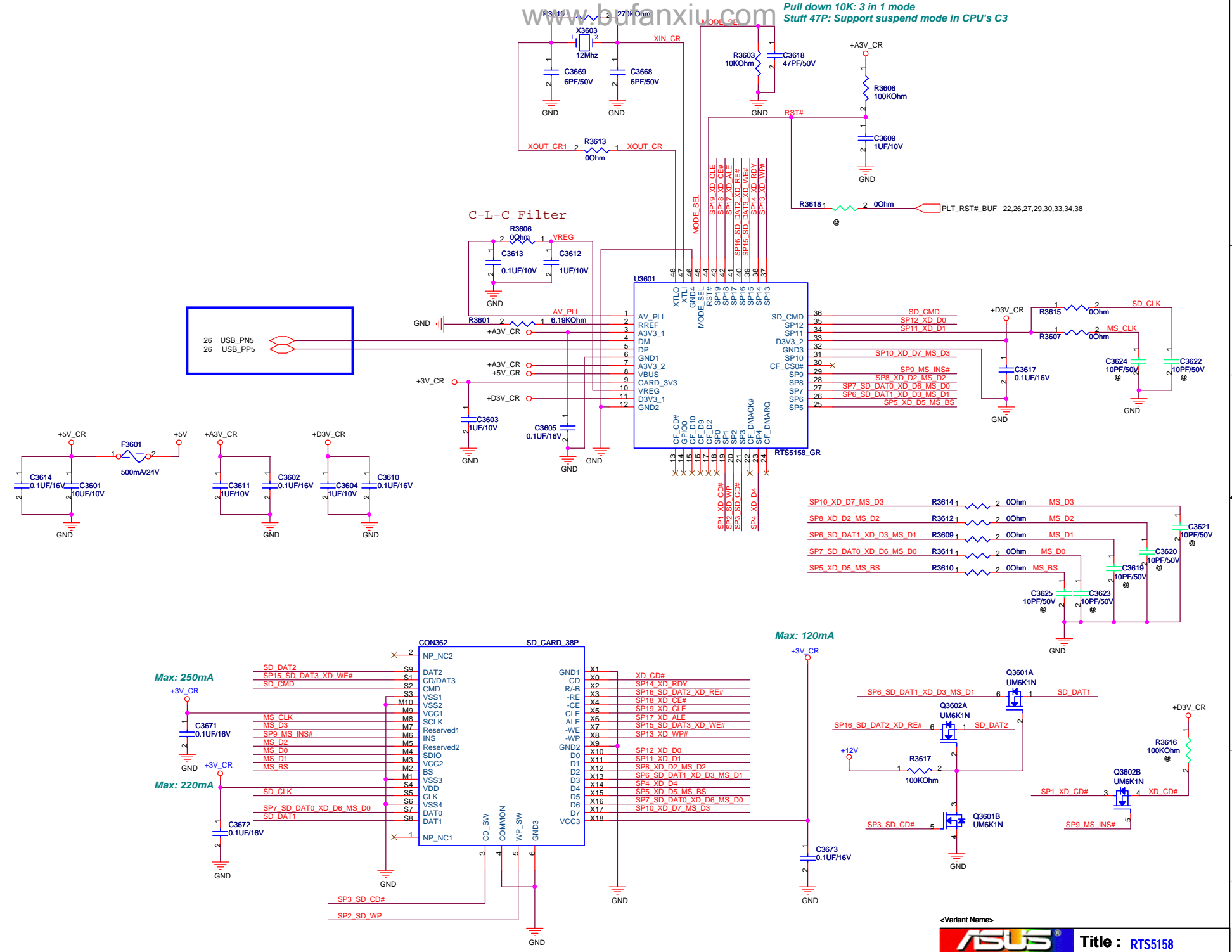


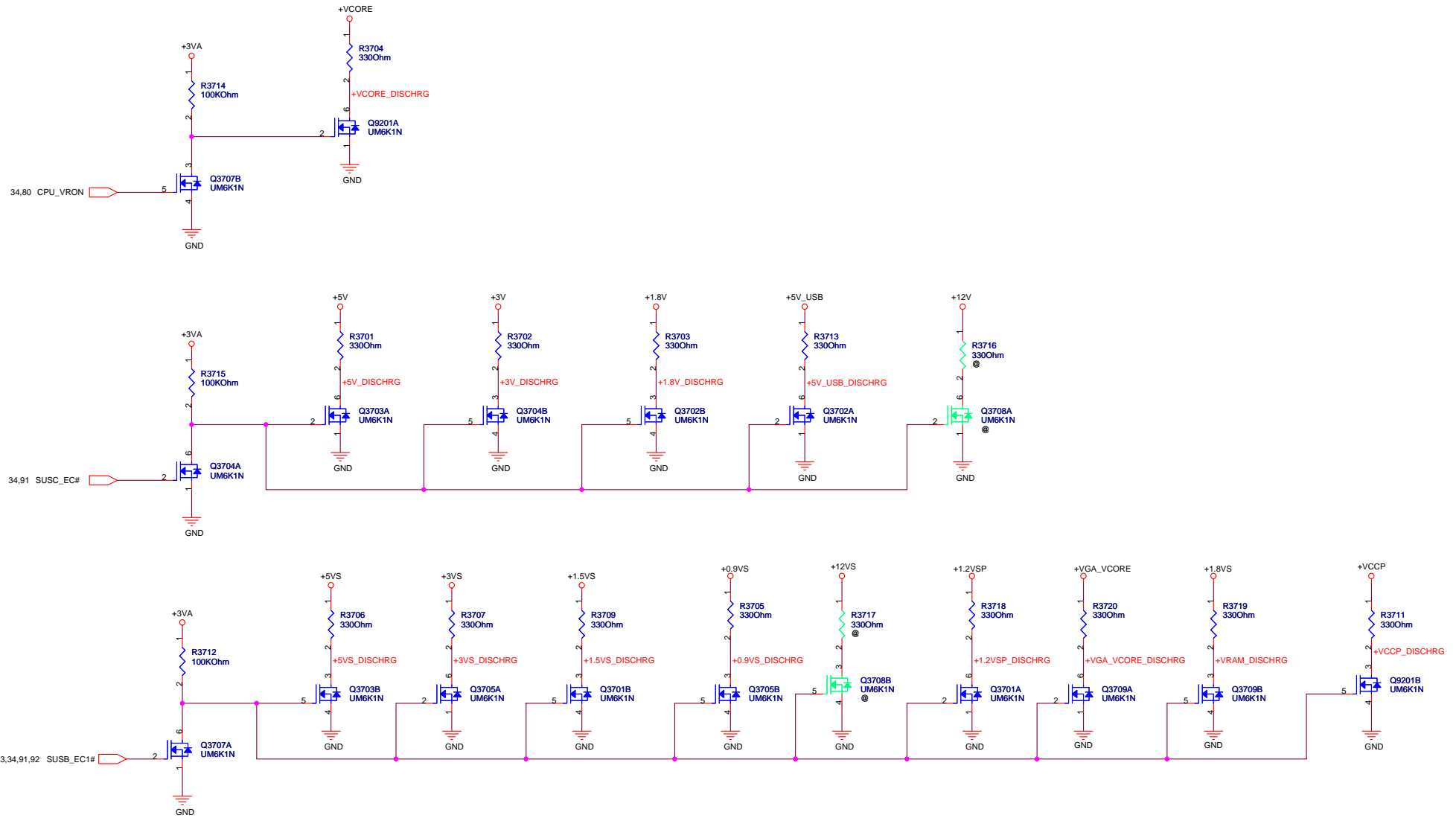
For Debug



PWRLMT Circuit: For Battery IP



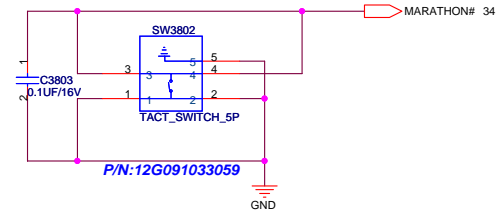




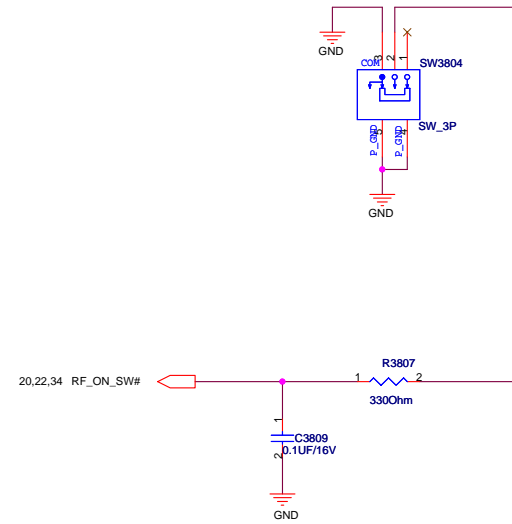
<Variant Name>

		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F6S	1.1	
Date: Tuesday, August 21, 2007		Sheet 37 of 94	

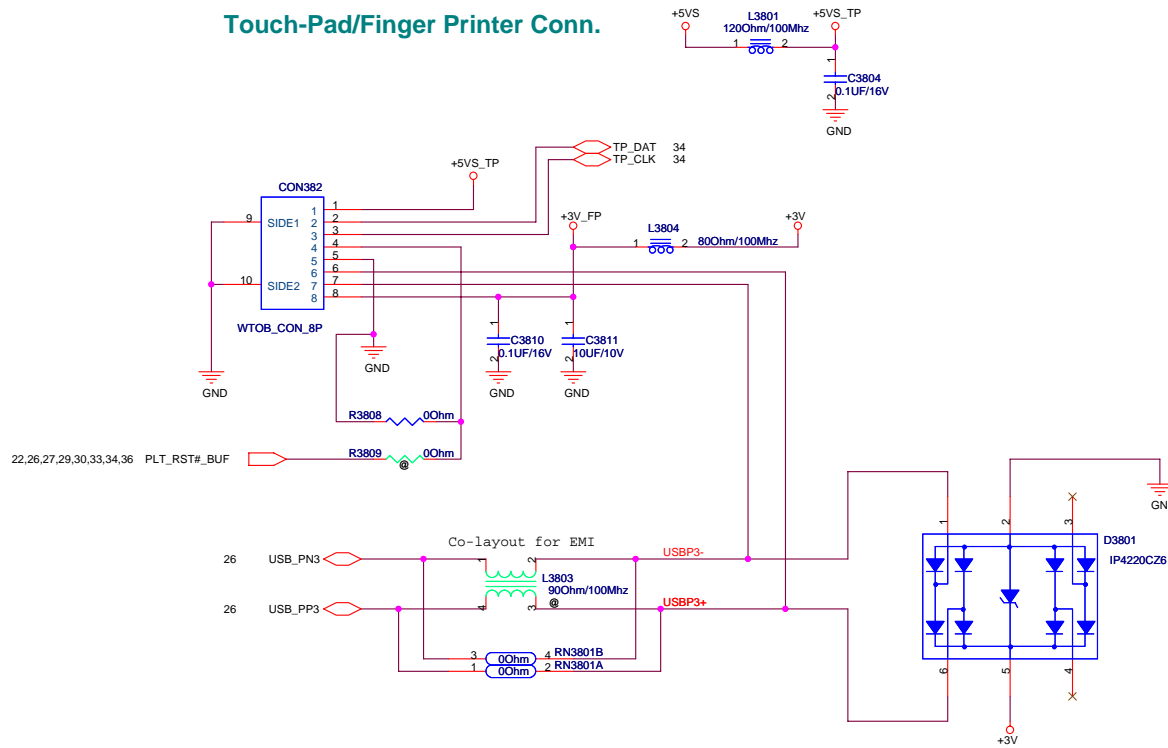
MARATHON#



BT/WLAN SW



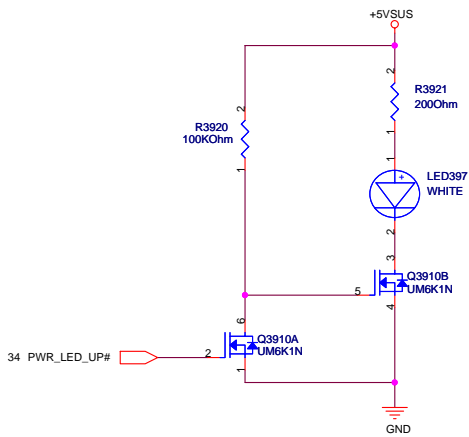
Touch-Pad/Finger Printer Conn.



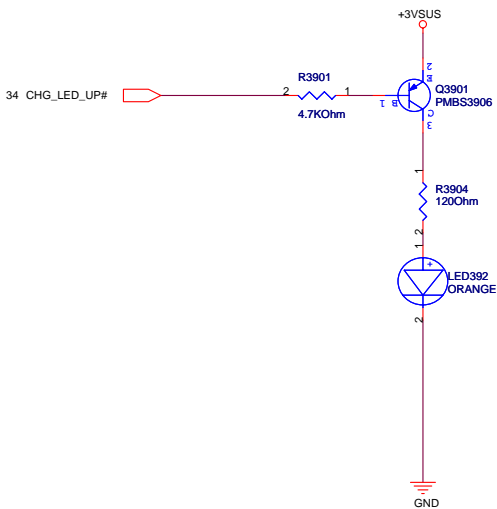
<Variant Name>

ASUS		Title : KEY & LED
ASUSTeK COMPUTER INC		Engineer:
Size Custom	Project Name F6S	Rev 1.1
Date: Tuesday, August 21, 2007	Sheet 38	of 94

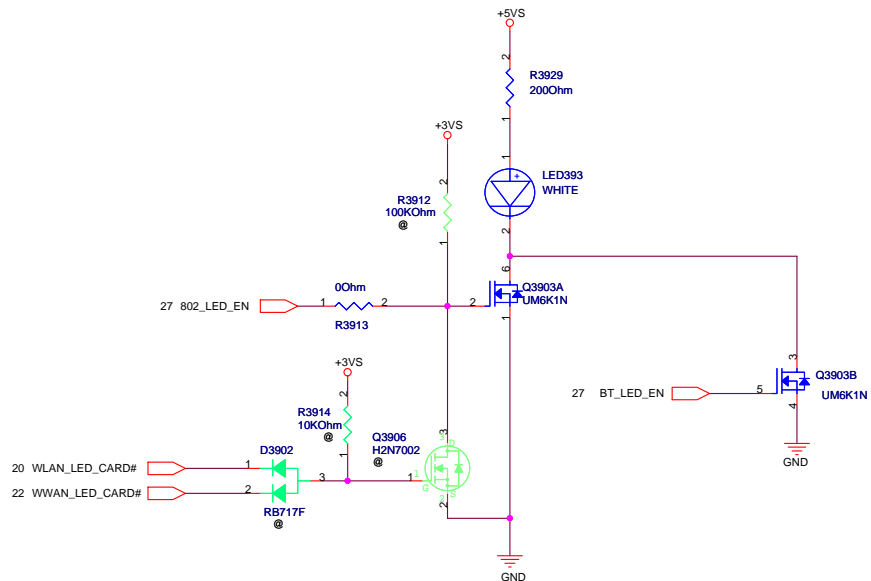
PWR LED



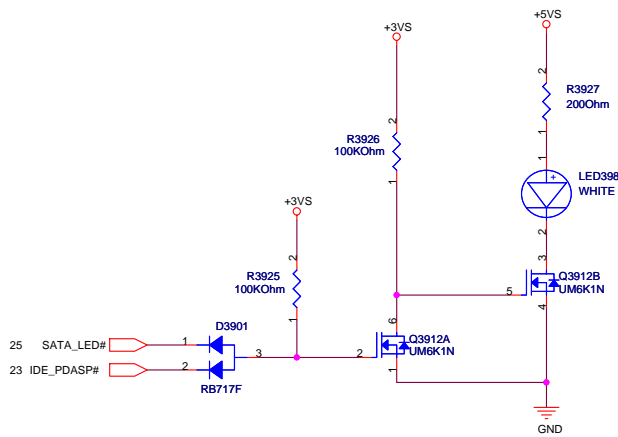
BATTERY LED



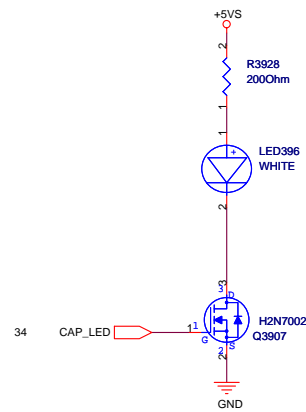
WireLess/BT LED



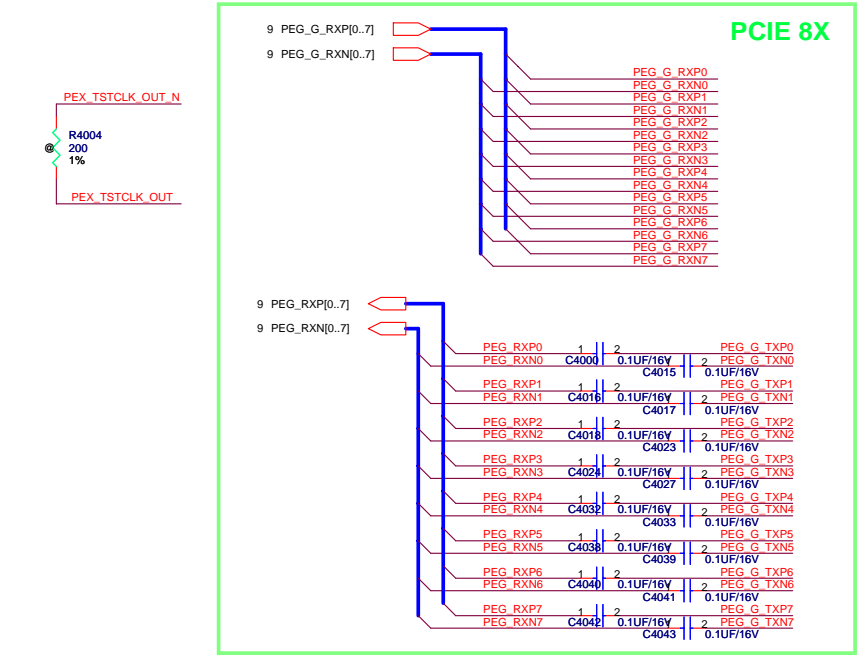
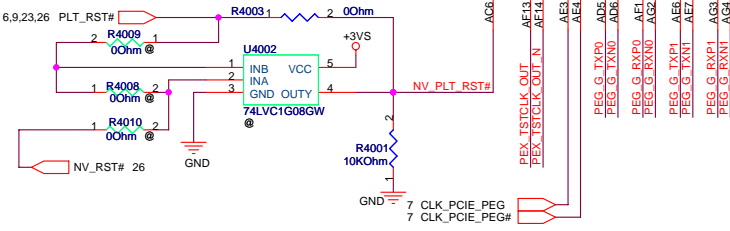
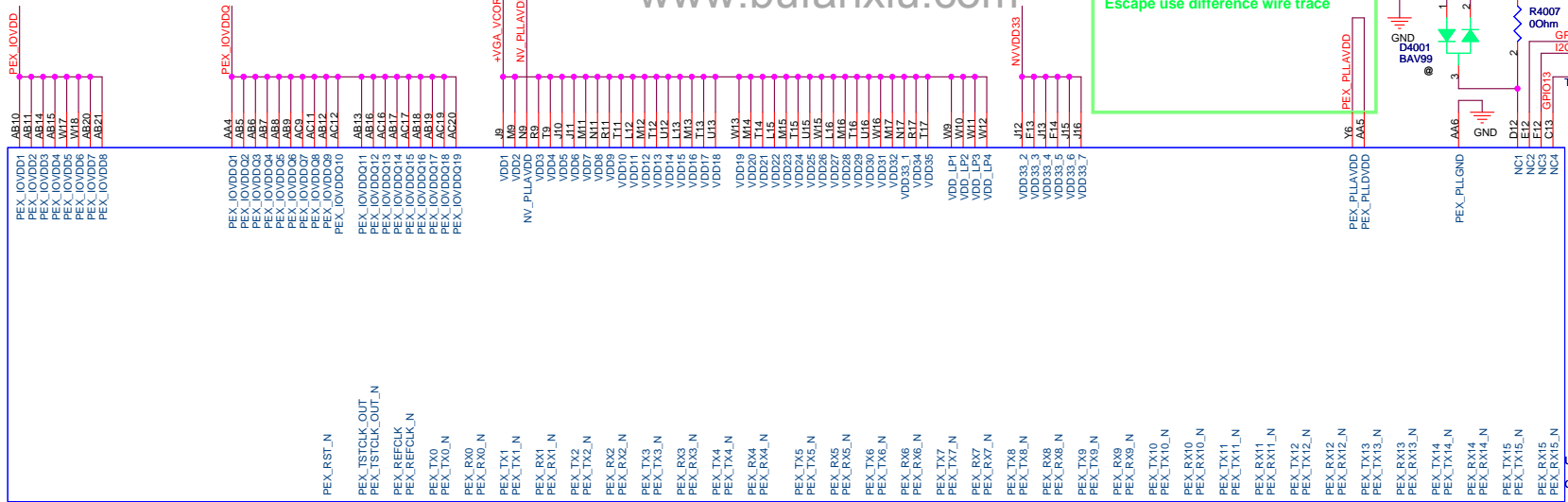
SATA/IDE LED



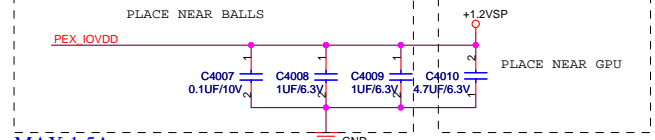
Cap. Lock



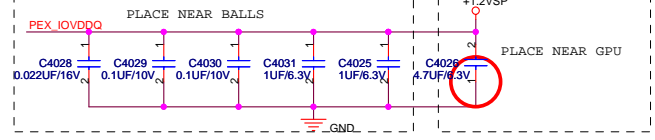
Escape use difference wire trace



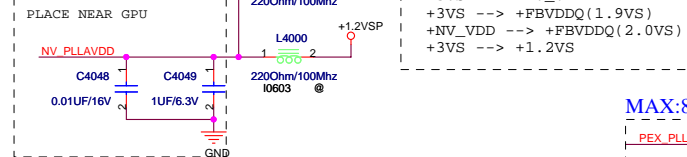
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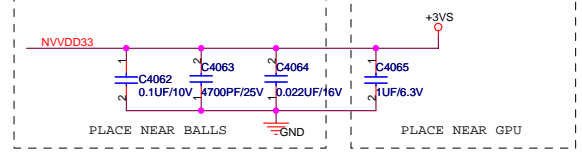
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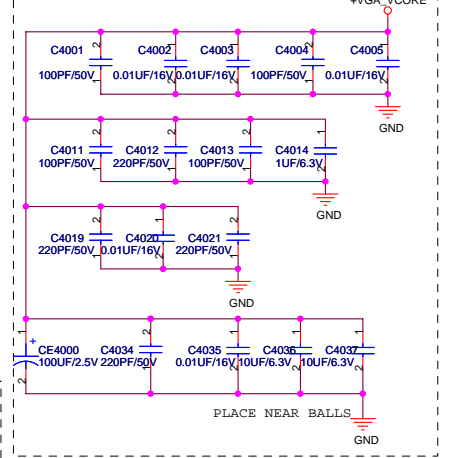
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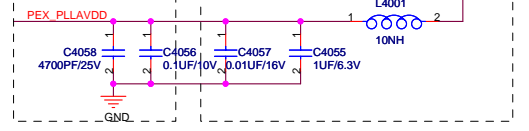
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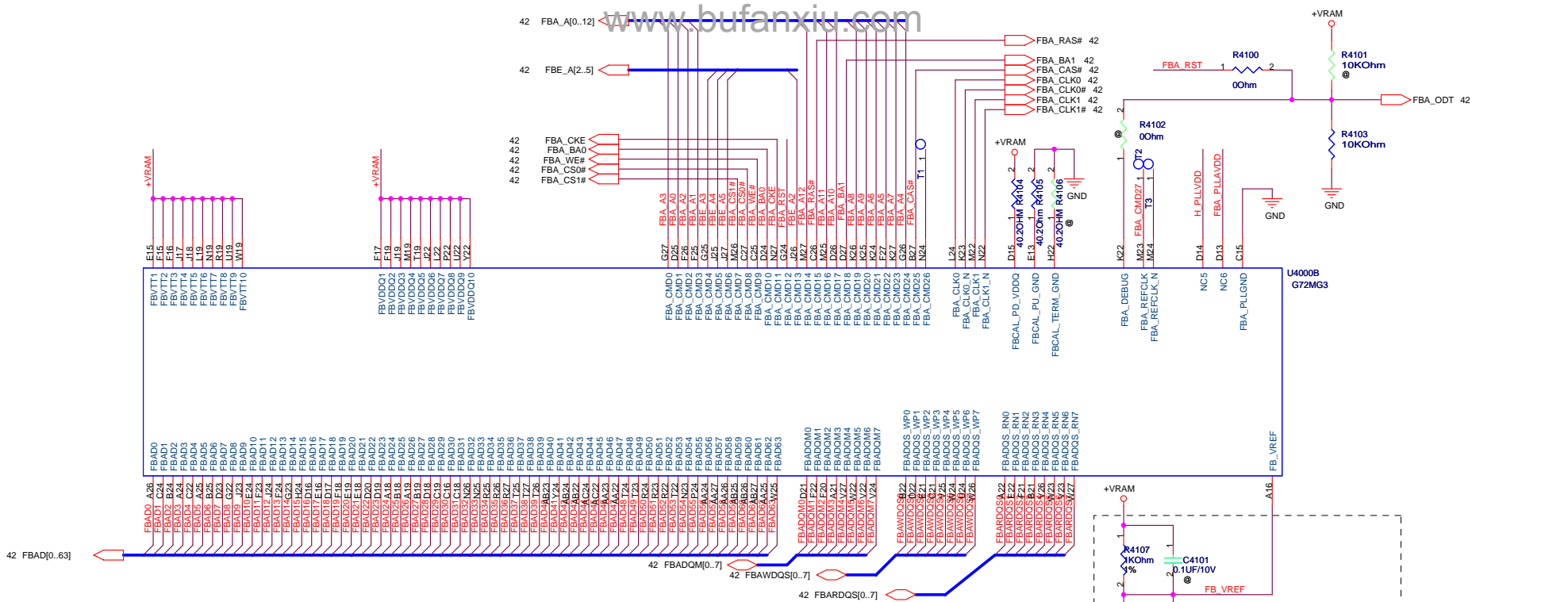


NB8M-SE : 1.15V(7.82A)



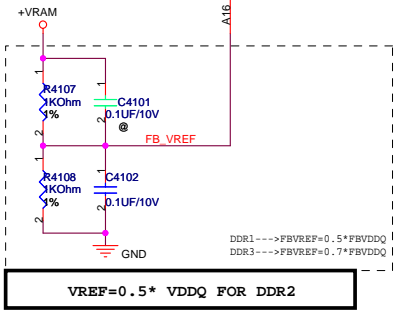
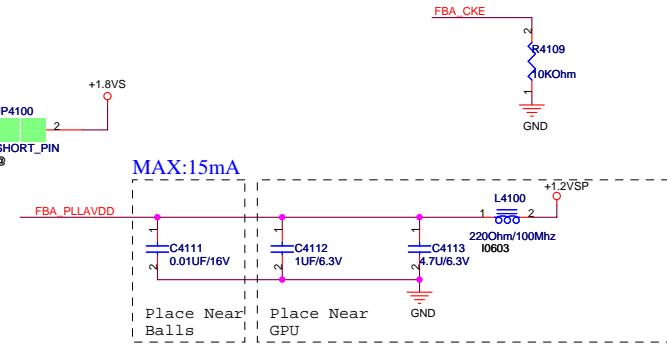
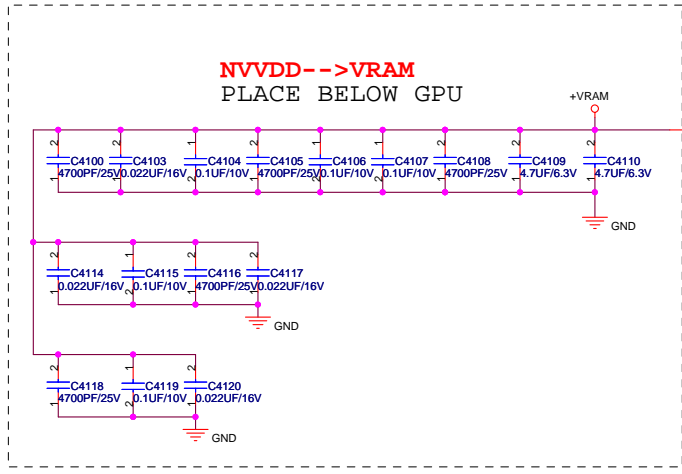
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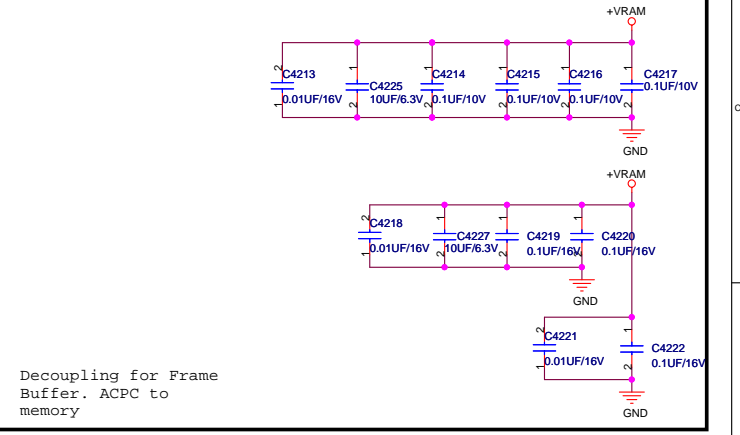
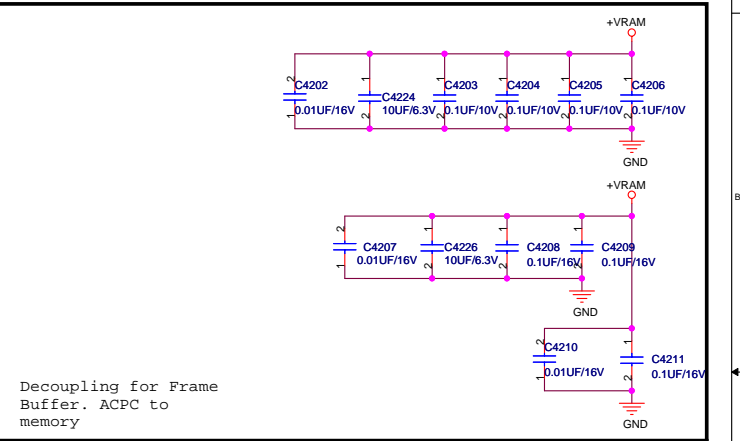
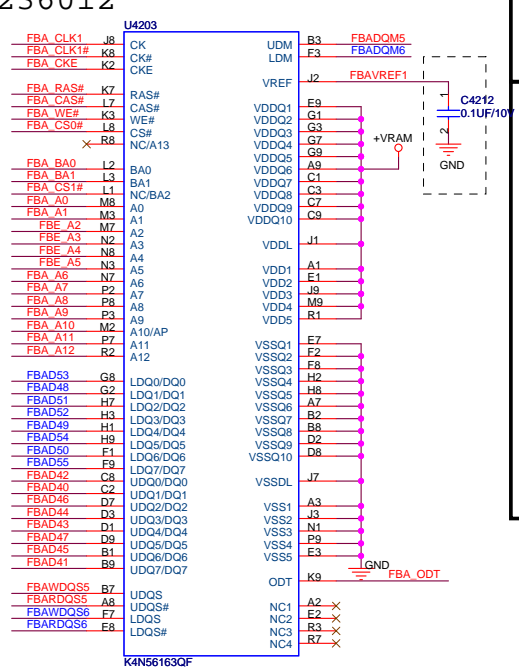
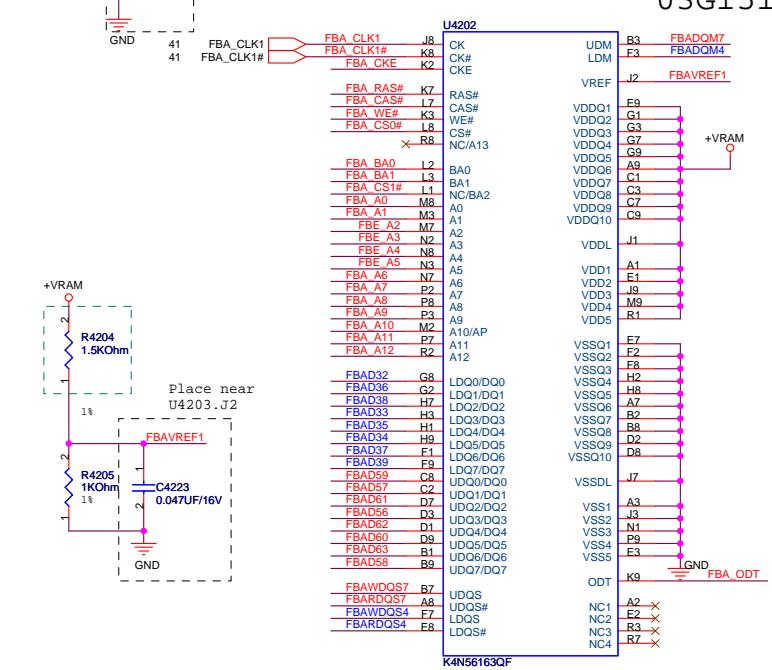
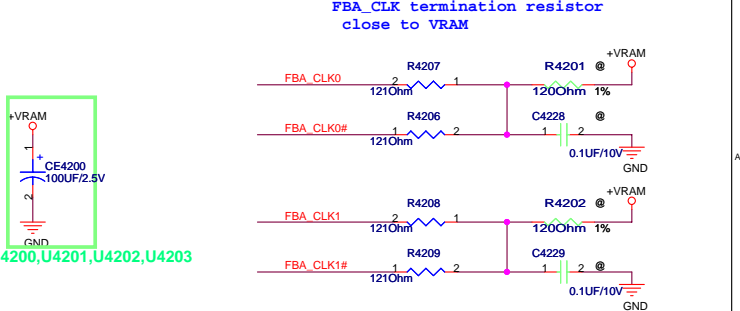
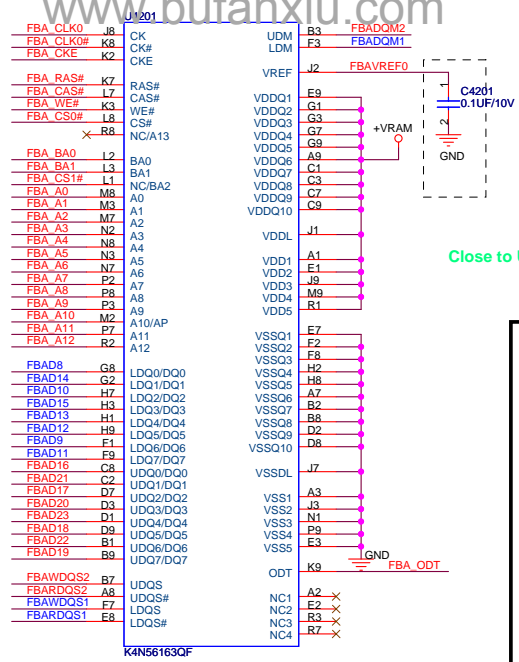
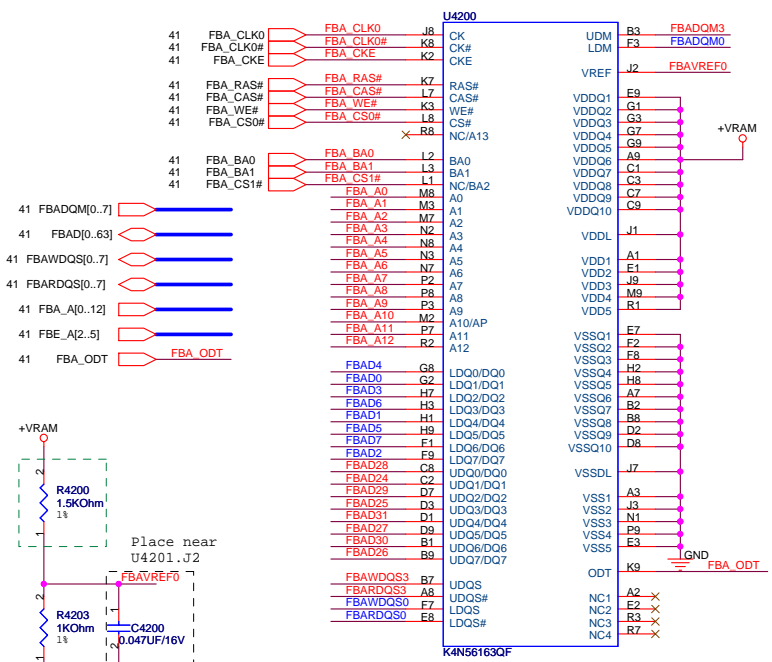




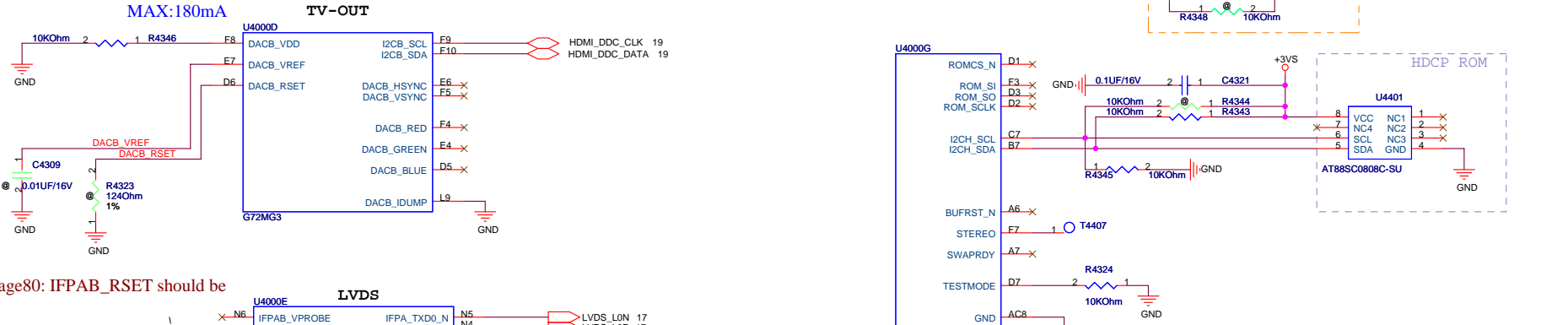
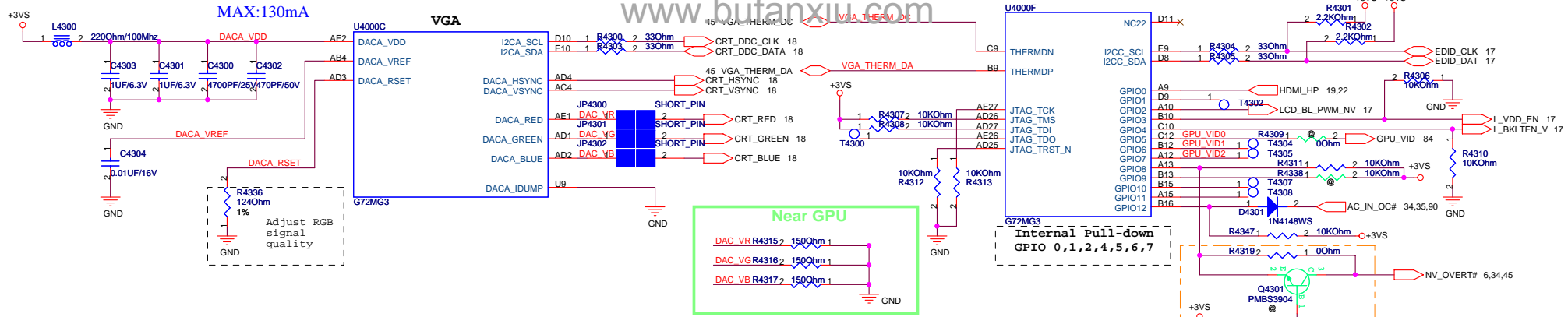
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G72M:MAX:2.075A
G72M-V:MAX:1A

GDDR2 16x16 FBVDDQ 1.8V 84PIN

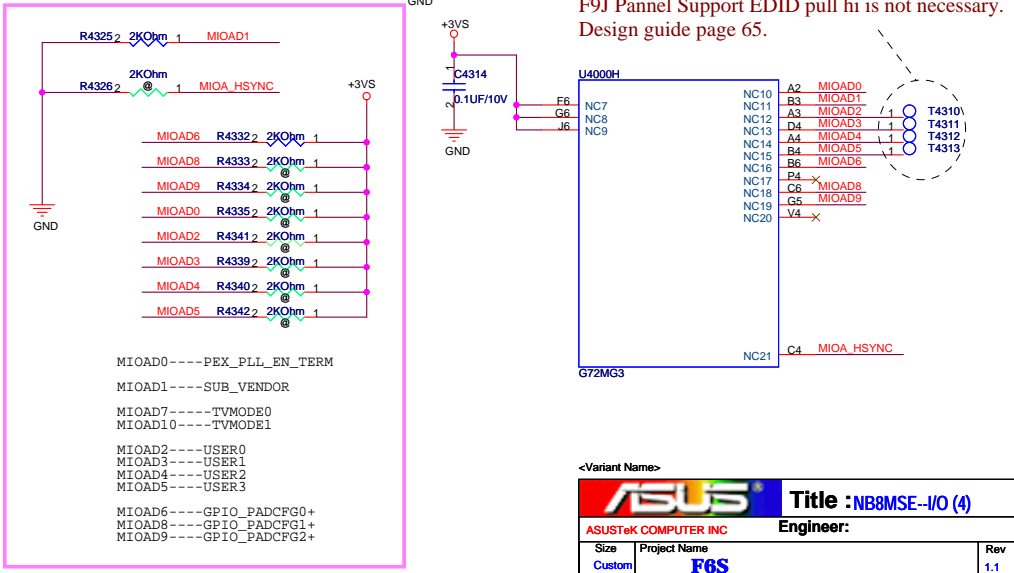
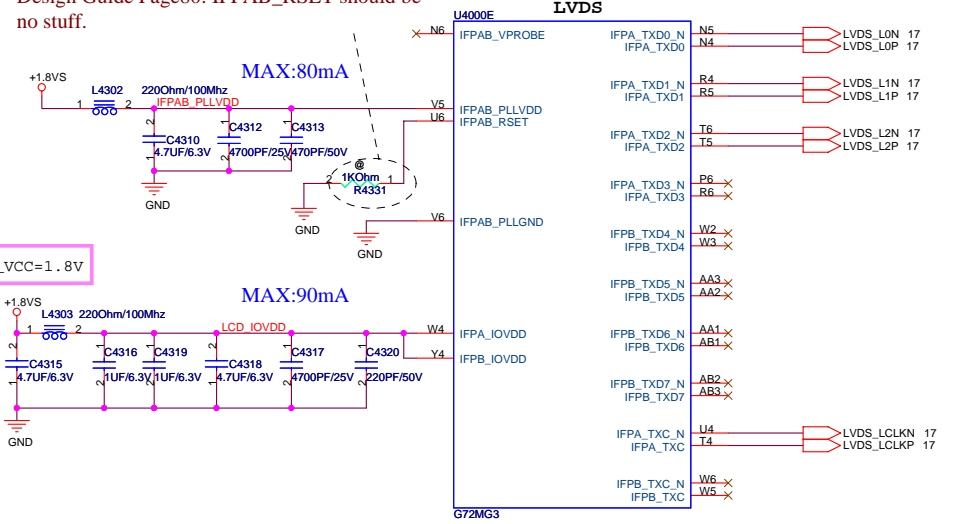




03G151236012



Design Guide Page80: IFPAB_RSET should be no stuff.



F9J Panel Support EDID pull hi is not necessary. Design guide page 65.

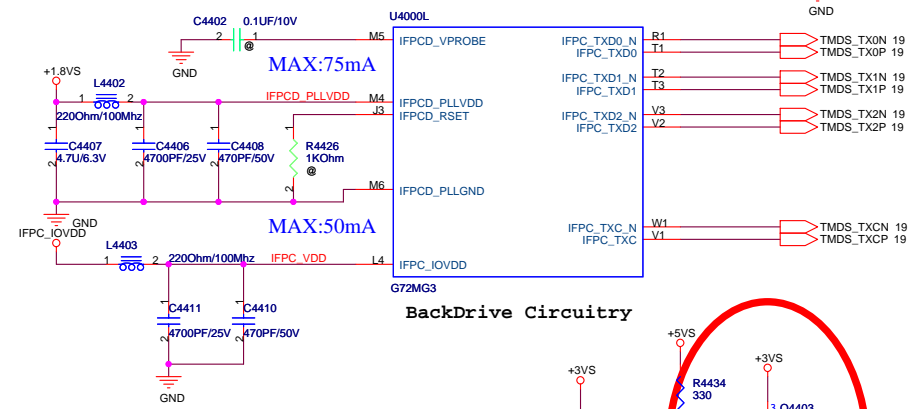
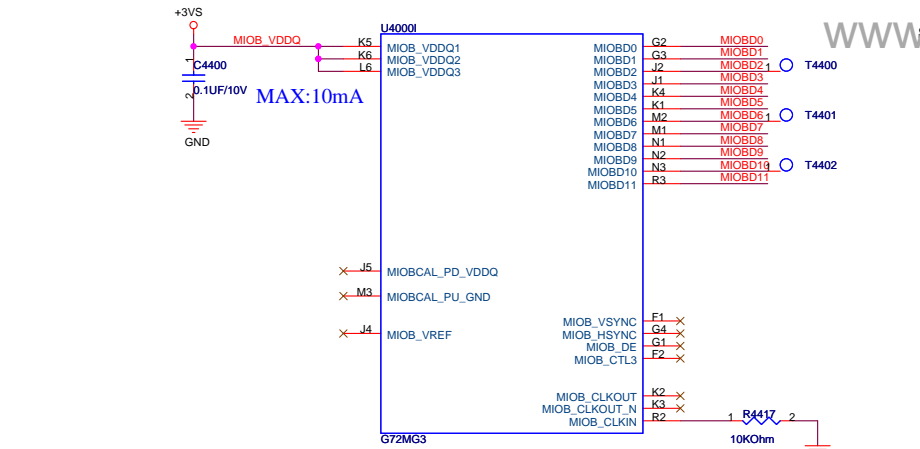
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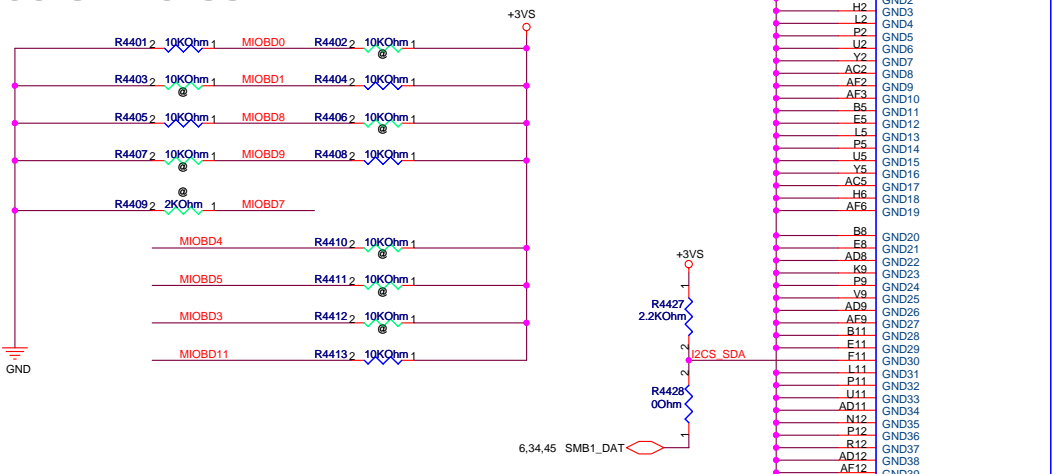
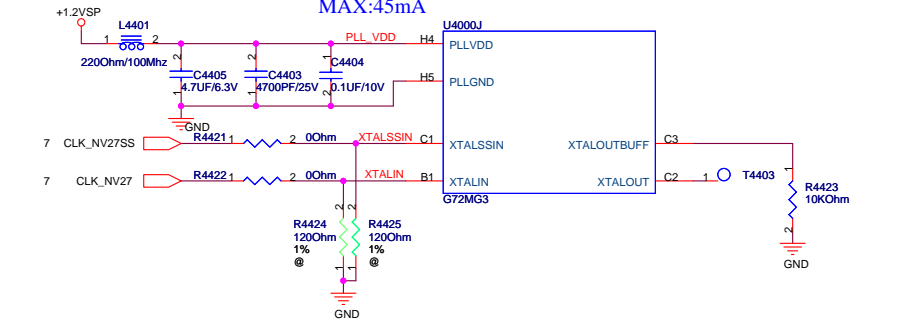
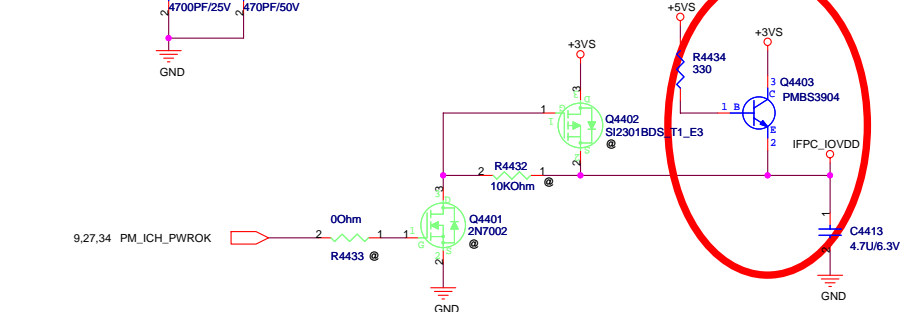
ASUSTek COMPUTER INC **Engineer:**

Size	Project Name	Rev
Custom	F6S	1.1

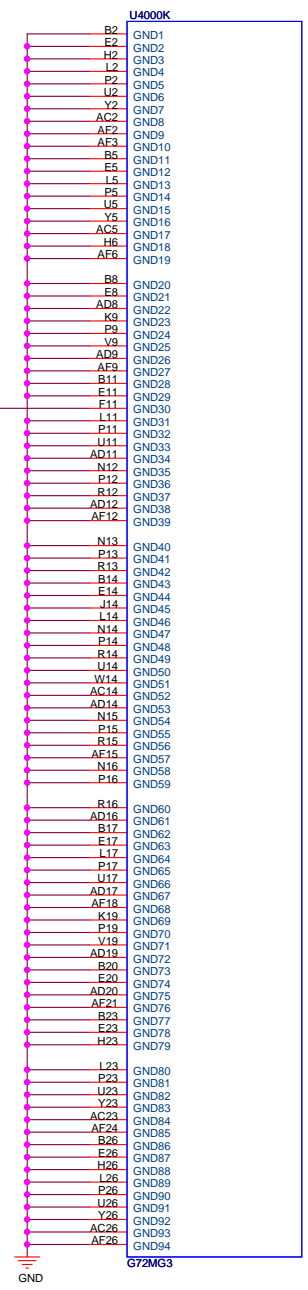
Date: Tuesday, August 21, 2007 Sheet 43 of 94



BackDrive Circuitry



- MIOB0----RAM_CFG0 0001 16M*16 DDR2 64-bit Samsung
- MIOB1----RAM_CFG1 0010 16M*16 DDR2 64-bit Infineon
- MIOB8----RAM_CFG2 0011 16M*16 DDR2 64-bit Hynix
- MIOB9----RAM_CFG3 0101 32M*16 DDR2 64-bit Samsung
- 0110 32M*16 DDR2 64-bit Infineon
- 0111 32M*16 DDR2 64-bit Hynix
- MIOB9----RAM_CFG3 0 Full width of the frame buffer
- 1 Half width of the frame buffer
- MIOB2----CRYSTAL0 00,13.5MHZ
- MIOB6----CRYSTAL1 01,14.318MHZ
- 10,27MHZ(Default)
- 11,RESERVED
- MIOB4----PCI_DEVID0 1000 NB8M-SE
- MIOB5----PCI_DEVID1
- MIOB3----PCI_DEVID2
- MIOBD1----PCI_DEVID3
- MIOBD10----ROMTYPE0 00,PARALLEL
- MIOB_VSYNC-ROMTYPE1 01,SERIAL AT25F
- 10,RESERVED
- 11,LPC
- MIOB7----MOBILE_MODE

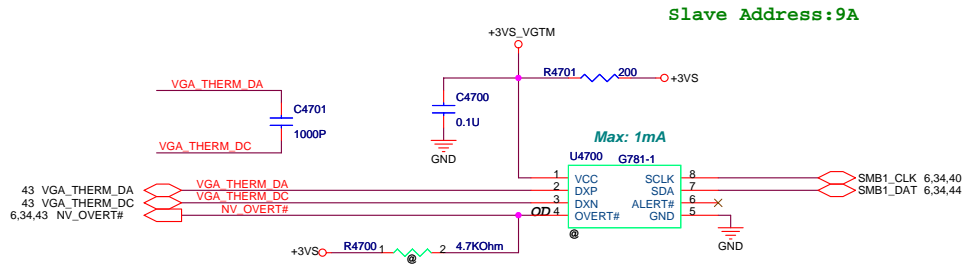


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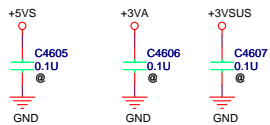
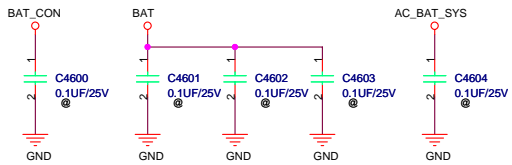
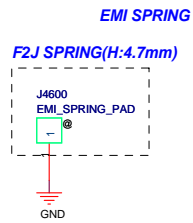
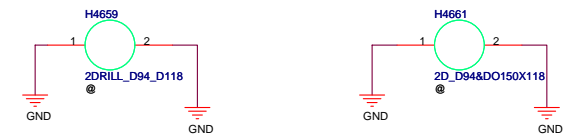
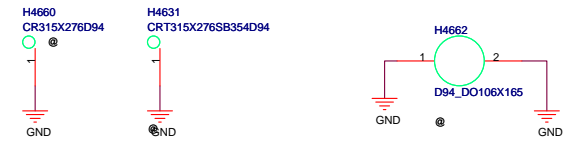
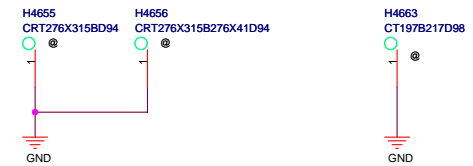
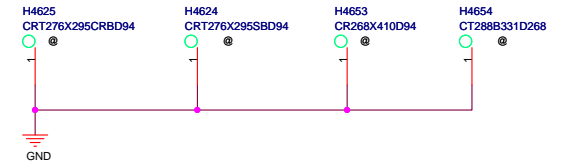
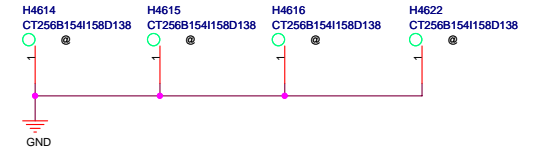
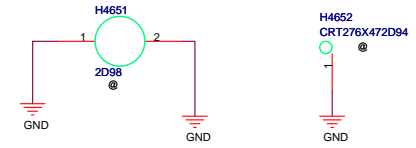
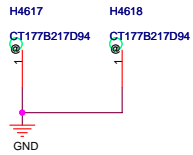
ASUS Title : **NB8MSE-TMDS (5)**

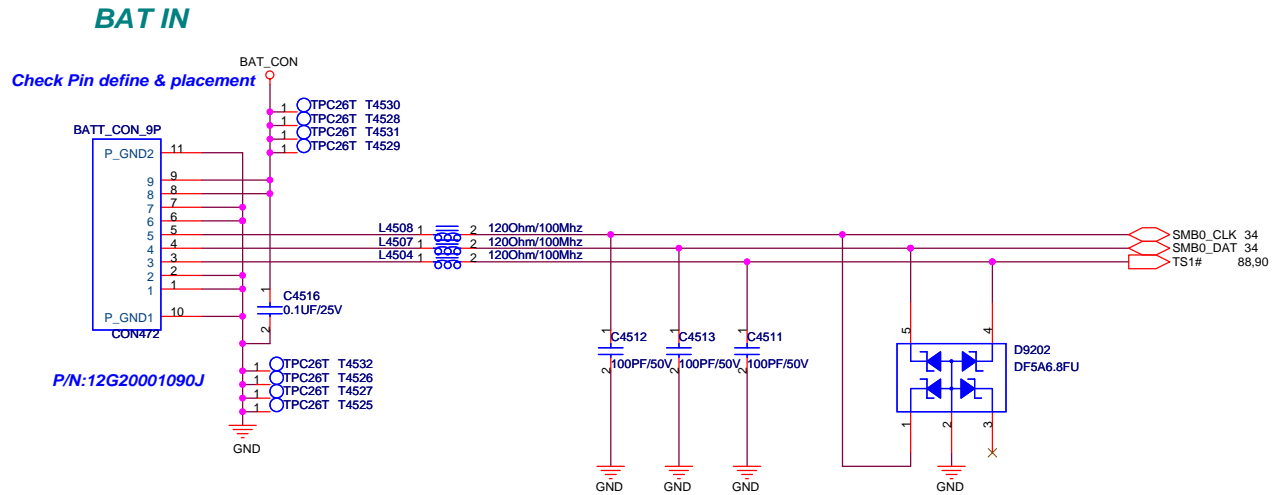
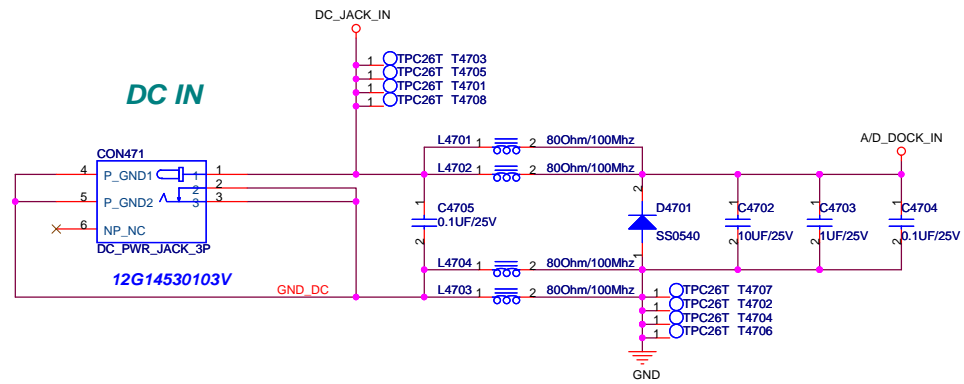
ASUSTek COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F6S	1.1
Date: Tuesday, August 21, 2007		Sheet 44 of 94



For frame buffer address/command lines those external pull up resistor can be removed for easy layout from Nvidia FAE





Rev0.3 (Change from R0.2)

- 1. Page 30: Change C3024, C3025 and C3029 from 4.7uF to 10uF for JMB FAE suggestion.
- 2. Page 30: Del R3002, R3004, R3005 and R3006.
- 3. Page 21: Del Finger printer power reset circuit for restart.
- 4. Page 29: Change C2938 4.7U 0603 to 0805 for cost down.
- 5. Page 38: Combine TP and F/P to one connector.
- 6. Page 19: Swap HDMI signals for layout request.
- 7. Page 20: change H2001 and H2002 to 13GNHC10M020-1.
- 8. Page 34: Add EC_RST# circuit for EC team suggestion.
- 9. Page 20: change H2001 and H2002 to 13GN7510M270-1 and change CON2001 to 12G030000523
- 10. Page 22: Swap CON2201 pin define for IO board layout.

Rev0.4 (Change from R0.3)

- 11. Page 30 and page 34: Swap RN3401 L3001 and RN3001 for layout.
- 12. Page 30 : Swap RN3001 and D3001 for layout.
- 13. Page 38 : Change SW3802 to 12G091033059.
- 14. Page 26 and 40 : Add NV_RST#(GPIO55) for NV8M-SE reset.
- 15. Page 7 : Add Q0701 for clk generator power saving.
- 16. Page 47 : Change CON472 to 12G20001090J
- 17. Page 19 : Change R1902 and C1901 from 0603 size to 0402 size.
- 18. Page 38 : Swap SW3804 Pin1 and Pin2 to meet ME request.
- 19. Page 38 : Del L1708 and add R1706 100 ohm for short protection.
- 20. Page 26, 35 and 40 : Change U2602, U3502 and U4002 from 06G004131011 to 06-004092010 for cost down.
- 21. Page 26: Change U2603 from 06G004603217 to 06G004603219 for cost down.
- 22. Page 7: Mount R0707 for PEREQ1# and PEREQ2#.
- 23. Page 28: Add C2839 for +VCCP_ICh.
- 24. Page 28: Change C2812 to 11G23521065320 for cost down.
- 25. Page 6: Add R0606 for PM_THRMTRIP# pull up to +VCCP.
- 26. Page 7: Change reference R785 to R0788
- 27. Page 16: Add C1603 4.7U for +0.9VS.
- 28. Page 27: Add R2703 and D2702 and DNI R2702 for ICH8_PWROK, to fix auto power on issue.
- 29. Page 24: Change R2411 0 ohm from 0603 to 0805 size.
- 30. Page 17: Add R1708 0 ohm for CCD.
- 31. Page 26 and 27: Del R2714 and R2738, add RN2613, swap RN2610, RN2612 and RN2700 for USB_OC[0-9]. USB_OC[1-7] can be set GPI if not needed(DNI RN2612 and RN2700).

- 32. Page 30: Jmicron suggest to dd R3020, C3035 and C3036 for eSATA JMB360.
- 33. Page 19: Del R1904-R1911, and add RN1901-RN1904.
- 34. Page 33: Change C3308 0.1u(Y5V) from 0603 to 0402. 0603 0.1u(Y5V) is single part.
- 35. Page 24: Del D2403, D2404, D2405 and D2406, add D2407 and D2408 for cost issue.
- 36. Page 43: Add R4314, R4318, R4319, R4338 and Q4301 for using NV8M-SE internal sensor.
- 37. Page 39: Del BT LED(DED395, R3909) and Num LED(LED394, R3906, Q3905) for sales PM request.
- 38. Page 47: Del D4504, D4505, D4506 and add D4507 for cost down.
- 39. Page 30 and 35: Change eSATA connector(CON301) and debug connector(CON352) for ME request.
- 40. Page 22: Add Q2202 for HDMI SPDIF jack sense.

Rev0.5 (Change from R0.4)

- 41. Page 39: Modify the LED circuit for white LED.
- 42. Page 46: Update all screw hole.
- 43. Page 6: Remane +5VS to +5V_FAN for FAN circuit as power request.
- 44. Page 46: Update H4631 screw hole.
- 45. Page 28: Change C2801 and C2801 from 0.1u to 1u.
- 46. Page 39: Change R3926 pin2 pull high from +5VS to +3VS.


Rev1.0 (Change from R0.5)

- 47. Change Rev from 0.5 to 1.0


Rev1.01 (Change from R1.0)

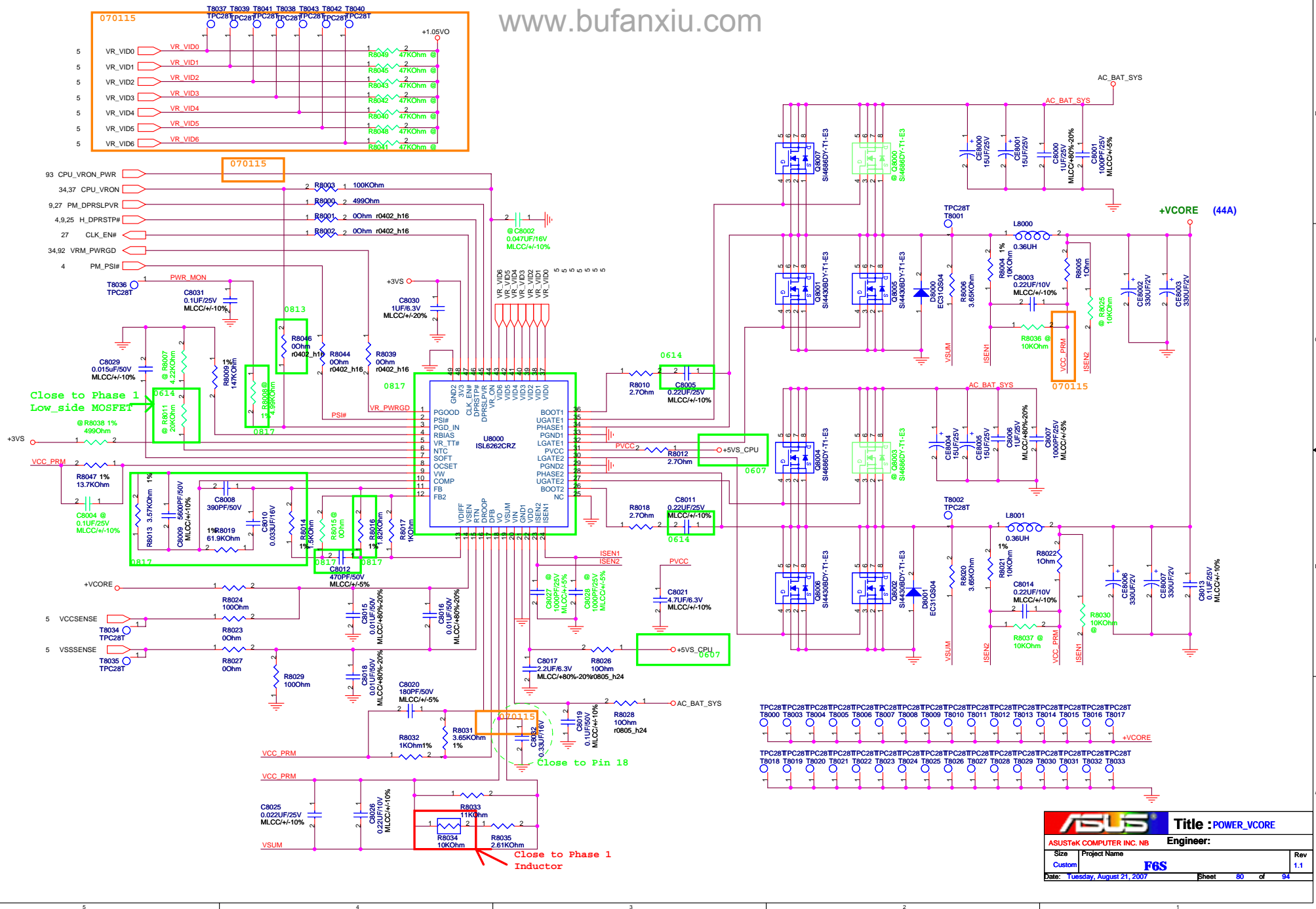
- 48. page 16: Change R1614 and R1615 from 10K to 1K, can meet S3 Vref voltage spec. DNI R1614, R1615 and Mount R1620 for Vref voltage provide from power.
- 49. page 07: Change R0713 from 33 ohm to 39 ohm to meet rise and fall timing.
- 50. page 12: Change C1220, C1227 and C1236 from 22uF to 4.7uF for cost down.
- 51. page 12: Change C1207, C1214, C1217 and C1224 from 22uF to 10uF for cost down.
- 52. page 12: Del C1202 4.7uF(0603) and Change C1201 from 4.7U(0603) to 10uF(0805) for cost down.
- 53. page 28: DNI C2805 and change C2806 from 22uF to 10uF for cost down.
- 54. page 28: Change CE2801 from 220uF to 100uF for cost down.

- 55. page 21 & 38: Del Q2101 and R3806 for never use.
- 56. page 40: Change C4016 from 22uF (1206) single part to 4.7uF for cost down.
- 57. page 6, 9, 30 & 34: Del 0 ohm R0655, R0937, R0938, R3010, R3015, R3418, R3419, R3445, R3449 and R3454 for cost down.
- 58. page 30: Del U3002, C3002 and C3015 for never use.
- 59. page 36: DNI R3608 and C3619, mount R3618 use PLT_RST#_BUF to reset RTS5158
- 60. page 29: Add C2941 and C2942 for _1.8V_LAN.
- 61. page 6: DNI R0606 and C0650.
- 62. page 6: Mount CN3501, CN3502, CN3503, CN3504, CN3505, and CN3506 for EMI request.
- 63. page 27: Del D2701, D2702 for no use as EC pin ICH8_PWROK, PM_RSMRST# open drain output.
- 64. page 30: DNI C3035, C3036 (eSATA Issue)
- 65. page 23: Del CE2301 100uF and add CE2302 and CE2303 47uF x2 for cost down.
- 66. page 30: Change CE3001 to CAP EL 100uF/10V for cost down.
- 67. page 36: Add R3619 for Realtek suggestion.
- 68. page 35: DNI R3505, R3507 and R3508 for EC team suggestion.
- 69. page 39: Del R3922, R3923, Q3911 for noise.
- 70. page 6: Add L4703 and L4704 for EMI request.
- 71. page 38: Change SW3804 to 12G09107003M.
- 72. page 17: Change CON175 to 12G17001030V.
- 73. page 46: Add screw hole H4663.
- 74. page 24: Change CON242 and CON243 to 12G131050044.
- 75. page 29: Colay TRL8111C.
- 76. page 29: Change R2903 to 2.21K ohm for GigaLan requires
- 77. page 22: DNI Q2202 for not support HDMI jack sense.
- 78. page 29: Mount C2943 for 100m cable link. Del C2941 and C2918.
- 79. page 38: Add R3808 and R3809(PLT_RST#_BUF) for Finger Printer.
- 80. page 36: Change C3668 and C3669 to 6pF for Realtek suggestion.
- 81. page 36: Mount C3618, C3609, R3608 and DNI R3618 for Realtek suggestion.
- 82. page 29 & 30: Change C2933, C2934, C3016 and C3017 to 27pF for ITTI suggestion.
- 83. page 7: Change C0709, C0710, 30pF for ITTI suggestion.

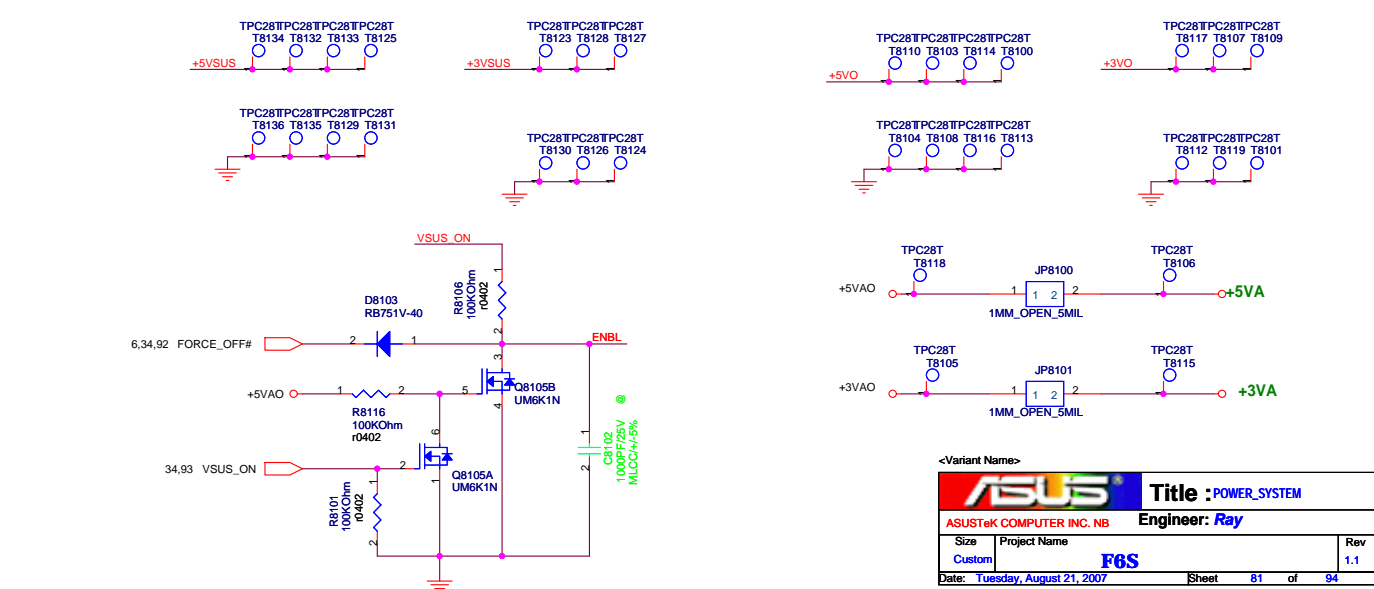
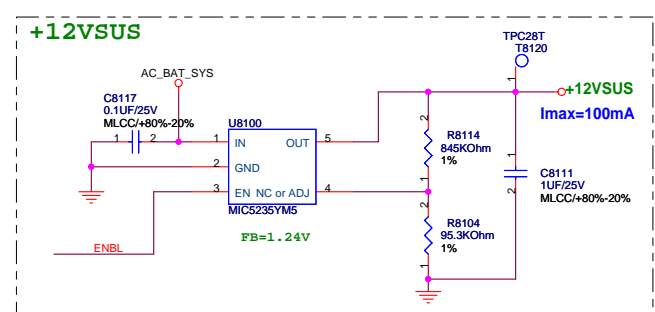
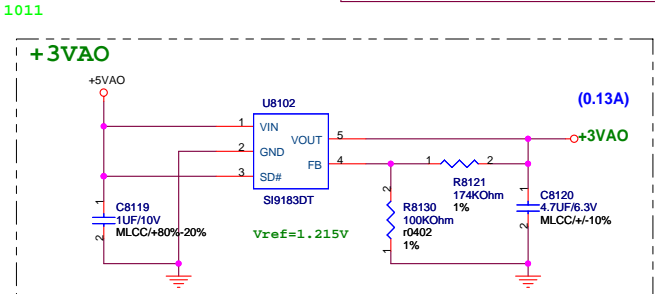
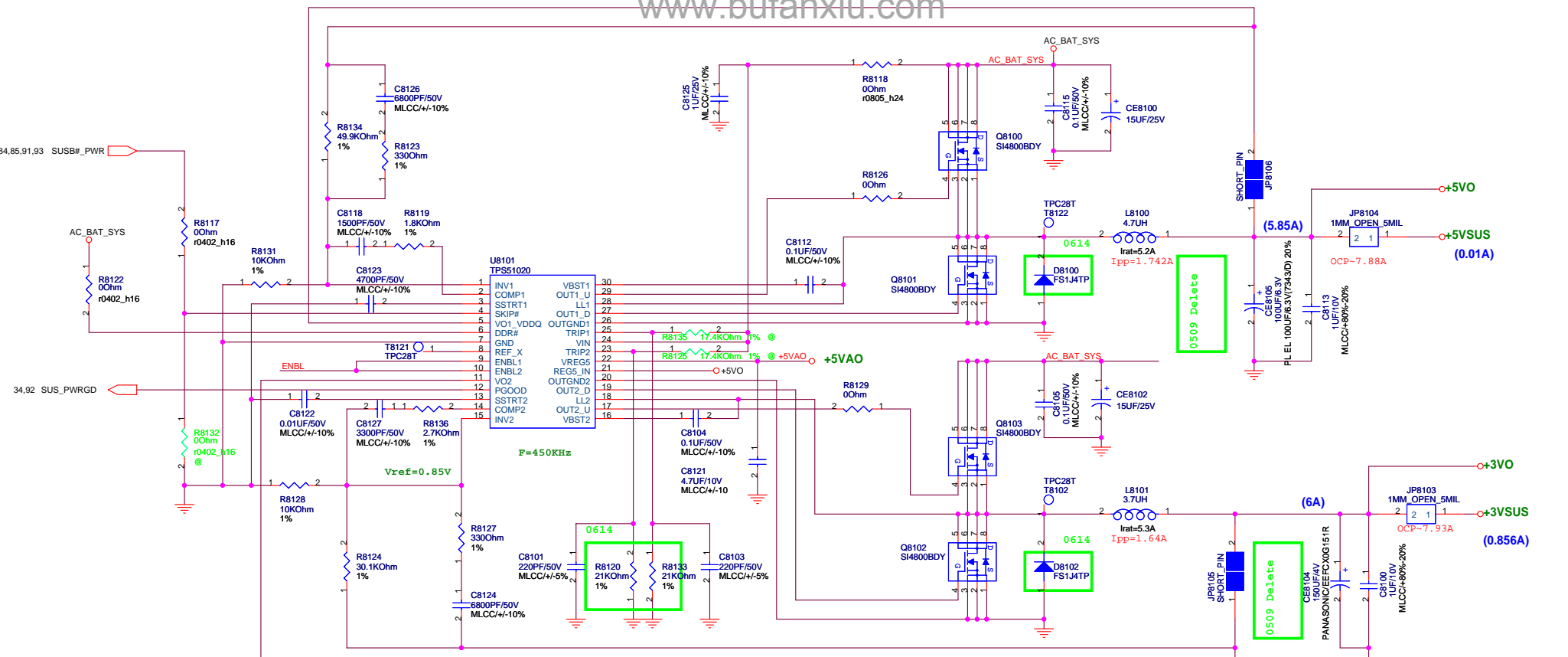
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ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	48 of 94

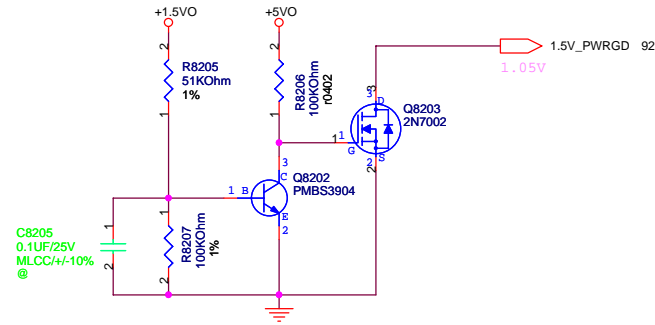
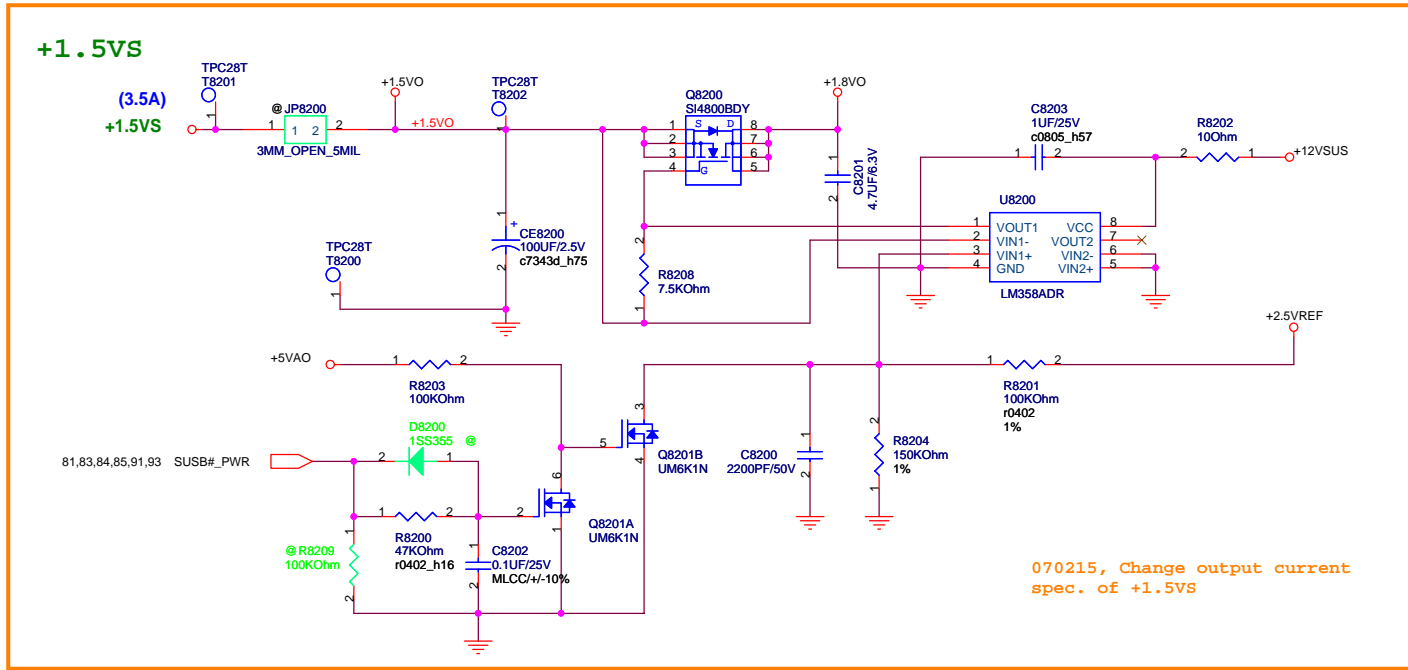
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Size	Project Name	Rev
Custom	F6S	1.1
Date: Tuesday, August 21, 2007		Sheet 49 of 94



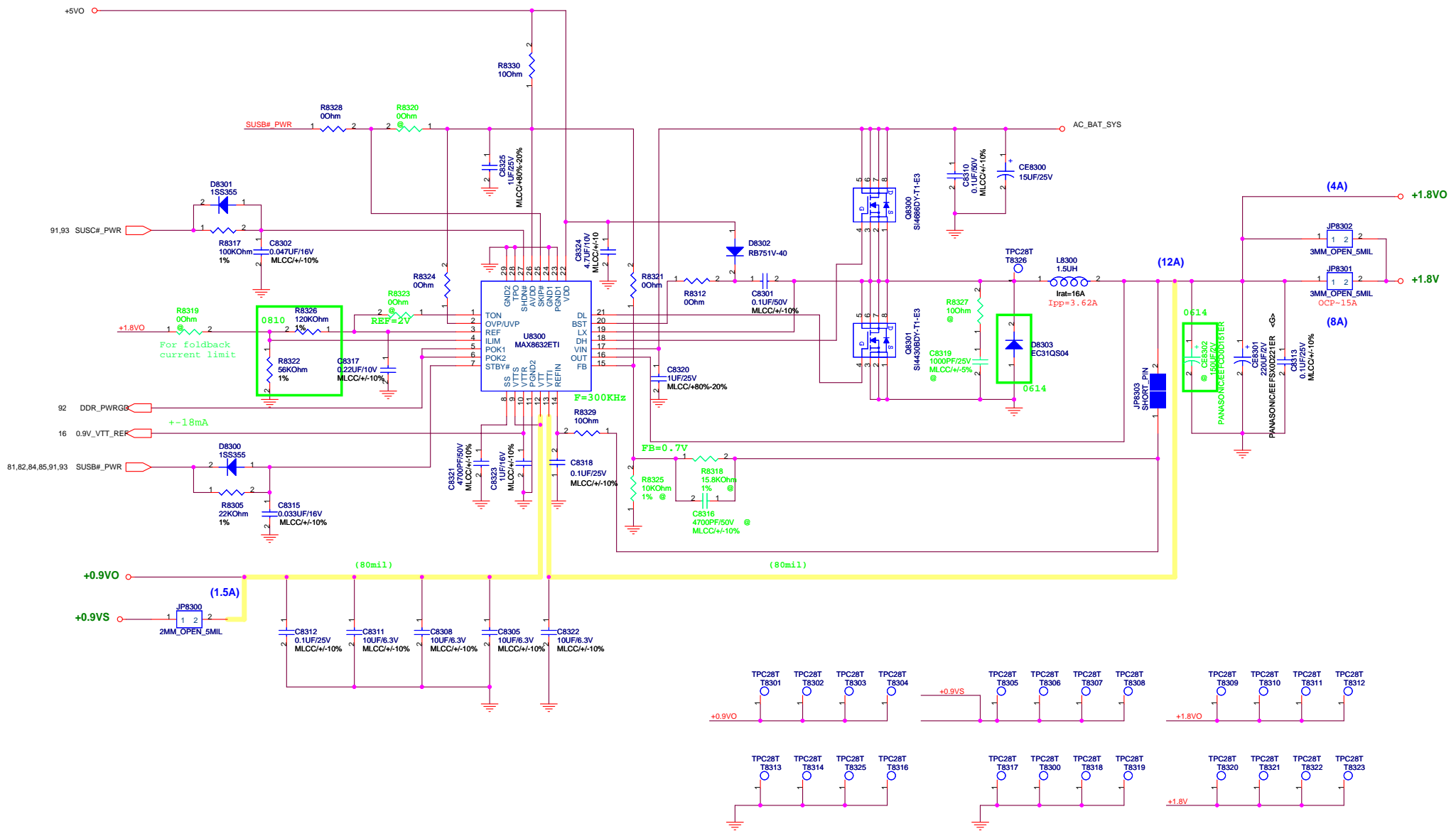
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ASUSTek COMPUTER INC. NB		Engineer:	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007	Sheet 80 of 84		

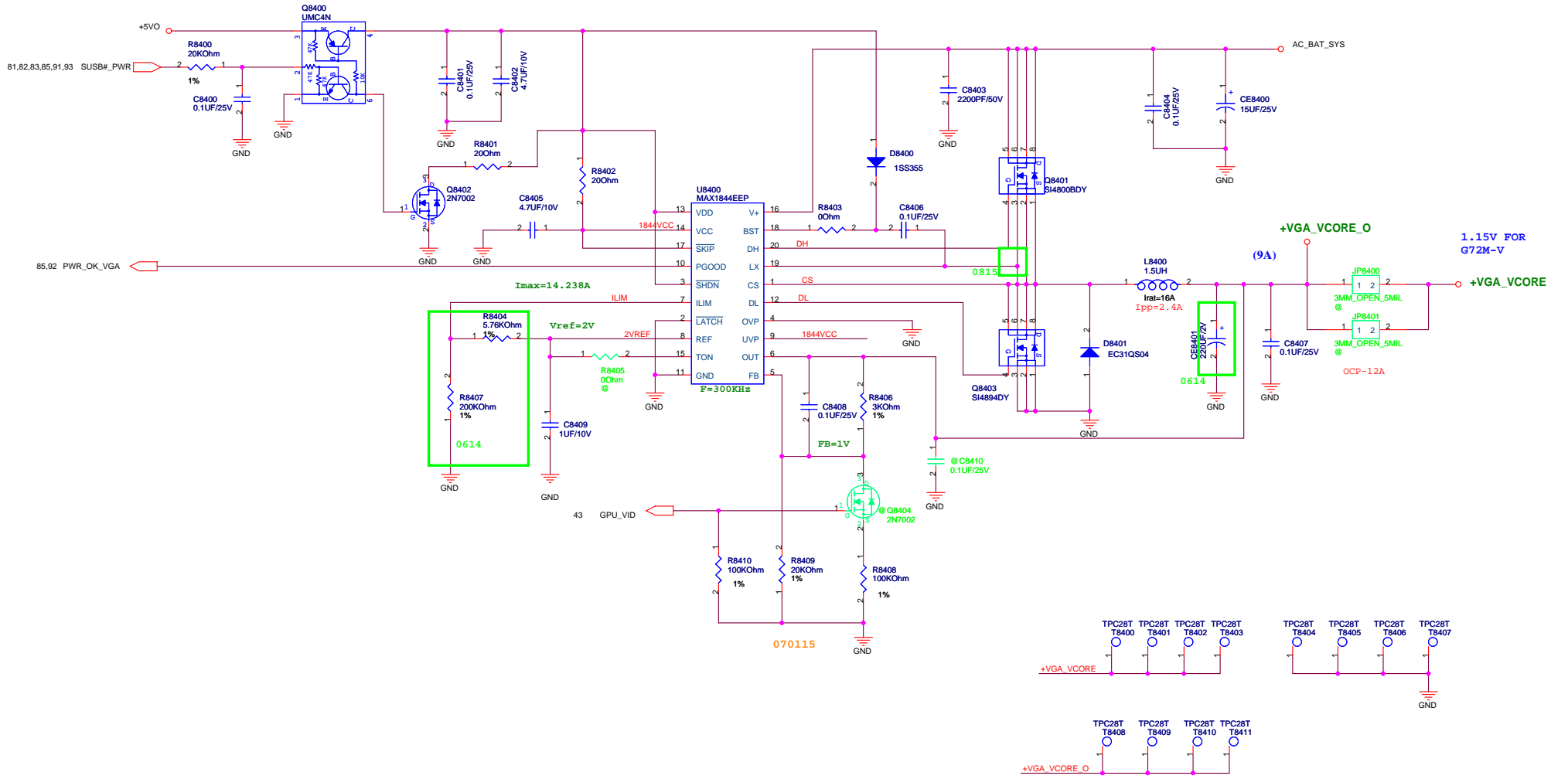




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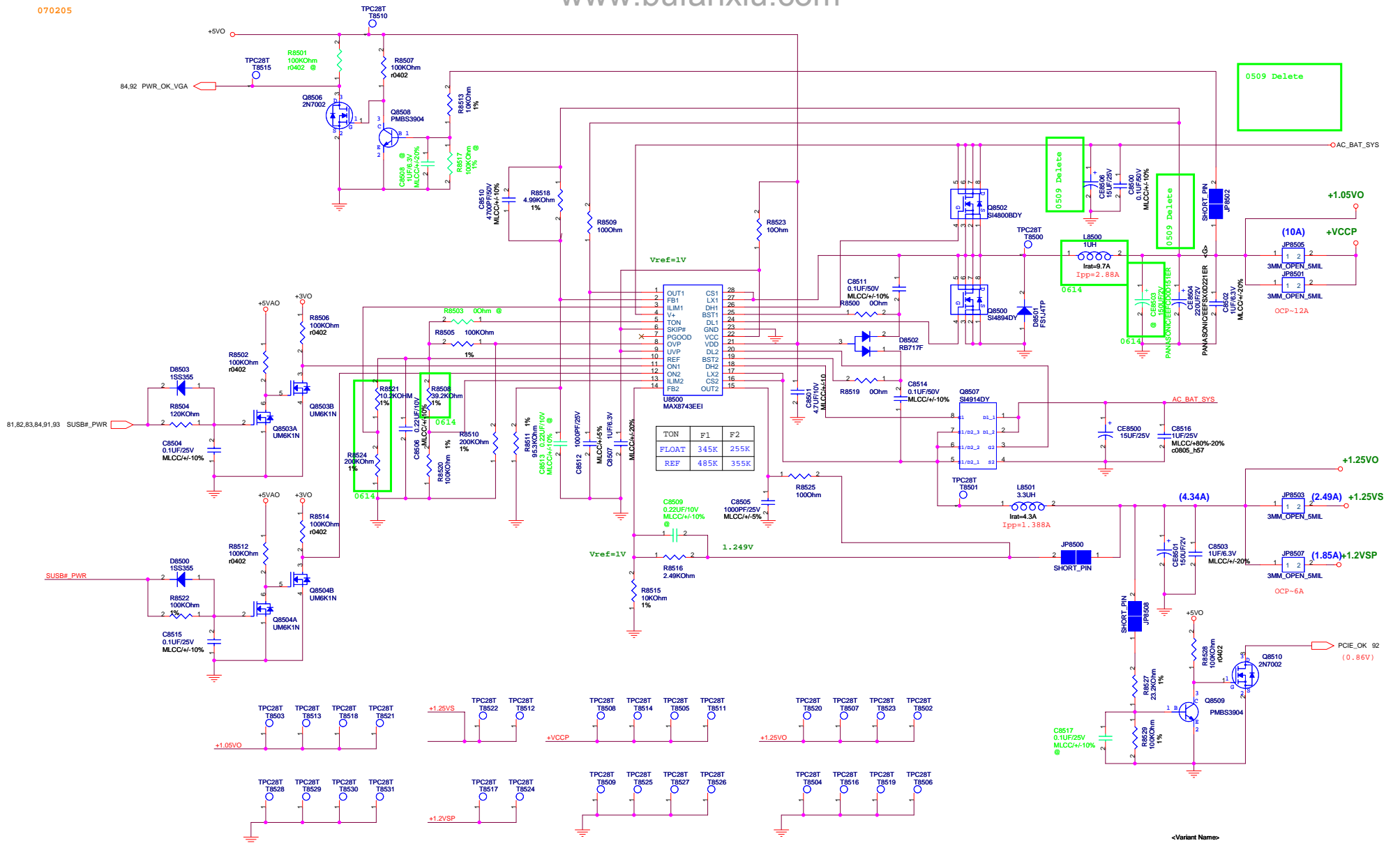
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ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size B	Project Name F6S		Rev 1.1
Date: Tuesday, August 21, 2007		Sheet	82 of 94





<Variant Name>

		Title : POWER_VGA_CORE	
ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007		Sheet	84 of 94



<Variant Name>


ASUS Title: POWER_+1.05V0 & +1.25V0

ASUSTek COMPUTER INC. NB Engineer: Ray

Size	Project Name	Rev
Custom	F6S	1.1

Date: Tuesday, August 21, 2007 Sheet 85 of 94

<Variant Name>

		Title : <i>N/A</i>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ray</i>	
Size	Project Name		Rev
B	F6S		1.0
Date: <i>Tuesday, August 21, 2007</i>		Sheet	86 of 94

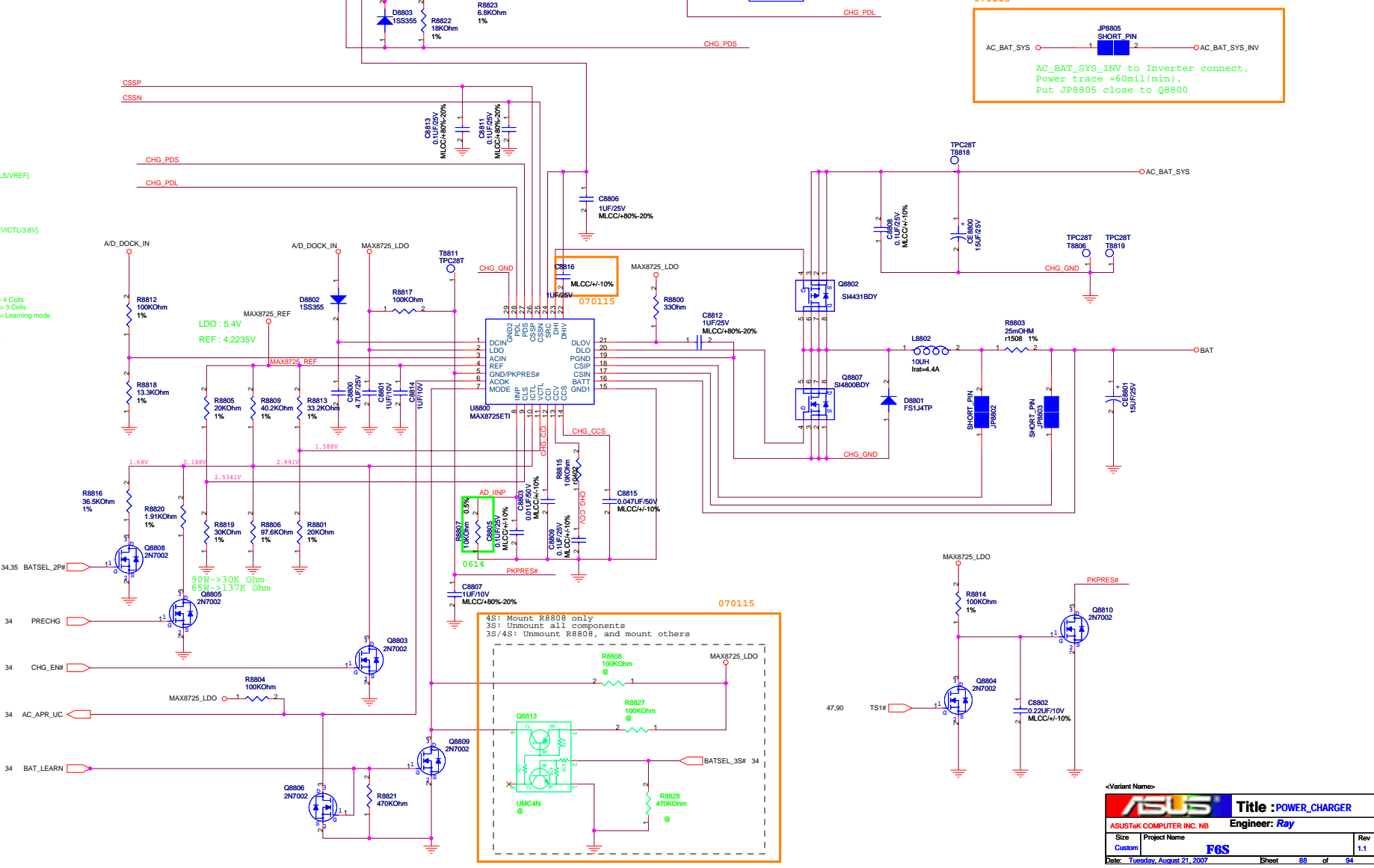
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		Title :POWER_SHUTDOWN#	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ray</i>	
Size	Project Name	Rev	
Custom	F6S	1.0	
Date: <u>Tuesday, August 21, 2007</u>		Sheet	87 of 94

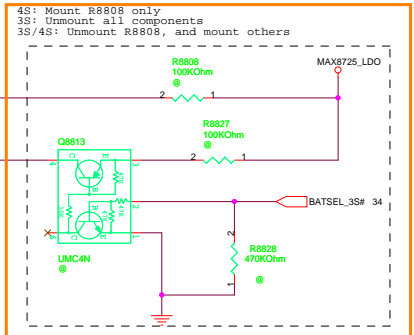
POWER PATH & BAT_LEARN

90 WATT

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Adapter In(max) = [0.075V/Rsense(Adin)] * [VCLS/VREF]
 Rsense(Adin) = 0.010ohm
 VCLS = 2.5341V
 => In(max) = 4.5A
 => Constant Power = 19 * 4.5 = 85.5W
 => RS710 = 20K, RS715 = 30K
 Charge Current Ichg = [0.075V/Rsense(CHG)] * [VICTL/3.6V]
 Rsense(CHG) = 0.025 ohm
 VICTL = 3V => Ichg = 2.5A
 VICTL = 1.58V => Ichg = 1.4A
 Vbatt = Cell * (Vref + (VCTL - 1.8V) / 9.52)
 VCTL = 1.58V
 => Vbatt = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
 2.0 > Vmode > 1.6V (floating) -> 3 Cells
 0.8 > Vmode (tie to GND) -> Learning mode
 VICTL < 0.8V or DCIN < 7V -> Charger Disable
 Precharge current = 150mA



AC_BAT_SYS_INV to Inverter connect,
 Power trace = 60mil(min),
 Put JP8805 close to Q8800



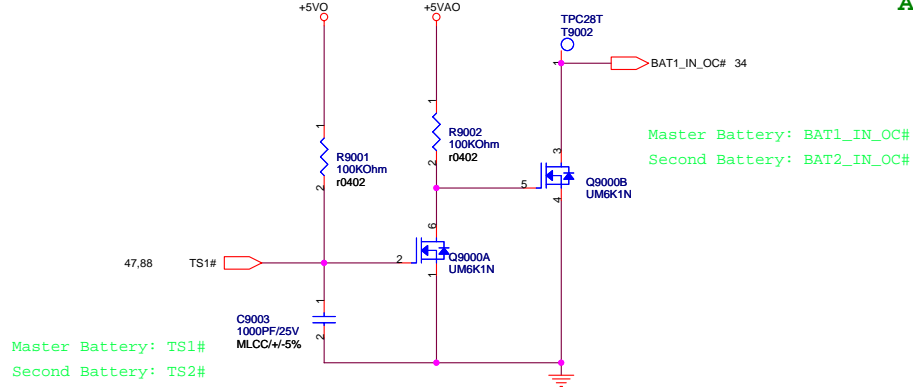
<Variant Name>

ASUS		Title : POWER_CHARGER	
ASUSTek COMPUTER INC. NB		Engineer: Ray	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007	Sheet	68	of 94

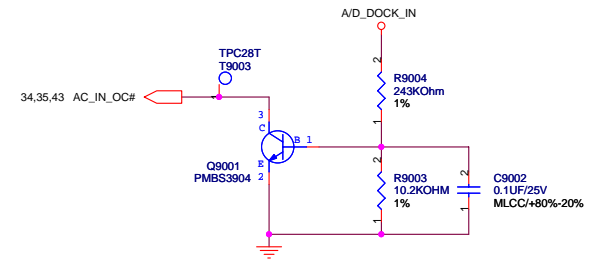
<Variant Name>

		Title : <i>N/A</i>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ehong-Ping</i>	
Size	Project Name		Rev
Custom	F9S		1.3
Date: <i>Tuesday, August 21, 2007</i>		Sheet	89 of 94

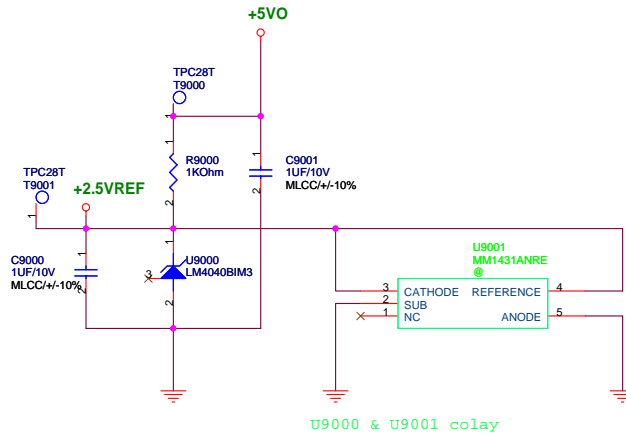
BATTERY IN DETECT



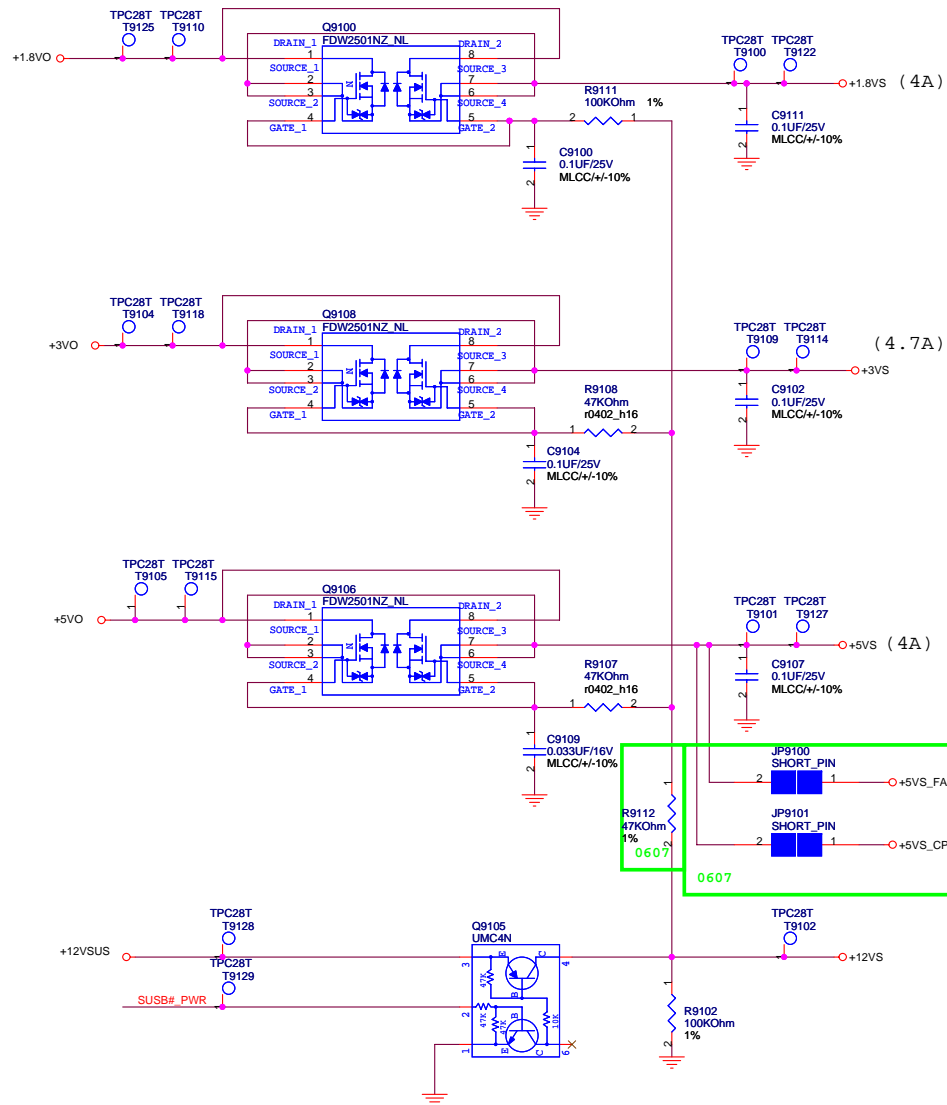
ADAPTER IN DETECT



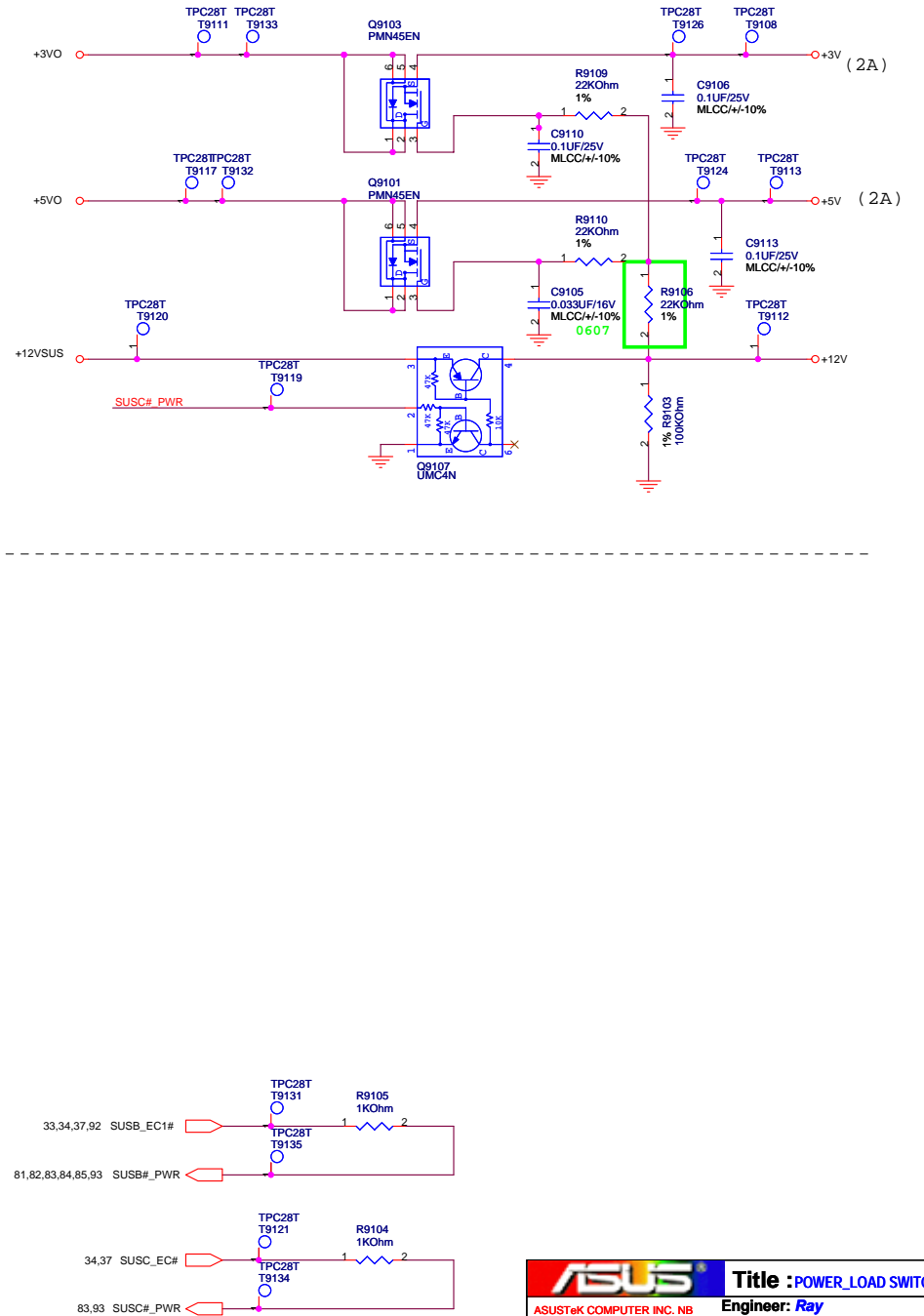
+2.5VREF



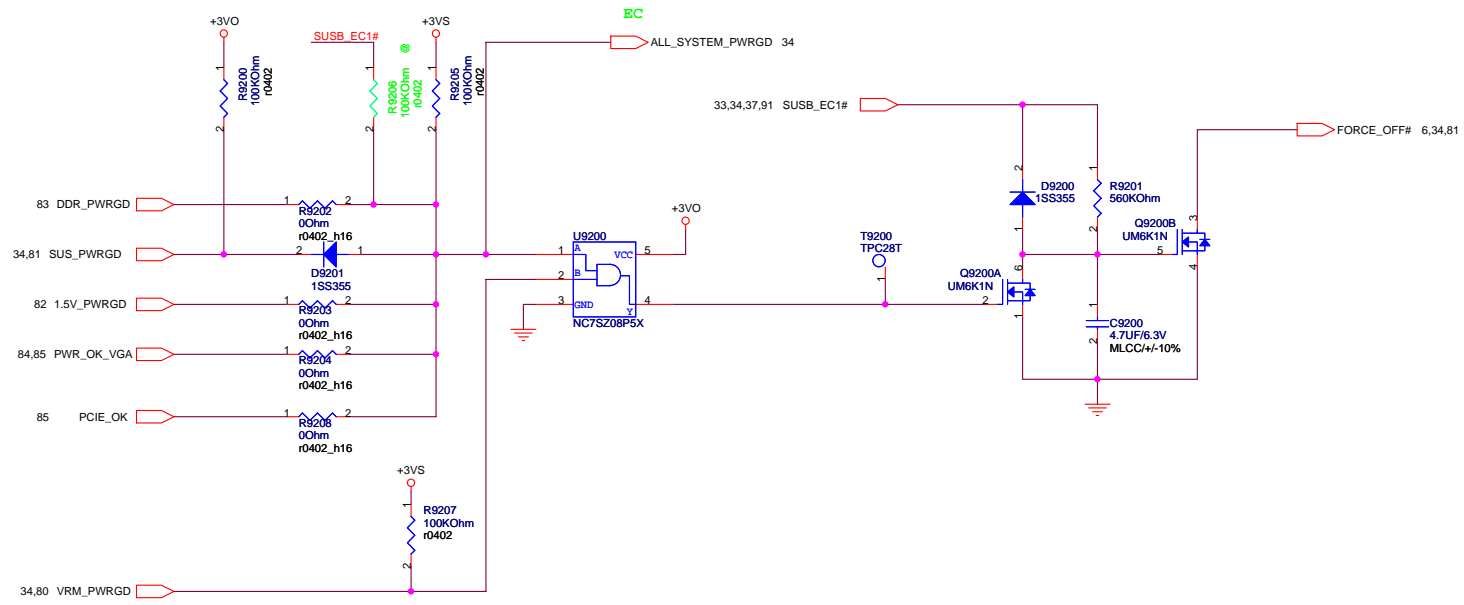
SUSB#_PWR POWER

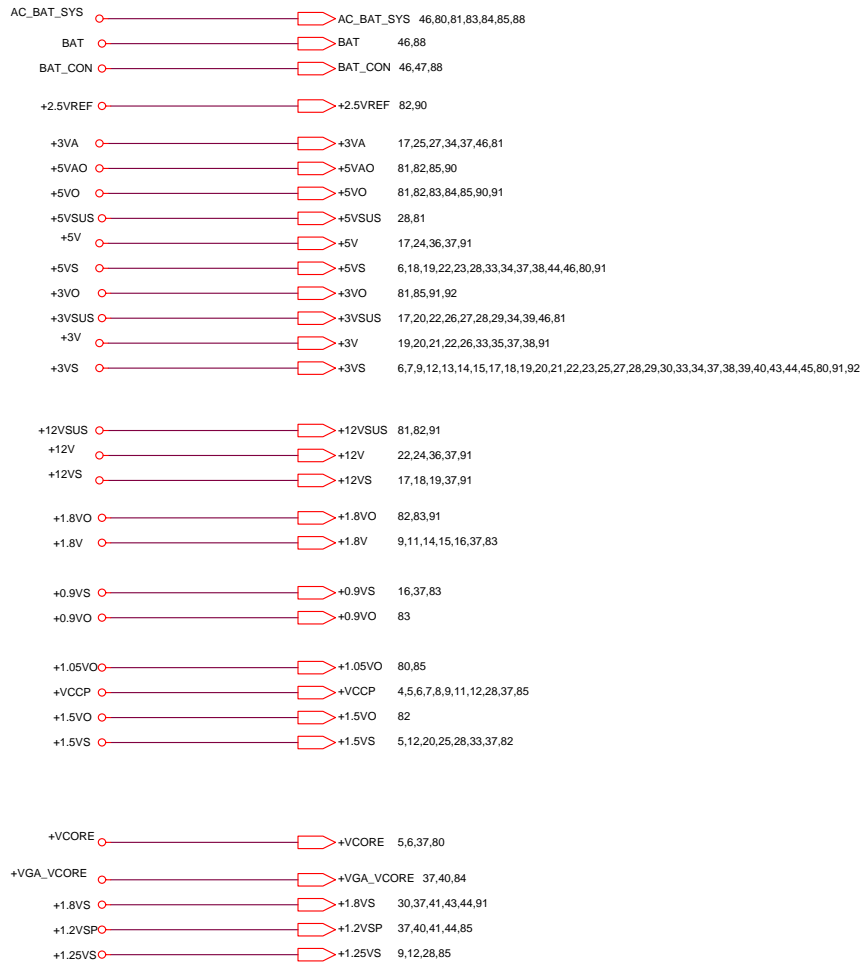


SUSC#_PWR POWER

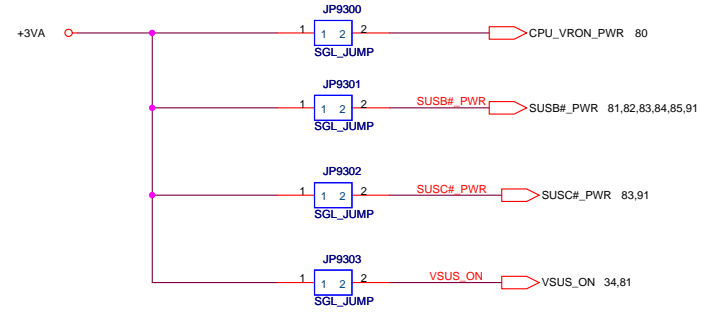


POWER GOOD DETECTER



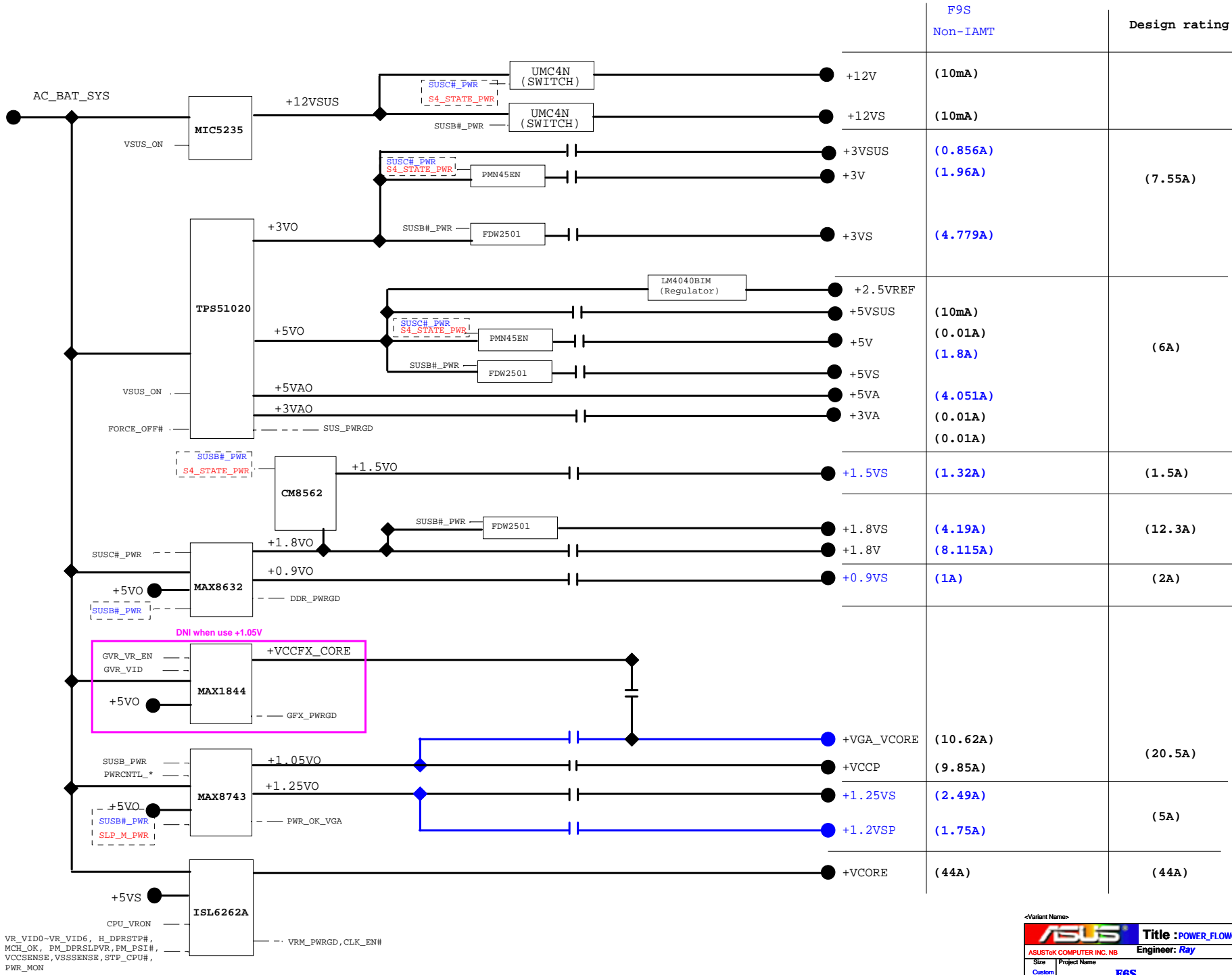


FOR POWER TEST



<Variant Names>

ASUS		Title :POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: Ray	
Size	Project Name		Rev
Custom	F6S		1.1
Date: Tuesday, August 21, 2007	Sheet	93	of 94



VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON