F6Ve SCHEMATIC Revision 1.0

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<Variant Name>

ASUSTeK COMPUTER INC

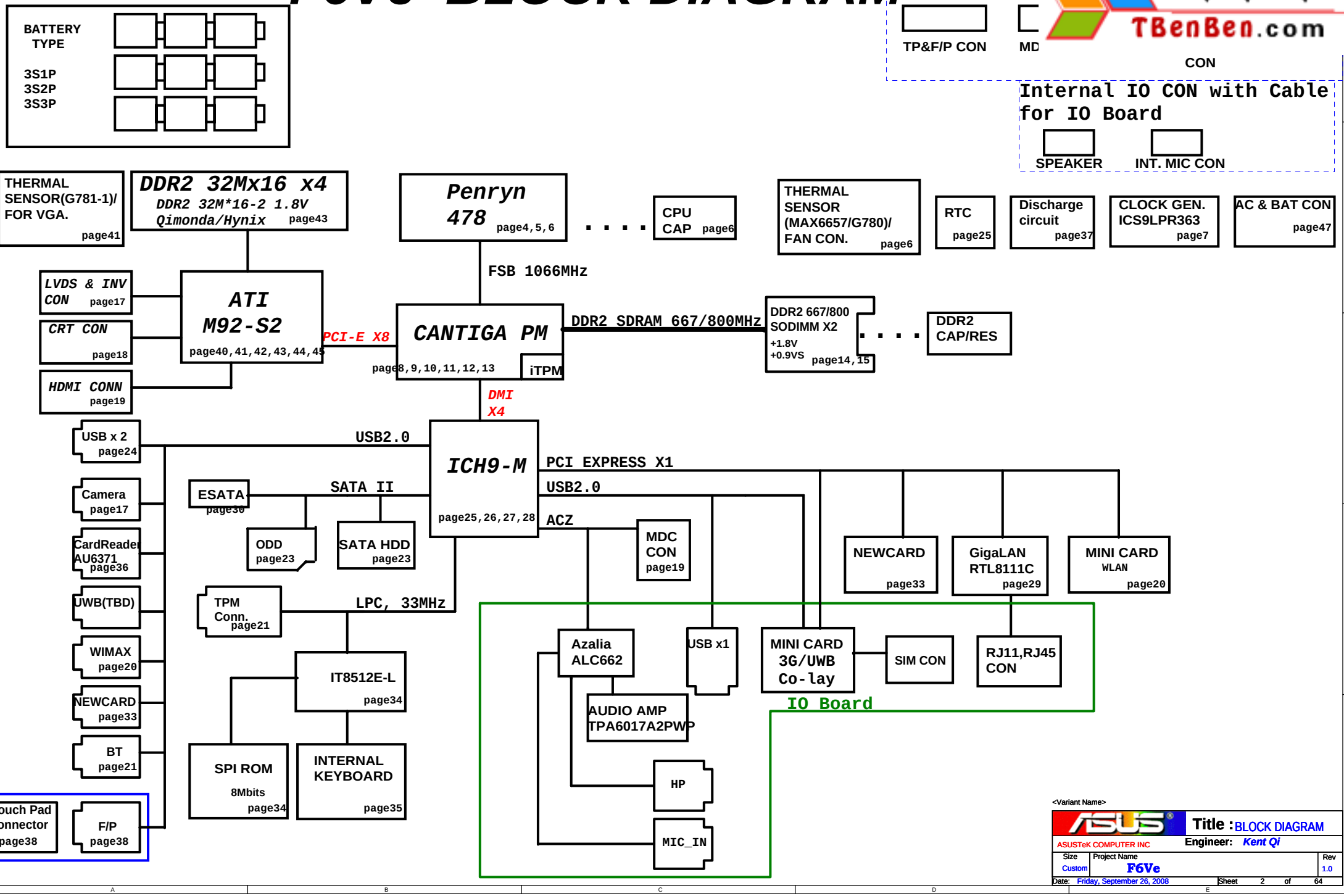
Title : PAGE REF.

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 1 of 64

F6Ve BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 2 of 64

ICH9-M GPIO

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	-	DOCKING_DET# EXT PU @	+3VS
GPIO [2:5]	GPI/OD	PCI_INT[E:H]# EXT PU	+3VS
GPIO 06	-	UNDOCKING_BTN# EXT PU @	+3VS
GPIO 07	-	IDE_BAY_IN# EXT PU @	+3VS
GPIO 08	-	EXT_SMI# EXT PU	+3VSUS
GPIO 09	-	WOL_EN EXT PU/PD @	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI	+3VSUS
GPIO 12	-	HDTV_DET# EXT PU @	+3VSUS
GPIO 13	-	CB_SD# (TP)	+3VSUS
GPIO 14	-	AC_PRESENT EXT PU	+3VSUS
GPIO 15(DT)	Native	STP_PCI#(PU to +3VS)	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD	+3VS
GPIO 17	GPO	WLAN_LED EXT PD	+3VS
GPIO 18	-	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	UWB_ON INT PD	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	-	BT_DET# EXT PU @	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	-	-	+3VSUS
GPIO 25(DT)	Native	STP_CPU#(PU to +3VS)	+3VSUS
GPIO 26	-	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32(DT)	Native	PM_CLKRUN#	+3VS
GPIO 33	-	- INT PU	+3VS
GPIO 34	-	-	+3VS
GPIO 35	-	SATACLKREQ# EXT PU @	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	+3VSUS
GPIO 45	Native	USB_OC9#	+3VSUS
GPIO 46	GPO	USB_OC10#/WLAN_ON	+3VSUS
GPIO 47	Native	USB_OC11#	+3VSUS
GPIO 48	GPI	EMAIL_LED EXT PD @	+3VS
GPIO 49	-	- INT PU	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU	+3VS
GPIO 56	-	- EXT PU	+3VSUS
GPIO 57	GPI	MEM_ID1 EXT PU @	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	GPO	RTLAN_DSM_EN/LINKALERT# EXT PU	+3VSUS

GPIO33 Internal Pull High, Go Low= Flash Descriptor Security will be overriden

EC IT8512

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	-	-	
GPA7	-	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	-	-	
GPB3	ALT	SMB0_CLK Battery	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	-	-	
GPC1	ALT	SMB1_CLK ThermalSensor	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	GPI	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	GPI	BAT1_IN_OC#	
GPC7	GPI	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	GPI	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	GPI	FAN0_TACH	
GPD7	GPO	SD_CD#_EC	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	GPI	PWR_SW#	
GPE5	-	-	
GPE6	GPI	LID_SW#	
GPE7	-	-	
GPF0	-	-	
GPF1	-	-	
GPF2	GPI	MARATHON#	
GPF3	-	-	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	-	-	
GPG0	GPO	PM_THERM#_EC	
GPG1	GPI	PM_SUSB#	
GPG2	-	-	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	-	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	GPO	3G_ON#	
GPH2	-	-	
GPH3	GPO	BAT_LEARN	
GPH4	-	-	
GPH5	-	-	
GPH6	GPO/OD	CAP_LED#	
-	-	-	
GPI0	GPI	VGA_ALERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	-	-	
GPI6	GPI	KB_ID0(NC)	
GPI7	GPI	KB_ID1(NC)	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	GPO	BATSEL_2P#	
GPJ4	-	-	
GPJ5	-	-	
GPK0	-	-	
GPK1	-	-	
GPK2	-	-	
GPK3	-	-	
GPK4	-	-	
GPK5	-	-	
GPL0	-	-	
GPL1	-	-	
GPL2	-	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	-	-	
GPL6	-	-	
GPL7	-	-	
GPK6	-	-	
GPK7	-	-	

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	UWB(TBD)
PCIE 6	LAN

SATA 0	SATA HDD
SATA1	SATA ODD
SATA4	
SATA5	ESATA

USB 0	USB Conn
USB 1	
USB 2	USB Conn
USB 3	USB Conn
USB 4	CMOS Camera
USB 5	CardReader
USB 6	UWB(TBD)
USB 7	WiMax
USB 8	NewCard
USB 9	3G Card
USB 10	Bluetooth
USB 11	FINGER PRINT

<Variant Name>

ASUSTeK COMPUTER INC

Title : Schematic Info.

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 3 of 64

[8] H_D#[63:0] — H_D#[63:0]

[8] H_A#[35:3] — H_A#[35:3]

[8] H_REQ#[4:0] — H_REQ#[4:0]

Place on Top

T0419 T0420

U0401A

ADDR GROUP 0

H_A#3 J4
H_A#4 L5
H_A#5 L4
H_A#6 K5
H_A#7 M3
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P5
H_A#12 P2
H_A#13 L2
H_A#14 P4
H_A#15 P1
H_A#16 R1
[8] H_ADSTB#0 M1

A[3]# A[4]# A[5]# A[6]# A[7]# A[8]# A[9]# A[10]# A[11]# A[12]# A[13]# A[14]# A[15]# A[16]# ADSTB[0]#

H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L1

REQ[0]# REQ[1]# REQ[2]# REQ[3]# REQ[4]#

ADDR GROUP 1

H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U1
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W2
H_A#28 W5
H_A#29 Y4
H_A#30 U2
H_A#31 V4
H_A#32 W3
H_A#33 AA4
H_A#34 AB2
H_A#35 AA3
[8] H_ADSTB#1 V1

A[17]# A[18]# A[19]# A[20]# A[21]# A[22]# A[23]# A[24]# A[25]# A[26]# A[27]# A[28]# A[29]# A[30]# A[31]# A[32]# A[33]# A[34]# A[35]# ADSTB[1]#

T0421

H_A20M# A6
H_FERR# A5
H_IGNNE# C4

A20M# FERR# IGNNE#

T0422

H_STPCLK# D5
H_INTR C6
H_NMI B4
H_SMI# A3

STPCLK# LINT0 LINT1 SMI#

T0409 M4
T0410 N5
T0411 T2
T0412 V3
T0413 B2
T0414 C3
T0415 D2
T0416 D22
T0417 D3
T0418 F6

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10

RESERVED

CONTROL

ADS# H1 — H_ADS# [8]
BNR# E2 — H_BNR# [8]
BPRI# G5 — H_BPRI# [8]

DEFER# H5 — H_DEFER# [8]
DRDY# F21 — H_DRDY# [8]
DBSY# E1 — H_DBSY# [8]

BR0# F1 — H_BR0# [8]

+VCCP_CPU

IERR# D20 — H_IERR# — R0401 1 2 56Ohm
INIT# B3 — H_INIT# [25]

LOCK# H4 — H_LOCK# [8]

RESET# C1 — H_CPURST# [8]
RS[0]# F3 — H_RS#0 [8]
RS[1]# F4 — H_RS#1 [8]
RS[2]# G3 — H_RS#2 [8]
TRDY# G2 — H_TRDY# [8]

HIT# G6 — H_HIT# [8]
HITM# E4 — H_HITM# [8]

XDP/ITP SIGNALS

BPM[0]# AD4 XDP_BPM#0 1 T0455
BPM[1]# AD3 XDP_BPM#1 1 T0456
BPM[2]# AD1 XDP_BPM#2 1 T0457
BPM[3]# AC4 XDP_BPM#3 1 T0458
PRDY# AC2 XDP_BPM#4 1 T0459
PREQ# AC1 XDP_PREQ# 1 T0460
TCK AC5 XDP_TCK 1 T0461
TDI AA6 XDP_TDI 1 T0462
TDO AB3 XDP_TDO 1 T0463
TMS AB5 XDP_TMS 1 T0464
TRST# AB6 XDP_TRST# 1 T0465
DBR# C20 XDP_DBR# 1 T0466

THERMAL

PROCHOT# D21 H_PROCHOT_S#
THRMDA A24 — CPU_THRM_DA [6]
THRMDC B25 — CPU_THRM_DC [6]

THERMTRIP# C7 — H_THRMTRIP# [6,9,25]

H CLK

T0405

BCLK[0] A22 — CLK_CPU_BCLK [7]
BCLK[1] A21 — CLK_CPU_BCLK# [7]

T0403

SOCKET478B

U0401B

DATA GRP 0

H_D#0 E22
H_D#1 F24
H_D#2 E26
H_D#3 G22
H_D#4 E23
H_D#5 G25
H_D#6 E25
H_D#7 E23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H22
H_D#13 F26
H_D#14 K22
H_D#15 H23

D[0]# D[1]# D[2]# D[3]# D[4]# D[5]# D[6]# D[7]# D[8]# D[9]# D[10]# D[11]# D[12]# D[13]# D[14]# D[15]#

[8] H_DSTBN#0 J26
[8] H_DSTBP#0 H26
[8] H_DINV#0 H25

DSTBN[0]# DSTBP[0]# DINV[0]#

DATA GRP 2

D[32]# D[33]# D[34]# D[35]# D[36]# D[37]# D[38]# D[39]# D[40]# D[41]# D[42]# D[43]# D[44]# D[45]# D[46]# D[47]#

Y22 H_D#32
AB24 H_D#33
V24 H_D#34
V26 H_D#35
V23 H_D#36
T22 H_D#37
U25 H_D#38
U23 H_D#39
Y25 H_D#40
W22 H_D#41
Y23 H_D#42
W24 H_D#43
W25 H_D#44
AA23 H_D#45
AA24 H_D#46
AB25 H_D#47

DSTBN[2]# DSTBP[2]# DINV[2]#

Y26 — H_DSTBN#2 [8]
AA26 — H_DSTBP#2 [8]
U22 — H_DINV#2 [8]

DATA GRP 1

H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L23
H_D#21 M24
H_D#22 L22
H_D#23 M23
H_D#24 P25
H_D#25 P23
H_D#26 P22
H_D#27 T24
H_D#28 R24
H_D#29 L25
H_D#30 T25
H_D#31 N25

D[16]# D[17]# D[18]# D[19]# D[20]# D[21]# D[22]# D[23]# D[24]# D[25]# D[26]# D[27]# D[28]# D[29]# D[30]# D[31]#

[8] H_DSTBN#1 L26
[8] H_DSTBP#1 M26
[8] H_DINV#1 N24

DSTBN[1]# DSTBP[1]# DINV[1]#

DATA GRP 3

D[48]# D[49]# D[50]# D[51]# D[52]# D[53]# D[54]# D[55]# D[56]# D[57]# D[58]# D[59]# D[60]# D[61]# D[62]# D[63]#

AE24 H_D#48
AD24 H_D#49
AA21 H_D#50
AB22 H_D#51
AB21 H_D#52
AC26 H_D#53
AD20 H_D#54
AE22 H_D#55
AF23 H_D#56
AC25 H_D#57
AE21 H_D#58
AD21 H_D#59
AC22 H_D#60
AD23 H_D#61
AF22 H_D#62
AC23 H_D#63

DSTBN[3]# DSTBP[3]# DINV[3]#

AE25 — H_DSTBN#3 [8]
AF24 — H_DSTBP#3 [8]
AC20 — H_DINV#3 [8]

MISC

GTLREF AD26
TEST1 C23
TEST2 D25
TEST3 C24
TEST4 AF26
TEST5 AE1
TEST6 A26

BSEL[0] B22
BSEL[1] B23
BSEL[2] C21

COMP[0] R26 H_COMP0 R0403 1 2 27.4Ohm 1%
COMP[1] U26 H_COMP1 R0404 1 2 54.9Ohm 1%
COMP[2] AA1 H_COMP2 R0405 1 2 27.4Ohm 1%
COMP[3] Y1 H_COMP3 R0406 1 2 54.9Ohm 1%

DPRSTP# E5 — H_DPRSTP# [9,25,80]
DPSLP# B5 — H_DPSLP# [25]
DPWR# D24 — H_DPWR# [8]
PWRGOOD D6 — H_DPWRD [25]
SLP# D7
PSI# AE6 — H_CPUSLP# [8] — PM_PSI# [80]

T0401 T0404

SOCKET478B

+VCCP_CPU

R0407 1KOhm 1%

[8] H_DSTBN#1
[8] H_DSTBP#1
[8] H_DINV#1

GTL_REF

R0415 2 @ 1% 1 1KOhm
R0416 2 @ 1% 1 1KOhm

T0406 1

C0466 0.1U @

T0407 T0408

T0436

[7] CPU_BSEL0
[7] CPU_BSEL1
[7] CPU_BSEL2

R0408 2KOhm 1%

C0401 0.1UF/10V @

Zo=55 Ohm, 0.5" max for GTL_REF

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

C0466
TEST4:CRB 0.1U Reserved
DG & Checklist:NC

BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

@ +VCCP_CPU
2 R0419 1
200Ohm

Follow DESIGN_IP M51Va

For XDP refer to #356027

+VCCP_CPU

XDP_PREQ# R0402 1 2 54.9Ohm 1%
XDP_TDI R0433 1 2 54.9Ohm 1%
XDP_TDO R0434 1 @ 2 54.9Ohm 1%
XDP_TMS R0435 1 2 54.9Ohm 1%

XDP_TCK R0417 1 2 54.9Ohm 1%
XDP_TRST# R0418 1 2 54.9Ohm 1%

Checklist:
PROCHOT# not used:56ohm
CPU & IMVP6:68ohm each side

+VCCP_CPU

R0410 68Ohm

H_PROCHOT_S#

[34,35] PWRLIMIT#

EC PU 47K TO +3VA

BAT54C D0403 @

Q0401 2N7002

THRO_CPU [34]

+3VS

R0409 10KOhm

UM6K1N Q0406B

Q0406A UM6K1N

PM_THERM#_EC [27,34]

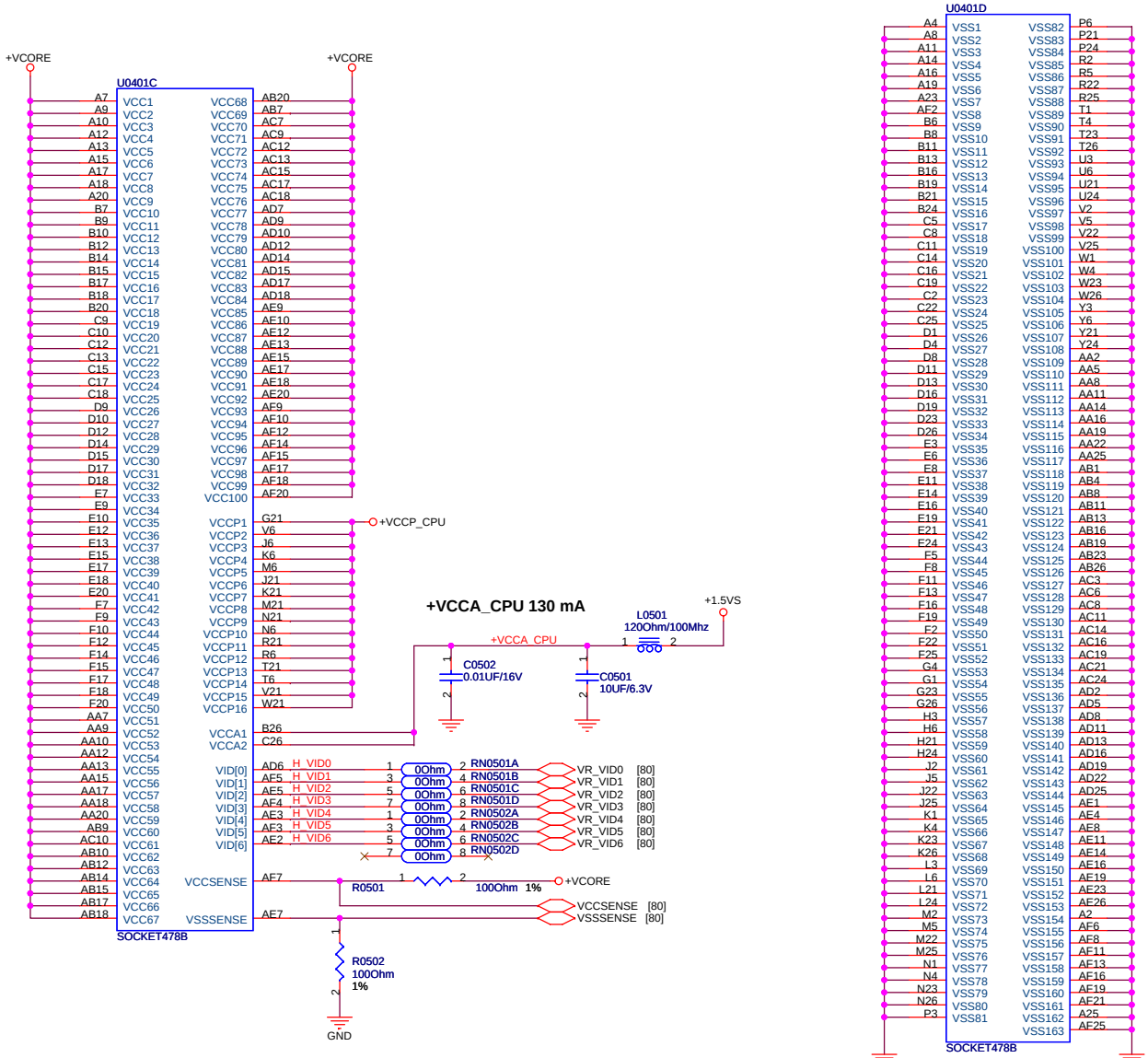
ASUSTeK COMPUTER INC. NB1

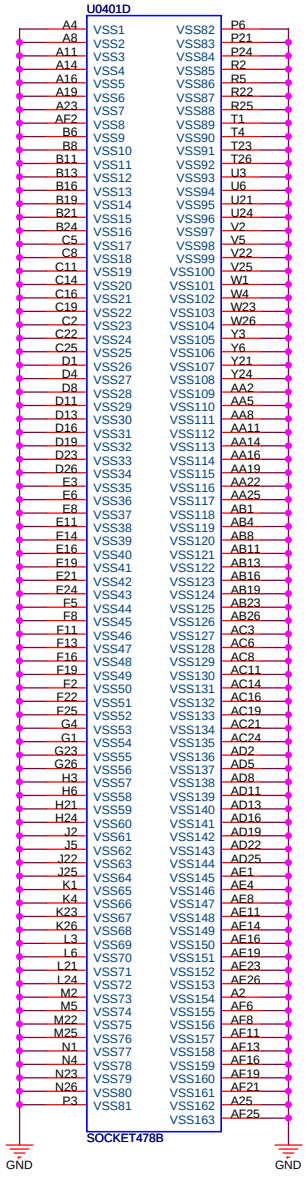
Title : CPU-Penryn(1)

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 4 of 64



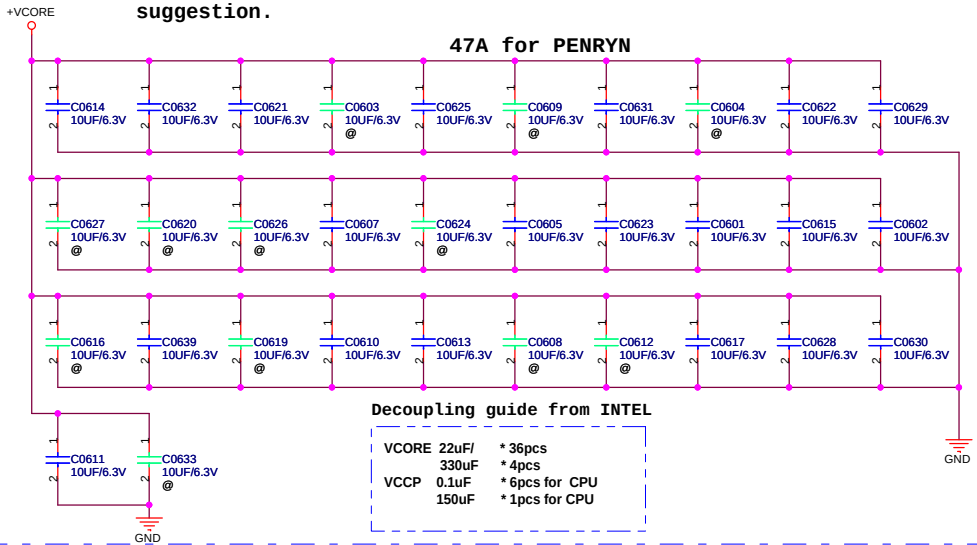


ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn(2)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 5 of 64	

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

Cap Follow DesignIP
22U/6.3V 0805_55:11G235222625320

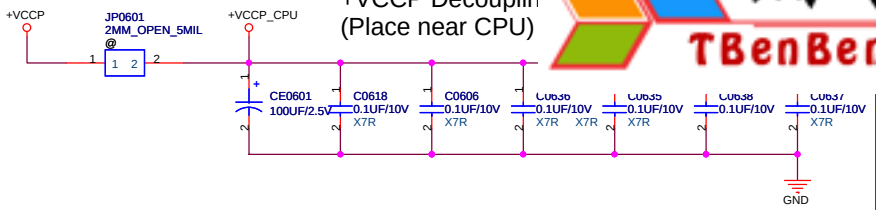
47A for PENRYN

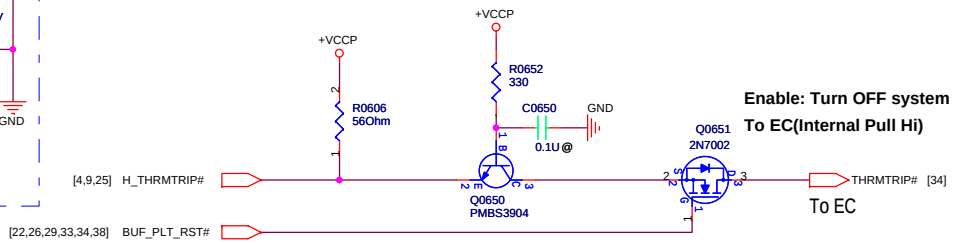


Decoupling guide from INTEL

VCORE	22uF/	* 36pcs
	330uF	* 4pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decouplin
(Place near CPU)

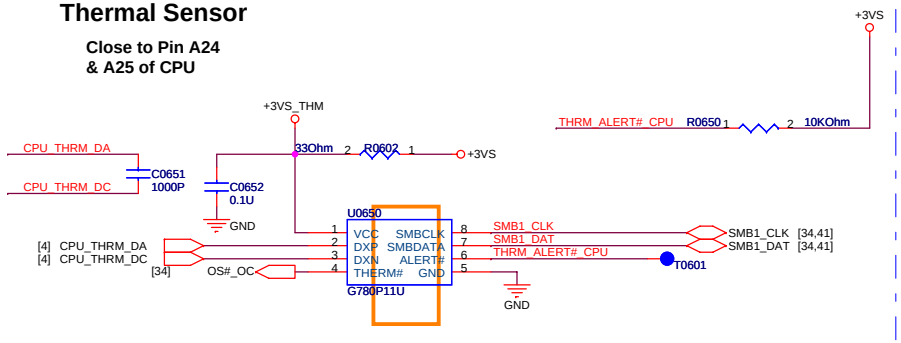




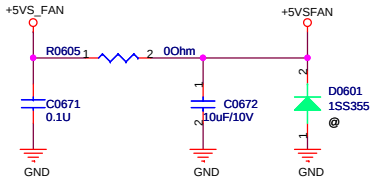
Enable: Turn OFF system
To EC(Internal Pull Hi)

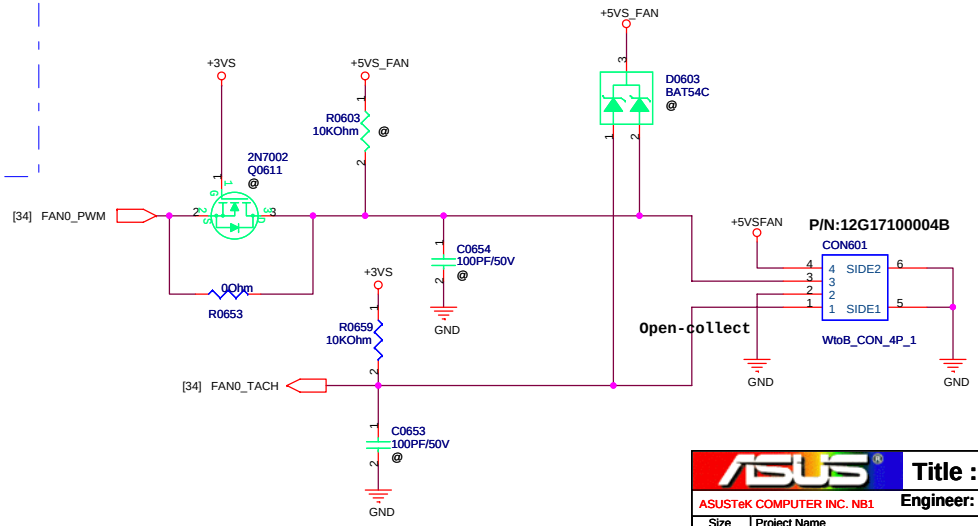
Thermal Sensor

Close to Pin A24
& A25 of CPU

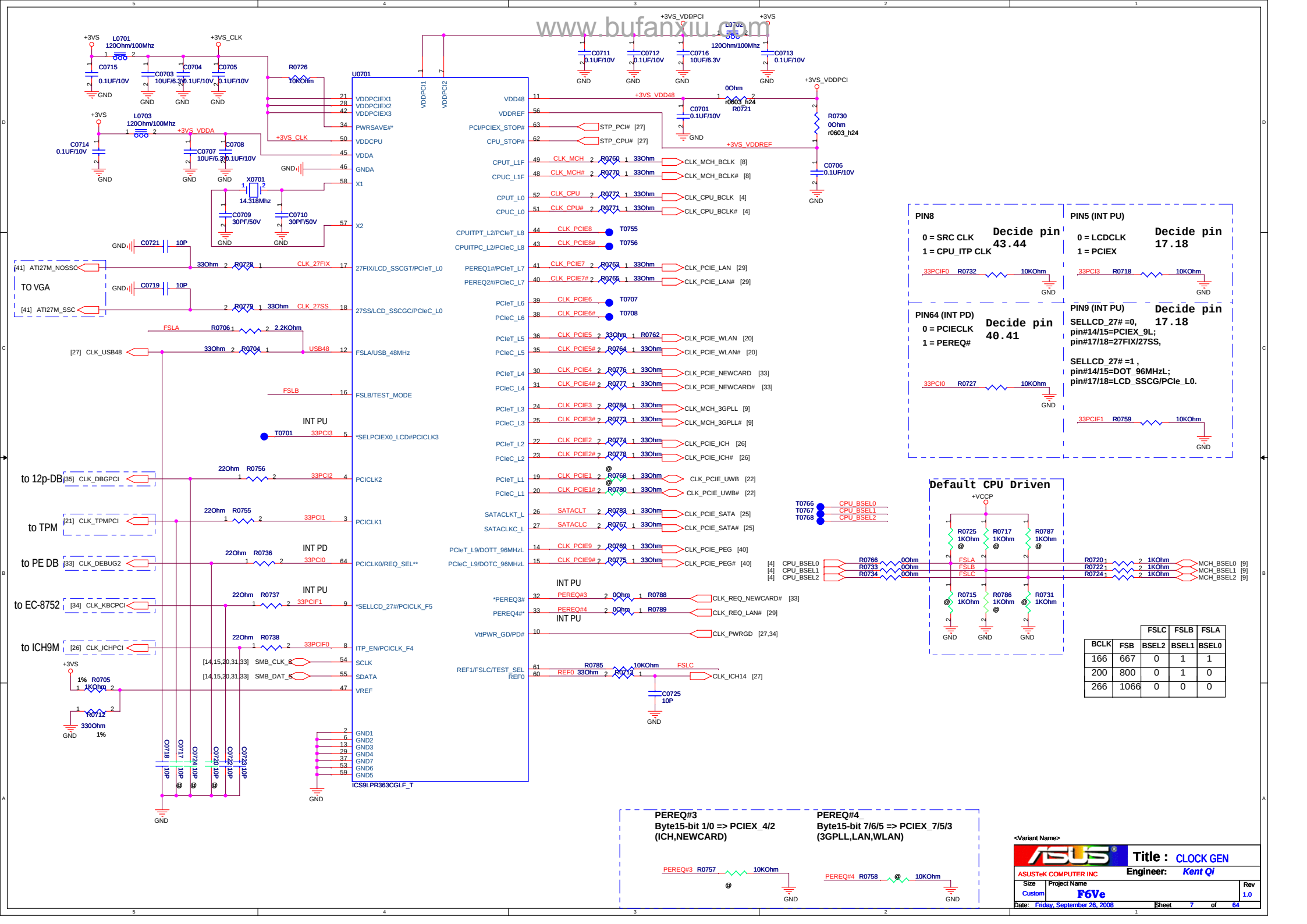


Slave address: 98h





ASUSTeK COMPUTER INC. NB1	Title : CAP,Thermal FAN	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 6 of 64	



BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

<Variant Name>

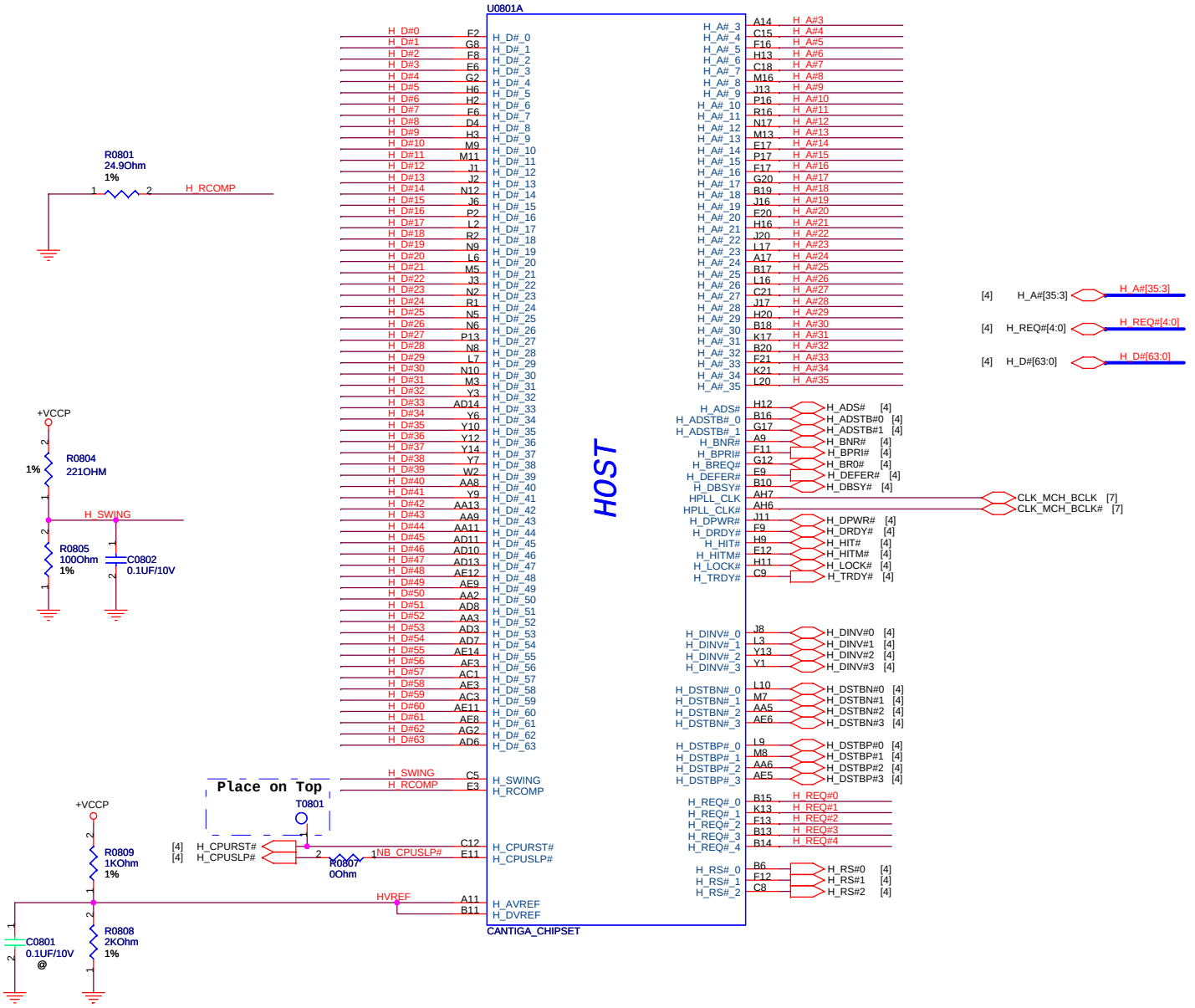
ASUSTeK COMPUTER INC

Title : CLOCK GEN

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 7 of 64



ASUSTeK COMPUTER INC. NB1	Title : Cantiga -- CPU (1)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 8 of 64	

U0801B

ME JTAG PORT
T0922 ME_JTAG_TCK
T0923 ME_JTAG_TDI
T0924 ME_JTAG_TDO
T0925 ME_JTAG_TMS

RSVD
M36 RSVD1
N36 RSVD2
R33 RSVD3
T33 RSVD4
AH9 RSVD5
AH10 RSVD6
AH12 RSVD7
AH13 RSVD8
K12 RSVD9
AL34 RSVD10
AK34 RSVD11
AN35 RSVD12
AM35 RSVD13
T24 RSVD14
B31 RSVD15
AJ6 RSVD16
M1 RSVD17
AY21 RSVD20
A47 RSVD21
BG23 RSVD22
BF23 RSVD23
BH18 RSVD24
BF18 RSVD25

DDR CONTROL/COMPENSATION
SA_CK_0 AP24 M_CLK_DDR0 [14]
SA_CK_1 AT21 M_CLK_DDR1 [14]
SB_CK_0 AV24 M_CLK_DDR2 [15]
SB_CK_1 AU20 M_CLK_DDR3 [15]
SA_CK#_0 AR24 M_CLK_DDR#0 [14]
SA_CK#_1 AR21 M_CLK_DDR#1 [14]
SB_CK#_0 AU24 M_CLK_DDR#2 [15]
SB_CK#_1 AV20 M_CLK_DDR#3 [15]
SA_CKE_0 BC28 M_CKE0 [14,16]
SA_CKE_1 AY28 M_CKE1 [14,16]
SB_CKE_0 AY36 M_CKE2 [15,16]
SB_CKE_1 BB36 M_CKE3 [15,16]
SA_CS#_0 BA17 M_CS#0 [14,16]
SA_CS#_1 AY16 M_CS#1 [14,16]
SB_CS#_0 AV16 M_CS#2 [15,16]
SB_CS#_1 AR13 M_CS#3 [15,16]
SA_ODT_0 BD17 M_ODT0 [14,16]
SA_ODT_1 AY17 M_ODT1 [14,16]
SB_ODT_0 BF15 M_ODT2 [15,16]
SB_ODT_1 AY13 M_ODT3 [15,16]
SM_RCOMP BG22 M_RCOMP 1 R0902 2 80.6Ohm 1%
SM_RCOMP# BH21 M_RCOMP# 1 R0903 2 80.6Ohm 1%
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42
SM_PWROK AR36
SM_REXT BF17 MCH_SM_REXT 499Ohm R0950 1%
SM_DRAMRST# BC36 T0963
C0969 0.01UF/16V
+1.8V
+VTT_REF

L_CTRL & L_DDC could NC or GND (Checklist R1.0)
SM_PWROK tie to GND for DDR2
SM_DRAMRST# :NC for DDR2 (checklist)

CLK
DPLL_REF_CLK B38
DPLL_REF_CLK# A38
DPLL_REF_SSCLK E41
DPLL_REF_SSCLK# F41
PEG_CLK E43 T0926 CLK_MCH_3GPLL [7]
PEG_CLK# E43 T0927 CLK_MCH_3GPLL# [7]

DMI
DMI_RXN_0 AE41 DMI_TXN0 [26]
DMI_RXN_1 AE37 DMI_TXN1 [26]
DMI_RXN_2 AE47 DMI_TXN2 [26]
DMI_RXN_3 AH39 DMI_TXN3 [26]
DMI_RXP_0 AE40 DMI_TXP0 [26]
DMI_RXP_1 AE38 DMI_TXP1 [26]
DMI_RXP_2 AE48 DMI_TXP2 [26]
DMI_RXP_3 AH40 DMI_TXP3 [26]
DMI_TXN_0 AE35 DMI_RXN0 [26]
DMI_TXN_1 AE43 DMI_RXN1 [26]
DMI_TXN_2 AE46 DMI_RXN2 [26]
DMI_TXN_3 AH42 DMI_RXN3 [26]
DMI_TXP_0 AD35 DMI_RXP0 [26]
DMI_TXP_1 AE44 DMI_RXP1 [26]
DMI_TXP_2 AF46 DMI_RXP2 [26]
DMI_TXP_3 AH43 DMI_RXP3 [26]

CFG
[7] MCH_BSEL0 T25 CFG_0
[7] MCH_BSEL1 R25 CFG_1
[7] MCH_BSEL2 P25 CFG_2
T0903 P20 CFG_3
T0902 P24 CFG_4
[13] MCH_CFG_5 C25 CFG_5
[13] MCH_CFG_6 N24 CFG_6
[13] MCH_CFG_7 M24 CFG_7
T0909 F21 CFG_8
[13] MCH_CFG_9 C23 CFG_9
[13] MCH_CFG_10 C24 CFG_10
T0908 N21 CFG_11
[13] MCH_CFG_12 P21 CFG_12
[13] MCH_CFG_13 T21 CFG_13
T0904 R20 CFG_14
T0933 M20 CFG_15
[13] MCH_CFG_16 L21 CFG_16
T0905 H21 CFG_17
T0910 P29 CFG_18
[13] MCH_CFG_19 R28 CFG_19
[13] MCH_CFG_20 T28 CFG_20

GRAPHICS VID
GFX_VID_0 B33 GFX_VID_0 1 T0950
GFX_VID_1 B32 GFX_VID_1 1 T0951
GFX_VID_2 G33 GFX_VID_2 1 T0952
GFX_VID_3 F33 GFX_VID_3 1 T0953
GFX_VID_4 E33 GFX_VID_4 1 T0954
GFX_VR_EN C34 GFX_VR_EN 1 T0906

PWR
[27] PMSYNC# R0968 0Ohm PMSYNC#_MCH R29 PM_SYNC#
[4,25,80] H_DPRSTP# B7 PM_DPRSTP#
PM_EXTTS#_0 N33 PM_EXT_TS#_0
PM_EXTTS#_1 P32 PM_EXT_TS#_1
[27,34,44] PM_PWROK R0913 0Ohm PM_PWROK_MCH AT40 PWROK
[26,40] PLT_RST# R0904 10KOhm AT11 RSTIN#
[4,6,25] H_THRMTRIP# T20 THERMTRIP#
[27,80] PM_DPRSLPVR R32 DPRSLPVR

ME
CL_CLK AH37 CL_CLK0 [27]
CL_DATA AH36 CL_DATA0 [27]
CL_PWROK AN36 CL_PWROK [27]
CL_RST# AJ35 CL_RST#0 [27]
CL_VREF AH34
CLPWROK must NOT assert Before RSMRSM# assert After PWROK assert
C0953 0.1UF/10V
R0917 1KOhm 1%
R0907 499Ohm 1%
DG,Checklist:500ohm CRB:511ohm

MISC
DDPC_CTRLCLK N28 DDPC_CTRLCLK 1 T0961
DDPC_CTRLDATA M28 DDPC_CTRLDATA 1 T0919
SDVO_CTRLCLK G36 SDVO_CTRLCLK 1 T0920
SDVO_CTRLDATA E36 SDVO_CTRLDATA 1 T0921 +3VS
CLKREQ# K36 R0966 10KOhm @
ICH_SYNC# H36 MCH_ICH_SYNC# [27] +VCCP
TSATN# B12 T0960 TSATN#
R0926 56Ohm
Checklist,DG:56 ohm PU if not used

HDA
HDA_BCLK B28
HDA_RST# B30
HDA_SDI B29
HDA_SDO C29
HDA_SYNC A28

NC
BG48 NC_1
BF48 NC_2
BD48 NC_3
BC48 NC_4
BH47 NC_5
BG47 NC_6
BE47 NC_7
BH46 NC_8
BF46 NC_9
BG45 NC_10
BH44 NC_11
BH43 NC_12
BH6 NC_13
BH5 NC_14
BG4 NC_15
BH3 NC_16
BF3 NC_17
BH2 NC_18
BG2 NC_19
BE2 NC_20
BG1 NC_21
BF1 NC_22
BD1 NC_23
BC1 NC_24
F1 NC_25

CANTIGA_CHIPSET

+3VS
R0908 10KOhm PM_EXTTS#_0 [14]
R0909 10KOhm PM_EXTTS#_1 [15]

+1.8V
R0901 1KOhm 1%
SM_RCOMP_VOH
C0958 0.01UF/16V
C0957 2.2UF/6.3V
R0911 3.01KOHM
SM_RCOMP_VOL
C0960 0.01UF/16V
C0959 2.2UF/6.3V
R0912 1KOhm 1%

U0801C

LVDS
L_BKLT_CTRL L32
L_BKLT_EN G32
L_CTRL_CLK M32
L_CTRL_DATA M33
L_DDC_CLK K33
L_DDC_DATA J33
LVDD_EN M29
LVDS_IBG C44
LVDS_VBG B43
LVDS_VREFH E37
LVDS_VREFL E38
LVDSA_CLK# C41
LVDSA_CLK C40
LVDSB_CLK# B37
LVDSB_CLK A37
LVDSA_DATA#_0 H47
LVDSA_DATA#_1 E46
LVDSA_DATA#_2 G40
LVDSA_DATA#_3 A40
LVDSA_DATA_0 H48
LVDSA_DATA_1 D45
LVDSA_DATA_2 E40
LVDSA_DATA_3 B40
LVDSB_DATA#_0 A41
LVDSB_DATA#_1 H38
LVDSB_DATA#_2 G37
LVDSB_DATA#_3 J37
LVDSB_DATA_0 B42
LVDSB_DATA_1 G38
LVDSB_DATA_2 E37
LVDSB_DATA_3 K37

TV
TVA_DAC F25
TVB_DAC H25
TVC_DAC K25
TV_RTN H24
TV_DCONSEL_0 C31
TV_DCONSEL_1 E32

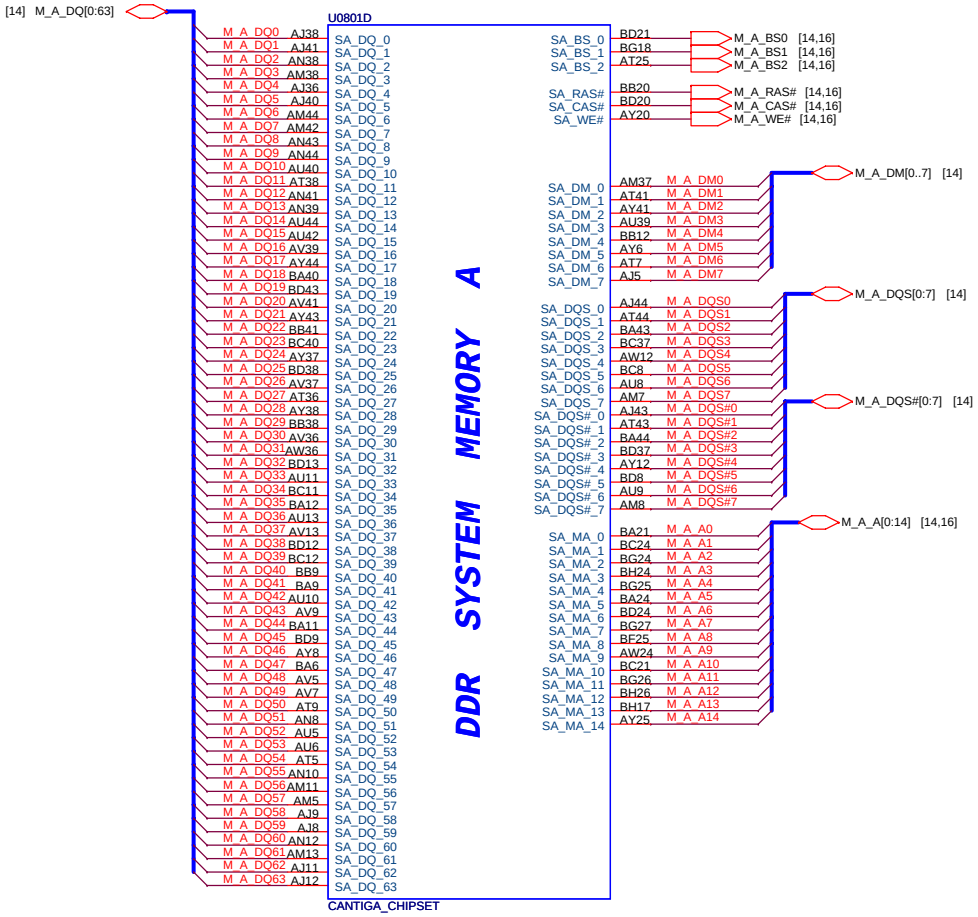
VGA
CRT_BLUE E28
CRT_GREEN G28
CRT_RED J28
CRT_IRTN G29
CRT_DDC_CLK H32
CRT_DDC_DATA J32
CRT_HSYNC J29
CRT_IVO_IREF E29
CRT_VSYNC L29

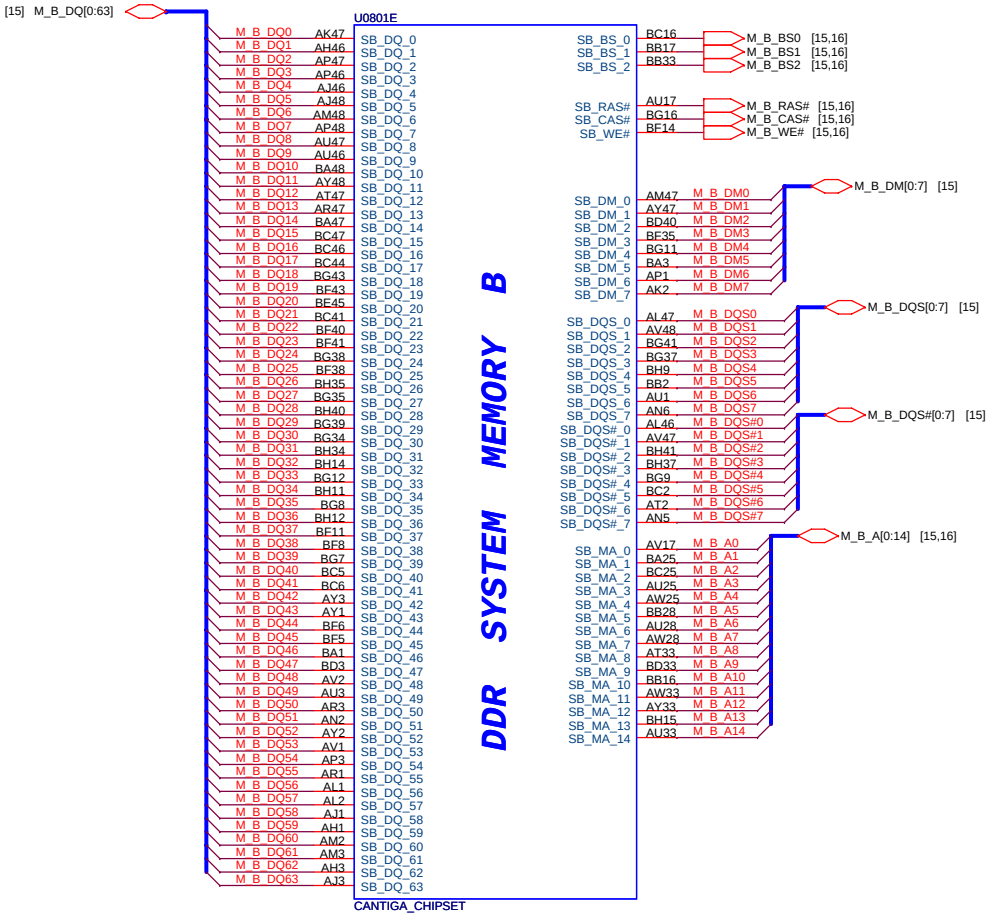
PCI-EXPRESS GRAPHICS
PEG_COMPI T37 PEG_COMP
PEG_COMPO T36
R0951 49.9Ohm 1%
+VCCP_PEG
PEG_RX#_0 H44 PCIENB_RXN0
PEG_RX#_1 J46 PCIENB_RXN1
PEG_RX#_2 L44 PCIENB_RXN2
PEG_RX#_3 L40 PCIENB_RXN3
PEG_RX#_4 N41 PCIENB_RXN4
PEG_RX#_5 P48 PCIENB_RXN5
PEG_RX#_6 N44 PCIENB_RXN6
PEG_RX#_7 T43 PCIENB_RXN7
PEG_RX#_8 U43
PEG_RX#_9 Y43
PEG_RX#_10 Y48
PEG_RX#_11 Y36
PEG_RX#_12 AA43
PEG_RX#_13 AD37
PEG_RX#_14 AC47
PEG_RX#_15 AD39
PEG_RX_0 H43 PCIENB_RXP0
PEG_RX_1 J44 PCIENB_RXP1
PEG_RX_2 L43 PCIENB_RXP2
PEG_RX_3 L41 PCIENB_RXP3
PEG_RX_4 N40 PCIENB_RXP4
PEG_RX_5 P47 PCIENB_RXP5
PEG_RX_6 N43 PCIENB_RXP6
PEG_RX_7 T42 PCIENB_RXP7
PEG_RX_8 U42
PEG_RX_9 Y42
PEG_RX_10 W47
PEG_RX_11 Y37
PEG_RX_12 AA42
PEG_RX_13 AD36
PEG_RX_14 AC48
PEG_RX_15 AD40
PEG_TX#_0 J41 PCIENB_TXN0 C0901 0.1UF/10V PCIEG_RXN0
PEG_TX#_1 M46 PCIENB_TXN1 C0902 0.1UF/10V PCIEG_RXN1
PEG_TX#_2 M47 PCIENB_TXN2 C0903 0.1UF/10V PCIEG_RXN2
PEG_TX#_3 M40 PCIENB_TXN3 C0904 0.1UF/10V PCIEG_RXN3
PEG_TX#_4 M42 PCIENB_TXN4 C0905 0.1UF/10V PCIEG_RXN4
PEG_TX#_5 R48 PCIENB_TXN5 C0906 0.1UF/10V PCIEG_RXN5
PEG_TX#_6 N38 PCIENB_TXN6 C0907 0.1UF/10V PCIEG_RXN6
PEG_TX#_7 T40 PCIENB_TXN7 C0908 0.1UF/10V PCIEG_RXN7
PEG_TX#_8 U37
PEG_TX#_9 U40
PEG_TX#_10 Y40
PEG_TX#_11 AA46
PEG_TX#_12 AA37
PEG_TX#_13 AA40
PEG_TX#_14 AD43
PEG_TX#_15 AC46
PEG_TX_0 J42 PCIENB_TXP0 C0917 0.1UF/10V PCIEG_RXP0
PEG_TX_1 L46 PCIENB_TXP1 C0918 0.1UF/10V PCIEG_RXP1
PEG_TX_2 M48 PCIENB_TXP2 C0919 0.1UF/10V PCIEG_RXP2
PEG_TX_3 M39 PCIENB_TXP3 C0920 0.1UF/10V PCIEG_RXP3
PEG_TX_4 M43 PCIENB_TXP4 C0921 0.1UF/10V PCIEG_RXP4
PEG_TX_5 R47 PCIENB_TXP5 C0922 0.1UF/10V PCIEG_RXP5
PEG_TX_6 N37 PCIENB_TXP6 C0923 0.1UF/10V PCIEG_RXP6
PEG_TX_7 T39 PCIENB_TXP7 C0924 0.1UF/10V PCIEG_RXP7
PEG_TX_8 U36
PEG_TX_9 U39
PEG_TX_10 Y39
PEG_TX_11 Y46
PEG_TX_12 AA36
PEG_TX_13 AA39
PEG_TX_14 AD42
PEG_TX_15 AD46

CANTIGA_CHIPSET

PCIENB_RXN[0..7] [40]
PCIENB_RXP[0..7] [40]
PCIEG_RXN[0..7] [40]
PCIEG_RXP[0..7] [40]

Title :	Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB1	Engineer: Kent Qi
Size: Custom	Project Name: F6Ve
Rev:	1.0
Date: Friday, September 26, 2008	Sheet 9 of 64





ASUSTeK COMPUTER INC. NB1	Title : Cantiga--DDR2 (3)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 10 of 64	

+1.8V_GMCH

2.6A for DDR2 667
3A for DDR2 800

U0801G

VCC_SM_1 … VCC_SM_35 (AP33, AN33, BH32, BG32, BF32, BD32, BC32, BB32, BA32, AY32, AW32, AV32, AU32, AT32, AR32, AP32, AN32, BH31, BG31, BF31, BG30, BH29, BG29, BF29, BD29, BC29, BB29, BA29, AY29, AW29, AV29, AU29, AT29, AR29, AP29)

VCC SM POWER

Confirm by Intel
TINNA Confirm.

T1103 T1104 T1105 T1106 T1107 T1108 T1109

VCC_SM_36/NC (BA36) … VCC_SM_42/NC (AT13)

VCC_AXG_1 … VCC_AXG_42 (Y26, AE25, AB25, AA25, AE24, AC24, AA24, Y24, AE23, AC23, AB23, AA23, AJ21, AG21, AE21, AC21, AA21, Y21, AH20, AF20, AE20, AC20, AB20, AA20, T17, T16, AM15, AL15, AE15, AJ15, AH15, AG15, AF15, AB15, AA15, Y15, V15, U15, AN14, AM14, U14, T14)

VCC GFX NCTF

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60 (W28, V28, W26, V26, W25, V25, W24, V24, W23, V23, AM21, AL21, AK21, W21, V21, U21, AM20, AK20, W20, U20, AM19, AL19, AK19, AJ19, AH19, AG19, AF19, AE19, AB19, AA19, Y19, W19, V19, U19, AM17, AK17, AH17, AG17, AF17, AE17, AC17, AB17, Y17, W17, V17, AM16, AL16, AK16, AJ16, AH16, AG16, AF16, AE16, AC16, AB16, AA16, Y16, W16, V16, U16)

VCC GFX

VCC_AXG_1 … VCC_AXG_42

Need to check

R1105 0Ohm @ VCC_AXG_SENSE AJ14
R1106 0Ohm @ VSS_AXG_SENSE AH14

VCC_AXG_SENSE
VSS_AXG_SENSE

Route VCC_AXG_SENSE and
VSS_AXG_SENSE differentially.

VCC SM LF

VCC_SM_LF1 … VCC_SM_LF7 (AV44, BA37, AM40, AV21, AY5, AM10, BB13)

C1120 0.1UF/10V
C1121 0.1UF/10V
C1122 0.22UF/6.3V
C1123 0.22UF/6.3V
C1124 0.47UF/6.3V
C1126 1UF/6.3V c0402
C1101 1UF/6.3V c0402

CANTIGA_CHIPSET

+VCCP
2MM_OPEN_5MIL
JP1103 @
2.178A(W ME)
1.67A (W/O ME)

CE1101 220UF/4V
C1102 10UF/6.3V
C1103 0.22UF/6.3V
C1104 0.22UF/6.3V
C1105 0.1UF/10V

+VCC_GMCH

U0801F

VCC_1 … VCC_35 (AG34, AC34, AB34, AA34, Y34, V34, U34, AM33, AK33, AJ33, AG33, AF33, AE33, AC33, AA33, Y33, W33, V33, U33, AH28, AF28, AC28, AA28, AJ26, AG26, AE26, AC26, AH25, AG25, AF25, AG24, AJ23, AH23, AF23, T32)

VCC CORE

2.6A for DDR2 667
3A for DDR2 800

+1.8V
2MM_OPEN_5MIL
JP1104@

CE1102 220UF/4V
C1111 10UF/6.3V
C1112 10UF/6.3V
C1113 0.1UF/10V

+1.8V_GMCH

POWER

VCC_NCTF_1 … VCC_NCTF_44 (AM32, AL32, AK32, AJ32, AH32, AG32, AE32, AC32, AA32, Y32, W32, U32, AM30, AL30, AK30, AH30, AG30, AF30, AE30, AC30, AB30, AA30, Y30, W30, V30, U30, AL29, AK29, AJ29, AH29, AG29, AE29, AC29, AA29, Y29, W29, V29, AL28, AK28, AL26, AK26, AK25, AK24, AK23)

VCC NCTF

CANTIGA_CHIPSET

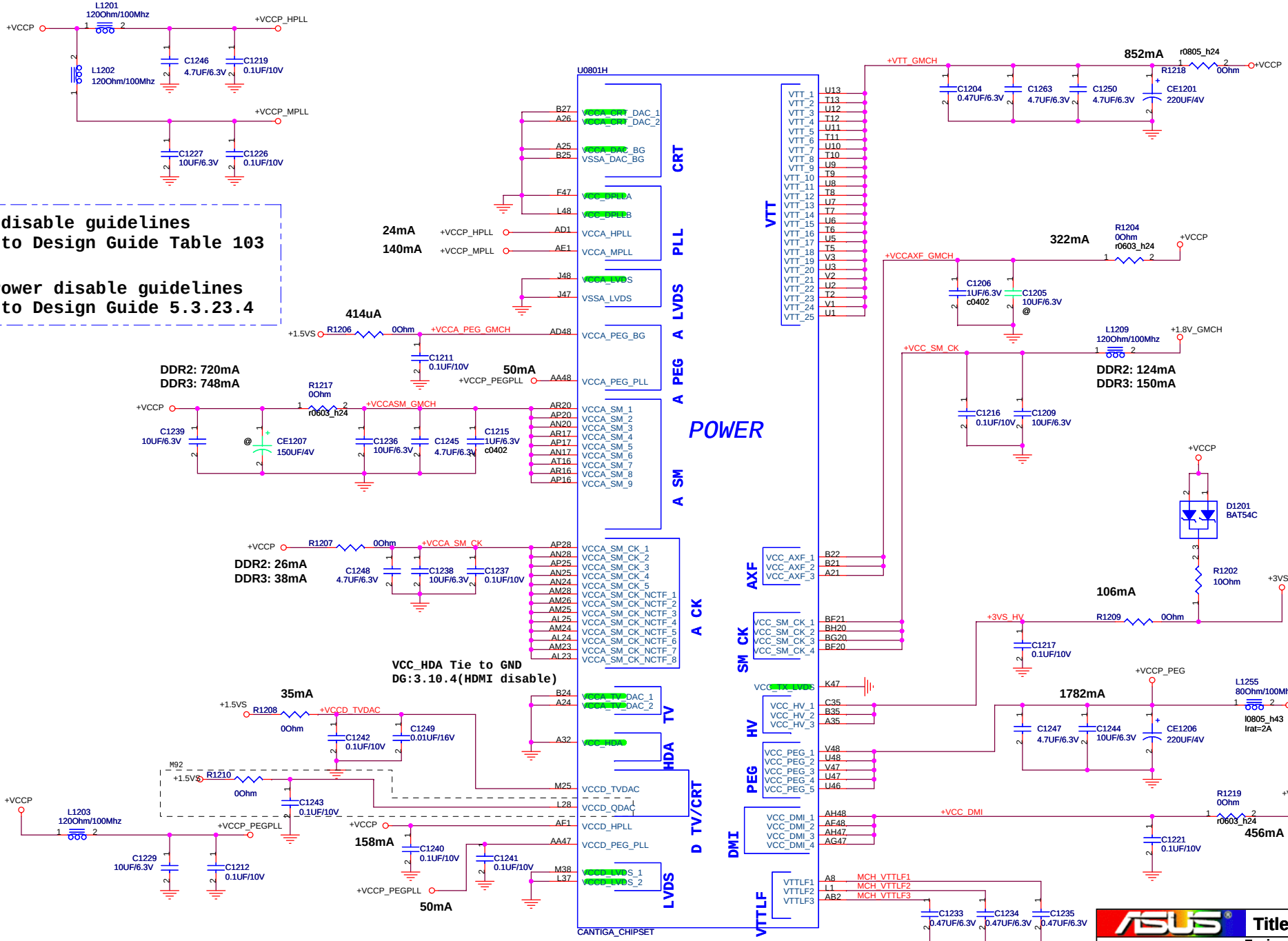
ASUSTeK COMPUTER INC. NB1

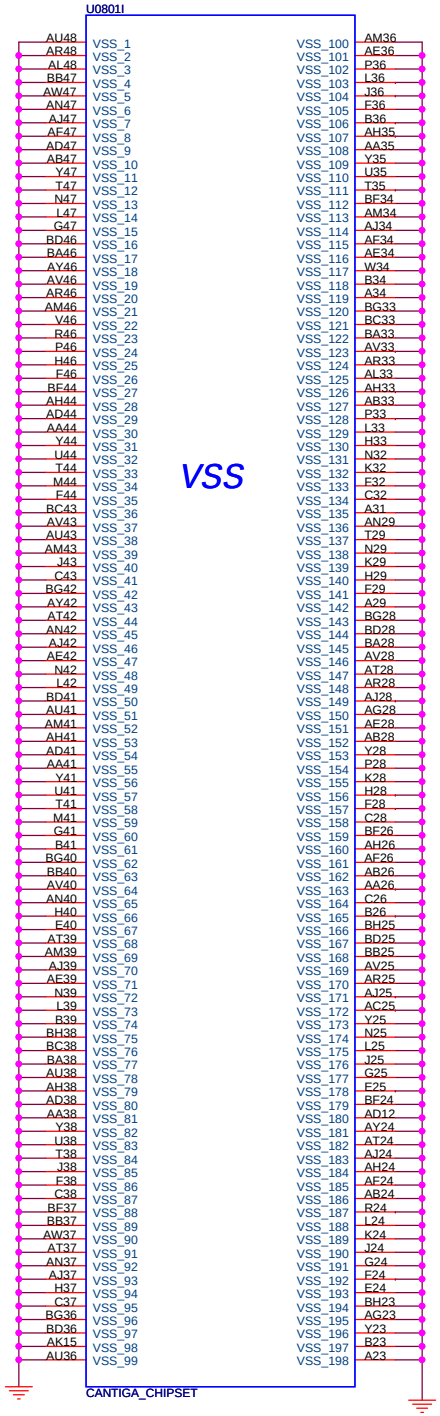
Title : Cantiga--POWER (4)

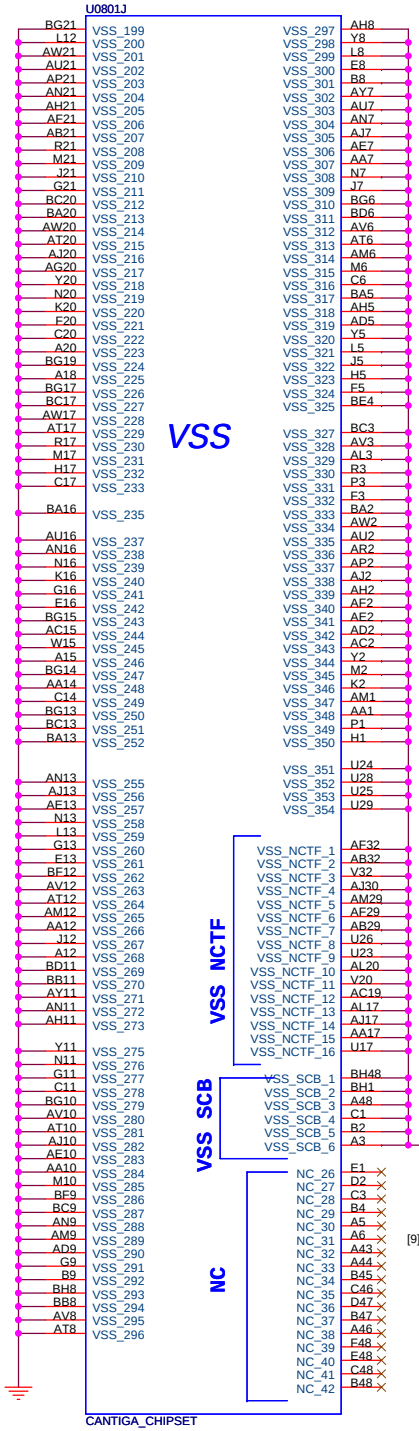
Engineer: Kent Qi

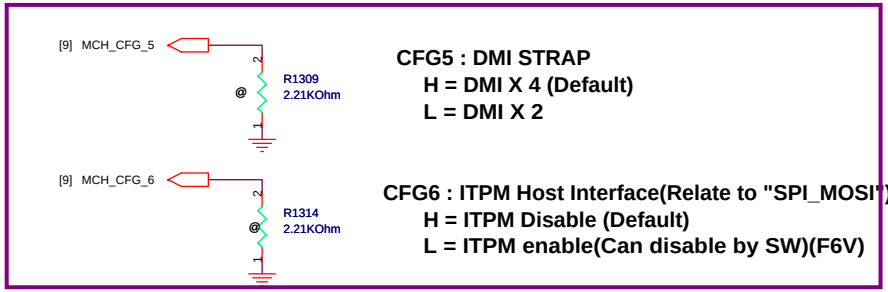
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 11 of 64



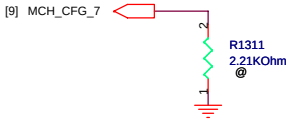




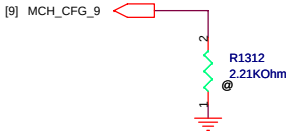


CFG5 : DMI STRAP
- H = DMI X 4 (Default)
- L = DMI X 2

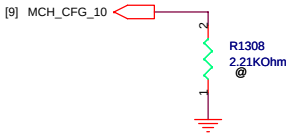
CFG6 : ITPM Host Interface(Relate to "SPI_MOSI")
- H = ITPM Disable (Default)
- L = ITPM enable(Can disable by SW)(F6V)



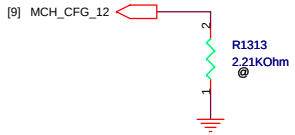
CFG7 : Intel ME Crypto Strap
- H = With confidentiality (Default)
- L = Without confidentiality



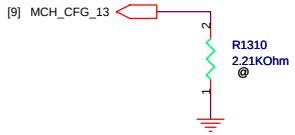
CFG9 : PCIE Graphic Lane Reverse
- H = Normal (Default)
- L = Lanes Reverse



CFG10 : PCIE Loopback
- H = Disable (Default)
- L = Enable

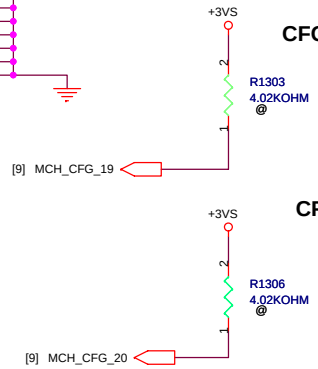


CFG12 : ALL-Z Mode
- H =Disable (Default)
- L = Enable



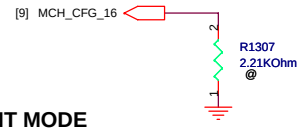
CFG13 : XOR Mode
- H = Disable (Default)
- L = Enable

CFG [13:12] : XOR/ALL-Z
- 00 = Reserved
- 01= XOR Mode Enabled
- 10= All-Z Mode Enabled
- 11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
- H =DMI Lane Reversal
- L = Normal (Default)

CFG20 : SDVO/PCIE CONCURRENT MODE
- L = Only Digital display port or PCIE is Operational (Default)
- H = Digital display port and PCIE are operating simultaneously via the PEG port



CFG16 : FSB Dynamic ODT
- H =Enable (Default)
- L = Disable

Title : Cantiga-GND		
ASUSTeK COMPUTER INC. NB1	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 13 of 64	

[10] M_A_DQ[0..63] M_A_DQ[0..63]

P/N : 12G025022004

M_CLK_DDR0
C1401 @ 10P
M_CLK_DDR#0
PLACE NEAR SO-DIMM_0
M_CLK_DDR1
C1402 @ 10P
M_CLK_DDR#1

[10,16] M_A_A[0..13]

CON140A

M_A_A0	102	A0	DQ0	5	M_A_DQ4
M_A_A1	101	A1	DQ1	7	M_A_DQ1
M_A_A2	100	A2	DQ2	17	M_A_DQ6
M_A_A3	99	A3	DQ3	19	M_A_DQ2
M_A_A4	98	A4	DQ4	4	M_A_DQ5
M_A_A5	97	A5	DQ5	6	M_A_DQ0
M_A_A6	94	A6	DQ6	14	M_A_DQ3
M_A_A7	92	A7	DQ7	16	M_A_DQ7
M_A_A8	93	A8	DQ8	23	M_A_DQ13
M_A_A9	91	A9	DQ9	25	M_A_DQ12
M_A_A10	105	A10/AP	DQ10	35	M_A_DQ10
M_A_A11	90	A11	DQ11	37	M_A_DQ11
M_A_A12	89	A12	DQ12	20	M_A_DQ9
M_A_A13	116	A13	DQ13	22	M_A_DQ8
[10,16] M_A_A14	86	A14	DQ14	36	M_A_DQ15
	84	A15	DQ15	38	M_A_DQ14
[10,16] M_A_BS2	85	A16_BA2	DQ16	43	M_A_DQ20
			DQ17	45	M_A_DQ16
[10,16] M_A_BS0	107	BA0	DQ18	55	M_A_DQ17
[10,16] M_A_BS1	106	BA1	DQ19	57	M_A_DQ22
[9,16] M_CS#0	110	S0#	DQ20	44	M_A_DQ21
[9,16] M_CS#1	115	S1#	DQ21	46	M_A_DQ19
[9] M_CLK_DDR0	30	CK0	DQ22	56	M_A_DQ18
[9] M_CLK_DDR#0	32	CK0#	DQ23	58	M_A_DQ23
[9] M_CLK_DDR1	164	CK1	DQ24	61	M_A_DQ28
[9] M_CLK_DDR#1	166	CK1#	DQ25	63	M_A_DQ25
[9,16] M_CKE0	79	CKE0	DQ26	73	M_A_DQ29
[9,16] M_CKE1	80	CKE1	DQ27	75	M_A_DQ24
[10,16] M_A_CAS#	113	CAS#	DQ28	62	M_A_DQ31
[10,16] M_A_RAS#	108	RAS#	DQ29	64	M_A_DQ30
[10,16] M_A_WE#	109	WE#	DQ30	74	M_A_DQ26
	198	SA0	DQ31	76	M_A_DQ27
[7,15,20,31,33] SMB_CLK_S	200	SA1	DQ32	123	M_A_DQ37
[7,15,20,31,33] SMB_DAT_S	197	SCL	DQ33	125	M_A_DQ36
	195	SDA	DQ34	135	M_A_DQ38
			DQ35	137	M_A_DQ35
[9,16] M_ODT0	114	ODT0	DQ36	124	M_A_DQ32
[9,16] M_ODT1	119	ODT1	DQ37	126	M_A_DQ39
[10] M_A_DM[0..7]			DQ38	134	M_A_DQ33
M_A_DM0	10	DM0	DQ39	136	M_A_DQ34
M_A_DM1	26	DM1	DQ40	141	M_A_DQ47
M_A_DM2	52	DM2	DQ41	143	M_A_DQ42
M_A_DM3	67	DM3	DQ42	151	M_A_DQ43
M_A_DM4	130	DM4	DQ43	153	M_A_DQ46
M_A_DM5	147	DM5	DQ44	140	M_A_DQ45
M_A_DM6	170	DM6	DQ45	142	M_A_DQ44
M_A_DM7	185	DM7	DQ46	152	M_A_DQ40
			DQ47	154	M_A_DQ41
[10] M_A_DQS[0..7]			DQ48	157	M_A_DQ49
M_A_DQS0	13	DQS0	DQ49	159	M_A_DQ54
M_A_DQS1	31	DQS1	DQ50	173	M_A_DQ51
M_A_DQS2	51	DQS2	DQ51	175	M_A_DQ50
M_A_DQS3	70	DQS3	DQ52	158	M_A_DQ53
M_A_DQS4	131	DQS4	DQ53	160	M_A_DQ48
M_A_DQS5	148	DQS5	DQ54	174	M_A_DQ52
M_A_DQS6	169	DQS6	DQ55	176	M_A_DQ55
M_A_DQS7	188	DQS7	DQ56	179	M_A_DQ57
[10] M_A_DQS#[0..7]			DQ57	181	M_A_DQ61
M_A_DQS#0	11	DQS#0	DQ58	189	M_A_DQ63
M_A_DQS#1	29	DQS#1	DQ59	191	M_A_DQ58
M_A_DQS#2	49	DQS#2	DQ60	180	M_A_DQ60
M_A_DQS#3	68	DQS#3	DQ61	182	M_A_DQ59
M_A_DQS#4	129	DQS#4	DQ62	192	M_A_DQ62
M_A_DQS#5	146	DQS#5	DQ63	194	M_A_DQ56
M_A_DQS#6	167	DQS#6			
M_A_DQS#7	186	DQS#7			

SWAP SWAP SWAP SWAP SWAP SWAP SWAP SWAP

GND

DDR2_DIMM_200P
DDR2 DIMM 200P,1.8V,H:4mm,STD
12G025022004

+1.8V
C1409 C1410 C1411 C1412 C1413 1UF/6.3V
GND

+3VS
C1403 0.1U
C1415 @ 2.2UF/6.3V
[9] PM_EXTTS#_0 R1410 0Ohm @
+VTT_REF
C1414 2.2UF/6.3V C1404 0.1U
GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V
C1405 C1406 C1407 C1408 0.1UF/16V
GND

CON140B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

GND GND

DDR2_DIMM_200P
DDR2 DIMM 200P,1.8V,H:4mm,STD
12G025022004

<Variant Name>

Title : DDR2 SO-DIMM 0

ASUSTeK COMPUTER INC

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 14 of 64

[10] M_B_DQ[0..63]

[10,16] M_B_A[0..13]

P/N : 12G025C22004

CON150A

PLACE NEAR SO-DIMM_0

M_CLK_DDR2 — C1501 @ 10P — M_CLK_DDR#2

M_CLK_DDR3 — C1502 @ 10P — M_CLK_DDR#3

+3VS — R1515 10KOhm — GND

M_B_A0	102	A0	DQ0	5	M_B_DQ5
M_B_A1	101	A1	DQ1	7	M_B_DQ0
M_B_A2	100	A2	DQ2	17	M_B_DQ6
M_B_A3	99	A3	DQ3	19	M_B_DQ2
M_B_A4	98	A4	DQ4	4	M_B_DQ1
M_B_A5	97	A5	DQ5	6	M_B_DQ4
M_B_A6	94	A6	DQ6	14	M_B_DQ3
M_B_A7	92	A7	DQ7	16	M_B_DQ7
M_B_A8	93	A8	DQ8	23	M_B_DQ13
M_B_A9	91	A9	DQ9	25	M_B_DQ12
M_B_A10	105	A10/AP	DQ10	35	M_B_DQ11
M_B_A11	90	A11	DQ11	37	M_B_DQ14
M_B_A12	89	A12	DQ12	20	M_B_DQ9
M_B_A13	116	A13	DQ13	22	M_B_DQ8
[10,16] M_B_A14	86	A14	DQ14	36	M_B_DQ10
	84	A15	DQ15	38	M_B_DQ15
[10,16] M_B_BS2	85	A16_BA2	DQ16	43	M_B_DQ16
			DQ17	45	M_B_DQ20
[10,16] M_B_BS0	107	BA0	DQ18	55	M_B_DQ23
[10,16] M_B_BS1	106	BA1	DQ19	57	M_B_DQ19
[9,16] M_CS#2	110	S0#	DQ20	44	M_B_DQ18
[9,16] M_CS#3	115	S1#	DQ21	46	M_B_DQ17
[9] M_CLK_DDR2	30	CK0	DQ22	56	M_B_DQ21
[9] M_CLK_DDR#2	32	CK0#	DQ23	58	M_B_DQ22
[9] M_CLK_DDR3	164	CK1	DQ24	61	M_B_DQ29
[9] M_CLK_DDR#3	166	CK1#	DQ25	63	M_B_DQ28
[9,16] M_CKE2	79	CKE0	DQ26	73	M_B_DQ26
[9,16] M_CKE3	80	CKE1	DQ27	75	M_B_DQ31
[10,16] M_B_CAS#	113	CAS#	DQ28	62	M_B_DQ24
[10,16] M_B_RAS#	108	RAS#	DQ29	64	M_B_DQ25
[10,16] M_B_WE#	109	WE#	DQ30	74	M_B_DQ27
	198	SA0	DQ31	76	M_B_DQ30
	200	SA1	DQ32	123	M_B_DQ34
[7,14,20,31,33] SMB_CLK_S	197	SCL	DQ33	125	M_B_DQ32
[7,14,20,31,33] SMB_DAT_S	195	SDA	DQ34	135	M_B_DQ35
			DQ35	137	M_B_DQ39
[9,16] M_ODT2	114	ODT0	DQ36	124	M_B_DQ33
[9,16] M_ODT3	119	ODT1	DQ37	126	M_B_DQ36
[10] M_B_DM[0..7]			DQ38	134	M_B_DQ37
M_B_DM0	10	DM0	DQ39	136	M_B_DQ38
M_B_DM1	26	DM1	DQ40	141	M_B_DQ45
M_B_DM2	52	DM2	DQ41	143	M_B_DQ47
M_B_DM3	67	DM3	DQ42	151	M_B_DQ46
M_B_DM4	130	DM4	DQ43	153	M_B_DQ42
M_B_DM5	147	DM5	DQ44	140	M_B_DQ44
M_B_DM6	170	DM6	DQ45	142	M_B_DQ41
M_B_DM7	185	DM7	DQ46	152	M_B_DQ40
			DQ47	154	M_B_DQ43
[10] M_B_DQS[0..7]				157	M_B_DQ53
M_B_DQS0	13	DQS0	DQ48	159	M_B_DQ49
M_B_DQS1	31	DQS1	DQ49	173	M_B_DQ55
M_B_DQS2	51	DQS2	DQ50	175	M_B_DQ51
M_B_DQS3	70	DQS3	DQ51	158	M_B_DQ52
M_B_DQS4	131	DQS4	DQ52	160	M_B_DQ48
M_B_DQS5	148	DQS5	DQ53	174	M_B_DQ50
M_B_DQS6	169	DQS6	DQ54	176	M_B_DQ54
M_B_DQS7	188	DQS7	DQ55	179	M_B_DQ57
[10] M_B_DQS#[0..7]					
M_B_DQS#0	11	DQS#0	DQ56	181	M_B_DQ56
M_B_DQS#1	29	DQS#1	DQ57	189	M_B_DQ63
M_B_DQS#2	49	DQS#2	DQ58	191	M_B_DQ62
M_B_DQS#3	68	DQS#3	DQ59	180	M_B_DQ60
M_B_DQS#4	129	DQS#4	DQ60	182	M_B_DQ61
M_B_DQS#5	146	DQS#5	DQ61	192	M_B_DQ59
M_B_DQS#6	167	DQS#6	DQ62	194	M_B_DQ58
M_B_DQS#7	186	DQS#7	DQ63		

SWAP

DDR2_DIMM_200P

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004

+1.8V — C1519 C1520 C1521 C1522 C1523 1UF/6.3V — GND

+3VS — C1503 0.1U — GND

C1506 2.2UF/6.3V @ — GND

[9] PM_EXTTS#_1 — R1510 0Ohm @

+VTT_REF — C1504 2.2UF/6.3V — C1505 0.1U — GND

Layout Note: Place these Caps near SO DIMM 1

+1.8V — C1517 C1518 C1515 C1516 0.1UF/16V — GND

CON150B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR2_DIMM_200P

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004

<Variant Name>

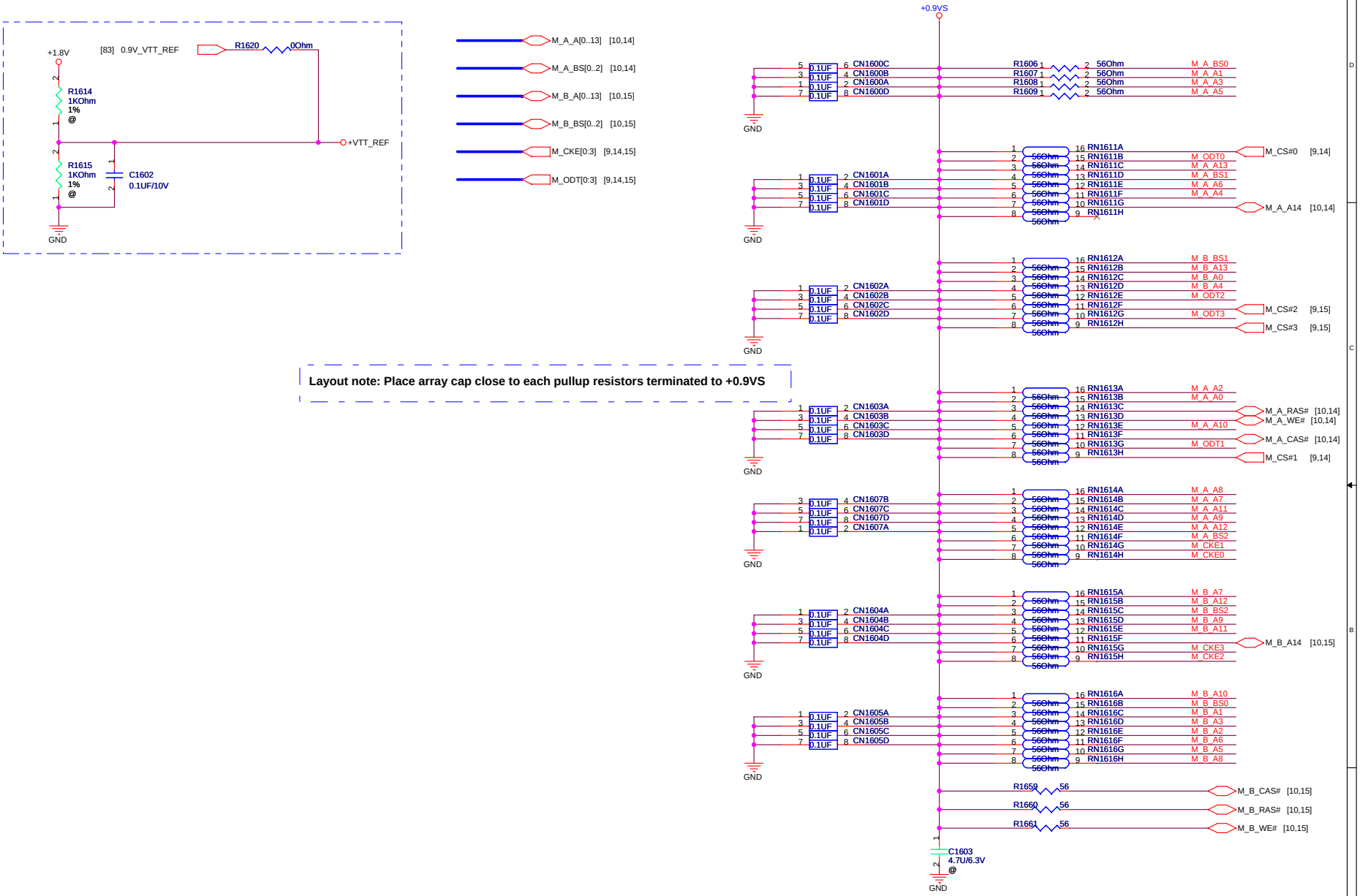
ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM_1

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 15 of 64

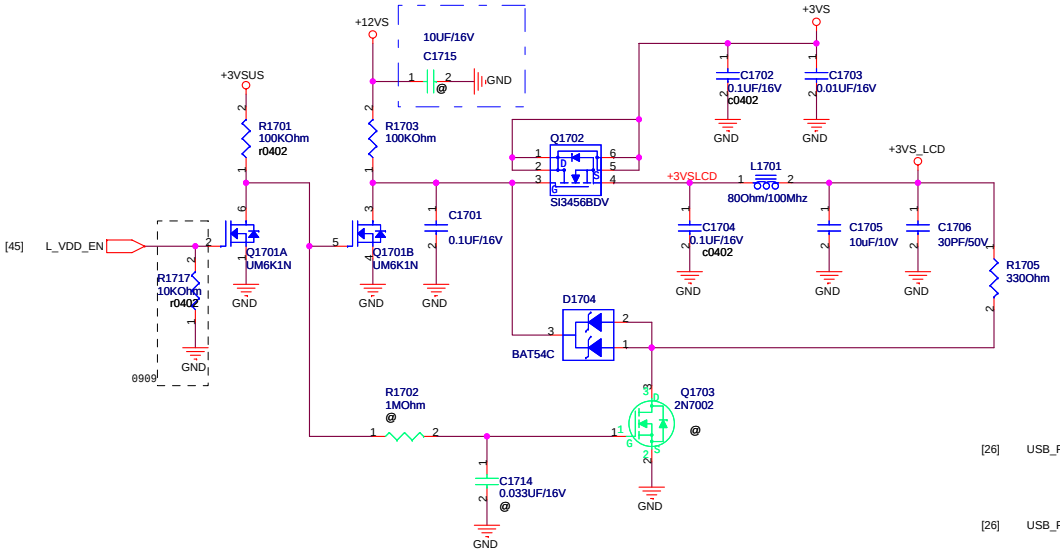


<Variant Name>

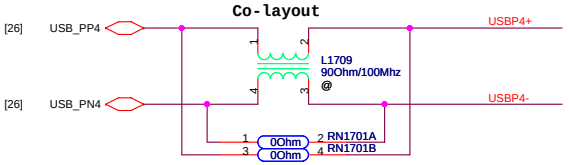
ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 16 of 64	

LCD Power

C1715 for EMI Request

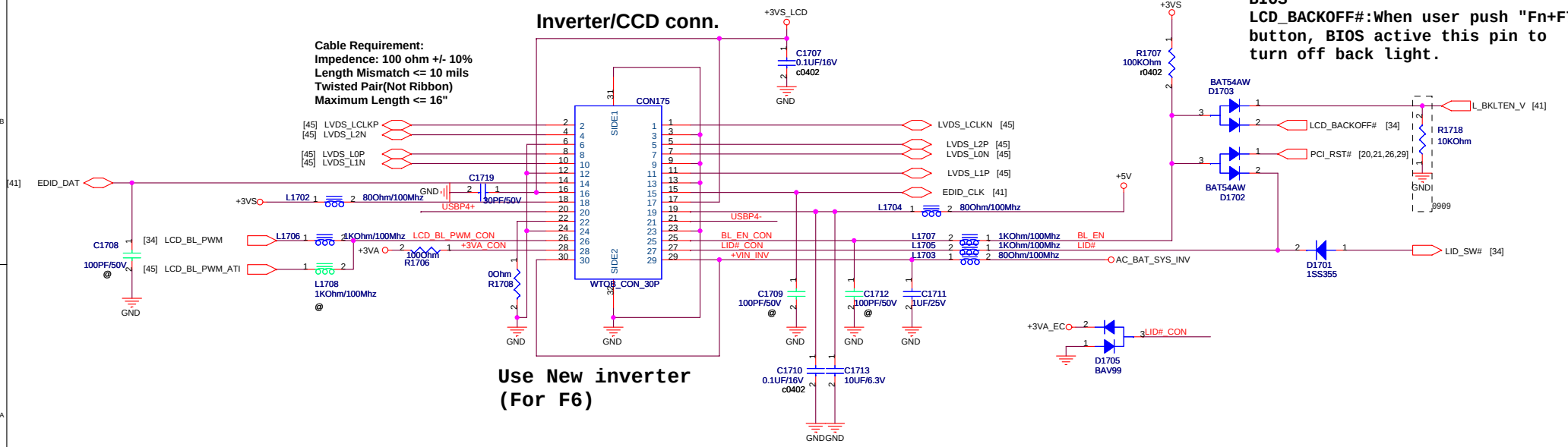


Co-layout



Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

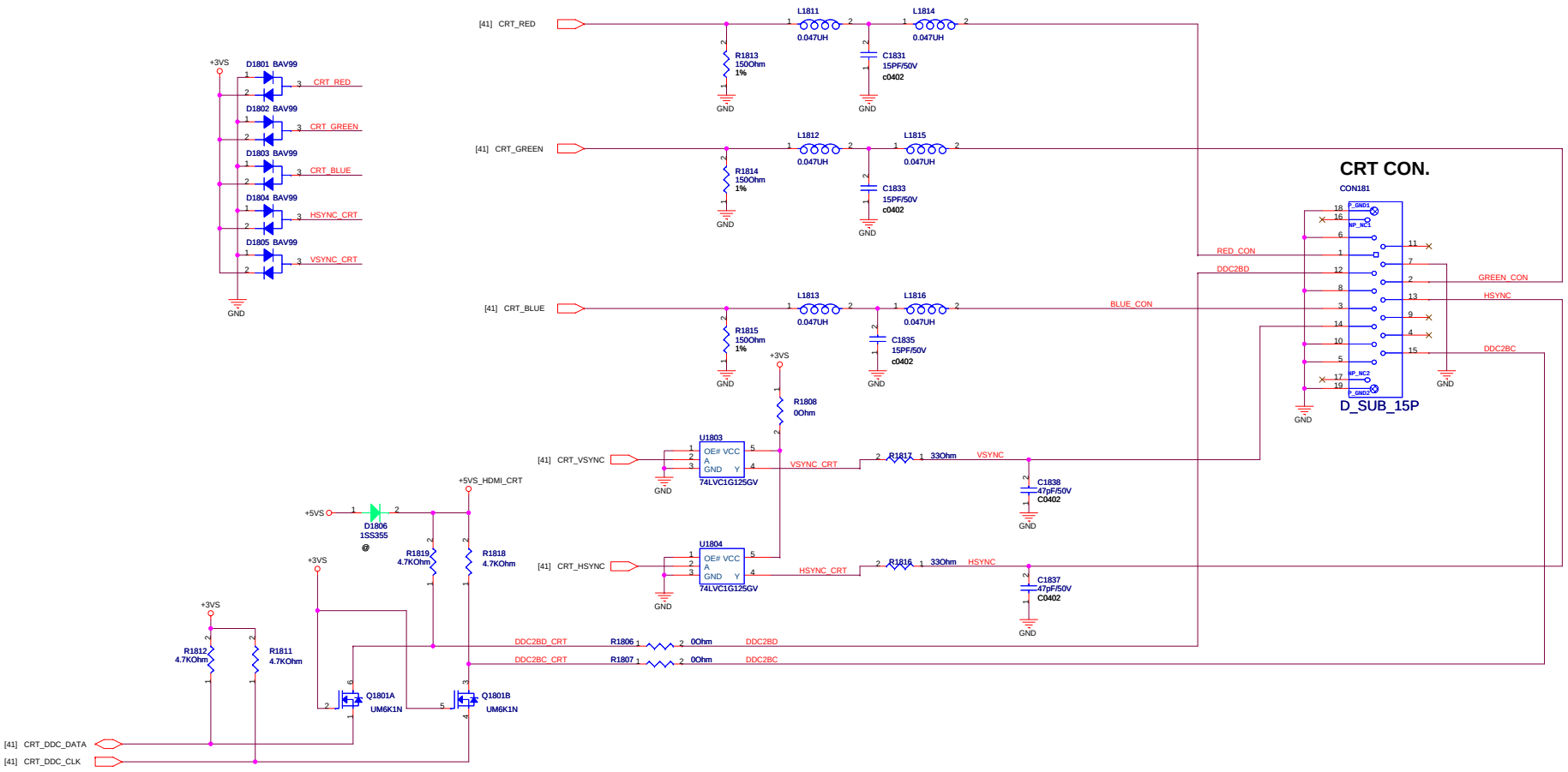


Use New inverter
(For F6)

BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 17 of 64	



<Variant Name>

ASUSTeK COMPUTER INC.

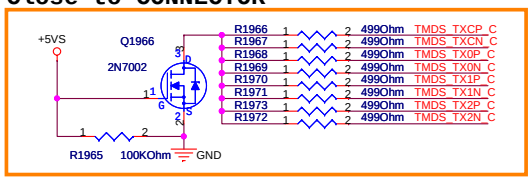
Title : CRT

Engineer: Kent Qi

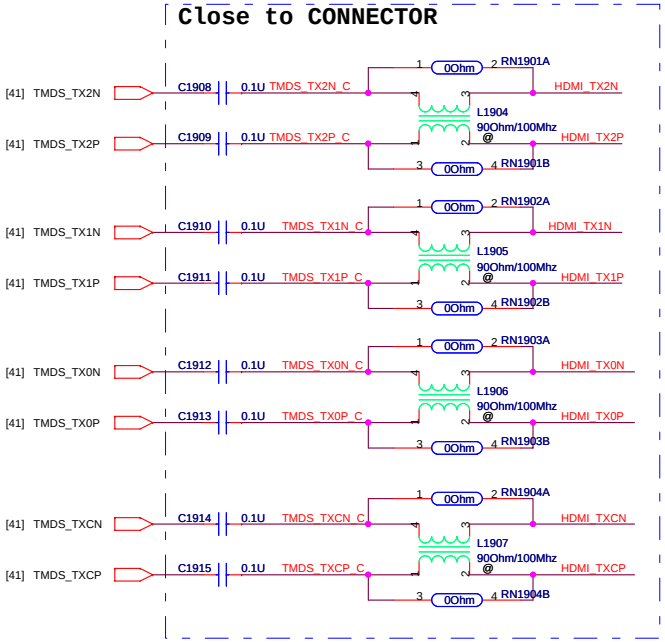
Size	Project Name	Rev
C	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 18 of 64

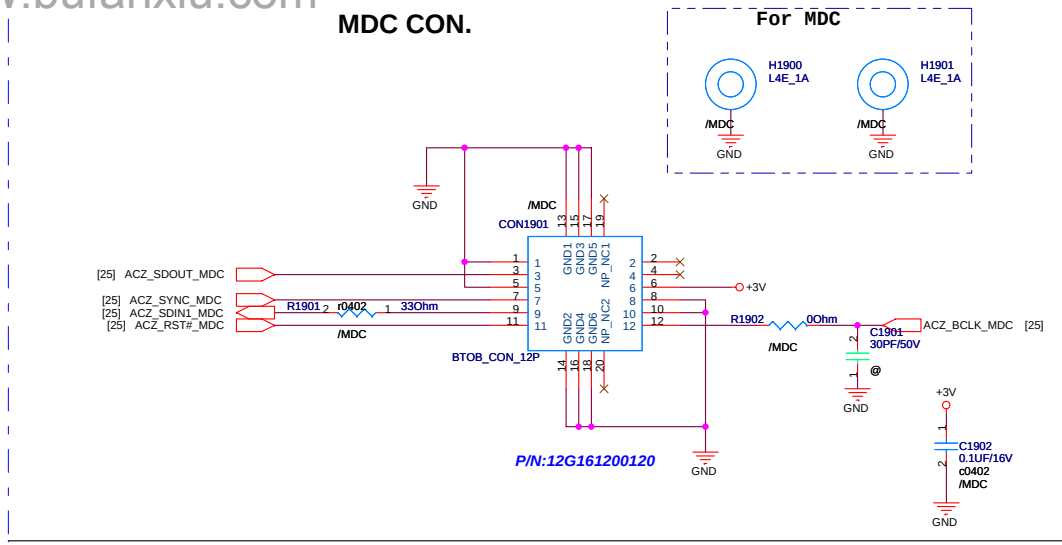
Close to CONNECTOR

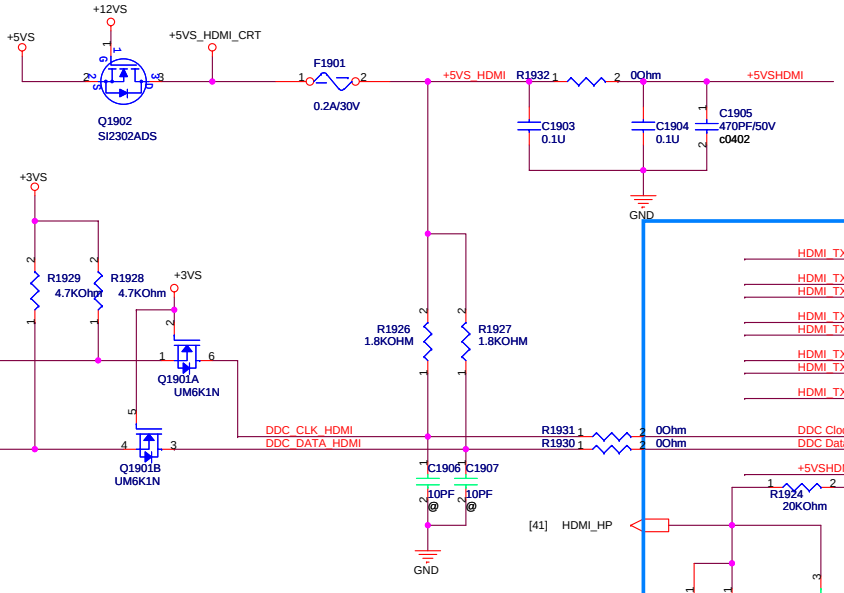


Close to CONNECTOR

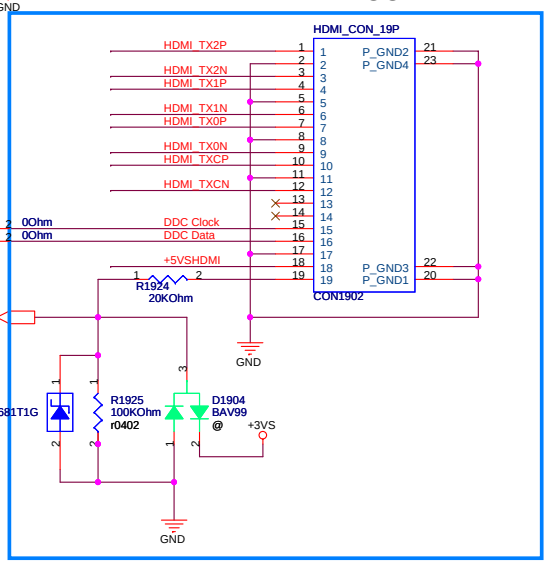


MDC CON.





HDMI CON.



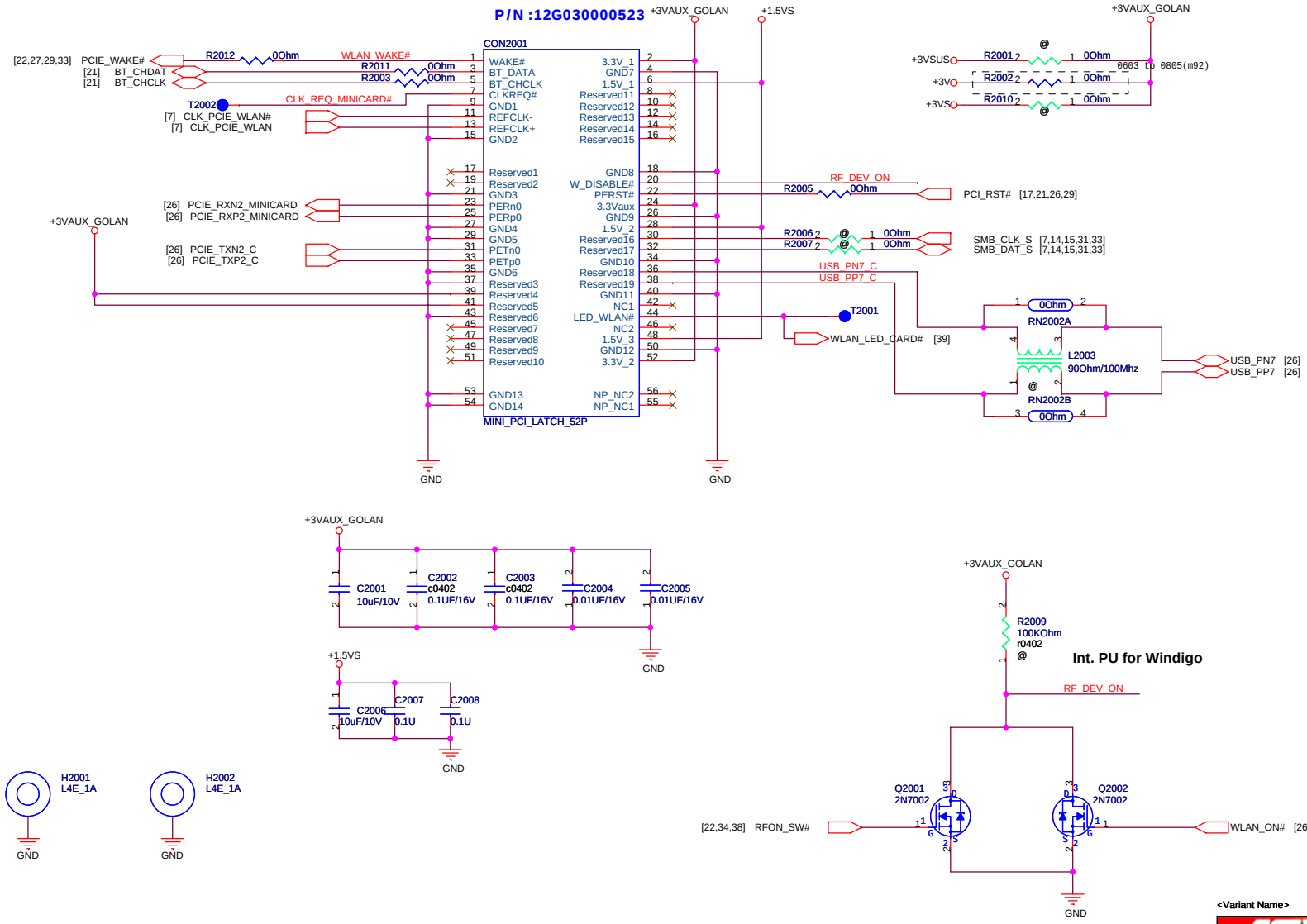
Note: 1. R1930,R1931,R1932: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +3V tolerant

<Variant Name>

ASUSTeK COMPUTER INC	Title : MDC,HDMI CON	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 19 of 64	

WLAN/WIMAX

P/N :12G030000523



<Variant Name>

ASUSTeK COMPUTER INC

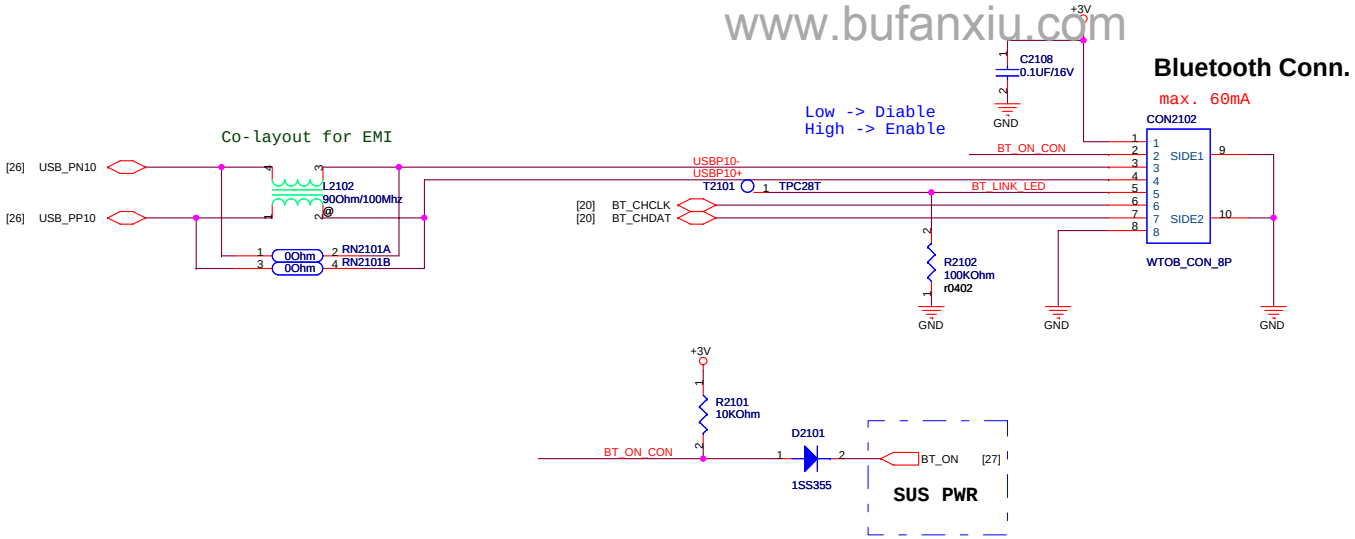
Title : MINI CARD--(1)

Engineer: Kent Qi

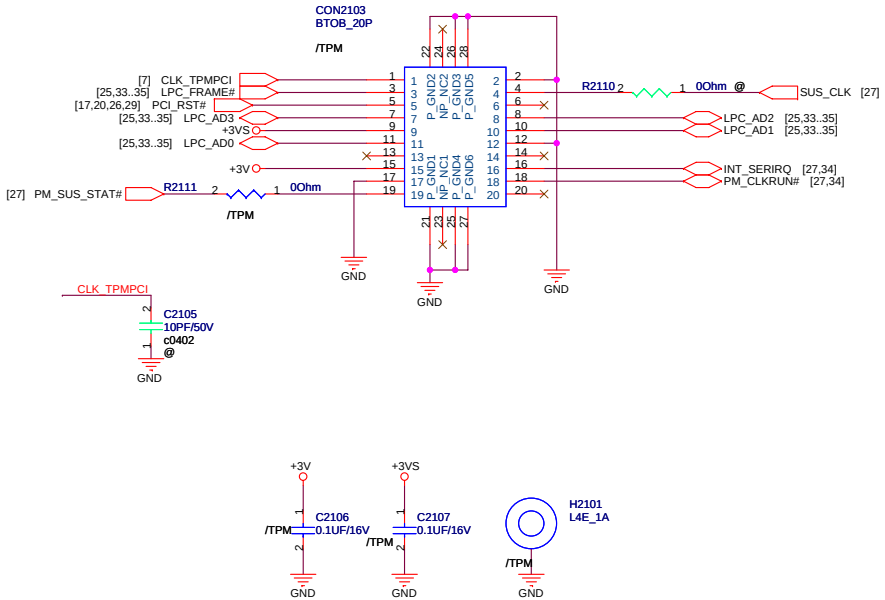
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 20 of 64

Bluetooth Conn.

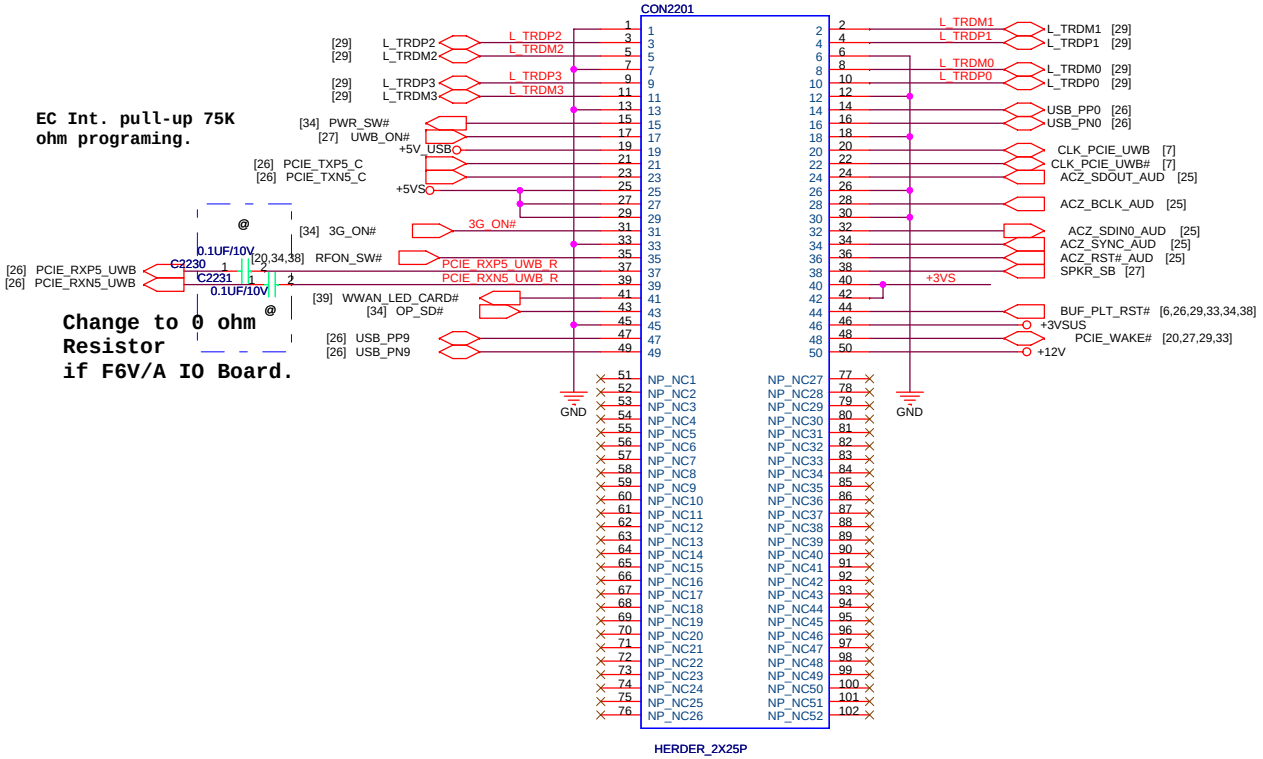


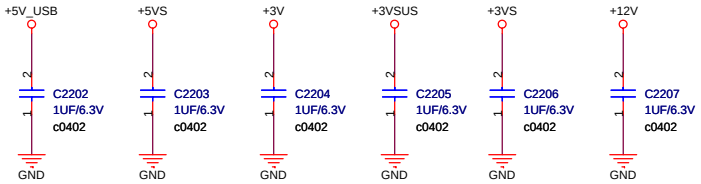
TPM Module Conn.



<Variant Name>

ASUSTeK COMPUTER INC	Title : B/T& TPM	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 21 of 64	





<Variant Name>

ASUSTeK COMPUTER INC

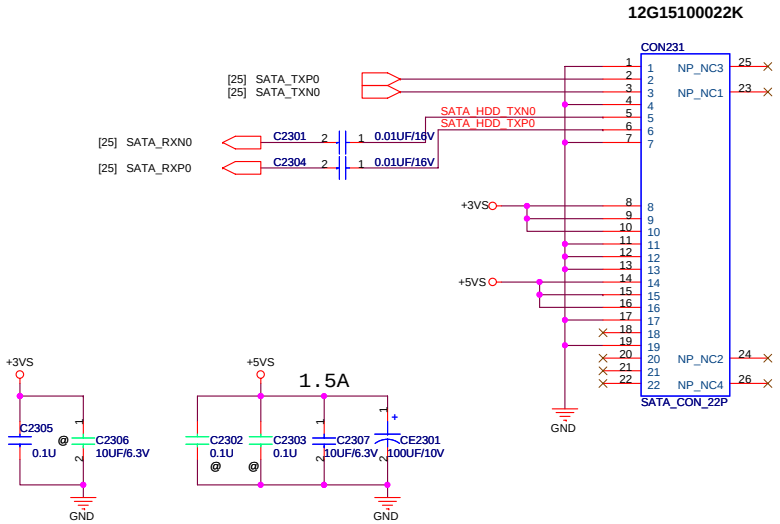
Title : B TO B CONN(M)

Engineer: Kent Qi

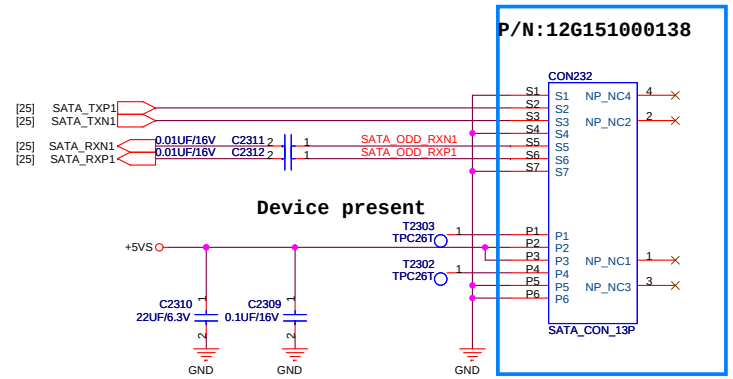
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 22 of 64

SATA HDD CON



SATA ODD CON



<Variant Name>

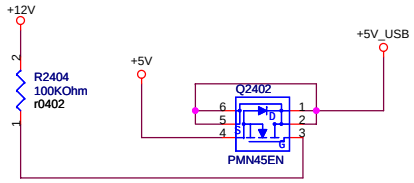
Title : HDD & CDROM

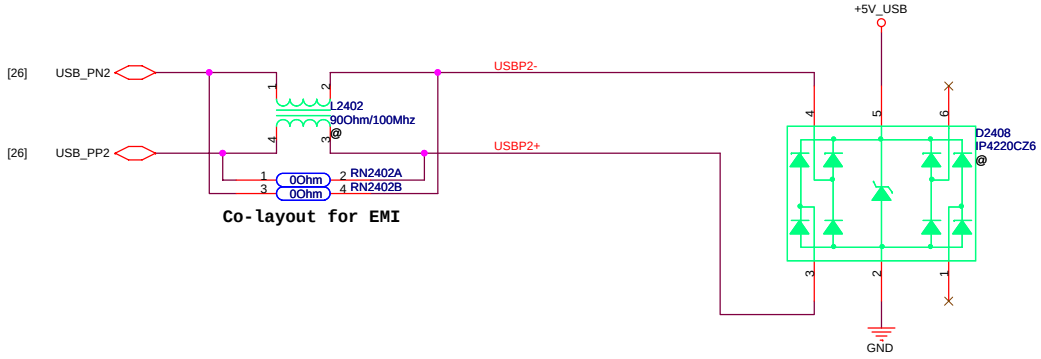
ASUSTeK COMPUTER INC

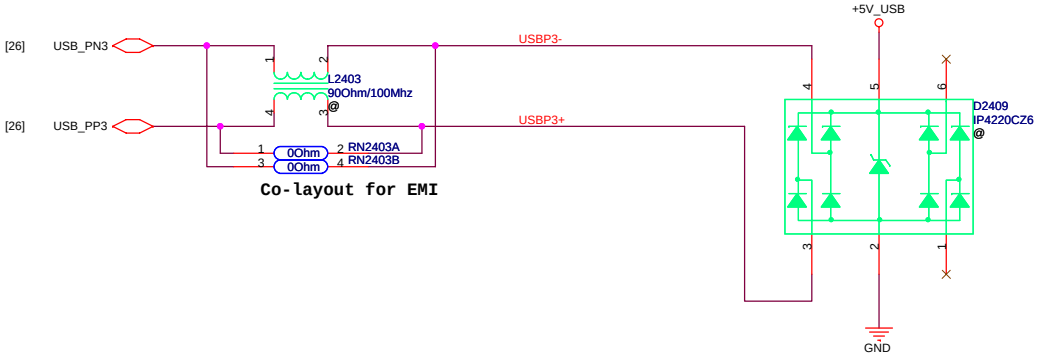
Engineer: Kent Qi

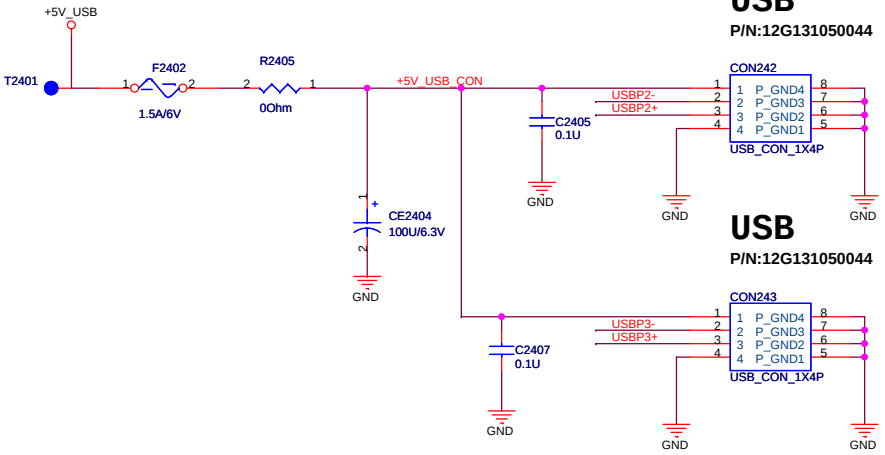
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 23 of 64



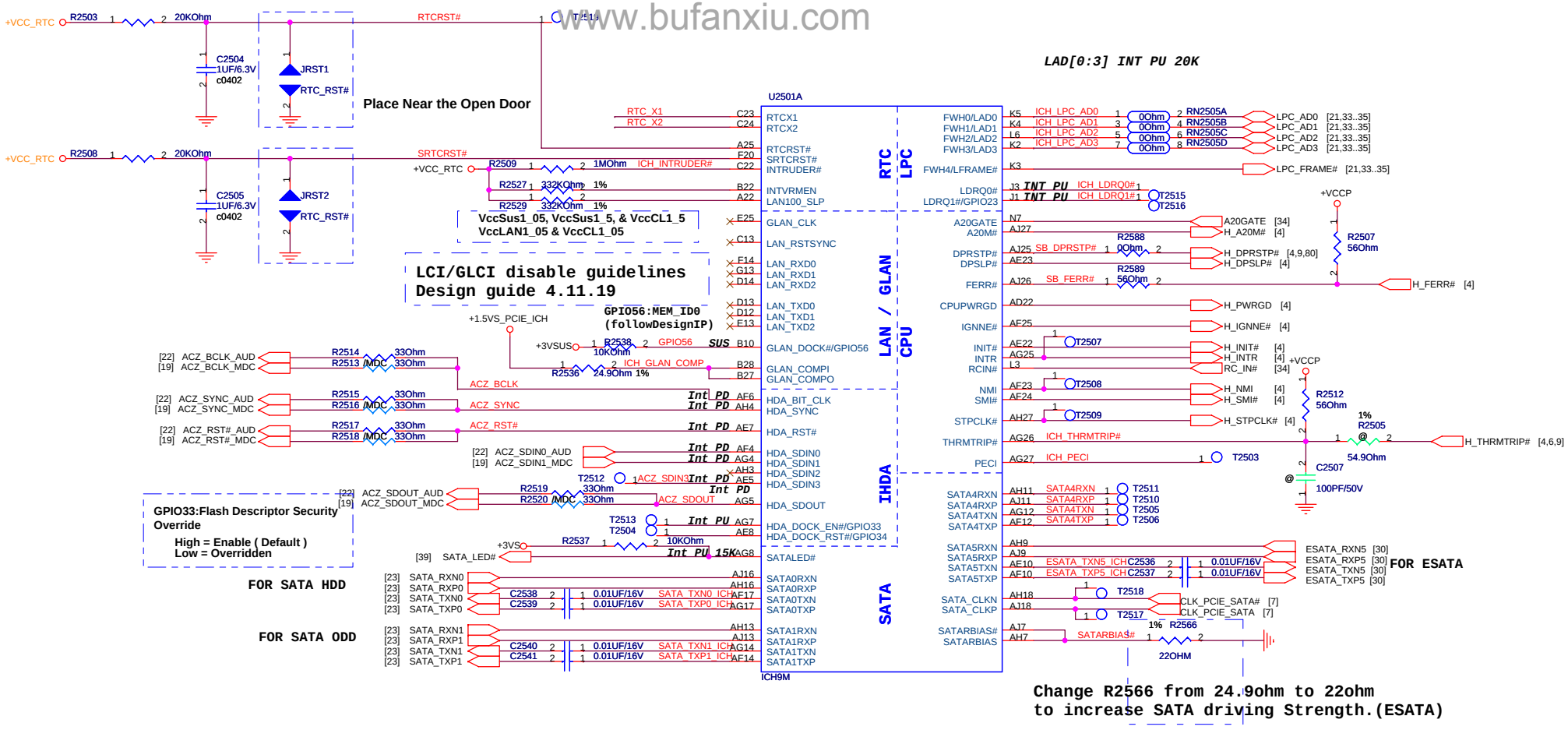


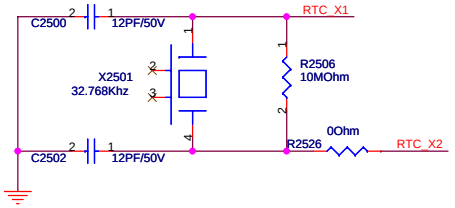


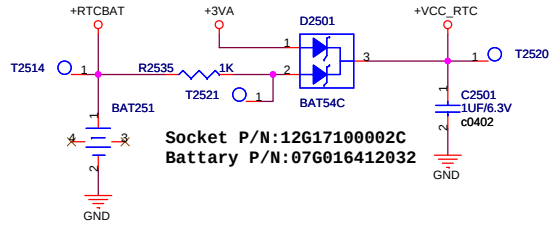


<Variant Name>

ASUSTeK COMPUTER INC	Title : USB PORTS	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 24 of 64	







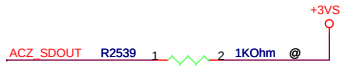
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

01= Enter XOR Chain

10= Normal Operation (Default)

11= Set PCIe Port Config Bit 1



ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(1)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 25 of 64	

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	UWB
PCIE 6	LAN

ICH9 Boot BIOS select

		GNT#0	SPICS#1
LPC	11	1	1 (default)
PCI	10	1	0
SPI	01	0	1

PCI_GNT#0 R2601 1 @ 2 1KOhm

SB_SPICS1# R2602 1 @ 2 1KOhm

GNT#[0:3]:INT PU

U2501B

PCI

Interrupt I/F

ICH9M

PCI_REQ#0 [27]
PCI_GNT#0 T2604
PCI_REQ#1 [27] T2601
PCI_REQ#2 [27] T2602
PCI_REQ#3 [27] T2603
PCI_IRDY# [27]
PCI_RST# [17,20,21,29]
PCI_DEVSEL# [27]
PCI_PERR# [27]
PCI_LOCK# [27]
PCI_SERR# [27]
PCI_STOP# [27]
PCI_TRDY# [27]
PCI_FRAME# [27]
PLT_RST# [9,40]
CLK_ICHPCI [7]
PCI_PME#
INT PU
R2609 2 @ +3VSUS
10KOhm

[27] PCI_INTA#
[27] PCI_INTB#
[27] PCI_INTC#
[27] PCI_INTD#
PCI_INTE# [27]
PCI_INTF# [27]
PCI_INTG# [27]
PCI_INTH# [27]

+3V
C2605 0.1UF/16V c0402
GND

U2603 @
INB VCC
INA
GND OUTY
74LVC1G08GW

PLT_RST#
BUF_PLT_RST# [6,22,29,33,34,38]
GND
R2608 0Ohm

U2501D

PCI-Express Direct Media Interface

[20] PCIE_RXN2_MINICARD
[20] PCIE_RXP2_MINICARD
[20] PCIE_TXN2_C
[20] PCIE_TXP2_C
C2643 0.1UF/10V PCIE_TXN2_MINICARD
C2644 0.1UF/10V PCIE_TXP2_MINICARD

[33] PCIE_RXN3_NEWCARD
[33] PCIE_RXP3_NEWCARD
[33] PCIE_TXN3_C
[33] PCIE_TXP3_C
C2645 0.1UF/10V PCIE_TXN3_NEWCARD
C2646 0.1UF/10V PCIE_TXP3_NEWCARD

[22] PCIE_RXN5_UWB
[22] PCIE_RXP5_UWB
[22] PCIE_TXN5_C
[22] PCIE_TXP5_C
C2650 0.1UF/10V PCIE_TXN5_UWB
C2649 0.1UF/10V PCIE_TXP5_UWB

[29] PCIE_RXN6_GLAN
[29] PCIE_RXP6_GLAN
[29] PCIE_TXN6_C
[29] PCIE_TXP6_C
C2648 0.1UF/10V PCIE_TXN6_GLAN
C2647 0.1UF/10V PCIE_TXP6_GLAN

DMI_RXN0 [9]
DMI_RXP0 [9]
DMI_TXN0 [9]
DMI_TXP0 [9]
DMI_RXN1 [9]
DMI_RXP1 [9]
DMI_TXN1 [9]
DMI_TXP1 [9]
DMI_RXN2 [9]
DMI_RXP2 [9]
DMI_TXN2 [9]
DMI_TXP2 [9]
DMI_RXN3 [9]
DMI_RXP3 [9]
DMI_TXN3 [9]
DMI_TXP3 [9]
T2608
T2609
CLK_PCIE_ICH# [7]
CLK_PCIE_ICH [7]
DMI_COMP R2603 1 2 24.9Ohm 1% +1.5VS_PCIE_ICH
L<500mils

[31] SPI_CLK
[31] SPI_CS#0
R2612 15Ohm
R2613 15Ohm
SB_SPICLK
SB_SPICS0#
SB_SPICS1# INT PU
T2607
[31] SPI_SI
R2615 15Ohm
SB_SPISI INT PD 20K
INT PU
[31] SPI_SO
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO

SPI

+3VS R2606 1 @ 2 1KOhm 1%

SPI_MOSI (relate to MCH_CFG_6)
iTPM Enable

H: Enable (F6V)

L: Disable(Default)

USB

USB_OC#0 N4
USB_OC#1 N5
USB_OC#2 N6
USB_OC#3 P6
USB_OC#4 M1
USB_OC#5 N2
USB_OC#6 M4
USB_OC#7 M3
USB_OC#8 N3
USB_OC#9 N1
USB_OC#10 P5
USB_OC#11 P3

WLAN_ON R2626 0Ohm

USBRBIAS_PN AG2
R2605 22.6Ohm 1%
USBRBIAS AG1
USBRBIAS#

Place within 500 mils of ICH

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P

USB_PN0 [22]
USB_PP0 [22]
USB_PN1
USB_PP1
T2613
T2614
USB_PN2 [24]
USB_PP2 [24]
USB_PN3 [24]
USB_PP3 [24]
USB_PN4 [17]
USB_PP4 [17]
USB_PN5 [36]
USB_PP5 [36]
USB_PN6
USB_PP6
T2611
T2612
USB_PN7 [20]
USB_PP7 [20]
USB_PN8 [33]
USB_PP8 [33]
USB_PN9 [22]
USB_PP9 [22]
USB_PN10 [21]
USB_PP10 [21]
USB_PN11 [38]
USB_PP11 [38]

USB INT PD 15K

+3V
R2611 100KOhm
WLAN_ON# [20]
Q2602 2N7002
WLAN_ON

+3VSUS

RN2606A USB_OC#1
RN2606B USB_OC#6
RN2606C USB_OC#2
RN2606D USB_OC#3
RN2607A USB_OC#4
RN2607B USB_OC#8
RN2607C USB_OC#7
RN2607D USB_OC#0
RN2609A USB_OC#11
RN2609B USB_OC#9
RN2609C USB_OC#10
RN2609D USB_OC#5
10KOhm

USB 0	USB Conn
USB 1	
USB 2	USB Conn
USB 3	USB Conn
USB 4	CMOS Camera
USB 5	CardReader
USB 6	UWB
USB 7	WiMax
USB 8	NewCard
USB 9	3G Card
USB 10	Bluetooth
USB 11	FINGER PRINT

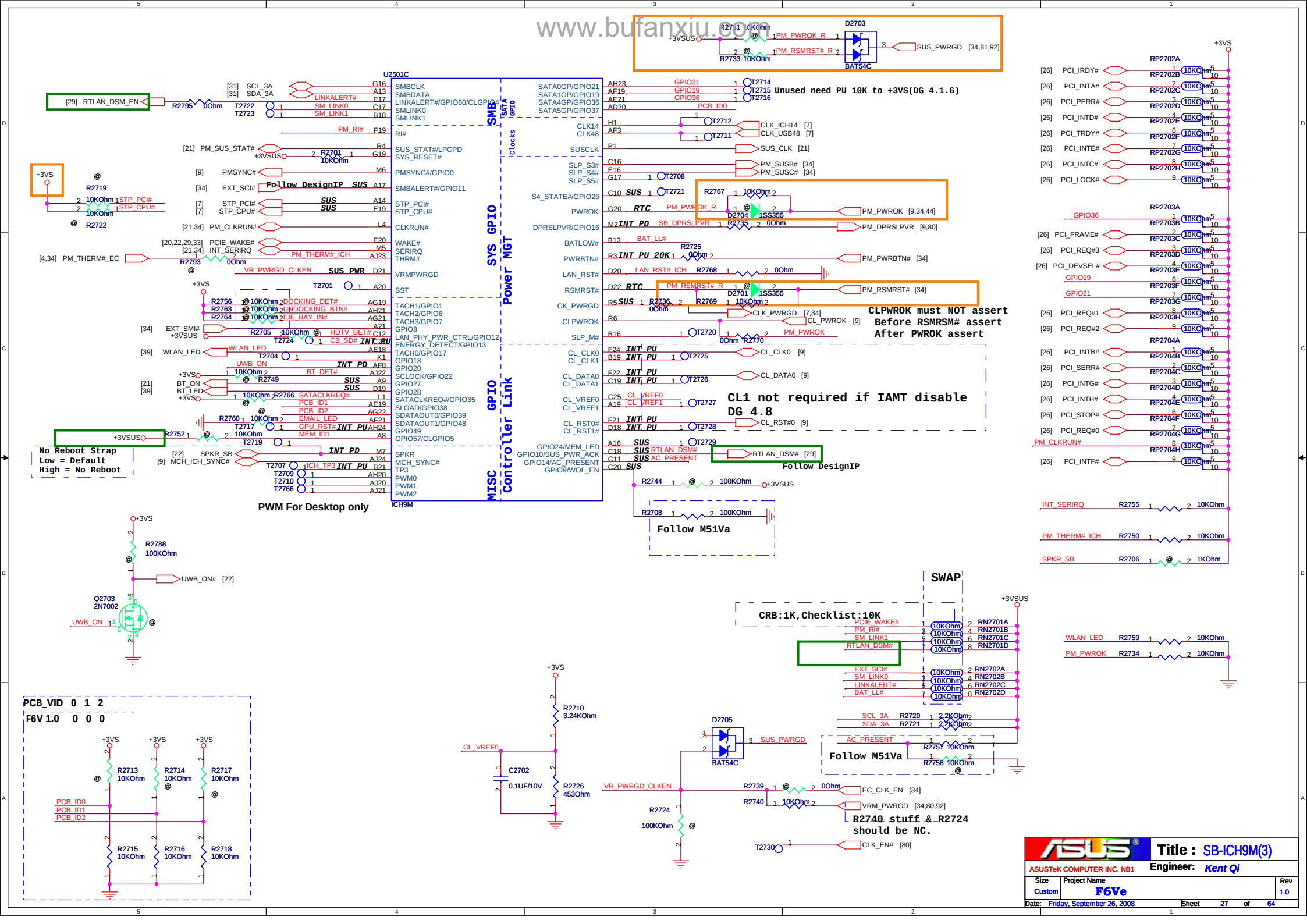
ASUSTeK COMPUTER INC. NB1

Title : SB-ICH9M(2)

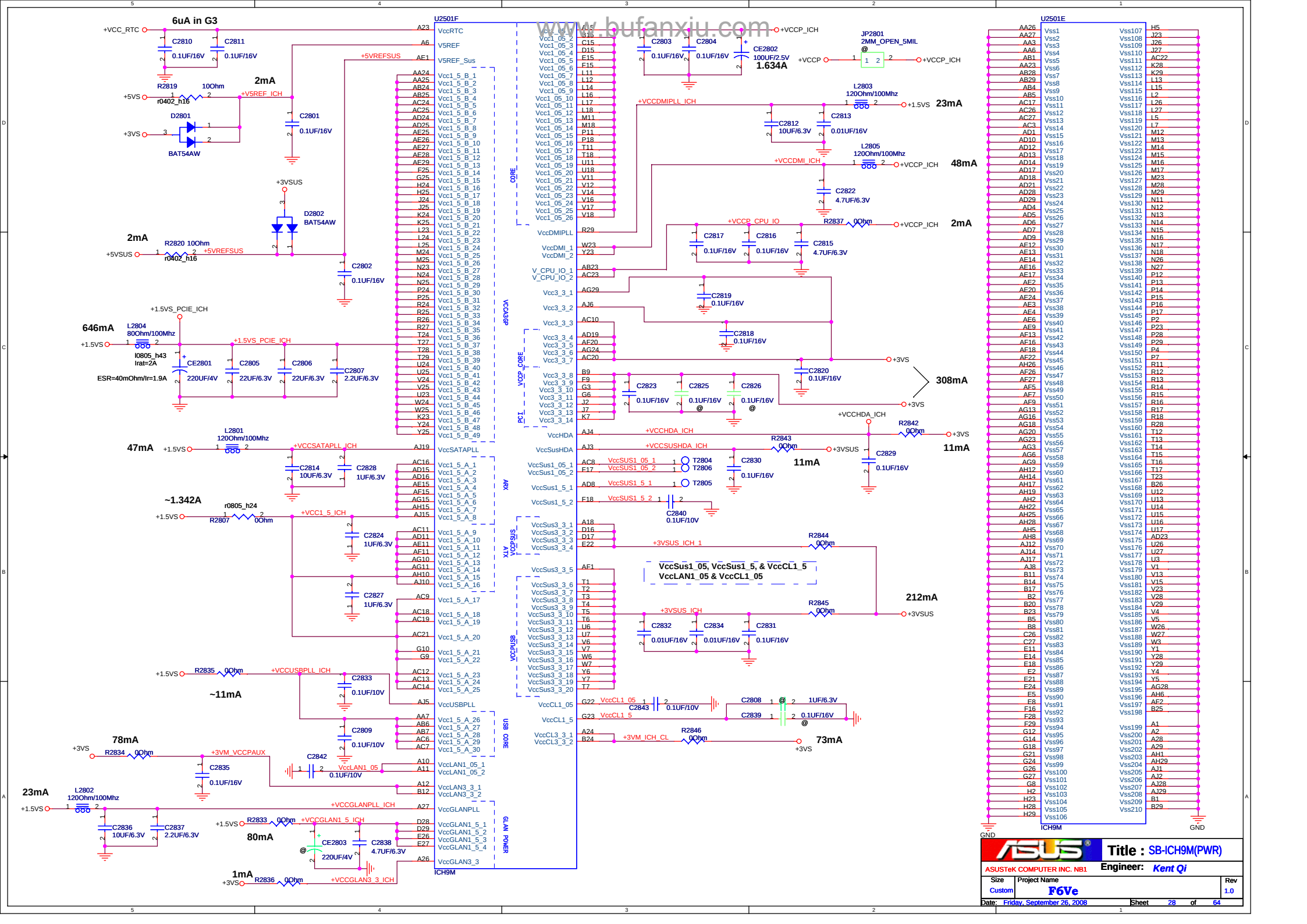
Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

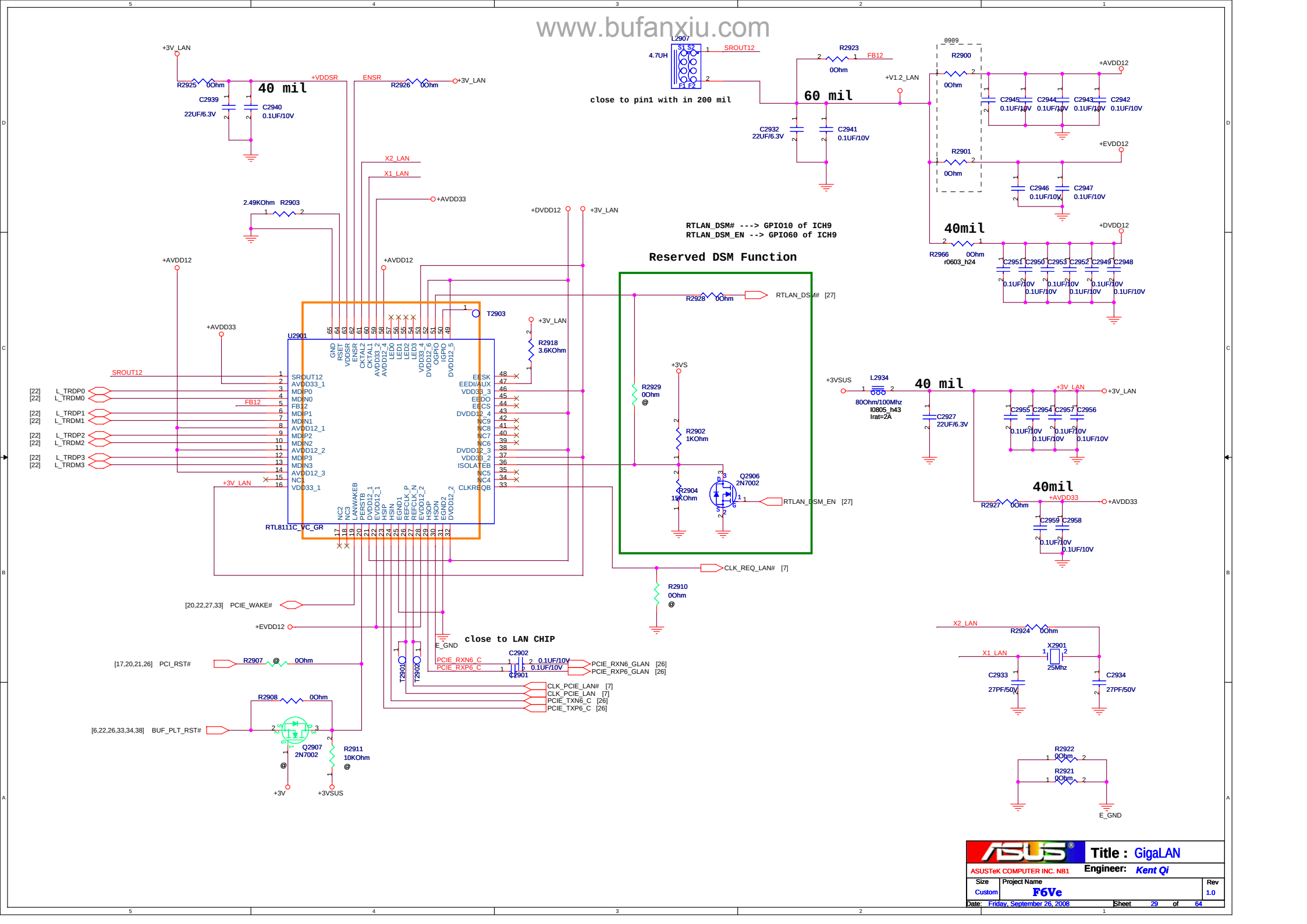
Date: Friday, September 26, 2008 Sheet 26 of 64



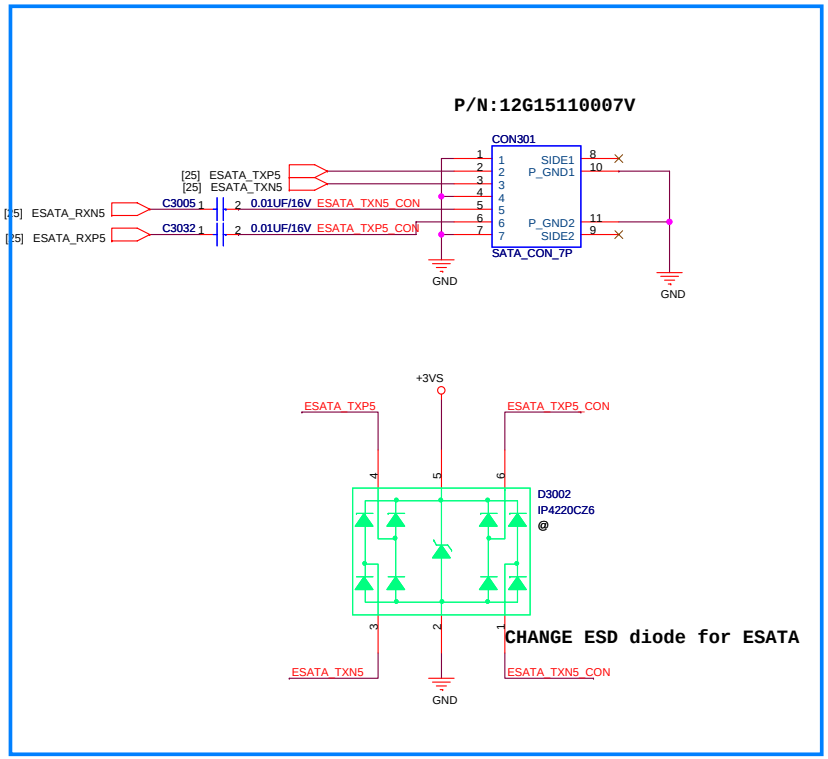
ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(3)		
	Engineer: Kent Qi		
Size: Custom	Project Name: F6Ve		Rev: 1.0
Date: Friday, September 26, 2008	Sheet 27 of 64		



Title : SB-ICH9M(PWR)			
ASUSTeK COMPUTER INC. NB1	Engineer: Kent Qi		
Size: Custom	Project Name: F6Ve		Rev: 1.0
Date: Friday, September 26, 2008	Sheet 28 of 64		



ASUSTeK COMPUTER INC. NB1	Title : GigaLAN		
	Engineer: Kent Qi		
Size: Custom	Project Name: F6Ve		Rev: 1.0
Date: Friday, September 26, 2008	Sheet 29 of 64		



<Variant Name>

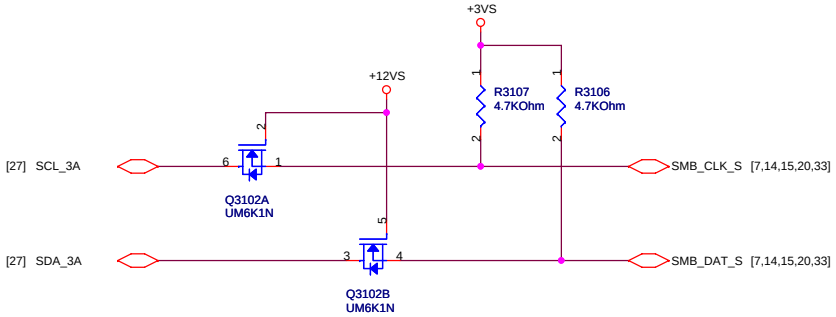
Title : ESATA

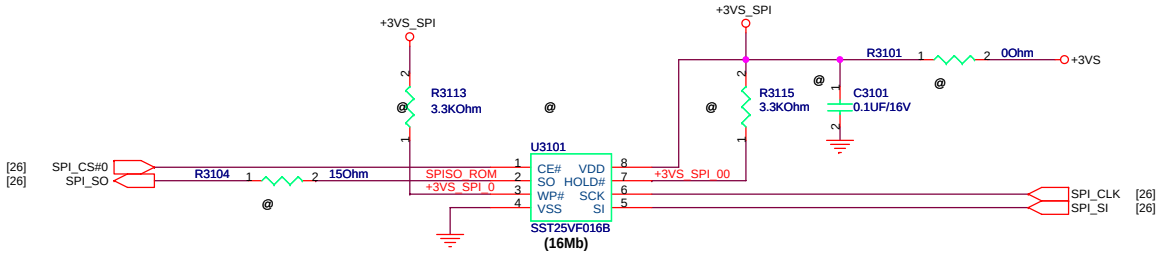
ASUSTeK COMPUTER INC

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 30 of 64





FOR iTPM

ASUSTeK COMPUTER INC. NB1	Title : ICH9M-Other	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 31 of 64	

<Variant Name>

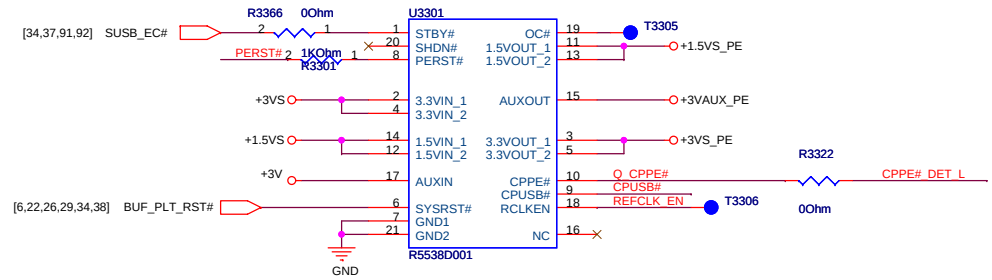
Title : EMPTY

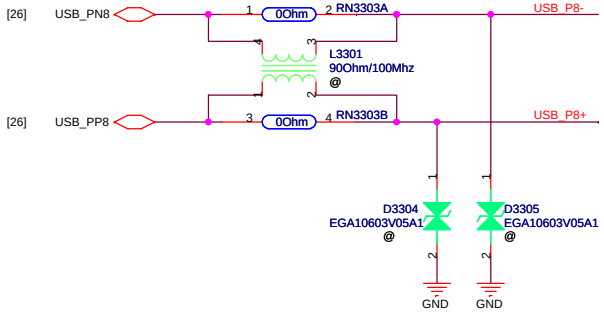
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

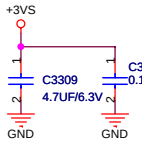
Date: Friday, September 26, 2008 Sheet 32 of 64

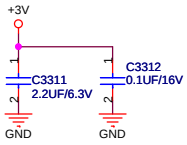


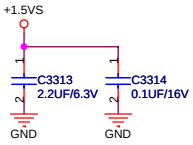


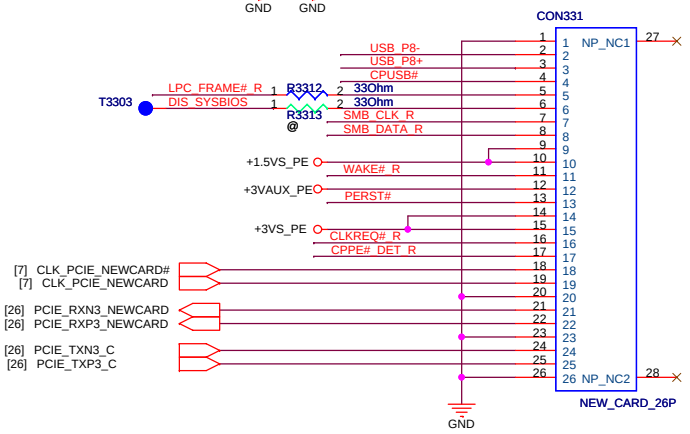
NewCard Header

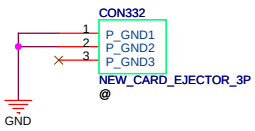
P/N:12G16130026R

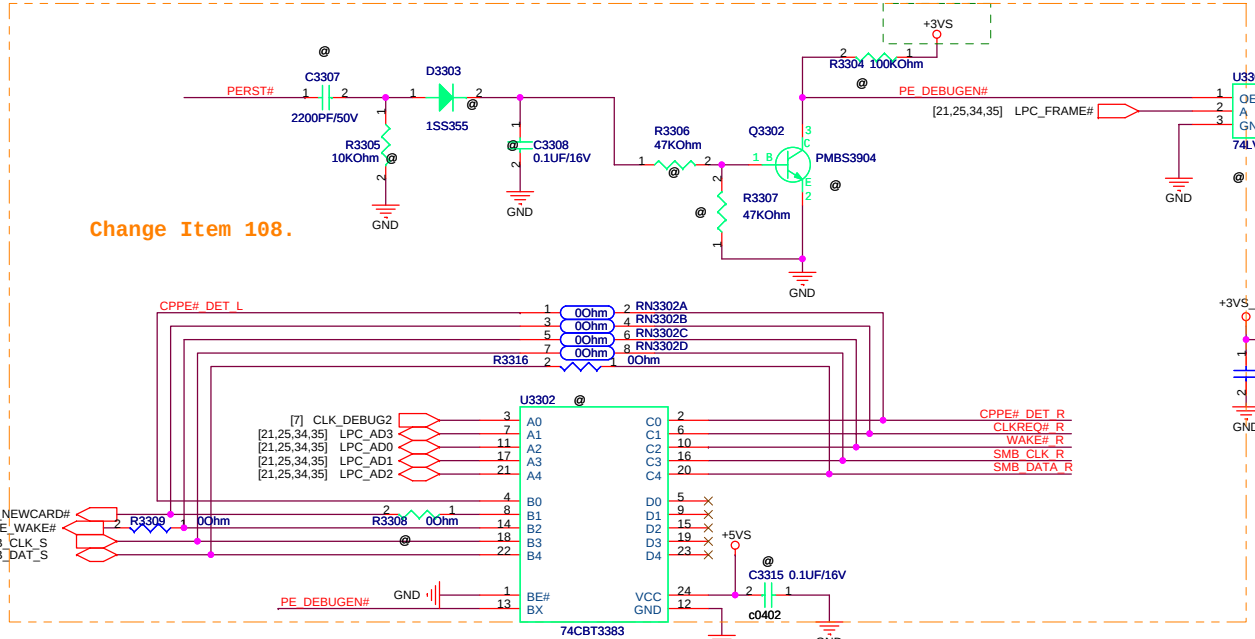


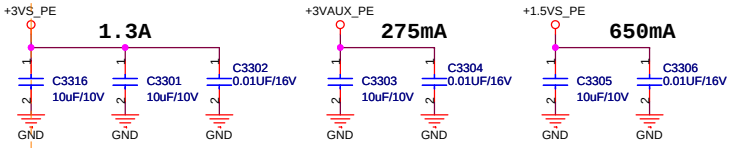












<Variant Name>

ASUSTeK COMPUTER INC

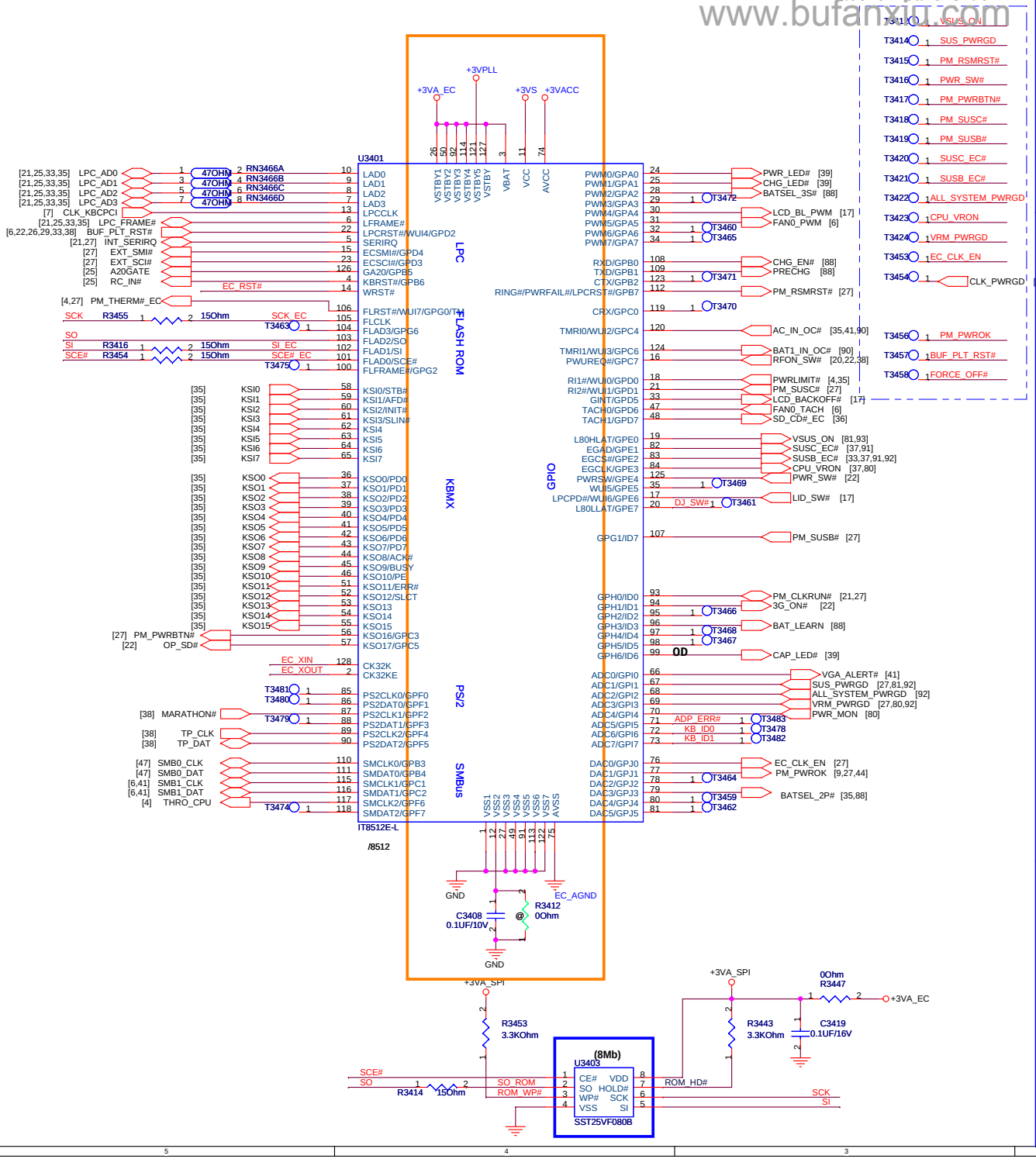
Title : NEW CARD

Engineer: Kent Qi

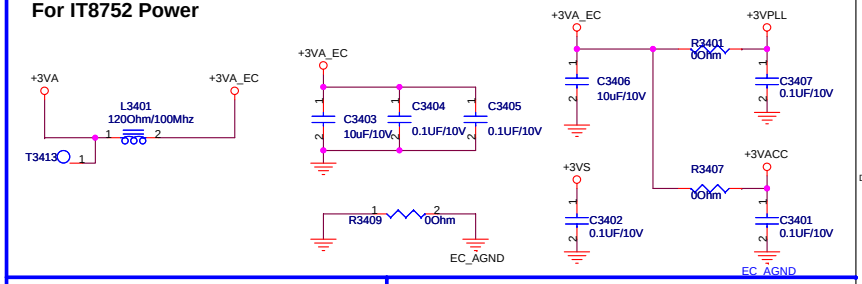
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 33 of 64

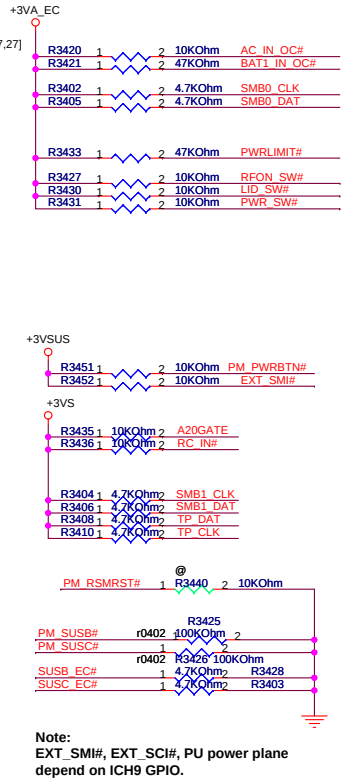
Place on same side



For IT8752 Power



For PU / PD

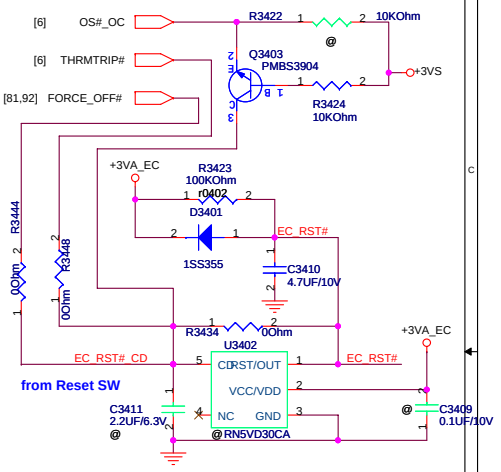


Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For EC Reset

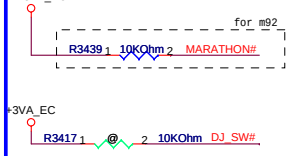
Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3402,C3409,C3411
DNI: D3401,C3410,R3434,R3423
Option 2:
Mount D3401,C3410,R3434,R3423
DNI: U3002, C3009, C3011



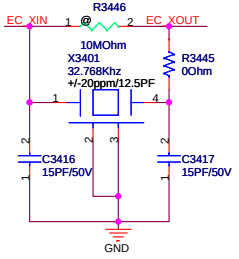
For Instant Key

Note: Close to EC



For X'tal

Note:
Cload=12.25PF
place close to EC



For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

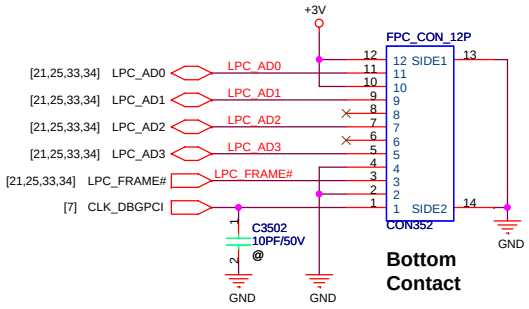
Note: Default Int. Pull-Low

For iAMT pin name

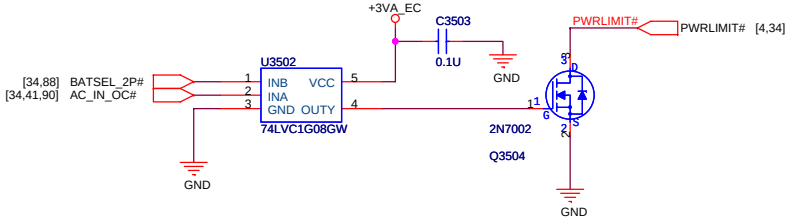
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM, +3VMCLK_PG
SUSPWR_ACK

ASUSTeK COMPUTER INC. NB1	Title : EC_IT8512E-L (1/2)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 34 of 64	

For Debug

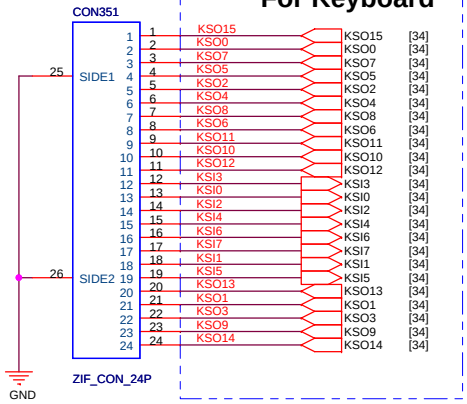


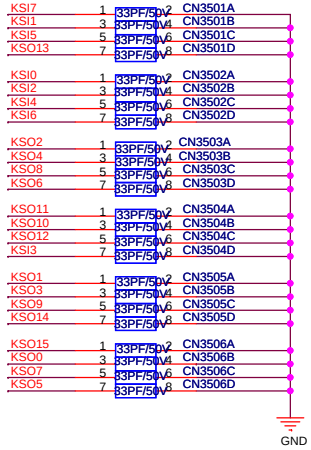
PWRLMT Circuit: For Battery 1P



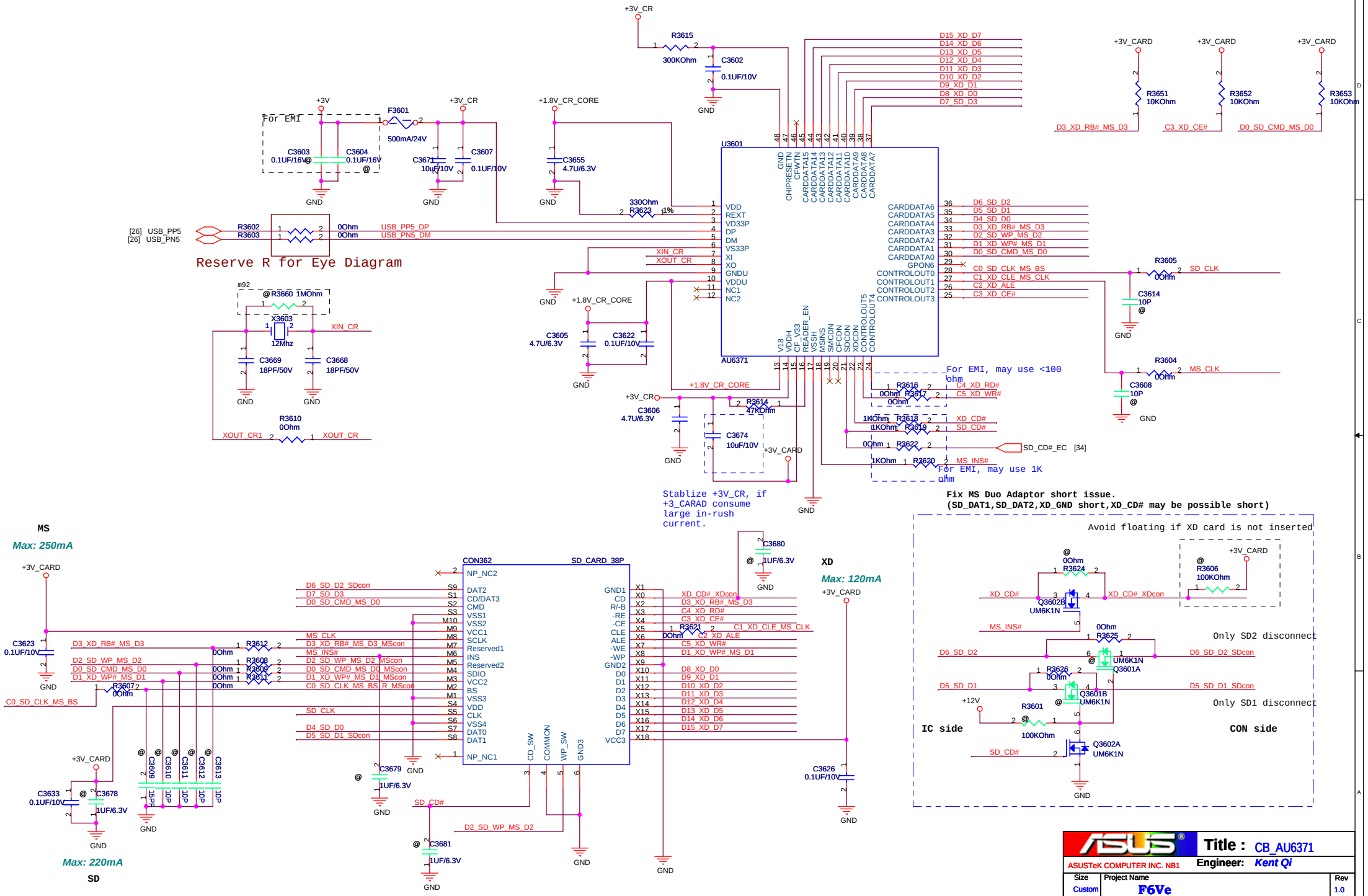
P/N:12G182402404

For Keyboard

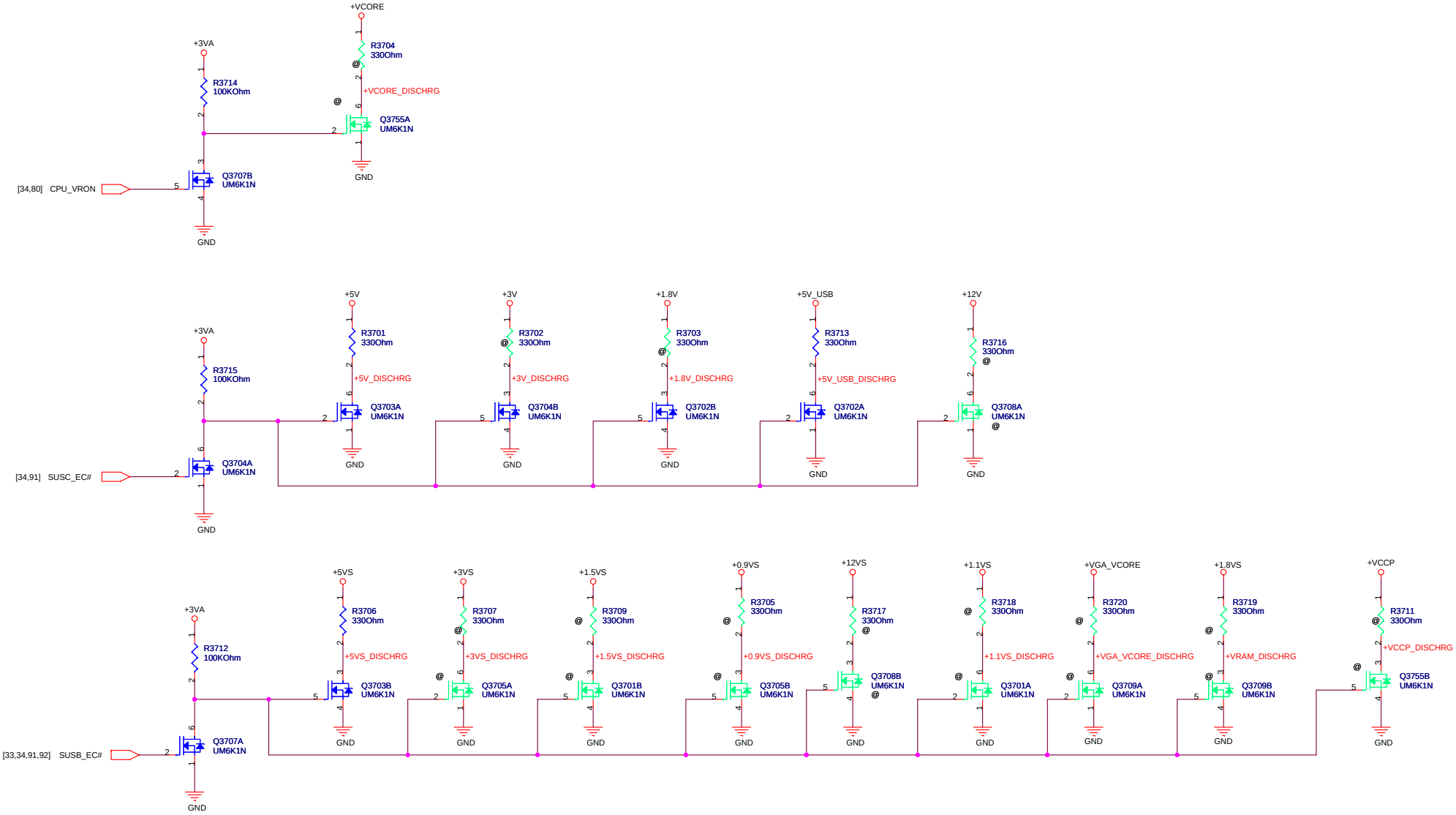




ASUSTeK COMPUTER INC. NB1	Title : EC_IT8752 (2/2)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 35 of 64	



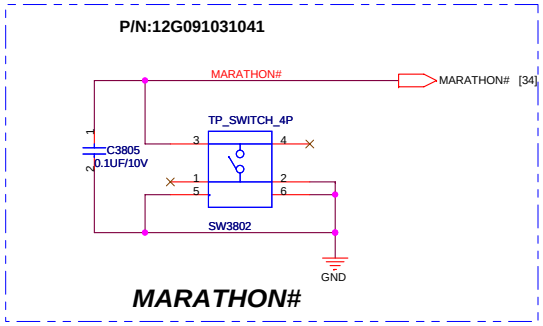
ASUSTeK COMPUTER INC. NB1	Title : CB_AU6371		
	Engineer: Kent Qi		
Size: Custom	Project Name: F6Ve		Rev: 1.0
Date: Friday, September 26, 2008	Sheet 36 of 64		

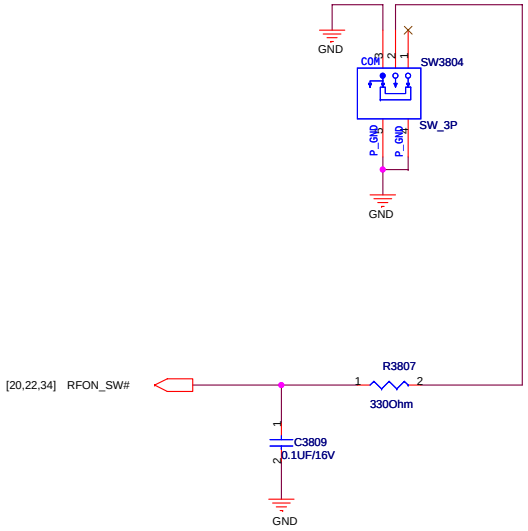


<Variant Name>

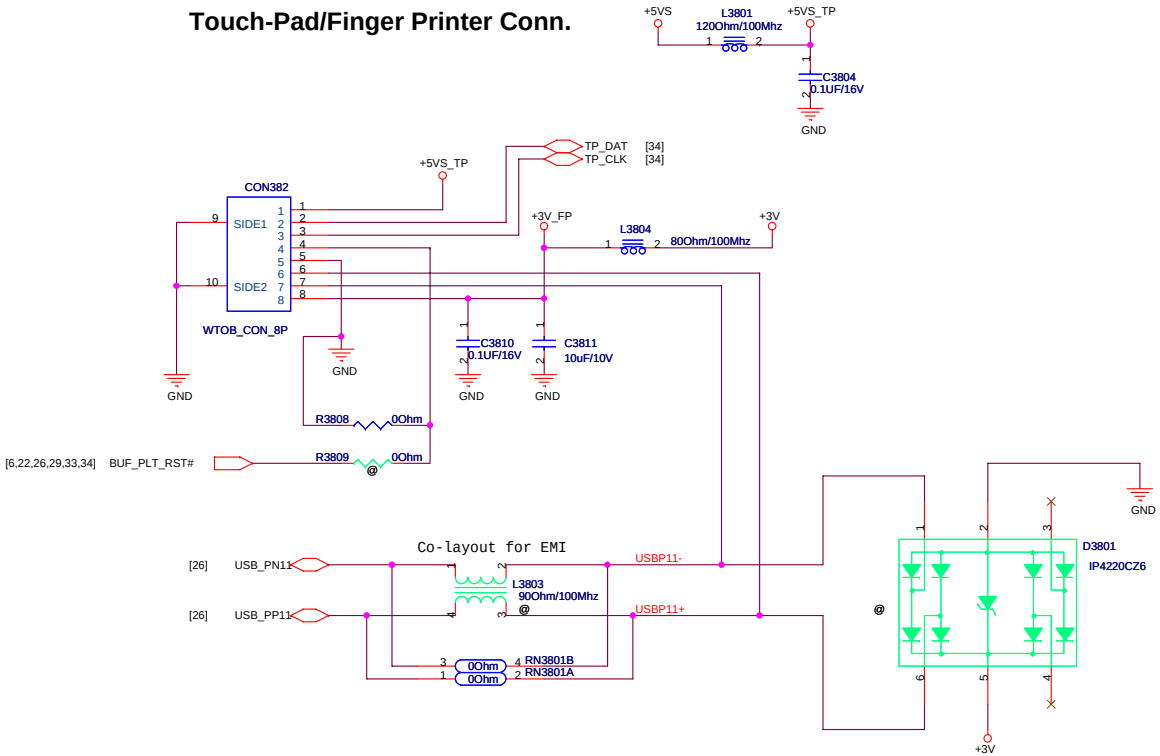
ASUSTeK COMPUTER INC	Title : DISCHARGE	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 37 of 64	

BT/WLAN SW





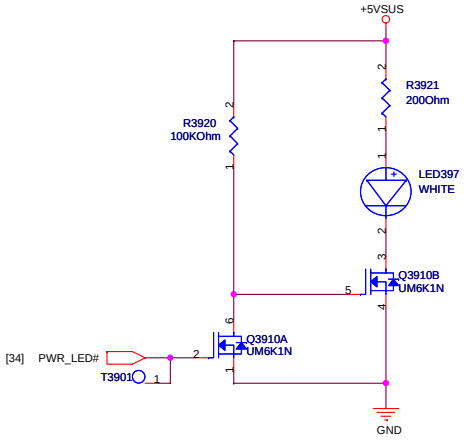
Touch-Pad/Finger Printer Conn.



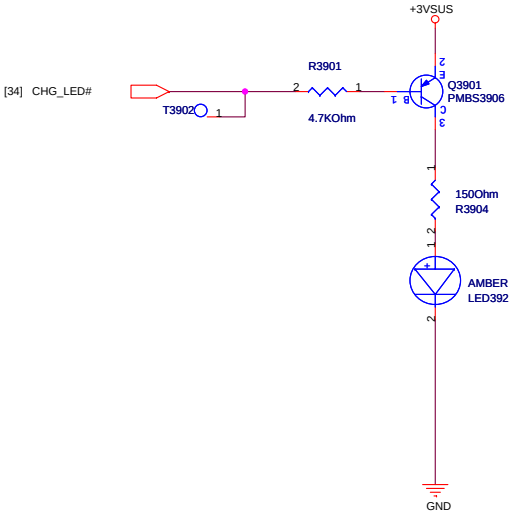
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 38 of 64	

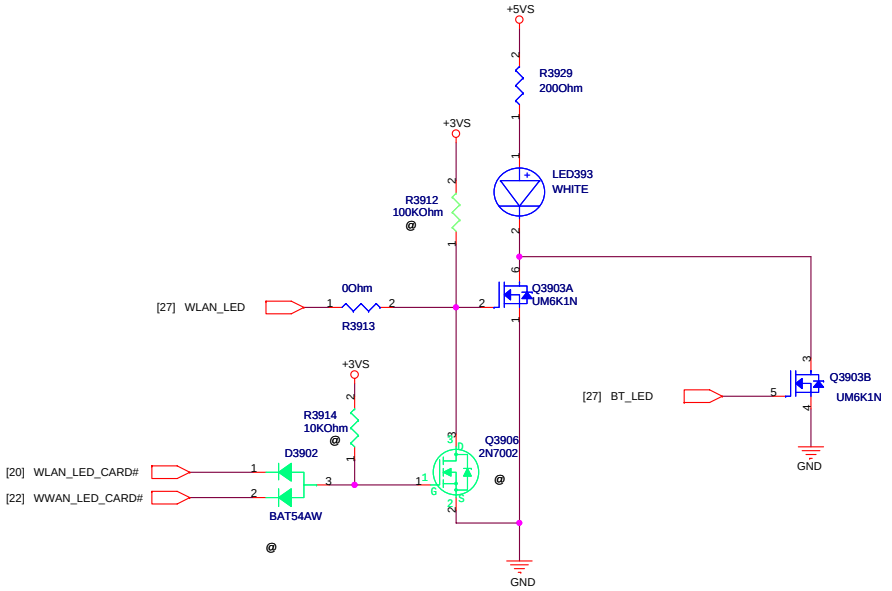
PWR LED



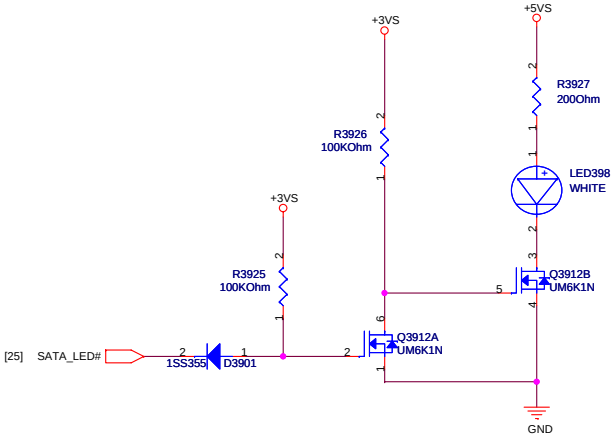
BATTERY LED



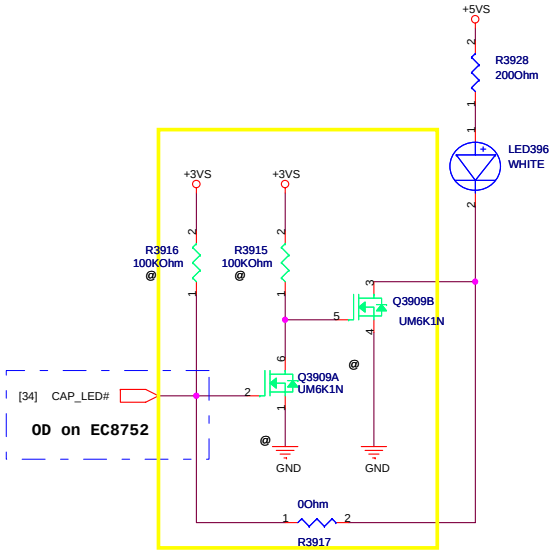
WireLess/BT LED



SATA LED

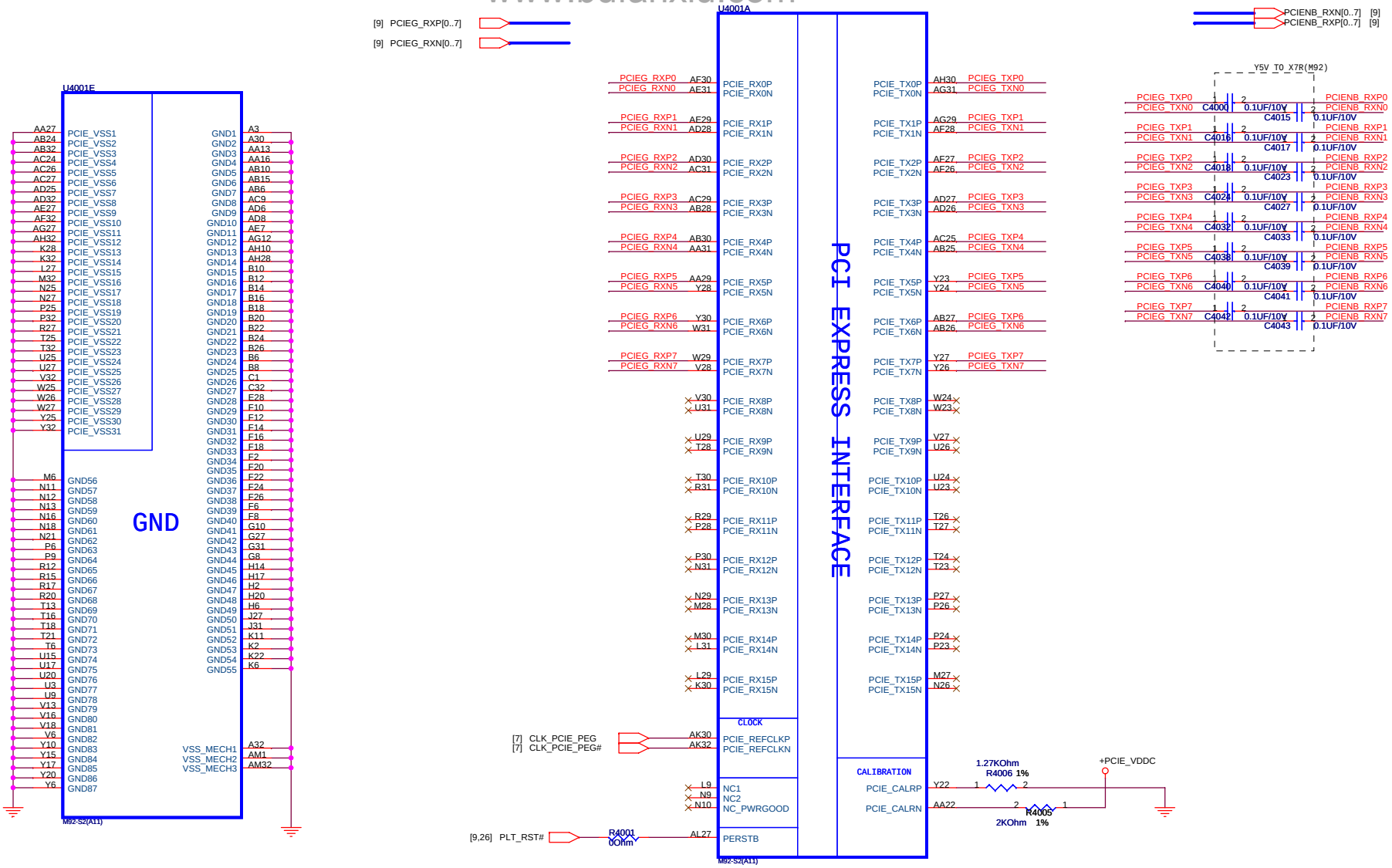


Cap. Lock



<Variant Name>

ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 39 of 64	



<Variant Name>

ASUSTeK COMPUTER INC	Title : M92S2-PCIE(1)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 40 of 64	

Close to U4001

37.5 ohm

55 ohm

CRT_M92_RED_S — @ JP4101 SHORT_PIN — 150Ohm R4170 1% — CRT_RED [18]

CRT_M92_GREEN_S — @ JP4102 SHORT_PIN — 150Ohm R4171 1% — CRT_GREEN [18]

CRT_M92_BLUE_S — @ JP4103 SHORT_PIN — 150Ohm R4172 1% — CRT_BLUE [18]

GND

VRAM SIZE

+3VSG_DELAY

R4125 10KOhm r0402 — R4133 10KOhm r0402 @ — R4131 10KOhm r0402

VGA_GPIO13 — VGA_GPIO12 — VGA_GPIO11

R4132 10KOhm r0402 — R4126 10KOhm r0402 — R4169 10KOhm r0402

GND

GPIO[13:11] = 001, 256M memory aperture(default)

GPIO[13:11] = 100, 512M memory aperture

Memory ID

+1.8VS — R4188 0Ohm

R4127 10KOhm r0402 @ — R4128 10KOhm r0402 @ — R4129 10KOhm r0402 @ — R4130 10KOhm r0402 @

VGAMEM_ID0 — VGAMEM_ID1 — VGAMEM_ID2 — VGAMEM_ID3

R4134 10KOhm r0402 — R4135 10KOhm r0402 — R4136 10KOhm r0402 — R4137 10KOhm r0402

GND

ID 0: Qimonda 64Mx16 A Channel(512M)

ID 8: SAMSUNG 64Mx16 A Channel(512M)

GPIO[0]: Tx Power Savings Enable
0: 50% Tx output swing (INT PD)
1: full Tx output swing

GPIO[1]: Tx De-emphasis Enable
0: Tx de-emphasis disbale(INT PD)
1: Tx de-emphasis enable.

GPIO2 for PCIE 2.5G/5G select.(L:2.5G default)

GPIO6 for Power control signals
GPIO8&GPIO9 for Serial ROM

GPIO19 VGA Thermtrip out(110 degree active)

PWRCNTL_0	PWRCNTL_1	+VGA_VCORE_O
L	L	1.20V
H	L	1.10V
L	H	1.00V
H	H	0.90V

HSYNC	VSYNC	Function
L	L	No audio Function
L	H	Displayport and HDMI if adapter is detected
H	L	Displayport only
H	H	Both Displayport and HDMI

Shunt R 180ohm for M7X

U4001B

MUTI GFX

DPA: TXCAP_DPA3P / TXCAM_DPA3N — TX0P_DPA2P / TX0M_DPA2N — TX1P_DPA1P / TX1M_DPA1N — TX2P_DPA0P / TX2M_DPA0N — TXCBP_DPB3P / TXCBM_DPB3N

DPB: TX3P_DPB2P / TX3M_DPB2N — TX4P_DPB1P / TX4M_DPB1N — TX5P_DPB0P / TX5M_DPB0N

→ TMDS_TXCP [19] / TMDS_TXCN [19] — TMDS_TX0P [19] / TMDS_TX0N [19] — TMDS_TX1P [19] / TMDS_TX1N [19] — TMDS_TX2P [19] / TMDS_TX2N [19]

T4105 T4106 T4103 T4107 T4104 T4108

DVPCNTL_MVP_0 … DVPCNTL_2 … DVPCLK … DVPDATA_0 … DVPDATA_23

T4110 PANEL_ID0 — T4111 PANEL_ID1

0908: VGAMEM_ID0 … VGAMEM_ID3

I2C: SCL / SDA

[17] EDID_CLK — [17] EDID_DAT — +3VSG — 2.7KOhm R4115 — 2.7KOhm R4116

GENERAL PURPOSE I/O

VGA_GPIO0 INT_PD — VGA_GPIO1 INT_PD — PCIE_GPIO2 — AC_BATT_Detect — VGA_GPIO5 INT_PD — [47] L_BKLTEN_V — VGA_GPIO8 — VGA_GPIO9 INT_PD — VGA_GPIO10 INT_PD — VGA_GPIO11 INT_PD — VGA_GPIO12 INT_PD — GPIO_23_CLKREQB — GPIO_TRSTB — JTAG_TDI — JTAG_TCK — JTAG_TMS — JTAG_TDO — TESTEN — GENERICA — GENERICB — GENERICC — GENERICD — GENERICE_HPD4 — HPD1

[85,92] VGA_PWRGD — [85] PWRCNTL_0 — [7] ATI27M_SSC — R4193 1 @0Ohm — ATI27M_SSC — VGA_ALERT# — @0Ohm — VGA_THERM — R4119 @0Ohm — VGA_TEMP_FAIL# — LVGA_GPIO19

[85] PWRCNTL_1 — [44] VGA_BBEN — R4120 — VGA_BBEN — T4131 INT_PD — T4133 — VGA_GPIO22 INT_PD — GPIO_23_CLKREQB

GPIO_TRSTB — T4136 GPIO_TDI — T4137 GPIO_TCK — T4138 GPIO_TMS — T4139 GPIO_TDO — 1KOhm R4151 — GND

T4141 — GEN_B INT_PD — T4143 — GEN_D_HPD4 — [19] HDMI_HP

DAC1: R RB — G GB — B BB — HSYNC — VSYNC — RSET — AVDD — AVSSQ — VDD1DI — VSS1DI

AM26 CRT_M92_RED_S — R4103 0Ohm — GND

AL25 CRT_M92_GREEN_S — R4104 0Ohm — GND

AH24 CRT_M92_BLUE_S — R4105 0Ohm — GND — 10KOhm @ R4110 — +3VSG_DELAY

AH26 CRT_HSYNC [18] — 10KOhm R4108

AJ27 CRT_VSYNC [18]

AD22 DAC_RSET — R4109 1% 499Ohm — GND

AG24 +1.8VS_AVDD — GND

AF23 +1.8VS_VDD1DI — GND

DAC2: R2 R2B — G2 G2B — B2 B2B — C Y COMP — H2SYNC V2SYNC — VDD2DI VSS2DI — A2VDD — A2VDDQ — A2VSSQ — R2SET

AL13 10KOhm @ R4112 — +3VSG_DELAY

AD19 +1.8VS_VDD2DI — GND

AE20 +3VSG_A2VDD

AE17 +1.8VS_A2VDDQ

AE19 GND

AG13 — R4111 1% 715Ohm — GND

PLL/CLOCK: DPLL_PVDD — DPLL_PVSS — DPLL_VDDC — XTALIN — XTALOUT

VREFG

DDC/AUX: DDC1CLK — DDC1DATA — AUX1P — AUX1N — DDC2CLK — DDC2DATA — AUX2P — AUX2N — RSVD2 — RSVD3 — DDCCLK_AUX5P — DDCDATA_AUX5N — DDC5CLK — DDC5DATA — NC_DDCCLK_AUX7P — NC_DDCDATA_AUX7N

AE6 CRT_DDC_CLK [18] — AE5 CRT_DDC_DATA [18]

AC11 HDMI_DDC_CLK [19] — AC13 HDMI_DDC_DATA [19]

THERMAL: DPLUS — DMINUS — TS_FDO — TSVDD — TSVSS

VGA_THERM_DA — VGA_THERM_DC — T4 — T2 — R5 — AD17 — AC17 — +TSVDD

+3VSG_VGTM — R4166 200 — +3VSG — C4162 0.1UF/10V — GND

VGA_THERM_DA — @ C4118 1000P — VGA_THERM_DC

not enable — [34] VGA_ALERT# — +3VSG — 2 4.7KOhm R4198 @

U4105 G781-1 (OD): VCC — DXP — DXN — OVERT# — SCLK — SDA — ALERT# — GND

VGA_THERM_DA — VGA_THERM_DC — VGA_THERM# — R4189 4.7KOhm @ — +3VSG

SMB1_CLK [6,34] — SMB1_DAT [6,34]

Slave Address:9A

GND

+1.8VS_AVDD — L4101 120Ohm/100Mhz — 70mA — +1.8VS — C4145 0.1UF/10V — C4144 1UF/6.3V — C4141 10uF/10V

+1.8VS_VDD2DI — R4106 0Ohm — L4102 120Ohm/100Mhz — 40mA — +1.8VS — C4147 0.1UF/10V — C4146 1UF/6.3V — C4142 10uF/10V

+3VSG_A2VDD — L4103 120Ohm/100Mhz — 65mA — +3VSG — C4149 0.1UF/10V — C4148 1UF/6.3V — C4143 10uF/10V

+1.8VS_A2VDDQ — L4104 120Ohm/100Mhz — 1mA — +1.8VS — C4152 0.1UF/10V — C4150 1UF/6.3V — C4151 10uF/10V

+1.8VS — L4105 120Ohm/100Mhz — 40mA/120mA — +DPLL_PVDD — C4160 10uF/10V — C4154 1UF/6.3V — C4155 0.1UF/10V — GND

+3VSG_DELAY — R4157 10KOhm — AC_BATT_Detect — Q4103 2N7002 — [34,35,90] AC_IN_OC# — GND

+1.8VS — R4152 499Ohm 1% r0402 — VGA_VREFG — R4154 249Ohm 1% r0402 — C4103 0.1UF/16V c0402 — GND

+1.8VS — L4107 120Ohm/100Mhz — 20mA — +TSVDD — C4156 10uF/10V — C4175 1UF/6.3V — C4161 0.1UF/10V — GND

+DPLL_PVDD — AF14 — AE14

+DPLL_VDDC — 150Ohm 1% — AD14

GND — R4155 1% — R4196 121Ohm — [7] ATI27M_NOSSC — ATI_27M — AM28 — AK28 — T4146

+1.1VS — L4108 120Ohm/100Mhz — 100mA/300mA — +DPLL_VDDC — C4153 10uF/10V — C4176 1UF/6.3V — C4164 0.1UF/10V — GND

Spread Spectrum

+3VSG — L4133 120Ohm/100Mhz — +3VS_SS — C4101 2.2UF/6.3V — C4102 0.01UF/16V — GND

R4101 0Ohm r0402 — +3VS_SS — VGA_SRS — GND — R4107 0Ohm r0402

R4114 0Ohm r0402 — U4102 P1819B_08SR (XIN, VSS, SRS, ModOUT, XOUT, VDD, PDI#, REF) — +3VS_SS

ATI27M_NOSSC — VGA_SRS — ATI27M_SSC — R4117 22OHM @ r0603_h24 — R4119 121Ohm @ r0603_h24 — ATI_27M

<Variant Name>

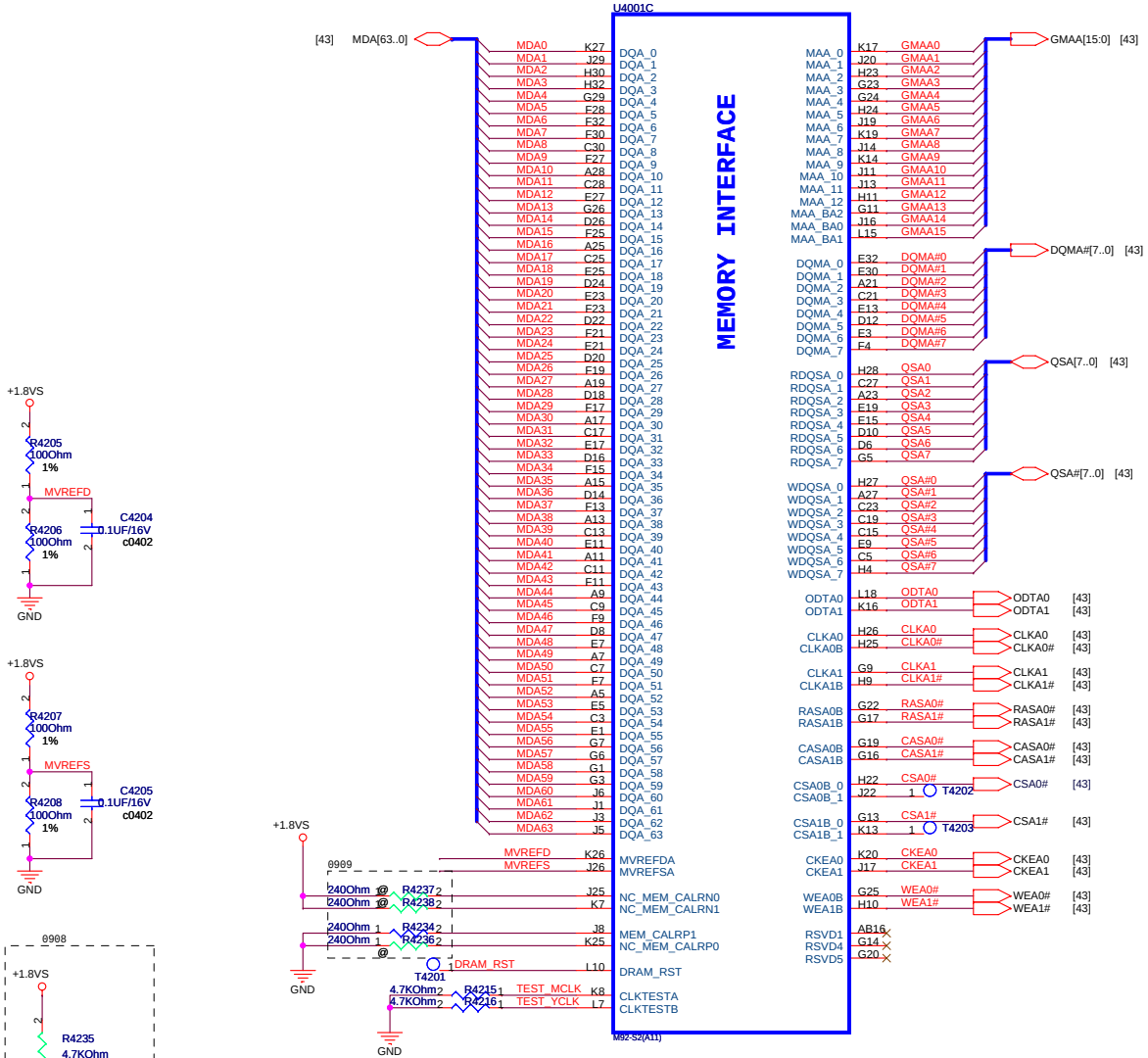
ASUSTeK COMPUTER INC

Title : M92S2-Main(2)

Engineer: Kent Qi

Size: Custom — Project Name: F6Ve — Rev: 1.0

Date: Friday, September 26, 2008 — Sheet 41 of 64



DRAM_RST NC for DDR2

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

<Variant Name>

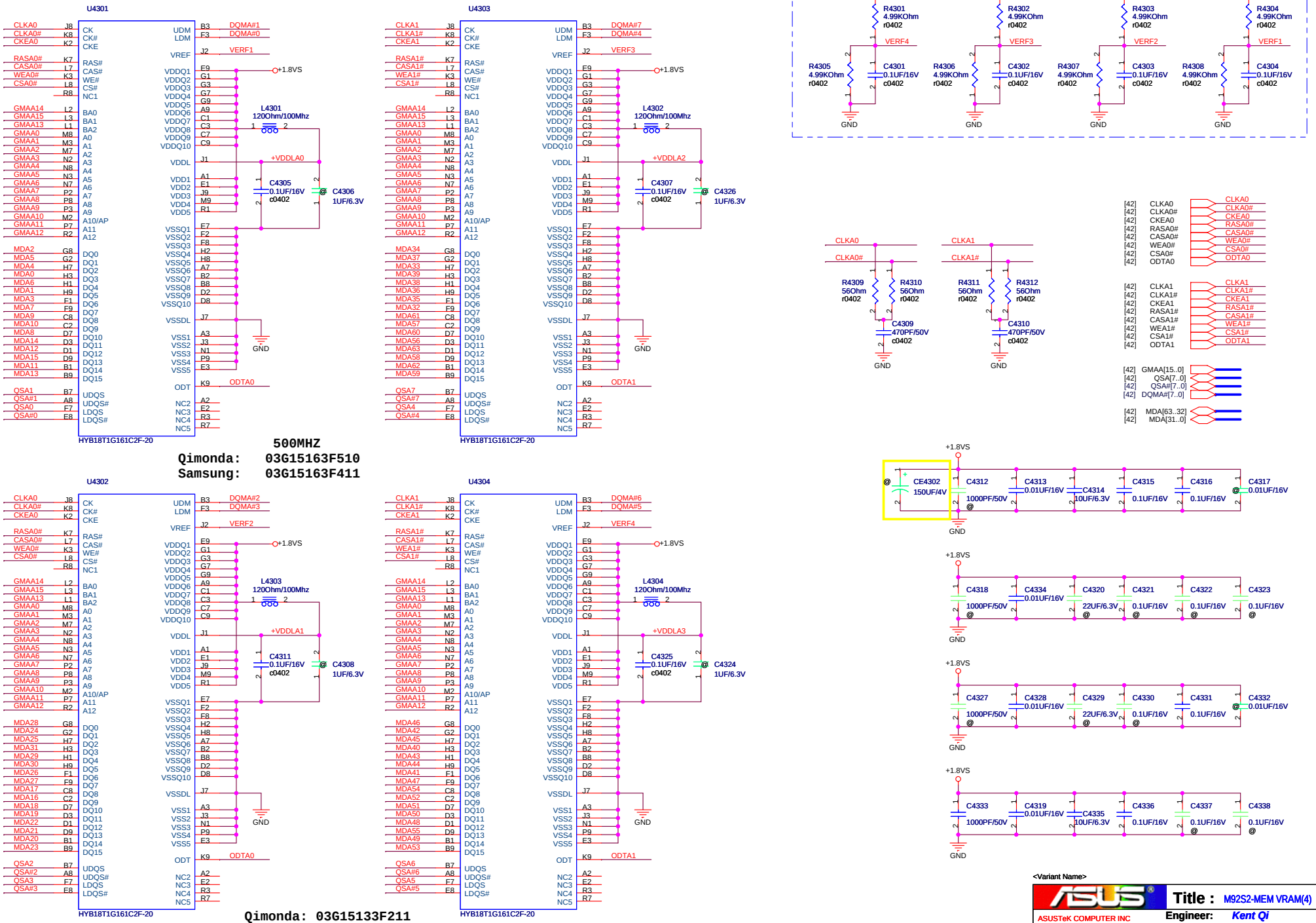
Title : M92S2-MEM CTRL(3)

ASUSTeK COMPUTER INC

Engineer: Kent Qi

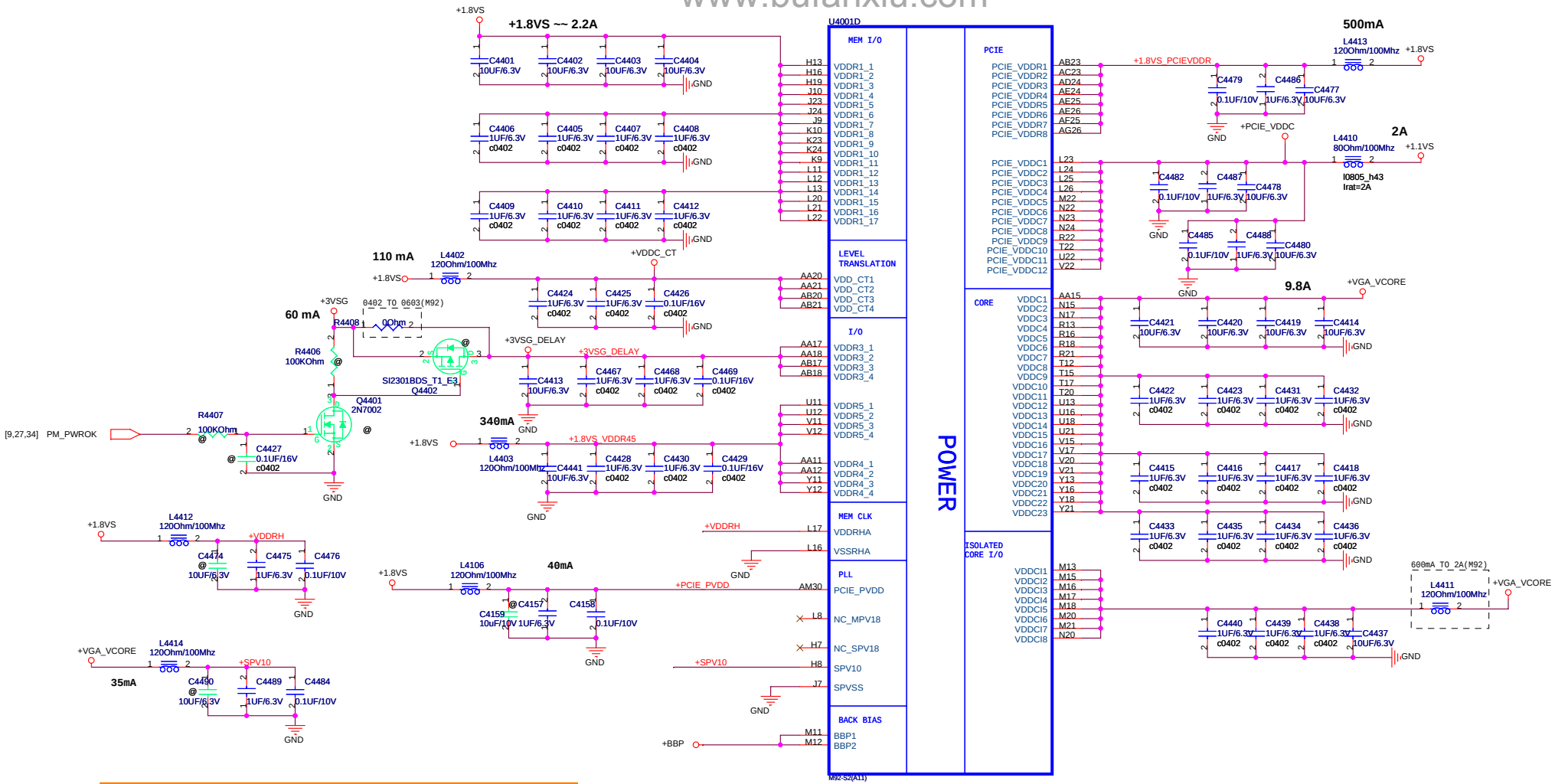
Size	Project Name	Rev
Custom	F6Ve	1.0

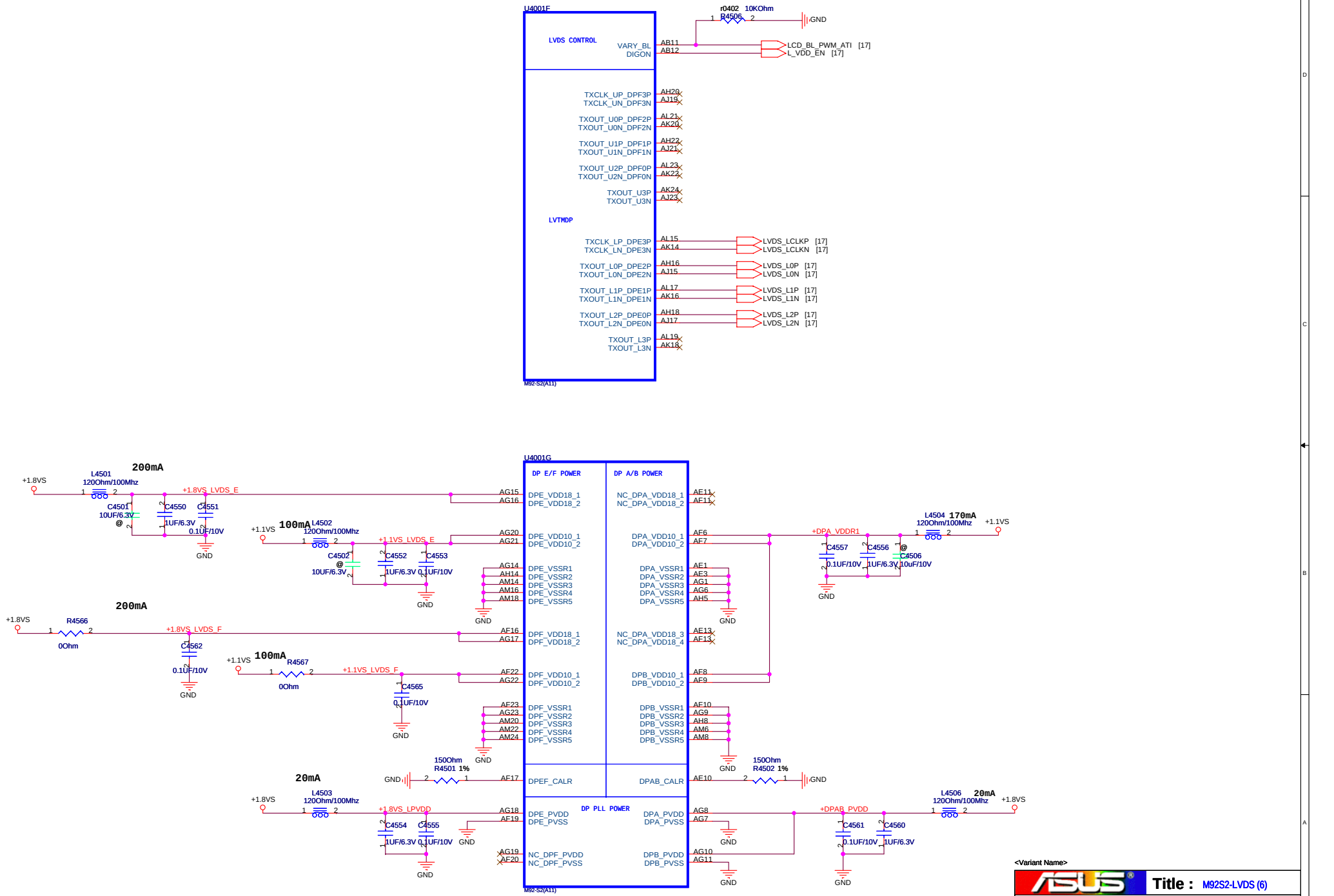
Date: Friday, September 26, 2008 Sheet 42 of 64



<Variant Name>

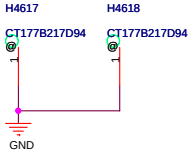
ASUSTeK COMPUTER INC	Title : M92S2-MEM VRAM(4)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 43 of 64	

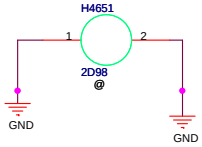


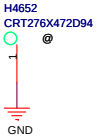


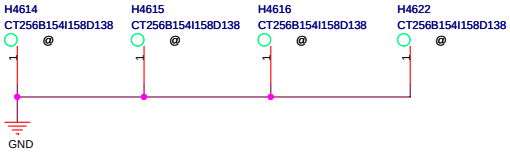
<Variant Name>

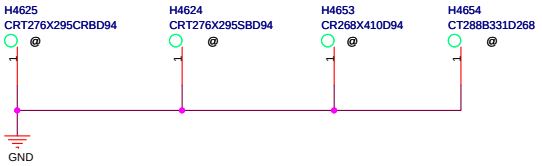
ASUSTeK COMPUTER INC	Title : M92S2-LVDS (6)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 45 of 64	





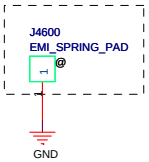


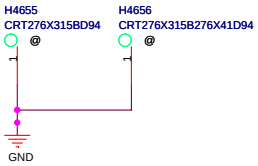


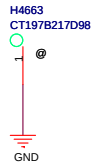


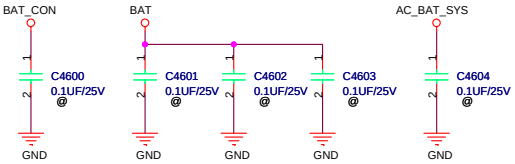
EMI SPRING

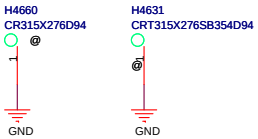
F2J SPRING(H:4.7mm)

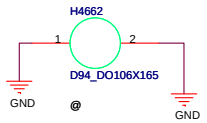


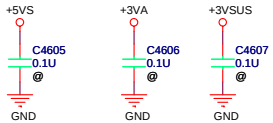


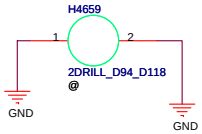


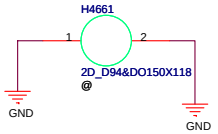


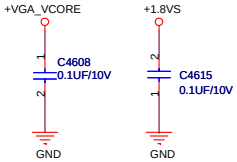


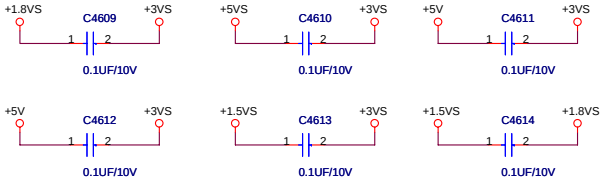




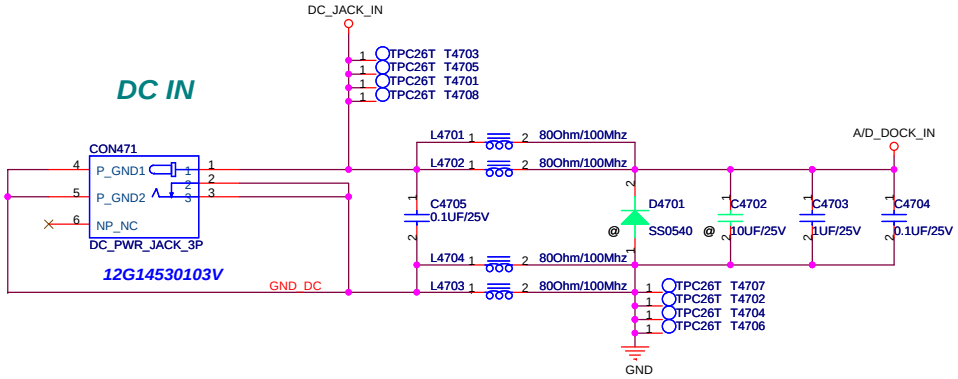




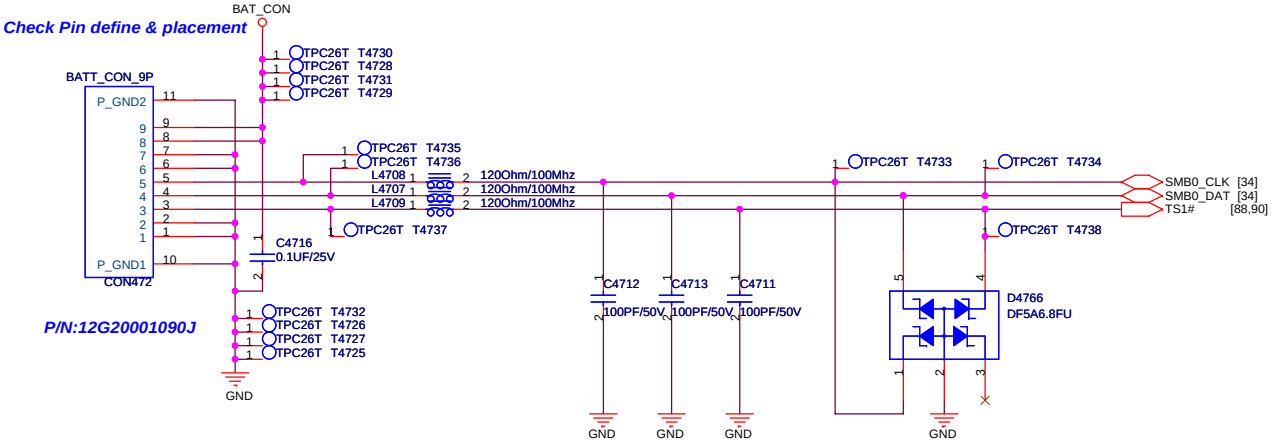




DC IN



BAT IN



<Variant Name>

Title : DC & BAT IN

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

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F6V-->F6Ve modify

9.1.1,Page40~45:Change GPU M82_SE to M92-S2

9.1.2,Page40:change PCIE series capacitance from Y5V to X7Y

9.1.3,Page44:change R4408 R4410 from 0402 to 0603 and change L4411 from 600mA to 2A for current

9.1.4,Page22:change R2002 from 0603 to 0805 for current

9.1.5,Page22:remove R2201 for current

9.2.1,Page36:reserved R3660 for crystal X3603

9.2.2,Page34:place R3439 for MARATHON# pull up +3VA_EC

9.2.3,Page17:remove F1702(INVERTER Pin19) for cost down

9.2.4,Page12:add R1210 and C1243 for VCCD_QDAC to 1.5VS

9.2.5,Page33:add R3309 for PCIE_WAKE

9.4.1,Page43:change same net name to divided different name, +1.8Vs_LVDS-->+1.8Vs_LVDS_E
and +1.8Vs_LVDS_F, +1.1Vs_LVDS-->+1.1Vs_LVDS_E and +1.1Vs_LVDS_F

9.4.2,Page41:change R4188 to 0603 for current

9.5.1,Page40:remove PCIE_[8..15] for layout

9.5.2,Page41:Place R4140 R4142 prevent can not link

9.5.3,Page41:reserved Q4103 R4157 for AC_BATT_Detect

9.8.1,Page41:move memory ID from DPVDATA[0..3] to DPVDATA[20..23]

9.8.2,Page41:reserved R4235 for DRAM_RST pull up

9.8.3,Page41:reserved R4120,connect GPIO_17_thermal to EC for thermal protect.

9.9.1,Page29:change L2904 L2903 to R2900 R2901

9.9.2,Page17:change R1717 from 100K to 10K,change R1718 from 1M to 10K

9.9.3,Page42:reserved R4237 R4238 for pull up NC_MEM_CALRN0 and NC_MEM_CALRN1 to +1.8VS,
reserved R4236 for pull down NC_MEM_CALRP0 to ground

9.9.4,Page17:reserved R4159 R4160 for GPIO_TRSTB and PCIE_GPIO2 pull down

9.18.1,Page41:reserved R4161 for GPIO_23_CLKREQB pull up.

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer:	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 48 of 64	

<Variant Name>

Title : History(2)

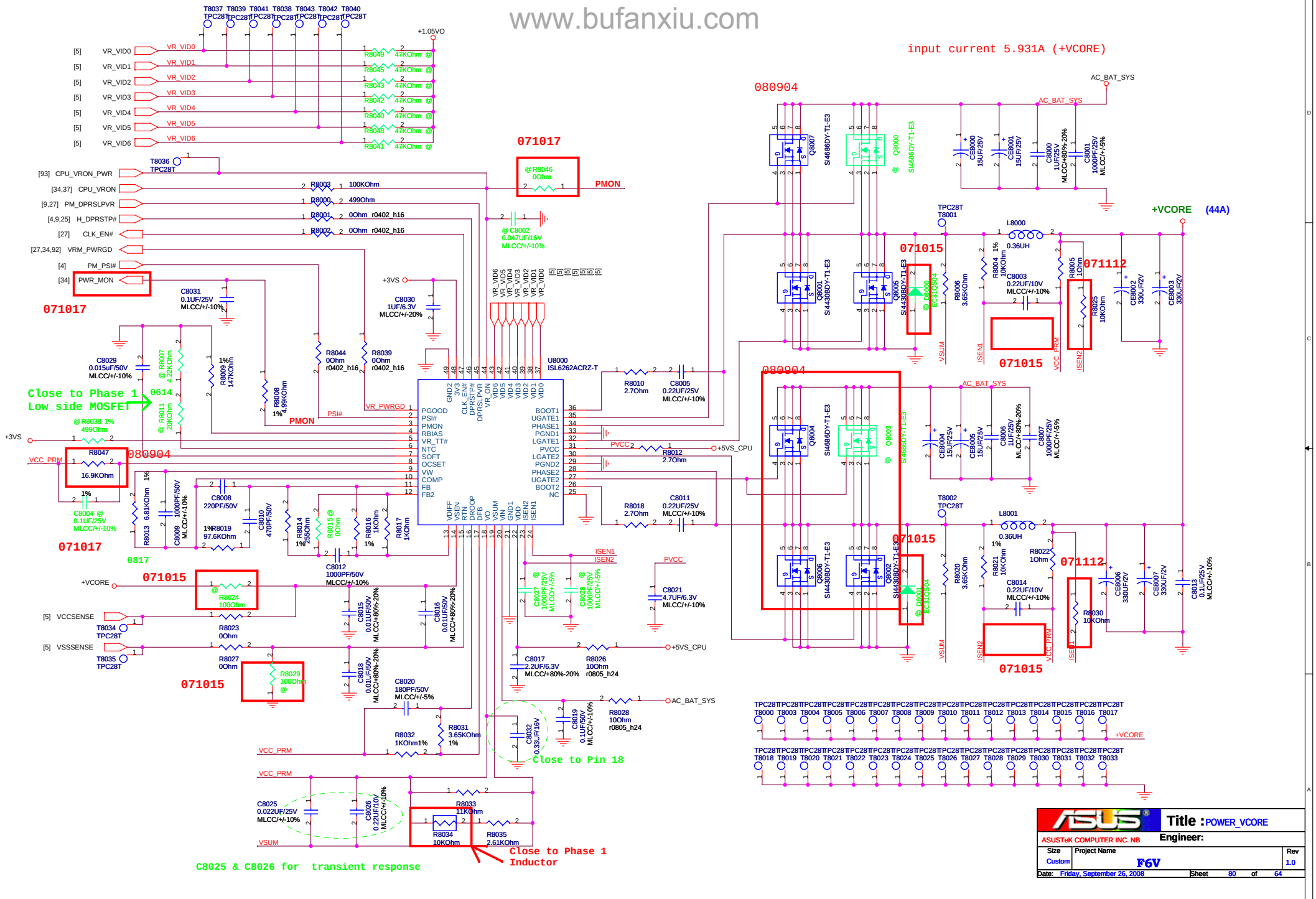
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 49 of 64

input current 5.931A (+VCORE)



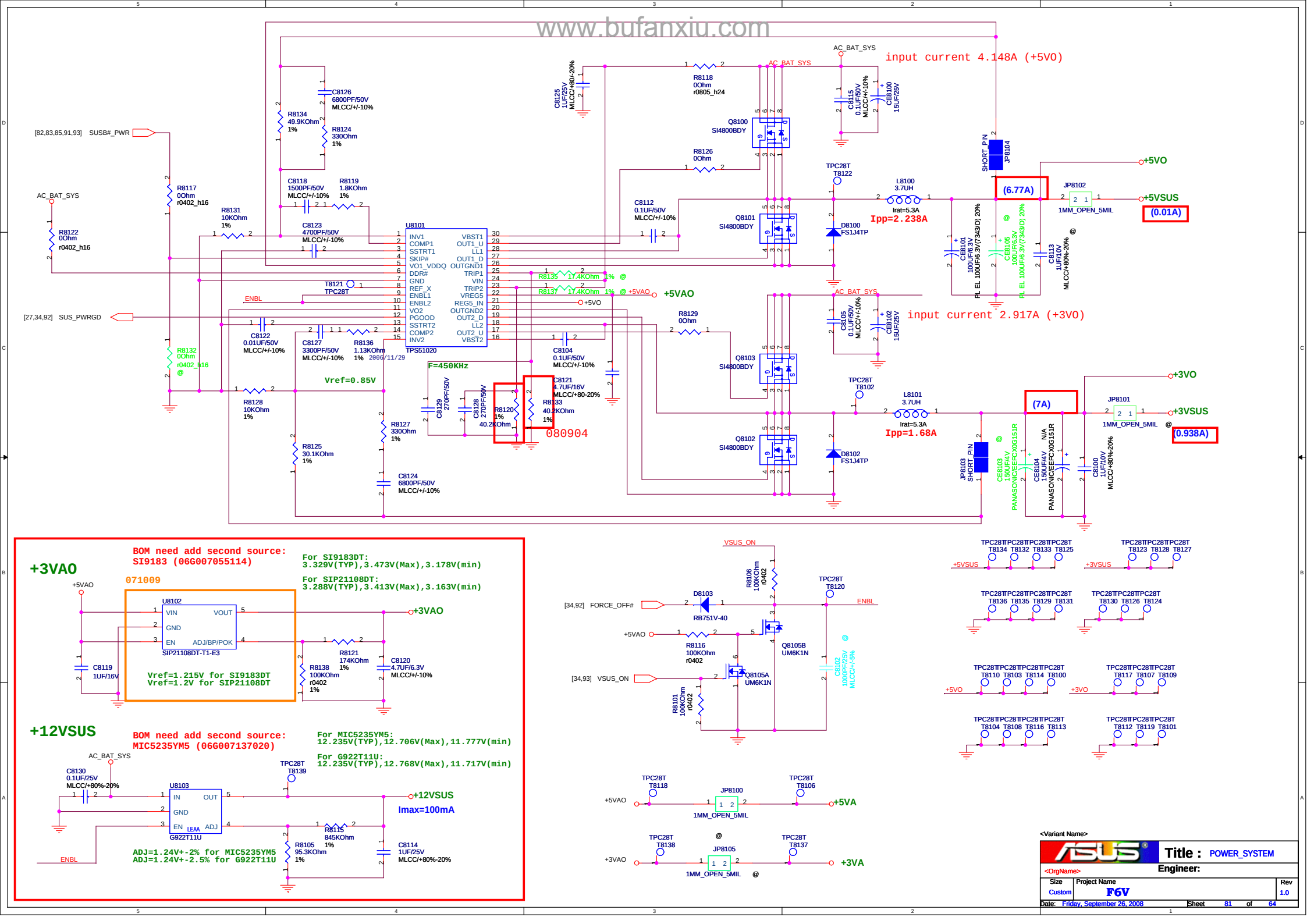
ASUSTeK COMPUTER INC. NB

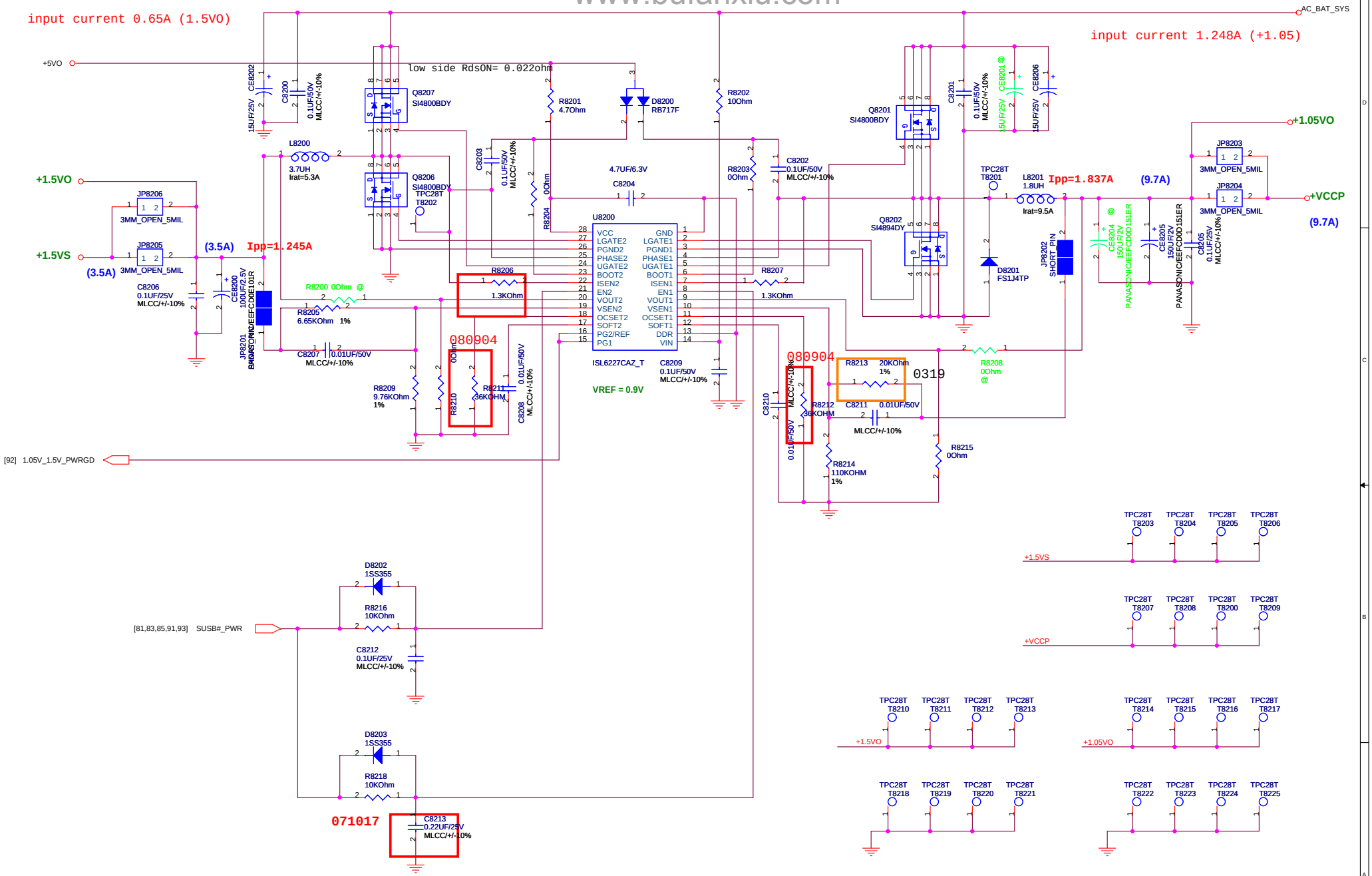
Title : POWER_VCORE

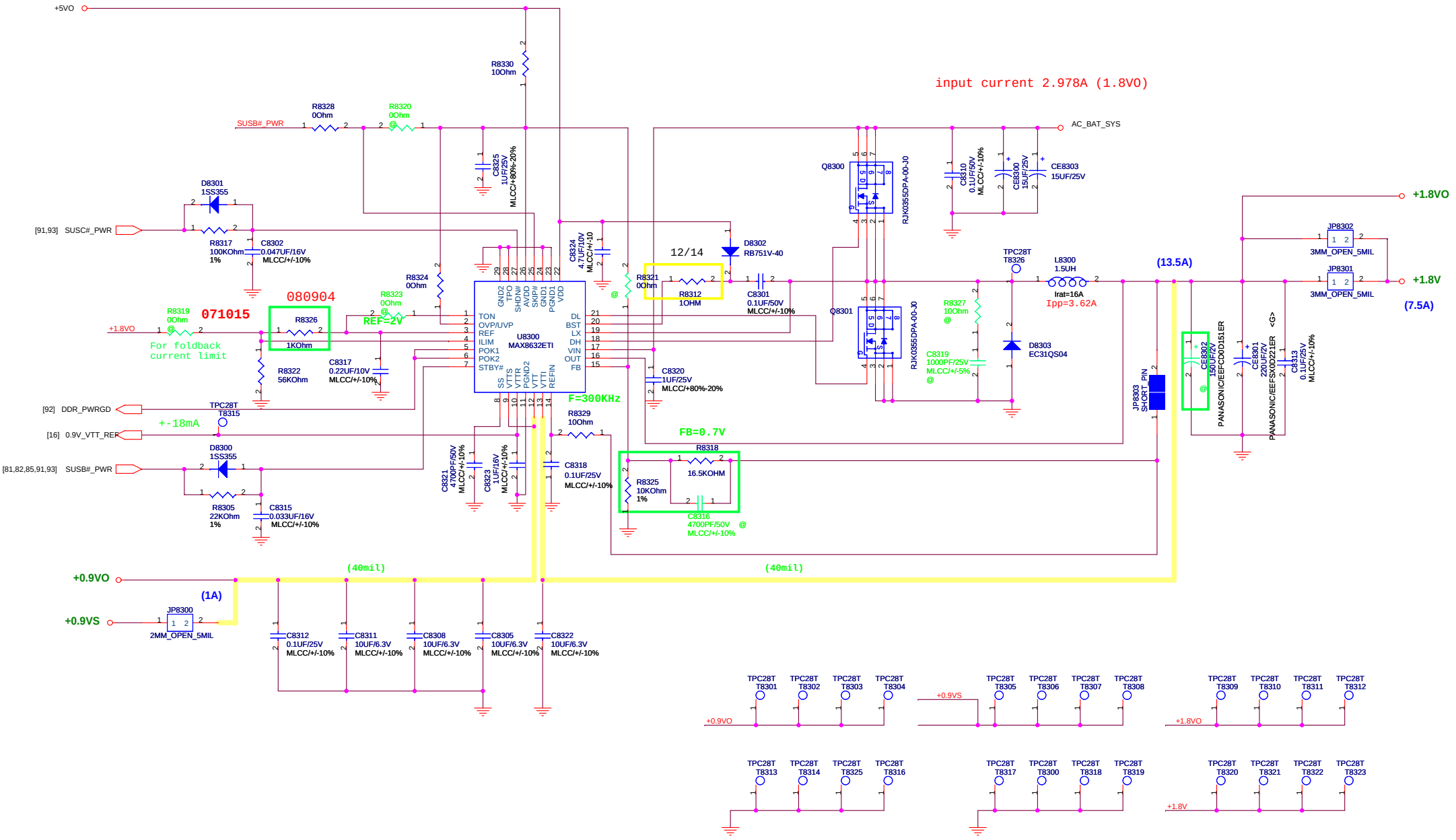
Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

Date: Friday, September 26, 2008 Sheet 80 of 64







<Variant Name>

Title : POWER_I/O_DDR & VTT

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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<Variant Name>

Title : POWER_I/O_+3VAO

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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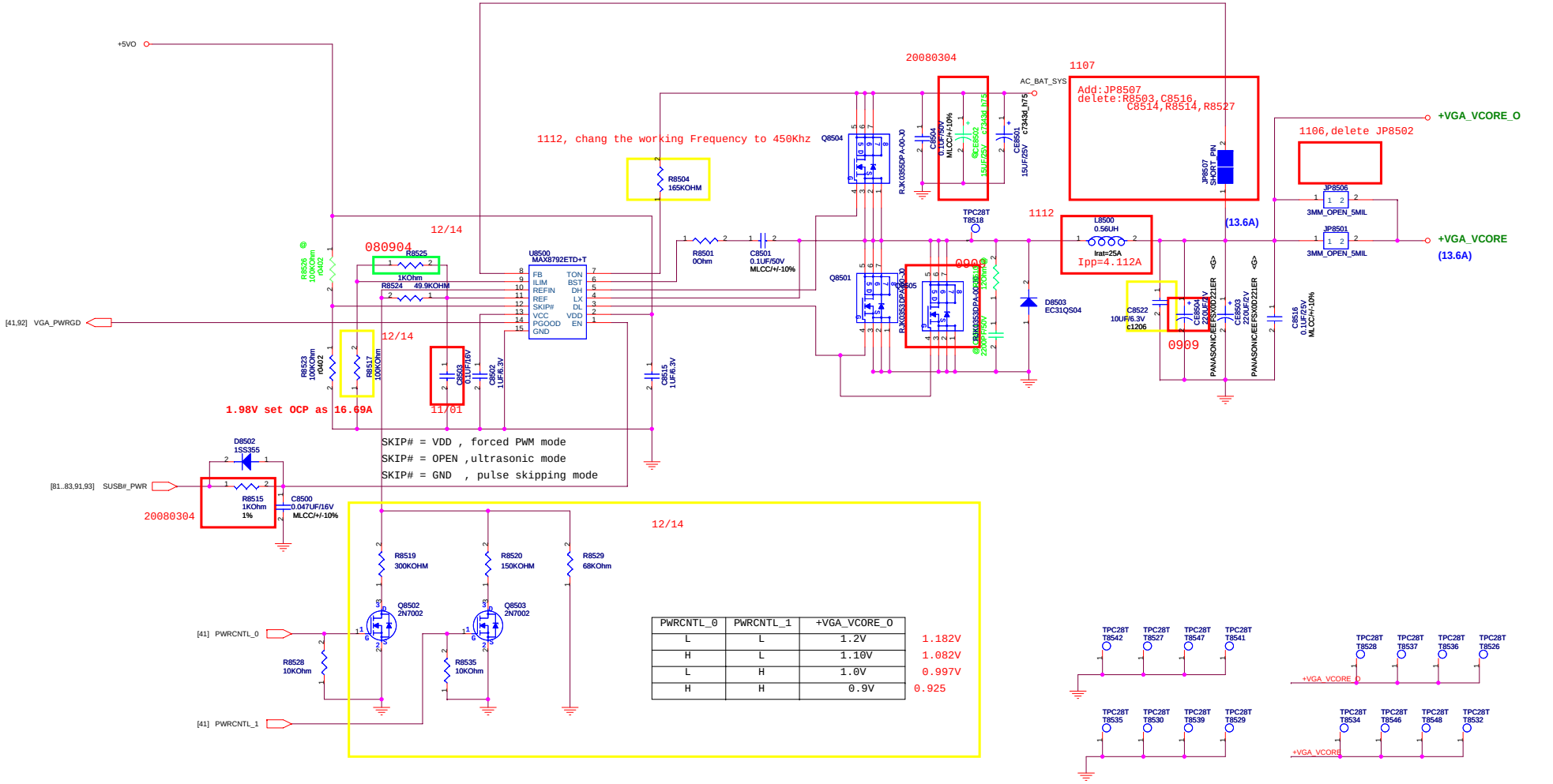
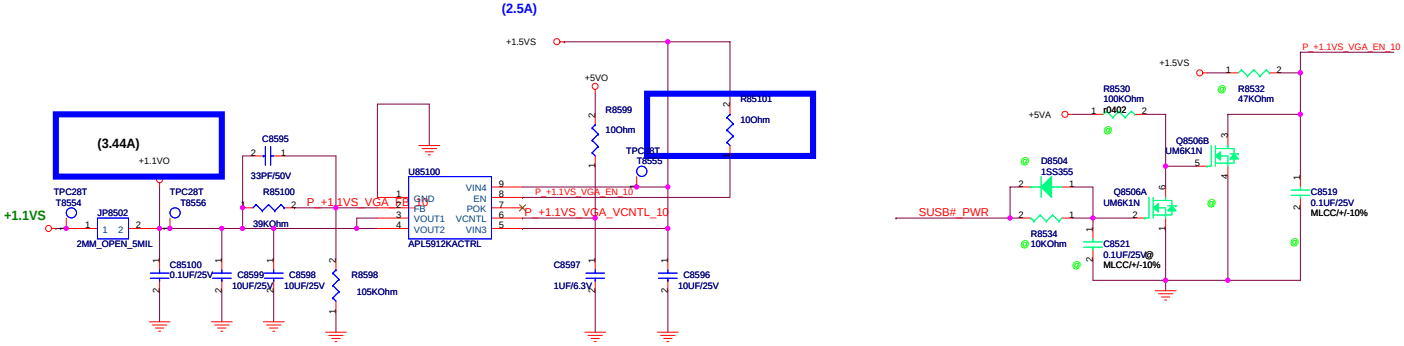
071017





Title :	POWER_VGACORE_1.1VO		
ASUSTECH	Engineer:		
Size: C	Project Name: F6V		Rev: 1.0
Date: Friday, September 26, 2008	Sheet 85 of 64		

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
B	F6V	1.0

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<Variant Name>

Title : POWER_SHUTDOWN#

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
Custom	F6V	1.0

Date: Friday, September 26, 2008 Sheet 87 of 64

POWER PATH & BAT_LEARN

90 WATT

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R5710=20K,R5715=30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA

LDO : 5.4V
REF : 4.2235V

90W->30K Ohm
65W->137K Ohm

90W->10m Ohm
65W->20m Ohm

071015

070115

0614

0319

4S: Mount R8808 only
3S: Unmount all components
3S/4S: Unmount R8808, and mount others

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

BAT

BAT_CON

<Variant Name>

Title : POWER_CHARGER

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

Date: Friday, September 26, 2008 Sheet 88 of 64

<Variant Name>

Title : N/A

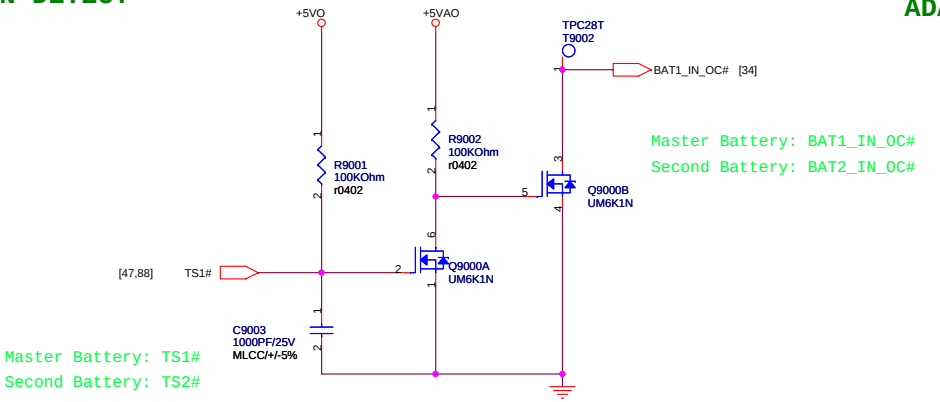
ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F6V	1.0

Date: Friday, September 26, 2008 Sheet 89 of 64

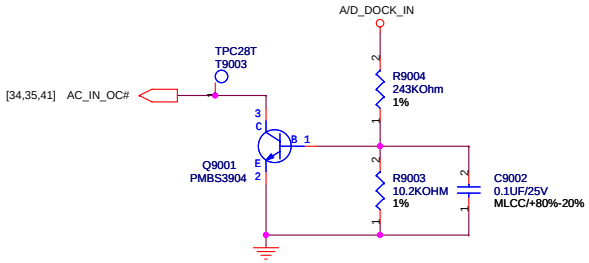
BATTERY IN DETECT



Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT



+2.5VREF

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_DETECT

Engineer: Ray

Size	Project Name	Rev
Custom	F6V	1.0

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SUSB#_PWR POWER

20080304

+1.8VO — TPC28T T9125, TPC28T T9110 — Q9100 FDW2501NZ_NL (DRAIN_1, DRAIN_2, SOURCE_1, SOURCE_2, SOURCE_3, SOURCE_4, GATE_1, GATE_2) — TPC28T T9100, TPC28T T9122 — +1.8VS (5.1A)

R9111 1KOhm 1%

C9111 0.1UF/25V MLCC/+/-10%

20080326

C9100 0.22UF/16V MLCC/+/-10%

071015

+3VO — TPC28T T9104, TPC28T T9118 — Q9108 SI4800BDY — TPC28T T9109, TPC28T T9114 — +3VS (4.2A)

R9108 47KOhm r0402_h16

C9104 0.1UF/25V MLCC/+/-10%

C9102 0.1UF/25V MLCC/+/-10%

+5VO — TPC28T T9105, TPC28T T9115 — Q9106 FDW2501NZ_NL — TPC28T T9101, TPC28T T9127 — +5VS (4.65A)

R9107 47KOhm r0402_h16

C9109 0.033UF/16V MLCC/+/-10%

C9107 0.1UF/25V MLCC/+/-10%

JP9100 SHORT_PIN — +5VS_FAN

JP9101 SHORT_PIN — +5VS_CPU

R9112 47KOhm 1%

0607

0607

+12VSUS — TPC28T T9128, TPC28T T9129 — Q9105 UMC4N — TPC28T T9102 — +12VS

SUSB#_PWR

R9102 100KOhm 1%

SUSC#_PWR POWER

071015

+3VO — TPC28T T9111, TPC28T T9133 — Q9103 SI4800BDY

R910 22KOhm 1%

C9106 0.1UF/25V MLCC/+/-10%

C9110 0.1UF/25V MLCC/+/-10%

+5VO — TPC28T T9117, TPC28T T9132 — Q9101 FDW2501NZ_NL — TPC28T T9124, TPC28T T9113 — +5V (2.1A)

R9110 22KOhm 1%

C9113 0.1UF/25V MLCC/+/-10%

C9105 0.033UF/16V MLCC/+/-10%

R9106 22KOhm 1%

+12VSUS — TPC28T T9120 — Q9107 UMC4N — TPC28T T9112 — +12V

TPC28T T9119

SUSC#_PWR

1% R9103 100KOhm

071015

[33,34,37,92] SUSB_EC# — TPC28T T9131 — R9105 1KOhm — TPC28T T9135

[81..83,85,93] SUSB#_PWR

[34,37] SUSC_EC# — TPC28T T9121 — R9104 1KOhm — TPC28T T9134

[83,93] SUSC#_PWR

ASUSTeK COMPUTER INC. NB

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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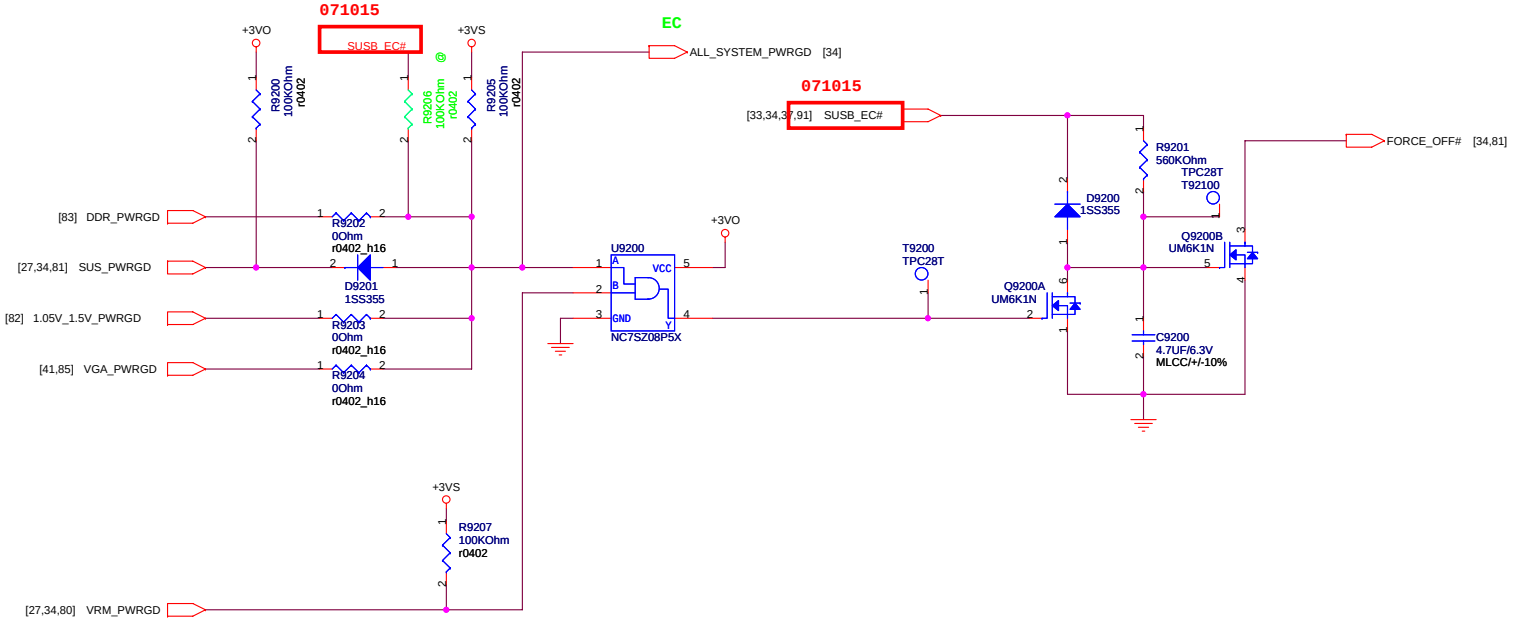
POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_PROTECT

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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AC_BAT_SYS → AC_BAT_SYS [46,80..83,85,88]
BAT → BAT [46,88]
BAT_CON → BAT_CON [46,47,88]

+3VA → +3VA [17,25,34,37,46,81]
+5VAO → +5VAO [81,90]
+5VO → +5VO [81..83,85,90,91]
+5VSUS → +5VSUS [28,39,81]
+5V → +5V [17,24,37,91]
+5VS → +5VS [18,19,22,23,28,33,37..39,46,91]
+3VO → +3VO [81,91,92]
+3VSUS → +3VSUS [17,20,22,25..29,34,39,46,81]
+3V → +3V [19..22,26,29,33,35..38,91]
+3VS → +3VS [4,6,7,9,12..15,17..23,25..31,33,34,37,39,44,80,91,92]

+12VSUS → +12VSUS [81,91]
+12V → +12V [22,24,36,37,91]
+12VS → +12VS [17,19,31,37,44,91]

+1.8VO → +1.8VO [83,91]
+1.8V → +1.8V [9,11,14..16,37,83]

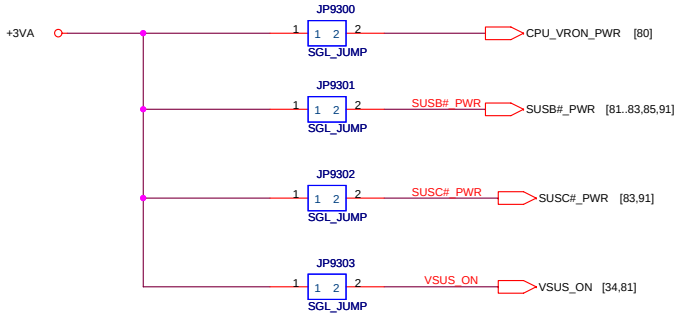
+0.9VS → +0.9VS [16,37,83]
+0.9VO → +0.9VO [83]

+1.05VO → +1.05VO [80,82]
+VCCP → +VCCP [6..9,11,12,25,28,37,82]
+1.5VO → +1.5VO [82]
+1.5VS → +1.5VS [5,12,20,28,33,37,82,85]

+VCORE → +VCORE [5,6,37,80]

+VGA_VCORE → +VGA_VCORE [37,44,85]
+1.8VS → +1.8VS [37,41..45,91]
+1.1VS → +1.1VS [37,41,44,45,85]

FOR POWER TEST



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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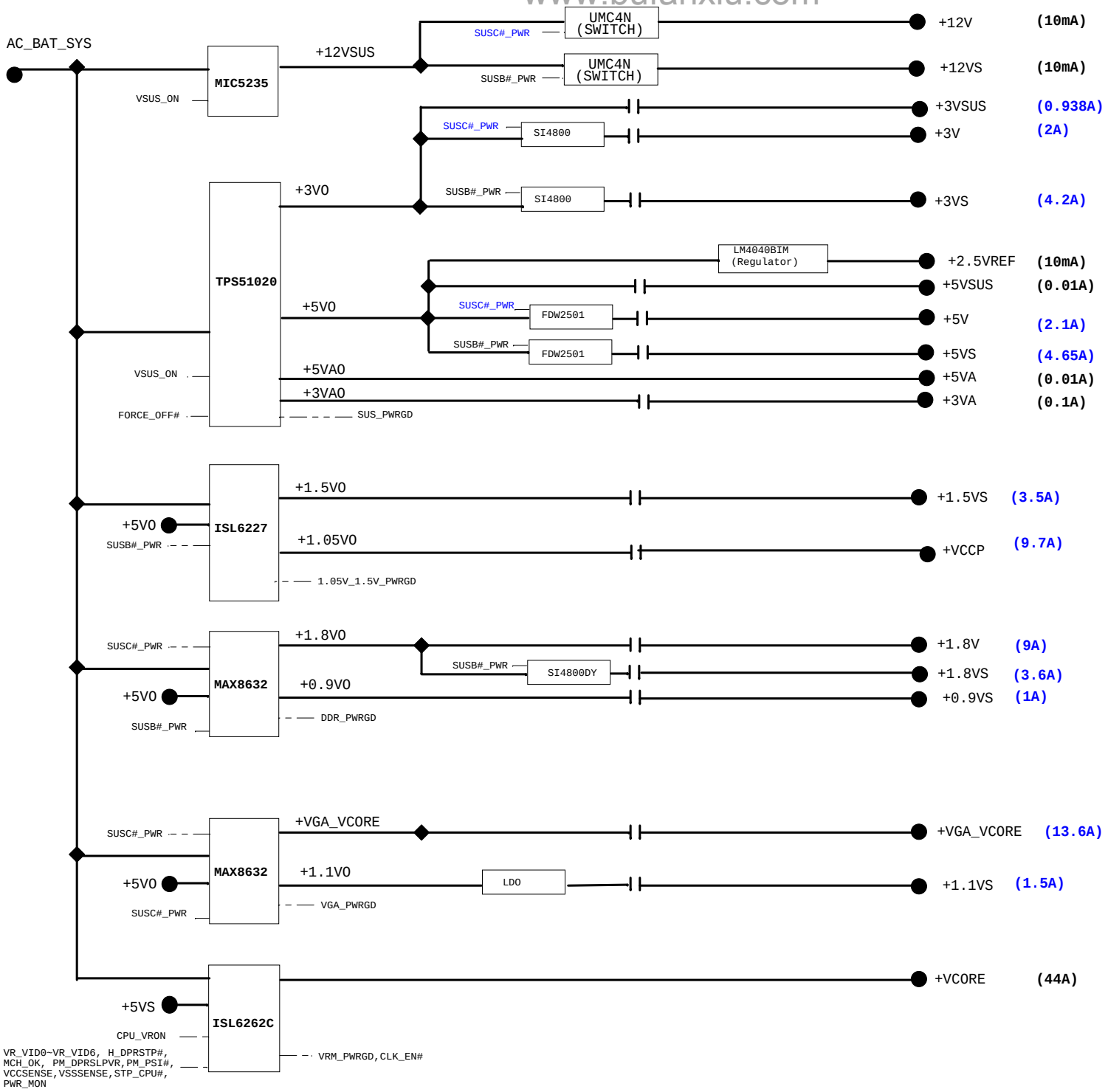

<Variant Name>

Title : POWER_FLOWCHART

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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