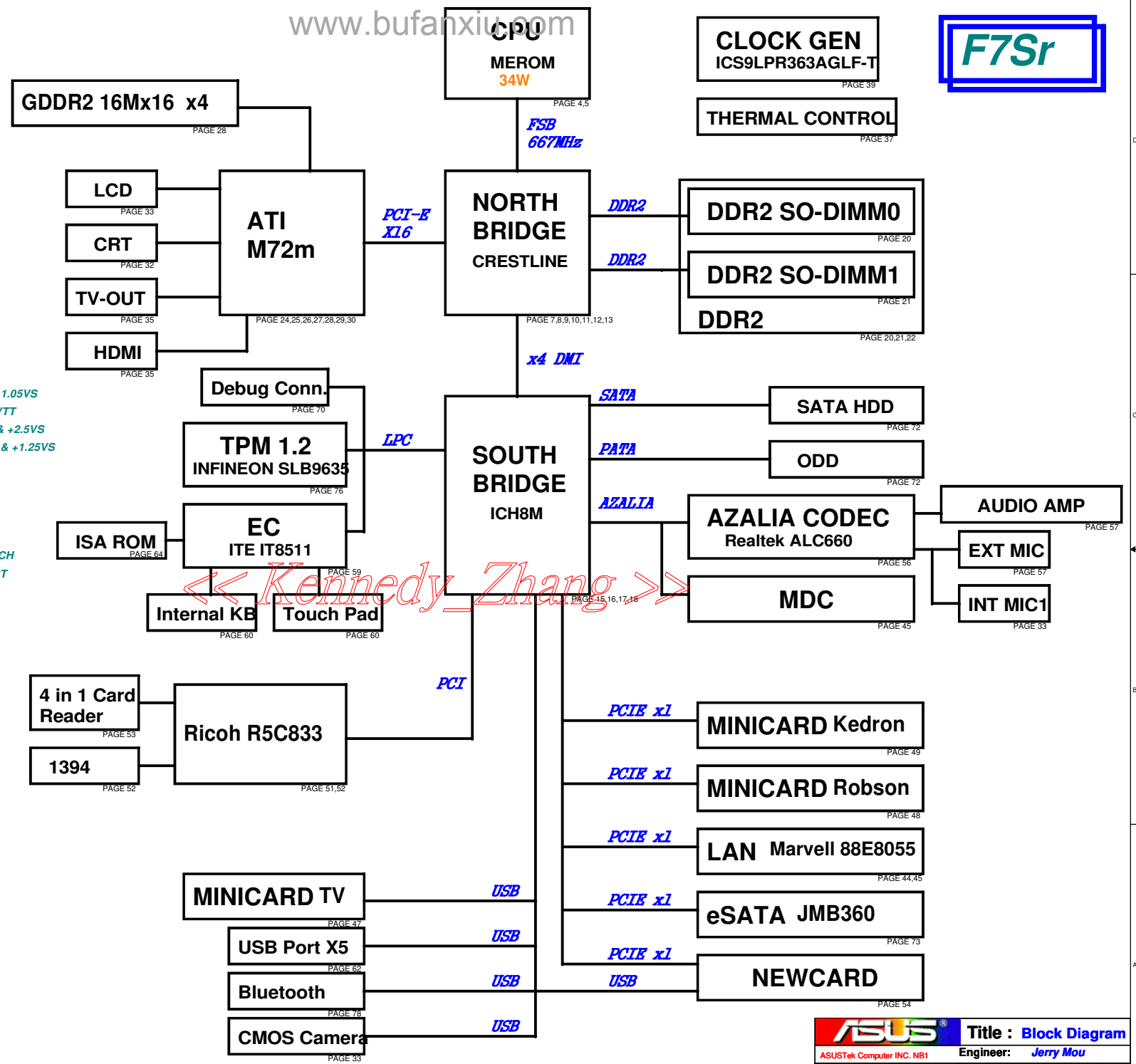




01	Block Diagram	61	*
02	System Setting	62	USB CONN
03	*	63	*
04	04_CPU-Merom(HOST)	64	ISA ROM
05	05_CPU-Merom(PWR)	65	SPI ROM
06	*	66	LED
07	07_CRESTLINE(HOST)	67	*
08	08_CRESTLINE(DMI & CFG)	68	DC & BAT IN
09	09_CRESTLINE(GRAPHIC)	69	*
10	10_CRESTLINE(DDR2)	70	Debug CONN.
11	11_CRESTLINE(PWR)	71	*
12	12_CRESTLINE(PWR2)	72	SATA-HDD & ODD
13	13_CRESTLINE(GND)	73	eSATA
14	*	74	SREW HOLE
15	15_SB-ICH8M(1)	75	*
16	16_SB-ICH8M(2)	76	TPM
17	17_SB-ICH8M(3)	77	SPRING_PAD
18	18_SB-ICH8M(PWR)	78	BT
19	*	79	POWER SEQUENCE
20	20_DDR2 SO-DIMM0	80	POWER_VCORE
21	21_DDR2 SO-DIMM1	81	POWER_SYSTEM
22	22_DDR2 TERMINATION	82	POWER_I/O_1.5VS & 1.05VS
23	*	83	POWER_I/O_DDR & VTT
24	24_VGA_ATL_M7X/66-M_MAIN(1)	84	POWER_I/O_+3VAO & +2.5VS
25	25_VGA_ATL_M7X/66-M_Memory(2)	85	POWER_VGA_CORE & +1.25VS
26	26_VGA_ATL_M7X/66-M_PCI-E(3)	86	N/A
27	VGA_ATL_M7X/66-M_POWER(4)	87	N/A
28	VGA_ATL_M7X/66-M_VRAM_A(5)	88	POWER_CHARGER
29	VGA_ATL_M7X/66-M_VRAM_B(6)	89	N/A
30	VGA_SPI_ROM (7)	90	POWER_DETECT
31	*	91	POWER_LOAD SWITCH
32	CRT	92	POWER_FLOWCHART
33	LVDS & INVERTER CONNECTOR	93	POWER_PROTECT
34	*	94	POWER_SIGNAL
35	TV OUT CONN	95	History
36	*		
37	THEIR SENSOR & FAN		
38	*		
39	CLOCK GEN-ICS9LPR363AGLF-T		
40	*		
41	Power on & Reset Freq.		
42	DISCHARGE		
43	*		
44	LAN-L1		
45	MDC & RJ45+11		
46	*		
47	MINI CARD-TV/Windigo		
48	MINI CARD-Robson		
49	MINI CARD-Kedron		
50	*		
51	CARD1394-R5C833(1)		
52	CARD1394-R5C833(2)		
53	4 in 1 CARD READER		
54	NEWCARD		
55	*		
56	CODEC-ALC660		
57	AUDIO AMP & JCAK		
58	Sequence Control Logic		
59	IT8511TE		
60	Touch Pad & KB		



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### EC\_IT8511TE SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRLED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	I
31	ECSC#/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	PM_SLP_M#	
110	PS2CLK0/GPF0	WALN_SW#	
111	PS2DAT0/GPF1	ME_ALERT#	
114	PS2CLK1/GPF2	/	I/O
115	PS2DAT1/GPF3	/	I/O
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	FA19	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80HL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
8	GPL0	PM_S4_STATE#		152	GP12		
11	GPL1	S4_STATE_ON	O	155	GPI3	CHG_EN#	O
12	GPL2	SLP_M_ON	O	168	GPI5	EC_CLK_EN	O
20	GPL3	EC_WLAN_PWR	O	85	KS016/GPM2	NETDETECT	O
21	GPL4	MP_PWRGD	I				
48	GPH0	VSUS_ON	I				
54	GPH1	VSUS_GD#	O				
55	GPH2	CPUPWR_GD#	O				
69	GPH3	PM_PWRBTN#	O				
70	GPH4	SUSC_ON	O				
75	GPH5	SUSB_ON	O				
76	GPH6	CPU_VRON	O				
105	GPH7	PM_RSMRST#	O				
148	GPI0	ICH8_PWROK	O				
149	GPI1	ALL_SYSTEM_PWRGD	I				

### ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
AG12	GPIO0/BM_BUSY#	PM_BMBUSY#	I	AG16	GPIO40/OC#1	USB_CON_OC01#	I
AJ8	GPIO1/TACH1	EXTSMI#	I	AG15	GPIO41/OC#2	USB_CON_OC23#	I
F8	GPIO2/PIRQE#	PCI_INTE#	I	AE15	GPIO42/OC#3	USB_CON_OC23#	I
G11	GPIO3/PIRQF#	PCI_INTF#	I	E18	GPIO50/REQ1#	PCI_REQ#1	
F12	GPIO4/PIRQG#	PCI_INTG#	I	C18	GPIO51/GNT1#	PCI_GNT#1	
B3	GPIO5/PIRQH#	PCI_INTH#	I	B19	GPIO52/REQ2#	PCI_REQ#2	
AJ9	GPIO6/TACH2	BIOS_REC	I/O	F18	GPIO53/GNT2#	PCI_GNT#2	
AH9	GPIO7/TACH3	WLAN_LED_EN	I	A11	GPIO54/REQ3#	PCI_REQ#3	
AE16	GPIO8	BT_ON#	I	C10	GPIO55/GNT3#	PCI_GNT#3	
AG19	GPIO9/WOL_EN	LAN_WOL_EN	I				
AJ24	GPIO10/CLGPIO1	ME_ALERT#	O				
AG22	GPIO11/SMBALERT#	SMB_ALERT#	I				
AC19	GPIO12	KBC_SC#	I				
AH21	GPIO13/GLAN_DOCK#						
AF22	GPIO14/CLGPIO2	NETDETECT					
AE20	GPIO15/STP_PCI#	STP_PCI#	I/O				
AJ14	GPIO16/DPRSLPVR	PM_DPRSLPVR	O				
AG8	GPIO17/TACH0	WLAN_ON#	O				
AH12	GPIO18	TP_LEDON	O				
AJ10	GPIO19/SATA1GP	PCB_ID0	I				
AE11	GPIO20	BTLED_ON	O				
AJ12	GPIO21/SATA0GP	CPU_Select	I				
AG10	GPIO22/SCLOCK	3G_ON#	I				
E6	GPIO23/LDRQ1#	LPC_DRQ#1	I/O				
AJ27	GPIO24/CLGPIO0						
AG18	GPIO25/STP_CPU#	STP_CPU#					
AH27	GPIO26/S4_STATE#	PM_S4_STATE#					
AH25	GPIO27/QRT_STATE0	BT_DET#	I				
AD16	GPIO28/QRT_STATE1	CB_SD#					
AG17	GPIO29/OC#5	USB_CON_OC5#	I				
AD12	GPIO30/OC#6	NEWCARD_OC#	I				
AJ18	GPIO31/OC#7	USB_OC#7	I				
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	O				
AE10	GPIO33/AZ_DOCK_EN#		O				
AG14	GPIO34/AZ_DOCK_RST#						
AG13	GPIO35/SATACLKREQ#	GPO35	O				
AF11	GPIO36/SATA2GP	PCB_ID1					
AG11	GPIO37/SATA3GP	PCB_ID2	I/O				
AF9	GPIO38/SLOAD	GPI38	I				
AJ11	GPIO39/SDATAOUT0	GPI39	I				
AD10	GPIO48/SDATAOUT1	PCI_GNT#4	O				
AG29	GPIO49/CPUPWRGD	H_PWRGD	O				

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

PCIe Device	Bus	PCIe Device	Bus
LAN	PE(T/R)(p/n)1	Robson	PE(T/R)(p/n)4
Kedron	PE(T/R)(p/n)2	NEWCARD	PE(T/R)(p/n)5
eSATA	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)6

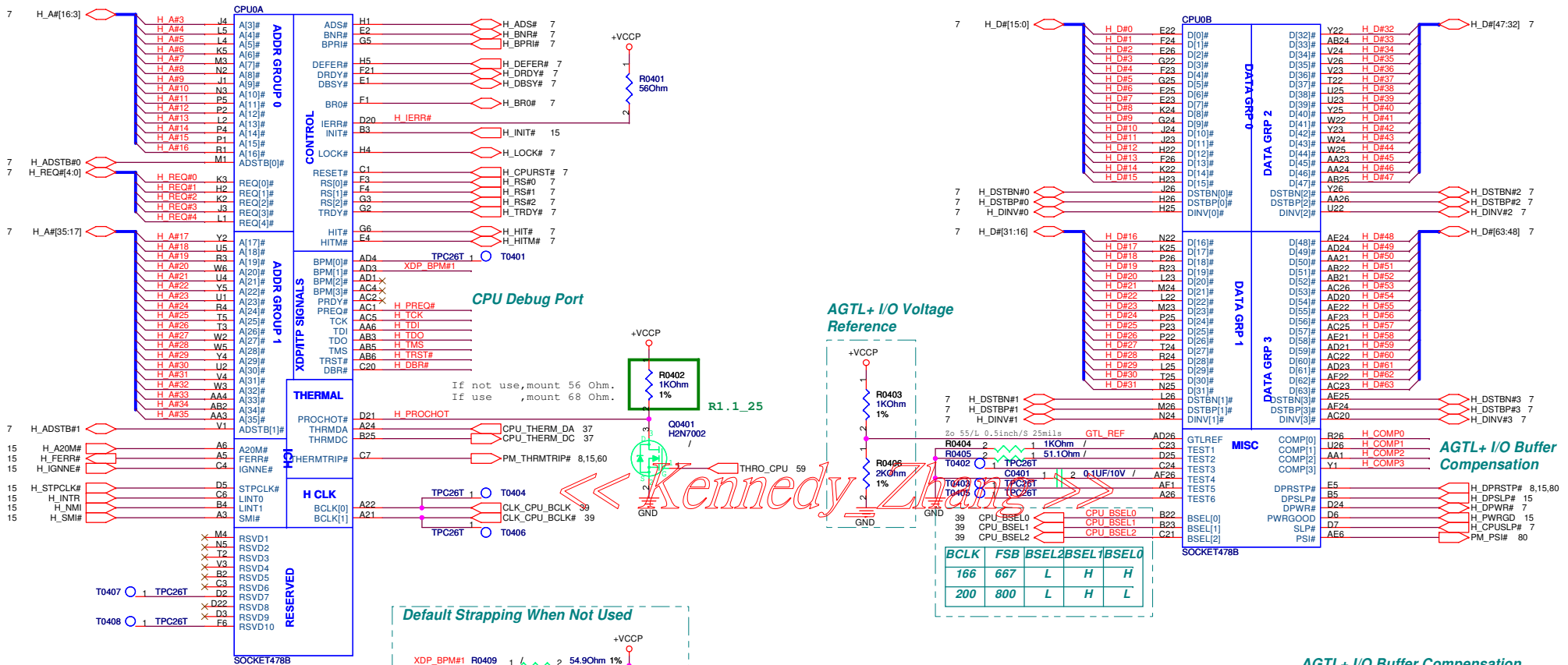
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
CPU Thermal Sensor(MAX6657)	0100110x ( 4C )
VGA Thermal Sensor(MAX6657)	0100110x ( 4C )

### ICS9LPR363AGLF-T SETTING

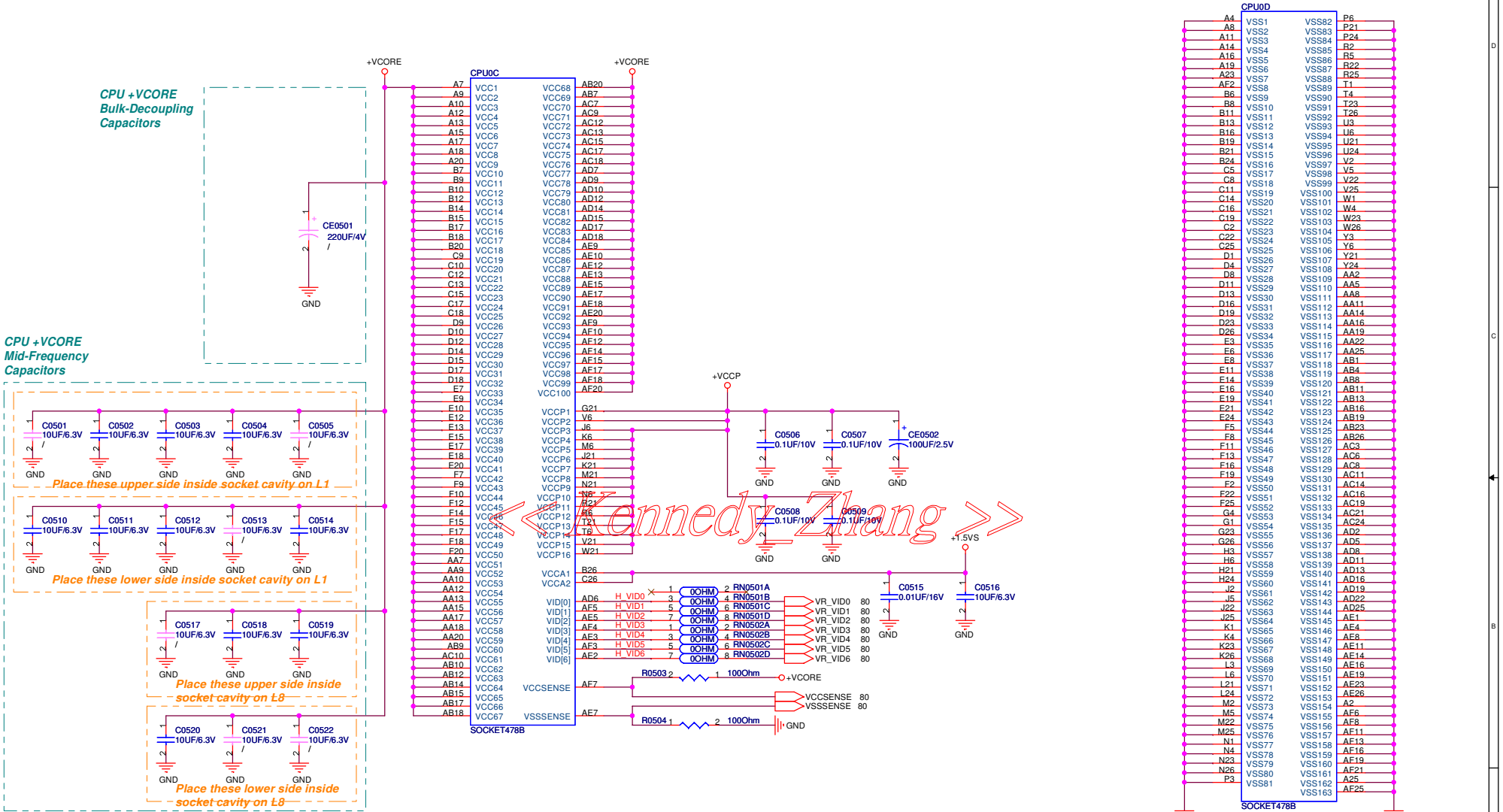
Pins	Pin Name	Device
3	PCICLK1	TPMPCI
4	PCICLK2	CardBus R5C832
5	SELPCIEX0_LCD#PCICLK3	EC IT8511E
8	ITP_EN/PCICLK_F0	ICH8
15	DOTC_96MHzL	X
14	DOTT_96MHzL	X
12	FSLA/USB_48MHz	ICH8
19	PCIeT_L1	eSATA
20	PCIeC_L1	eSATA
36	PCIeT_L5	M66M
35	PCIeC_L5	M66M
39	PCIeT_L6	MiniCard(Rob)
38	PCIeC_L6	MiniCard(Rob)
22	PCIeT_L2	ICH8
23	PCIeC_L2	ICH8
24	PCIeT_L3	MCH
25	PCIeC_L3	MCH
26	SATACLKT_L	ICH8
27	SATACLKC_L	ICH8
44	CPUITPT_L2 / PCIeT_L8	LAN
43	CPUITPC_L2 / PCIeC_L8	LAN
14	27FIX/LCD_SSCGT/PCIeT_L0M72M	
15	DOTC_96MHzL	M72M
41	PEREQ1# / PCIeT_L7	MiniCard
40	PEREQ2# / PCIeC_L7	MiniCard
32	PEREQ3#	NewCard
33	PEREQ4#	MiniCard
30	PCIeT_L4	NewCard
31	PCIeC_L4	NewCard
49	CPUT_L1F	MCH
48	CPUC_L1F	MCH
52	CPUT_L0	CPU
51	CPUC_L0	CPU
57	X2	14.318MHz
58	X1	14.318MHz
60	REF0	ICH8
61	REF1/FSLC/TEST_SEL	X

		<b>Title : GPIO setting</b>	
ASUSTek Computer INC. NBI		Engineer: Jerry Mou	
Size	Project Name		Rev
Custom	F7Sr		1.1
Date: 星期五, 五月 10, 2007		Sheet	2 of 95

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Kennedy Zhu



**+VCORE Mid-Frequency Capacitor**  
 Intel: 22UF \*32  
 F3S: 10UF \*16

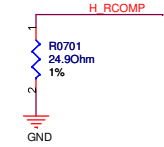
**+VCCP Decoupling Capacitor**  
 Intel: 270UF \*1, 0.1UF \*6  
 F3S: 100UF \*1, 0.1UF \*4

*Kennedy Zhang*

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**RCOMP**

For Calibrating the FSB I/O Buffer



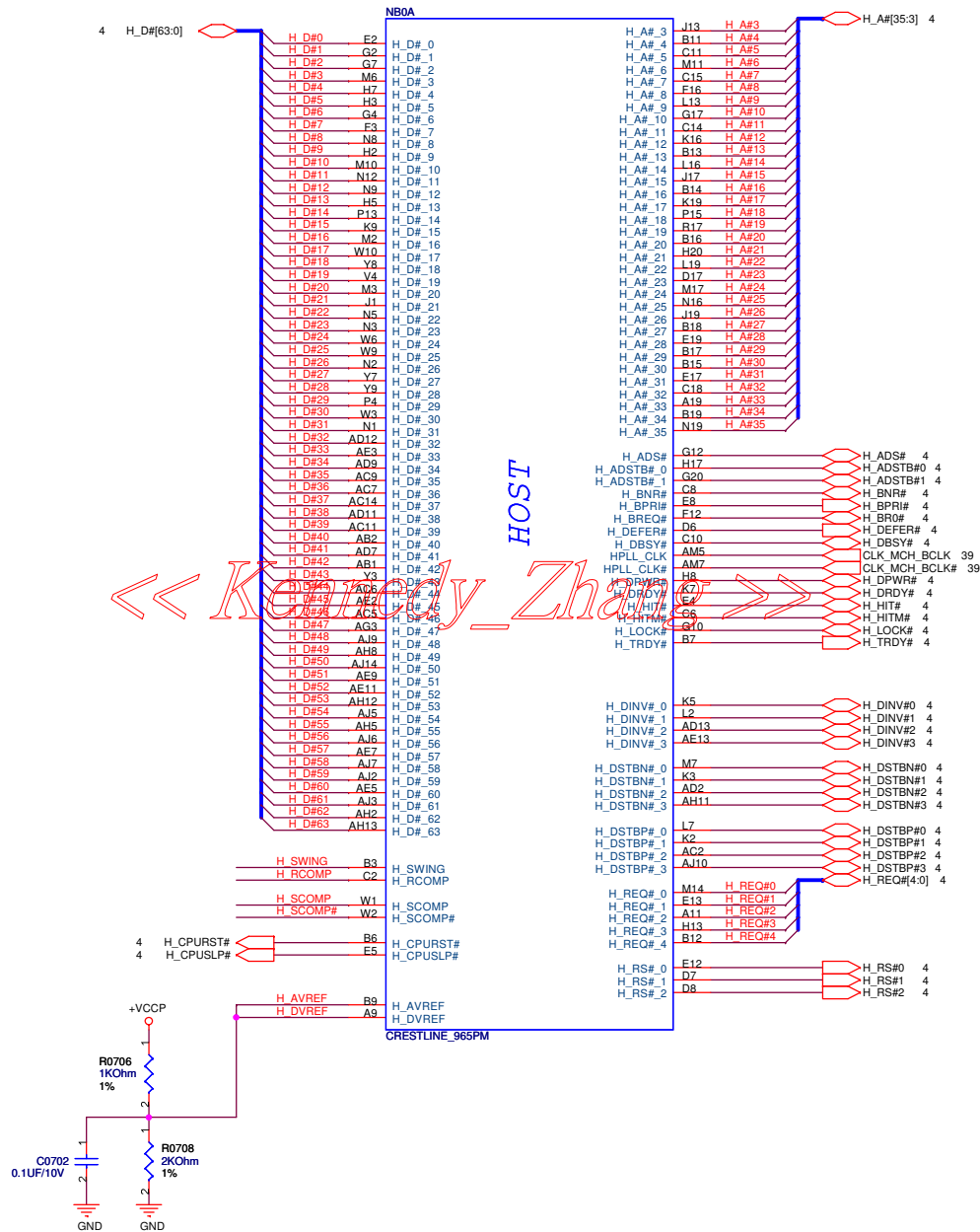
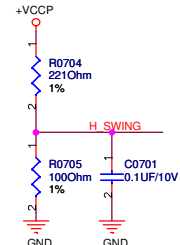
**SCOMP**

For Slew Rate Compensation on the FSB

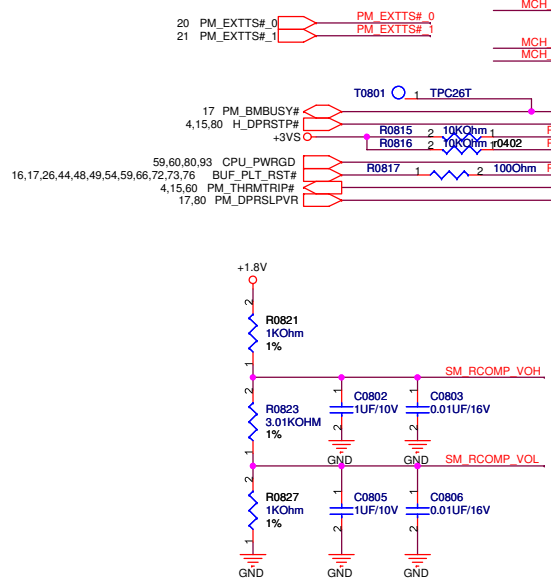
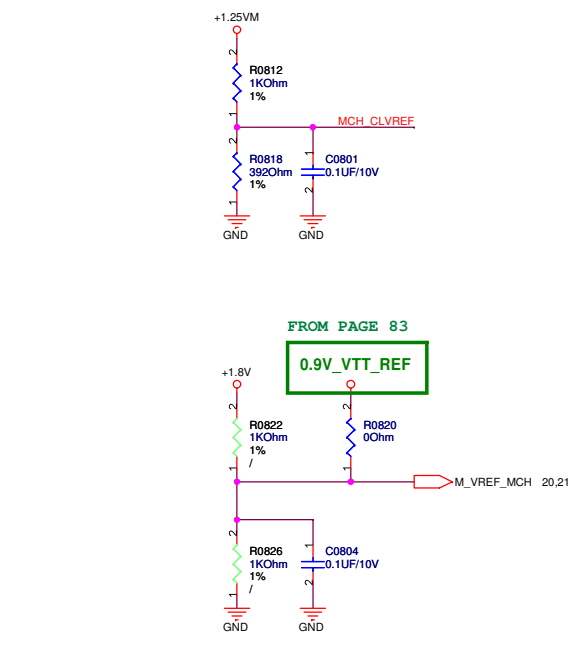
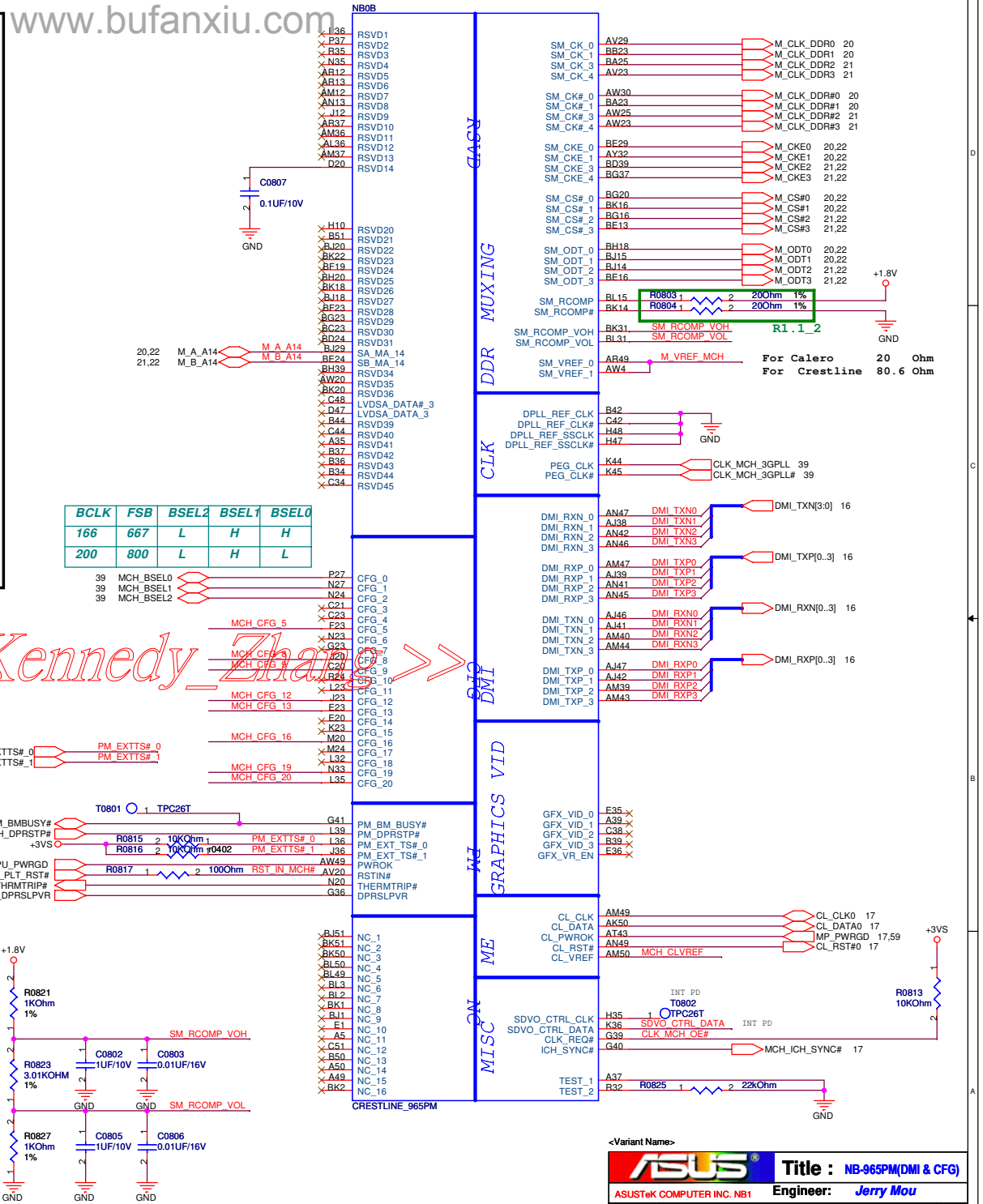
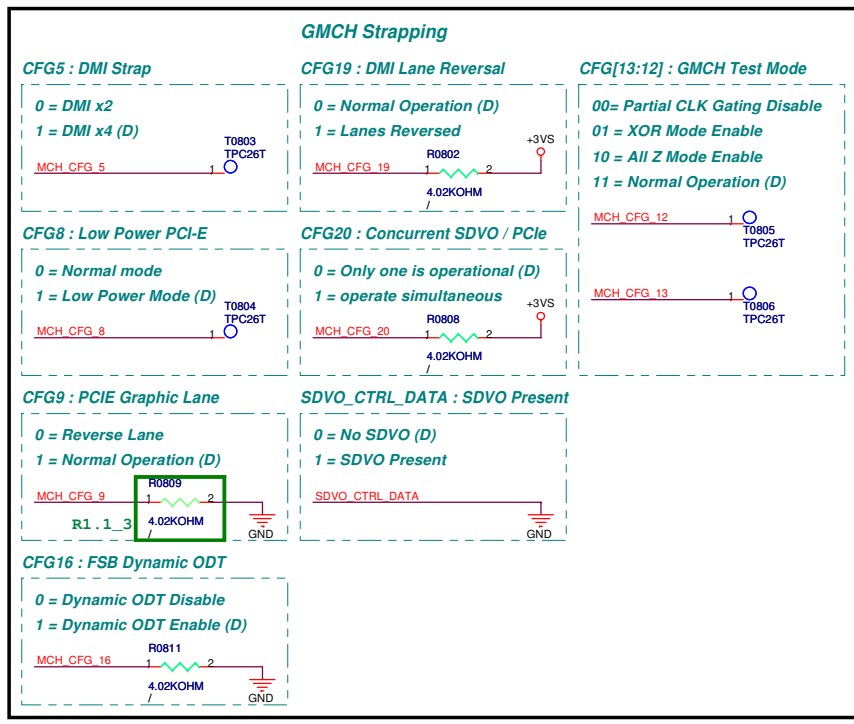


**Voltage Swing**

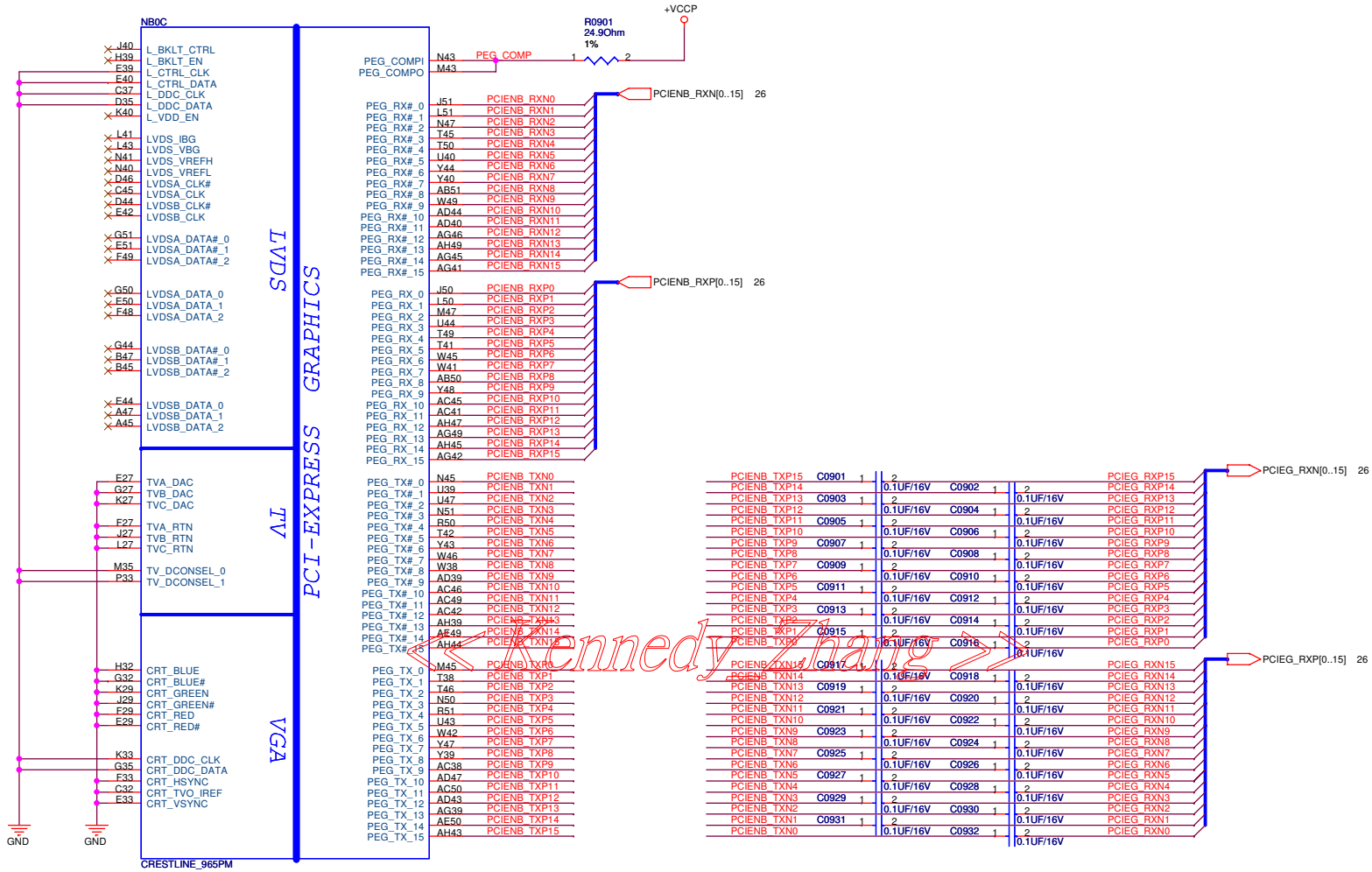
For Providing a Reference Voltage to The FSB RCOMP circuits

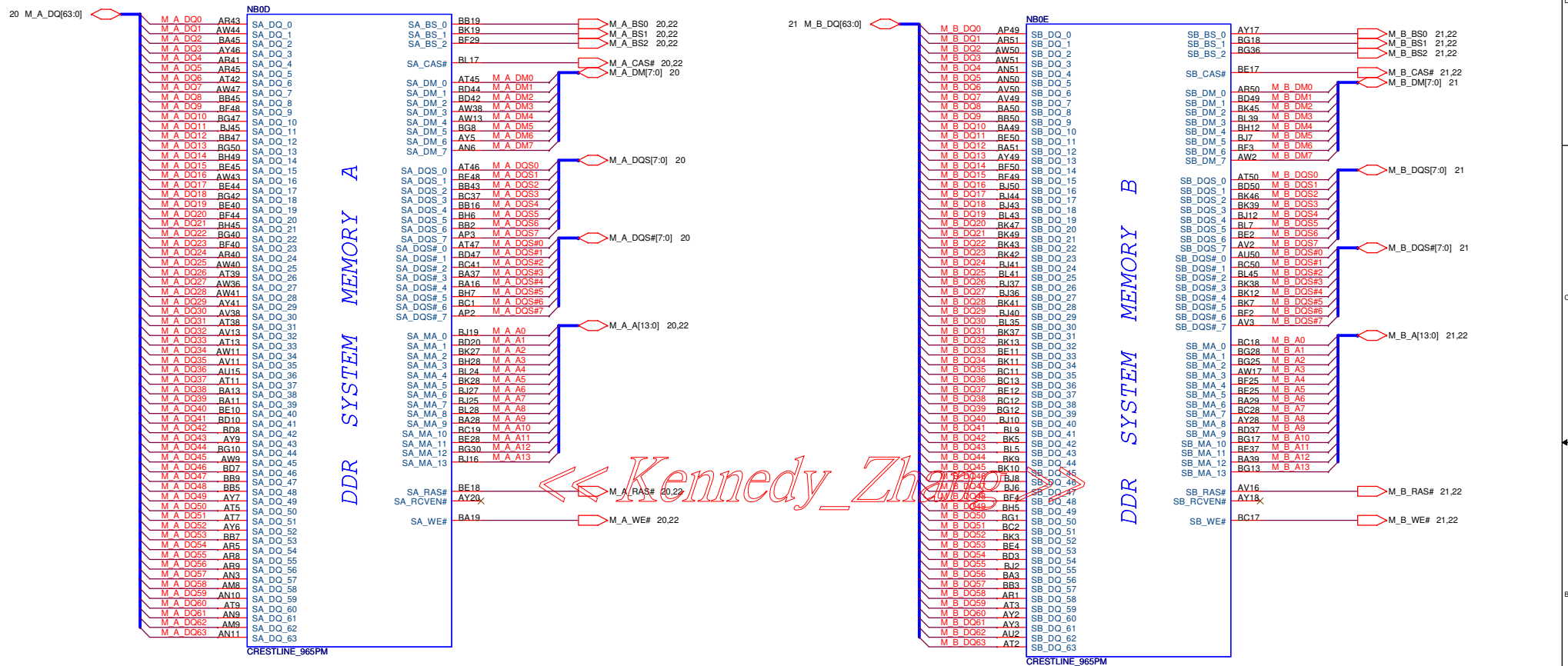


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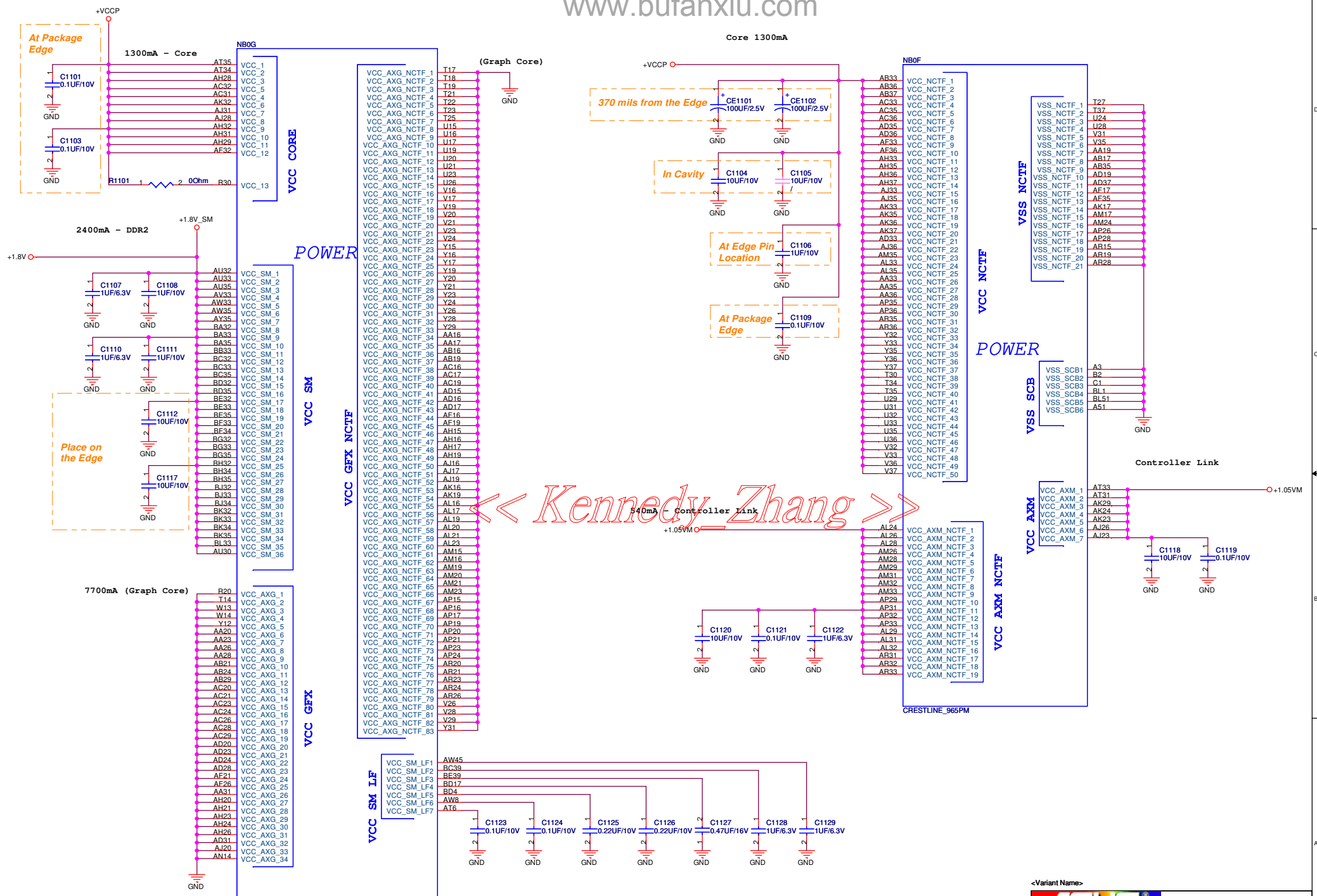








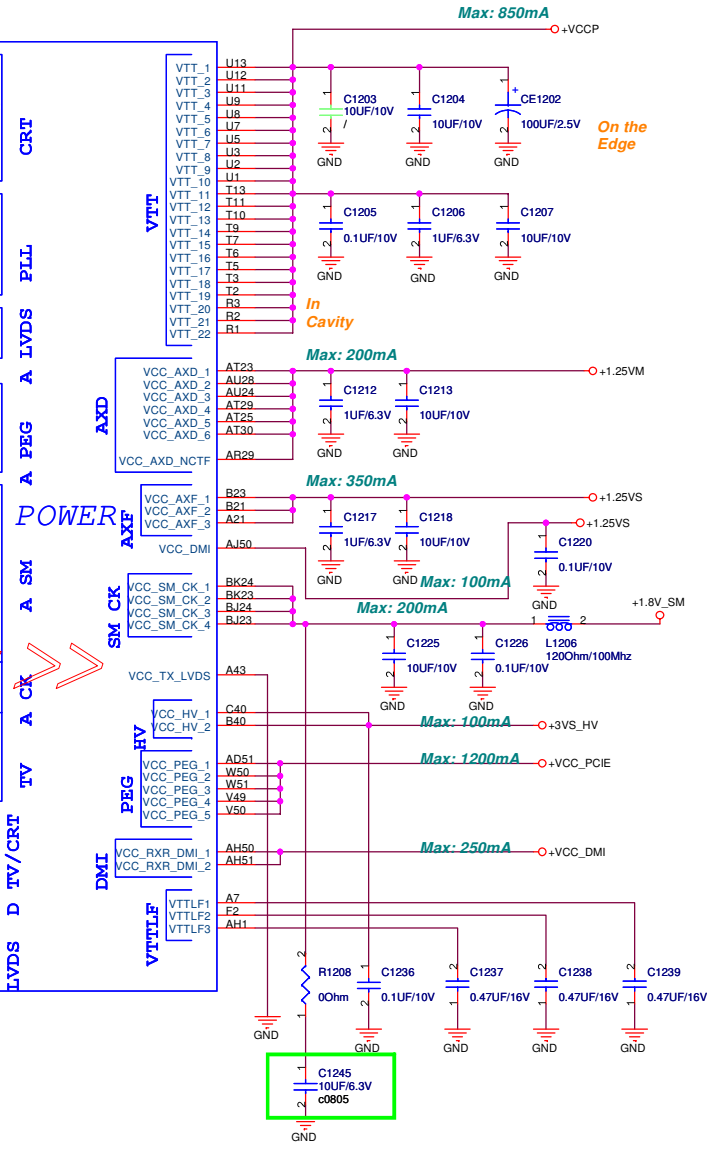
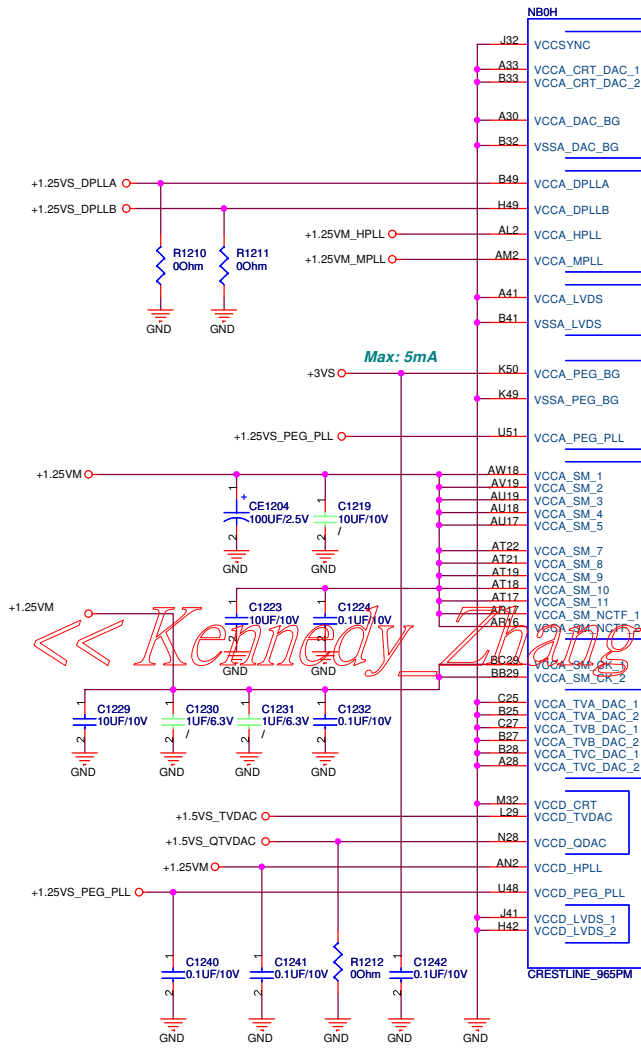
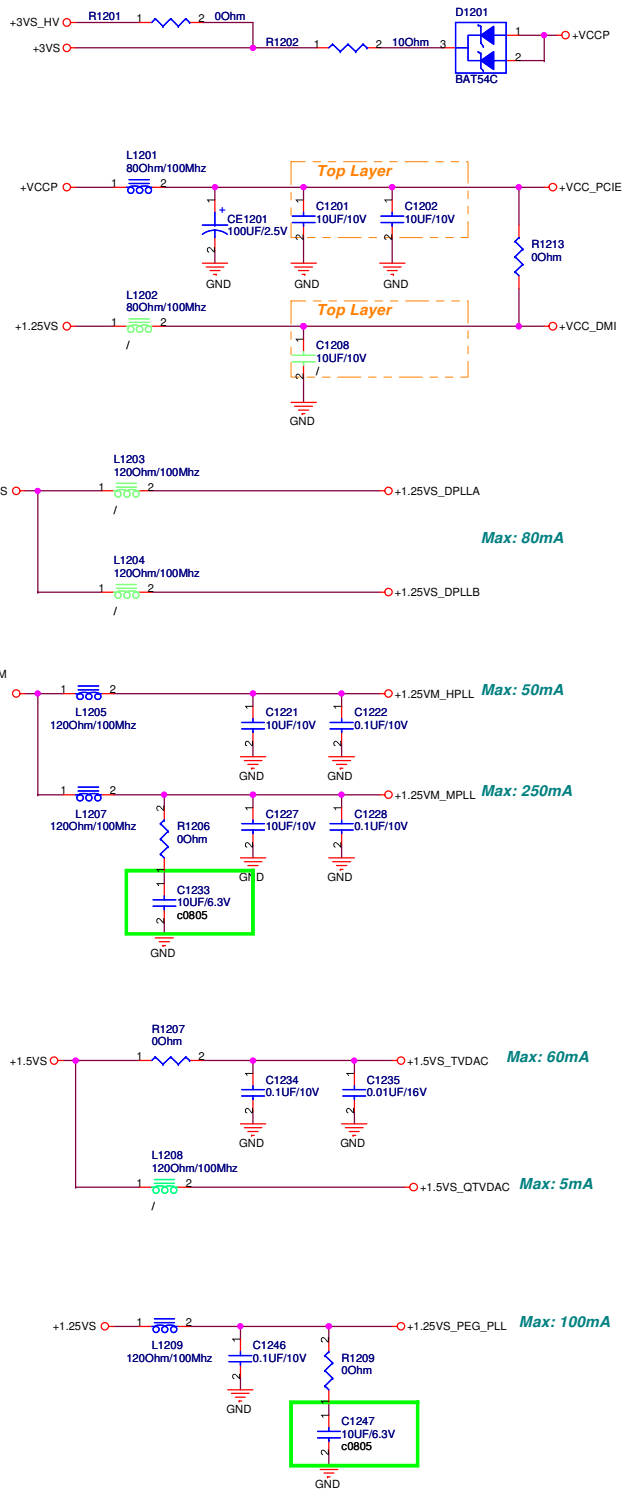
Kennedy\_Zh



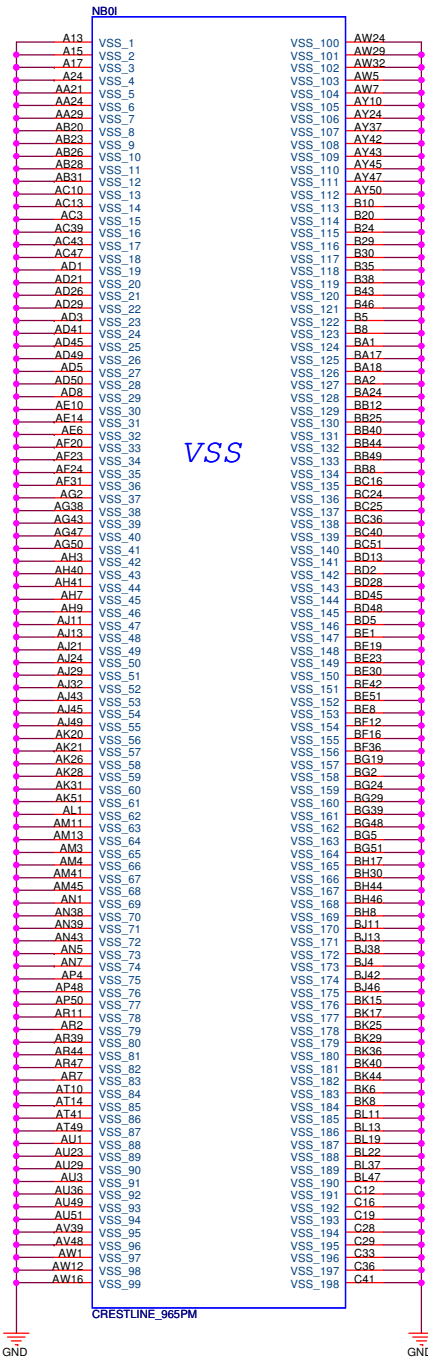
« Kennedy Zhang »

<Variant Names>

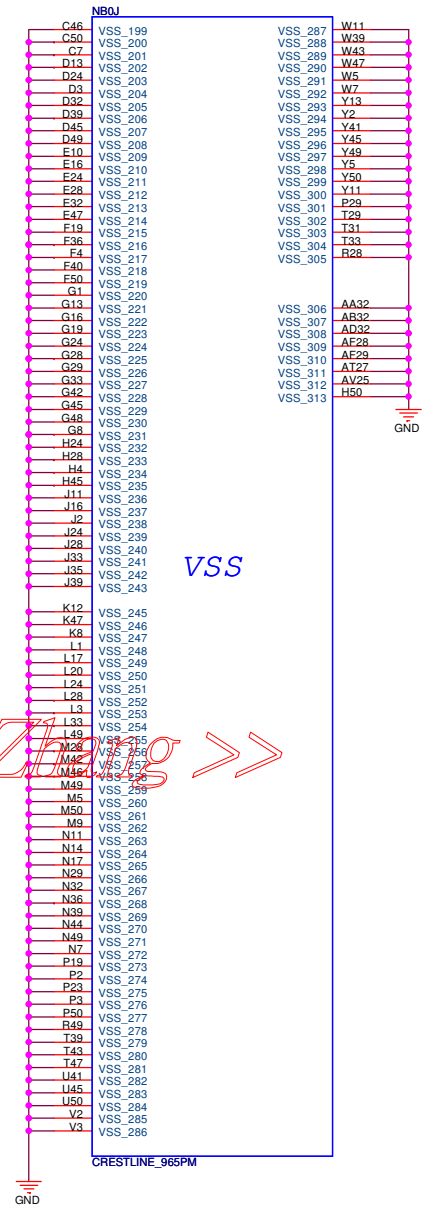
<b>ASUS</b>		<b>Title : CRESTLINE(PWR)</b>
ASUSTek COMPUTER INC. N81		Engineer: Jerry Mou
Size Custom	Project Name <b>F7Sr</b>	Rev 1.1
Date: 2007.05.10	Sheet 11	of 95



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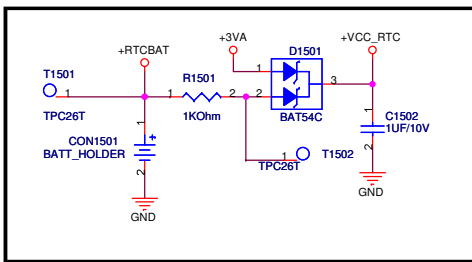


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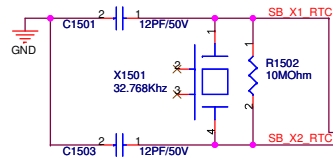


**ASUS** Title : CRESTLINE(GND)  
 ASUSTeK COMPUTER INC. NB1 Engineer: Jerry Mou  
 Size Project Name  
 Custom F7Sr  
 Date: 星期五, 五月 10, 2007 Sheet 13 of 95  
 Rev 1.1

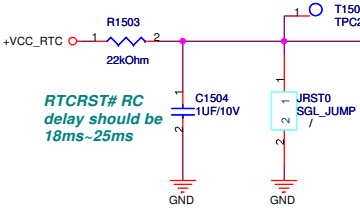
<< Kennedy\_Zhang >>



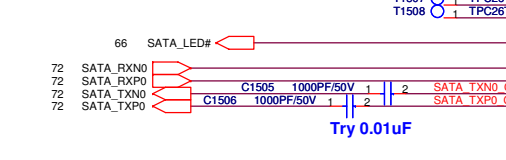
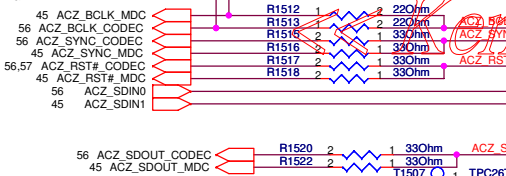
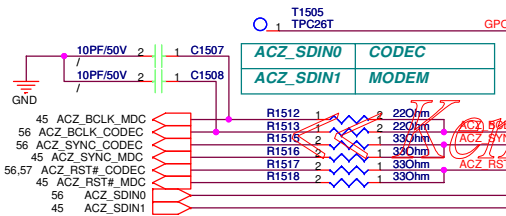
Request of CSC for CMOS clear function  
Place Near the Open Door



RTCST# RC delay should be 18ms~25ms

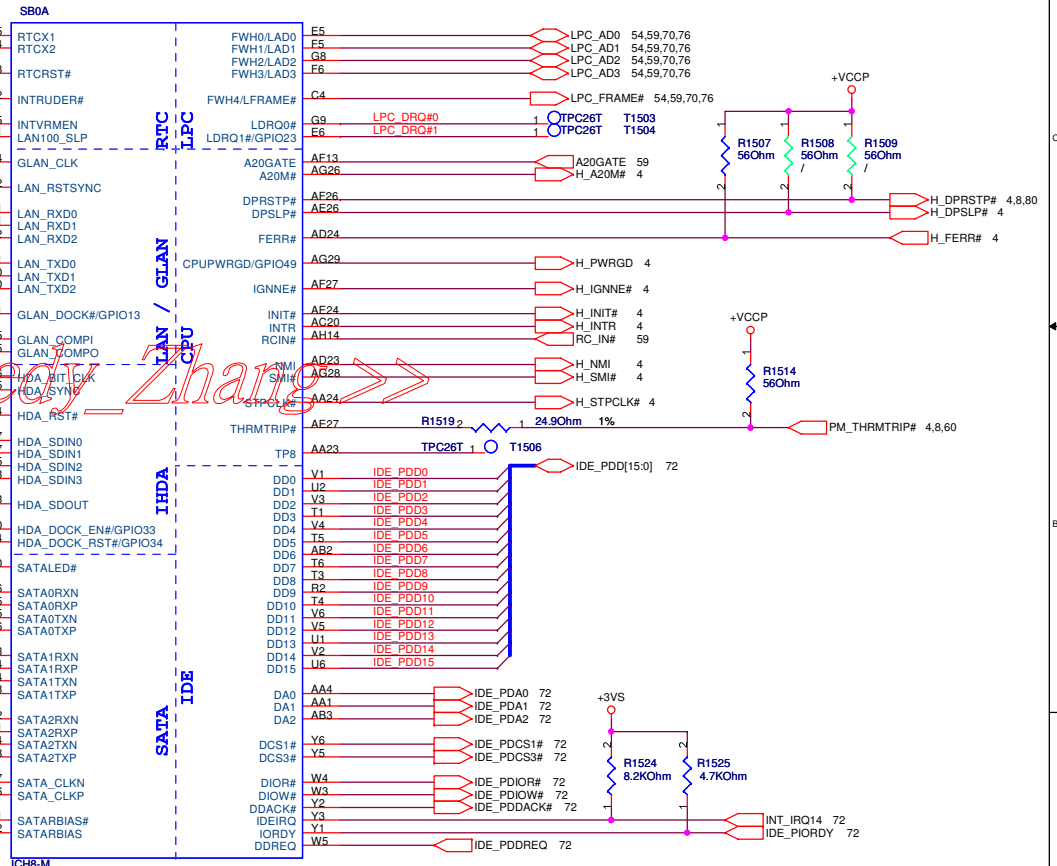
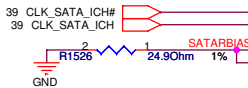


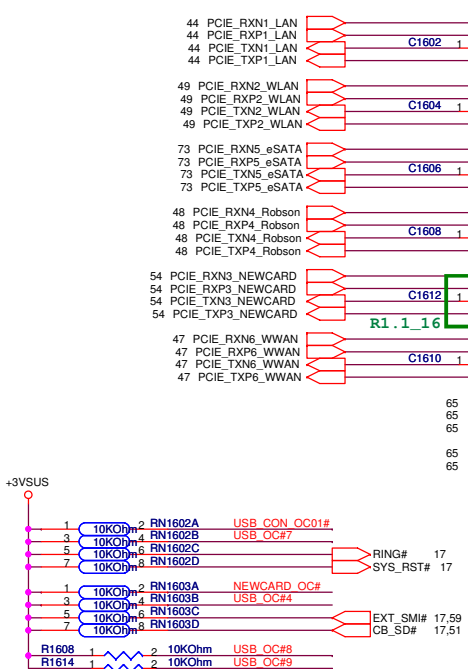
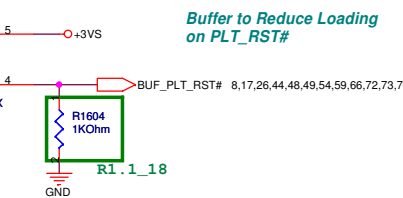
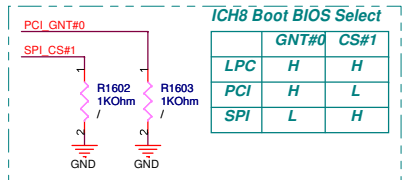
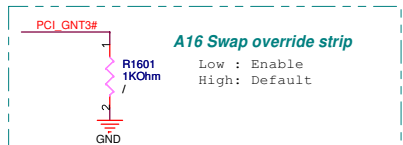
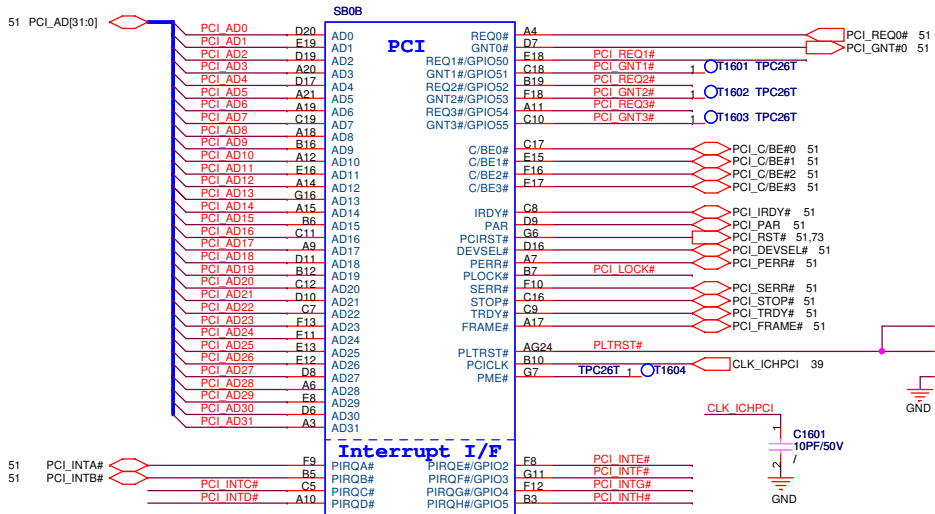
ICH\_INTVRMEN (VCCSUS1\_05,VCCSUS1\_5,VCCCL1\_5)  
Low - Disabled Internal VR  
High - Enable Internal VR (D)  
ICH\_LAN100 (VCCLAN1\_05,VCCCL1\_05)  
Low - Disabled Internal VR  
High - Enable Internal VR (D)



XOR Chain Entrance Strap

ICH_TP3	ACZ_SDO0	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (D)
1	1	Set PCIe port config bit 1





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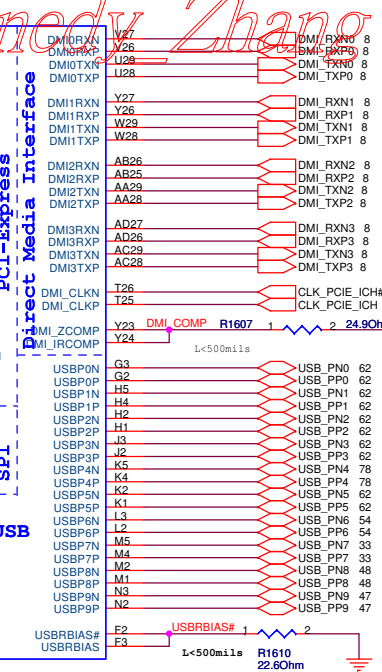
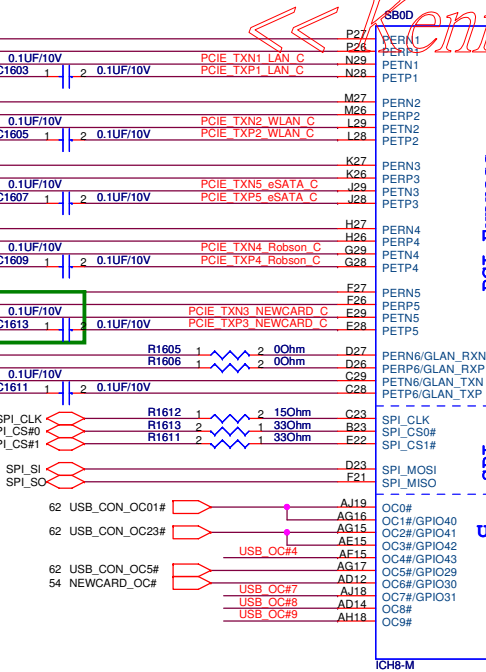
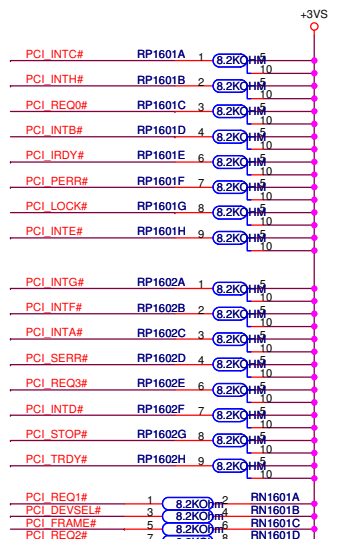
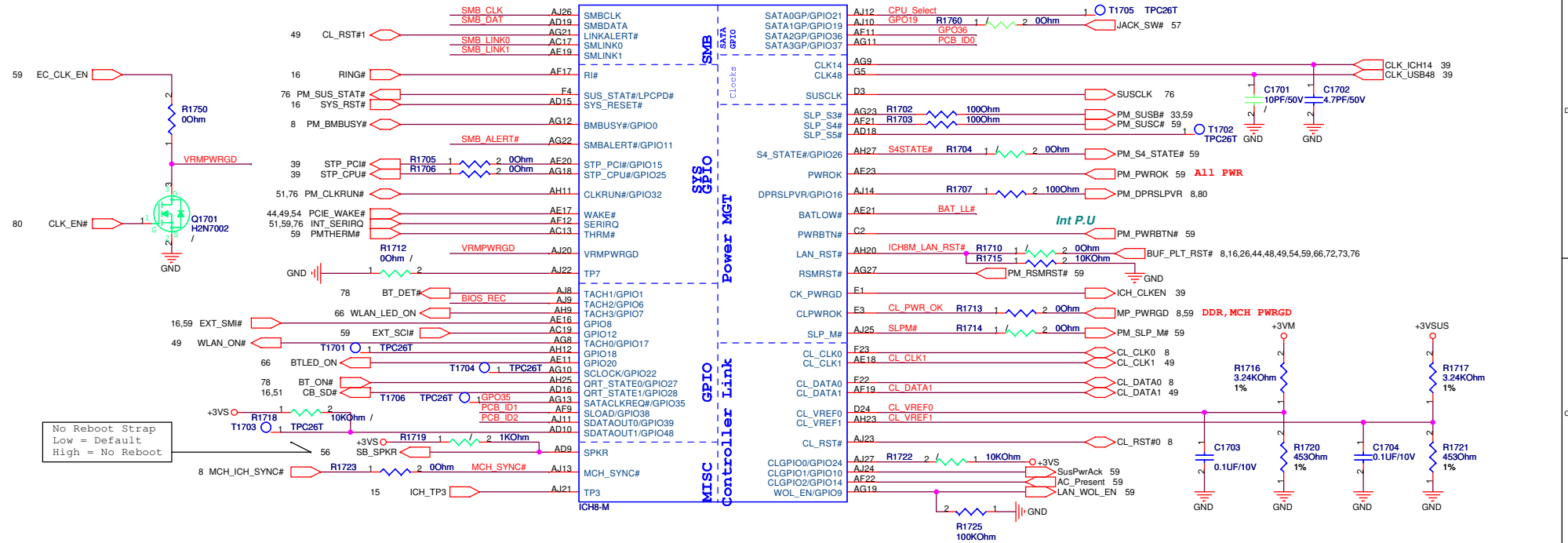


Table mapping USB ports to their functions: USB 0 (USB Conn.), USB 1 (USB Conn.), USB 2 (USB Conn.), USB 3 (USB Conn.), USB 4 (Bluetooth), USB 5 (USB Conn.), USB 6 (Newcard), USB 7 (CMOS Camera), USB 8 (Windigo), USB 9 (TV).

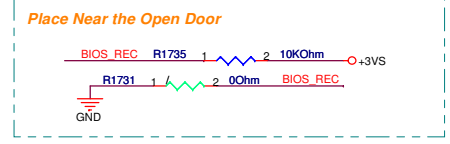


ASUS logo and project information: Title: SB-ICH8M(2), ASUSTek COMPUTER INC. NBI, Engineer: Jerry Mou, Project Name: F7Sr, Rev: 1.1, Date: 星期四, 五月 10, 2007, Sheet: 16 of 95.

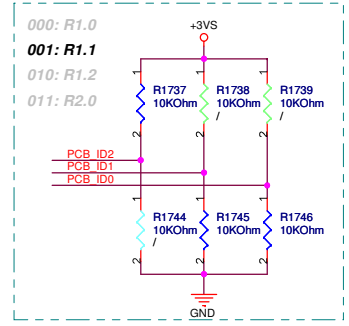




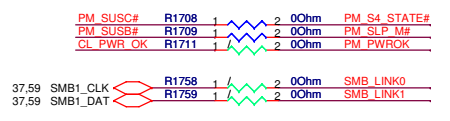
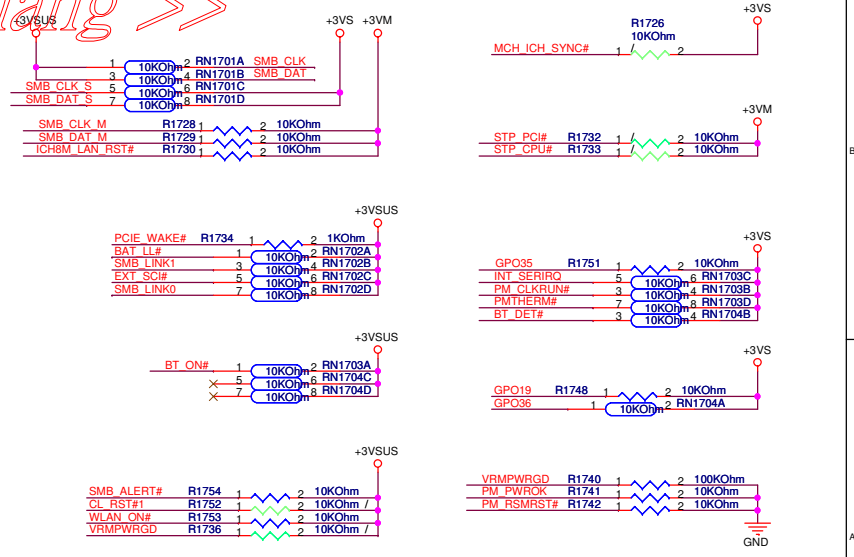
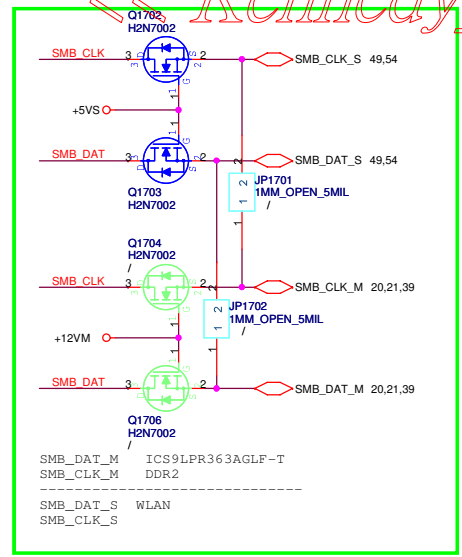
Mount for BIOS Recovery



PCB\_ID[0:2]

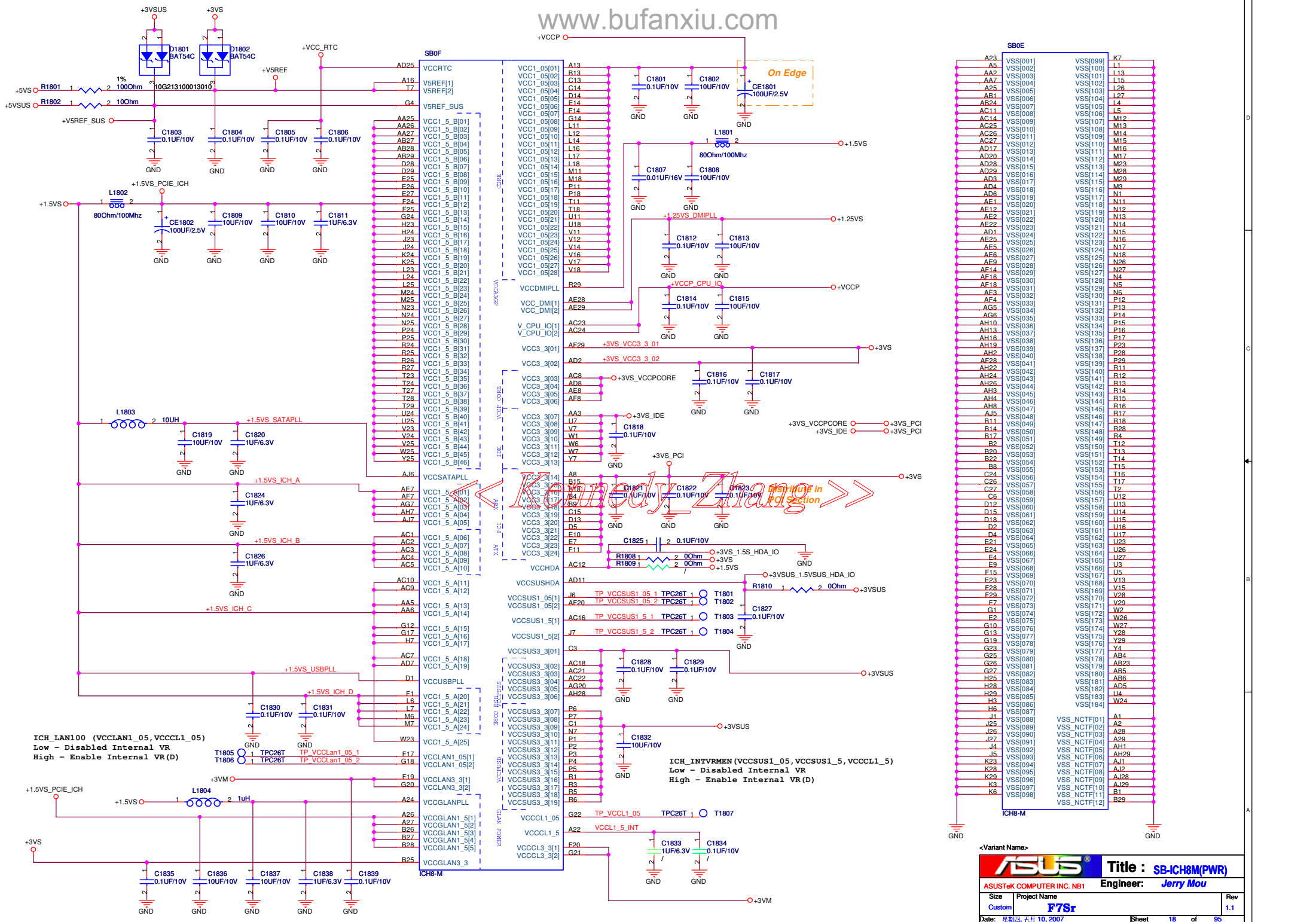


<< Kennedy\_Zhang >>



<Variant Name>

Title : SB-ICH8M(3)  
 ASUSTek COMPUTER, INC. N81 Engineer: Jerry Mou  
 Size Project Name  
 Custom F7Sr  
 Date: 2007.05.10 Rev 1.1  
 Sheet 17 of 95



ICH\_LAN100 (VCCLAN1\_05, VCCCL1\_05)  
Low - Disabled Internal VR  
High - Enable Internal VR (D)

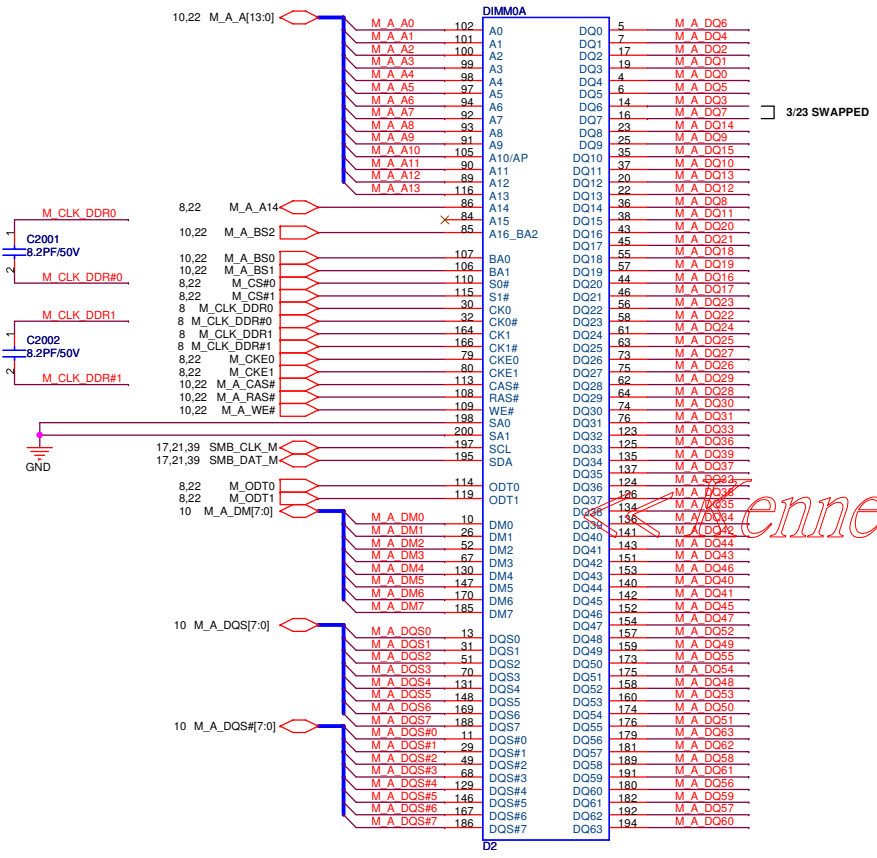
ICH\_INTVRMEN (VCCSUS1\_05, VCCSUS1\_5, VCCCL1\_5)  
Low - Disabled Internal VR  
High - Enable Internal VR (D)

SB0E	VSS	VSS	K7
A23	VSS[001]	VSS[099]	L1
A5	VSS[002]	VSS[100]	L13
AA2	VSS[003]	VSS[101]	L15
AA7	VSS[004]	VSS[102]	L17
A25	VSS[005]	VSS[103]	L26
AB1	VSS[006]	VSS[104]	L4
AB24	VSS[007]	VSS[105]	L4
AC11	VSS[008]	VSS[106]	L5
AC14	VSS[009]	VSS[107]	M12
AC25	VSS[010]	VSS[108]	M13
AC26	VSS[011]	VSS[109]	M14
AC27	VSS[012]	VSS[110]	M15
AD17	VSS[013]	VSS[111]	M16
AD20	VSS[014]	VSS[112]	M17
AD28	VSS[015]	VSS[113]	M23
AD29	VSS[016]	VSS[114]	M28
AD3	VSS[017]	VSS[115]	M29
AD4	VSS[018]	VSS[116]	M3
AD6	VSS[019]	VSS[117]	M11
AE12	VSS[020]	VSS[118]	M12
AE2	VSS[021]	VSS[119]	M13
AE22	VSS[022]	VSS[120]	M17
AD1	VSS[023]	VSS[121]	N14
AD1	VSS[024]	VSS[122]	N15
AE25	VSS[025]	VSS[123]	N16
AE5	VSS[026]	VSS[124]	N17
AE6	VSS[027]	VSS[125]	N18
AE9	VSS[028]	VSS[126]	N26
AE14	VSS[029]	VSS[127]	N27
AE15	VSS[030]	VSS[128]	N5
AF3	VSS[031]	VSS[129]	N6
AF4	VSS[033]	VSS[131]	P12
AG5	VSS[034]	VSS[132]	P13
AG6	VSS[035]	VSS[133]	P15
AH10	VSS[036]	VSS[134]	P16
AH13	VSS[037]	VSS[135]	P17
AH16	VSS[038]	VSS[136]	P23
AH19	VSS[039]	VSS[137]	P28
AH2	VSS[040]	VSS[138]	P29
AF28	VSS[041]	VSS[139]	R11
AH22	VSS[042]	VSS[140]	R12
AH24	VSS[043]	VSS[141]	R12
AH26	VSS[044]	VSS[142]	R13
AH3	VSS[045]	VSS[143]	R14
AH4	VSS[046]	VSS[144]	R15
AH8	VSS[047]	VSS[145]	R16
AJ5	VSS[048]	VSS[146]	R17
B11	VSS[049]	VSS[147]	R18
B12	VSS[050]	VSS[148]	R18
B1	VSS[051]	VSS[149]	R4
B2	VSS[052]	VSS[150]	T12
B20	VSS[053]	VSS[151]	T13
B22	VSS[054]	VSS[152]	T14
B8	VSS[055]	VSS[153]	T15
C24	VSS[056]	VSS[154]	T16
C26	VSS[057]	VSS[155]	T17
C27	VSS[058]	VSS[156]	T2
D12	VSS[059]	VSS[157]	U12
D15	VSS[060]	VSS[158]	U12
D18	VSS[061]	VSS[159]	U14
D19	VSS[062]	VSS[160]	U15
D4	VSS[063]	VSS[161]	U16
D2	VSS[064]	VSS[162]	U17
E21	VSS[065]	VSS[163]	U23
E4	VSS[066]	VSS[164]	U26
E23	VSS[067]	VSS[165]	U27
E9	VSS[068]	VSS[166]	U3
E23	VSS[069]	VSS[167]	U5
F28	VSS[070]	VSS[168]	U15
F29	VSS[071]	VSS[169]	U28
G1	VSS[072]	VSS[170]	V29
F7	VSS[073]	VSS[171]	W2
E2	VSS[074]	VSS[172]	W26
G10	VSS[075]	VSS[173]	W27
G13	VSS[076]	VSS[174]	Y28
G19	VSS[077]	VSS[175]	Y29
G23	VSS[078]	VSS[176]	Y4
G25	VSS[079]	VSS[177]	Y4
G26	VSS[080]	VSS[178]	AB23
G27	VSS[081]	VSS[179]	AB5
H25	VSS[082]	VSS[180]	AB6
H28	VSS[083]	VSS[181]	AB5
H29	VSS[084]	VSS[182]	AB6
H3	VSS[085]	VSS[183]	UA4
H6	VSS[086]	VSS[184]	W24
J1	VSS[087]	VSS[087]	
J25	VSS[088]	VSS_NCTF[01]	A1
J26	VSS[089]	VSS_NCTF[02]	A2
J27	VSS[090]	VSS_NCTF[03]	A29
J4	VSS[091]	VSS_NCTF[04]	AH1
J5	VSS[092]	VSS_NCTF[05]	AH1
K23	VSS[093]	VSS_NCTF[06]	AH29
K28	VSS[094]	VSS_NCTF[07]	AJ1
K29	VSS[095]	VSS_NCTF[08]	AJ28
K3	VSS[096]	VSS_NCTF[09]	AJ29
K6	VSS[098]	VSS_NCTF[11]	B1
	VSS[098]	VSS_NCTF[12]	B29

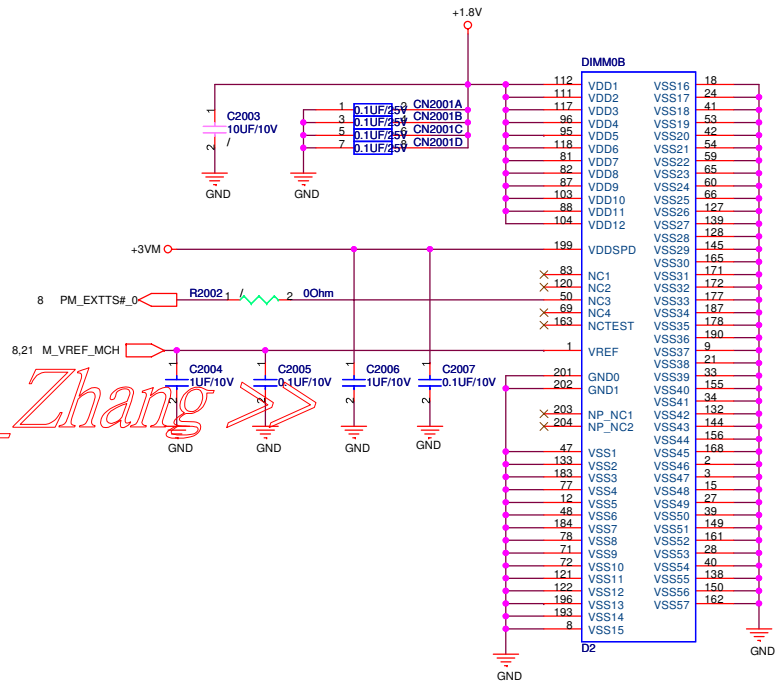
ASUS® Title: SB-ICH8M(PWR)  
 ASUSTeK COMPUTER INC. NBI Engineer: Jerry Mou  
 Size Project Name  
 Custom F7Sr  
 Date: 2007.10.10 Sheet 18 of 95

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**REV Type - 12G025122006**  
**ME - 12G025332003**

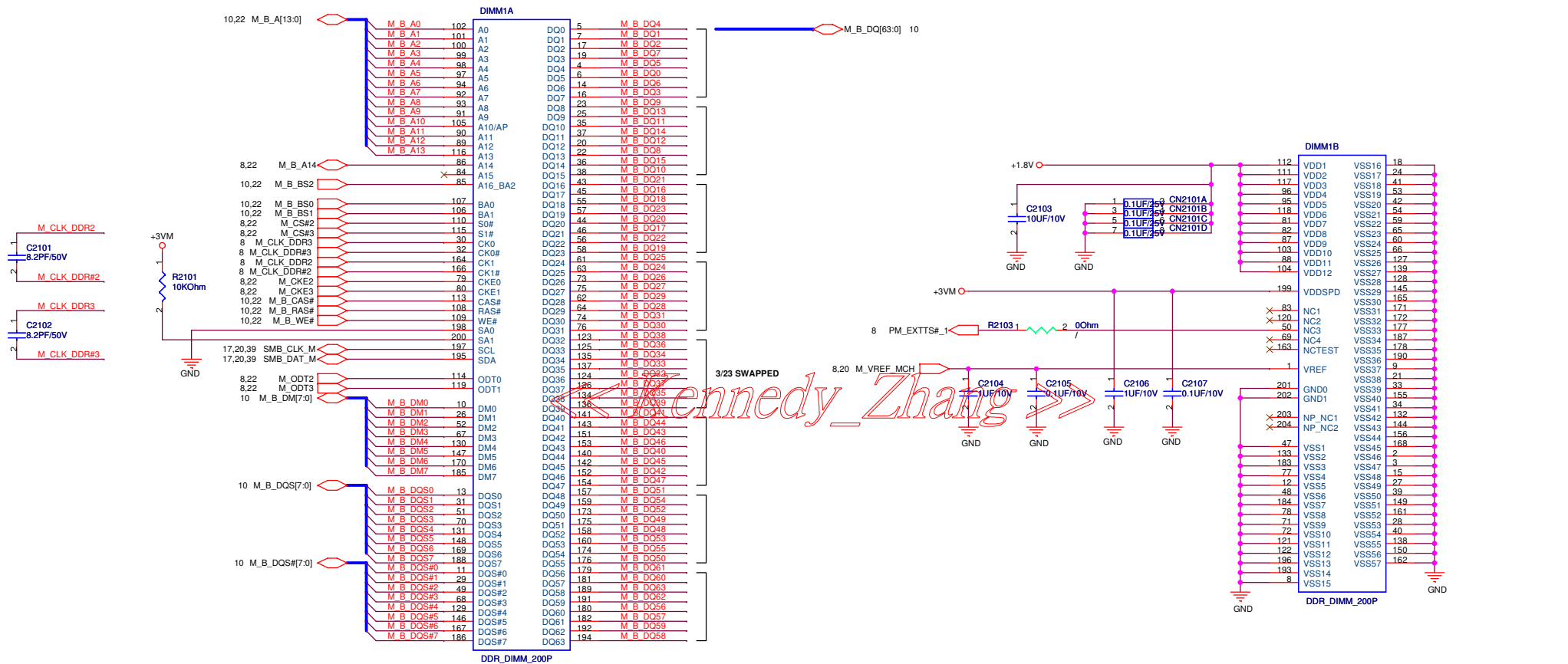


3/23 SWAPPED

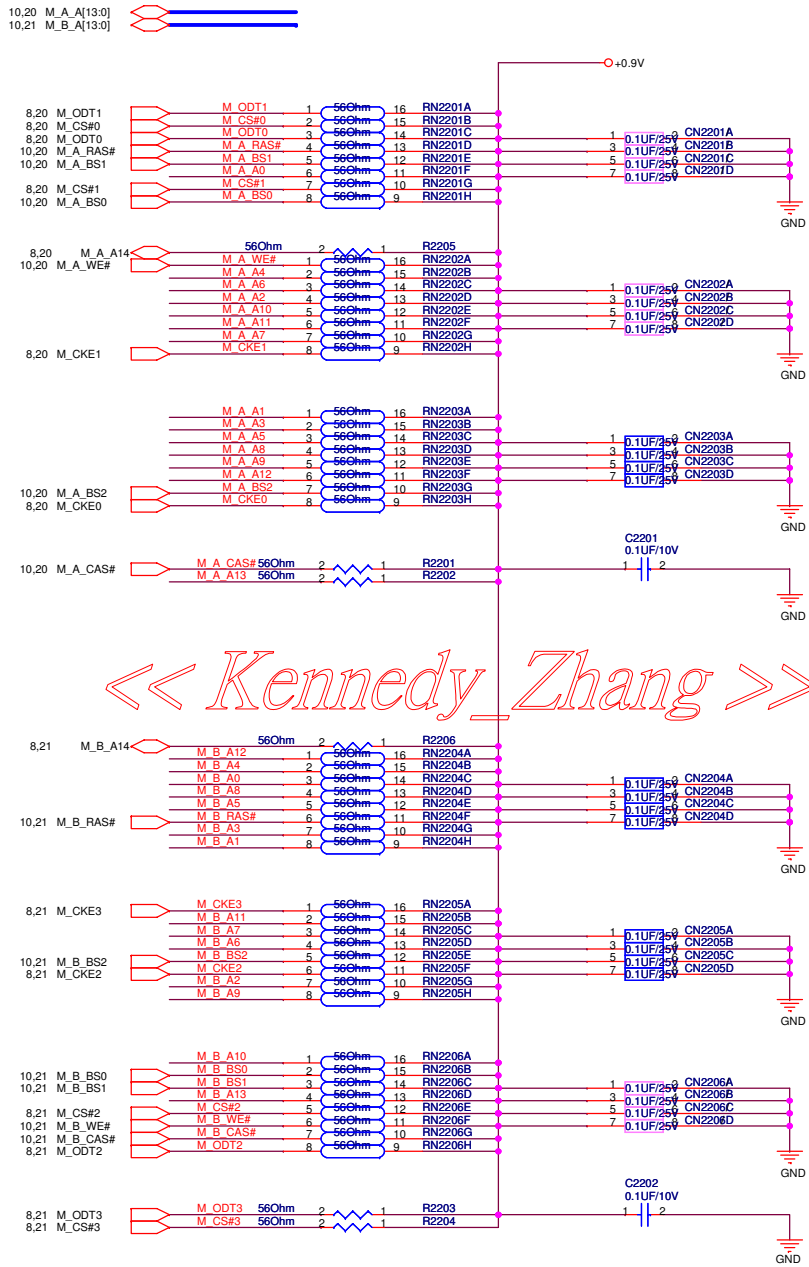


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### STD Type - 12G025122000



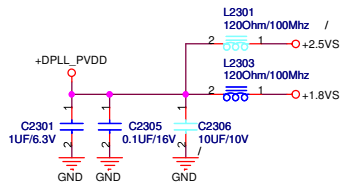
Kennedy\_Zhang



<Variant Name>

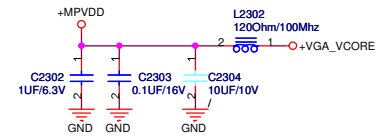
<b>ASUS</b>		<b>Title : DDR2 TERMINATION</b>
ASUSTeK COMPUTER INC. NBI		Engineer: Jerry Mou
Size	Project Name	Rev
Custom	F7Sr	1.1
Date: 2007.05.10	Sheet 22	of 95

### M66/M76M Power

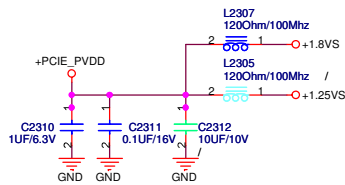


(2.5V @ 170MA DPLL\_PVDD) INSTALL DPLL\_PVDD TO +2.5V FOR M66M

(1.8V @ 40MA DPLL\_PVDD) INSTALL DPLL\_PVDD TO +1.8V FOR M76M

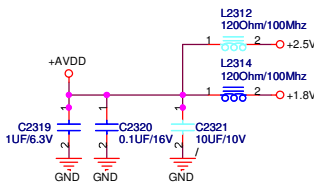


(0.95V-1.1V @ 345MA MPVDD)



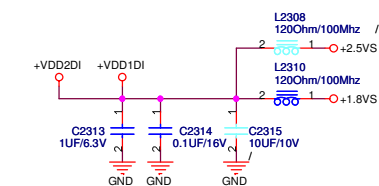
(1.8V @ 40ma PCIE\_PVDD) INSTALL PCIE\_PVDD TO +1.8V FOR M76M

(1.2V @ 90ma PCIE\_PVDD) INSTALL PCIE\_PVDD TO +1.2V FOR M66M



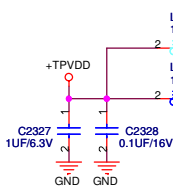
(2.5V @ 100MA AVDD) INSTALL AVDD TO +2.5V FOR M66M

(1.8V @ 100MA AVDD) INSTALL AVDD TO +1.8V FOR M76M



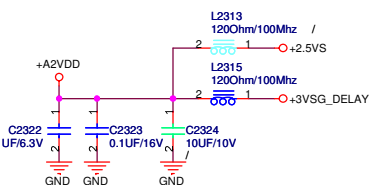
(2.5V @ 110 MA VDD1DI) INSTALL VDD1DI, VDD2DI TO +2.5V FOR M66M

(1.8V @ 100MA VDD1DI) INSTALL VDD1DI, VDD2DI TO +1.8V FOR M76M



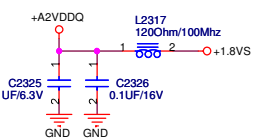
(2.5V @ 60MA TPVDD) INSTALL TPVDD TO +2.5V FOR M66M

(1.8V @ 20MA TPVDD) INSTALL TPVDD TO +1.8V FOR M76M



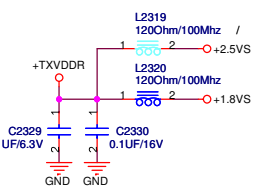
(2.5V @ 120MA A2VDD) INSTALL A2VDD TO +2.5V FOR M66M

(3.3V @ 135MA A2VDD) INSTALL A2VDD TO +3.3V FOR M76M



(1.8V @ 2MA A2VDDQ) INSTALL A2VDDQ TO +1.8V FOR M76M

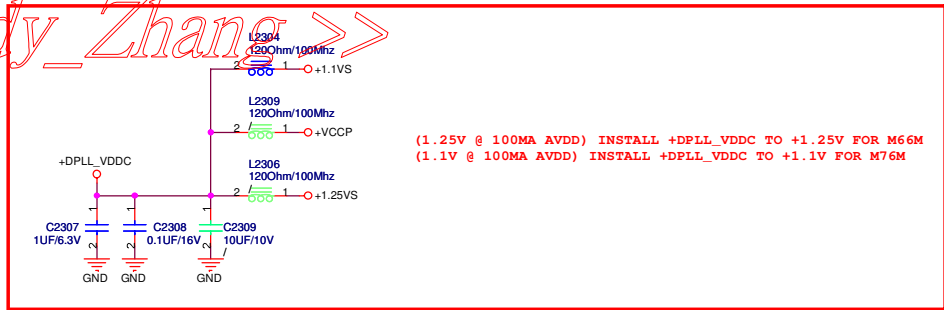
DO NOT INSTALL A2VDDQ FOR M66M



(2.5V @ 155MA TXVDDR) INSTALL TXVDDR TO +2.5V FOR M66M

(1.8V @ 200ma TXVDDR) INSTALL TXVDDR TO +1.8V FOR M76M

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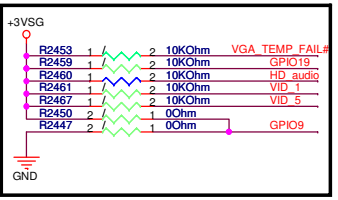
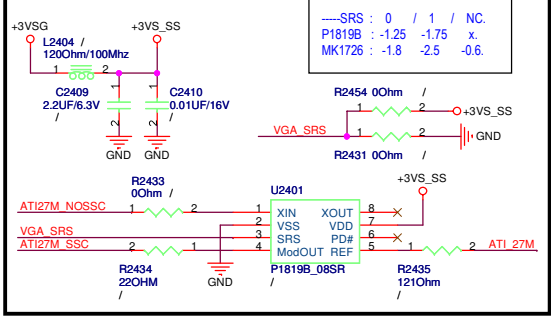


(1.25V @ 100MA AVDD) INSTALL +DPLL\_VDDC TO +1.25V FOR M66M  
(1.1V @ 100MA AVDD) INSTALL +DPLL\_VDDC TO +1.1V FOR M76M

<Variant Name>

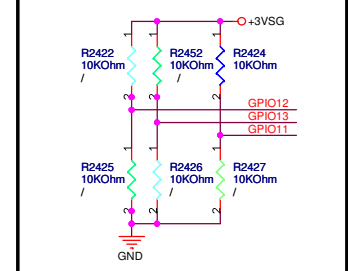
<b>ASUS</b>		<b>Title : VGA M72M POWER</b>	
ASUS TeK COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 星期五, 五月 10, 2007	Sheet	23	of 95

### Spread Spectrum

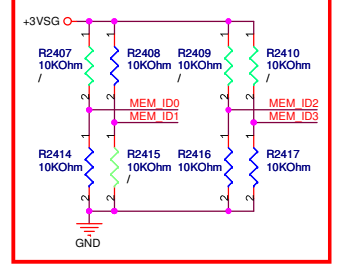


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### ROM Strap



### Memory ID

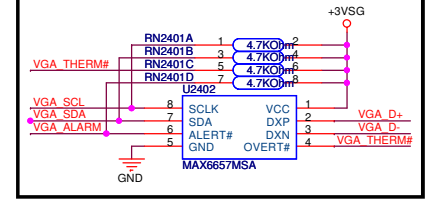


**Infineon (DDR2 16M\*16 for A Channel 1.8V 128M)**  
 MEM\_ID[0:3] = 0100  
**Hynix (DDR2 16M\*16 for A Channel 1.8V 128M)**  
 MEM\_ID[0:3] = 1100

Primary Memory Aperture size requested at PCI Configuration

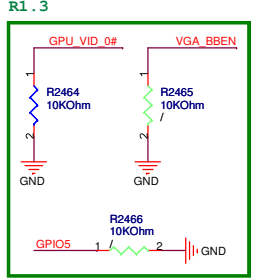
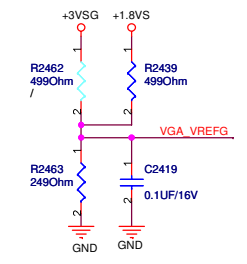
	GPIO_13	GPIO_12	GPIO_11
1GB	1	0	1
512MB	1	0	0
256MB	0	0	1
128MB	0	0	0
64MB	0	1	0
32MB	0	1	1

### Thermal

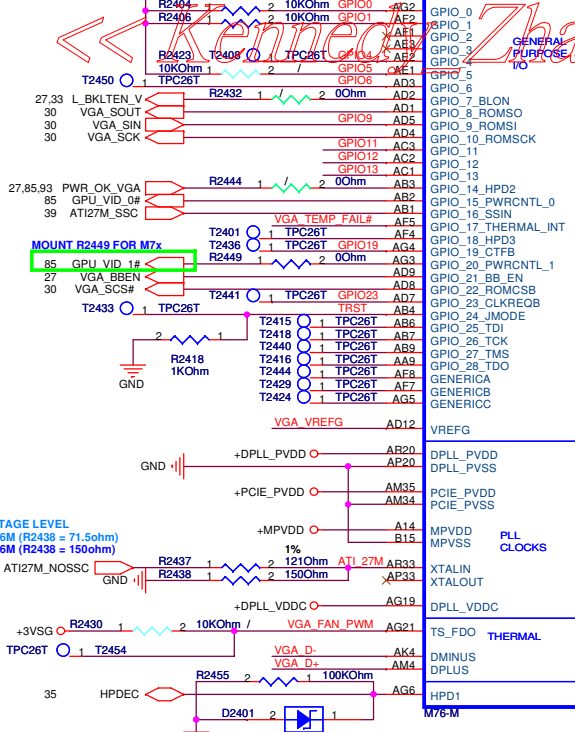
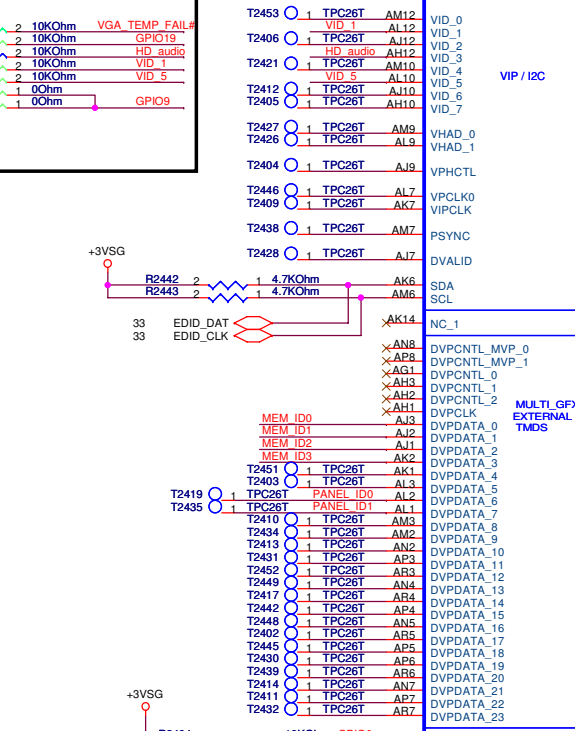


**FOR M76M**  
 VREFG VOLTAGE DIVIDER IS  $VREFG = VDDR4,5 = 1.8V / 3 = 0.6V$   
 $R2463=249\Omega$

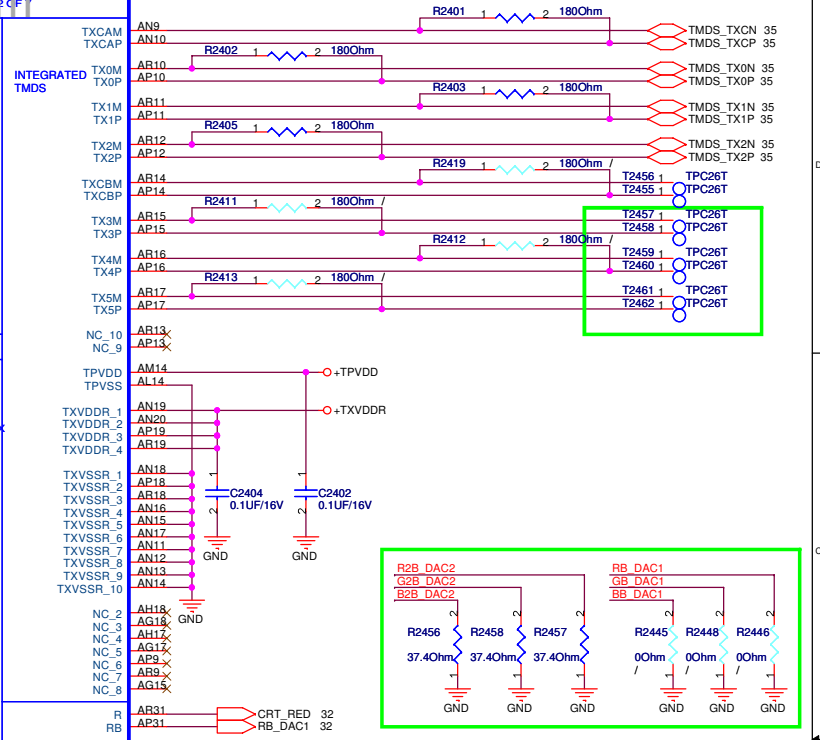
**FOR M66M**  
 VREFG VOLTAGE DIVIDER IS  $VREFG = 3.3V / 2 = 1.65V$   
 $R2463=499\Omega$



**XTALIN VOLTAGE LEVEL**  
 1.2V FOR M66M (R2438 = 71.5ohm)  
 1.8V FOR M76M (R2438 = 150ohm)



### INSTALL TERMINATION RESISTORS CLOSE TO ASIC



M72 - Close to GPU

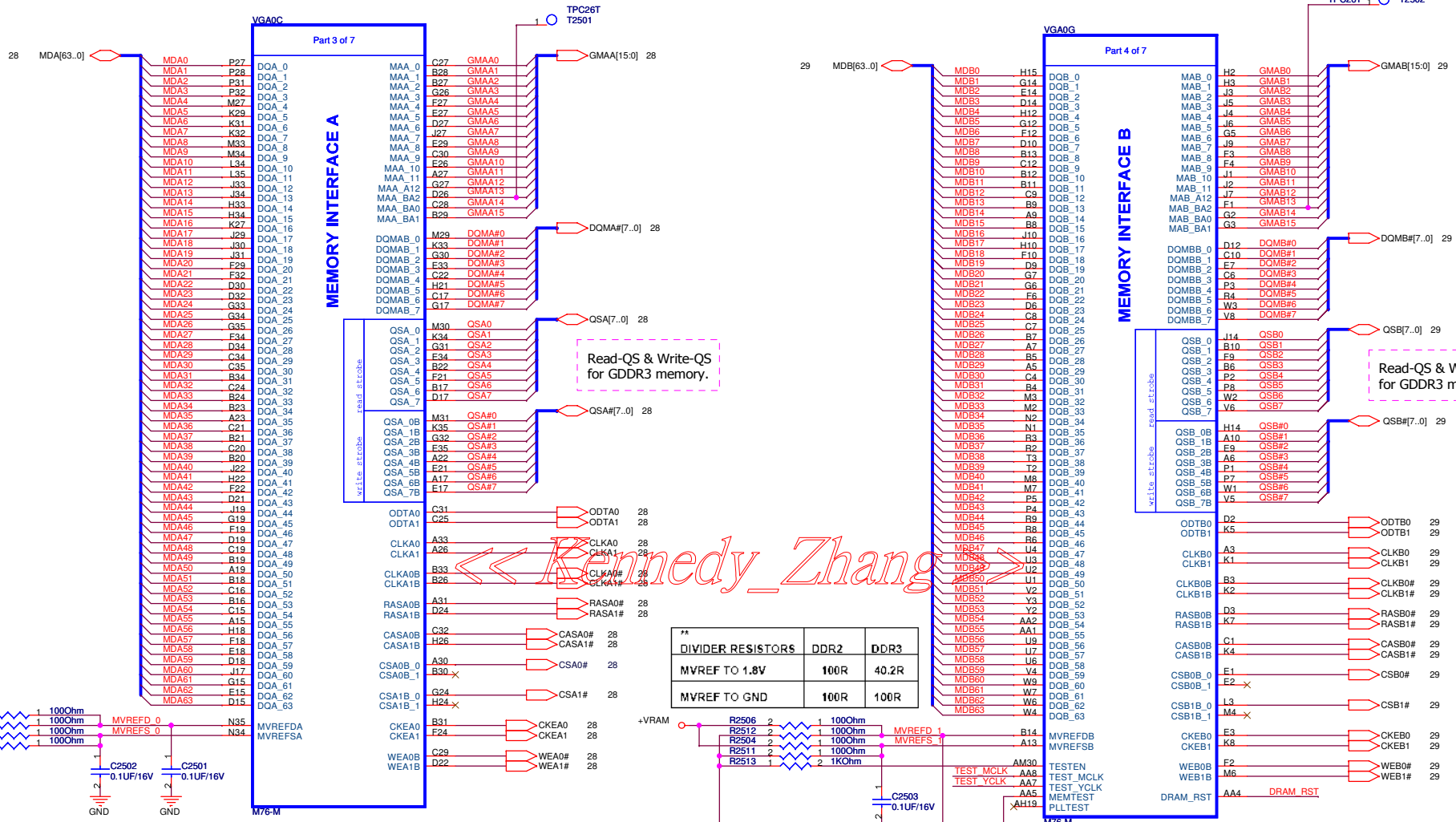
M76 - All mount 0 ohm

HDMI\_EN

CHANGE BOM P/N TO M72

**ASUS** Title: **ATI M7X/66-M\_MAIN**  
 ASUSTek COMPUTER INC Engineer: **Jerry Mou**  
 Size Project Name  
 Custom **F7Sr**  
 Date: 2007.05.10, 2007 Sheet 24 of 95

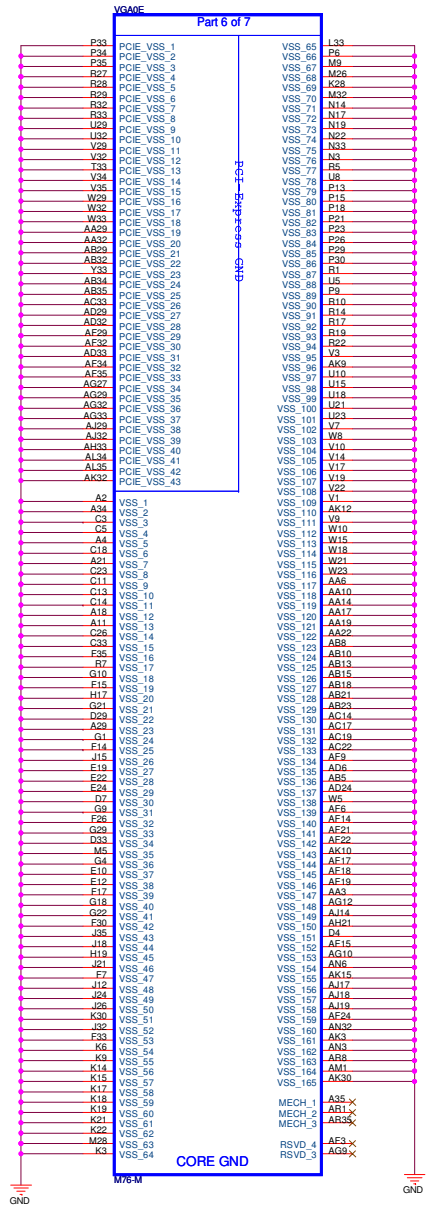




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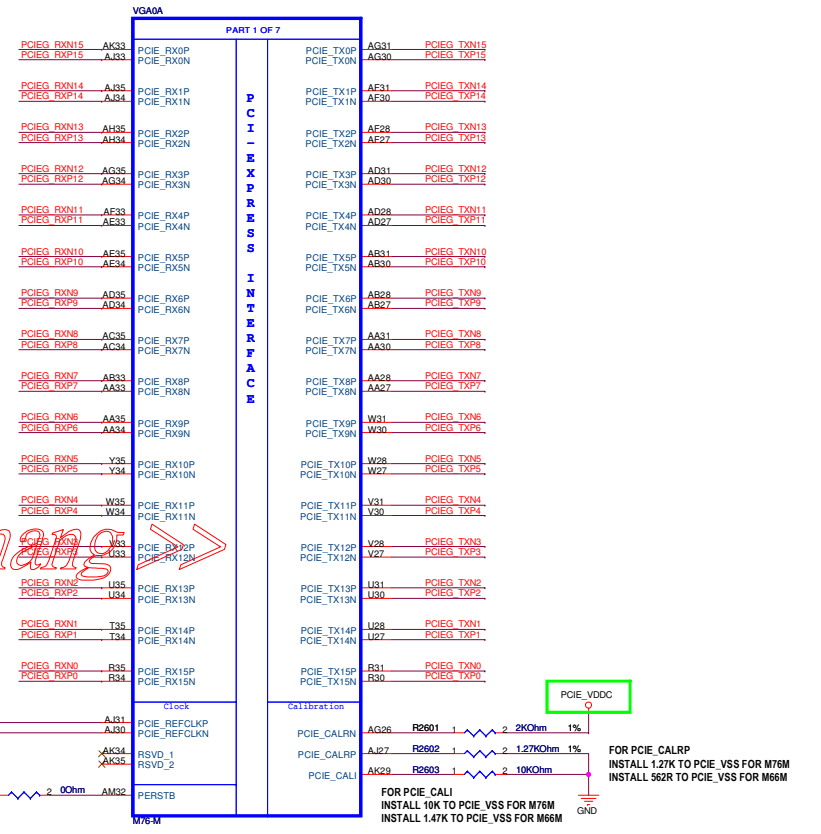
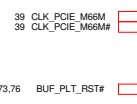
** DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

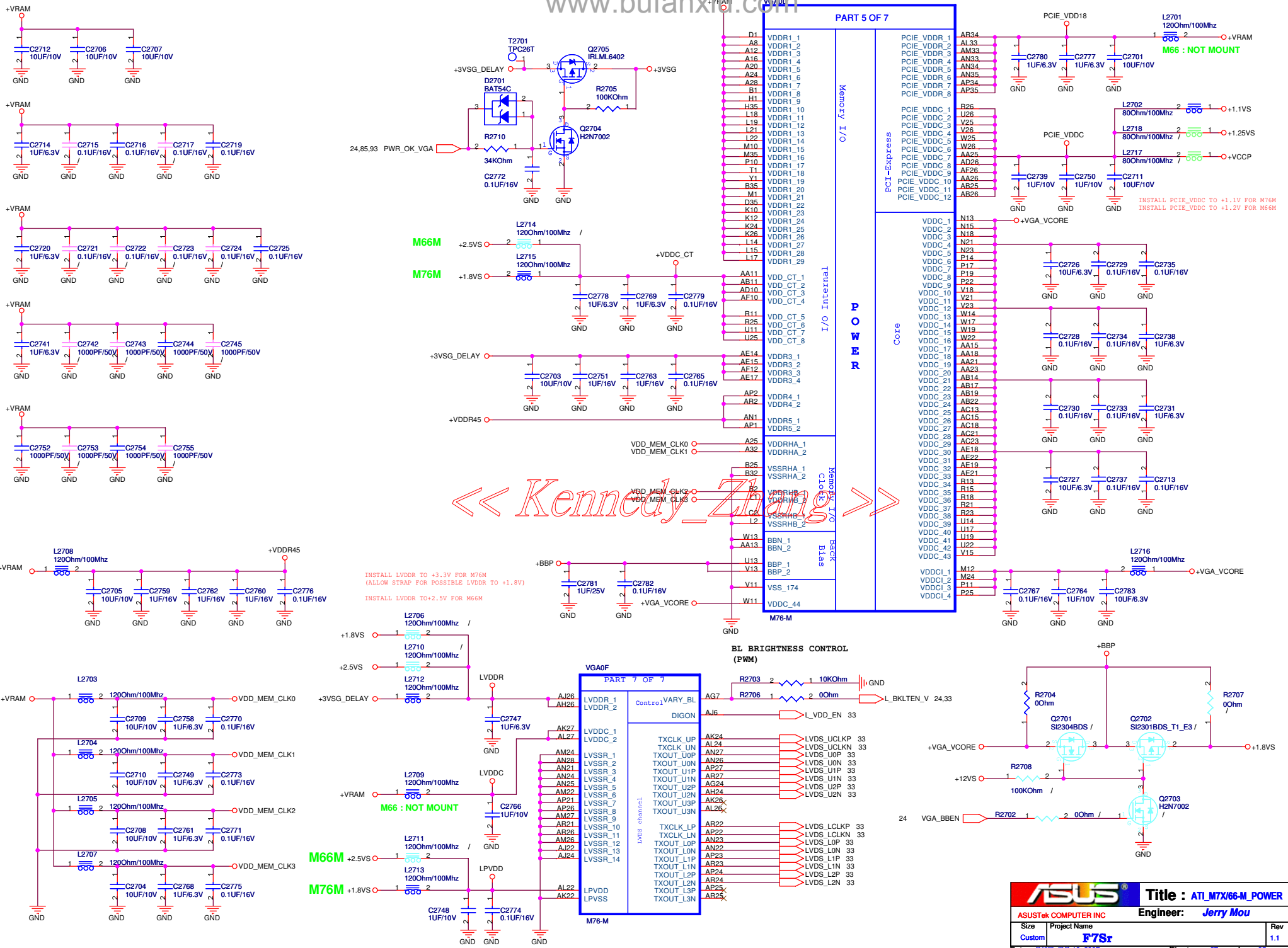
** DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

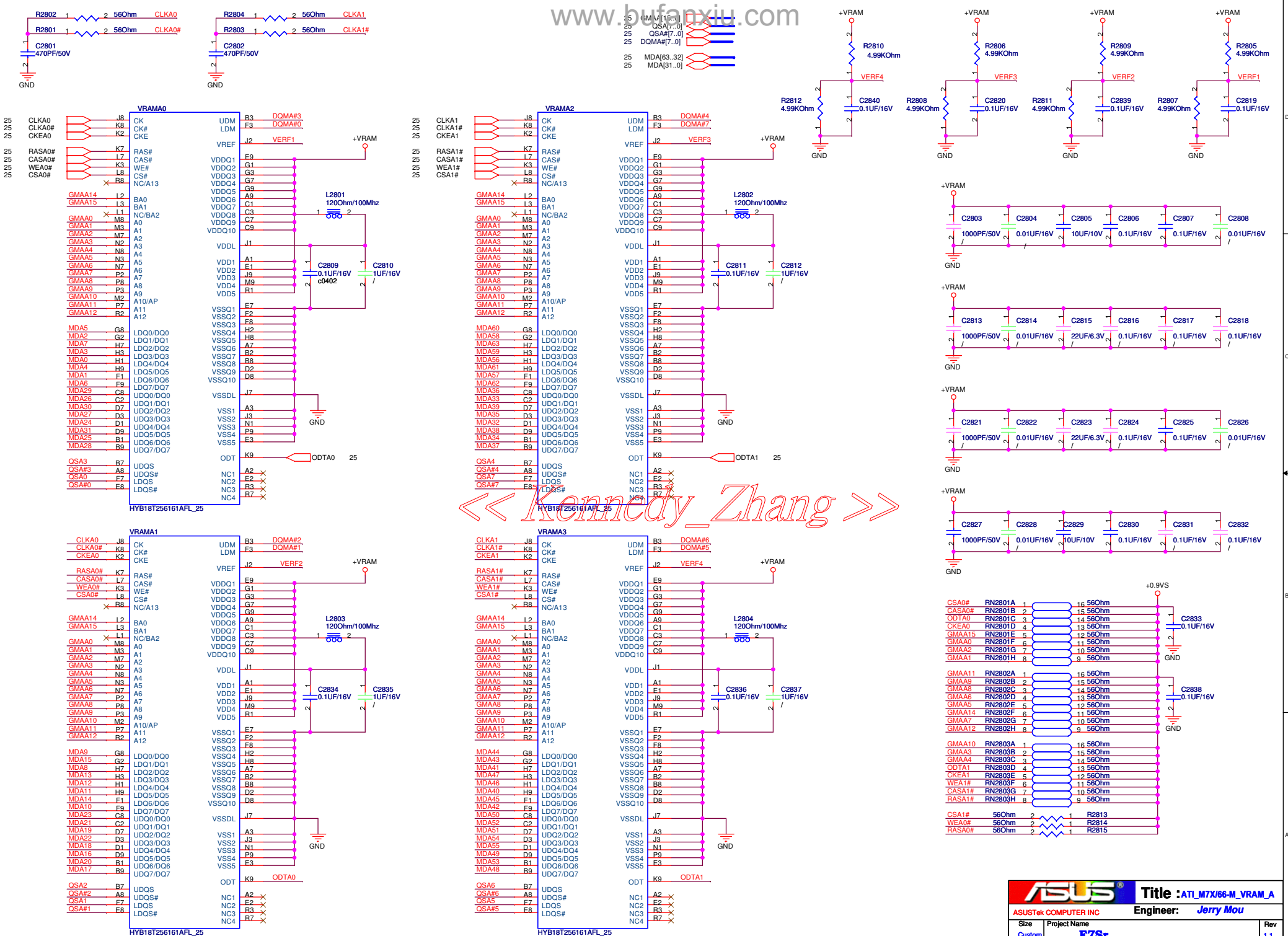


PCIEB_RXN15	C2601	1	2	0.1UF/16V	PCIEG_TXN15
PCIEB_RXP15	C2602	1	2	0.1UF/16V	PCIEG_TXP15
PCIEB_RXN14	C2603	1	2	0.1UF/16V	PCIEG_TXN14
PCIEB_RXP14	C2604	1	2	0.1UF/16V	PCIEG_TXP14
PCIEB_RXN13	C2605	1	2	0.1UF/16V	PCIEG_TXN13
PCIEB_RXP13	C2606	1	2	0.1UF/16V	PCIEG_TXP13
PCIEB_RXN12	C2607	1	2	0.1UF/16V	PCIEG_TXN12
PCIEB_RXP12	C2608	1	2	0.1UF/16V	PCIEG_TXP12
PCIEB_RXN11	C2609	1	2	0.1UF/16V	PCIEG_TXN11
PCIEB_RXP11	C2610	1	2	0.1UF/16V	PCIEG_TXP11
PCIEB_RXN10	C2611	1	2	0.1UF/16V	PCIEG_TXN10
PCIEB_RXP10	C2612	1	2	0.1UF/16V	PCIEG_TXP10
PCIEB_RXN9	C2613	1	2	0.1UF/16V	PCIEG_TXN9
PCIEB_RXP9	C2614	1	2	0.1UF/16V	PCIEG_TXP9
PCIEB_RXN8	C2615	1	2	0.1UF/16V	PCIEG_TXN8
PCIEB_RXP8	C2616	1	2	0.1UF/16V	PCIEG_TXP8
PCIEB_RXN7	C2617	1	2	0.1UF/16V	PCIEG_TXN7
PCIEB_RXP7	C2618	1	2	0.1UF/16V	PCIEG_TXP7
PCIEB_RXN6	C2619	1	2	0.1UF/16V	PCIEG_TXN6
PCIEB_RXP6	C2620	1	2	0.1UF/16V	PCIEG_TXP6
PCIEB_RXN5	C2621	1	2	0.1UF/16V	PCIEG_TXN5
PCIEB_RXP5	C2622	1	2	0.1UF/16V	PCIEG_TXP5
PCIEB_RXN4	C2623	1	2	0.1UF/16V	PCIEG_TXN4
PCIEB_RXP4	C2624	1	2	0.1UF/16V	PCIEG_TXP4
PCIEB_RXN3	C2625	1	2	0.1UF/16V	PCIEG_TXN3
PCIEB_RXP3	C2626	1	2	0.1UF/16V	PCIEG_TXP3
PCIEB_RXN2	C2627	1	2	0.1UF/16V	PCIEG_TXN2
PCIEB_RXP2	C2628	1	2	0.1UF/16V	PCIEG_TXP2
PCIEB_RXN1	C2629	1	2	0.1UF/16V	PCIEG_TXN1
PCIEB_RXP1	C2630	1	2	0.1UF/16V	PCIEG_TXP1
PCIEB_RXN0	C2631	1	2	0.1UF/16V	PCIEG_TXN0
PCIEB_RXP0	C2632	1	2	0.1UF/16V	PCIEG_TXP0

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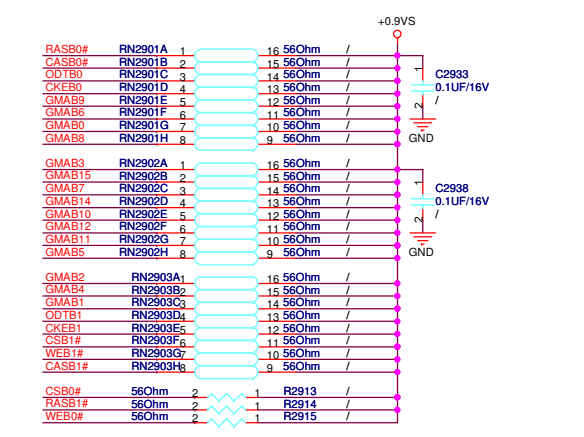
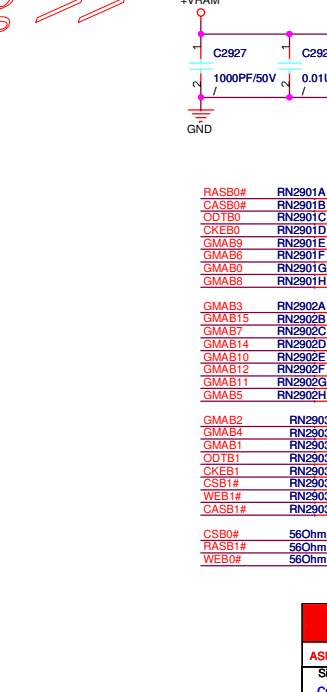
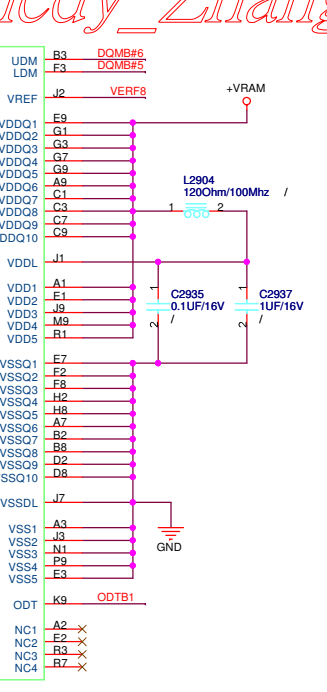
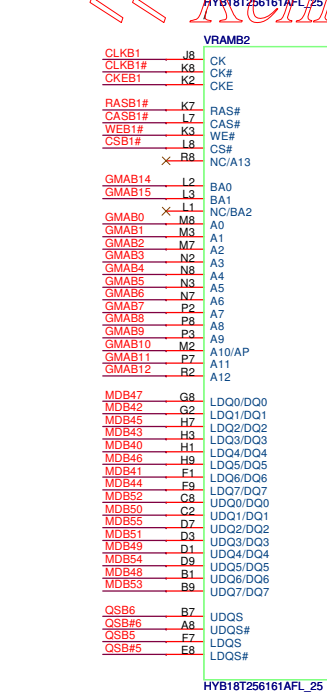
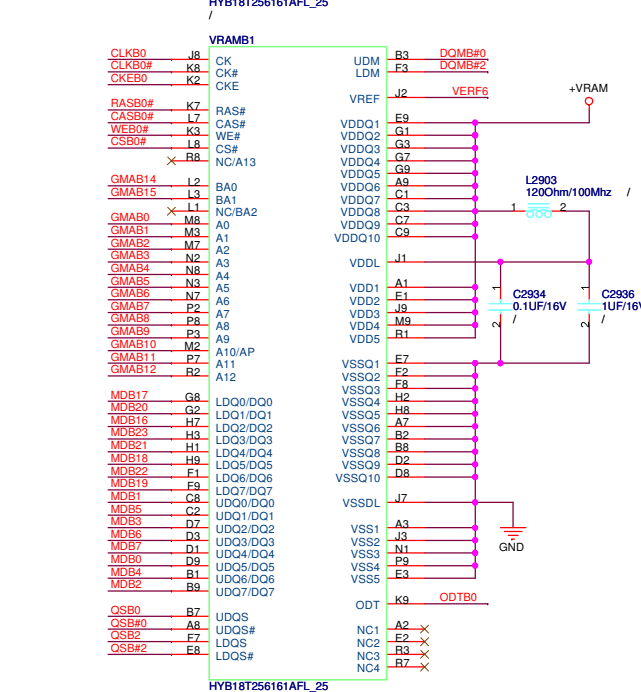
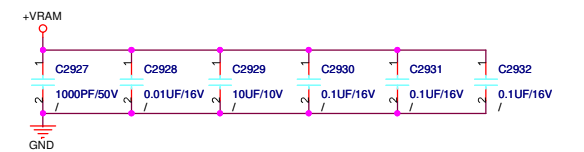
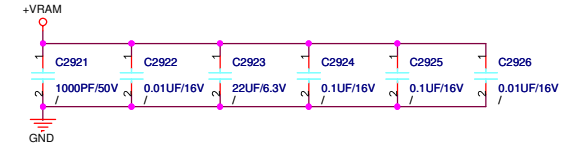
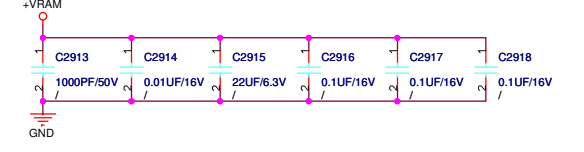
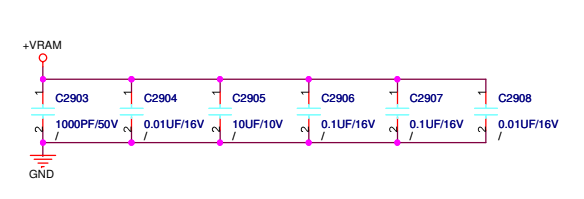
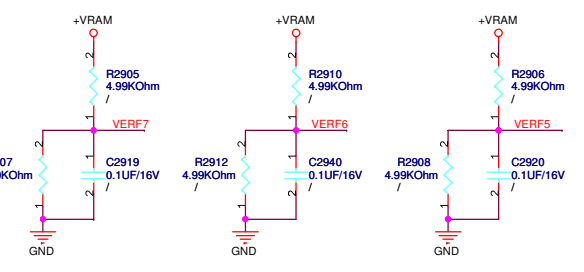
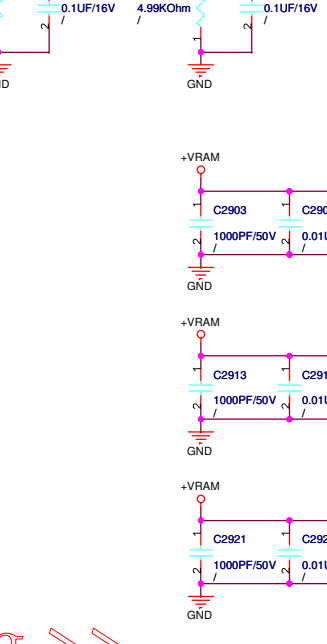
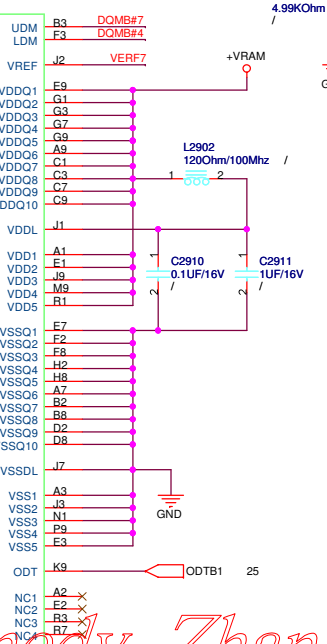
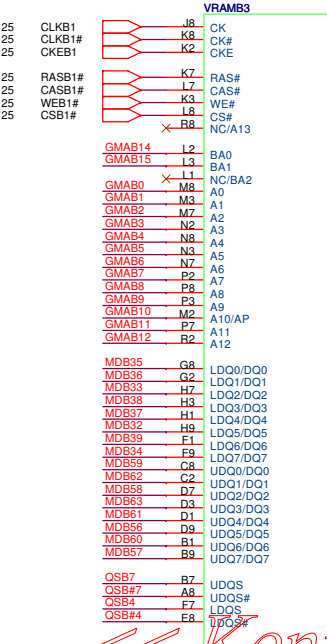
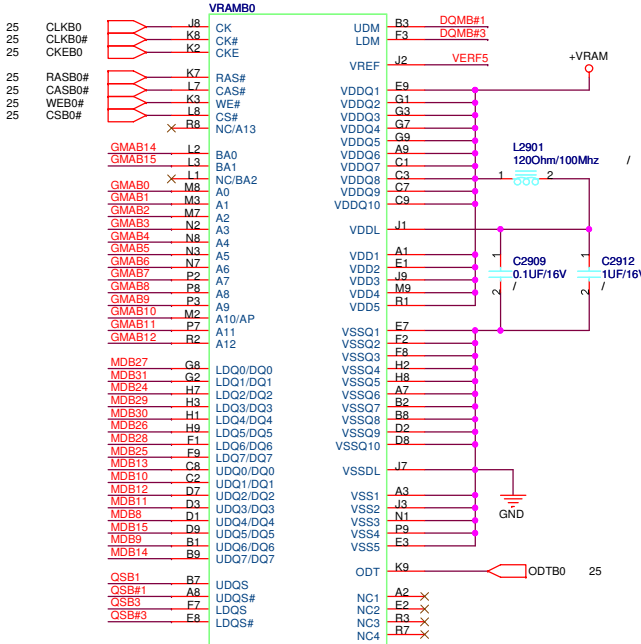
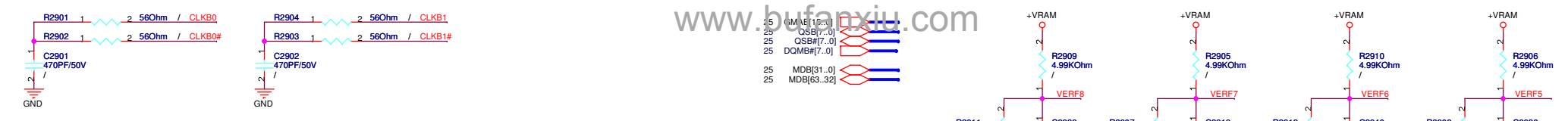






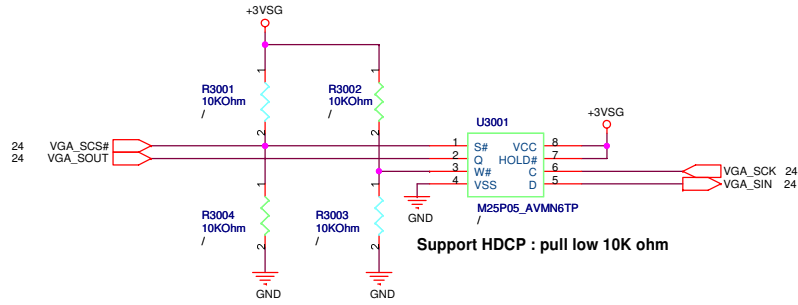
<< Kennedy\_Zhang >>

<b>ASUS</b>		<b>Title : ATU_M7X/66-M_VRAM_A</b>	
ASUSTek COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 星期五, 五月 10, 2007		Sheet	28 of 95



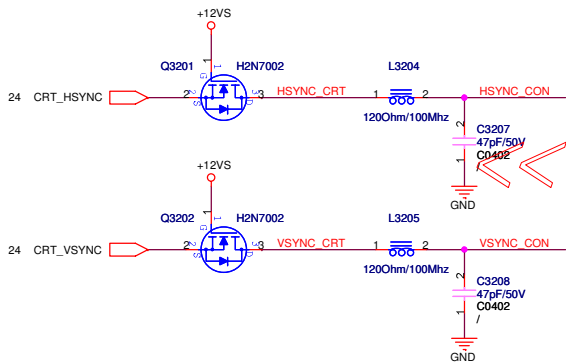
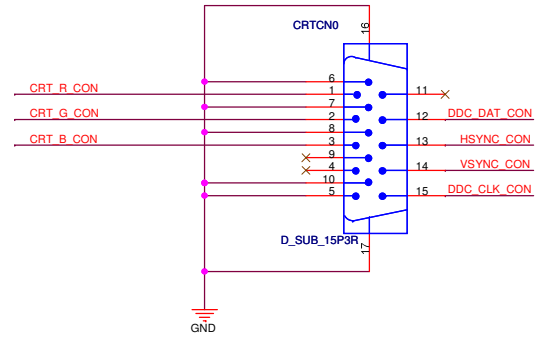
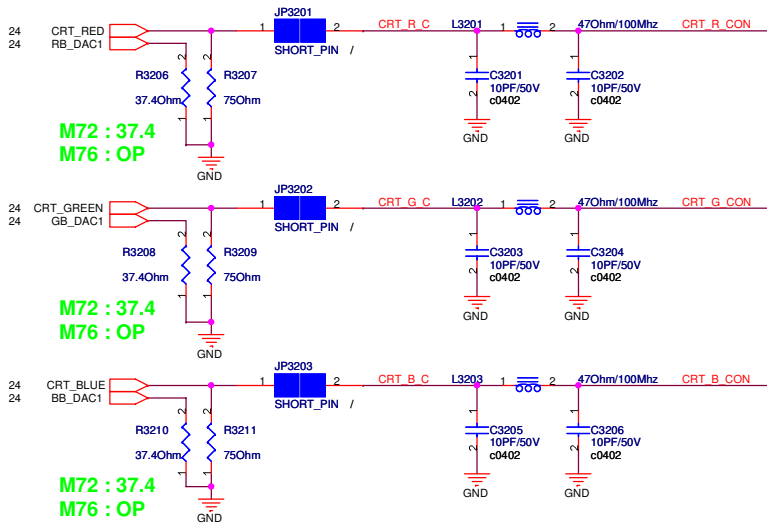
ASUS logo and title block: Title : AT1\_M7X66-M\_VRAM\_B, Engineer: Jerry Mou, Date: 2007.05.10, Sheet 29 of 95.

<< Kennedy\_Zhang >>



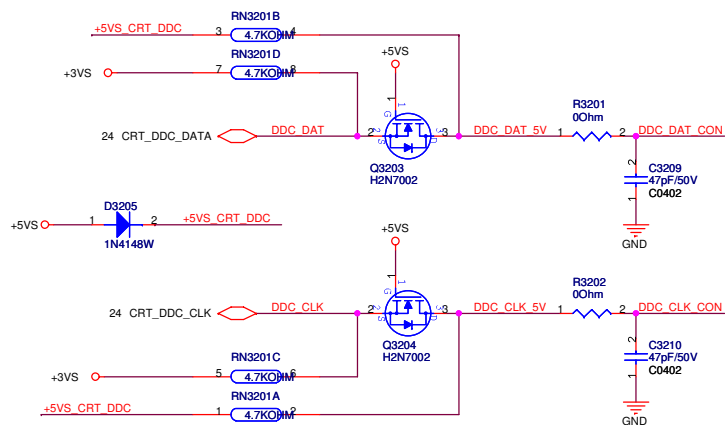
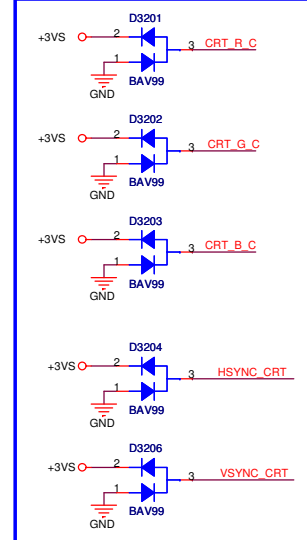
<< Kennedy\_Zhang >>

<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

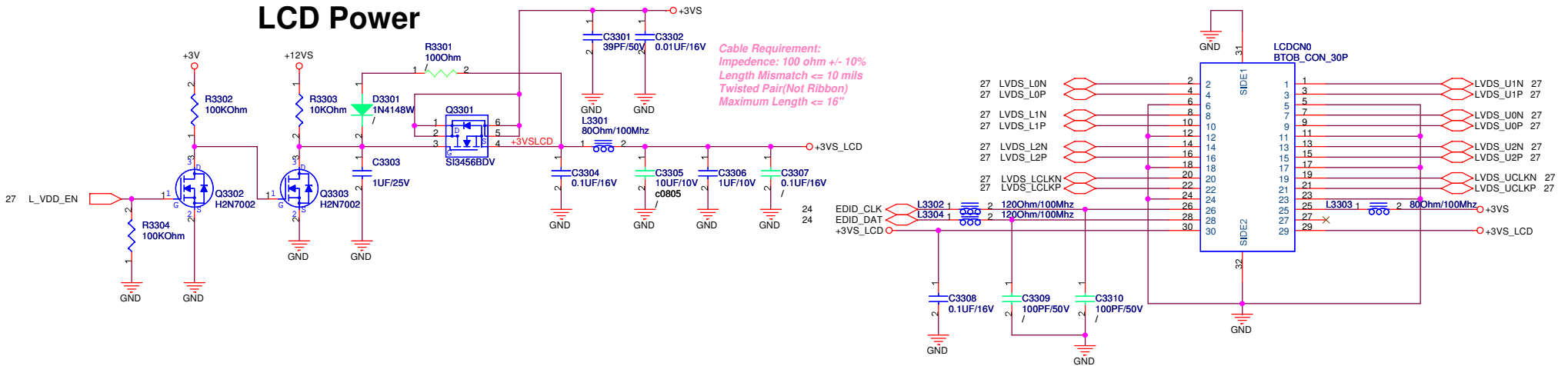
PLACE ESD Diodes near VGA port



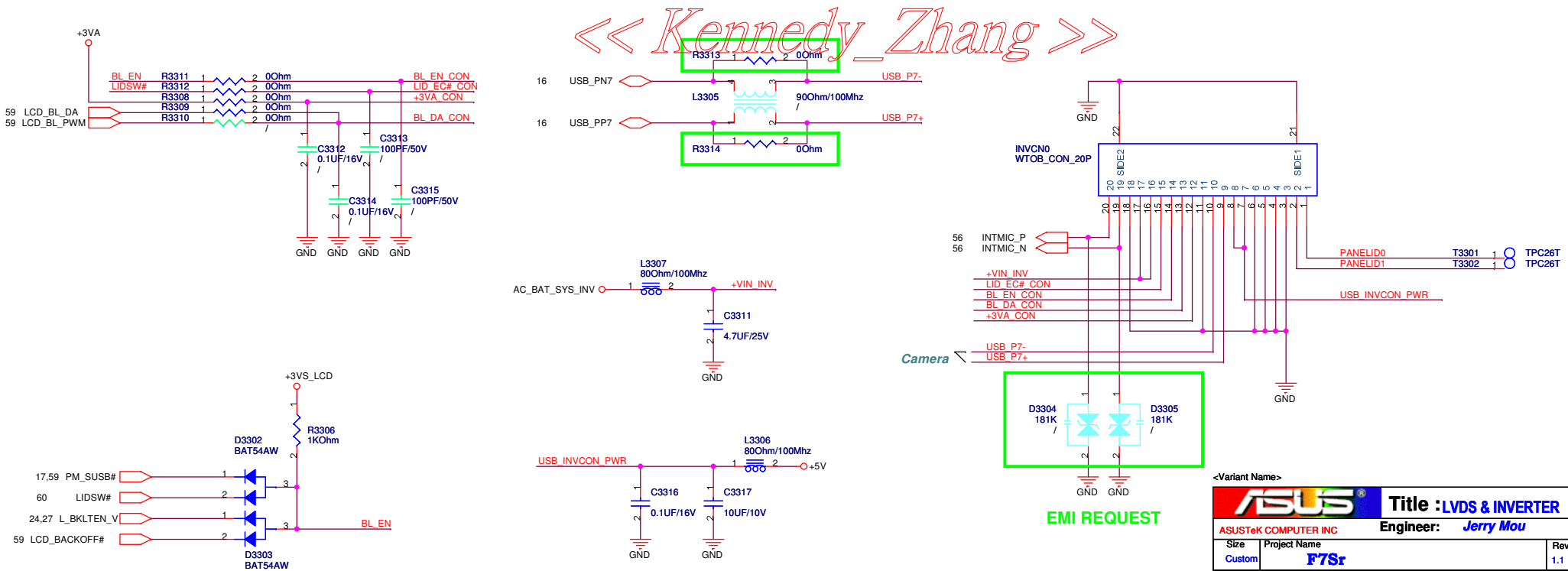


LCD LVDS Interface

LCD Power



INVERTER Interface/Speaker CONN.

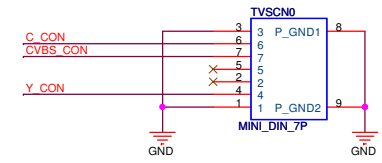
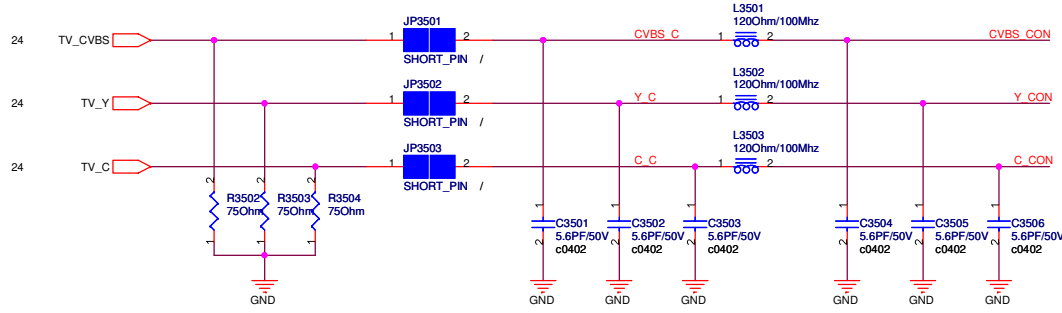
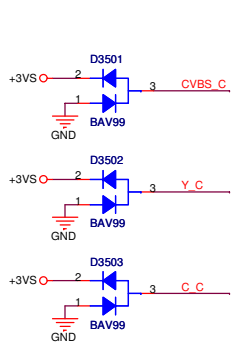


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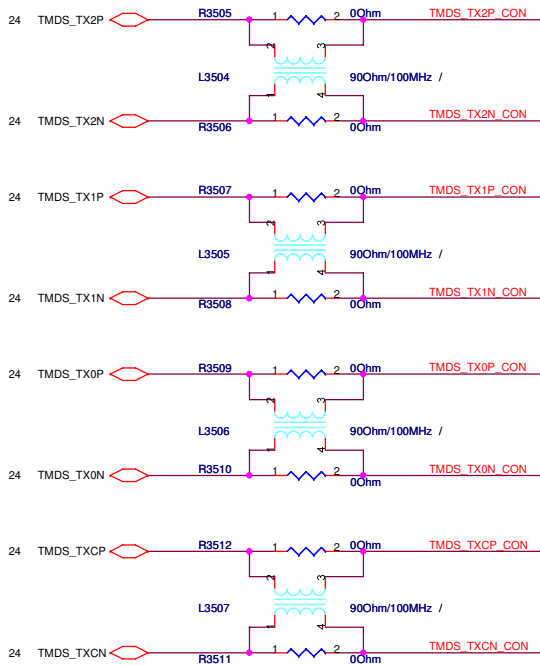
<b>ASUS</b>		<b>Title :LVDS &amp; INVERTER</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Jerry Mou</b>	
Size	Project Name	Rev	1.1
Custom	<b>F7Sr</b>	Date:	星期四, 五月 10, 2007
Date: 星期四, 五月 10, 2007		Sheet	33 of 95

<< Kennedy\_Zhang >>

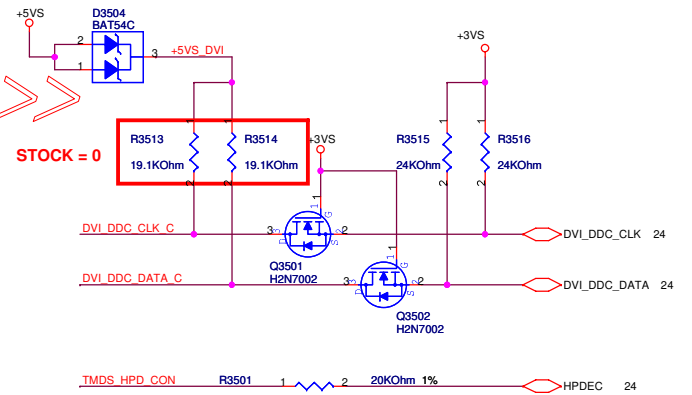
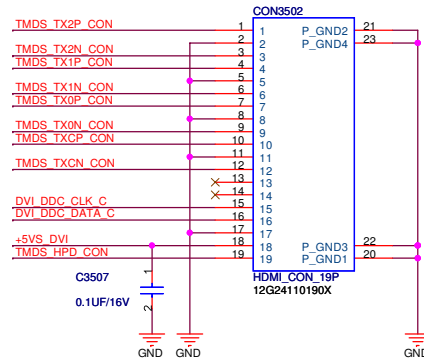
# TV OUT



# HDMI

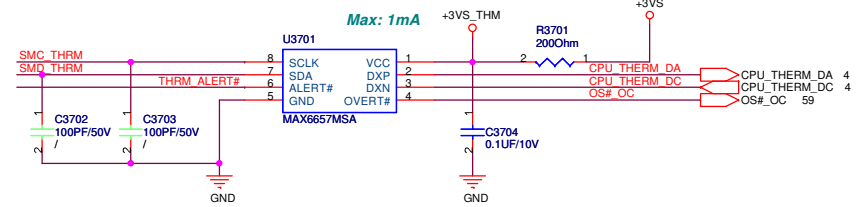
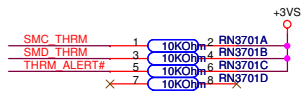
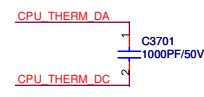
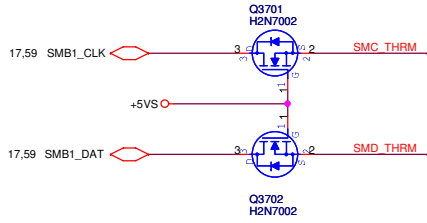


<< Kennedy\_Zhang >>



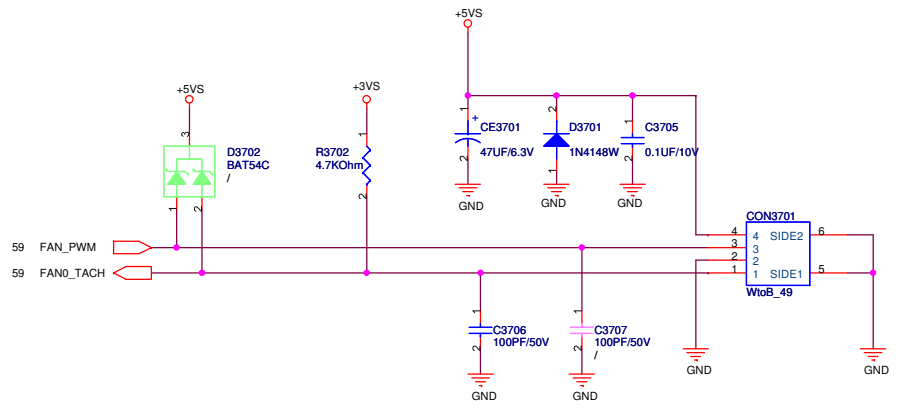
<< Kennedy\_Zhang >>

### Thermal Sensor

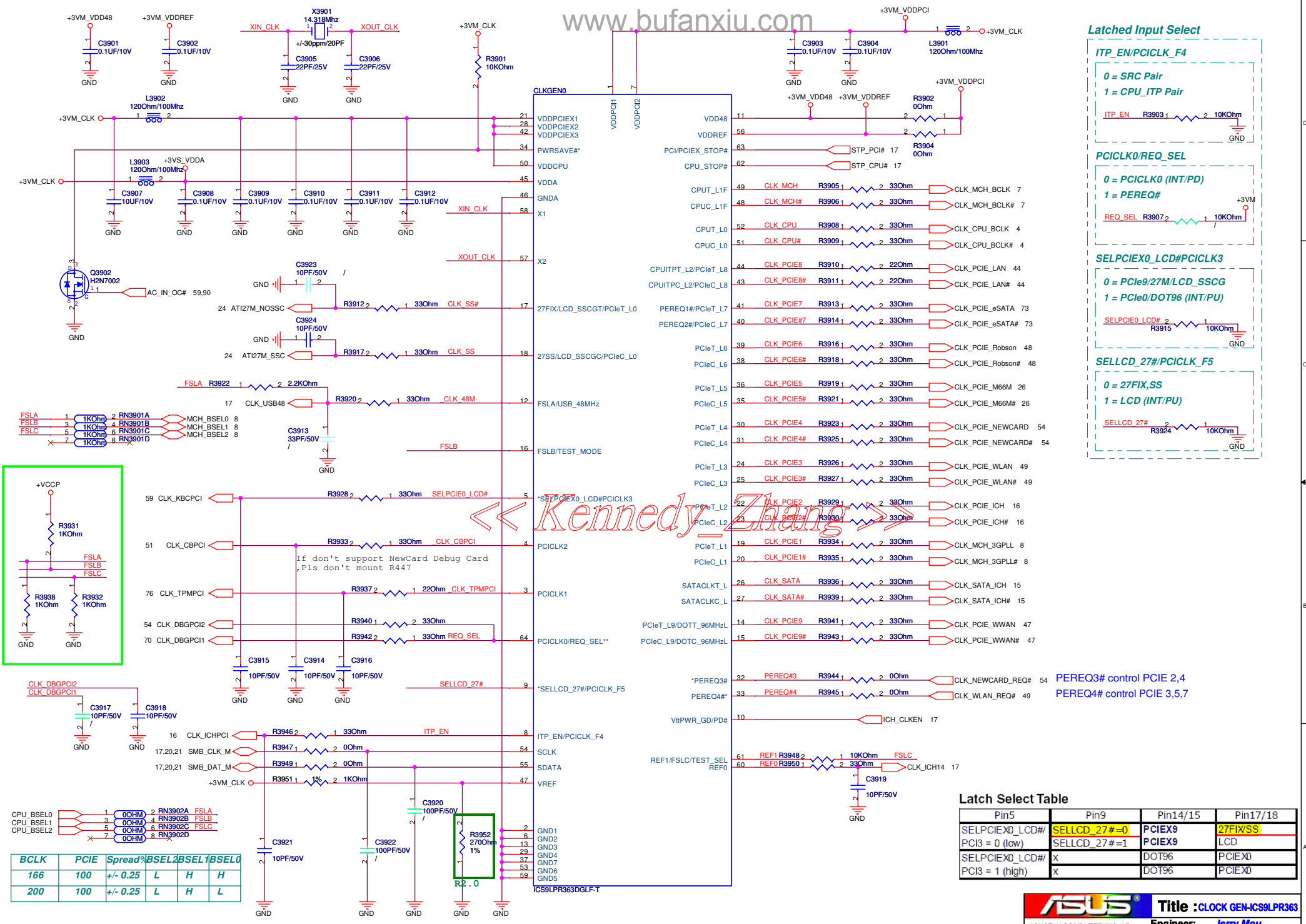


### DC FAN Control

<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>



**Latched Input Select**

**ITP\_EN/PCICLK\_F4**

0 = SRC Pair  
1 = CPU\_ITP Pair

**PCICLK0/REQ\_SEL**

0 = PCICLK0 (INT/PD)  
1 = PEREQ#

**SELPCIEX0\_LCD#PCICLK3**

0 = PCIe9/27M/LCD\_SSCG  
1 = PCIe0/DOT96 (INT/PU)

**SELLCD\_27#/PCICLK\_F5**

0 = 27FIX,SS  
1 = LCD (INT/PU)

PEREQ3# control PCIe 2,4  
PEREQ4# control PCIe 3,5,7

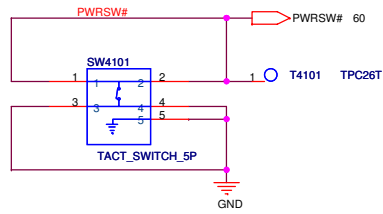
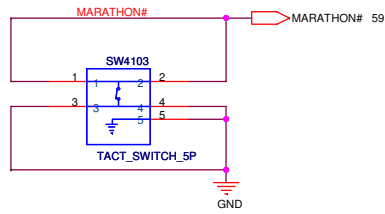
**Latch Select Table**

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#	SELLCD_27# = 0	PCIEX9	27FIX/SS
PCI3 = 0 (low)	SELLCD_27# = 1	PCIEX9	LCD
SELPCIEX0_LCD#	X	DOT96	PCIEX0
PCI3 = 1 (high)	X	DOT96	PCIEX0

BCLK	PCIE	Spread%	%BSEL2	%BSEL1	%BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L

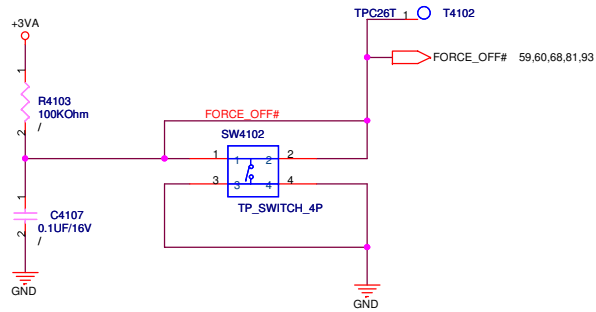
<< Kennedy\_Zhang >>

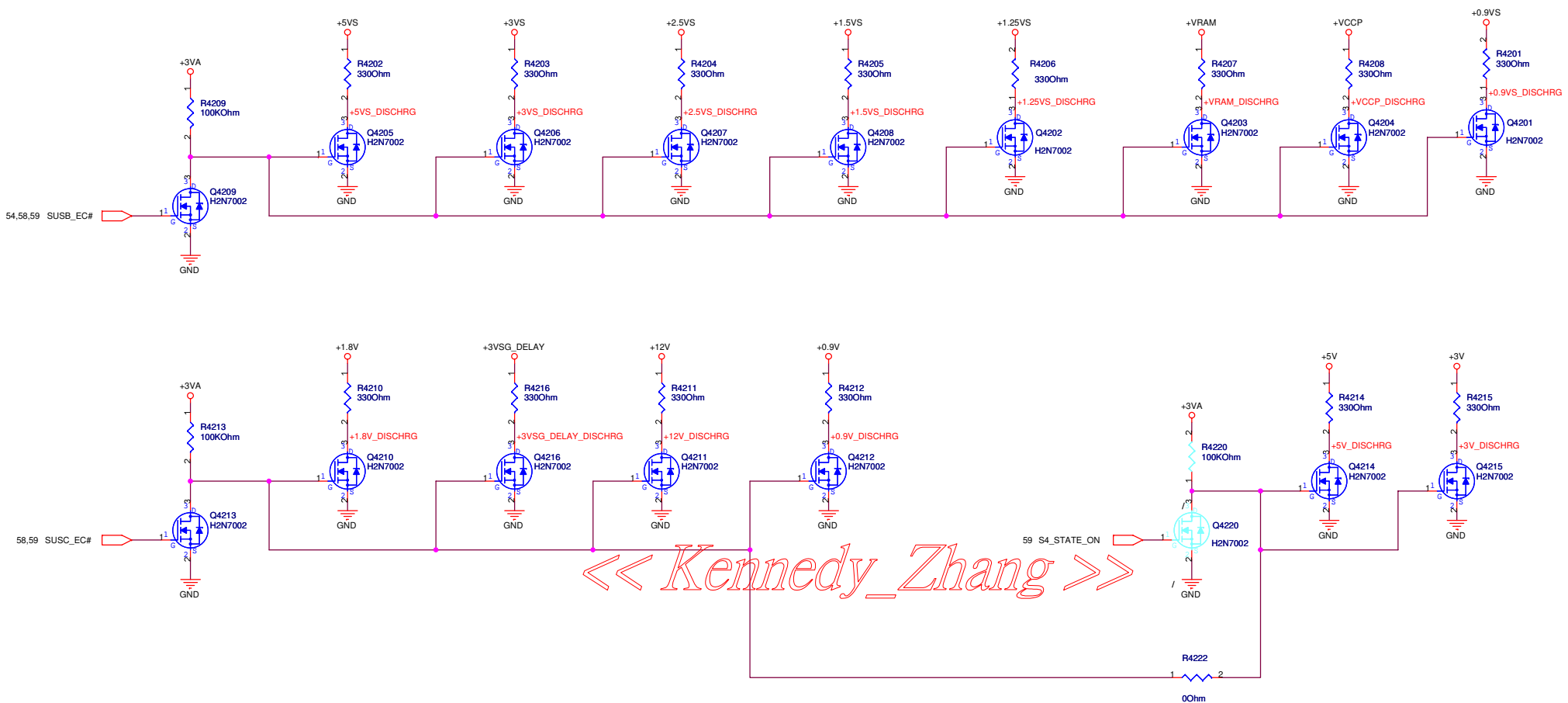




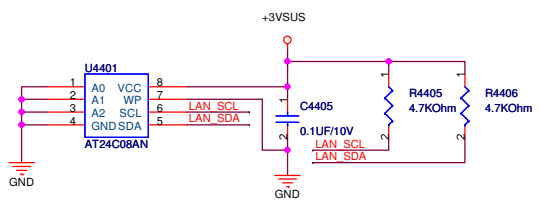
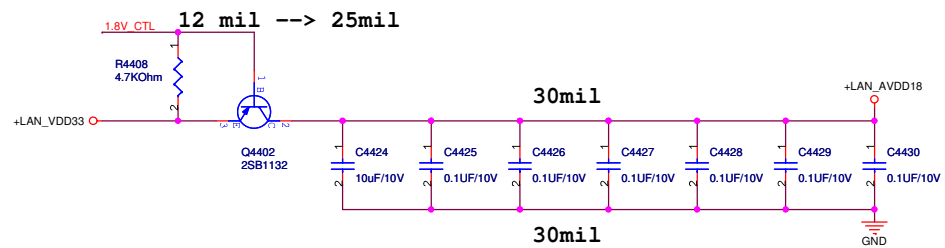
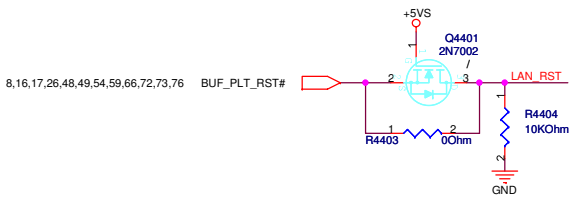
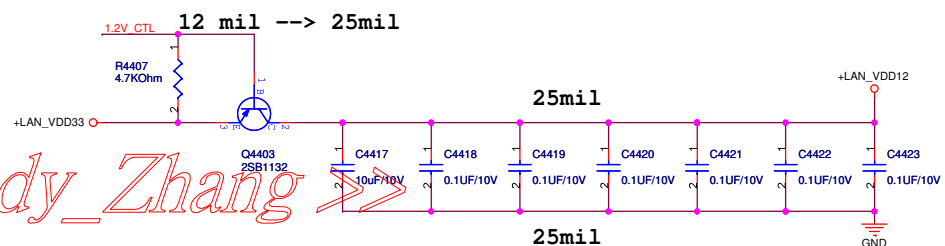
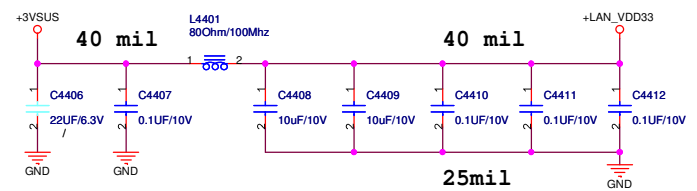
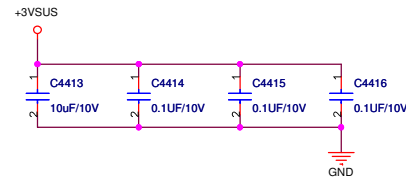
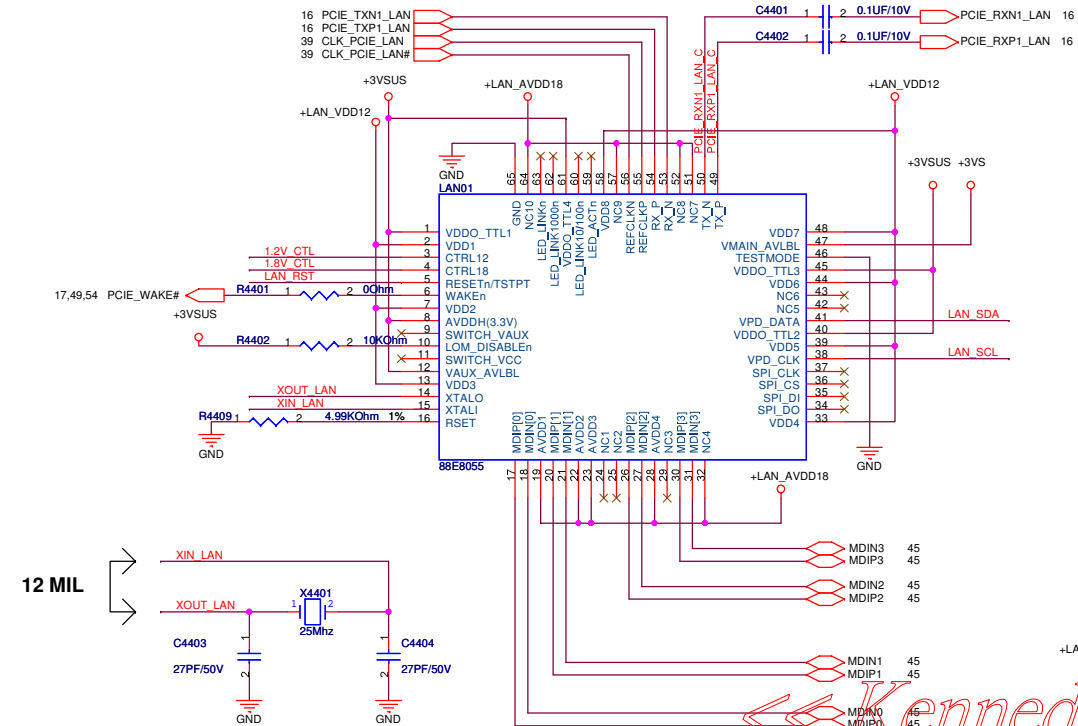
<< Kennedy\_Zhang >>

SHUT\_DOWN#



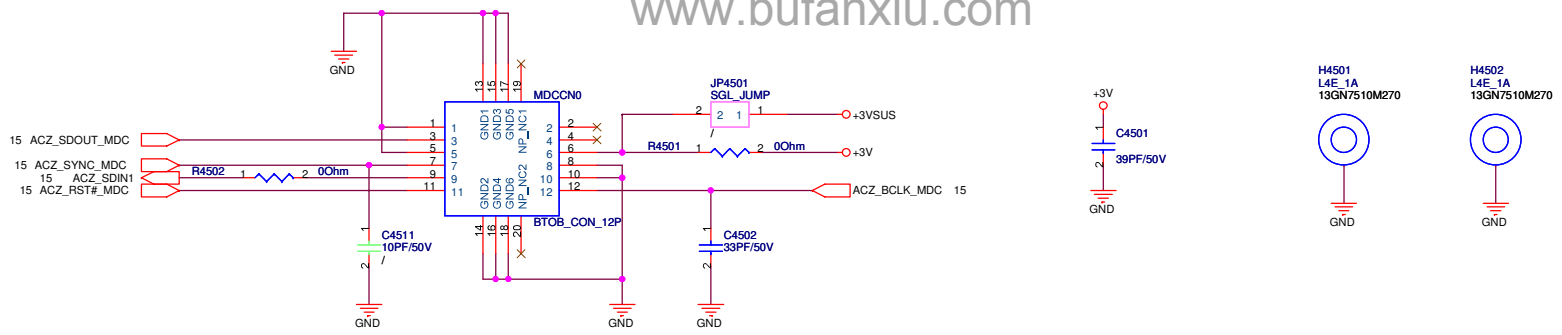


<< Kennedy\_Zhang >>



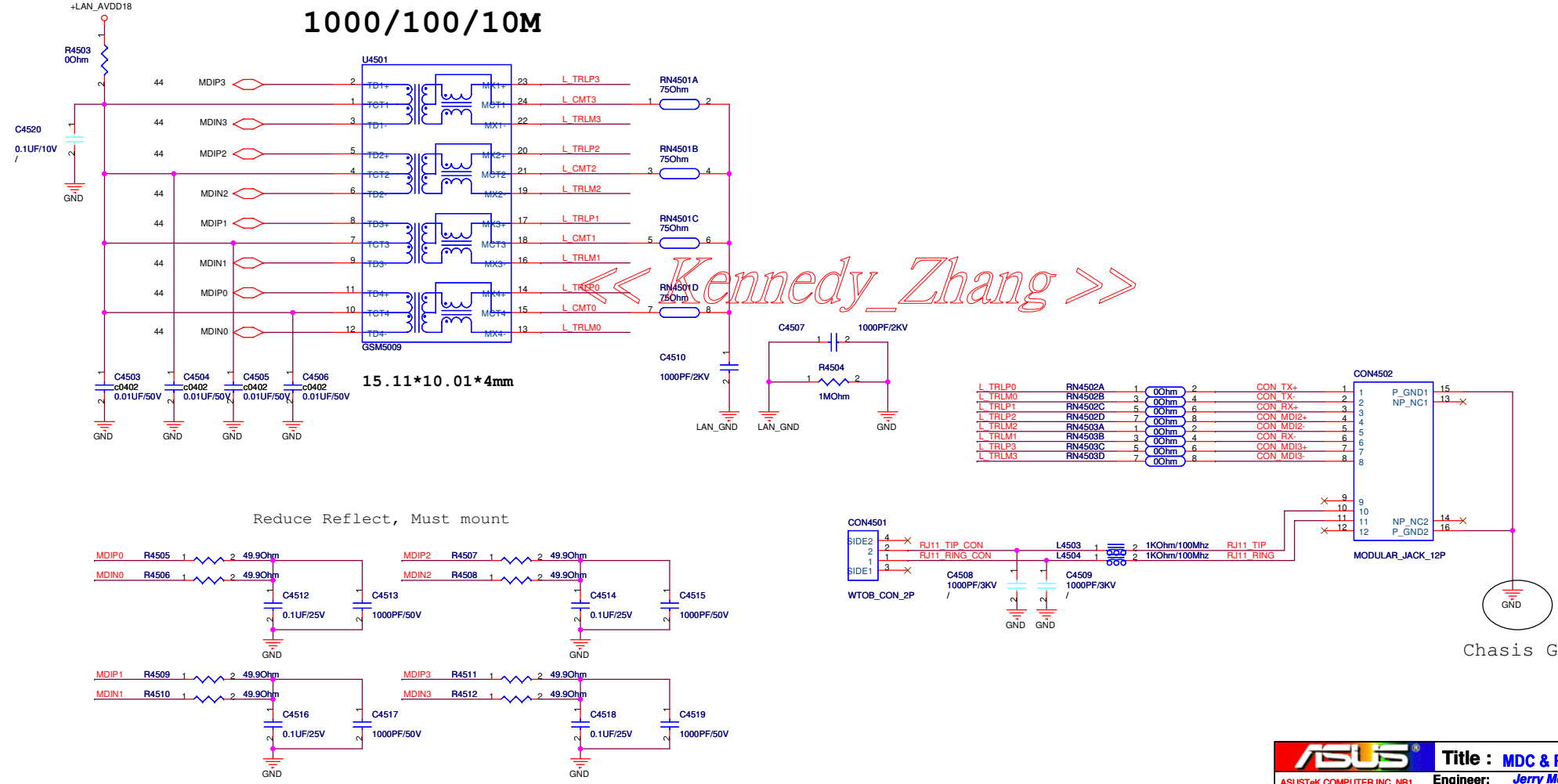
« Kennedy\_Zhang »

MDC CONN.

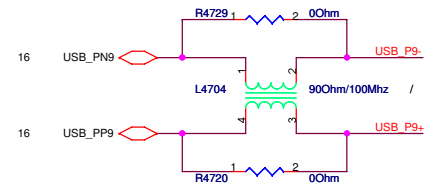
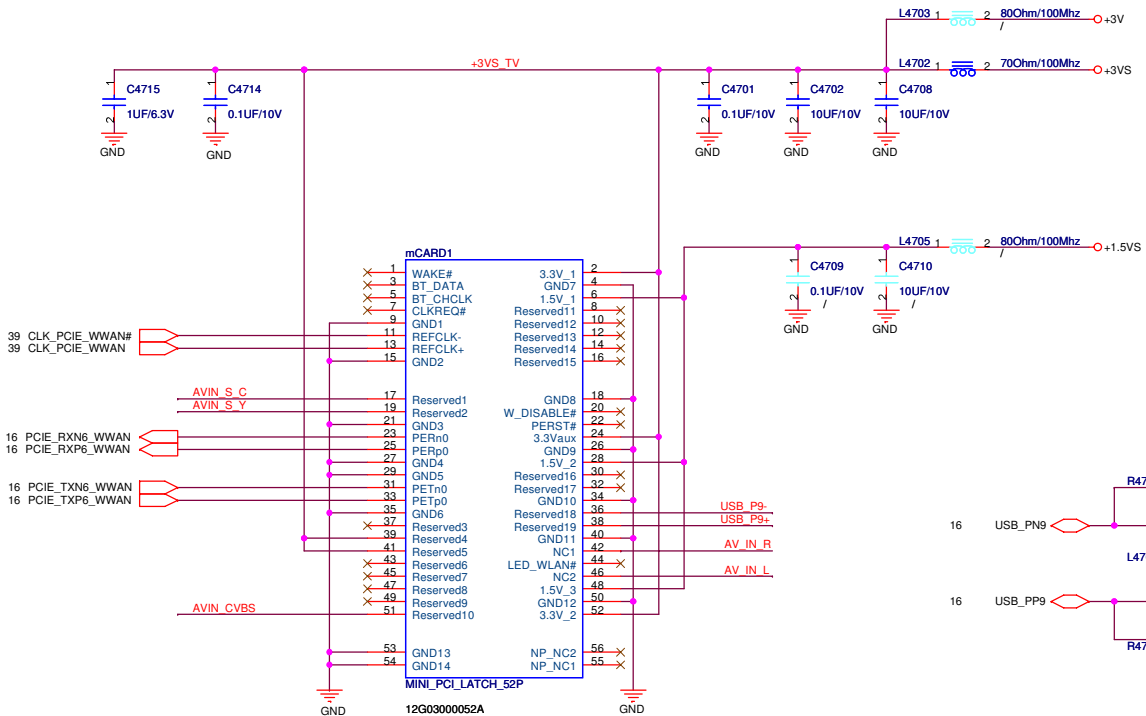


LAN CONN.

1000/100/10M

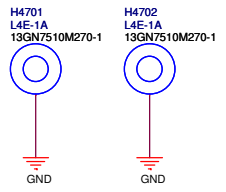
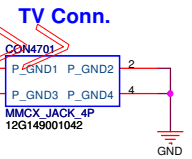


<< Kennedy\_Zhang >>



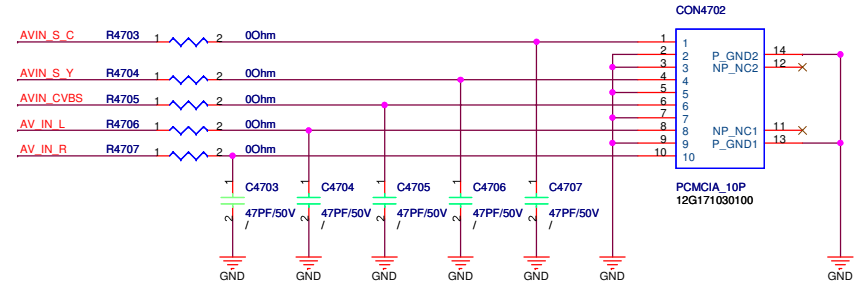
**H = 5.2mm**  
**FOR TV TUNER**  
**(UWB OPTION)**

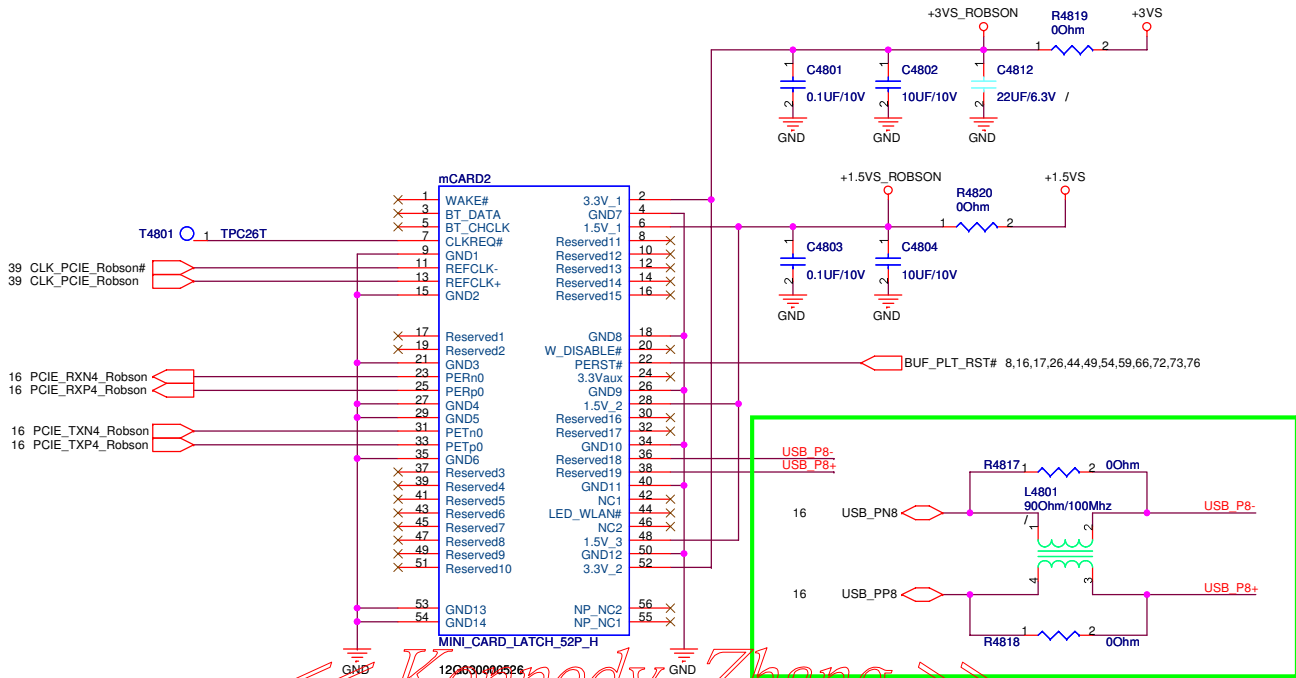
Kennedy\_Zhang



**H = 3.0mm**

**ME P/N : 14G152075000**

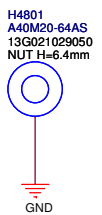




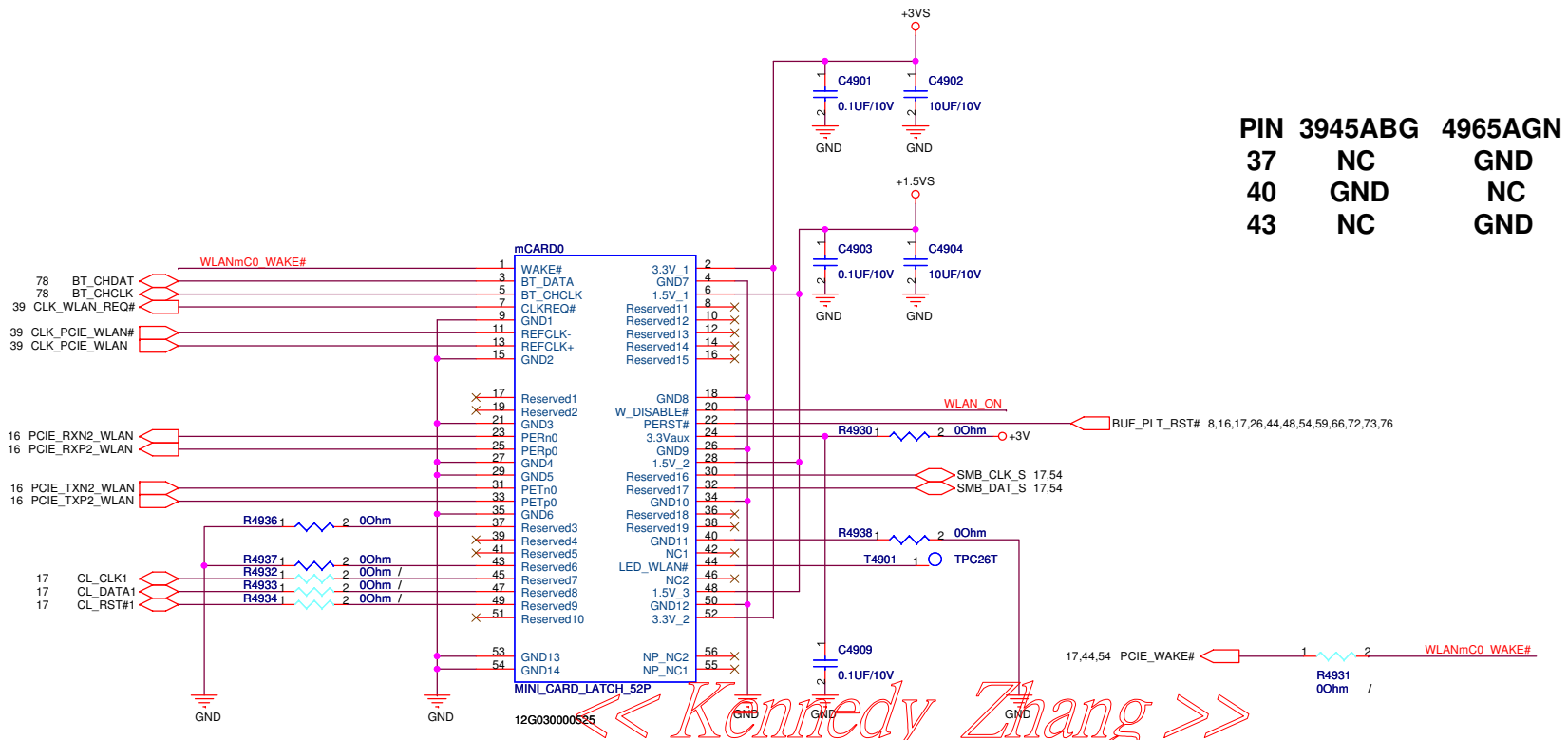
« Kennedy\_Zhang »

RESERVED

FOR ROBSON  
H=9.0mm

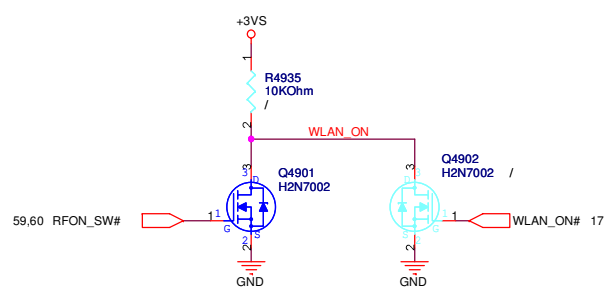
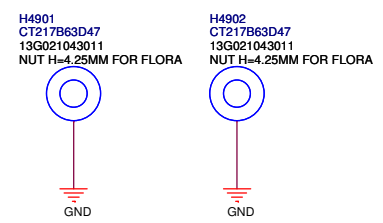




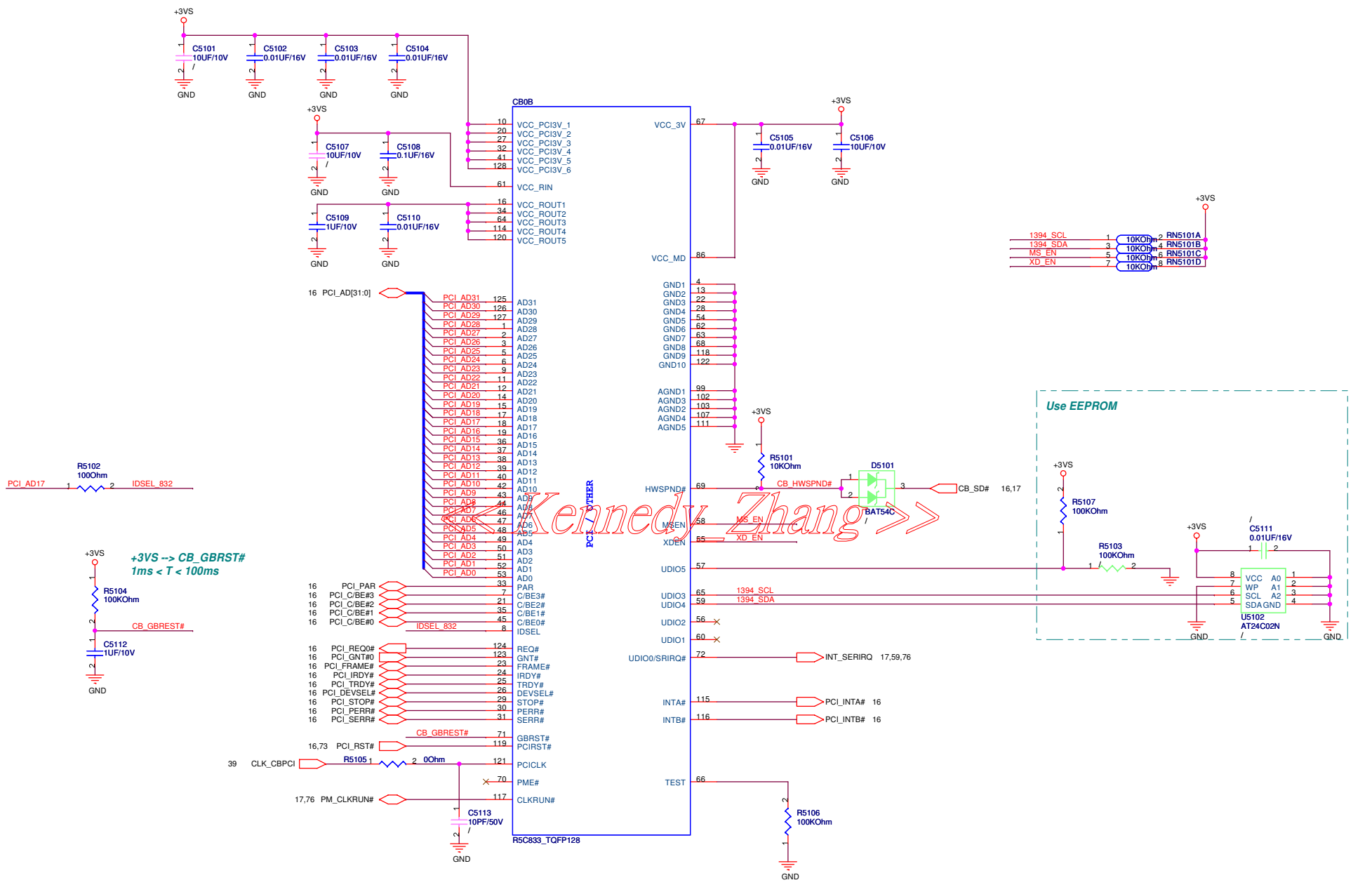


PIN	3945ABG	4965AGN
37	NC	GND
40	GND	NC
43	NC	GND

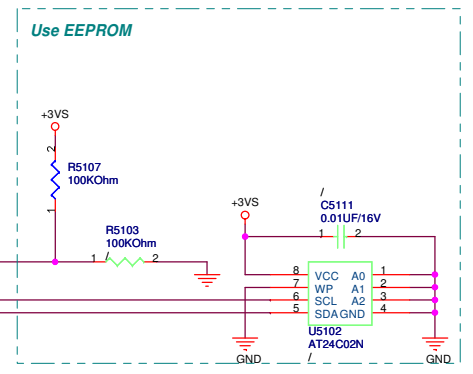
H = 6.75mm  
FOR WLAN

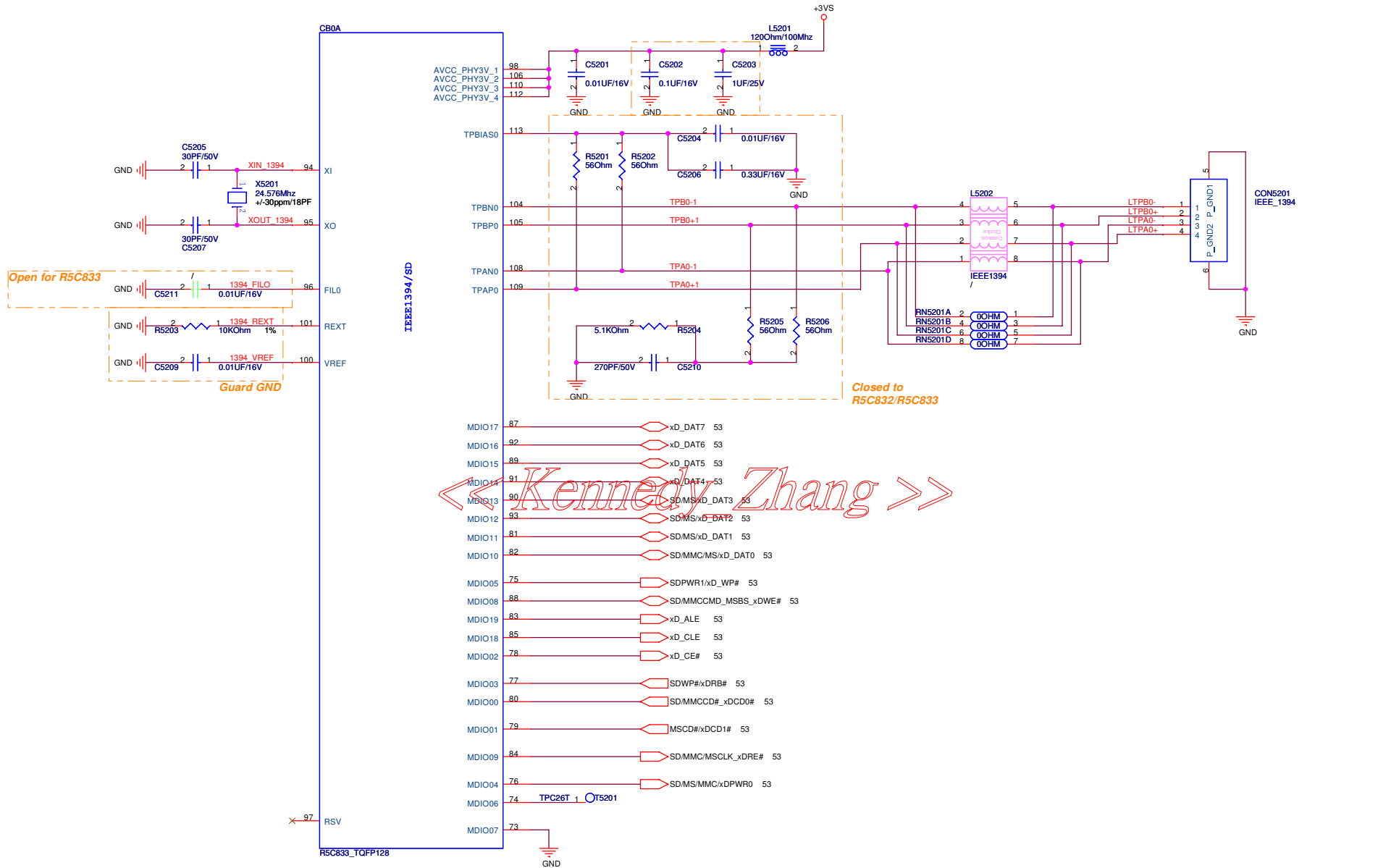


<< Kennedy\_Zhang >>



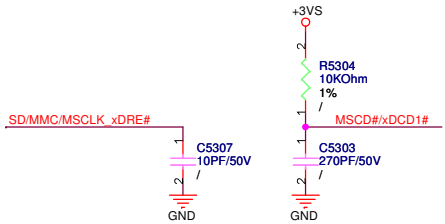
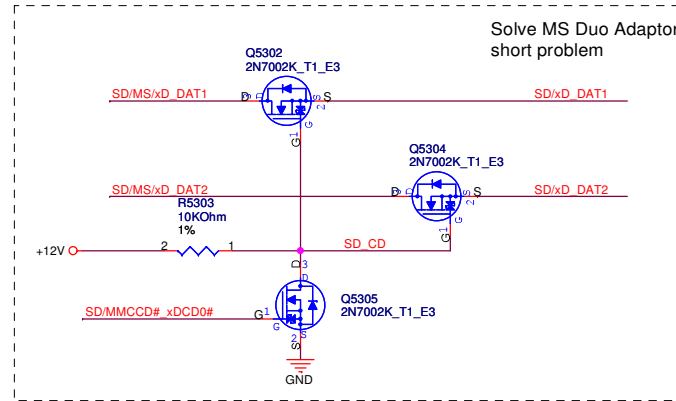
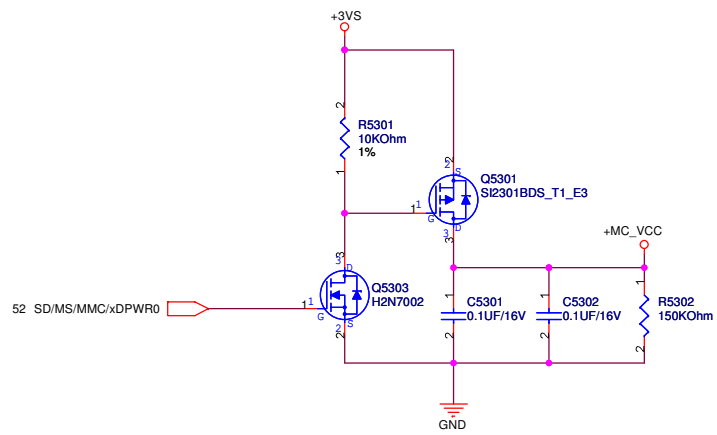
Kennedy Zhang



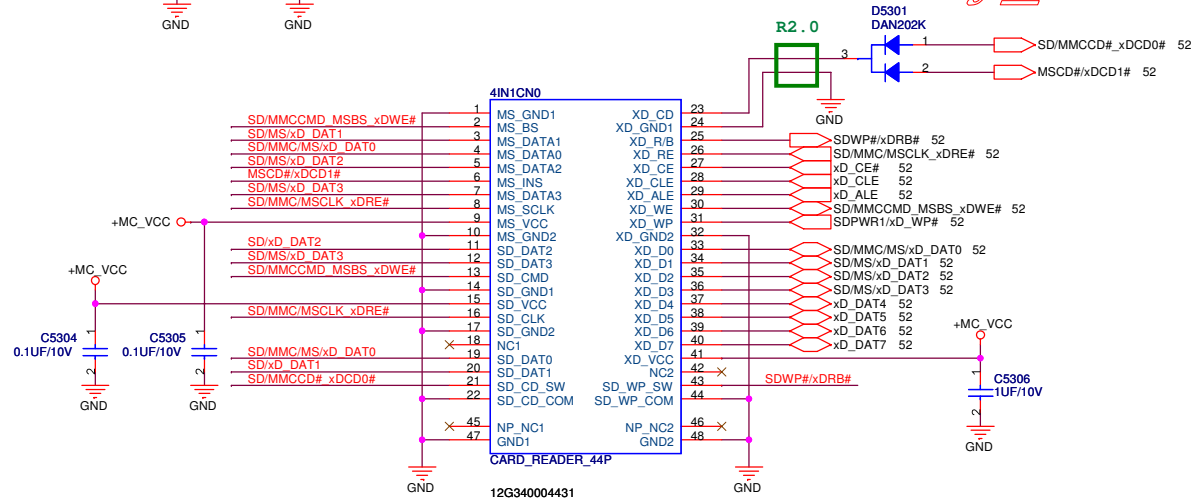


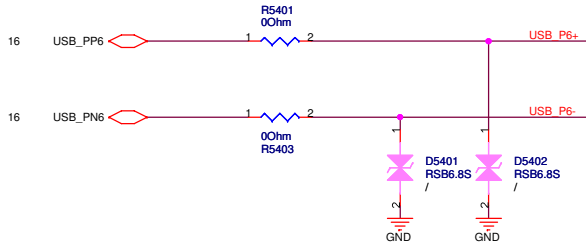
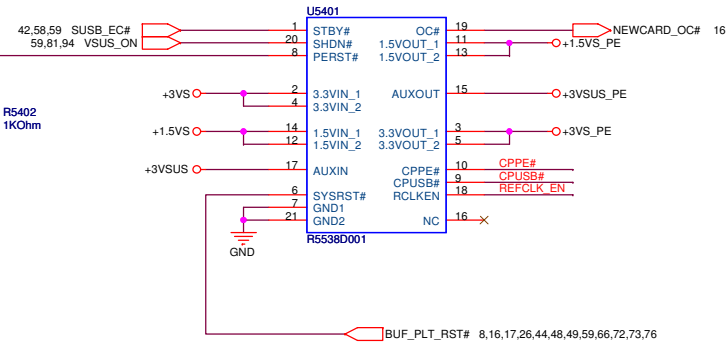
<< Kennedy Zhang >>

- MDIO17 87 xD\_DAT7 53
- MDIO16 92 xD\_DAT6 53
- MDIO15 89 xD\_DAT5 53
- MDIO14 91 xD\_DAT4 53
- MDIO13 90 SD/MSxD\_DAT3 53
- MDIO12 93 SD/MSxD\_DAT2 53
- MDIO11 81 SD/MSxD\_DAT1 53
- MDIO10 82 SD/MMC/MSxD\_DAT0 53
- MDIO05 75 SDPWR1xD\_WP# 53
- MDIO08 88 SD/MMCCMD\_MSBS\_xDWE# 53
- MDIO19 83 xD\_ALE 53
- MDIO18 85 xD\_CLE 53
- MDIO02 78 xD\_CE# 53
- MDIO03 77 SDWP#xDRB# 53
- MDIO00 80 SD/MMCCD#\_xD CD0# 53
- MDIO01 79 MSCD#xD CD1# 53
- MDIO09 84 SD/MMC/MSCLK\_xDRE# 53
- MDIO04 76 SD/MS/MMCxD\_PWR0 53
- MDIO06 74 TPC26T 1 T5201
- MDIO07 73 GND



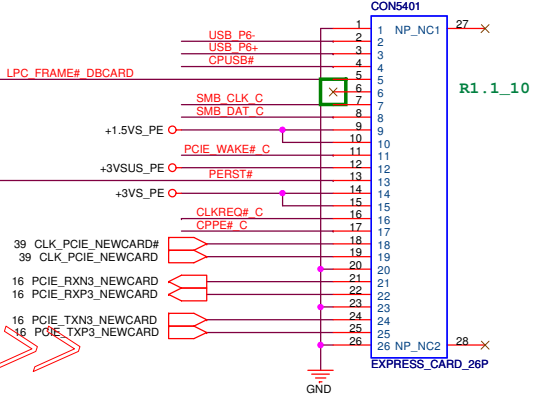
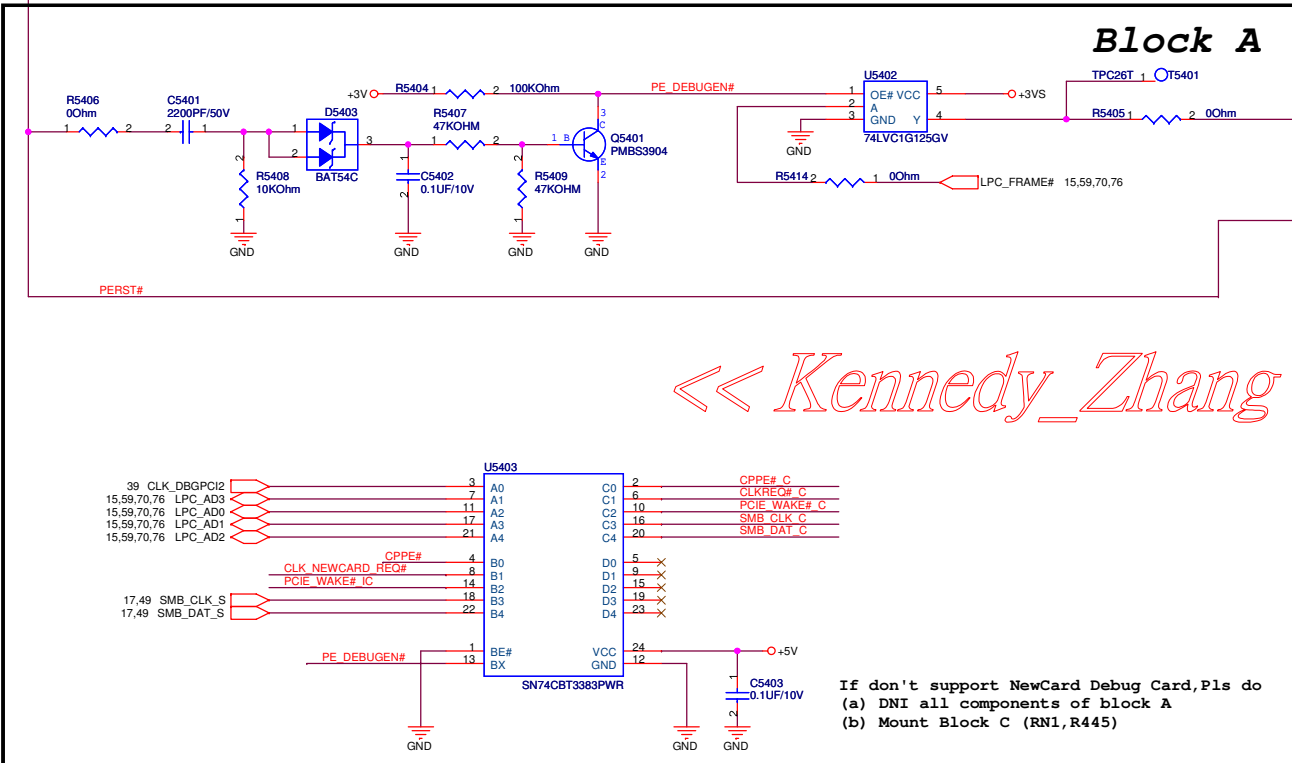
<< Kennedy\_Zhang >>



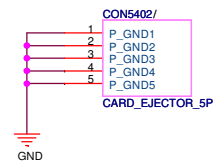


!! ExpressCard Standard 1.0:  
Change Pin7 from RESERVED to SMBCLK  
Change Pin8 from SMBCLK to SMBDATA  
Change Pin9 from SMBDATA to +1.5V

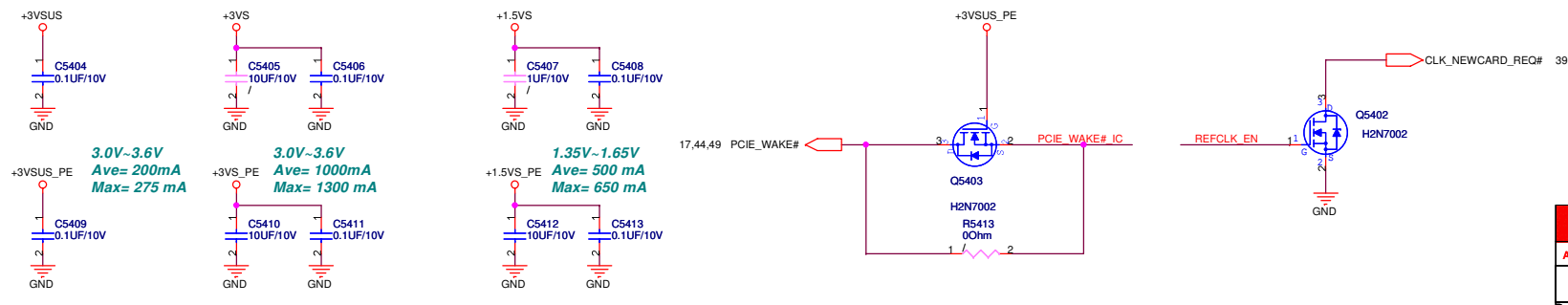
NewCard Header



NewCard Ejecter



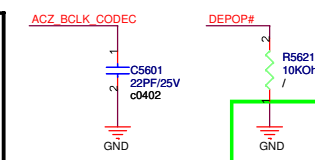
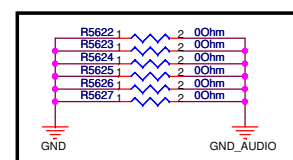
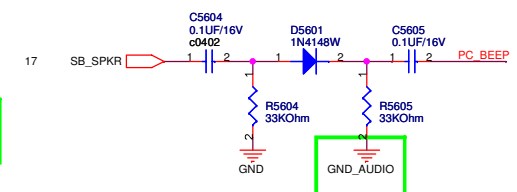
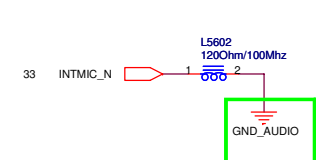
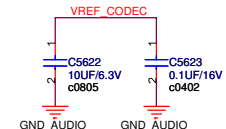
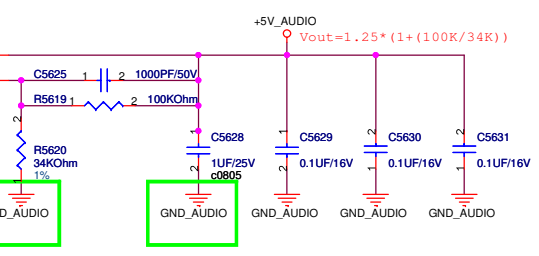
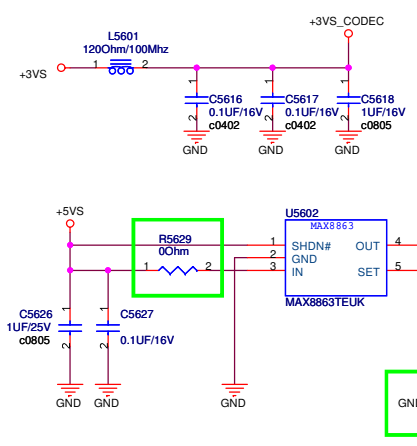
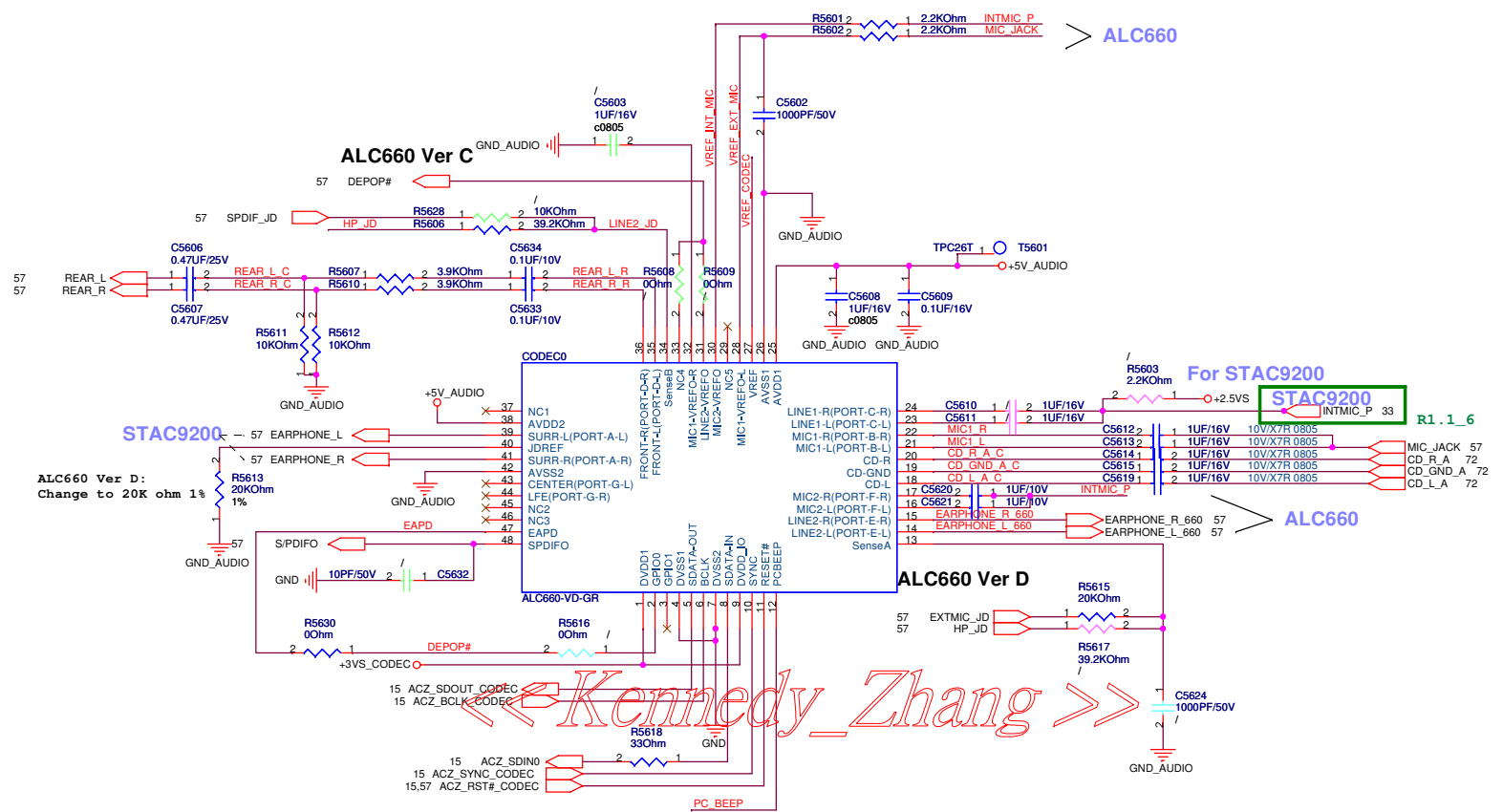
If don't support NewCard Debug Card, PLS do  
(a) DNI all components of block A  
(b) Mount Block C (RN1,R445)



<< Kennedy\_Zhang >>

<Variant Name>

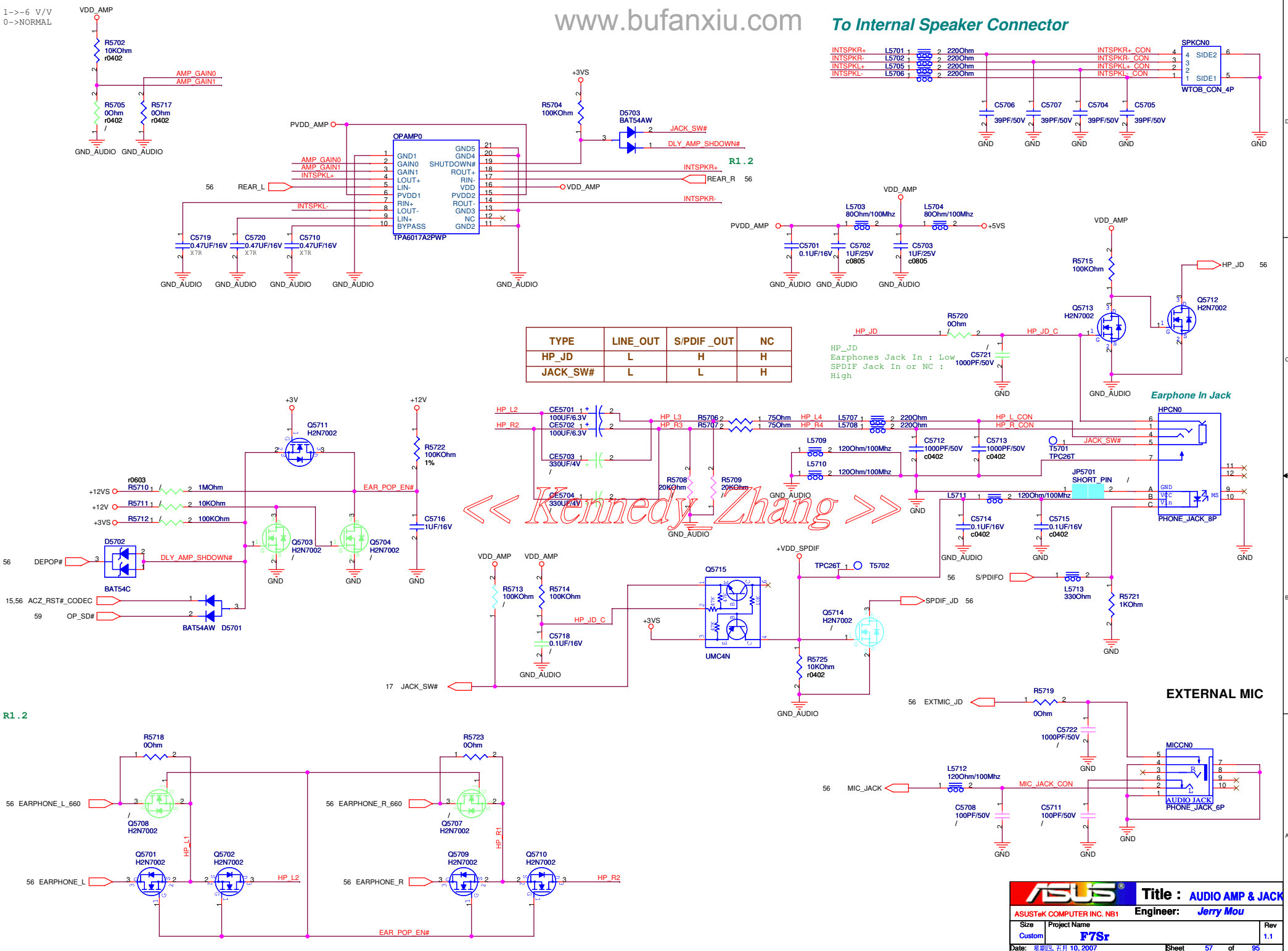
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ASUSTeK COMPUTER INC		Engineer: Jerry Mou	
Size	Project Name		Rev
Custom	F7Sr		1.1
Date: 星期五, 五月 10, 2007		Sheet 55 of 95	



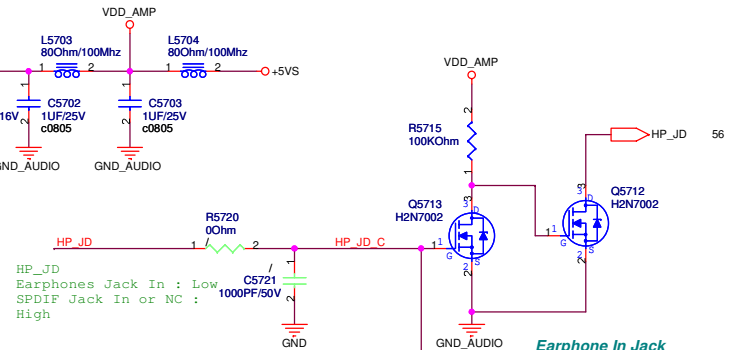
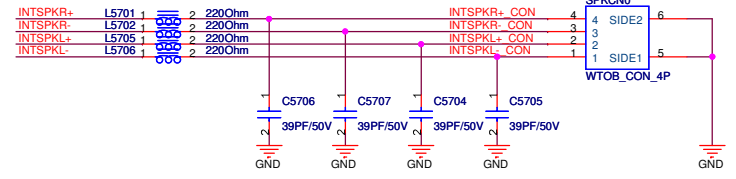
<b>ASUS</b>		<b>Title : CODEC-ALC660</b>	
ASUSTeK COMPUTER INC. N81		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	<b>F7Sr</b>	1.1	
Date: 2007.07.10	Sheet	56	of 95



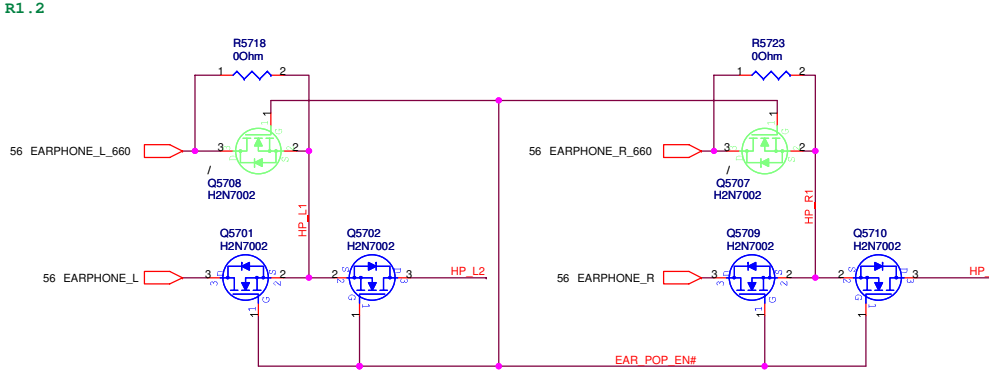
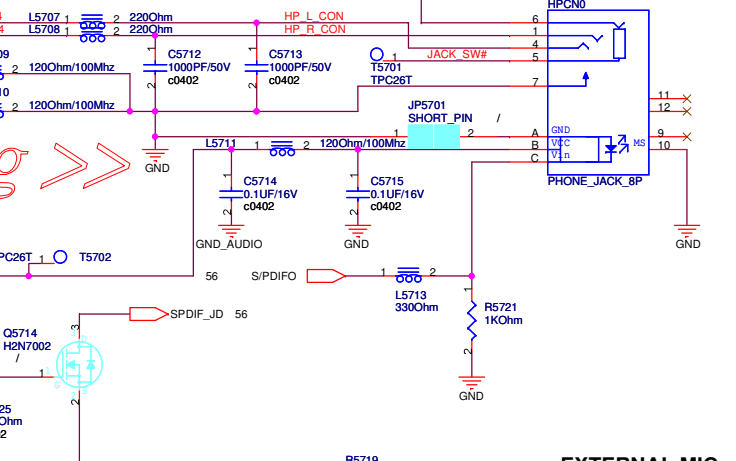
1->-6 V/V  
0->NORMAL

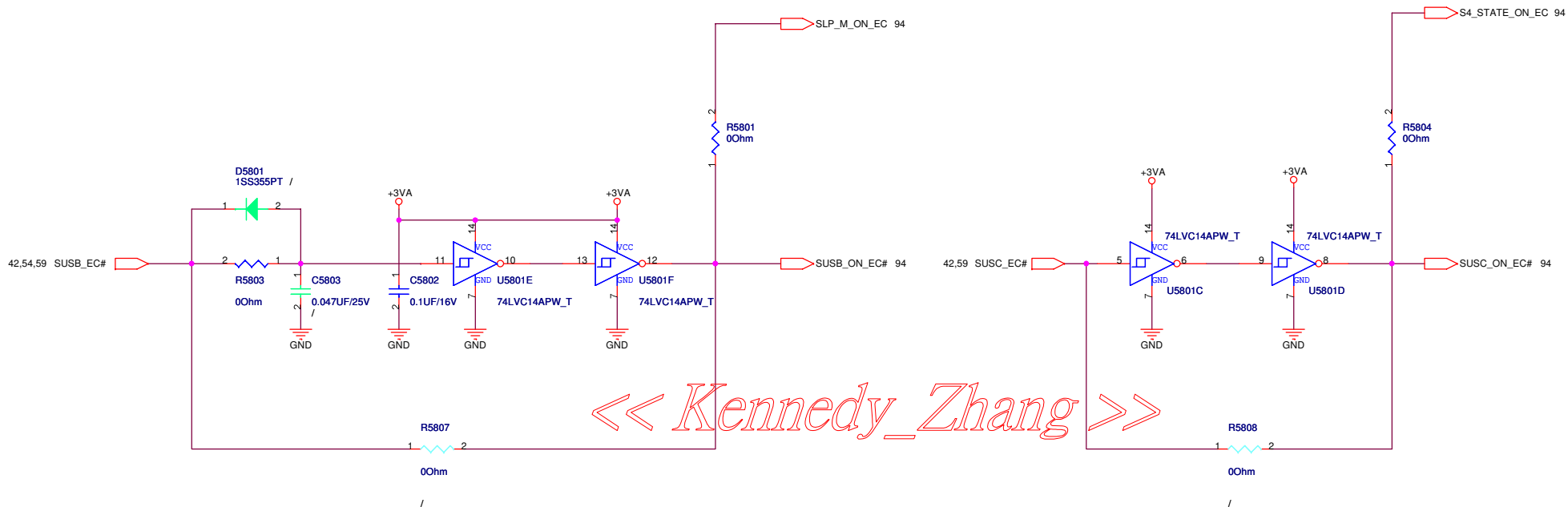


TYPE	LINE_OUT	S/PDIF_OUT	NC
HP_JD	L	H	H
JACK_SW#	L	L	H

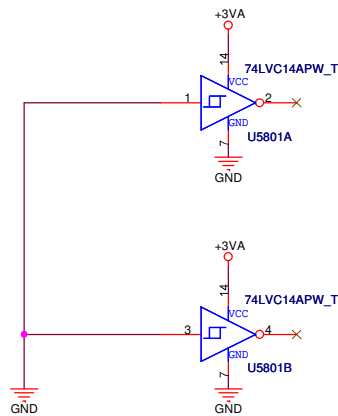


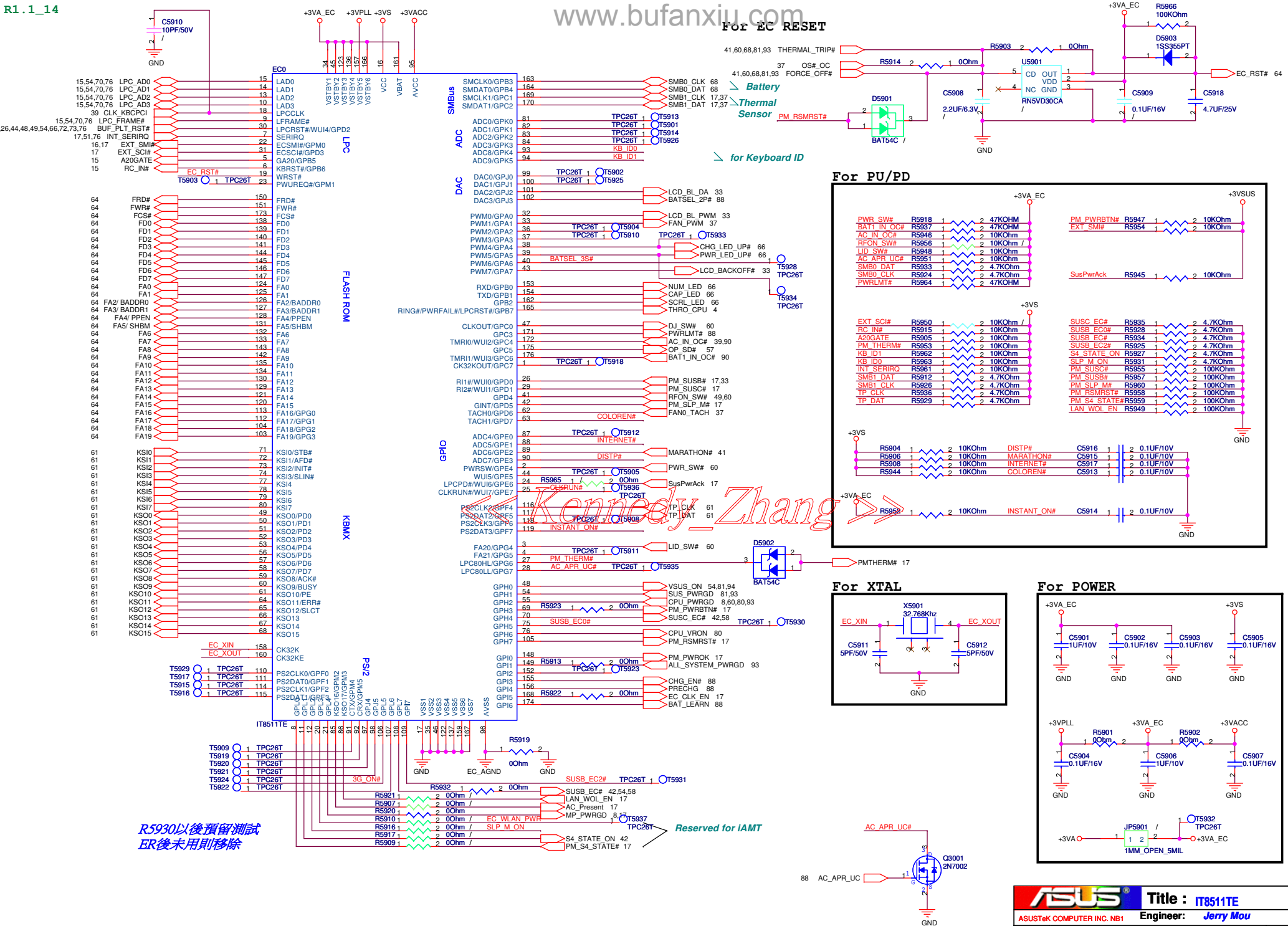
<< Kennedy Zhang >>



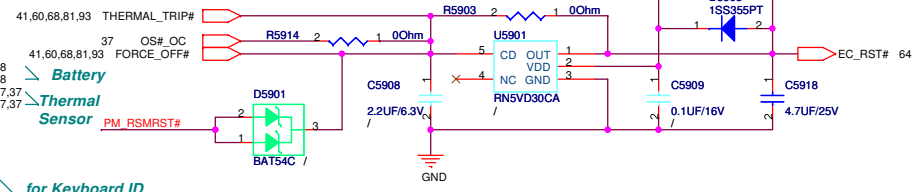


<< Kennedy\_Zhang >>

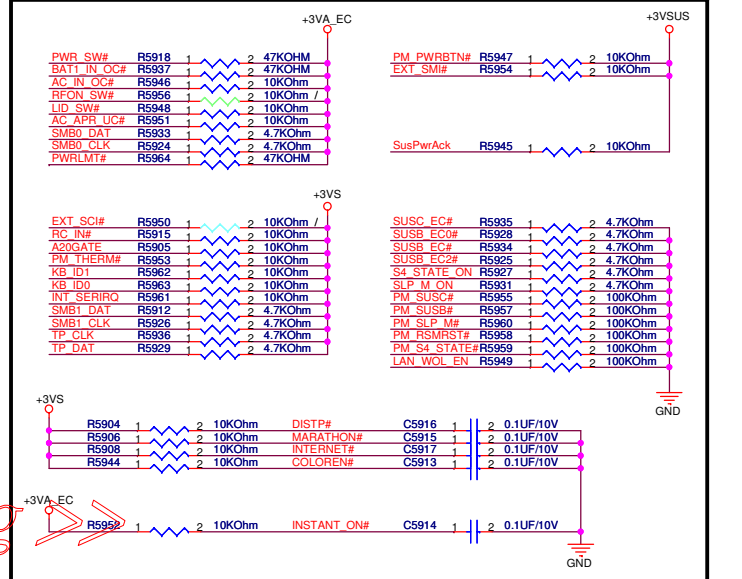




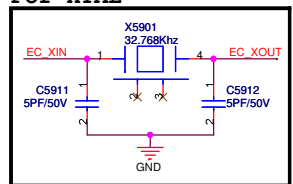
For EC RESET



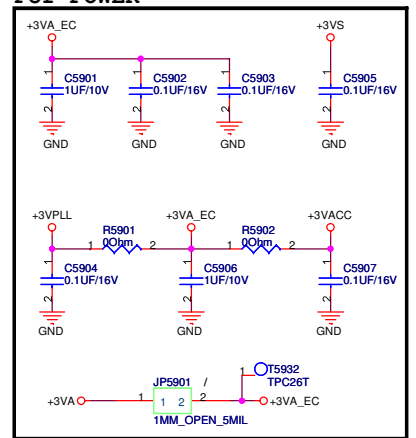
For PU/PD



For XTAL



For POWER

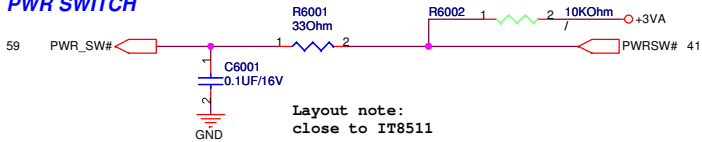


R5930以後預留測試 ER後未用則移除

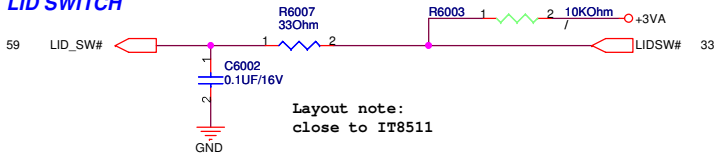
Reserved for iAMT

### For Switch

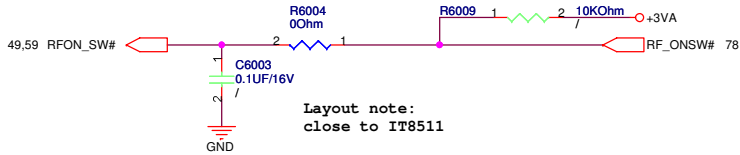
#### PWR SWITCH



#### LID SWITCH



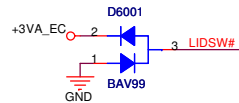
#### RF ON SWITCH



If you don't use Audio DJ function, please use this schematics

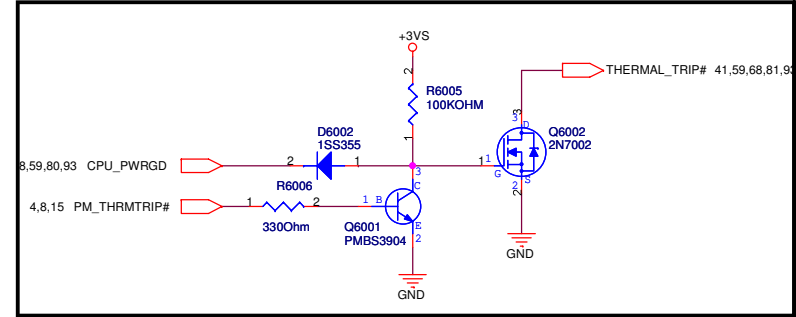
**Note:**

This LID\_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.



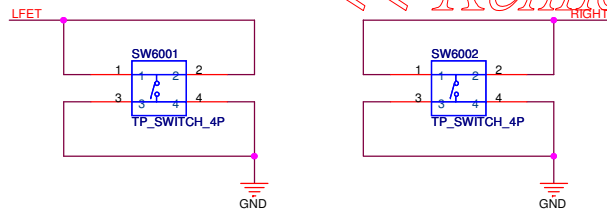
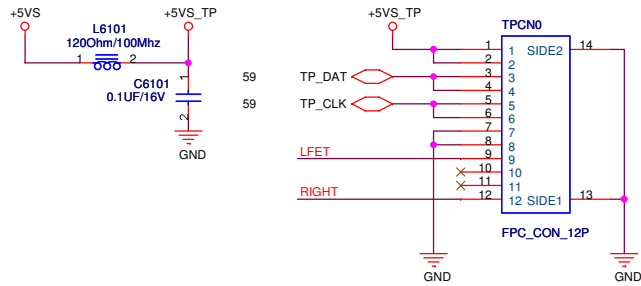
Layout note:  
close to connector

### For Thermal Control Method



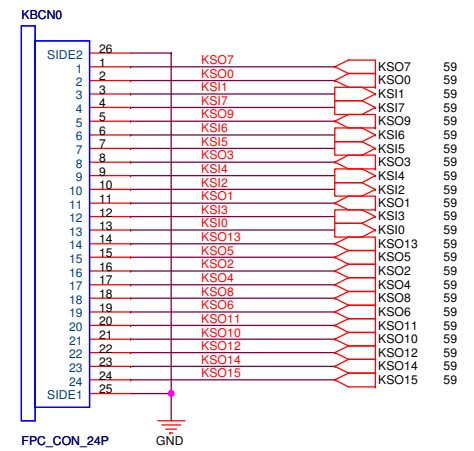
<< Kennedy\_Zhang >>

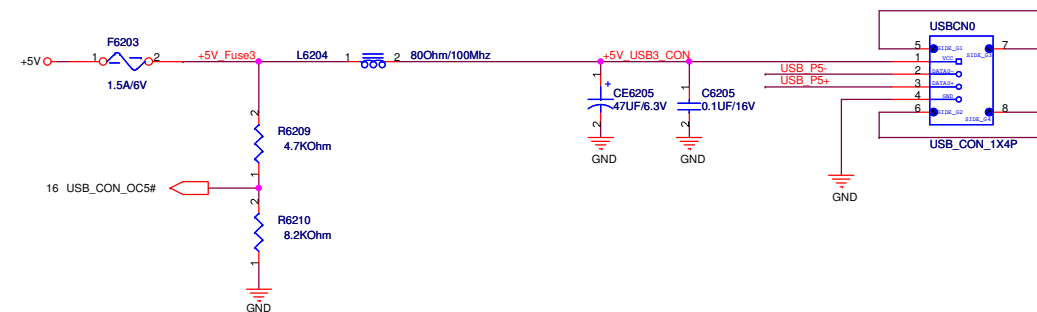
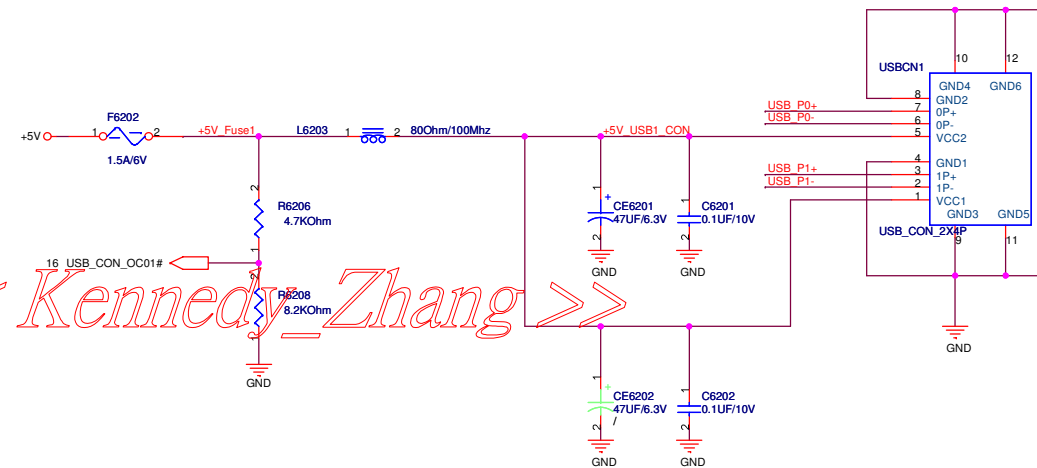
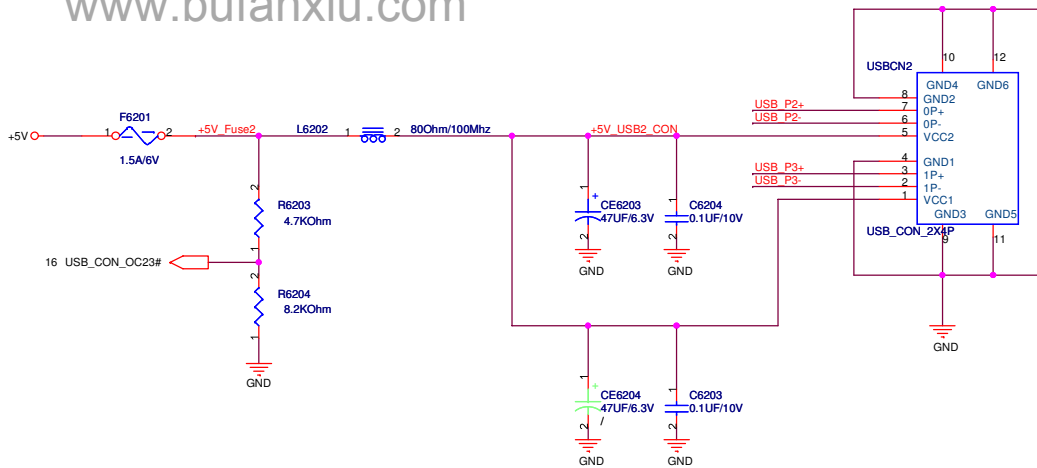
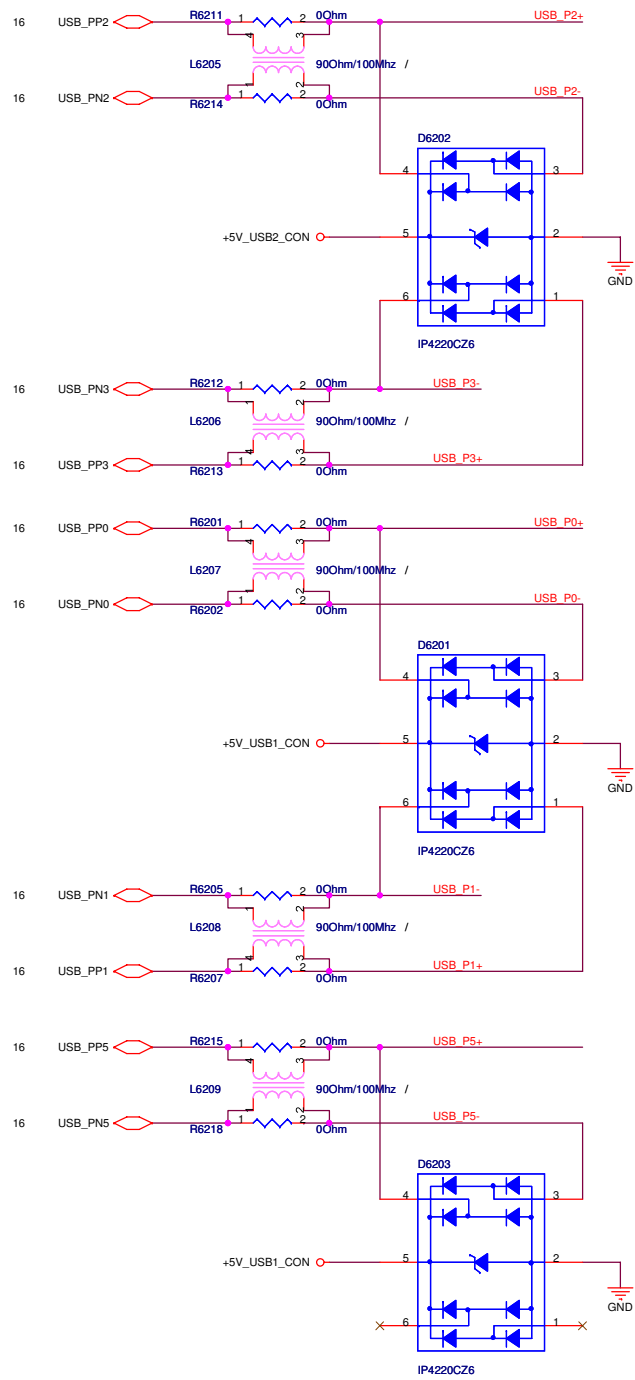
For Touch-Pad



<< Kennedy\_Zhang >>

FOR A7 K/B , Matrix B





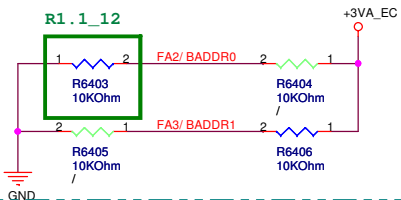
<< Kennedy\_Zhang >>

<< Kennedy\_Zhang >>

**EC Hardware Strapping**

**FA2/ BADDR0 & FA3/ BADDR1**

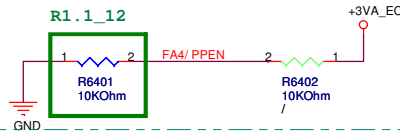
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

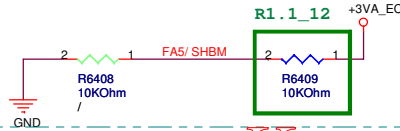
**FA4/ PPEN**

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

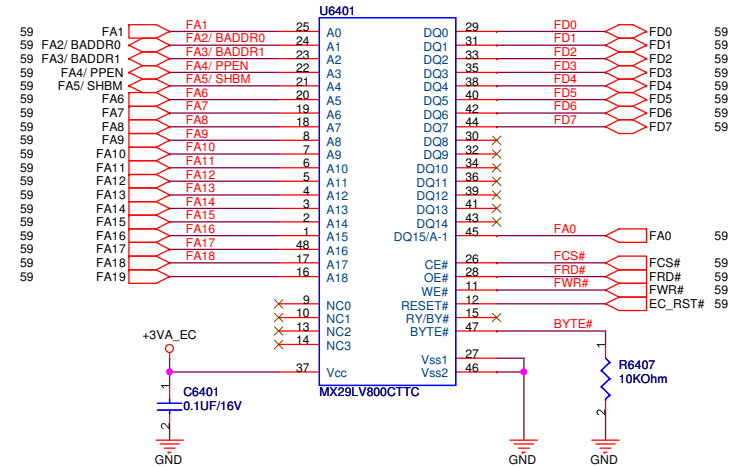


**FA5/ SHBM**

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

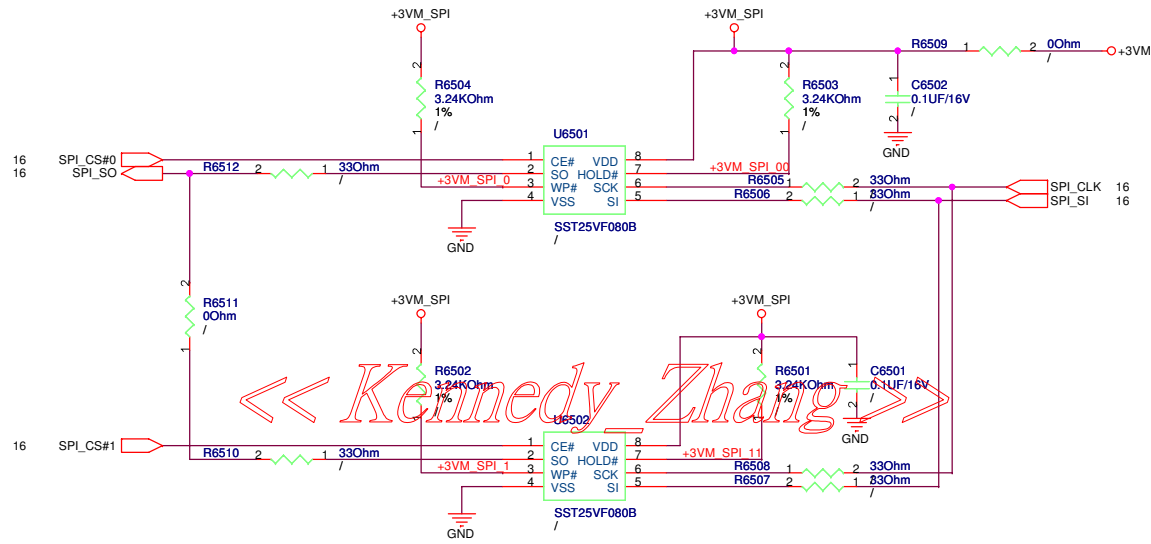


**8M TSOP**

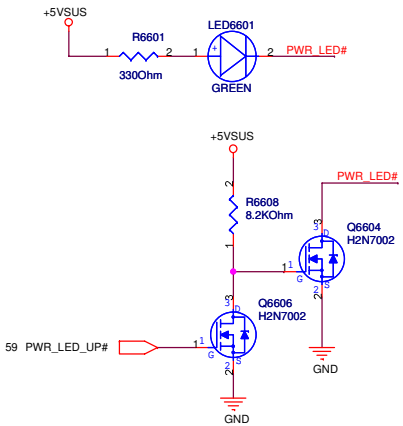


<< Kennedy\_Zhang >>

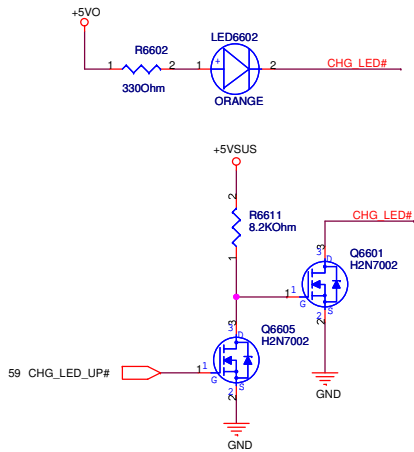




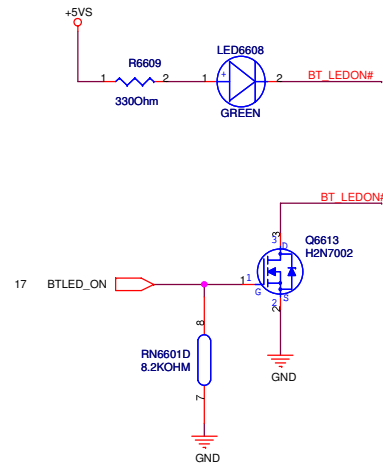
For Power LED



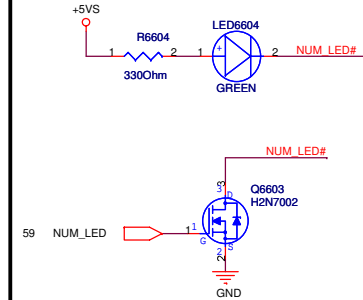
For Battery LED



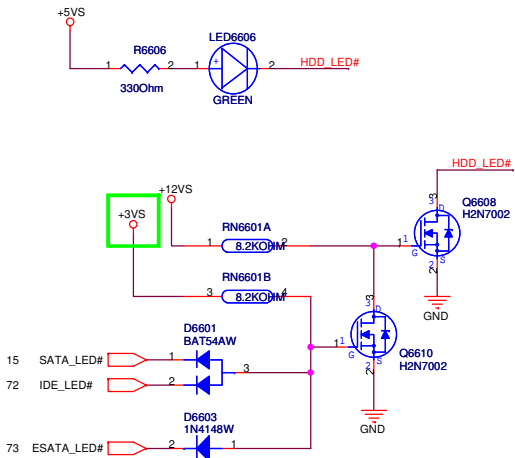
For BT LED



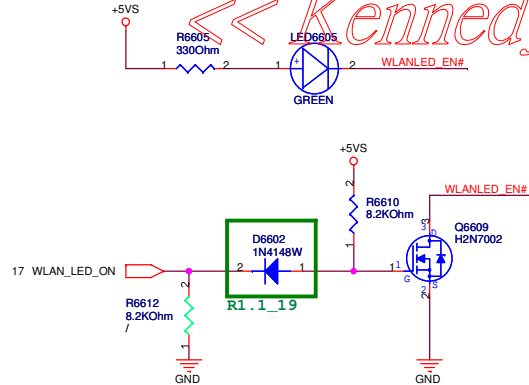
For Number Lock



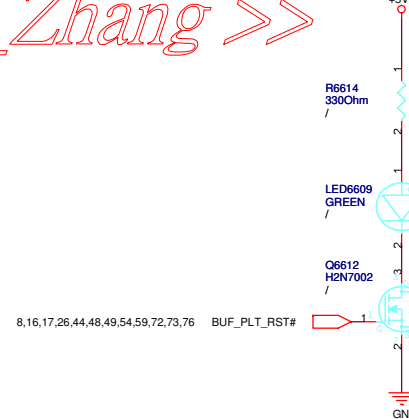
For SATA/IDE LED



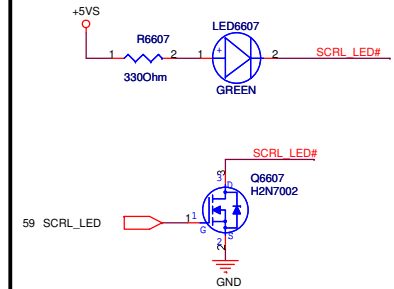
For WireLess LED



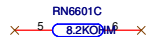
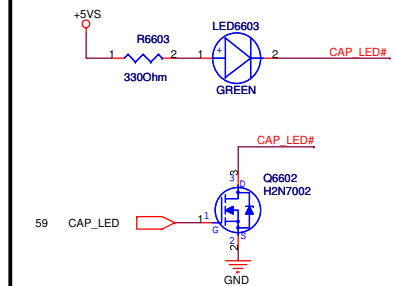
Reserved LED



For Scroll Lock



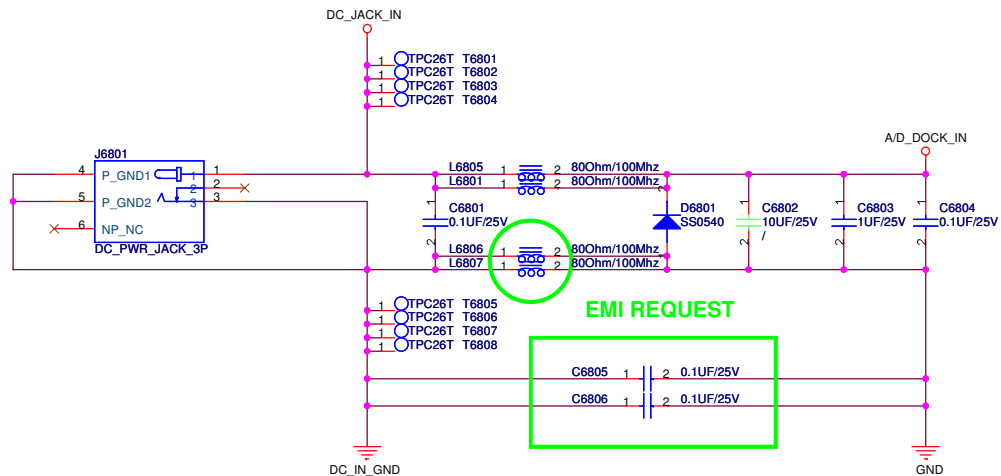
For Caps. Lock



<< Kennedy Zhang >>

<< Kennedy\_Zhang >>

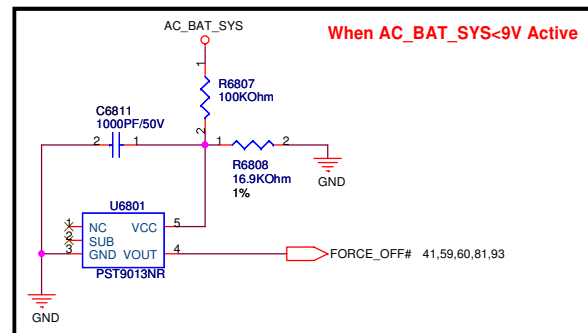
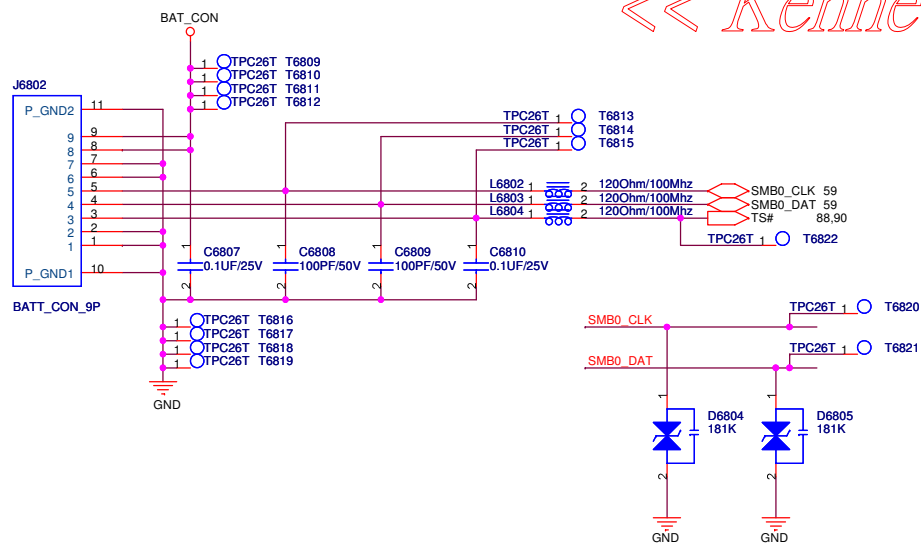
# DC IN



# BAT IN

<< Kennedy\_Zhang >>

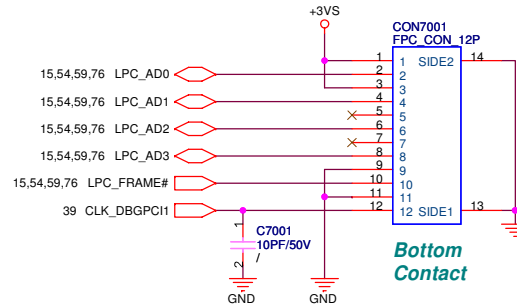
Without Battery & Pull out Adapter



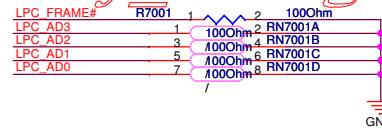
<< Kennedy\_Zhang >>

**For Debug**

If support NewCard Debug Card,  
Pls don't mount all components.



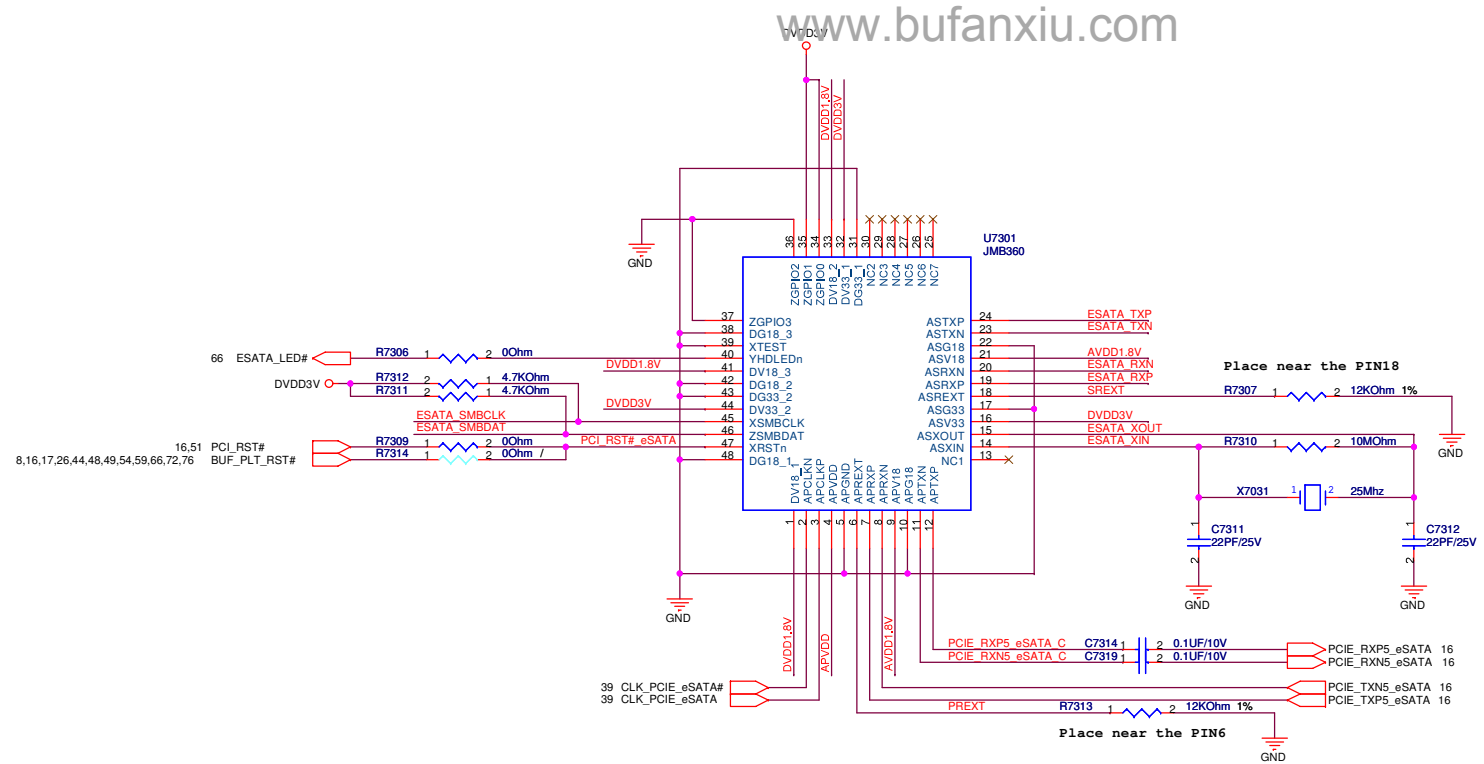
<< Kennedy Zhang >>



<< Kennedy\_Zhang >>

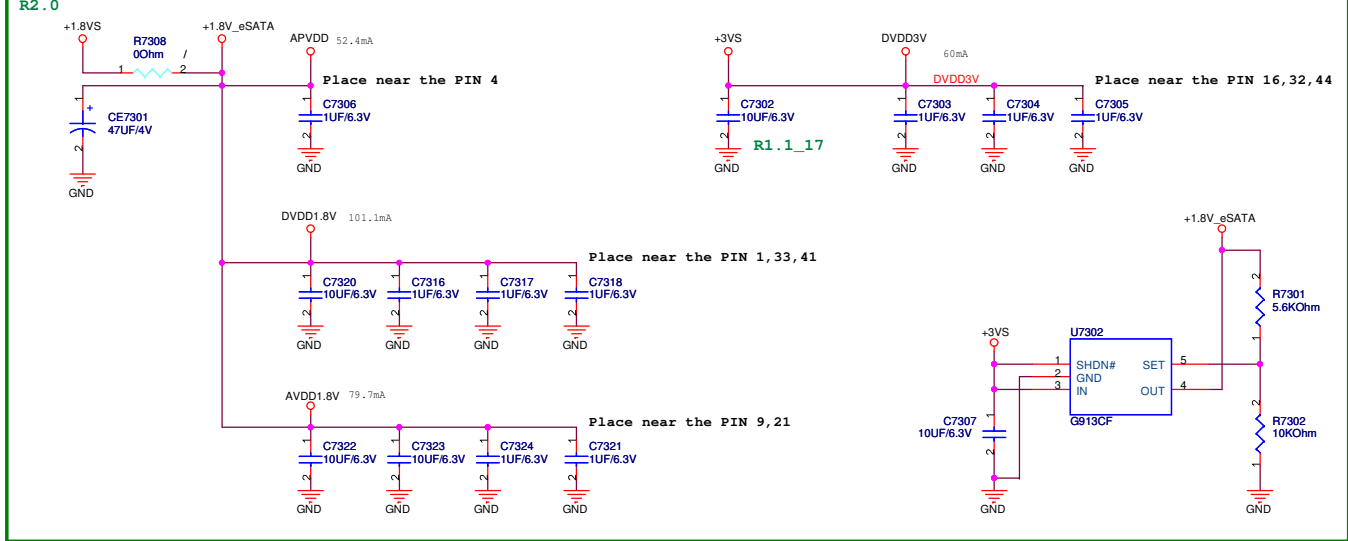




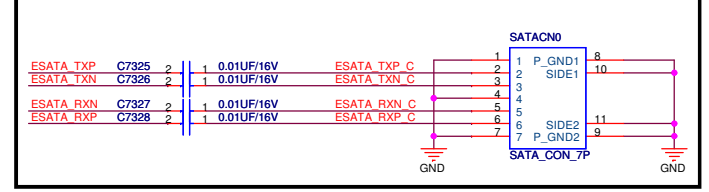


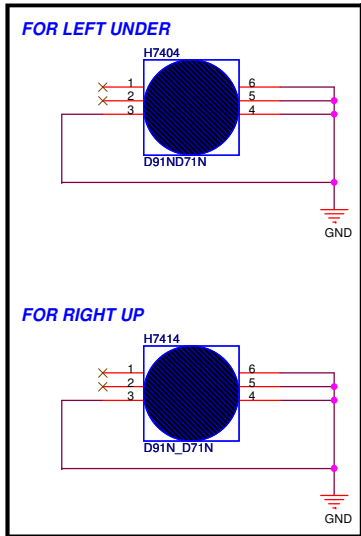
<< Kennedy\_Zhang >>

eSATA Power

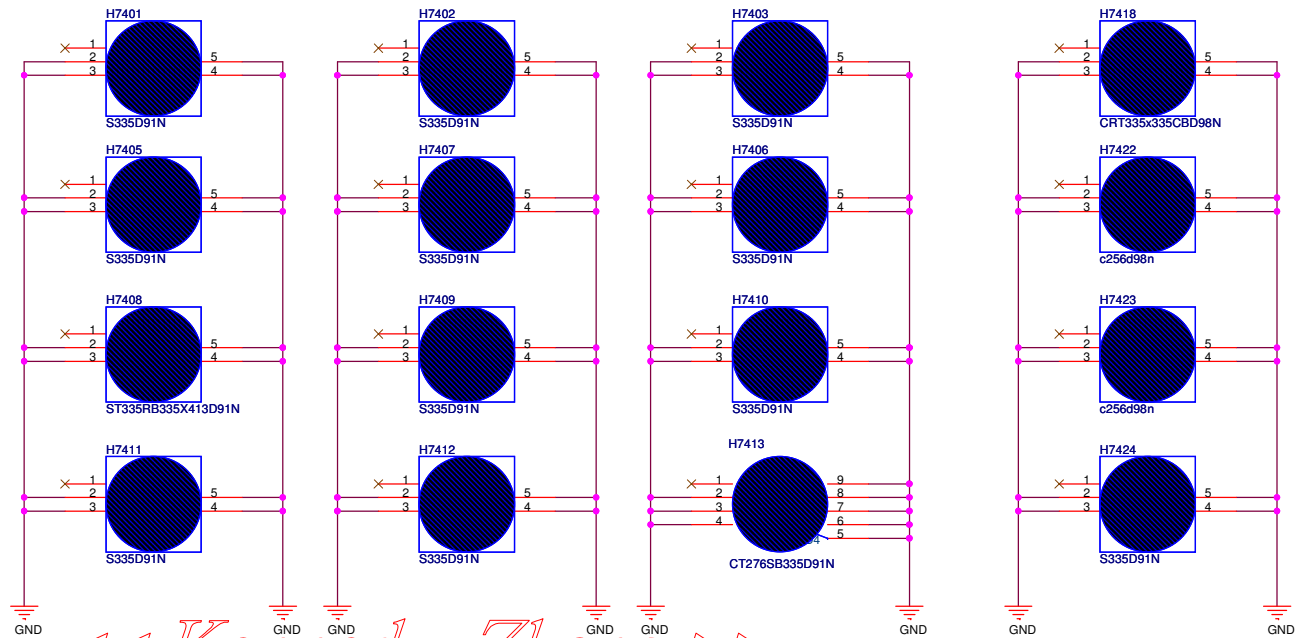


eSATA Connector



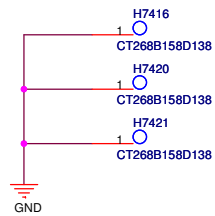


**FOR SCREW HOLE**

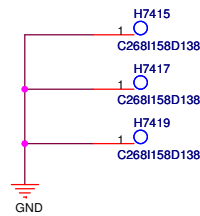


<< Kennedy\_Zhang >>

**FOR CPU**



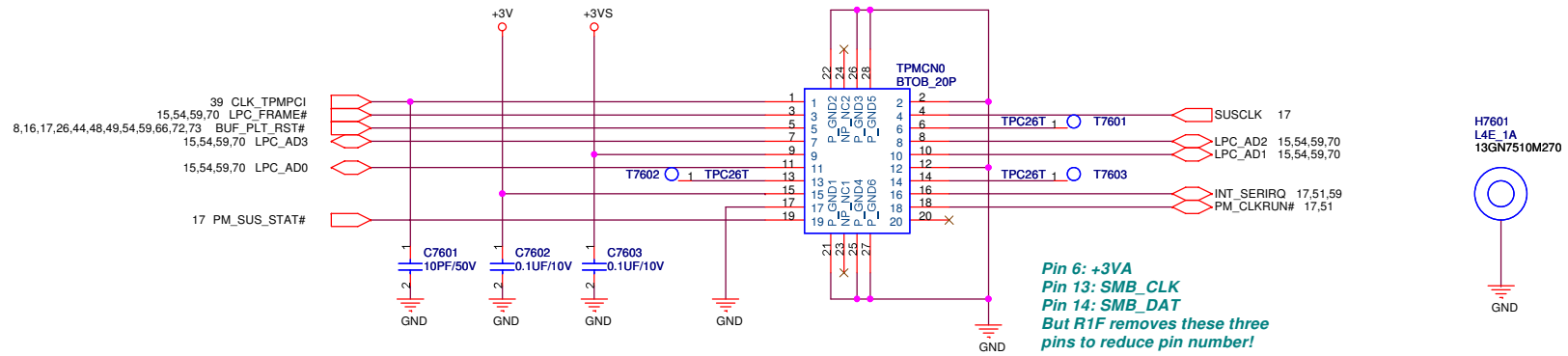
**FOR VGA**



- H7499 CB177D71N
- H7498 CB177D71N
- H7497 CB177D71N


<< Kennedy\_Zhang >>

For TPM module

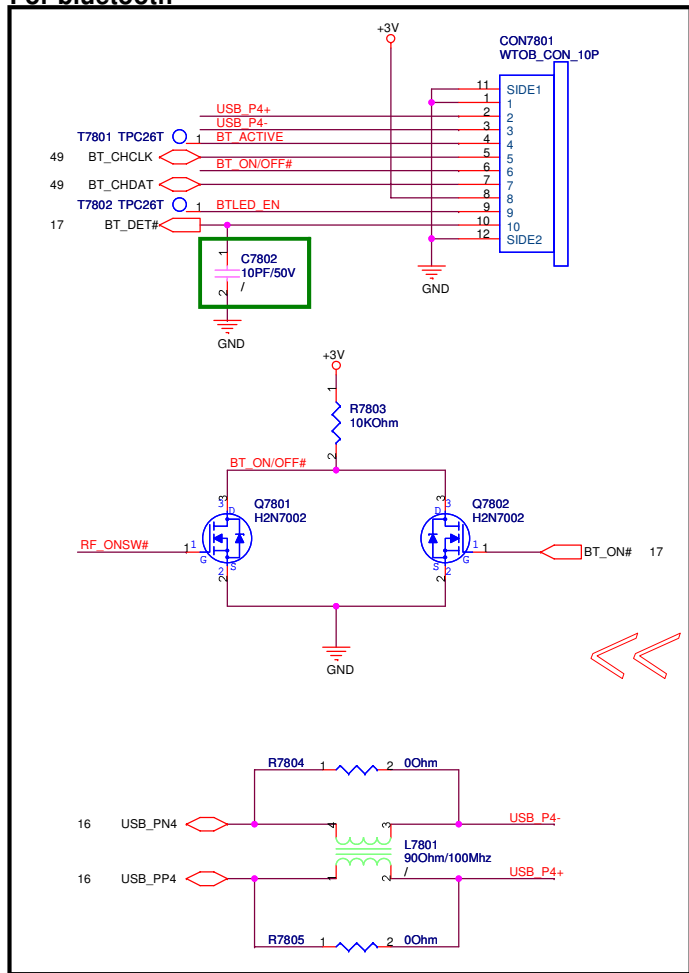


<< Kennedy\_Zhang >>

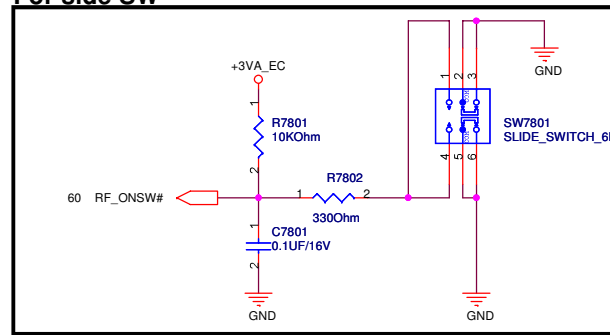
<< Kennedy\_Zhang >>

		<b>Title :</b> SPRING	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Jerry Mou	
Size	Project Name	Rev	
Custom	F7Sr	1.1	
Date: 星期四, 五月 10, 2007		Sheet	77 of 95

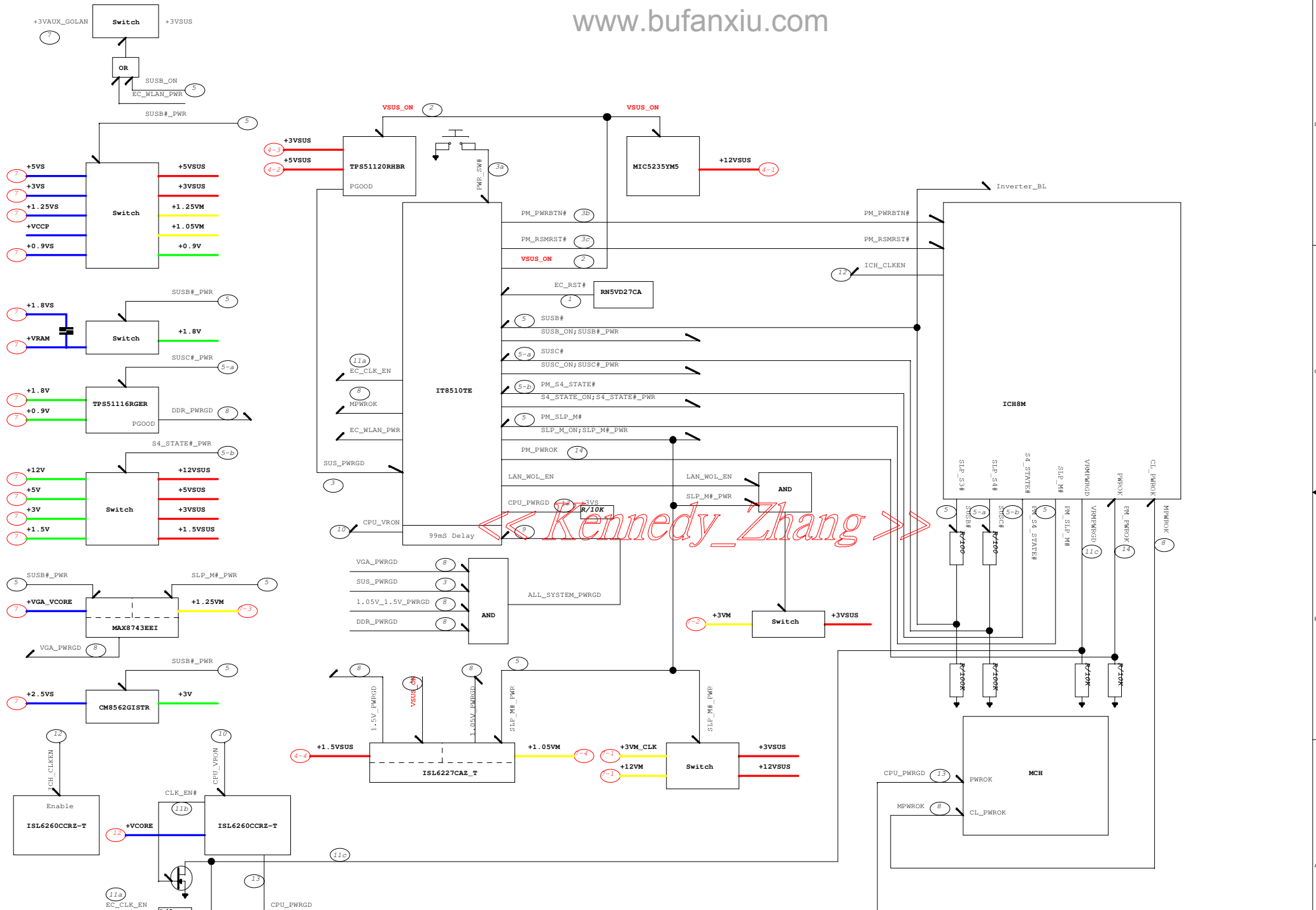
For bluetooth

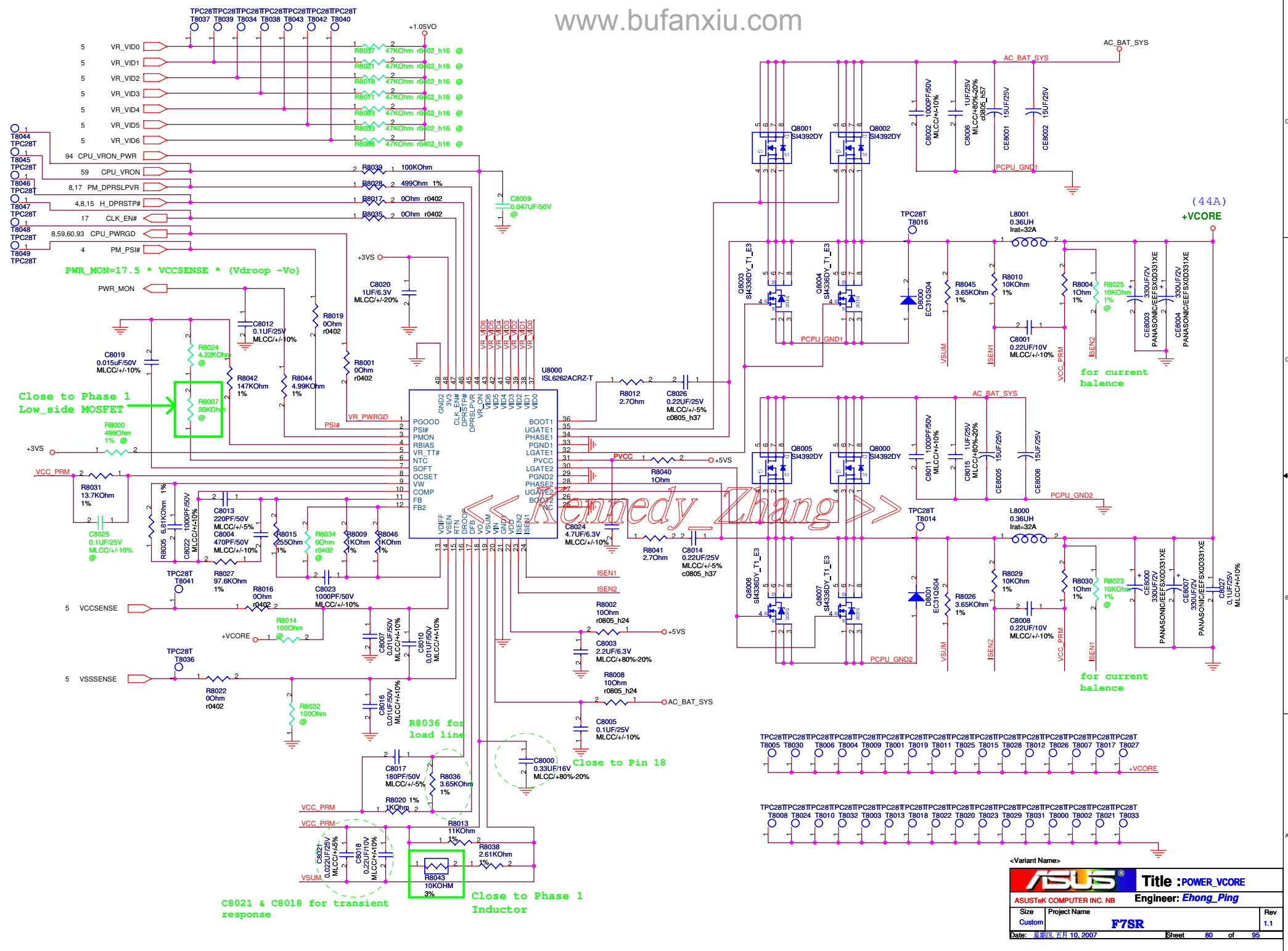


For side SW



<< Kennedy\_Zhang >>





$PWR\_MON = 17.5 * VCCSENSE * (Vdroop - Vc)$

Close to Phase 1 Low\_side MOSFET

VCC\_PRM

VCCSENSE

VSSSENSE

VCC\_PRM

VCC\_PRM

VSUM

C8021 & C8018 for transient response

Close to Phase 1 Inductor

Close to Pin 18

R8036 for load line

(44A)  
+VCORE

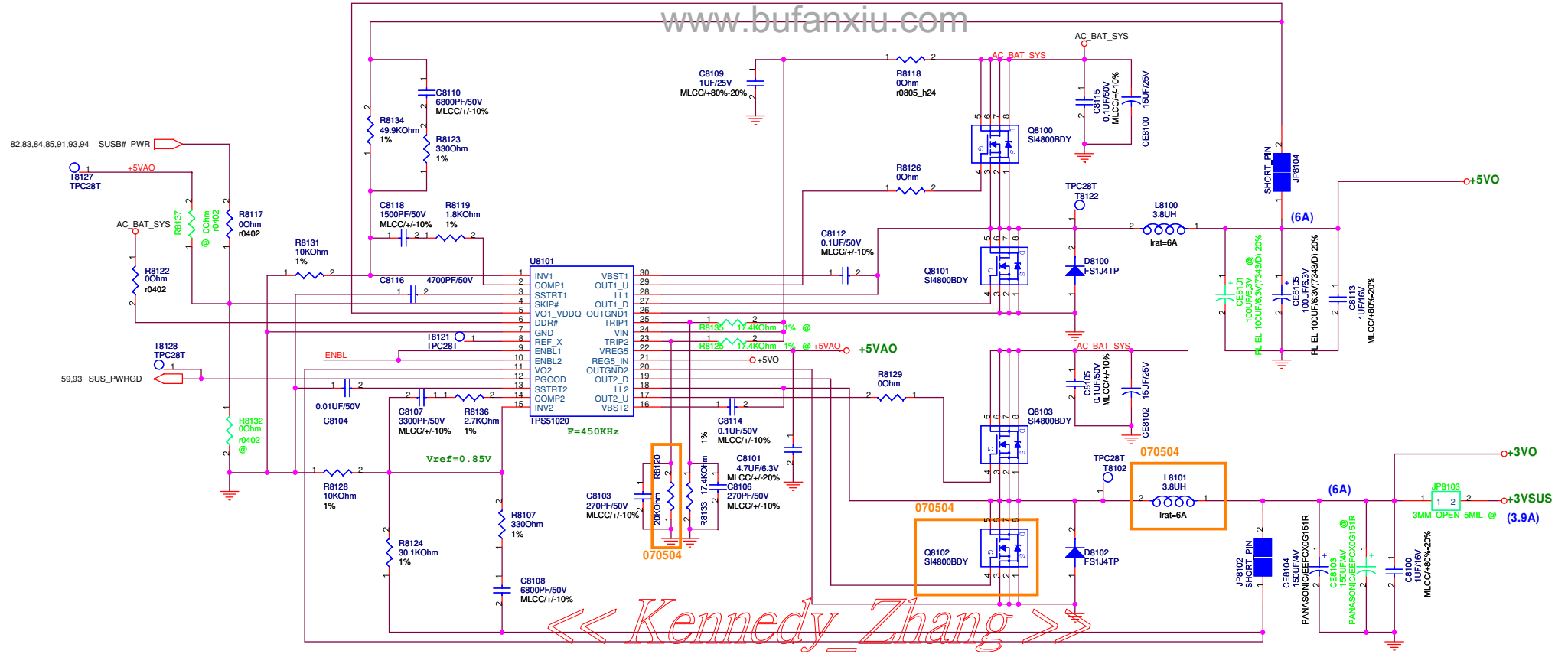
for current balance

for current balance

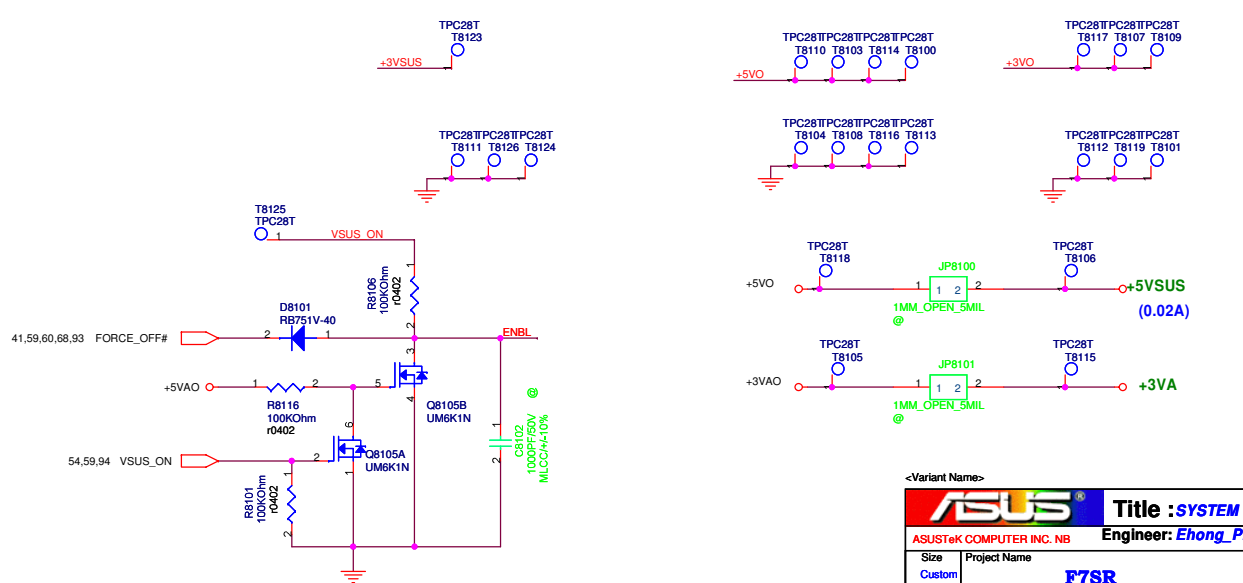
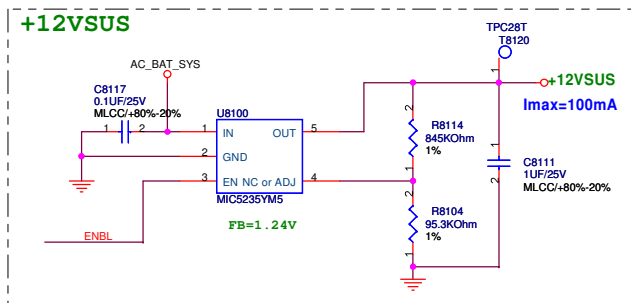
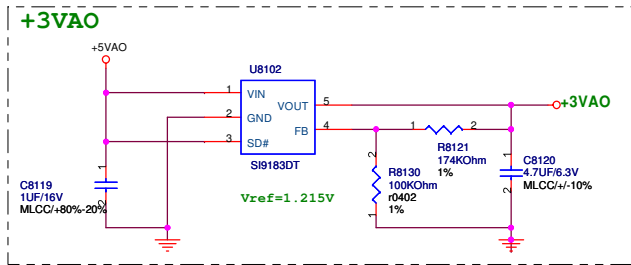
<Variant Name>

		Title :POWER_VCORE	
ASUSTek COMPUTER INC. NB		Engineer: Hong_Ping	
Size	Project Name	Rev	
Custom	F7SR	1.1	
Date: 星期四, 五月 10, 2007	Sheet	80	of 95



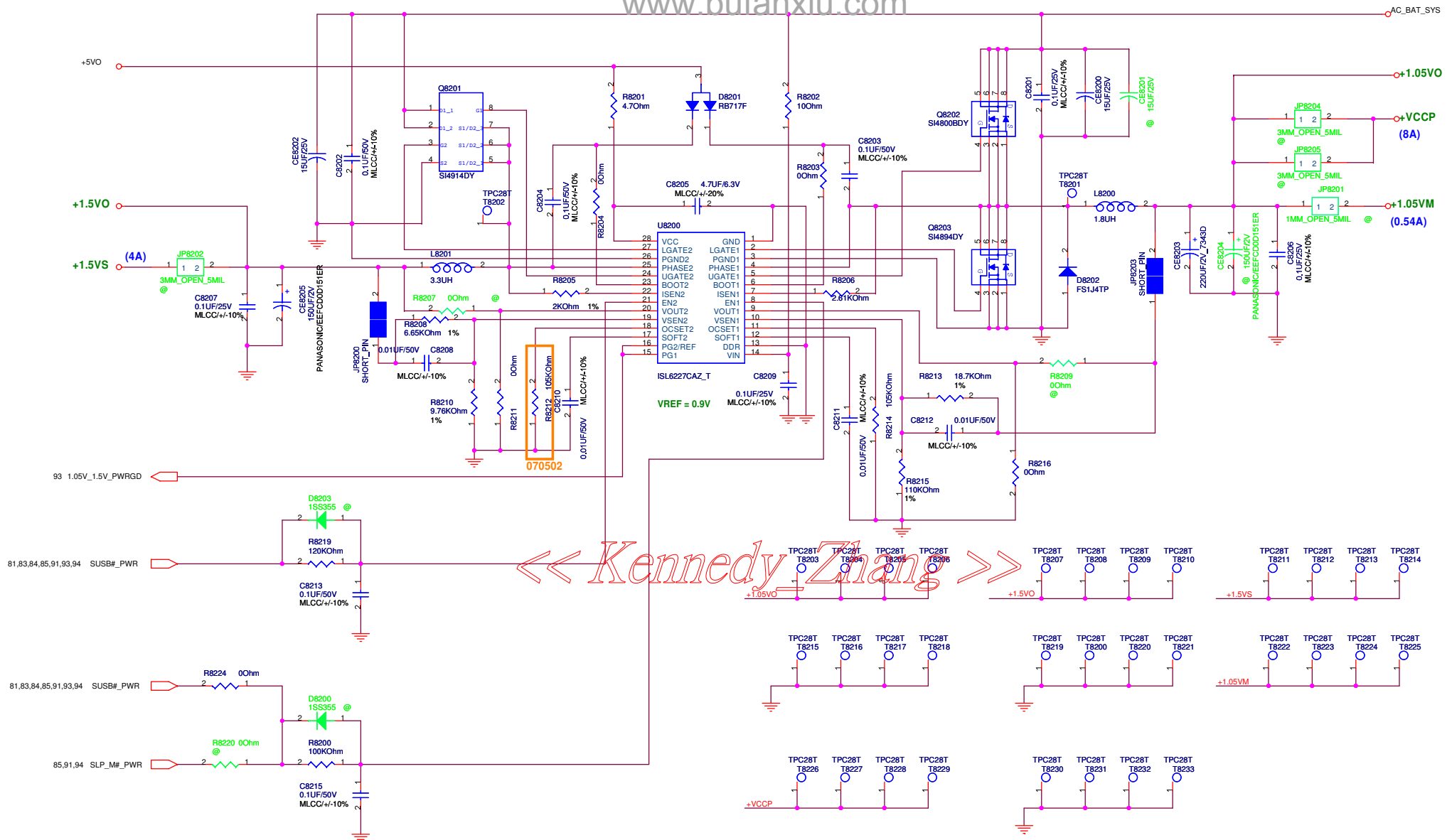


« Kennedy\_Zhang »

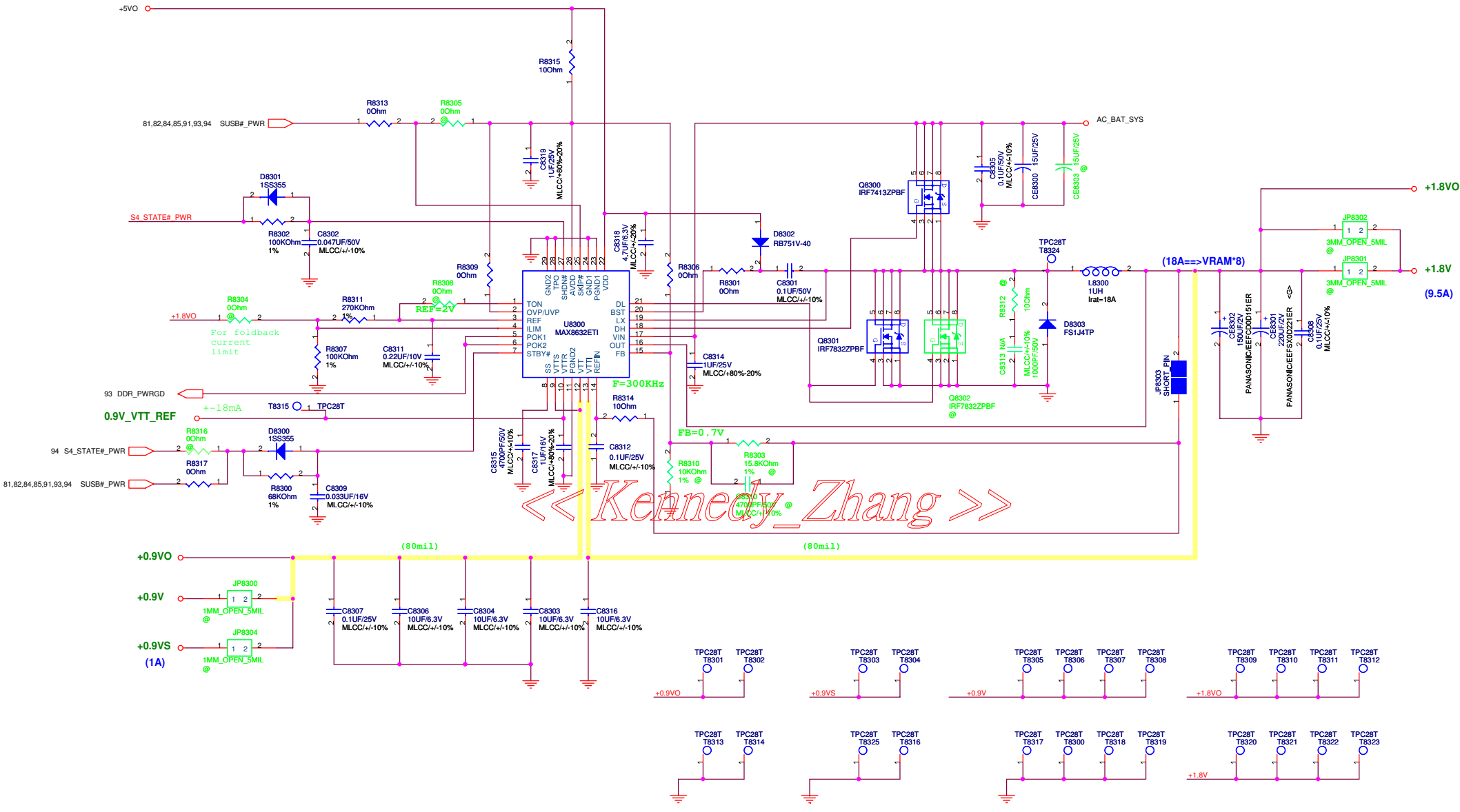


<Variant Name>

<b>ASUS</b>		Title : <b>SYSTEM</b>	
ASUSTek COMPUTER INC. NB		Engineer: <b>Ehong_Ping</b>	
Size	Project Name	Rev	
Custom	<b>F7SR</b>	1.1	
Date:	日期: 五月 10, 2007	Sheet	81 of 95



« Kennedy Zhang »

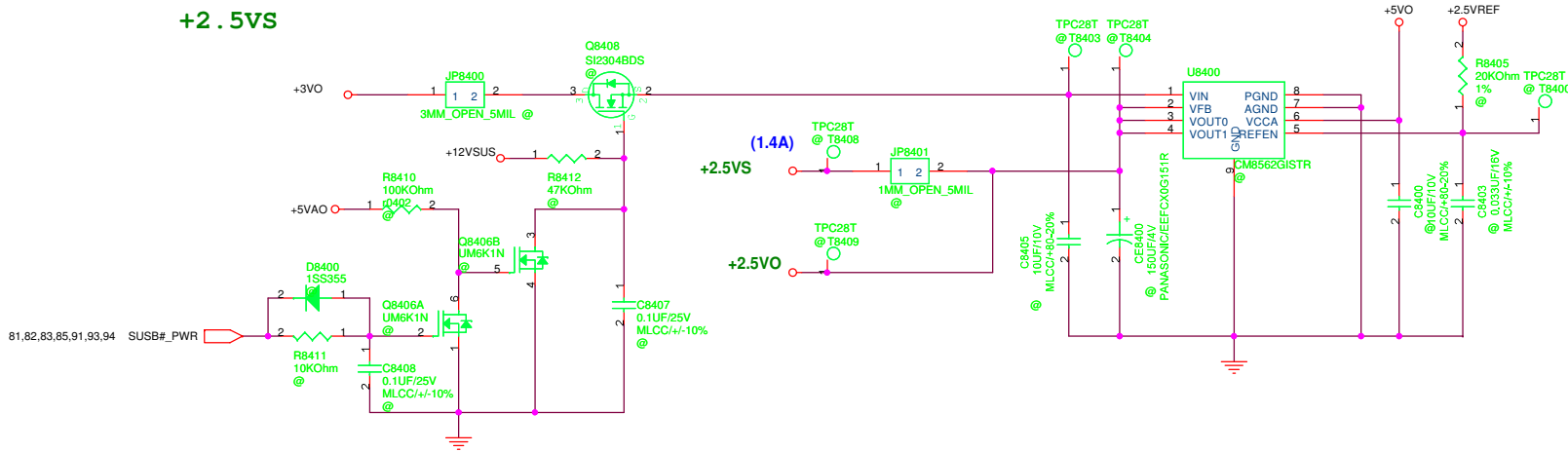


<< Kennedy\_Zhang >>

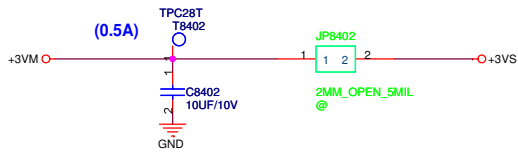
<Variant Name>

<b>ASUS</b>		<b>Title : POWER_I/O_DDR &amp; VTT</b>	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name	Rev	
Custom	F7SR	1.1	
Date: 华硕, 五月 10, 2007	Sheet 83	of 95	

+2.5VS

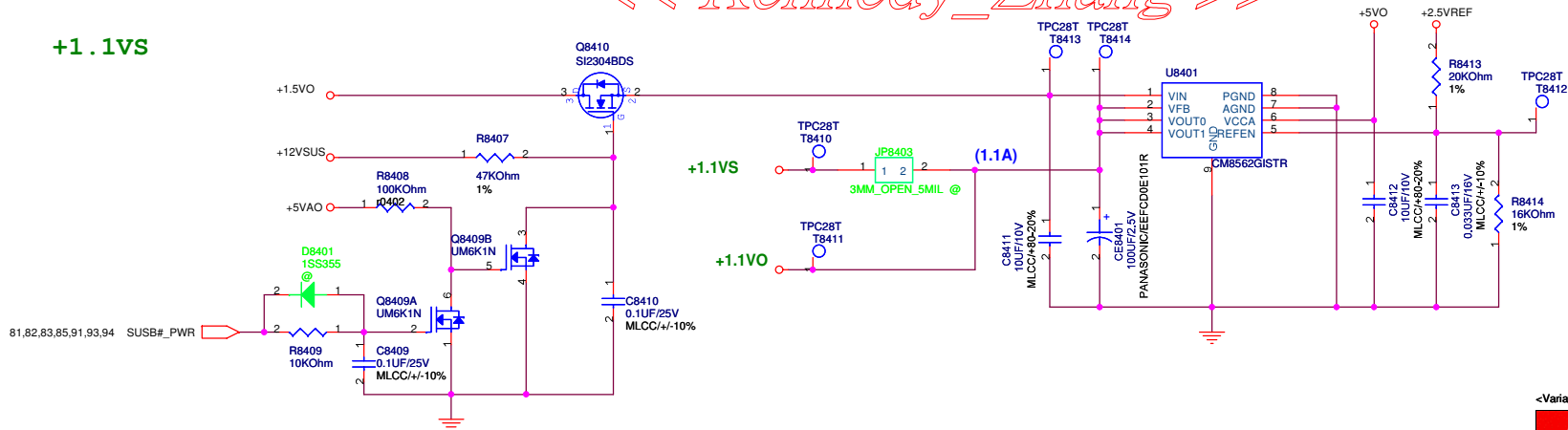


+3VM



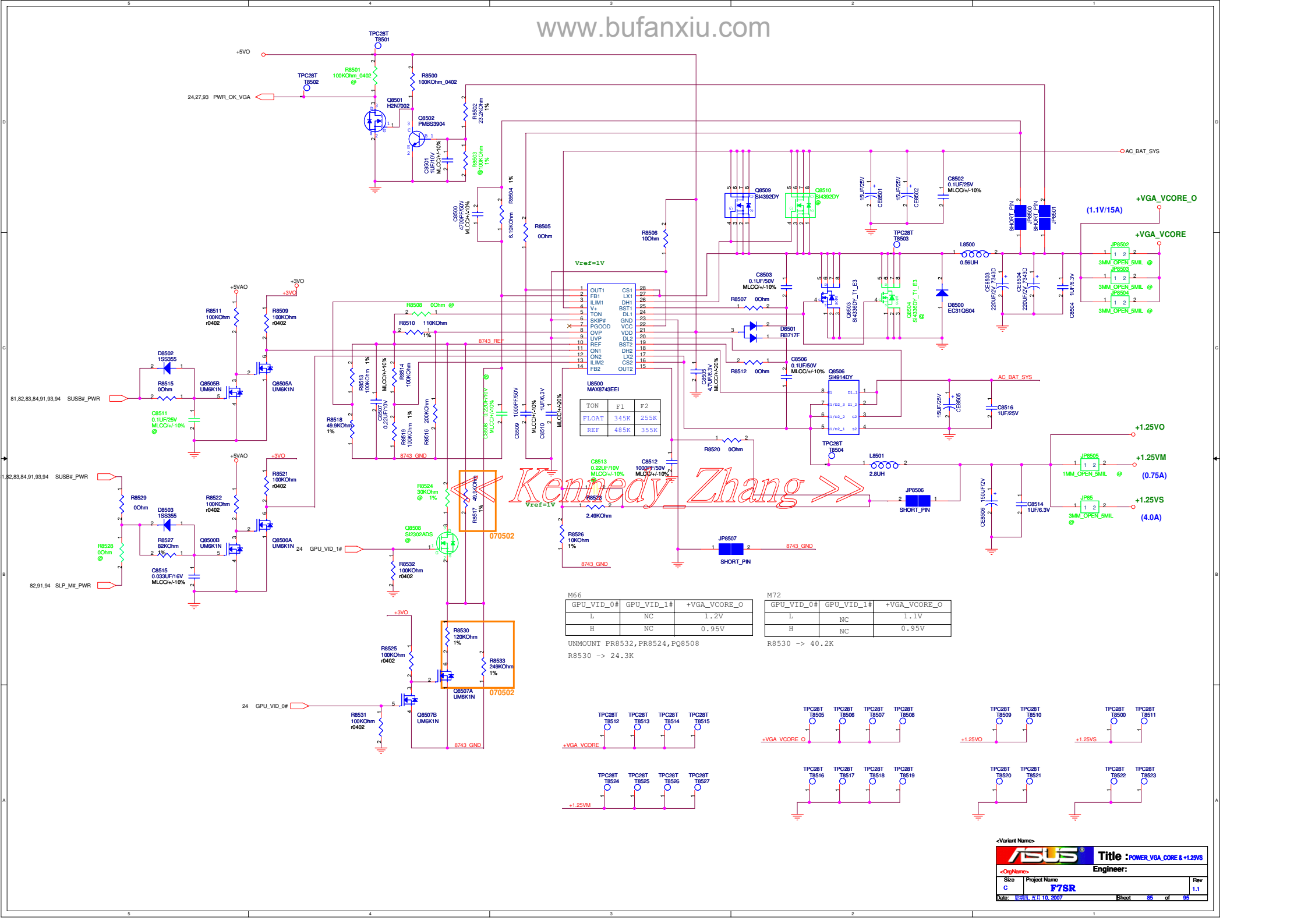
<< Kennedy\_Zhang >>

+1.1VS



<Variant Name>

<b>ASUS</b>		<b>Title</b> POWER_I/O_+3VM & +2.5VS
<b>Engineer:</b>		
<b>Size</b>	<b>Project Name</b>	<b>Rev</b>
Custom	<b>F7SR</b>	1.1
<b>Date:</b> 星期四, 五月 10, 2007		<b>Sheet</b> 84 <b>of</b> 95



Vref=1V

OUT1	CS1	27
FB1	LK1	28
ILM1	DH1	29
V+	BST1	30
TON	DL1	31
SKIP#	GND	32
PGOOD	VCC	33
OV	VDD	34
UVP	DL2	35
REF	BST2	36
ON1	DH2	37
ON2	LX2	38
ILM2	CS2	39
FB2	OUT2	40

U8500 MAX8743EEI

TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

M66

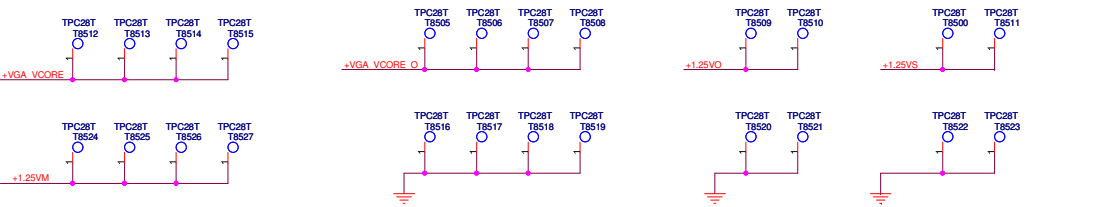
GPU_VID_0#	GPU_VID_1#	+VGA_VCORE_O
L	NC	1.2V
H	NC	0.95V

UNMOUNT PR8532, PR8524, PQ8508  
R8530 -> 24.3K

M72


GPU_VID_0#	GPU_VID_1#	+VGA_VCORE_O
L	NC	1.1V
H	NC	0.95V

R8530 -> 40.2K




<< Kennedy\_Zhang >>

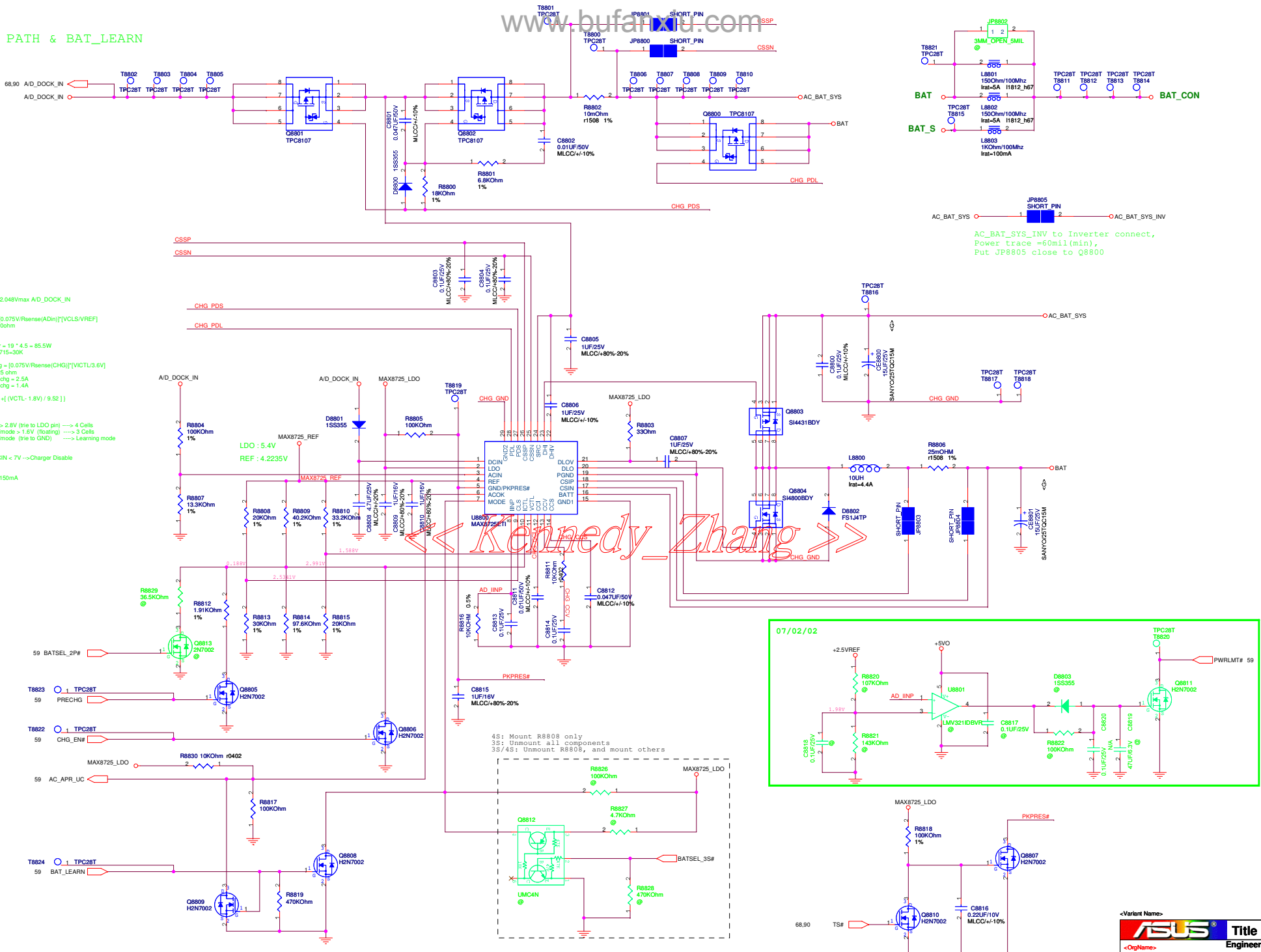
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		<b>Title :</b> N/A
<OrgName>		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>F7SR</b>	1.1
Date: 星期四, 五月 10, 2007		Sheet 86 of 95

<< Kennedy\_Zhang >>

<Variant Name>		
 <b>Title : N/A</b>		
<OrgName> <b>Engineer:</b>		
Size C	Project Name <b>F7SR</b>	Rev 1.1
Date: 五月 10, 2007		Sheet 87 of 95

POWER PATH & BAT\_LEARN



● AC\_IN Threshold 2.045Vmax A/D\_DOCK\_IN > 17.44V active

Adapter lin(max) = [0.075V/Rsense(ADin)]\*[VCLS/VREF]  
 Rsense(ADin) = 0.010ohm  
 VCLS = 2.5341V  
 => lin(max) = 4.5A  
 => Constant Power = 19 \* 4.5 = 85.5W  
 => R5710 = 20K, R5715 = 30K

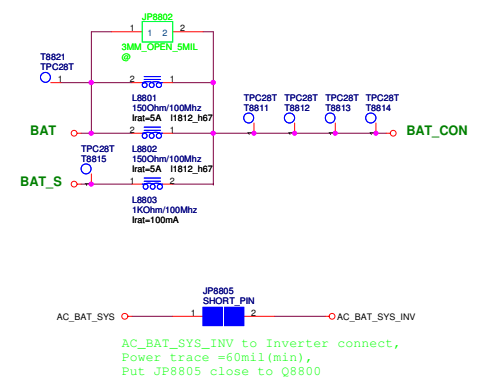
Charge Current Ichg = [0.075V/Rsense(CHG)]\*[VICTL/3.6V]  
 Rsense(CHG) = 0.025ohm  
 VICTL = 3V => Ichg = 2.5A  
 VICTL = 1.88V => Ichg = 1.4A

Vbatt = Cell \* [Vref + (VCTL - 1.8V) / 9.52]  
 VCTL = 1.588V  
 => Vbatt = 4.2V

Mode pin : Vmode > 2.6V (tie to LDO pin) => 4 Cells  
 2.0 > Vmode > 1.6V (floating) => 3 Cells  
 0.8 > Vmode > 0V => Learning mode

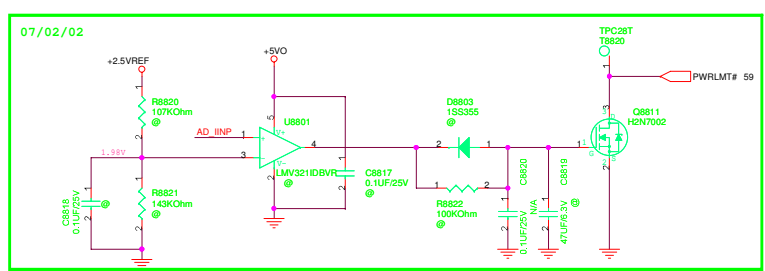
VICTL = 0.8V or DCIN < 7V => Charger Disable

Preccharge current = 150mA



AC\_BAT\_SYS\_INV to Inverter connect,  
 Power trace = 60mil(min),  
 Put JP8805 close to Q8800

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4S: Mount R8808 only  
 3S: Unmount all components  
 3S/4S: Unmount R8808, and mount others

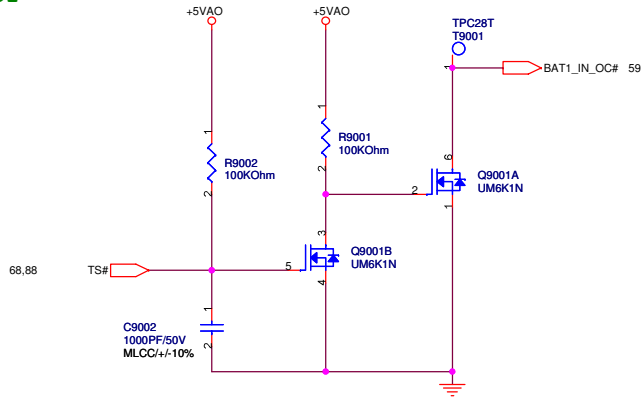
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<OrgName>		F7SR		Engineer:	
Size	Project Name	Rev			
Custom		1.1			
Date: 星期日, 五月 10, 2007	Sheet	88	of 95		



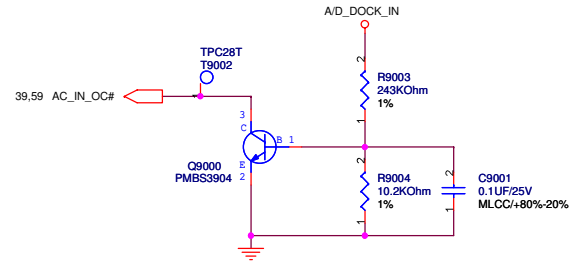
<< Kennedy\_Zhang >>

<Variant Name>		
		Title : N/A
<OrgName>		Engineer:
Size Custom	Project Name <b>F7SR</b>	Rev 1.1
Date: 星期四, 五月 10, 2007		Sheet 89 of 95

### BATTERY IN DETECT

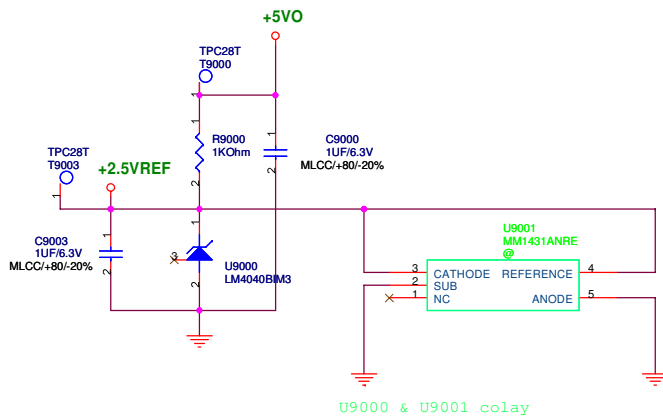


### ADAPTER IN DETECT



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### +2.5VREF

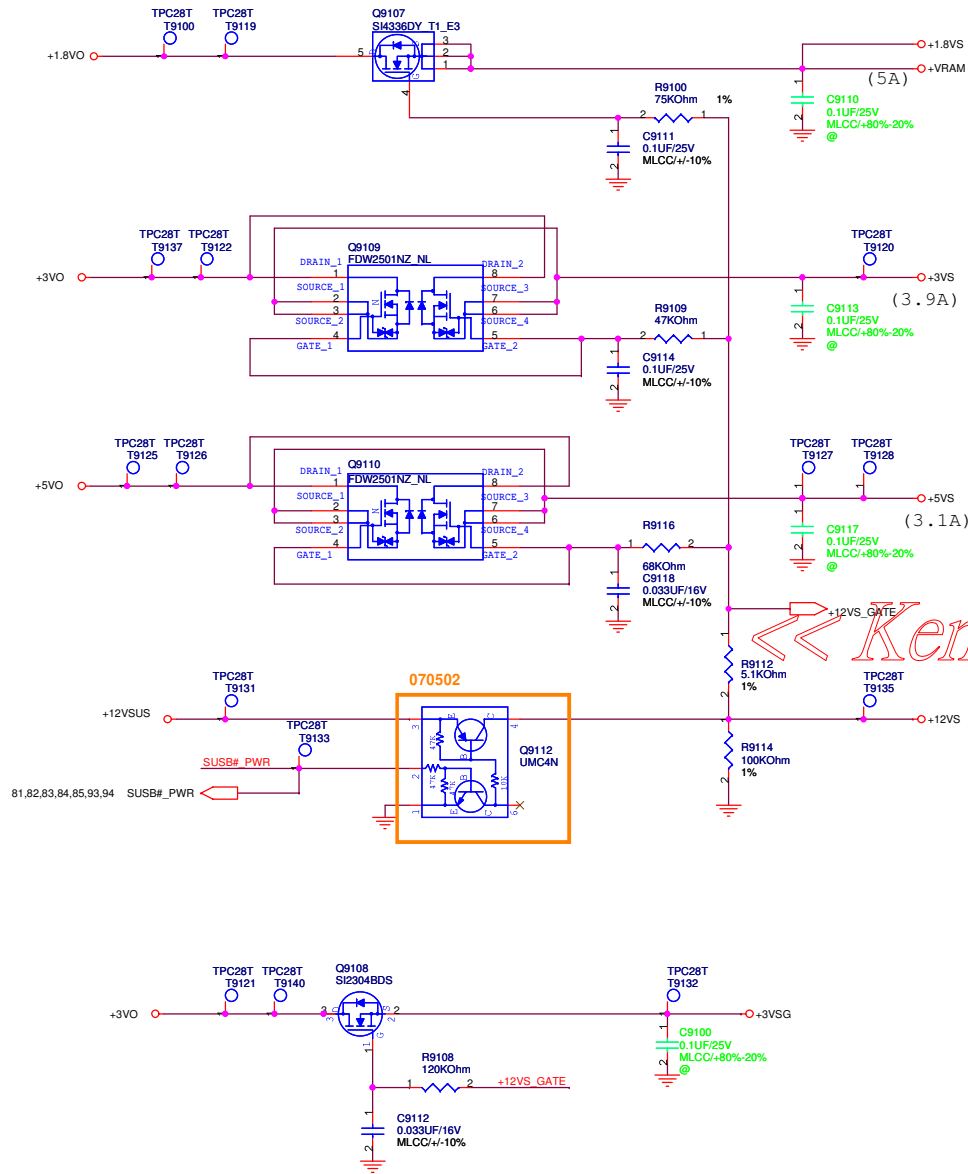


U9000 & U9001 colay

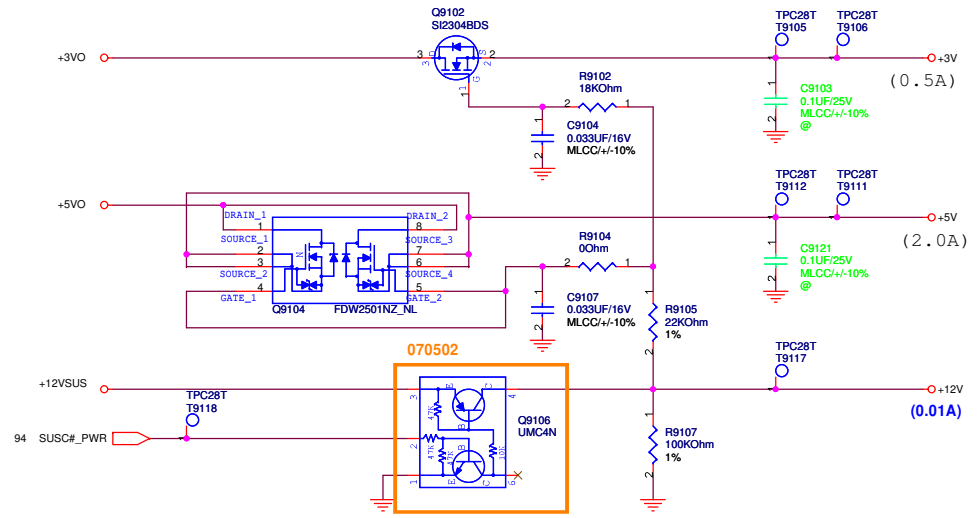
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		Title : POWER_DETECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	F7SR	1.1	
Date: 星期日, 五月 10, 2007	Sheet	90	of 95

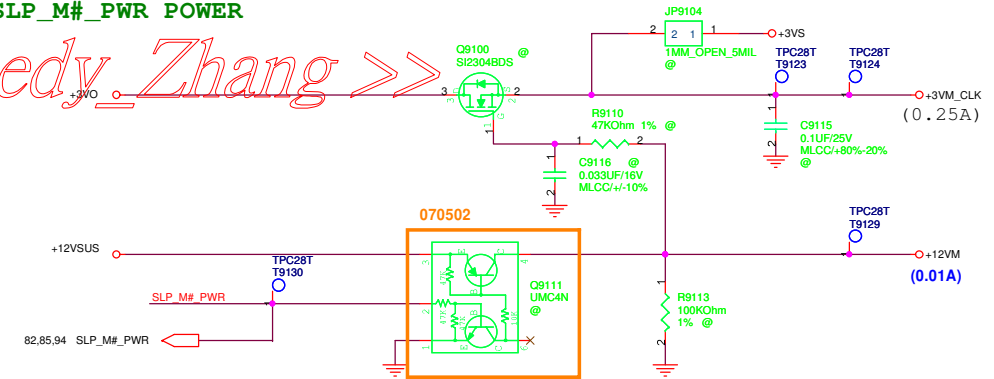
### SUSB#\_PWR POWER



### SUSC#\_PWR POWER



### SLP\_M#\_PWR POWER

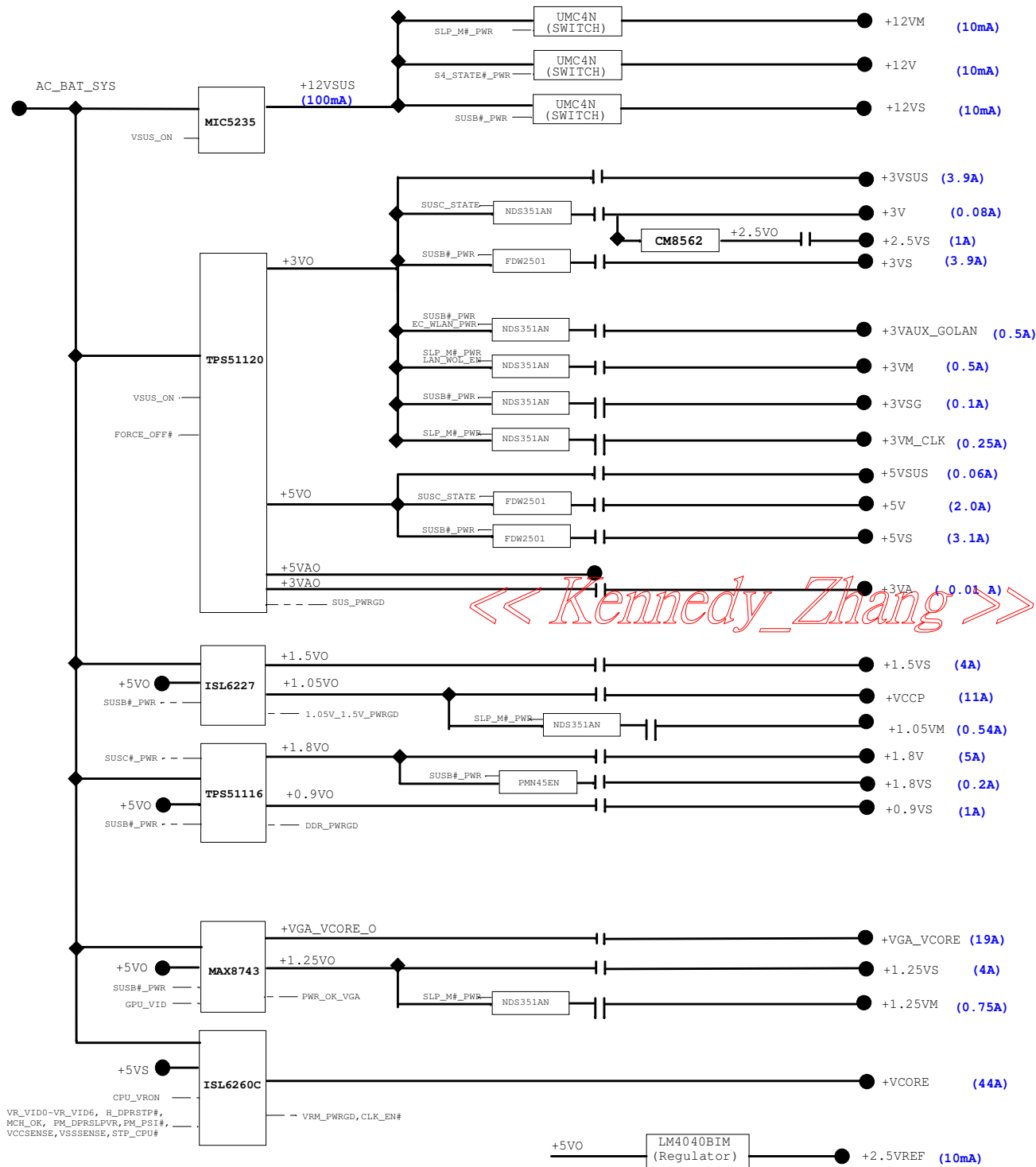


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<Variant Name>

<b>ASUS</b>		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	<b>F7SR</b>	1.1	
Date: 星期四, 五月 10, 2007	Sheet	91	of 95

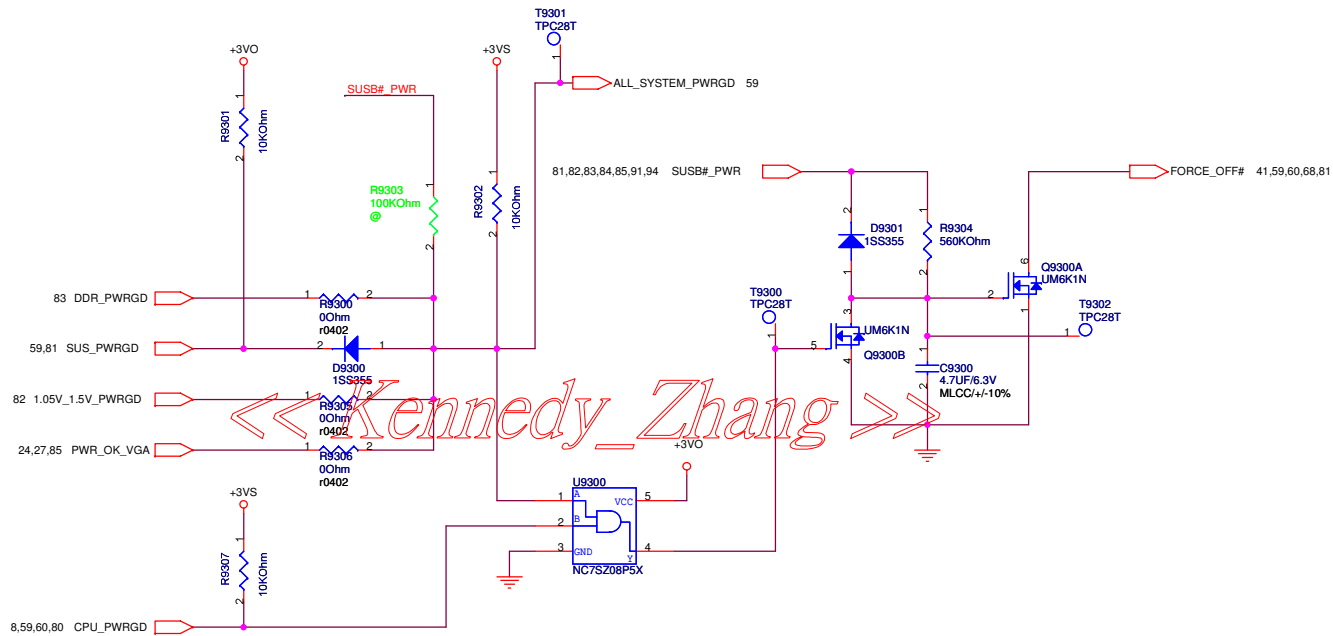
A/D\_DOCK\_IN



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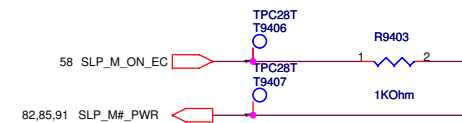
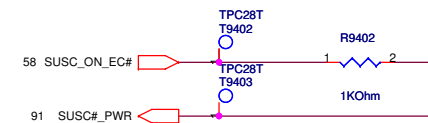
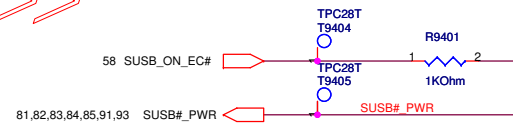
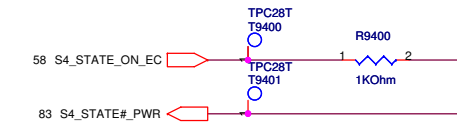
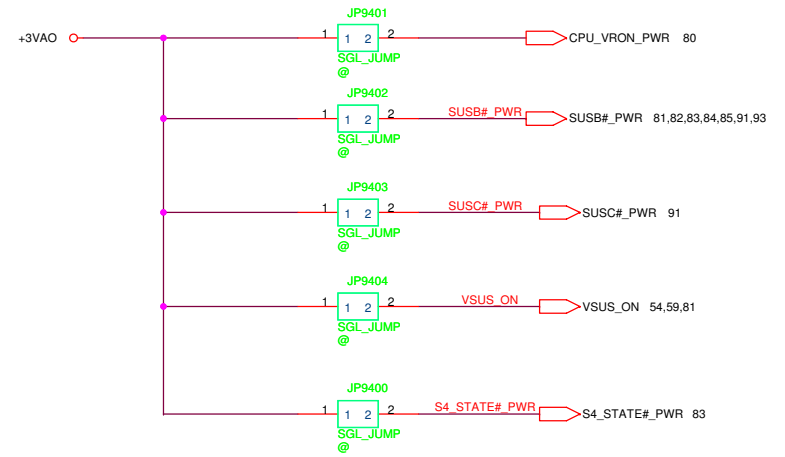
VR\_VID0-VR\_VID6, H\_DPRSTP#, MCH\_OK, PM\_DPRSLEPVR, PM\_PSI#, VCCSENSE, VSSSENSE, STP\_CPU#

### POWER GOOD DETECTOR



AC_BAT_SYS	AC_BAT_SYS	68,80,81,82,83,85,88
+3VA	+3VA	15,33,41,42,58,59,60,81
+1.5VSUS	+1.5VSUS	
+5VO	+5VO	66,81,82,83,84,85,88,90,91
+3VO	+3VO	81,84,85,91,93
+3VSUS	+3VSUS	16,17,18,44,45,54,59,81
+5VSUS	+5VSUS	18,66,81
+3V	+3V	33,42,45,47,49,54,57,76,78,91
+3VS	+3VS	4,8,12,15,16,17,18,32,33,35,37,42,44,47,48,49,51,52,53,54,56,57,59,60,66,70,72,73,76,80,84,91,93
+3VM	+3VM	17,18,20,21,39,65,84
+3VAUX_GOLAN	+3VAUX_GOLAN	
+3VM_CLK	+3VM_CLK	39,91
+12VSUS	+12VSUS	81,84,91
+12V	+12V	42,53,57,91
+12VS	+12VS	27,32,33,57,66,91
+5V	+5V	33,42,54,62,91
+5VS	+5VS	17,18,32,35,37,42,44,56,57,61,66,72,80,91
+2.5VO	+2.5VO	84
+2.5VS	+2.5VS	23,27,42,56,84
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	8,11,12,20,21,42,83
+VCCP	+VCCP	4,5,7,9,11,12,15,18,23,27,39,42,82
+1.05VM	+1.05VM	11,82
+0.9VO	+0.9VO	83
+0.9V	+0.9V	22,42,83
+0.9VS	+0.9VS	28,29,42,83
BAT	BAT	88
+2.5VREF	+2.5VREF	84,88,90
+VCORE	+VCORE	5,80
+VGA_VCORE	+VGA_VCORE	23,27,85
+VRAM	+VRAM	23,24,25,27,28,29,42,73,91
+1.25VS	+1.25VS	12,18,23,27,42,85
+1.25VM	+1.25VM	8,12,85
BAT_CON	BAT_CON	68,88
+1.1VS	+1.1VS	23,27,84

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<Variant Name>

<b>ASUS</b>		<b>Title : POWER_SIGNAL</b>
<OrgName>		Engineer:
Size Custom	Project Name <b>F7SR</b>	Rev 1.1
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Rev	Date	Description
1.0	2006/07/	1. Initial release.
1.1	2006/09/29	1.Enable INTVRMEN and LAN100_SLP (Remove R1506, R1511).[15] 2.Change R0803 R0804 to 20ohm.[8] 3.Set PCIE graphic lane to normal mode.(Unmount R0809).[8] 4.Pull high 10Kohm at 3GSIM_DATA.[33] 5.Change INVCN0 to 20 pin.[33] 6.Change net name "INT_MIC_P" to "INTMIC_P".[56] 7.Change R5706 and R5707 to 75ohm.[56] 8.Change CE5701 and CE5702 to 100UF.[57] 9.Add +1.5V discharg circuit.[42] 10.Remove R5415.[54] 11.Change power "+12V" to "+12VS".[54] 12.Change R6401,R6403,R6409 to10KOhm.[64] 13.Change C2940 to0.1uF.[28] 14.Change EC_GPIO pin define for design IP.[59] 15.Add debounce and thermal circuit for EC design IP.[60] 16.Change C1612,C1613 to 0.1uF.[16] 17.Change C7302,C7308 to 10uF and remove C7315, C7307,C7321,C7301,C7309,C7313,C7310,C7320, C7321.[73] 18.Remove Q4401,Q5404 and change R1604 to 1Kohm.[16,44,54] 19.Revers D6602.[66] 20.Remove C4401,C4404.[44] 21.Colay M66/M76M.[23~30] 22.Connect ICH8M_LAN_RST# to GND.[17] 23.Add JACK detect circuit at DOS mode.[15] 24.Connect M_VREF_MCH to" 0.9V_VTT_REF".[8] 25.Change R0402 to 1Kohm.[4] 26.Change R3952 to 270Ohm.[39] 27.Swap "xD_GND1" and "xD_CD".[53] 28.Add R and C to avoid pop.[56] 29.Add 3G Led circuit.[66] 30.Connect "BUF_PLT_RST#" and "IDERST#" by 47Ohm.[72]

Rev	Date	Description

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