

« Kennedy Zhano »

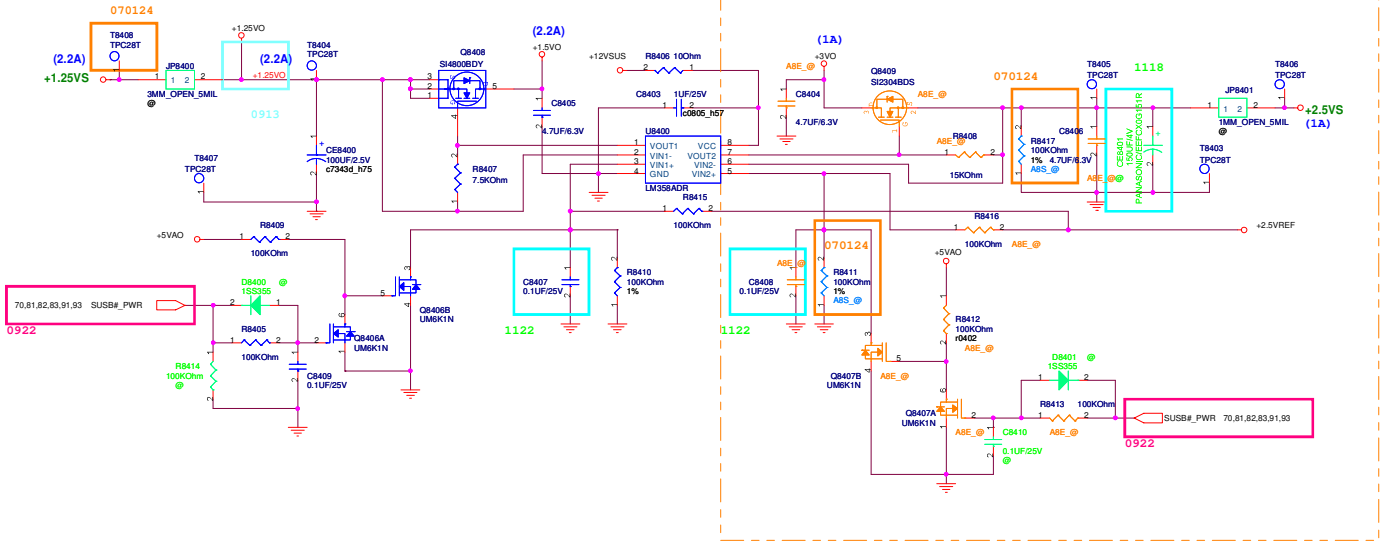
电路分析
整机图纸
点位图
BIOS程序
维修教程

# 不凡修笔记本维修

http://bufanxiu.taobao.com

首页
信用评价
店铺介绍
交流区

+1.25VS & +2.5VS




ECNR2.0:070319  
 Add: C8404, C8406, C8408, R8408, R8412, R8413, R8416, Q8407, Q8409  
 Del: R8411, R8417


A8E: unmount --> @ & A8E\_@  
 A8S: unmount --> @ & A8S\_@

ASUS		Title : POWER_IQ_+3VA & +2.5V	
Project Name		Engineer:	
Site	Custom	ABS	
Date: 2018-08-23	Sheet	0	of 15

<< Kennedy\_Zhang >>

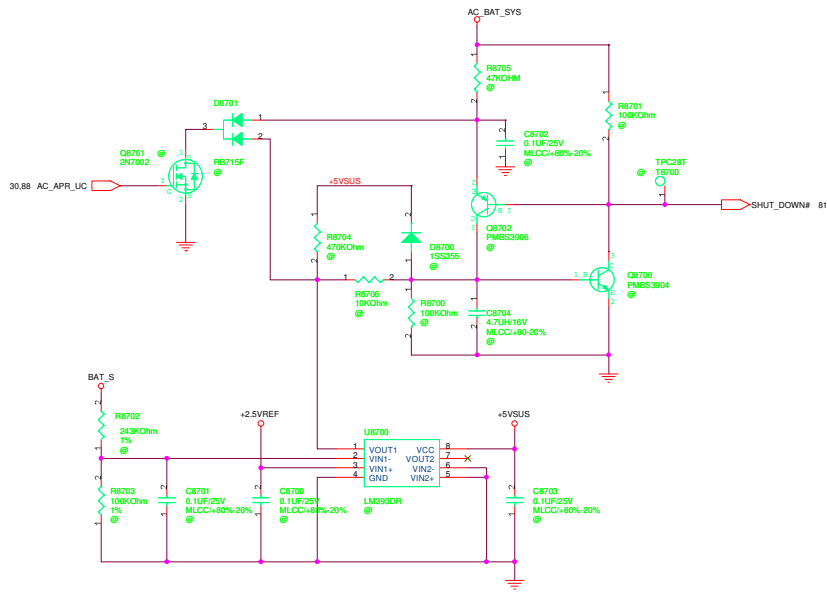
« Kennedy\_Zhang »

-Variant Name-		Title : POWER_VIA_CORE & RAM	
		Engineer:	
-Circuit Name-	Project Name	Rev	
C	ROSA	1.1	
Date: 11/11/2017	Sheet: 0	of	15

<Variant Name>		
		Title : N/A
<OrgName>		Engineer:
Size B	Project Name <b>ROSA</b>	Rev 1.1
Date: 2007年08月08日		Sheet 0 of 15

*<< Kennedy\_Zhang >>*

PIC only



<Variant Name>		<b>ASUS</b>		<b>Title : POWER_SHUTDOWN#</b>	
<OrigName>		Engineer:			
Size	Project Name	Rev			
Custom	ARES	2.0			
Date: 8/8	7:1 08.2007	Sheet	0	of	16

« Kennedy\_Zhang »

POWER PATH & BAT\_LEARN

● AC\_IN Threshold > 2.048Vmax AD\_DOCK\_IN > 17.44V active  
 Adapter (In/ma) = (0.075V/Rsense/Adm)/(VCLS/VREF)  
 Rsense=Adm/0.075  
 VCLS=2.534V  
 => In/ma=4.5A  
 => Constant Power = 12.15 + 55.5W  
 => RBS2=20k,RBS1=137k-->65W  
 => RBS5=20k,RBS19=30k-->60W

Charge Current Idcg = (0.075V/Rsense/CHG)/(VCTL3.6V)  
 Rsense=CHG/0.075  
 VCTL=3V => Ichg = 2.5A  
 VCTL=1.58V => Ichg = 1.4A

Vbat = Cch \* (Vbat - (VCTL - 1.5V) / 9.52)  
 VCTL = 1.58V  
 => Vbat = 4.2V

Mode pin: Vinode > 2.8V (9k to LDO pin) => 4 Cells  
 2.8 > Vinode > 1.6V (Resistor) => 3 Cells  
 0.8 > Vinode (pin to GND) => Learning mode

VCTL=0.8V or DCIN = 7V --> Charger Disable

Package current=150mA

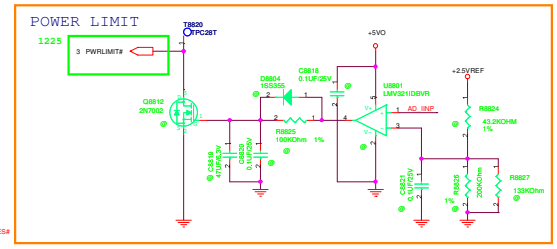
AD\_DOCK\_IN  
 AD\_DOCK\_IN  
 MAX8725\_LDO  
 MAX8725\_REF  
 LDO: 5.4V  
 REF: 4.2235V

9929  
 90W -> 10K Ohm -> VCLS=2.534V  
 65W -> 13.7K Ohm -> VCLS=3.653V

9919  
 mount: 4S  
 umount: 3S

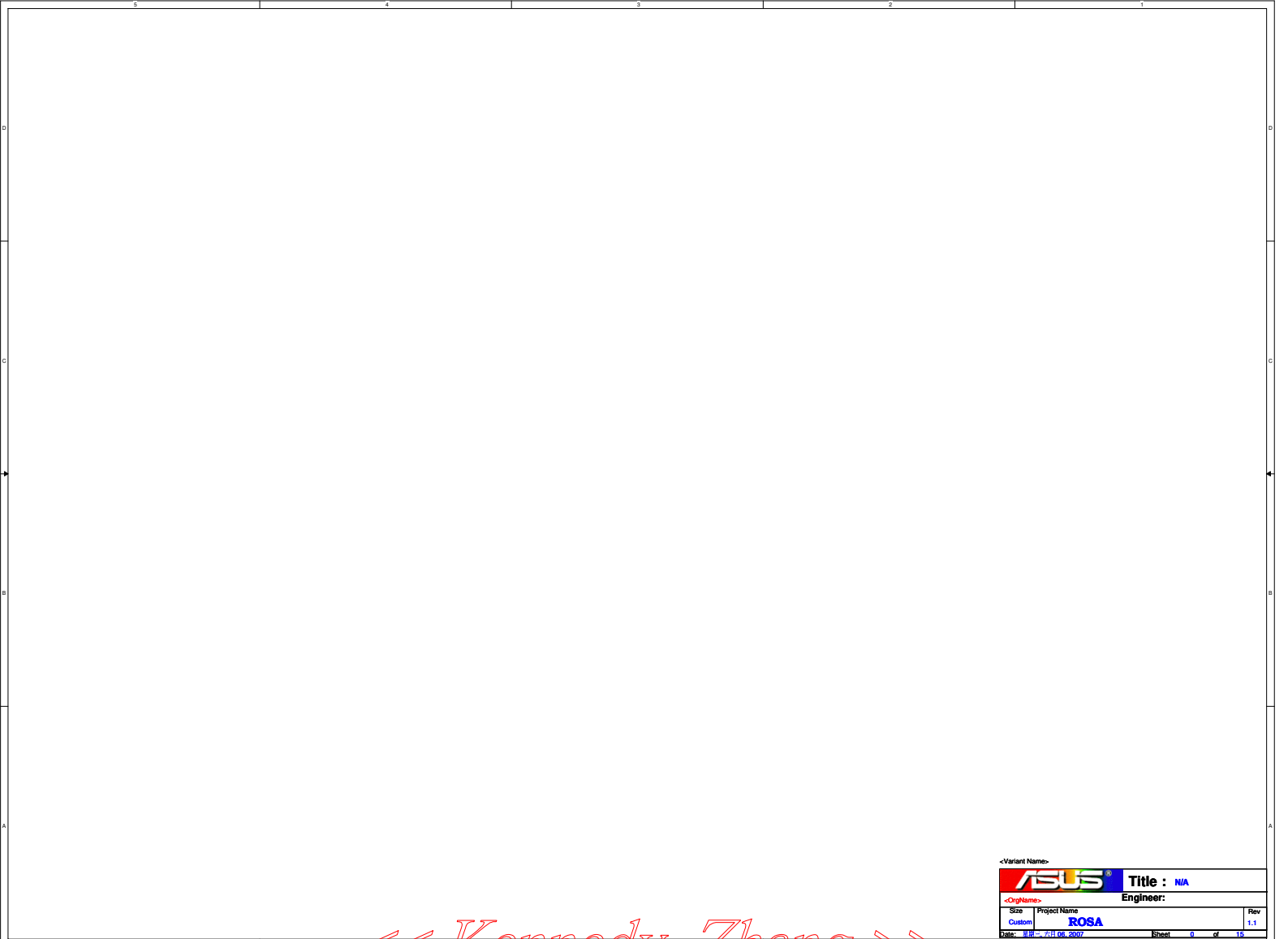
9922  
 60.90 TSH

30.92 BAT\_LEARN




ASUS		Title: POWER_CHARGER	
Design	Project Name	Engineer	
C	ABS		Rev 2.0
Date: 11/02/2017	Doc No: 2017	Sheet	1 of 15

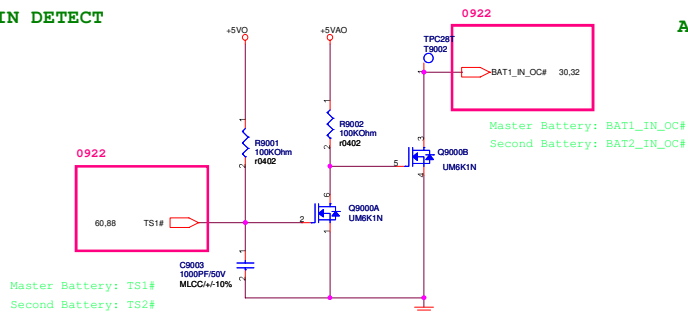
« Kennedy\_Zhang »



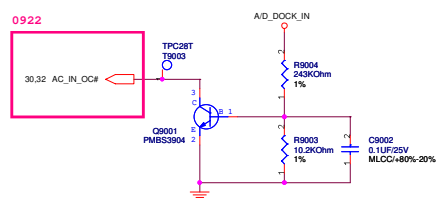
*« Kennedy\_Zhang »*

<Variant Name>		
		Title : NA
<OrigName>		Engineer:
Site	Project Name	Rev
Custom	<b>ROSA</b>	1.1
Date: 8/8/2007		Sheet 0 of 16

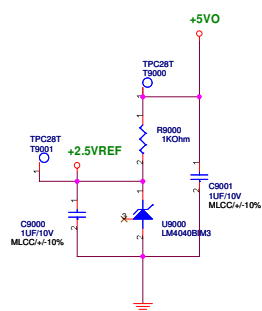
**BATTERY IN DETECT**



**ADAPTER IN DETECT**



**+2.5VREF**



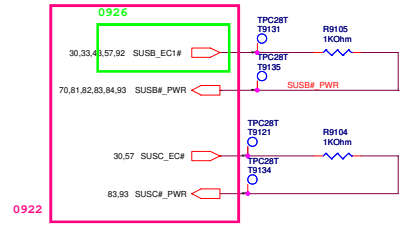
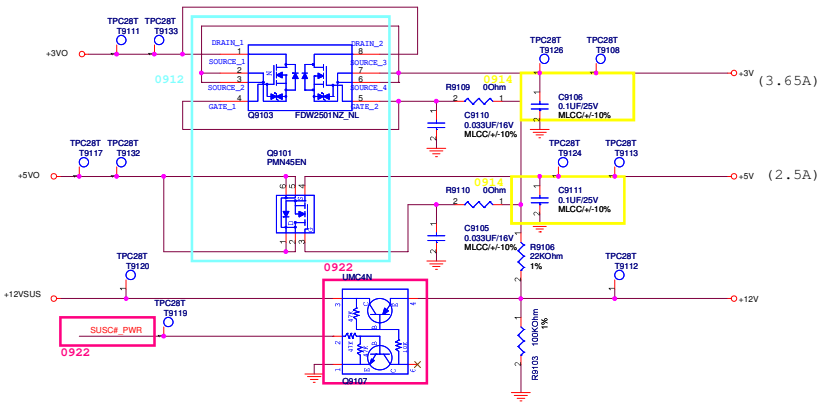
-Variant Name-		Title : POWER_DETECT	
ASUS		Engineer:	
Size	Project Name	Rev	
Custom	ABES	2.0	
Date: 08/06/2007	Sheet 0 of 15		

« Kennedy\_Zhang »



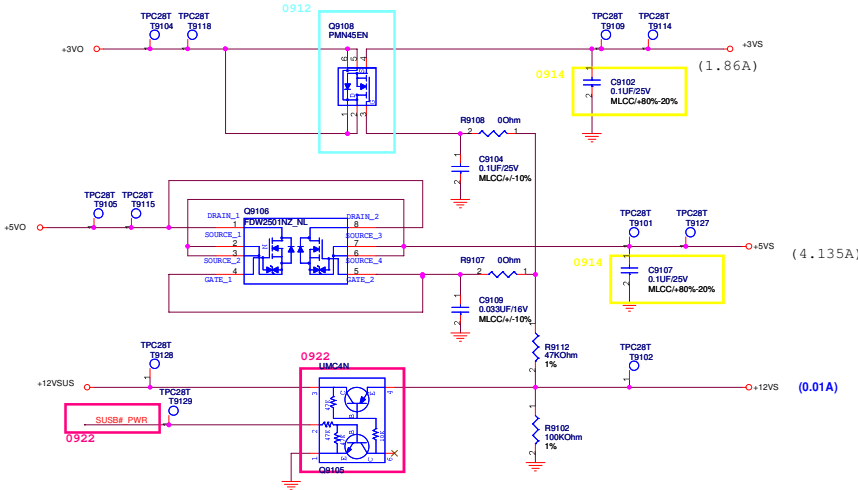
**SUSC#\_PWR POWER**

0922



**SUSB#\_PWR POWER**

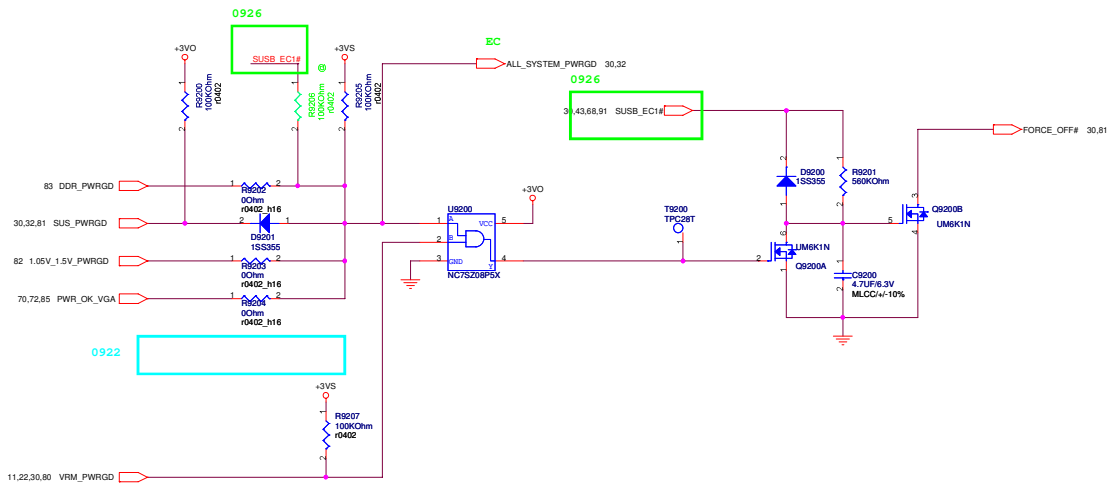
0922



Title : POWER_LOAD SWITCH	
Engineer:	
Size	Project Name
Custom	AES
Date: 8/11/2007	Sheet 8 of 15

« Kennedy\_Zhang »

POWER GOOD DETECTOR

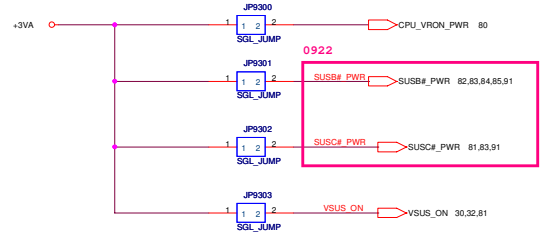


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<Variant Name>		<b>ASUS</b>		<b>Title : POWER_PROTECT</b>	
<OrigName>		Engineer:			
Site	Project Name	Rev			
Custom	<b>ARES</b>	2.0			
Date: 8/8/2007	7:11 08.2007	Sheet	0	of	16

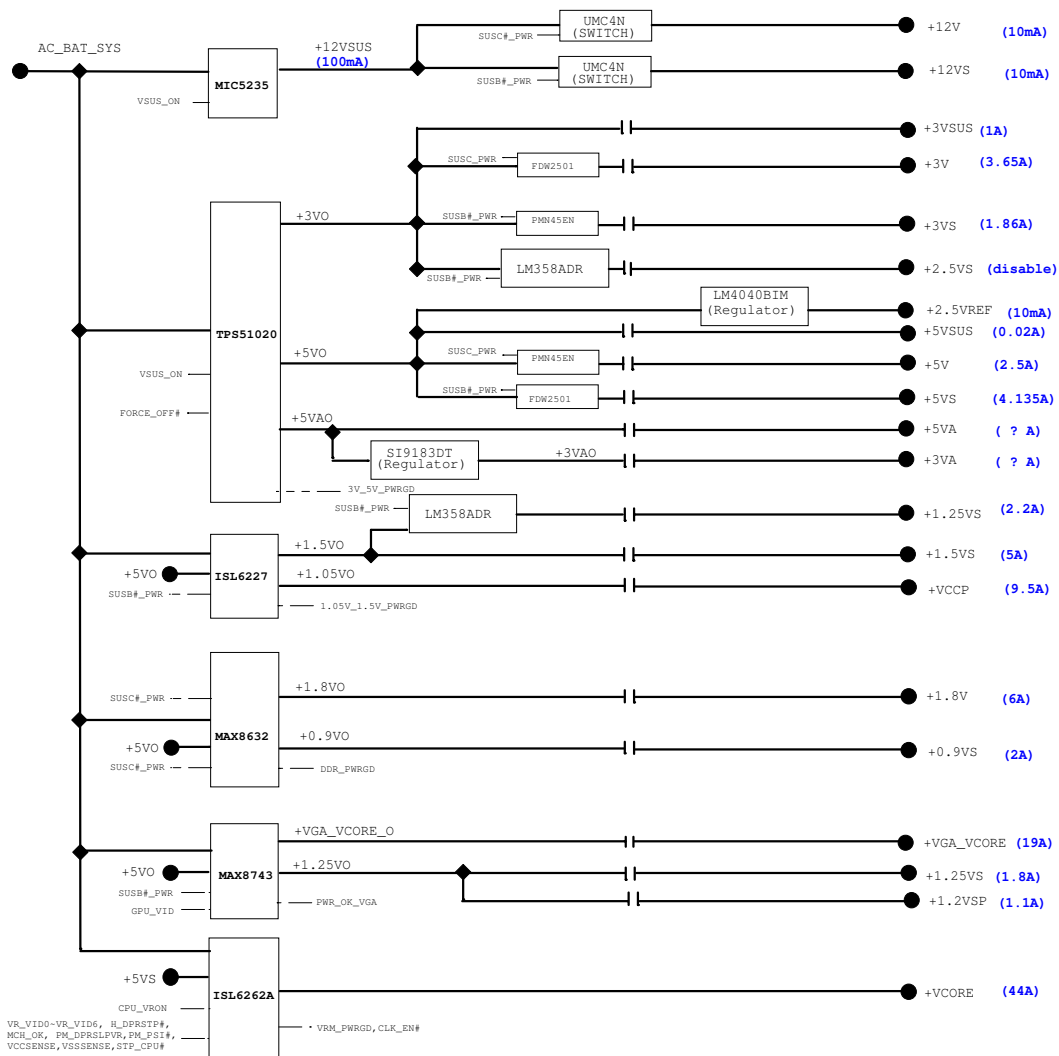
AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,85,87,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	84,87,90
+3VA	+3VA	20,22,30,34,67,68,81,88
0922 +5VAD	+5VAD	20,22,30,34,67,68,81,88
+5VDO	+5VDO	81,82,83,84,85,90,91
+5VSUS	+5VSUS	23,51,52,81,87
+5V	+5V	9,43,52,57,67,91
+5VS	+5VS	23,24,31,46,50,51,57,67,70,76,77,80,91
+3VO	+3VO	81,82,83,85,91,93
+3VSUS	+3VSUS	21,22,23,30,33,51,52,81
+3V	+3V	21,34,43,53,57,62,77,84,91
+3VS	+3VS	3,7,8,11,14,15,22,23,24,29,30,32,33,40,41,42,43,45,46,50,51,53,57,58,61,62,66,67,70,76,77,80,91,93
+12VSUS	+12VSUS	52,81,91
+12V	+12V	42,84,91
+12VS	+12VS	45,91
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	7,8,9,11,13,83
+1.8VS	+1.8VS	66,76,91
+0.9VS	+0.9VS	9,83
0922 +0.9VO	+0.9VO	9,83
0922 +1.05VDO	+1.05VDO	3,5,10,11,13,14,23,29,37,82
+VCCP	+VCCP	3,5,10,11,13,14,23,29,37,82
+1.5VO	+1.5VO	66,76,91
0922 +1.5VS	+1.5VS	66,76,91
+2.5VO	+2.5VO	84
+2.5VS	+2.5VS	57,70,72,84
+VCCORE	+VCCORE	4,5,80
+VRAM	+VRAM	70,72,73,74,91
+1.2VSP	+1.2VSP	85
+1.2VS	+1.2VS	11,14,23,70,71,72,85

FOR POWER TEST



<Variant Name>			
<b>ASUS</b>		Title :	POWER_SIGNAL
<OrgName>		Engineer:	<OrgAddr1>
Site	Project Name		Rev
Custom	ABES		2.0
Date: 2007-06-28		Sheet	0 of 15

« Kennedy\_Zhang »

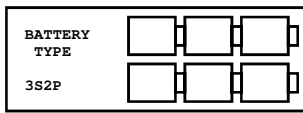


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# A8E/A8S/F8S Merom/GM965/PM965 BLOCK DIAGRAM

Sub block Diagram / BOM option 64

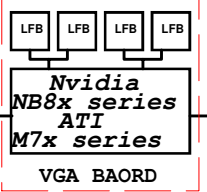
**CLOCK GEN**  
ICS9LPR363AGLF-T  
29



**CPU**  
MEROM 3,4

CPU CAP 5

POWER SEQUENCE 2



**CRESTLINE**  
GM965/PM965  
11~15

DDR2 SDRAM 533/667MHz  
SODIMM X2  
+1.8V  
+0.9VS  
7,8

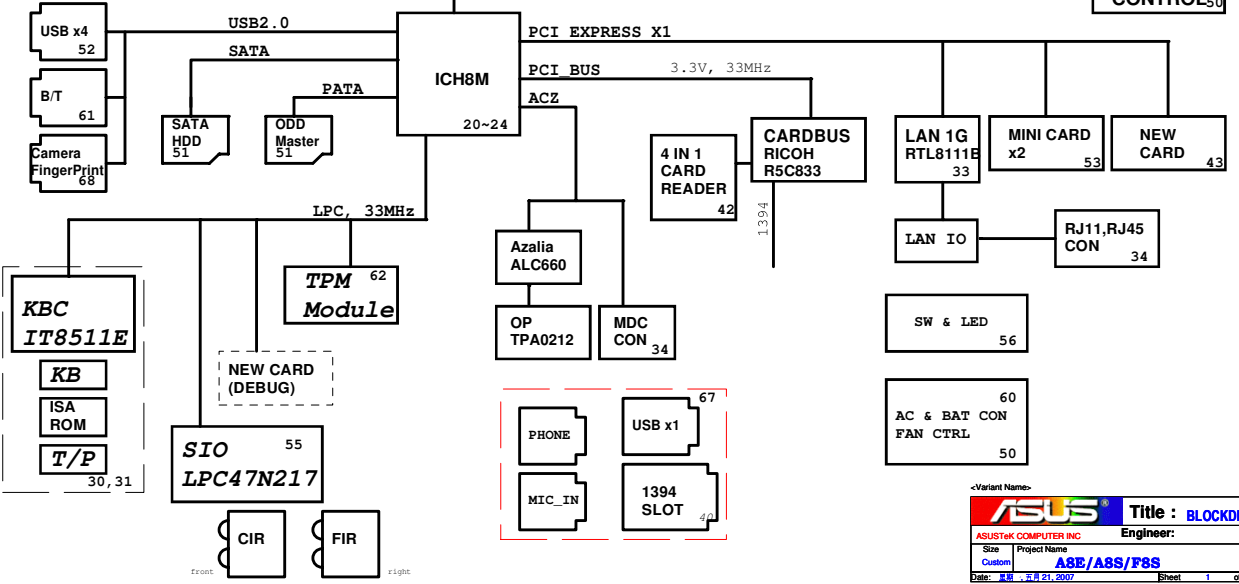
DDR CAP/RES 9

DCIN  
RTC  
FAN CON.

**THERMAL CONTROL**  
50

DVI Dual CH. 47  
VGA CON  
CRT & TV CON 46  
LVDS & INV CON 45

- VCORE
- SYSTEM
- 1.5VS & 1.05VS
- DDR & VTT
- +3VAO & +2.5VS
- CHARGER
- DETECT
- PROTECT
- LOAD SWITCH
- FLOWCHART
- SIGNAL

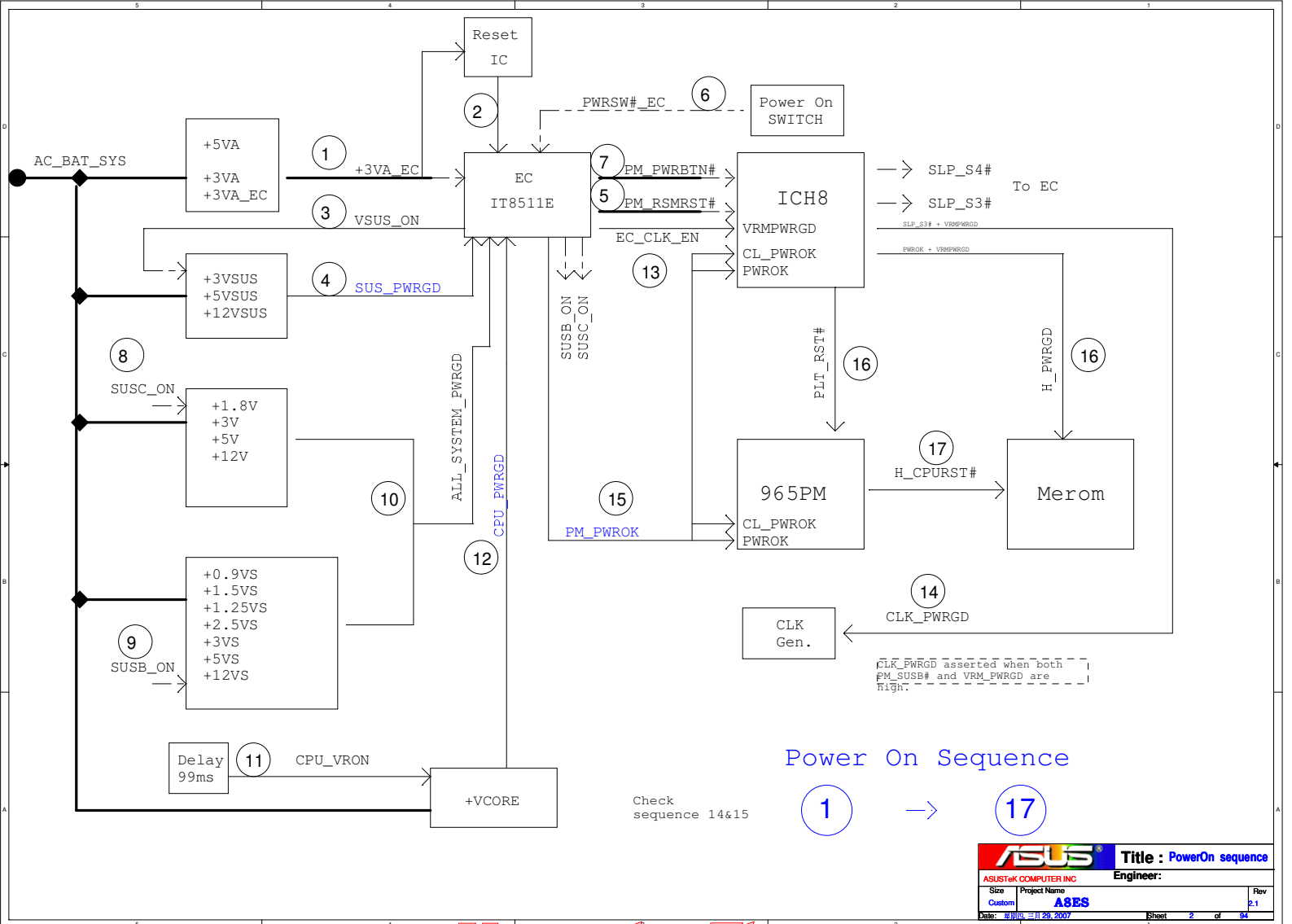


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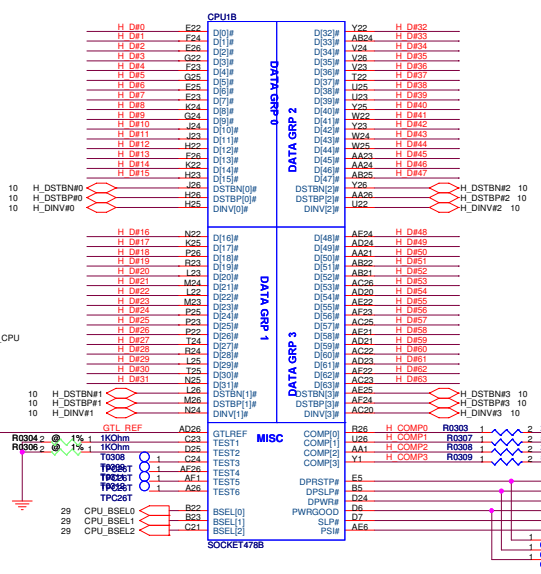
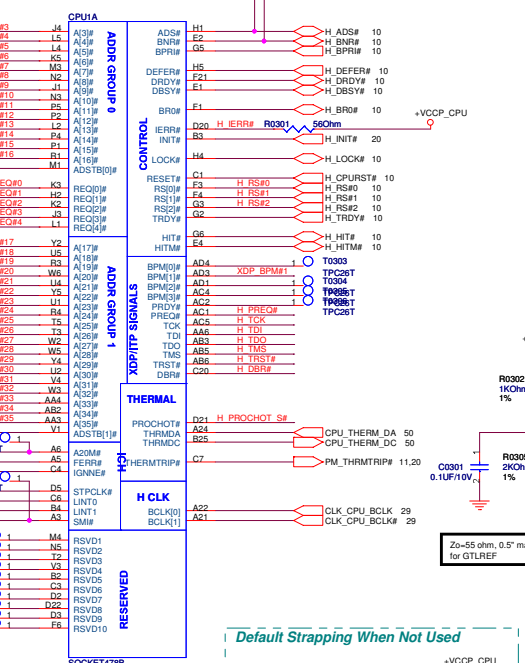
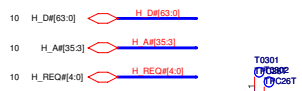
**Title : BLOCKDIAGRAM**

ASUSTek COMPUTER INC.	Engineer:
Size: Custom	Project Name: A8E/A8S/F8S
Date: 08/21/2007	Rev: 2.2
Sheet: 1	of: 64

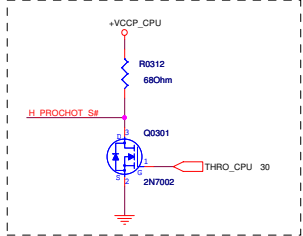
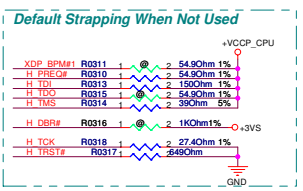
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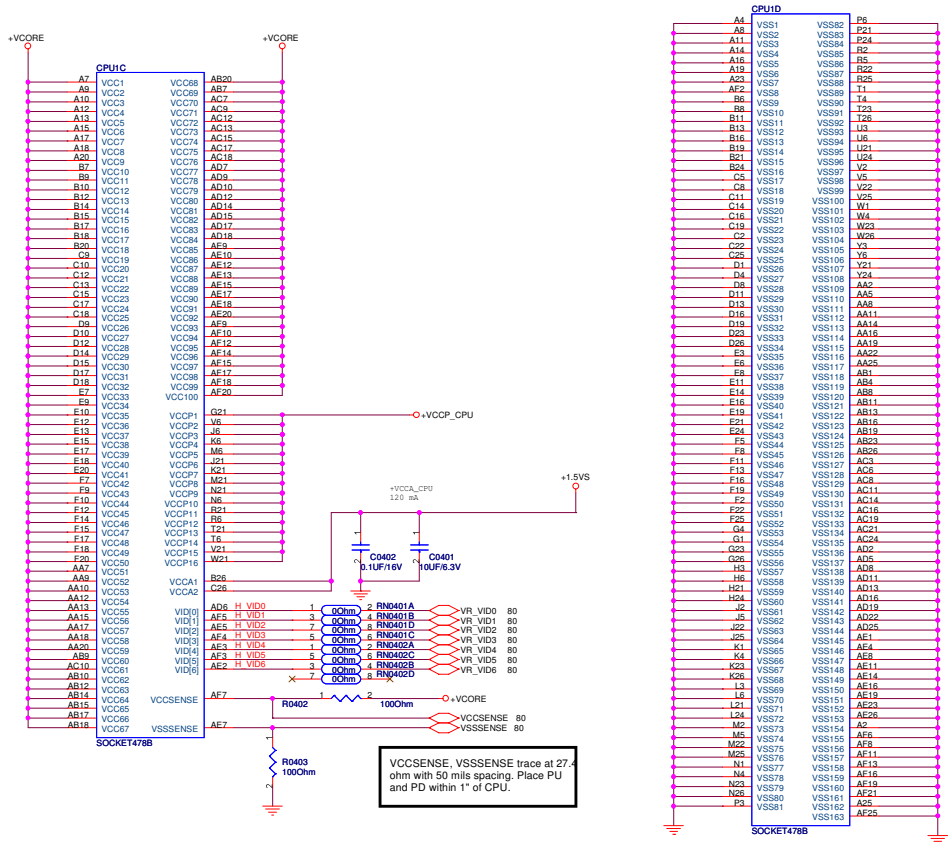


Comp0.2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
 Comp.1.3 connect with Zo=55 ohm, make trace length shorter than 0.5".



<b>ASUS</b>		<b>Title : MEROM CPU (1)</b>	
ASUSTEK COMPUTER INC.		Engineer:	
Size	Project Name	Rev	
Custom	<b>ABES</b>	1.0	
Date: 8/21/2007		Sheet	3 of 94

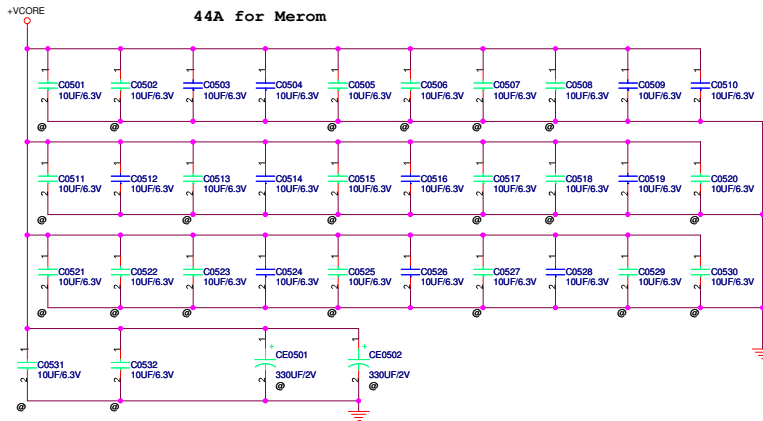
« Kennedy\_Zhang »



<b>ASUS</b>		<b>Title : MEROM CPU (2)</b>	
ASUSTek COMPUTER INC.		Engineer:	
Size	Project Name	Rev	
Custom	<b>ABES</b>	1.0	
Date: 8月16, 2007		Sheet	4 of 84

« Kennedy\_Zhang »

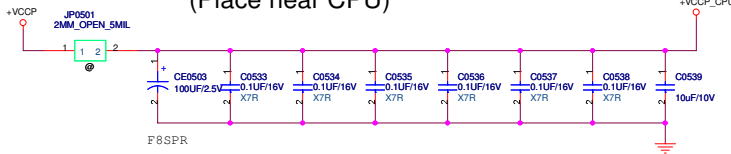




Decoupling guide from INTEL


VCCP	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
VCCP	10uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 16pcs
	5/2(1F8S)	* 11pcs

+VCCP Decoupling Capacitor  
(Place near CPU)

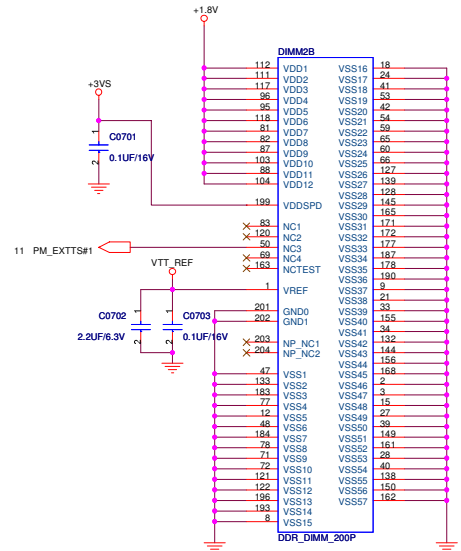
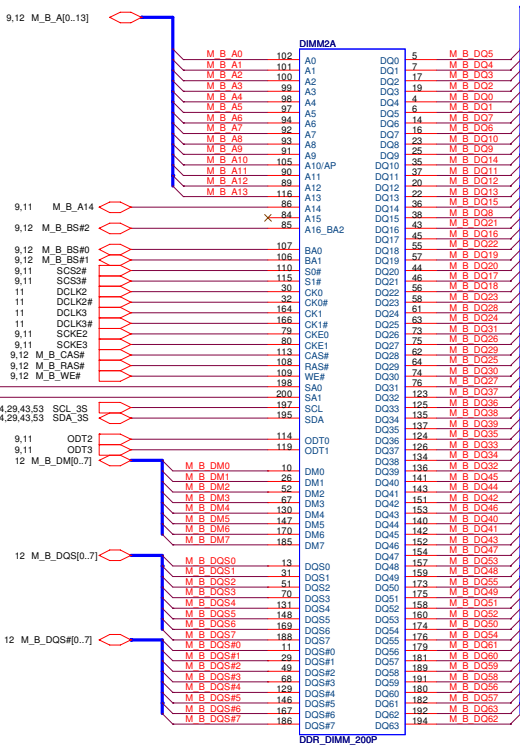


<b>ASUS</b>		<b>Title :CPU CAP</b>
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
B	ABES	1.0
Date: 星期二, 7月21, 2007	Sheet	5 of 94

<< Kennedy\_Zhang >>

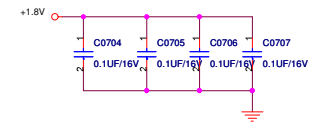
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ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>ASES</b>	Rev 0	
Date: 星期三, 十月 11, 2006		Sheet	6 of 94

←← Kennedy\_Zhang →→

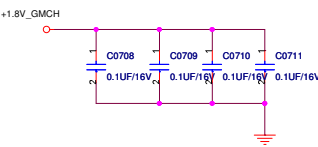


Higher slot:  
SPD/TS=A4/34

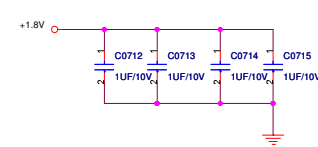
Layout Note: Place these Caps near SO DIMM 0



Layout Note: Place these High-Freq decoupling Caps near the GMCH



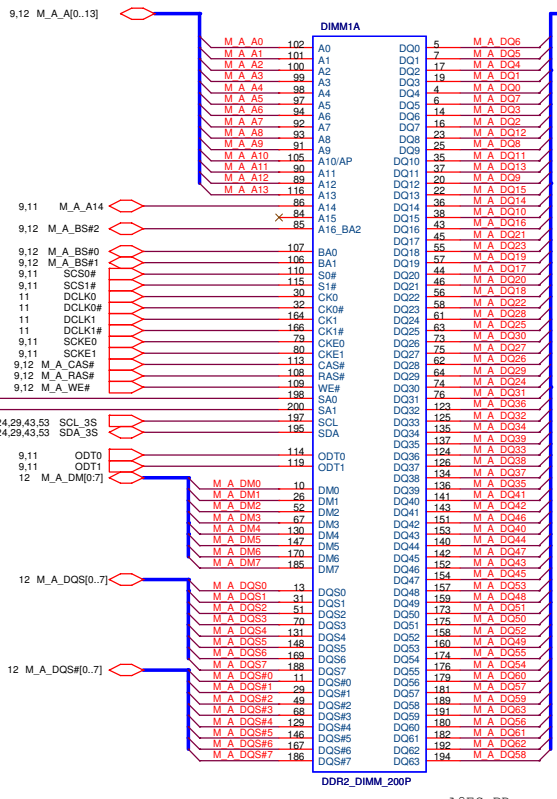
Layout Note: Place these Caps near SO DIMM 0



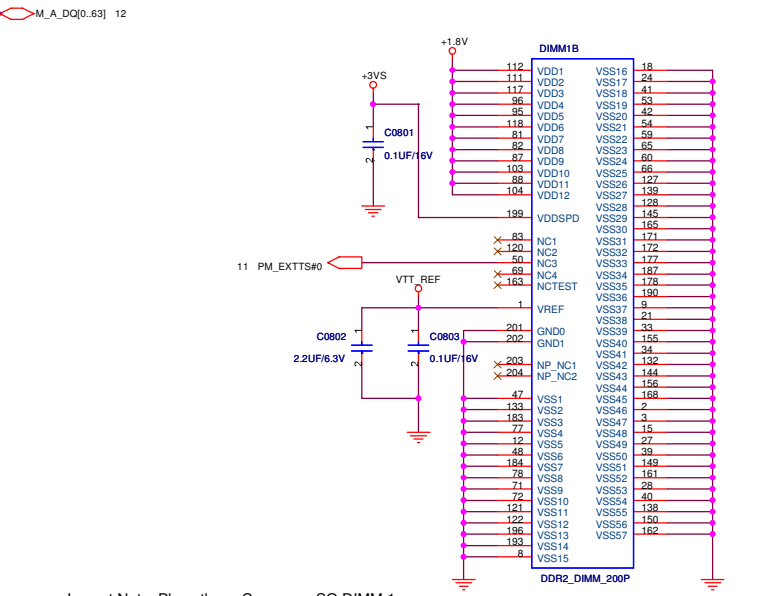
**Upper:Channel B**

<b>ASUS</b>		Title :DDR SO-DIMM	
ASUSTek COMPUTER INC			
Size		Project Name	
Custom		A8ES	
Date: 2007-07-21	Rev	Sheet	7 of 94

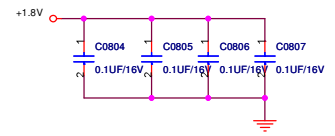
« Kennedy\_Zhang »



Lower slot:  
SPD/TS=A0/30

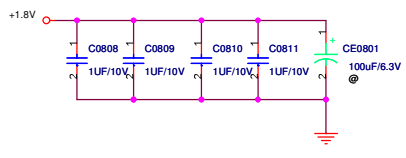


Layout Note: Place these Caps near SO DIMM 1



A8ES.PR

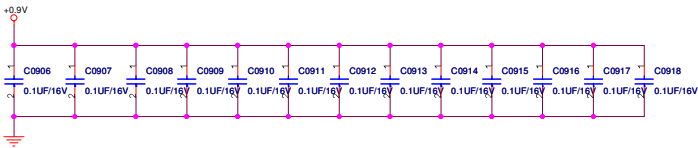
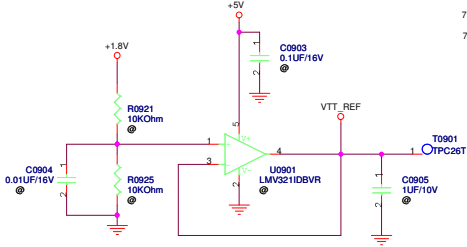
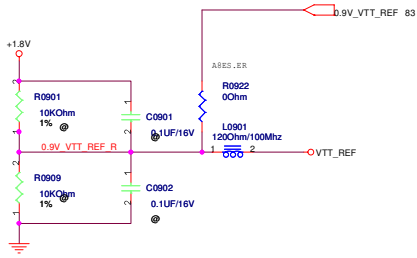
Layout Note: Place these Caps near SO DIMM 1



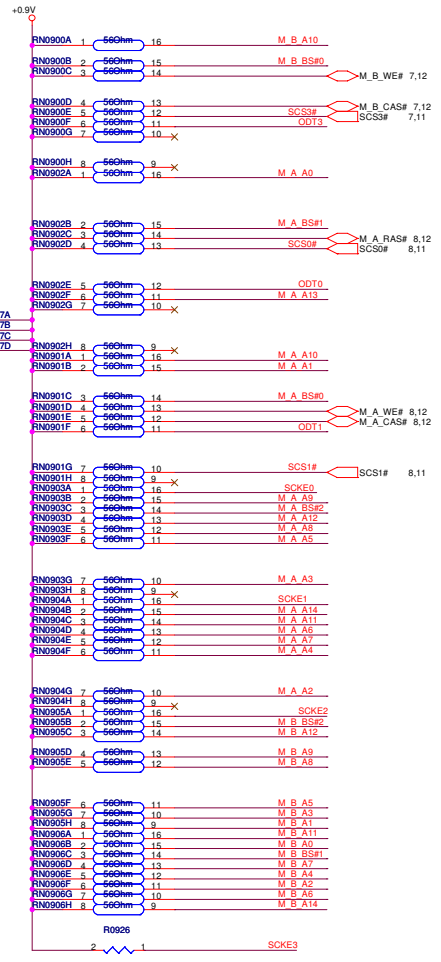
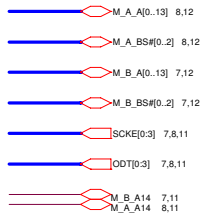
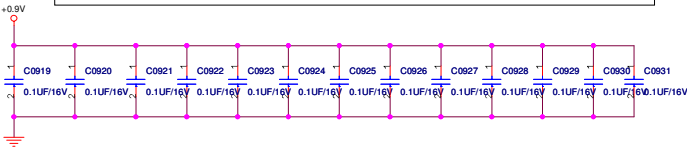
Lower:Channel A

<b>ASUS</b>		<b>Title : DDR SO-DIMM_TOP</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date:	日期: 五月 21, 2007	Sheet	8 of 94

<< Kennedy\_Zhang >>

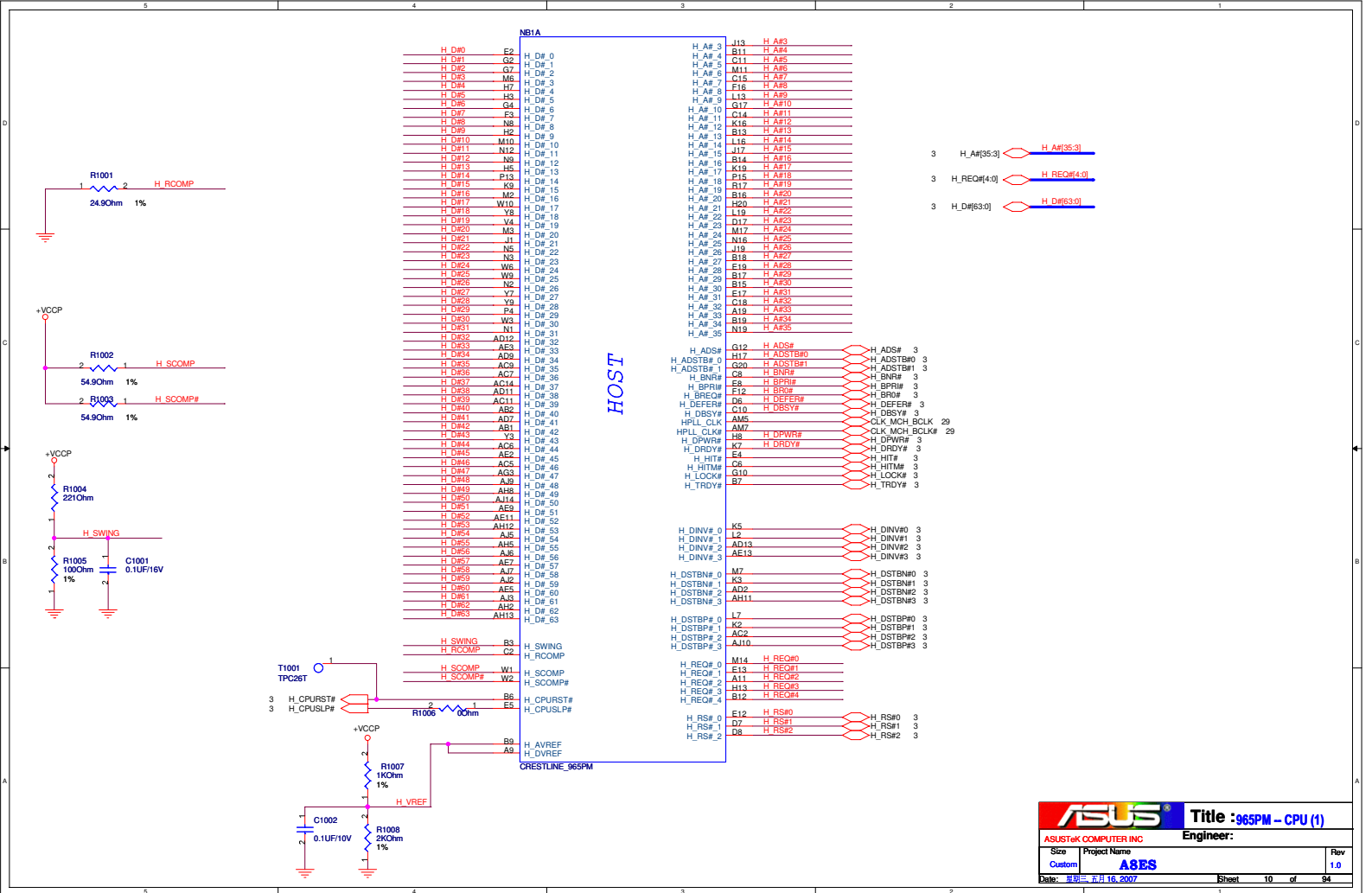


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



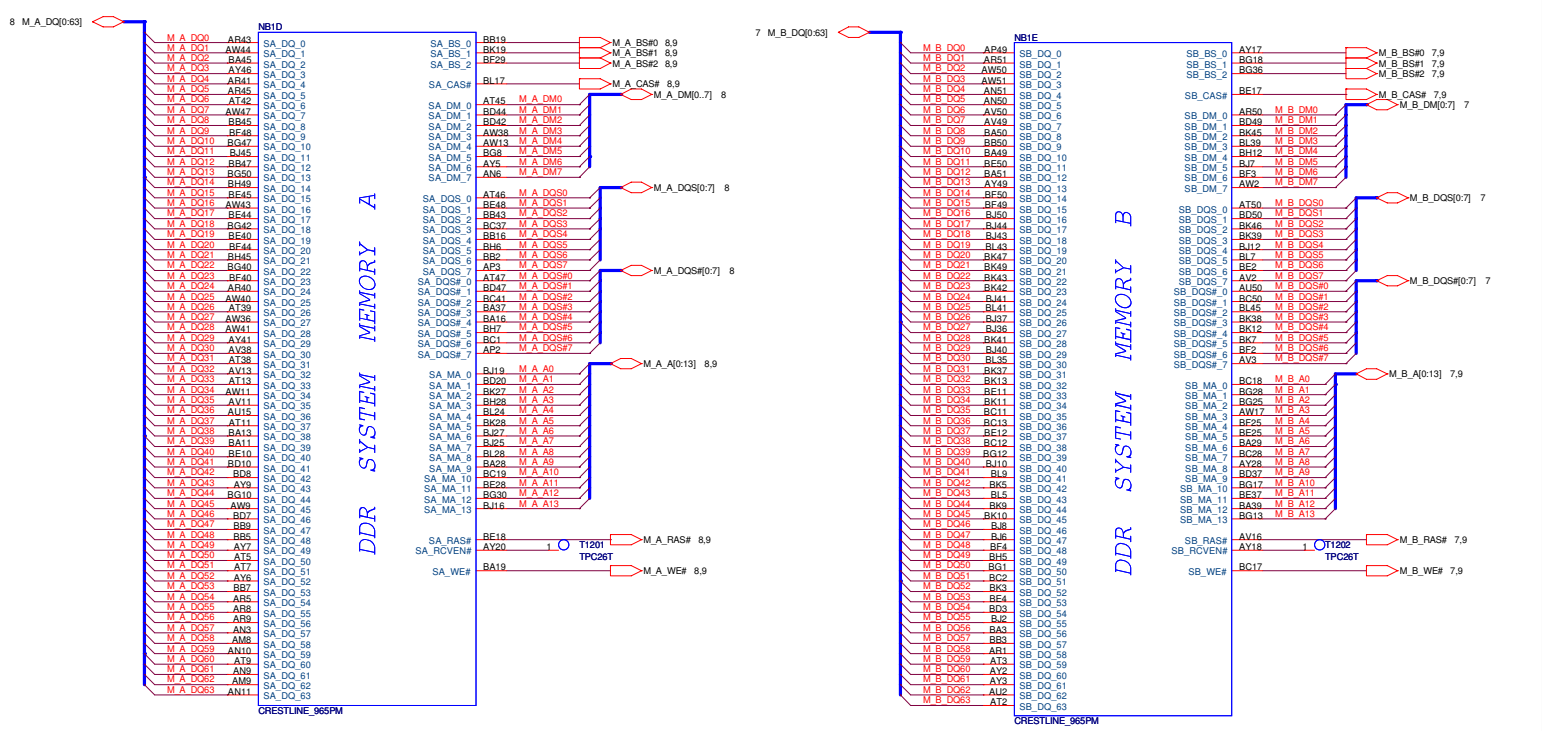
<b>ASUS</b>		<b>Title : DDR2 ADDR TERM</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8BS	1.0	
Date	File Path	Sheet	of
8/8	J:\P1_21_2007	8	94

« Kennedy\_Zhang »



<< Kennedy\_Zhang >>

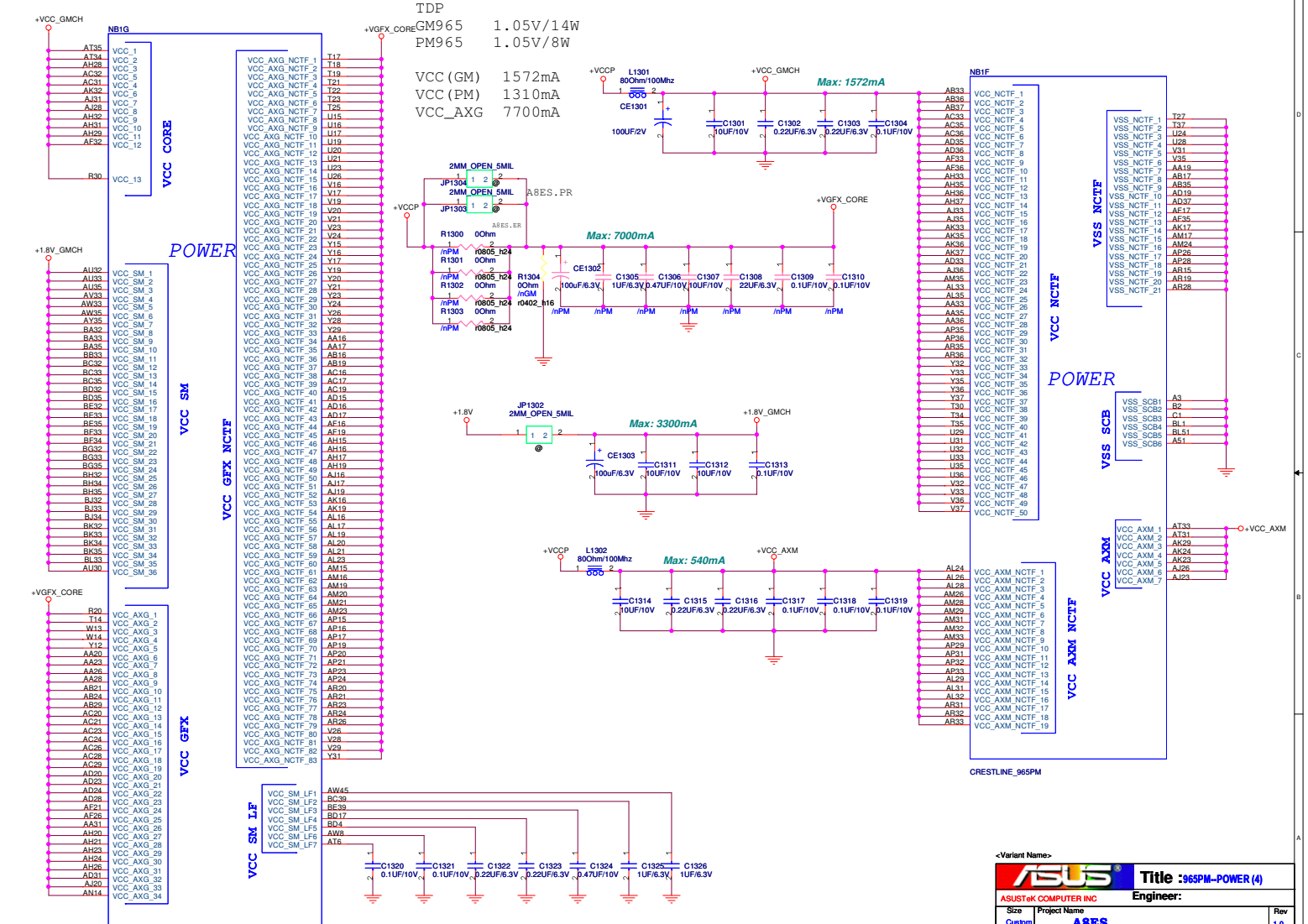




**ASUS** Title : 965PM-DDR2 bus (3)  
 ASUSTeK COMPUTER INC Engineer:  
 Size B Project Name **ASES** Rev 1.0  
 Date: 星期二, 7月29, 2007 Sheet 12 of 94

<< Kennedy\_Zhang >>





**ASUS** Title: 965PM-POWER (4)

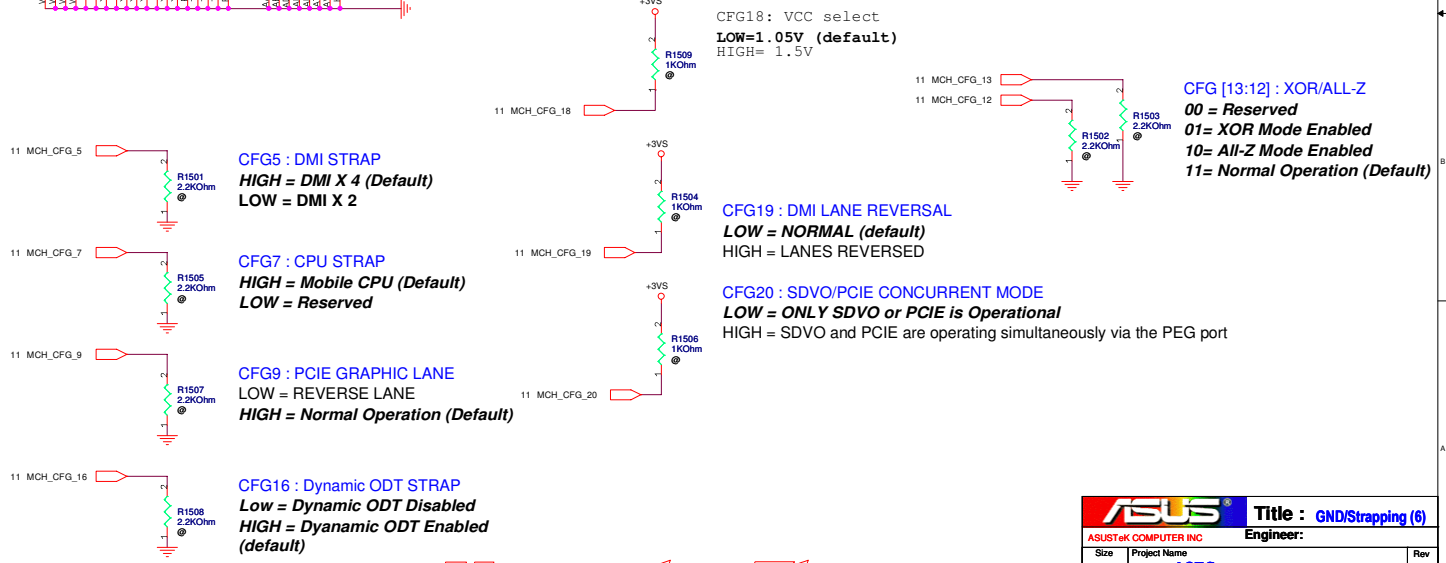
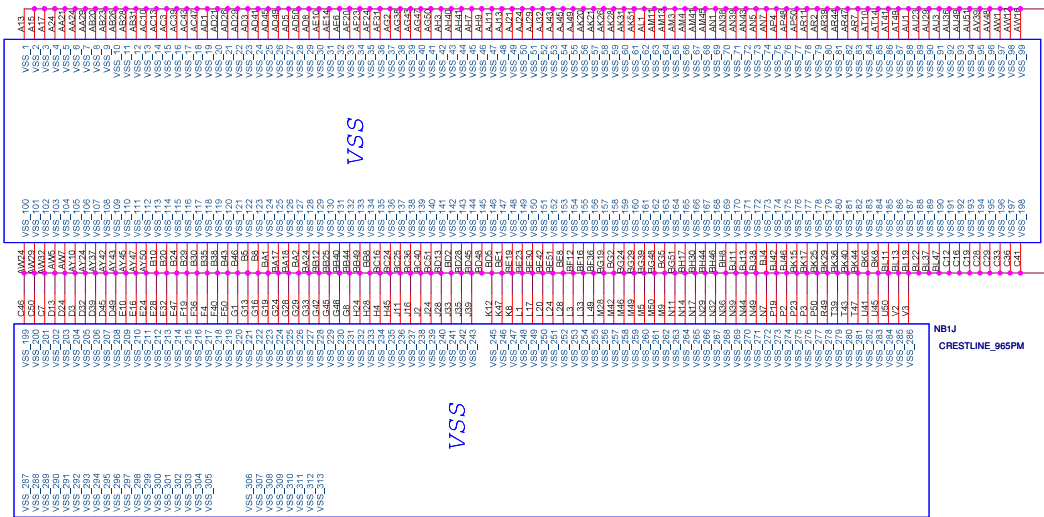
ASUSTeK COMPUTER INC. Engineer:

Site: Project Name: Custom: A8ES


Date: 8月20, 2007 Sheet 13 of 94

« Kennedy\_Zhang »







<< Kennedy\_Zhang >>

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	ASES	0
Date: 星期三, 十月 11, 2006		Sheet 16 of 94

← Kennedy\_Zhang →

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>ASES</b>	Rev 0	
Date: 星期三, 十月 11, 2006		Sheet	17 of 94

←← Kennedy\_Zhang →→

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8ES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet 18 of 94	

*← Kennedy\_Zhang →*

D

D

C


C

B

B

A

A

		<b>Title : BLANK</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>ASES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 19 of 94

← Kennedy\_Zhang →

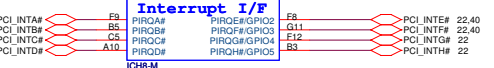
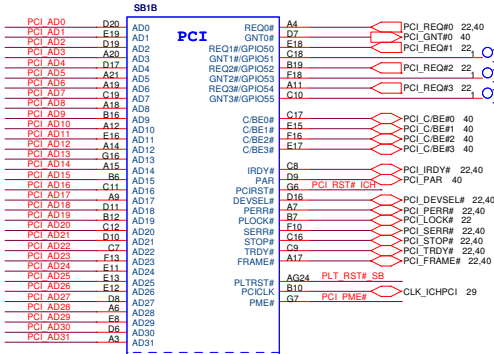
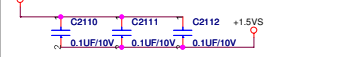




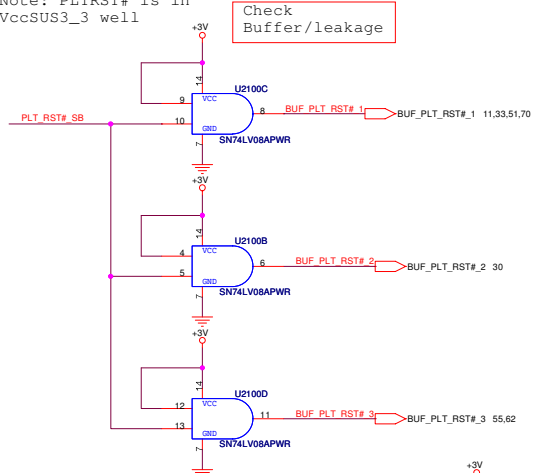
40 PCI\_AD[0..31]

PCI\_AD[0..31]

+3V3 PCI BUS cross moat, add stitching cap

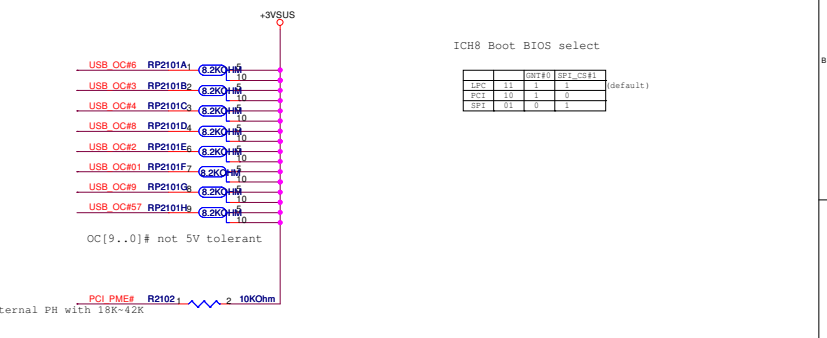
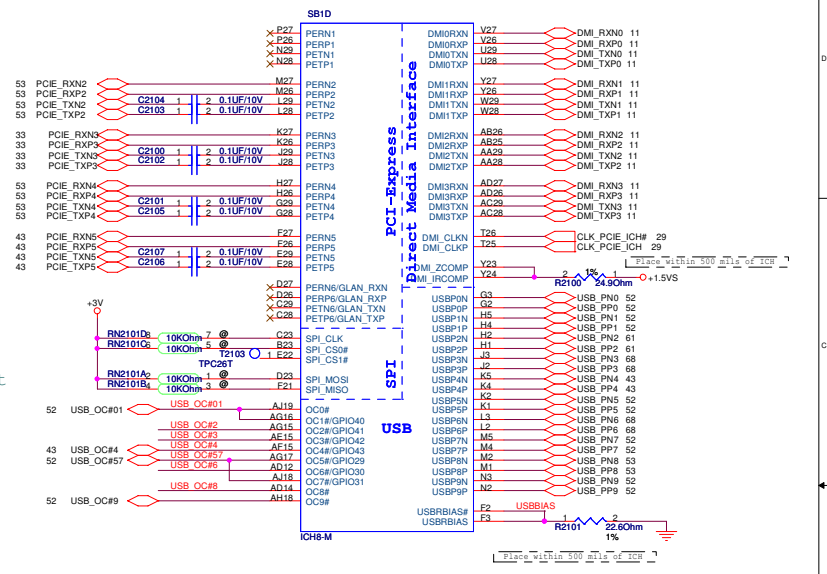


Note: PLTRST# is in VccSUS3\_3 well



miniCard 1  
LAN  
miniCard 2  
NEW CARD

- 0:I/O
- 1:I/O
- 2:Bluetooth
- 3:Finger Print
- 4:New Card
- 5:I/O
- 6:Camera
- 7:I/O
- 8:miniCard 2
- 9:I/O

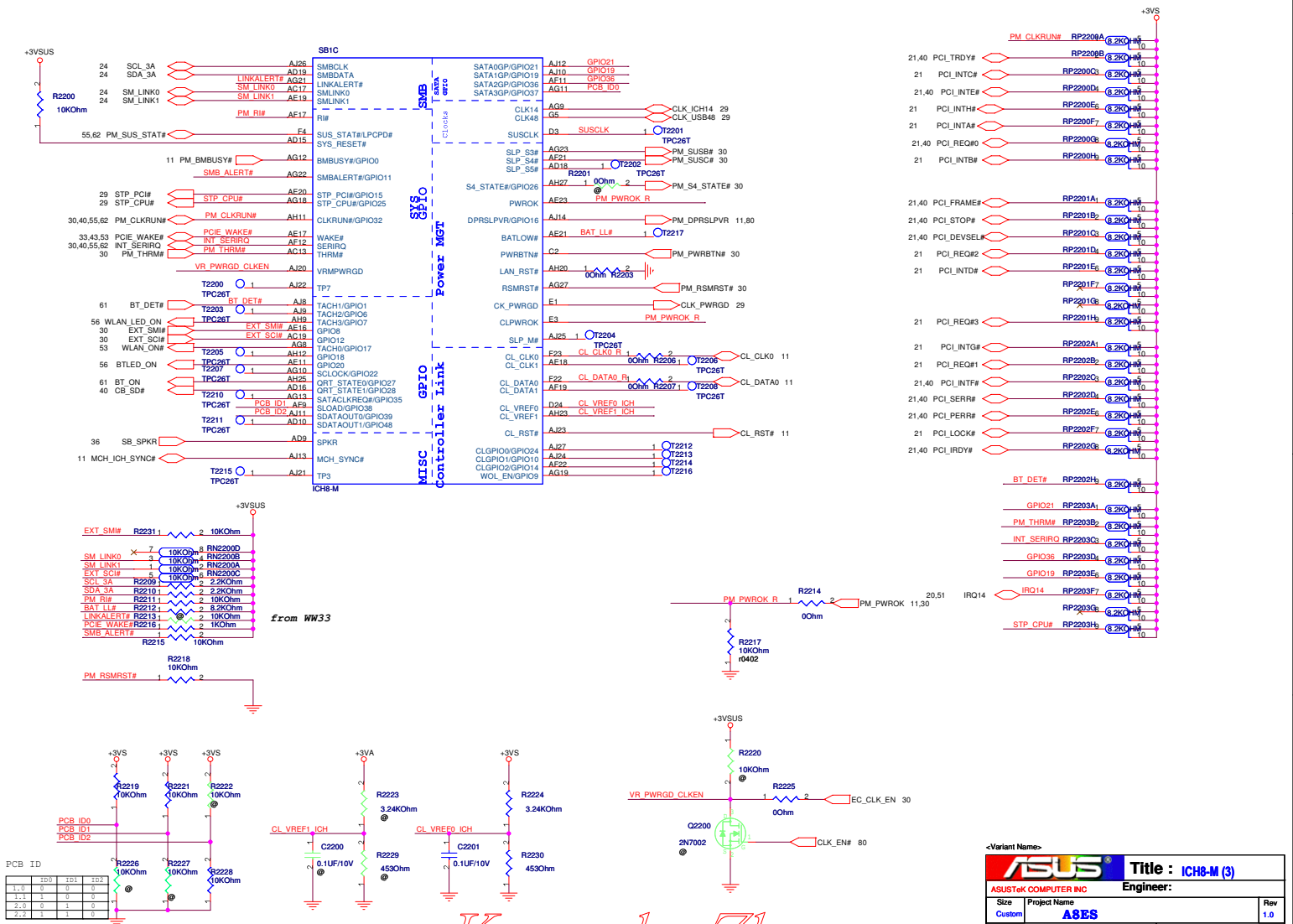


ICH8 Boot BIOS select

	INT#0	SPI_CS#1	(default)
LPC	1	1	1
PC2	1	1	0
SPT	0	0	1

ASUS Logo  
ASUSTeK COMPUTER INC  
Project Name: ICH8-M (2)  
Engineer:  
Date: 08-21-2007  
Sheet 21 of 94

« Kennedy\_Zhang »



<Variant Name>

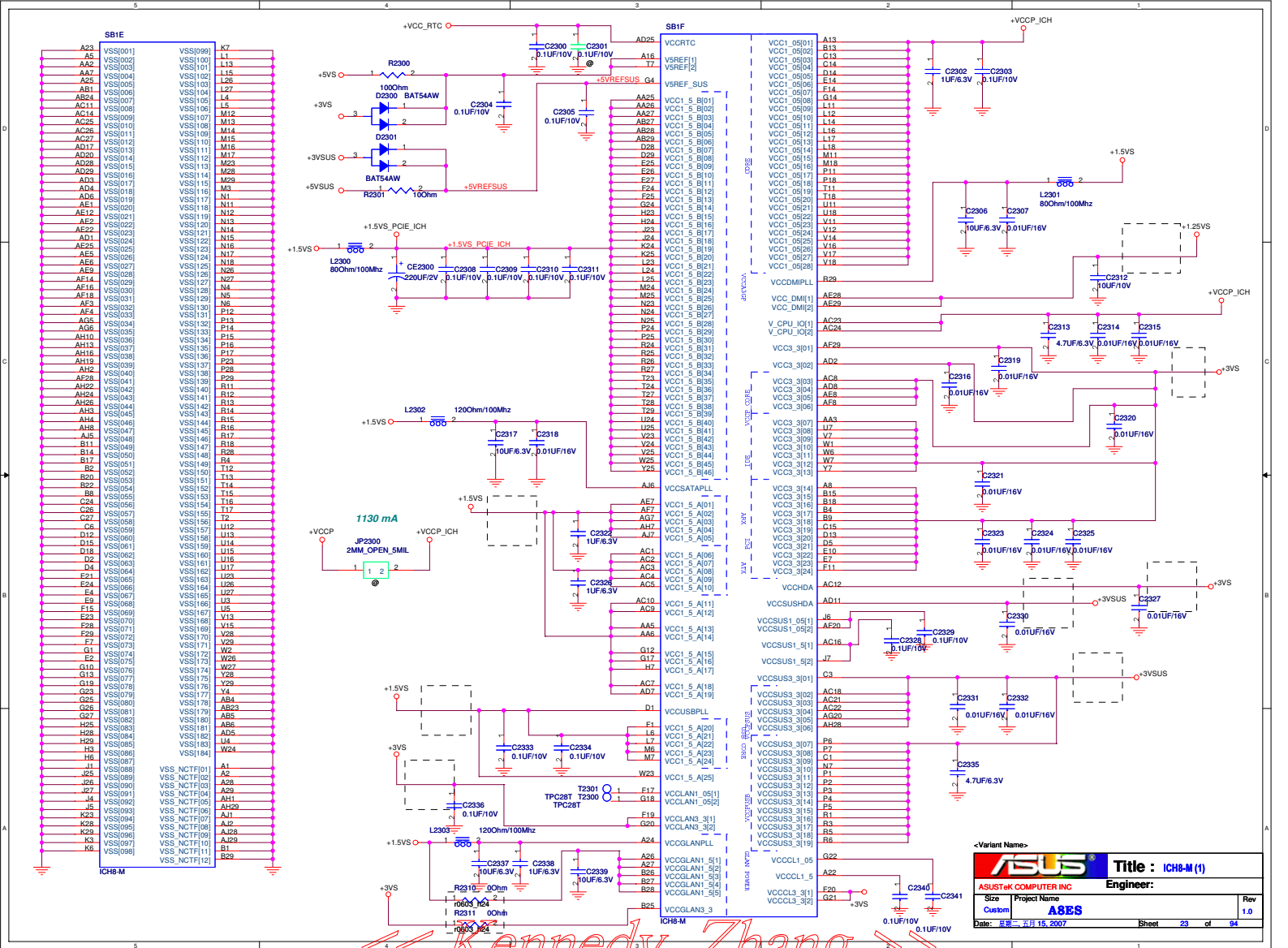
**ASUS** Title : ICH8-M (3)

ASUSTek COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	ABES	1.0

Date: 2007-07-21 21:00:00 Sheet 22 of 94

<< Kennedy\_Zhang >>



Kennedy\_Zhang

<b>ASUS</b>		<b>Title : ICH-M (1)</b>	
ASUSTeK COMPUTER INC		Engineer:	
Site:	Project Name:		
Custom:	ASUS		
Date: 08月15, 2007	Sheet 23 of 94		

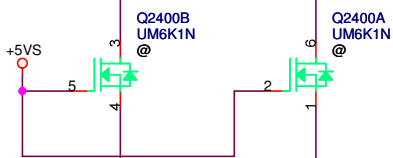
Check

Connect SMLINK and SMBUS for SMBus 2.0 compliance.

ICH8-M

22 SM\_LINK0

22 SM\_LINK1



ICH8-M

22 SCL\_3A

22 SDA\_3A

Q2401B UM6K1N

Q2401A UM6K1N

+5VS

+3VS

+3VS

R2400

R2401

4.7KOhm

4.7KOhm

SCL\_3S

SCL\_3S

7,8,29,43,53

SDA\_3S

SDA\_3S

7,8,29,43,53

<Variant Name>

		<b>Title : BLOCK DIAGRAM</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name <b>ASES</b>		Rev 1.0
Date: 星期三, 五月 16, 2007		Sheet 24 of 94	

« Kennedy Zhang »


Name	HW Pin Definition	Type	Tolerance	Power We	Default	Mux	Native Name	Real Name	Note
GPIO0	PM_BMBUSY#	I/O	3.3V	Core	GPI	Yes	BMBUSY	PM_BMBUSY#	
GPIO1	BT_DET#	I/O	3.3V	Core	GPI	No			
GPIO2	PCI_INTE#	I/O	5V	Core	GPI	Yes	PIRQE#	PCI_INTE#	
GPIO3	PCI_INTF#	I/O	5V	Core	GPI	Yes	PIRQF#	PCI_INTF#	
GPIO4	PCI_INTG#	I/O	5V	Core	GPI	Yes	PIRQG#	PCI_INTG#	
GPIO5	PCI_INTH#	I/O	5V	Core	GPI	Yes	PIRQH#	PCI_INTH#	
GPIO6	BIOS_REC	I/O	3.3V	Core	GPI	No			
GPIO7	WLAN_LED_ON	I/O	3.3V	Core	GPI	No			
GPIO8	EXT_SM#	I/O	3.3V	Resume	GPI	No			
GPIO9	LAN_WOL_EN	I/O	3.3V	Resume	GPI	Yes	WOL_EN		
GPIO10	ME_ALERT#	I/O	3.3V	Resume	GPI	Yes	CLGPIO1		
GPIO11		I/O	3.3V	Resume	Native	Yes	SMBALERT#	pull high +3VSUS	
GPIO12	EXT_SC#	I/O	3.3V	Resume	GPI	No			
GPIO13	ODD_DET	I/O	3.3V	Resume	Native	Yes	GLAN_DOCK#		removing from EC
GPIO14	NETDETECT	I/O	3.3V	Resume	GPI	Yes	CLGPIO2		
GPIO15	STP_PC#	I/O	3.3V	Resume	Native	No	STP_PC#	STP_PC#	
GPIO16	PM_DPRSLPVR	I/O	3.3V	Core	Native	Yes	DPRSLPVR	PM_DPRSLPVR	
GPIO17	WLAN_ON#	I/O	3.3V	Core	GPI	No			
GPIO18		I/O	3.3V	Core	GPO	No			
GPIO19		I/O	3.3V	Core	GPI	Yes	SATA1GP		
GPIO20	BTLED_ON	I/O	3.3V	Core	GPO	No			
GPIO21		I/O	3.3V	Core	GPI	Yes	SATA0GP		
GPIO22		I/O	3.3V	Core	GPI	Yes	SCLOCK		
GPIO23		I/O	3.3V	Core	Native	Yes	LDRQ1#		
GPIO24	PS_CPPE#	I/O	3.3V	Resume	GPO	Yes	CLGPIO0		removing from EC; note by Alan
GPIO25	STP_CPU#	I/O	3.3V	Resume	Native	No	STP_CPU#	STP_CPU#	
GPIO26	PM_S4_STATE#	I/O	3.3V	Resume	Native	Yes	S4_STATE#		
GPIO27	BT_ON# BT_ON	I/O	3.3V	Resume	GPO	Yes	QRT_STATE0		
GPIO28	CB_SD#	I/O	3.3V	Resume	GPO	Yes	QRT_STATE1		Cardbus_Shutdown#
GPIO29	OC5#	I/O	3.3V	Resume	Native	Yes	OC5#		OC#
GPIO30	OC6#	I/O	3.3V	Resume	Native	Yes	OC6#		OC#
GPIO31	OC7#	I/O	3.3V	Resume	Native	Yes	OC7#		OC#
GPIO32	PM_CLKRUN#	I/O	3.3V	Core	Native	No	CLKRUN#	PM_CLKRUN#	
GPIO33		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_EN#		
GPIO34		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_RST#		
GPIO35	SATACLKREQ#	I/O	3.3V	Core	GPO	Yes	SATACLKREQ#		
GPIO36	EMAIL_LED#	I/O	3.3V	Core	GPI	Yes	SATA2GP		
GPIO37	PCB_ID0	I/O	3.3V	Core	GPI	Yes	SATA3GP		
GPIO38	PCB_ID1	I/O	3.3V	Core	GPI	Yes	SLOAD		
GPIO39	PCB_ID2	I/O	3.3V	Core	GPI	Yes	SATAOUT0		
GPIO40	OC4#	I/O	3.3V	Resume	Native	Yes	OC4#		OC#
GPIO41	OC3#	I/O	3.3V	Resume	Native	Yes	OC3#		OC#
GPIO42	OC2#	I/O	3.3V	Resume	Native	Yes	OC2#		OC#
GPIO43	OC1#	I/O	3.3V	Resume	Native	Yes	OC1#		OC#
GPIO44		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO45		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO46		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO47		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO48		I/O	3.3V	Core	GPI	Yes	SDATAOUT1		
GPIO49	H_PWRGD	I/O	V_CPU_IO	V_CPU_IO	Native	Yes	CPUPWRGD	H_PWRGD	
GPIO50	PCI_REQ1#	I/O	5.5V	Core	Native	Yes	REQ1#		
GPIO51	PCI_GNT1#	I/O	3.3V	Core	Native	Yes	GNT1#		
GPIO52	PCI_REQ2#	I/O	5.5V	Core	Native	Yes	REQ2#		
GPIO53	PCI_GNT2#	I/O	3.3V	Core	Native	Yes	GNT2#		
GPIO54		I/O	5.5V	Core	Native	Yes	REQ3#		reserved for GPIO
GPIO55		I/O	3.3V	Core	Native	Yes	GNT3#		reserved for GPIO

← Kennedy\_Zhang →


Title : BLANK

ASUSTeK COMPUTER INC  
Engineer:


Rev	0
Project Name	A8ES
Size	A
Date: 星期三, 十月 11, 2006	Sheet 25 of 94

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name ASES	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 26 of 94

*← Kennedy\_Zhang →*

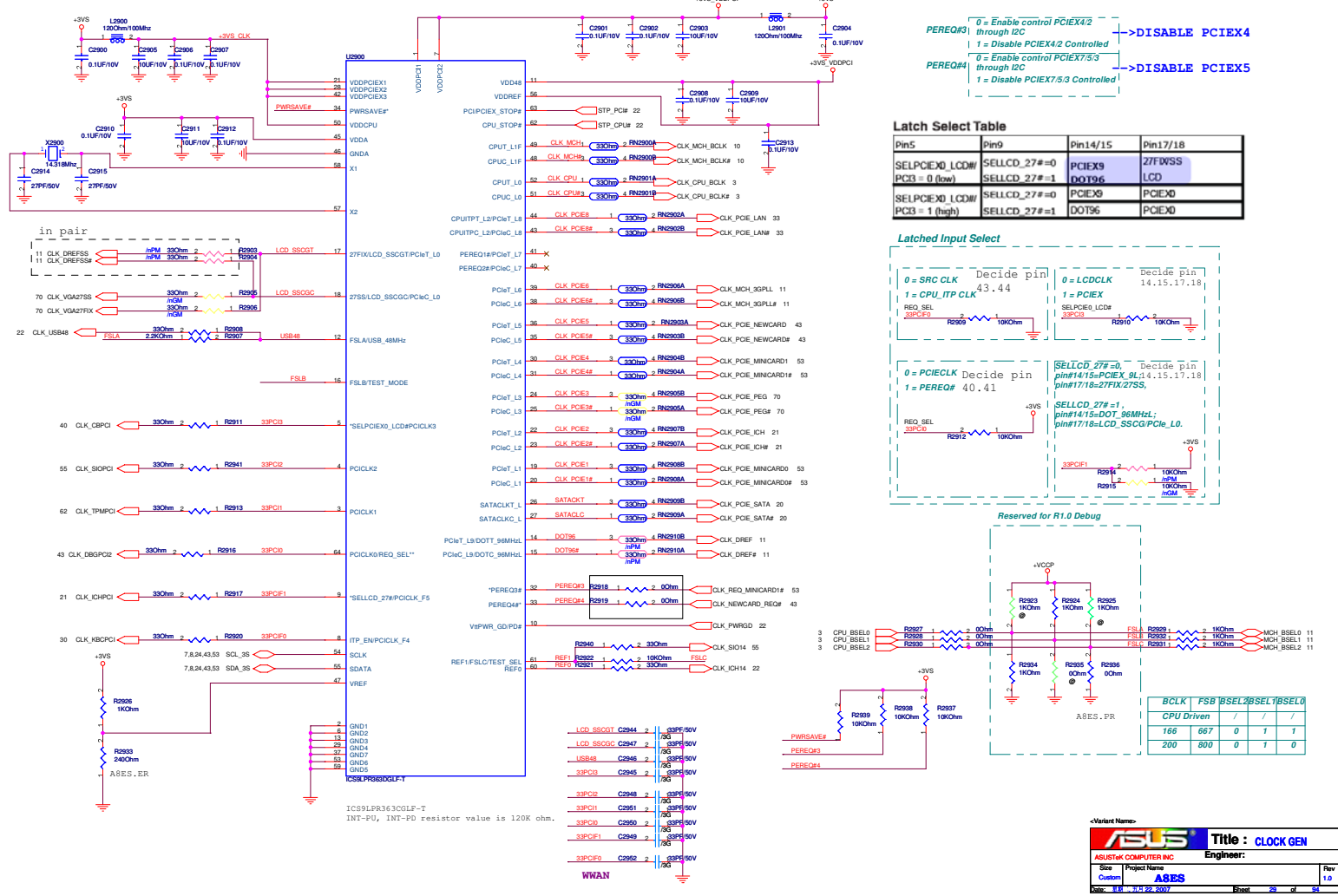
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ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8ES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet 27 of 94	

*← Kennedy\_Zhang →*

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name ASES	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 28 of 94

*← Kennedy\_Zhang →*



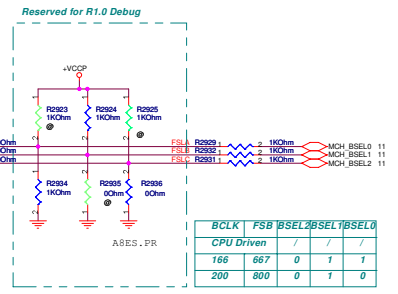
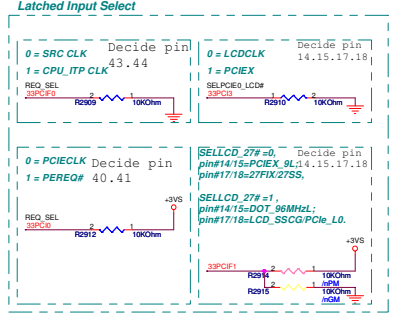


PEREQ#3 0 = Enable control PCIe4/2 through I2C  
1 = Disable PCIe4/2 Controlled  
PEREQ#4 0 = Enable control PCIe7/5/3 through I2C  
1 = Disable PCIe7/5/3 Controlled

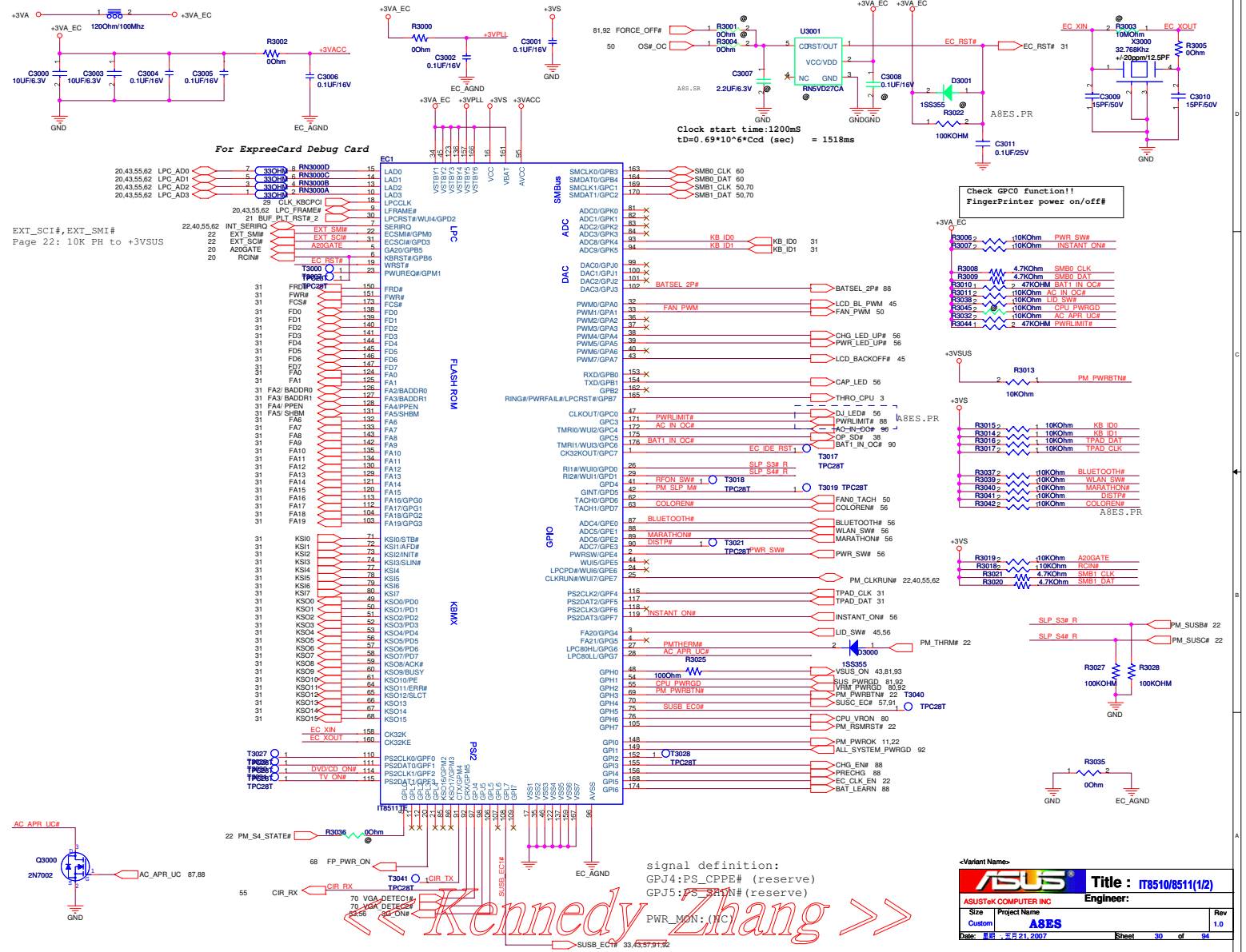
->DISABLE PCIe4  
->DISABLE PCIe5

**Latch Select Table**

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE#0_LCD#	SELCD_27#=#0	PCIE#9	27FDVSS
PC#3 = 0 (low)	SELCD_27#=#1	DOT#9	LCD
SELPCIE#0_LCD#	SELCD_27#=#0	PCIE#9	PCIE#0
PC#3 = 1 (high)	SELCD_27#=#1	DOT#6	PCIE#0



<< Kennedy\_Zhang >>

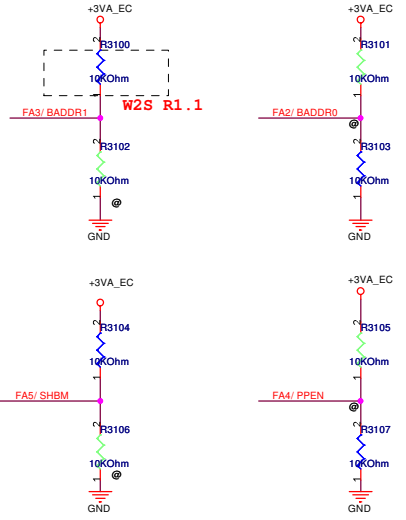


DVD/CD ON# DVD/CD ON#

*Kennedy Zhang*

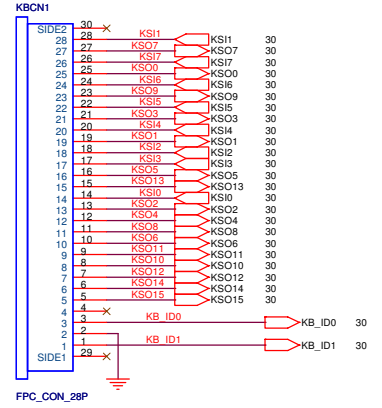
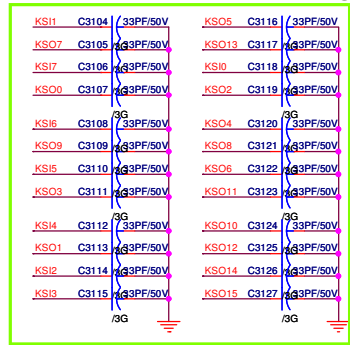
**ASUS** Title : IT8510/8511(12)  
ASUSTek COMPUTER INC Engineer:  
Size Project Name Rev  
Custom A8ES 1.0  
Date: 2007.05.21, 2007 Sheet 30 of 94

10:Determined by EC



BADDR[1:0]  
No pull up:  
The register pair to access PNPCFG is 002Eh and 002Fh  
Ext 10K up on BADDR0:  
The register pair to access PNPCFG is 004Eh and 004Fh  
Ext 10K up on BADDR1:  
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

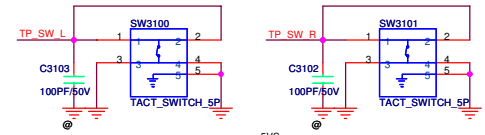
KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP



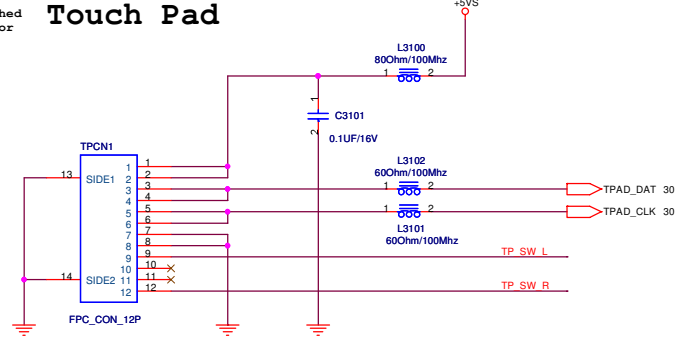
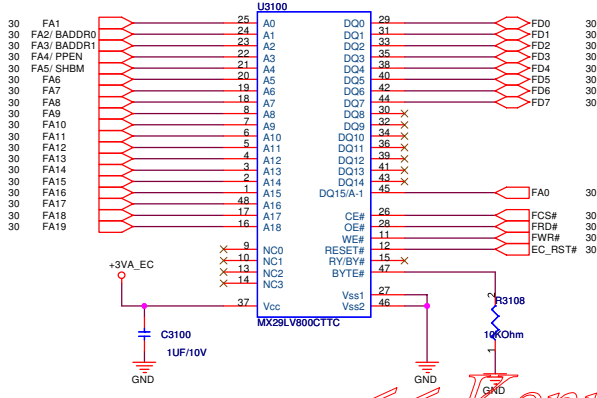
SHBM  
No pull up:  
disable shared memory with host BIOS  
Ext 10K up:  
enable shared memory with host BIOS

PPEN  
No pull up:  
Normal  
Ext 10K up:  
KBS interface pins are switched to parallel port interface for in-system programming.

Touch Pad




8M TSOP



<Variant Name>

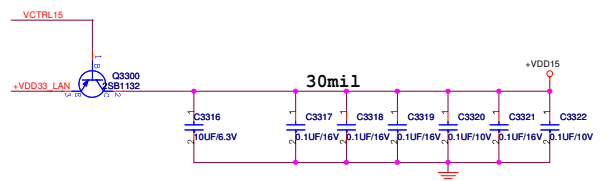
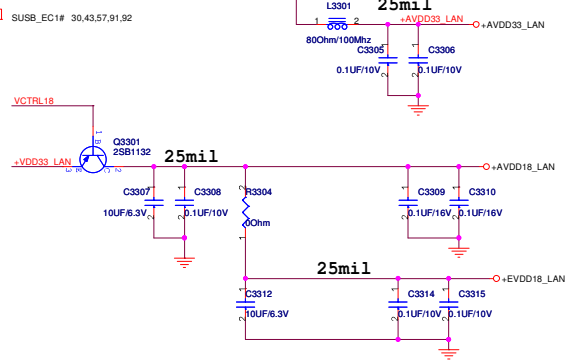
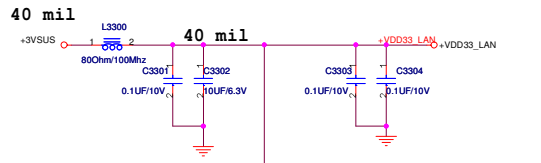
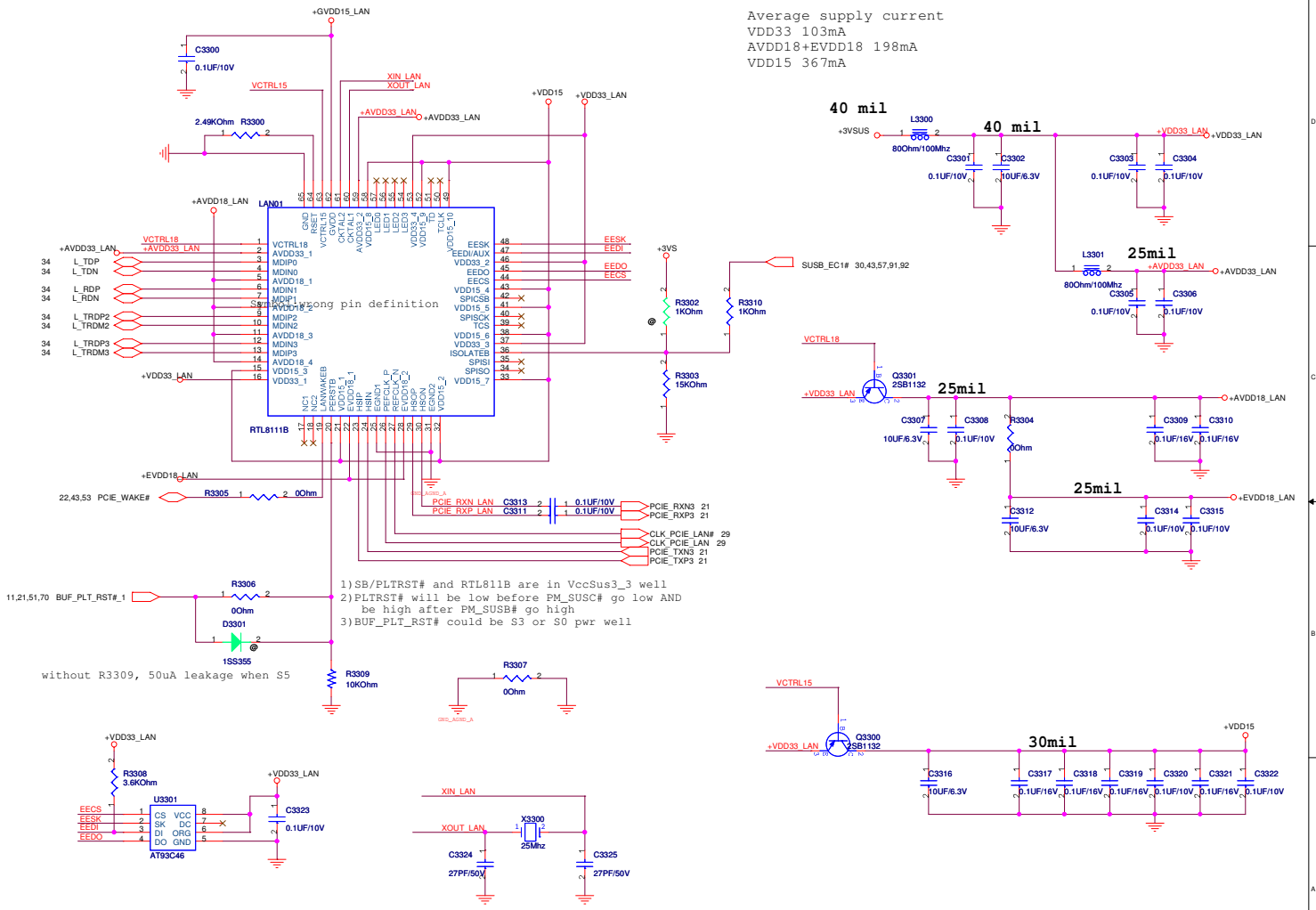
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ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABES	1.0	
Date: 星期五, 五月 16, 2007	Sheet	31	of 94

« Kennedy\_Zhang »

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>ASES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet 32 of 94	

*← Kennedy\_Zhang →*

Average supply current  
 VDD33 103mA  
 AVDD18+EVDD18 198mA  
 VDD15 367mA

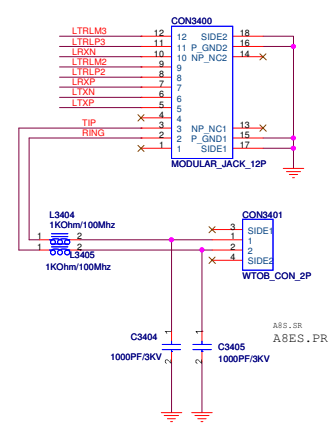
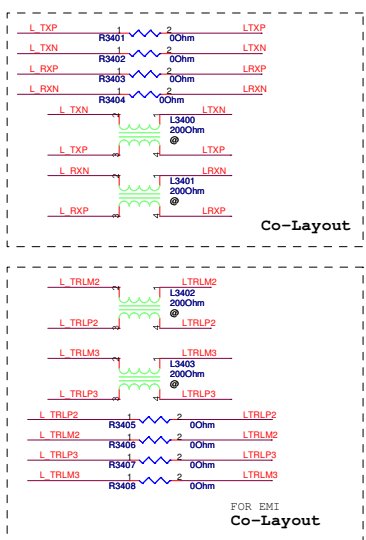
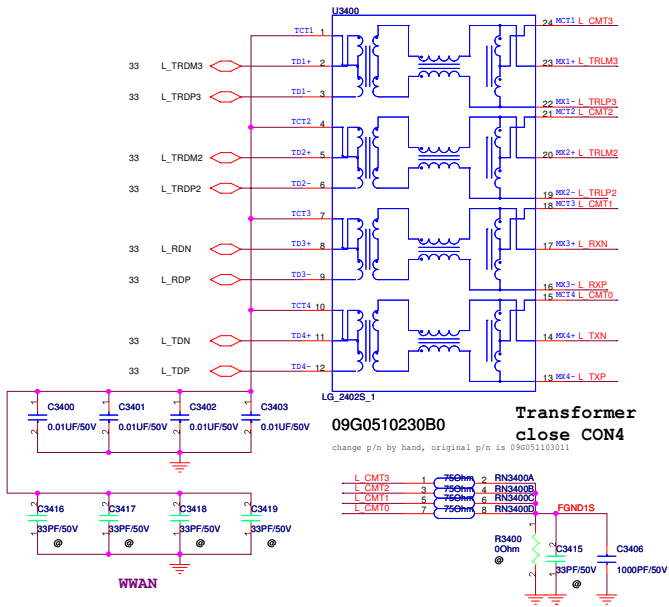


<Variant Name>

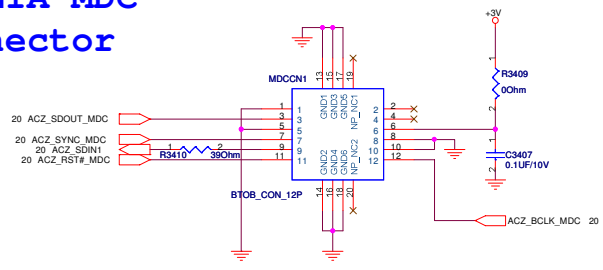
<b>ASUS</b>		<b>Title : GigalAN</b>	
ASUSTek COMPUTER INC	Project Name	Engineer:	Rev
Custom	ABES		1.0
Date: 2007.08.21	Sheet 33	of 84	

<< Kennedy\_Zhang >>

2402S have issue after IR reflow,  
alternative part:LG-2410S-1




### AZALIA MDC Connector



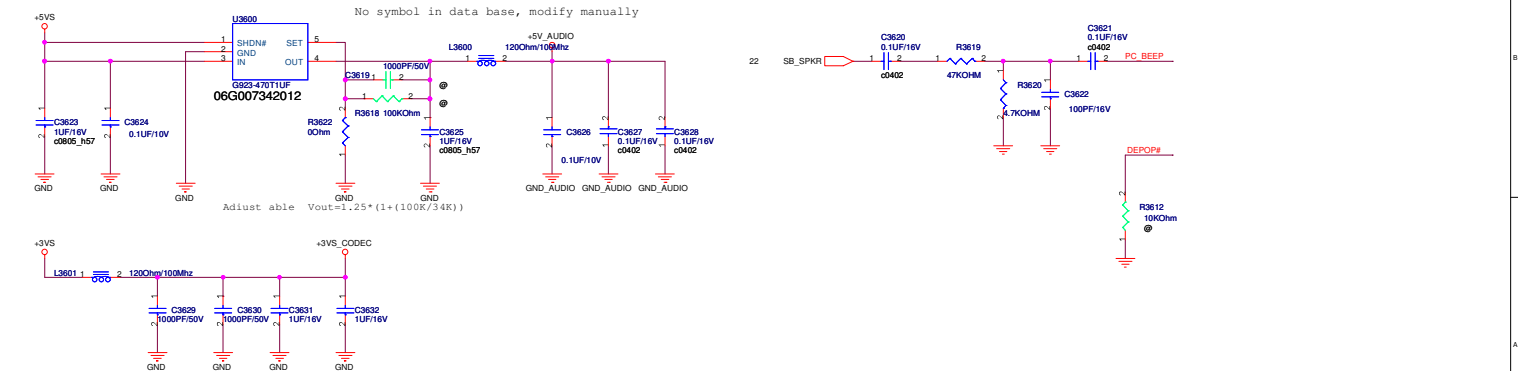
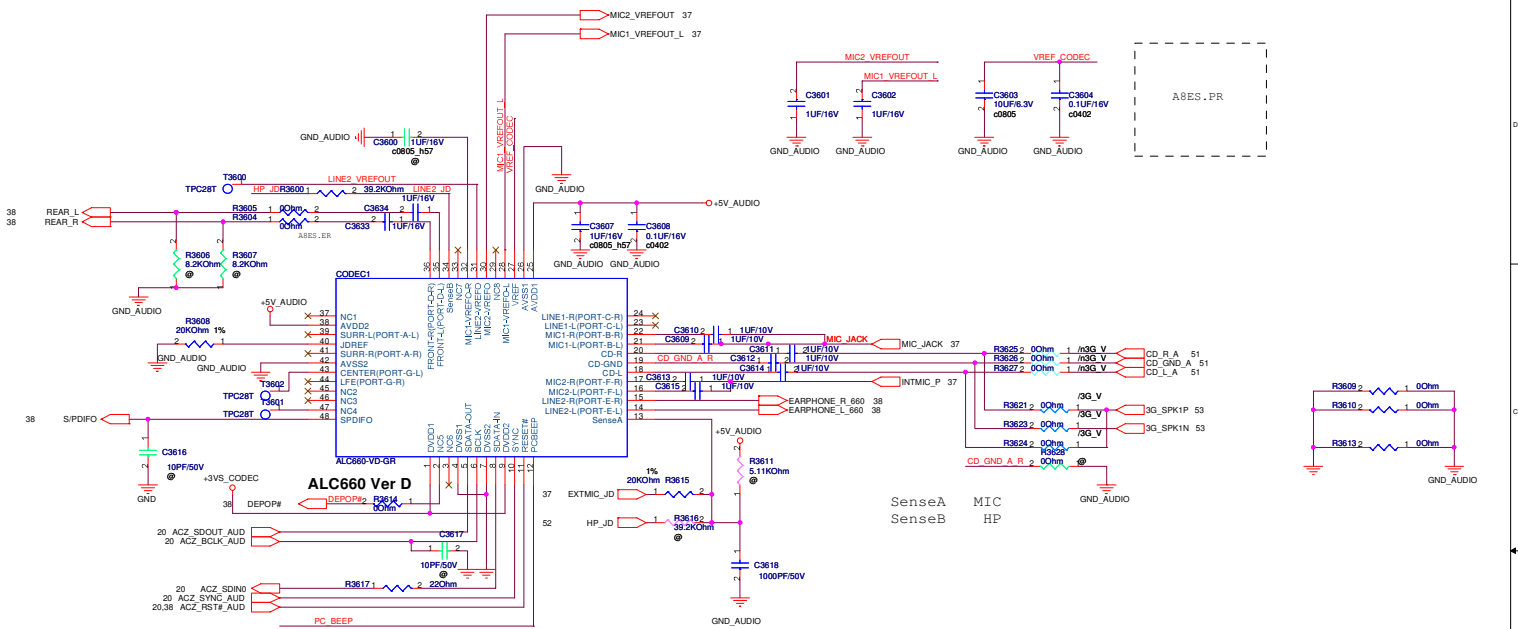
<Variant Name>

<b>ASUS</b>		<b>Title : RJ11+45, MDC</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 08-11-2007	Sheet 34	of 94	

« Kennedy\_Zhang »

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8ES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet	35 of 94

*← Kennedy\_Zhang →*

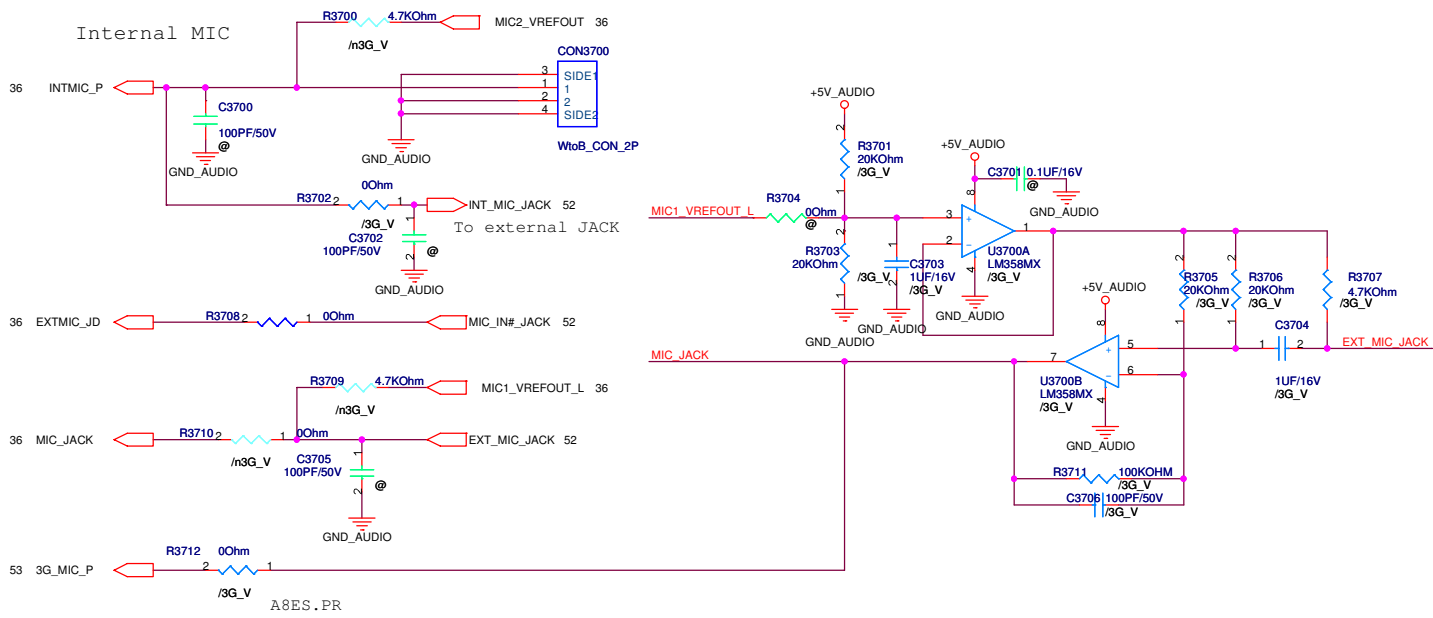


-Variant Names-

<b>ASUS</b>		<b>Title : CODEC-ALC660</b>	
ASUSTAK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	<b>ABES</b>	1.0	
Date: JUN 24, 2007		Sheet	38 of 84

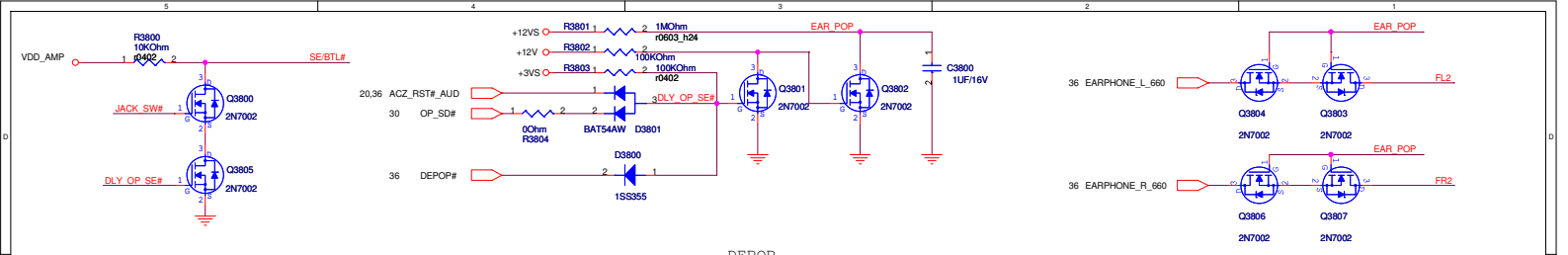
« Kennedy\_Zhang »



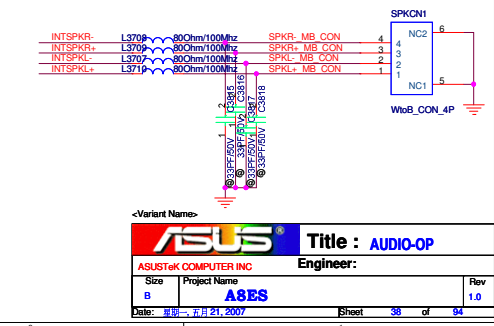
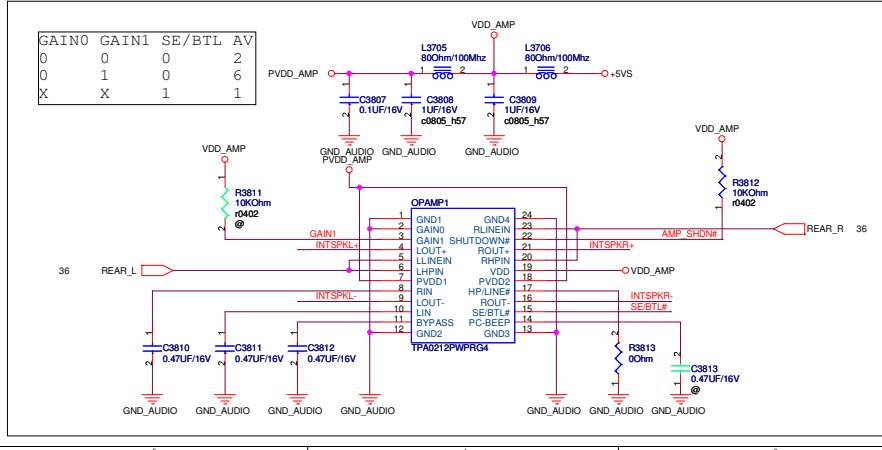
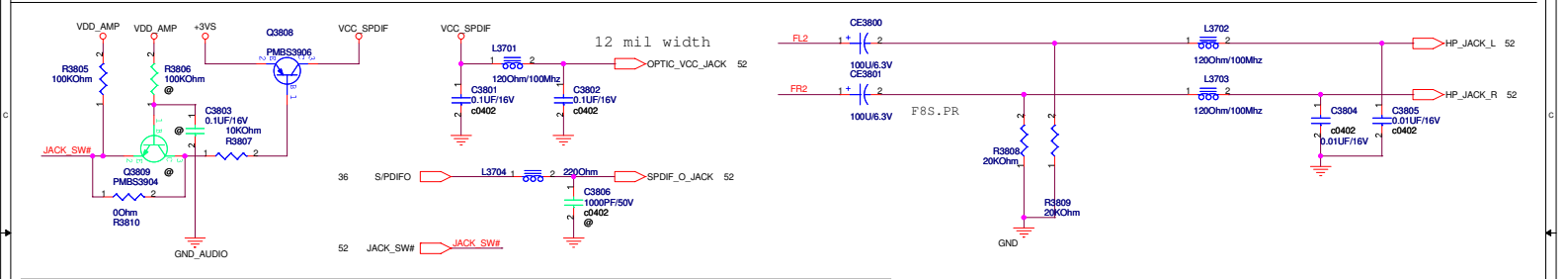


<b>ASUS</b>		<b>Title : AUDIO-MIC</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	<b>ASES</b>	1.0	
Date: 星期一, 五月 21, 2007		Sheet 37 of 94	

*<< Kennedy\_Zhang >>*



DEPOP



<Variant Name>


**ASUS** Title : **AUDIO-OP**

ASUSTek COMPUTER INC Engineer:

Size	Project Name	Rev
B	A8ES	1.0

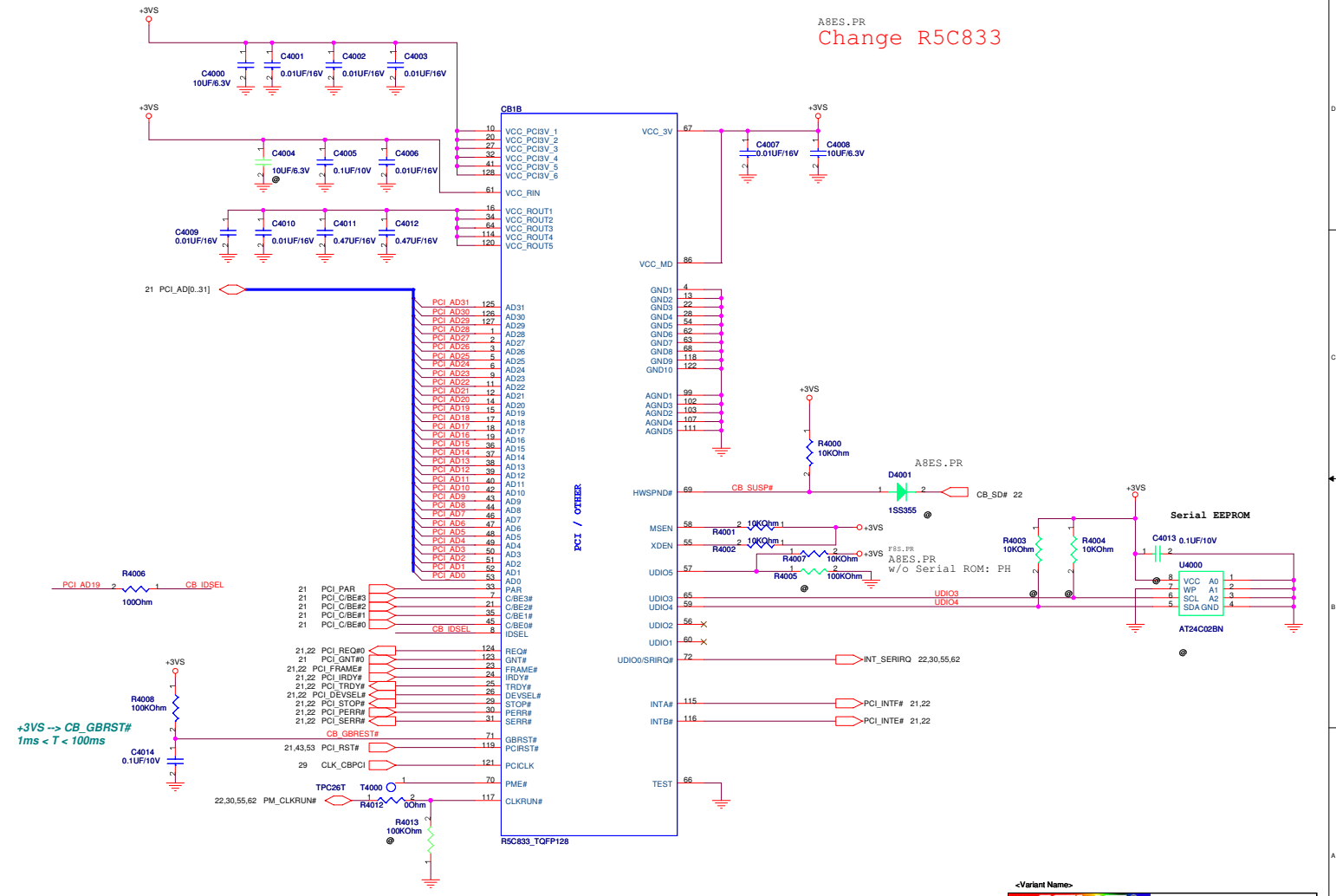
Date: 2007.07.21, 2007 Sheet 38 of 84

<< Kennedy\_Zhang >>

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>ASES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet	39 of 94

*← Kennedy\_Zhang →*

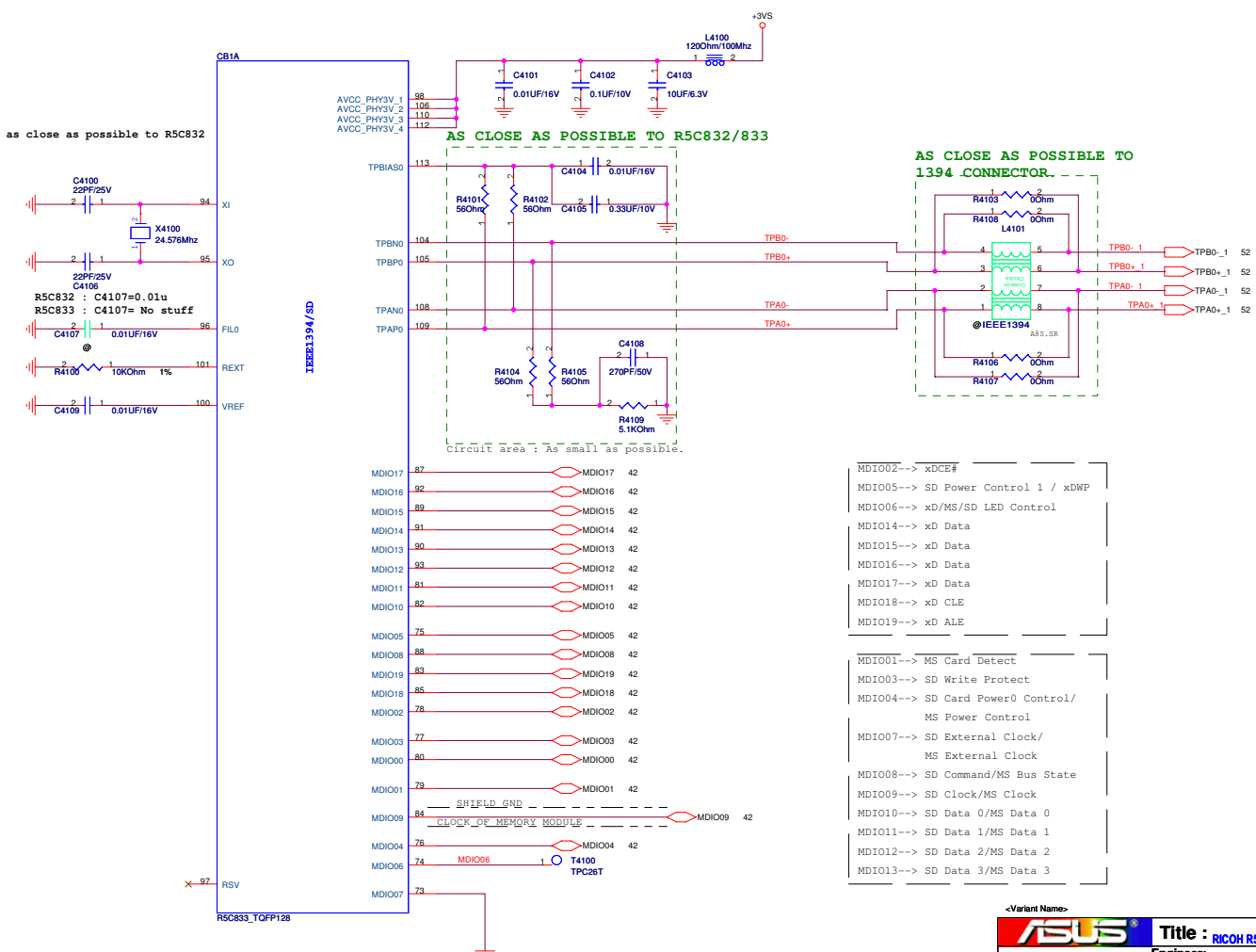
ABES.PR  
Change R5C833



<Variant Name>

<b>ASUS</b>		<b>Title : RICOH R5C832/PCI B</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	ABES		1.0
Date: 8/21/2007		Sheet	40 of 94

<< Kennedy\_Zhang >>

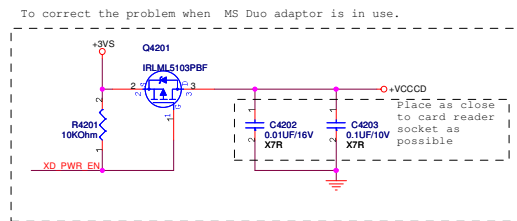
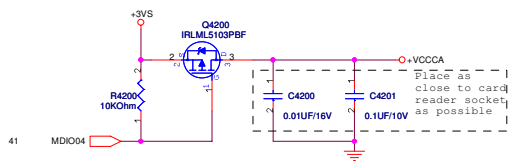


« Kennedy\_Zhang »

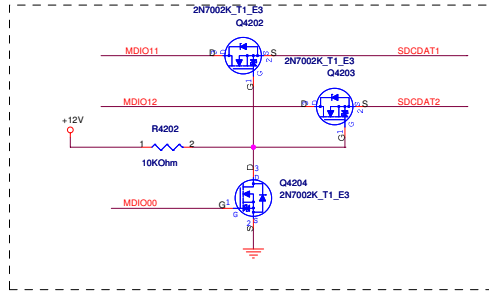
<Variant Name>

**ASUS** Title : RICOH R5C832/PCI A  
ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	ABES	1.0
Date: 2007.08.21	Sheet 41 of 94	



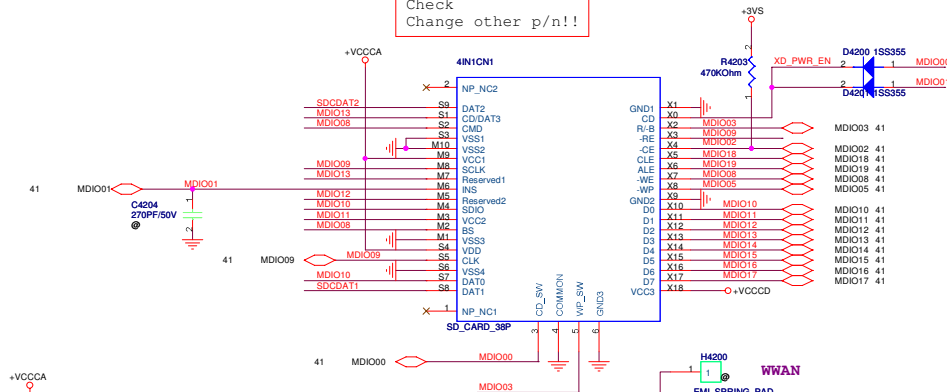
**Solve MS Duo Adaptor short issue.**



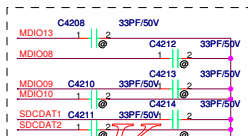
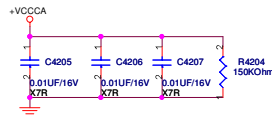
ABES.PR  
Change to 07G005000214, 2KV ESD

- MDIO00--> SD Card Detect
- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/MS Power Control
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3

Check  
Change other p/n!!



- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE



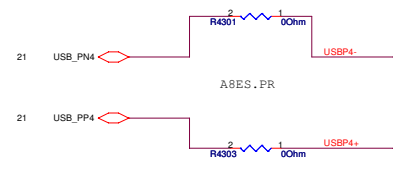
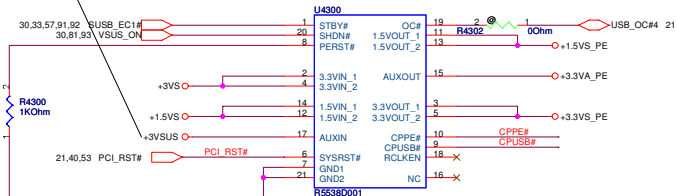
F8S.PR  
EMI Impact MS function

<Variant Name>

<b>ASUS</b>		<b>Title : CardReader</b>
ASUSTek COMPUTER INC		Engineer:
Size Custom	Project Name	Rev 1.0
Date: 11/06/2007	Sheet 42 of 94	

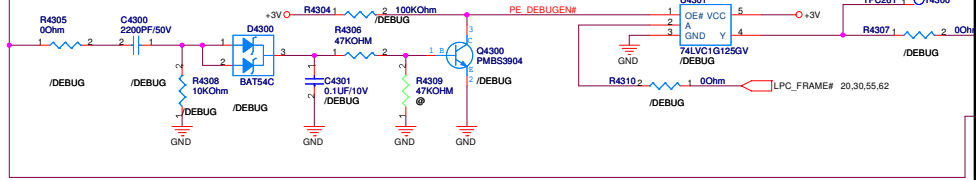
« Kennedy\_Zhang »

Check +3V

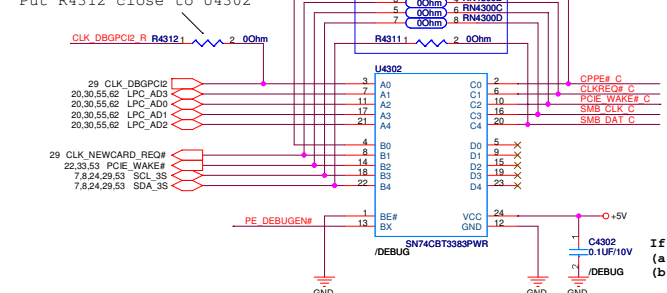


A8ES.PR  
Delete NewCars/LPC

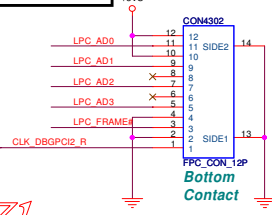
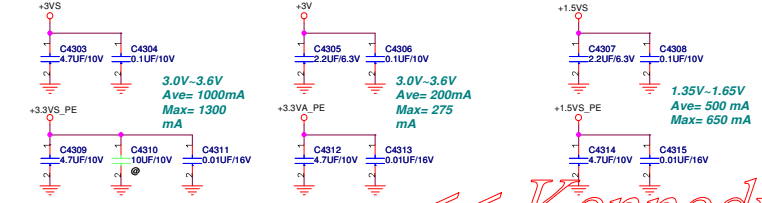
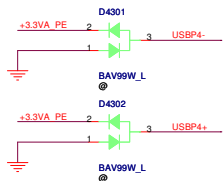
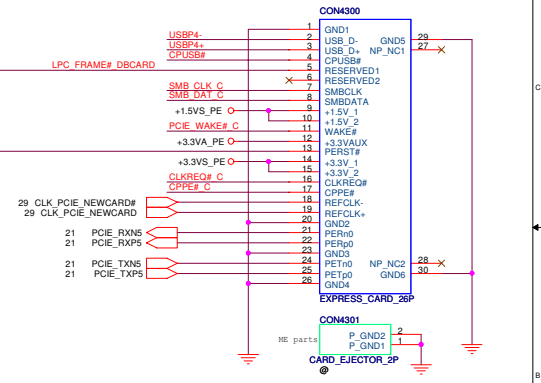
### Block A



### Block C



If don't support NewCard Debug Card, Pls do  
 (a) DNI all components of block A  
 (b) Mount Block C (RNS401, R6975)



ASUS		Title : Express Card	
ASUSTek COMPUTER INC	Project Name	Engineer:	Rev 1.0
Customer: A8ES			
Date: 8/8/2007	Sheet 43	of 94	

« Kennedy\_Zhang »

D

D

C


C

B

B

A

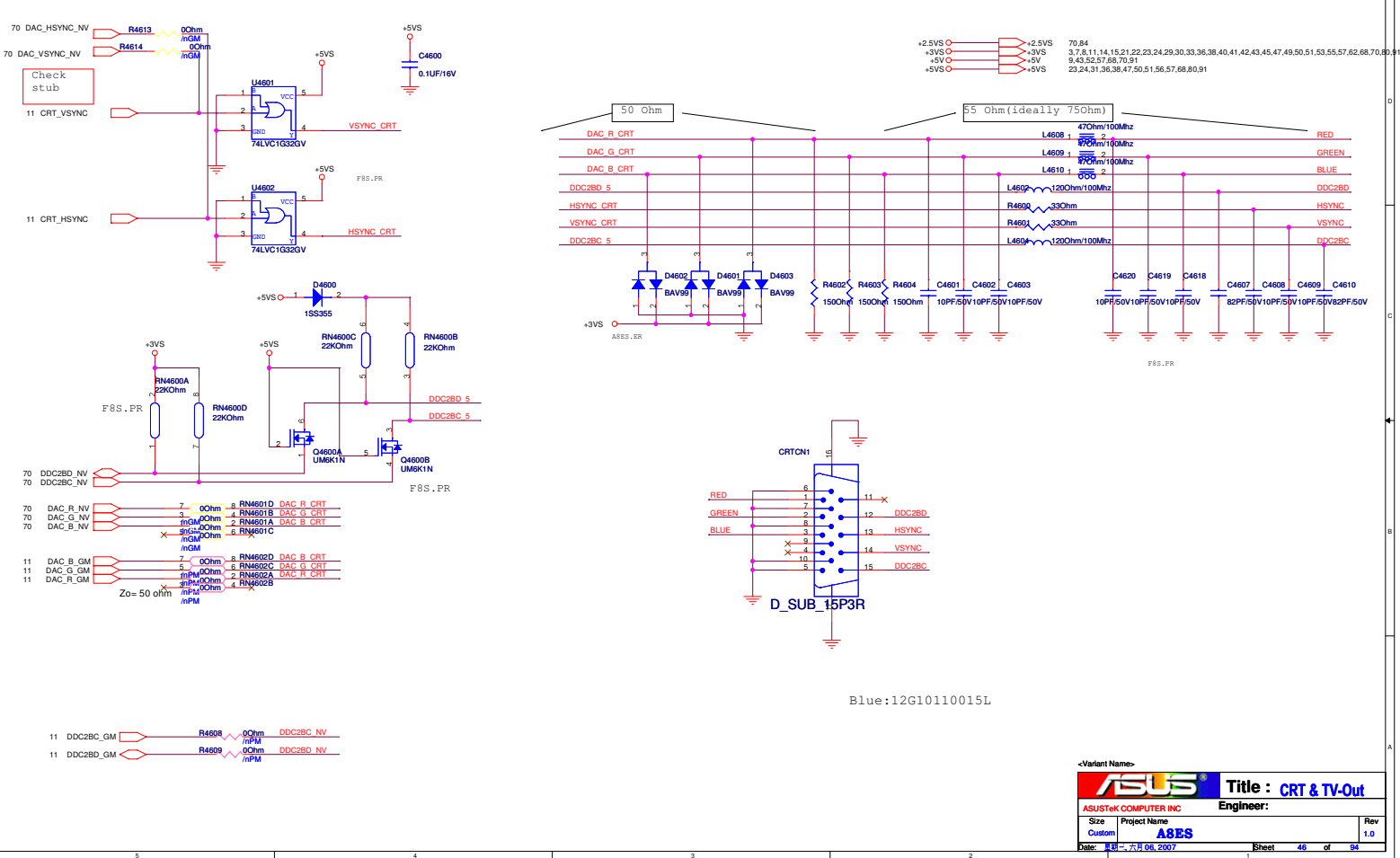
A

		<b>Title : Blank</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>A8ES</b>	1.0
Date: 星期二十月 31, 2006		Sheet 44 of 94

« Kennedy\_Zhang »

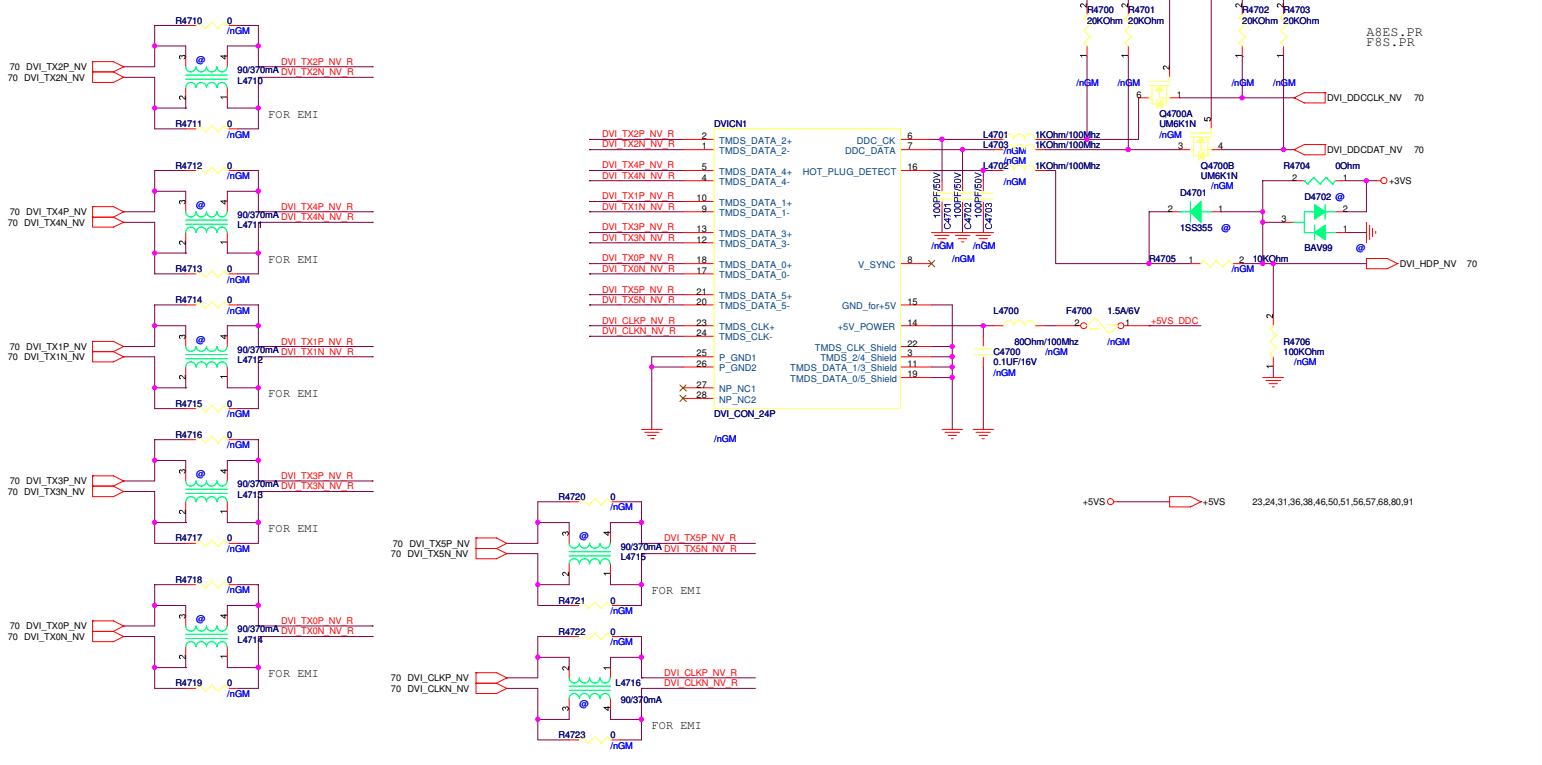






<< Kennedy\_Zhang >>

ASUS  
 ASUSTEK COMPUTER INC  
 Project Name: ASES  
 Title: CRT & TV-Out  
 Engineer:  
 Size: Custom  
 Date: 08-27-06, 2007  
 Sheet: 46 of 94  
 Rev: 1.0



<b>ASUS</b>		<b>Title : DVI</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name	Rev	
	<b>ABES</b>	1.0	
Date: 2007.07.24		Sheet 47 of 94	

<< Kennedy\_Zhang >>

D

D

C


C

B

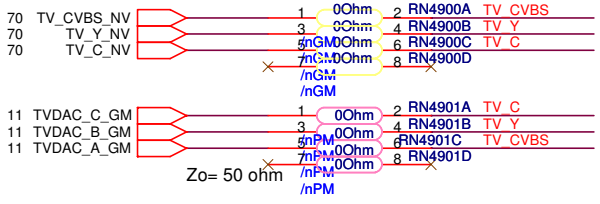
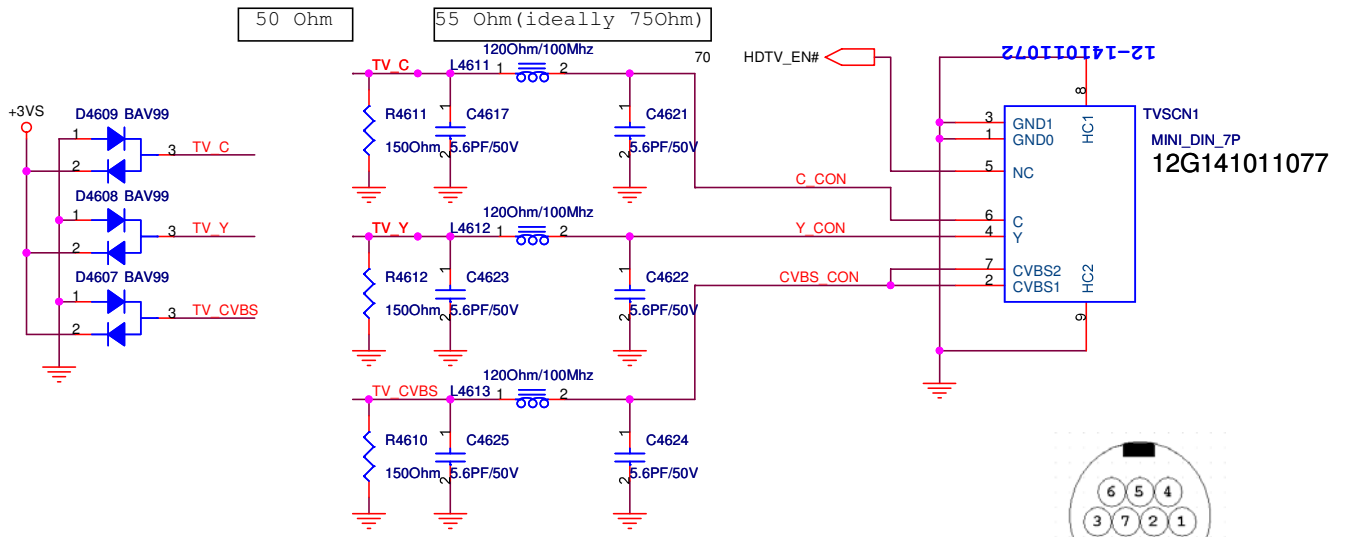
B

A

A

		<b>Title : BLANK</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>ASES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 48 of 94

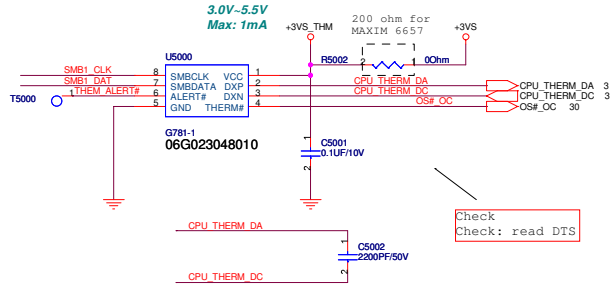
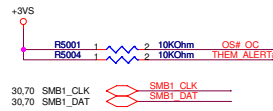
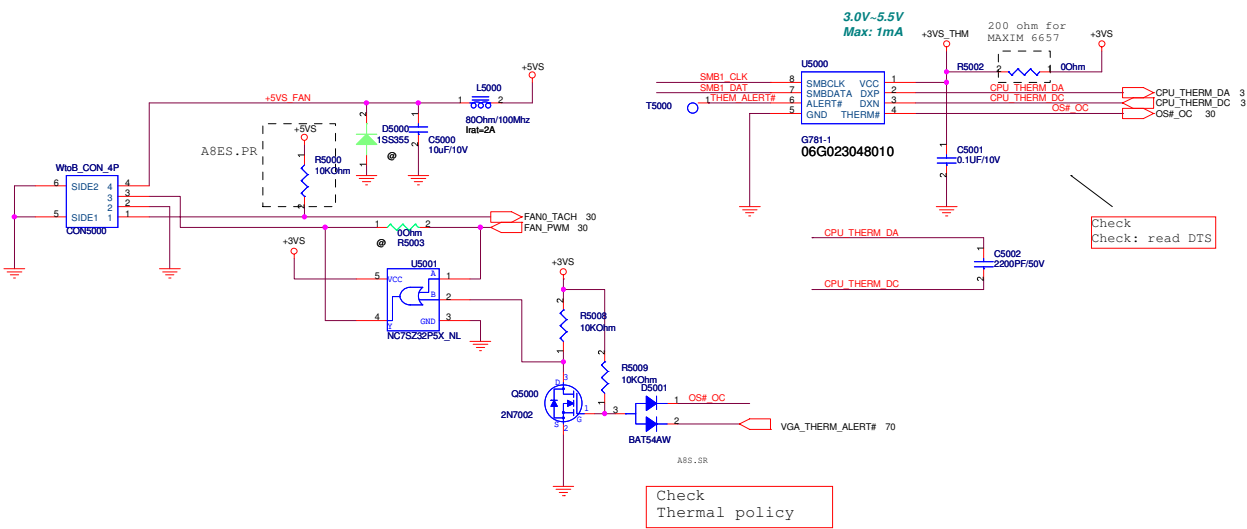
← Kennedy\_Zhang →



<b>ASUS</b>		<b>Title : TV</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name <b>A8ES</b>	Rev 1.0	
Date: 星期二 五月 21, 2007		Sheet 49 of 94	

« Kennedy\_Zhang »

# FAN & THERMAL CONTROLLER



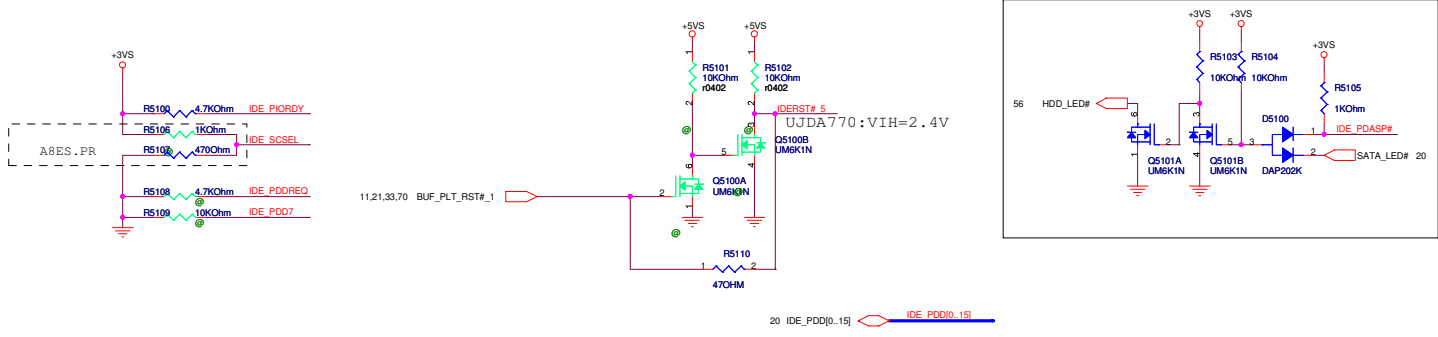
Check  
Check: read DIS

G781-1 (0x9A)  
06G023048010  
G781 (0x98)  
06G023048011

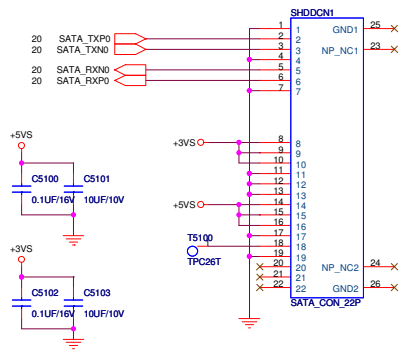
Check  
Thermal policy

ASUS		Title : FAN & THERMAL	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name ABES	Rev 1.0	
Date: 2007.7.21	Sheet 50	of 94	

<< Kennedy\_Zhang >>



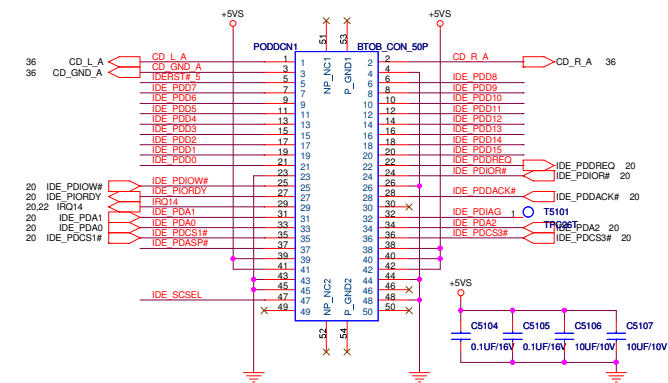
**SATA HDD CON**



+3V5 +3V5  
 +5V5 +5V5  
 +5V +5V

3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,53,55,57,62,68,70,80,91,92  
 23,24,31,36,38,46,47,50,56,57,68,80,91  
 9,43,52,57,68,70,91

**PATA CD-ROM CON**

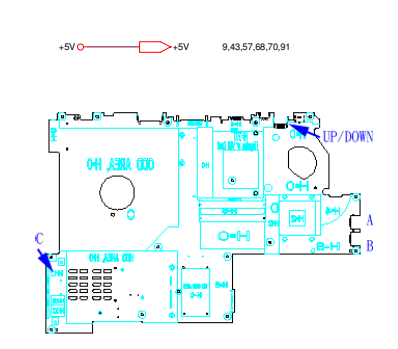
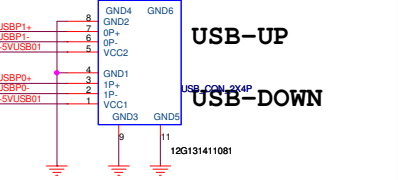
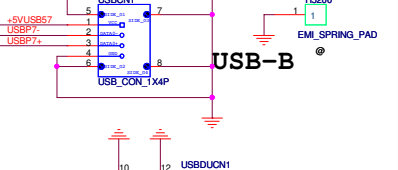
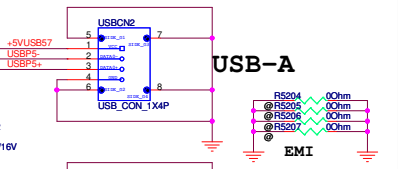
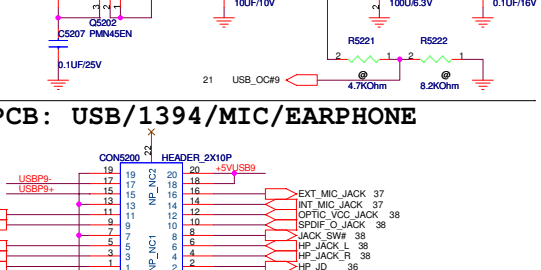
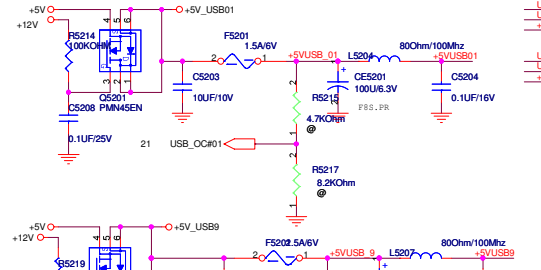
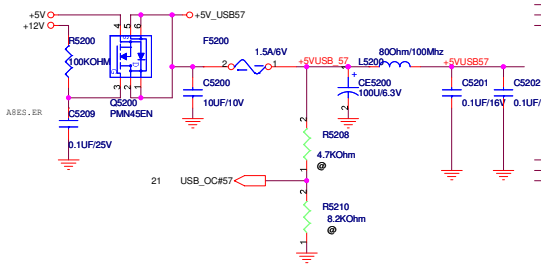
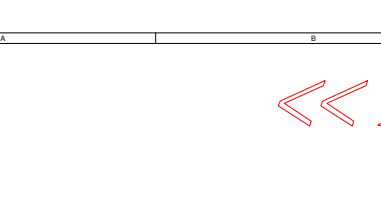
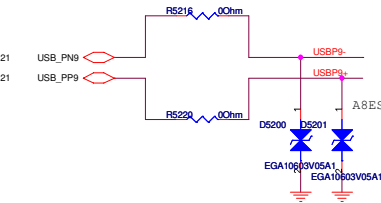
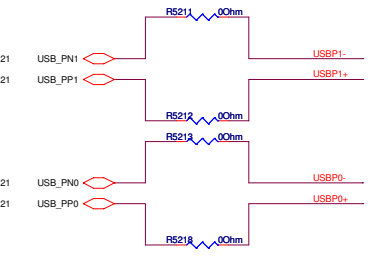
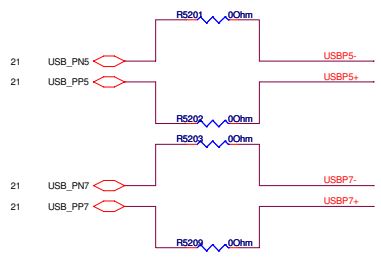


**ASUS** Title : HDD & ODD  
 ASUSTek COMPUTER INC Engineer:  
 Size Project Name Rev  
 B ASES 1.0  
 Date: 2007.7.21.2007 Sheet 51 of 94

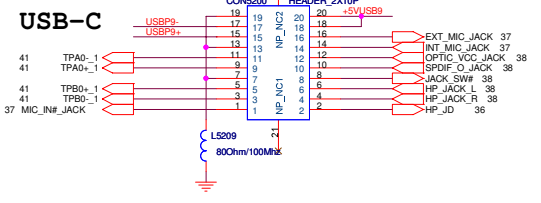
<< Kennedy\_Zhang >>

A8ES.PR  
Remove USB  
common  
choke  
co-layer

A8ES.PR EMI  
H5201  
EMI\_SPRING\_PAD



**SUB-PCB: USB/1394/MIC/EARPHONE**




<Variant Name>  
**ASUS** Title: USB/SUB PCB  
 ASUSTeK COMPUTER INC Engineer:  
 Size Project Name  
 Custom **ABES** Rev 1.0  
 Date: 2007.05.21.2007 Sheet 02 of 04

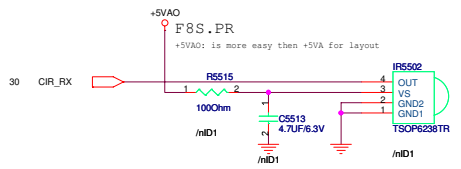
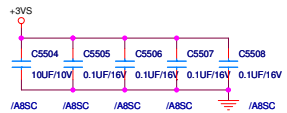
<< Kennedy\_Zhang >>



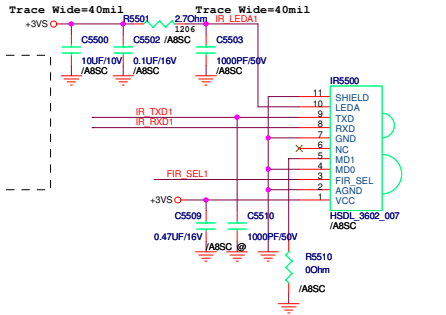
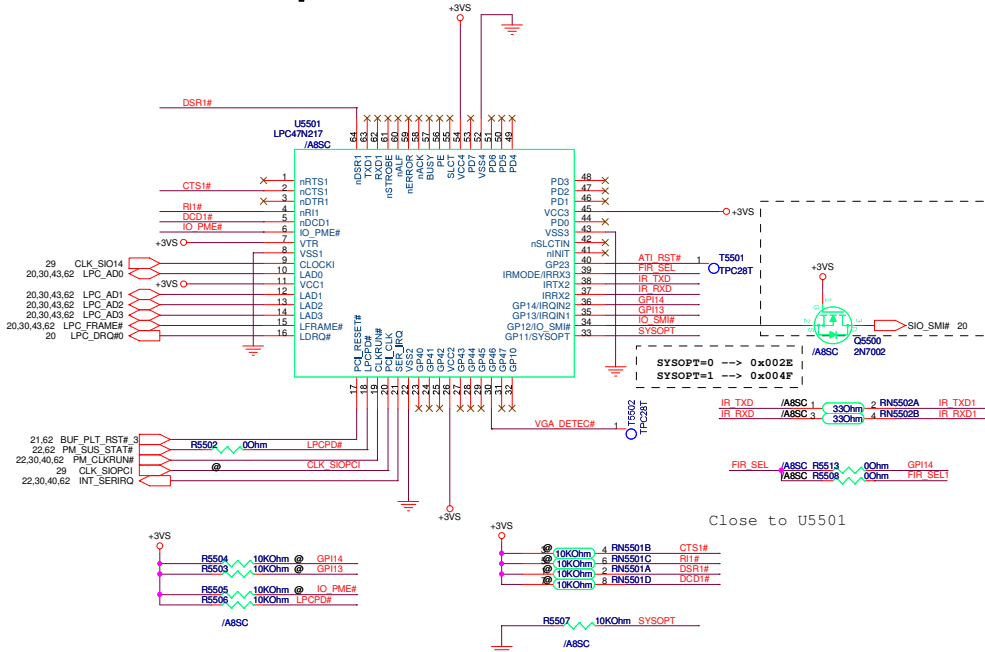


		<b>Title : BLANK</b>	
ASUSTEK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	<b>ABES</b>	0	
Date: 11月11, 2006		Sheet 54 of 94	

<< Kennedy\_Zhang >>



### Super I/O

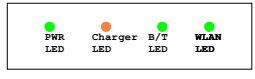
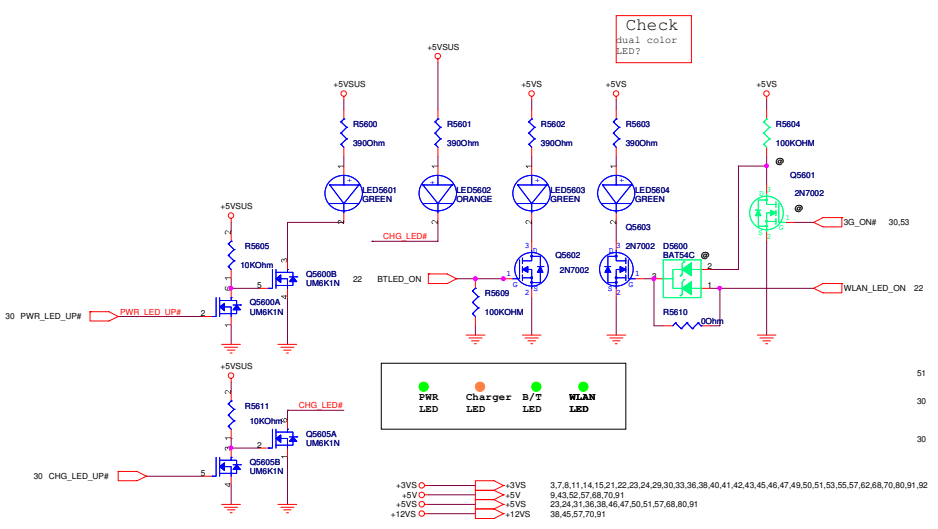
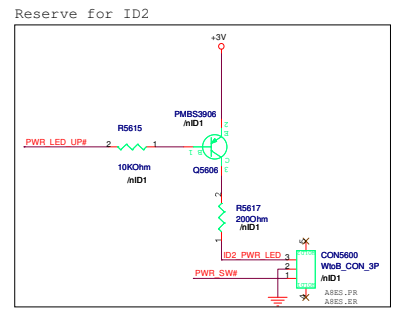
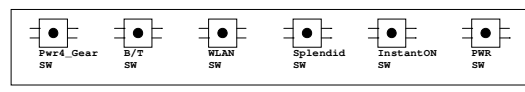
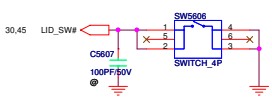
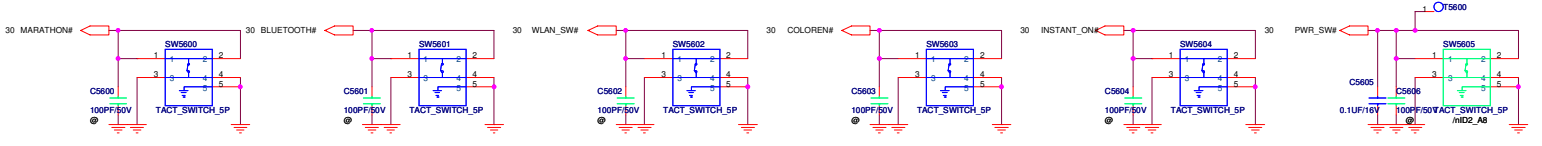


**Transceiver Control Truth Table**

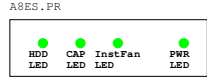
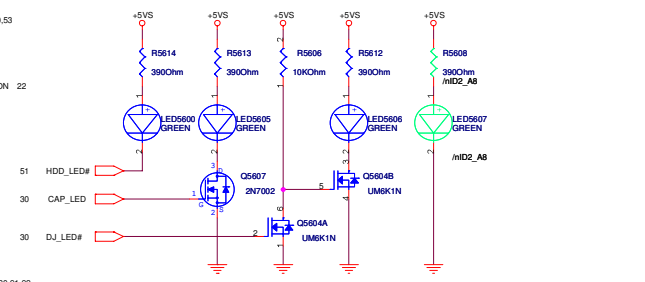
Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power

**ASUS** Title: **hDA**  
**ASUSTeK COMPUTER INC** Engineer:  
 Size: **B** Project Name: **A8ES** Rev: **2.0**  
 Date: **2007.07.21** Sheet: **65** of **94**

<< Kennedy\_Zhang >>

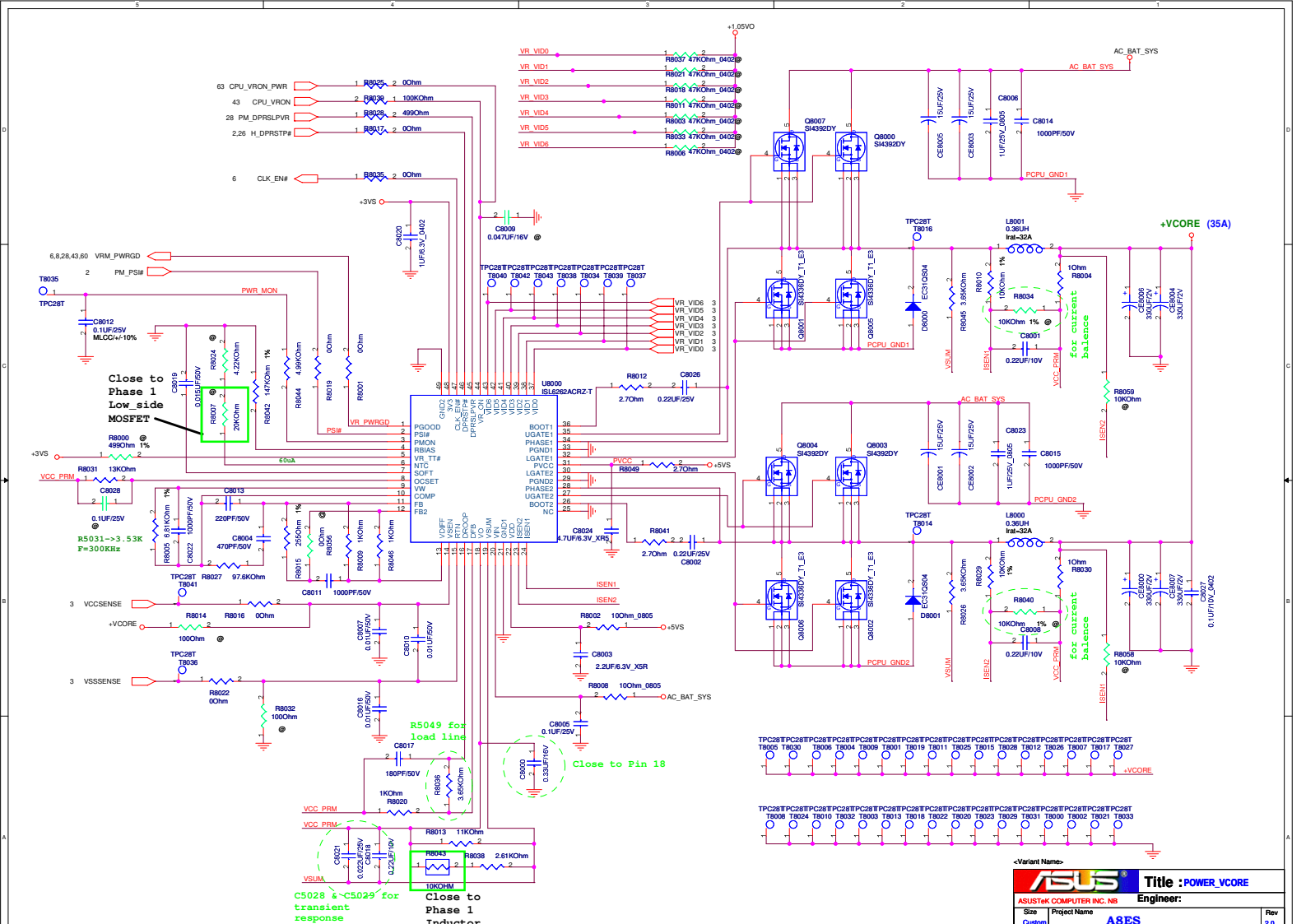


+3VS	+3VS	3.7, 8, 11, 14, 15, 21, 22, 23, 24, 29, 30, 33, 36, 38, 40, 41, 42, 43, 45, 46, 47, 49, 50, 51, 53, 55, 57, 62, 68, 70, 80, 91, 92
+5V	+5V	9, 43, 52, 57, 68, 70, 91
+5VS	+5VS	23, 24, 31, 26, 38, 46, 47, 50, 51, 57, 68, 80, 91
+12VS	+12VS	38, 45, 57, 70, 91



ASUS		Title : LED/instant key	
ASUSTEK COMPUTER INC			
Size	Project Name	Engineer:	
Custom	ABES		
Date: 08-14/121, 2007	Sheet	56	of 84

<< Kennedy\_Zhang >>

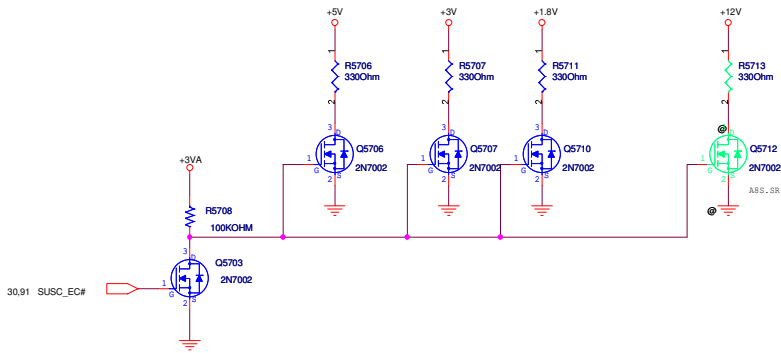
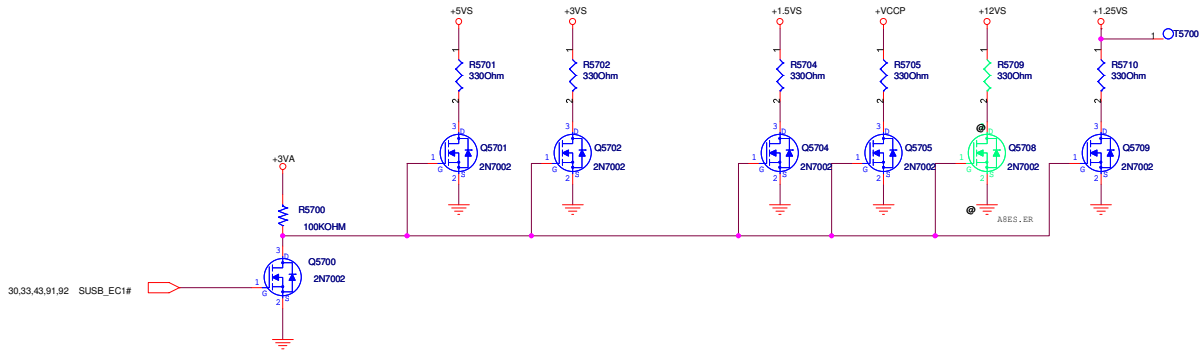


« Kennedy\_Zhang »

<Variant Name>

<b>ASUS</b>		<b>Title : POWER_VCORE</b>	
ASUSTek COMPUTER INC. NB	Project Name	Engineer:	
Size	Custom	<b>A8ES</b>	Rev 2.0
Date: 2007.06.07		Sheet 56 of 70	

# Discharge Circuit




<Variant Name>

<b>ASUS</b>		<b>Title : Discharge</b>
ASUSTek COMPUTER INC		Engineer:
Size	Project Name	Rev
B	A8ES	1.0
Date: 2007.07.16	Sheet	of 84

<< Kennedy\_Zhang >>

<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>A8ES</b>	1.0
Date: 星期三, 十月 11, 2006		Sheet of 94

← Kennedy\_Zhang →

D

D

C

C

B

B

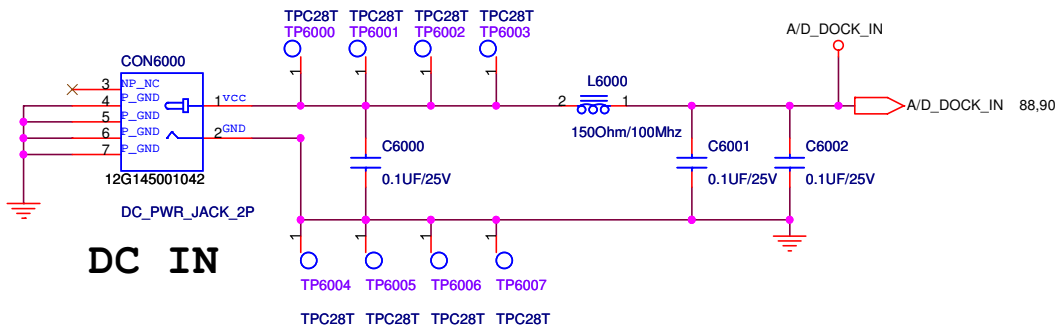
A

A

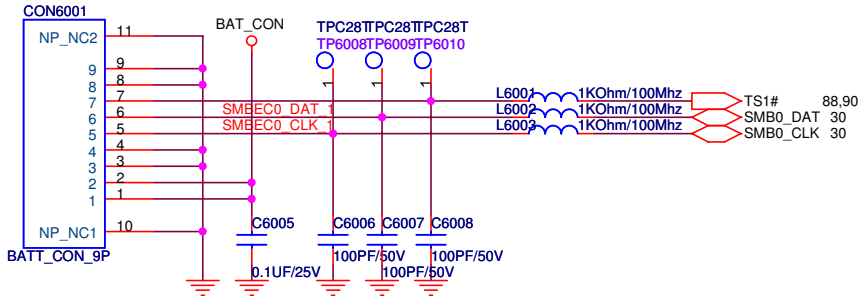
Title		
<Title>		
Size	Document Number	Rev
A	W2S	1.1
Date:	星期三, 十月 11, 2006	Sheet 59 of 94

« Kennedy\_Zhang »

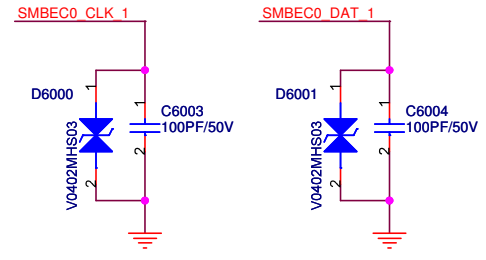




### DC IN



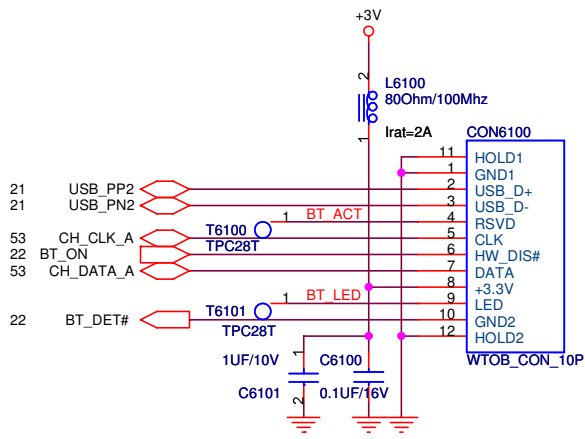
### Battery Connector



<Variant Name>

<b>ASUS</b>		<b>Title : DC IN / BAT</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name <b>ASES</b>		Rev 1.0
Date: 星期一, 五月 21, 2007		Sheet 60	of 94

« Kennedy\_Zhang »

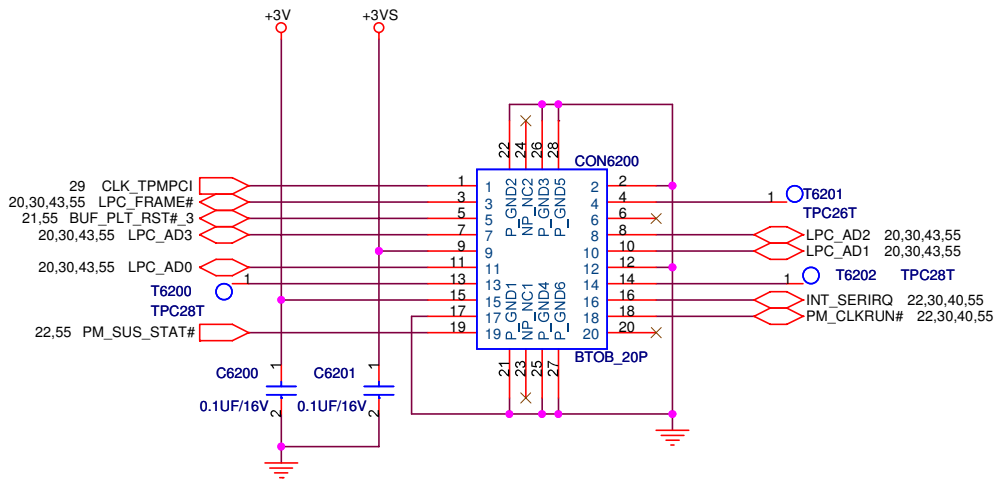


## Bluetooth Module CON

<b>ASUS</b>		<b>Title : BT/CAMERA</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name		Rev
A	A8ES		1.0
Date: 星期三, 五月 16, 2007		Sheet	61 of 94

*« Kennedy\_Zhang »*


# TPM 1.2 Module



<Variant Name>

<b>ASUS</b>		<b>Title :TPM</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name <b>ASES</b>	Rev 1.0	
Date: 星期三, 五月 16, 2007		Sheet	62 of 94

« Kennedy\_Zhang »

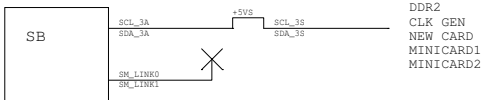
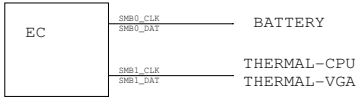
		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>ASES</b>	Rev 0
Date: 星期二, 十月 11, 2006		
Sheet 63 of 94		

← Kennedy\_Zhang →

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 ( Internal )		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)  
SM-Bus Mapping 1001100



## BOM option

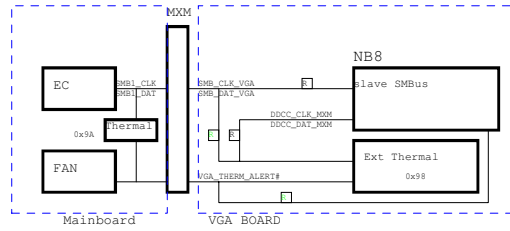
nGM:yellow  
nPM:light red  
=====

@ : no stuff for all  
nGM :no stuff for A8E  
nPM :no stuff for A8S  
nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance  
3G :for Windigo,SIERRA MC8775V  
nA8E :no stuff Irda for A8E

## Support ID2:

Support ID2:  
page 68,Finger print  
page 55,IR  
Page 56,pwr switch and LED

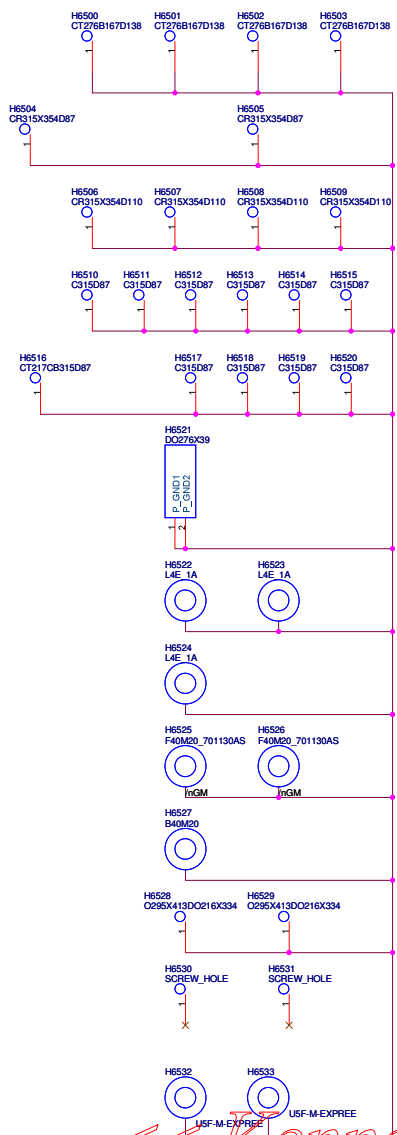
## Thermal block diagram



<Variant Name>

<b>ASUS</b>		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size B	Project Name <b>A8ES</b>	Rev 1.0
Date: 2007-06-06	Sheet 64	of 94

<< Kennedy\_Zhang >>



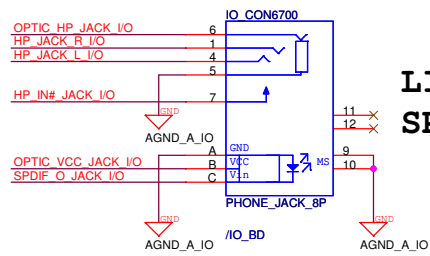
CPU  
 SCREW  
 U HOLE  
 SCREW  
 IO Board  
 MDC\_NUT  
 TPM\_NUT  
 VGA\_NUT  
 KB\_NUT  
 KEYBOARD  
 FIXED HOLE  
 miniCard

« Kennedy\_Zhang »

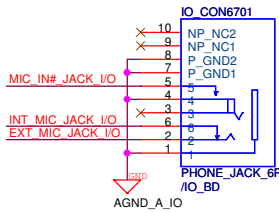
File: <Title>		Rev
Doc	Document Number	1.1
Customer	W2S	
Date: 星期三, 11 07, 2007	Sheet 65	of 94

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
B	ASES		0
Date: 1/11/2006	Sheet	66	of 94

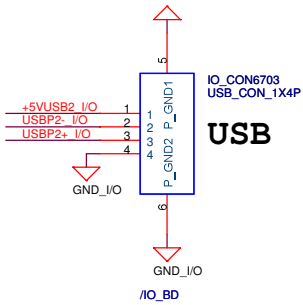
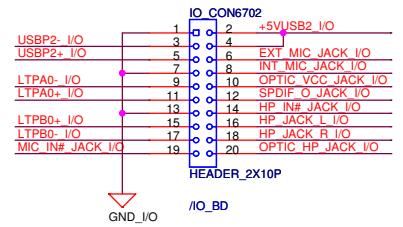
<< Kennedy\_Zhang >>



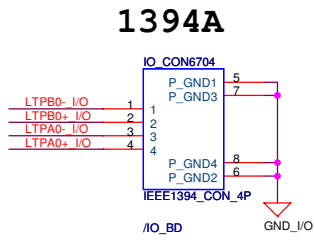
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SPDIF**



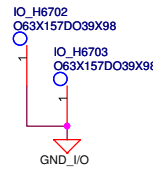
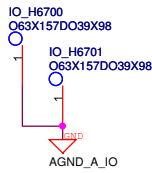
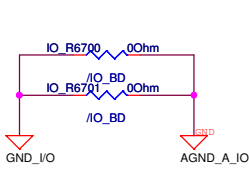
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**USB**



**1394A**

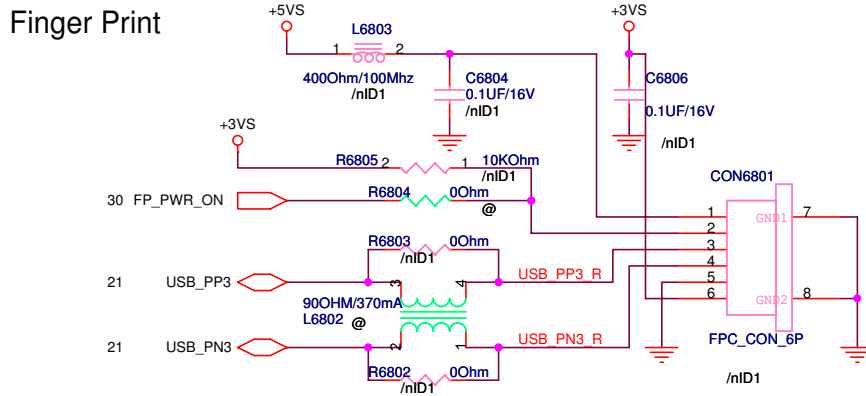
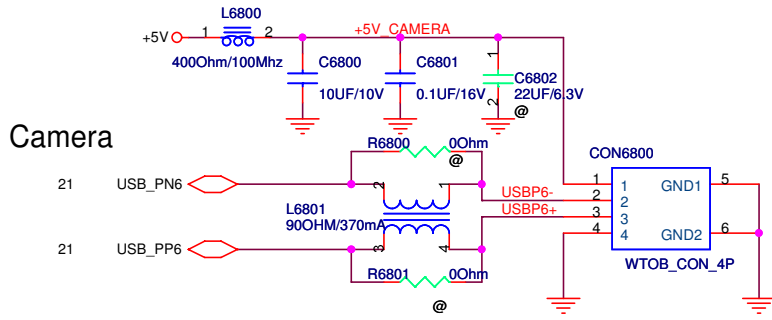


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<b>ASUS</b>		<b>Title : SUB_PCB</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name <b>A8ES</b>		Rev 1.0
Date: 星期五, 三月 30, 2007		Sheet 67	of 94

<< Kennedy\_Zhang >>






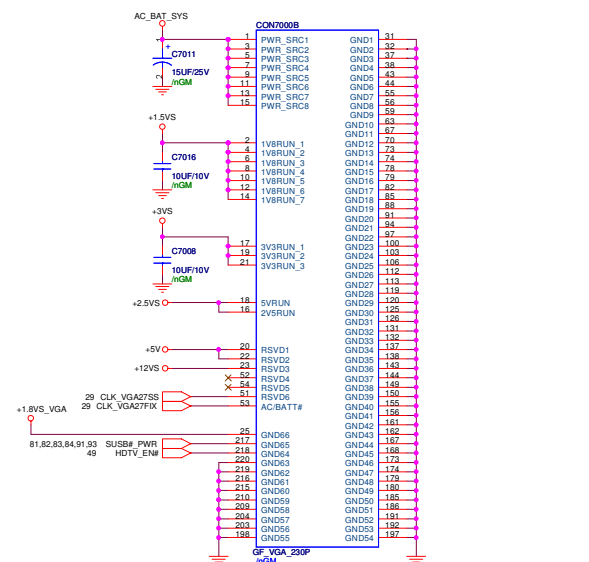
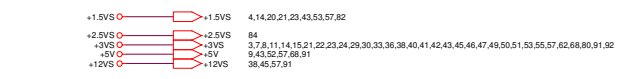
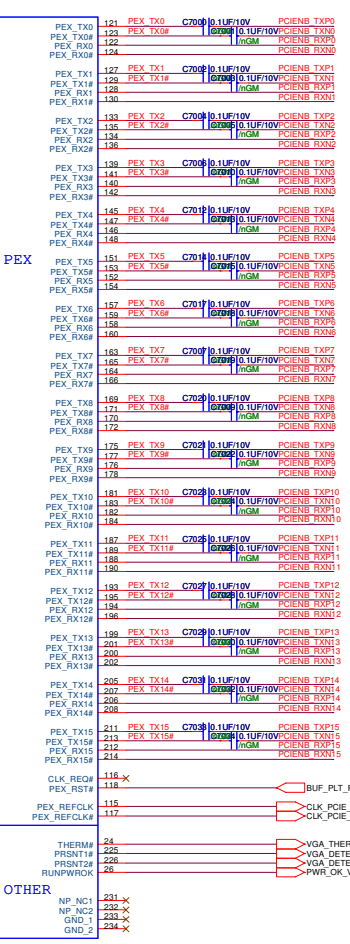
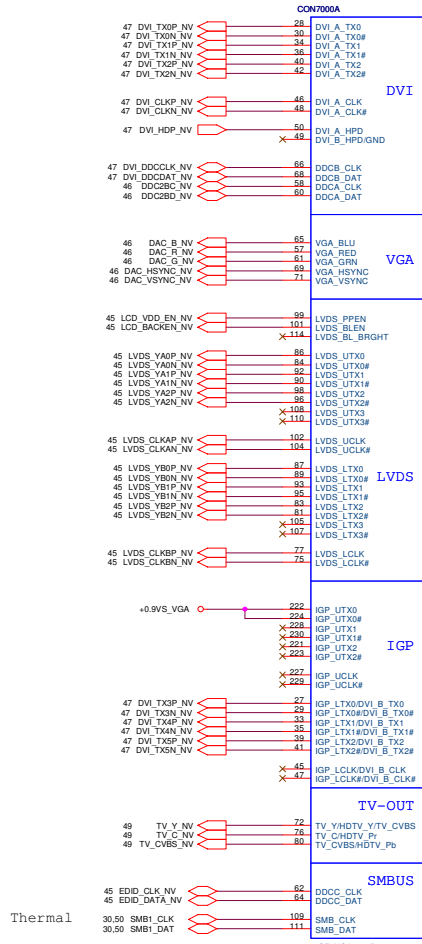
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		<b>Title : CAMERA/FingerPrinter</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A	<b>A8ES</b>	1.0	
Date: 星期五, 五月 22, 2007		Sheet	60 of 94

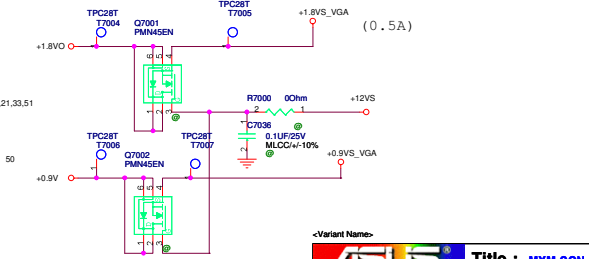
« Kennedy Zhang »

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ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 69 of 94

←← Kennedy\_Zhang →→



Check SUPPORTED VGA BOARD remove Q7001, Q7002 if is no need



Thermal

ASUS  
ASUSTeK COMPUTER INC  
Title: MXM CON  
Engineer:  
Date: 2007-11-21  
Sheet 29 of 84

<< Kennedy\_Zhang >>

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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 71 of 84

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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 72 of 84

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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 73 of 84

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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 74 of 84

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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 75 of 84



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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 78 of 84

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<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	日期: 1月11, 2006	Sheet 77 of 84

		<b>Title : BLANK</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	<b>ABS</b>	0	
Date: 星期三, 十月 11, 2006		Sheet	78 of 94

<< Kennedy\_Zhang >>

4/20 costdown

1)del (16 pcs)

C0501,C0502,C0505,C0506,C0507

C0508,C0511,C0513,C0515,C0518

C0522,C0523,C0527,C0529,C0531

C0532

2)料號由11G235222625320改為11G235310636360 (13 pcs)

C1311,C1421,C1424,

C1428,C1431,

C1301,C1312,C1314,

C1408,C1418,C1446,

C1449,C2312

5/21 costdown

1)del 0ohm:

R0401,R1114,R1118,R1405,R1409,R1413,R1416,R1419,R1420

R1414,R2023,R2208,R2205,R2204,R2202,R2309,R2308,R2304,

R2302,R2303,R2305,R2306,R2307,R2901,R2902,R2900,R3023,


R3024,R3012,R4011

2)cpu 10u\*16-->10u\*11

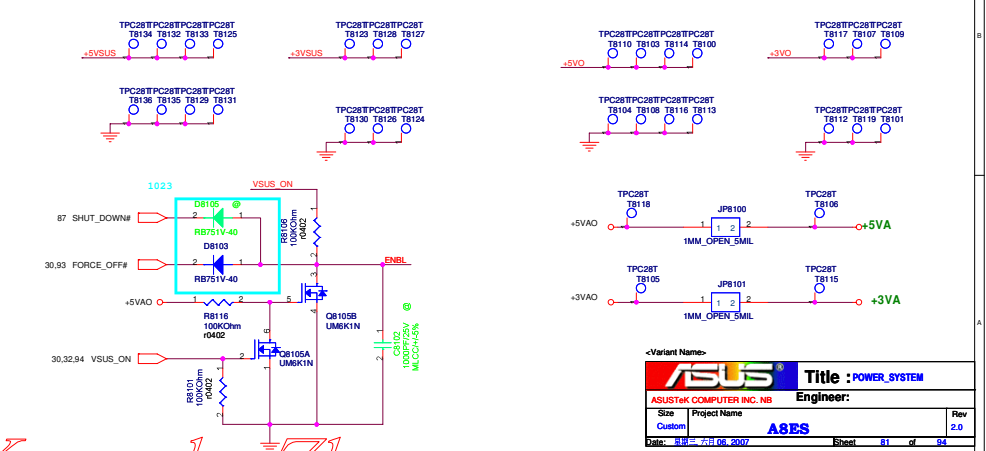
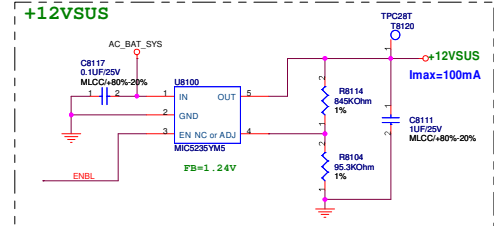
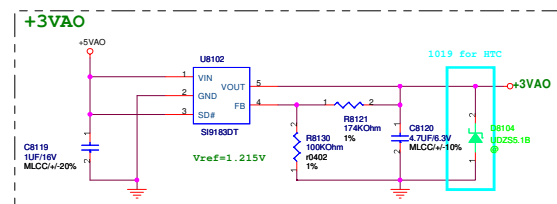
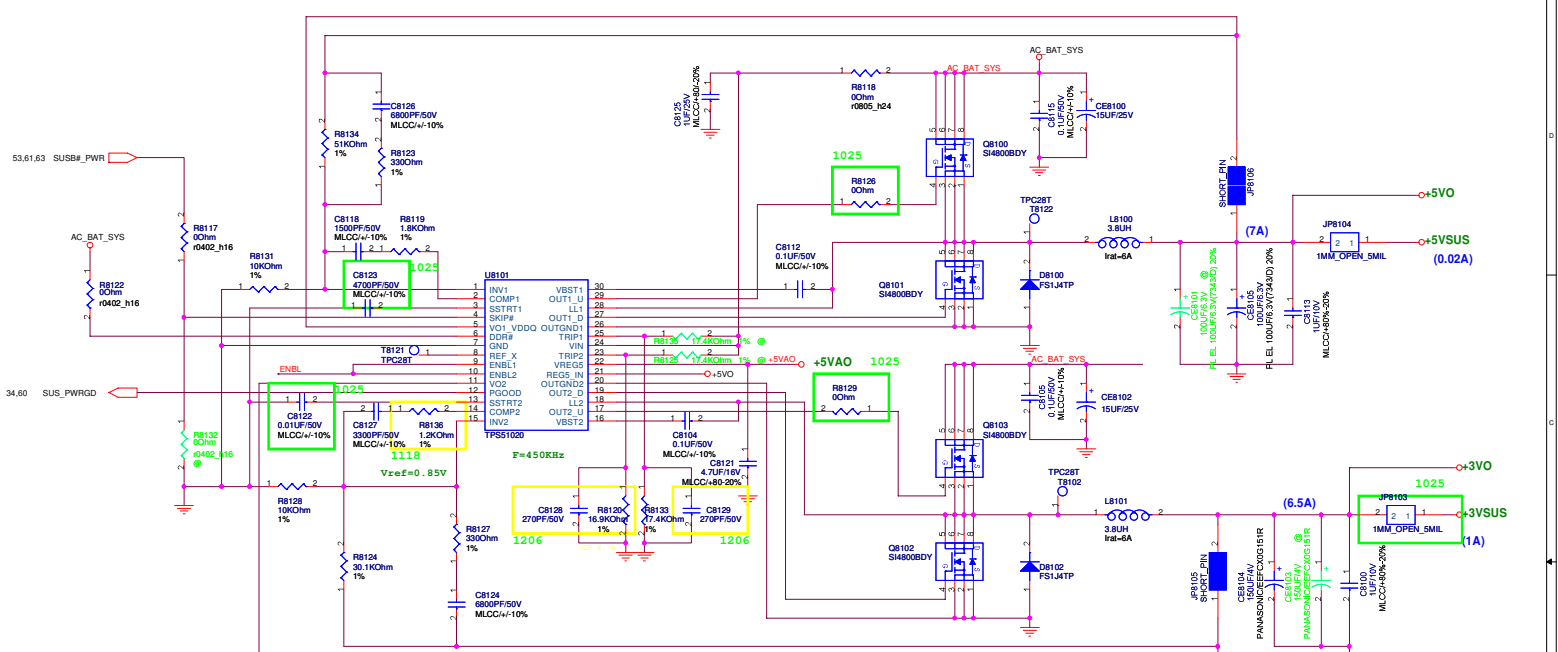
3)Vccp 150u-->100u

4)Audio output 330u-->100u

<Variant Name>

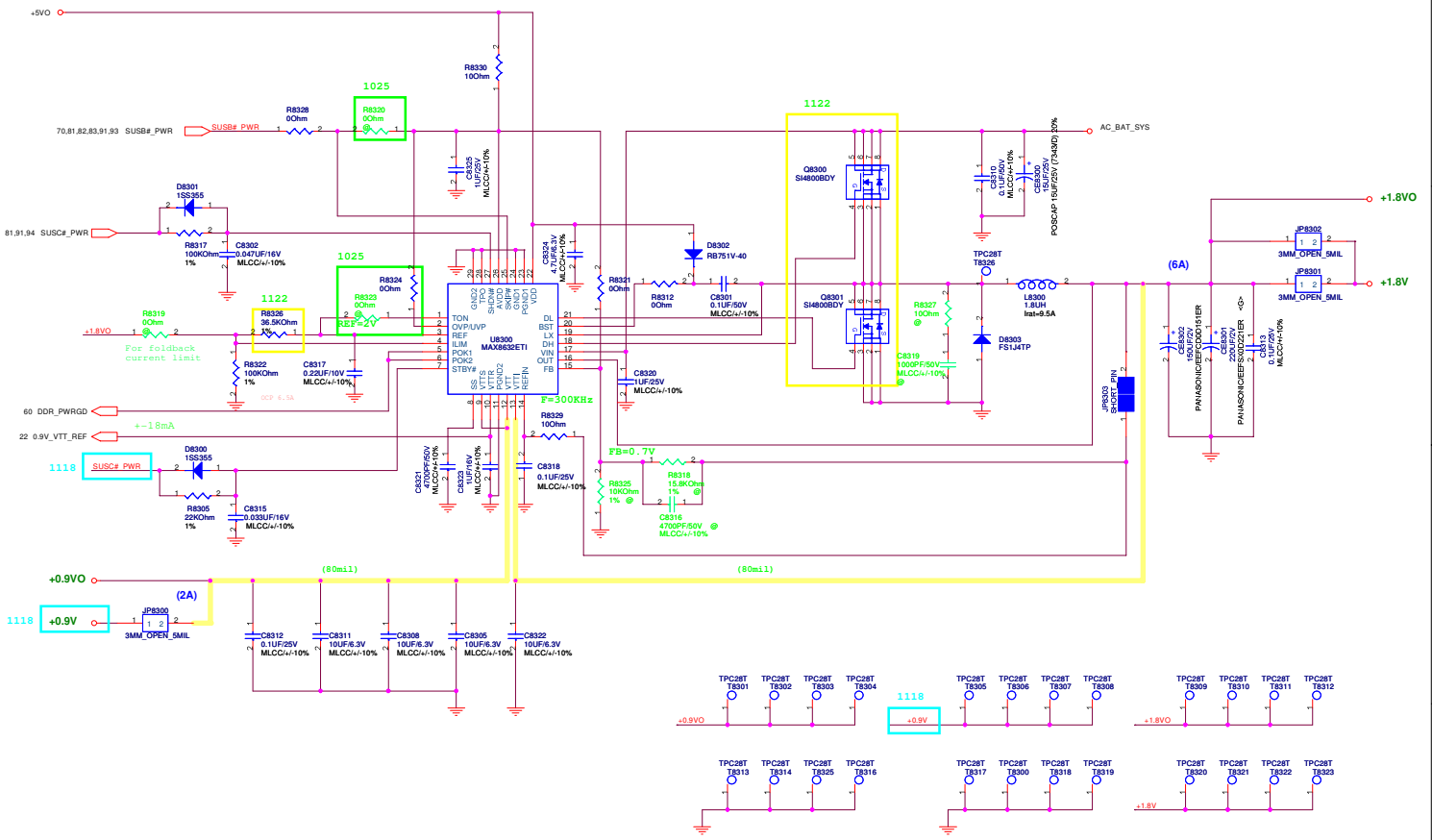
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ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A4	ABES	1.0
Date: 星期一, 五月 21, 2007		Sheet 1 of 94

<< Kennedy\_Zhang >>



**ASUS** Title: POWER\_SYSTEM  
**ASUSTEK COMPUTER INC. NB** Engineer:  
 Size: Project Name: A8ES Rev: 2.0  
 Custom: Date: 08/06/2007 Sheet: 81 of 94

« Kennedy\_Zhang »



<Variant Name>

<b>ASUS</b>		<b>Title : POWER_IO_DDR &amp; VTT</b>	
ASUSTeK COMPUTER INC. NS		Engineer:	
Size	Project Name	Rev	
Custom	ABES	2.0	
Date: 8/17/2007	Sheet	83	of 84

<< Kennedy\_Zhang >>