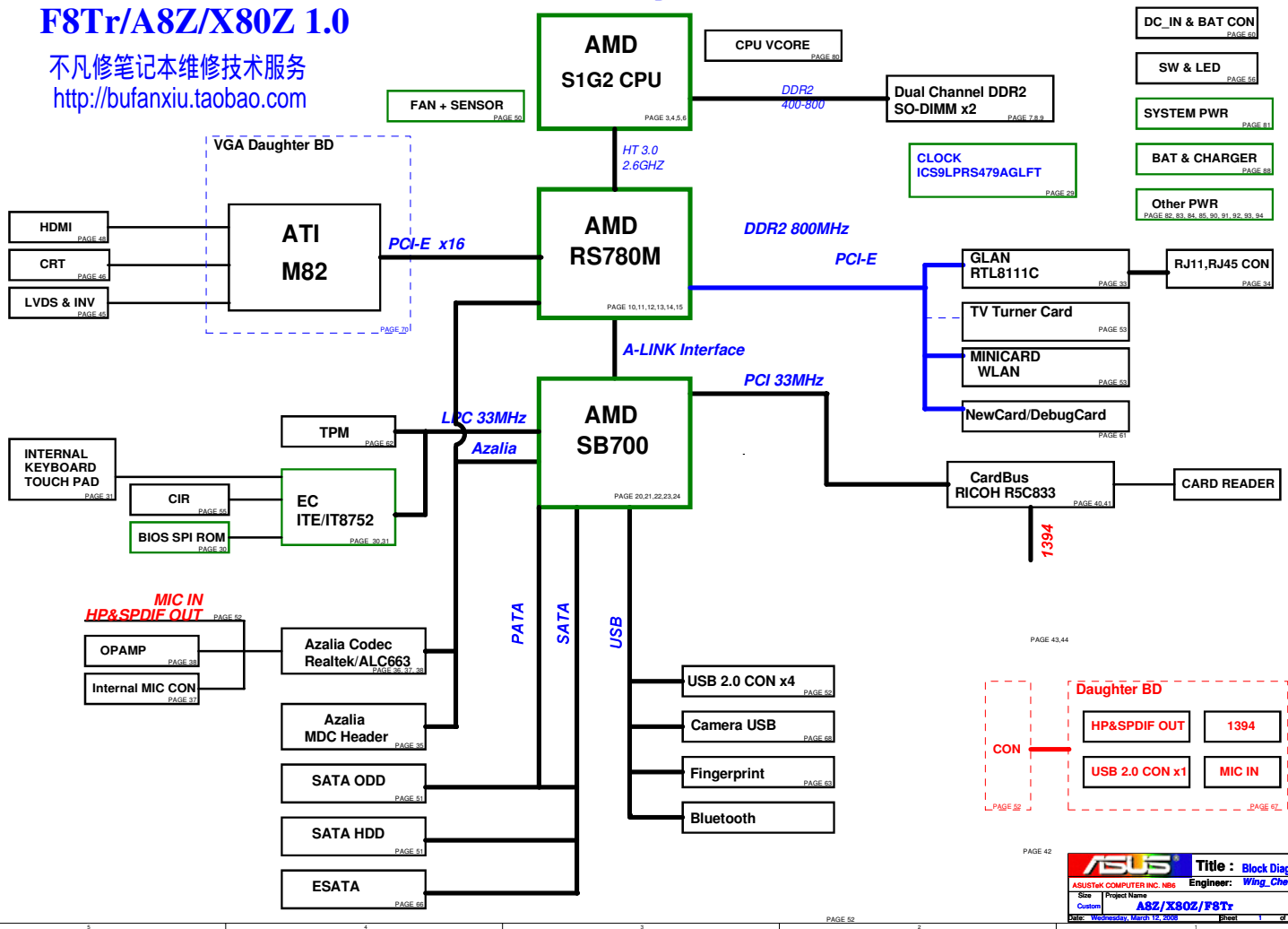


# Block Diagram

## F8Tr/A8Z/X80Z 1.0

不凡修笔记本维修服务  
<http://bufanxiu.taobao.com>



ASUS		Title : Block Diagram	
ASUSTek COMPUTER INC. HKS		Engineer: Wing_Cheng	
Size	Project Name	Rev	
Custom	ASZ/X80Z/F8Tr	0.1	
Date: Wednesday, March 18, 2009		Sheet	1 of 8

<< MaryL\_Liu >>

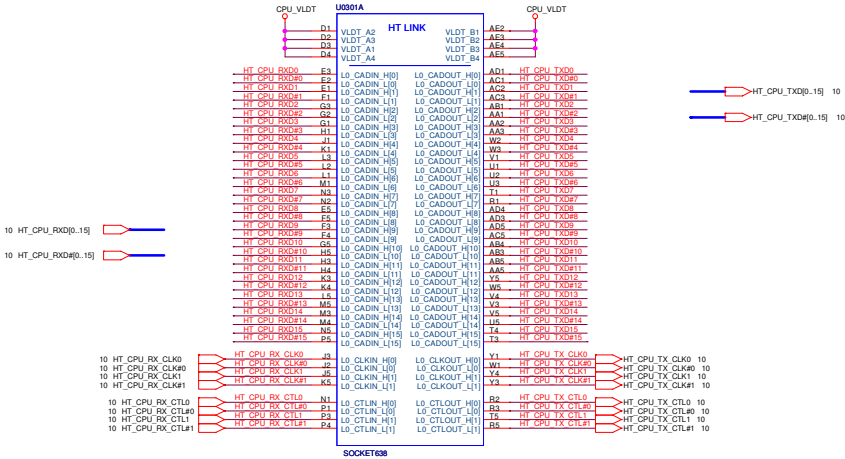
<http://bufanxiu.taobao.com>

81104	add 81051,81052 to 8441
81105	add 81051,81052 to 8441
81106	add 81051,81052 to 8441
81107	add 81051,81052 to 8441
81108	add 81051,81052 to 8441
81109	add 81051,81052 to 8441
81110	add 81051,81052 to 8441
81111	add 81051,81052 to 8441
81112	add 81051,81052 to 8441
81113	add 81051,81052 to 8441
81114	add 81051,81052 to 8441
81115	add 81051,81052 to 8441
81116	add 81051,81052 to 8441
81117	add 81051,81052 to 8441
81118	add 81051,81052 to 8441
81119	add 81051,81052 to 8441
81120	add 81051,81052 to 8441
81121	add 81051,81052 to 8441
81122	add 81051,81052 to 8441
81123	add 81051,81052 to 8441
81124	add 81051,81052 to 8441
81125	add 81051,81052 to 8441
81126	add 81051,81052 to 8441
81127	add 81051,81052 to 8441
81128	add 81051,81052 to 8441
81129	add 81051,81052 to 8441
81130	add 81051,81052 to 8441
81131	add 81051,81052 to 8441
81132	add 81051,81052 to 8441
81133	add 81051,81052 to 8441
81134	add 81051,81052 to 8441
81135	add 81051,81052 to 8441
81136	add 81051,81052 to 8441
81137	add 81051,81052 to 8441
81138	add 81051,81052 to 8441
81139	add 81051,81052 to 8441
81140	add 81051,81052 to 8441
81141	add 81051,81052 to 8441
81142	add 81051,81052 to 8441
81143	add 81051,81052 to 8441
81144	add 81051,81052 to 8441
81145	add 81051,81052 to 8441
81146	add 81051,81052 to 8441
81147	add 81051,81052 to 8441
81148	add 81051,81052 to 8441
81149	add 81051,81052 to 8441
81150	add 81051,81052 to 8441
81151	add 81051,81052 to 8441
81152	add 81051,81052 to 8441
81153	add 81051,81052 to 8441
81154	add 81051,81052 to 8441
81155	add 81051,81052 to 8441
81156	add 81051,81052 to 8441
81157	add 81051,81052 to 8441
81158	add 81051,81052 to 8441
81159	add 81051,81052 to 8441
81160	add 81051,81052 to 8441
81161	add 81051,81052 to 8441
81162	add 81051,81052 to 8441
81163	add 81051,81052 to 8441
81164	add 81051,81052 to 8441
81165	add 81051,81052 to 8441
81166	add 81051,81052 to 8441
81167	add 81051,81052 to 8441
81168	add 81051,81052 to 8441
81169	add 81051,81052 to 8441
81170	add 81051,81052 to 8441
81171	add 81051,81052 to 8441
81172	add 81051,81052 to 8441
81173	add 81051,81052 to 8441
81174	add 81051,81052 to 8441
81175	add 81051,81052 to 8441
81176	add 81051,81052 to 8441
81177	add 81051,81052 to 8441
81178	add 81051,81052 to 8441
81179	add 81051,81052 to 8441
81180	add 81051,81052 to 8441
81181	add 81051,81052 to 8441
81182	add 81051,81052 to 8441
81183	add 81051,81052 to 8441
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81185	add 81051,81052 to 8441
81186	add 81051,81052 to 8441
81187	add 81051,81052 to 8441
81188	add 81051,81052 to 8441
81189	add 81051,81052 to 8441
81190	add 81051,81052 to 8441
81191	add 81051,81052 to 8441
81192	add 81051,81052 to 8441
81193	add 81051,81052 to 8441
81194	add 81051,81052 to 8441
81195	add 81051,81052 to 8441
81196	add 81051,81052 to 8441
81197	add 81051,81052 to 8441
81198	add 81051,81052 to 8441
81199	add 81051,81052 to 8441
81200	add 81051,81052 to 8441

		Title :	
ASUSTeK COMPUTER INC. (NBI)		Engineer: <OrgAddrs>	
Disc	Project Name	Rev	1.1
Custom	ASZ/X80Z/F8Ty		
Date	Wednesday, March 16, 2005	Sheet	2 of 22

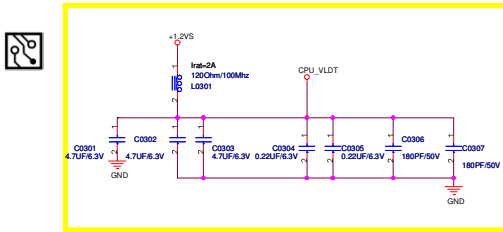
<< MaryL\_Liu >>

1. 5A



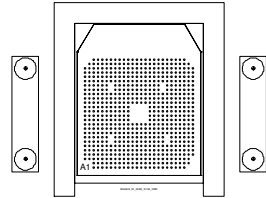
12G011306384 071113

Do not cross plane.



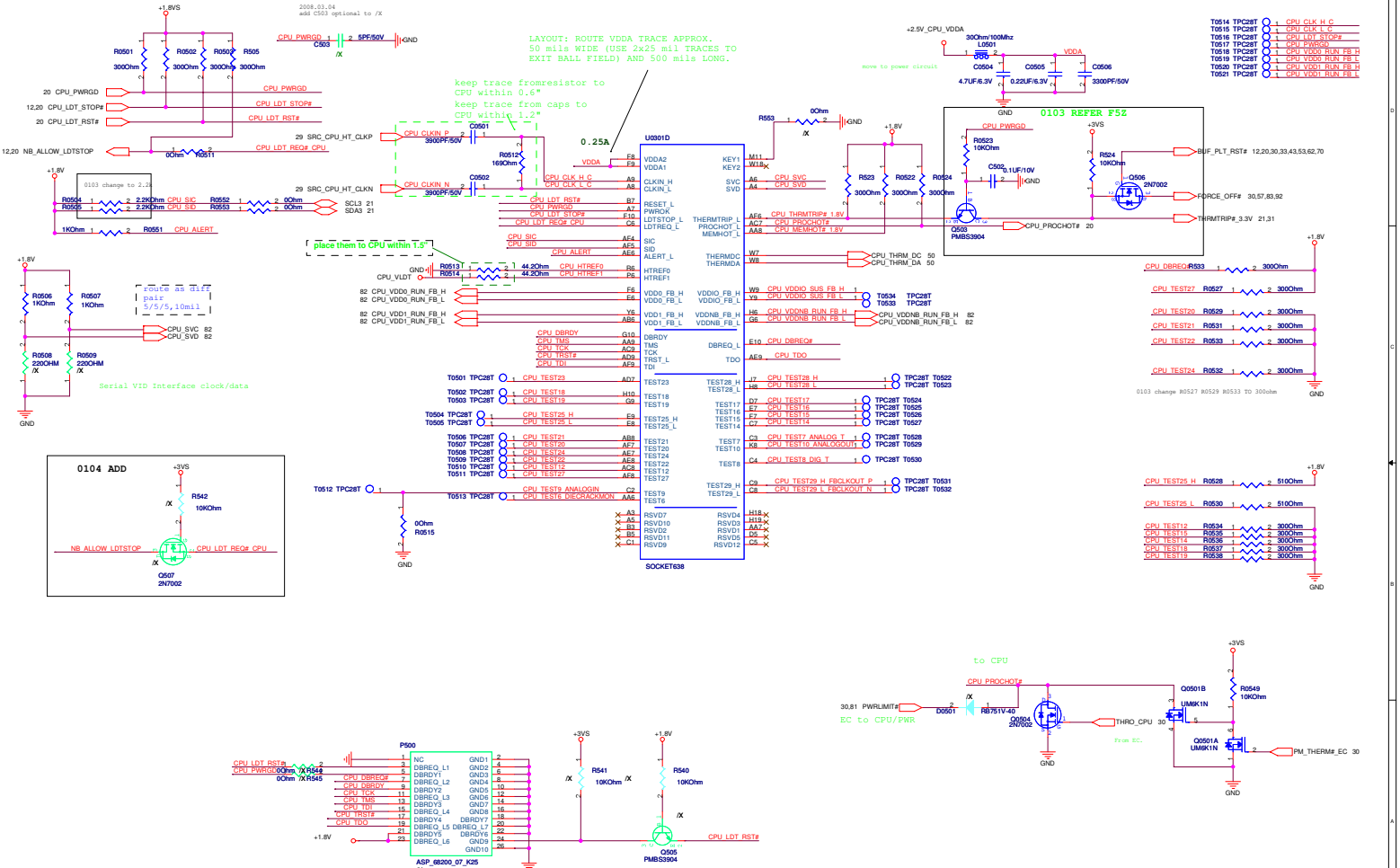
Place close to socket

\* If VLDT is connected only on one side, one 4.7uF cap should be added to the other side



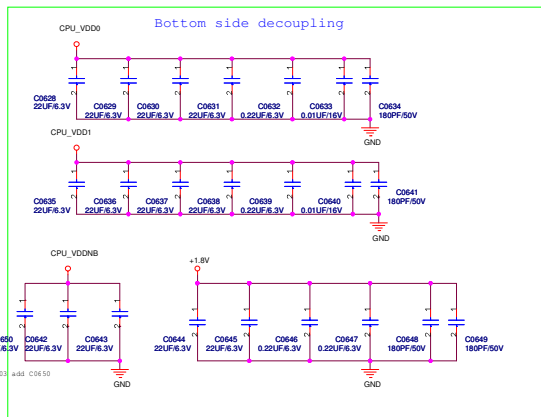
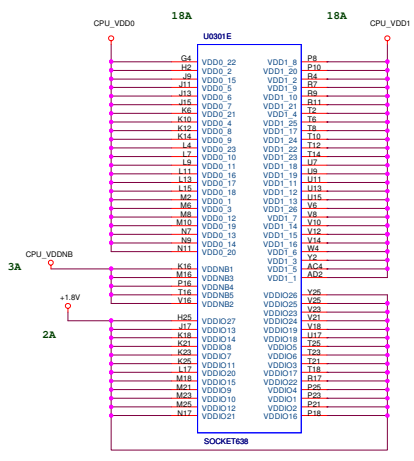
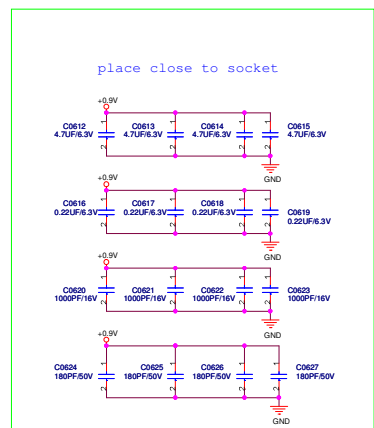
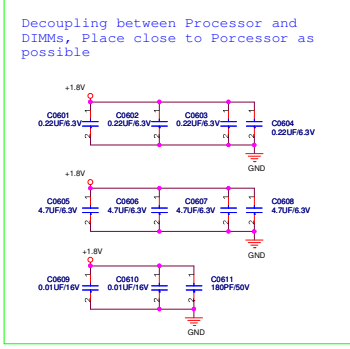
<< MaryL\_Liu >>



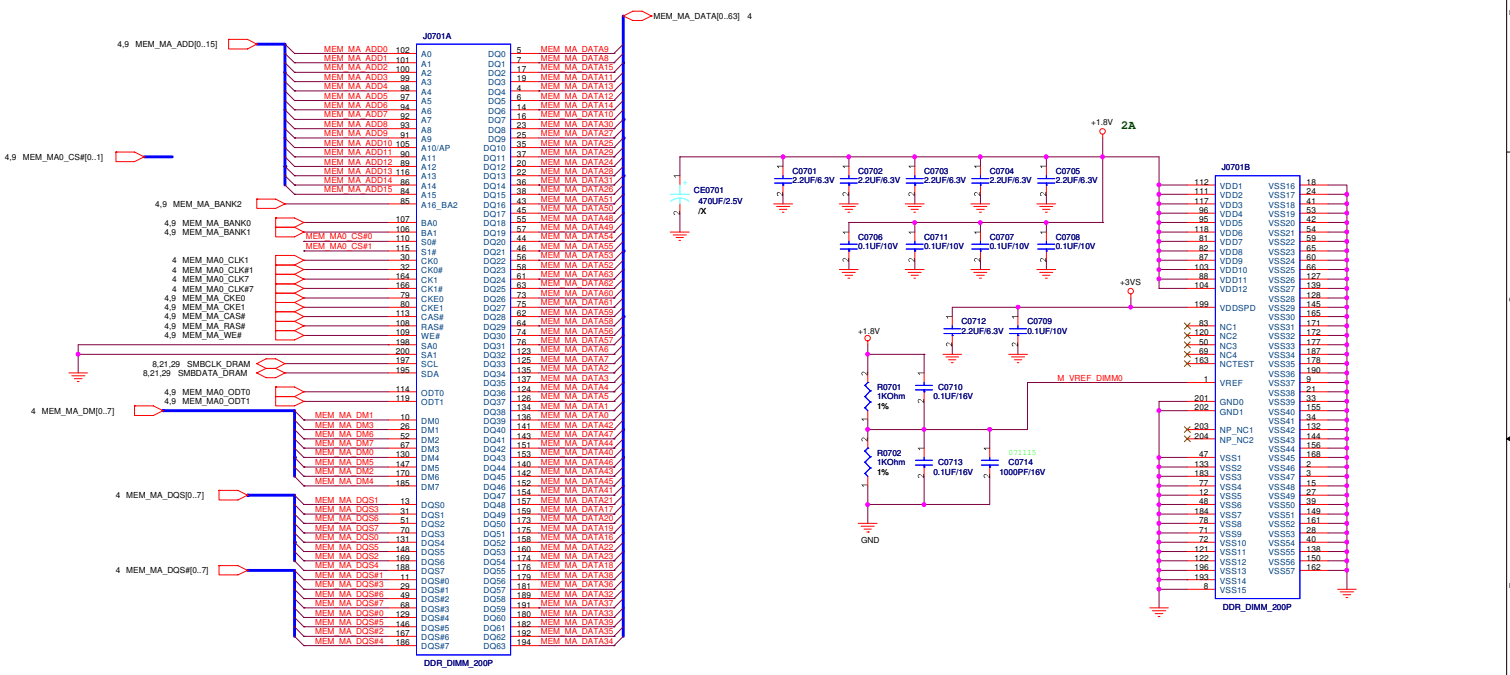


<< MaryL\_Liu >>

U0301F	
AA4	VSS49
AA11	VSS128
AA15	VSS116
AA16	VSS115
AA17	VSS75
AA18	VSS26
AA19	VSS44
AA20	VSS79
AA21	VSS28
AA22	VSS91
AA23	VSS90
AA24	VSS92
AA25	VSS93
AA26	VSS94
AA27	VSS39
AA28	VSS38
AA29	VSS95
AA30	VSS96
AA31	VSS97
AA32	VSS129
AA33	VSS86
AA34	VSS85
AA35	VSS34
AA36	VSS83
AA37	VSS82
AA38	VSS74
AA39	VSS73
AA40	VSS72
AA41	VSS91
AA42	VSS90
AA43	VSS92
AA44	VSS93
AA45	VSS94
AA46	VSS39
AA47	VSS38
AA48	VSS95
AA49	VSS96
AA50	VSS97
AA51	VSS129
AA52	VSS86
AA53	VSS85
AA54	VSS34
AA55	VSS83
AA56	VSS82
AA57	VSS74
AA58	VSS73
AA59	VSS72
AA60	VSS91
AA61	VSS90
AA62	VSS92
AA63	VSS93
AA64	VSS94
AA65	VSS39
AA66	VSS38
AA67	VSS95
AA68	VSS96
AA69	VSS97
AA70	VSS129
AA71	VSS86
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AA73	VSS34
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AA77	VSS73
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AA82	VSS93
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AA115	VSS73
AA116	VSS72
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AA121	VSS94
AA122	VSS39
AA123	VSS38
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AA126	VSS97
AA127	VSS129
AA128	VSS86
AA129	VSS85
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AA131	VSS83
AA132	VSS82
AA133	VSS74
AA134	VSS73
AA135	VSS72
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AA137	VSS90
AA138	VSS92
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AA180	VSS38
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AA192	VSS72
AA193	VSS91
AA194	VSS90
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AA197	VSS94
AA198	VSS39
AA199	VSS38
AA200	VSS95



<< MaryL\_Liu >>

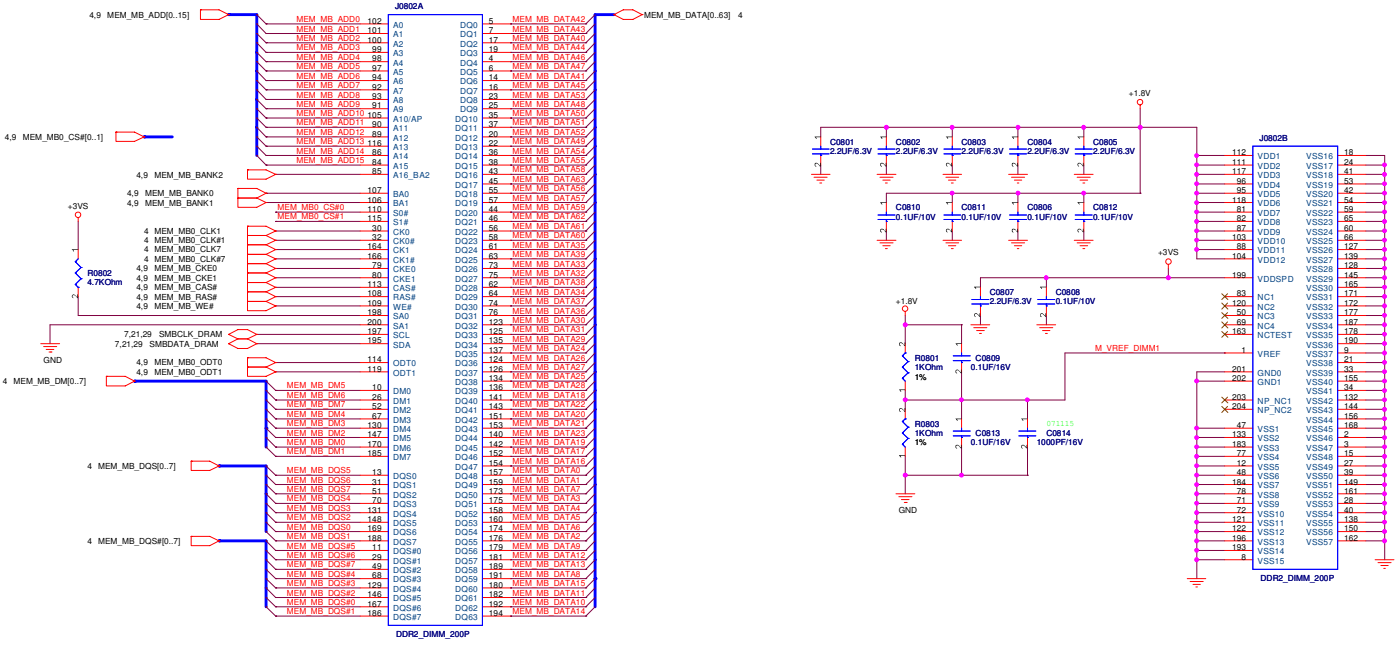


High

-Variant Name-

<b>ASUS</b>		<b>Title : DDR2 SO-DIMM0</b>	
ASUSTEK COMPUTER INC		Engineer:	
Site	Project Name	Rev	
Custom	ABZ/X80Z/F8T	0.1	
Date: Wednesday, March 12 2008	Sheet	7	of 92

<< MaryL\_Liu >>

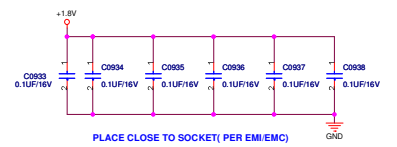
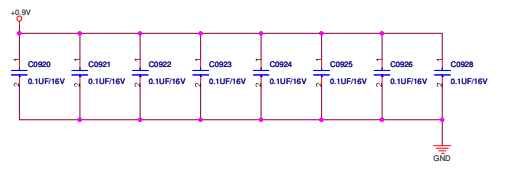
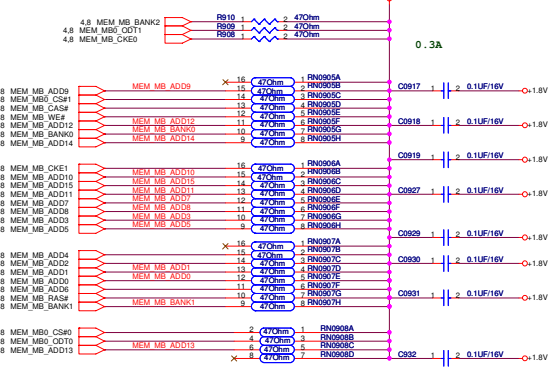
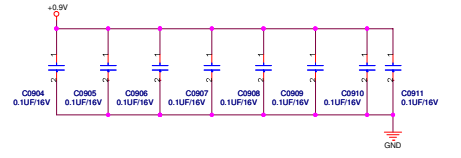
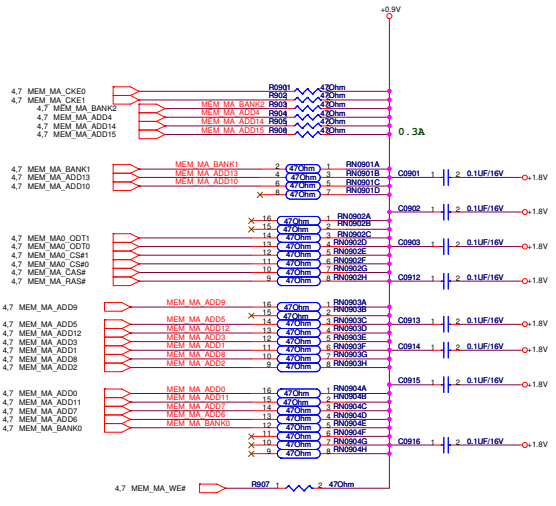


low

<b>ASUS</b>		<b>Title : DDR2 SO-DIMM1</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABZ/XB02/F8T	0.1	
Date: Wednesday, March 12, 2008	Sheet	8	of 92

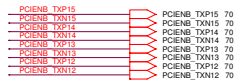
« MaryL\_Liu »





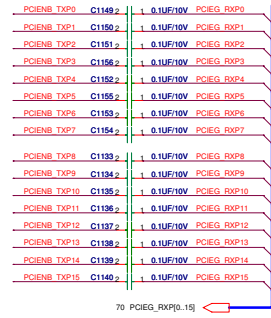
<< MaryL\_Liu >>



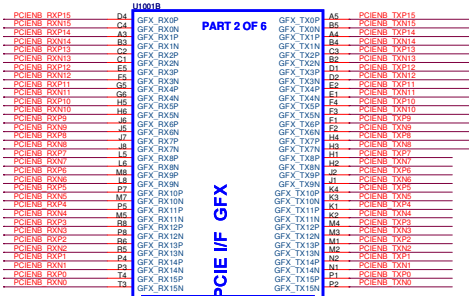
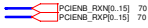


PCI-E:  
0-3 HDMI@ RS780M  
4-7 NC  
8-15 VGABx

Refer to RS780M datasheet Table 3-10



Caps on VGA card

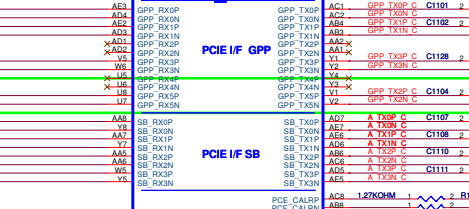
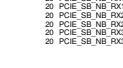
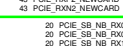
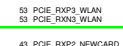
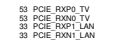


PART 2 OF 6

PCI-E I/F GFX

PCI-E I/F GPP

PCI-E I/F SB

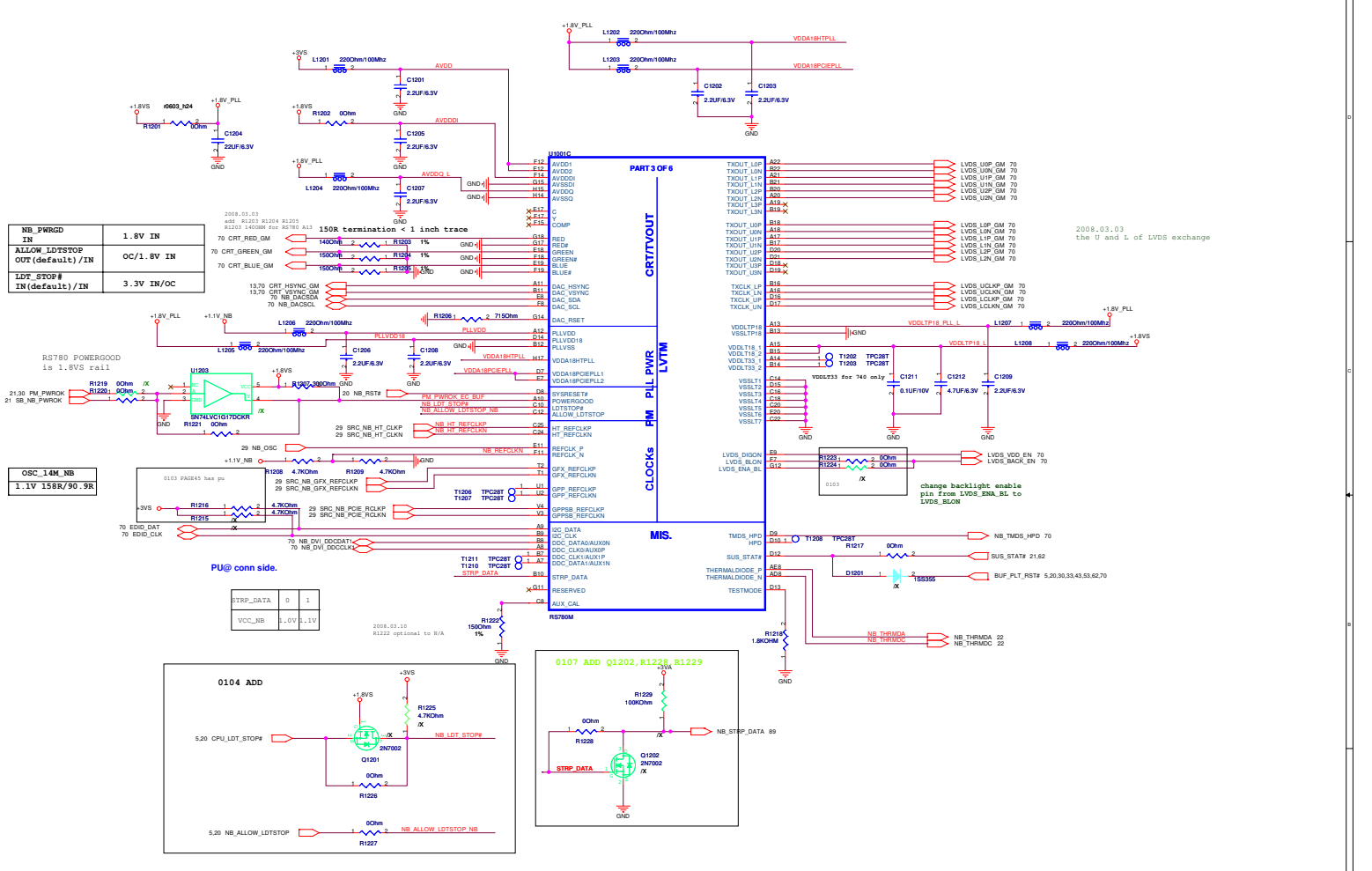


RS780M



**ASUS** Title: RS780M-PCI-E LINK I/F  
ASUSTek Computer INC. Engineer: <OrgAddrt>  
Size: Custom Project Name: ABZ/X80Z/F8T Rev: 0.1  
Date: Wednesday, March 19, 2008 Sheet 11 of 28

<< MaryL\_Liu >>



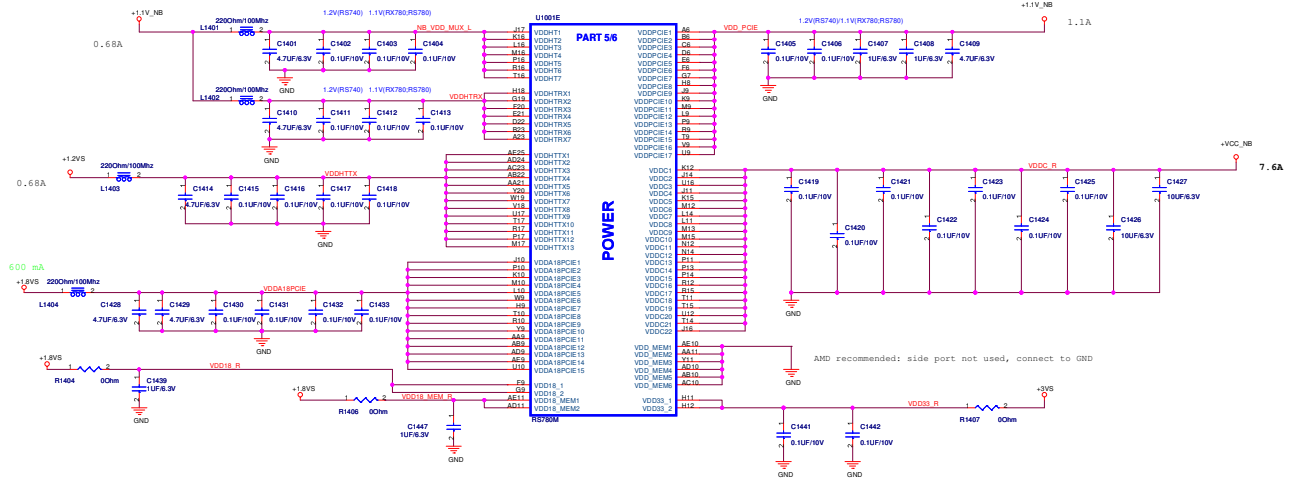
2008.03.03  
the U and L of LVDS exchange

?? for external graphic

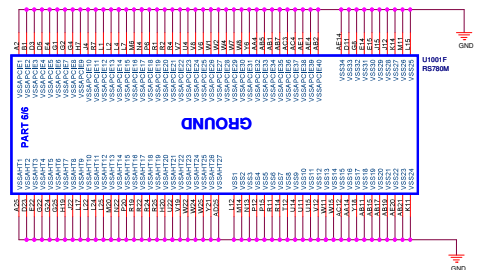
<< MaryL\_Liu >>

<b>ASUS</b>		<b>Title: RS780M-SYS I/F</b>	
ASUSTek Computer INC		Engineer: <OrgAdapt>	
Ver	Project Name	Rev	
C	AS2/X802/P81r	0.1	
Date: Wednesday, March 12, 2008		Sheet: 15 of 25	







3.3V rails ramp high relative to 1.8V  
Display and PLL rails. max 2.1V



<< MaryL\_Liu >>


		<b>Title :</b>
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>
<b>Size</b>	<b>Project Name</b>	<b>Rev</b>
A	<b>ABZ/X80Z/F8Tr</b>	0.1
<b>Date:</b> Wednesday, March 12, 2008		<b>Sheet</b> 15 <b>of</b> 92

*<< MaryL\_Liu >>*


		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>ASZ/X80Z/F8Tr</b>	0.1
Date: <b>Wednesday, March 12, 2008</b>		Sheet <b>16</b> of <b>92</b>

*<< MaryL\_Liu >>*




		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>ASZ/X80Z/F8Tr</b>	Rev 0.1	
Date: <b>Wednesday, March 12, 2008</b>		Sheet	<b>17</b> of <b>92</b>

*<< MaryL\_Liu >>*

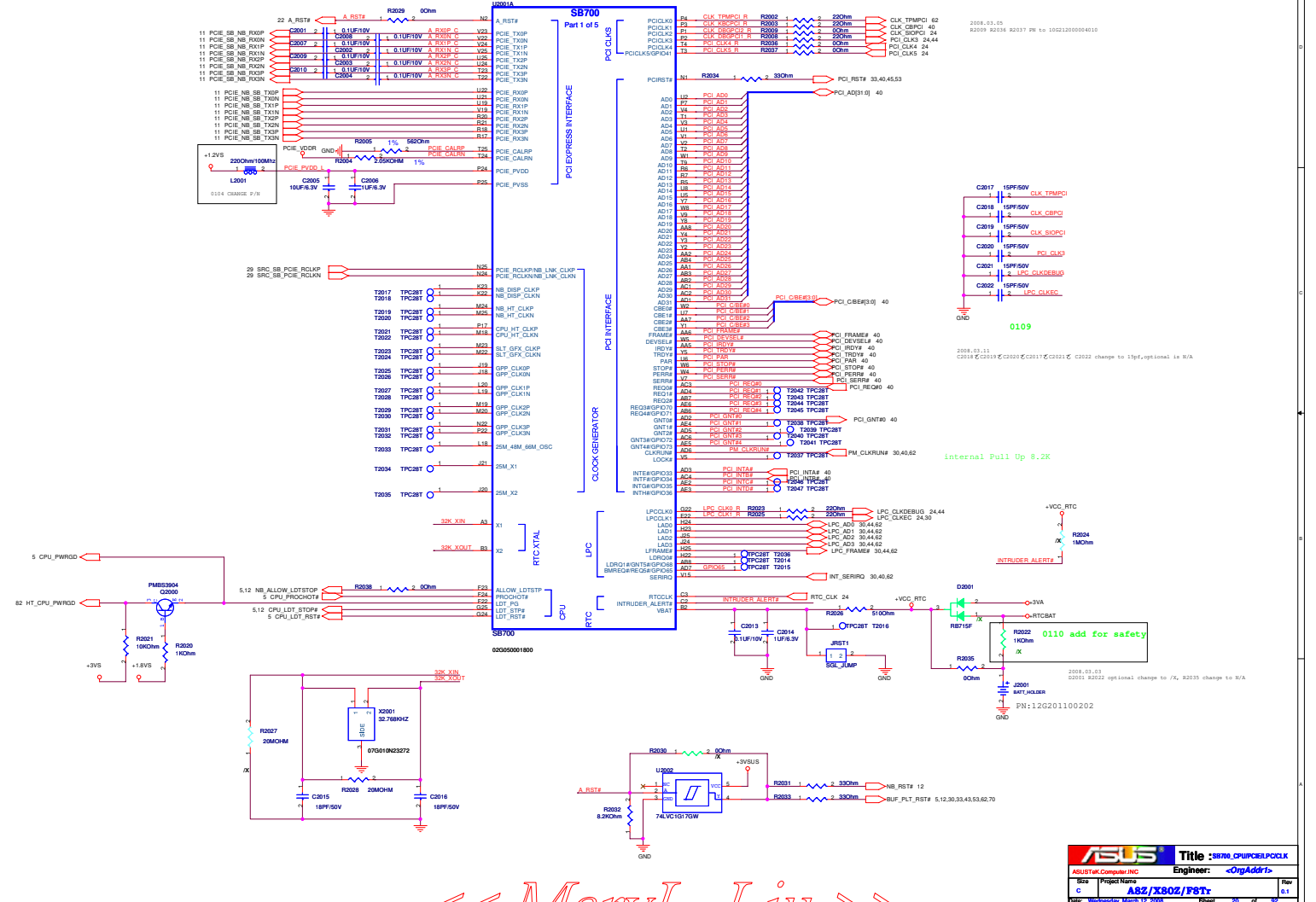
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ASUSTeK COMPUTER INC		<b>Engineer:</b>
<b>Size</b>	<b>Project Name</b>	<b>Rev</b>
A	<b>A8Z/X80Z/F8Tr</b>	0.1
<b>Date:</b> Wednesday, March 12, 2008		<b>Sheet</b> 18 <b>of</b> 92

*<< MaryL\_Liu >>*

		<b>Title : BLANK</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>ASZ/X80Z/F8Tr</b>	Rev 0.1
Date: <b>Wednesday, March 12, 2008</b>		Sheet <b>19</b> of <b>92</b>

*<< MaryL\_Liu >>*

0108 change R2008 TO 22 ohm

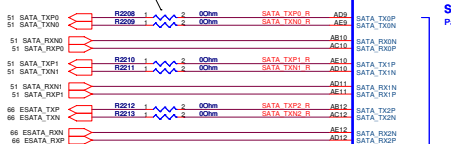


		Title : SB700_CPU_PCIE_POOLK	
		Asustek Computer INC	
Size	Project Name	Engineer: <OrgAdm>	
C	A82/X302/P8Tr	Rev	0.1
Date: Wednesday, March 22, 2006		Sheet	25 of 25

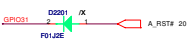
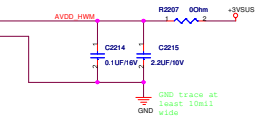
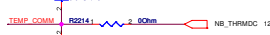
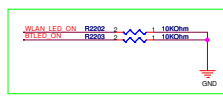
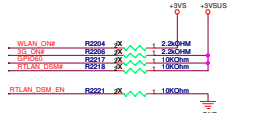
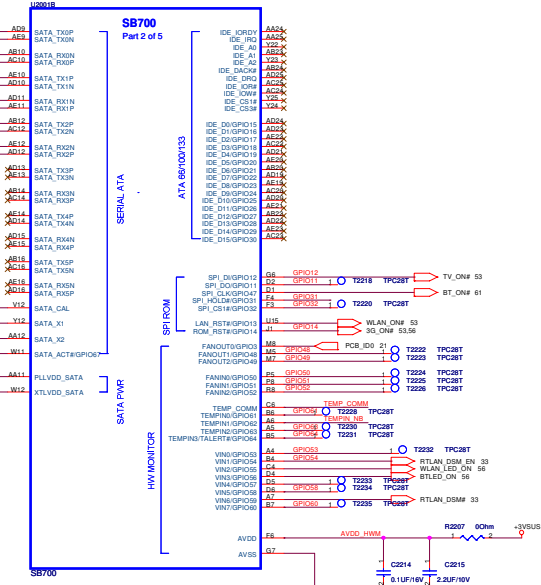
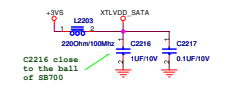
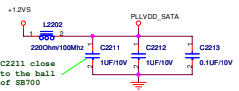
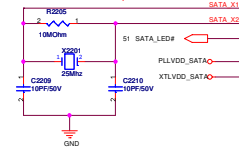


for sata II close sb in 0.5"

for SATA HDD  
for SATA ODD  
for E-SATA



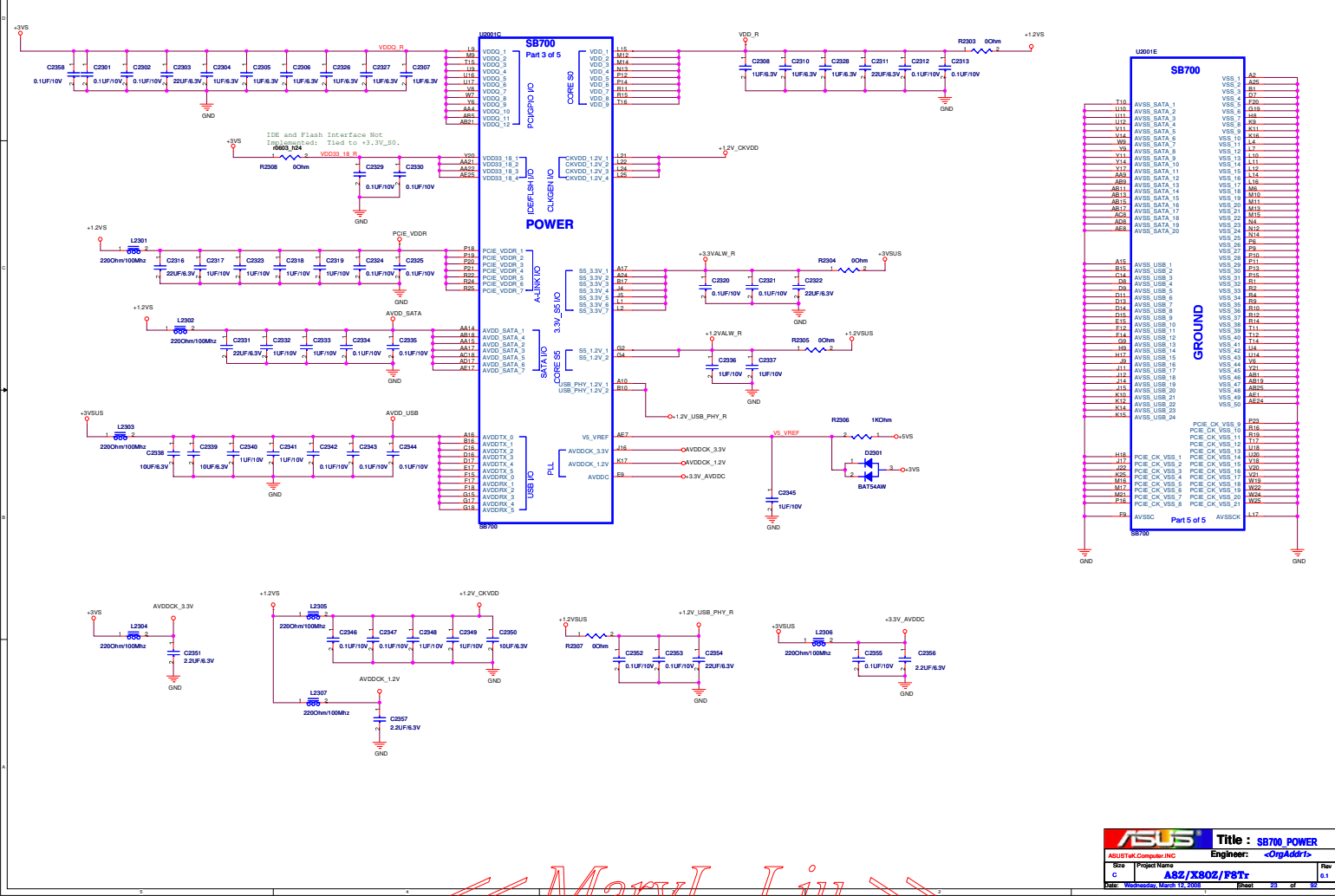
Place SATA\_CAL  
RES very close  
to ball of SB700



2008\_03\_05  
add optional to FX

<b>ASUS</b>		<b>Title : SB700_PATA/SATA</b>	
ASUSTek Computer Inc.		Engineer: <OrgAdit>	
Size	Project Name	Rev	
C	A82/X302/P8T	0.1	
Date: Wednesday, March 27, 2008		Sheet: 25 of 25	

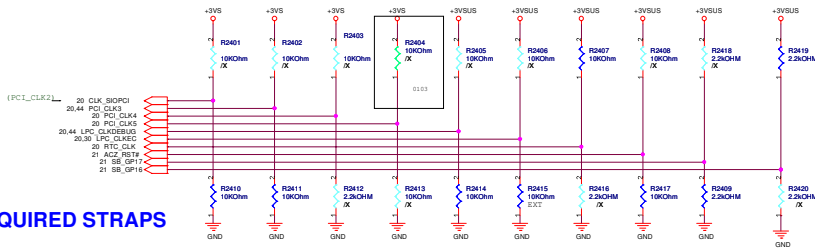
<< MaryL\_Liu >>



<b>ASUS</b>		<b>Title: SB700_POWER</b>	
ASUSTeK Computer Inc.		Engineer: <OrgAddt>	
Sca	Project Name	Rev	
C	A82/X804/P8Tr	0.1	
Date: Wednesday, March 12, 2008		Sheet: 25 of 25	

<< MaryL\_Liu >>

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



**REQUIRED STRAPS**


	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEB	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC	EC ENABLED	HJ = Reserved HL = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PC) on XT, apply 32KHz to RTC_CLK	EC DISABLED DEFAULT	LH = LPC ROM (Default) LL = FWH ROM	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.  
I.E. LPC\_CLK0 FOR EC ENABLE, AZ\_RST# FOR MEM BOOT ENABLE.


<b>ASUS</b>		<b>Title : SB700_STRAP</b>	
ASUSTeK Computer INC.		Engineer: <OrgAdd>	
Size	Project Name	Rev	
C	A82/X802/P8T	0.1	
Date: Wednesday, March 12, 2008	Sheet: 24	of	25

<< MaryL\_Liu >>




		<b>Title :</b>
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>
Size	Project Name	Rev
A	<b>ABZ/X80Z/F8Tr</b>	0.1
Date: Wednesday, March 12, 2008		Sheet 25 of 92


*<< MaryL\_Liu >>*

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>A8Z/X80Z/F8Tr</b>	0.1
Date: Wednesday, March 12, 2008		Sheet 26 of 92

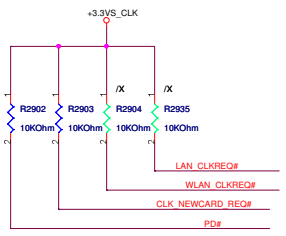
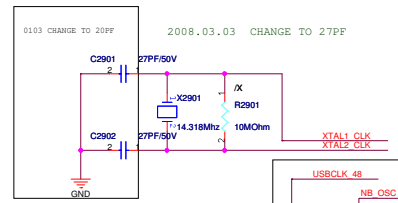
*<< MaryL\_Liu >>*

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8Z/X80Z/F8Tr</b>	0.1	
Date: Wednesday, March 12, 2008		Sheet 27 of 92	

*<< MaryL\_Liu >>*

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>A8Z/X80Z/F8Tr</b>	0.1
Date: <b>Wednesday, March 12, 2008</b>		Sheet <b>28</b> of <b>92</b>

*<< MaryL\_Liu >>*



SEL_27	0	100 MHz differential Spread SRC clock
	1	27MHz 3.3V 27MHz spread clock
SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

SIO-14.318Mhz  
2008.03.06  
del1 R2930

NB-14.318Mhz  
2008.03.06  
del1 R2930

PCIE P0: Minicard  
7.8.21 SMBCLK\_DRAM  
7.8.21 SMBDATA\_DRAM

PCIE P3: Minicard  
7.8.21 SMBCLK\_DRAM  
7.8.21 SMBDATA\_DRAM

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD

PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

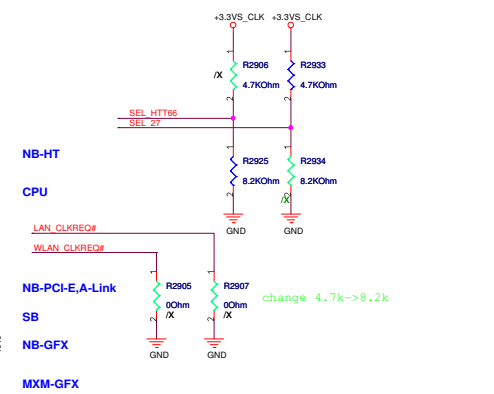
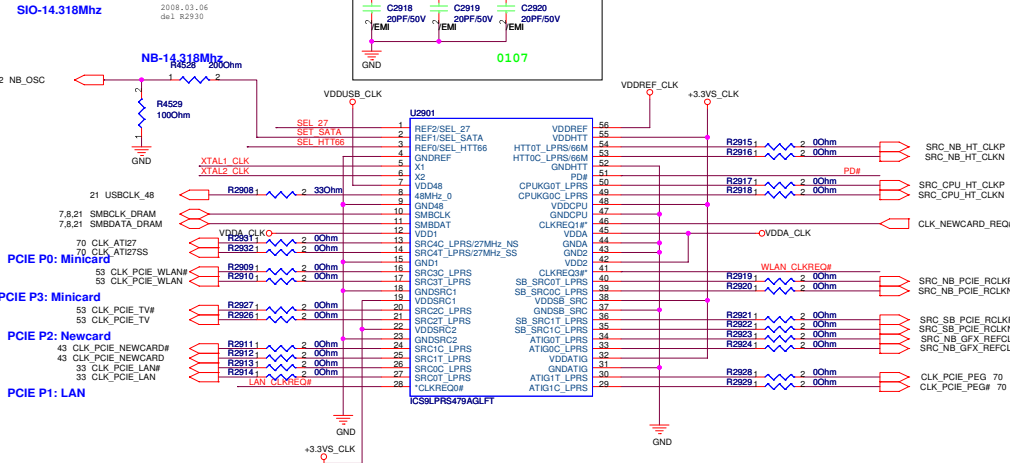
PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
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43 CLK\_PCIE\_NEWCARD

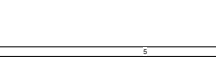
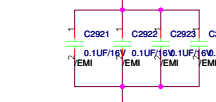
PCIE P1: LAN  
33 CLK\_PCIE\_LAN#  
33 CLK\_PCIE\_LAN

PCIE P0: Minicard  
53 CLK\_PCIE\_WLAN#  
53 CLK\_PCIE\_WLAN

PCIE P2: Newcard  
43 CLK\_PCIE\_NEWCARD#  
43 CLK\_PCIE\_NEWCARD



0112 ADD FOR EMI

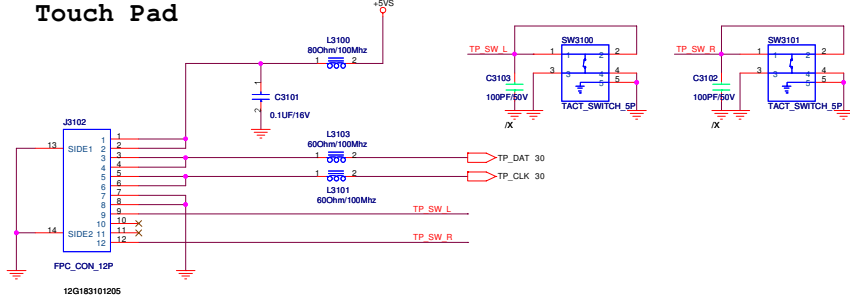


<< MaryL\_Liu >>

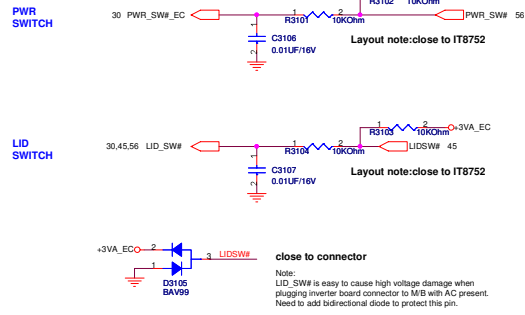
ASUS		Title : ICS9LPRS489AGLFT	
ASUSTeK COMPUTER INC		Engineer: Richard Lu	
Size	Project Name	Rev	
Custom	A8Z/X80Z/F8Tr	0.1	
Date:	Wednesday, March 12, 2008	Sheet	29 of 92



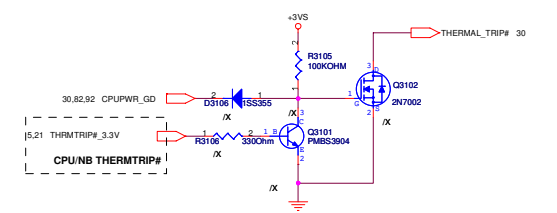
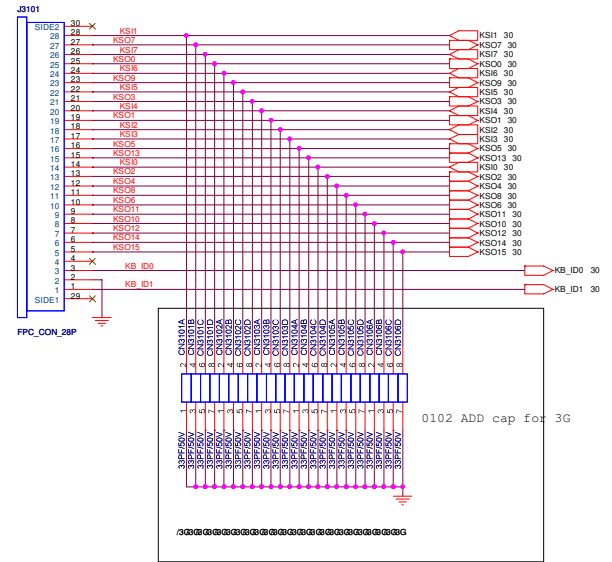
# Touch Pad



## For Switch




KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP



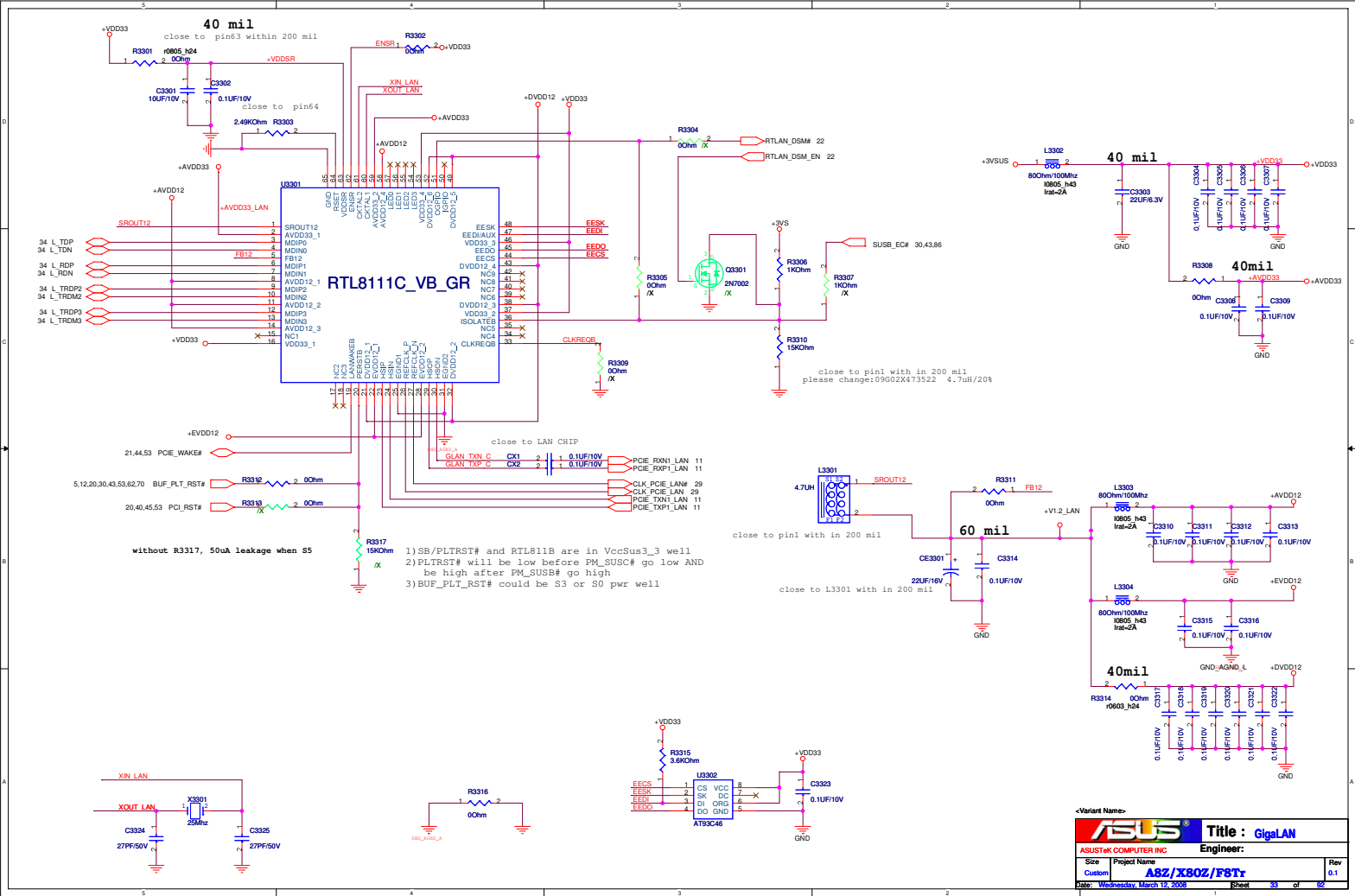
<b>ASUS</b>		<b>Title : EC_IT8511 (2/2)</b>
ASUSTeK COMPUTER INC. (NBI)		Engineer: <OrgAddr1>
Site	Project Name	Rev
Custom	ARZ/X80Z/F8T	0.1
Date: Wednesday, March 12, 2008	Sheet	31 of 92

<< MaryL\_Liu >>

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>ASZ/X80Z/F8Tr</b>	0.1
Date: <b>Wednesday, March 12, 2008</b>		Sheet <b>32</b> of <b>92</b>

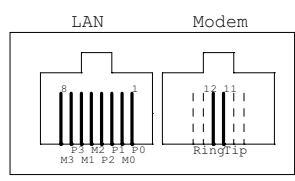
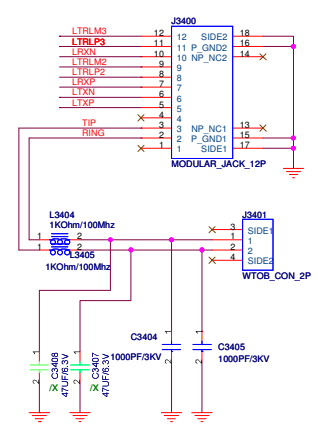
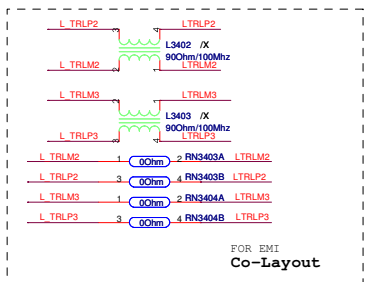
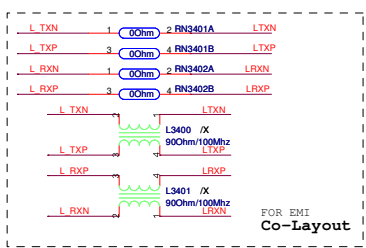
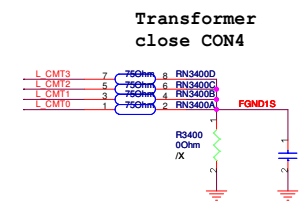
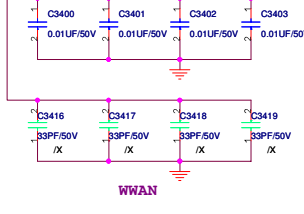
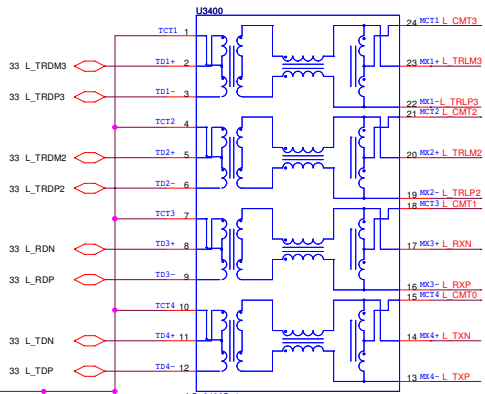
*<< MaryL\_Liu >>*





<< MaryL\_Liu >>

2402S have issue after IR reflow,  
 alternative part:LG-2410S-1



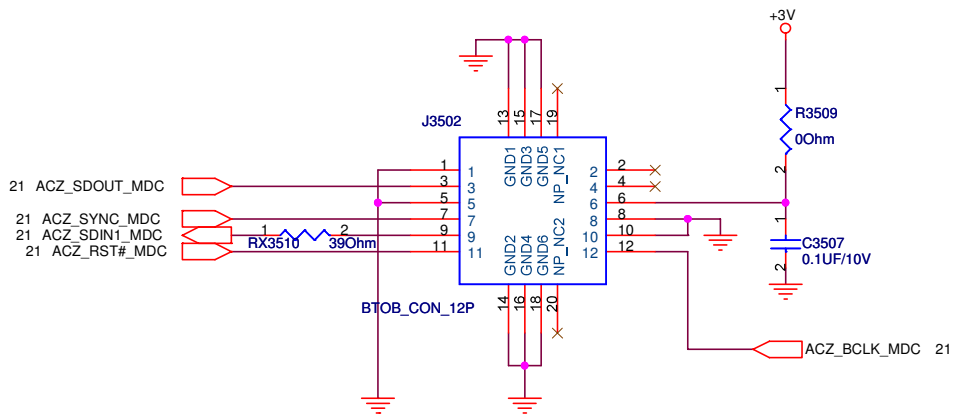
<Variant Name>

<b>ASUS</b>		<b>Title : RJ11+45</b>
ASUSTeK COMPUTER INC		Engineer:
Site:	Project Name:	
Custom	<b>A8Z/X80Z/F8T</b>	
Date: Wednesday, March 12, 2008	Sheet	34 of 92

Rev 0.1

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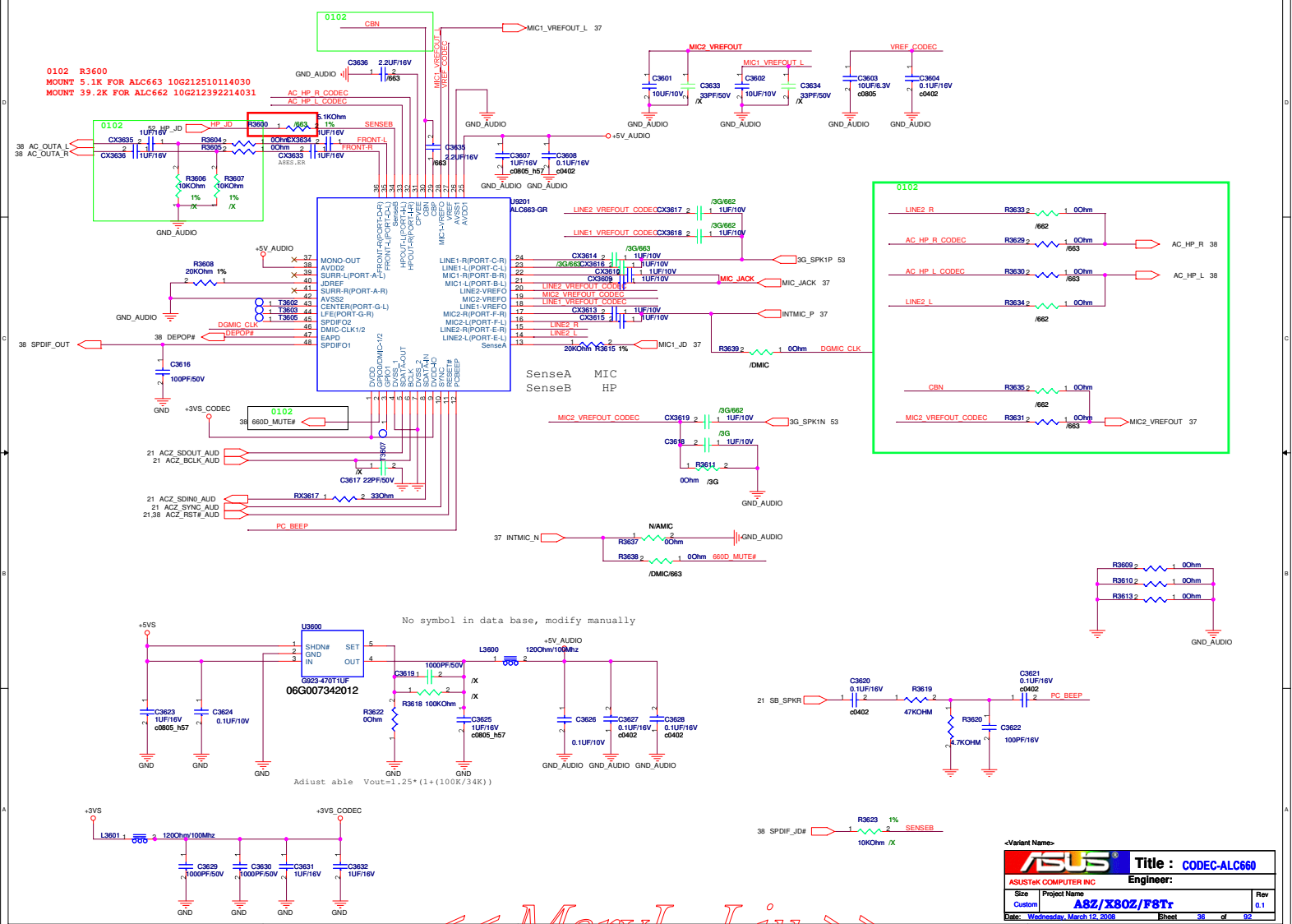
# AZALIA MDC Connector



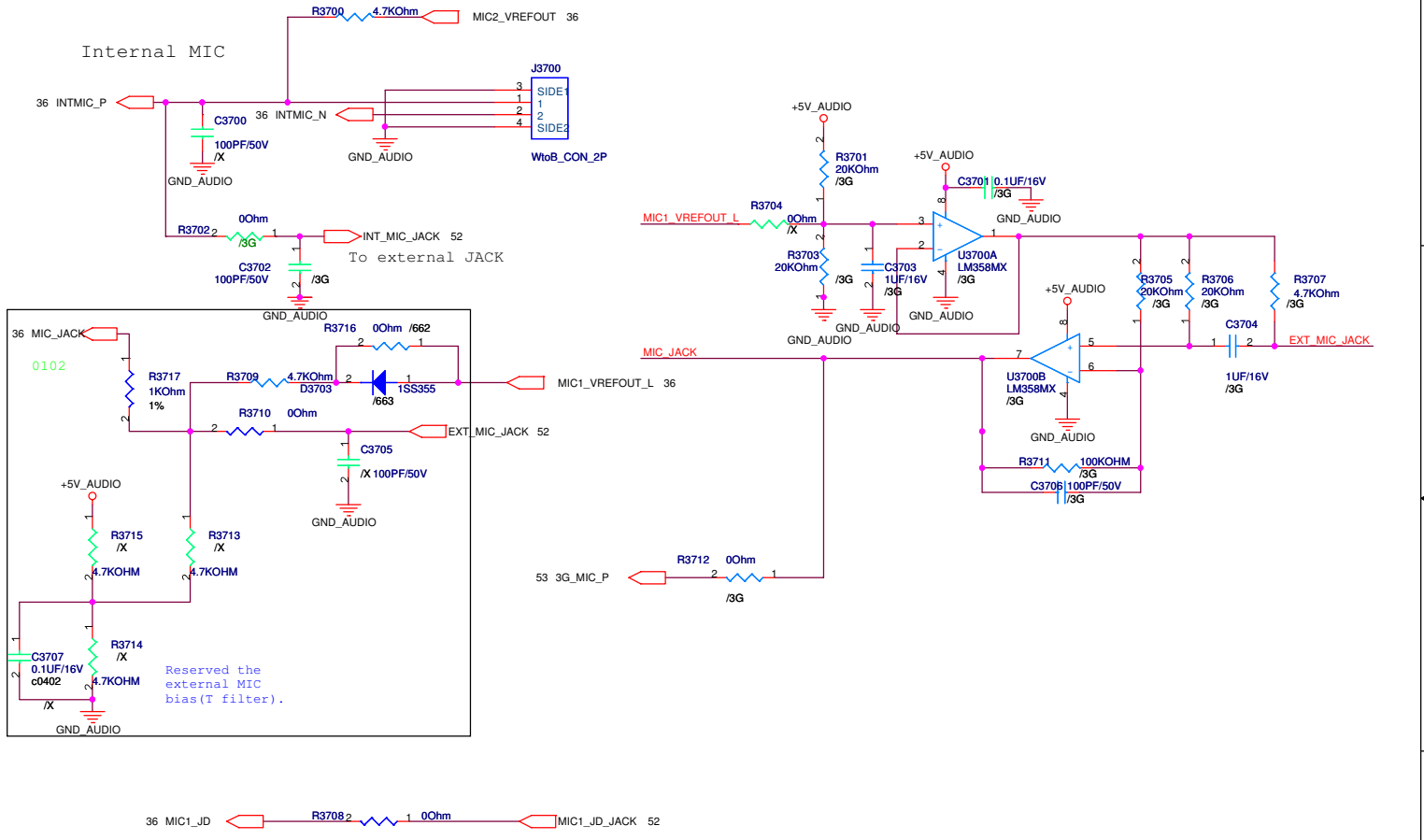
		<b>Title : MDC</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>A8Z/X80Z/F8Tr</b>		Rev 0.1
Date: Wednesday, March 12, 2008		Sheet	35 of 92

*<< MaryL\_Liu >>*

0102 R3600  
 MOUNT 5.1K FOR ALC663 106212510114030  
 MOUNT 39.2K FOR ALC662 106212392214031

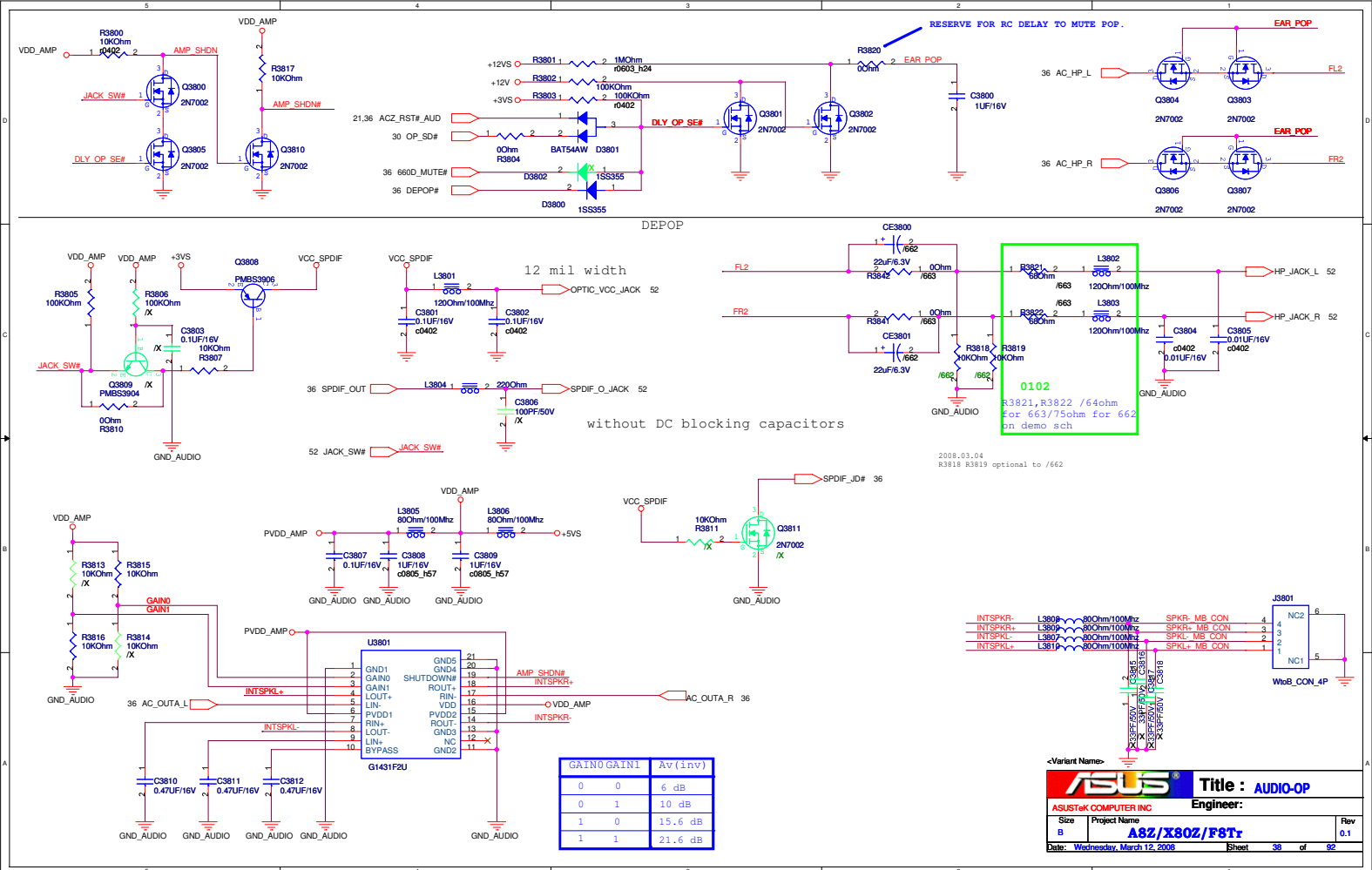


« MaryL\_Liu »



<b>ASUS</b>		<b>Title : AUDIO-MIC</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name		Rev
Custom	<b>A8Z/X80Z/F8Tr</b>		0.1
Date: Wednesday, March 12, 2008		Sheet 37 of 92	

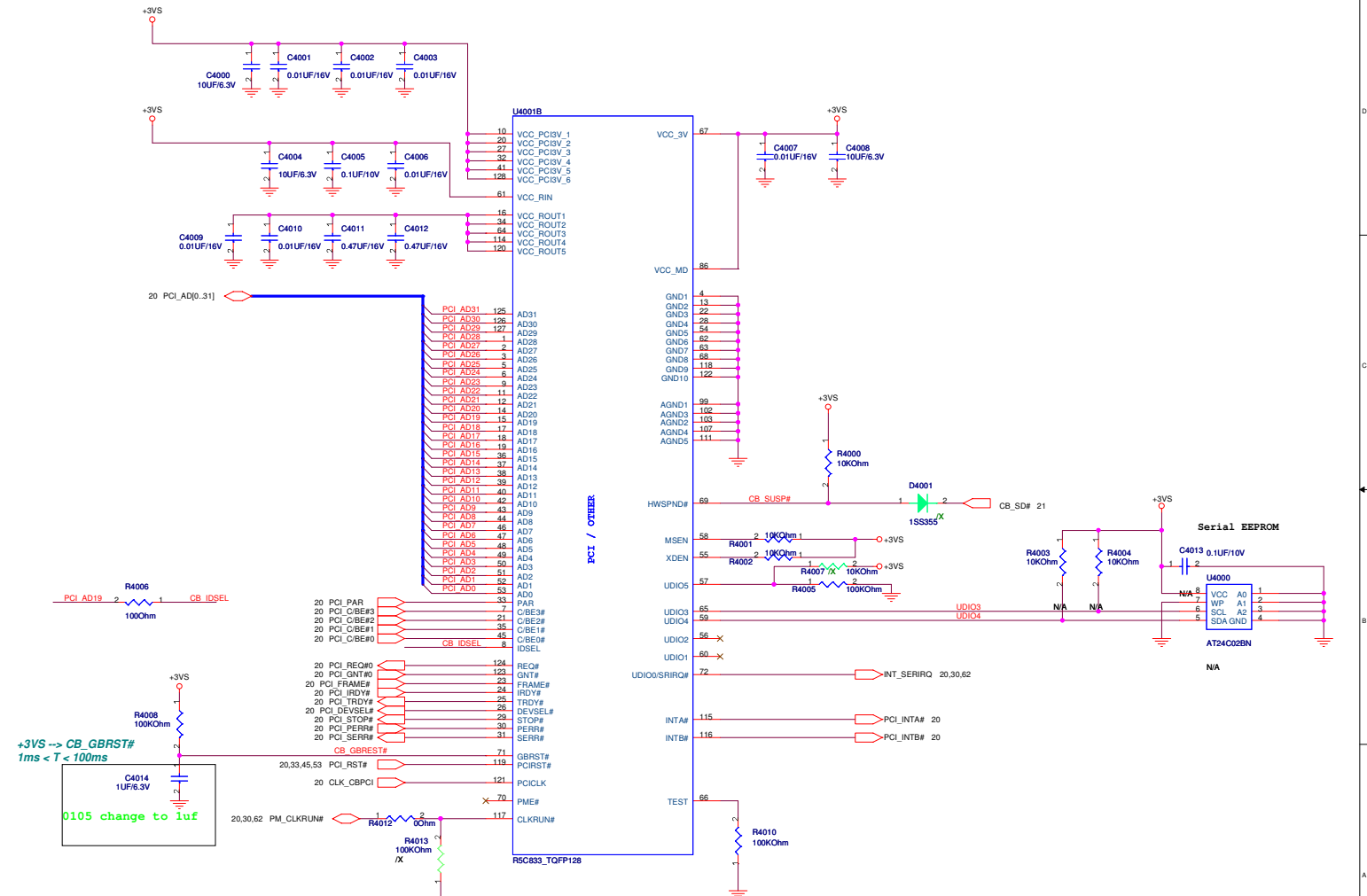
<< MaryL\_Liu >>



<< MaryL\_Liu >>

		<b>Title :</b> BLANK
ASUSTeK COMPUTER INC		<b>Engineer:</b>
<b>Size</b> A	<b>Project Name</b> A8Z/X80Z/F8Tr	<b>Rev</b> 0.1
<b>Date:</b> Wednesday, March 12, 2008		<b>Sheet</b> 39 <b>of</b> 92

*<< MaryL\_Liu >>*

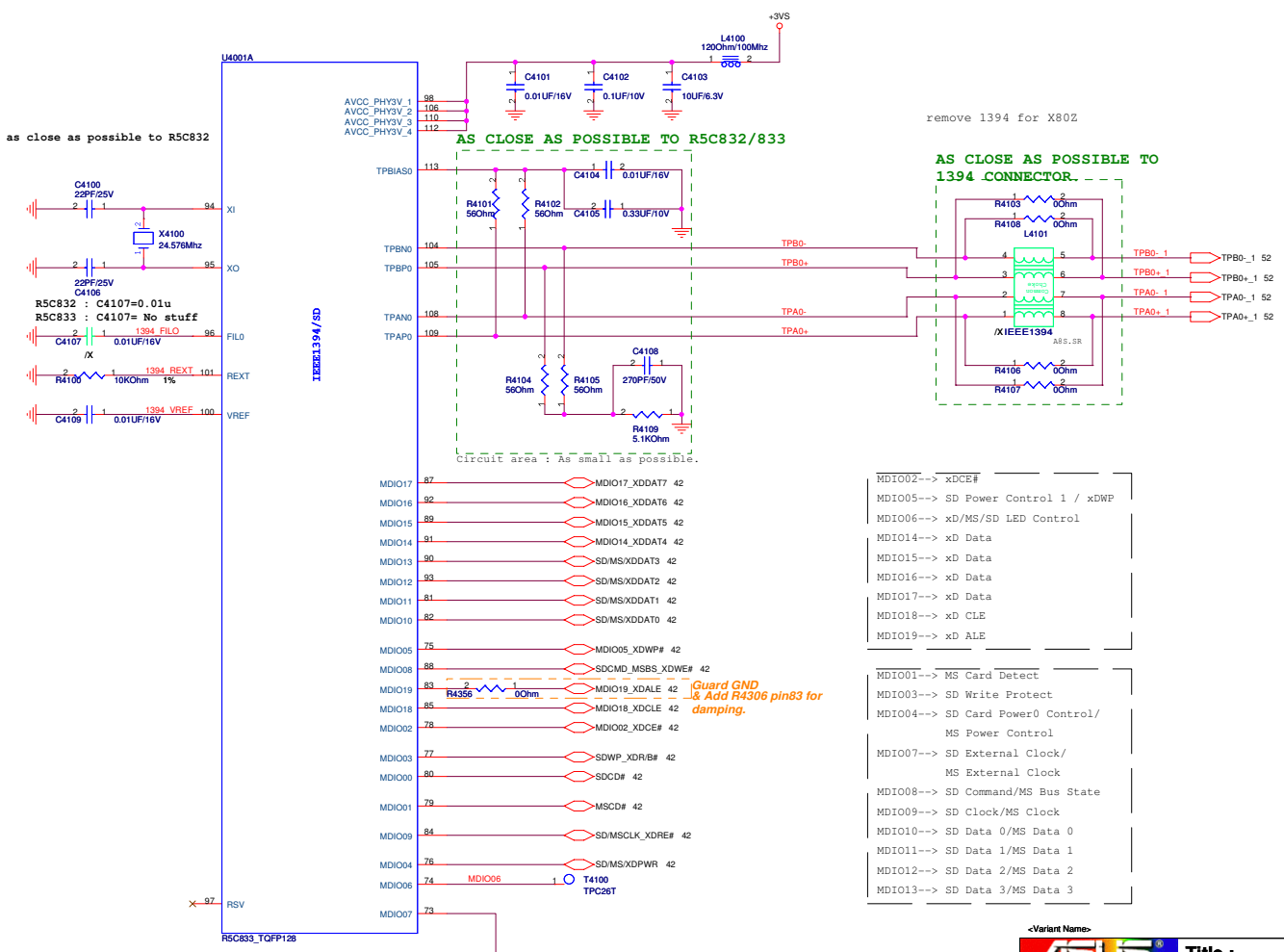


<Variant Name>

<b>ASUS</b>		<b>Title : RICOH R5C832/PCI B</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	<b>A8Z/X80Z/F8Tr</b>		0.1
Date: Wednesday, March 12, 2008	Sheet	40	of 92

<< MaryL\_Liu >>





as close as possible to R5C832

AS CLOSE AS POSSIBLE TO R5C832/833

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR

Circuit area : As small as possible.

- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE

- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/ MS Power Control
- MDIO07--> SD External Clock/ MS External Clock
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3

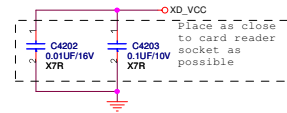
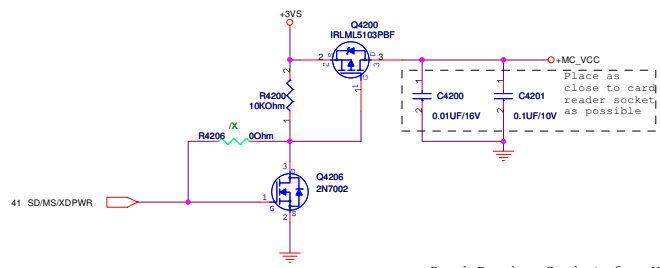
Guard GND & Add R4306 pin83 for damping.

<Variant Name>

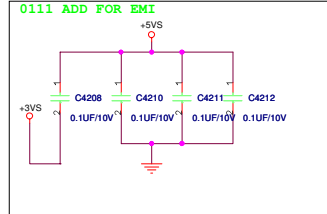
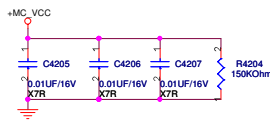
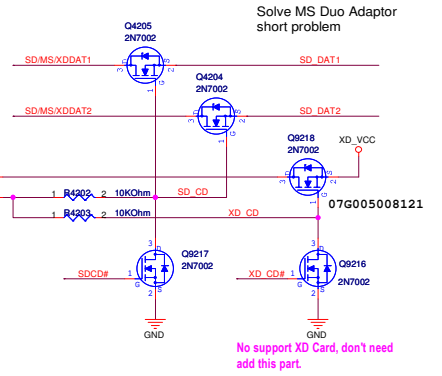
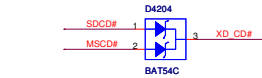
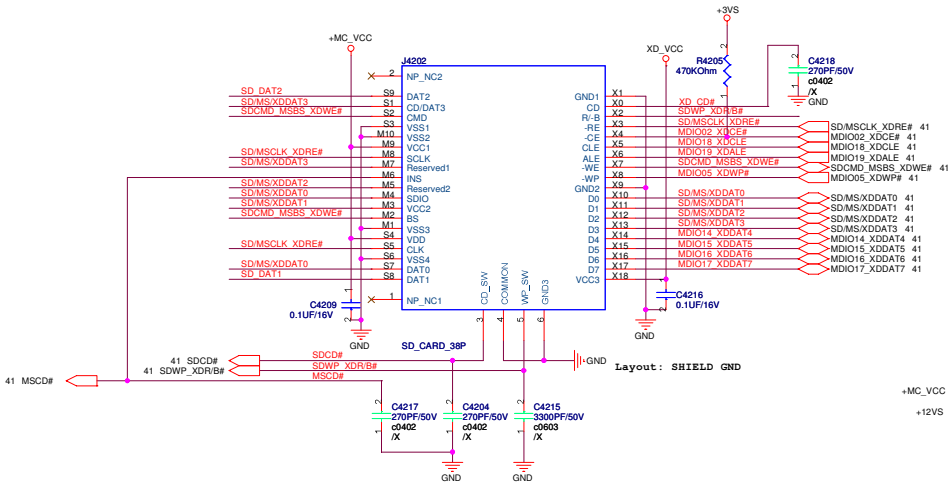
<b>ASUS</b>		<b>Title : RICOH R5C832/PCI A</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	<b>A8Z/X80Z/F8Tr</b>	0.1	
Date: Wednesday, March 12, 2008	Sheet	41	of 92

<< MaryL\_Liu >>

To correct the problem when MS Duo adaptor is in use.



remove Card Reader Socket for X80Z

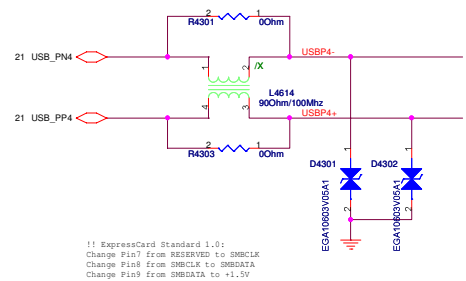
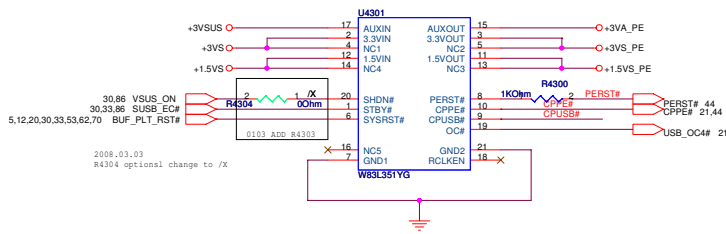


<Variant Name>

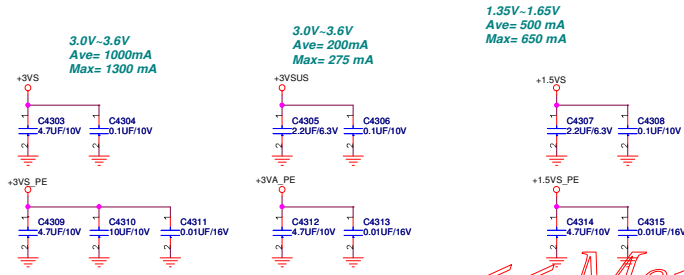
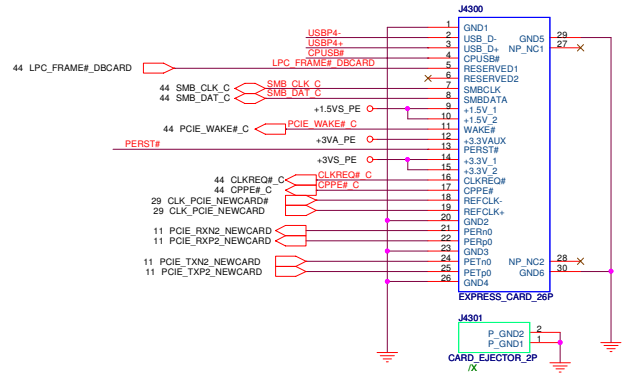
<b>ASUS</b>		<b>Title :</b> CardReader
ASUSTek COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
Custom	<b>ASZ/X80Z/F8T</b>	0.1
Date: Wednesday, March 12, 2008	Sheet	42 of 92

<< MaryL\_Liu >>

Change RICOH R5538 as 2nd source and Winbond W83L351YG (06G030091010) put on 1st source.

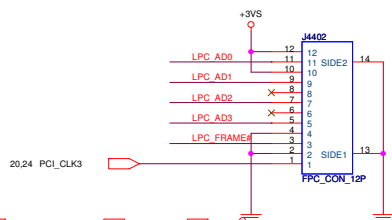
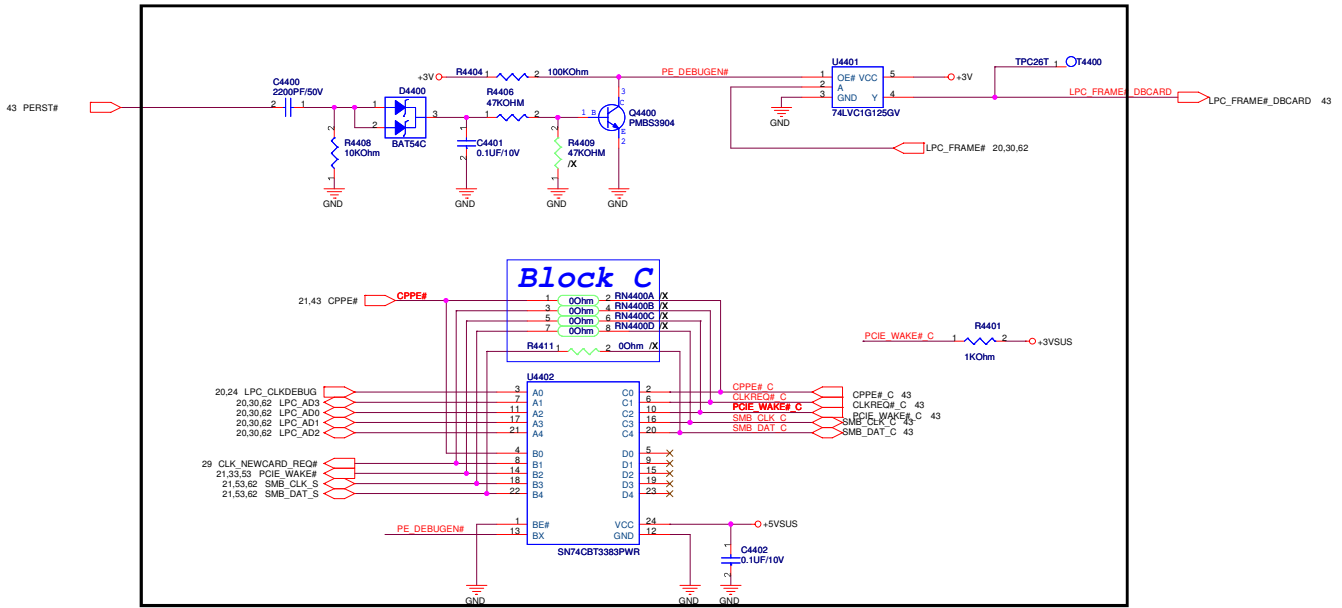


!! ExpressCard Standard 1.0:  
Change Pin7 from RESERVED to SMBCLK  
Change Pin8 from SMBCLK to SMBDATA  
Change Pin9 from SMBDATA to +1.5V



ASUS		Title : Express Card	
ASUSTeK COMPUTER INC		Engineer:	
Site:	Project Name:	Rev:	0.1
Custom:	A82/X80Z/F8T	Date:	Wednesday, March 12, 2008
Date: Wednesday, March 12, 2008		Sheet:	43 of 92

<< MaryL\_Liu >>

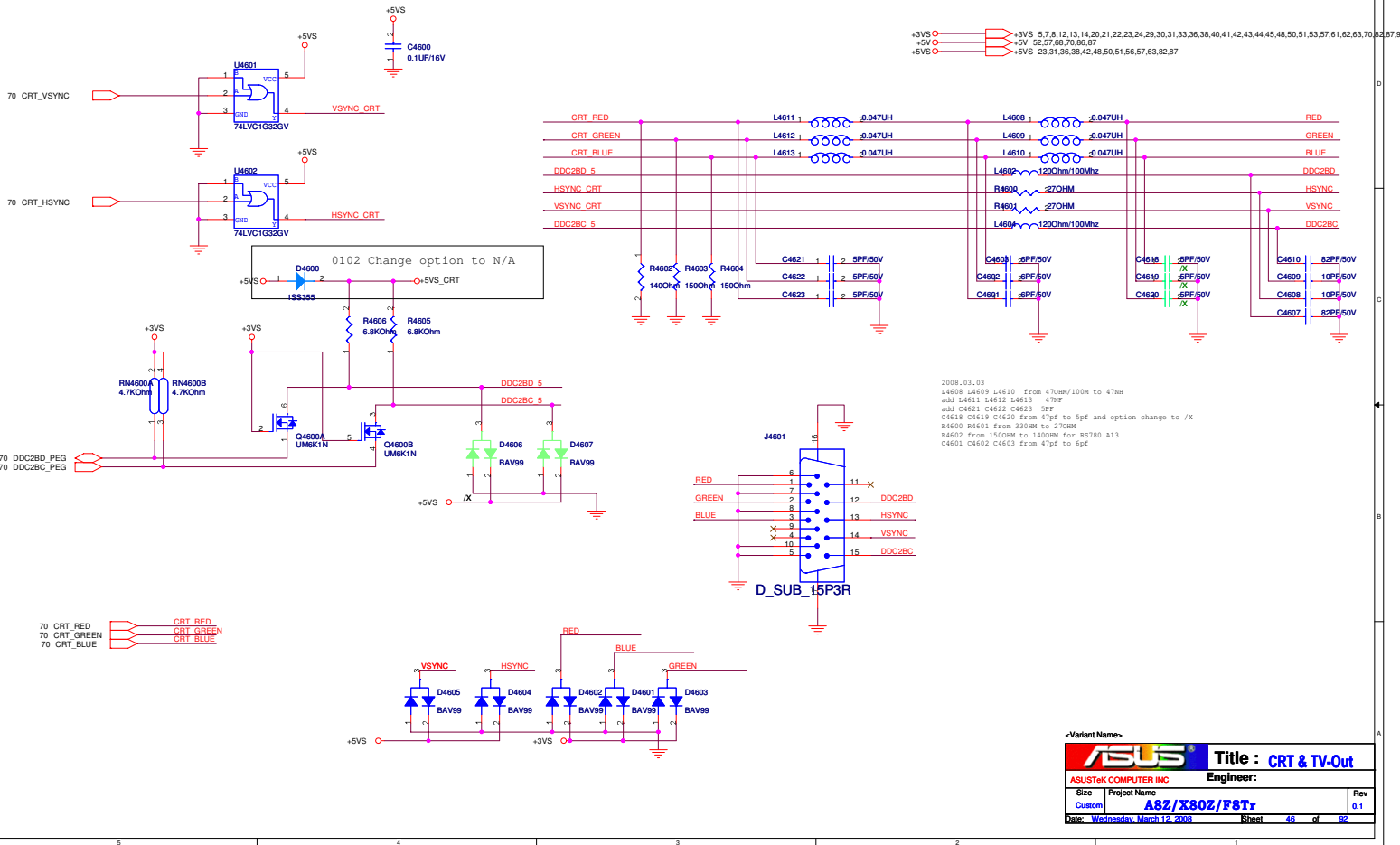


<Variant Name>


<b>ASUS</b>		<b>Title : Express Card</b>	
ASUSTeK COMPUTER INC		Engineer:	
Site:	Project Name:	Rev:	0.1
Custom:	<b>ASZ/X80Z/F8T</b>	Date:	Wednesday, March 12, 2008
Date: Wednesday, March 12, 2008		Sheet:	44 of 92

<< MaryL\_Liu >>

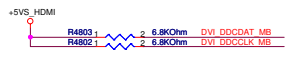
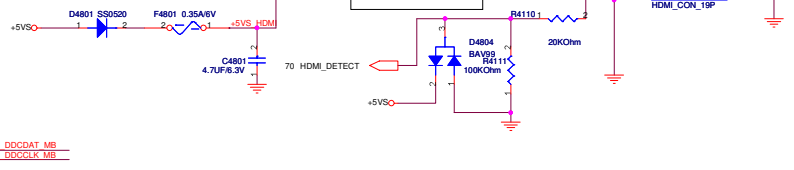
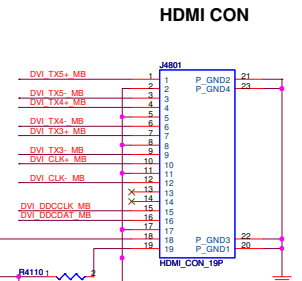
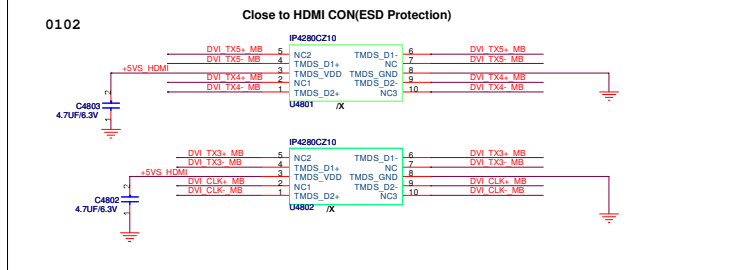




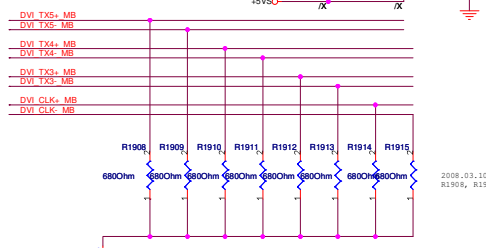
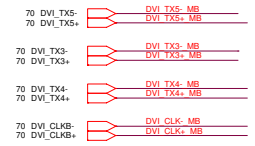
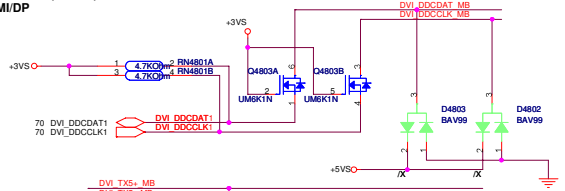
<< MaryL\_Liu >>

<Variant Name>		
		Title : DVL*****
ASUSTeK COMPUTER INC		Engineer:
Size B	Project Name <b>A8Z/X80Z/F8Tr</b>	Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 47 of 92

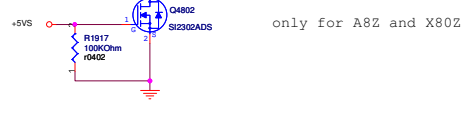
*<< MaryL\_Liu >>*



DDPC\_CTRLDATA Strapping:(Port C)  
Low = No HDMI/DP (default)  
High = HDMI/DP




2008\_03\_10  
R1908, R1909, R1910, R1911, R1912, R1913, R1914, R1915 change to 680Ohm



<b>ASUS</b>		<b>Title : HDMI</b>	
ASUSTAY COMPUTER INC. HWS		Engineer: <b>Wing Cheng</b>	
Size	Project Name	Rev	
Custom	<b>A8Z/X80Z/F8T</b>	0.1	
Date: <b>Wednesday, March 12 2008</b>		Sheet	48 of 92

<< MaryL\_Liu >>

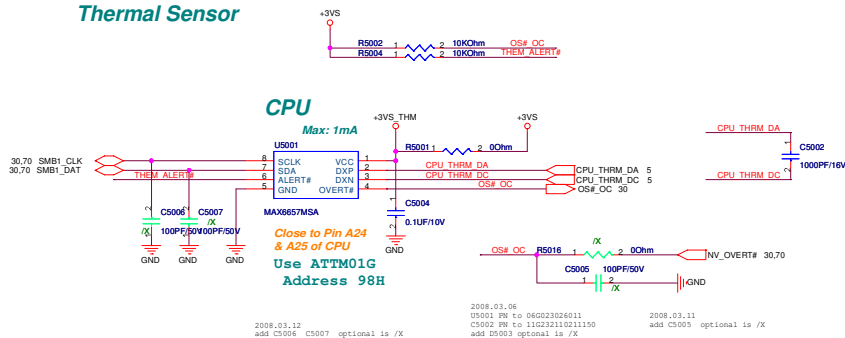


		<b>Title :</b>
ASUSTeK COMPUTER INC. NB6		<b>Engineer:</b> <i>Wing Cheng</i>
Size	Project Name	Rev
A	<b>ASZ/X80Z/F8Tr</b>	0.1
Date: <u>Wednesday, March 12, 2008</u>		Sheet <u>49</u> of <u>92</u>

*<< MaryL\_Liu >>*

### Thermal Sensor

To EC

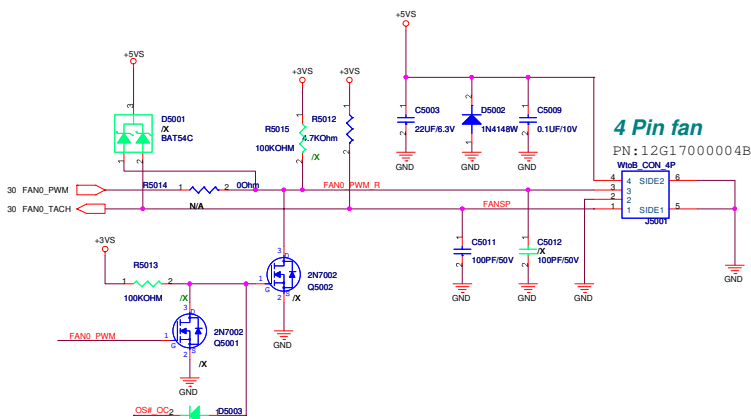


Route H\_THERMDA and H\_THERMDC on the same layer

-----OTHER SIGNALS  
15 mils  
=====GND  
10 mils  
=====H\_THERMDA(10 mils)  
10 mils  
=====H\_THERMDC(10 mils)  
10 mils  
=====GND  
15 mils  
-----OTHER SIGNALS

Avoid FSB\_Power

### DC FAN Control

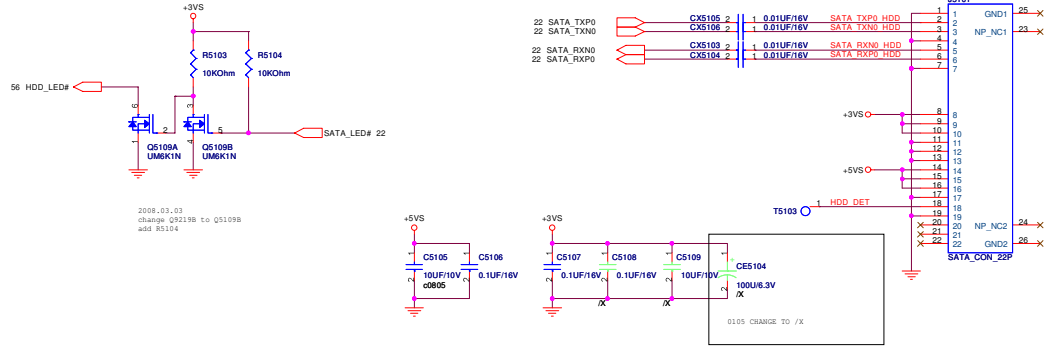


<Variant Name>

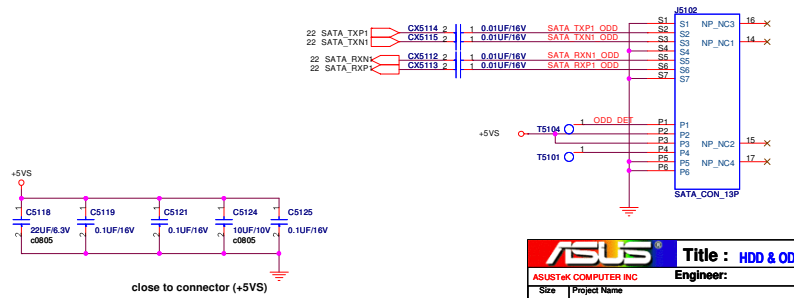
<b>ASUS</b>		<b>Title : THER SENSOR &amp; FAN</b>	
ASUSTek COMPUTER INC		Engineer: Richard Lu	
Size	Project Name		Rev
Custom	ASZ/X80Z/F8T		0.1
Date: Wednesday, March 12, 2008		Sheet	50 of 92

<< MaryL\_Liu >>

**SATA HDD CON**



**SATA ODD CON**



**ASUS** Title : HDD & ODD

ASUSTek COMPUTER INC Engineer:

Size Project Name

Custom ABZ/X80Z/F8T Rev

Date: Wednesday, March 15, 2006 Sheet 61 of 92

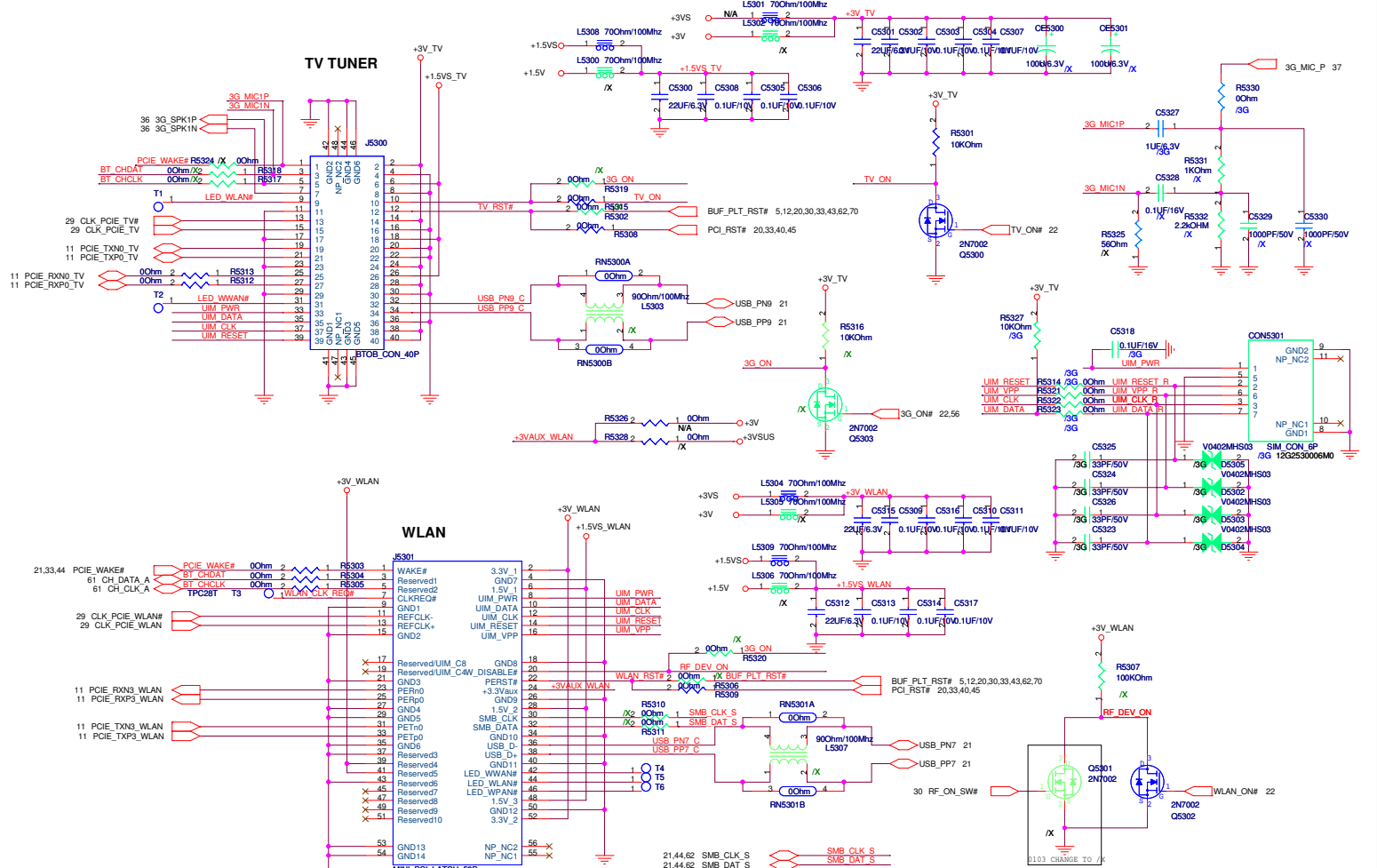
+3VS 5,7,12,13,14,20,21,22,23,24,29,30,31,33,36,38,40,41,42,43,44,45,46,48,50,53,57,61,62,63,70,82,87,91,92

+5VS 23,31,36,38,42,46,48,50,56,57,63,62,87

+5V 52,57,68,70,86,87

<< MaryL\_Liu >>





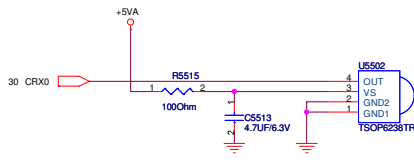
<b>ASUS</b>		<b>Title : MINI CARD</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	<b>A82/X80Z/F8T+</b>		0.1
Date: Wednesday, March 12, 2008	Sheet	33	of 82

<< MaryL\_Liu >>

		<b>Title : BLANK</b>	
ASUSTEK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	<b>ASZ/X80Z/F8Tr</b>	0.1	
Date: <b>Wednesday, March 12, 2008</b>		Sheet	54 of 92

*<< MaryL\_Liu >>*

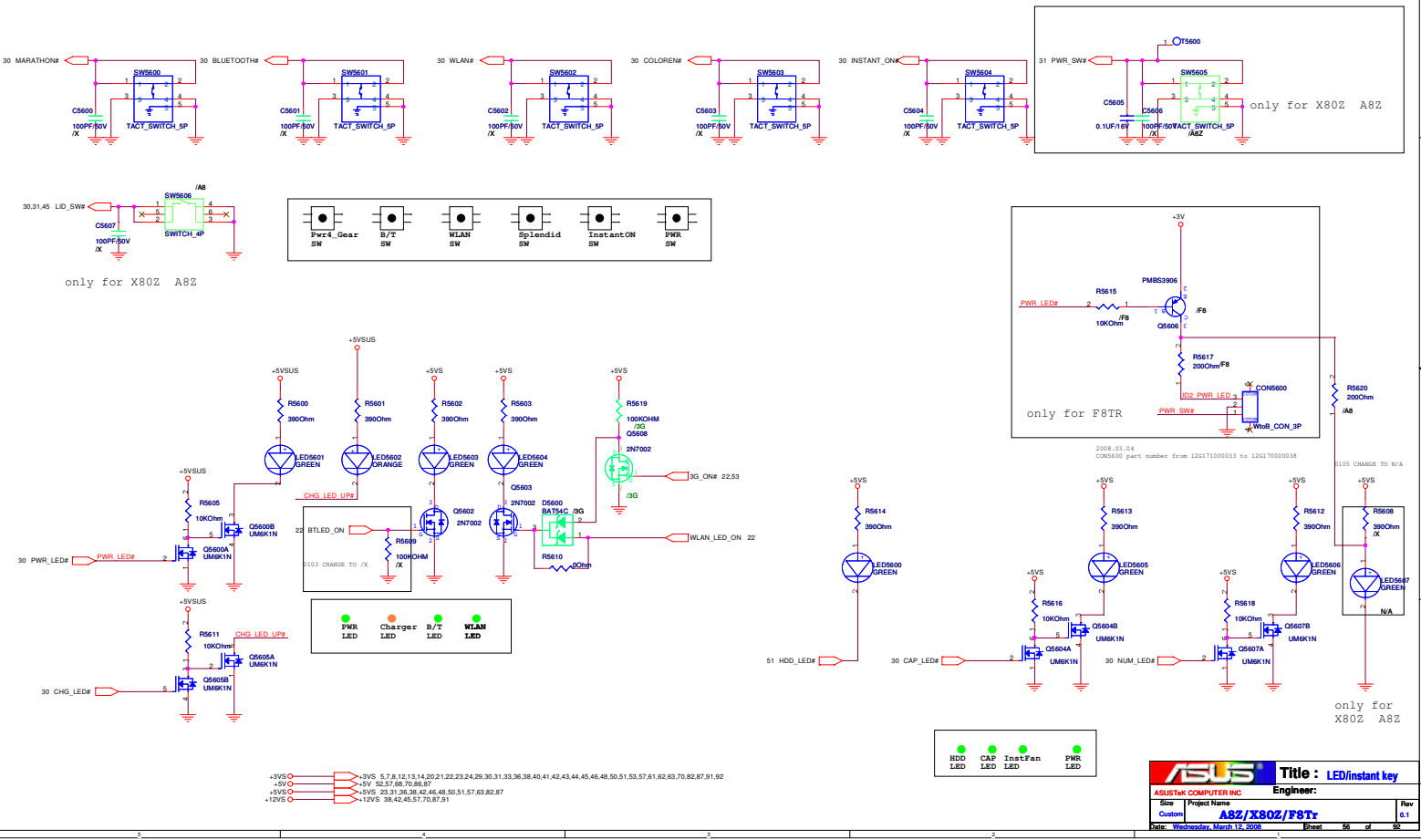
CIR  
040231020500  
TSOP6238TR



CIR for F8TR only

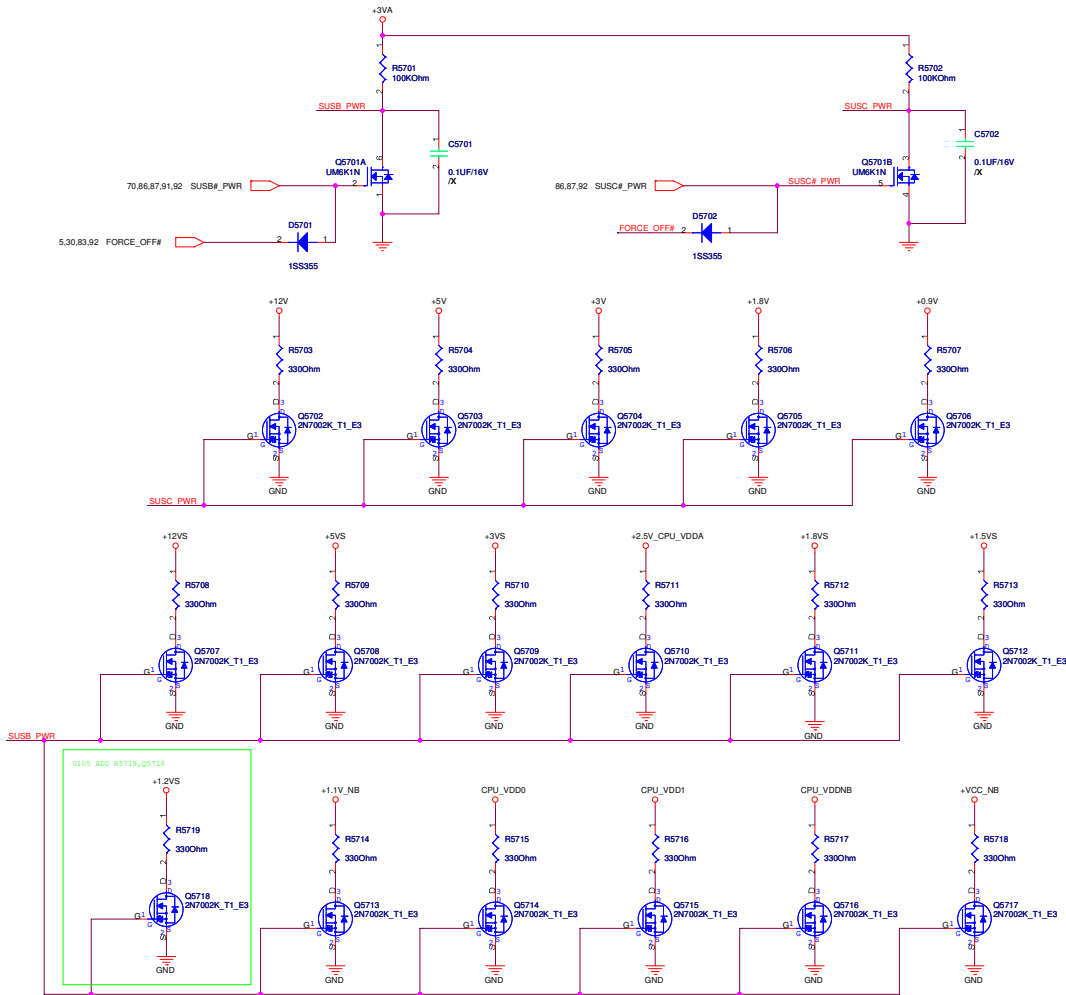
<b>ASUS</b>		<b>Title : IrDA</b>	
ASUSTeK COMPUTER INC		Engineer :	
Size	Project Name		Rev
B	A82/X80Z/F8Tr		0.1
Date: Wednesday, March 12, 2008		Sheet	55 of 82

<< MaryL\_Liu >>



<< MaryL\_Liu >>






ASUS		<b>Title : DISCHARGE</b>	
ASUSTEK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A3	F6S	2.0	
Date: Wednesday, March 12, 2008		Sheet 57 of 92	

<< MaryL\_Liu >>

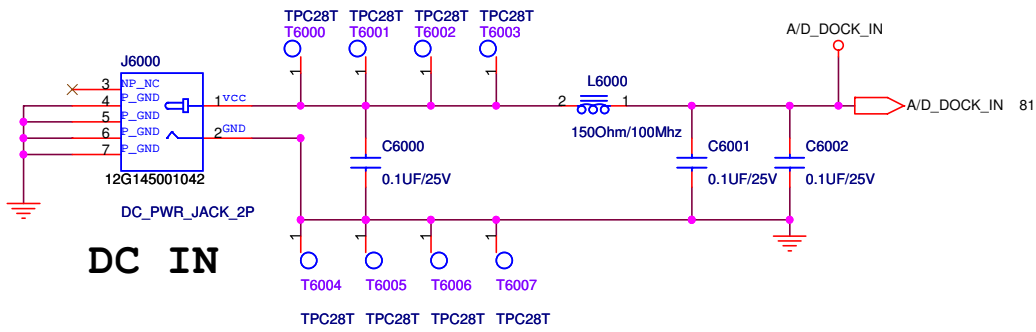
<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>ASZ/X80Z/F8Tr</b>	0.1
Date: <u>Wednesday, March 12, 2008</u>		Sheet of 92

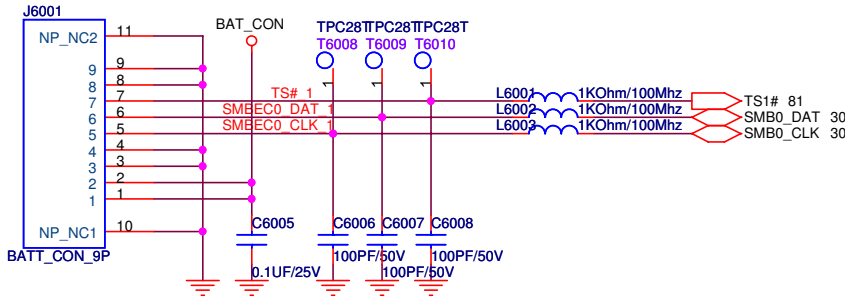
*<< MaryL\_Liu >>*

Title		
<Title>		
Size	Document Number	Rev
A	A8Z/X80Z/F8Tr	0.1
Date:	Wednesday, March 12, 2008	Sheet 59 of 92

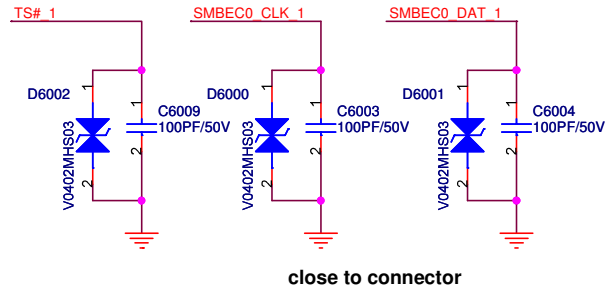
*« MaryL\_Liu »*



### DC IN



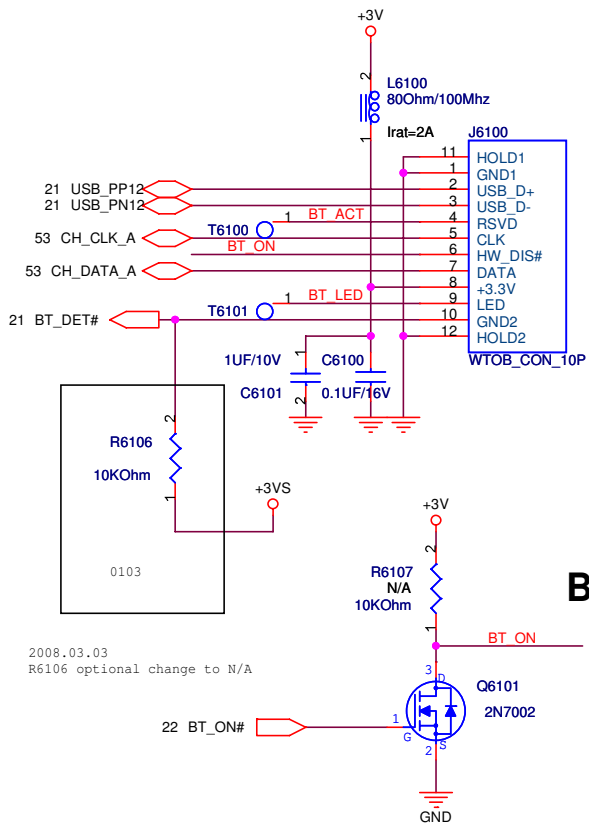
### Battery Connector



<Variant Name>

<b>ASUS</b>		<b>Title : DC IN / BAT</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name <b>A8Z/X80Z/F8Tr</b>		Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 60 of 92	

<< MaryL\_Liu >>



remove bluetooth for X80Z

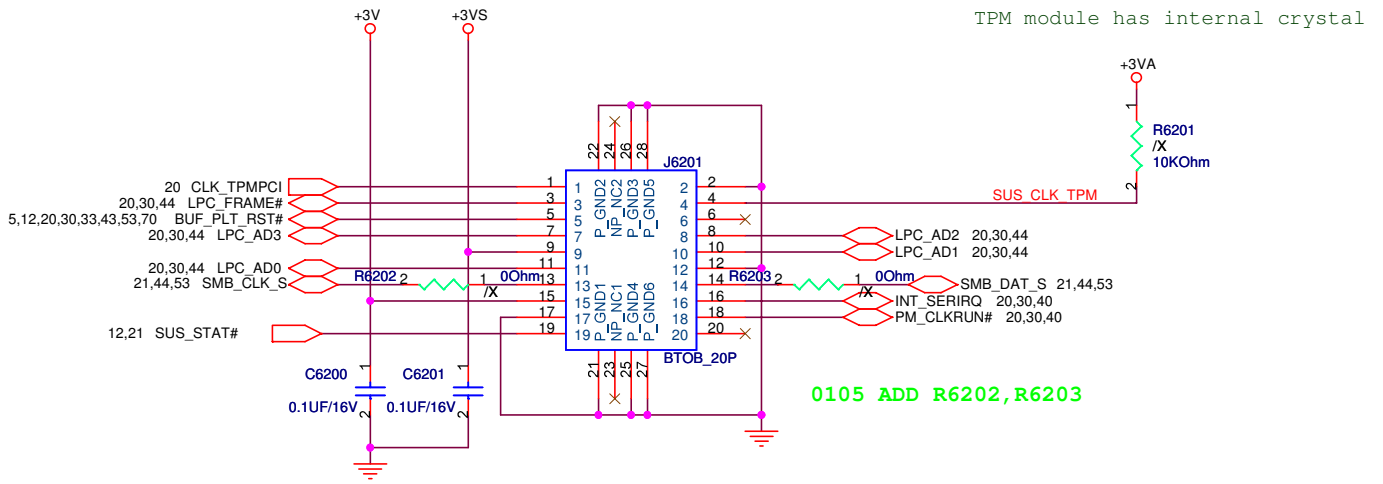
### Bluetooth Module CON

2008.03.03  
R6106 optional change to N/A

<b>ASUS</b>		<b>Title : BT/CAMERA</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>ASZ/X80Z/F8Tr</b>		Rev 0.1
Date: <b>Wednesday, March 12, 2008</b>		Sheet	61 of 92

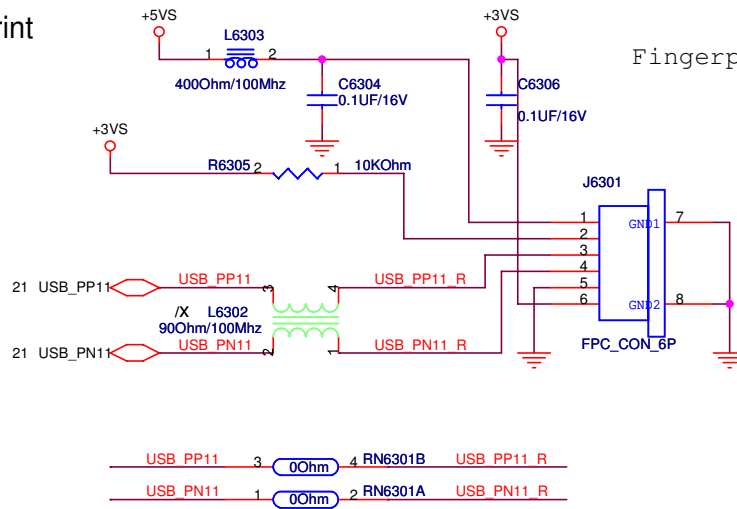
<< MaryL\_Liu >>

# TPM 1.2 Module



# Finger Print

Fingerprint for F8TR only



<Variant Name>

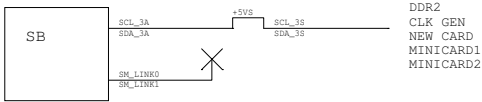
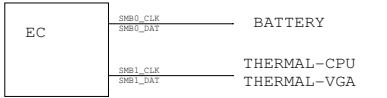
		<b>Title :FingerPrinter</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name		Rev
A	<b>A8Z/X80Z/F8Tr</b>		0.1
Date: Wednesday, March 12, 2008		Sheet	63 of 92

«Maryl\_Liu»

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 ( Internal )		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)  
**SM-Bus Mapping** 1001100



## BOM option

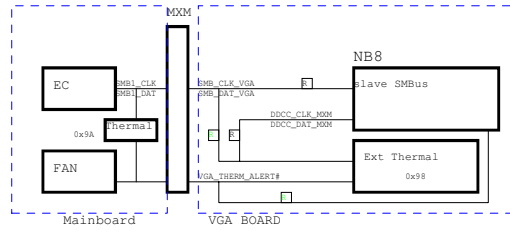
nGM:yellow  
nPM:light red  
=====

@ : no stuff for all  
nGM :no stuff for A8E  
nPM :no stuff for A8S  
nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance  
3G :for Windigo,SIERRA MC8775V  
nA8E :no stuff Irda for A8E

## Support ID2:

Support ID2:  
page 68,Finger print  
page 55,IR  
Page 56,pwr switch and LED

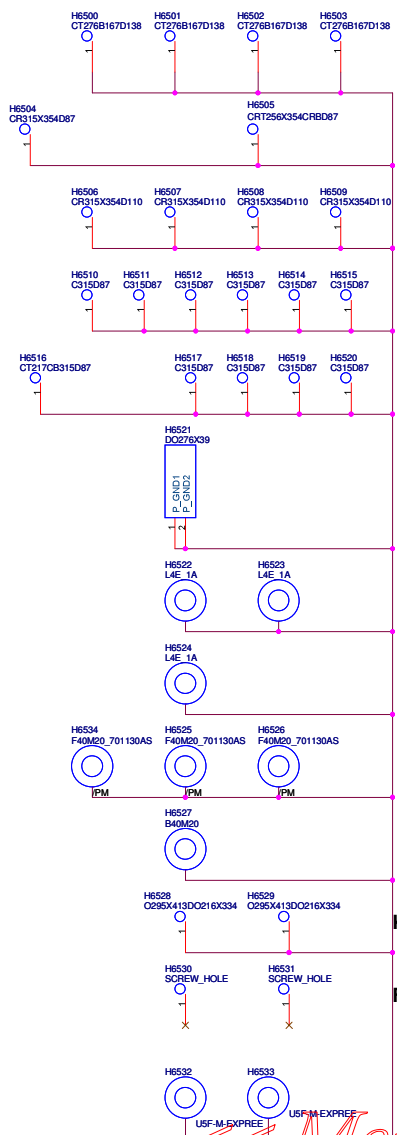
## Thermal block diagram



ASUS		Title :
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
B	A8Z/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008	Sheet	64 of 92

<< MaryL\_Liu >>



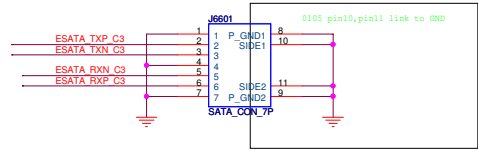


CPU  
SCREW  
U HOLE  
SCREW  
IO Board  
MDC\_NUT  
TPM\_NUT  
VGA\_NUT  
KB\_NUT  
KEYBOARD  
FIXED HOLE

←← MaryL\_Liu →→  
miniCard

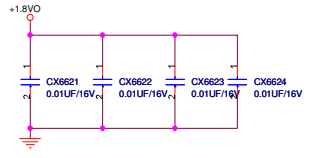
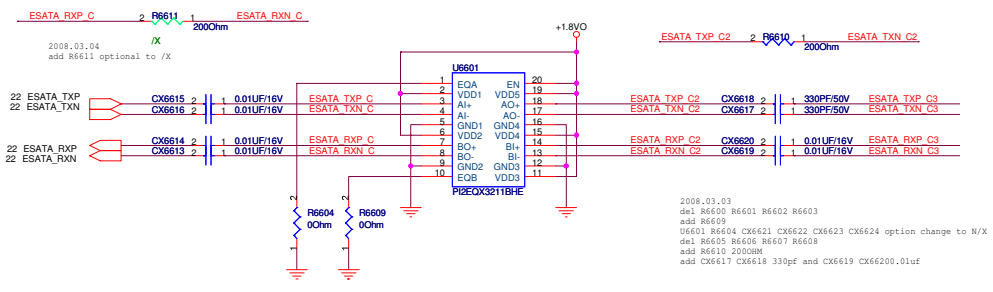
Title		Rev	
Document Number		0.1	
Customer: A8Z/X90Z/F8T			
Date: Wednesday, March 12, 2008	Sheet	65	of 92

PIN	FUNCTION
1	Gnd
2	A+
3	A-
4	Gnd
5	B-
6	B+
7	Gnd



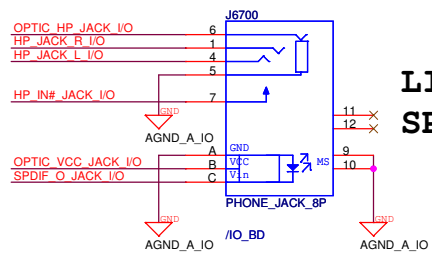
remove E-SATA for X80Z

0109 add re-driver

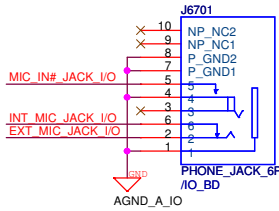


<b>ASUS</b>		<b>Title : E-SATA</b>
ASUSTek COMPUTER INC		Engineer:
Size	Project Name	Rev
B	<b>A8Z/X80Z/F8Tr</b>	0.1
Date: Wednesday, March 12, 2008		Sheet 66 of 92

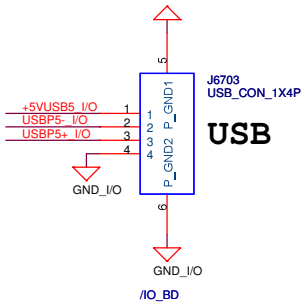
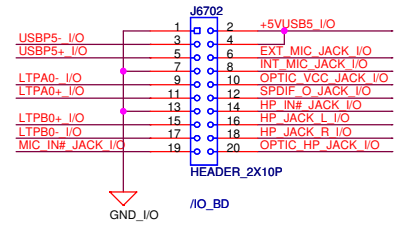
<< MaryL\_Liu >>



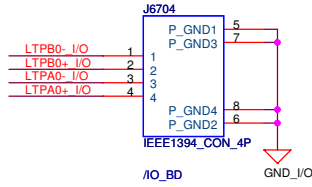
**LINE\_OUT  
SPDIF**



**MIC**

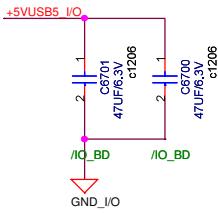


**USB**

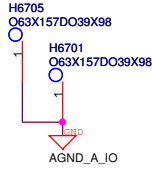
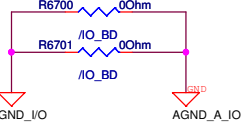


**1394A**

remove 1394 for X80Z



2008.03.10  
add C6700 C6701

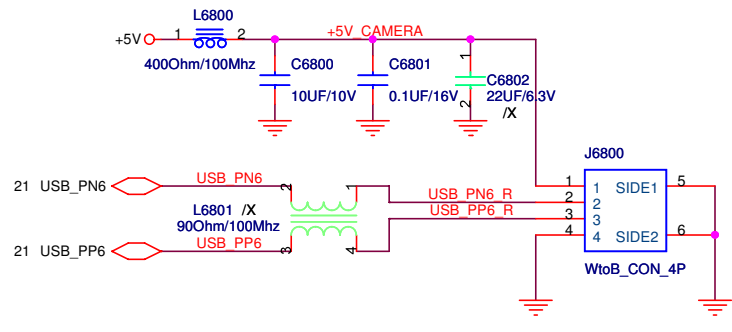


<Variant Name>

<b>ASUS</b>		<b>Title :SUB_PCB</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name <b>A8Z/X80Z/F8Tr</b>	Date: Wednesday, March 12, 2008	Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 67	of 92

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# Camera



<Variant Name>

		<b>Title :CAMERA</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name		Rev
A	<b>A8Z/X80Z/F8Tr</b>		0.1
Date: Wednesday, March 12, 2008		Sheet	60 of 92

*<< MaryL\_Liu >>*

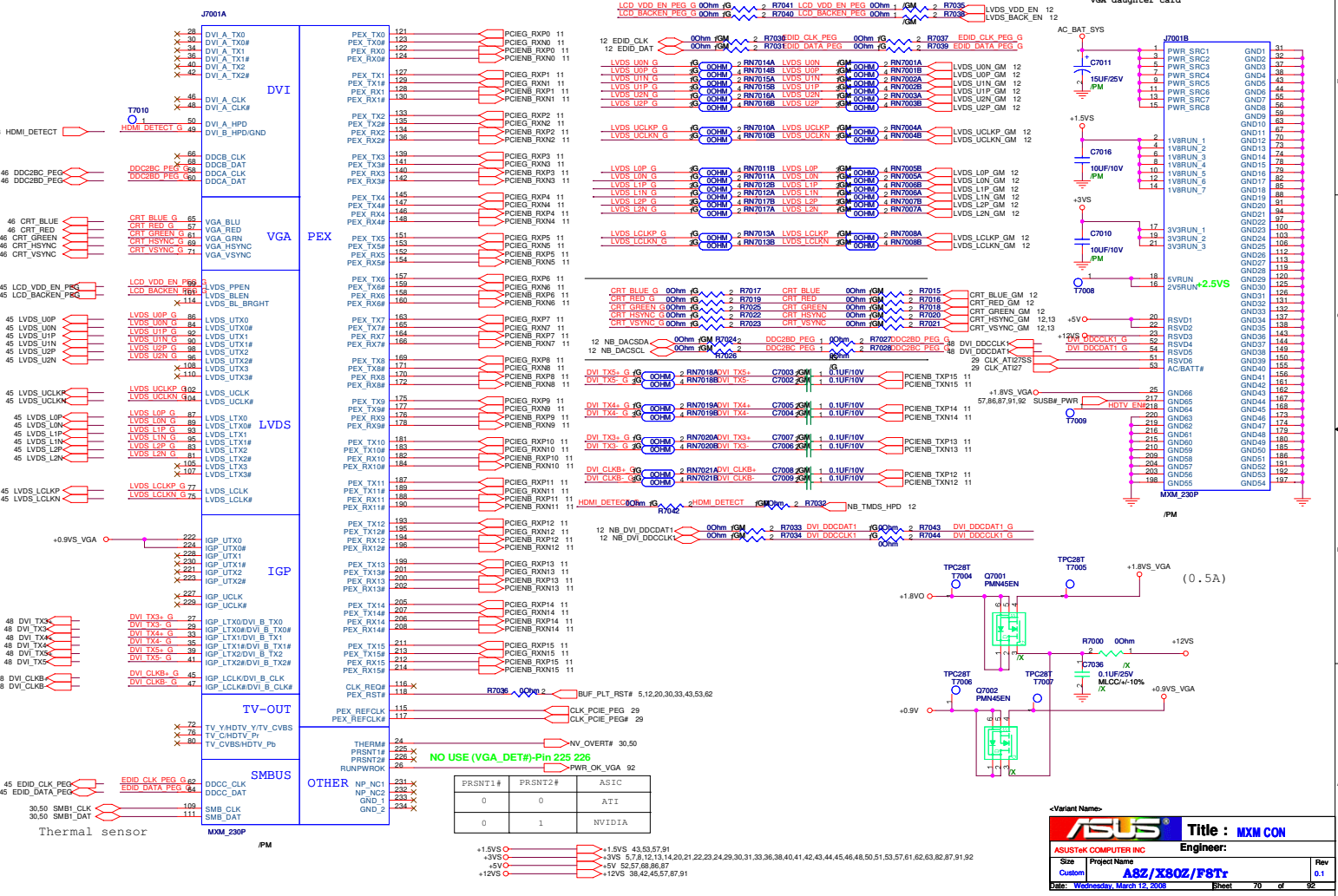
		<b>Title :</b> Other
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>ASZ/X80Z/F8Tr</b>	0.1
Date: Wednesday, March 12, 2008		Sheet 69 of 92

*<< MaryL\_Liu >>*

only for F8TR

RESISTORS CLOSE TO MXM

+2.5VS design always on VGA daughter card



NO USE (VGA\_DET#)-Pin 225 226

PRSENT1#	PRSENT2#	ASIC
0	0	ATI
0	1	NVIDIA

- +1.5VS 43,53,57,51
- +3VS 5,7,8,12,13,14,20,21,22,23,24,29,30,31,33,36,38,40,41,42,43,44,45,46,48,50,51,53,57,61,62,63,62,87,91,92
- +12VS 38,42,45,57,87,91

ASUS Title: MXM CON

ASUSTEK COMPUTER INC Engineer:

Size Project Name: A8Z/X80Z/F8TR Rev: 0.1

Custom Date: Wednesday, March 12, 2008 Sheet: 70 of 82

<< MaryL\_Liu >>

D

D

C

C

B

B

A

A

<< *MaryL\_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 71 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< *MaryL\_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 72 of 82



D

D

C

C

B

B

A

A

<< *MaryL\_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/FST	0.1
Date:	Wednesday, March 12, 2008	Sheet 73 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< *MaryL\_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F6T1	0.1
Date:	Wednesday, March 12, 2008	Sheet 74 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< *MaryL\_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 75 of 82

D

D

C

C

B

B

A

A

<< *MaryL\_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 78 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< MaryL\_Liu >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F6T1	0.1
Date:	Wednesday, March 12, 2008	Sheet 77 of 82

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	<b>A8Z/X80Z/F8Tr</b>	0.1	
Date: Wednesday, March 12, 2008		Sheet	78 of 92

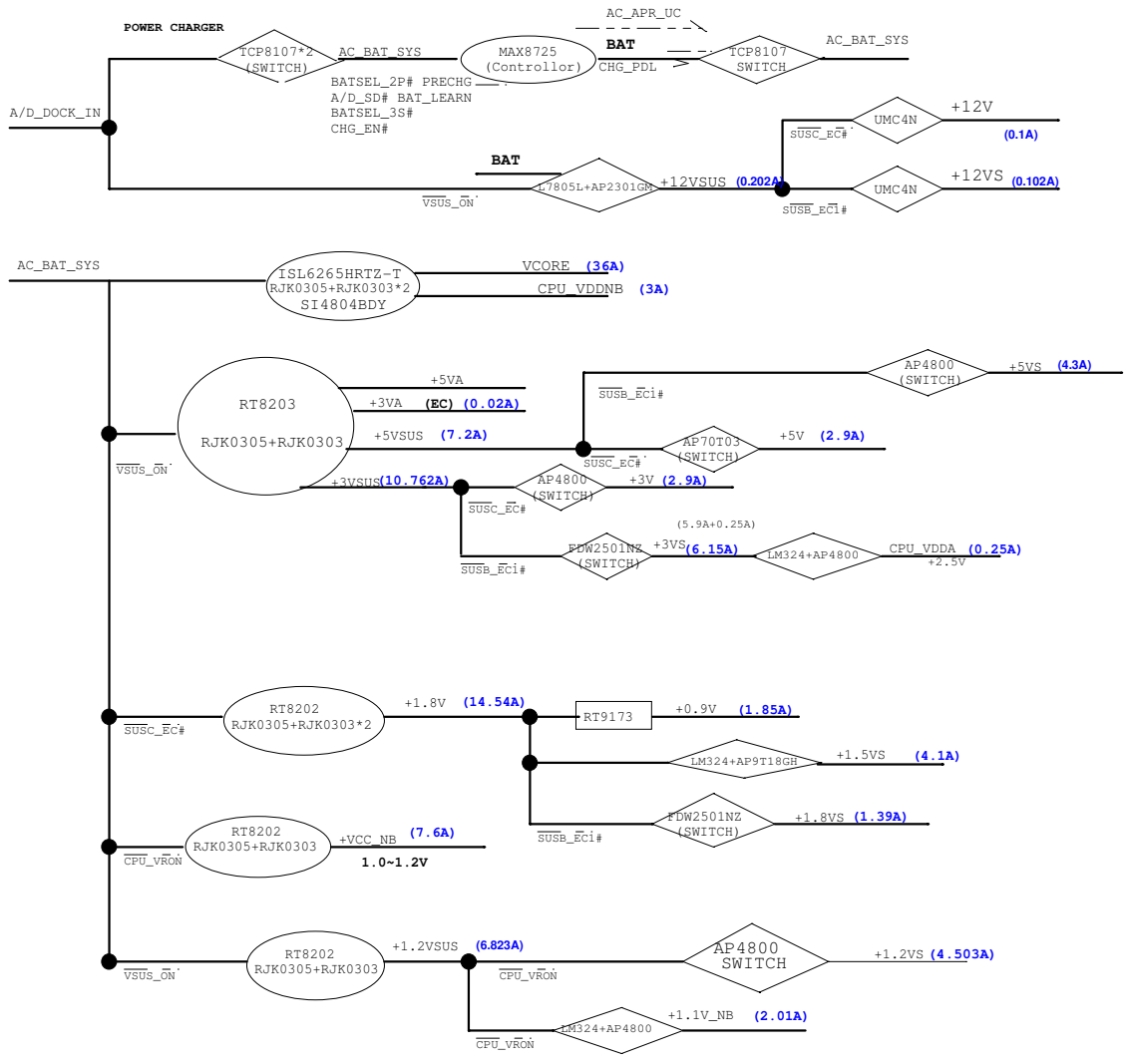
*<< MaryL\_Liu >>*

# REVISION LIST

---

		TIME : History
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
AS2	AS2/ X302/ FSTy	1.0
Date: 2010/05/10 10:00:00 AM		Page 11 of 11

<< MaryL\_Liu >>



Variant Name:

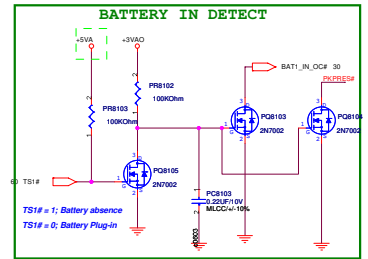
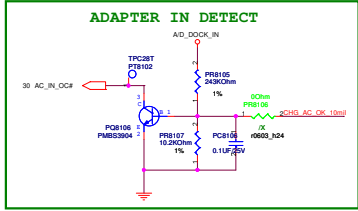
<b>ASUS</b>		<b>Title : POWER FLOW</b>	
ASUSTEK COMPUTER INC		Engineer: N/A	
Size:	Project Name:	Rev:	1.0
Drawn by:	<b>PETR</b>	Checked:	
Date: Wednesday, March 12, 2008		Sheet:	80 of 82

<< MaryL\_Liu >>



# POWER PATH & BAT\_LEARN

AC\_IN Threshold 2.049Vmax AD\_DOCK\_IN > 15.70V active  
 Adapter Inhibit = 0.075V/Rsense(ADIN)[VCLSLVREF]  
 Rsense=0.01515 Ohm  
 VCLSL = 3.301V  
 => Constant Power = 19 \* 4.5 = 85.5W  
 => P 85.5/15=5.70A/PR5100=100V  
 Charge Current Ichg = 0.075V/Rsense(CHG)[VCTL3.6V]  
 Rsense(CHG)= 15m Ohm  
 VICTL= 1.850V => Ichg = 2.63A  
 VICTL= 1.810V => Ichg = 1.401A  
 VICTL= 1.810V => Ichg = 1.401A  
 VICTL= 1.550V  
 => Vsel = 4.2V  
 VICTL= 0.8V or DCIN < 7V -> Charger Disable



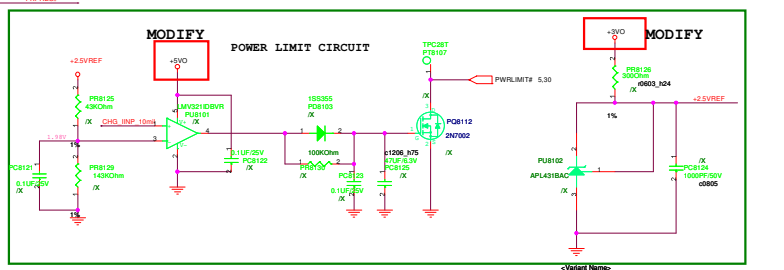
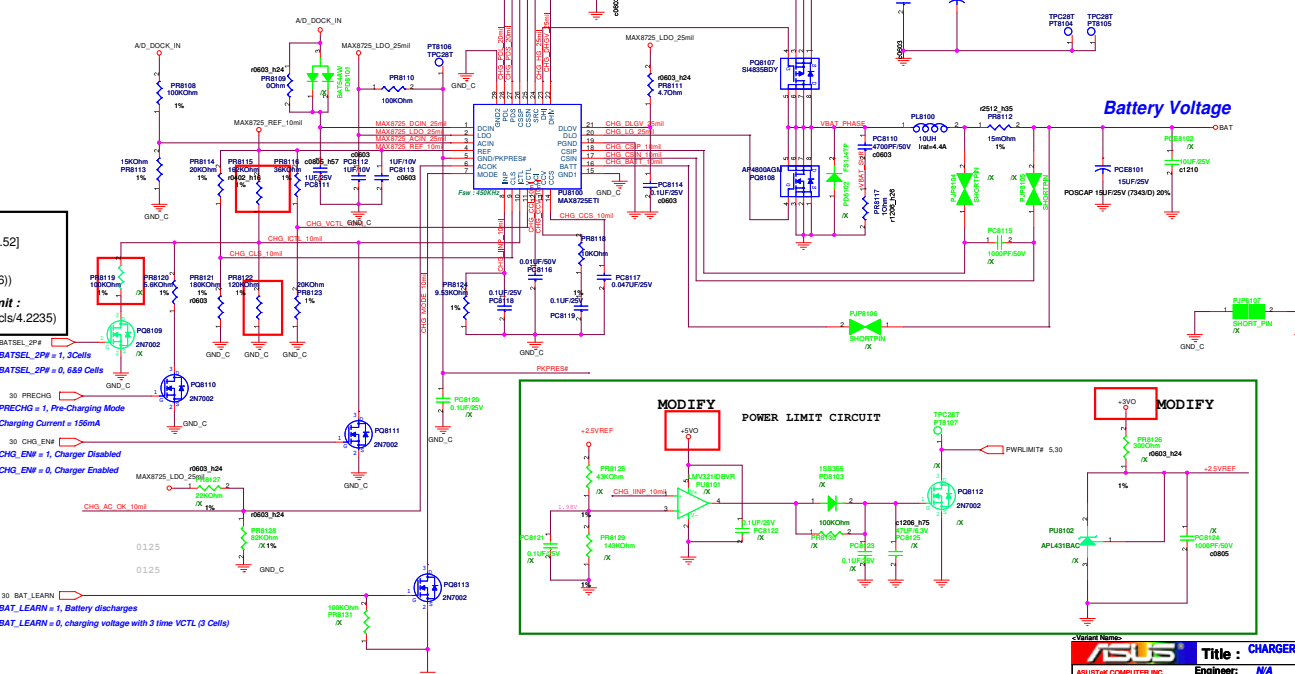
**MODE (Pin7) Battery**  
 High (>2.8V) 4-Cell  
 Low (<0.8V) 3-Cell  
 High Impedance Battery Learn  
 (1.6V-Vmoco=2V) Battery Learn

MAX8725\_REF : 4.2235V  
 MAX8725\_LDO : 5.4V

**Battery Charging Voltage :**  
 +V\_BAT = 4 x [4.2235 + (VctL-1.8)/9.52]  
**Battery Charging Current :**  
 Icharge = (0.075/PR5706) x (VctL/3.6)  
**Input Adaptor Max. Current Limit :**  
 Ilimit\_current = (0.075/PR5701) x (Vds/4.2235)

**Pre-Charging Mode :**  
 Precharging current = 190.5mA  
 VctL = 0.137V  
**BATSEL\_2P# = 1, 3Cells**  
**BATSEL\_2P# = 0, 6Cell**  
**PRECHG = 1, Pre-Charging Mode**  
 Charging Current = 156mA  
 => Icharge = 1.469A  
**BATSEL\_2P# = 0, 6 Cells; VctL = 1.836V**  
 => Icharge = 2.55A  
**CHG\_EN# = 1, Charger Enabled**  
**CHG\_EN# = 0, Charger Disabled**

A/D\_SDI# = 1, Enable charger  
 A/D\_SDI# = 0, Disable charger  
 30 BAT\_LEARN = 1, Battery discharges  
 BAT\_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

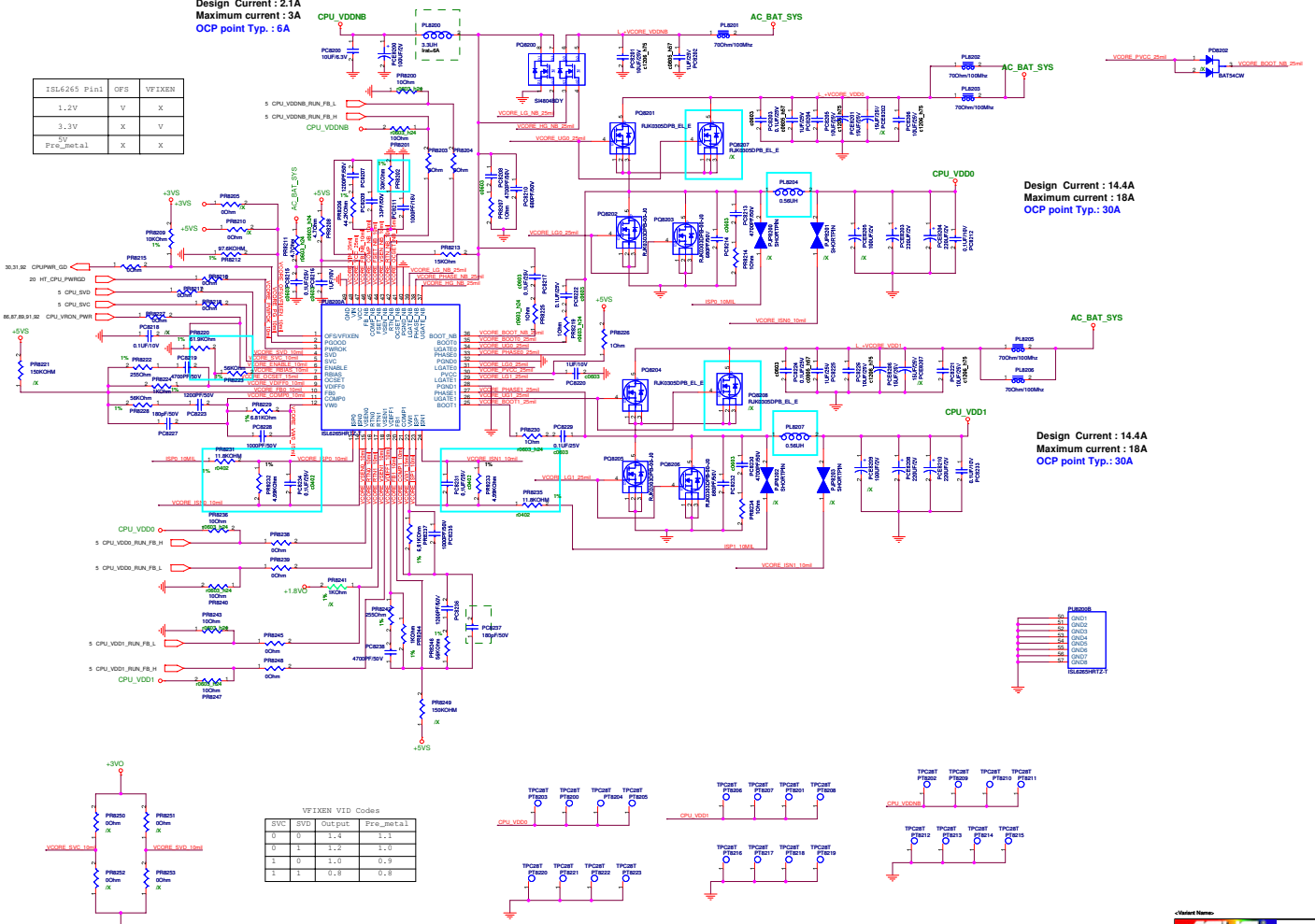


ASUS		Title: CHARGER
ASUSTEK COMPUTER INC.		Engineer: N/A
Size	Project Name	Rev
C	P6TR	1.0
Date: Wednesday, March 12, 2008	Sheet: 81	of 85

<< MaryL\_Liu >>

ISL6245 Pin#	QFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X
Pre_Metal	X	X

Design Current : 2.1A  
Maximum current : 3A  
OCP point Typ. : 6A



Design Current : 14.4A  
Maximum current : 18A  
OCP point Typ. : 30A

Design Current : 14.4A  
Maximum current : 18A  
OCP point Typ. : 30A

VFIXEN VID Codes

SVC	SVID	Output	Pre_Metal
0	0	1.8	1.8
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.9	0.8

ASUS TITLE : VCORE  
ASUSTeK COMPUTER INC. Engineer: MFA  
Rev: 1.0  
Date: 2008.03.10  
PSTR

<< MaryL\_Liu >>



5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< MaryL\_Liu >>

		Title : <Title>	
<OrigName>		Engineer: <i>chang-sheng liu</i>	
Size	Project Name	Rev	
A3	<Doc>	1.00	
Date: <i>Wednesday, March 12, 2008</i>		Sheet <i>84</i> of <i>92</i>	

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

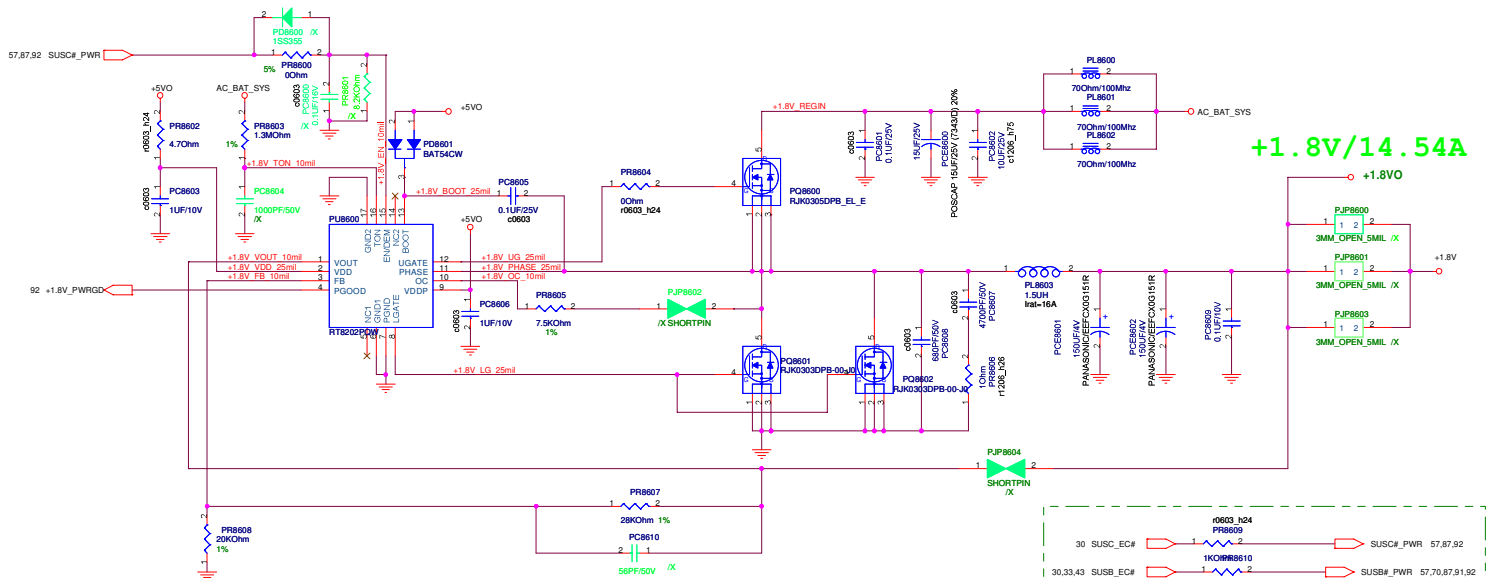
3

2

1

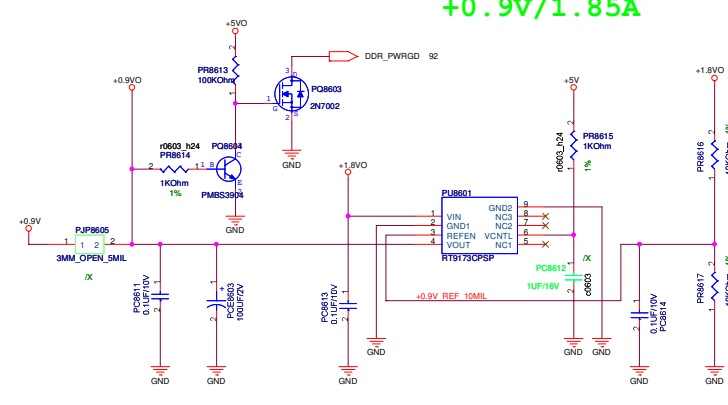
		Title : <Title>	
-<CrgName>		Engineer: <i>chang-sheng_liu</i>	
Size	Project Name	Rev	
A3	<Doc>	1.00	
Date: <i>Wednesday, March 19, 2008</i>		Sheet	85 of 92

<< *MaryL\_Liu* >>

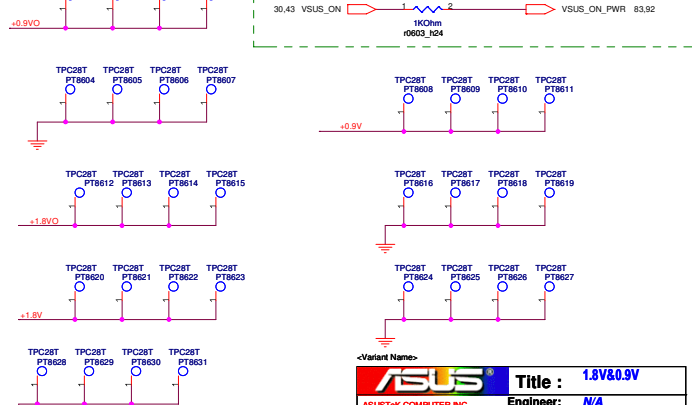


**+1.8V/14.54A**

+1.8V



**+0.9V/1.85A**



-0.9V

-0.9V

+1.8V

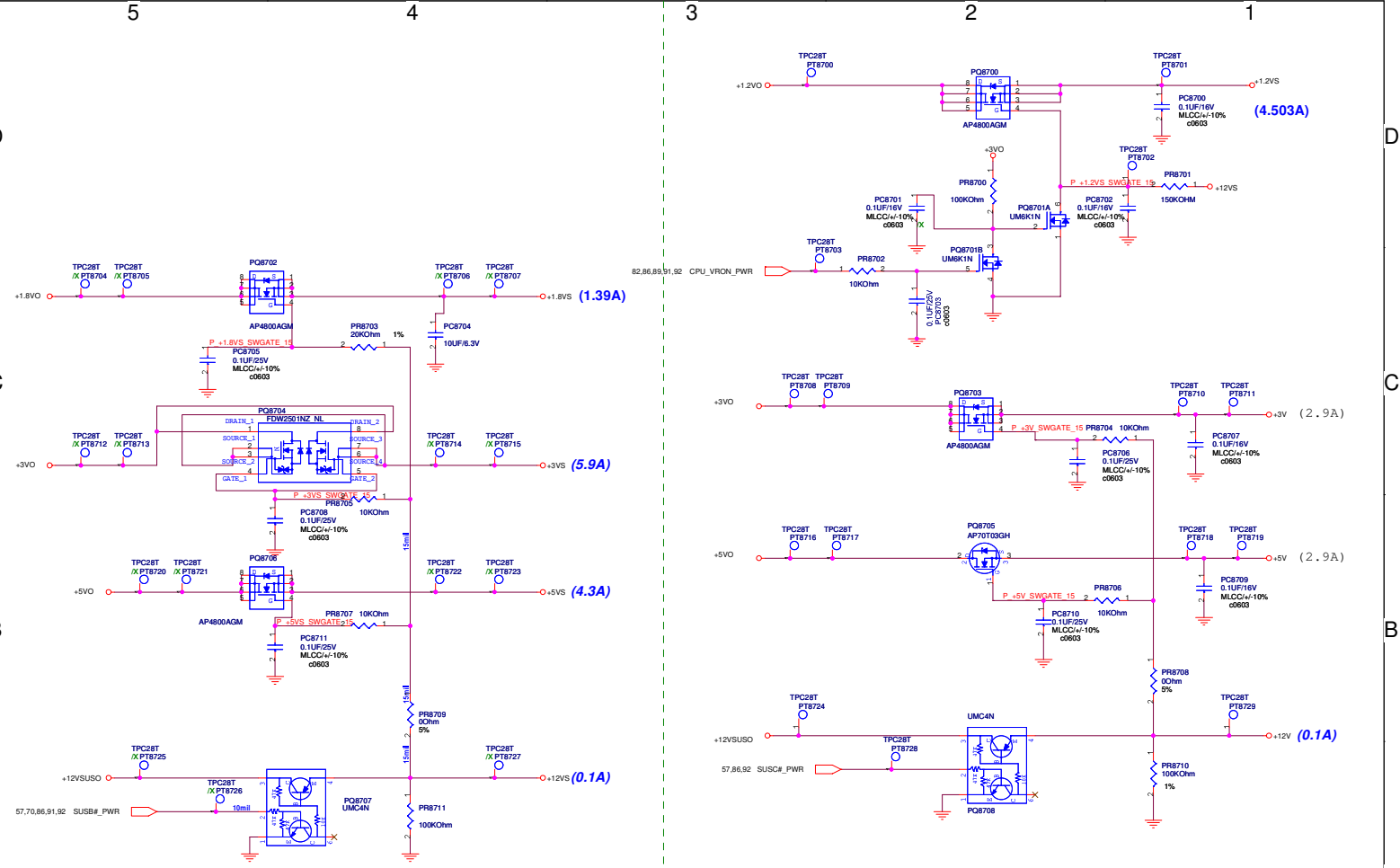
+1.8V

+1.8V

<Variant Name>

<b>ASUS</b>		<b>Title :</b> 1.8V&0.9V
ASUSTeK COMPUTER INC		<b>Engineer :</b> N/A
Size	Project Name	Rev
Custom	<b>F6TR</b>	1.0
Date: Wednesday, March 12, 2008	Sheet	86 of 92

<< MaryL\_Liu >>



<Variant Name>

<b>ASUS</b>		<b>Title : LOAD SWITCH</b>
ASUSTeK COMPUTER INC		Engineer: N/A
Site	Project Name	Rev
A3	P6TR	1.0
Date: Wednesday, March 12, 2008	Sheet	87 of 92

<< MaryL\_Liu >>

D

D

C

C


B

B

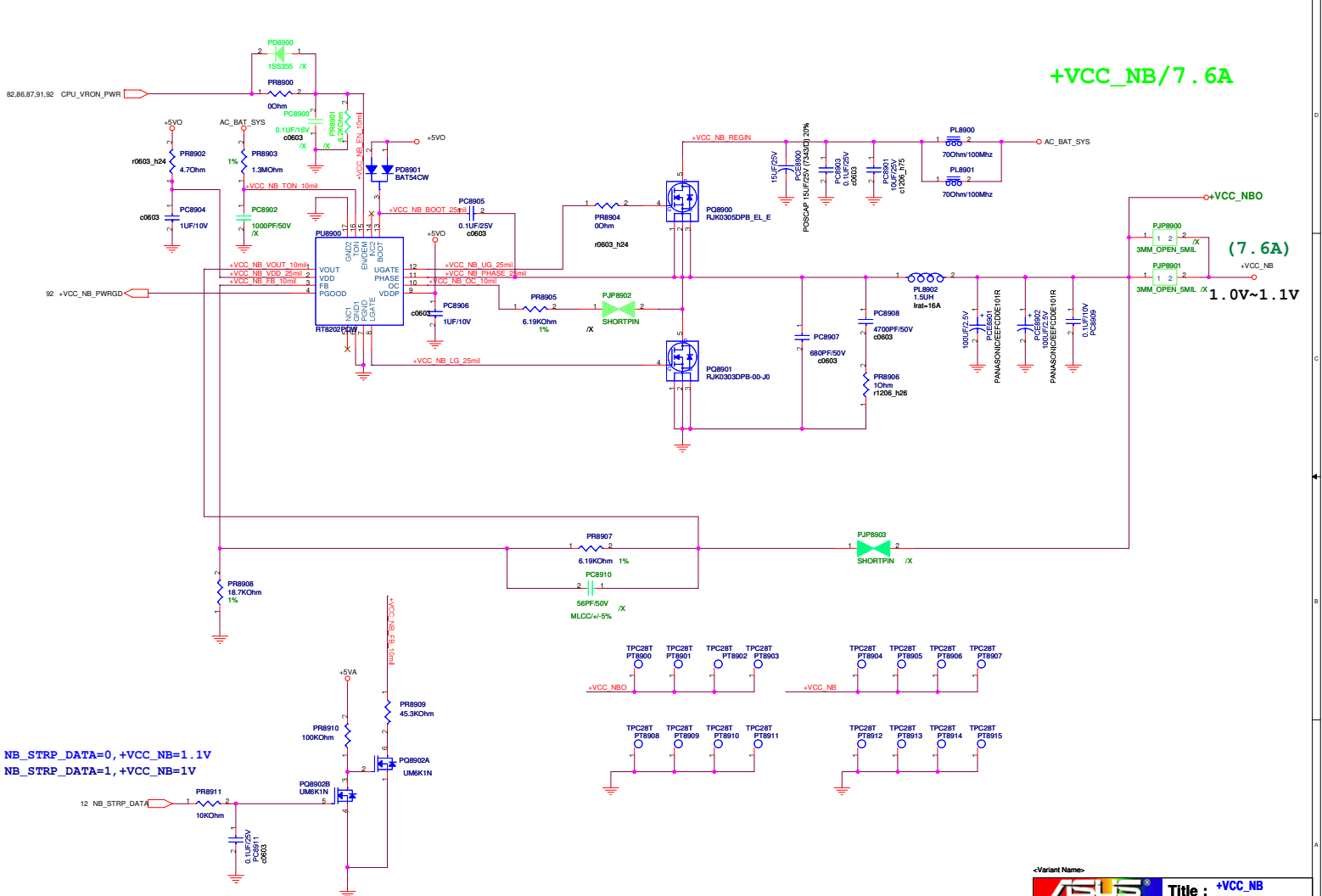
A

A

<< MaryL\_Liu >>

		Title : <Title>	
<OrigName>		Engineer: chang-sheng_lu	
Size	Project Name		Rev
A3	<Doc>		1.00
Date: Wednesday, March 12, 2008		Sheet	88 of 82





NB\_STRP\_DATA=0, +VCC\_NB=1.1V  
 NB\_STRP\_DATA=1, +VCC\_NB=1V

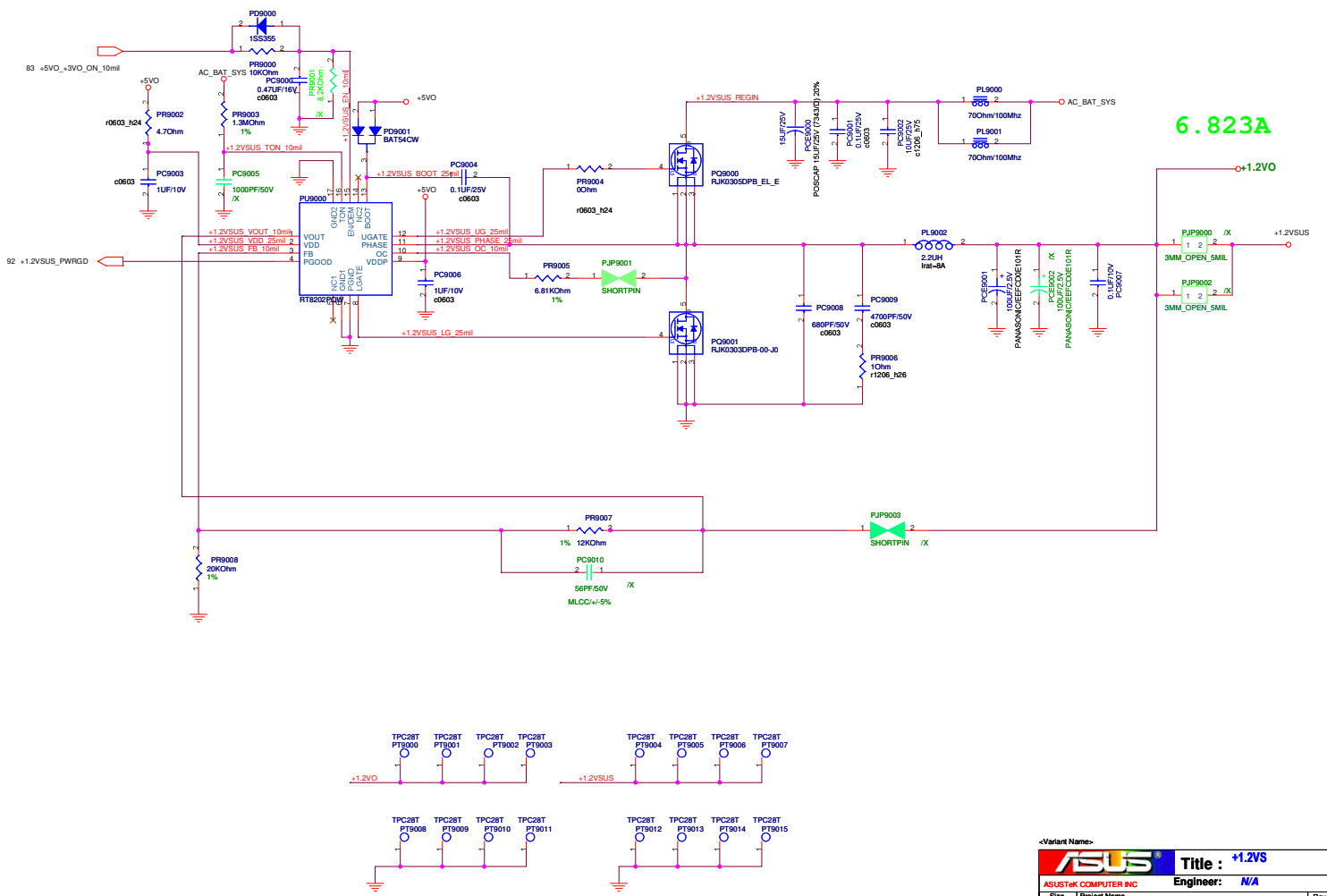
+VCC\_NB/7.6A

(7.6A)  
 +VCC\_NB  
 1.0V~1.1V

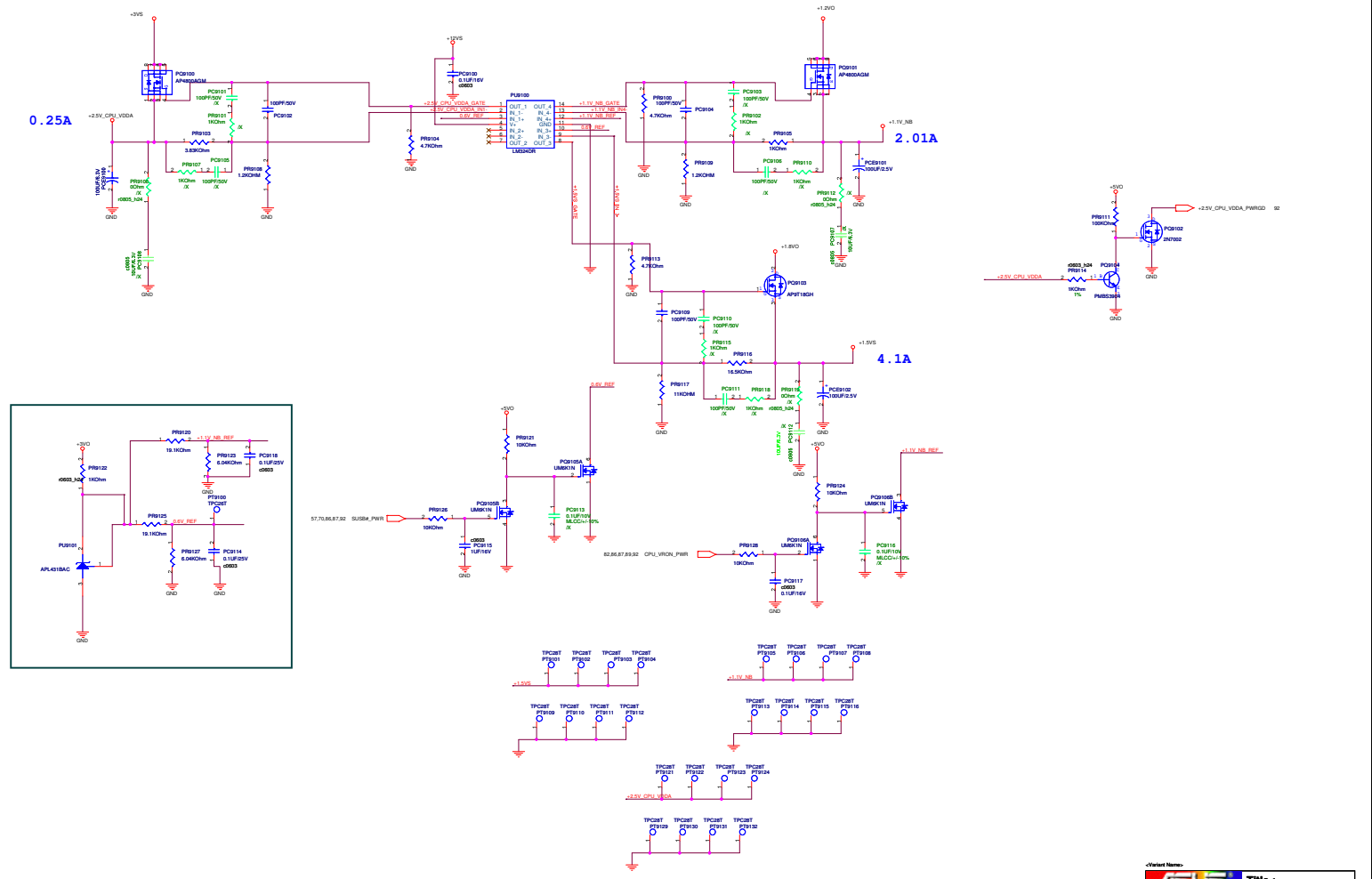
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<b>ASUS</b>		<b>Title : +VCC_NB</b>	
ASUSTEK COMPUTER INC	Project Name:	Engineer:	N/A
Size:	Project Name:		Rev
Custom	<b>FSTR</b>		1.0
Date: Wednesday, March 12, 2008	Sheet	89	of 92

<< MaryL\_Liu >>



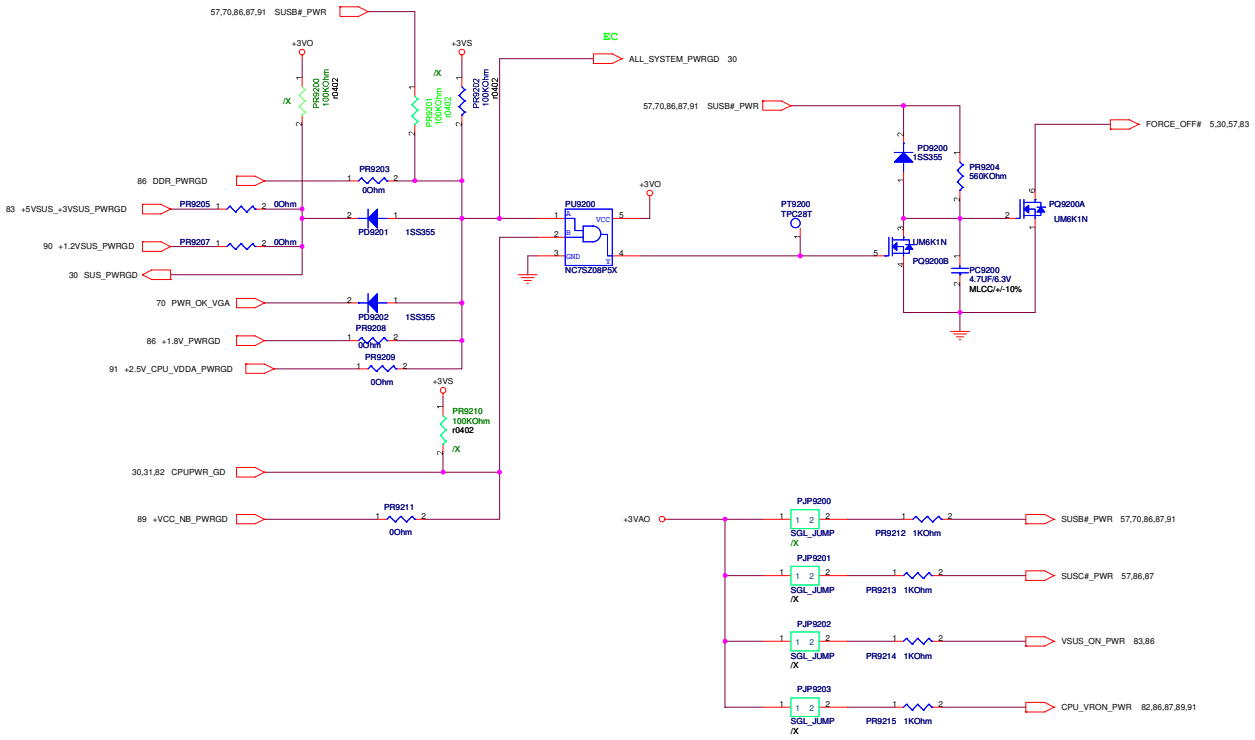
<< MaryL\_Liu >>



ASUS		Title : OP+MGS
Asustek Computer Inc		Engineer : N/A
Size : [ ]	Project Name :	Part :
As : [ ]	FCTR	1.0
Date : Wednesday, March 14, 2007		Sheet : 11 of 31

<< MaryL\_Liu >>

# POWER GOOD DETECTOR



-Variant Name-		<b>ASUS</b>		<b>Title : POWER GOOD DETECTOR</b>	
ASUSTEK COMPUTER INC		Project Name:		Engineer: N/A	
Site:	Custom	Project Name:		Rev: 1.0	
Date: Wednesday, March 12, 2008		Sheet: 82		of 82	

« MaryL\_Liu »