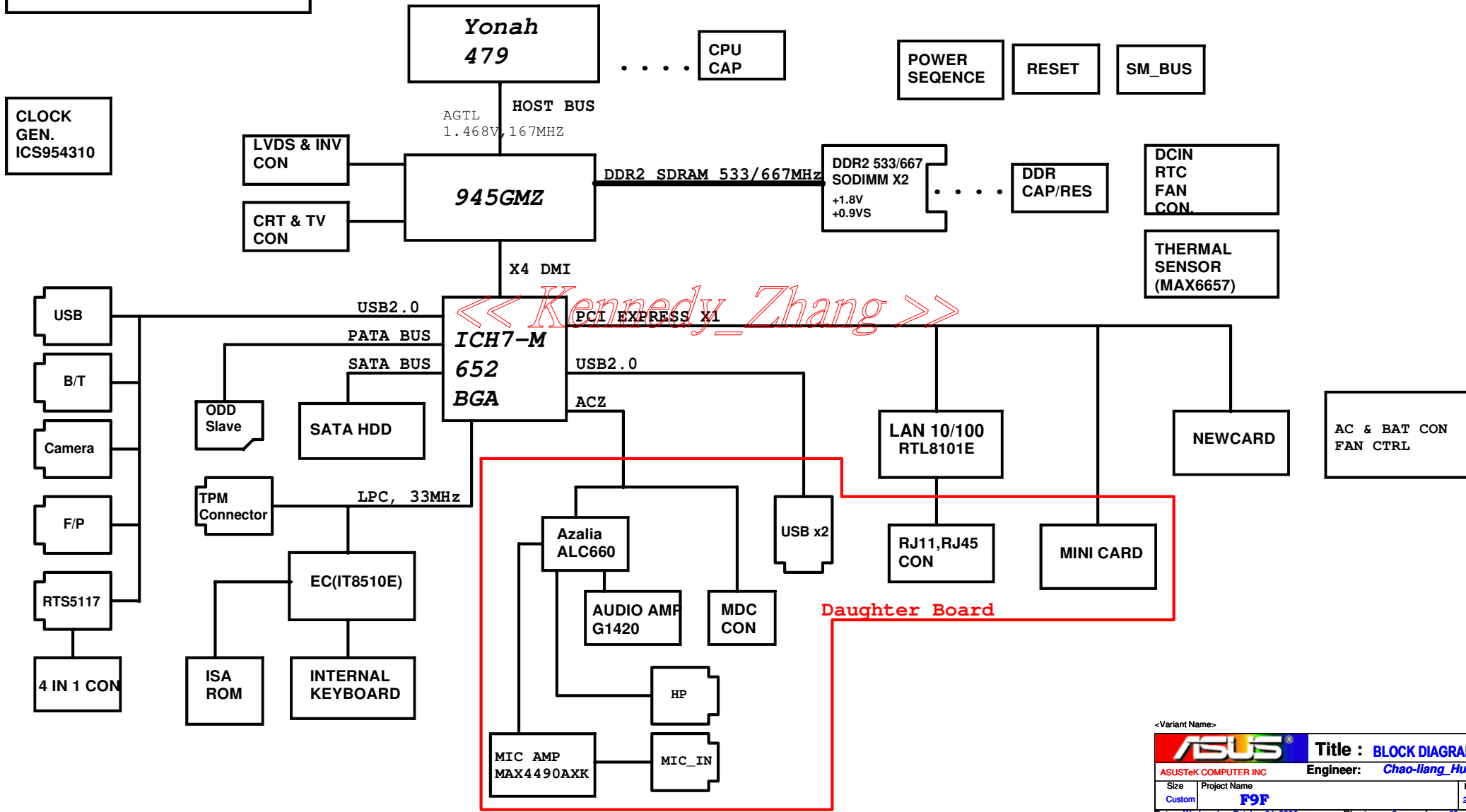
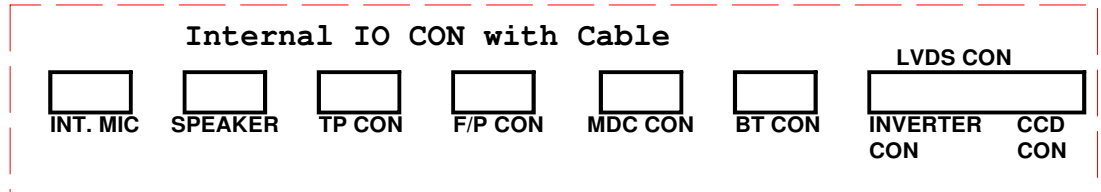
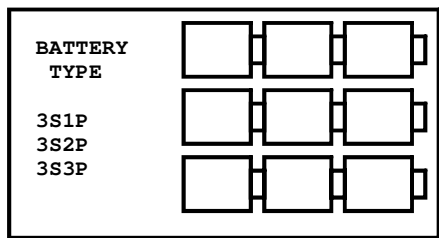




# F9F BLOCK DIAGRAM



<< Kennedy\_Zhang >>

Daughter Board

**EC GPIO SETTING**

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	N/A	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	N/A	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	N/A	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	BT_SW#	I
89	ADC6/GPE2	N/A	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	BAT_AD	I
82	ADC1	ADP_ERR#	I
83	ADC2	AC_AD	I
84	ADC3	N/A	
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

**ICH7M\_PCI EXPRESS**

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

PCI Device	IDSEL#	REQ/GNT#	Interrupts

**SM BUS ADDRESS :**

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A4 )
Thermal Sensor( MAX6657)	1001100x ( 98 )

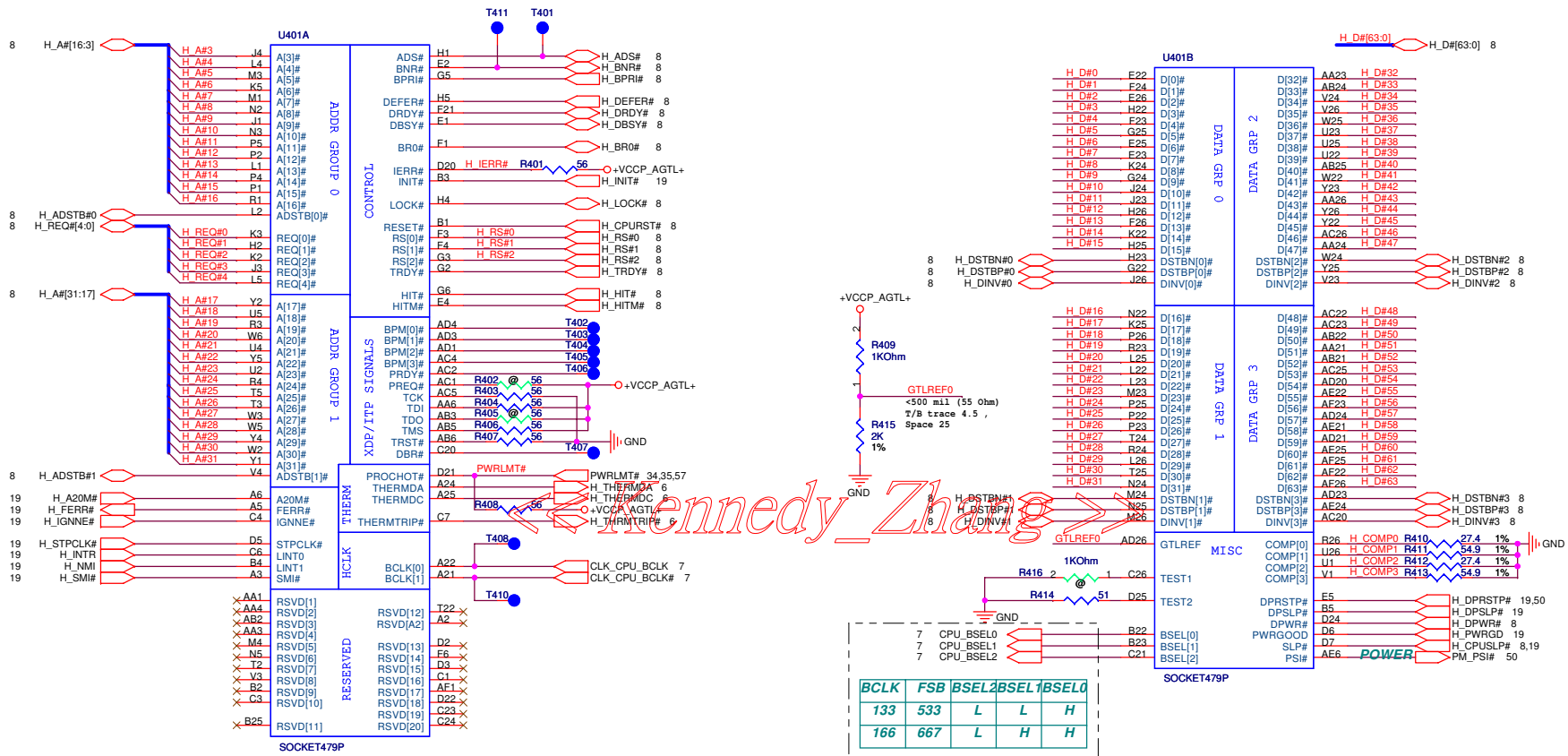
**ICH7M GPIO**

Pin	Use As	Signal Name	Power
GPIO 00	i GPI	PM_BMBUSY#	+3VS
GPIO 01	i GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i GPO	BT_LED_EN	+3VS
GPIO 07	i GPI	RF_ON_SW#	+3VS
GPIO 08	i GPI	EXTSMI#	+3VSUS
GPIO 09	i GPI	N/A	+3VSUS
GPIO 10	i GPI	N/A	+3VSUS
GPIO 11	i Native	SMB_ALERT#	+3VSUS
GPIO 12	i GPI	KBC_SCI#	+3VSUS
GPIO 13	i GPI	N/A	+3VSUS
GPIO 14	i GPI	N/A	+3VSUS
GPIO 15	i GPO	802_LED_EN	+3VSUS
GPIO 16	O 0 GPO	PM DPRSLPVR	+3VS
GPIO 17	O 1 GPO	PCI_GNT#5	+3VS
GPIO 18	O 1 GPO	STP_PCI#	+3VS
GPIO 19	i 1 GPI	N/A	+3VS
GPIO 20	O 1 GPO	STP_CPU#	+3VS
GPIO 21	i 1 GPO	N/A	+3VS
GPIO 22	i 1 Native	PCI_REQ#4	+3VS
GPIO 23	i 1 Native	N/A	+3VS
GPIO 24	O 0 GPO	MSK_PCIRST	+3VSUS
GPIO 25	O 1 GPO	N/A	+3VSUS
GPIO 26	O 0 GPO	BT_ON#	+3VSUS
GPIO 27	O 0 GPO	WLAN_ON#	+3VSUS
GPIO 28	O 0 GPO	N/A	+3VSUS
GPIO 29	i 0 Native	USB_OC#5	+3VSUS
GPIO 30	i 0 Native	USB_OC#6	+3VSUS
GPIO 31	i 0 Native	USB_OC#7	+3VSUS
GPIO 32	O 1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O 1 GPO	N/A	+3VS
GPIO 34	O 0 GPO	N/A	+3VS
GPIO 35	O 0 GPO	N/A	+3VS
GPIO 36	i 0 GPO	N/A	+3VS
GPIO 37	i 0 GPI	PCB_ID0	+3VS
GPIO 38	i 0 GPI	PCB_ID1	+3VS
GPIO 39	i 0 GPI	PCB_ID2	+3VS
GPIO [40:47]	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS
GPIO 49	Native	H_PWRGD	+VCORE

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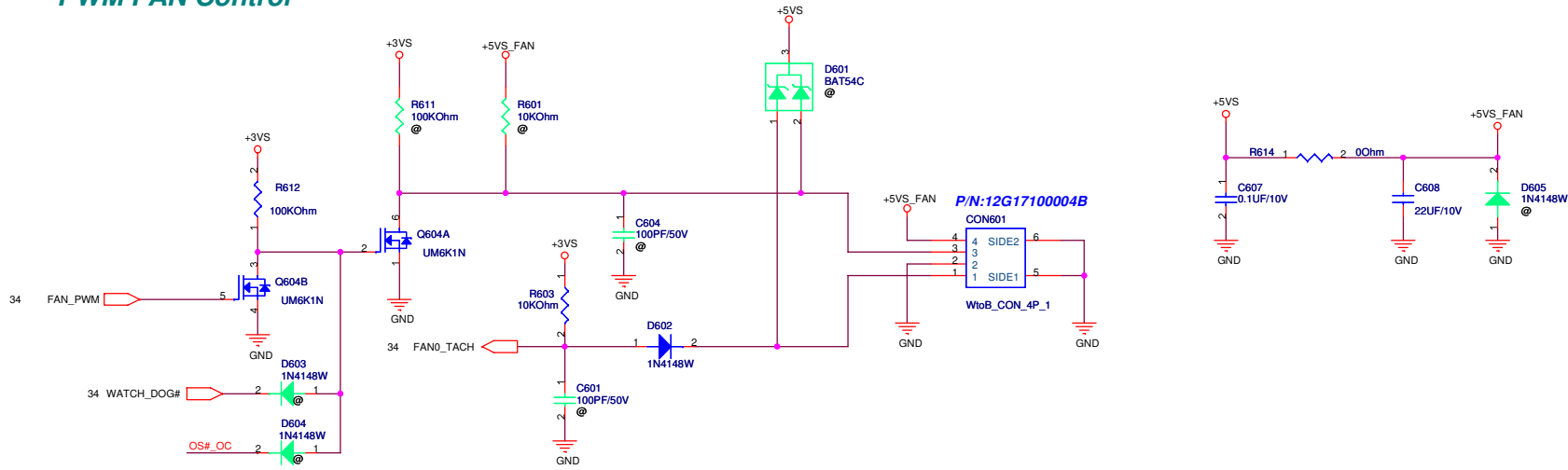
<Variant Name>

		<b>Title :</b> Schematic data
ASUSTeK COMPUTER INC		<b>Engineer:</b> Chao-liang Hung
Size Custom	Project Name <b>F9F</b>	Rev 2.00
Date: Wednesday, October 04, 2006		Sheet 3 of 63

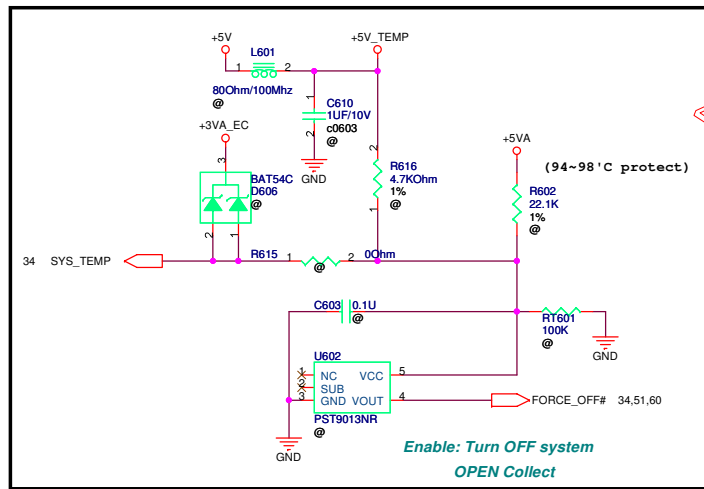




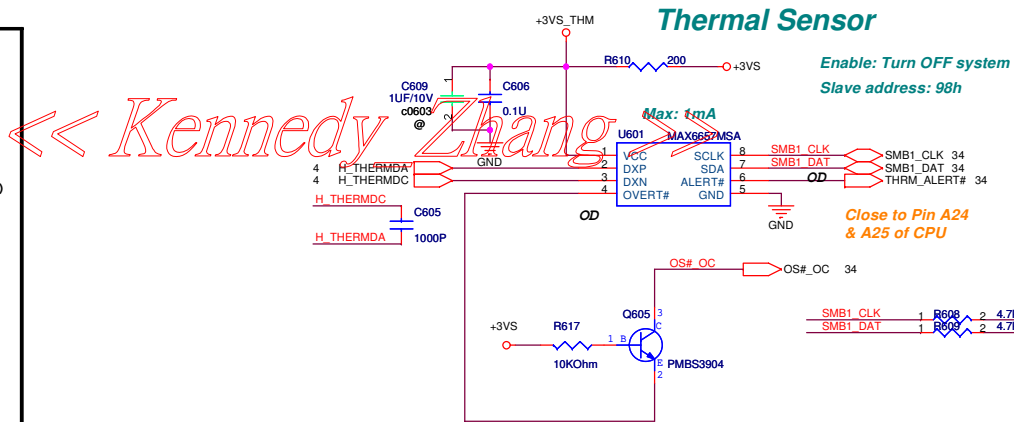
**PWM FAN Control**



**CPU FAN will be forced on:**  
 1) Thermal Sensor Over-temperature  
 2) WATCHDOG asserted by EC

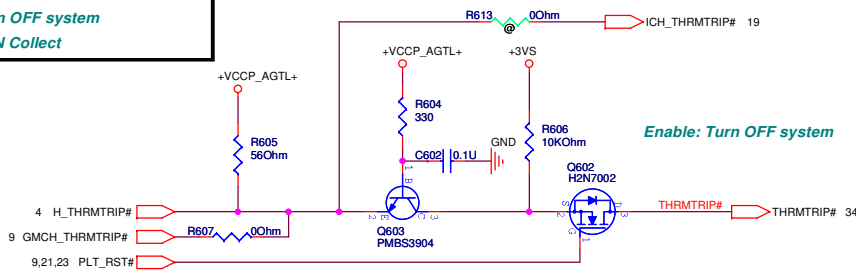


**Enable: Turn OFF system  
OPEN Collect**



**Enable: Turn OFF system  
Slave address: 98h**

**Close to Pin A24  
& A25 of CPU**



**Enable: Turn OFF system**

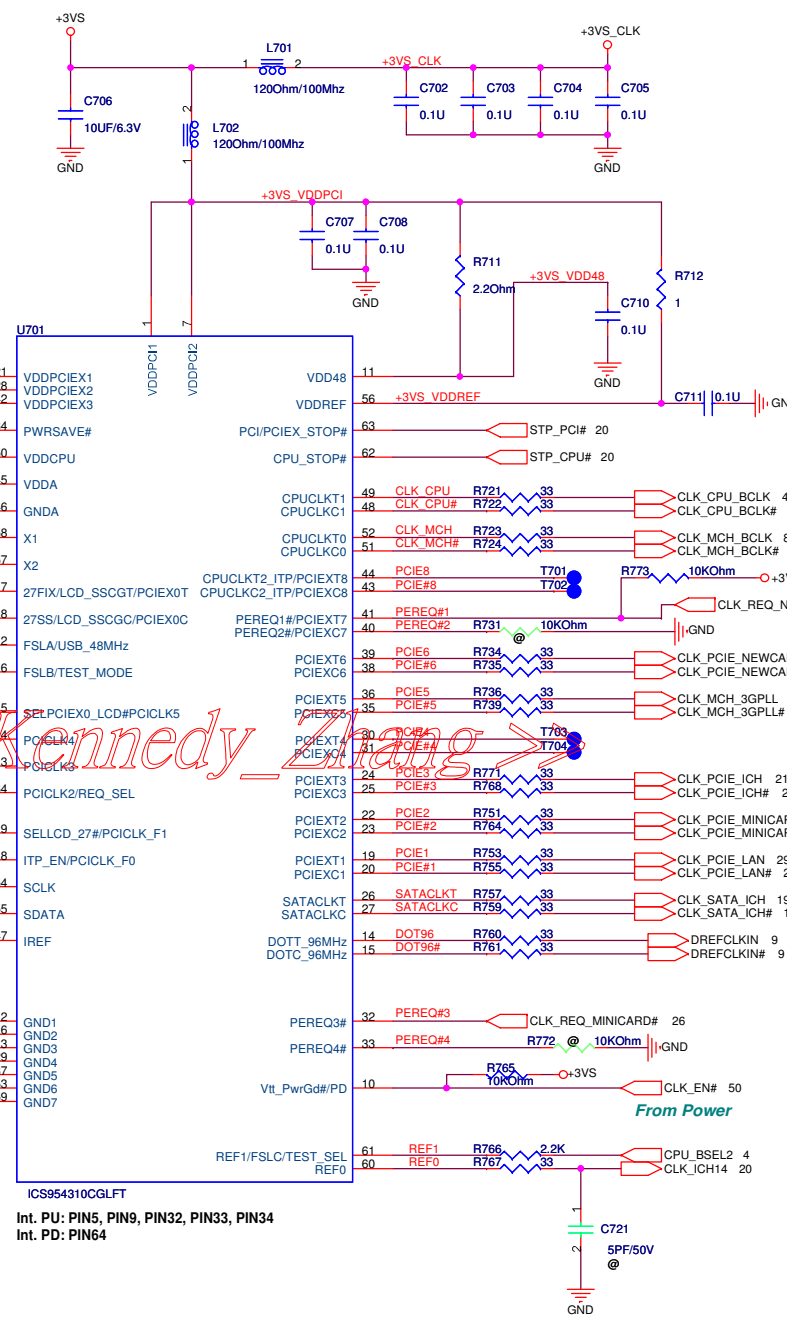
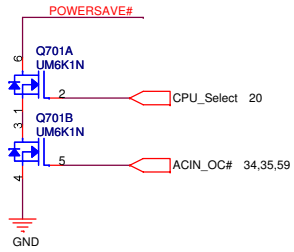
<Variant Name>

<b>ASUS</b>		<b>Title :FAN_CTRL&amp;Thermal</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Chao-liang Hung</b>	
Size	Project Name	Rev	
Custom	<b>F9F</b>	2.00	
Date: Monday, October 16, 2006	Sheet	6	of 63

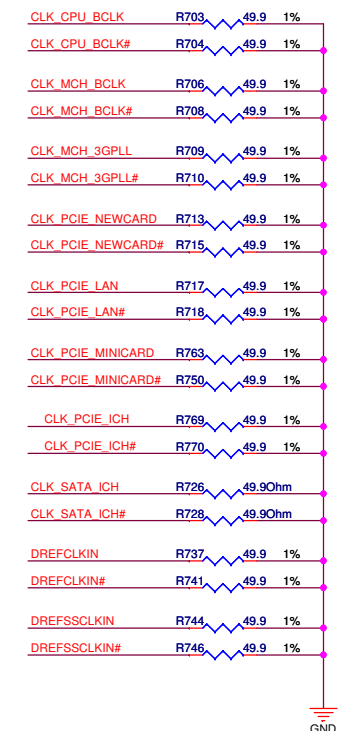


FSLC FSLB FSLA

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



PLACE termination close to source IC



Latched Input Select

PIN9	PIN5	PIN17	PIN18
0	X	27FIX	27SS
1	0	96MSS_T	96MSS_C
1	1	PCIEX0_T	PCIEX0_C

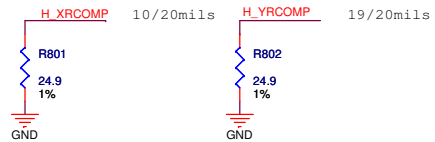
PEREQ#1: PCIEX0, PCIEX6  
 PEREQ#2: PCIEX1, PCIEX8  
 PEREQ#3: PCIEX2, PCIEX4  
 PEREQ#4: PCIEX3, PCIEX5, PCIEX7

ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCL_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)

ASUS Logo  
**Title : ICS954310**  
 ASUSTek COMPUTER INC  
 Engineer: **Chao-liang Hung**  
 Project Name: **F9F**  
 Date: Monday, October 16, 2006  
 Sheet 7 of 63

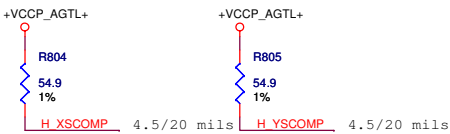
### RCOMP

For Calibrating FSB I/O Buffer



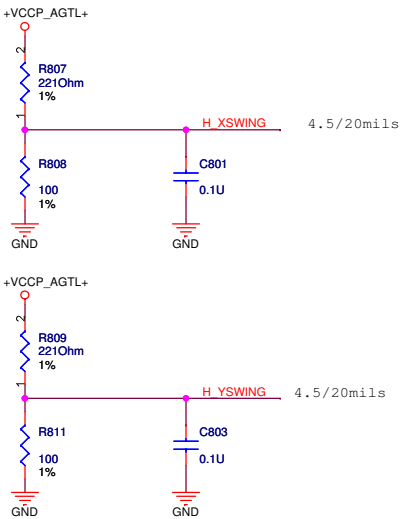
### SCOMP

For Slew Rate Compensation on the FSB



### Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit



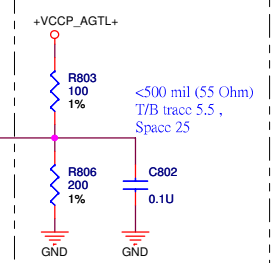
4 H\_D#[0..63]  $\leftarrow$  H\_D#[0..63] U801A CALISTOGA Q137 H\_A#[3..31]  $\leftarrow$  H\_A#[3..31] 4

H_D#0	F1	H_D#_0	H_A#_3	H9	H_A#3
H_D#1	J1	H_D#_1	H_A#_4	C9	H_A#4
H_D#2	H1	H_D#_2	H_A#_5	E11	H_A#5
H_D#3	J6	H_D#_3	H_A#_6	G11	H_A#6
H_D#4	H3	H_D#_4	H_A#_7	F11	H_A#7
H_D#5	K2	H_D#_5	H_A#_8	G12	H_A#8
H_D#6	G1	H_D#_6	H_A#_9	F9	H_A#9
H_D#7	G2	H_D#_7	H_A#_10	H11	H_A#10
H_D#8	K9	H_D#_8	H_A#_11	J12	H_A#11
H_D#9	K4	H_D#_9	H_A#_12	G14	H_A#12
H_D#10	K7	H_D#_10	H_A#_13	D9	H_A#13
H_D#11	J8	H_D#_11	H_A#_14	J14	H_A#14
H_D#12	H4	H_D#_12	H_A#_15	H13	H_A#15
H_D#13	J3	H_D#_13	H_A#_16	J15	H_A#16
H_D#14	K11	H_D#_14	H_A#_17	F14	H_A#17
H_D#15	G4	H_D#_15	H_A#_18	D12	H_A#18
H_D#16	T10	H_D#_16	H_A#_19	A11	H_A#19
H_D#17	W11	H_D#_17	H_A#_20	C11	H_A#20
H_D#18	T3	H_D#_18	H_A#_21	A12	H_A#21
H_D#19	U7	H_D#_19	H_A#_22	A13	H_A#22
H_D#20	U9	H_D#_20	H_A#_23	E13	H_A#23
H_D#21	U11	H_D#_21	H_A#_24	G13	H_A#24
H_D#22	T11	H_D#_22	H_A#_25	F12	H_A#25
H_D#23	W9	H_D#_23	H_A#_26	B12	H_A#26
H_D#24	T1	H_D#_24	H_A#_27	B14	H_A#27
H_D#25	T8	H_D#_25	H_A#_28	C12	H_A#28
H_D#26	T4	H_D#_26	H_A#_29	A14	H_A#29
H_D#27	W7	H_D#_27	H_A#_30	C14	H_A#30
H_D#28	U5	H_D#_28	H_A#_31	D14	H_A#31
H_D#29	T9	H_D#_29			
H_D#30	W6	H_D#_30			
H_D#31	T5	H_D#_31			
H_D#32	AB7	H_D#_32			
H_D#33	AA9	H_D#_33			
H_D#34	W4	H_D#_34			
H_D#35	Y3	H_D#_35			
H_D#36	Y7	H_D#_36			
H_D#37	Y3	H_D#_37			
H_D#38	W5	H_D#_38			
H_D#39	Y10	H_D#_39			
H_D#40	AB8	H_D#_40			
H_D#41	W2	H_D#_41			
H_D#42	AA4	H_D#_42			
H_D#43	AA7	H_D#_43			
H_D#44	AA2	H_D#_44			
H_D#45	AA6	H_D#_45			
H_D#46	AA10	H_D#_46			
H_D#47	AB5	H_D#_47			
H_D#48	AB4	H_D#_48			
H_D#49	AC9	H_D#_49			
H_D#50	AB11	H_D#_50			
H_D#51	AC11	H_D#_51			
H_D#52	AC1	H_D#_52			
H_D#53	AB3	H_D#_53			
H_D#54	AC2	H_D#_54			
H_D#55	AD1	H_D#_55			
H_D#56	AD9	H_D#_56			
H_D#57	AC1	H_D#_57			
H_D#58	AD7	H_D#_58			
H_D#59	AC6	H_D#_59			
H_D#60	AB5	H_D#_60			
H_D#61	AD10	H_D#_61			
H_D#62	AD4	H_D#_62			
H_D#63	AC8	H_D#_63			

HOST

<< Kennedy\_Zhang >>

### AGTL+ I/O Voltage Reference



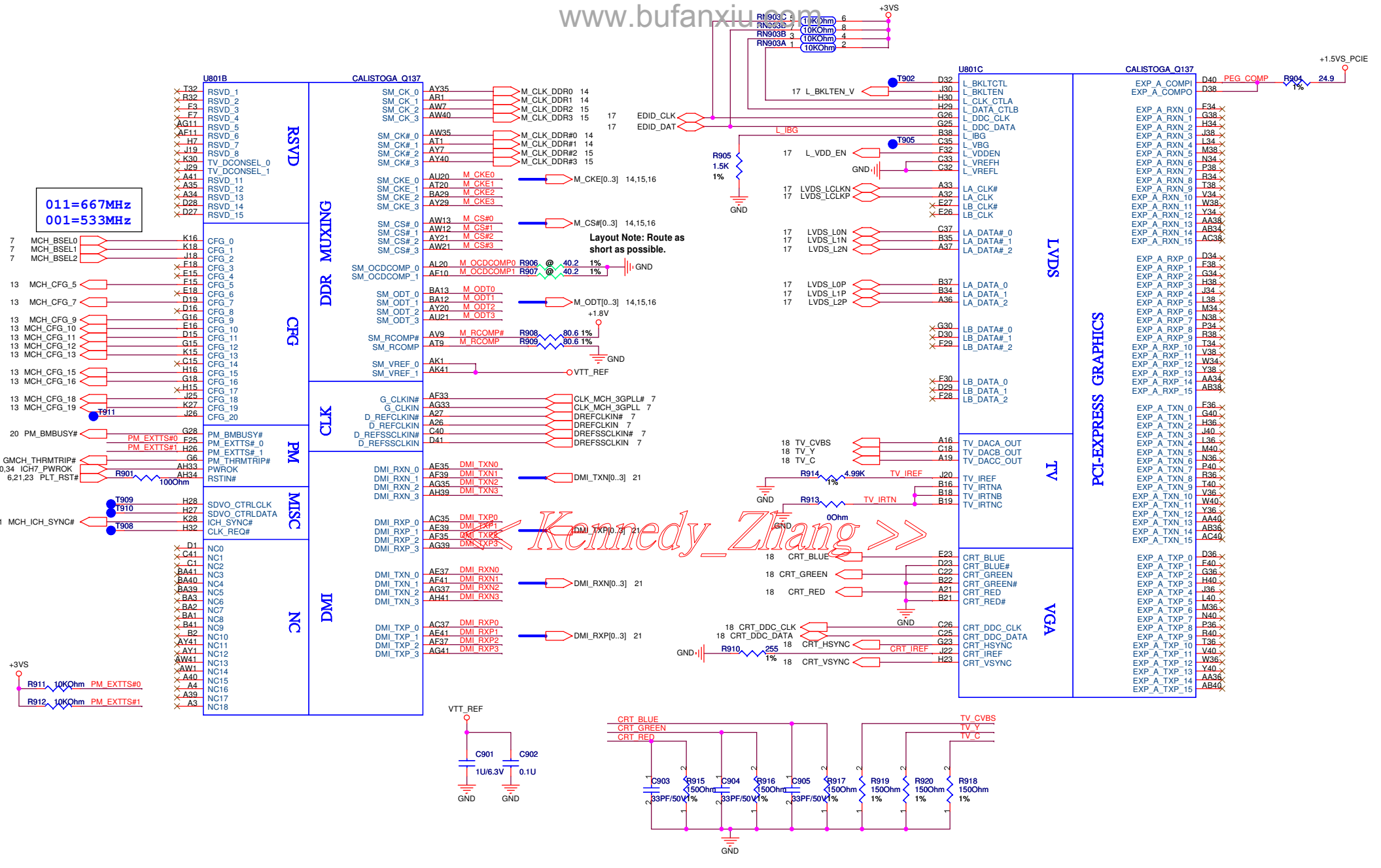
H\_CPURST# T801

H_ADS#	E8	H_ADS#	4
H_ADSTB#_0	B9	H_ADSTB#_0	4
H_ADSTB#_1	C13	H_ADSTB#_1	4
H_AVREF	J13		
H_BNRF#	C6	H_BNRF#	4
H_BPRF#	E6	H_BPRF#	4
H_BRF#	F7	H_BRF#	4
H_CPURST#	B7	H_CPURST#	4
H_OBSV#	A7	H_OBSV#	4
H_DEFER#	C3	H_DEFER#	4
H_DPWR#	J9	H_DPWR#	4
H_DRDY#	H8	H_DRDY#	4
H_DVREF	K13		
H_DINV#_0	J7	H_DINV#_0	4
H_DINV#_1	W8	H_DINV#_1	4
H_DINV#_2	U3	H_DINV#_2	4
H_DINV#_3	U3	H_DINV#_3	4
H_DSTBN#_0	AB10	H_DSTBN#_0	4
H_DSTBN#_1	K4	H_DSTBN#_1	4
H_DSTBN#_2	G7	H_DSTBN#_2	4
H_DSTBN#_3	AC4	H_DSTBN#_3	4
H_DSTBP#_0	K3	H_DSTBP#_0	4
H_DSTBP#_1	T6	H_DSTBP#_1	4
H_DSTBP#_2	AA5	H_DSTBP#_2	4
H_DSTBP#_3	AC5	H_DSTBP#_3	4
H_HIT#	D3	H_HIT#	4
H_HITM#	D4	H_HITM#	4
H_LOCK#	B3	H_LOCK#	4
H_REQ#_0	D8	H_REQ#_0	4
H_REQ#_1	G8	H_REQ#_1	4
H_REQ#_2	B8	H_REQ#_2	4
H_REQ#_3	F8	H_REQ#_3	4
H_REQ#_4	A8	H_REQ#_4	4
H_RS#_0	B4	H_RS#_0	4
H_RS#_1	E6	H_RS#_1	4
H_RS#_2	D6	H_RS#_2	4
H_SLP#	E3	H_SLP#	4
H_TRDY#	E7	H_TRDY#	4

<Variant Name>

**ASUS** Title : Calistoga-CPU  
 ASUSTek COMPUTER INC Engineer: Chao-liang Hung  
 Size Project Name  
 Custom F9F  
 Date: Wednesday, October 04, 2006 Sheet 8 of 63  
 Rev 2.00





14 M\_A\_DQ[0..63]

15 M\_B\_DQ[0..63]

U801D		CALISTOGA_Q137	
M_A_D00	AJ35	SA_D00	SA_BS_0
M_A_D01	AJ34	SA_D01	SA_BS_1
M_A_D02	AM31	SA_D02	SA_BS_2
M_A_D03	AM33	SA_D03	
M_A_D04	AJ36	SA_D04	SA_CAS#
M_A_D05	AK35	SA_D05	SA_DM_0
M_A_D06	AJ32	SA_D06	SA_DM_1
M_A_D07	AH31	SA_D07	SA_DM_2
M_A_D08	AN35	SA_D08	SA_DM_3
M_A_D09	AP33	SA_D09	SA_DM_4
M_A_D010	AR31	SA_D010	SA_DM_5
M_A_D011	AP31	SA_D011	SA_DM_6
M_A_D012	AN38	SA_D012	SA_DM_7
M_A_D013	AM36	SA_D013	
M_A_D014	AM34	SA_D014	SA_DQS_0
M_A_D015	AN33	SA_D015	SA_DQS_1
M_A_D016	AK26	SA_D016	SA_DQS_2
M_A_D017	AL27	SA_D017	SA_DQS_3
M_A_D018	AM26	SA_D018	SA_DQS_4
M_A_D019	AN24	SA_D019	SA_DQS_5
M_A_D020	AK28	SA_D020	SA_DQS_6
M_A_D021	AL28	SA_D021	SA_DQS_7
M_A_D022	AM24	SA_D022	SA_DQS#_0
M_A_D023	AP26	SA_D023	SA_DQS#_1
M_A_D024	AP23	SA_D024	SA_DQS#_2
M_A_D025	AL22	SA_D025	SA_DQS#_3
M_A_D026	AP21	SA_D026	SA_DQS#_4
M_A_D027	AN20	SA_D027	SA_DQS#_5
M_A_D028	AL23	SA_D028	SA_DQS#_6
M_A_D029	AP24	SA_D029	SA_DQS#_7
M_A_D030	AP20	SA_D030	
M_A_D031	AT21	SA_D031	SA_MA_0
M_A_D032	AR12	SA_D032	SA_MA_1
M_A_D033	AR14	SA_D033	SA_MA_2
M_A_D034	AP13	SA_D034	SA_MA_3
M_A_D035	AP12	SA_D035	SA_MA_4
M_A_D036	AT13	SA_D036	SA_MA_5
M_A_D037	AT12	SA_D037	SA_MA_6
M_A_D038	AL14	SA_D038	SA_MA_7
M_A_D039	AL12	SA_D039	SA_MA_8
M_A_D040	AK9	SA_D040	SA_MA_9
M_A_D041	AN7	SA_D041	SA_MA_10
M_A_D042	AK8	SA_D042	SA_MA_11
M_A_D043	AK7	SA_D043	SA_MA_12
M_A_D044	AP9	SA_D044	SA_MA_13
M_A_D045	AN9	SA_D045	
M_A_D046	AT5	SA_D046	SA_RAS#
M_A_D047	AL5	SA_D047	SA_RCVENIN#
M_A_D048	AY2	SA_D048	SA_RCVENOUT#
M_A_D049	AW2	SA_D049	SA_WE#
M_A_D050	AP1	SA_D050	
M_A_D051	AN2	SA_D051	
M_A_D052	AV2	SA_D052	
M_A_D053	AT3	SA_D053	
M_A_D054	AN1	SA_D054	
M_A_D055	AL2	SA_D055	
M_A_D056	AG7	SA_D056	
M_A_D057	AF9	SA_D057	
M_A_D058	AG4	SA_D058	
M_A_D059	AF6	SA_D059	
M_A_D060	AG9	SA_D060	
M_A_D061	AH6	SA_D061	
M_A_D062	AF4	SA_D062	
M_A_D063	AF8	SA_D063	

DDR SYSTEM MEMORY A

AU12	M_A_BS#0	14,16
AV14	M_A_BS#1	14,16
BA20	M_A_BS#2	14,16
AY13	M_A_CAS#	14,16
AJ33	M_A_DM0	
AM35	M_A_DM1	
AL26	M_A_DM2	
AN22	M_A_DM3	
AM14	M_A_DM4	
AL9	M_A_DM5	
AR3	M_A_DM6	
AH4	M_A_DM7	
AK33	M_A_DQS0	
AT33	M_A_DQS1	
AN28	M_A_DQS2	
AM22	M_A_DQS3	
AN12	M_A_DQS4	
AN8	M_A_DQS5	
AG5	M_A_DQS6	
AK32	M_A_DQS#0	
AU33	M_A_DQS#1	
AN27	M_A_DQS#2	
AM21	M_A_DQS#3	
AM12	M_A_DQS#4	
AN3	M_A_DQS#5	
AH5	M_A_DQS#6	
AY16	M_A_A0	
AU14	M_A_A1	
AV16	M_A_A2	
BA16	M_A_A3	
BA17	M_A_A4	
AU16	M_A_A5	
AV17	M_A_A6	
AU17	M_A_A7	
AV17	M_A_A8	
AT16	M_A_A9	
AU13	M_A_A10	
AT17	M_A_A11	
AV20	M_A_A12	
AV12	M_A_A13	
AW14	M_A_RAS#	14,16
AK23	M_A_WE#	14,16
AK24		
AY14	M_A_WE#	14,16

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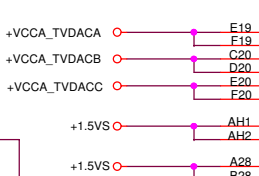
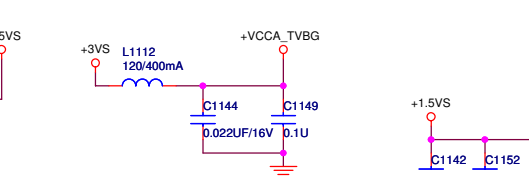
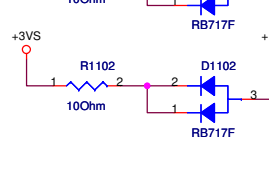
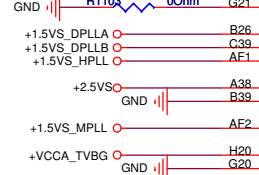
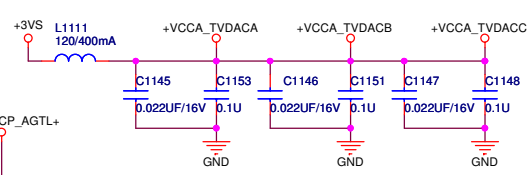
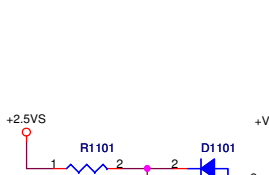
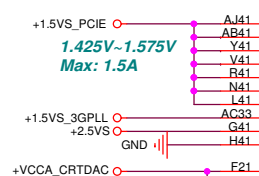
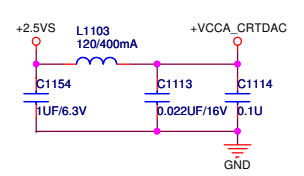
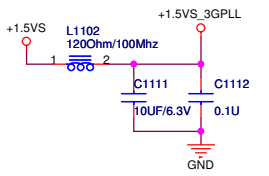
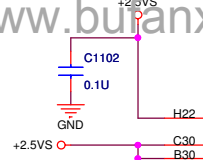
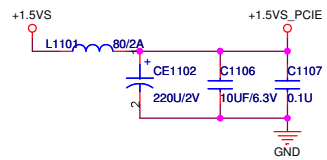
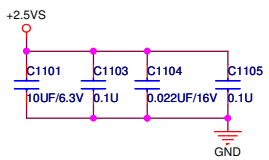
U801E		CALISTOGA_Q137	
M_B_D00	AK39	SB_D00	SB_BS_0
M_B_D01	AJ37	SB_D01	SB_BS_1
M_B_D02	AP39	SB_D02	SB_BS_2
M_B_D03	AR41	SB_D03	
M_B_D04	AJ38	SB_D04	SB_CAS#
M_B_D05	AK38	SB_D05	SB_DM_0
M_B_D06	AP41	SB_D06	SB_DM_1
M_B_D07	AN41	SB_D07	SB_DM_2
M_B_D08	AT40	SB_D08	SB_DM_3
M_B_D09	AV41	SB_D09	SB_DM_4
M_B_D010	AU38	SB_D010	SB_DM_5
M_B_D011	AV38	SB_D011	SB_DM_6
M_B_D012	AP38	SB_D012	SB_DM_7
M_B_D013	AR40	SB_D013	
M_B_D014	AW38	SB_D014	SB_DQS_0
M_B_D015	AY38	SB_D015	SB_DQS_1
M_B_D016	BA38	SB_D016	SB_DQS_2
M_B_D017	AV36	SB_D017	SB_DQS_3
M_B_D018	AR36	SB_D018	SB_DQS_4
M_B_D019	BA36	SB_D019	SB_DQS_5
M_B_D020	AP36	SB_D020	SB_DQS_6
M_B_D021	AU36	SB_D021	SB_DQS_7
M_B_D022	AP35	SB_D022	SB_DQS#_0
M_B_D023	AP34	SB_D023	SB_DQS#_1
M_B_D024	AY33	SB_D024	SB_DQS#_2
M_B_D025	BA33	SB_D025	SB_DQS#_3
M_B_D026	AT31	SB_D026	SB_DQS#_4
M_B_D027	AU29	SB_D027	SB_DQS#_5
M_B_D028	AU31	SB_D028	SB_DQS#_6
M_B_D029	AW31	SB_D029	SB_DQS#_7
M_B_D030	AV29	SB_D030	
M_B_D031	AW29	SB_D031	SB_MA_0
M_B_D032	AM19	SB_D032	SB_MA_1
M_B_D033	AM19	SB_D033	SB_MA_2
M_B_D034	AP14	SB_D034	SB_MA_3
M_B_D035	AN14	SB_D035	SB_MA_4
M_B_D036	AN17	SB_D036	SB_MA_5
M_B_D037	AM16	SB_D037	SB_MA_6
M_B_D038	AP15	SB_D038	SB_MA_7
M_B_D039	AL17	SB_D039	SB_MA_8
M_B_D040	AU14	SB_D040	SB_MA_9
M_B_D041	AH10	SB_D041	SB_MA_10
M_B_D042	AJ9	SB_D042	SB_MA_11
M_B_D043	AN10	SB_D043	SB_MA_12
M_B_D044	AK13	SB_D044	SB_MA_13
M_B_D045	AK11	SB_D045	
M_B_D046	AK10	SB_D046	SB_RAS#
M_B_D047	AJ8	SB_D047	SB_RCVENIN#
M_B_D048	BA10	SB_D048	SB_RCVENOUT#
M_B_D049	AW10	SB_D049	SB_WE#
M_B_D050	BA4	SB_D050	
M_B_D051	AW4	SB_D051	
M_B_D052	AY10	SB_D052	
M_B_D053	AY9	SB_D053	
M_B_D054	AW5	SB_D054	
M_B_D055	AY5	SB_D055	
M_B_D056	AV4	SB_D056	
M_B_D057	AR5	SB_D057	
M_B_D058	AK4	SB_D058	
M_B_D059	AK3	SB_D059	
M_B_D060	AT4	SB_D060	
M_B_D061	AK5	SB_D061	
M_B_D062	AJ5	SB_D062	
M_B_D063	AJ3	SB_D063	

DDR SYSTEM MEMORY B

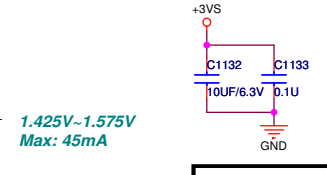
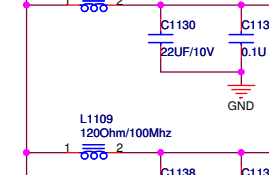
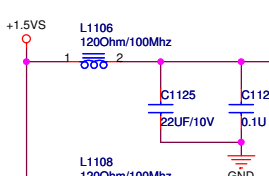
AT24	M_B_BS#0	15,16
AV23	M_B_BS#1	15,16
AY28	M_B_BS#2	15,16
AR24	M_B_CAS#	15,16
AK36	M_B_DM0	
AR38	M_B_DM1	
AT36	M_B_DM2	
BA31	M_B_DM3	
AL17	M_B_DM4	
AH8	M_B_DM5	
BA5	M_B_DM6	
AN4	M_B_DM7	
AM39	M_B_DQS0	
AT39	M_B_DQS1	
AU35	M_B_DQS2	
AR29	M_B_DQS3	
AR16	M_B_DQS4	
AR10	M_B_DQS5	
AR7	M_B_DQS6	
AN5	M_B_DQS7	
AM40	M_B_DQS#0	
AU39	M_B_DQS#1	
AT35	M_B_DQS#2	
AP29	M_B_DQS#3	
AP16	M_B_DQS#4	
AT10	M_B_DQS#5	
AT7	M_B_DQS#6	
AP5	M_B_DQS#7	
AY23	M_B_A0	
AW24	M_B_A1	
AY24	M_B_A2	
AR28	M_B_A3	
AT27	M_B_A4	
AT28	M_B_A5	
AU27	M_B_A6	
AV28	M_B_A7	
AV27	M_B_A8	
AW27	M_B_A9	
AV24	M_B_A10	
BA27	M_B_A11	
AY27	M_B_A12	
AR23	M_B_A13	
AU23	M_B_RAS#	15,16
AK16	M_B_WE#	15,16
AK14		
AR27	M_B_WE#	15,16

<Variant Name>

		<b>Title : Calistoga-DDR2</b>	
ASUSTek COMPUTER INC		Engineer: Chao-liang Hung	
Size	Project Name		Rev
Custom	F9F		2.00
Date: Wednesday, October 04, 2006	Sheet	10	of 63



NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.



NOTE:0.1uF CAPS USED IN +1.5VS, +3VS +2.5VS should be placed within 200 mils of edge.

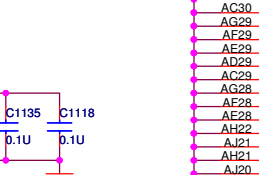
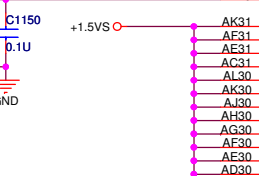
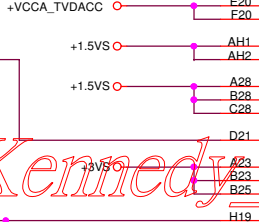
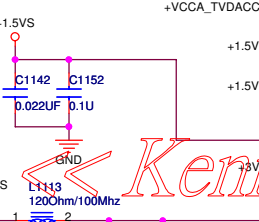
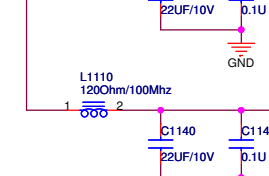
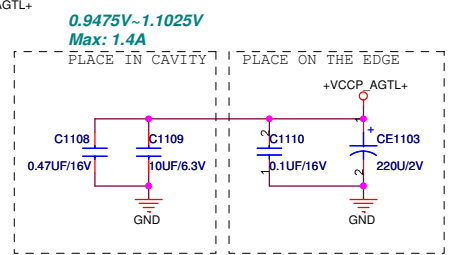


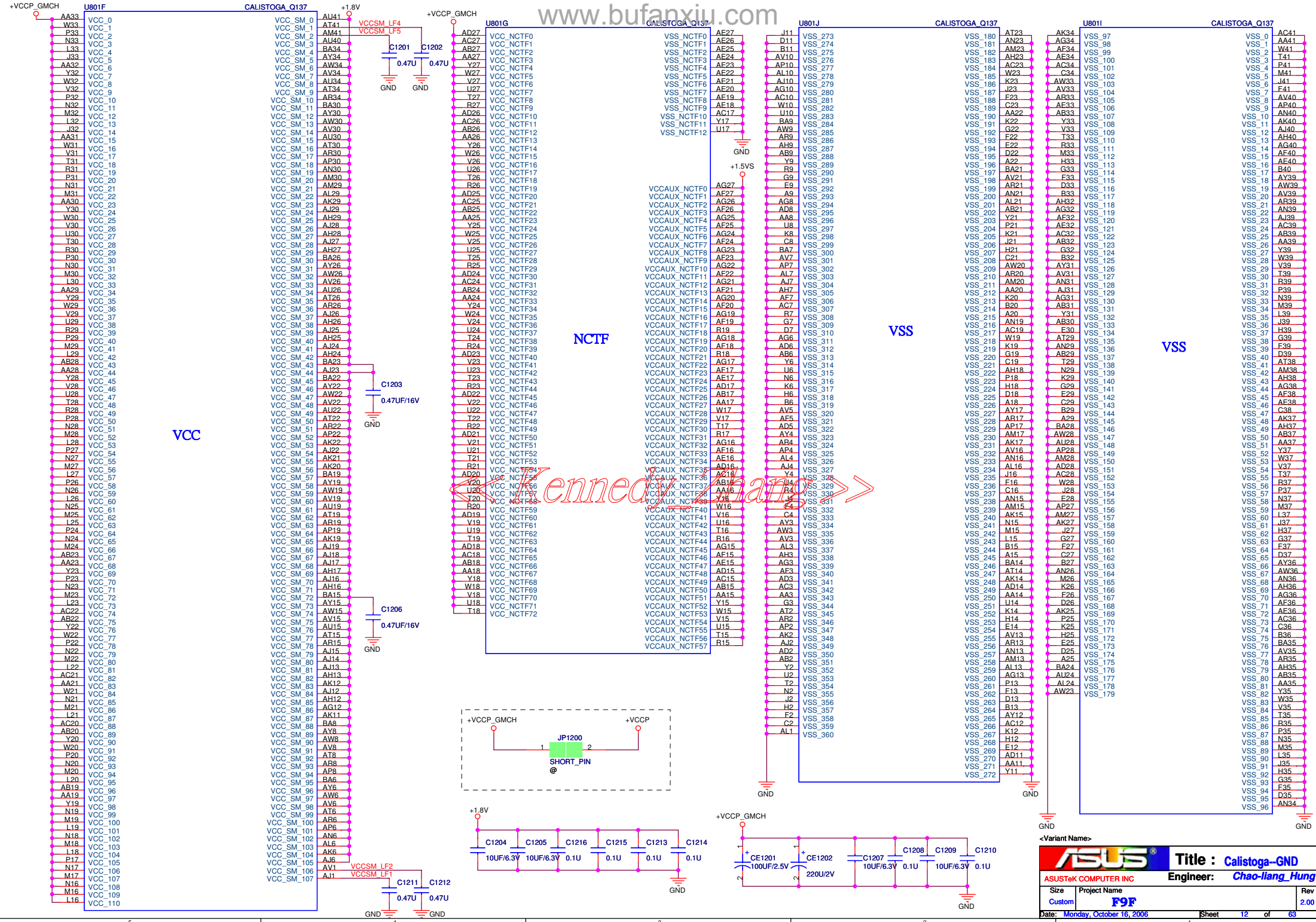
Table of component connections for U801H and CALISTOGA Q137, listing pins and their corresponding components.



POWER

<< Kennedy Zhang >>

ASUS logo, Title: Calistoga-POWER, Engineer: Chao-liang Hung, Date: Wednesday, October 04, 2006, Sheet 11 of 63.



Pin list for U801F: AA33 VCC\_0, W33 VCC\_1, P33 VCC\_2, N33 VCC\_3, L33 VCC\_4, J33 VCC\_5, AA32 VCC\_6, Y32 VCC\_7, W32 VCC\_8, V32 VCC\_9, P32 VCC\_10, N32 VCC\_11, M32 VCC\_12, L32 VCC\_13, R32 VCC\_14, AA31 VCC\_15, W31 VCC\_16, V31 VCC\_17, R31 VCC\_18, P31 VCC\_19, N31 VCC\_20, M31 VCC\_21, AA30 VCC\_22, Y30 VCC\_23, W30 VCC\_24, V30 VCC\_25, L30 VCC\_26, T30 VCC\_27, R30 VCC\_28, P30 VCC\_29, N30 VCC\_30, M30 VCC\_31, L30 VCC\_32, AA29 VCC\_33, Y29 VCC\_34, W29 VCC\_35, V29 VCC\_36, R29 VCC\_37, P29 VCC\_38, M29 VCC\_39, L29 VCC\_40, AA28 VCC\_41, Y28 VCC\_42, W28 VCC\_43, V28 VCC\_44, L28 VCC\_45, AA27 VCC\_46, Y27 VCC\_47, W27 VCC\_48, V27 VCC\_49, P27 VCC\_50, N27 VCC\_51, M27 VCC\_52, L27 VCC\_53, AA26 VCC\_54, Y26 VCC\_55, W26 VCC\_56, V26 VCC\_57, L26 VCC\_58, AA25 VCC\_59, Y25 VCC\_60, W25 VCC\_61, V25 VCC\_62, L25 VCC\_63, AA24 VCC\_64, Y24 VCC\_65, W24 VCC\_66, V24 VCC\_67, L24 VCC\_68, AA23 VCC\_69, Y23 VCC\_70, W23 VCC\_71, V23 VCC\_72, L23 VCC\_73, AA22 VCC\_74, Y22 VCC\_75, W22 VCC\_76, V22 VCC\_77, L22 VCC\_78, AA21 VCC\_79, Y21 VCC\_80, W21 VCC\_81, V21 VCC\_82, L21 VCC\_83, AA20 VCC\_84, Y20 VCC\_85, W20 VCC\_86, V20 VCC\_87, L20 VCC\_88, AA19 VCC\_89, Y19 VCC\_90, W19 VCC\_91, V19 VCC\_92, L19 VCC\_93, AA18 VCC\_94, Y18 VCC\_95, W18 VCC\_96, V18 VCC\_97, L18 VCC\_98, AA17 VCC\_99, Y17 VCC\_100, W17 VCC\_101, V17 VCC\_102, L17 VCC\_103, AA16 VCC\_104, Y16 VCC\_105, W16 VCC\_106, V16 VCC\_107, L16 VCC\_108, AA15 VCC\_109, Y15 VCC\_110

Pin list for CALISTOGA Q137: VCC\_SM\_0 VCC\_SM\_1, VCC\_SM\_2 VCC\_SM\_3, VCC\_SM\_4 VCC\_SM\_5, VCC\_SM\_6 VCC\_SM\_7, VCC\_SM\_8 VCC\_SM\_9, VCC\_SM\_10 VCC\_SM\_11, VCC\_SM\_12 VCC\_SM\_13, VCC\_SM\_14 VCC\_SM\_15, VCC\_SM\_16 VCC\_SM\_17, VCC\_SM\_18 VCC\_SM\_19, VCC\_SM\_20 VCC\_SM\_21, VCC\_SM\_22 VCC\_SM\_23, VCC\_SM\_24 VCC\_SM\_25, VCC\_SM\_26 VCC\_SM\_27, VCC\_SM\_28 VCC\_SM\_29, VCC\_SM\_30 VCC\_SM\_31, VCC\_SM\_32 VCC\_SM\_33, VCC\_SM\_34 VCC\_SM\_35, VCC\_SM\_36 VCC\_SM\_37, VCC\_SM\_38 VCC\_SM\_39, VCC\_SM\_40 VCC\_SM\_41, VCC\_SM\_42 VCC\_SM\_43, VCC\_SM\_44 VCC\_SM\_45, VCC\_SM\_46 VCC\_SM\_47, VCC\_SM\_48 VCC\_SM\_49, VCC\_SM\_50 VCC\_SM\_51, VCC\_SM\_52 VCC\_SM\_53, VCC\_SM\_54 VCC\_SM\_55, VCC\_SM\_56 VCC\_SM\_57, VCC\_SM\_58 VCC\_SM\_59, VCC\_SM\_60 VCC\_SM\_61, VCC\_SM\_62 VCC\_SM\_63, VCC\_SM\_64 VCC\_SM\_65, VCC\_SM\_66 VCC\_SM\_67, VCC\_SM\_68 VCC\_SM\_69, VCC\_SM\_70 VCC\_SM\_71, VCC\_SM\_72 VCC\_SM\_73, VCC\_SM\_74 VCC\_SM\_75, VCC\_SM\_76 VCC\_SM\_77, VCC\_SM\_78 VCC\_SM\_79, VCC\_SM\_80 VCC\_SM\_81, VCC\_SM\_82 VCC\_SM\_83, VCC\_SM\_84 VCC\_SM\_85, VCC\_SM\_86 VCC\_SM\_87, VCC\_SM\_88 VCC\_SM\_89, VCC\_SM\_90 VCC\_SM\_91, VCC\_SM\_92 VCC\_SM\_93, VCC\_SM\_94 VCC\_SM\_95, VCC\_SM\_96 VCC\_SM\_97, VCC\_SM\_98 VCC\_SM\_99, VCC\_SM\_100 VCC\_SM\_101 VCC\_SM\_102 VCC\_SM\_103 VCC\_SM\_104 VCC\_SM\_105 VCC\_SM\_106 VCC\_SM\_107

Pin list for U801G: VCC\_NCTF0 VCC\_NCTF1, VCC\_NCTF2 VCC\_NCTF3, VCC\_NCTF4 VCC\_NCTF5, VCC\_NCTF6 VCC\_NCTF7, VCC\_NCTF8 VCC\_NCTF9, VCC\_NCTF10 VCC\_NCTF11, VCC\_NCTF12 VCC\_NCTF13, VCC\_NCTF14 VCC\_NCTF15, VCC\_NCTF16 VCC\_NCTF17, VCC\_NCTF18 VCC\_NCTF19, VCC\_NCTF20 VCC\_NCTF21, VCC\_NCTF22 VCC\_NCTF23, VCC\_NCTF24 VCC\_NCTF25, VCC\_NCTF26 VCC\_NCTF27, VCC\_NCTF28 VCC\_NCTF29, VCC\_NCTF30 VCC\_NCTF31, VCC\_NCTF32 VCC\_NCTF33, VCC\_NCTF34 VCC\_NCTF35, VCC\_NCTF36 VCC\_NCTF37, VCC\_NCTF38 VCC\_NCTF39, VCC\_NCTF40 VCC\_NCTF41, VCC\_NCTF42 VCC\_NCTF43, VCC\_NCTF44 VCC\_NCTF45, VCC\_NCTF46 VCC\_NCTF47, VCC\_NCTF48 VCC\_NCTF49, VCC\_NCTF50 VCC\_NCTF51, VCC\_NCTF52 VCC\_NCTF53, VCC\_NCTF54 VCC\_NCTF55, VCC\_NCTF56 VCC\_NCTF57, VCC\_NCTF58 VCC\_NCTF59, VCC\_NCTF60 VCC\_NCTF61, VCC\_NCTF62 VCC\_NCTF63, VCC\_NCTF64 VCC\_NCTF65, VCC\_NCTF66 VCC\_NCTF67, VCC\_NCTF68 VCC\_NCTF69, VCC\_NCTF70 VCC\_NCTF71, VCC\_NCTF72

Pin list for CALISTOGA Q137: VSS\_VCC0 VSS\_VCC1, VSS\_VCC2 VSS\_VCC3, VSS\_VCC4 VSS\_VCC5, VSS\_VCC6 VSS\_VCC7, VSS\_VCC8 VSS\_VCC9, VSS\_VCC10 VSS\_VCC11, VSS\_VCC12 VSS\_VCC13, VSS\_VCC14 VSS\_VCC15, VSS\_VCC16 VSS\_VCC17, VSS\_VCC18 VSS\_VCC19, VSS\_VCC20 VSS\_VCC21, VSS\_VCC22 VSS\_VCC23, VSS\_VCC24 VSS\_VCC25, VSS\_VCC26 VSS\_VCC27, VSS\_VCC28 VSS\_VCC29, VSS\_VCC30 VSS\_VCC31, VSS\_VCC32 VSS\_VCC33, VSS\_VCC34 VSS\_VCC35, VSS\_VCC36 VSS\_VCC37, VSS\_VCC38 VSS\_VCC39, VSS\_VCC40 VSS\_VCC41, VSS\_VCC42 VSS\_VCC43, VSS\_VCC44 VSS\_VCC45, VSS\_VCC46 VSS\_VCC47, VSS\_VCC48 VSS\_VCC49, VSS\_VCC50 VSS\_VCC51, VSS\_VCC52 VSS\_VCC53, VSS\_VCC54 VSS\_VCC55, VSS\_VCC56 VSS\_VCC57, VSS\_VCC58 VSS\_VCC59, VSS\_VCC60 VSS\_VCC61, VSS\_VCC62 VSS\_VCC63, VSS\_VCC64 VSS\_VCC65, VSS\_VCC66 VSS\_VCC67, VSS\_VCC68 VSS\_VCC69, VSS\_VCC70 VSS\_VCC71, VSS\_VCC72 VSS\_VCC73, VSS\_VCC74 VSS\_VCC75, VSS\_VCC76 VSS\_VCC77, VSS\_VCC78 VSS\_VCC79, VSS\_VCC80 VSS\_VCC81, VSS\_VCC82 VSS\_VCC83, VSS\_VCC84 VSS\_VCC85, VSS\_VCC86 VSS\_VCC87, VSS\_VCC88 VSS\_VCC89, VSS\_VCC90 VSS\_VCC91, VSS\_VCC92 VSS\_VCC93, VSS\_VCC94 VSS\_VCC95, VSS\_VCC96 VSS\_VCC97, VSS\_VCC98 VSS\_VCC99, VSS\_VCC100 VSS\_VCC101, VSS\_VCC102 VSS\_VCC103 VSS\_VCC104 VSS\_VCC105 VSS\_VCC106 VSS\_VCC107 VSS\_VCC108 VSS\_VCC109 VSS\_VCC110

Pin list for U801J: VSS\_V273 VSS\_V274, VSS\_V275 VSS\_V276, VSS\_V277 VSS\_V278, VSS\_V279 VSS\_V280, VSS\_V281 VSS\_V282, VSS\_V283 VSS\_V284, VSS\_V285 VSS\_V286, VSS\_V287 VSS\_V288, VSS\_V289 VSS\_V290, VSS\_V291 VSS\_V292, VSS\_V293 VSS\_V294, VSS\_V295 VSS\_V296, VSS\_V297 VSS\_V298, VSS\_V299 VSS\_V300, VSS\_V301 VSS\_V302, VSS\_V303 VSS\_V304, VSS\_V305 VSS\_V306, VSS\_V307 VSS\_V308, VSS\_V309 VSS\_V310, VSS\_V311 VSS\_V312, VSS\_V313 VSS\_V314, VSS\_V315 VSS\_V316, VSS\_V317 VSS\_V318, VSS\_V319 VSS\_V320, VSS\_V321 VSS\_V322, VSS\_V323 VSS\_V324, VSS\_V325 VSS\_V326, VSS\_V327 VSS\_V328, VSS\_V329 VSS\_V330, VSS\_V331 VSS\_V332, VSS\_V333 VSS\_V334, VSS\_V335 VSS\_V336, VSS\_V337 VSS\_V338, VSS\_V339 VSS\_V340, VSS\_V341 VSS\_V342, VSS\_V343 VSS\_V344, VSS\_V345 VSS\_V346, VSS\_V347 VSS\_V348, VSS\_V349 VSS\_V350, VSS\_V351 VSS\_V352, VSS\_V353 VSS\_V354, VSS\_V355 VSS\_V356, VSS\_V357 VSS\_V358, VSS\_V359 VSS\_V360

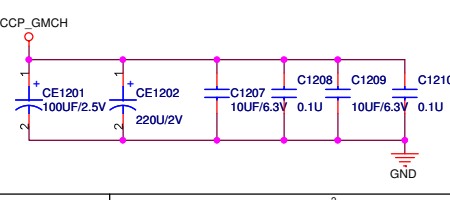
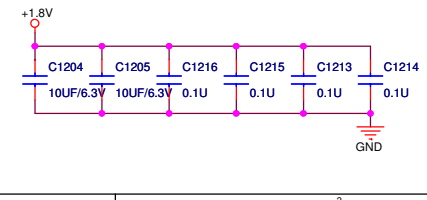
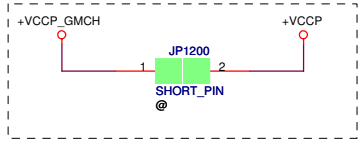
Pin list for CALISTOGA Q137: VSS\_V180 VSS\_V181, VSS\_V182 VSS\_V183, VSS\_V184 VSS\_V185, VSS\_V186 VSS\_V187, VSS\_V188 VSS\_V189, VSS\_V190 VSS\_V191, VSS\_V192 VSS\_V193, VSS\_V194 VSS\_V195, VSS\_V196 VSS\_V197, VSS\_V198 VSS\_V199, VSS\_V200 VSS\_V201, VSS\_V202 VSS\_V203, VSS\_V204 VSS\_V205, VSS\_V206 VSS\_V207, VSS\_V208 VSS\_V209, VSS\_V210 VSS\_V211, VSS\_V212 VSS\_V213, VSS\_V214 VSS\_V215, VSS\_V216 VSS\_V217, VSS\_V218 VSS\_V219, VSS\_V220 VSS\_V221, VSS\_V222 VSS\_V223, VSS\_V224 VSS\_V225, VSS\_V226 VSS\_V227, VSS\_V228 VSS\_V229, VSS\_V230 VSS\_V231, VSS\_V232 VSS\_V233, VSS\_V234 VSS\_V235, VSS\_V236 VSS\_V237, VSS\_V238 VSS\_V239, VSS\_V240 VSS\_V241, VSS\_V242 VSS\_V243, VSS\_V244 VSS\_V245, VSS\_V246 VSS\_V247, VSS\_V248 VSS\_V249, VSS\_V250 VSS\_V251, VSS\_V252 VSS\_V253, VSS\_V254 VSS\_V255, VSS\_V256 VSS\_V257, VSS\_V258 VSS\_V259, VSS\_V260 VSS\_V261, VSS\_V262 VSS\_V263, VSS\_V264 VSS\_V265, VSS\_V266 VSS\_V267, VSS\_V268 VSS\_V269, VSS\_V270 VSS\_V271 VSS\_V272

Pin list for U801I: VSS\_V97 VSS\_V98, VSS\_V99 VSS\_V100, VSS\_V101 VSS\_V102, VSS\_V103 VSS\_V104, VSS\_V105 VSS\_V106, VSS\_V107 VSS\_V108, VSS\_V109 VSS\_V110, VSS\_V111 VSS\_V112, VSS\_V113 VSS\_V114, VSS\_V115 VSS\_V116, VSS\_V117 VSS\_V118, VSS\_V119 VSS\_V120, VSS\_V121 VSS\_V122, VSS\_V123 VSS\_V124, VSS\_V125 VSS\_V126, VSS\_V127 VSS\_V128, VSS\_V129 VSS\_V130, VSS\_V131 VSS\_V132, VSS\_V133 VSS\_V134, VSS\_V135 VSS\_V136, VSS\_V137 VSS\_V138, VSS\_V139 VSS\_V140, VSS\_V141 VSS\_V142, VSS\_V143 VSS\_V144, VSS\_V145 VSS\_V146, VSS\_V147 VSS\_V148, VSS\_V149 VSS\_V150, VSS\_V151 VSS\_V152, VSS\_V153 VSS\_V154, VSS\_V155 VSS\_V156, VSS\_V157 VSS\_V158, VSS\_V159 VSS\_V160, VSS\_V161 VSS\_V162, VSS\_V163 VSS\_V164, VSS\_V165 VSS\_V166, VSS\_V167 VSS\_V168, VSS\_V169 VSS\_V170, VSS\_V171 VSS\_V172, VSS\_V173 VSS\_V174, VSS\_V175 VSS\_V176, VSS\_V177 VSS\_V178, VSS\_V179 VSS\_V180, VSS\_V181 VSS\_V182, VSS\_V183 VSS\_V184, VSS\_V185 VSS\_V186, VSS\_V187 VSS\_V188, VSS\_V189 VSS\_V190, VSS\_V191 VSS\_V192, VSS\_V193 VSS\_V194, VSS\_V195 VSS\_V196, VSS\_V197 VSS\_V198, VSS\_V199 VSS\_V200

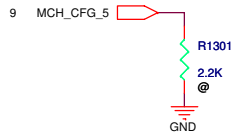
Pin list for CALISTOGA Q137: VSS\_V0 VSS\_V1, VSS\_V2 VSS\_V3, VSS\_V4 VSS\_V5, VSS\_V6 VSS\_V7, VSS\_V8 VSS\_V9, VSS\_V10 VSS\_V11, VSS\_V12 VSS\_V13, VSS\_V14 VSS\_V15, VSS\_V16 VSS\_V17, VSS\_V18 VSS\_V19, VSS\_V20 VSS\_V21, VSS\_V22 VSS\_V23, VSS\_V24 VSS\_V25, VSS\_V26 VSS\_V27, VSS\_V28 VSS\_V29, VSS\_V30 VSS\_V31, VSS\_V32 VSS\_V33, VSS\_V34 VSS\_V35, VSS\_V36 VSS\_V37, VSS\_V38 VSS\_V39, VSS\_V40 VSS\_V41, VSS\_V42 VSS\_V43, VSS\_V44 VSS\_V45, VSS\_V46 VSS\_V47, VSS\_V48 VSS\_V49, VSS\_V50 VSS\_V51, VSS\_V52 VSS\_V53, VSS\_V54 VSS\_V55, VSS\_V56 VSS\_V57, VSS\_V58 VSS\_V59, VSS\_V60 VSS\_V61, VSS\_V62 VSS\_V63, VSS\_V64 VSS\_V65, VSS\_V66 VSS\_V67, VSS\_V68 VSS\_V69, VSS\_V70 VSS\_V71, VSS\_V72 VSS\_V73, VSS\_V74 VSS\_V75, VSS\_V76 VSS\_V77, VSS\_V78 VSS\_V79, VSS\_V80 VSS\_V81, VSS\_V82 VSS\_V83, VSS\_V84 VSS\_V85, VSS\_V86 VSS\_V87, VSS\_V88 VSS\_V89, VSS\_V90 VSS\_V91, VSS\_V92 VSS\_V93, VSS\_V94 VSS\_V95, VSS\_V96 VSS\_V97, VSS\_V98 VSS\_V99, VSS\_V100 VSS\_V101, VSS\_V102 VSS\_V103 VSS\_V104 VSS\_V105 VSS\_V106 VSS\_V107 VSS\_V108 VSS\_V109 VSS\_V110

Pin list for U801I: VSS\_V0 VSS\_V1, VSS\_V2 VSS\_V3, VSS\_V4 VSS\_V5, VSS\_V6 VSS\_V7, VSS\_V8 VSS\_V9, VSS\_V10 VSS\_V11, VSS\_V12 VSS\_V13, VSS\_V14 VSS\_V15, VSS\_V16 VSS\_V17, VSS\_V18 VSS\_V19, VSS\_V20 VSS\_V21, VSS\_V22 VSS\_V23, VSS\_V24 VSS\_V25, VSS\_V26 VSS\_V27, VSS\_V28 VSS\_V29, VSS\_V30 VSS\_V31, VSS\_V32 VSS\_V33, VSS\_V34 VSS\_V35, VSS\_V36 VSS\_V37, VSS\_V38 VSS\_V39, VSS\_V40 VSS\_V41, VSS\_V42 VSS\_V43, VSS\_V44 VSS\_V45, VSS\_V46 VSS\_V47, VSS\_V48 VSS\_V49, VSS\_V50 VSS\_V51, VSS\_V52 VSS\_V53, VSS\_V54 VSS\_V55, VSS\_V56 VSS\_V57, VSS\_V58 VSS\_V59, VSS\_V60 VSS\_V61, VSS\_V62 VSS\_V63, VSS\_V64 VSS\_V65, VSS\_V66 VSS\_V67, VSS\_V68 VSS\_V69, VSS\_V70 VSS\_V71, VSS\_V72 VSS\_V73, VSS\_V74 VSS\_V75, VSS\_V76 VSS\_V77, VSS\_V78 VSS\_V79, VSS\_V80 VSS\_V81, VSS\_V82 VSS\_V83, VSS\_V84 VSS\_V85, VSS\_V86 VSS\_V87, VSS\_V88 VSS\_V89, VSS\_V90 VSS\_V91, VSS\_V92 VSS\_V93, VSS\_V94 VSS\_V95, VSS\_V96 VSS\_V97, VSS\_V98 VSS\_V99, VSS\_V100 VSS\_V101, VSS\_V102 VSS\_V103 VSS\_V104 VSS\_V105 VSS\_V106 VSS\_V107 VSS\_V108 VSS\_V109 VSS\_V110

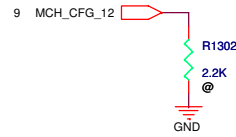
Pin list for CALISTOGA Q137: VSS\_V0 VSS\_V1, VSS\_V2 VSS\_V3, VSS\_V4 VSS\_V5, VSS\_V6 VSS\_V7, VSS\_V8 VSS\_V9, VSS\_V10 VSS\_V11, VSS\_V12 VSS\_V13, VSS\_V14 VSS\_V15, VSS\_V16 VSS\_V17, VSS\_V18 VSS\_V19, VSS\_V20 VSS\_V21, VSS\_V22 VSS\_V23, VSS\_V24 VSS\_V25, VSS\_V26 VSS\_V27, VSS\_V28 VSS\_V29, VSS\_V30 VSS\_V31, VSS\_V32 VSS\_V33, VSS\_V34 VSS\_V35, VSS\_V36 VSS\_V37, VSS\_V38 VSS\_V39, VSS\_V40 VSS\_V41, VSS\_V42 VSS\_V43, VSS\_V44 VSS\_V45, VSS\_V46 VSS\_V47, VSS\_V48 VSS\_V49, VSS\_V50 VSS\_V51, VSS\_V52 VSS\_V53, VSS\_V54 VSS\_V55, VSS\_V56 VSS\_V57, VSS\_V58 VSS\_V59, VSS\_V60 VSS\_V61, VSS\_V62 VSS\_V63, VSS\_V64 VSS\_V65, VSS\_V66 VSS\_V67, VSS\_V68 VSS\_V69, VSS\_V70 VSS\_V71, VSS\_V72 VSS\_V73, VSS\_V74 VSS\_V75, VSS\_V76 VSS\_V77, VSS\_V78 VSS\_V79, VSS\_V80 VSS\_V81, VSS\_V82 VSS\_V83, VSS\_V84 VSS\_V85, VSS\_V86 VSS\_V87, VSS\_V88 VSS\_V89, VSS\_V90 VSS\_V91, VSS\_V92 VSS\_V93, VSS\_V94 VSS\_V95, VSS\_V96 VSS\_V97, VSS\_V98 VSS\_V99, VSS\_V100 VSS\_V101, VSS\_V102 VSS\_V103 VSS\_V104 VSS\_V105 VSS\_V106 VSS\_V107 VSS\_V108 VSS\_V109 VSS\_V110



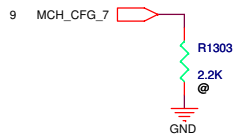
ASUS logo and project information: Title: Calistoga-GND, Engineer: Chao-liang Hung, Date: Monday, October 16, 2006, Sheet 12 of 63, Rev 2.00



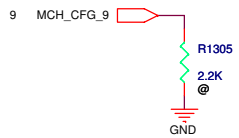
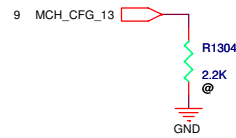
**CFG5 : DMI STRAP**  
 LOW = DMI X 2  
**HIGH = DMI X 4 (Default)**



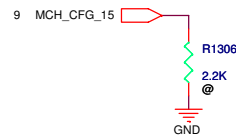
**CFG[13:12] : GMCH TEST MODE SELECT**  
 00 = Partial CLK gating disable  
 01 = XOR Mode Enable  
 10 = ALL Z Mode Enable  
**11 = NORMAL OPERATION (Default)**



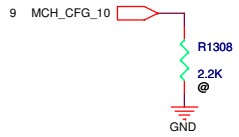
**CFG7 : CPU STRAP**  
 LOW = RESERVED  
**HIGH = Mobile Yonah CPU (Default)**



**CFG9 : PCIE GRAPHIC LANE**  
**LOW = REVERSE LANE**  
 HIGH = NORMAL OPERATION (Default)



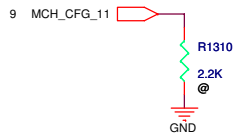
**CFG15 : ICH RESET Disable**  
 LOW = ICH RESET Disabled  
**HIGH = Normal Operation (Default)**



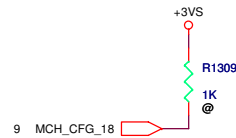
**CFG10 : HOST PLL VCO SELECT**  
 LOW = RESERVED  
**HIGH = MOBILITY (Default)**



**CFG16 : FSB Dynamic ODT**  
 LOW = Dynamic ODT Disabled  
**HIGH = Dynamic ODT Enabled (Default)**

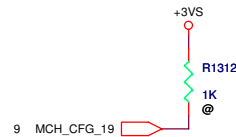


**CFG11 : PSB 4x CLK ENABLE**  
 LOW = 4X ENABLED  
**HIGH = 8X ENABLED (Default)**



**CFG18 : GMCH Core Voltage Level**  
**LOW = 1.05V (Default)**  
 HIGH = 1.5V

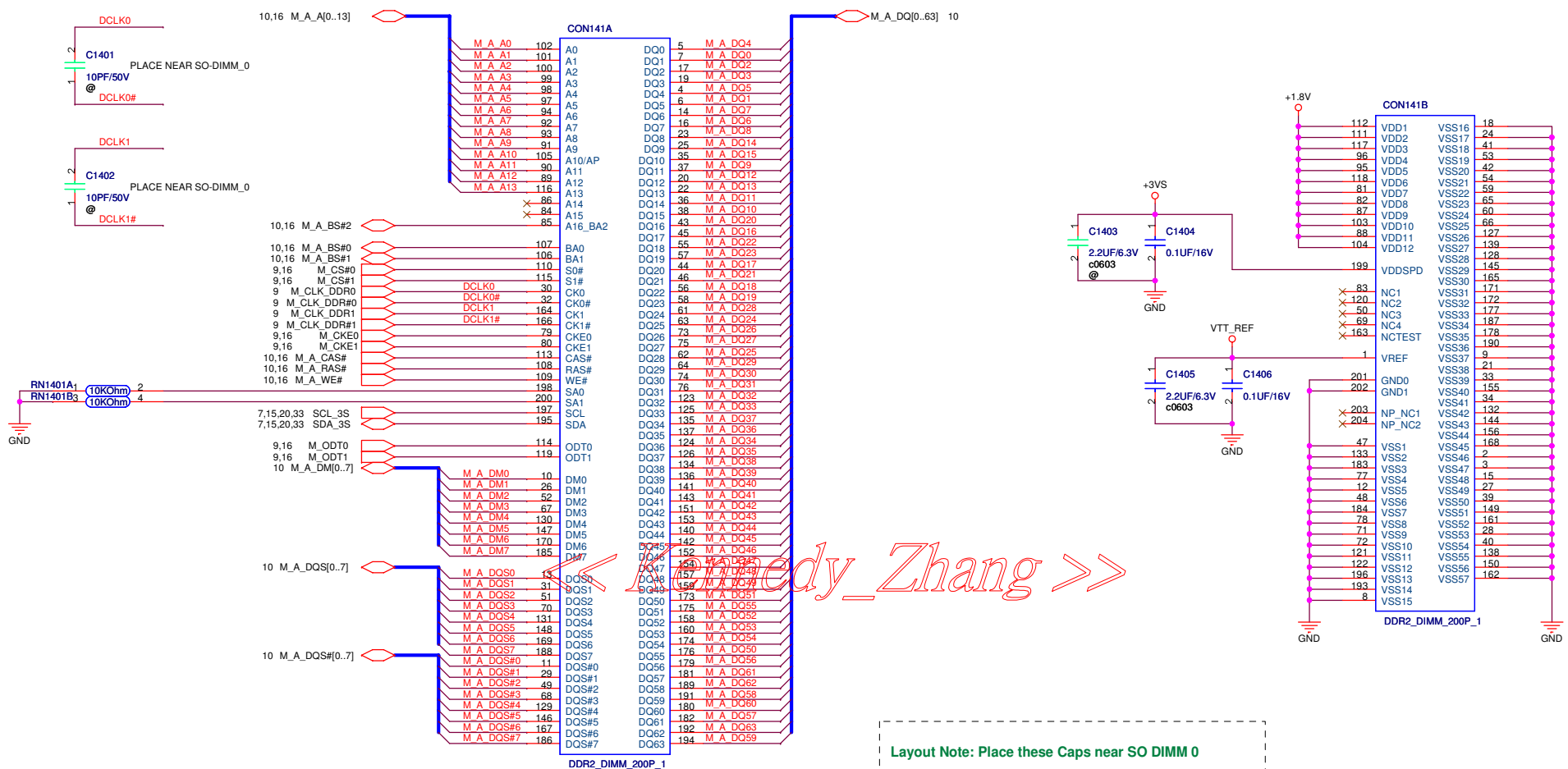
CFG[17..3] have internal pullup resistors.  
 CFG[19..18] have internal pulldown resistors.  
 SDVOCRTL\_DATA has internal pulldown resistors.



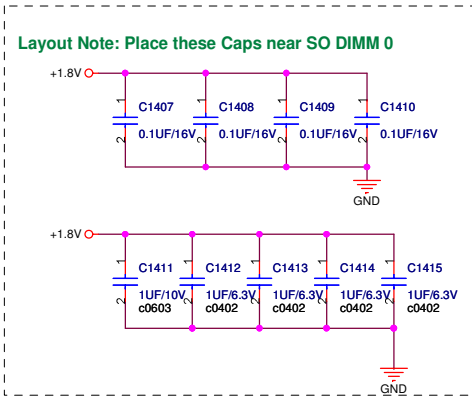
**CFG19 : DMI LANE REVERSAL**  
**LOW = NORMAL (Default)**  
 HIGH = LANES REVERSED

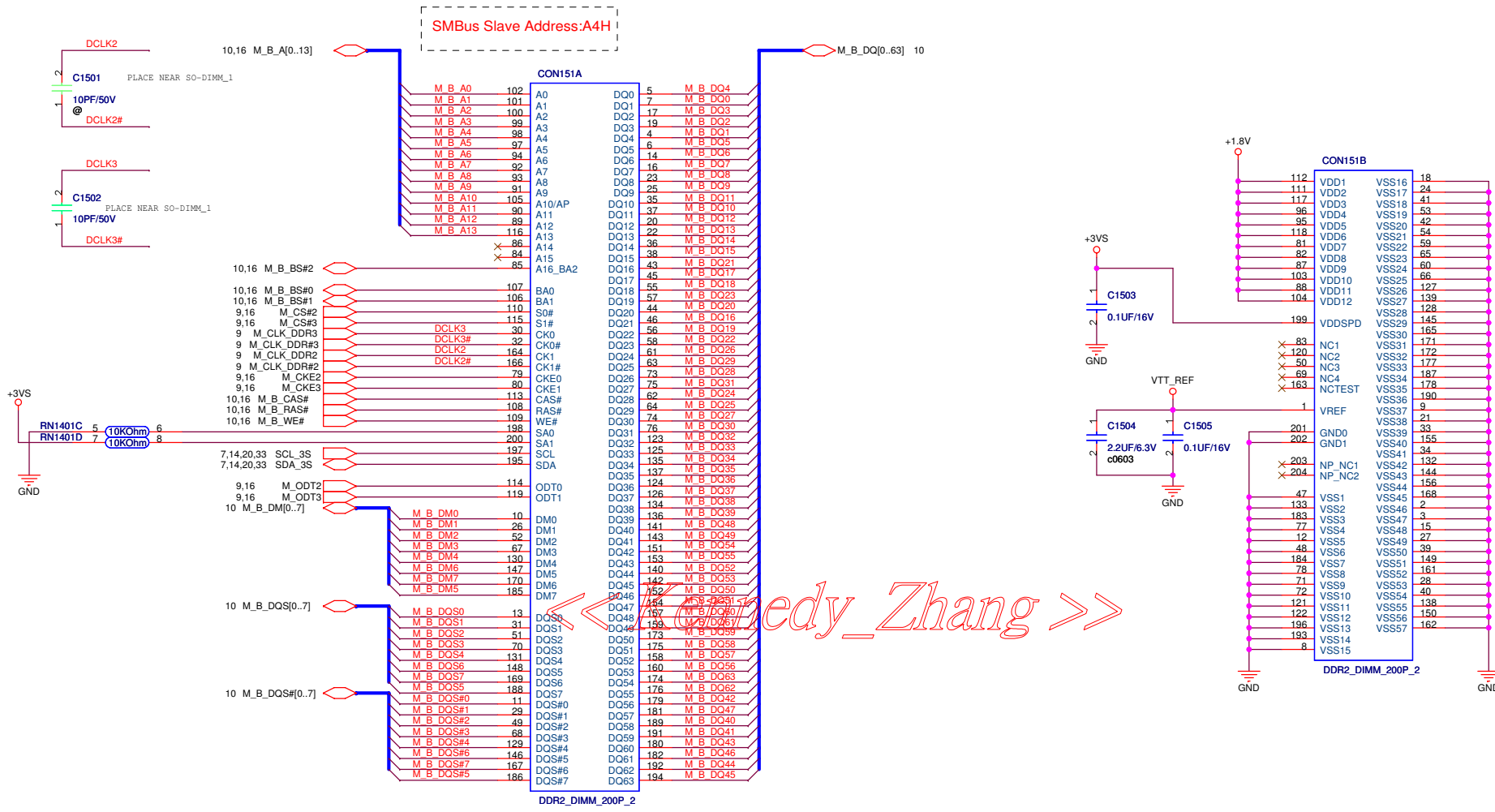
Kennedy\_Zhang

SMBus Slave Address:A0H

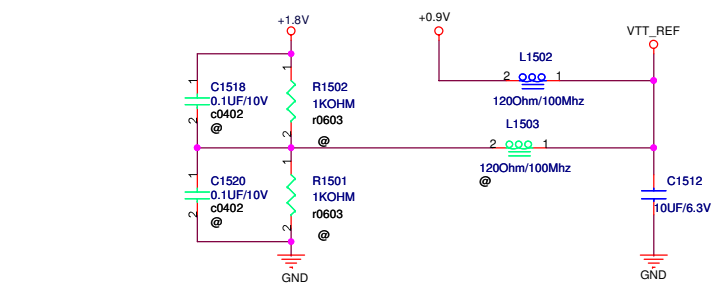
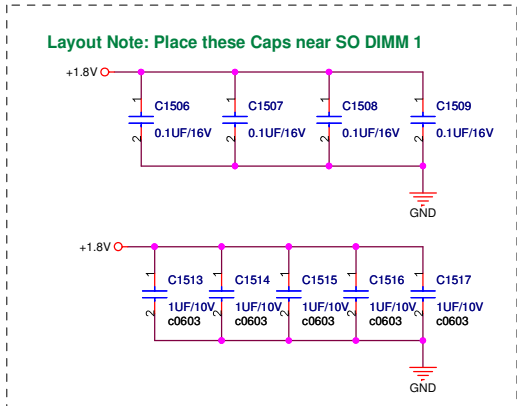


High: 4.0 mm





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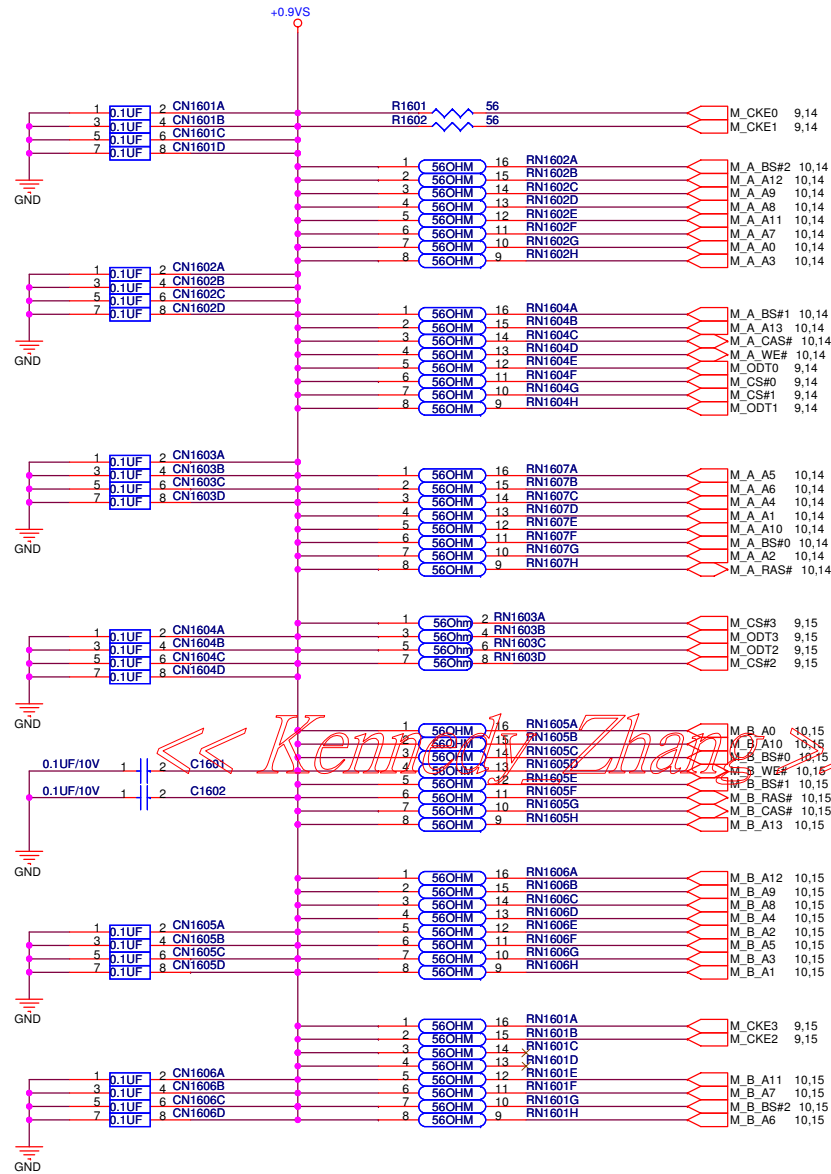
<Variant Name>

**ASUS** Title : **DDR2 SO-DIMM\_1**

ASUSTek COMPUTER INC Engineer: **Chao-liang\_Hung**

Size	Project Name	Rev
Custom	<b>F9F</b>	2.00

Date: Wednesday, October 04, 2006 Sheet 15 of 63



Kenji Zhan

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

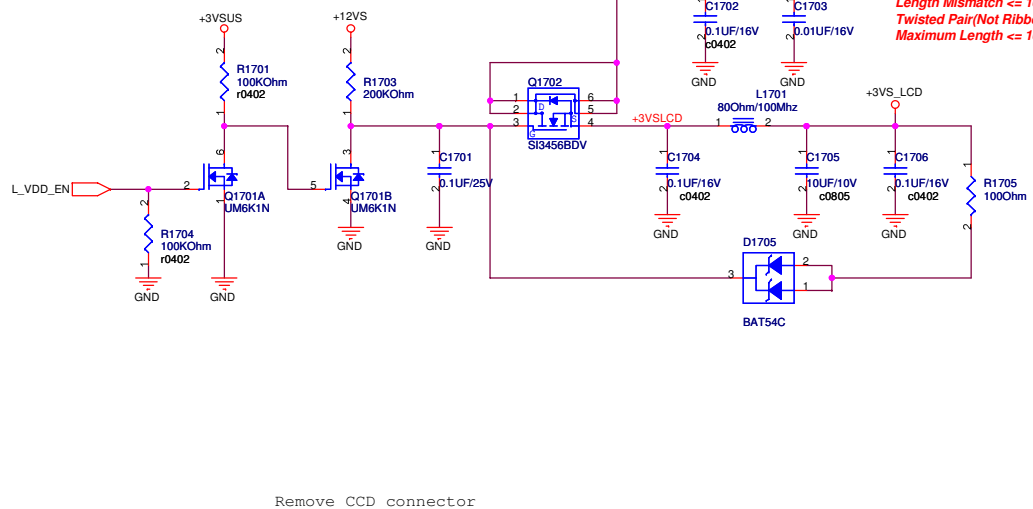
<Variant Name>

<b>ASUS</b>		<b>Title :DDR2 TERMINATION</b>
ASUSTek COMPUTER INC		Engineer: <i>Chao-Iiang Hung</i>
Size Custom	Project Name <b>F9F</b>	Rev 2.00
Date: Wednesday, October 04, 2006		Sheet 16 of 63

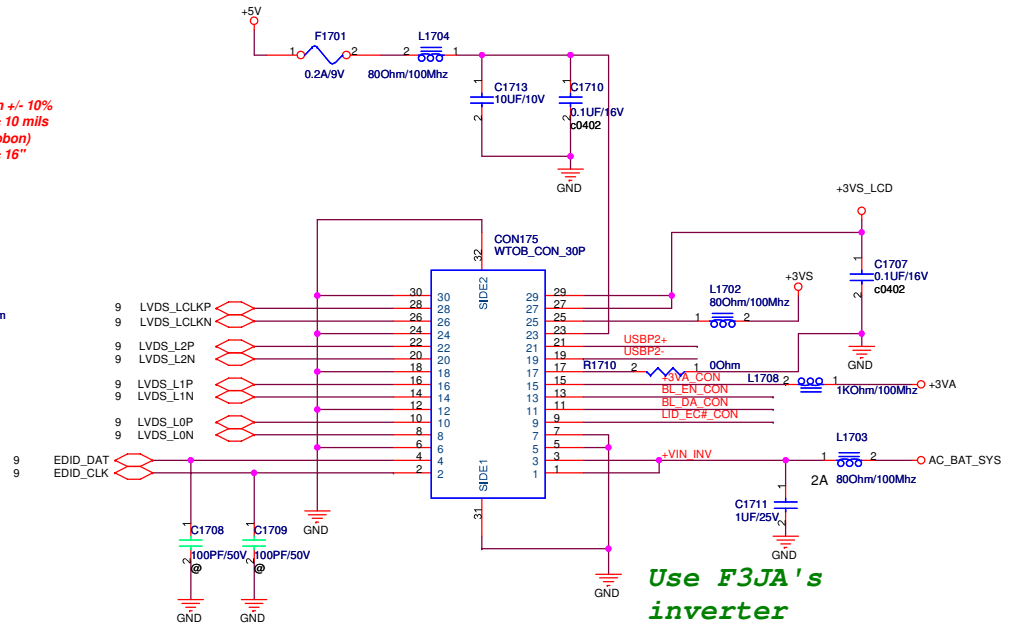


# LCD Backlight Control

## LCD Power



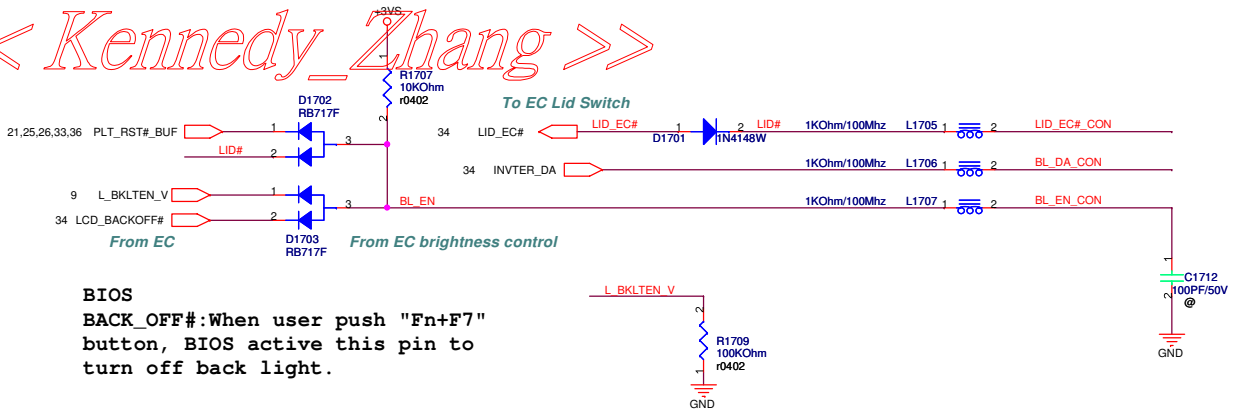
**Cable Requirement:**  
 Impedence: 100 ohm +/- 10%  
 Length Mismatch <= 10 mils  
 Twisted Pair(Not Ribbon)  
 Maximum Length <= 16"



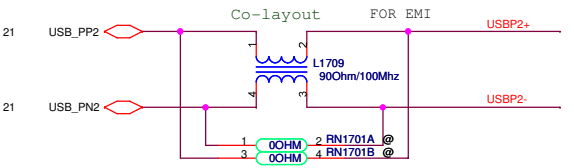
Use F3JA's inverter

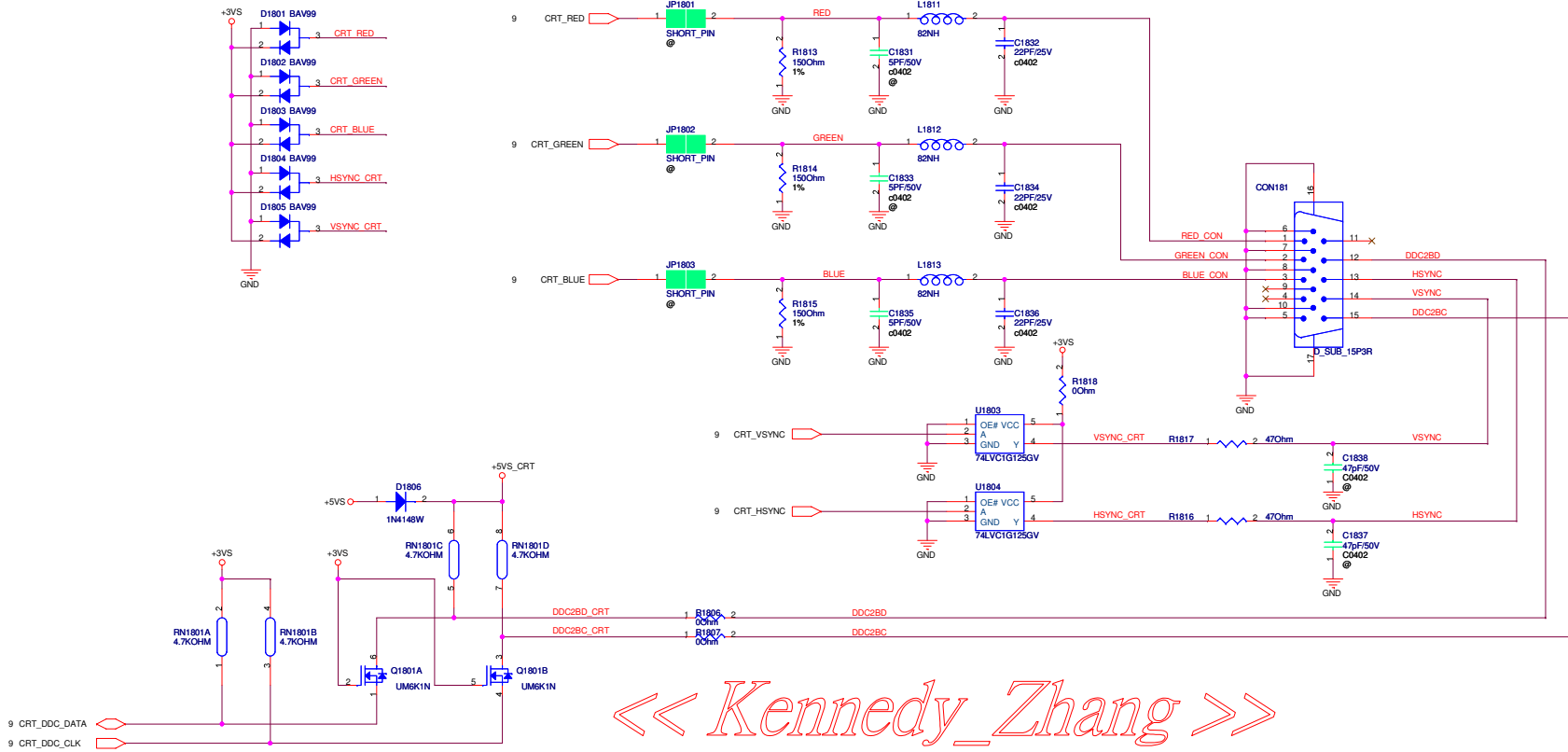
Remove CCD connector

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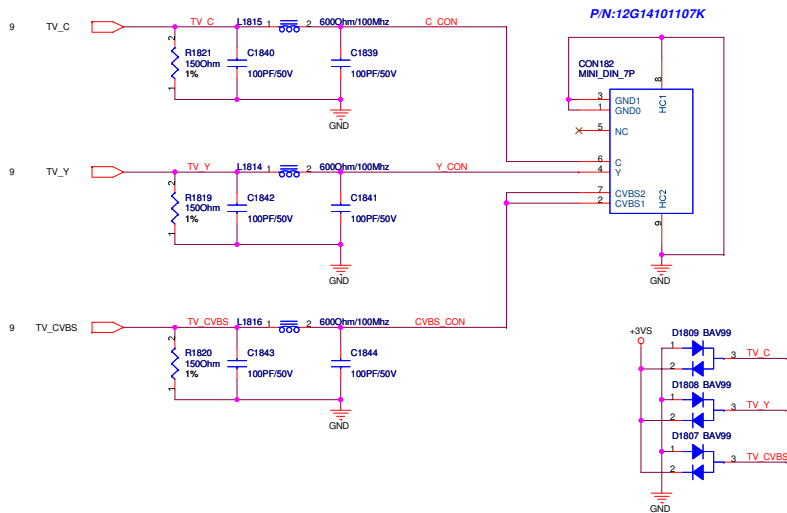
**BIOS BACK\_OFF#:** When user push "Fn+F7" button, BIOS active this pin to turn off back light.



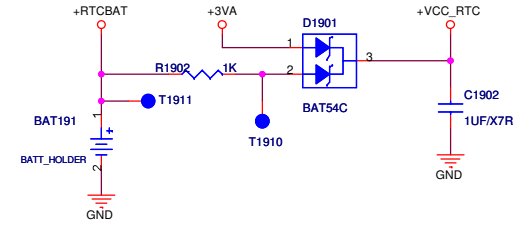
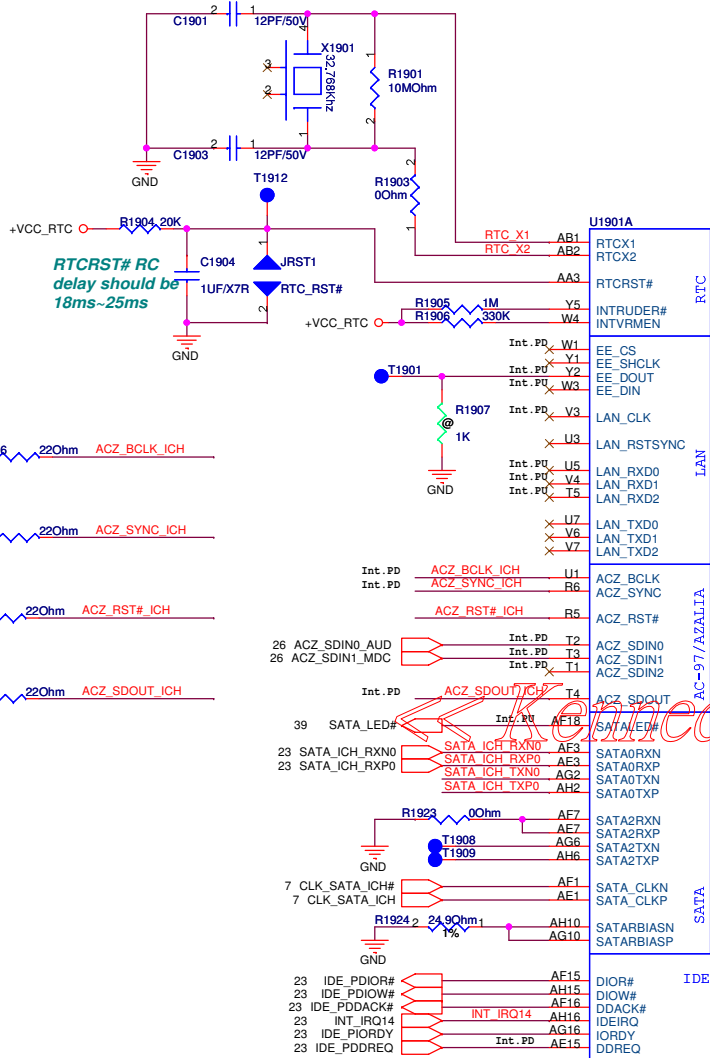


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TV

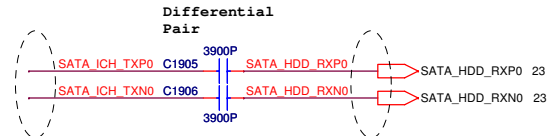


Request of CSC for CMOS clear function



RTCST# RC delay should be 18ms-25ms

- 26 ACZ\_BCLK → R1926 220hm ACZ\_BCLK\_ICH
- 26 ACZ\_SYNC → R1928 220hm ACZ\_SYNC\_ICH
- 26 ACZ\_RST# → R1925 220hm ACZ\_RST#\_ICH
- 26 ACZ\_SDIN0\_AUD → T2
- 26 ACZ\_SDIN1\_MDC → T3
- 26 ACZ\_SDOUT → R1927 220hm ACZ\_SDOUT\_ICH



<Variant Name>

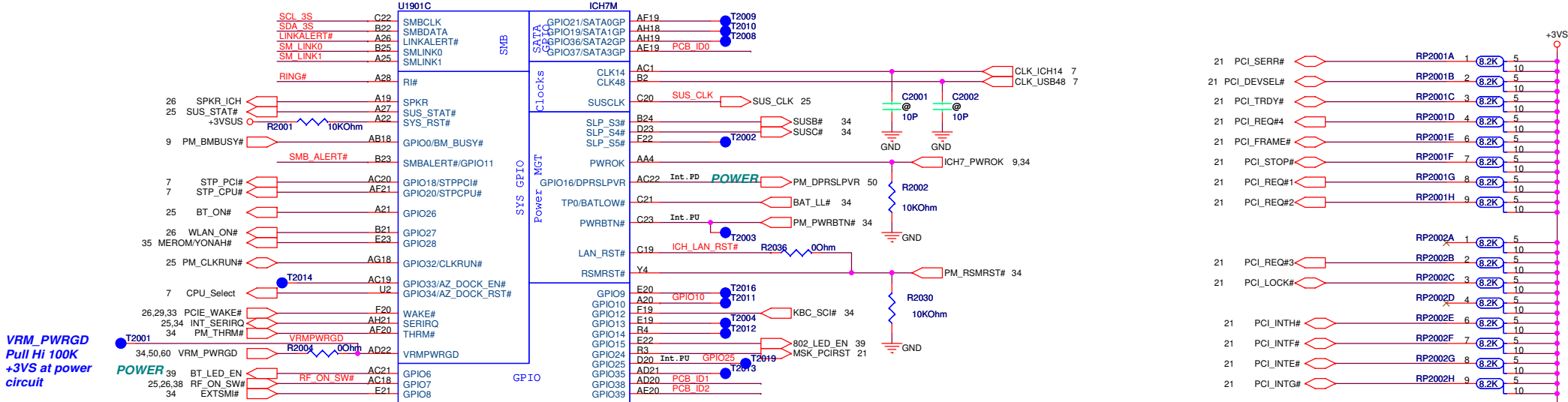
**ASUS** Title : ICH7M (1)

ASUSTek COMPUTER INC Engineer: Chao-liang Hung

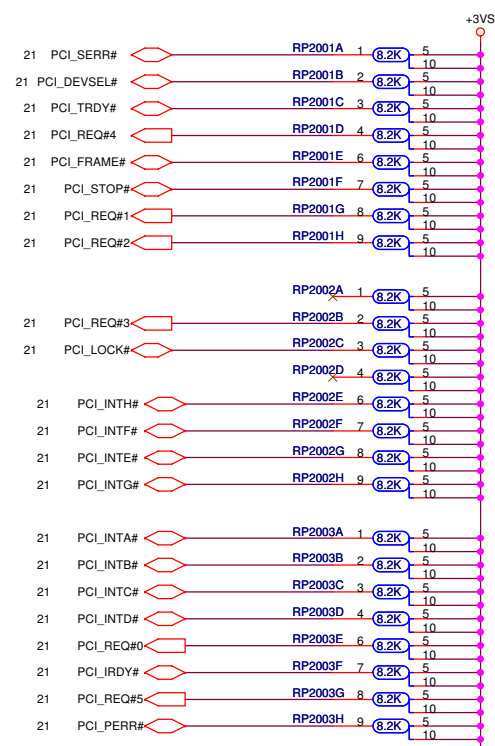
Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 19 of 63

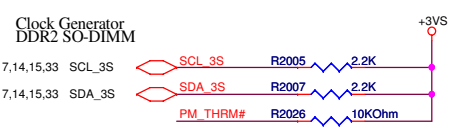
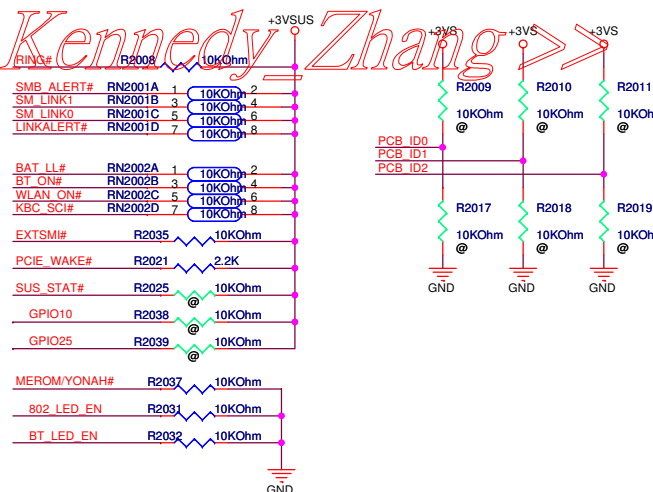
To new card check power plane

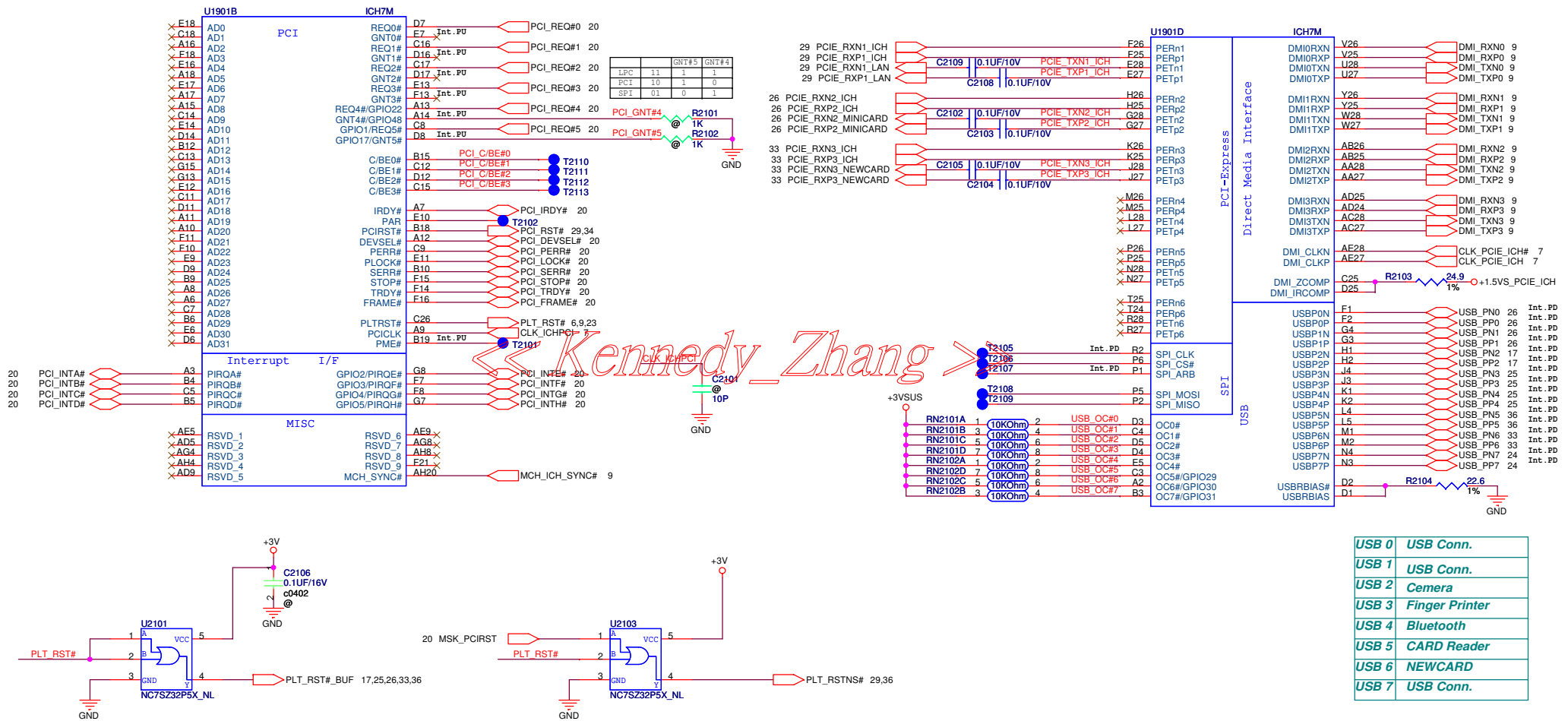


VRM\_PWRGD Pull Hi 100K +3VS at power circuit



<< Kennedy Zhang >>

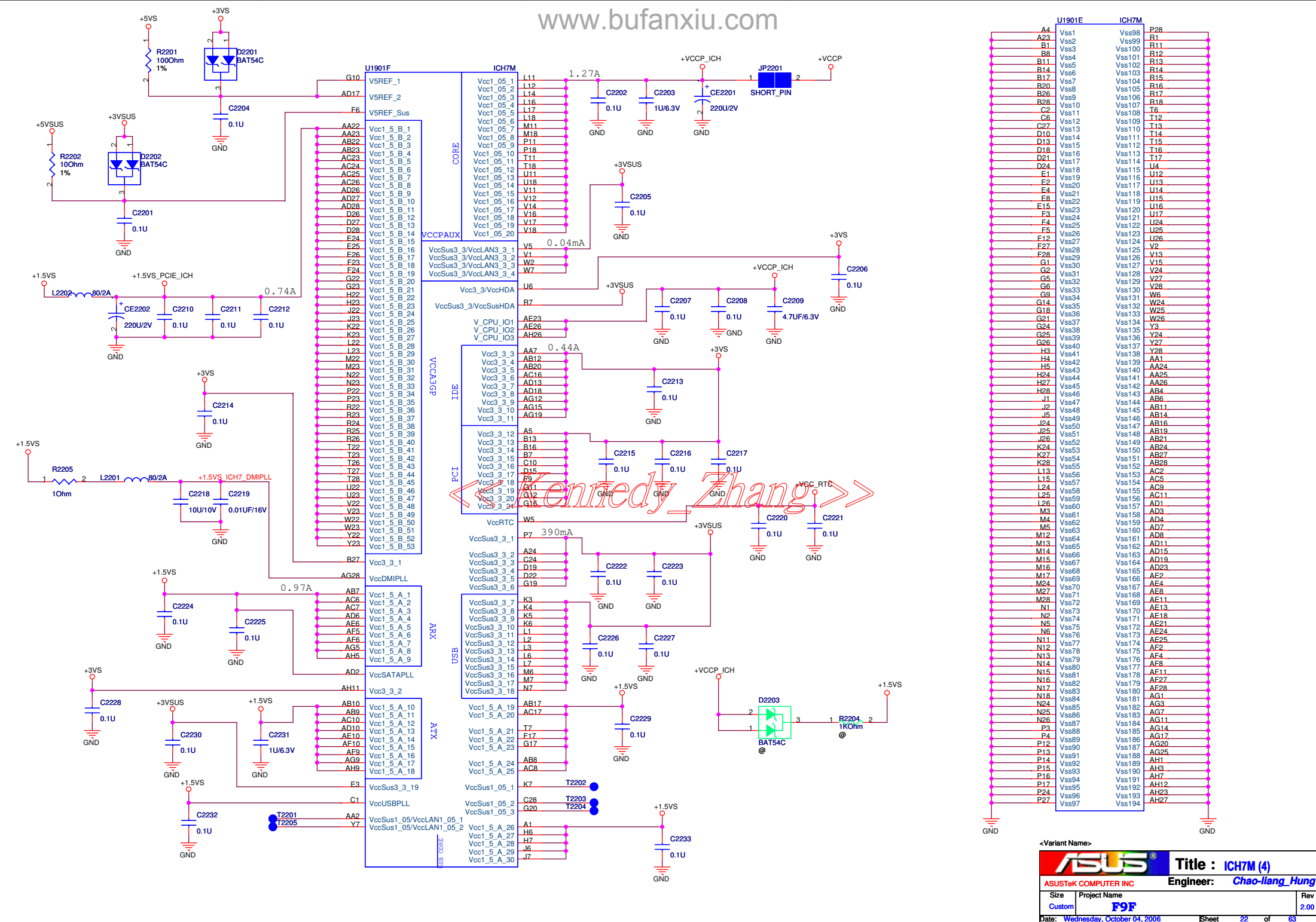




Kennedy\_Zhang

<Variant Name>

<b>ASUS</b>		<b>Title : ICH7M (3)</b>
ASUSTek COMPUTER INC		Engineer: <b>Chao-liang Hung</b>
Size Custom	Project Name <b>F9F</b>	Rev 2.00
Date: Wednesday, October 04, 2006	Sheet 21	of 63



Kennedy Zhang

U1901E	ICH7M	P28
A4	Vss1	R1
A23	Vss2	R11
B1	Vss3	R100
B8	Vss4	Vss101
B11	Vss5	Vss102
B14	Vss6	Vss103
B17	Vss7	Vss104
B26	Vss8	Vss105
B28	Vss9	Vss106
B30	Vss10	Vss107
C2	Vss11	Vss108
C6	Vss12	Vss109
C7	Vss13	Vss110
D10	Vss14	T14
D13	Vss15	T15
D18	Vss16	T16
D21	Vss17	T17
D24	Vss18	U4
E1	Vss19	U12
E2	Vss20	U13
E8	Vss21	U14
E15	Vss22	U15
F3	Vss23	U16
F4	Vss24	U17
F5	Vss25	U24
F12	Vss26	U25
F27	Vss27	U26
F28	Vss28	V2
G1	Vss29	V13
G2	Vss30	V15
G5	Vss31	V24
G6	Vss32	V27
G9	Vss33	W6
G14	Vss34	W24
G18	Vss35	W25
G21	Vss36	W33
G24	Vss37	W34
G25	Vss38	Y3
G26	Vss39	Y27
H3	Vss40	Y28
H4	Vss41	Y38
H5	Vss42	Y39
H24	Vss43	AA24
H28	Vss44	AA25
H28	Vss45	AA26
J2	Vss46	AB4
J5	Vss47	AB6
J24	Vss48	AB11
J25	Vss49	AB14
J26	Vss50	AB16
K24	Vss51	AB19
K27	Vss52	AB19
K28	Vss53	AB24
L13	Vss54	AB27
L15	Vss55	AC2
L24	Vss56	AC5
L25	Vss57	AC9
L26	Vss58	AC11
M3	Vss59	AD1
M4	Vss60	AD3
M5	Vss61	AD4
M12	Vss62	AD7
M13	Vss63	AD8
M14	Vss64	AD15
M15	Vss65	AD19
M16	Vss66	AD23
M17	Vss67	AE2
M24	Vss68	AE4
M27	Vss69	AE8
M28	Vss70	AE18
N1	Vss71	AE18
N2	Vss72	AE21
N5	Vss73	AE24
N6	Vss74	AE25
N11	Vss75	AE2
N12	Vss76	AE25
N13	Vss77	AF4
N14	Vss78	AF8
N15	Vss79	AF11
N16	Vss80	AF17
N17	Vss81	AF27
N18	Vss82	AF28
N24	Vss83	AG1
N25	Vss84	AG3
N26	Vss85	AG7
P3	Vss86	AG11
P4	Vss87	AG14
P12	Vss88	AG17
P13	Vss89	AG20
P14	Vss90	AG25
P15	Vss91	AH1
P16	Vss92	AH3
P17	Vss93	AH7
P24	Vss94	AH12
P27	Vss95	AH23
	Vss96	AH27
	Vss97	

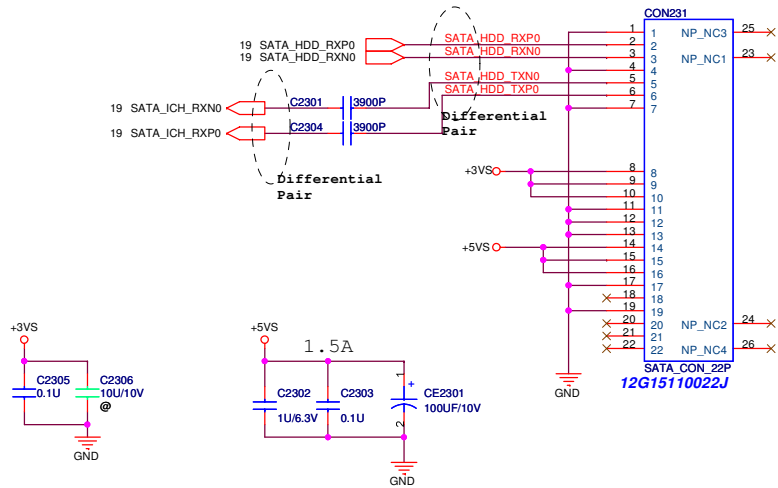
<Variant Name>

**Title : ICH7M (4)**  
**Engineer: Chao-liang Hung**

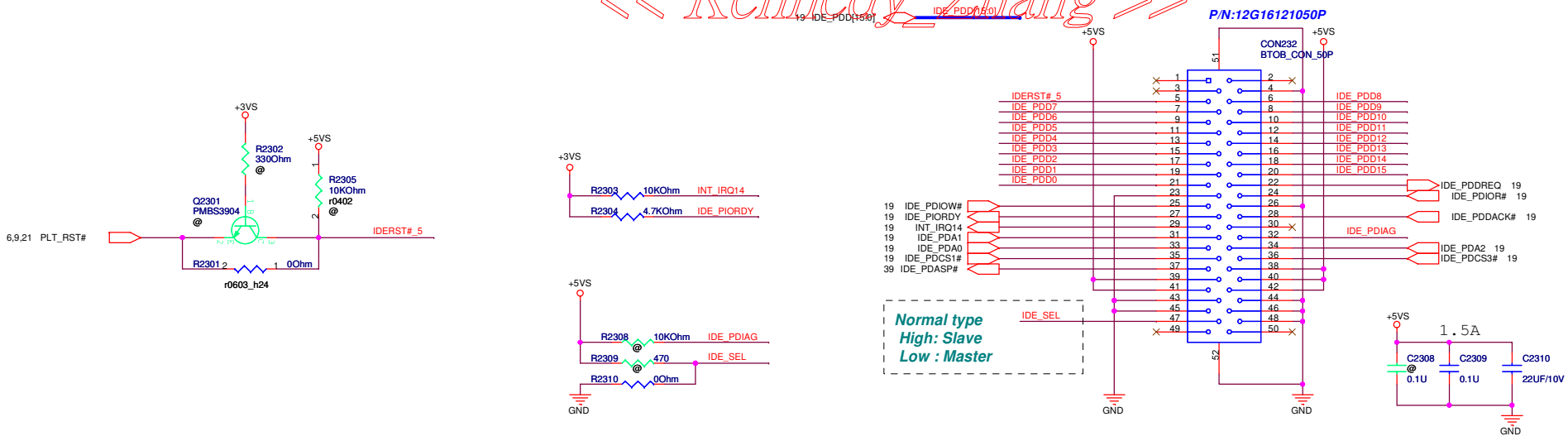
Size	Project Name	Rev
Custom	F9F	2.00

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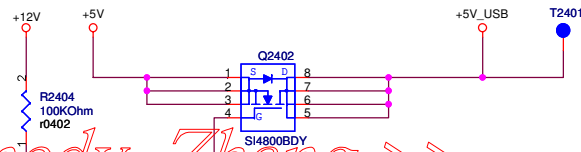
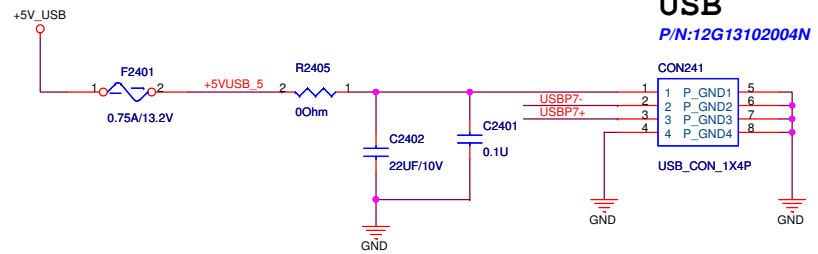
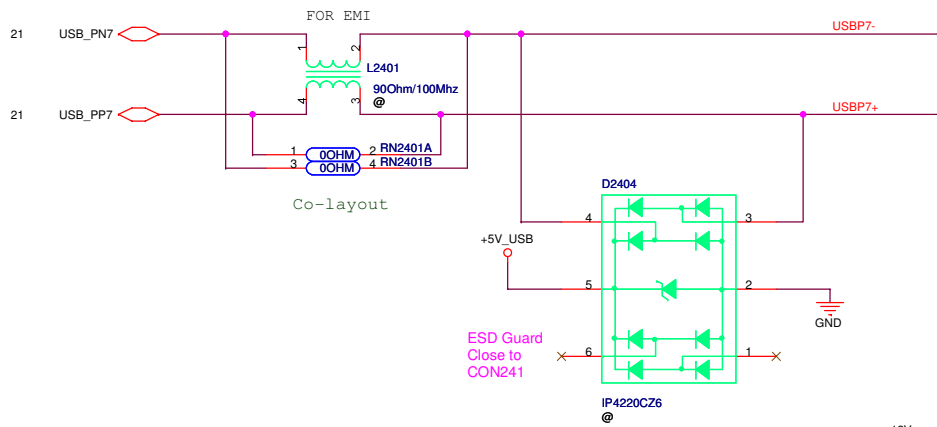
### SATA HDD CON



### << Kennedy Zhang >> PATA CD-ROM CON



<-Variant Name>

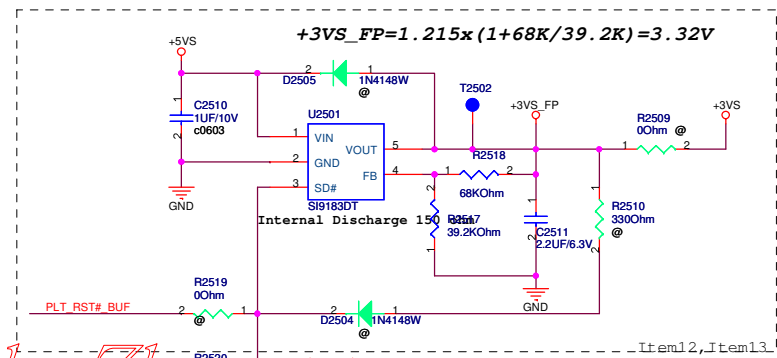
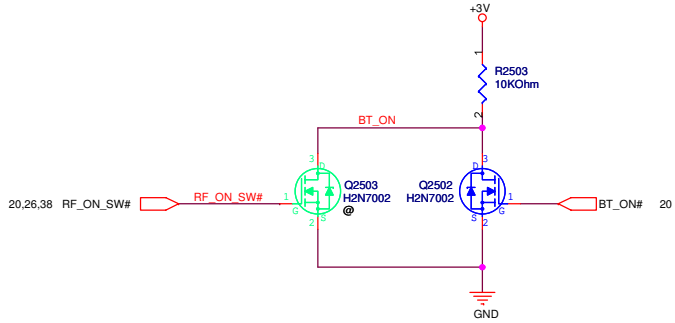
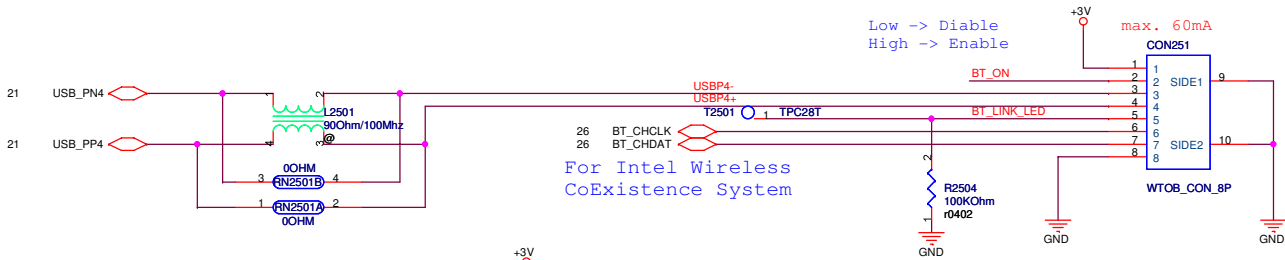


<< Kennedy\_Zhang >>

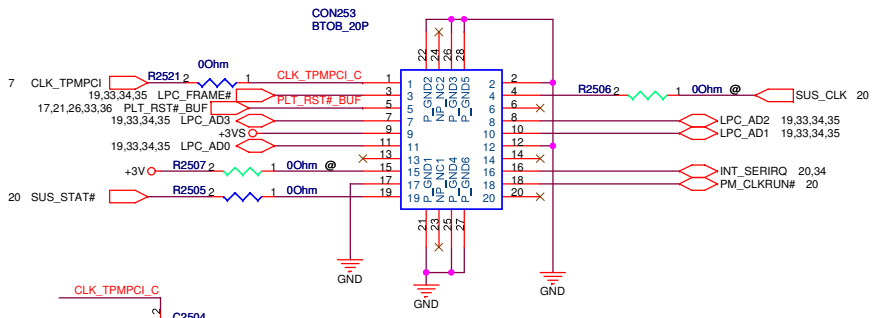
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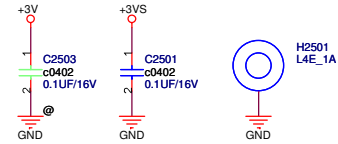
Co-layout FOR EMI



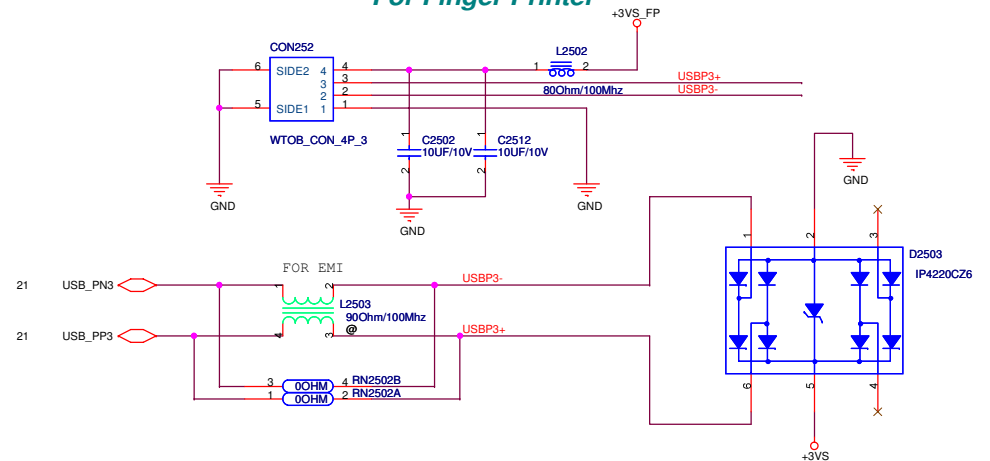
<< Kennedy\_Zhang >>



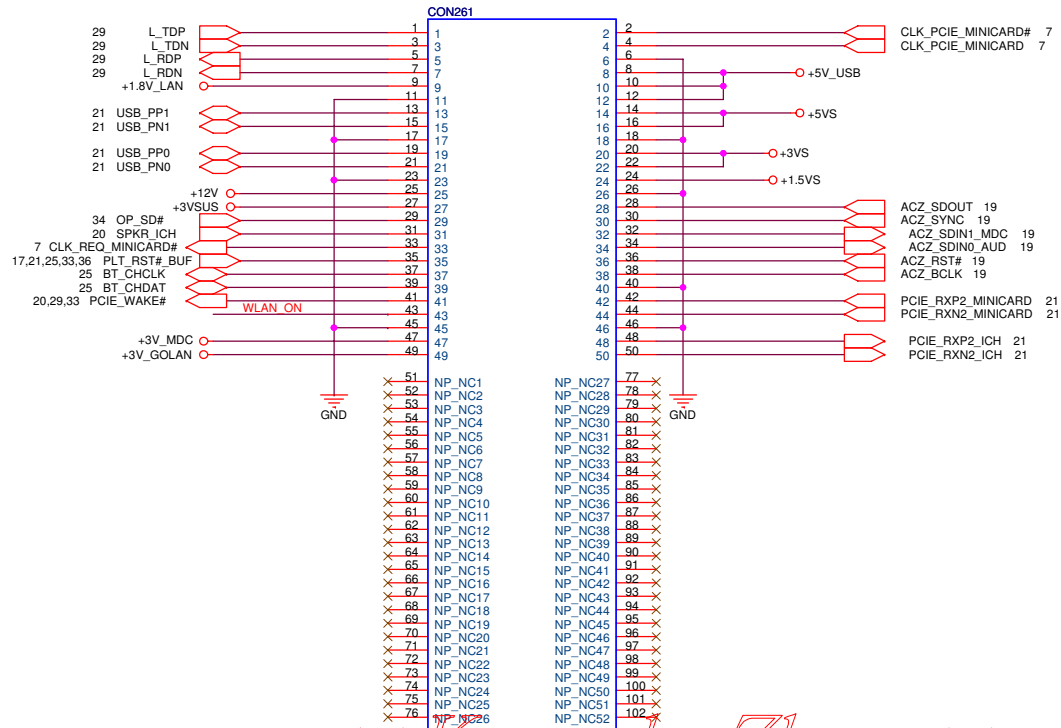
TPM Module CON



For Finger Printer



<Variant Name>



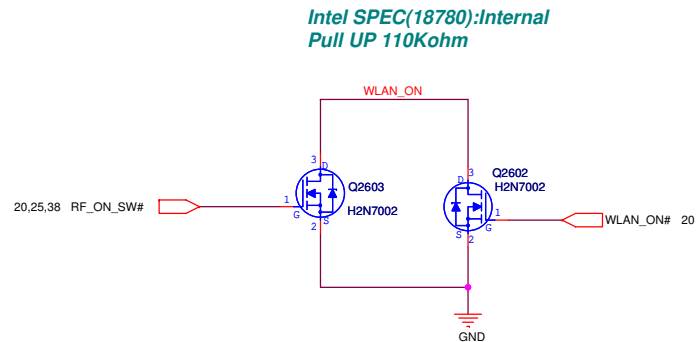
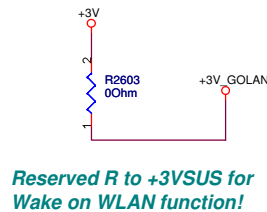
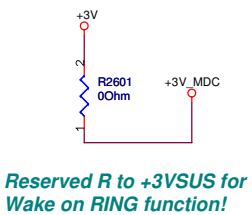
**POWER CONSUMPTION:**  
**+3VS: +3.003V~+3.597V**  
**Max= 750 mA**

**+1.5VS:+1.425V~+1.575V**  
**Max= 375 mA**

**+3VAUX\_GOLAN:+3.003V~+3.597V**  
**Max= 250 mA**


**+3VAUX\_MDC:+3.003V~+3.597V**  
**Max= 300 mA**

<< Kennedy\_Zhang >>




<< Kennedy\_Zhang >>

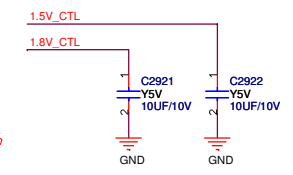
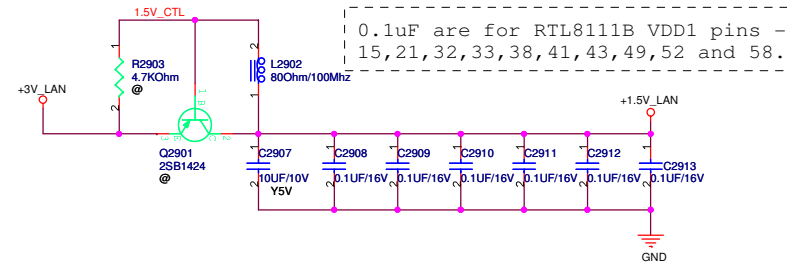
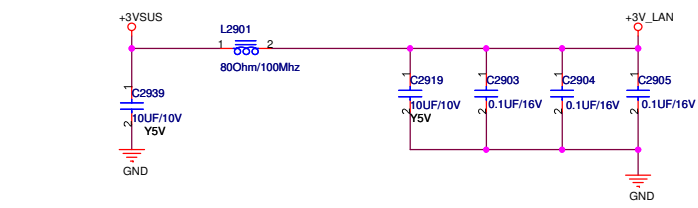
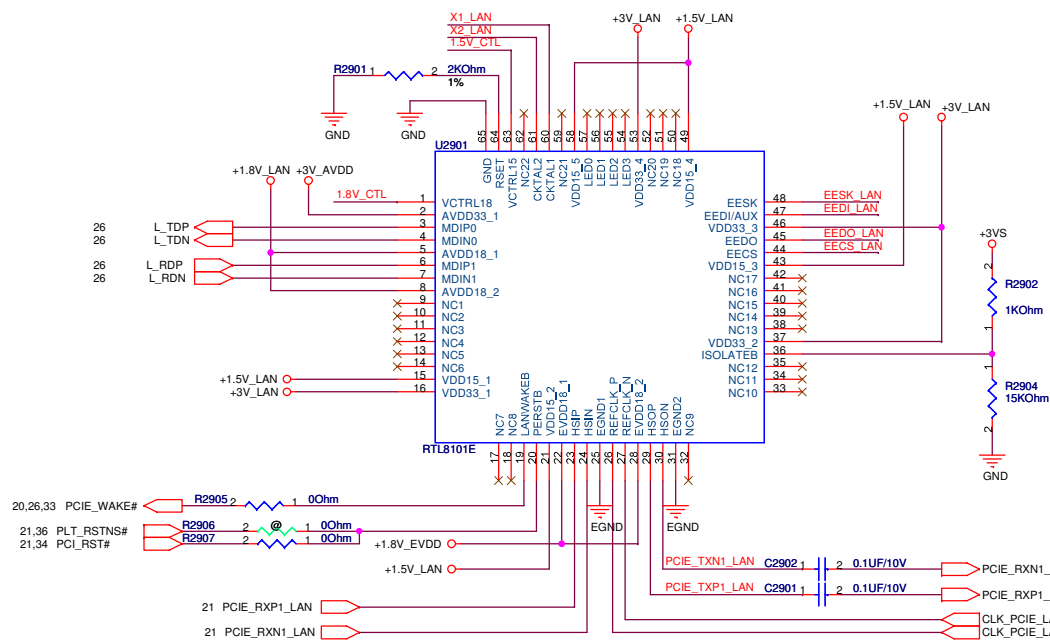
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		<b>Title :</b> EMPTY	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Chao-liang_Hung	
Size	Project Name	Rev	
Custom	F9F	2.00	
Date: Wednesday, October 04, 2006		Sheet	27 of 63

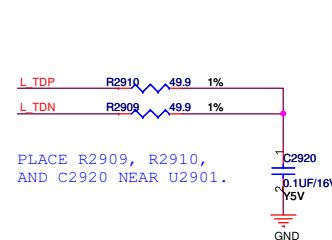
<< Kennedy\_Zhang >>

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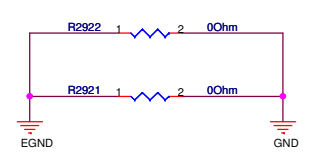
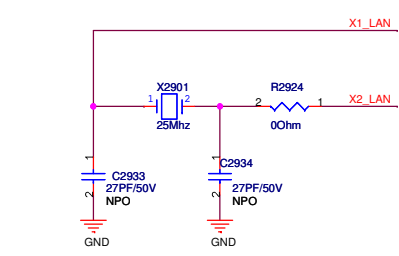
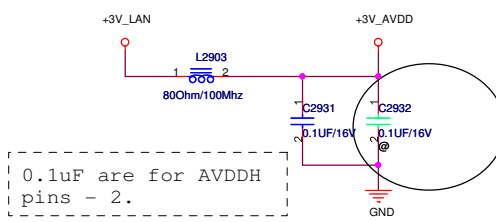
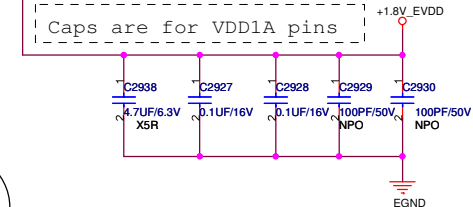
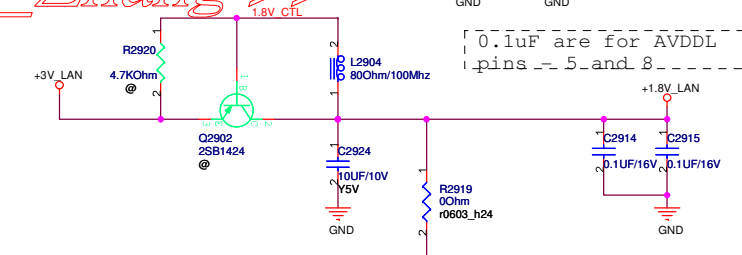
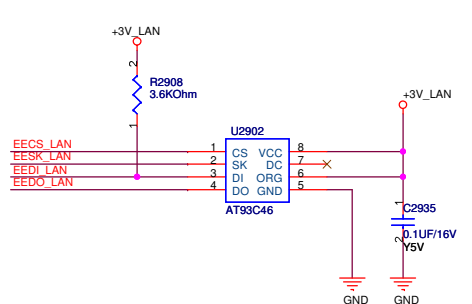
		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Chao-liang_Hung</i>	
Size	Project Name	Rev	
Custom	<b>F9F</b>	2.00	
Date: Wednesday, October 04, 2006		Sheet	28 of 63



<< Kennedy\_Zhang >>



PLACE R2909, R2910, AND C2920 NEAR U2901.




<< Kennedy\_Zhang >>

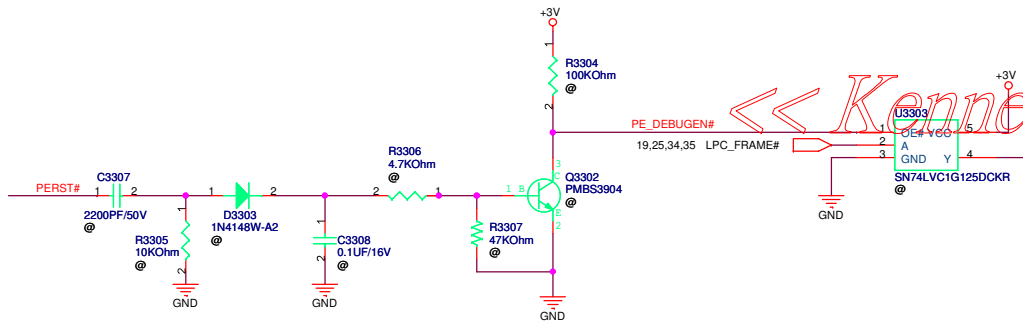
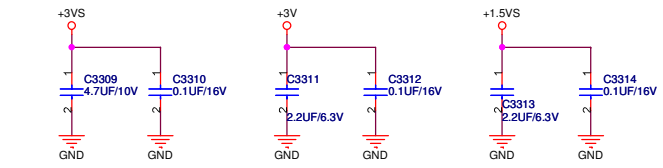
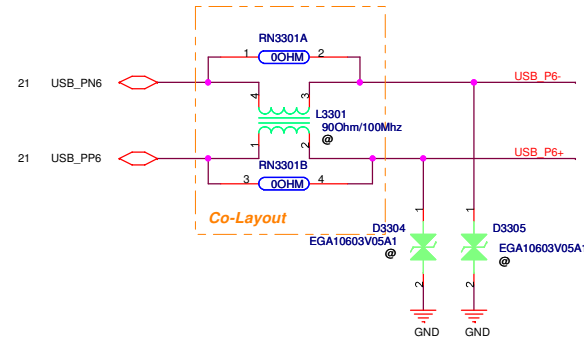
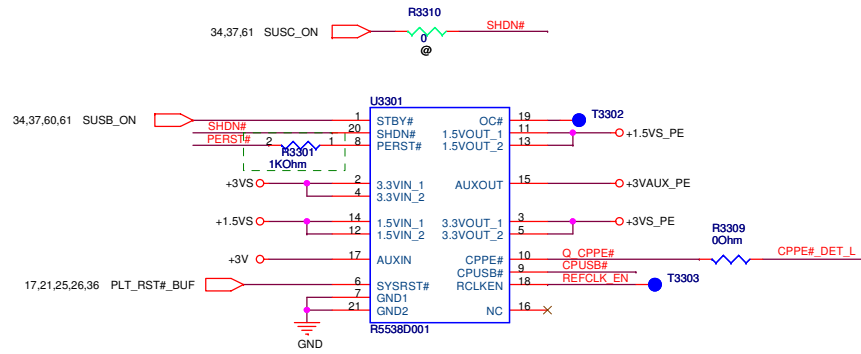
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<< Kennedy\_Zhang >>

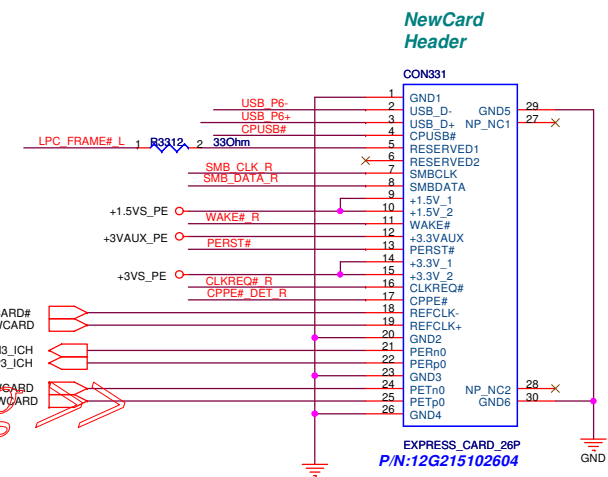
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		<b>Title :</b> EMPTY
ASUSTeK COMPUTER INC		<b>Engineer:</b> Chao-liang_Hung
Size Custom	Project Name <b>F9F</b>	Rev 2.00
Date: Wednesday, October 04, 2006		Sheet 32 of 63

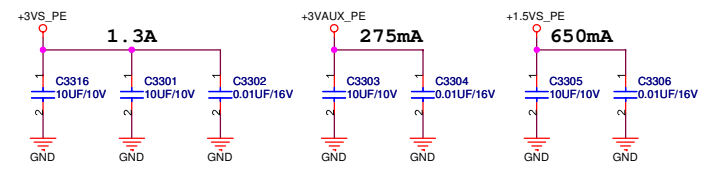
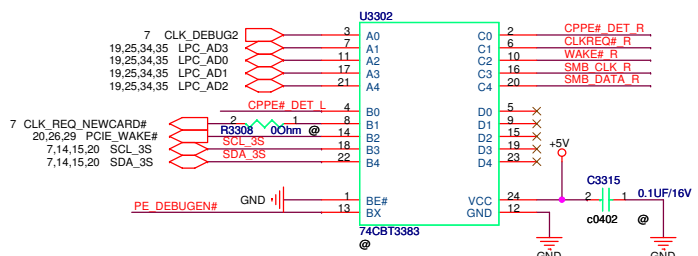


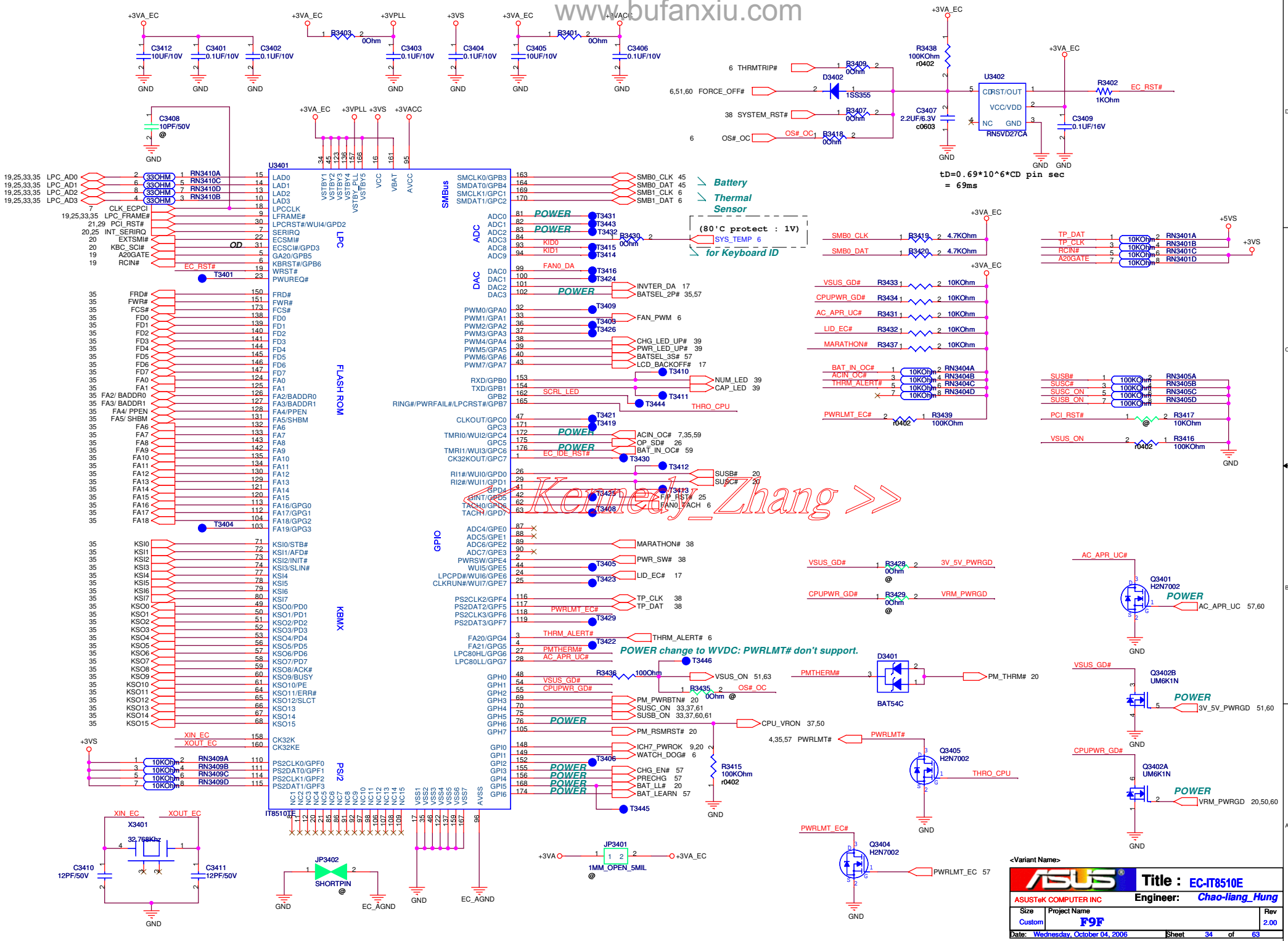


« Kennedy Zhang »



CPPE#_DET_L	R3316	1	0402	2	0Ohm	CPPE#_DET_R
CLK_REQ_NEWCARD#	RN3302A	1	00HM	2	CLKREQ#_R	
PCIE_WAKE#	RN3302B	3	00HM	4	WAKE#_R	
SCL_3S	RN3302C	5	00HM	6	SMB5_CLK_R	
SDA_3S	RN3302D	7	00HM	8	SMB_DATA_R	



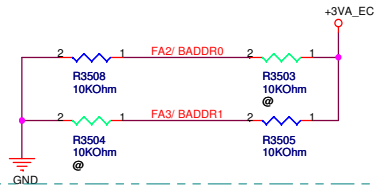


Kernel Zhang >>

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

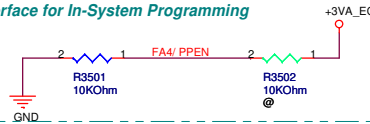
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

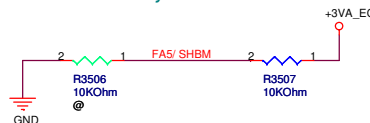
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

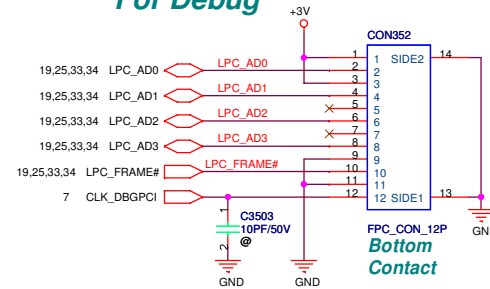


FA5/ SHBM

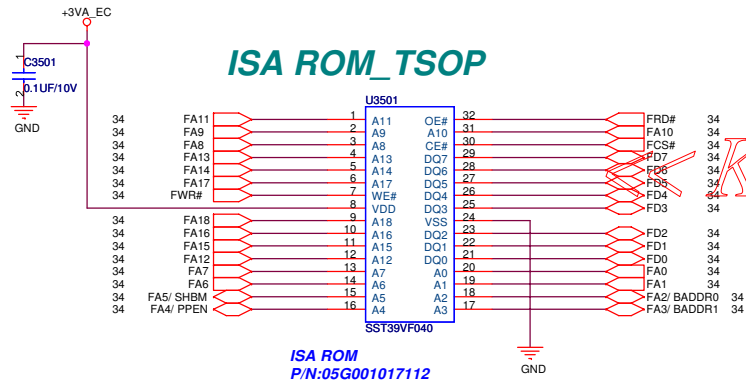
- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS



For Debug

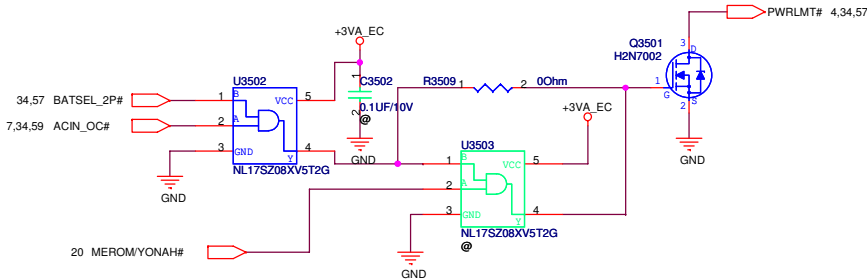
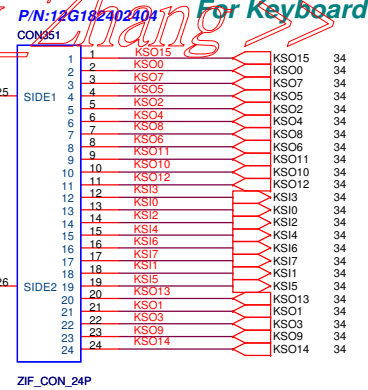


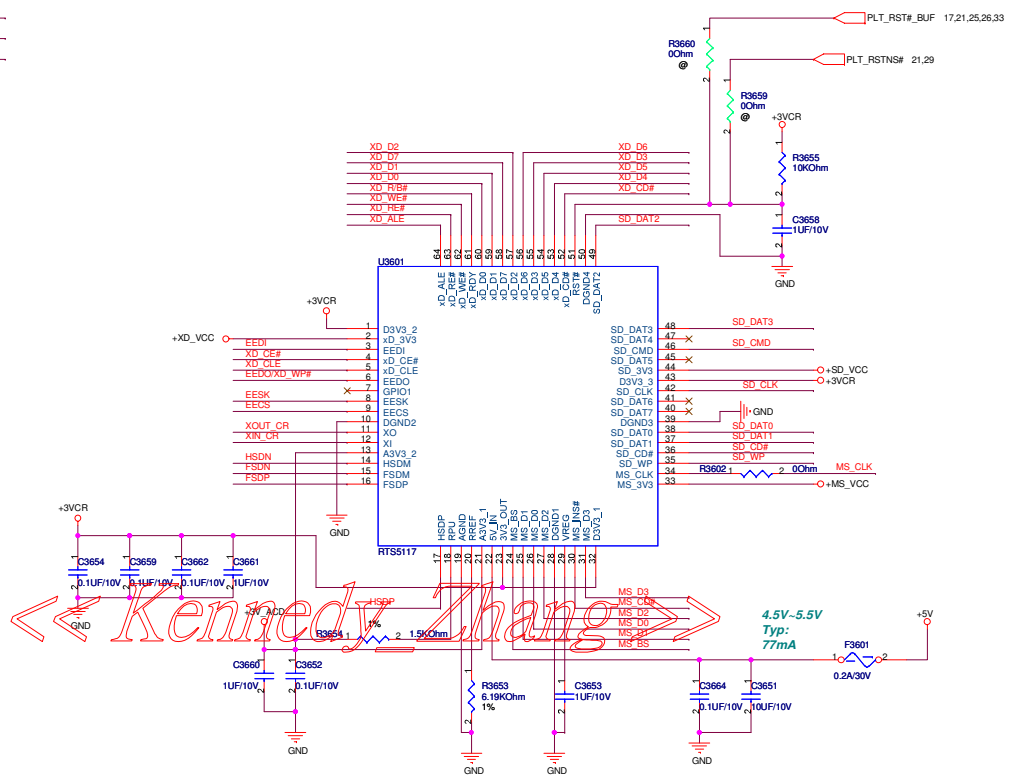
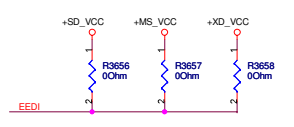
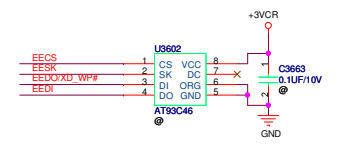
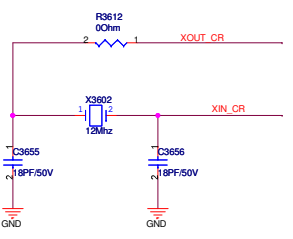
ISA ROM\_TSOP



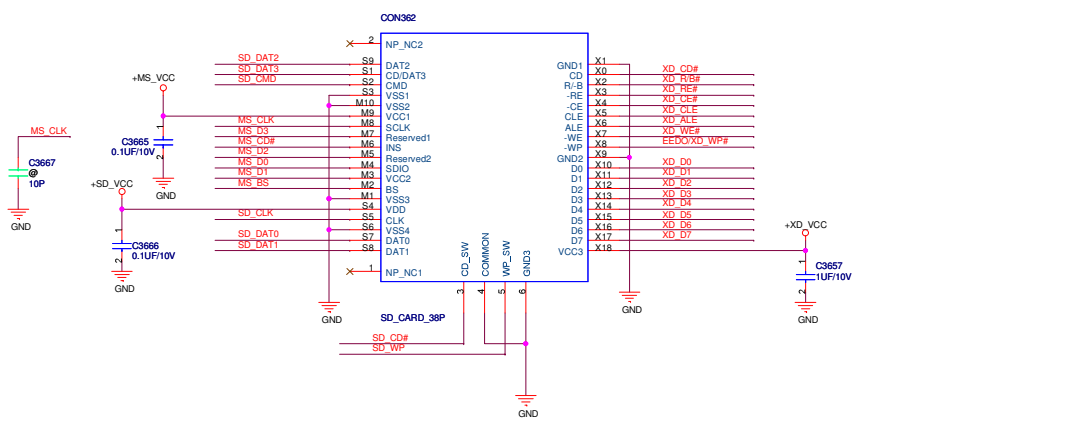
ISA ROM  
P/N:05G001017112

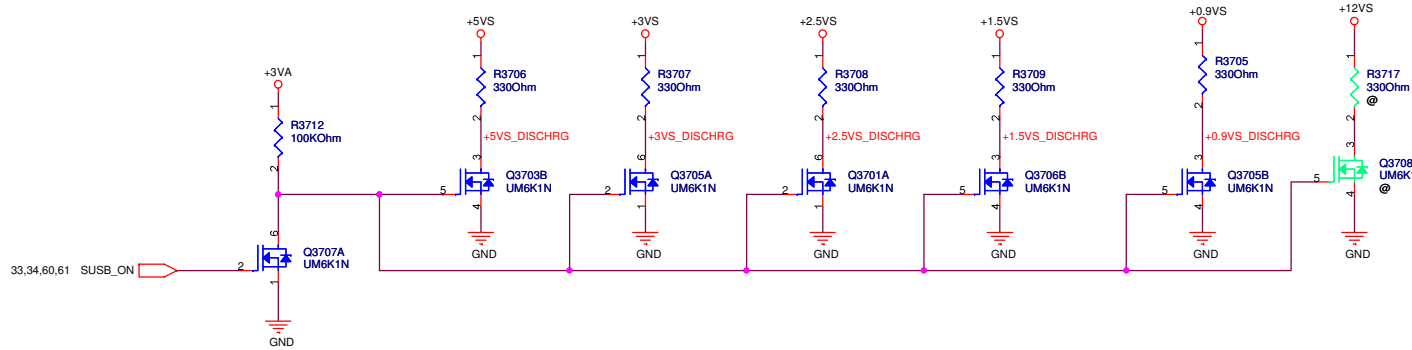
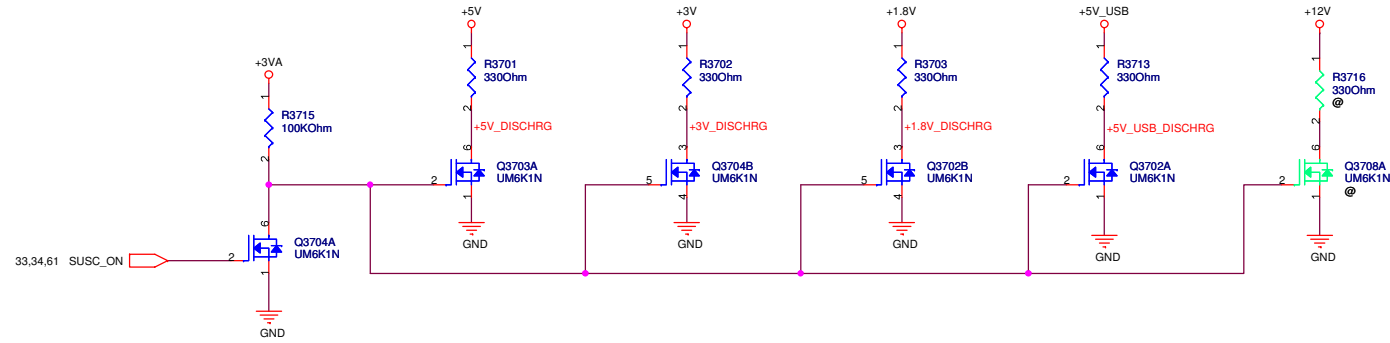
*Kennedy Zhang* For Keyboard



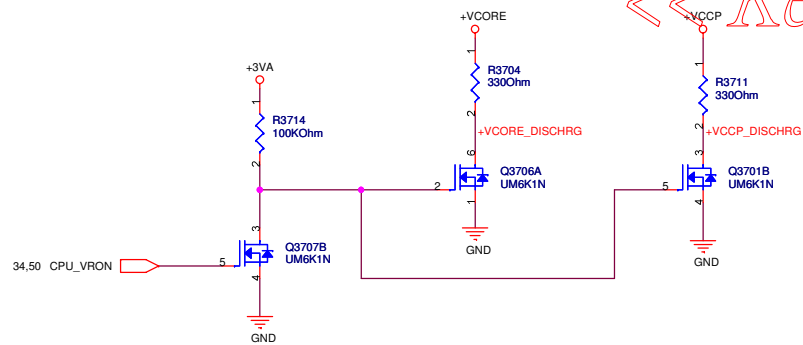


« Kennedy Zhang »



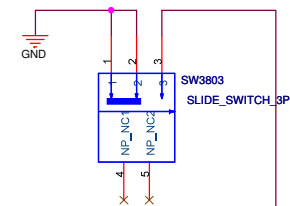
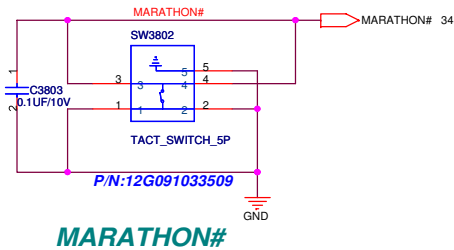
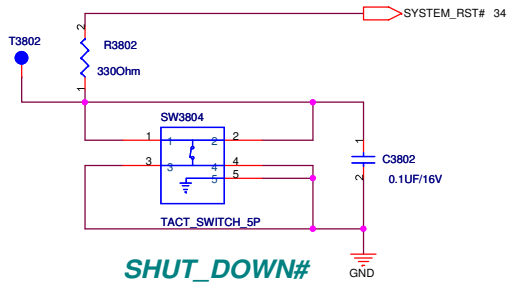
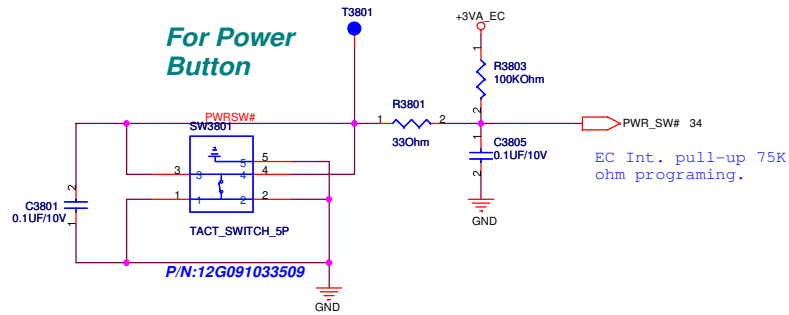


<< Kennedy\_Zhang >>



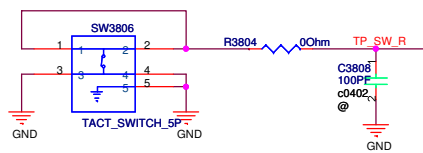
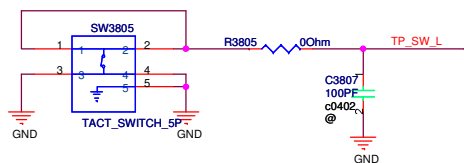
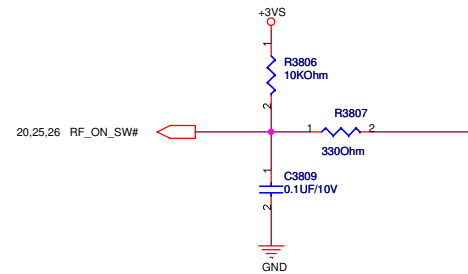
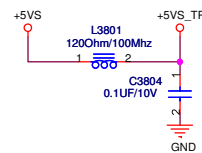
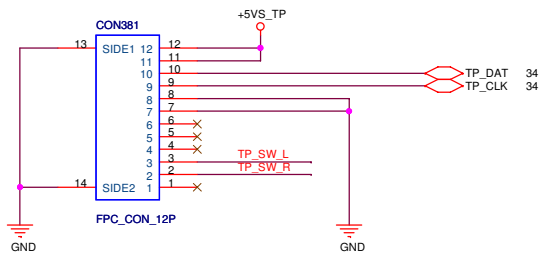
<Variant Name>

		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: Chao-liang Hung	
Size	Project Name		Rev
Custom	F9F		2.00
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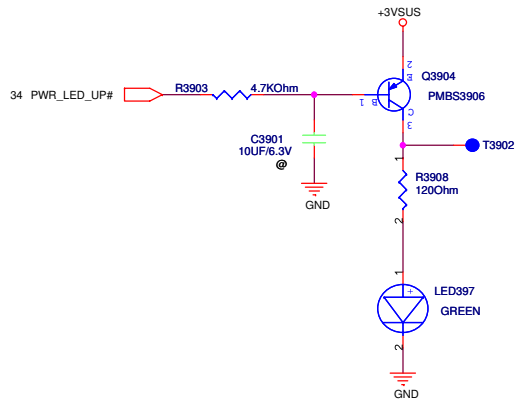
<< Kennedy\_Zhang >>

**For Touch-Pad**

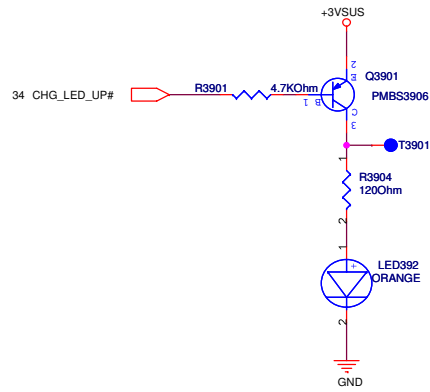


<Variant Name>

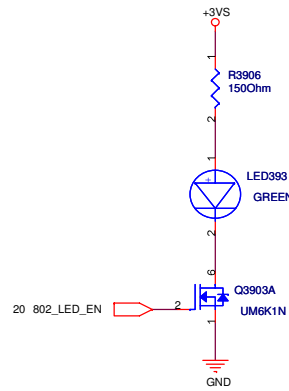
For PWR LED



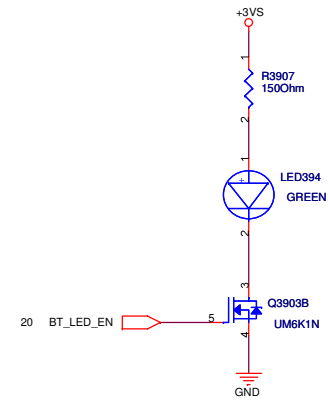
For BATTERY LED



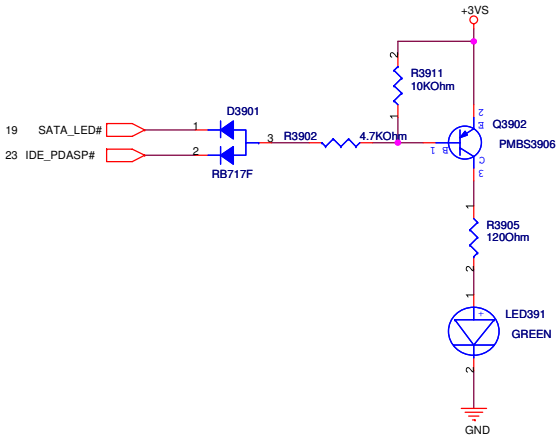
For WireLess LED



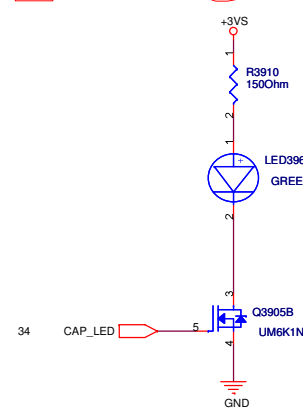
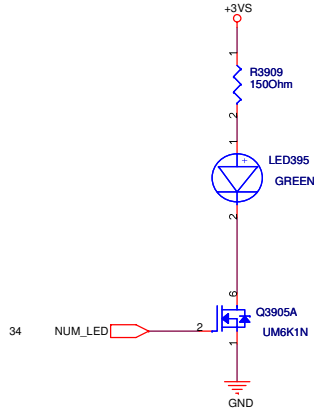
For BT LED



For SATA/IDE LED



<< Kennedy\_Zhang >>




<Variant Name>

<b>ASUS</b>		<b>Title : LEDs</b>	
ASUSTeK COMPUTER INC		Engineer: Chao-liang Hung	
Size	Project Name	Rev	
Custom	F9F	2.00	
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<Variant Name>


		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer: Chao-liang_Hung	
Size	Project Name	Rev	
Custom	F9F	2.00	
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<< Kennedy\_Zhang >>


<< Kennedy\_Zhang >>

<Variant Name>

		<b>Title :</b> EMPTY	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Chao-liang_Hung	
Size	Project Name	Rev	
Custom	F9F	2.00	
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<< Kennedy\_Zhang >>

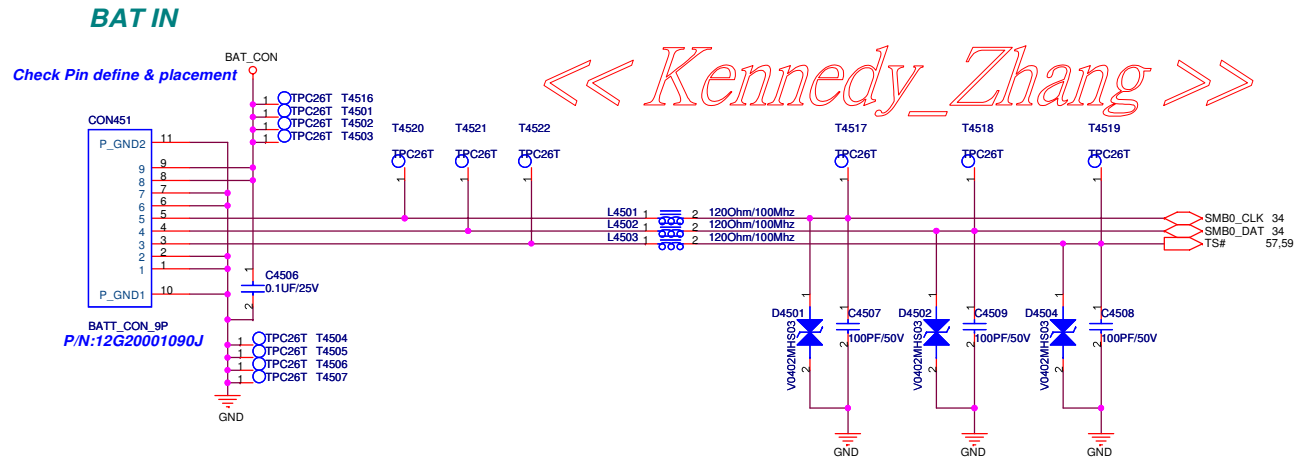
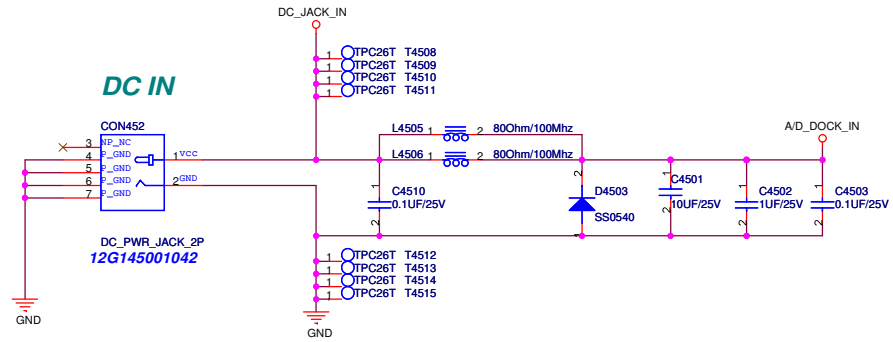
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ASUSTeK COMPUTER INC		Engineer: <i>Chao-liang_Hung</i>	
Size	Project Name	Rev	
Custom	<b>F9F</b>	2.00	
Date: Wednesday, October 04, 2006		Sheet	43 of 63

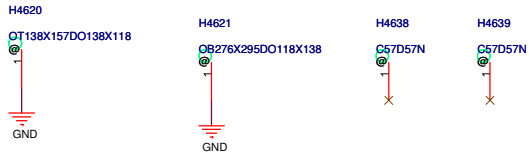
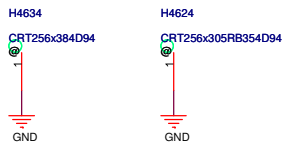
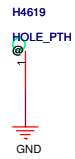
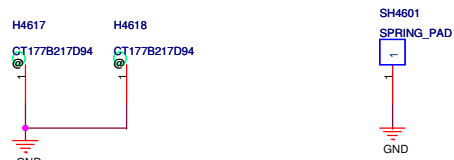
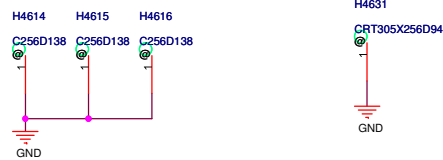
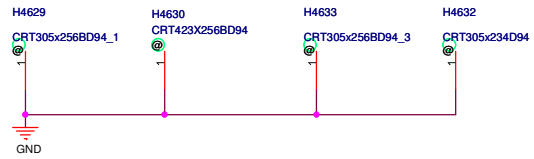
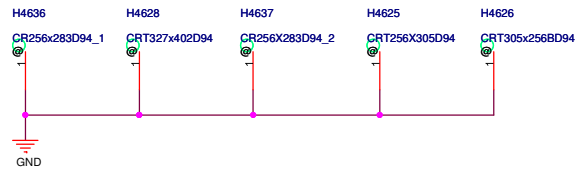
<< Kennedy\_Zhang >>

<Variant Name>

		<b>Title :</b> EMPTY	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Chao-liang_Hung	
Size	Project Name	Rev	
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<Variant Name>

<b>ASUS</b>		<b>Title : HDD &amp; CDROM</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Chao-liang Hung</i>	
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**Rev1.10**

1.Page 34: Change R3419 and R3420 from 1.5K to 4.7K ,in order to let the Battery SM Bus can be low enough.

2.Page 6:Change CON601 pin define for FAN.

3.Page26:Change CON261 pin define for I/O Board.

4.Page 34:Add R3438 100K and change C3407 to 2.2U for EC timing request.

5.page 6:Change R608 and R609 from 1.5K to 4.7K ,in order to the meet the EC request

5.page 17:Add F1701 for CCD power over current protection.

6.page 45:Change DC in Jack

7.page 17:Change Inverter and LCD LVDS connector for ME request.

8.page 39:Change LED392 to from green to orange.

9.page 34:Add R3439 and Q3403 for power limit.

10.page 9 & page 11 :Add TV out function.

11.page 33&34 Change PE\_DEBUGEN# pull high to +3V ,U3303 power pin to +3V and R3306 to 4.7K.

12.page25:Add power circuit for Finger Printer.

13.page25:Change power circuit for Finger Printer and add P/F\_RST#.

14.page12:DNI CE1201 for cost down.

15.page5:DNI CE501 for cost down.

16.page36:Change R3656,R3657,R3658 from 4.7K to 0 ohm ,and DNI U3602 and C3663 for new RTS5117

**Rev1.11**

17.page7:Swap U701 pin48,49 and pin51,52 pin name.

18.page39:Change LED393,LED394 from blue to green,for Marketing Spec.

**Rev1.20**

19.Page 35:Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

20.Page 34:DNI R3435 and mount R3408, R3418 for EC\_RST#

21.Page 7:Mount R747 for select PEREQ# and add R773 for CLK\_REQ\_NEWCARD# pull high.

22.Page 15:Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

23.Page 38:Change CON381 from 12G18340120E to 12G18340120K

24.Page 35:Modify circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

25.Page 46:Change screw holes beside H4614,H4615,H4616 for me request.

26.Page 18: Change L1811, L1812, and L1813 from bead to inductor.

27.Page 6:DNI D604 because OS\_OC# will shut down the system.

28.Page 17:Remove CCD connectorand add CCD signal to CON175.

**Rev1.21**

29.Page 17:Change R1703 from 100K to 200K to meet LCD power sequence.

30.Page 6:Modify the Hardware protect circuit.

31.Page 25:DNI Q2503 for BIOS can detect BT during BOOT.

32.Page 20:DNI R2017,R2018,R2019,because no need PCBA ID.

33.Page 23:Add R2309 and R2310 for IDE select.

34 Page 34:Del Q3403 UM6K1N and add 2N7002 for Q3404, Q3405.

35.Page 6: Change R610 from 100ohm to 200ohm for spec suggestion and reverse C609 1uF decoupling CAP.

36.Page 19: Change R1925,R1926,R1927 and R1928 from 0 ohm to 22 ohm.

37.Page 9: DNI C1831,C1833 and C1833.AND add C903,C904, C905 for 33P and R1103 for EMI request.

38.Page 17: Del D1704 ,add D1075 and change R1703 to 100 ohm to meet LCD power off sequence.

39.Page 7:Change C712 and C713 from 27P to 24P for ITTI request.

40.Page 19:Change C1901 and C1903 from 15P to 12P for ITTI request.

41.Page 36:Change C3655 and C3656 from 15P to 18P for ITTI request.

42.Page 6:Add R617 and Q605 for OS\_OC#,to keep the U3403 pin5 voltage can meet RNSVD27CA request.

43.Page 25:Add C2512 and mount D2503 for EMI request.

**Rev2.00**

44.Page 39:Change R3904,R3905 and R3908 to 120 ohm, change R3906,R3907,R3909and R2910 to 150 ohm to control LED current is about 10mA.

45.Page 34:Del R3408and add D3402 for the OS\_OC function

46.Page 20:Add R2038 10K for GPIO10 pull high and R2039 10K for GPIO25 pull high.

47.Page 46:Change H4626 and H4630.

48.Page 36:Del CON361 and add CON362 ALPS/SCDE1C0200

49.Page 25:Change R2510 from 2.2U to 10U to meet SI9183DT spec.

50.Page 21:Change USB external ports for controller0.


51.Page 25:Change C2502 from 0.1U to 10U for EMI request.

52.Page 46:ADD S4601 spring for EMI.

53.Page 18:Change TV out pi filter for EMI request.

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<Variant Name>

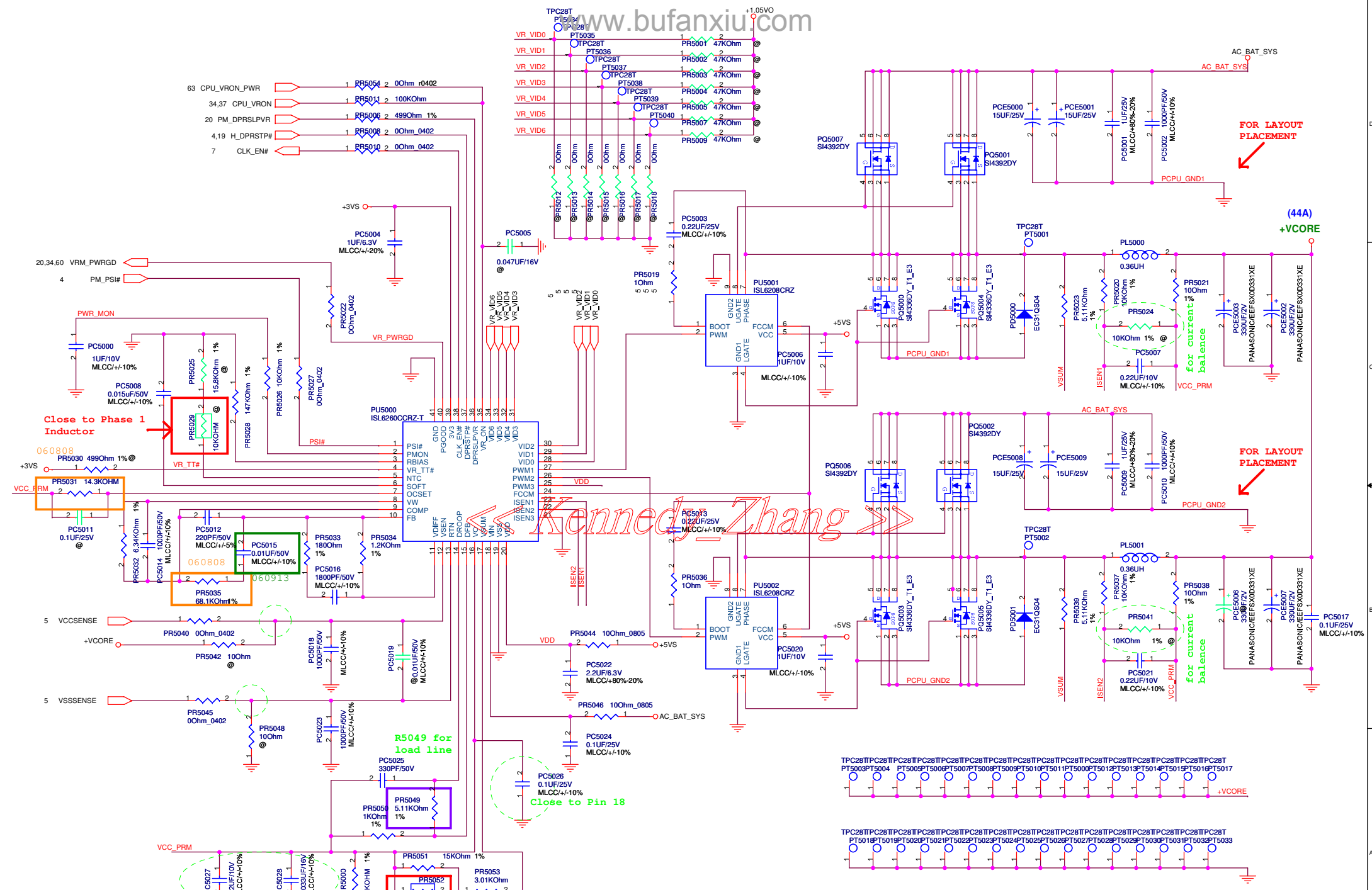
		<b>Title : History(1)</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Chao-liang Hung</i>	
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Custom	<b>F9F</b>	2.00	
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<Variant Name>

		<b>Title :</b> History(2)	
ASUSTeK COMPUTER INC		<b>Engineer:</b> Chao-liang_Hung	
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Custom	F9F	2.00	
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FOR LAYOUT PLACEMENT

FOR LAYOUT PLACEMENT

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C5028 & C5029 for transient response

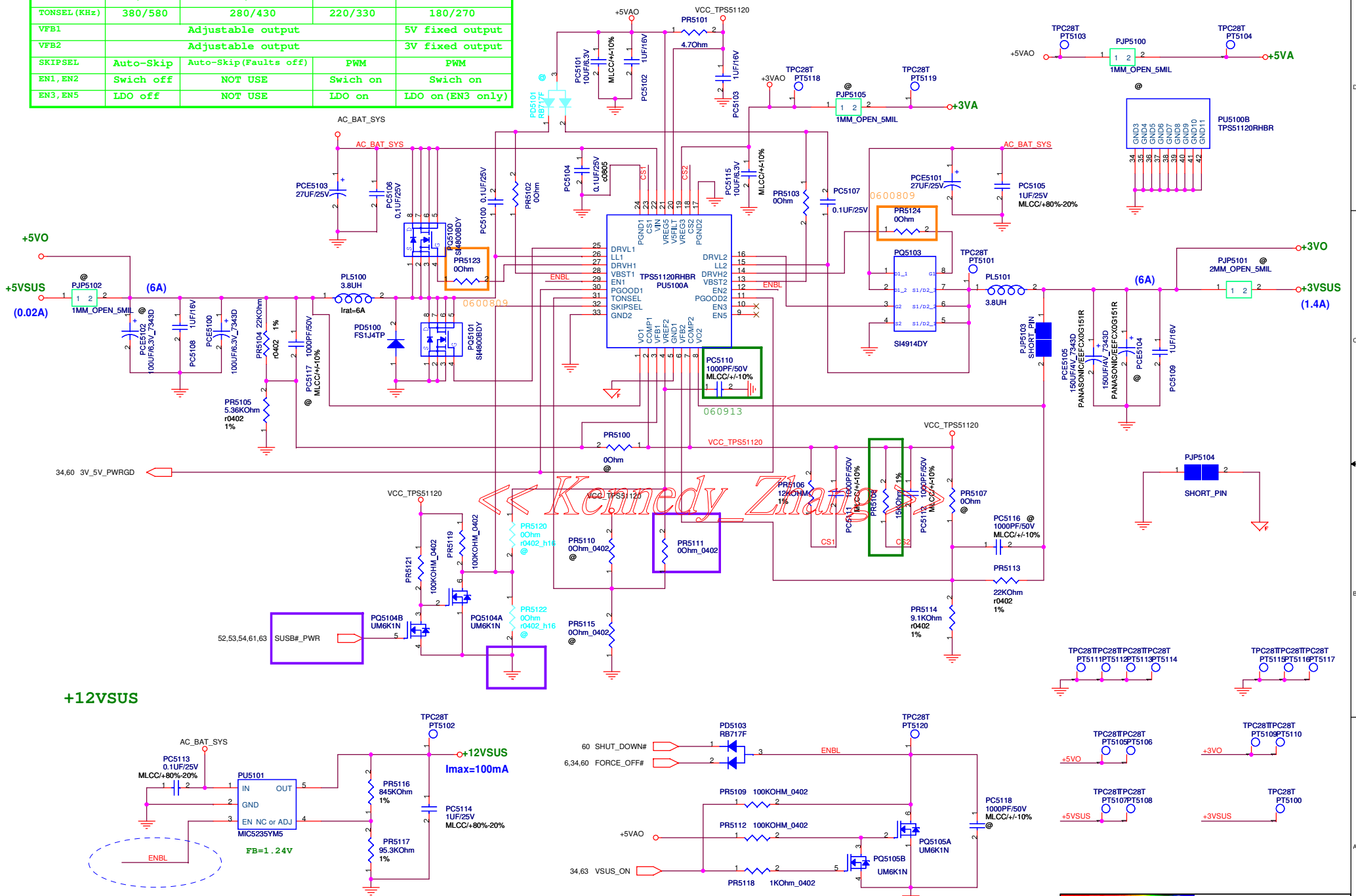
Close to Phase 1 Inductor

Close to Pin 18

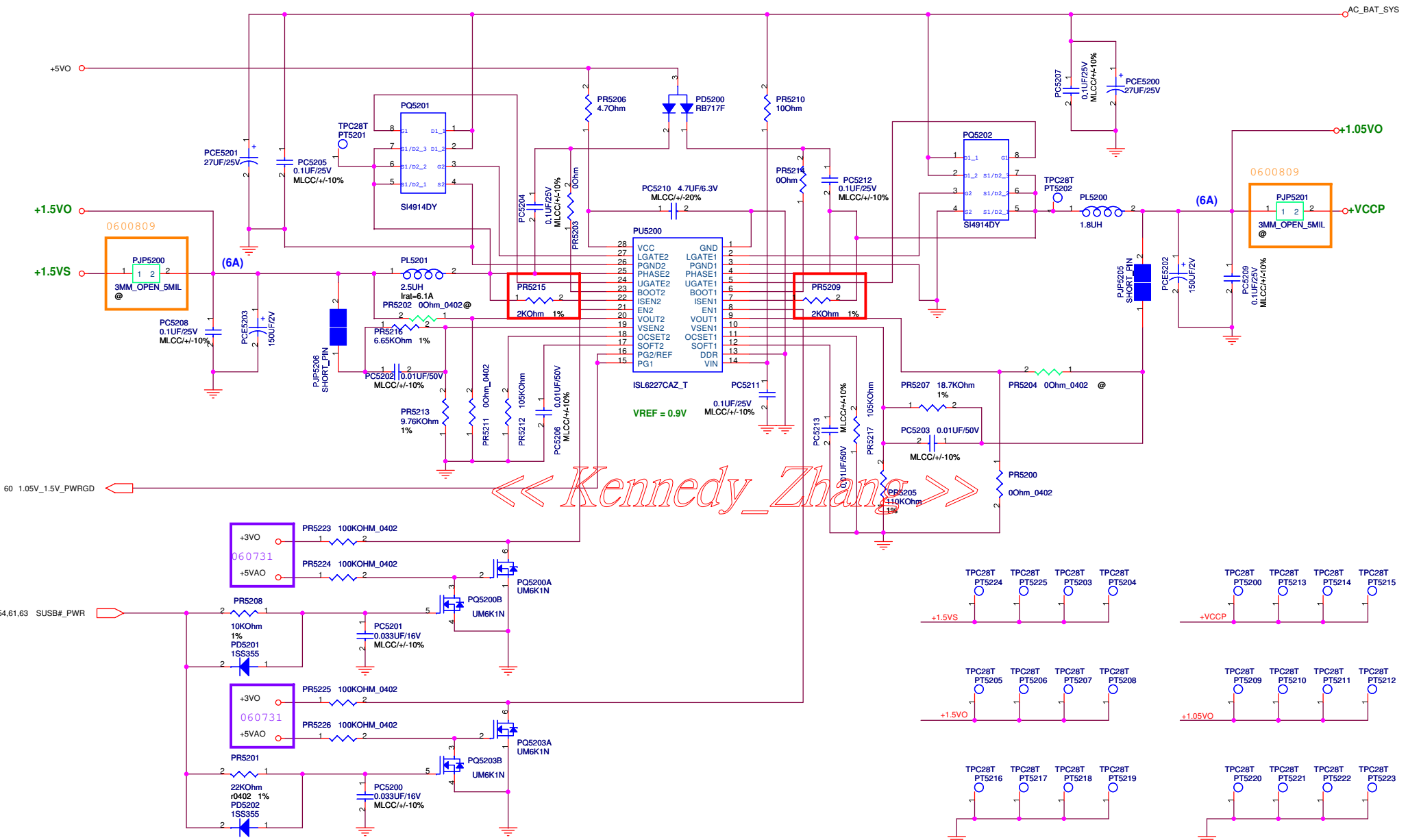
R5049 for load line

<b>ASUS</b>		<b>Title : POWER_VCORE</b>	
<OrigName>		Engineer:	
Size	Project Name	Rev	
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PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL (KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output		5V fixed output	
VFB2	Adjustable output		3V fixed output	
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1, EN2	Switch off	NOT USE	Switch on	Switch on
EN3, EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)



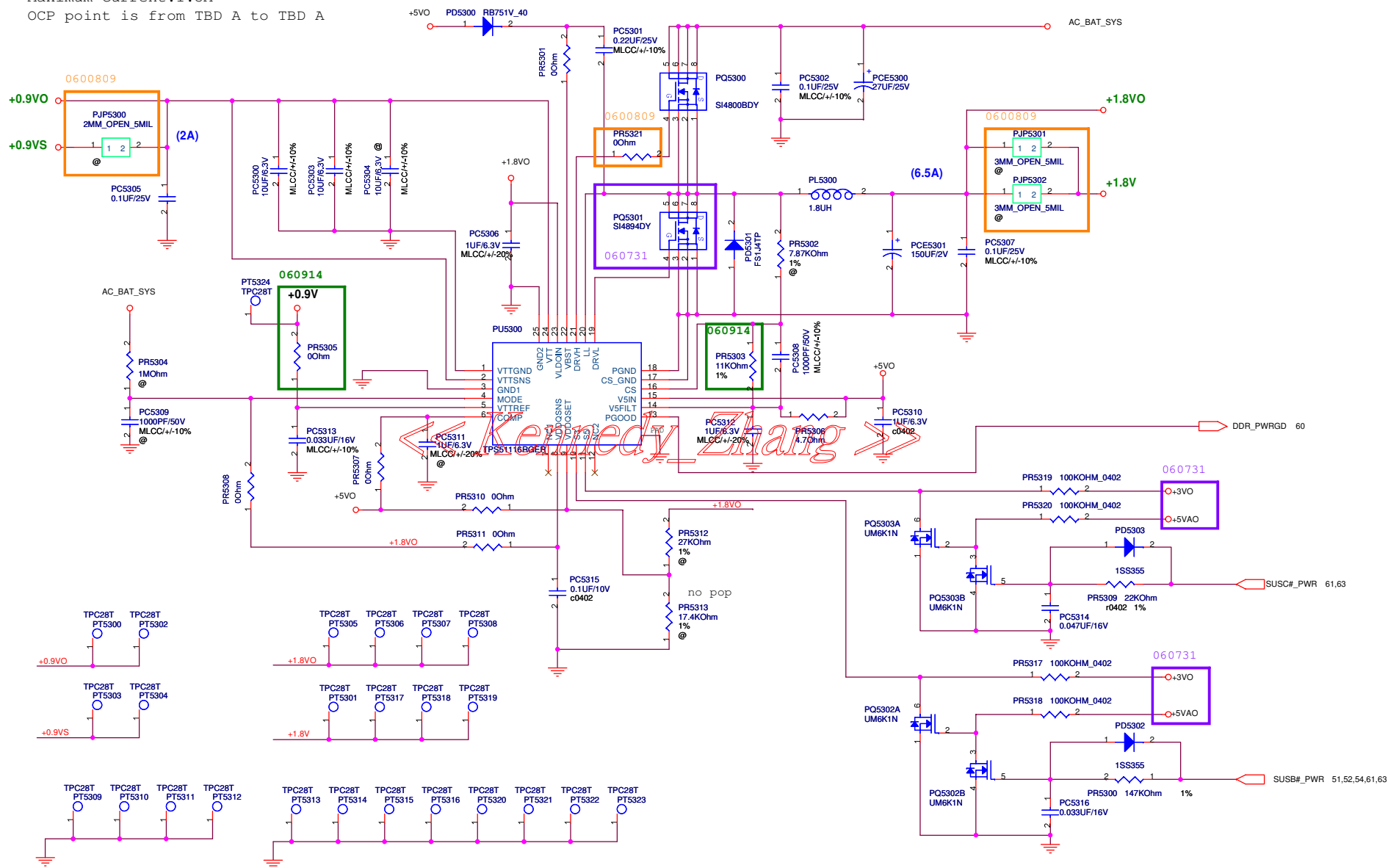
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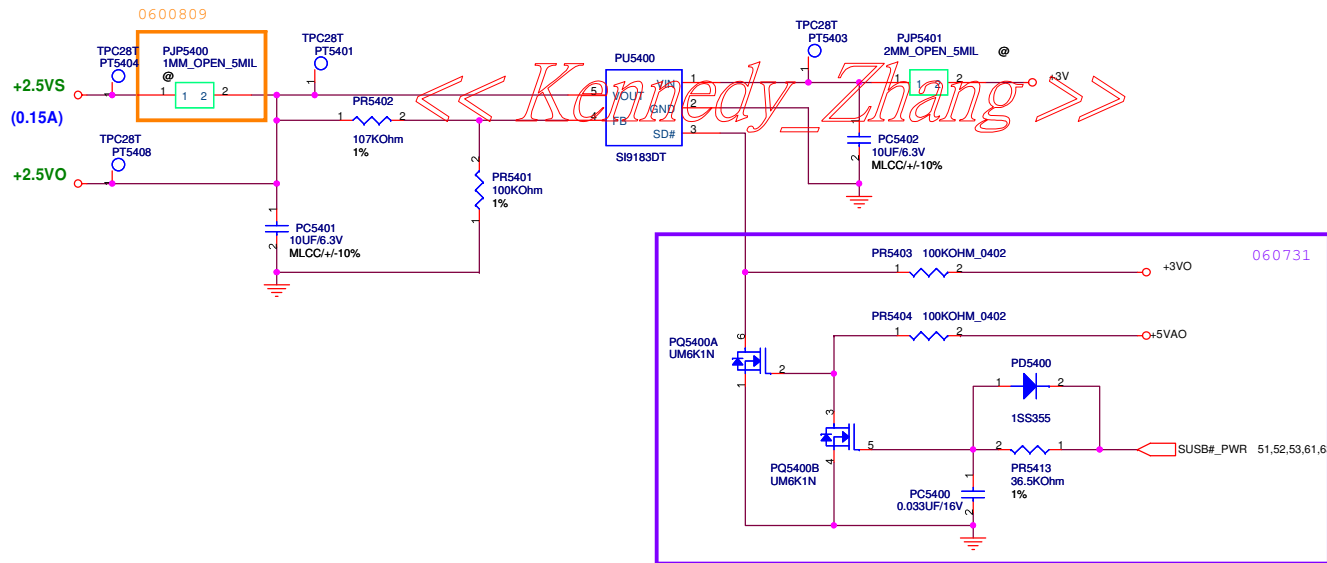
« Kennedy\_Zhang »

.9 Volt +/-5% .9 Volt +/-5%  
Design Current:1.05A  
Maximum current:1.5A  
OCP point is from TBD A to TBD A

1.8Volt +/-5%  
Design Current:7.3A  
Maximum current:10.5A  
OCP point is from TBD A to TBD A



+2.5VS



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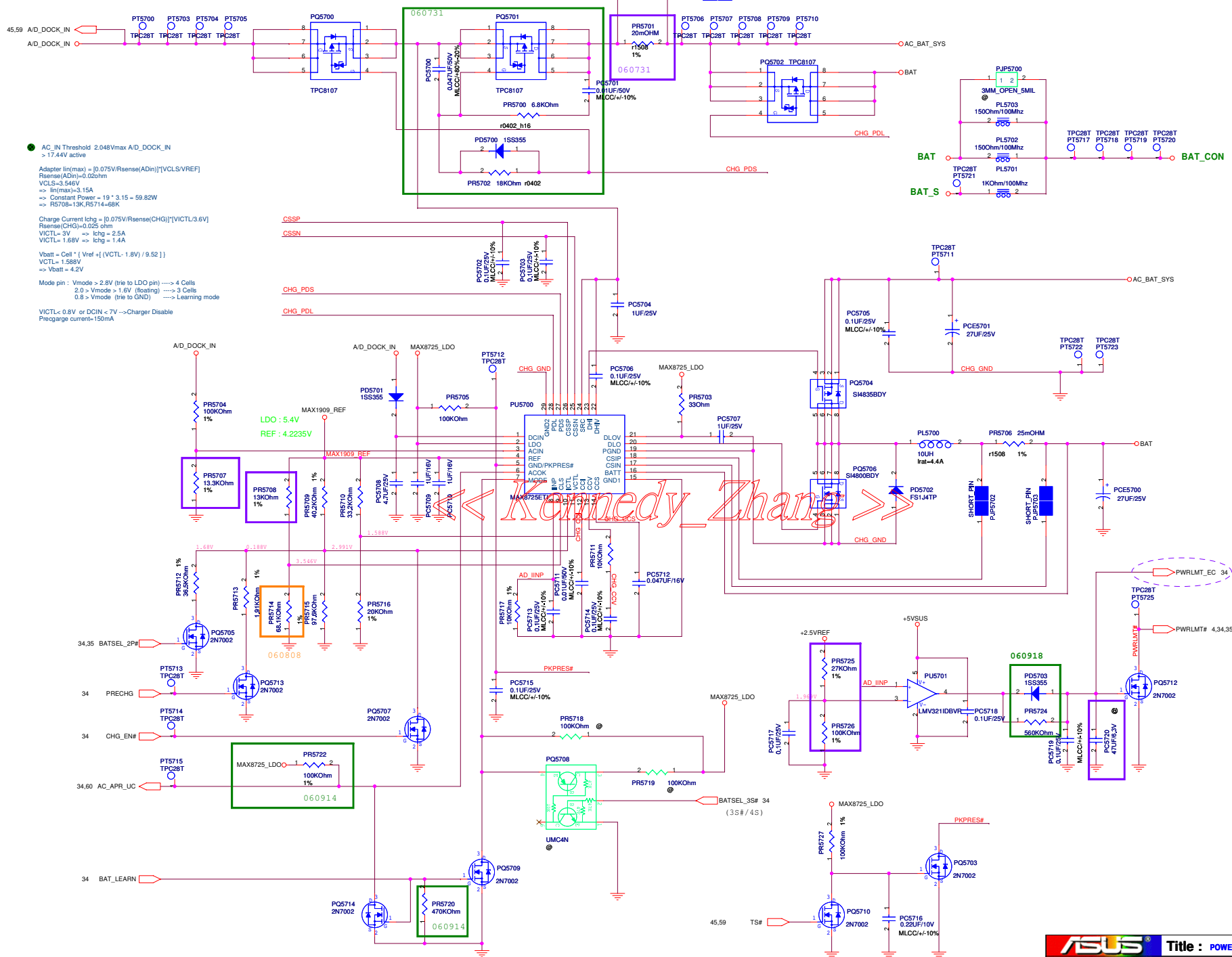
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<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	F9F	2.00	
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		Title : EMPTY	
<OrgName>		Engineer:	
Size	Project Name		Rev
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POWER PATH & BAT\_LEARN



● AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN > 17.44V active

Adapter lin(max) = (0.075V/Rsense(ADin))\*[VCLS/VREF]  
 Rsense(ADin)=0.02ohm  
 VCLS=3.546V  
 => lin(max)=3.15A  
 => Constant Power = 19 \* 3.15 = 59.82W  
 => R5708=13K,R5714=68K


Charge Current Ichg = (0.075V/Rsense(CHG))\*[VICTL/3.6V]  
 Rsense(CHG)=0.025 ohm  
 VICTL= 3V => Ichg = 2.5A  
 VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell \* [ Vref + [(VCTL- 1.8V) / 9.52] ]  
 VCTL= 1.588V  
 => Vbatt = 4.2V

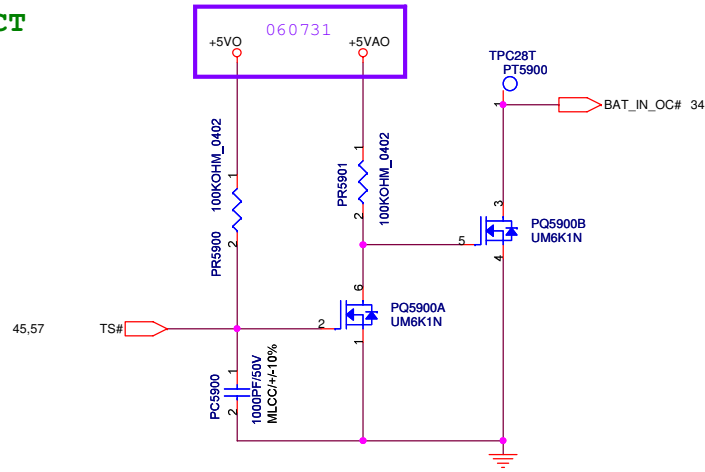
Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells  
 2.0 > Vmode > 1.6V (floating) ----> 3 Cells  
 0.8 > Vmode (tie to GND) ----> Learning mode

VICTL= 0.8V or DCIN < 7V -->Charger Disable  
 Precharge current=150mA

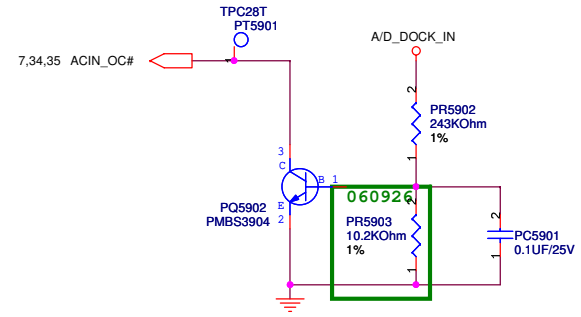
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		<b>Title : POWER_PIC</b>	
<OrgName>		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>F9F</b>	2.00	
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BATTERY IN DETECT

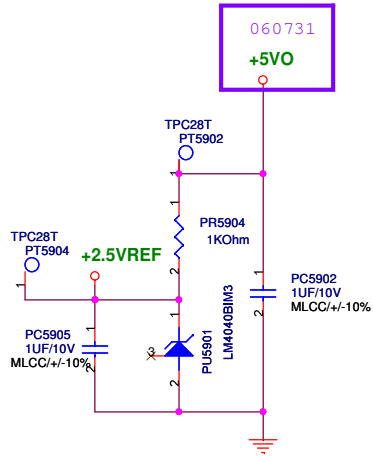


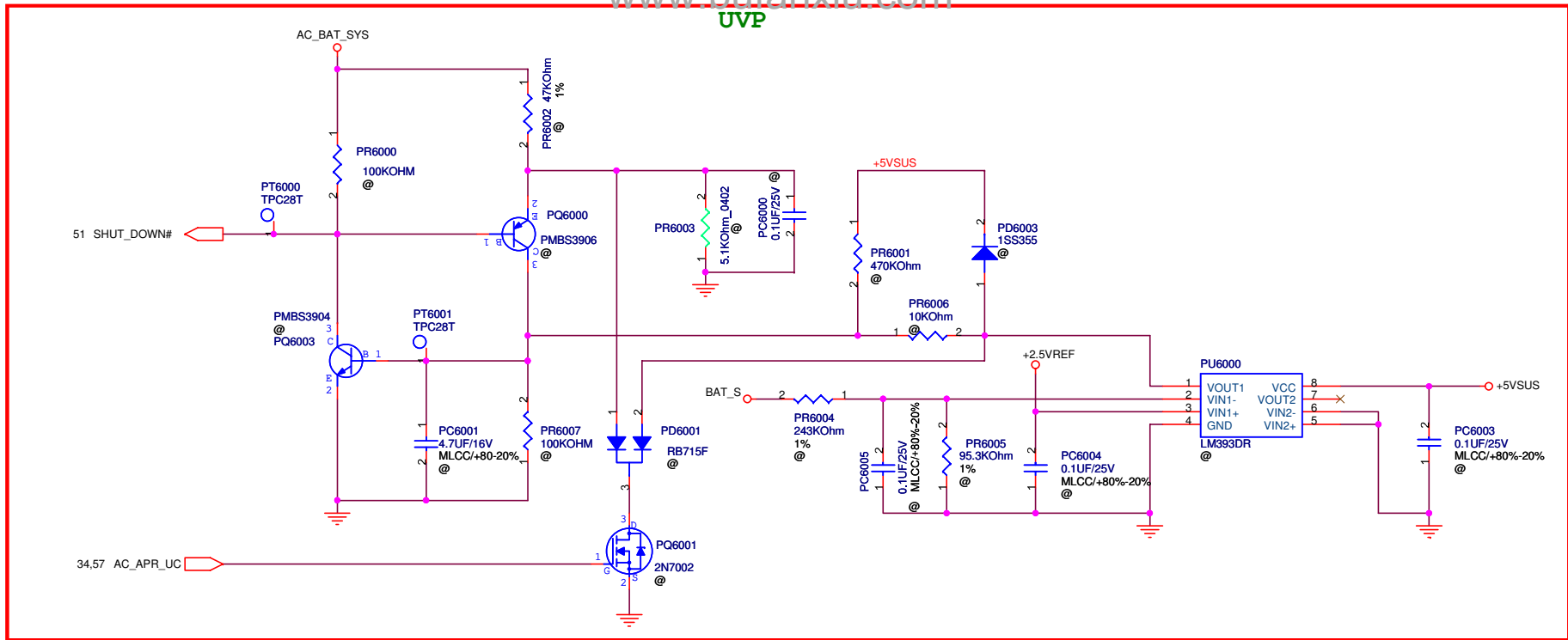
ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF

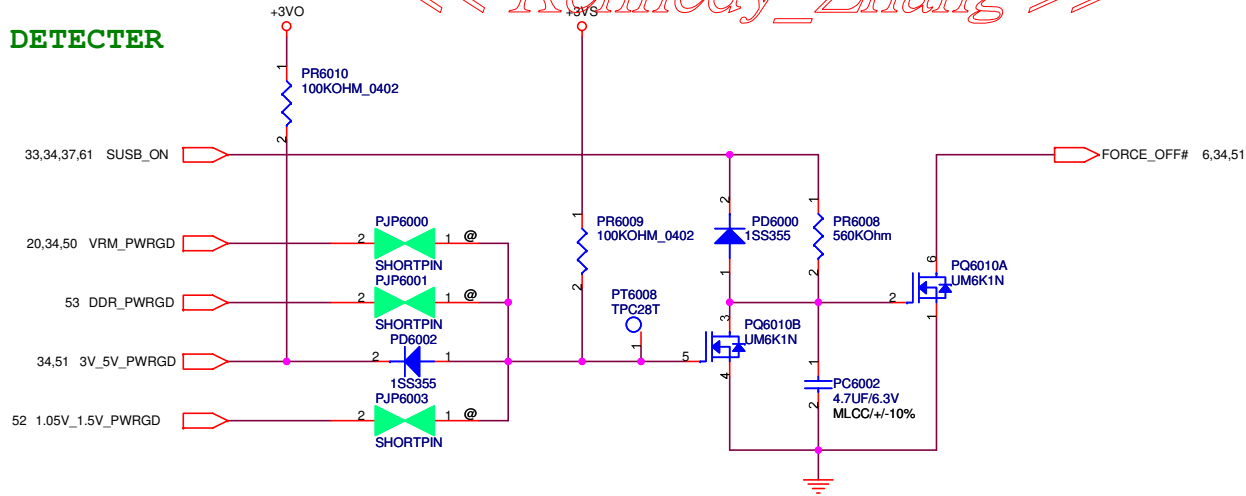
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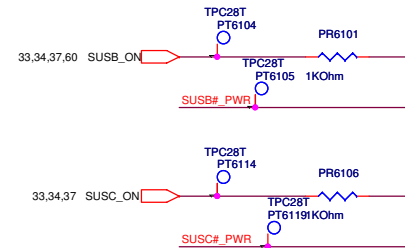
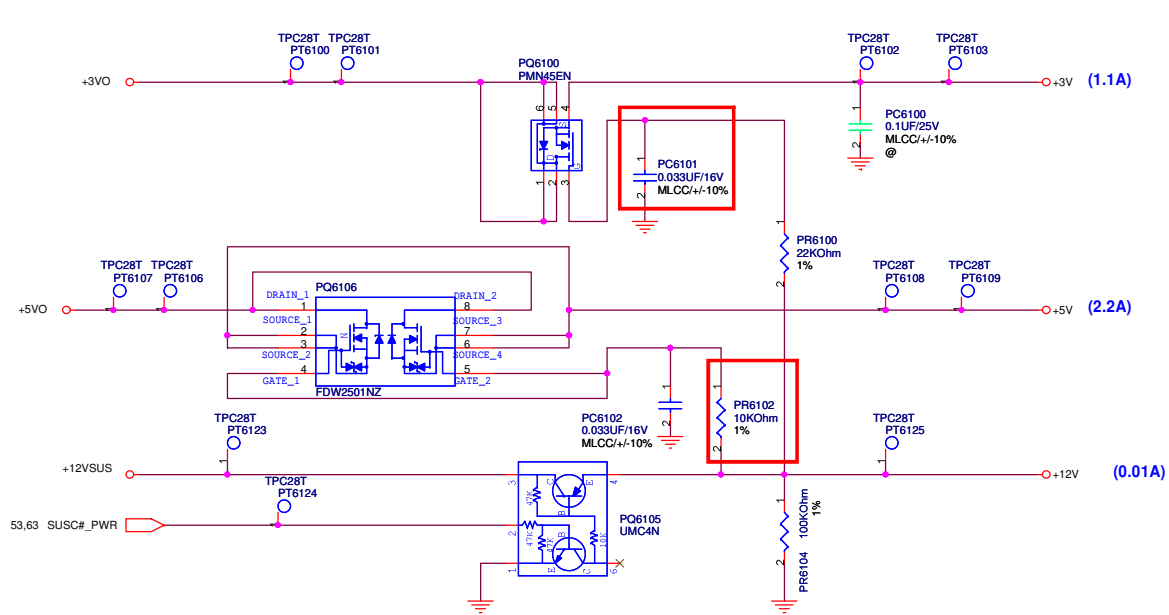
POWER GOOD DETECTOR



- TPC28T PT6003 1 VRM\_PWRGD
- TPC28T PT6004 1 DDR\_PWRGD
- TPC28T PT6005 1 3V\_5V\_PWRGD
- TPC28T PT6006 1 1.05V\_1.5V\_PWRGD

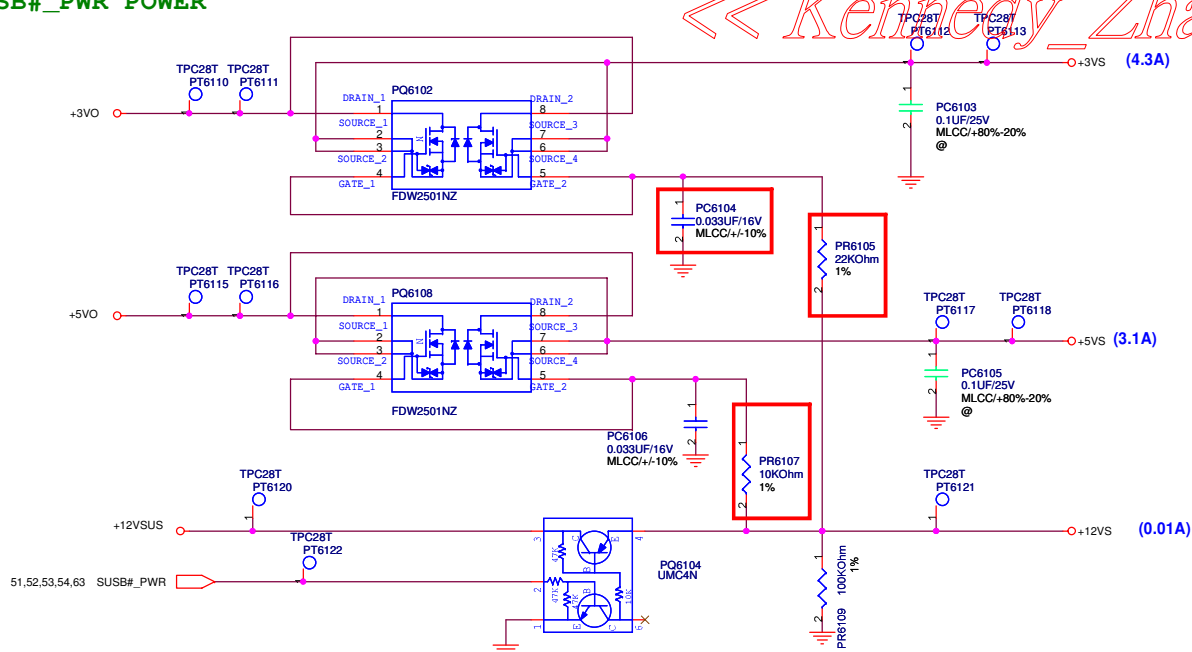
<b>ASUS</b>		<b>Title : POWER_PROTECT</b>	
<OrgName>		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>F9F</b>	2.00	
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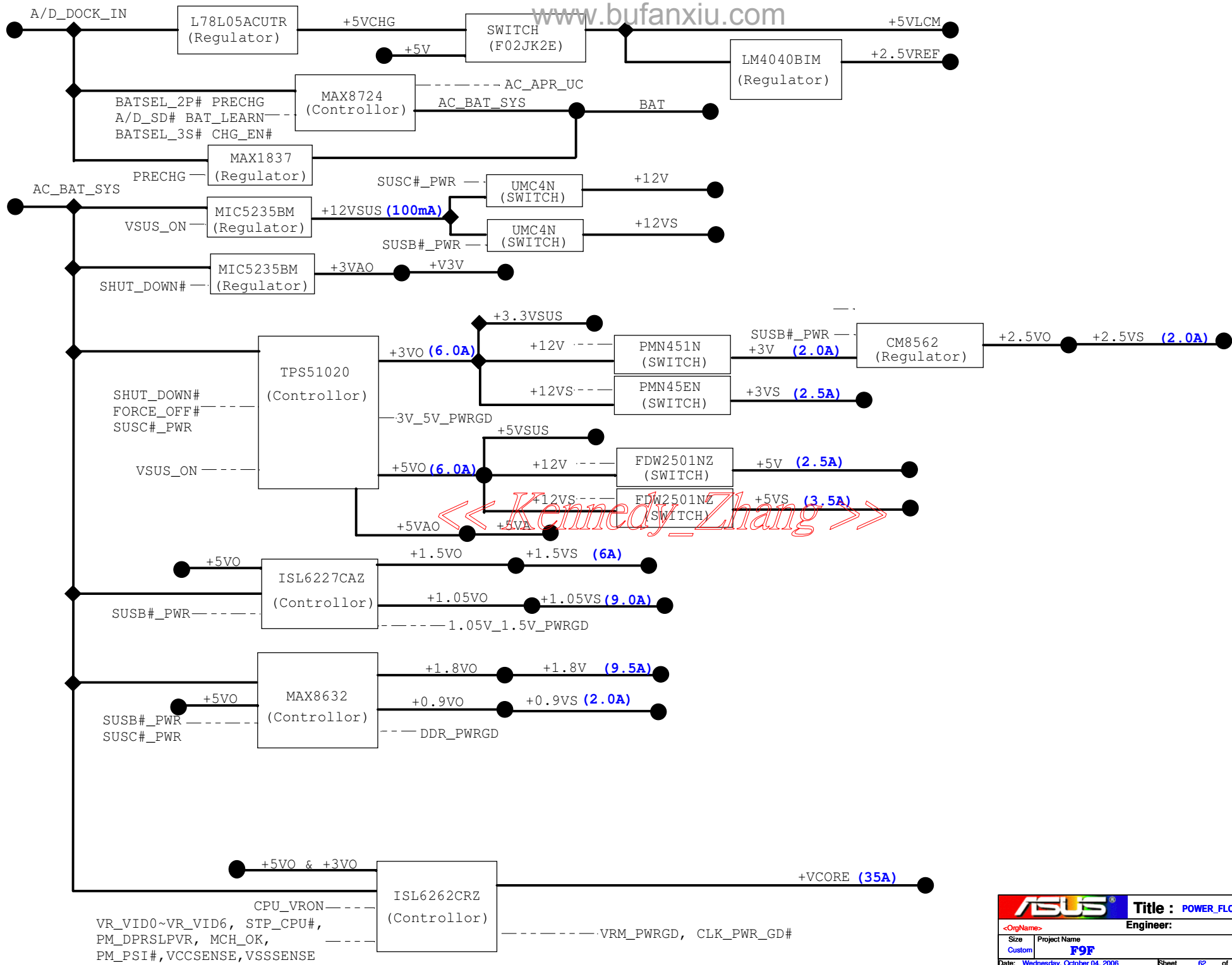
SUSC#\_PWR POWER



SUSB#\_PWR POWER

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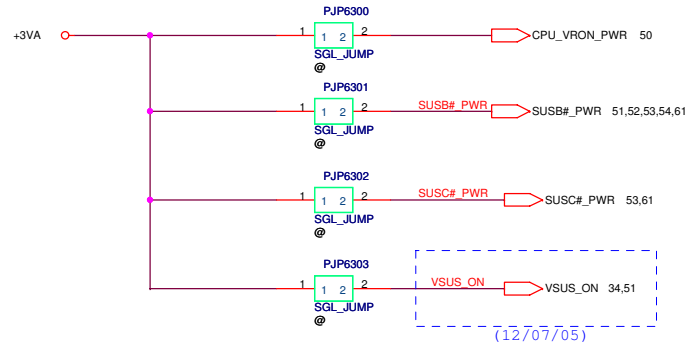




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FOR POWER TEST



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