F9F MB SCHEMATIC Revision 2.00

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5	YONAH CPU (2)
6	FAN CTRL&Thernal protection
7	CLK GEN-ICS954310
8	Calistoga--CPU
9	Calistoga--PCIE
10	Calistoga--DDR2
11	Calistoga--POWER
12	Calistoga--GND
13	Calistoga--Strap
14	DDR2 SO-DIMM_0
15	DDR2 SO-DIMM_1
16	DDR2 ADDRESS TERMINATION
17	LVDS & INVERTER CONN
18	CRT & TV OUT
19	ICH7M--CPU,IDE,AUDIO
20	ICH7M--GPIO
21	ICH7M--PCI,PCI-E,USB
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24	USB PORT
25	B/T,F/P& TPM
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27	EMPTY
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32	EMPTY
33	EMPTY
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36	CARD READER_RST5117
37	DISCHARGE
38	Instant Key & Touch Pad
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53	53_POWER_I/O_DDR & VTT
54	54_POWER_I/O_VTT & +2.5VS
55	55_POWER_VGA_CORE(Empty)
56	56_POWER_VGA_RAM(Empty)
57	57_POWER_CHARGER
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59	59_POWER_DETECT
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61	61_POWER_LOAD SWITCH
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63	63_POWER_SIGNAL

<Variant Name>

ASUSTeK COMPUTER INC

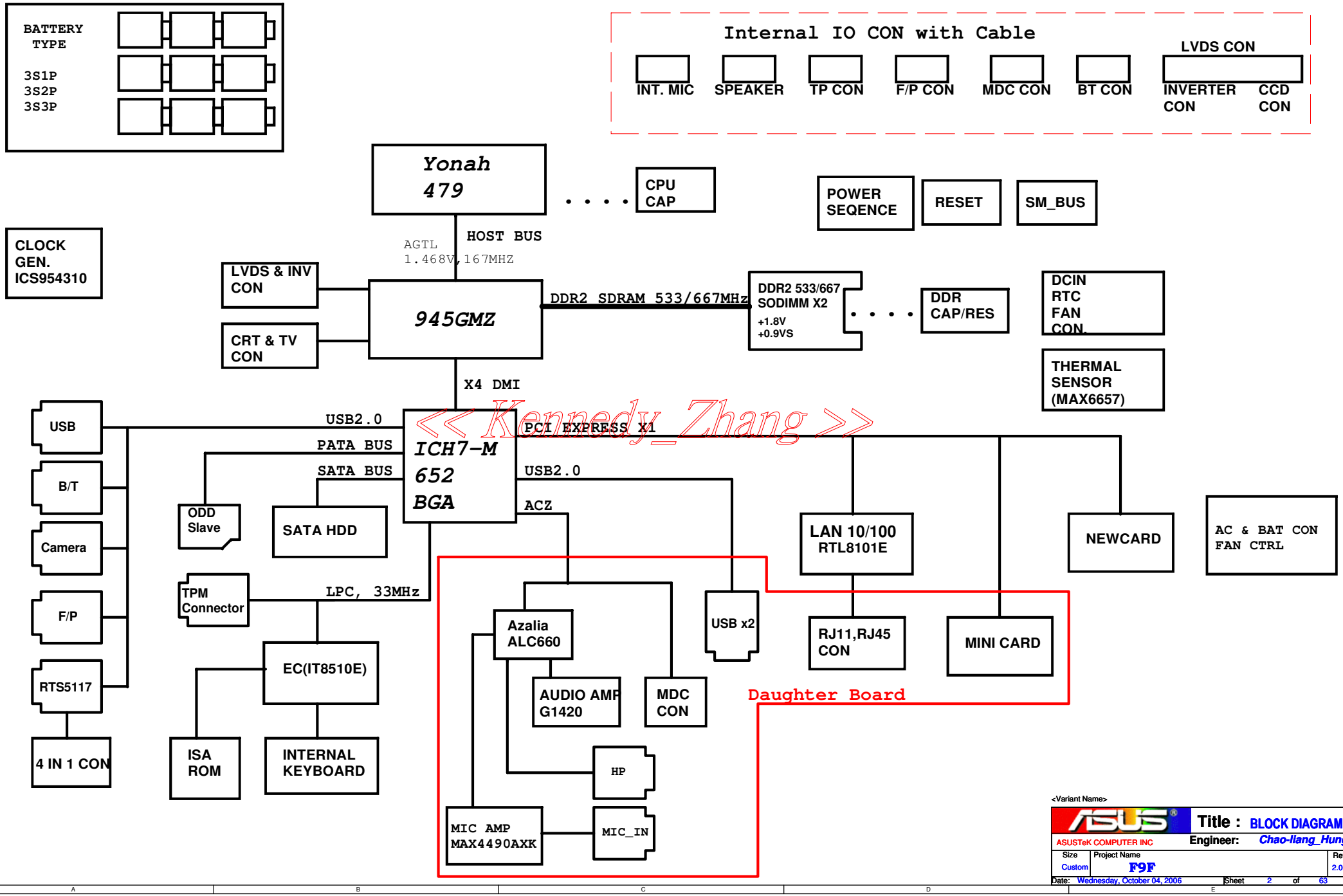
Title : PAGE REF.

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 1 of 63

F9F BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 2 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	N/A	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	N/A	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	N/A	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	BT_SW#	I
89	ADC6/GPE2	N/A	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	BAT_AD	I
82	ADC1	ADP_ERR#	I
83	ADC2	AC_AD	I
84	ADC3	N/A	
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

PCI Device	IDSEL#	REQ/GNT#	Interrupts

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

ICH7M_GPIO

Pin			Use As	Signal Name	Power
GPIO 00	i		GPI	PM_BMBUSY#	+3VS
GPIO 01	i		GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i		GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i		GPO	BT_LED_EN	+3VS
GPIO 07	i		GPI	RF_ON_SW#	+3VS
GPIO 08	i		GPI	EXTSMI#	+3VSUS
GPIO 09	i		GPI	N/A	+3VSUS
GPIO 10	i		GPI	N/A	+3VSUS
GPIO 11	i		Native	SMB_ALERT#	+3VSUS
GPIO 12	i		GPI	KBC_SCI#	+3VSUS
GPIO 13	i		GPI	N/A	+3VSUS
GPIO 14	i		GPI	N/A	+3VSUS
GPIO 15	i		GPO	802_LED_EN	+3VSUS
GPIO 16	O	0	GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1	GPO	PCI_GNT#5	+3VS
GPIO 18	O	1	GPO	STP_PCI#	+3VS
GPIO 19	i	1	GPI	N/A	+3VS
GPIO 20	O	1	GPO	STP_CPU#	+3VS
GPIO 21	i	1	GPO	N/A	+3VS
GPIO 22	i	1	Native	PCI_REQ#4	+3VS
GPIO 23	i	1	Native	N/A	+3VS
GPIO 24	O	0	GPO	MSK_PCIRST	+3VSUS
GPIO 25	O	1	GPO	N/A	+3VSUS
GPIO 26	O	0	GPO	BT_ON#	+3VSUS
GPIO 27	O	0	GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0	GPO	N/A	+3VSUS
GPIO 29	i	0	Native	USB_OC#5	+3VSUS
GPIO 30	i	0	Native	USB_OC#6	+3VSUS
GPIO 31	i	0	Native	USB_OC#7	+3VSUS
GPIO 32	O	1	GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1	GPO	N/A	+3VS
GPIO 34	O	0	GPO	N/A	+3VS
GPIO 35	O	0	GPO	N/A	+3VS
GPIO 36	i	0	GPO	N/A	+3VS
GPIO 37	i	0	GPI	PCB_ID0	+3VS
GPIO 38	i	0	GPI	PCB_ID1	+3VS
GPIO 39	i	0	GPI	PCB_ID2	+3VS
GPIO [40:47]			NA	NA	NA
GPIO 48			Native	PCI_GNT#4	+3VS
GPIO 49			Native	H_PWRGD	+VCORE

<Variant Name>

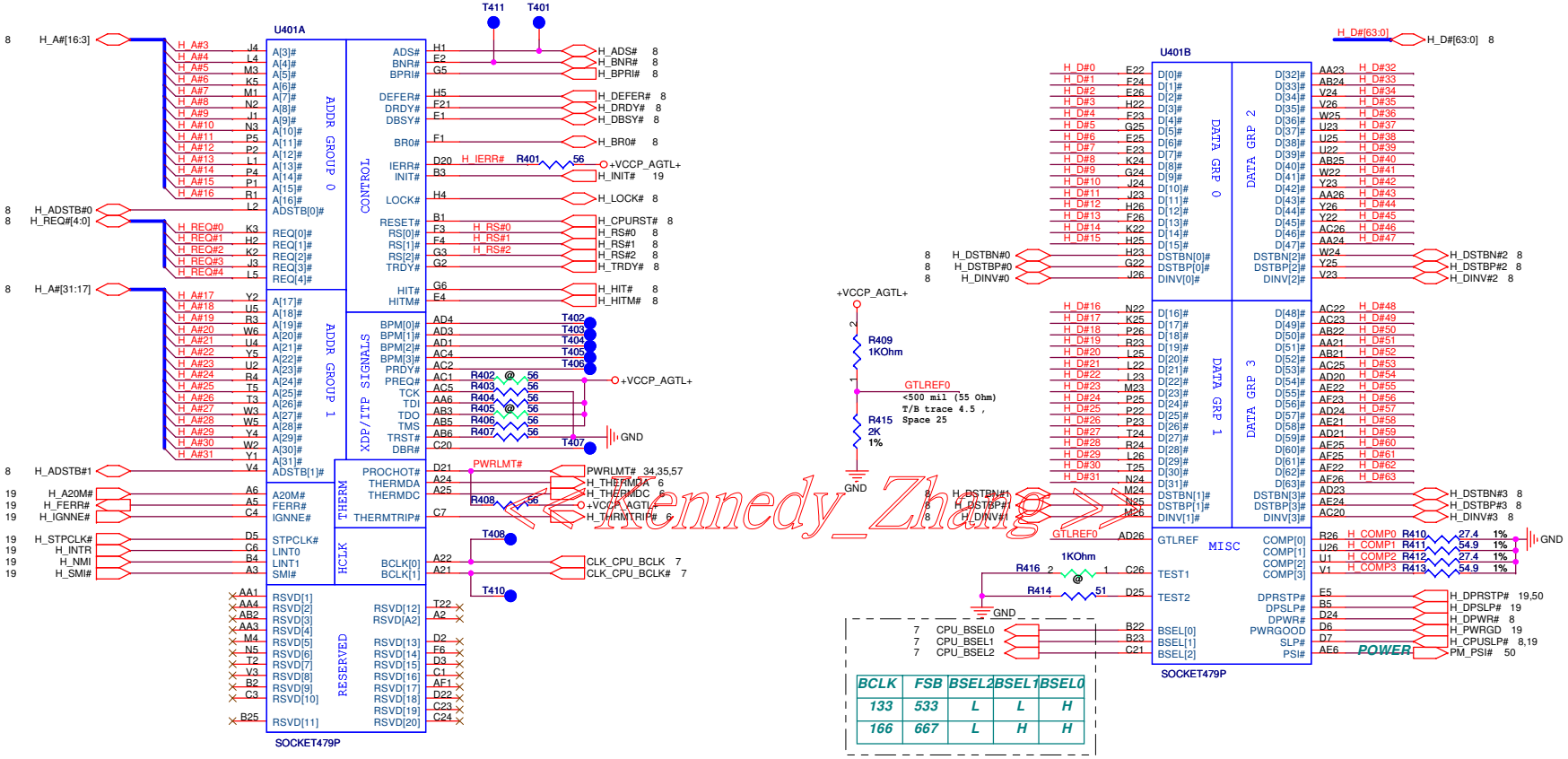
ASUSTeK COMPUTER INC

Title : Schematic data

Engineer: Chao-liang_Hung

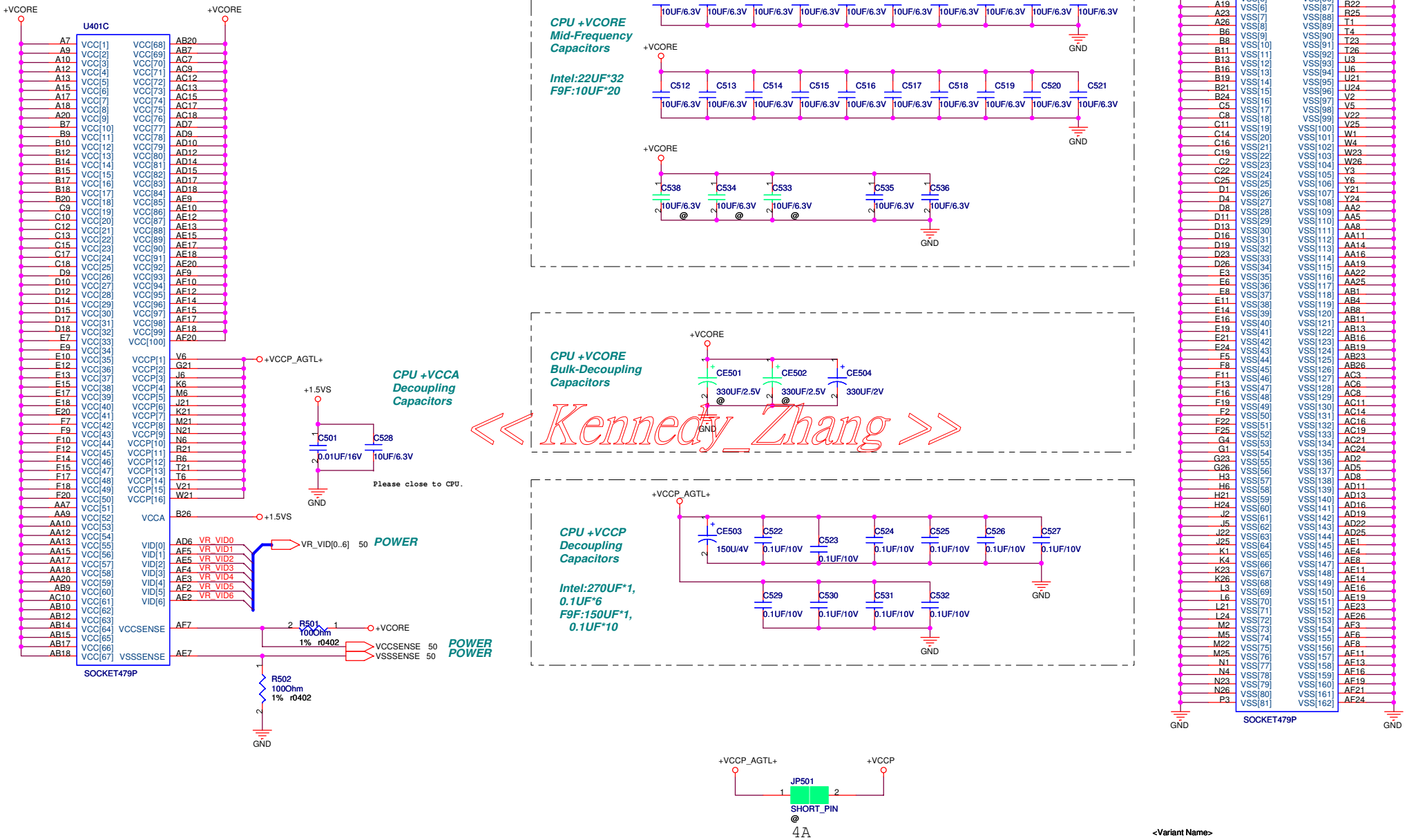
Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 3 of 63



<Variant Name>

ASUSTeK COMPUTER INC	Title : YONAH CPU (1)		
	Engineer: Chao-liang_Hung		
Size: Custom	Project Name: F9F		Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 4 of 63		

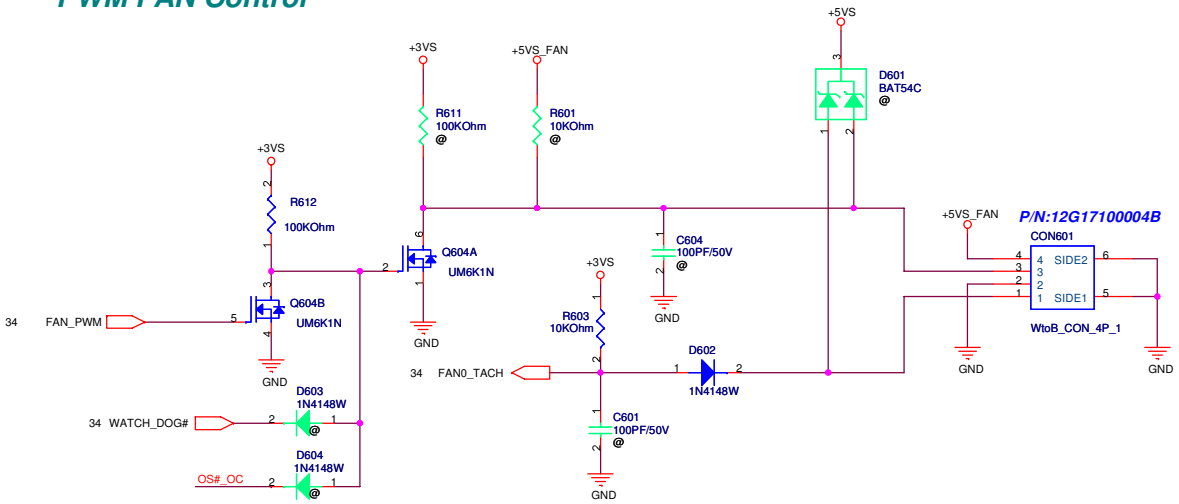


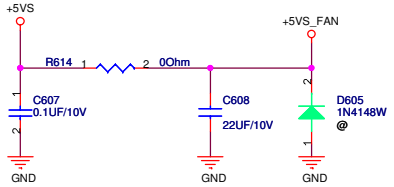
4A

<Variant Name>

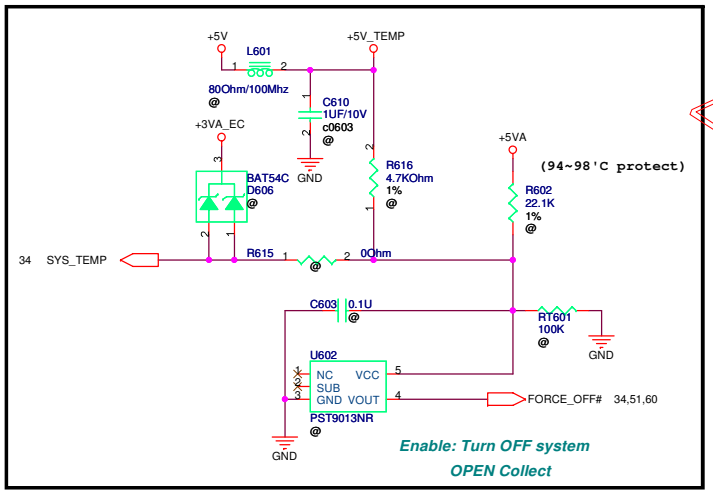
ASUSTeK COMPUTER INC	Title : YONAH CPU (2)	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 5 of 63	

PWM FAN Control

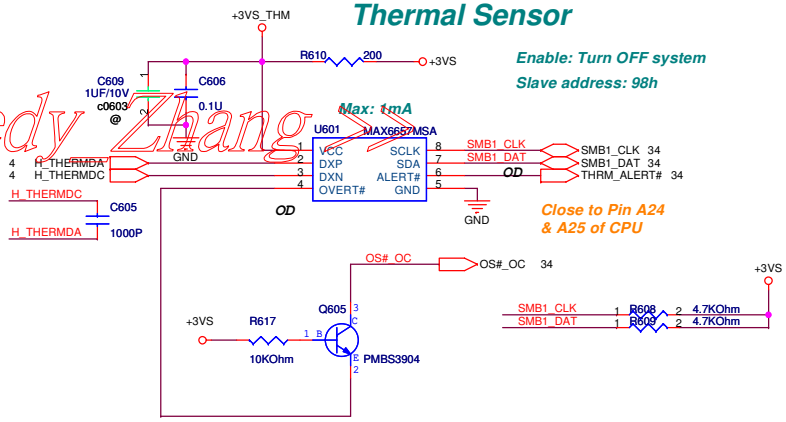


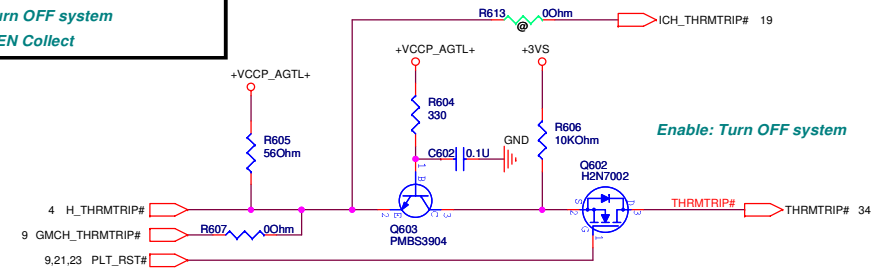


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC



Thermal Sensor





<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN_CTRL&Thernal	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Monday, October 16, 2006	Sheet 6 of 63	

CPU_BSEL0 R701 1K MCH_BSEL0 9
CPU_BSEL1 R702 1K MCH_BSEL1 9
CPU_BSEL2 R705 1K MCH_BSEL2 9

FSLC FSLB FSLA

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

PLACE termination close to source IC

CLK_CPU_BCLK R703 49.9 1%
CLK_CPU_BCLK# R704 49.9 1%
CLK_MCH_BCLK R706 49.9 1%
CLK_MCH_BCLK# R708 49.9 1%
CLK_MCH_3GPLL R709 49.9 1%
CLK_MCH_3GPLL# R710 49.9 1%
CLK_PCIE_NEWCARD R713 49.9 1%
CLK_PCIE_NEWCARD# R715 49.9 1%
CLK_PCIE_LAN R717 49.9 1%
CLK_PCIE_LAN# R718 49.9 1%
CLK_PCIE_MINICARD R763 49.9 1%
CLK_PCIE_MINICARD# R750 49.9 1%
CLK_PCIE_ICH R769 49.9 1%
CLK_PCIE_ICH# R770 49.9 1%
CLK_SATA_ICH R726 49.9Ohm
CLK_SATA_ICH# R728 49.9Ohm
DREFCLKIN R737 49.9 1%
DREFCLKIN# R741 49.9 1%
DREFSSCLKIN R744 49.9 1%
DREFSSCLKIN# R746 49.9 1%

U701 ICS954310CGLFT

Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64

Latched Input Select

/ PIN9	PIN5	PIN17	PIN18
* 0	X	27FIX	27SS
1	0	96MSS_T	96MSS_C
1	1	PCIEX0_T	PCIEX0_C

PEREQ#1: PCIEX0, PCIEX6
PEREQ#2: PCIEX1, PCIEX8
PEREQ#3: PCIEX2, PCIEX4
PEREQ#4: PCIEX3, PCIEX5, PCIEX7

From Power

ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)

<Variant Name>

ASUSTeK COMPUTER INC
Title : ICS954310
Engineer: Chao-liang_Hung
Size: Custom | Project Name: F9F | Rev: 2.00
Date: Monday, October 16, 2006 | Sheet 7 of 63

RCOMP

For Calibrating FSB I/O Buffer

H_XRCOMP 10/20mils R801 24.9 1% GND

H_YRCOMP 19/20mils R802 24.9 1% GND

SCOMP

For Slew Rate Compensation on the FSB

+VCCP_AGTL+ R804 54.9 1% H_XSCOMP 4.5/20 mils

+VCCP_AGTL+ R805 54.9 1% H_YSCOMP 4.5/20 mils

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit

+VCCP_AGTL+ R807 221Ohm 1% H_XSWING 4.5/20mils R808 100 1% C801 0.1U GND GND

+VCCP_AGTL+ R809 221Ohm 1% H_YSWING 4.5/20mils R811 100 1% C803 0.1U GND GND

H_D#[0..63] 4

U801A HOST

CALISTOGA_Q137

H_A#[3..31] H_A#[3..31] 4

7 CLK_MCH_BCLK
7 CLK_MCH_BCLK#

H_ADS# 4
H_ADSTB#0 4
H_ADSTB#1 4
H_BNR# 4
H_BPRI# 4
H_BR0# 4
H_CPURST# 4
H_DBSY# 4
H_DEFER# 4
H_DPWR# 4
H_DRDY# 4

H_DINV#0 4
H_DINV#1 4
H_DINV#2 4
H_DINV#3 4

H_DSTBN#0 4
H_DSTBN#1 4
H_DSTBN#2 4
H_DSTBN#3 4

H_DSTBP#0 4
H_DSTBP#1 4
H_DSTBP#2 4
H_DSTBP#3 4

H_HIT# 4
H_HITM# 4
H_LOCK# 4

H_REQ#[4..0] 4
H_RS#[0..2] 4

H_CPUSLP# 4,19
H_TRDY# 4

H_VREF

H_CPURST# T801

AGTL+ I/O Voltage Reference

+VCCP_AGTL+ R803 100 1% R806 200 1% C802 0.1U GND GND

<500 mil (55 Ohm) T/B tracc 5.5 , Space 25

<Variant Name>

Title : Calistoga--CPU

ASUSTeK COMPUTER INC Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

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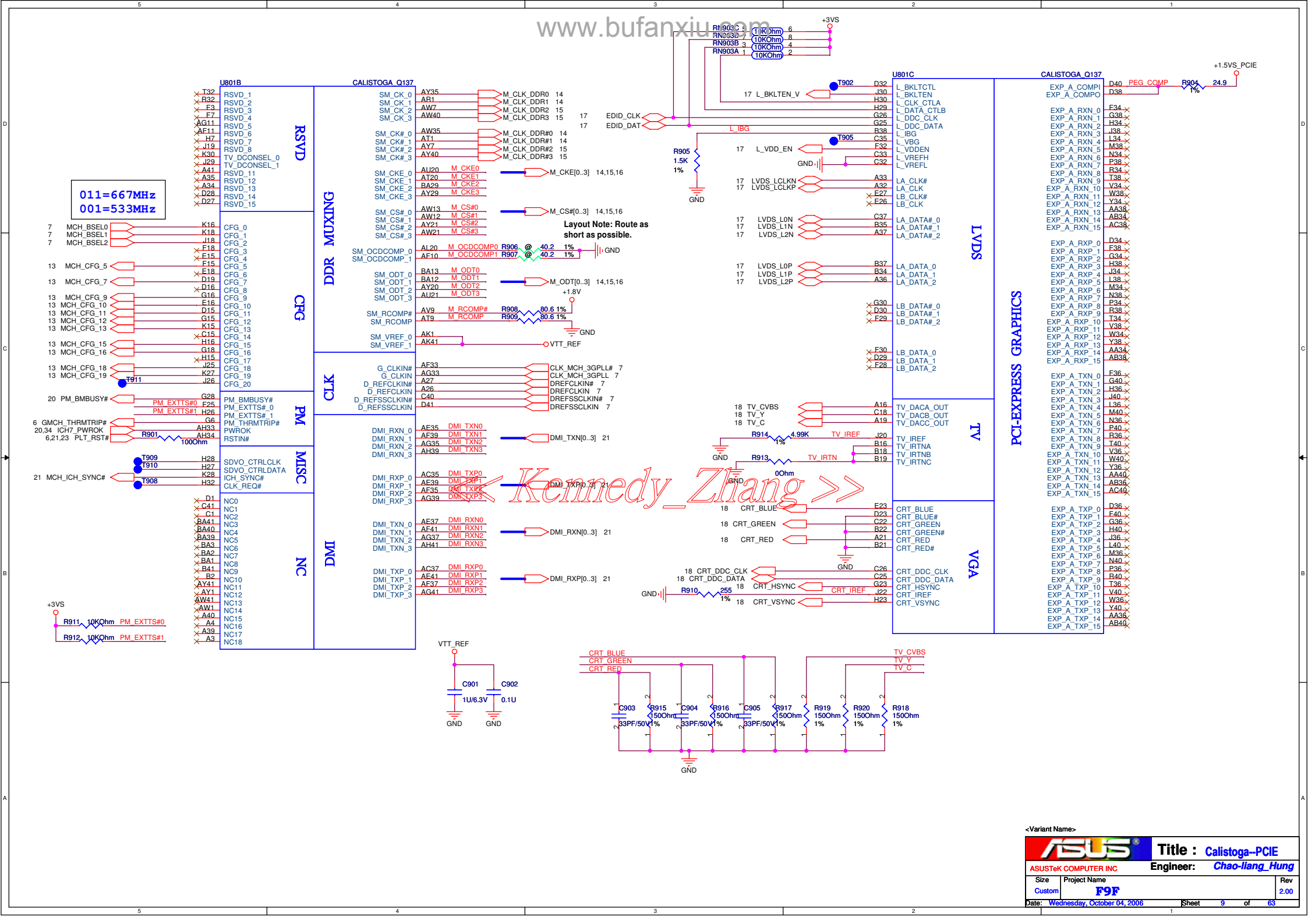

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--PCIE

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

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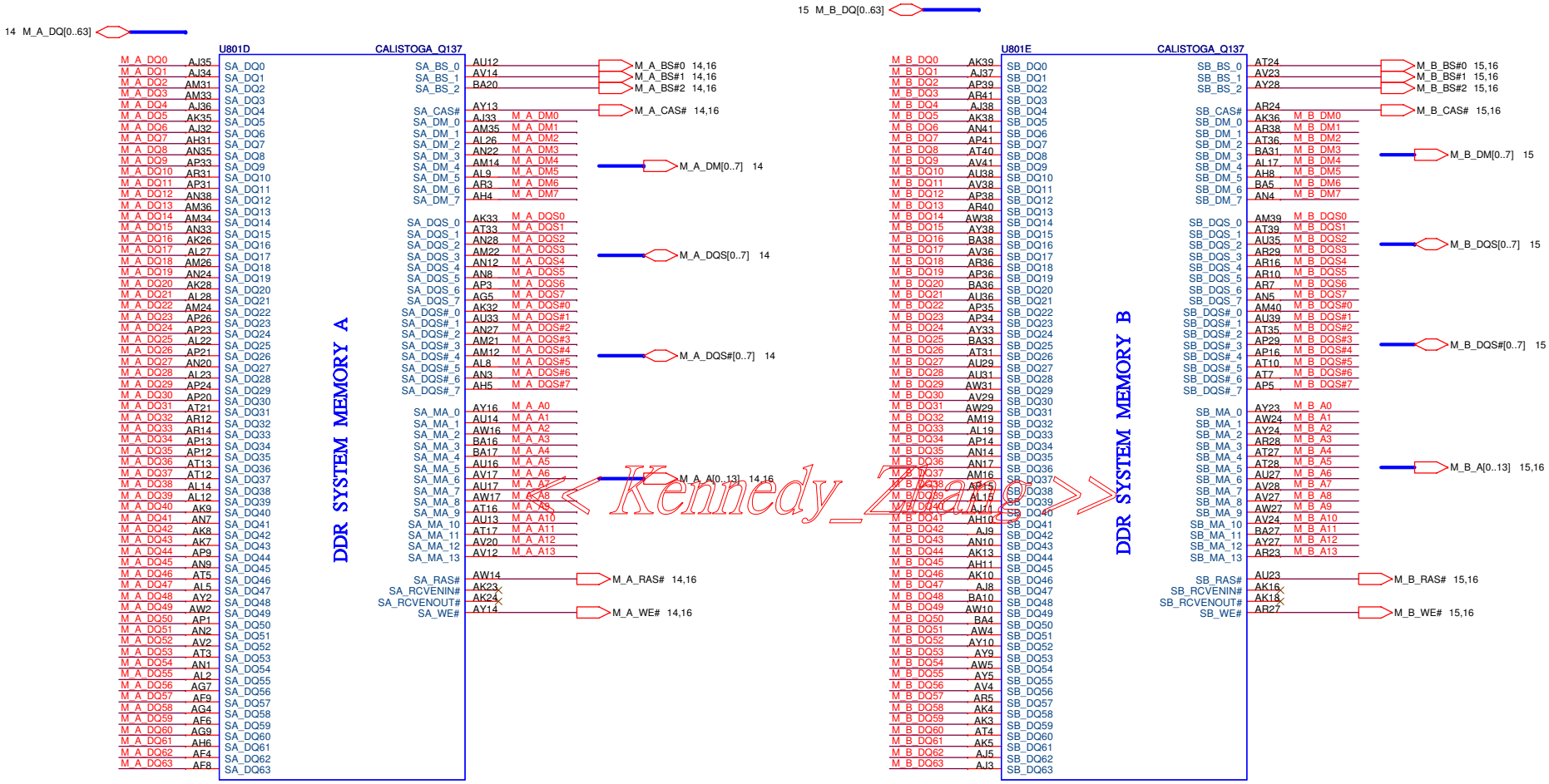

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--DDR2

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

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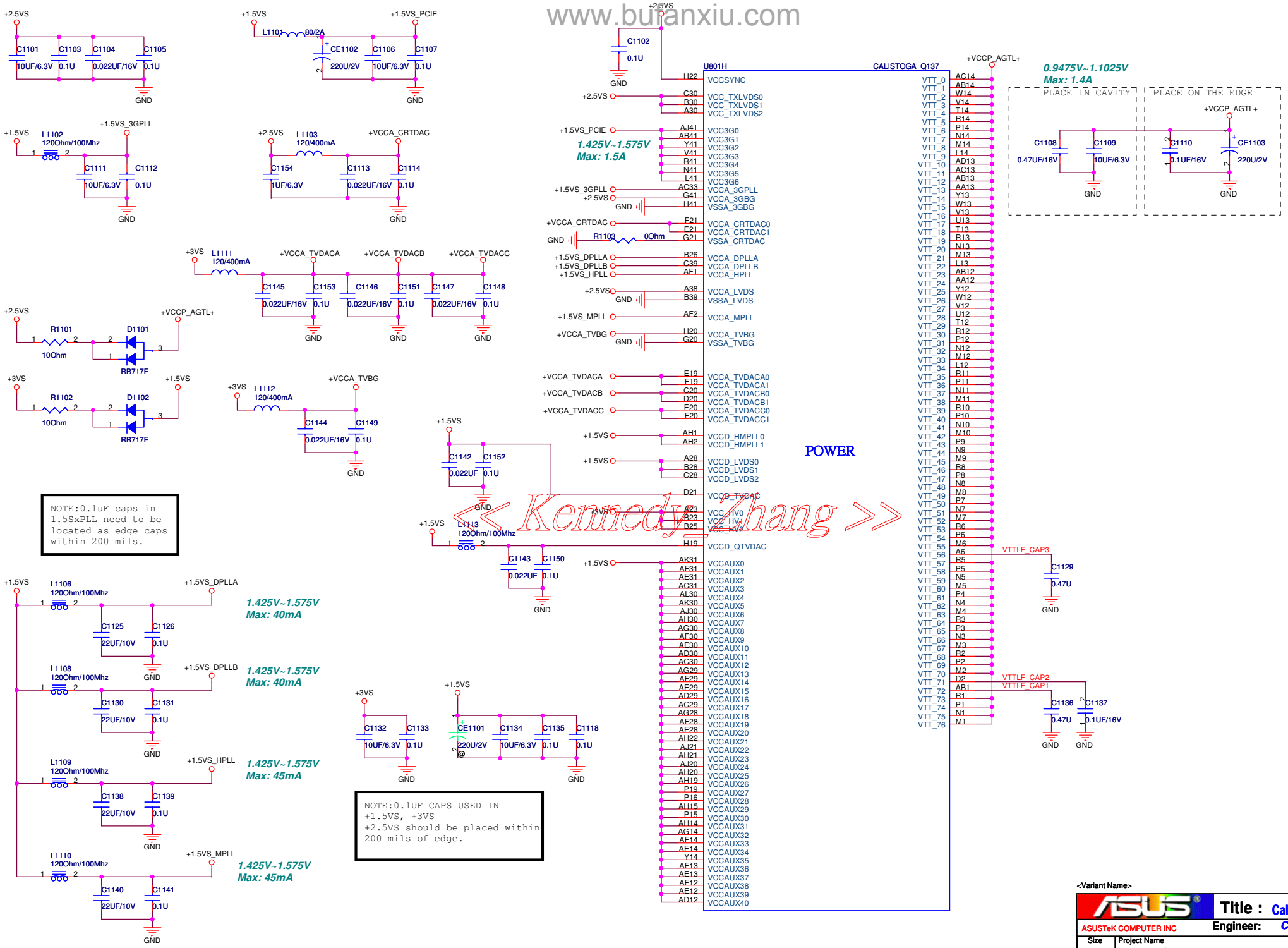
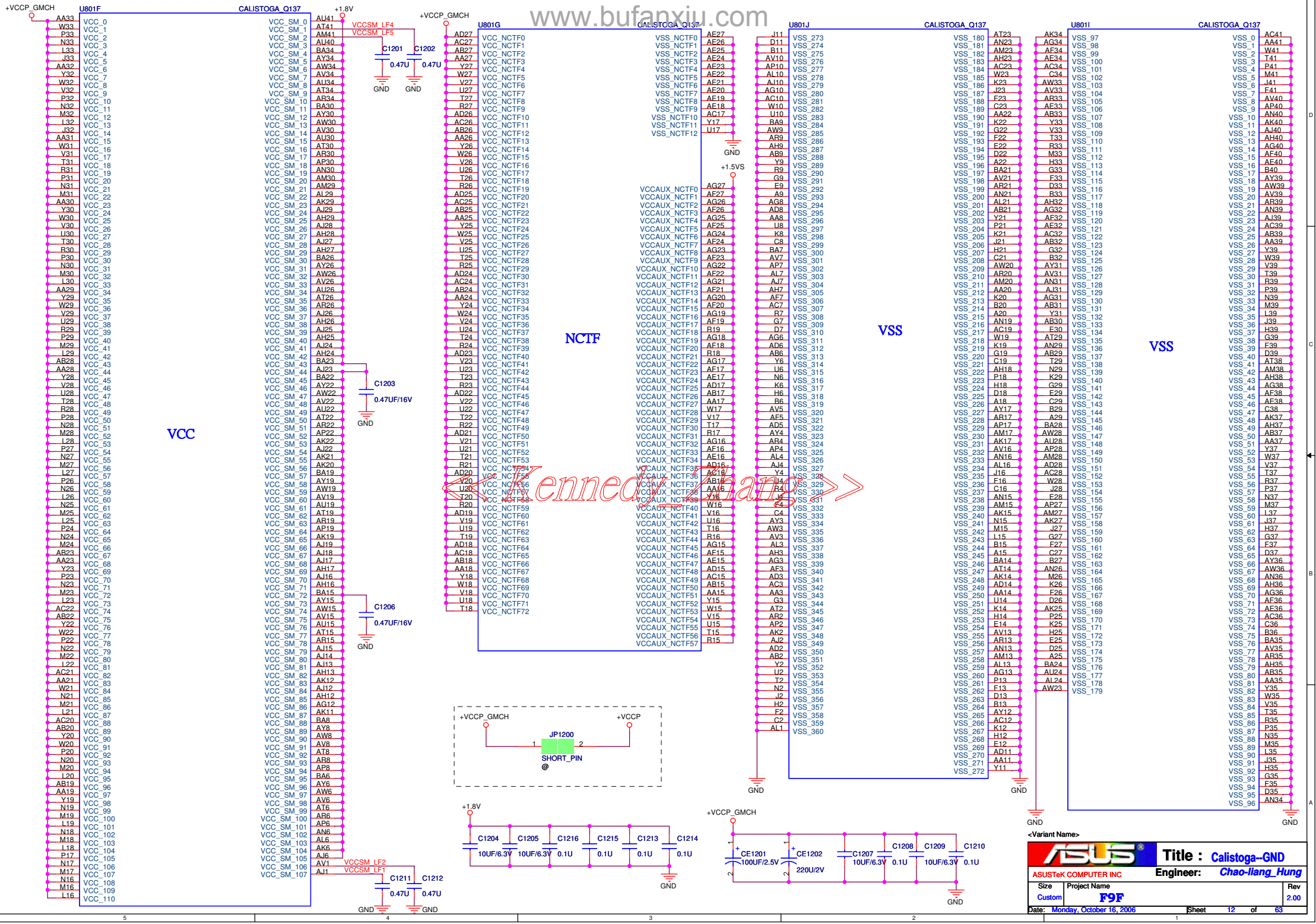
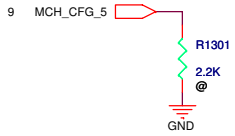


<variant_name>

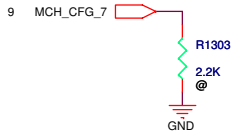
ASUSTeK COMPUTER INC	Title : Calistoga--POWER	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 11 of 63	





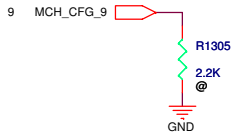
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



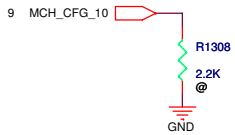
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



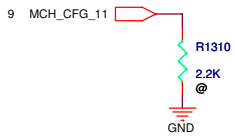
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

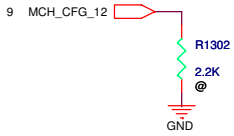
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

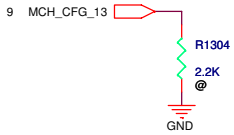
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

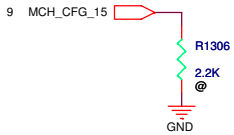
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



CFG[13:12] : GMCH TEST MODE SELECT

00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)



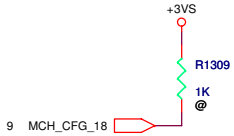


CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)

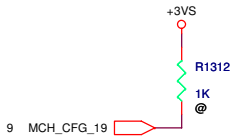
CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



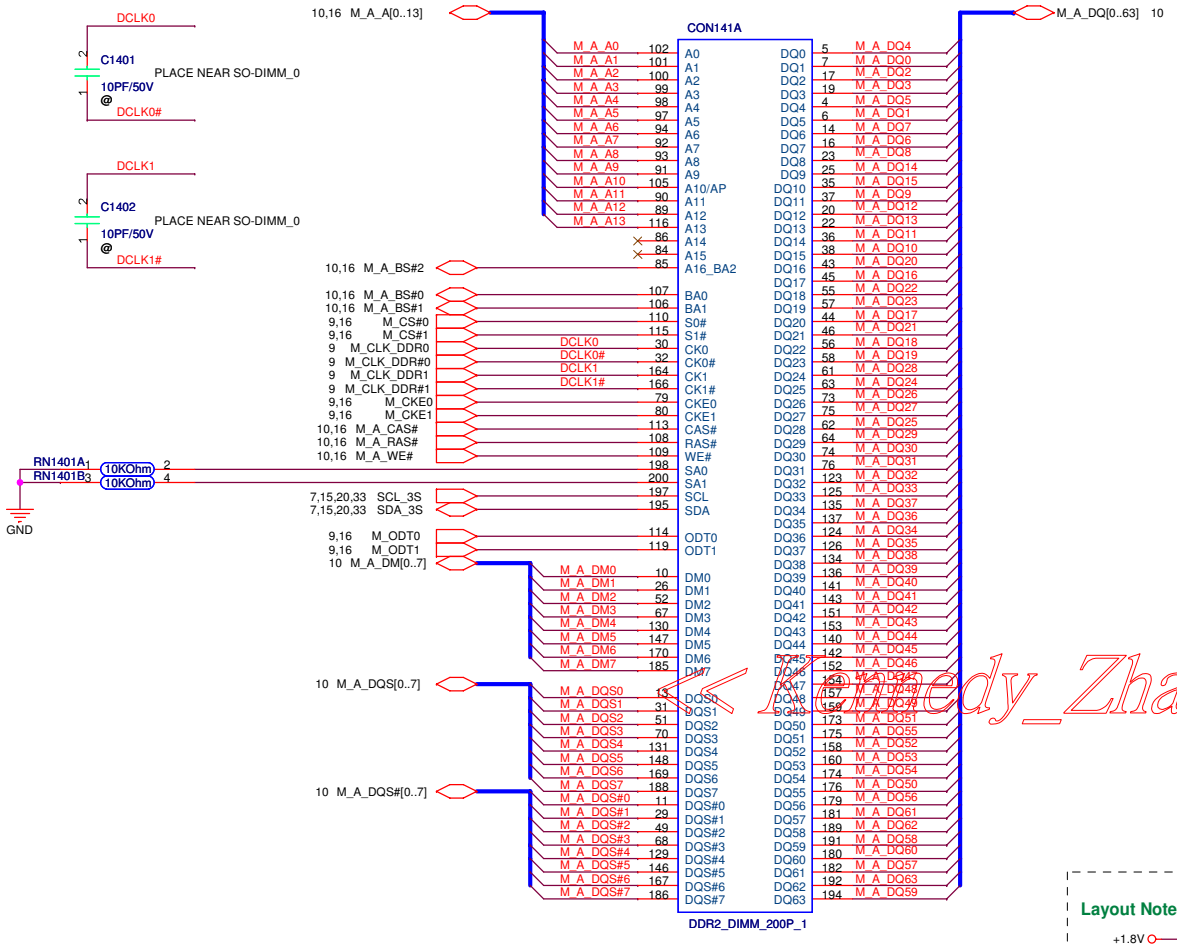
CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

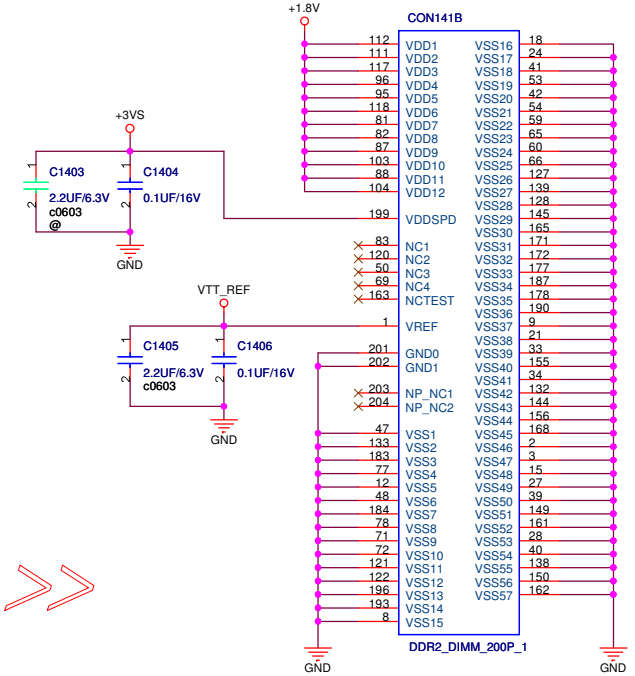
<Variant Name>

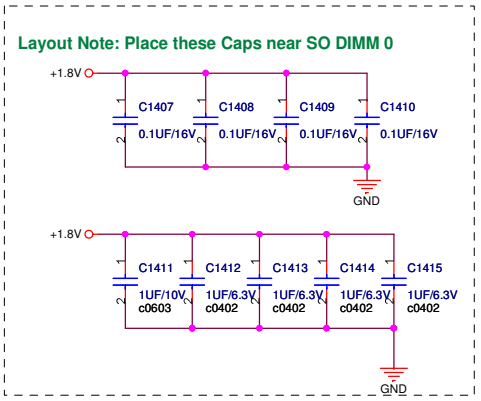
ASUSTeK COMPUTER INC	Title : Calistoga--Strap	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 13 of 63	

SMBus Slave Address:A0H



Hight: 4.0 mm

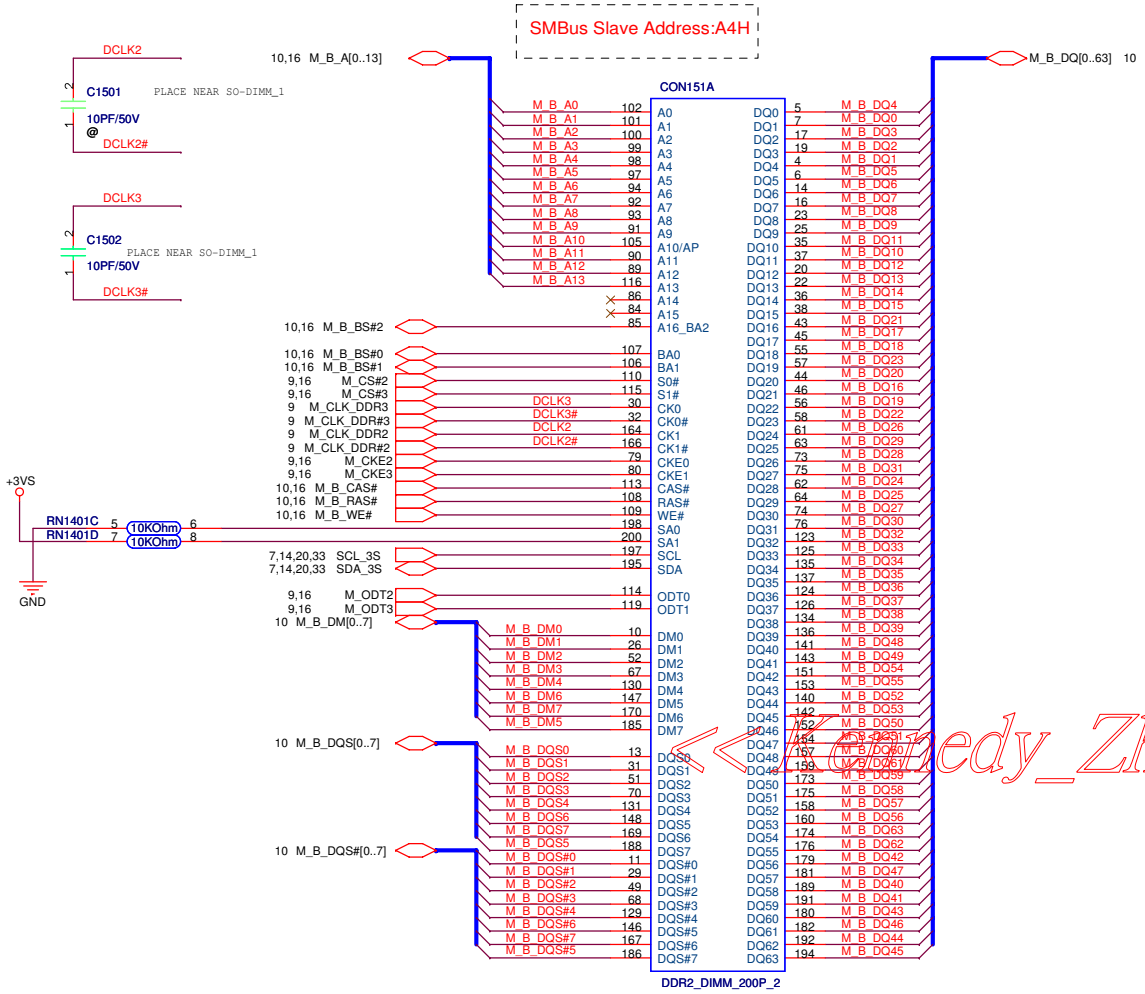


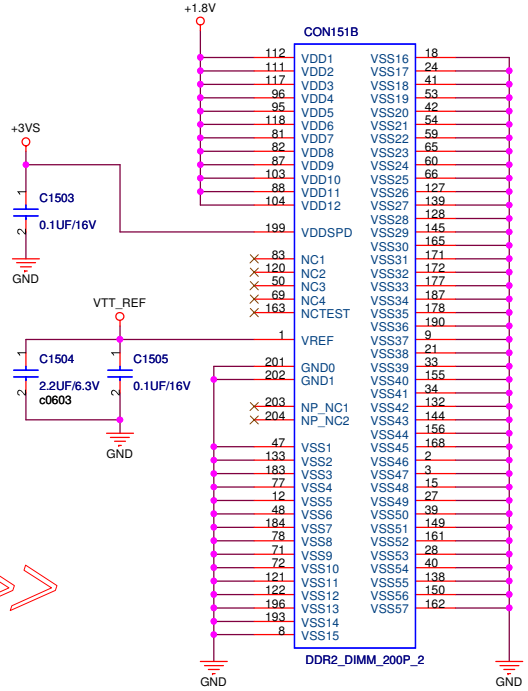


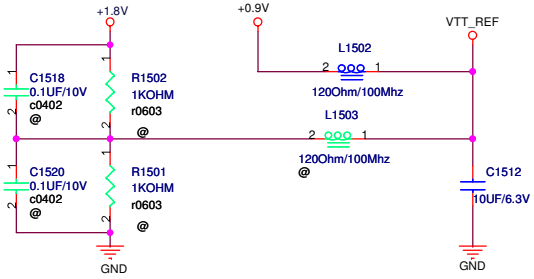
<Variant Name>

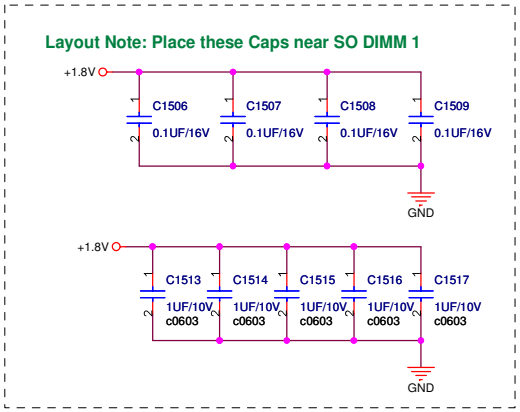
ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_0	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 14 of 63	

SMBus Slave Address:A4H









<Variant Name>

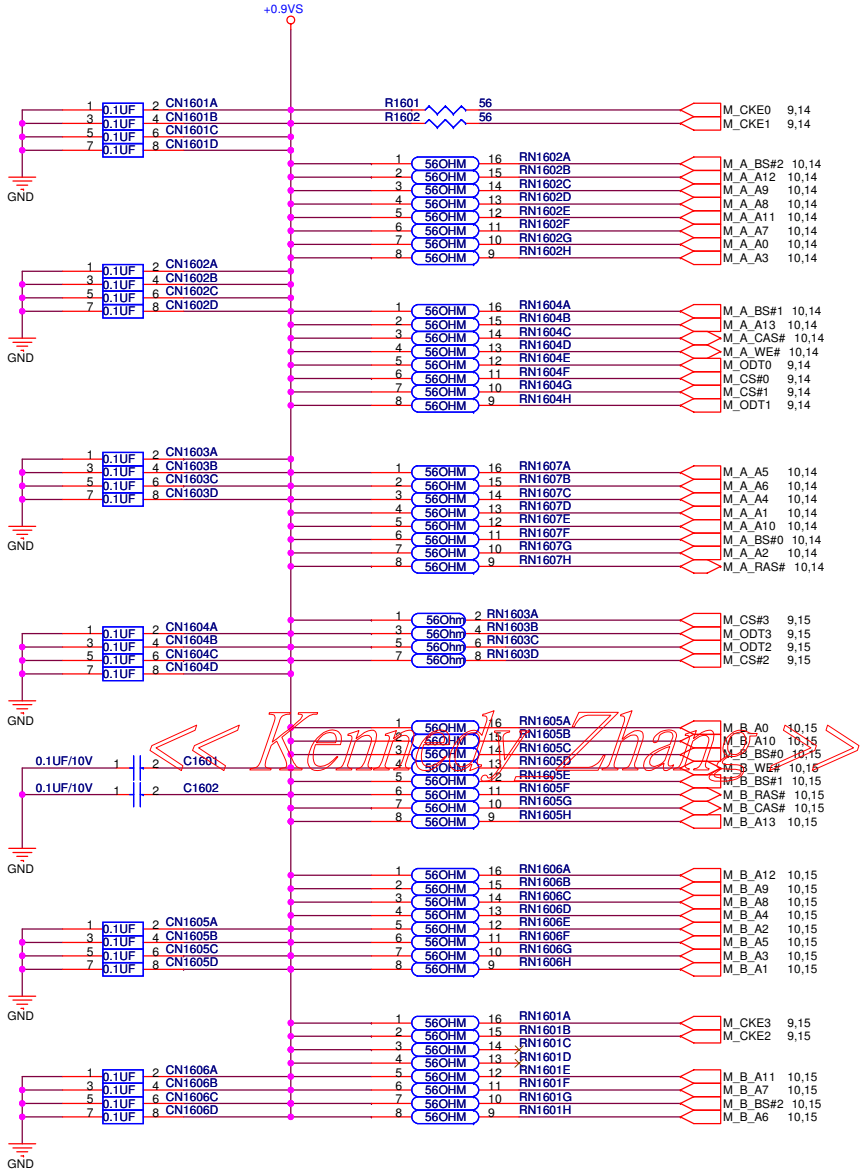
Title : DDR2 SO-DIMM_1

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 15 of 63



Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 TERMINATION

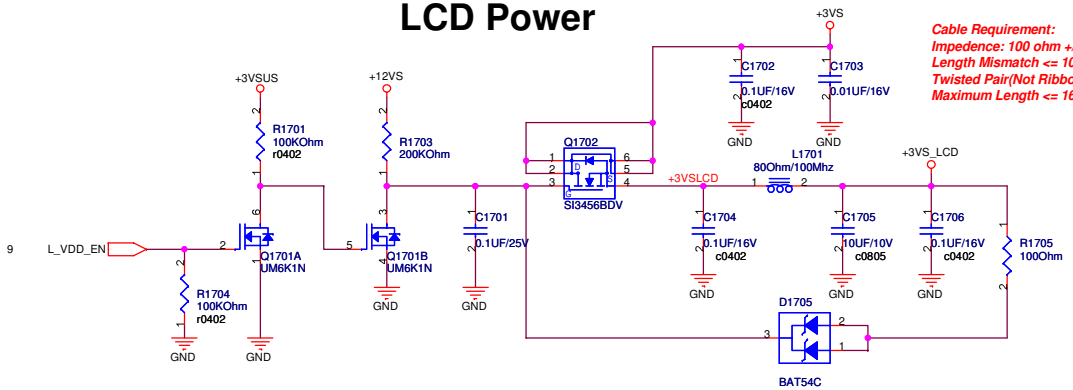
Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

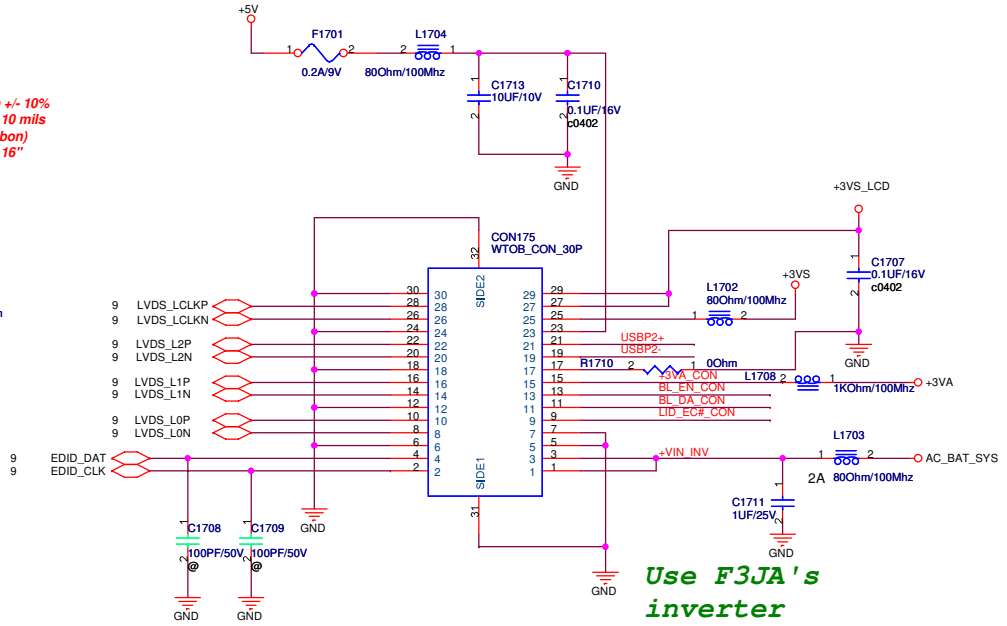
Date: Wednesday, October 04, 2006 Sheet 16 of 63

LCD Backlight Control

LCD Power



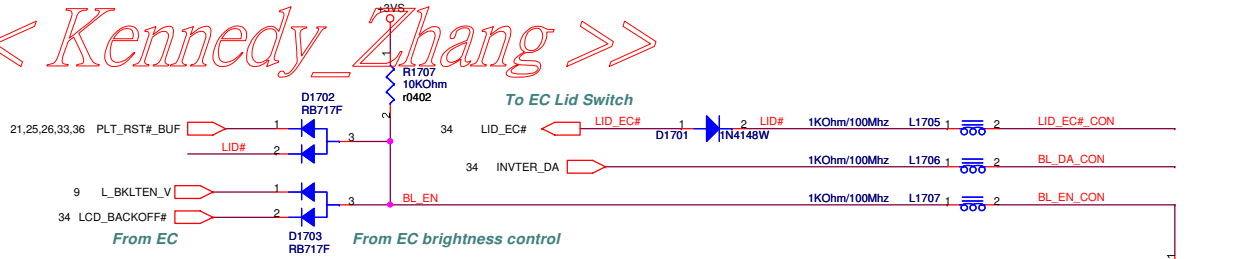
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



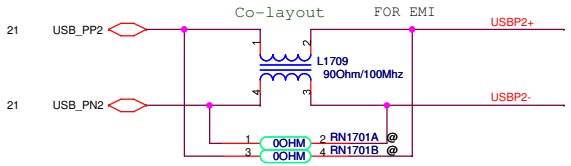
Use F3JA's inverter

Remove CCD connector

<< Kennedy_Zhang >>

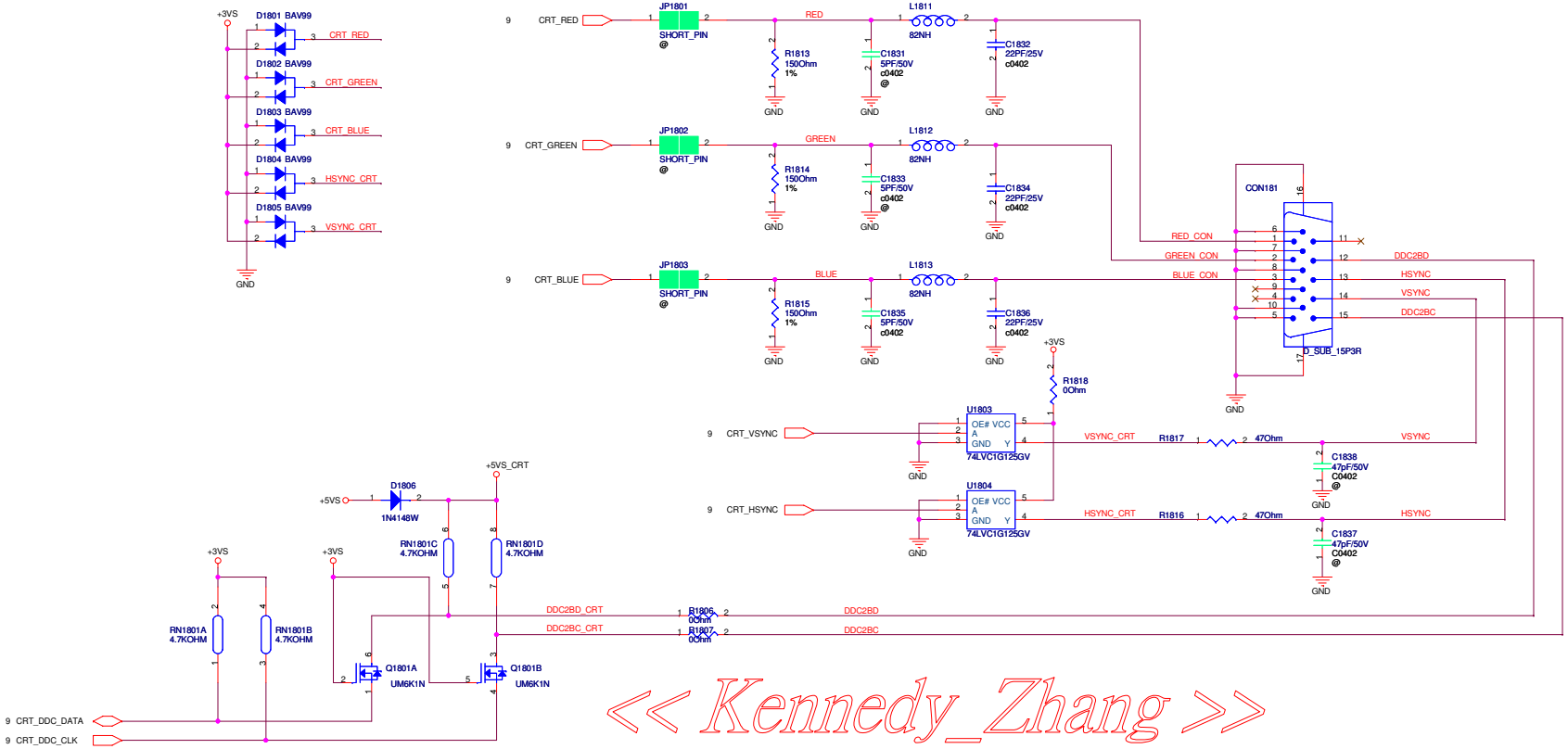


BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

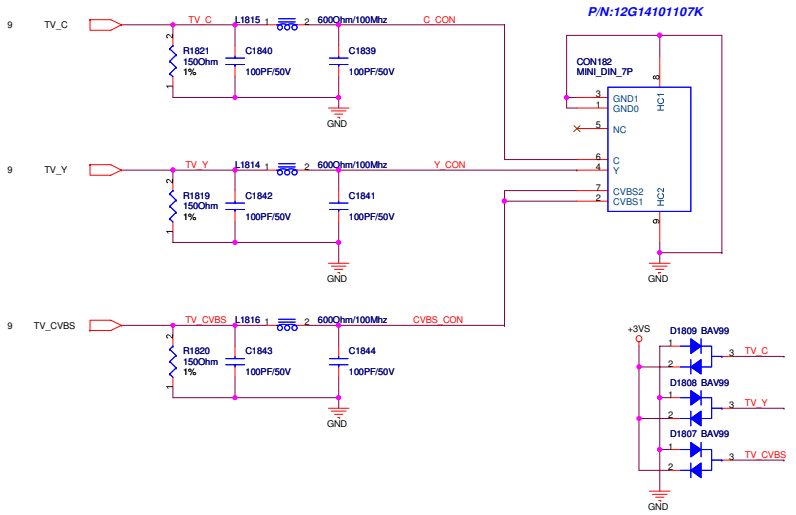


<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 17 of 63	



TV



<Variant Name>

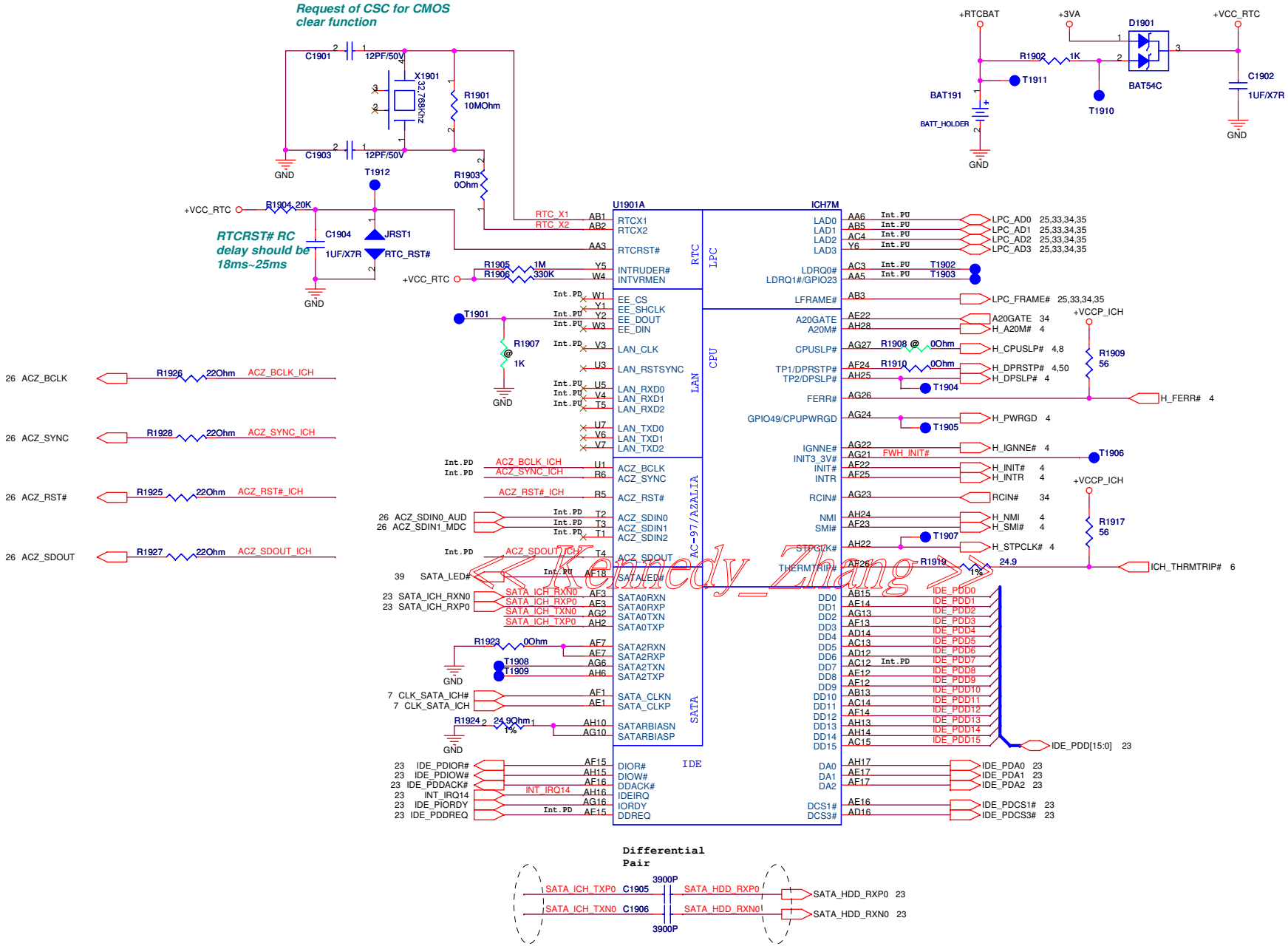
ASUSTeK COMPUTER INC

Title : CRT & TV OUT

Engineer: Chao-liang_Hung

Size	Project Name	Rev
C	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 18 of 63



To new card check power plane

U1901C

ICH7M

SMB: SCL_3S C22 SMBCLK; SDA_3S B22 SMBDATA; LINKALERT# A26 LINKALERT#; SM_LINK0 B25 SMLINK0; SM_LINK1 A25 SMLINK1

SATA GPIO: GPIO21/SATA0GP AF19 → T2009; GPIO19/SATA1GP AH18 → T2010; GPIO36/SATA2GP AH19 → T2008; GPIO37/SATA3GP AE19 PCB_ID0

RING# A28 RI#

26 SPKR_ICH A19 SPKR; 25 SUS_STAT# A27 SUS_STAT#; +3VSUS A22 SYS_RST#; R2001 10KOhm

9 PM_BMBUSY# AB18 GPIO0/BM_BUSY#

SMB_ALERT# B23 SMBALERT#/GPIO11

7 STP_PCI# AC20 GPIO18/STPPCI#; 7 STP_CPU# AF21 GPIO20/STPCPU#

25 BT_ON# A21 GPIO26

26 WLAN_ON# B21 GPIO27; 35 MEROM/YONAH# E23 GPIO28

25 PM_CLKRUN# AG18 GPIO32/CLKRUN#

T2014 AC19 GPIO33/AZ_DOCK_EN#; U2 GPIO34/AZ_DOCK_RST#

7 CPU_Select

26,29,33 PCIE_WAKE# F20 WAKE#; 25,34 INT_SERIRQ AH21 SERIRQ; 34 PM_THRM# AF20 THRM#

T2001 VRMPWRGD; 34,50,60 VRM_PWRGD; R2004 0Ohm AD22 VRMPWRGD

POWER 39 BT_LED_EN AC21 GPIO6; 25,26,38 RF_ON_SW# RF_ON_SW AC18 GPIO7; 34 EXTSMI# F21 GPIO8

GPIO: GPIO9 E20 → T2016; GPIO10 A20 GPIO10 → T2011; GPIO12 F19 → KBC_SCI# 34; GPIO13 E19 → T2004; GPIO14 R4 → T2012; GPIO15 E22; GPIO24 R3 → 802_LED_EN 39; GPIO25 D20 Int.PU GPIO25 → T2019; GPIO35 AD21 → T2013; GPIO38 AD20 PCB_ID1; GPIO39 AE20 PCB_ID2

Clocks: CLK14 AC1; CLK48 B2 → CLK_ICH14 7, CLK_USB48 7; SUSCLK C20 SUS_CLK → SUS_CLK 25

C2001 @ 10P; C2002 @ 10P; GND

Power MGT: SLP_S3# B24 → SUSB# 34; SLP_S4# D23 → SUSC# 34; SLP_S5# F22 → T2002

PWROK AA4 → ICH7_PWROK 9,34

GPIO16/DPRSLPVR AC22 Int.PD POWER → PM_DPRSLPVR 50

TP0/BATLOW# C21 → BAT_LL# 34

PWRBTN# C23 Int.PU → PM_PWRBTN# 34 → T2003

R2002 10KOhm; GND

LAN_RST# C19 ICH_LAN_RST# R2036 0Ohm

RSMRST# Y4 → PM_RSMRST# 34

R2030 10KOhm; GND

VRM_PWRGD
Pull Hi 100K
+3VS at power circuit

ICH7_PWROK R2006 @ 0Ohm VRMPWRGD

<< Kennedy Zhang >>

Clock Generator
DDR2 SO-DIMM

+3VS

7,14,15,33 SCL_3S → SCL_3S R2005 2.2K

7,14,15,33 SDA_3S → SDA_3S R2007 2.2K

PM_THRM# R2026 10KOhm

+3VSUS

RING# R2008 10KOhm

SMB_ALERT# RN2001A 1 10KOhm 2
SM_LINK1 RN2001B 3 10KOhm 4
SM_LINK0 RN2001C 5 10KOhm 6
LINKALERT# RN2001D 7 10KOhm 8

BAT_LL# RN2002A 1 10KOhm 2
BT_ON# RN2002B 3 10KOhm 4
WLAN_ON# RN2002C 5 10KOhm 6
KBC_SCI# RN2002D 7 10KOhm 8

EXTSMI# R2035 10KOhm

PCIE_WAKE# R2021 2.2K

SUS_STAT# R2025 @ 10KOhm

GPIO10 R2038 @ 10KOhm

GPIO25 R2039 @ 10KOhm

MEROM/YONAH# R2037 10KOhm

802_LED_EN R2031 10KOhm

BT_LED_EN R2032 10KOhm

GND

+3VS

PCB_ID0
PCB_ID1
PCB_ID2

R2009 10KOhm @; R2010 10KOhm @; R2011 10KOhm @

R2017 10KOhm @; R2018 10KOhm @; R2019 10KOhm @

GND

+3VS

21 PCI_SERR# RP2001A 1 8.2K 5 10
21 PCI_DEVSEL# RP2001B 2 8.2K 5 10
21 PCI_TRDY# RP2001C 3 8.2K 5 10
21 PCI_REQ#4 RP2001D 4 8.2K 5 10
21 PCI_FRAME# RP2001E 6 8.2K 5 10
21 PCI_STOP# RP2001F 7 8.2K 5 10
21 PCI_REQ#1 RP2001G 8 8.2K 5 10
21 PCI_REQ#2 RP2001H 9 8.2K 5 10

21 PCI_REQ#3 RP2002A 1 8.2K 5 10
21 PCI_LOCK# RP2002B 2 8.2K 5 10
RP2002C 3 8.2K 5 10
RP2002D 4 8.2K 5 10
21 PCI_INTH# RP2002E 6 8.2K 5 10
21 PCI_INTF# RP2002F 7 8.2K 5 10
21 PCI_INTE# RP2002G 8 8.2K 5 10
21 PCI_INTG# RP2002H 9 8.2K 5 10

21 PCI_INTA# RP2003A 1 8.2K 5 10
21 PCI_INTB# RP2003B 2 8.2K 5 10
21 PCI_INTC# RP2003C 3 8.2K 5 10
21 PCI_INTD# RP2003D 4 8.2K 5 10
21 PCI_REQ#0 RP2003E 6 8.2K 5 10
21 PCI_IRDY# RP2003F 7 8.2K 5 10
21 PCI_REQ#5 RP2003G 8 8.2K 5 10
21 PCI_PERR# RP2003H 9 8.2K 5 10

PM_CLKRUN# R2023 10KOhm
INT_SERIRQ R2013 10KOhm
STP_PCI# R2015 @ 10KOhm
STP_CPU# R2020 @ 10KOhm

<Variant Name>

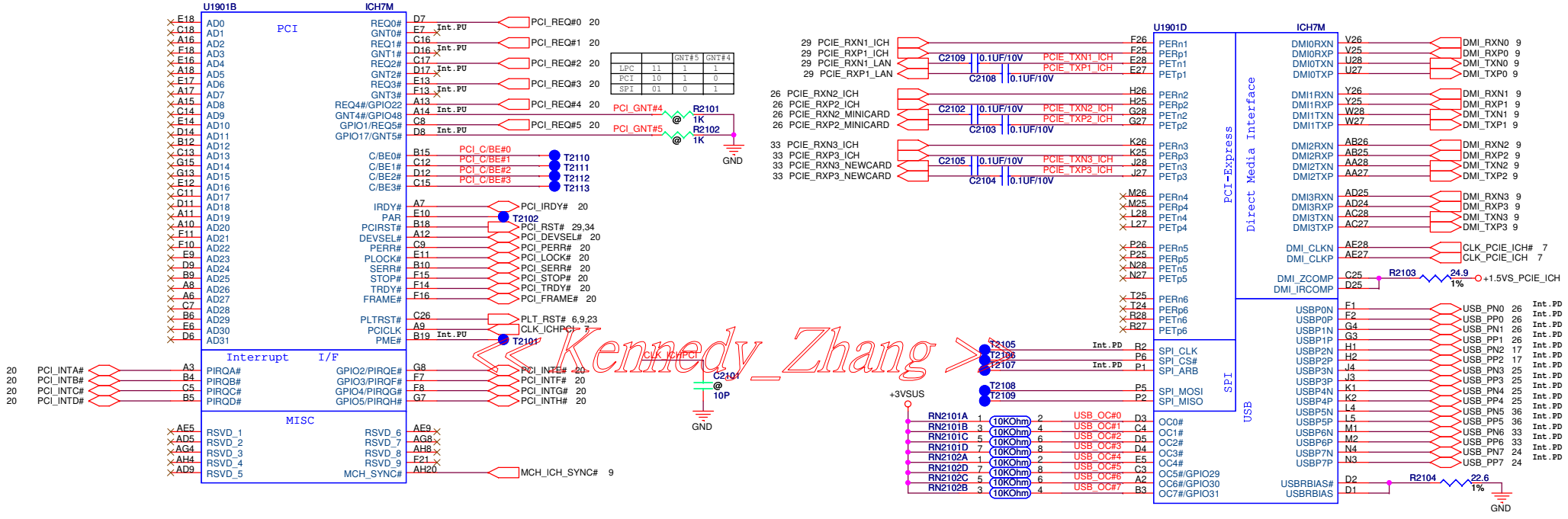
Title : ICH7M (2)

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 20 of 63



USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Cemera
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	CARD Reader
USB 6	NEWCARD
USB 7	USB Conn.

<Variant Name>

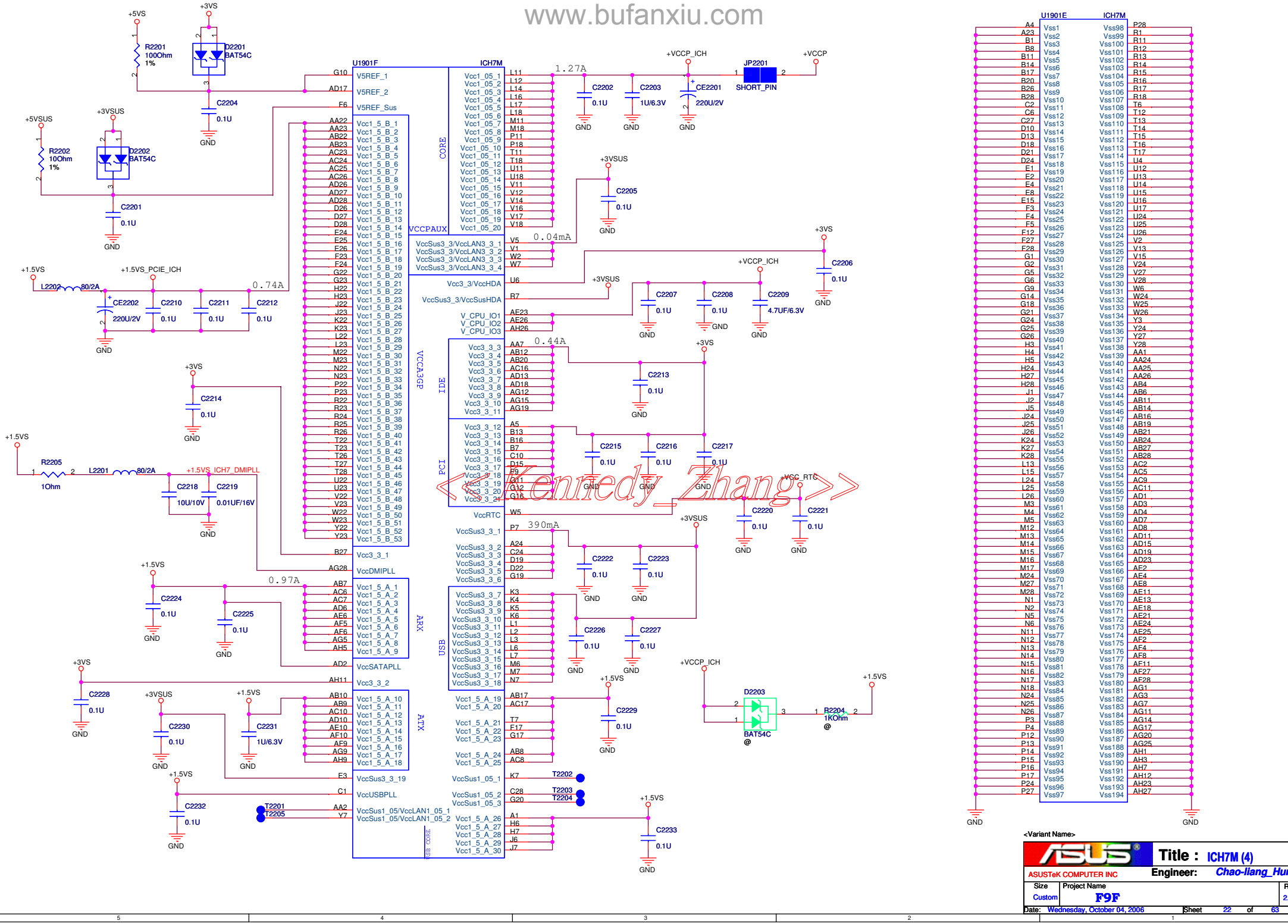
ASUSTeK COMPUTER INC

Title : ICH7M (3)

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 21 of 63



<Variant Name>

ASUSTeK COMPUTER INC

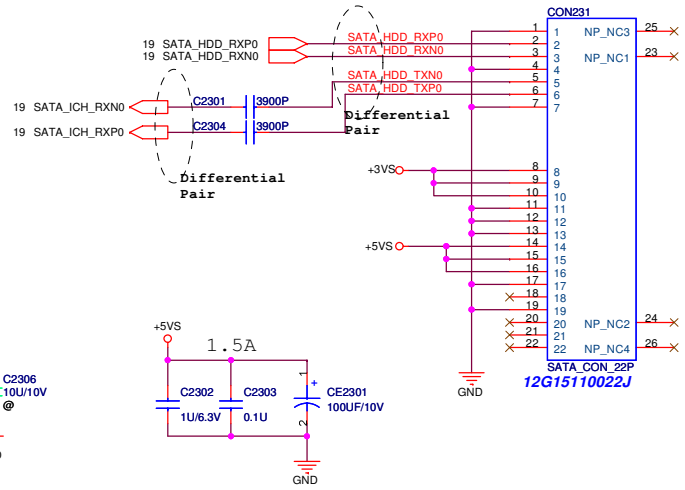
Title : ICH7M (4)

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

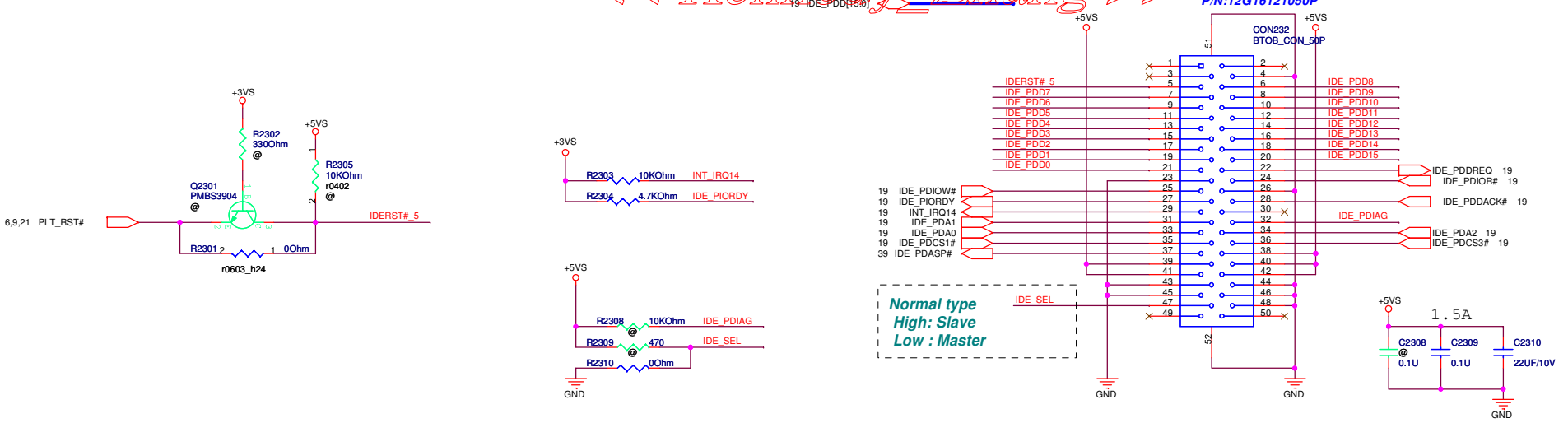
Date: Wednesday, October 04, 2006 Sheet 22 of 63

SATA HDD CON



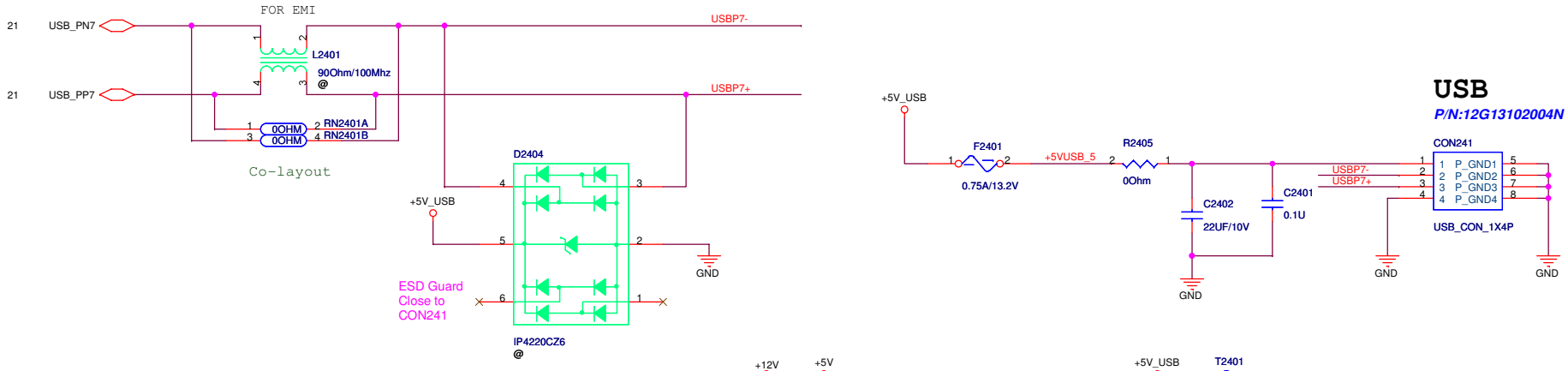
PATA CD-ROM CON

P/N:12G16121050P



<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Saturday, October 14, 2006	Sheet 23 of 63	



<Variant Name>

ASUSTeK COMPUTER INC	Title : USB PORTS	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 24 of 63	

Co-layout FOR EMI

Low -> Diable
High -> Enable

max. 60mA

21 USB_PN4
21 USB_PP4
L2501 90Ohm/100Mhz @
0OHM RN2501B
RN2501A 0OHM
USBP4-
USBP4+
T2501 TPC28T
26 BT_CHCLK
26 BT_CHDAT
BT_ON
BT_LINK_LED
For Intel Wireless CoExistence System
R2504 100KOhm r0402
CON251 WTOB_CON_8P
+3V
GND

R2503 10KOhm
BT_ON
20,26,38 RF_ON_SW#
RF_ON_SW#
Q2503 H2N7002 @
Q2502 H2N7002
BT_ON# 20

+3VS_FP=1.215x(1+68K/39.2K)=3.32V

+5VS
D2505 1N4148W @
C2510 1UF/10V c0603
U2501 SI9183DT
VIN VOUT GND FB SD#
T2502
+3VS_FP
R2509 0Ohm @
+3VS
R2518 68KOhm
R2517 39.2KOhm
C2511 2.2UF/6.3V
R2510 330Ohm @
Internal Discharge 150
Item12,Item13
R2519 0Ohm @
PLT_RST#_BUF
D2504 1N4148W @
R2520 0Ohm
34 F/P_RST#

<< Kennedy_Zhang >>

For Finger Printer

CON253 BTOB_20P
7 CLK_TPMPCI
R2521 0Ohm
CLK_TPMPCI_C
19,33,34,35 LPC_FRAME#
PLT_RST#_BUF
17,21,26,33,36 PLT_RST#_BUF
19,33,34,35 LPC_AD3
19,33,34,35 LPC_AD0
+3VS
+3V
R2507 0Ohm @
20 SUS_STAT#
R2505 0Ohm
R2506 0Ohm @
SUS_CLK 20
LPC_AD2 19,33,34,35
LPC_AD1 19,33,34,35
INT_SERIRQ 20,34
PM_CLKRUN# 20
P_GND1 P_GND2 NP_NC1 NP_NC2 P_GND3 P_GND4 P_GND5 P_GND6
C2504 10PF/50V c0402 @
GND

TPM Module CON

CON252 WTOB_CON_4P_3
L2502 80Ohm/100Mhz
USBP3+
USBP3-
C2502 10UF/10V
C2512 10UF/10V
+3VS_FP
GND

FOR EMI
21 USB_PN3
21 USB_PP3
L2503 90Ohm/100Mhz @
0OHM RN2502B
RN2502A 0OHM
USBP3-
USBP3+
D2503 IP4220CZ6
+3VS

C2503 c0402 0.1UF/16V @
C2501 c0402 0.1UF/16V
H2501 L4E_1A

<Variant Name>

ASUSTeK COMPUTER INC

Title : B/T,F/P& TPM

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

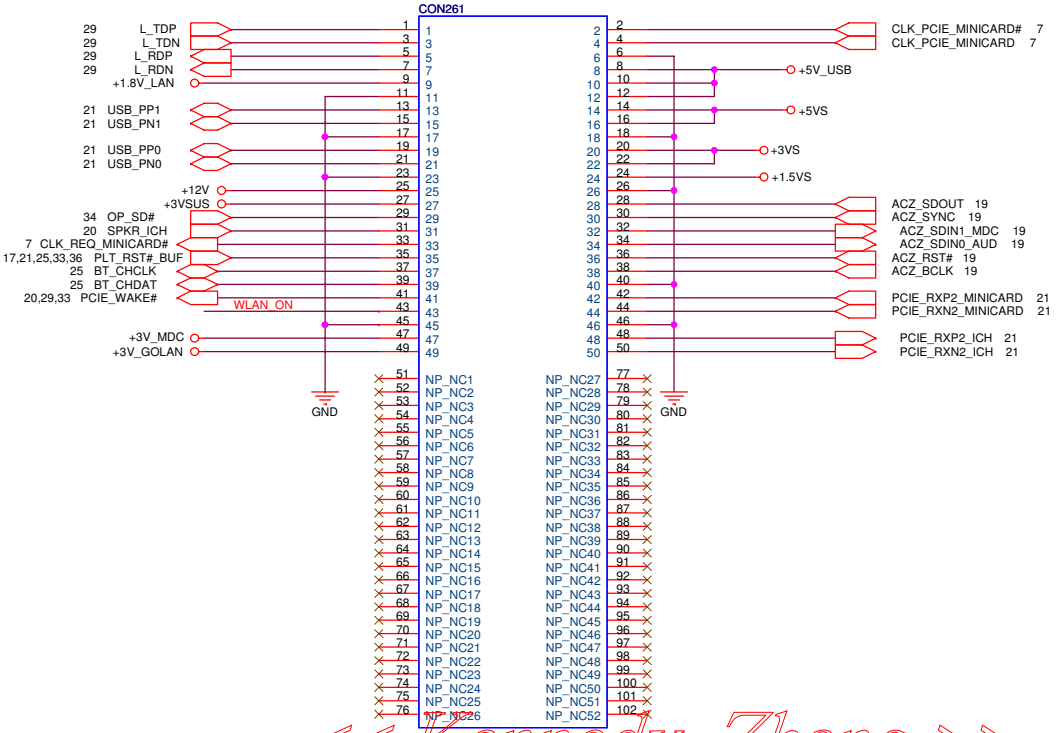
Date: Wednesday, October 04, 2006 Sheet 25 of 63

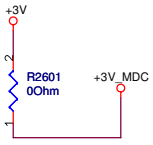
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

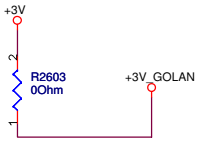
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA



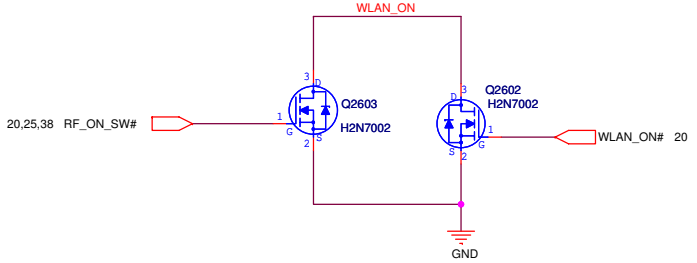


Reserved R to +3VSUS for Wake on RING function!



Reserved R to +3VSUS for Wake on WLAN function!

Intel SPEC(18780):Internal Pull UP 110Kohm



<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 26 of 63	

<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 27 of 63

<< Kennedy_Zhang >>

<Variant Name>

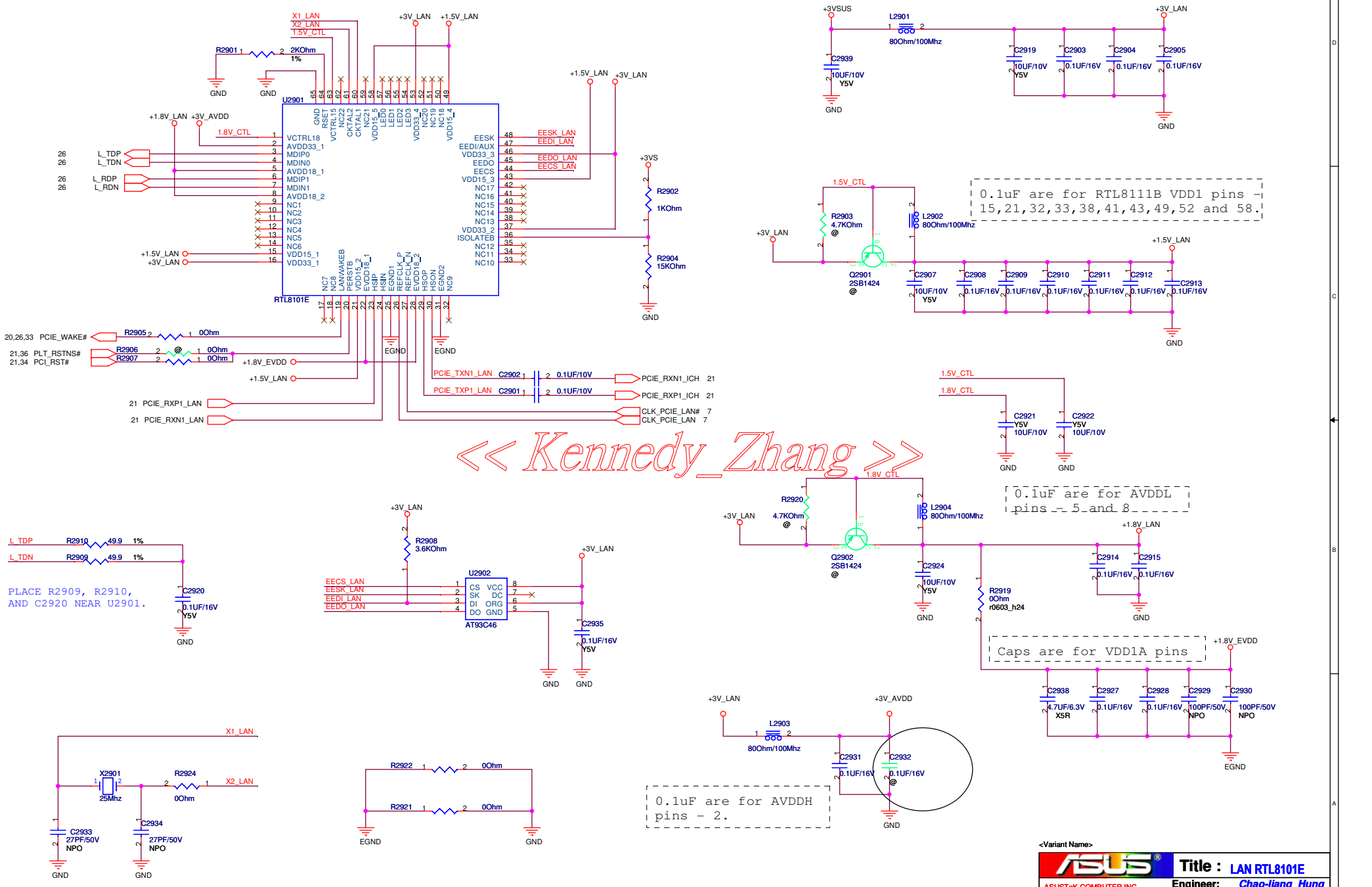
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 28 of 63



<Variant Name>

ASUSTeK COMPUTER INC	Title : LAN RTL8101E	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 29 of 63	

<< Kennedy_Zhang >>

ASUSTek COMPUTER INC	Title : EMPTY		
	Engineer: Chao-liang_Hung		
Size: Custom	Project Name: F9F		Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 30 of 63		

ASUSTek COMPUTER INC	Title : EMPTY		
	Engineer: Chao-liang_Hung		
Size: Custom	Project Name: F9F		Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 31 of 63		

<< Kennedy_Zhang >>

<Variant Name>

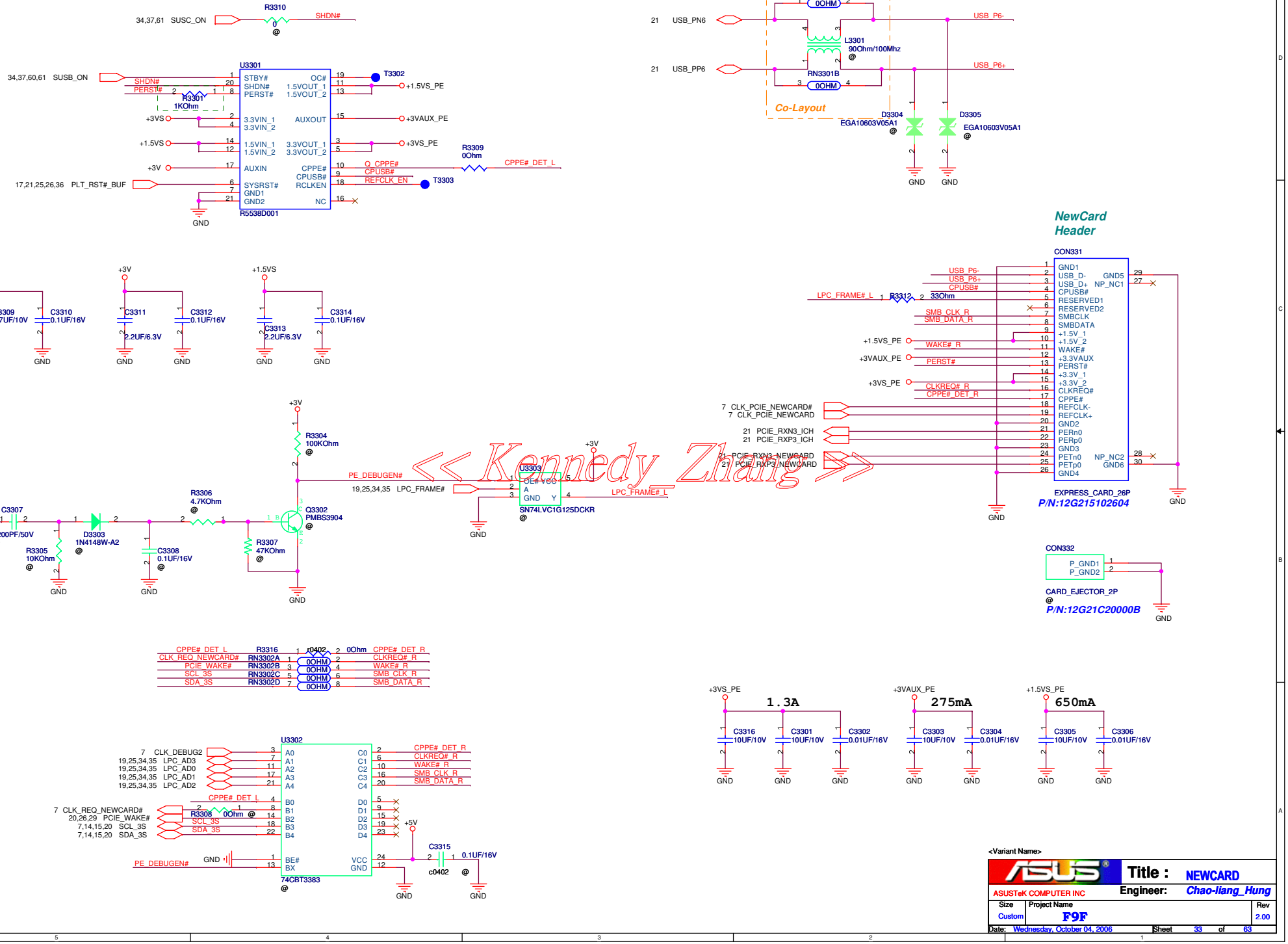
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

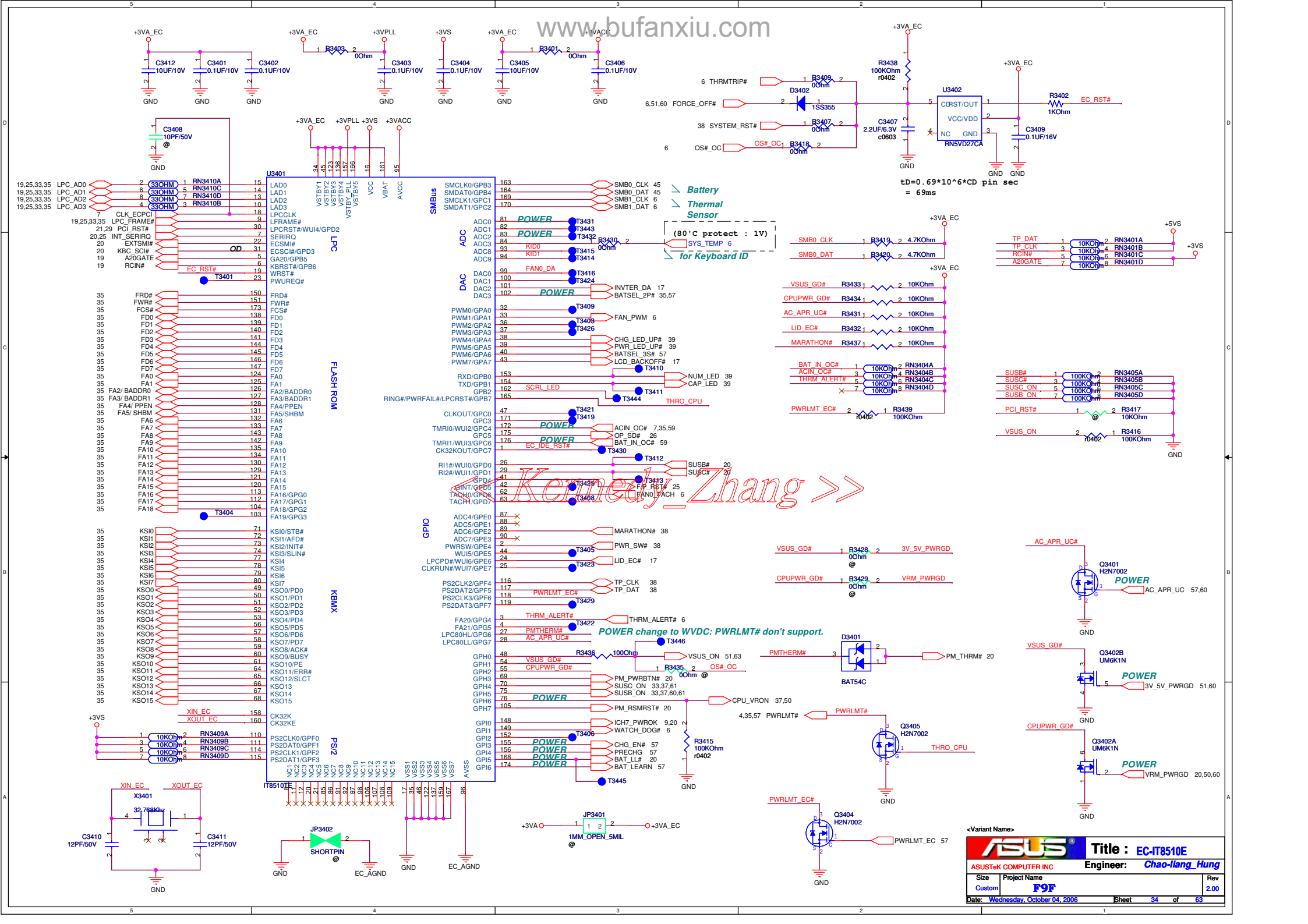
Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 32 of 63



<Variant Name>

ASUSTeK COMPUTER INC	Title : NEWCARD	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 33 of 63	



EC Hardware Strapping

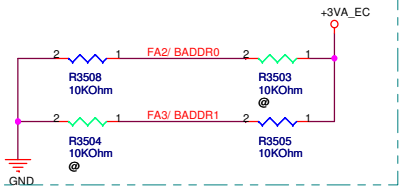
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

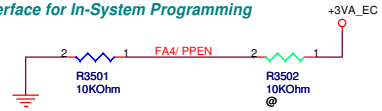


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

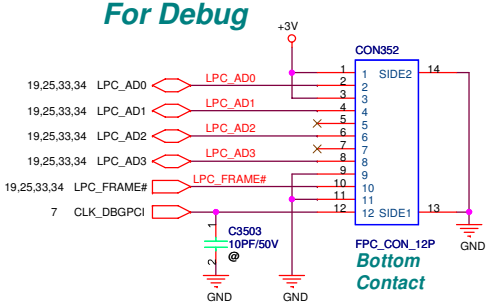


FA5/ SHBM

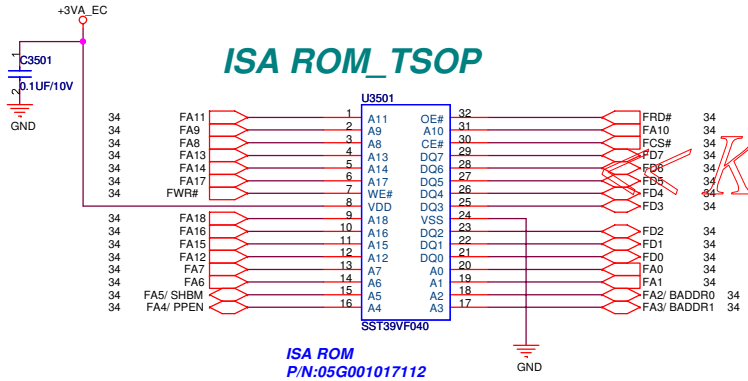
0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

For Debug



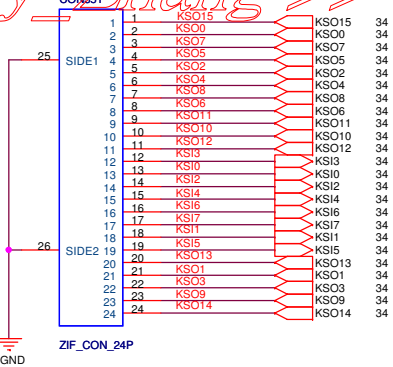
ISA ROM_TSOP

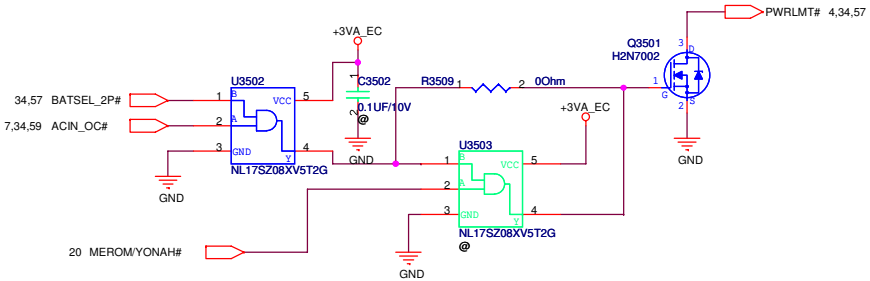


ISA ROM
P/N:05G001017112

For Keyboard

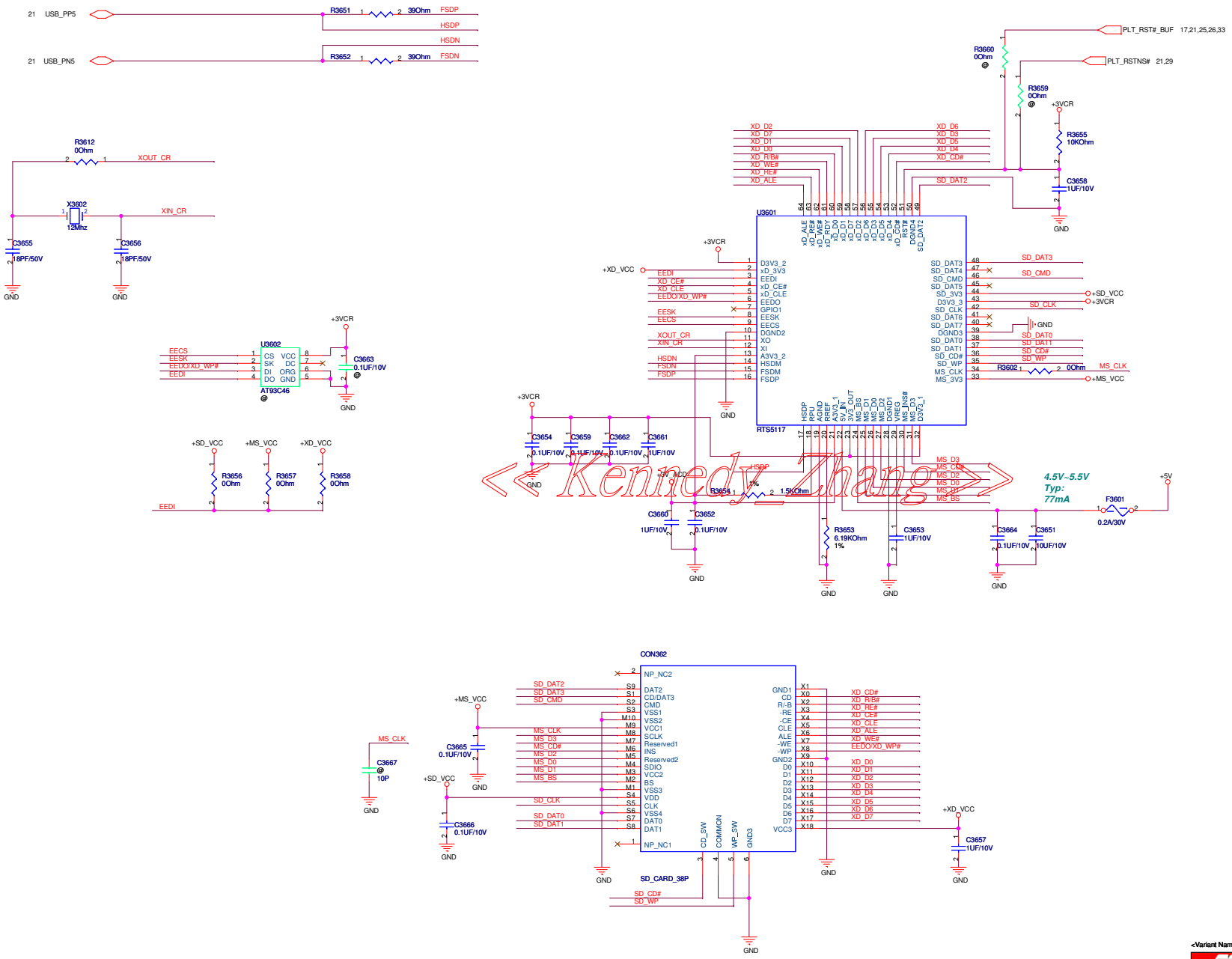
P/N:12G182402404





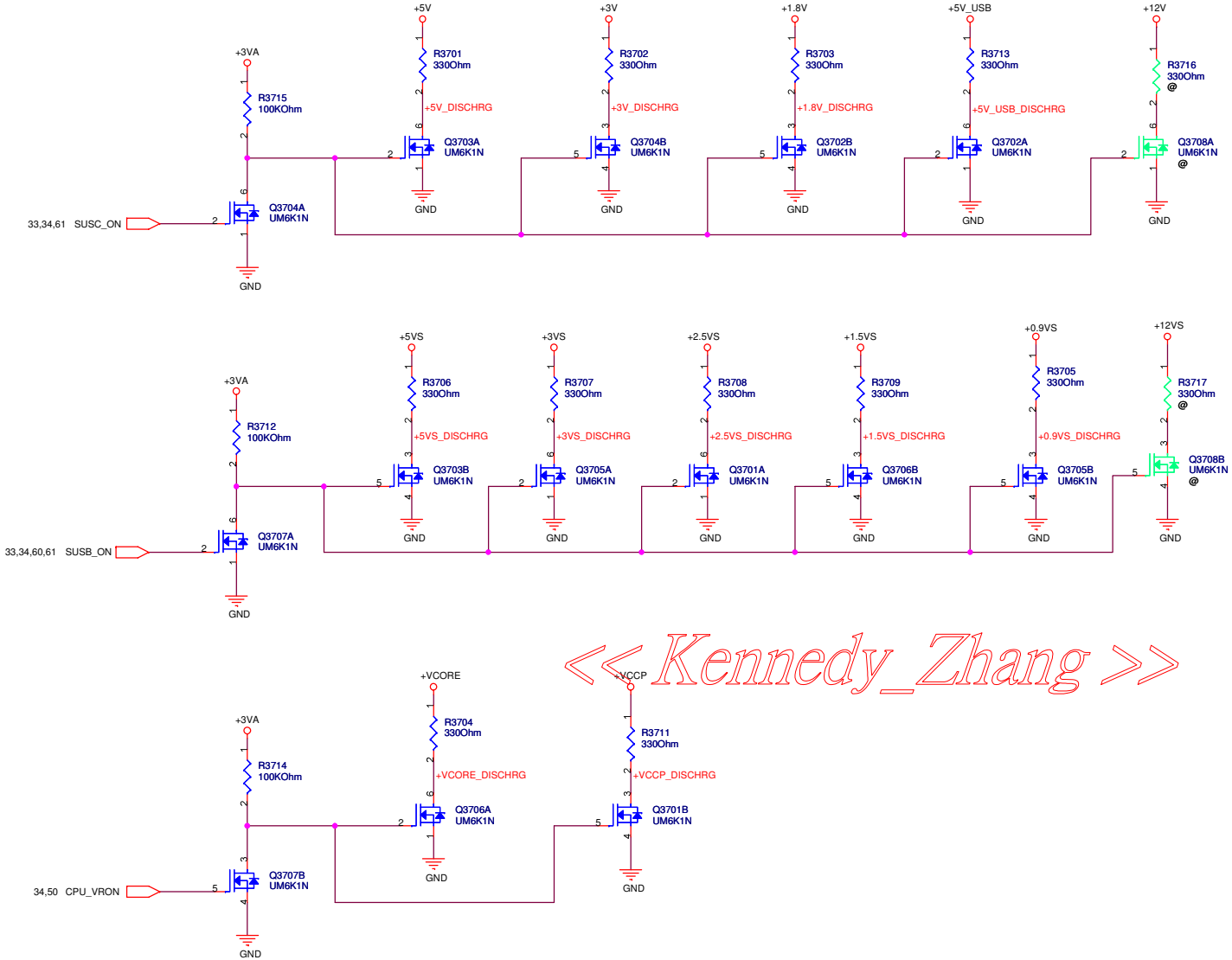
<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA_ROM&KB conn	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 35 of 63	



<Variant Name>

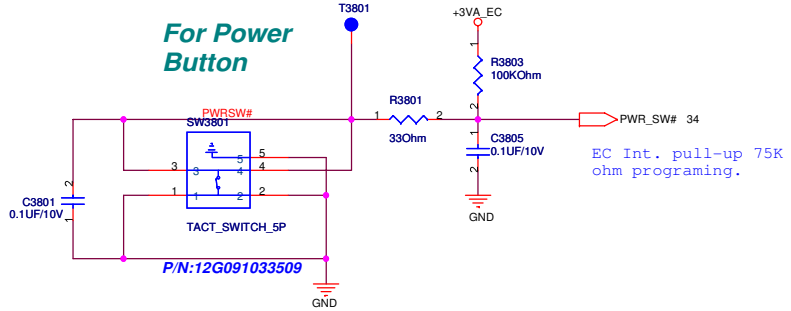
ASUSTeK COMPUTER INC	Title : RTS5117	
	Engineer: Chao-liang_Hung	
Size: C	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 36 of 63	

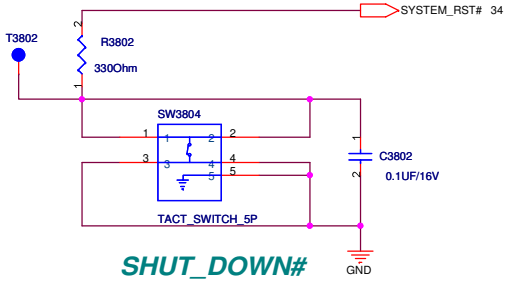


<Variant Name>

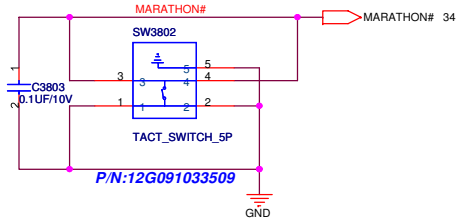
ASUSTeK COMPUTER INC	Title : DISCHARGE	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 37 of 63	

For Power Button

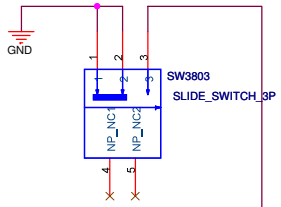




SHUT_DOWN#

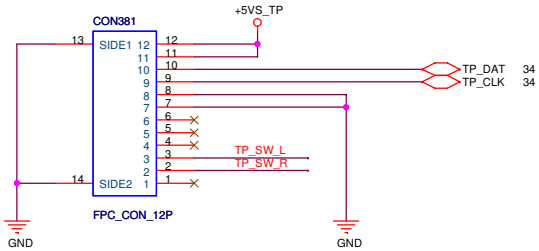


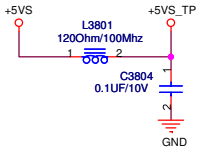
MARATHON#

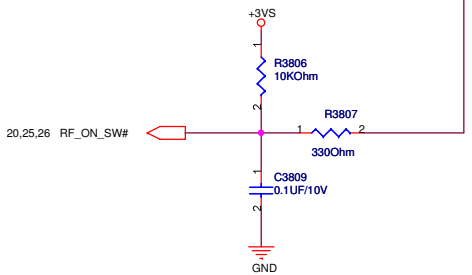


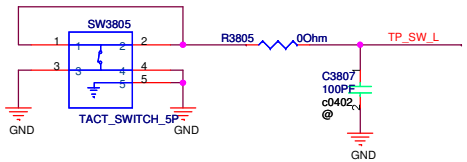
BT/WLAN SW

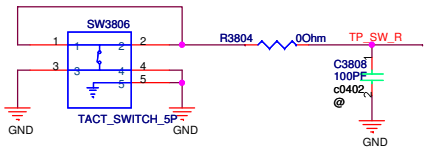
For Touch-Pad







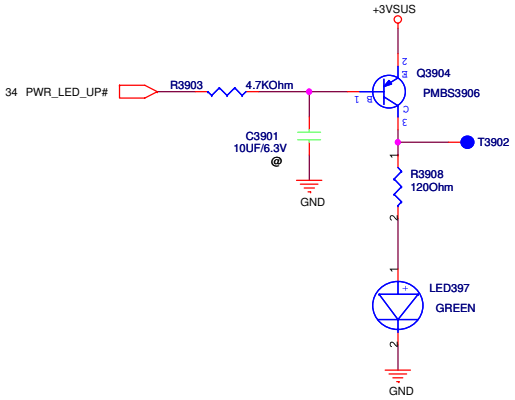




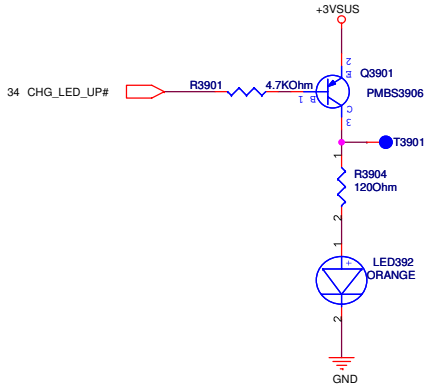
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 38 of 63	

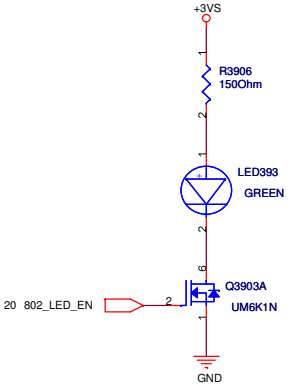
For PWR LED



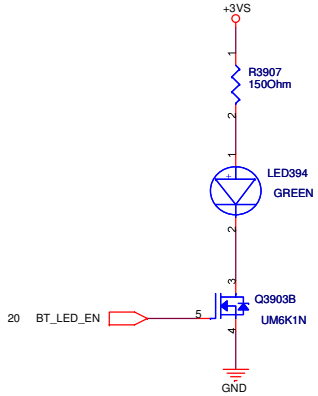
For BATTERY LED



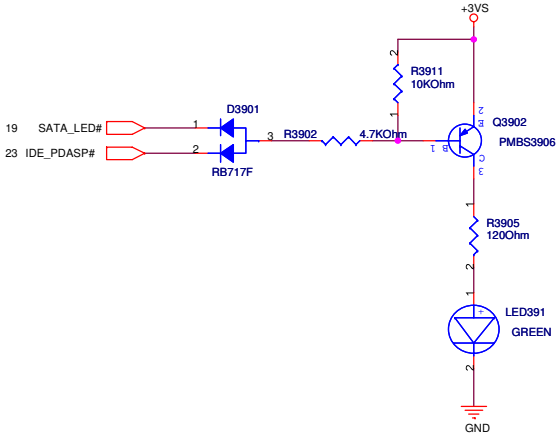
For WireLess LED



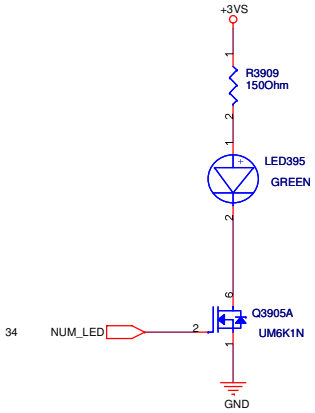
For BT LED



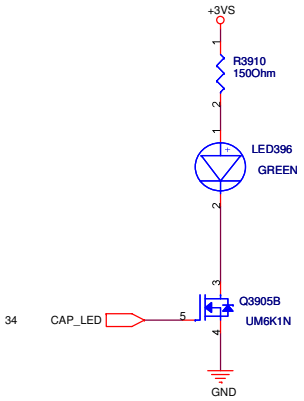
For SATA/IDE LED



For Num Lock



For Cap. Lock



<Variant Name>

ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 39 of 63	

<< Kennedy_Zhang >>

<Variant Name>

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 40 of 63	

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
C	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 41 of 63

<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 42 of 63

<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 43 of 63

<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

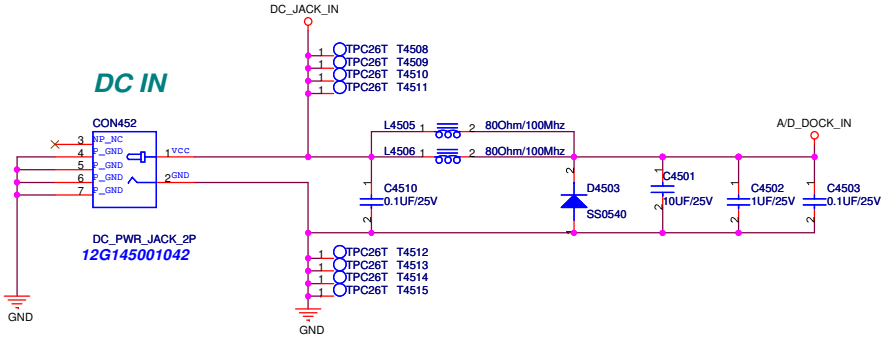
ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 44 of 63

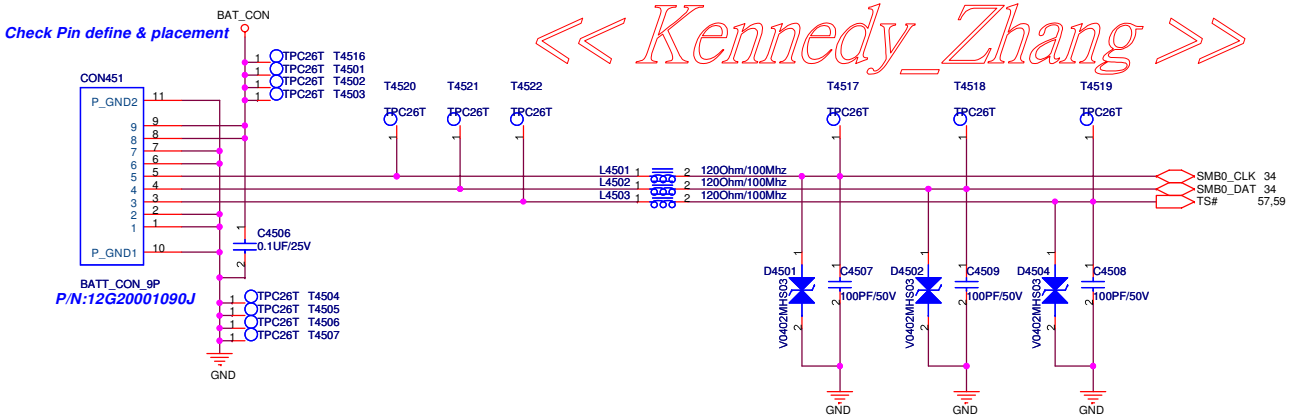
DC IN



BAT IN

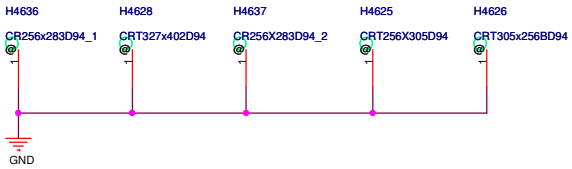
Check Pin define & placement

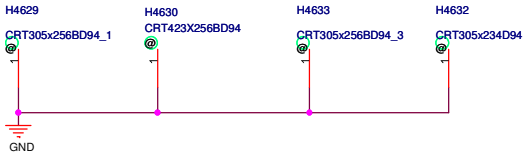
<< Kennedy_Zhang >>

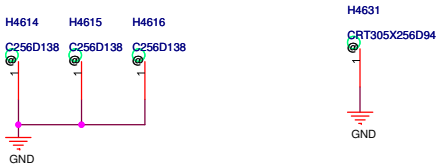


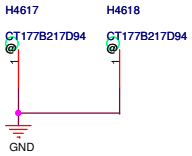
<Variant Name>

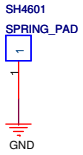
ASUSTeK COMPUTER INC	Title : BAT&Adapter conn	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 45 of 63	

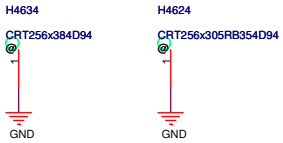


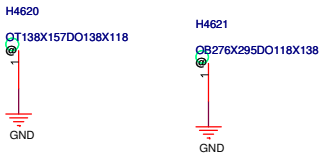












<Variant Name>

ASUSTeK COMPUTER INC

Title : HDD & CDROM

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 46 of 63

<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
C	F9F	2.00

Date: Wednesday, October 04, 2006 Sheet 47 of 63

Rev1.10

1.Page 34: Change R3419 and R3420 from 1.5K to 4.7K ,in order to let the Battery SM Bus can be low enough.

2.Page 6:Change CON601 pin define for FAN.

3.Page26:Change CON261 pin define for I/O Board.

4.Page 34:Add R3438 100K and change C3407 to 2.2U for EC timing request.

5.page 6:Change R608 and R609 from 1.5K to 4.7K ,in order to the meet the EC request

5.page 17:Add F1701 for CCD power over current protection.

6.page 45:Change DC in Jack

7.page 17:Change Inverter and LCD LVDS connector for ME request.

8.page 39:Change LED392 to from green to orange.

9.page 34:Add R3439 and Q3403 for power limit.

10.page 9 & page 11 :Add TV out function.

11.page 33&34 Change PE_DEBUGEN# pull high to +3V ,U3303 power pin to +3V and R3306 to 4.7K.

12.page25:Add power circuit for Finger Printer.

13.page25:Change power circuit for Finger Printer and add P/F_RST#.

14.page12:DNI CE1201 for cost down.

15.page5:DNI CE501 for cost down.

16.page36:Change R3656,R3657,R3658 from 4.7K to 0 ohm ,and DNI U3602 and C3663 for new RTS5117

Rev1.11

17.page7:Swap U701 pin48,49 and pin51,52 pin name.

18.page39:Change LED393,LED394 from bule to green,for Marketing Spec.

Rev1.20

19.Page 35:Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

20.Page 34:DNI R3435 and mount R3408, R3418 for EC_RST#

21.Page 7:Mount R747 for select PEREQ# and add R773 for CLK_REQ_NEWCARD# pull high.

22.Page 15:Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

23.Page 38:Change CON381 from 12G18340120E to 12G18340120K

24.Page 35:Modify circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

25.Page 46:Change screw holes beside H4614,H4615,H4616 for me request.

26.Page 18: Change L1811, L1812, and L1813 from bead to inductor.

27.Page 6:DNI D604 because OS_OC# will shut down the system.

28.Page 17:Remove CCD connectorand add CCD signal to CON175.

Rev1.21

29.Page 17:Change R1703 from 100K to 200K to meet LCD power sequence.

30.Page 6:Modify the Hardware protect circuit.

31.Page 25:DNI Q2503 for BIOS can detect BT during BOOT.

32.Page 20:DNI R2017,R2018,R2019,because no meed PCBA ID.

33.Page 23:Add R2309 and R2310 for IDE select.

34 Page 34:Del Q3403 UM6K1N and add 2N7002 for Q3404, Q3405.

35.Page 6: Change R610 from 100ohm to 200ohm for spec suggestion and reverse C609 1uF decoupling CAP.

36.Page 19: Change R1925,R1926,R1927 and R1928 from 0 ohm to 22 ohm.

37.Page 9: DNI C1831,C1833 and C1833.AND add C903,C904, C905 for 33P and R1103 for EMI request.

38.Page 17: Del D1704 ,add D1075 and change R1703 to 100 ohm to meet LCD power off sequence.

39.Page 7:Change C712 and C713 from 27P to 24P for ITTI request.

40.Page 19:Change C1901 and C1903 from 15P to 12P for ITTI request.

41.Page 36:Change C3655 and C3656 from 15P to 18P for ITTI request.

42.Page 6:Add R617 and Q605 for OS_OC#,to keep the U3403 pin5 voltage can meet RN5VD27CA request.

43.Page 25:Add C2512 and mount D2503 for EMI request.

Rev2.00

44.Page 39:Change R3904,R3905 and R3908 to 120 ohm, change R3906,R3907,R3909and R2910 to 150 ohm to control LED current is about 10mA.

45.Page 34:Del R3408and add D3402 for the OS# OC function.

46.Page 20:Add R2038 10K for GPIO10 pull high and R2039 10K for GPIO25 pull high.

47.Page 46:Change H4626 and H4630.

48.Page 36:Del CON361 and add CON362 ALPS/SCDE1C0200

49.Page 25:Change C2510 from 0.1U to 1U to meet SI9183DT spec.

50.Page 21:Change USB external ports for controller0.

51.Page 25:Change C2502 from 0.1U to 10U for EMI request.

52.Page 46:ADD S4601 spring for EMI.

53.Page 18:Change TV out pi filter for EMI request.

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer: Chao-liang_Hung	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Thursday, October 05, 2006	Sheet 48 of 63	

<< Kennedy_Zhang >>

<Variant Name>

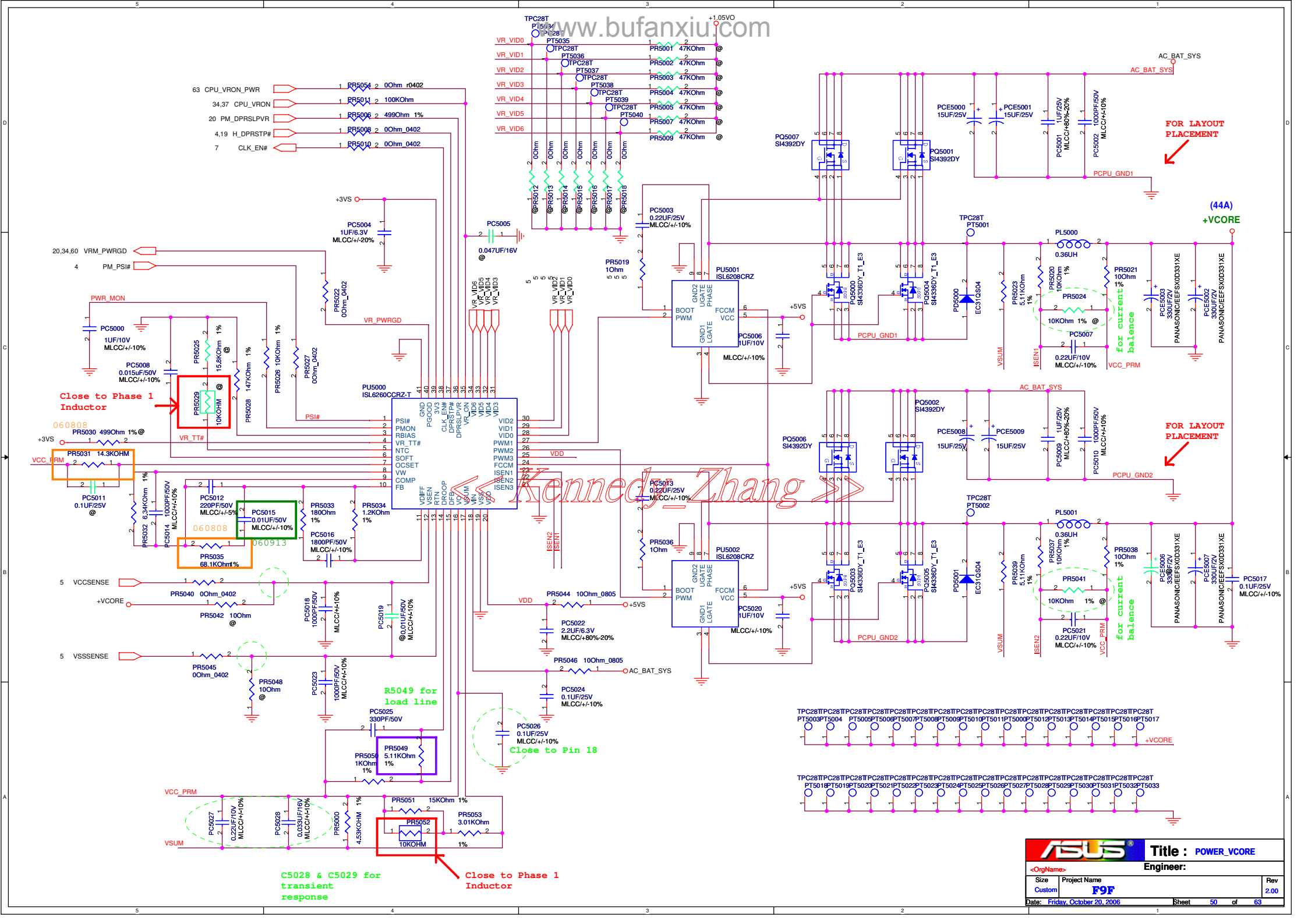
Title : History(2)

ASUSTeK COMPUTER INC

Engineer: Chao-liang_Hung

Size	Project Name	Rev
Custom	F9F	2.00

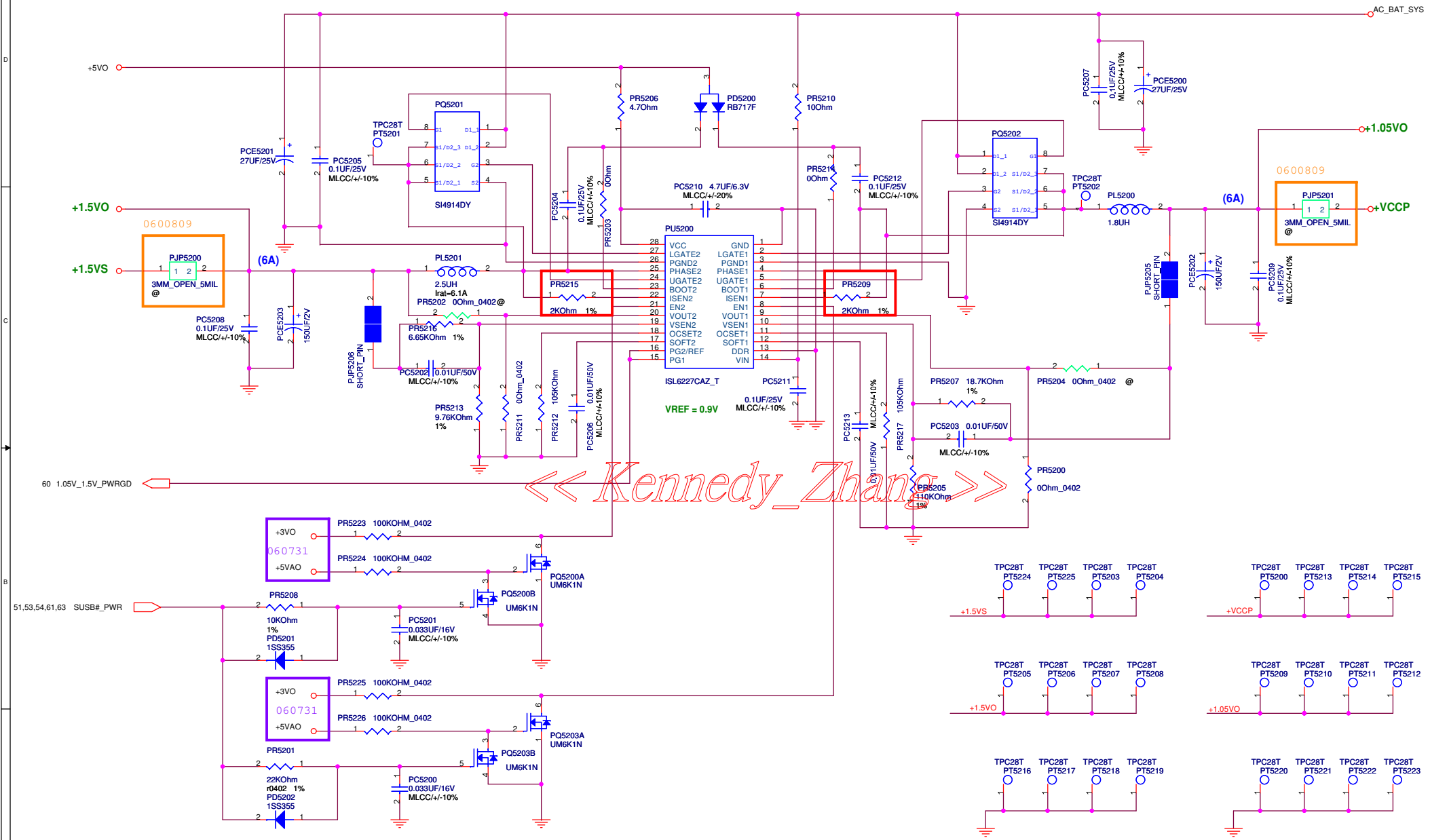
Date: Wednesday, October 04, 2006 Sheet 49 of 63


www.bufanxiu.com
<Kennedy_Zhang>
(44A)
+VCORE
FOR LAYOUT PLACEMENT
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
for current balence
Title : POWER_VCORE
Engineer:
Project Name F9F
Rev 2.00
Date: Friday, October 20, 2006
Sheet 50 of 63

PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)

+12VSUS

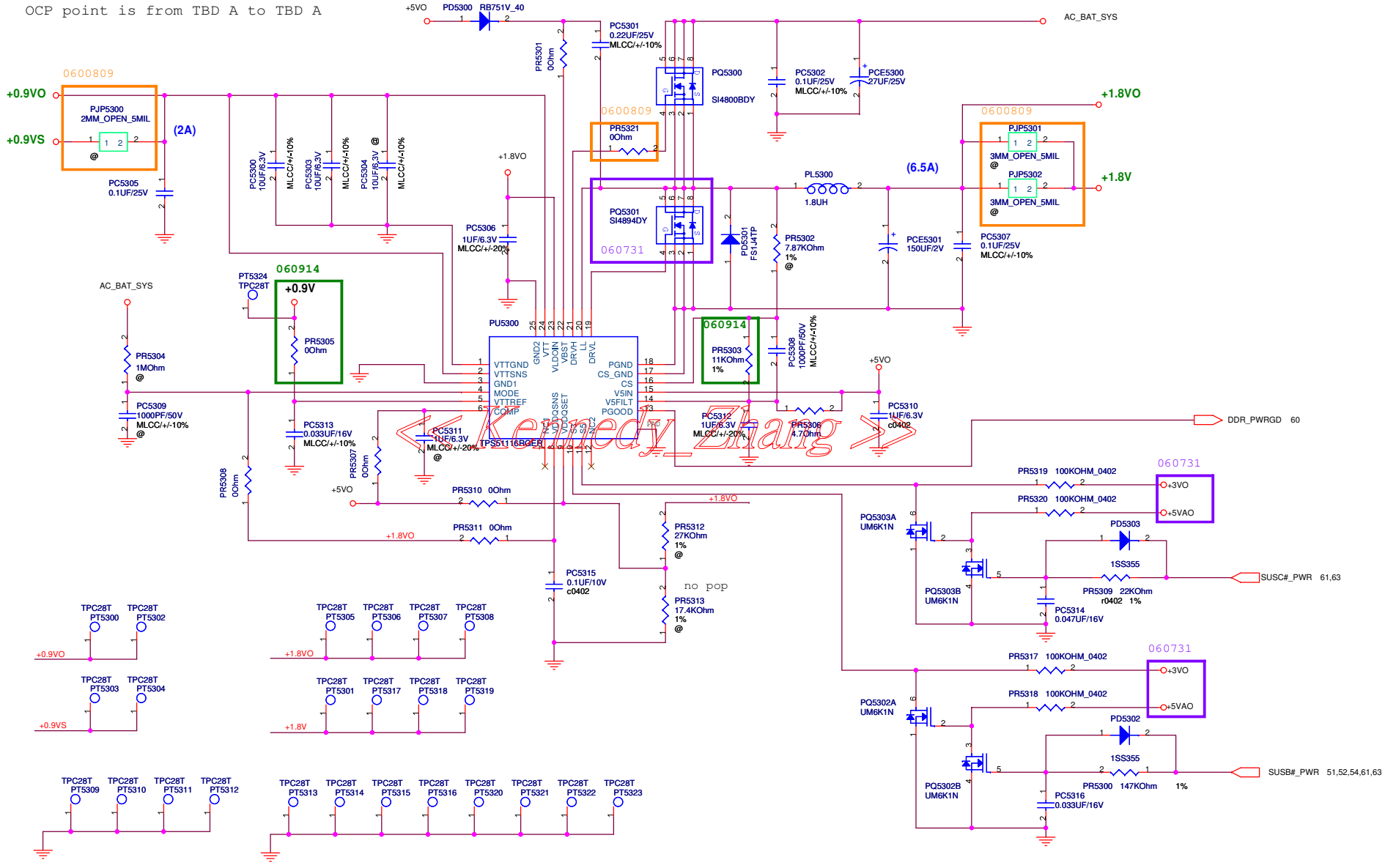
Title :	POWER_SYSTEM
<OrgName>	Engineer:
Size: Custom	Project Name: F9F
Rev: 2.00	
Date: Wednesday, October 04, 2006	Sheet 51 of 63



ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
Date: Wednesday, October 04, 2006	Sheet 52 of 63	

.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A

1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A



ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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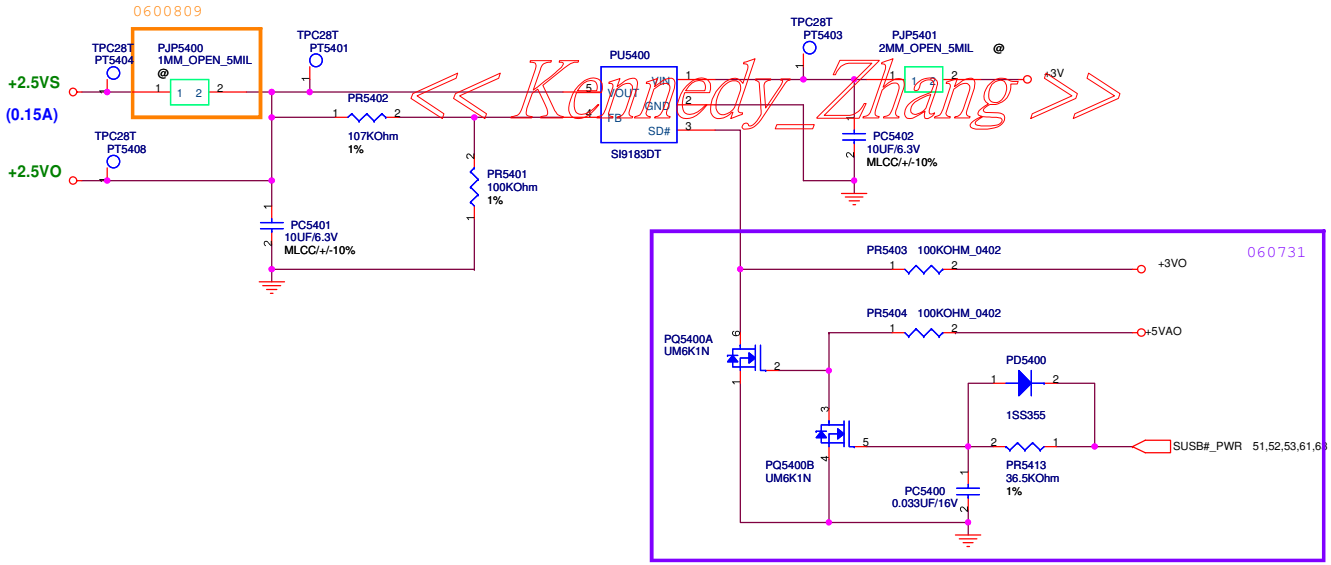
+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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ASUS	Title : EMPTY		
<OrgName>	Engineer:		
Size: Custom	Project Name: F9F		Rev: 2.00
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ASUS	Title : EMPTY	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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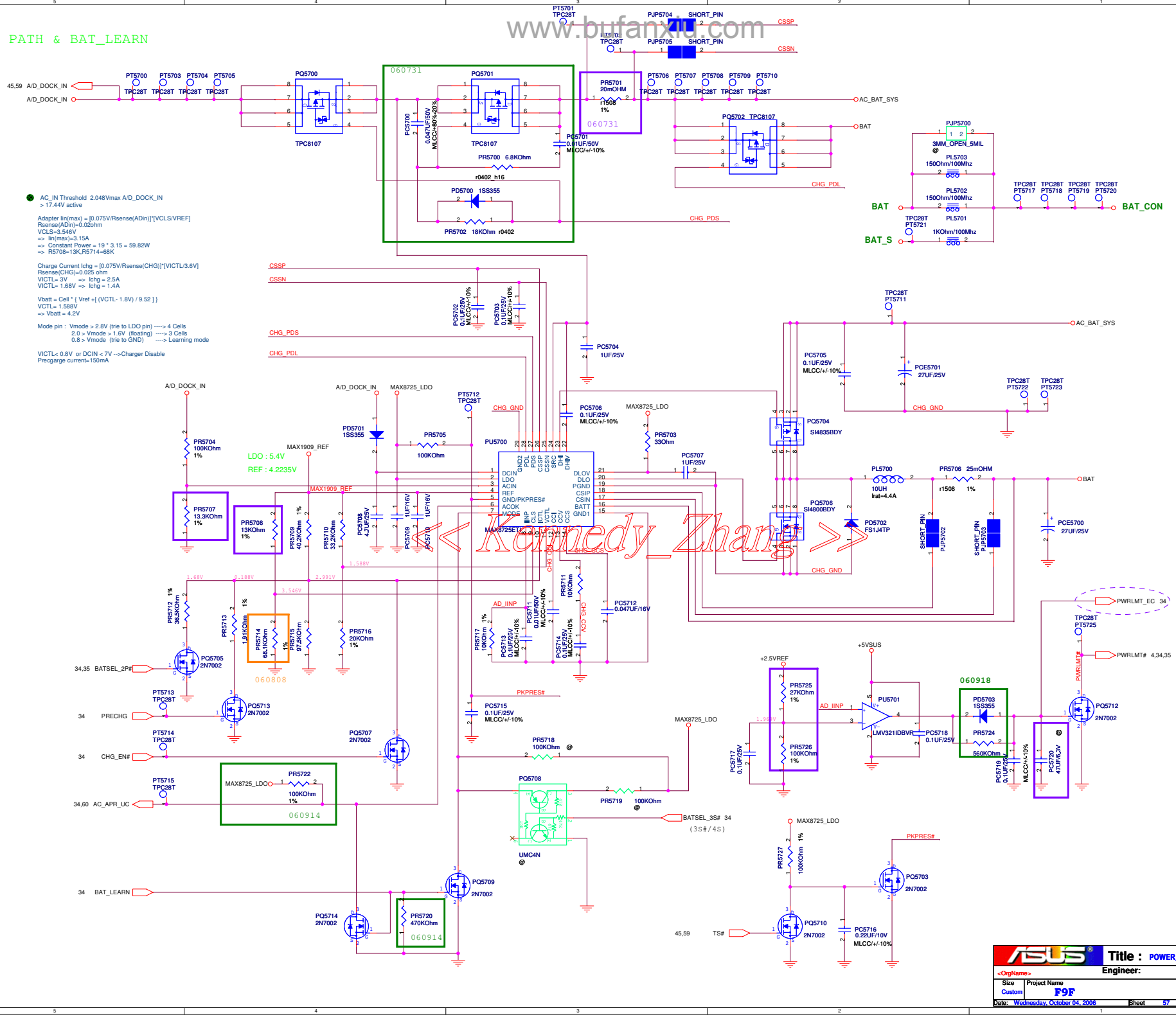
POWER PATH & BAT_LEARN



<< Kennedy_Zhang >>

ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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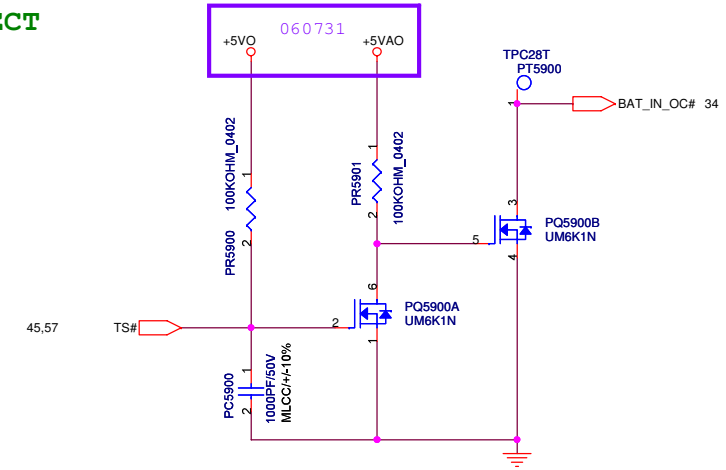
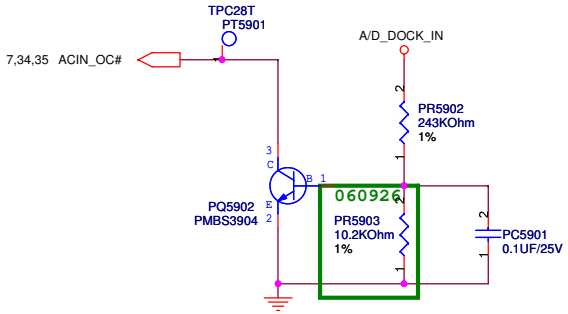
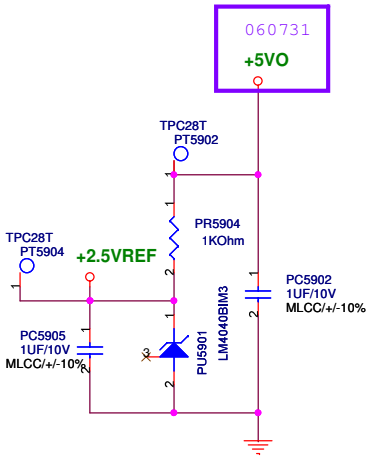
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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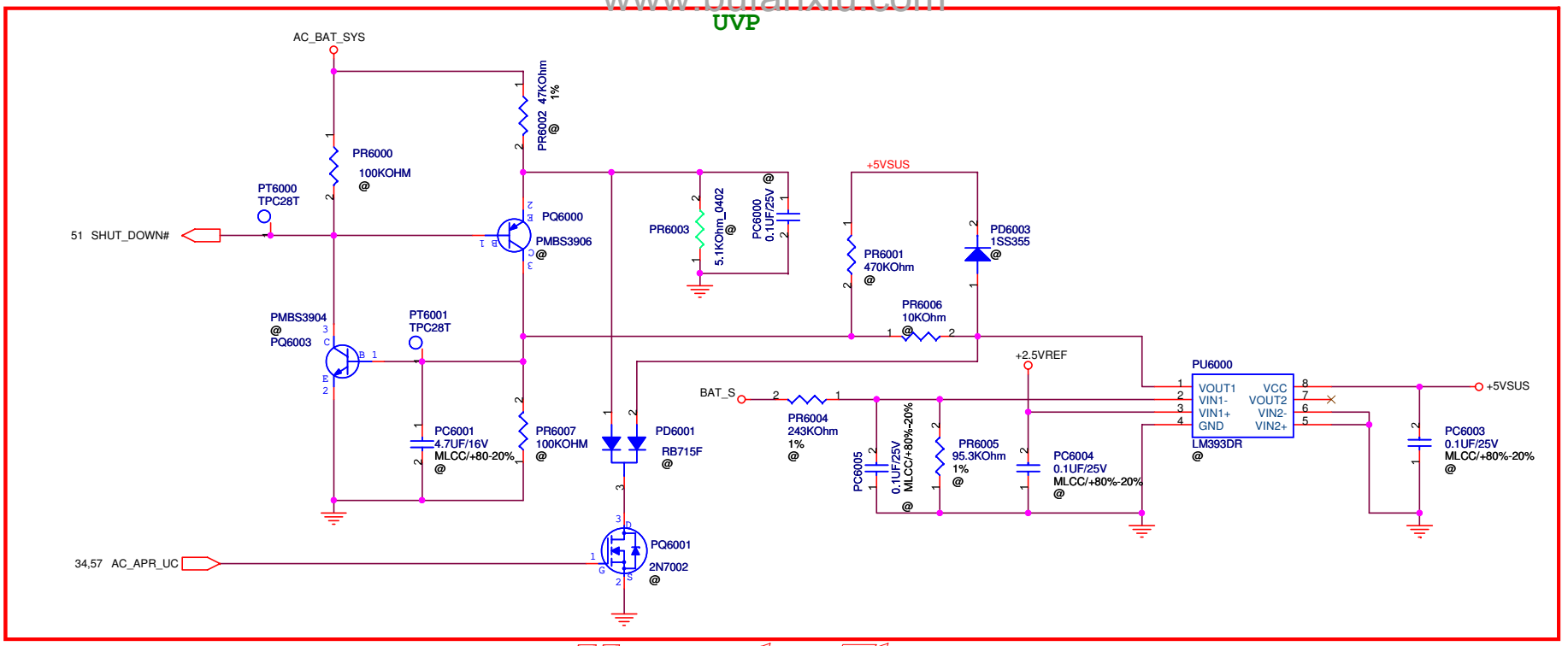
UVP



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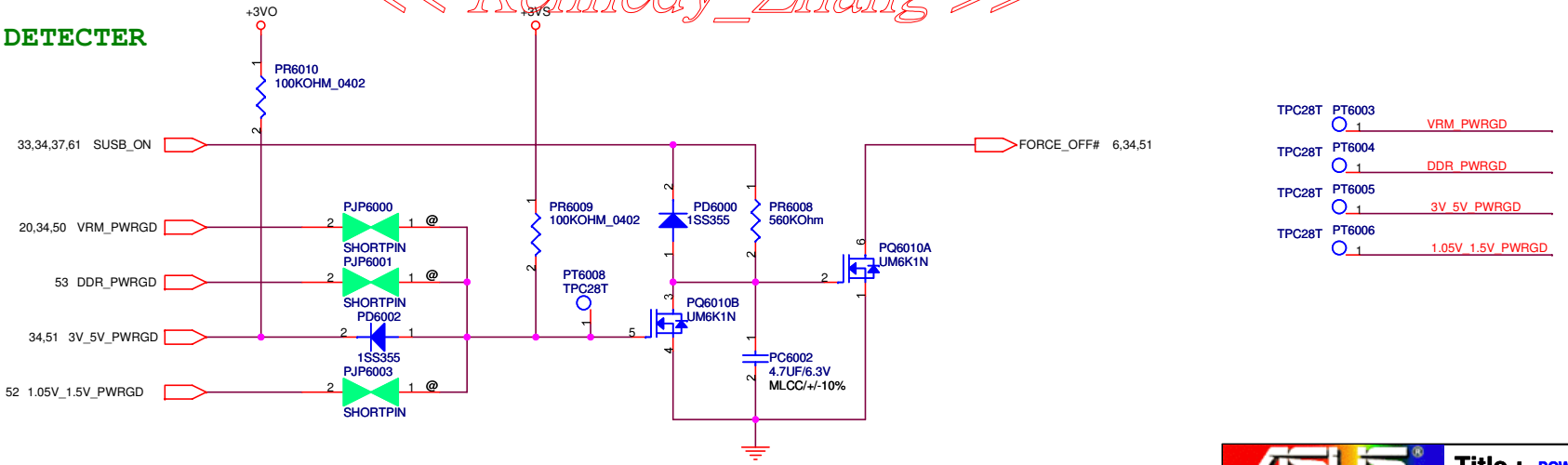
POWER GOOD DETECTER



Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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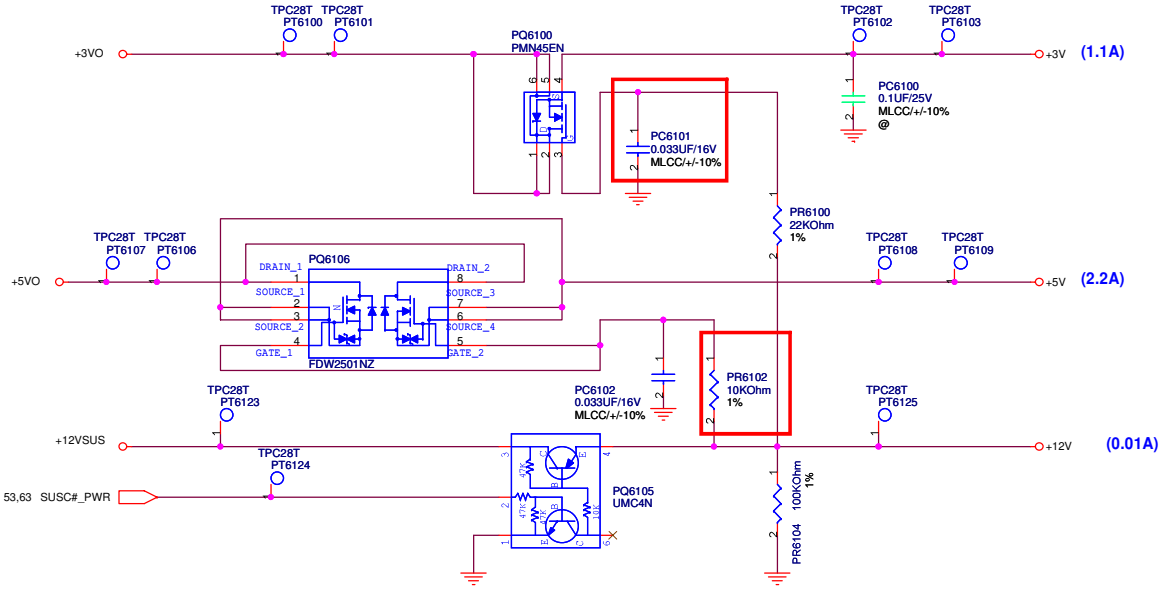
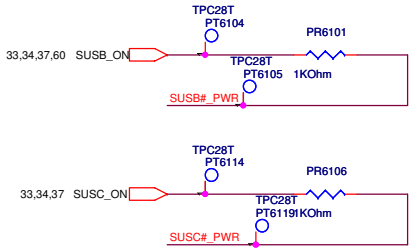
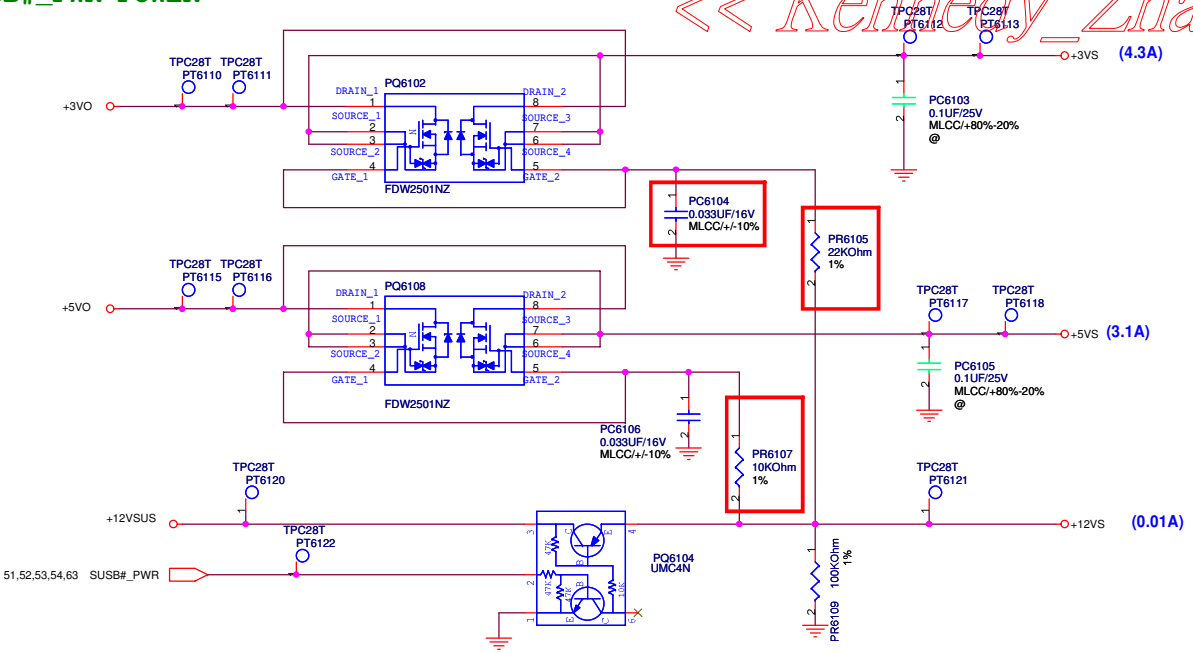
SUSC#_PWR POWER





SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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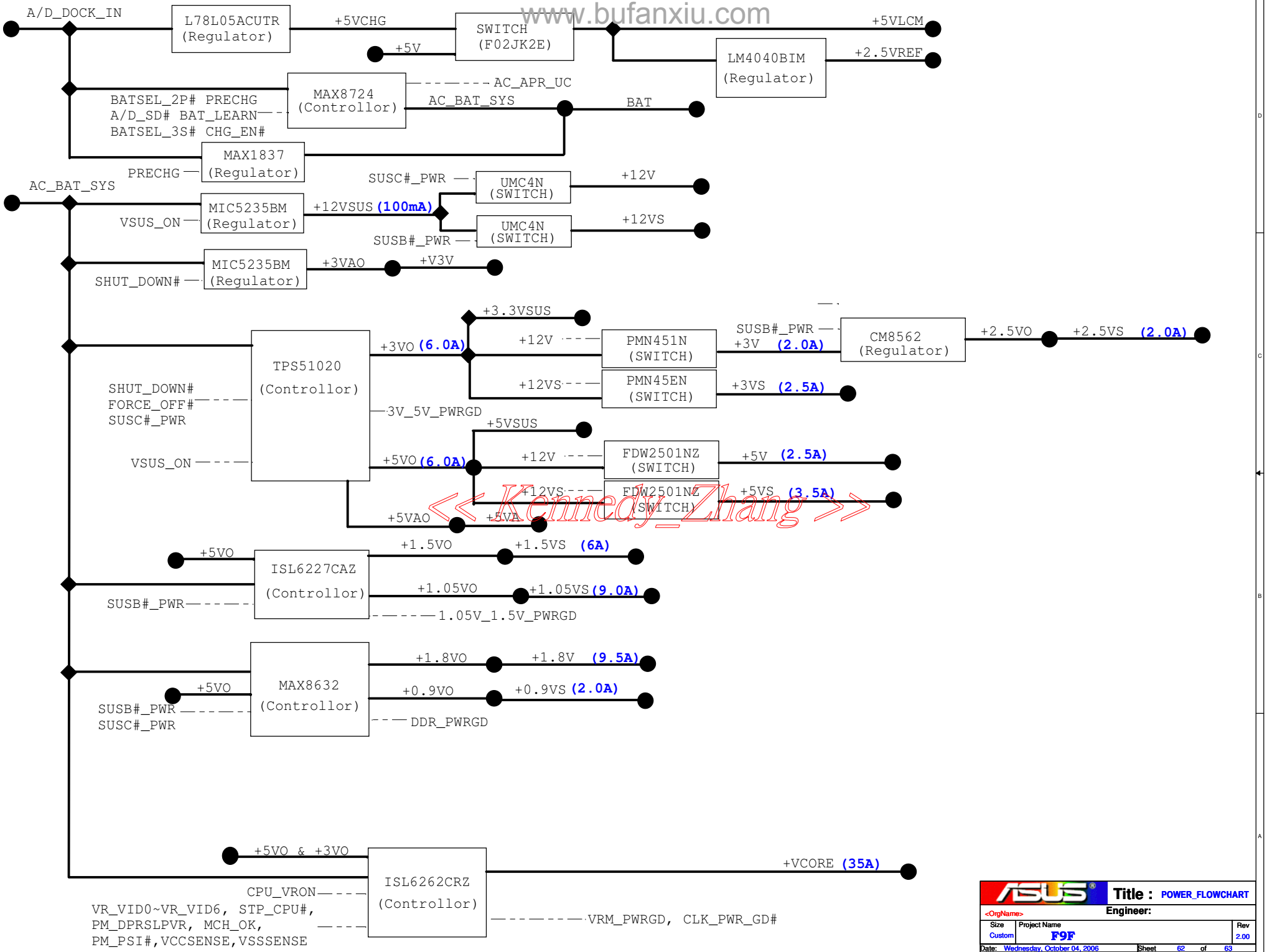

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9F	Rev: 2.00
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AC_BAT_SYS → AC_BAT_SYS 17,50,51,52,53,57,60
+3VA → +3VA 17,19,34,37,51
+5VA → +5VA 6,51
+5VO → +5VO 51,52,53,59,61
+3VO → +3VO 51,52,53,54,60,61
+3VSUS → +3VSUS 17,20,21,22,26,29,39,51
+5VSUS → +5VSUS 22,51,57,60
+3V → +3V 21,25,26,33,35,37,54,61
+3VS → +3VS 6,7,9,11,13,14,15,17,18,20,22,23,25,26,29,33,34,37,38,39,50,60,61

+12VSUS → +12VSUS 51,61
+12V → +12V 24,26,37,61
+12VS → +12VS 17,37,61

+5V → +5V 6,17,24,33,36,37,61
+5VS → +5VS 6,18,22,23,25,26,34,37,38,50,61

+2.5VO → +2.5VO 54
+2.5VS → +2.5VS 11,37,54
+1.8VO → +1.8VO 53
+1.8V → +1.8V 9,12,14,15,37,53

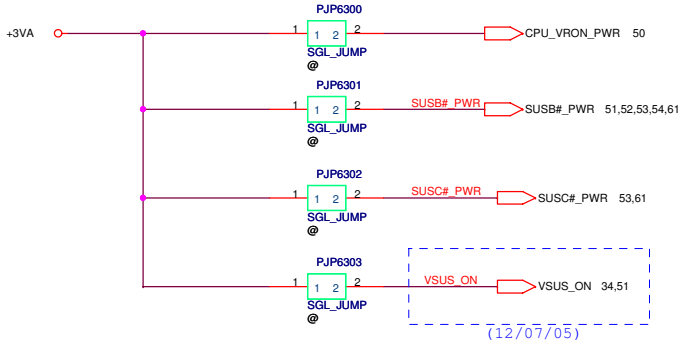
+VCCP → +VCCP 5,12,22,37,52

+0.9VS → +0.9VS 16,37,53
BAT → BAT 57

+2.5VREF → +2.5VREF 57,59,60
+VCORE → +VCORE 5,37,50

BAT_CON → BAT_CON 45,57

FOR POWER TEST



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ASUS	Title : POWER_SIGNAL		
<OrgName>	Engineer:		
Size: Custom	Project Name: F9F		Rev: 2.00
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