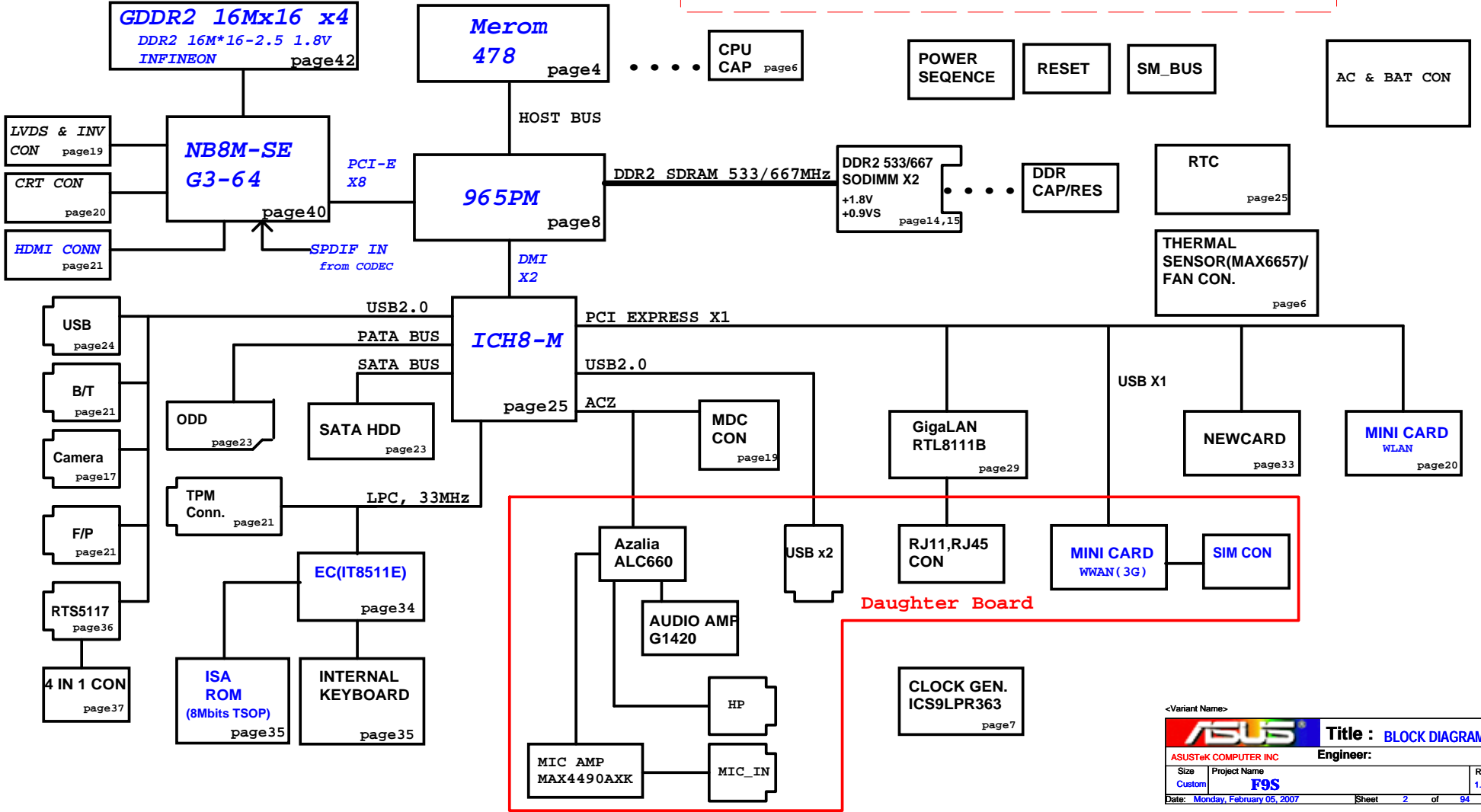
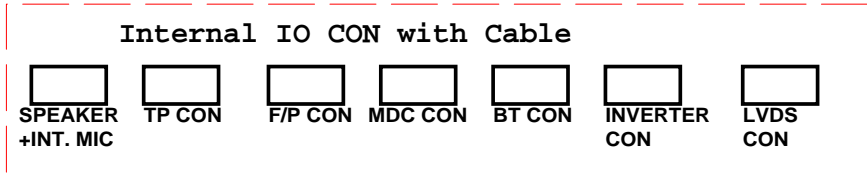
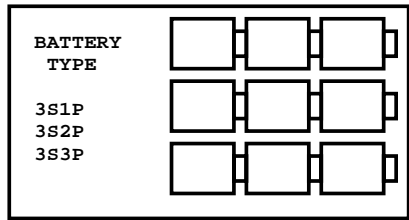


www.bufanxiu.com
F9S BLOCK DIAGRAM



ASUS		Title : BLOCK DIAGRAM	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9S	Rev 1.1	
Date: Monday, February 05, 2007	Sheet 2 of 94		

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	PWRLIMIT#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	
31	ECSCH#/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	GIN7/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/O
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APPR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPIO	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

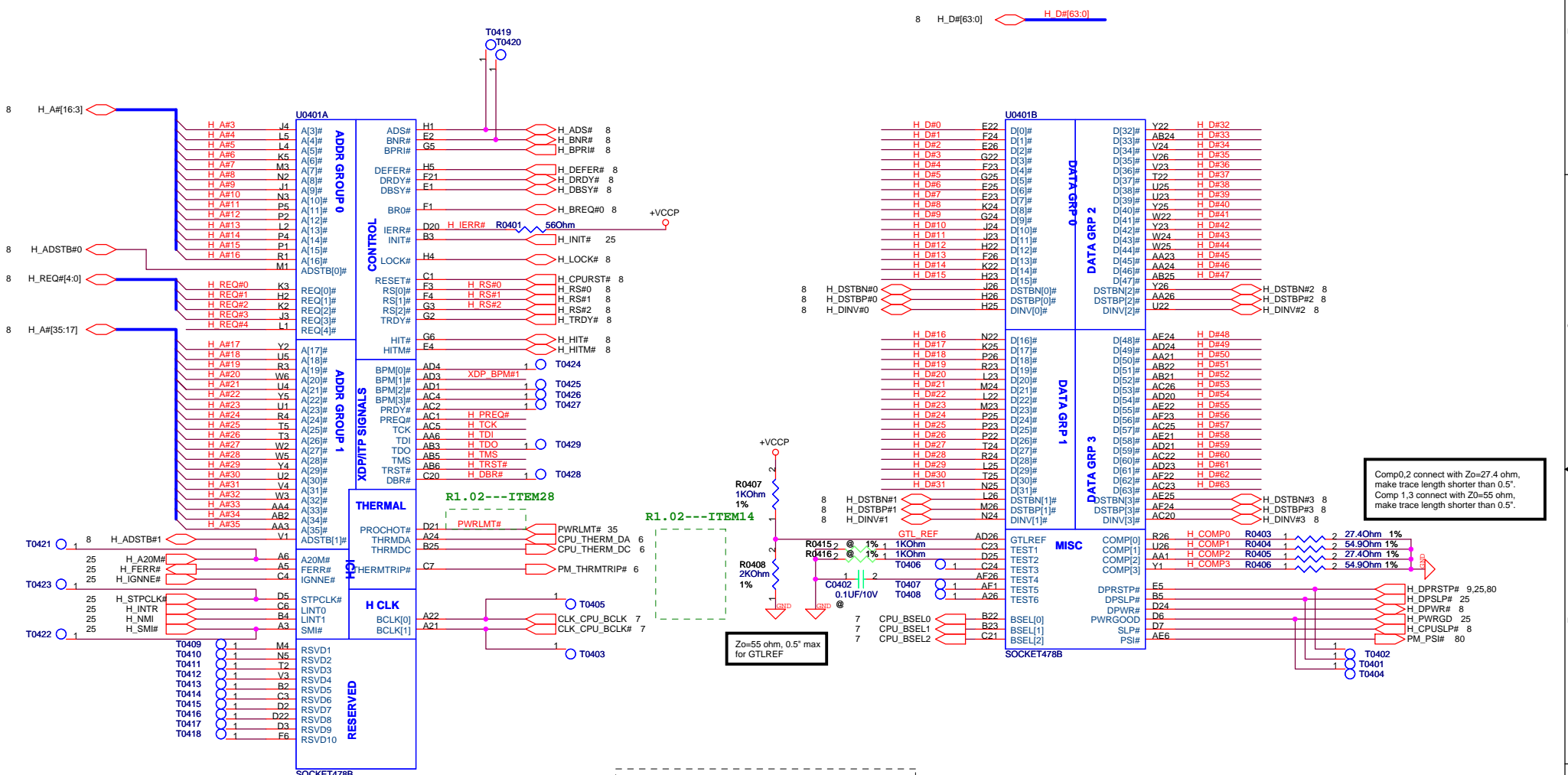
ICH8M_GPIO

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i 0	GPI	BT_DET#	+3VS	FACH1
GPIO [5:2]	i ^{H-Z}	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i 0	GPO	BIOS_REC_?_(TP)	+3VS	FACH2
GPIO 07	i 0	GPO	802_LED_EN	+3VS	FACH3
GPIO 08	i	GPI	EXTSM#	+3VSUS	N/A
GPIO 09	i ^{H-Z}	GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i ^{H-Z}	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat ^{H-Z}	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SC#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i ^{H-Z}	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat 1	Native	STP_PC#	+3VSUS	STP_PC# , No-GPIO in Mobile
GPIO 16	Nat 0	Native	PM DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i 1	GPO	WLAN_ON#	+3VS	FACH0
GPIO 18	O ^{freq}	GPO	N/A	+3VS	N/A
GPIO 19	i ^{HK}	GPO	CPU_SELECT	+3VS	SATA0P
GPIO 20	O 1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat	Native	N/A	+3VS	LDRQ1#
GPIO 24	O ^{H-Z}	GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED) , Not Cleared by CF9h RST event.
GPIO 25	Nat 1	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO in Mobile
GPIO 26	Nat	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O 0	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O 0	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O 0	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO in Mobile
GPIO 33	O 1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O 0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O 0	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i 0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	Use As	Signal Name	Power	Mux
GPIO 39	i	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a	N/A	N/A	N/A	No implement
GPIO 48	i 1	Native		+3VS	SDATAOUT1
GPIO 49	Nat	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat 1	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat 1	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat 1	Native	PCI_GNT3#	+3VS	GNT3#

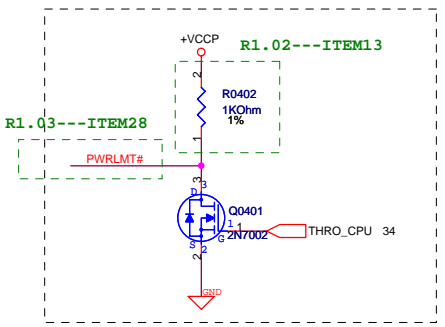
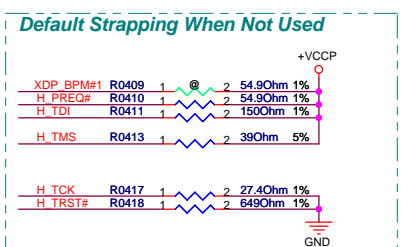
<Variant Name>

		Title : Schematic Info.	
ASUSTeK COMPUTER INC		Engineer: <OrgAddri>	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Monday, February 05, 2007	Sheet	3	of 94



Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp 1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Zo=55 ohm, 0.5" max for GTLREF



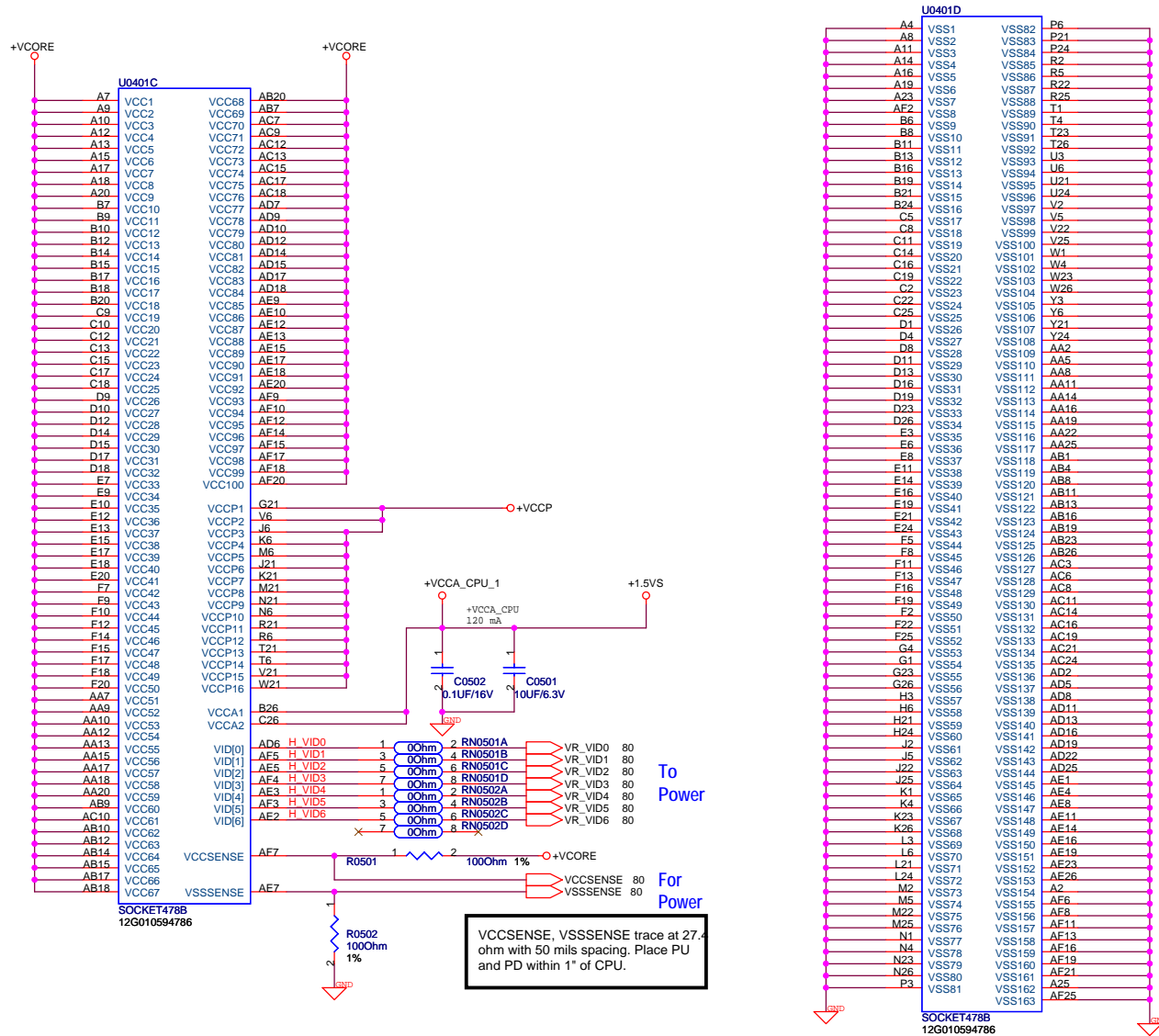
<Variant Name>

ASUS Title : **MEROM.CPU (1)**

ASUSTek COMPUTER INC Engineer: <OrgAddr>

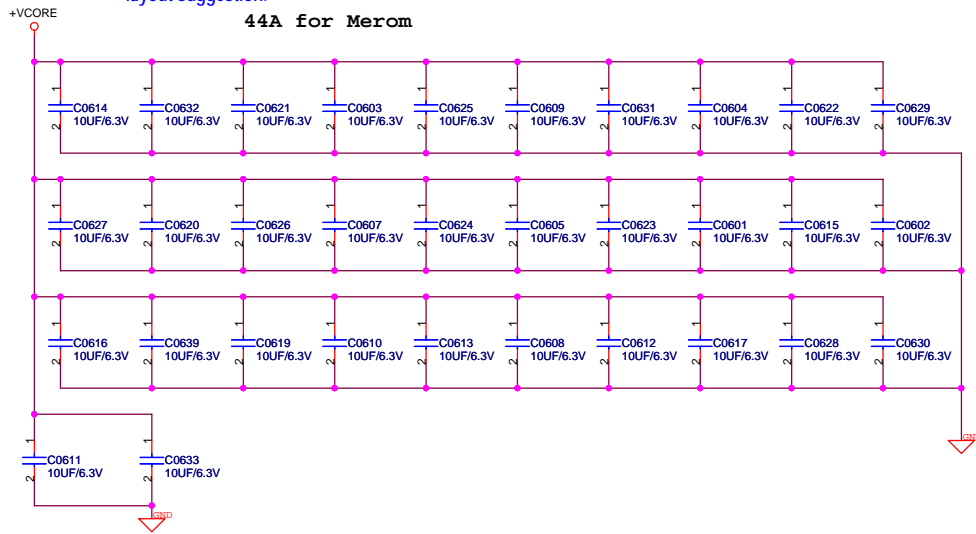
Size	Project Name	Rev
Custom	F9S	1.1

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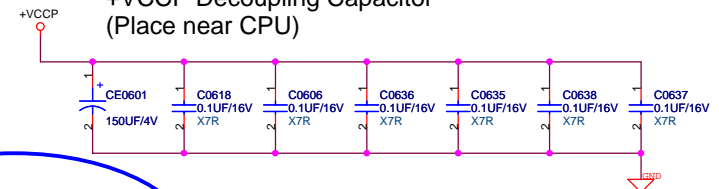


Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom



+VCCP Decoupling Capacitor (Place near CPU)

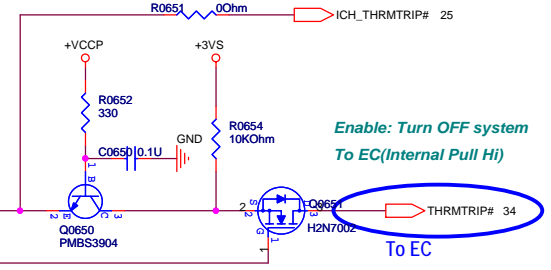


Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it !_0907

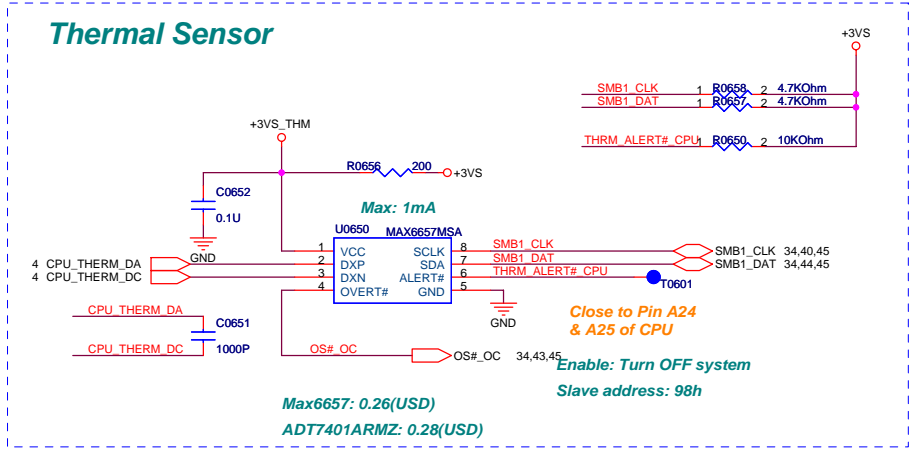
Sub-SYS=CPU CAP



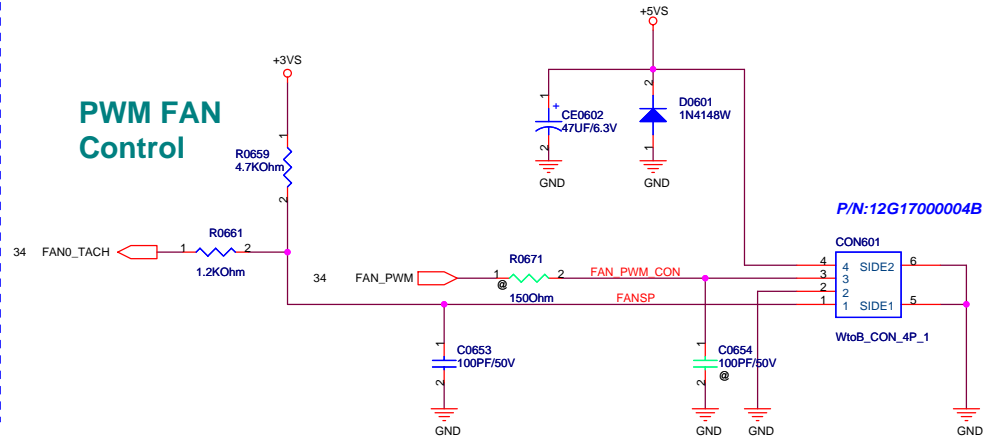
Enable: Turn OFF system To EC (Internal Pull Hi)

To EC

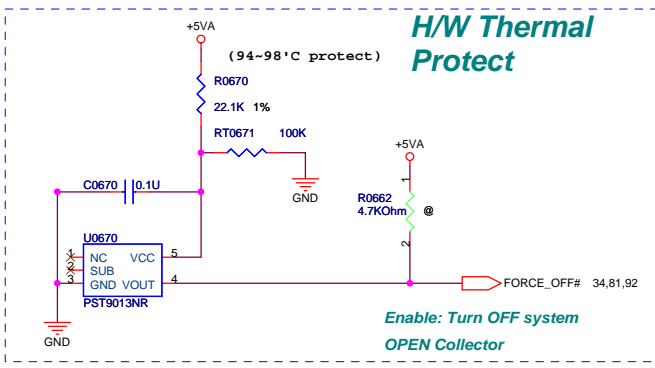
Thermal Sensor



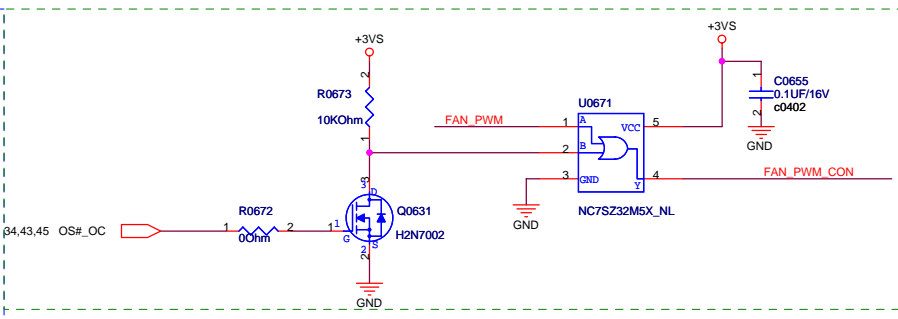
PWM FAN Control



H/W Thermal Protect

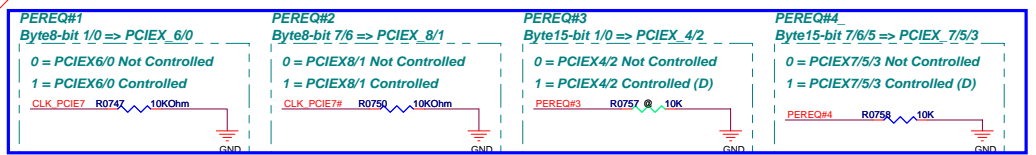
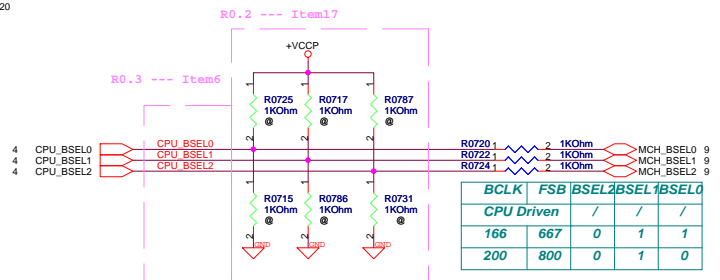
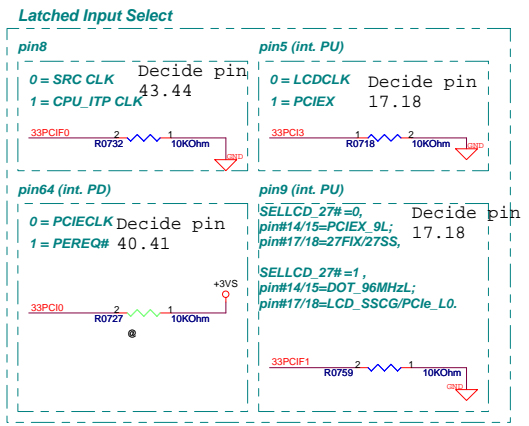
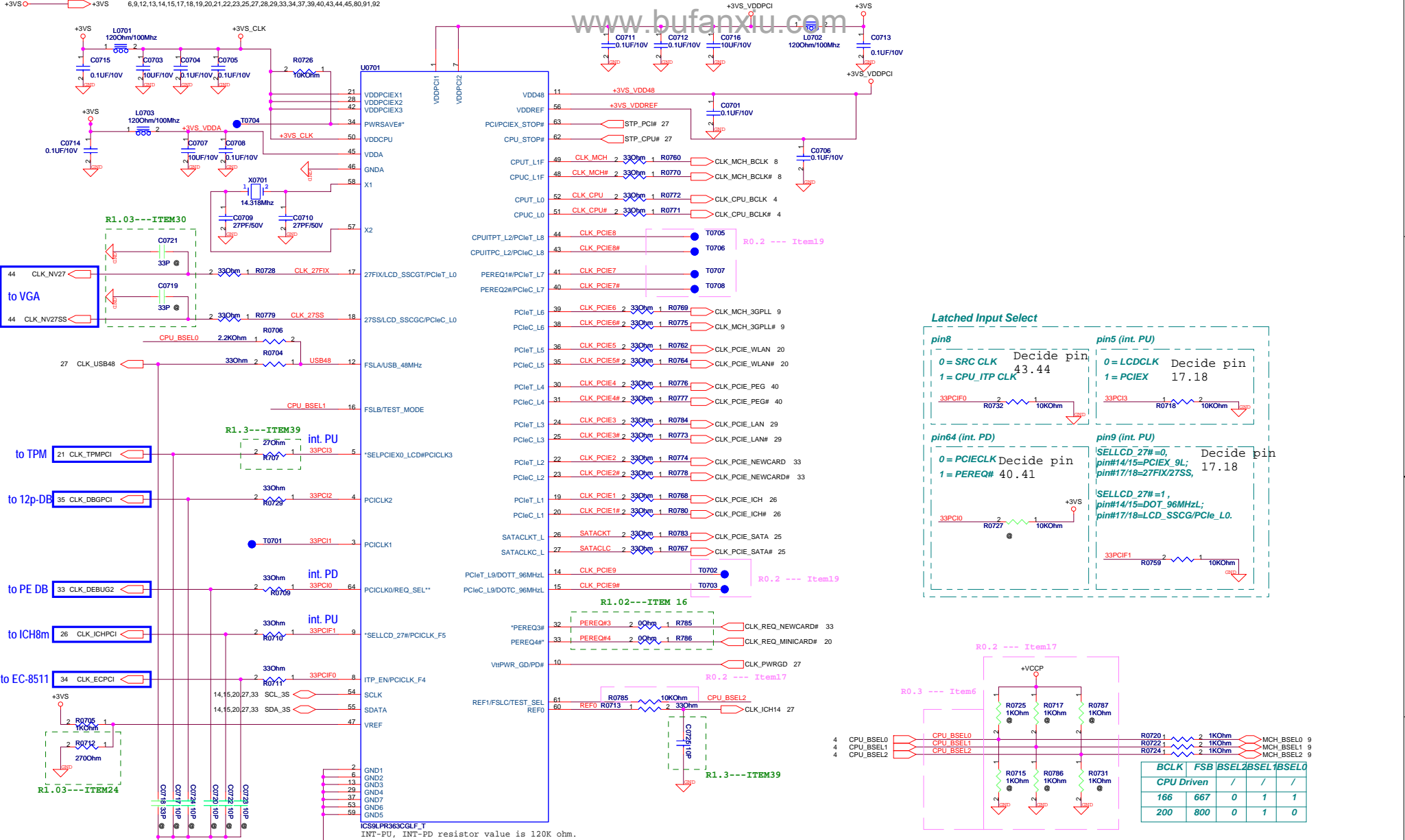


R1.02---ITEM12



<Variant Name>

ASUS		Title : CPU CAP, Thermal,FAN_CTRL	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name F9S	Rev 1.1	
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4 H_D#[63:0] H_D#[63:0]

4 H_A#[35:3] H_A#[35:3]

U0801A

H_D#0	E2	H_D#_0	H_A#_3
H_D#1	G2	H_D#_1	H_A#_4
H_D#2	G7	H_D#_2	H_A#_5
H_D#3	M6	H_D#_3	H_A#_6
H_D#4	H7	H_D#_4	H_A#_7
H_D#5	H3	H_D#_5	H_A#_8
H_D#6	G4	H_D#_6	H_A#_9
H_D#7	F3	H_D#_7	H_A#_10
H_D#8	N8	H_D#_8	H_A#_11
H_D#9	H2	H_D#_9	H_A#_12
H_D#10	M10	H_D#_10	H_A#_13
H_D#11	N9	H_D#_11	H_A#_14
H_D#12	N12	H_D#_12	H_A#_15
H_D#13	H5	H_D#_13	H_A#_16
H_D#14	P13	H_D#_14	H_A#_17
H_D#15	K9	H_D#_15	H_A#_18
H_D#16	M2	H_D#_16	H_A#_19
H_D#17	W10	H_D#_17	H_A#_20
H_D#18	Y4	H_D#_18	H_A#_21
H_D#19	V4	H_D#_19	H_A#_22
H_D#20	M3	H_D#_20	H_A#_23
H_D#21	J1	H_D#_21	H_A#_24
H_D#22	N5	H_D#_22	H_A#_25
H_D#23	N3	H_D#_23	H_A#_26
H_D#24	W6	H_D#_24	H_A#_27
H_D#25	W9	H_D#_25	H_A#_28
H_D#26	Y7	H_D#_26	H_A#_29
H_D#27	Y7	H_D#_27	H_A#_30
H_D#28	Y9	H_D#_28	H_A#_31
H_D#29	P4	H_D#_29	H_A#_32
H_D#30	W3	H_D#_30	H_A#_33
H_D#31	N1	H_D#_31	H_A#_34
H_D#32	AD12	H_D#_32	H_A#_35
H_D#33	AE3	H_D#_33	
H_D#34	AD9	H_D#_34	H_ADS#
H_D#35	AC9	H_D#_35	H_ADSTB#0
H_D#36	AC7	H_D#_36	H_ADSTB#1
H_D#37	AC14	H_D#_37	H_BNR#
H_D#38	AD11	H_D#_38	H_BPRI#
H_D#39	AC11	H_D#_39	H_BREQ#0
H_D#40	AB2	H_D#_40	H_DEFER#
H_D#41	AD7	H_D#_41	H_DBSY#
H_D#42	AB1	H_D#_42	HPLL_CLK
H_D#43	Y3	H_D#_43	H_DPWR#
H_D#44	AC6	H_D#_44	H_DRDY#
H_D#45	AC5	H_D#_45	H_HIT#
H_D#46	AG3	H_D#_46	H_HITM#
H_D#47	AJ9	H_D#_47	H_LOCK#
H_D#48	AH8	H_D#_48	H_TRDY#
H_D#49	AJ14	H_D#_49	
H_D#50	AE9	H_D#_50	
H_D#51	AH12	H_D#_51	
H_D#52	AJ5	H_D#_52	
H_D#53	AH5	H_D#_53	
H_D#54	AJ6	H_D#_54	
H_D#55	AE7	H_D#_55	
H_D#56	AJ7	H_D#_56	
H_D#57	AJ2	H_D#_57	
H_D#58	AE5	H_D#_58	
H_D#59	AJ3	H_D#_59	
H_D#60	AH2	H_D#_60	
H_D#61	AH2	H_D#_61	
H_D#62	AH2	H_D#_62	
H_D#63	AH13	H_D#_63	

HOST

H_ADS#	G12	H_ADS#	H_ADS#_4
H_ADSTB#_0	H17	H_ADSTB#0	H_ADSTB#0_4
H_ADSTB#_1	G20	H_ADSTB#1	H_ADSTB#1_4
H_BNR#	C8	H_BNR#	H_BNR#_4
H_BPRI#	E8	H_BPRI#	H_BPRI#_4
H_BREQ#0	F12	H_BREQ#0	H_BREQ#0_4
H_DEFER#	D6	H_DEFER#	H_DEFER#_4
H_DBSY#	C10	H_DBSY#	H_DBSY#_4
HPLL_CLK	AM5		CLK_MCH_BCLK#_7
H_DPWR#	AM7	H_DPWR#	CLK_MCH_BCLK#_7
H_DRDY#	H8	H_DRDY#	H_DRDY#_4
H_HIT#	K7	H_HIT#	H_HIT#_4
H_HITM#	E4	H_HITM#	H_HITM#_4
H_LOCK#	C6	H_LOCK#	H_LOCK#_4
H_TRDY#	G10	H_TRDY#	H_TRDY#_4

H_DIN#_0	K5	H_DIN#0	H_DIN#0_4
H_DIN#_1	L2	H_DIN#1	H_DIN#1_4
H_DIN#_2	AD13	H_DIN#2	H_DIN#2_4
H_DIN#_3	AE13	H_DIN#3	H_DIN#3_4
H_DSTB#_0	M7	H_DSTB#0	H_DSTB#0_4
H_DSTB#_1	K3	H_DSTB#1	H_DSTB#1_4
H_DSTB#_2	AD2	H_DSTB#2	H_DSTB#2_4
H_DSTB#_3	AH11	H_DSTB#3	H_DSTB#3_4
H_DSTBP#_0	L7	H_DSTBP#0	H_DSTBP#0_4
H_DSTBP#_1	K2	H_DSTBP#1	H_DSTBP#1_4
H_DSTBP#_2	AC2	H_DSTBP#2	H_DSTBP#2_4
H_DSTBP#_3	AJ10	H_DSTBP#3	H_DSTBP#3_4

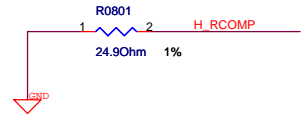
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H_REQ#_1	E13	H_REQ#1	
H_REQ#_2	A11	H_REQ#2	
H_REQ#_3	H13	H_REQ#3	
H_REQ#_4	B12	H_REQ#4	

H_RS#_0	E12	H_RS#0	H_RS#0_4
H_RS#_1	D7	H_RS#1	H_RS#1_4
H_RS#_2	D8	H_RS#2	H_RS#2_4

4 H_REQ#[4:0] H_REQ#[4:0]

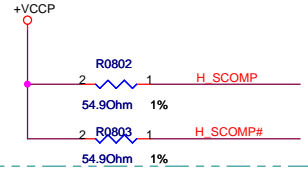
RCOMP

For Calibrating the FSB I/O Buffer



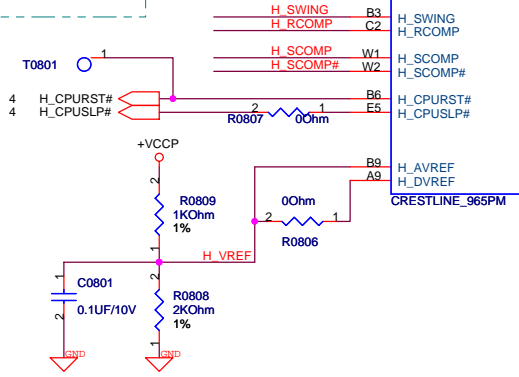
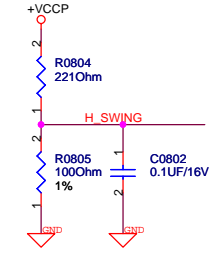
SCOMP

For Slew Rate Compensation on the FSB



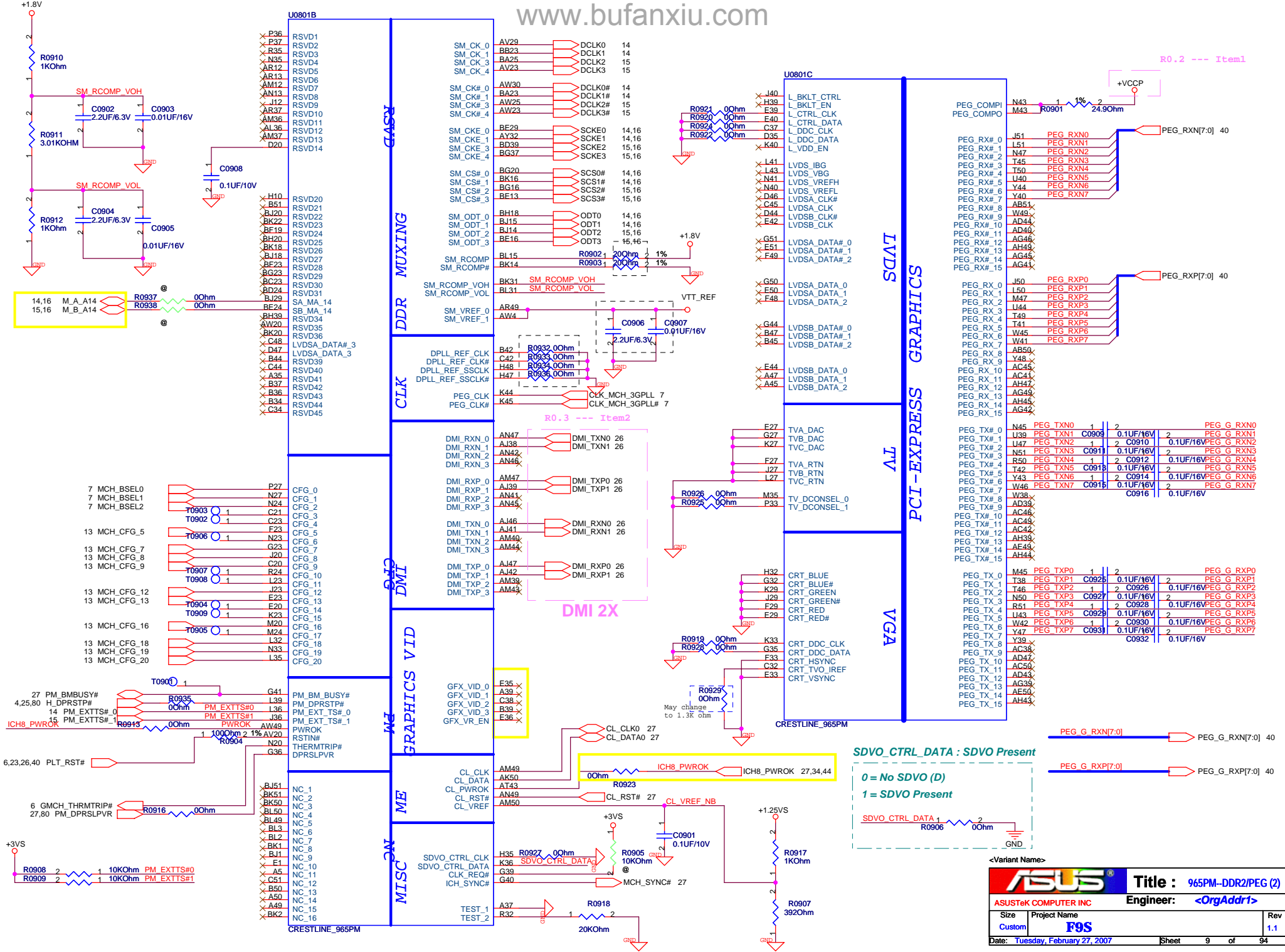
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



<Variant Name>

ASUS		Title : 965PM -- CPU (1)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddrt>	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Tuesday, February 27, 2007		Sheet	8 of 94



14 M_A_DQ[0:63]

U0801D

M_A_DQ0	AR43	SA_DQ_0
M_A_DQ1	AW44	SA_DQ_1
M_A_DQ2	BA45	SA_DQ_2
M_A_DQ3	AY46	SA_DQ_3
M_A_DQ4	AR41	SA_DQ_4
M_A_DQ5	AR45	SA_DQ_5
M_A_DQ6	AW47	SA_DQ_6
M_A_DQ7	AT42	SA_DQ_7
M_A_DQ8	BR45	SA_DQ_8
M_A_DQ9	BF48	SA_DQ_9
M_A_DQ10	BG47	SA_DQ_10
M_A_DQ11	BJ45	SA_DQ_11
M_A_DQ12	BB47	SA_DQ_12
M_A_DQ13	BG50	SA_DQ_13
M_A_DQ14	BJ49	SA_DQ_14
M_A_DQ15	BE45	SA_DQ_15
M_A_DQ16	AW43	SA_DQ_16
M_A_DQ17	BE44	SA_DQ_17
M_A_DQ18	BG42	SA_DQ_18
M_A_DQ19	BE40	SA_DQ_19
M_A_DQ20	BF44	SA_DQ_20
M_A_DQ21	BJ45	SA_DQ_21
M_A_DQ22	BG40	SA_DQ_22
M_A_DQ23	BE40	SA_DQ_23
M_A_DQ24	AR40	SA_DQ_24
M_A_DQ25	AW40	SA_DQ_25
M_A_DQ26	AT39	SA_DQ_26
M_A_DQ27	AV36	SA_DQ_27
M_A_DQ28	AW41	SA_DQ_28
M_A_DQ29	AY41	SA_DQ_29
M_A_DQ30	AV38	SA_DQ_30
M_A_DQ31	AT38	SA_DQ_31
M_A_DQ32	AV13	SA_DQ_32
M_A_DQ33	AT13	SA_DQ_33
M_A_DQ34	AW11	SA_DQ_34
M_A_DQ35	AV11	SA_DQ_35
M_A_DQ36	AU15	SA_DQ_36
M_A_DQ37	AT11	SA_DQ_37
M_A_DQ38	BA13	SA_DQ_38
M_A_DQ39	BA11	SA_DQ_39
M_A_DQ40	BE10	SA_DQ_40
M_A_DQ41	BD10	SA_DQ_41
M_A_DQ42	BD8	SA_DQ_42
M_A_DQ43	AY9	SA_DQ_43
M_A_DQ44	BG10	SA_DQ_44
M_A_DQ45	AW9	SA_DQ_45
M_A_DQ46	BD7	SA_DQ_46
M_A_DQ47	BB9	SA_DQ_47
M_A_DQ48	BB5	SA_DQ_48
M_A_DQ49	AY7	SA_DQ_49
M_A_DQ50	AT5	SA_DQ_50
M_A_DQ51	AT7	SA_DQ_51
M_A_DQ52	AY6	SA_DQ_52
M_A_DQ53	BB7	SA_DQ_53
M_A_DQ54	AR5	SA_DQ_54
M_A_DQ55	AR8	SA_DQ_55
M_A_DQ56	AR9	SA_DQ_56
M_A_DQ57	AN3	SA_DQ_57
M_A_DQ58	AM8	SA_DQ_58
M_A_DQ59	AN10	SA_DQ_59
M_A_DQ60	AT9	SA_DQ_60
M_A_DQ61	AN9	SA_DQ_61
M_A_DQ62	AM9	SA_DQ_62
M_A_DQ63	AN11	SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0	BB19	M_A_BS#0 14,16
SA_BS_1	BK19	M_A_BS#1 14,16
SA_BS_2	BF29	M_A_BS#2 14,16
SA_CAS#	BL17	M_A_CAS# 14,16
SA_DM_0	AT45	M_A_DM0
SA_DM_1	BD44	M_A_DM1
SA_DM_2	AW38	M_A_DM2
SA_DM_3	AW13	M_A_DM3
SA_DM_4	BG8	M_A_DM4
SA_DM_5	AY5	M_A_DM5
SA_DM_6	AN6	M_A_DM6
SA_DM_7		
SA_DQS_0	AT46	M_A_DQS0
SA_DQS_1	BE48	M_A_DQS1
SA_DQS_2	BB43	M_A_DQS2
SA_DQS_3	BC37	M_A_DQS3
SA_DQS_4	BB16	M_A_DQS4
SA_DQS_5	BH6	M_A_DQS5
SA_DQS_6	AP3	M_A_DQS6
SA_DQS_7	AT47	M_A_DQS7
SA_DQS#_0	BD47	M_A_DQS#0
SA_DQS#_1	BC41	M_A_DQS#1
SA_DQS#_2	BA37	M_A_DQS#2
SA_DQS#_3	BA16	M_A_DQS#3
SA_DQS#_4	BH7	M_A_DQS#4
SA_DQS#_5	BC1	M_A_DQS#5
SA_DQS#_6	AP2	M_A_DQS#6
SA_DQS#_7		
SA_MA_0	BJ19	M_A_A0
SA_MA_1	BD20	M_A_A1
SA_MA_2	BK27	M_A_A2
SA_MA_3	BH28	M_A_A3
SA_MA_4	BL24	M_A_A4
SA_MA_5	BK28	M_A_A5
SA_MA_6	BJ27	M_A_A6
SA_MA_7	BJ25	M_A_A7
SA_MA_8	BL28	M_A_A8
SA_MA_9	BA28	M_A_A9
SA_MA_10	BC19	M_A_A10
SA_MA_11	BE28	M_A_A11
SA_MA_12	BG30	M_A_A12
SA_MA_13	BJ16	M_A_A13
SA_RAS#	BE18	M_A_RAS# 14,16
SA_RCVEN#	AY20	M_A_RCVEN#
SA_WE#	BA19	M_A_WE# 14,16

CRESTLINE_965PM

15 M_B_DQ[0:63]

U0801E

M_B_DQ0	AP49	SB_DQ_0
M_B_DQ1	AR51	SB_DQ_1
M_B_DQ2	AW50	SB_DQ_2
M_B_DQ3	AW51	SB_DQ_3
M_B_DQ4	AN51	SB_DQ_4
M_B_DQ5	AN50	SB_DQ_5
M_B_DQ6	AV50	SB_DQ_6
M_B_DQ7	AV49	SB_DQ_7
M_B_DQ8	BA50	SB_DQ_8
M_B_DQ9	BB50	SB_DQ_9
M_B_DQ10	BA49	SB_DQ_10
M_B_DQ11	BE50	SB_DQ_11
M_B_DQ12	BA51	SB_DQ_12
M_B_DQ13	AY49	SB_DQ_13
M_B_DQ14	BE50	SB_DQ_14
M_B_DQ15	BF49	SB_DQ_15
M_B_DQ16	BJ50	SB_DQ_16
M_B_DQ17	BJ44	SB_DQ_17
M_B_DQ18	BJ43	SB_DQ_18
M_B_DQ19	BL43	SB_DQ_19
M_B_DQ20	BK47	SB_DQ_20
M_B_DQ21	BK49	SB_DQ_21
M_B_DQ22	BK43	SB_DQ_22
M_B_DQ23	BK42	SB_DQ_23
M_B_DQ24	BJ41	SB_DQ_24
M_B_DQ25	BL41	SB_DQ_25
M_B_DQ26	BL43	SB_DQ_26
M_B_DQ27	BJ36	SB_DQ_27
M_B_DQ28	BK41	SB_DQ_28
M_B_DQ29	BJ40	SB_DQ_29
M_B_DQ30	BL35	SB_DQ_30
M_B_DQ31	BK37	SB_DQ_31
M_B_DQ32	BK13	SB_DQ_32
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M_B_DQ34	BK11	SB_DQ_34
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M_B_DQ37	BE12	SB_DQ_37
M_B_DQ38	BC12	SB_DQ_38
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M_B_DQ41	BL9	SB_DQ_41
M_B_DQ42	BK5	SB_DQ_42
M_B_DQ43	BL5	SB_DQ_43
M_B_DQ44	BK9	SB_DQ_44
M_B_DQ45	BK10	SB_DQ_45
M_B_DQ46	BJ6	SB_DQ_46
M_B_DQ47	BJ6	SB_DQ_47
M_B_DQ48	BF4	SB_DQ_48
M_B_DQ49	BH5	SB_DQ_49
M_B_DQ50	BG1	SB_DQ_50
M_B_DQ51	BC2	SB_DQ_51
M_B_DQ52	BK3	SB_DQ_52
M_B_DQ53	BF4	SB_DQ_53
M_B_DQ54	BD3	SB_DQ_54
M_B_DQ55	BJ2	SB_DQ_55
M_B_DQ56	BA3	SB_DQ_56
M_B_DQ57	BB3	SB_DQ_57
M_B_DQ58	AR1	SB_DQ_58
M_B_DQ59	AT3	SB_DQ_59
M_B_DQ60	AY2	SB_DQ_60
M_B_DQ61	AY3	SB_DQ_61
M_B_DQ62	AU2	SB_DQ_62
M_B_DQ63	AT2	SB_DQ_63

CRESTLINE_965PM

DDR SYSTEM MEMORY B

SB_BS_0	AY17	M_B_BS#0 15,16
SB_BS_1	BG18	M_B_BS#1 15,16
SB_BS_2	BG36	M_B_BS#2 15,16
SB_CAS#	BE17	M_B_CAS# 15,16
SB_DM_0	AR50	M_B_DM0
SB_DM_1	BD49	M_B_DM1
SB_DM_2	BK45	M_B_DM2
SB_DM_3	BL39	M_B_DM3
SB_DM_4	BH12	M_B_DM4
SB_DM_5	BJ7	M_B_DM5
SB_DM_6	BE3	M_B_DM6
SB_DM_7	AW2	M_B_DM7
SB_DQS_0	AT50	M_B_DQS0
SB_DQS_1	BD50	M_B_DQS1
SB_DQS_2	BK46	M_B_DQS2
SB_DQS_3	BK39	M_B_DQS3
SB_DQS_4	BL12	M_B_DQS4
SB_DQS_5	BL7	M_B_DQS5
SB_DQS_6	BE2	M_B_DQS6
SB_DQS_7	AV2	M_B_DQS7
SB_DQS#_0	AU50	M_B_DQS#0
SB_DQS#_1	BC50	M_B_DQS#1
SB_DQS#_2	BL45	M_B_DQS#2
SB_DQS#_3	BK38	M_B_DQS#3
SB_DQS#_4	BK12	M_B_DQS#4
SB_DQS#_5	BK7	M_B_DQS#5
SB_DQS#_6	BE2	M_B_DQS#6
SB_DQS#_7	AV3	M_B_DQS#7
SB_MA_0	BC18	M_B_A0
SB_MA_1	BG28	M_B_A1
SB_MA_2	BG25	M_B_A2
SB_MA_3	AW17	M_B_A3
SB_MA_4	BE25	M_B_A4
SB_MA_5	BE25	M_B_A5
SB_MA_6	BA29	M_B_A6
SB_MA_7	RC28	M_B_A7
SB_MA_8	AY28	M_B_A8
SB_MA_9	BD37	M_B_A9
SB_MA_10	BG17	M_B_A10
SB_MA_11	BE37	M_B_A11
SB_MA_12	BA39	M_B_A12
SB_MA_13	BG13	M_B_A13
SB_RAS#	AV16	M_B_RAS# 15,16
SB_RCVEN#	AY18	M_B_RCVEN#
SB_WE#	BC17	M_B_WE# 15,16

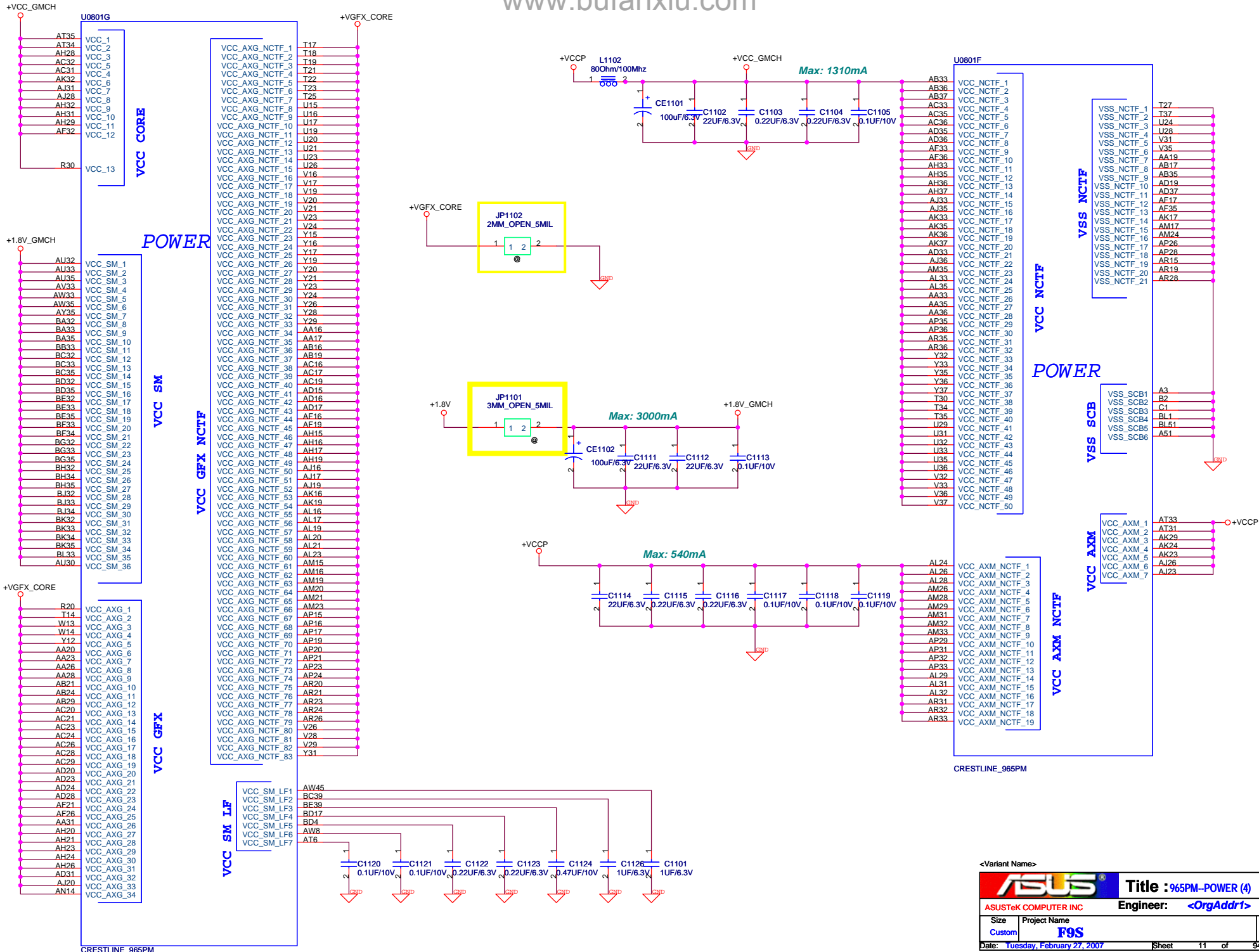
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ASUS Title : 965PM--DDR2 bus (3)

ASUSTeK COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 10 of 94



<Variant Name>

ASUS Title : 965PM-POWER (4)

ASUSTeK COMPUTER INC Engineer: <OrgAddr1>

Size Project Name

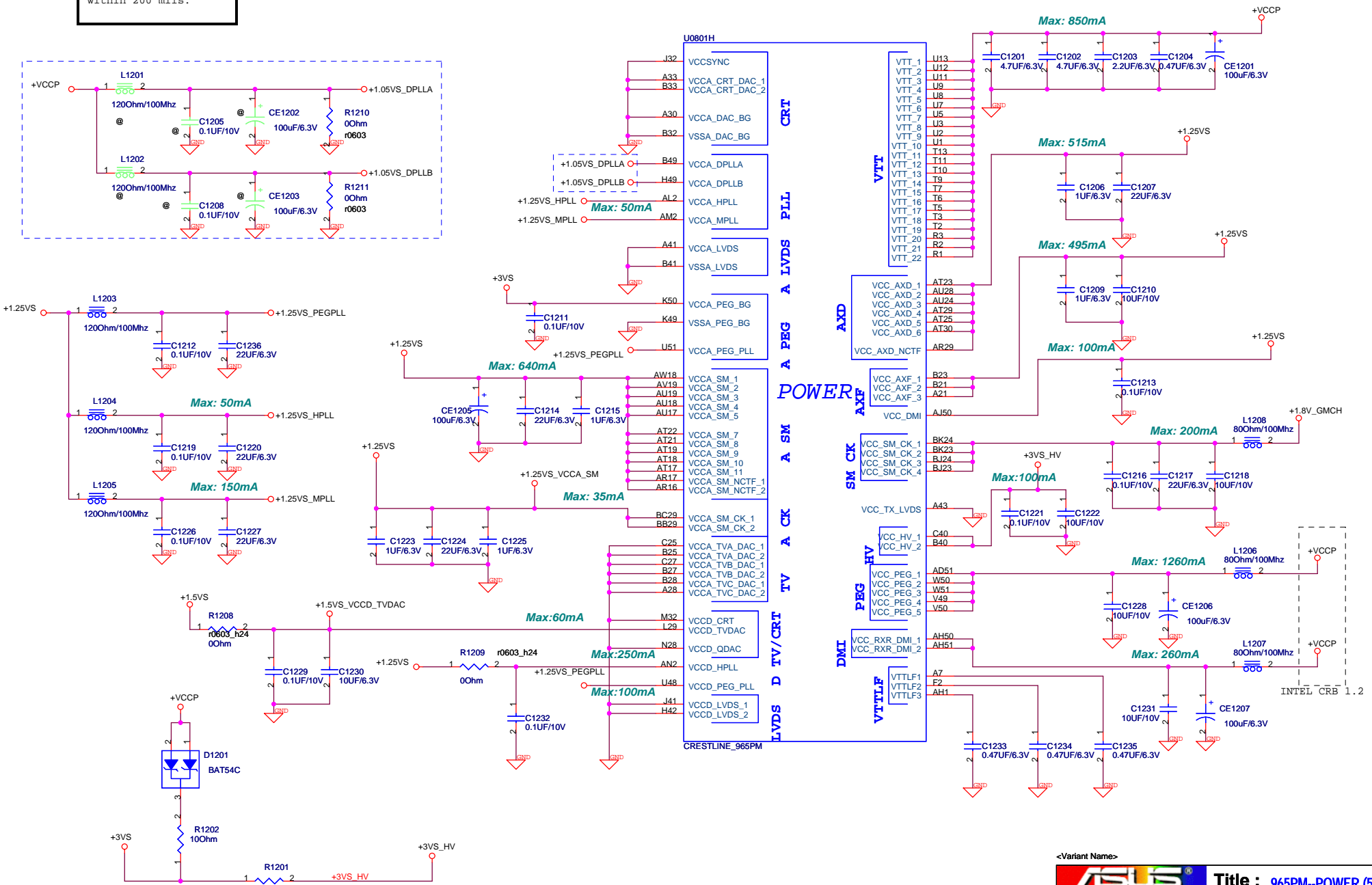
Custom F9S

Date: Tuesday, February 27, 2007 Sheet 11 of 94

CRESTLINE_965PM

CRESTLINE_965PM

NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.



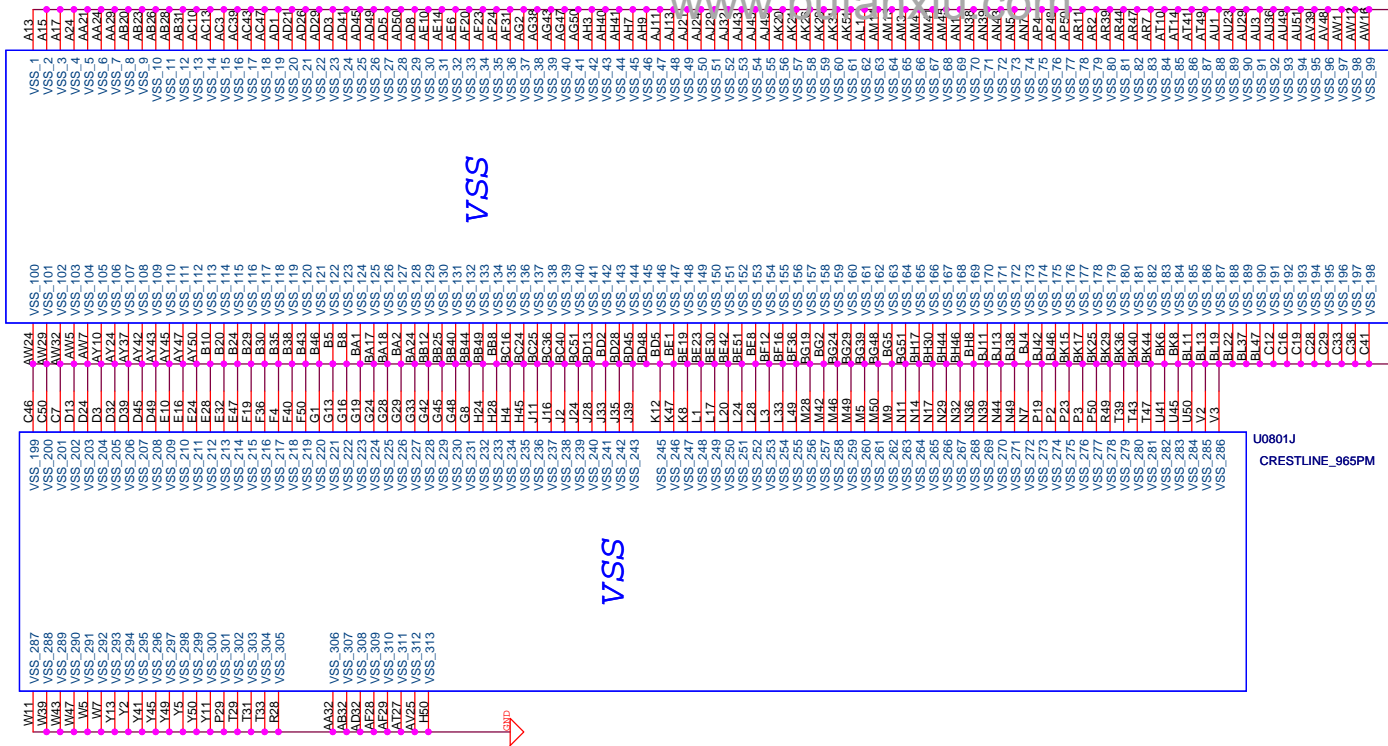
<Variant Name>

ASUS Title : 965PM--POWER (5)

ASUSTeK COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 12 of 94



U08011
CRESTLINE_965PM

U0801J
CRESTLINE_965PM

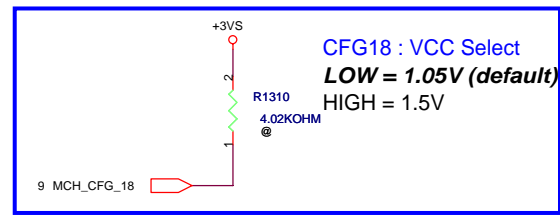
9 MCH_CFG_5 **CFG5 : DMI STRAP**
HIGH = DMI X 4 (Default)
LOW = DMI X 2

9 MCH_CFG_7 **CFG7 : CPU STRAP**
HIGH = Mobile CPU (Default)
LOW = Reserved

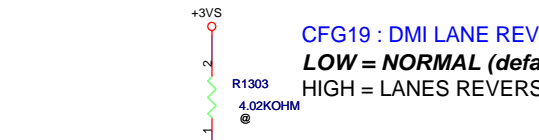
9 MCH_CFG_8 **CFG8 : Low Power PCI-E**
0 = Normal mode
1 = Low Power Mode (Default)

9 MCH_CFG_9 **CFG9 : PCIE GRAPHIC LANE**
LOW = REVERSE LANE
HIGH = Normal Operation (Default)

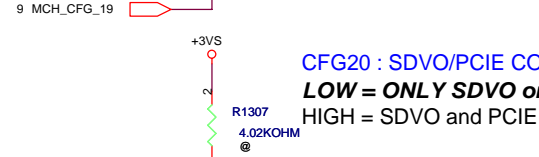
9 MCH_CFG_16 **CFG16 : Dynamic ODT STRAP**
Low = Dynamic ODT Disabled
HIGH = Dyanamic ODT Enabled (default)



CFG18 : VCC Select
LOW = 1.05V (default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL
LOW = NORMAL (default)
HIGH = LANES REVERSED



CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

9 MCH_CFG_13 **CFG [13:12] : XOR/ALL-Z**
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)



		Title : GND/Strapping (6)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size Custom	Project Name F9S	Rev 1.1	
Date: Tuesday, February 27, 2007		Sheet 13 of 94	

10 M_A_DQ[0..63] M A DQ[0..63]

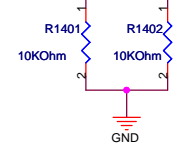
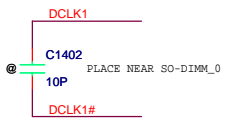
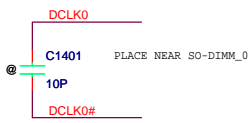
P/N : 12G025022004

CON140A

M A A0	102	A0	DQ0	5	M A DQ4
M A A1	101	A1	DQ1	7	M A DQ0
M A A2	100	A2	DQ2	17	M A DQ2
M A A3	99	A3	DQ3	19	M A DQ1
M A A4	98	A4	DQ4	4	M A DQ5
M A A5	97	A4	DQ5	6	M A DQ6
M A A6	94	A6	DQ6	14	M A DQ3
M A A7	92	A7	DQ7	16	M A DQ7
M A A8	93	A8	DQ8	23	M A DQ15
M A A9	91	A9	DQ9	35	M A DQ11
M A A10	105	A10/AP	DQ10	37	M A DQ10
M A A11	90	A11	DQ11	20	M A DQ12
M A A12	89	A12	DQ12	22	M A DQ8
M A A13	116	A13	DQ13	38	M A DQ14
M A A14	86	A14	DQ14	36	M A DQ13
M A A15	84	A15	DQ15	38	M A DQ14
A16_BA2	85	A16_BA2	DQ16	43	M A DQ21
			DQ17	55	M A DQ22
			DQ18	57	M A DQ23
			DQ19	44	M A DQ17
			DQ20	44	M A DQ17
			DQ21	46	M A DQ20
			DQ22	56	M A DQ18
			DQ23	58	M A DQ19
			DQ24	61	M A DQ28
			DQ25	63	M A DQ29
			DQ26	73	M A DQ25
			DQ27	75	M A DQ26
			DQ28	62	M A DQ24
			DQ29	64	M A DQ27
			DQ30	74	M A DQ31
			DQ31	76	M A DQ30
			DQ32	123	M A DQ32
			DQ33	125	M A DQ36
			DQ34	135	M A DQ34
			DQ35	137	M A DQ37
			DQ36	124	M A DQ38
			DQ37	126	M A DQ33
			DQ38	134	M A DQ35
			DQ39	136	M A DQ39
			DQ40	141	M A DQ44
			DQ41	143	M A DQ45
			DQ42	151	M A DQ46
			DQ43	153	M A DQ43
			DQ44	140	M A DQ47
			DQ45	142	M A DQ41
			DQ46	152	M A DQ40
			DQ47	154	M A DQ42
			DQ48	157	M A DQ49
			DQ49	159	M A DQ54
			DQ50	173	M A DQ51
			DQ51	175	M A DQ50
			DQ52	158	M A DQ48
			DQ53	160	M A DQ53
			DQ54	174	M A DQ52
			DQ55	176	M A DQ55
			DQ56	179	M A DQ61
			DQ57	181	M A DQ56
			DQ58	188	M A DQ58
			DQ59	191	M A DQ59
			DQ60	180	M A DQ60
			DQ61	182	M A DQ57
			DQ62	192	M A DQ62
			DQ63	194	M A DQ63

DDR2_DIMM_200P
DDR2 DIMM 200P,1.8V,H:4mm,STD
12G025022004

R0.3 --- Item24



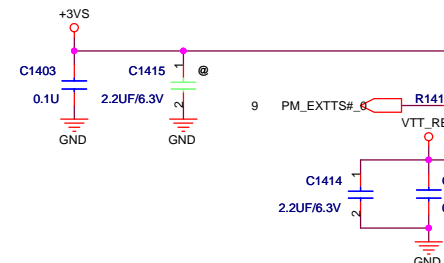
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP

+1.8V

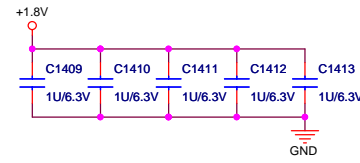
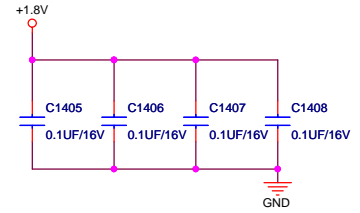
CON140B

112	VDD1	VSS16	18
111	VDD2	VSS17	41
117	VDD3	VSS18	53
96	VDD4	VSS19	42
95	VDD5	VSS20	60
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	66
103	VDD10	VSS25	127
88	VDD11	VSS26	139
104	VDD12	VSS27	128
199	VDDSPD	VSS29	145
		VSS30	165
		VSS31	171
83	NC1	VSS32	177
120	NC2	VSS33	177
50	NC3	VSS34	187
69	NC4	VSS35	178
163	NCTEST	VSS36	190
		VSS37	9
	VREF	VSS38	21
		VSS39	33
201	GND0	VSS40	155
202	GND1	VSS41	34
		VSS42	132
203	NP_NC1	VSS43	144
204	NP_NC2	VSS44	156
		VSS45	168
47	VSS1	VSS46	2
133	VSS2	VSS47	3
183	VSS3	VSS48	15
77	VSS4	VSS49	27
12	VSS5	VSS50	39
48	VSS6	VSS51	149
184	VSS7	VSS52	161
78	VSS8	VSS53	28
71	VSS9	VSS54	40
72	VSS10	VSS55	138
121	VSS11	VSS56	150
122	VSS12	VSS57	162
196	VSS13		
133	VSS14		
8	VSS15		

DDR2_DIMM_200P
DDR2 DIMM 200P,1.8V,H:4mm,STD
12G025022004



Layout Note: Place these Caps near SO DIMM 0

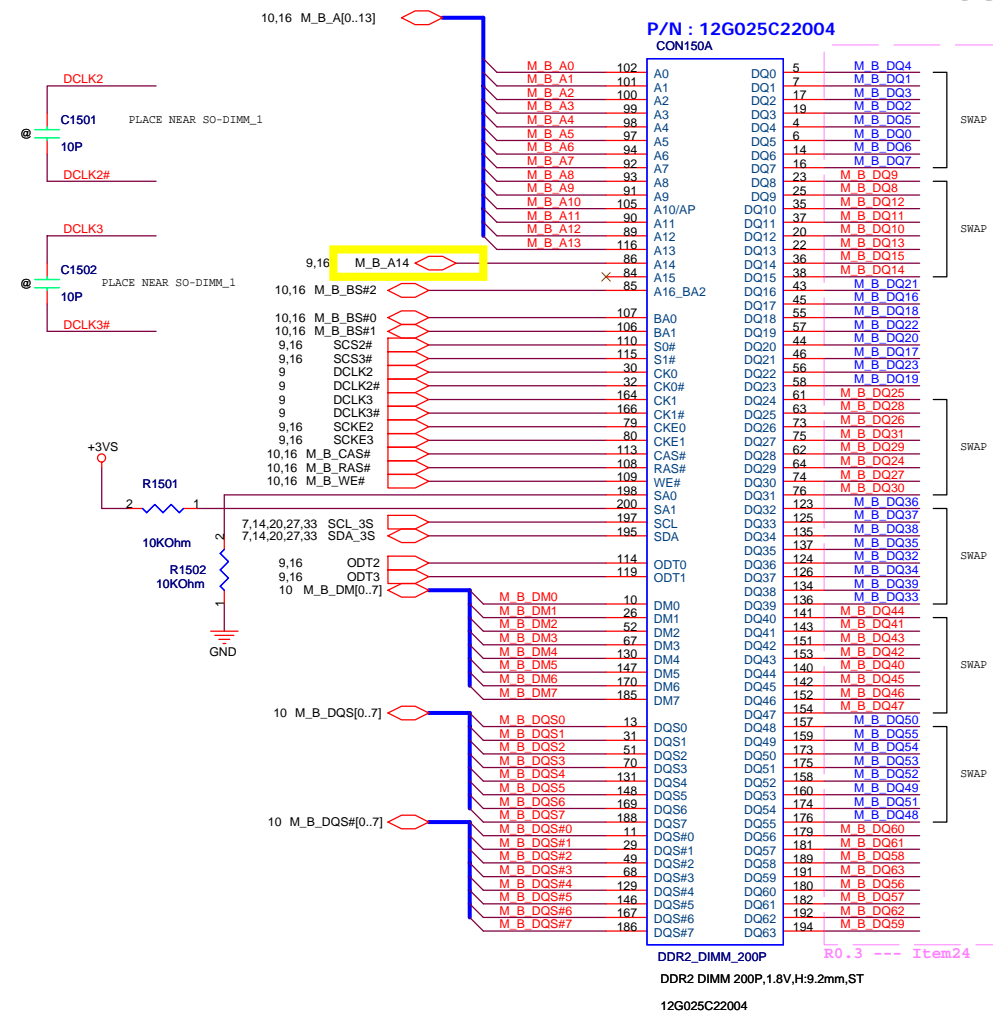


<Variant Name>

ASUS Title : DDR SO-DIMM 0
ASUSTeK COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 14 of 94



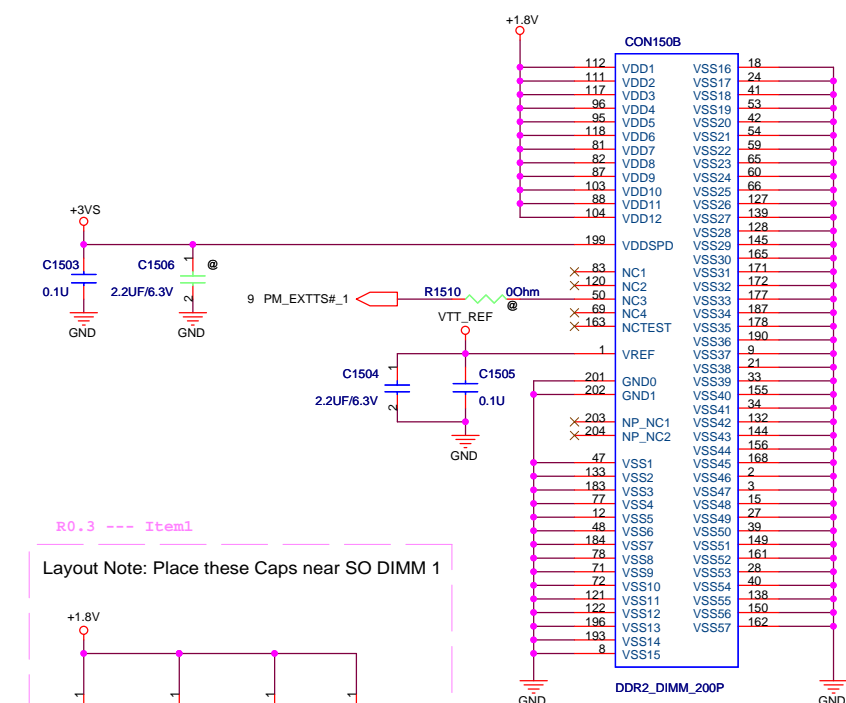
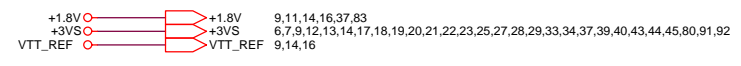
P/N : 12G025C22004

CON150A

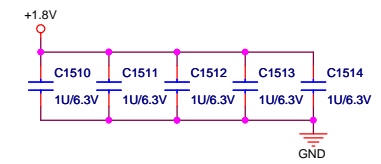
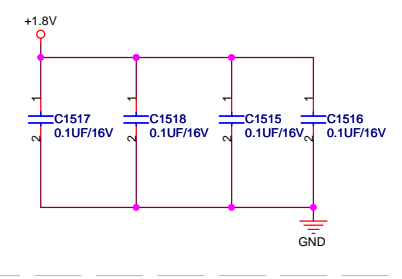
DDR2_DIMM_200P R0.3 --- Item24

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004



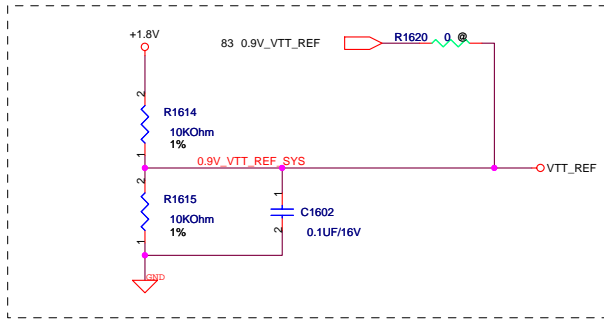
Layout Note: Place these Caps near SO DIMM 1



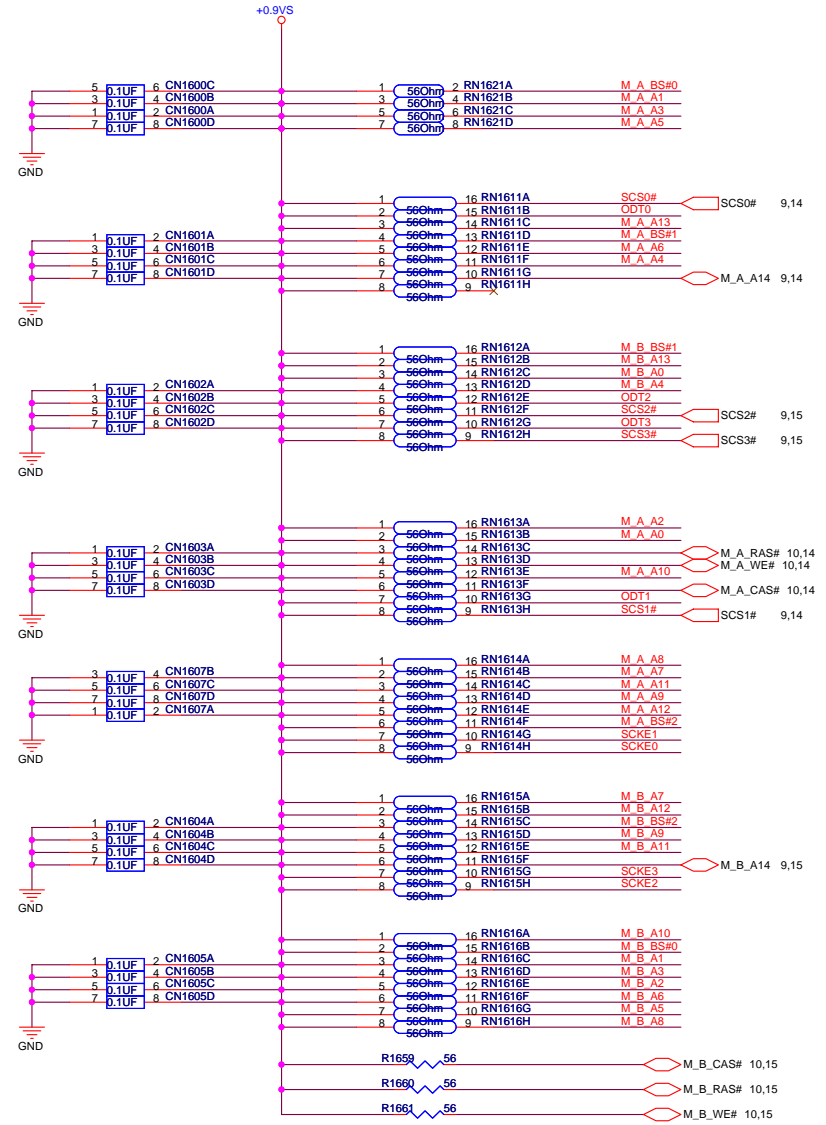
<Variant Name>

ASUS		Title : DDR SO-DIMM_1	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr>	
Size Custom	Project Name F9S	Rev 1.1	
Date: Tuesday, February 27, 2007		Sheet	15 of 94

SWAPPED



- M_A_A[0..13] 10,14
- M_A_BS#[0..2] 10,14
- M_B_A[0..13] 10,15
- M_B_BS#[0..2] 10,15
- SCKE[0:3] 9,14,15
- ODT[0:3] 9,14,15

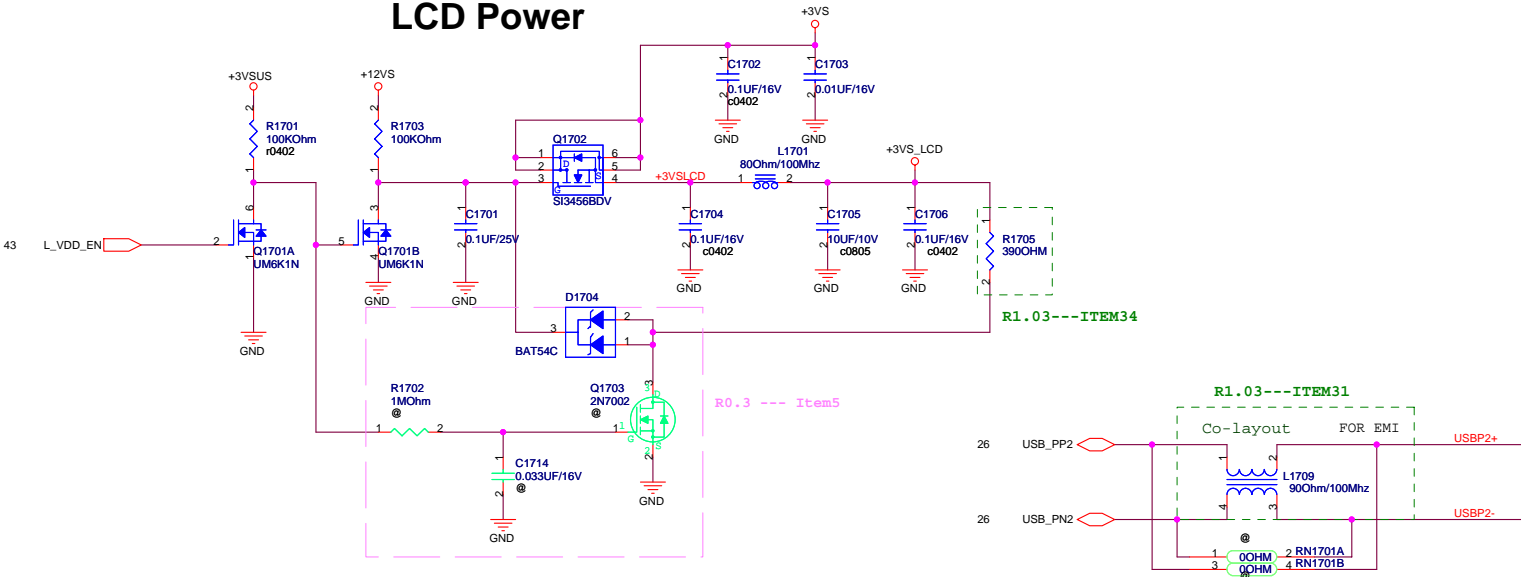


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

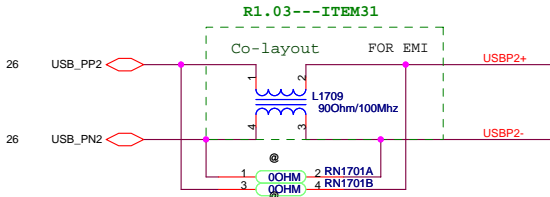
<Variant Names>

ASUS		Title : DDR2 ADDR TERM
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>
Size	Project Name	Rev
Custom	F9S	1.1
Date: Tuesday, February 27, 2007	Sheet	16 of 94

LCD Power

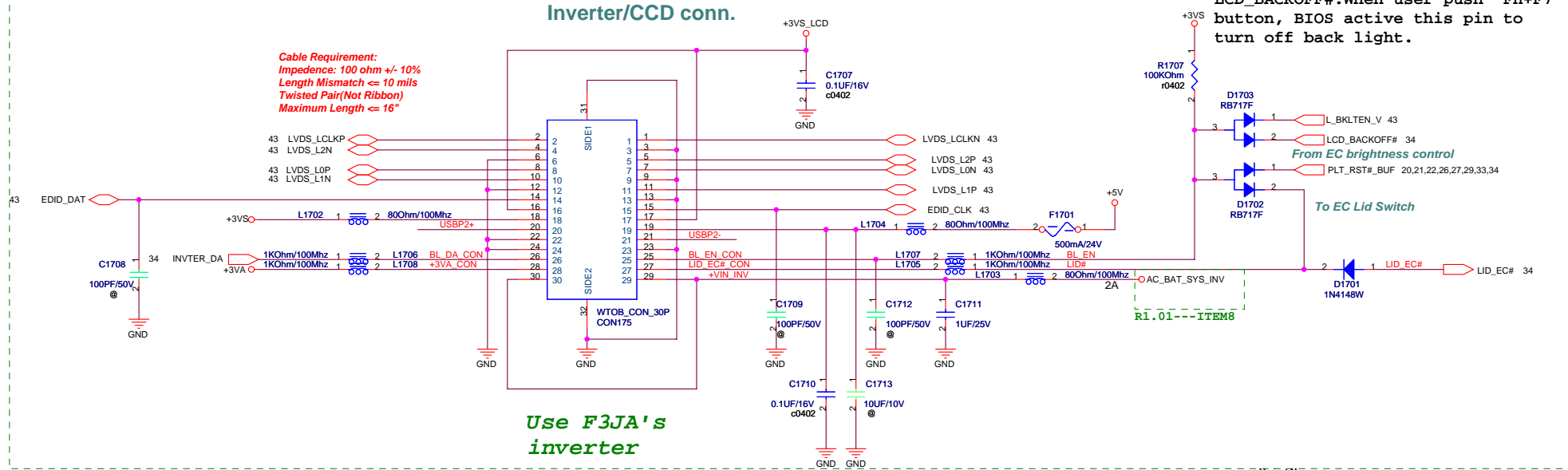


R1.2---ITEM36



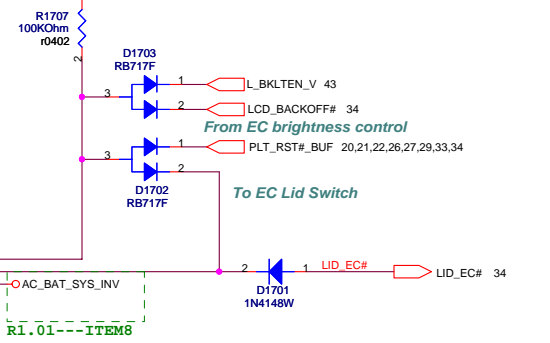
Inverter/CCD conn.

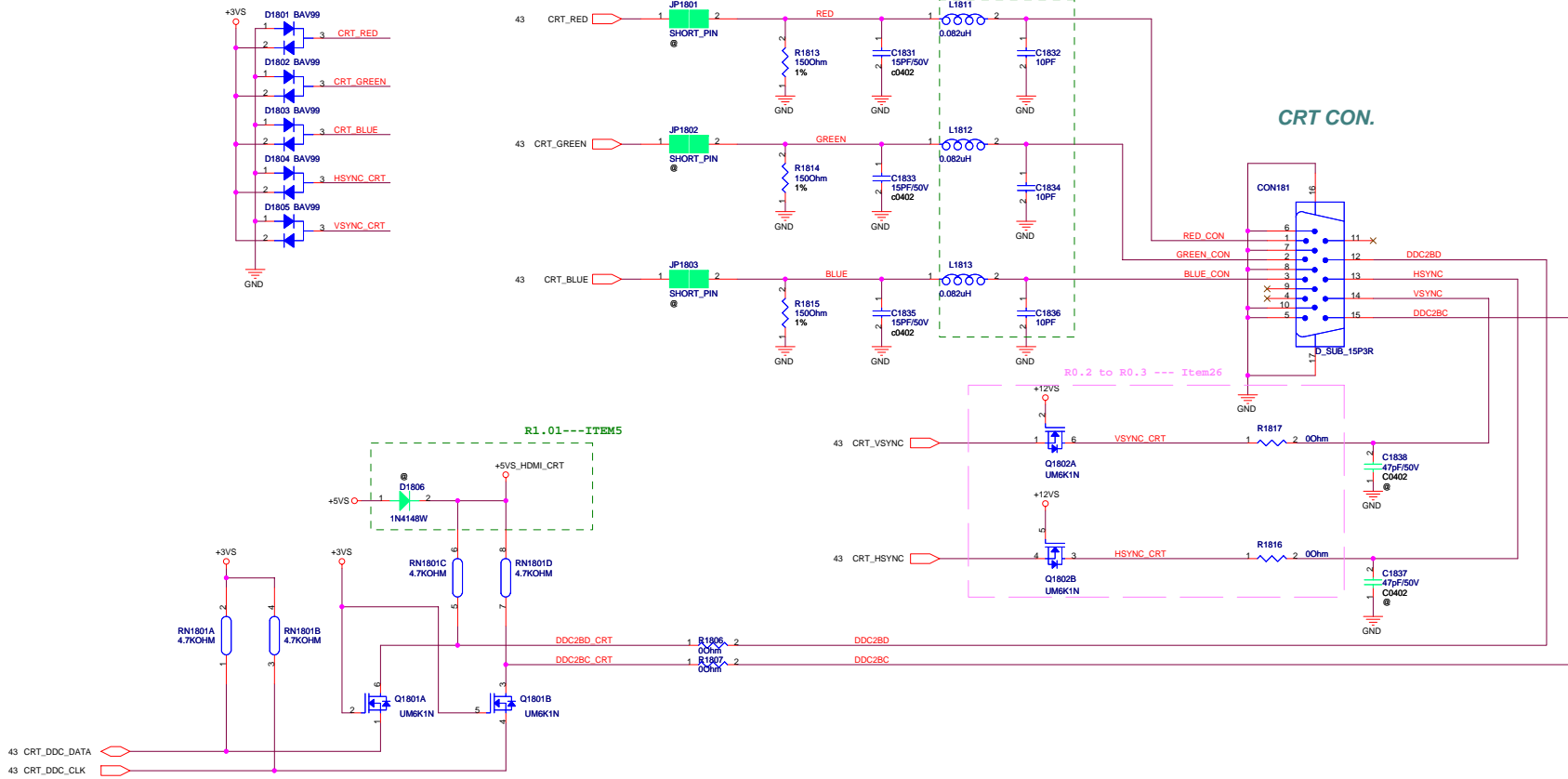
Cable Requirement:
 Impedence: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

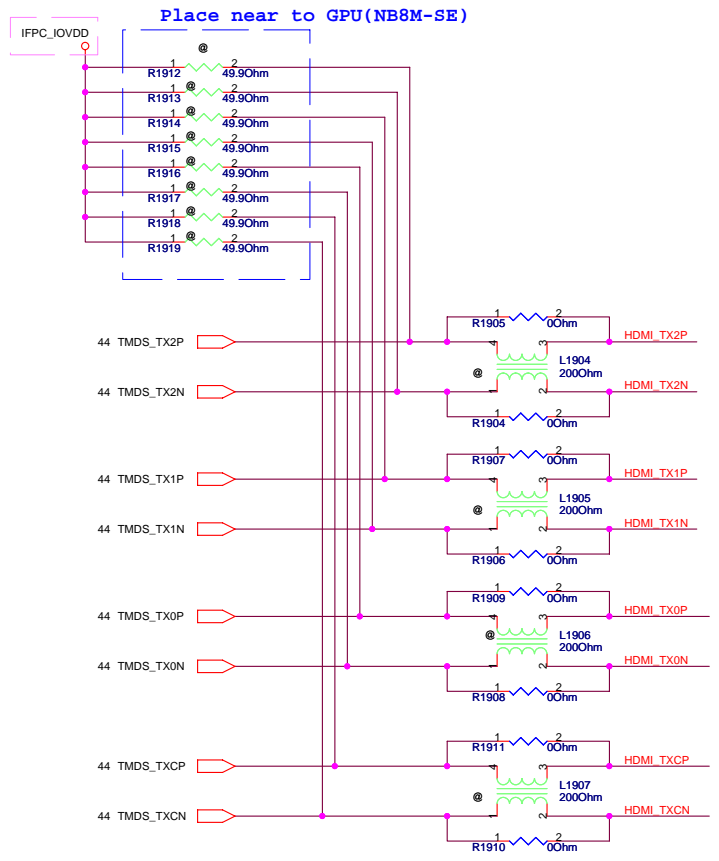


Use F3JA's inverter

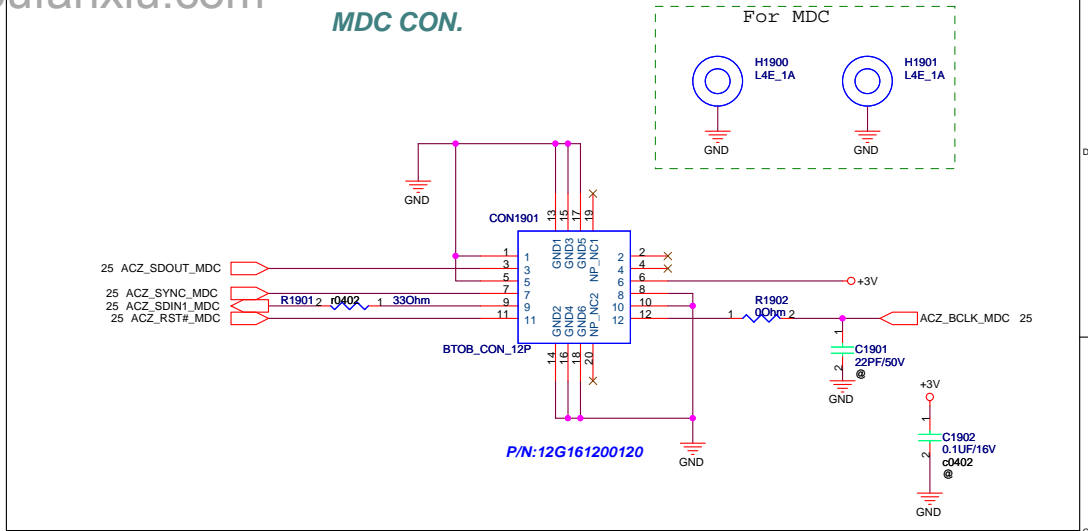
BIOS
 LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



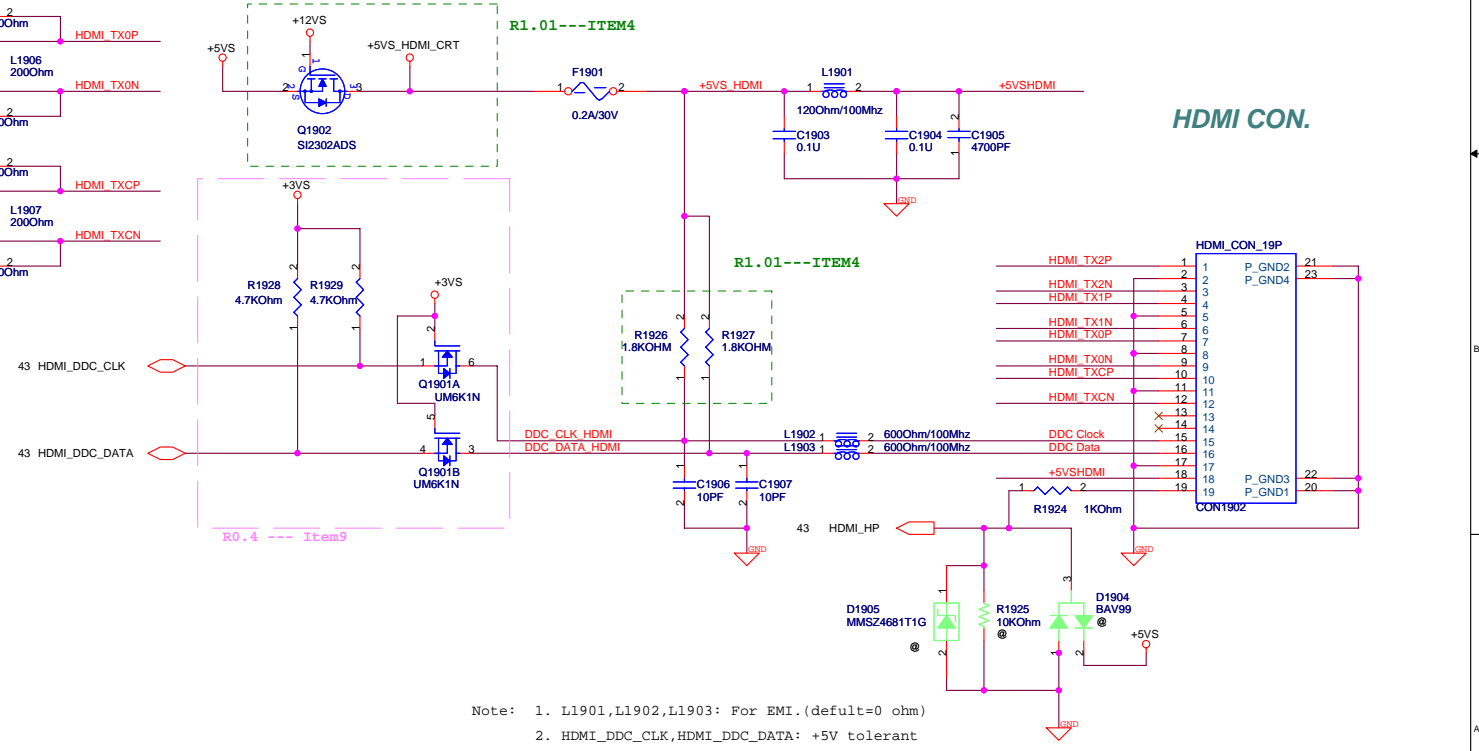




MDC CON.



HDMI CON.



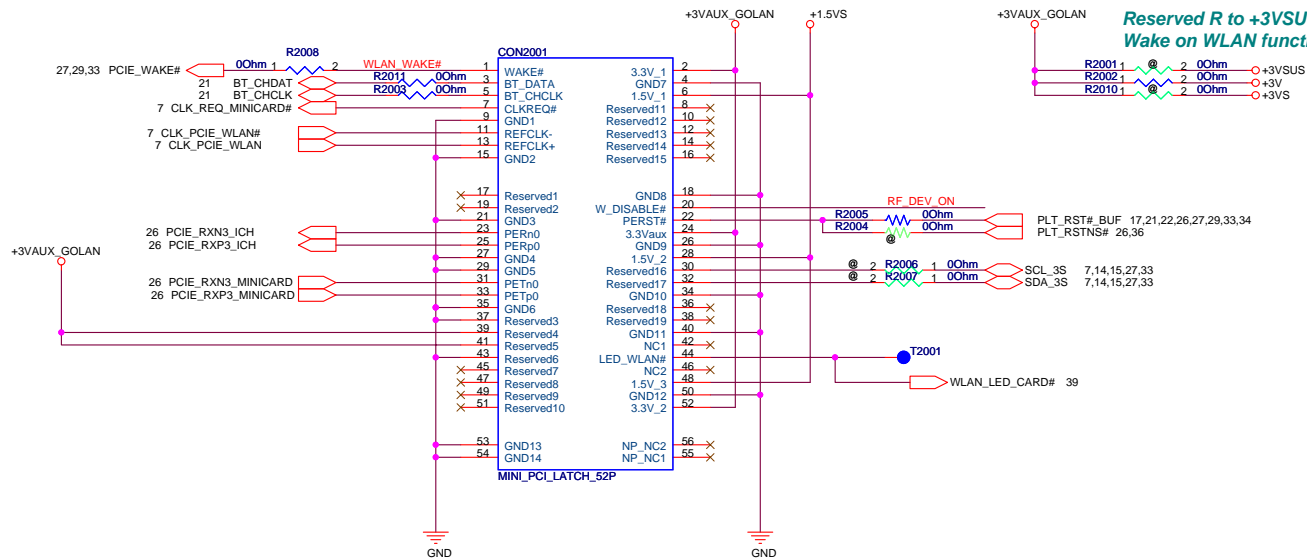
R0.4 --- Item9

- Note:
1. L1901,L1902,L1903: For EMI.(default=0 ohm)
 2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant

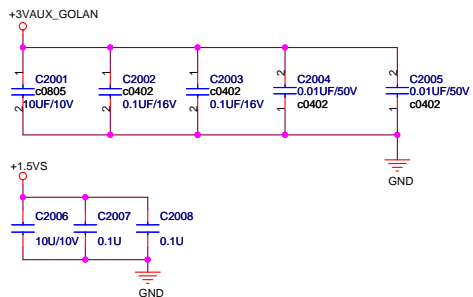
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

P/N : 12G030100525_2006/1024

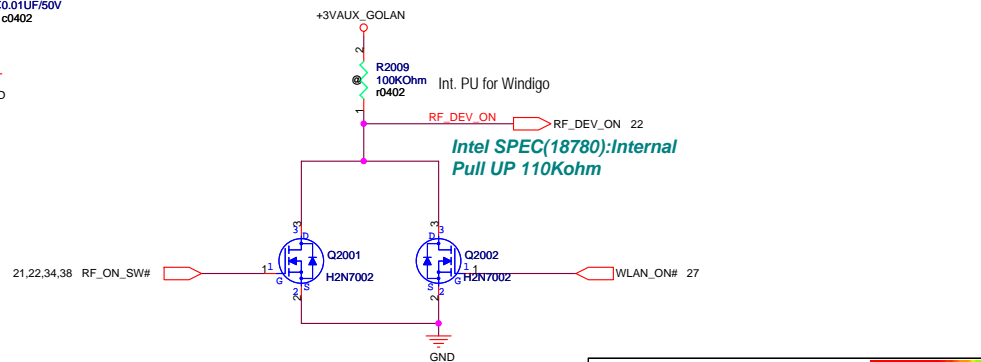
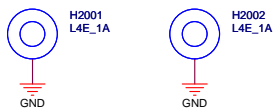
WLAN



Reserved R to +3VSUS for Wake on WLAN function!

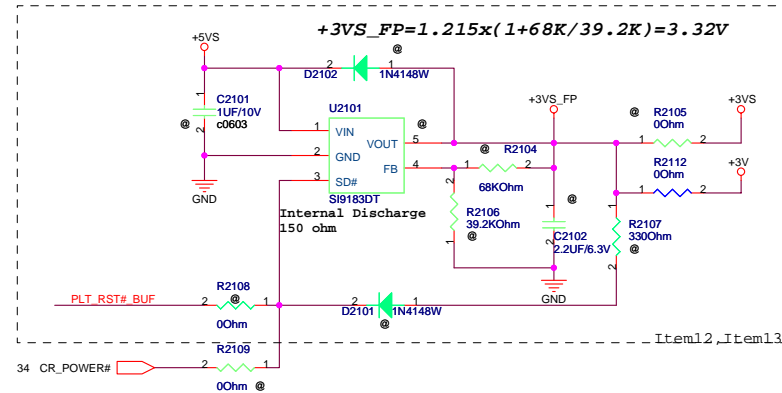
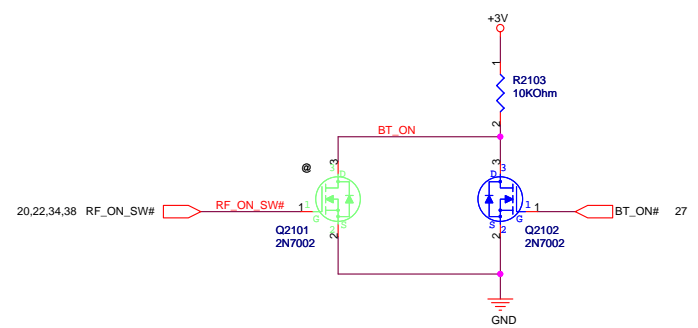
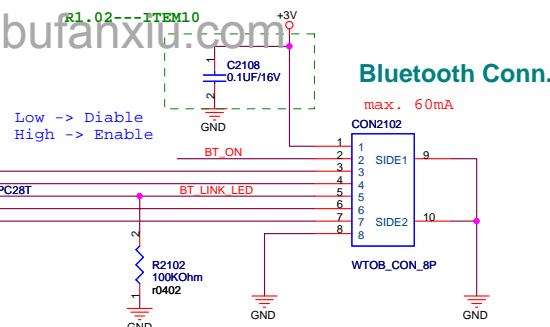
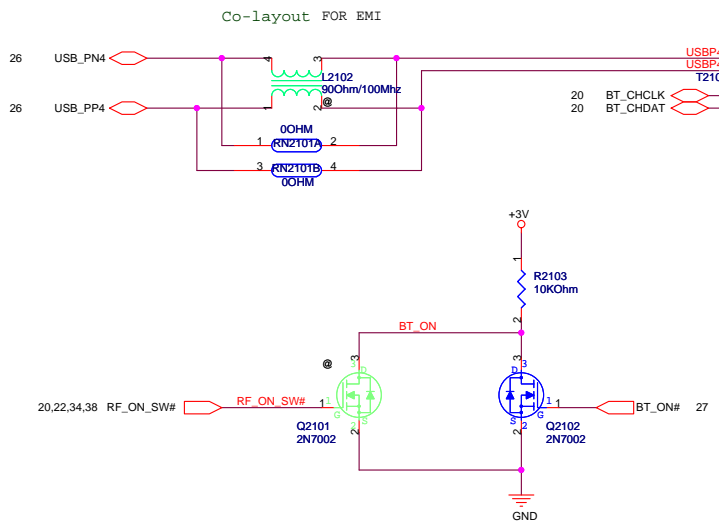


+1.5VS ○ +1.5VS 5,12,25,28,33,37,82
 +3V ○ +3V 19,21,22,26,33,35,37,91
 +3VS ○ +3VS 6,7,9,12,13,14,15,17,18,19,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92

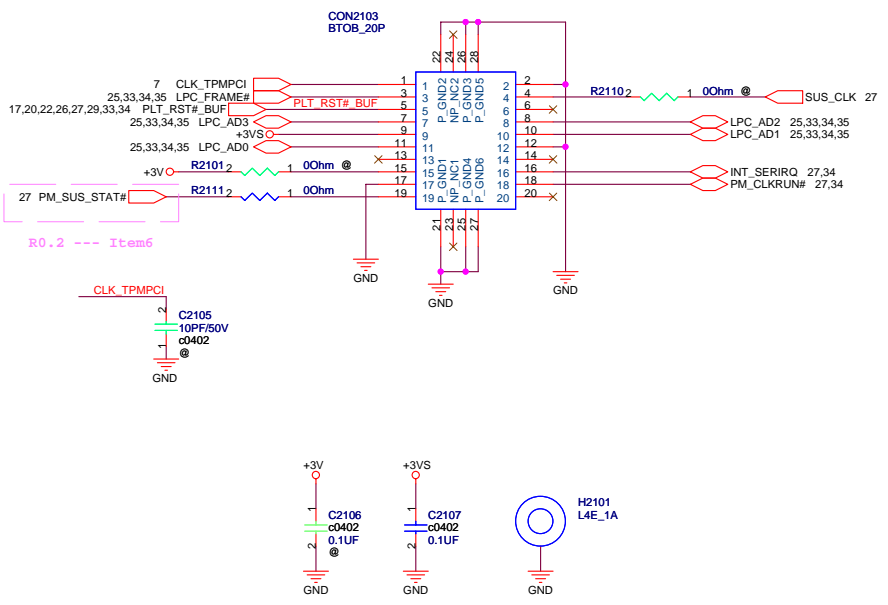


Intel SPEC(18780):Internal Pull UP 110kOhm

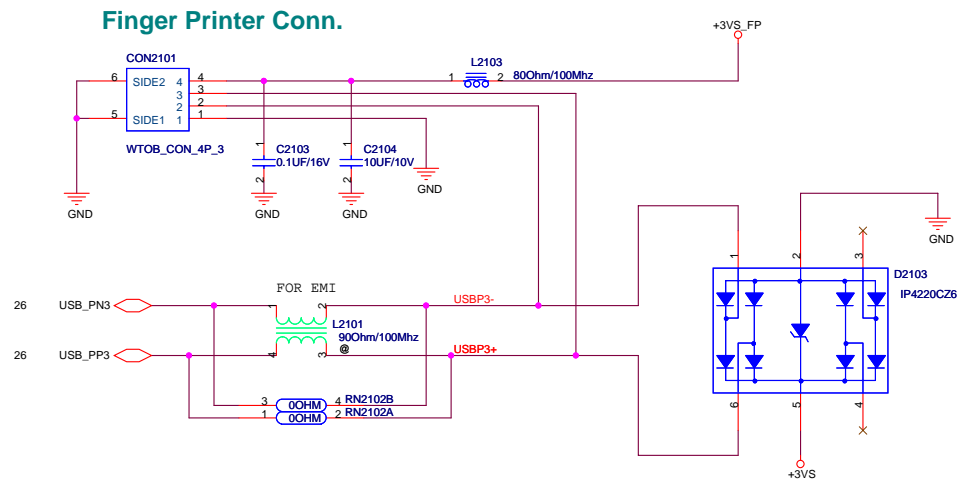
ASUSTek COMPUTER INC.		
c:OrgAddr1> Li-Te Rd.,Paitou, Taipei,Taiwan, ROC		
Title		
MINI CARD-(1)		
Size	Document Number	Rev
Custom	F9S	1.1
Date:	Tuesday, February 27, 2007	Sheet 20 of 94

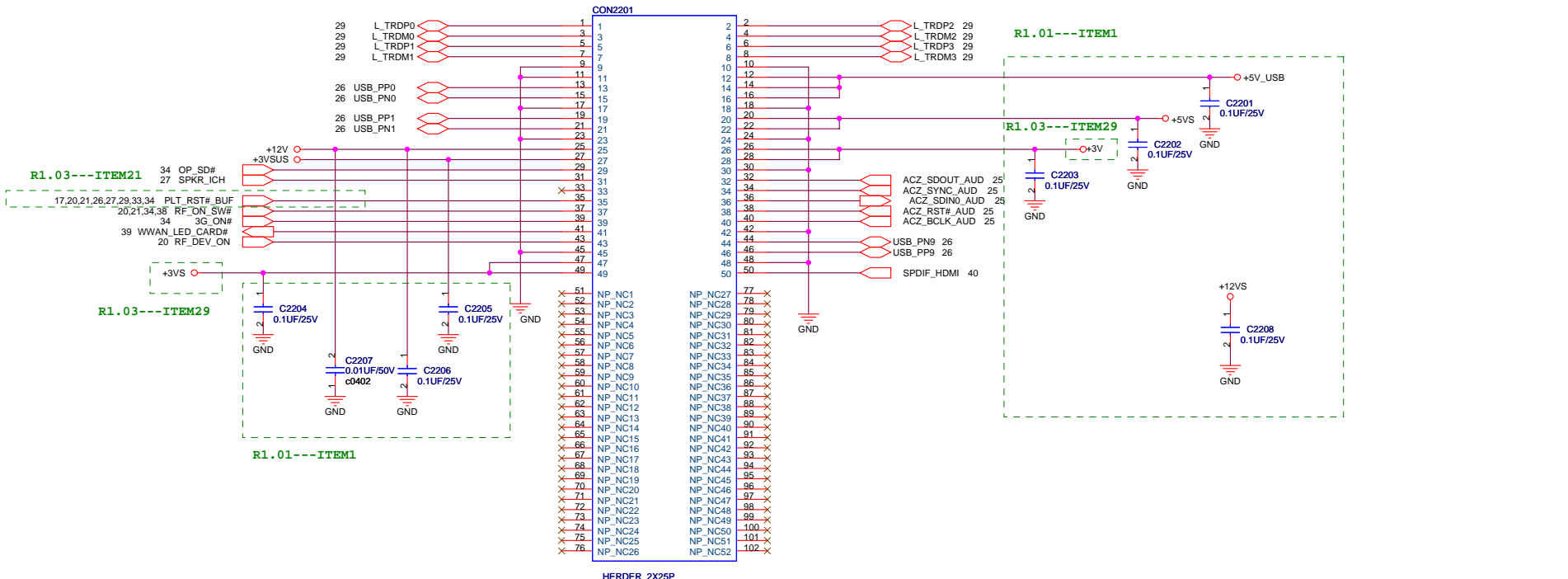


TPM Module Conn.



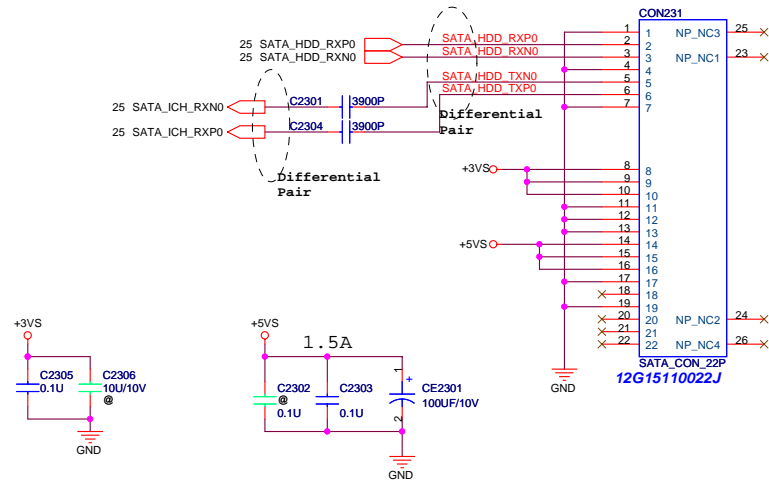
Finger Printer Conn.



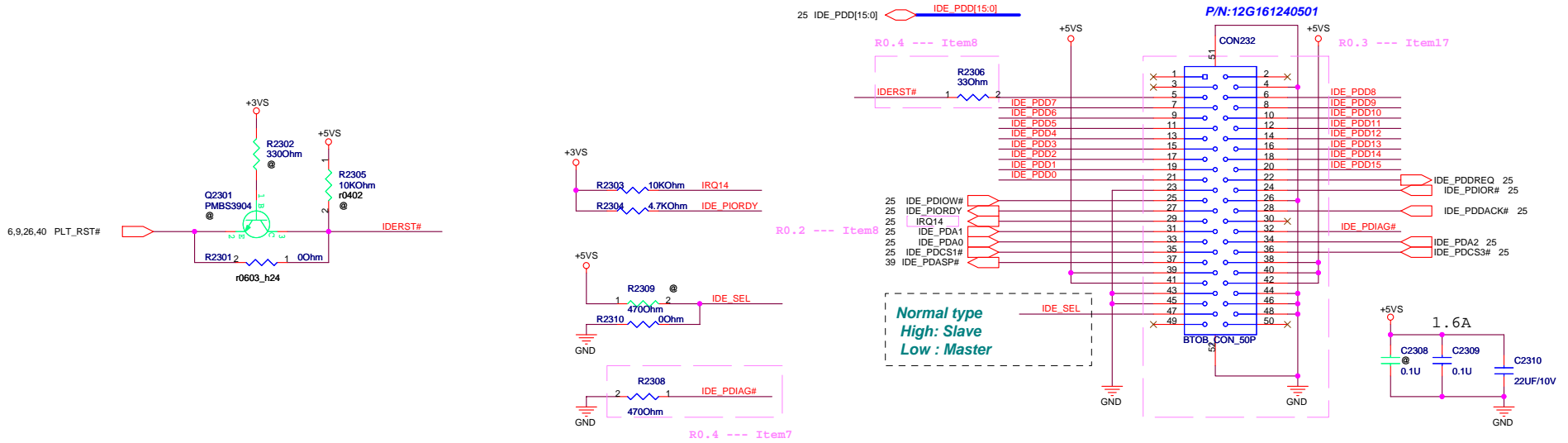


HERDER_2X25P

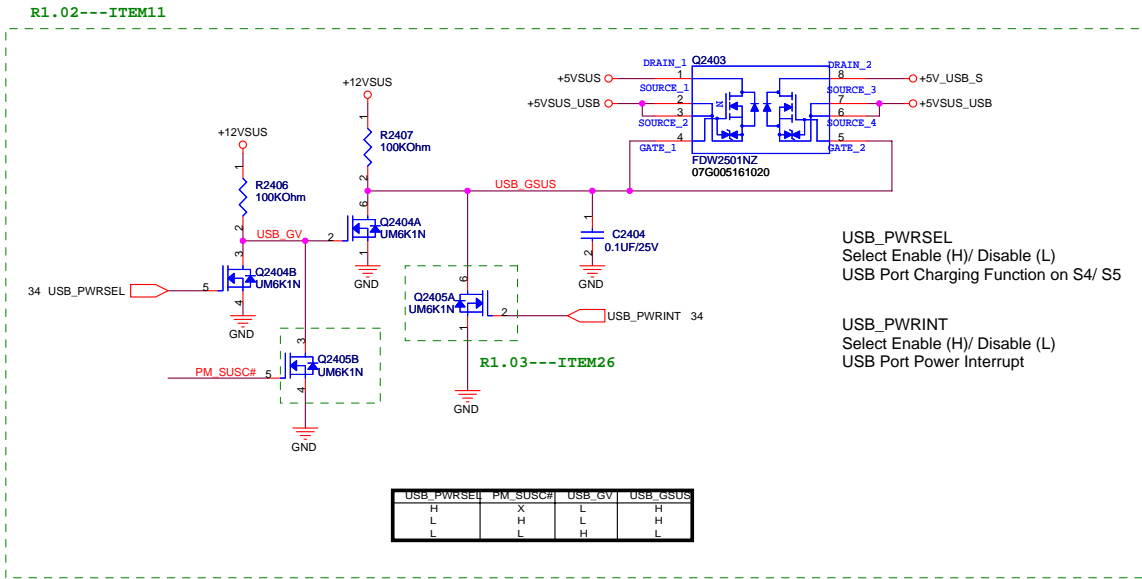
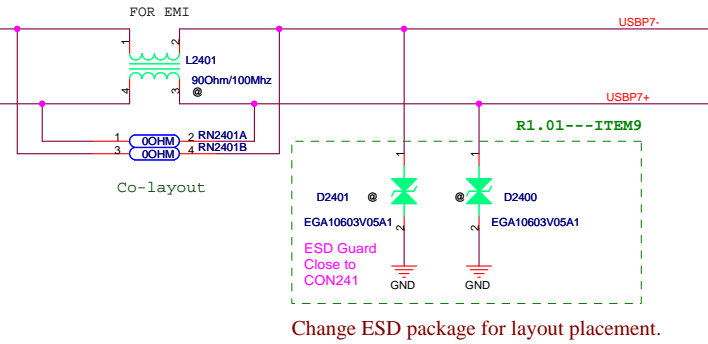
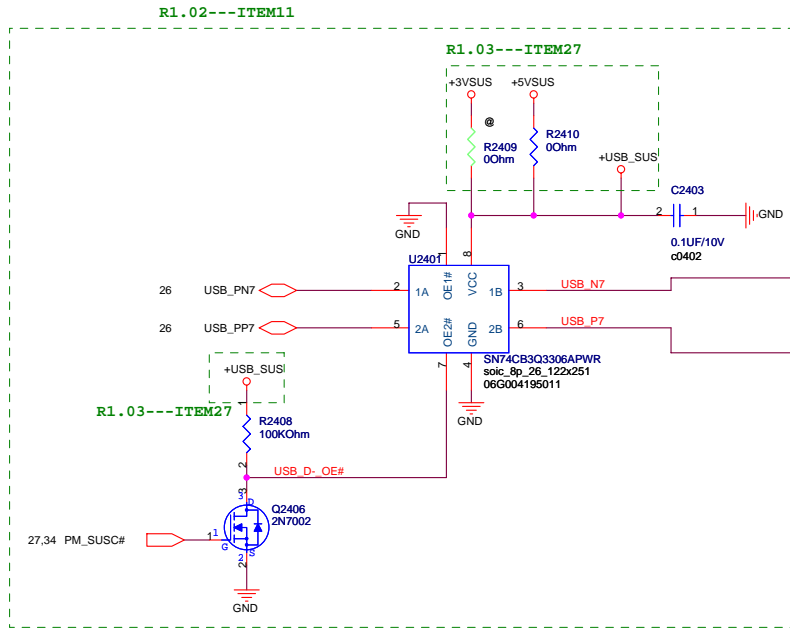
SATA HDD CON



PATA CD-ROM CON

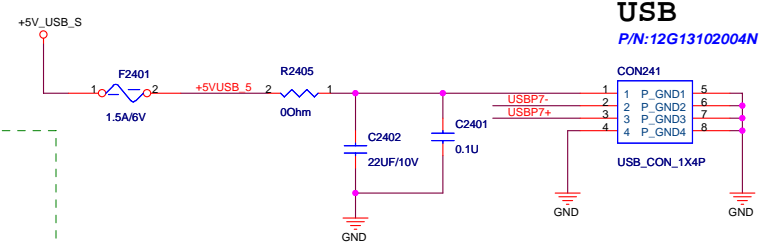


<Variant Names>

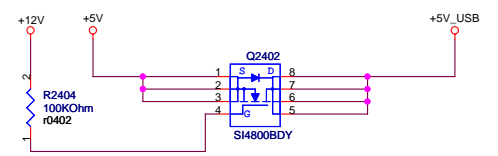


USB_PWRSEL
Select Enable (H)/ Disable (L)
USB Port Charging Function on S4/ S5

USB_PWRINT
Select Enable (H)/ Disable (L)
USB Port Power Interrupt

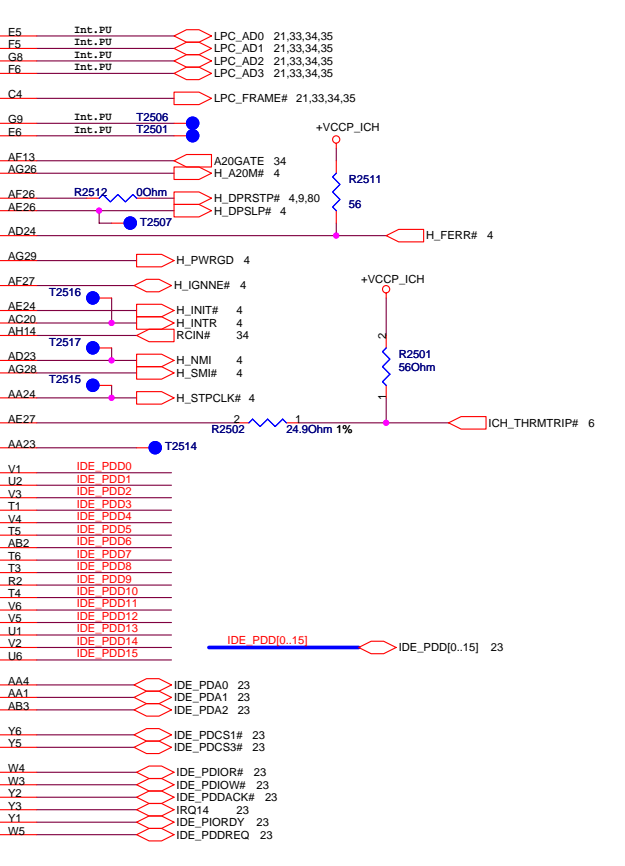
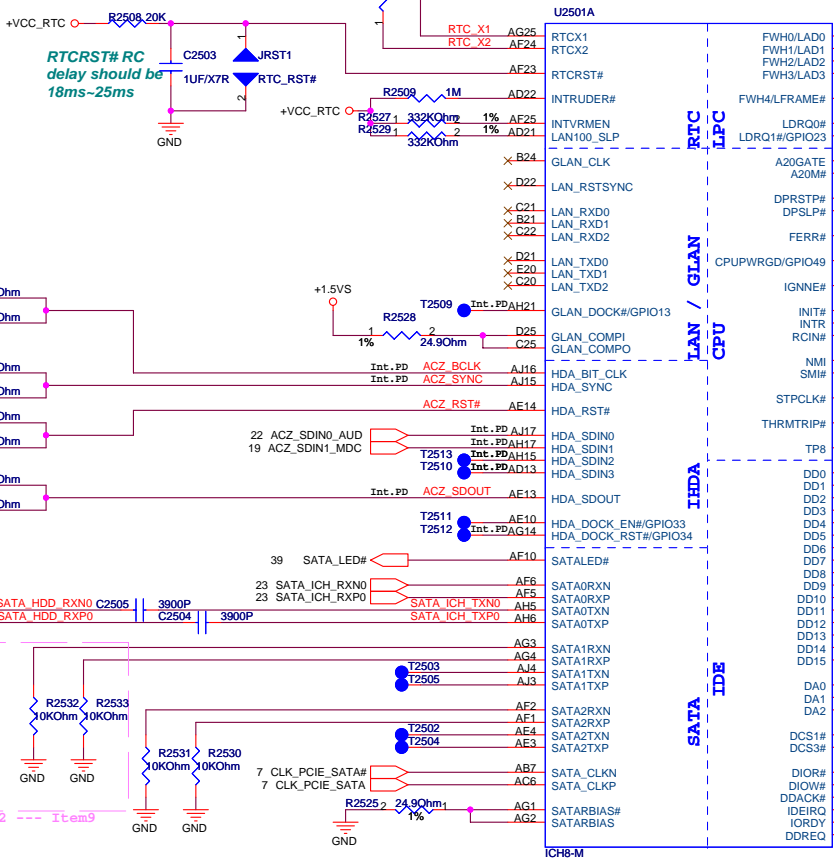
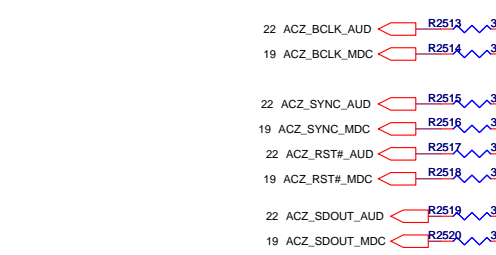
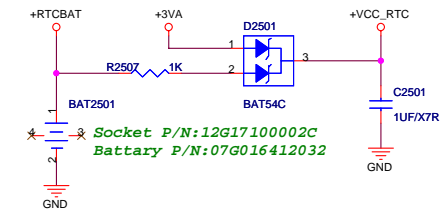
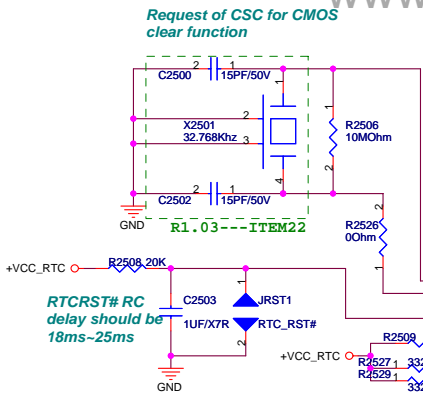
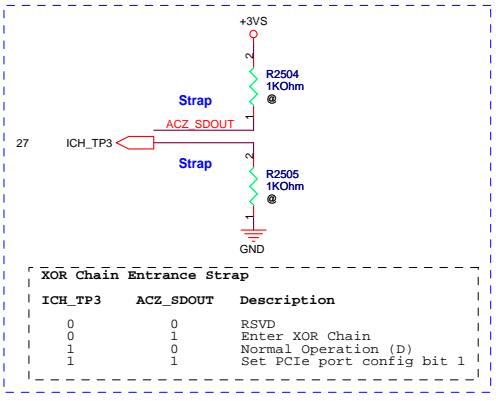


USB
P/N: 12G13102004N



<Variant Name>

ASUS		Title : USB PORTS	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name F9S	Rev 1.1	
Date: Friday, March 02, 2007		Sheet 24 of 94	



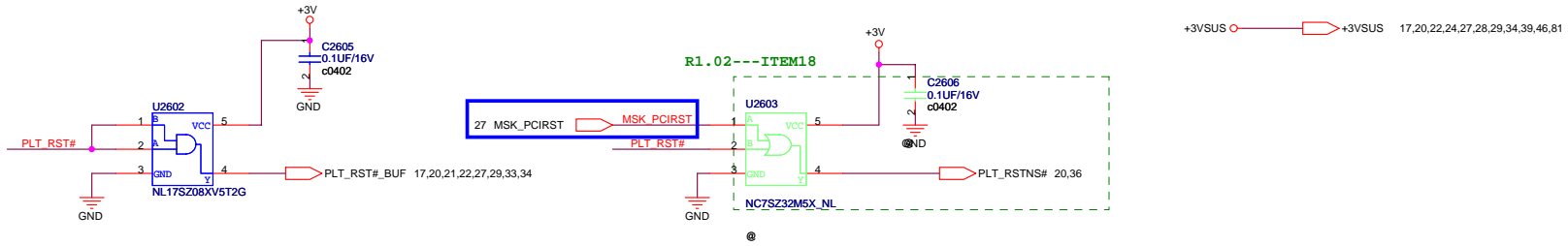
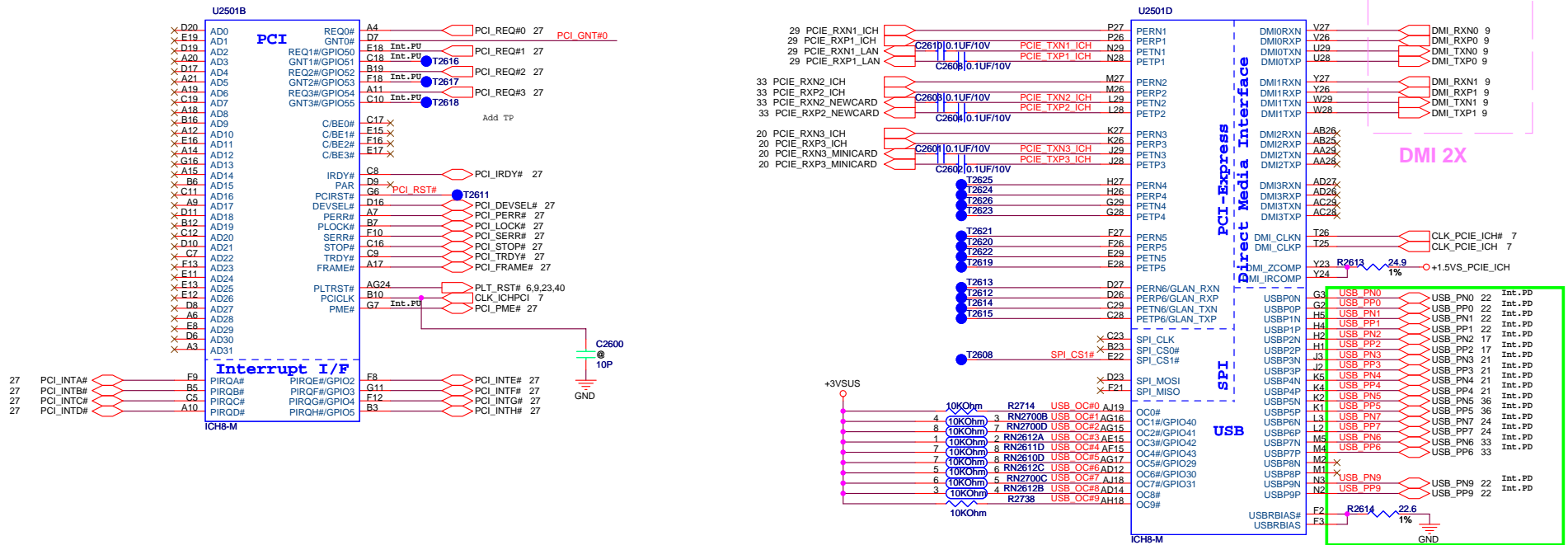
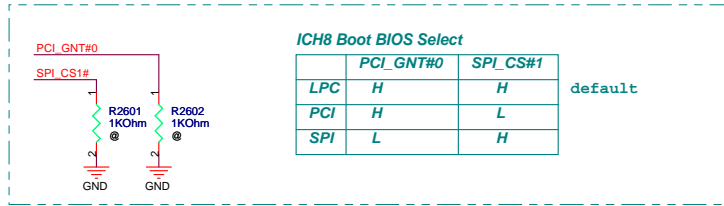
<Variant Name>

ASUS Title : ICH8-M (1)

ASUSTek COMPUTER INC Engineer: <OrgAddr>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 25 of 94



USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Camera
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	Card Reader
USB 6	Newcard
USB 7	USB Conn.
USB 8	NC
USB 9	WWAN

<Variant Name>

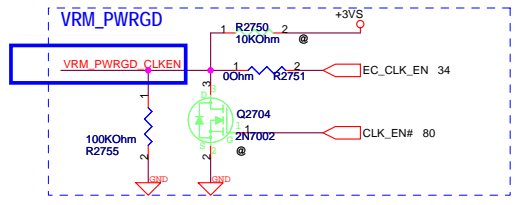
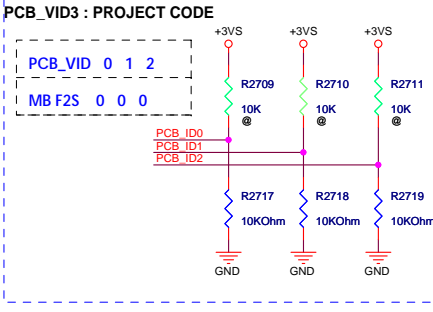
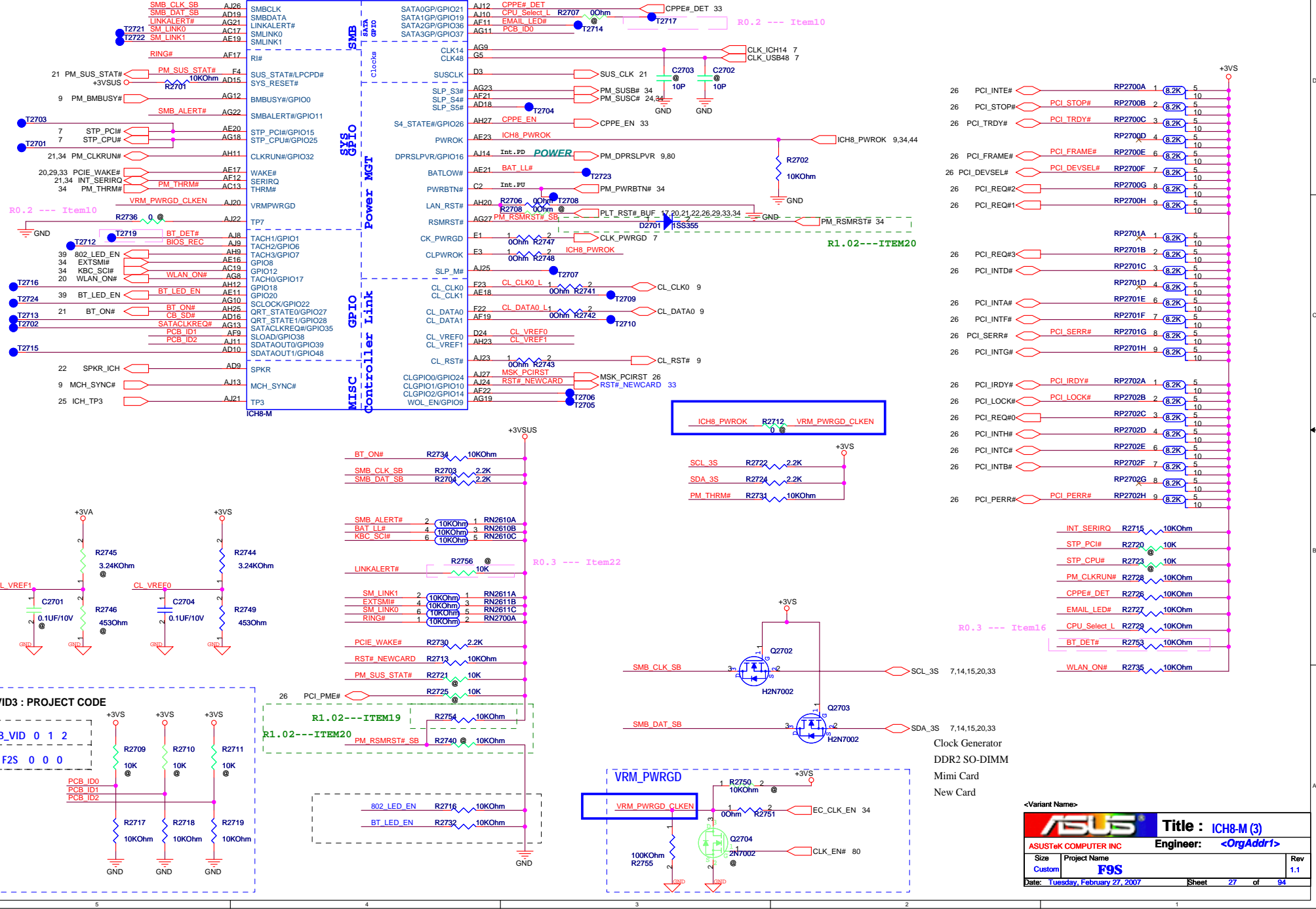
ASUS Title : **ICH8-M (2)**

ASUSTek COMPUTER INC Project Name Engineer: <OrgAddr>

Size Project Name Rev
 Custom **F9S** 1.1

Date: Tuesday, February 27, 2007 Sheet 26 of 94

U2501C



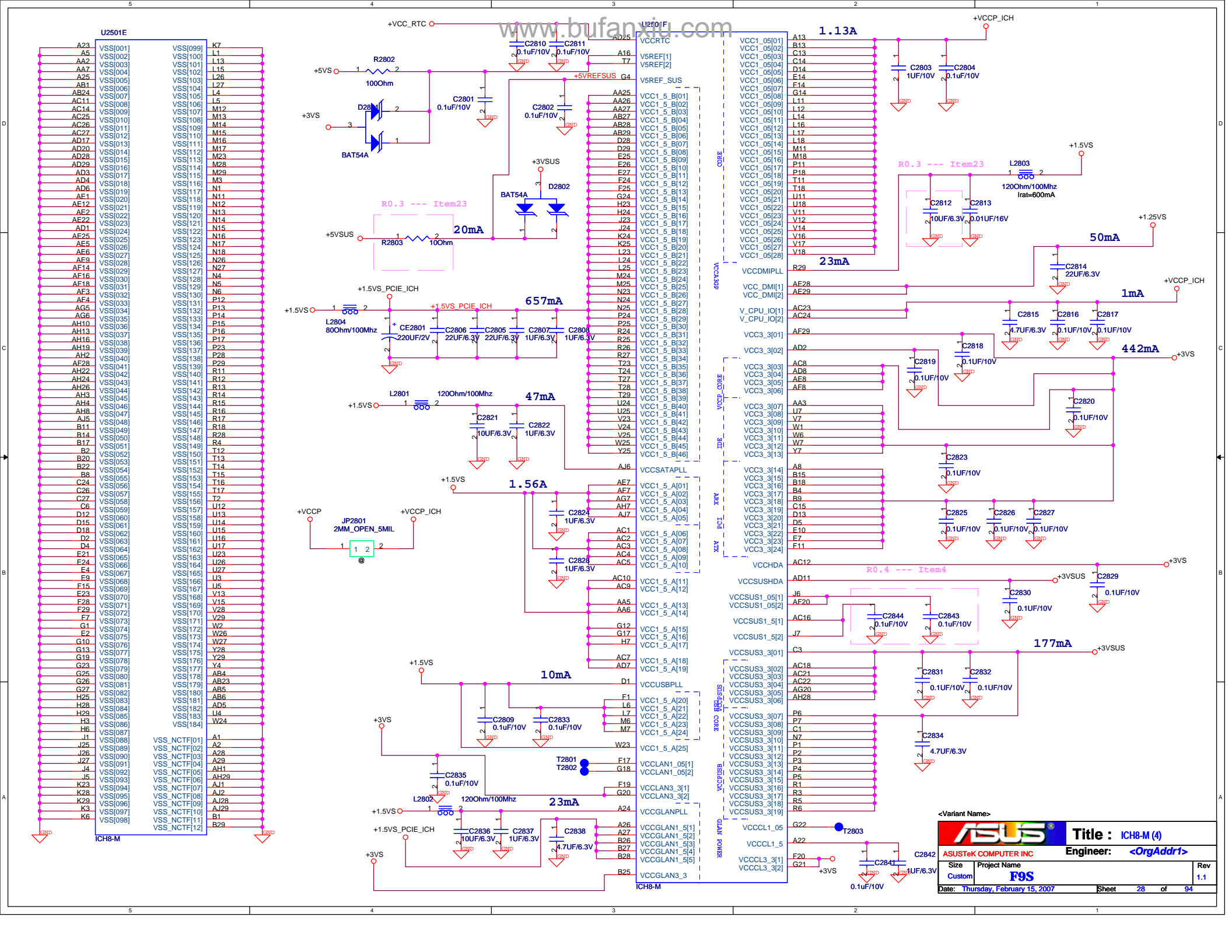
<Variant Name>

ASUS Title : ICH8-M (3)
ASUSTek COMPUTER INC Engineer: <OrgAddr>

Size	Project Name	Rev
Custom	F9S	1.1

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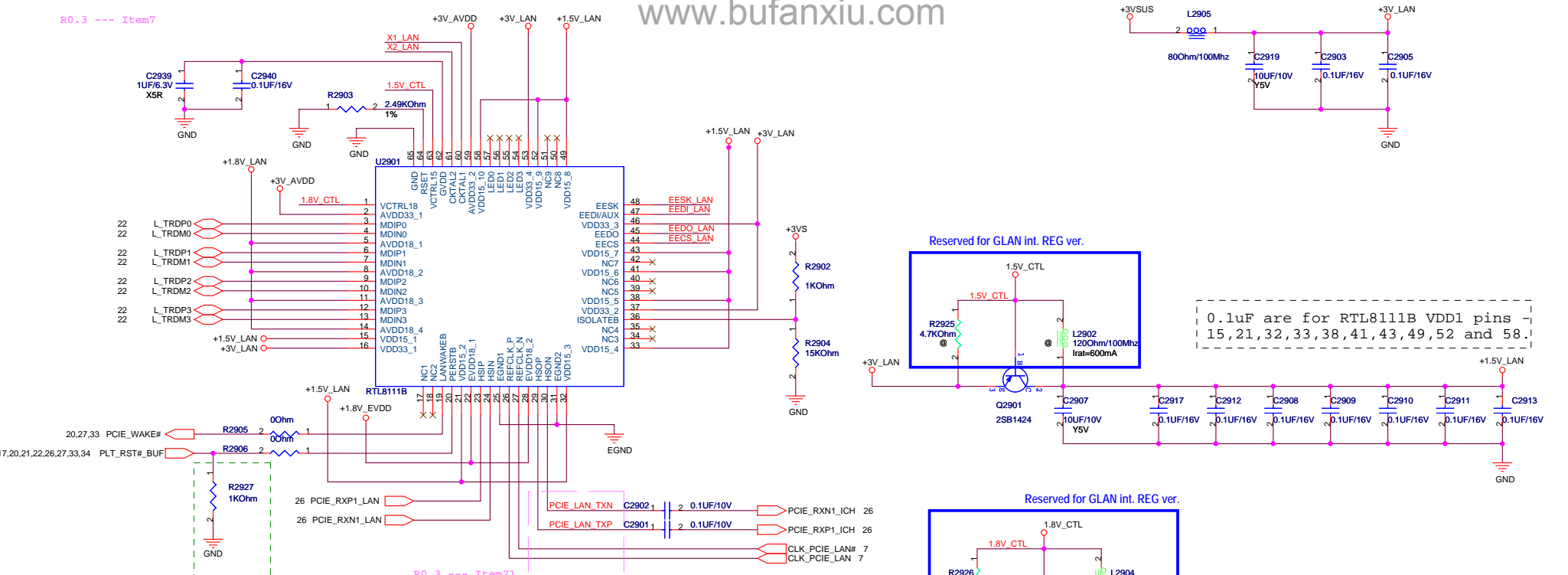
Clock Generator
DDR2 SO-DIMM
Mimi Card
New Card



<Variant Name>

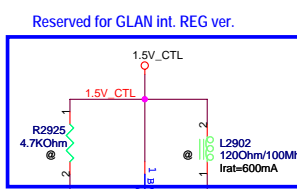
ASUS		Title : ICH8-M (4)	
ASUSTeK COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name	F9S	Rev 1.1
Custom			
Date: Thursday, February 15, 2007		Sheet 28 of 94	

R0.3 --- Item7

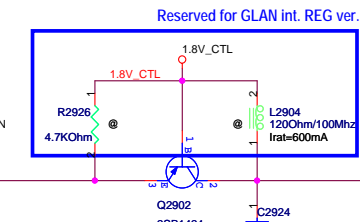


R0.3 --- Item21

Avoid current leakage from LAN when RST#



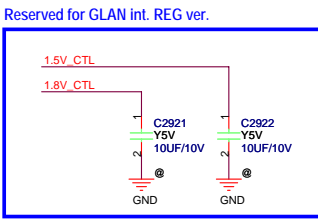
0.1uF are for RTL8111B VDD1 pins - 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.



0.1uF are for AVDDL pins - 5, 8, 11 and 14

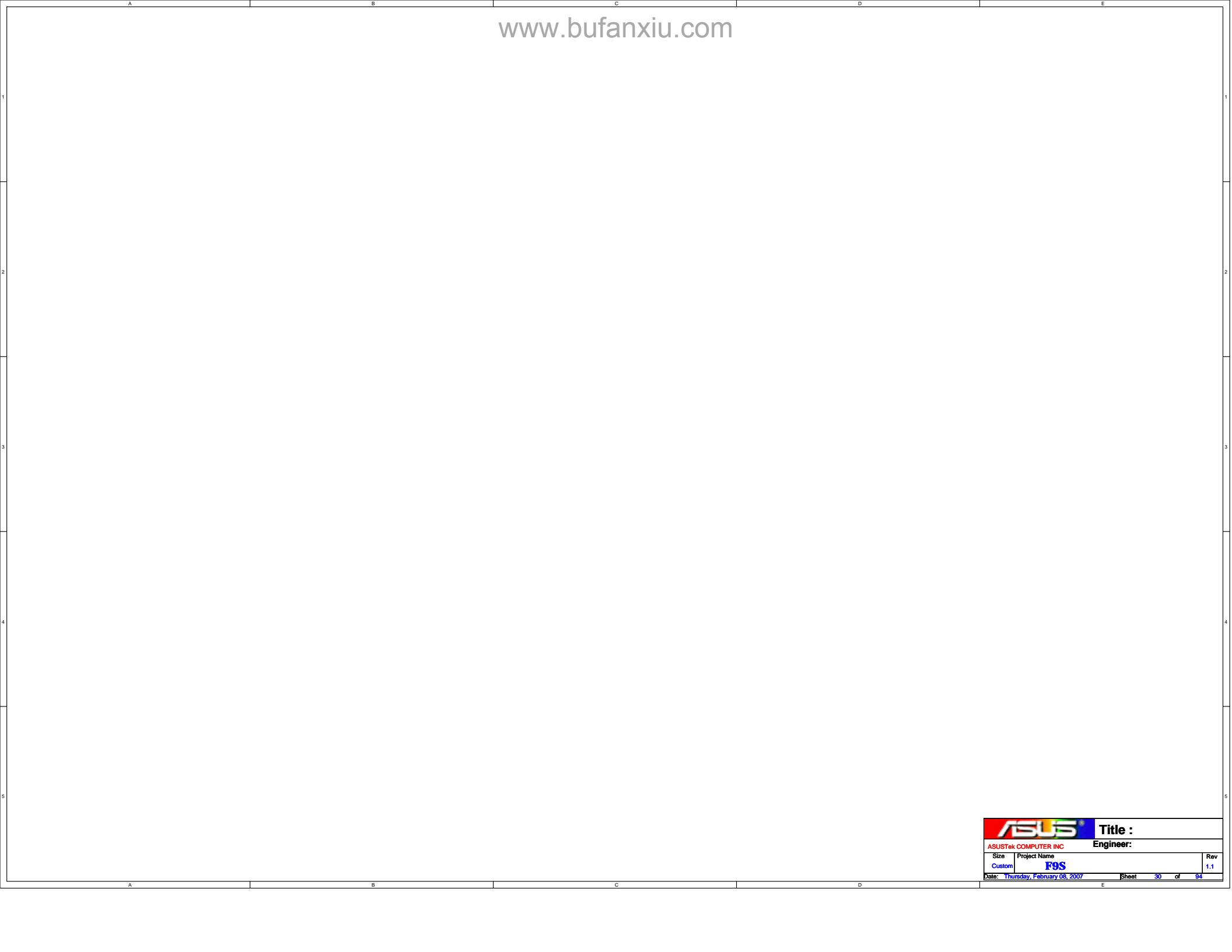
Caps are for VDD1A pins


0.1uF are for AVDDH pins - 2 and 59.

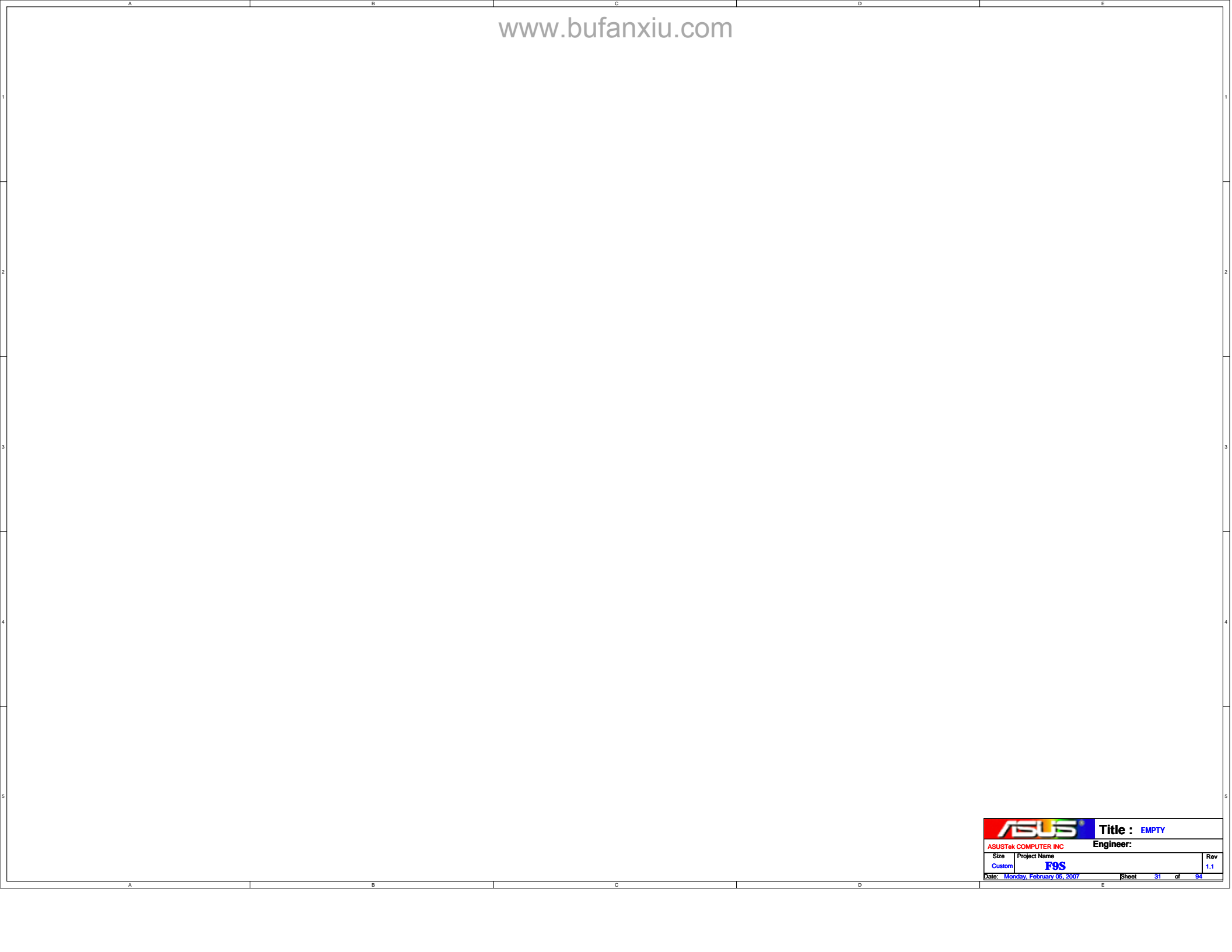


<Variant Name>

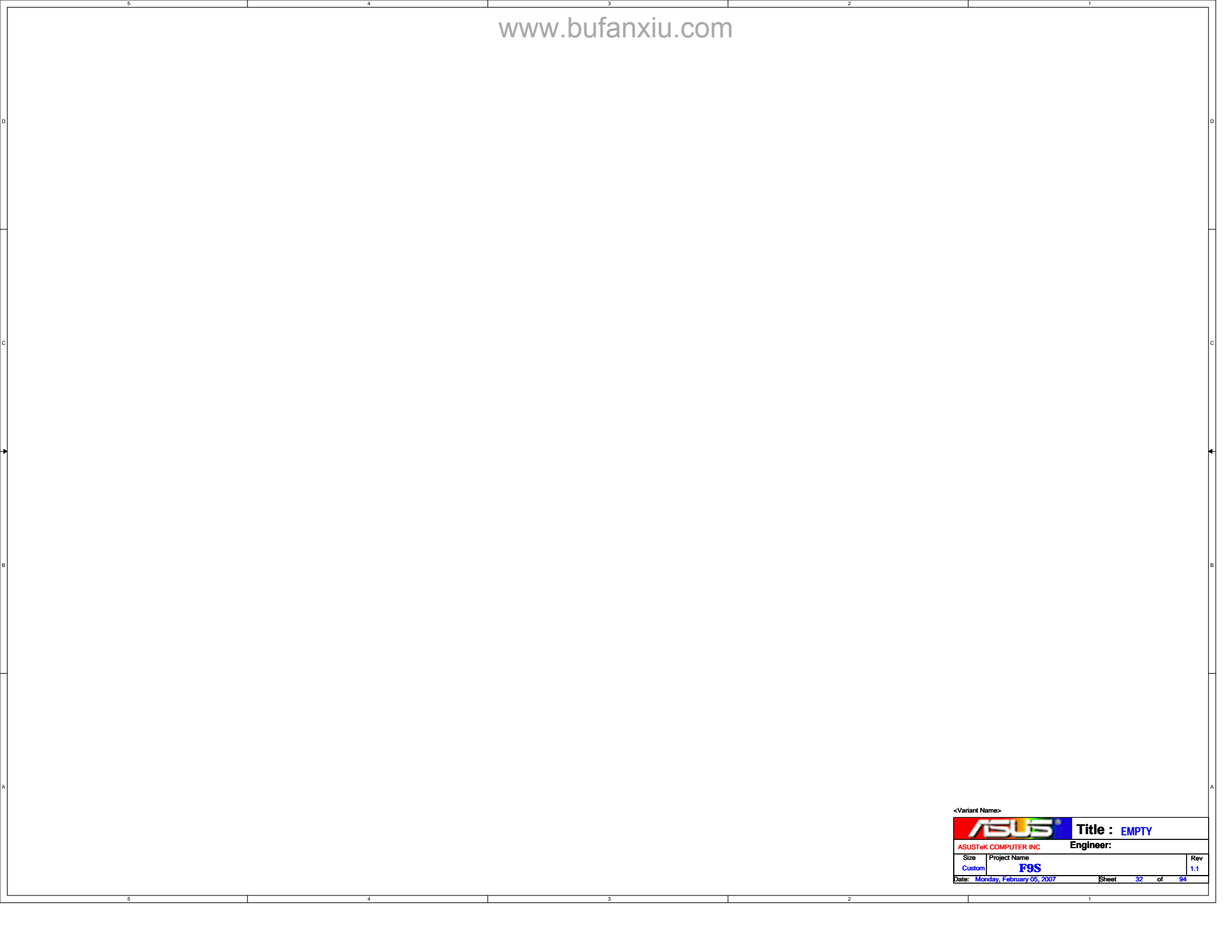
ASUS		Title : LAN RTL8111B	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date:	Tuesday, February 27, 2007	Sheet	29 of 94



		Title :	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Thursday, February 08, 2007		Sheet	30 of 94



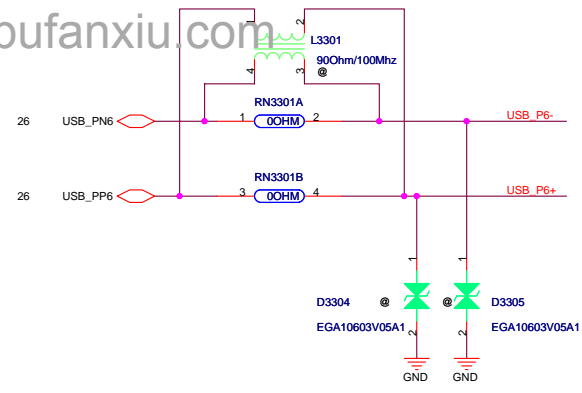
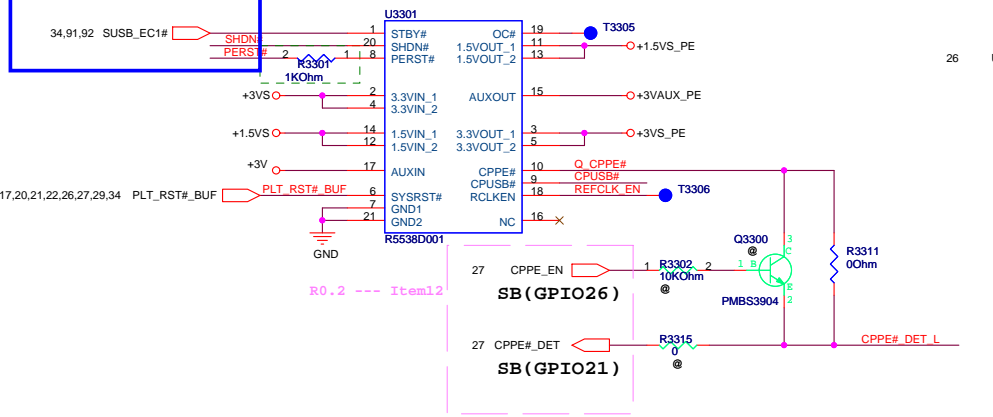
		Title : EMPTY	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Monday, February 05, 2007		Sheet	31 of 94



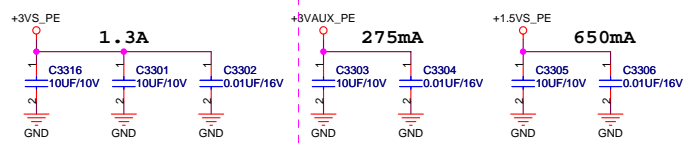
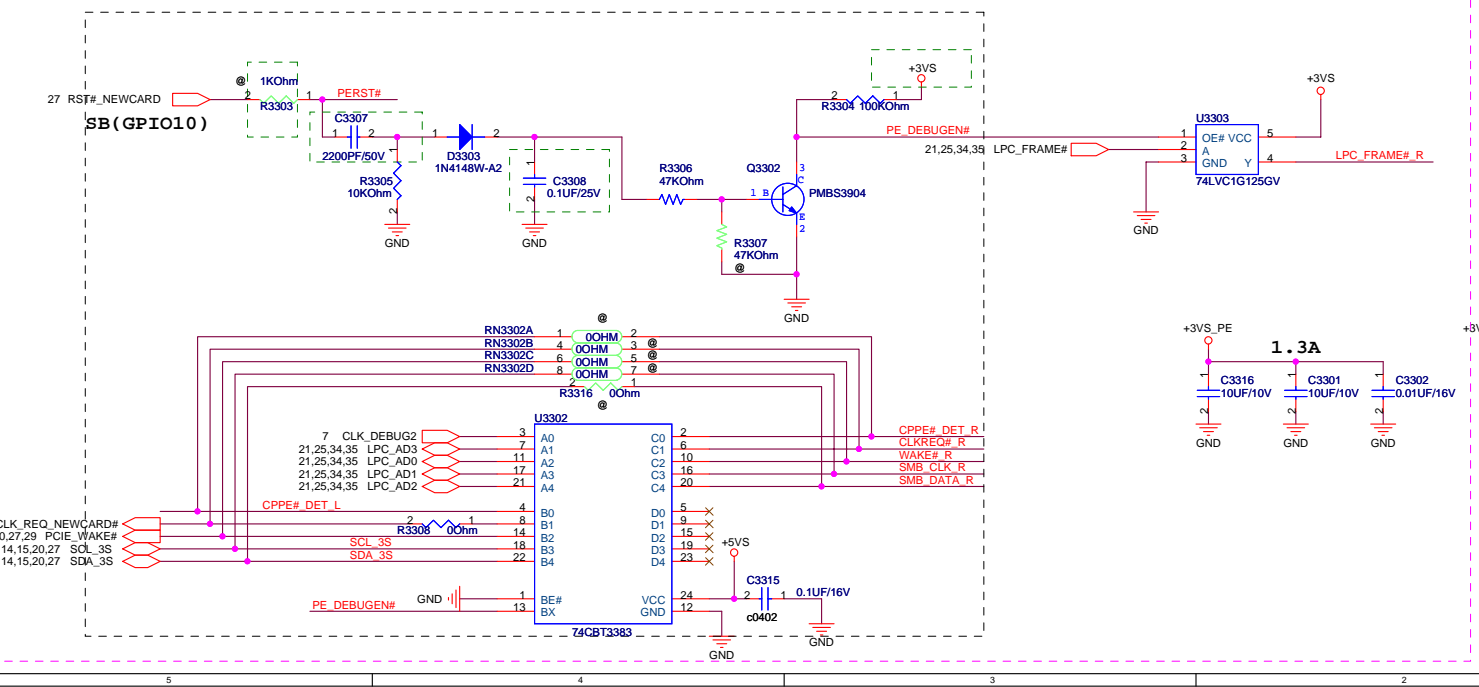
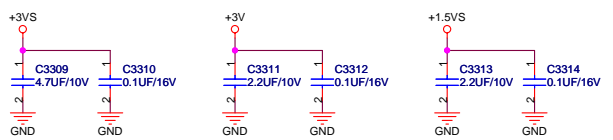
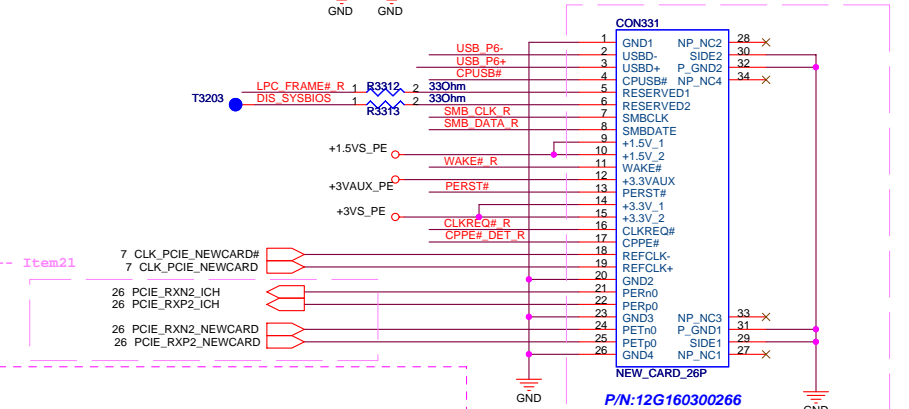
<Variant Name>

		Title : EMPTY	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Monday, February 05, 2007		Sheet	32 of 94

New EC pin to avoid the re-recognize when resume from S3/S4.



NewCard Header

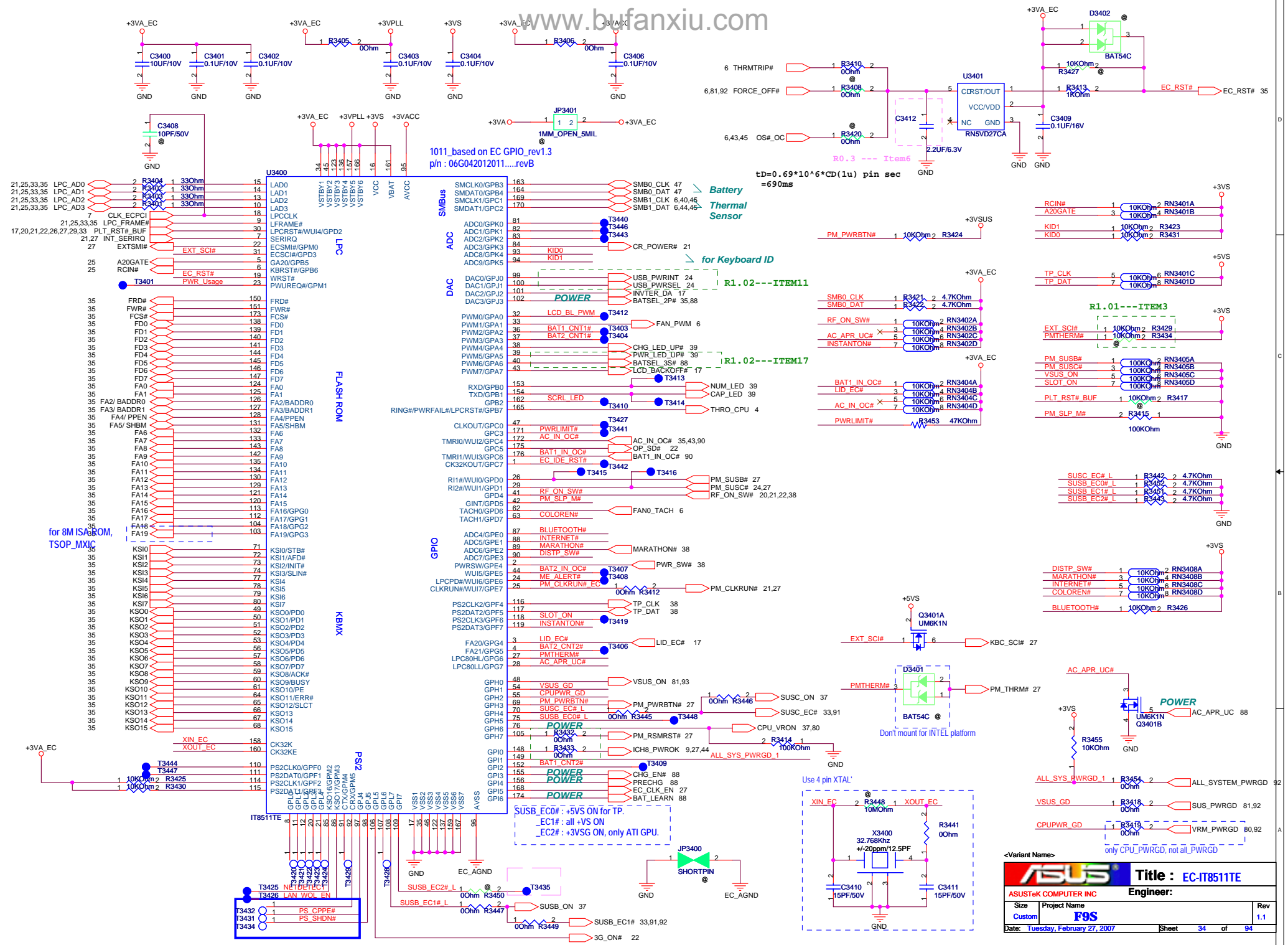


ASUSTek COMPUTER INC. ASUS

4 FL_No.150, Li-Te Rd.,Pailou, Taipei,Taiwan, ROC

Title: **NEW CARD**

Size Custom	Document Number	Rev
F9S		1.1
Date: Tuesday, February 27, 2007	Sheet	33 of 94



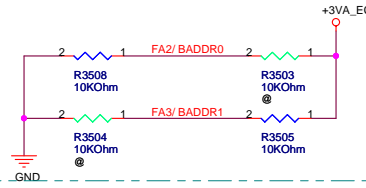
ASUS Title: EC-IT851ITE
 ASUSTeK COMPUTER INC Engineer:
 Size Project Name
 Custom F9S
 Date: Tuesday, February 27, 2007 Sheet 34 of 94

ISA ROM_TSOP

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

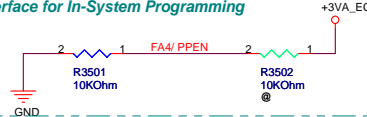
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
- 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
- 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

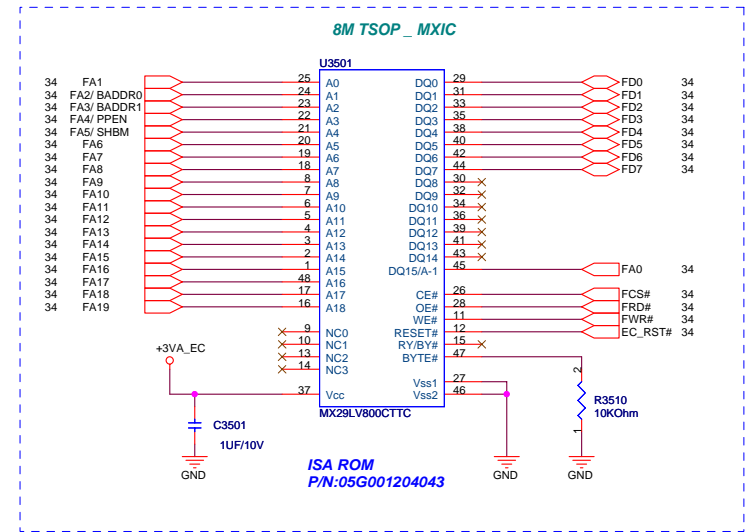
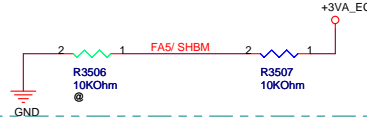
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



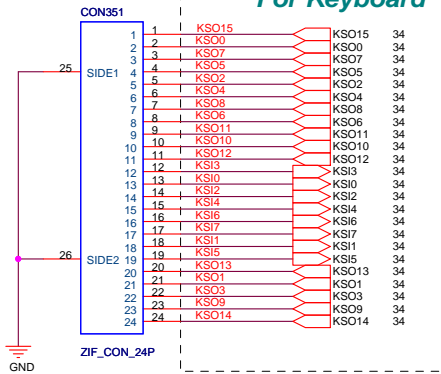
FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

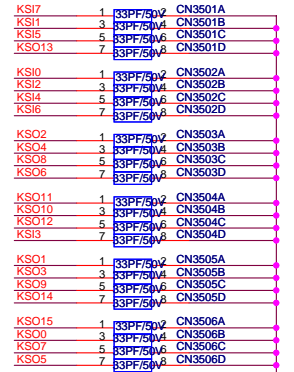


P/N:12G182402404

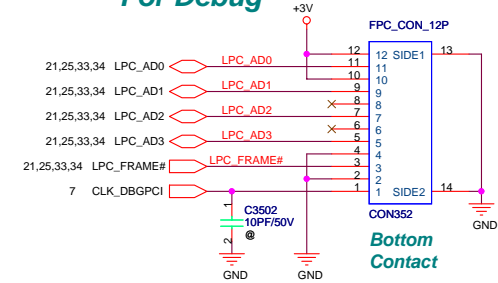
For Keyboard



R1.3---ITEM38

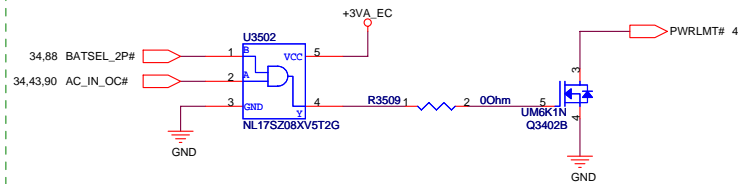


For Debug



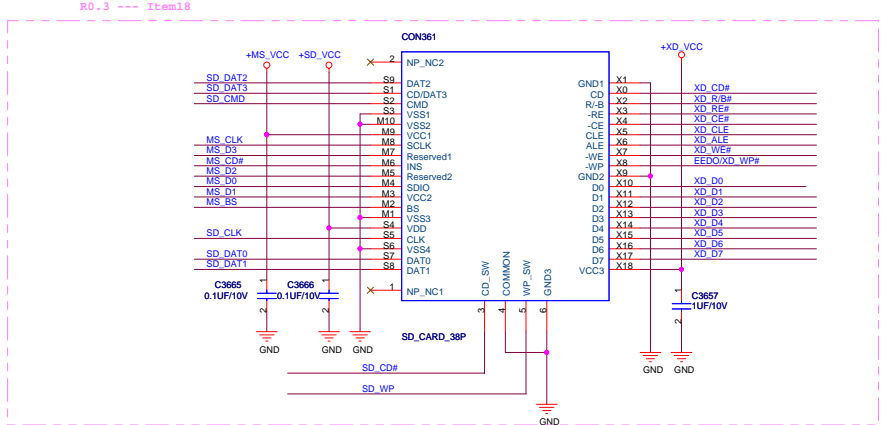
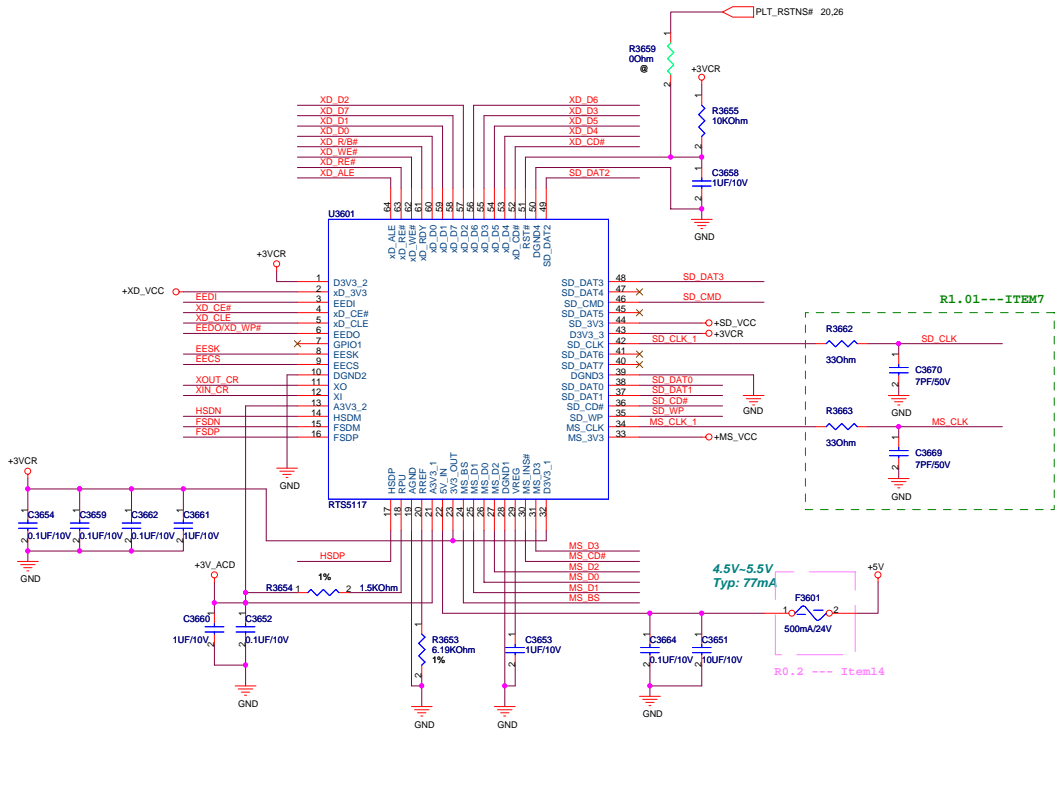
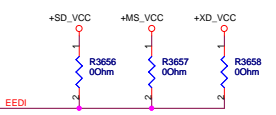
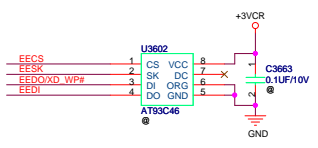
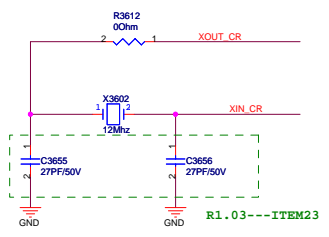
R1.03---ITEM28

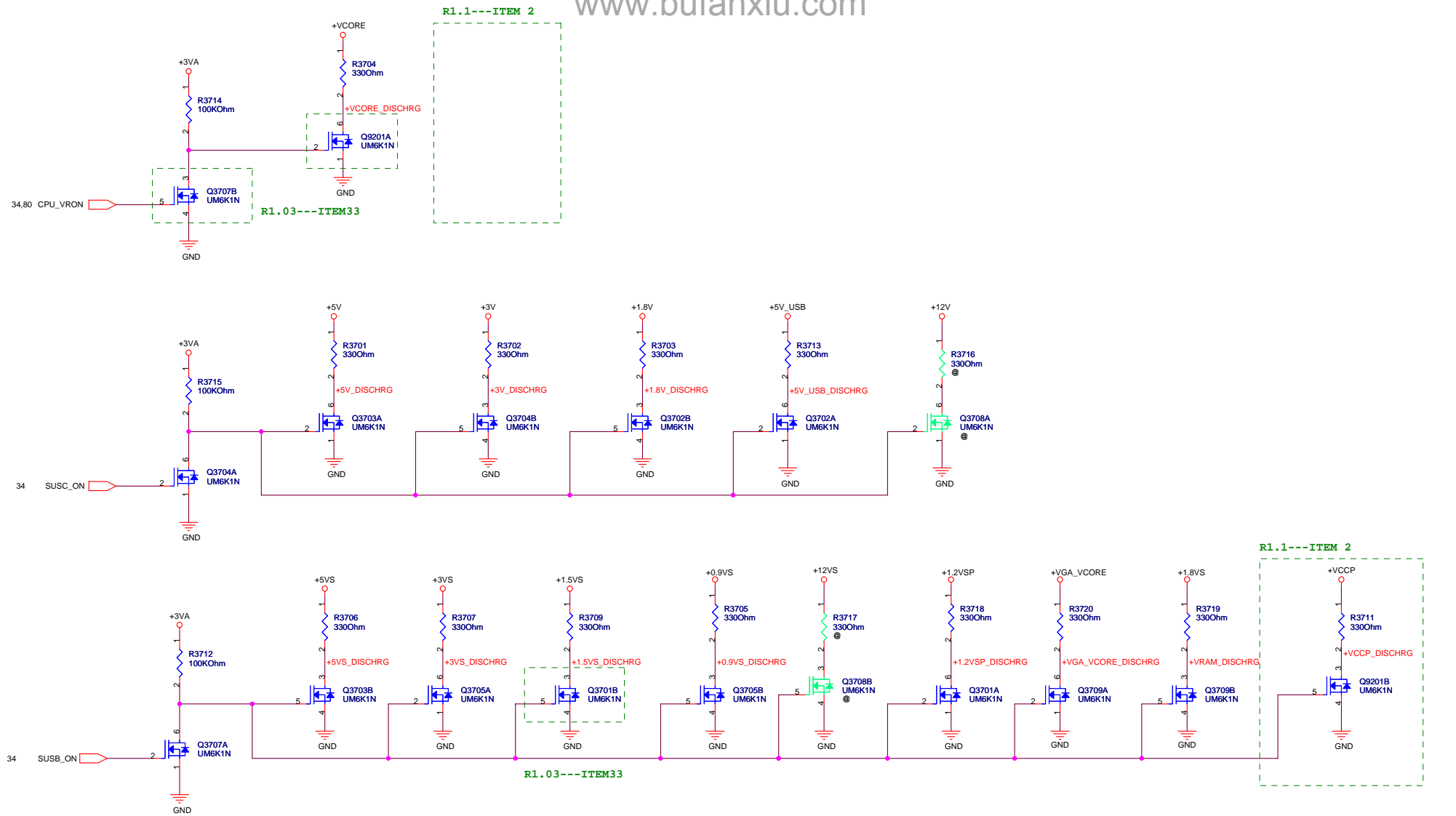
PWRLMT Circuit: For Battery 1P



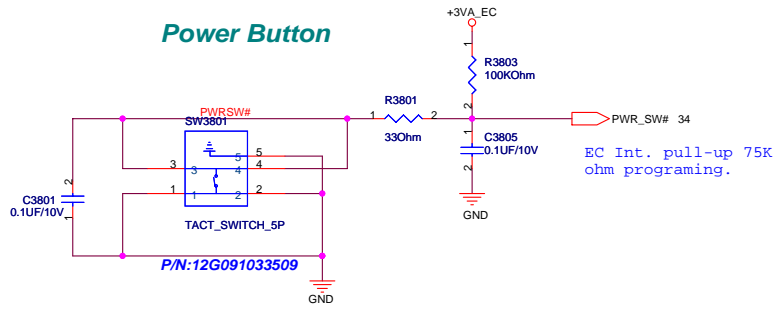
<Variant Names>

ASUS		Title : ISA_ROM&KB conn	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
Date: Tuesday, February 27, 2007	Sheet	35	of 94

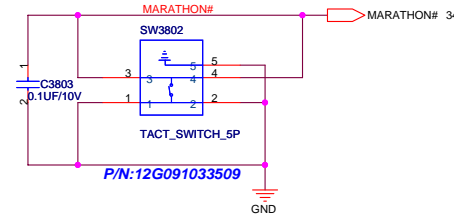




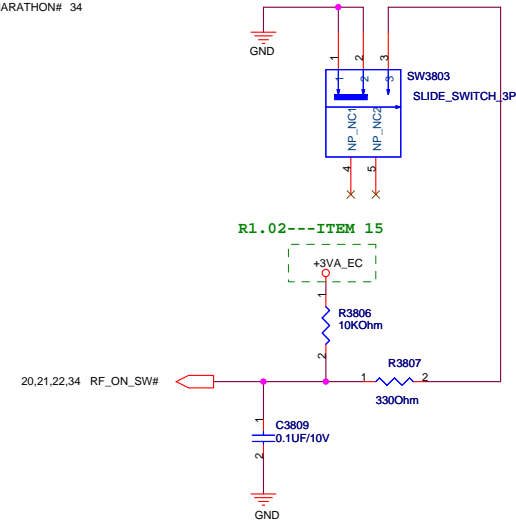
Power Button



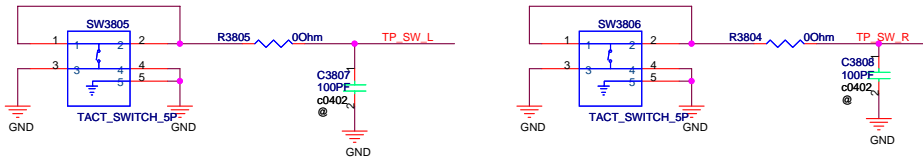
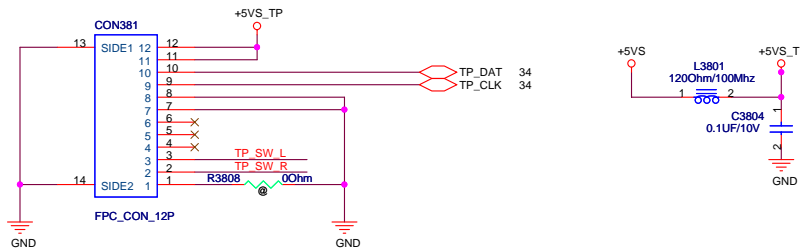
MARATHON#



BT/WLAN SW



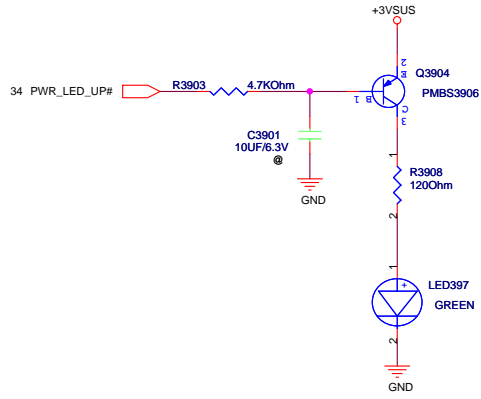
Touch-Pad



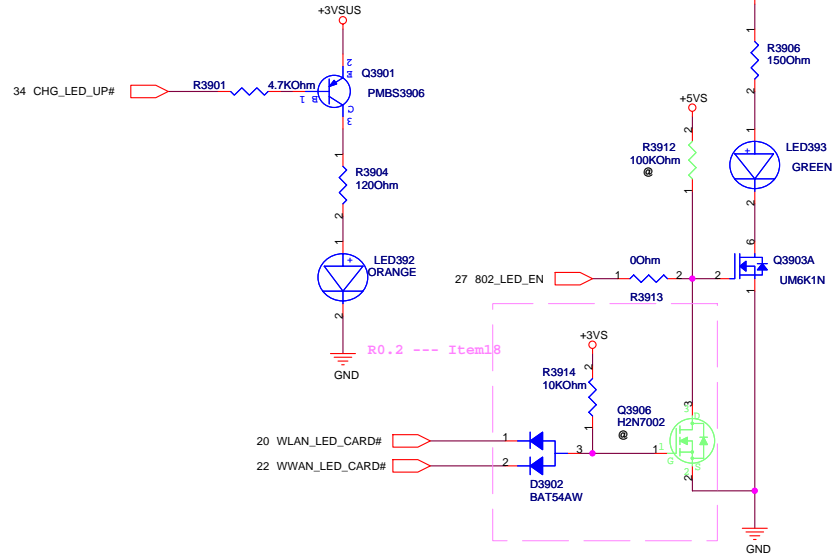
<Variant Name>

ASUS		Title : KEY & LED	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F9S	1.1	
Date:	Tuesday, February 27, 2007	Sheet	38 of 94

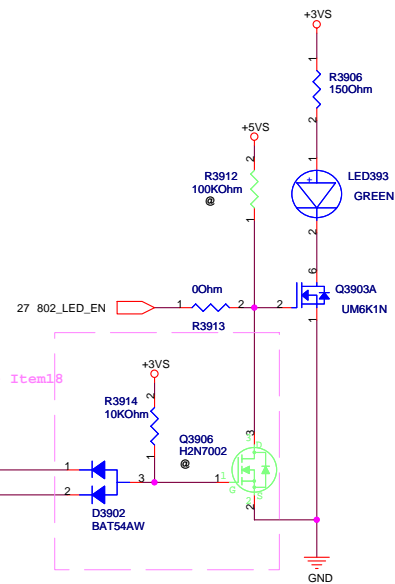
PWR LED



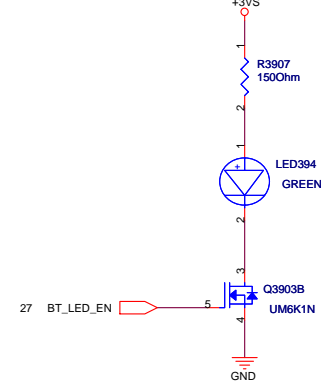
BATTERY LED



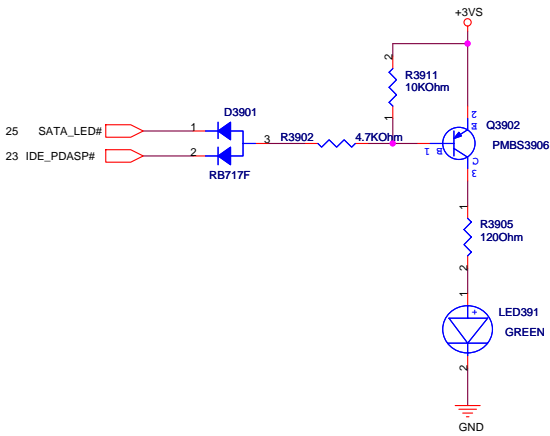
WireLess LED



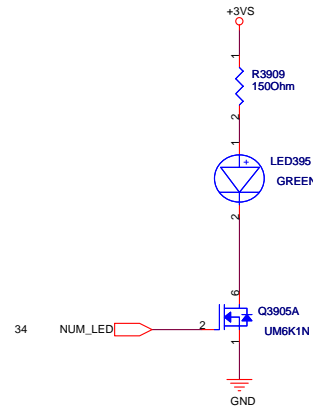
BT LED



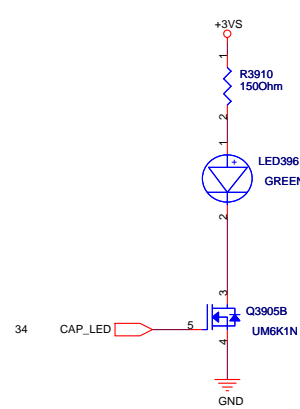
SATA/IDE LED



Num Lock



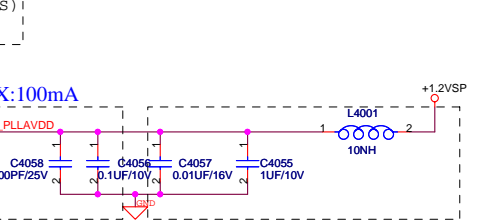
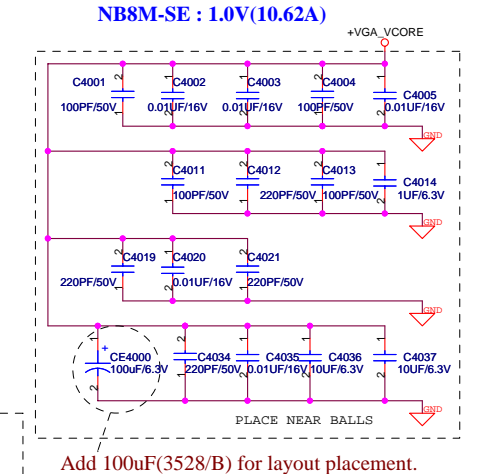
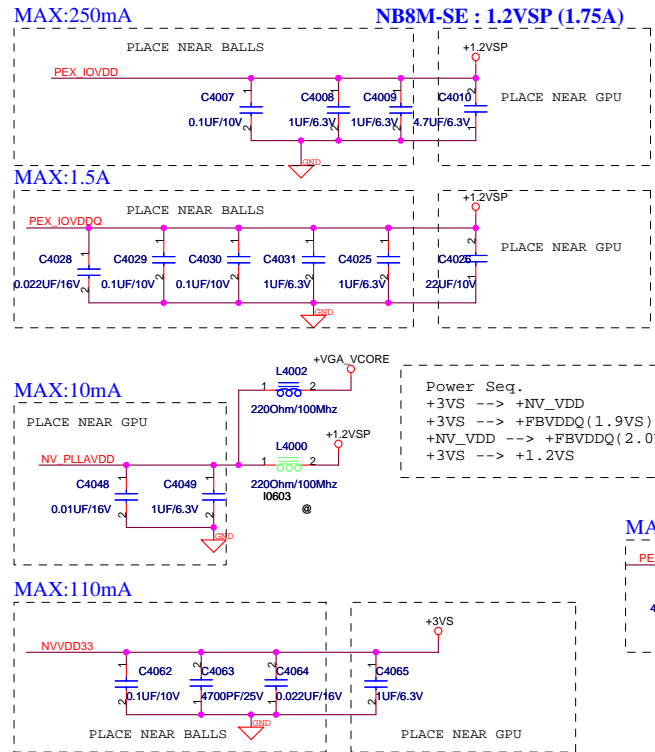
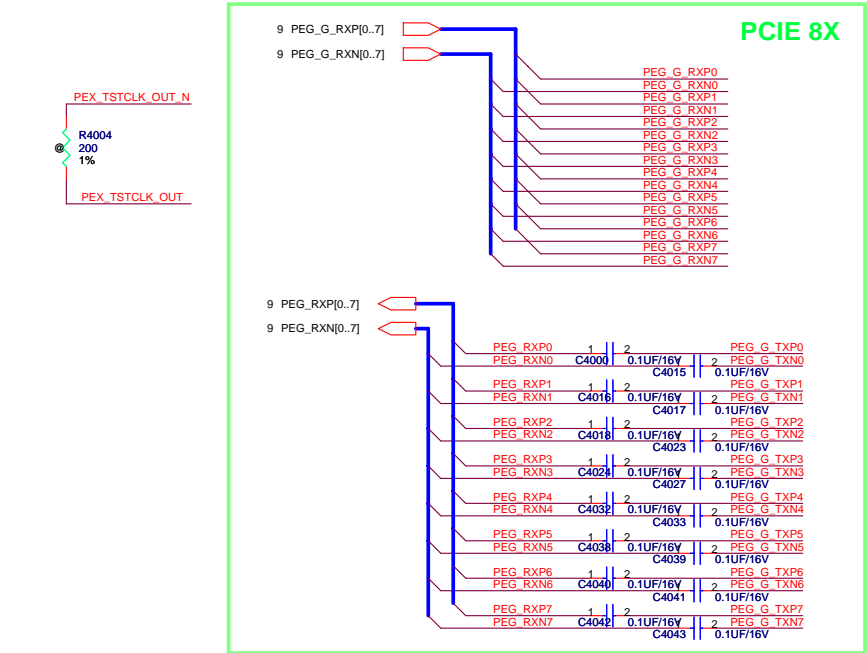
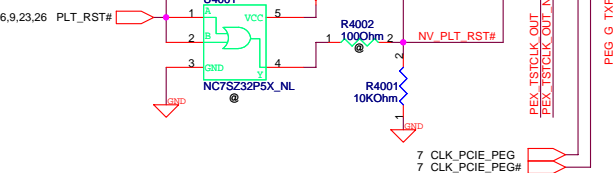
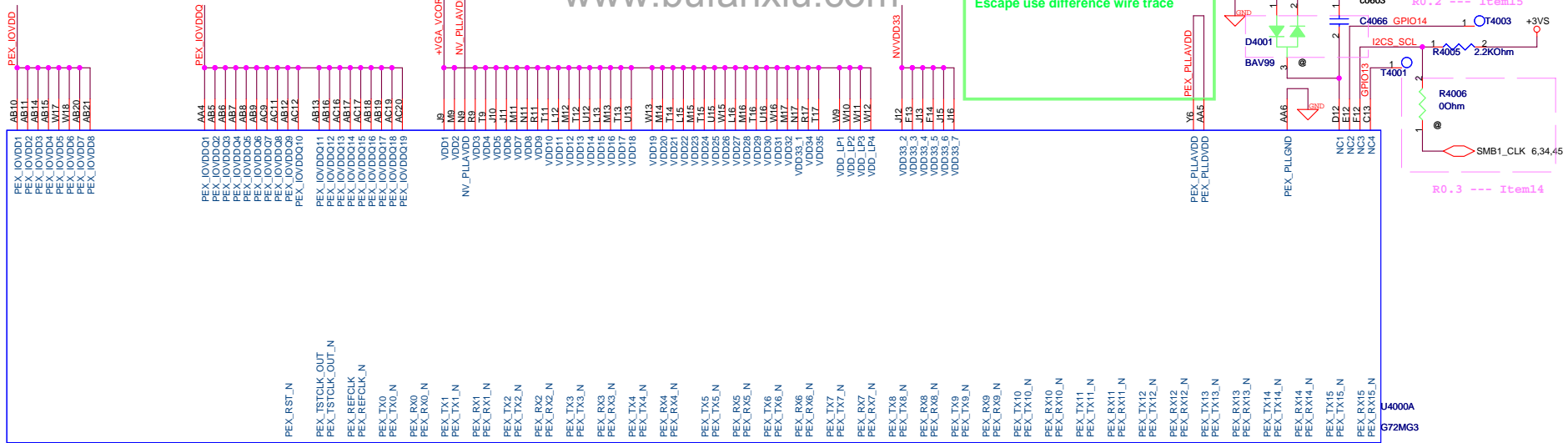
Cap. Lock



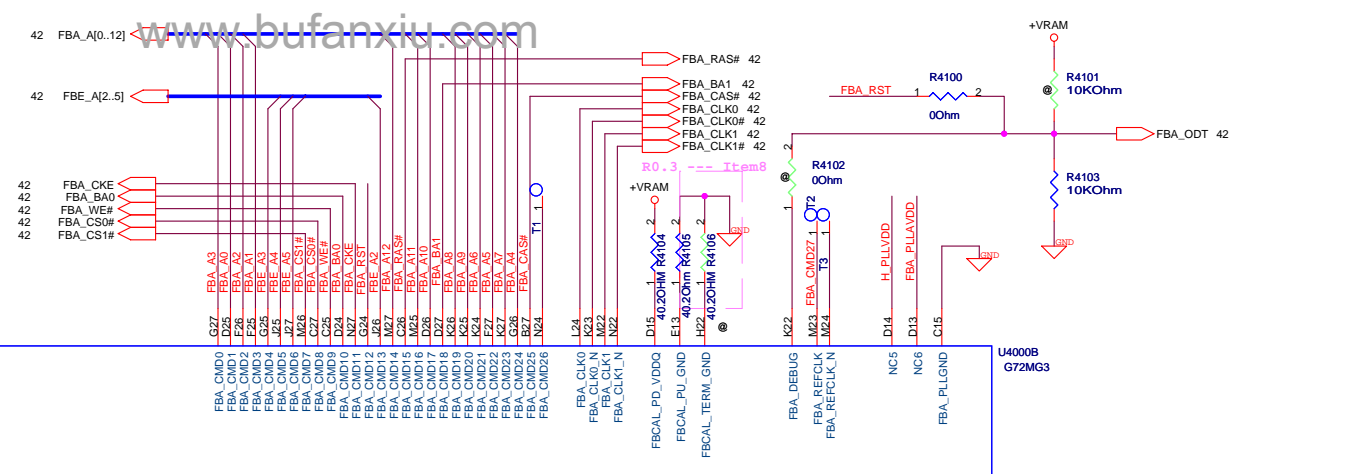
<Variant Name>

ASUS		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer:	
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Escape use difference wire trace

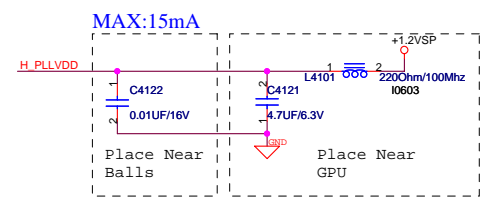
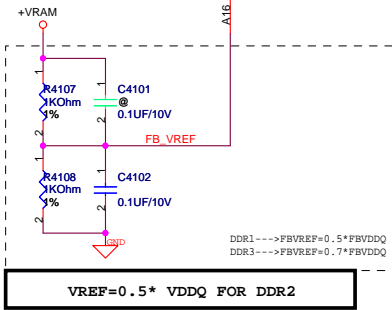
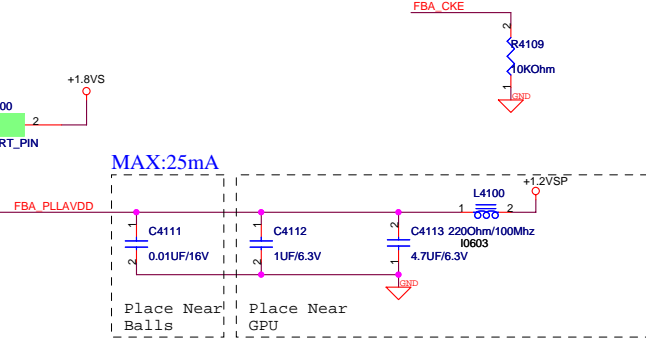
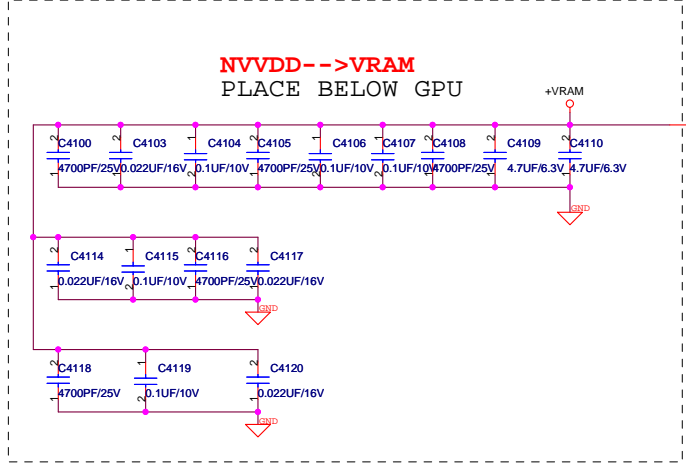


ASUS Title : G72MV-PCIE (1)
 ASUSTEK COMPUTER INC Engineer:
 Size Custom Project Name **F9S**
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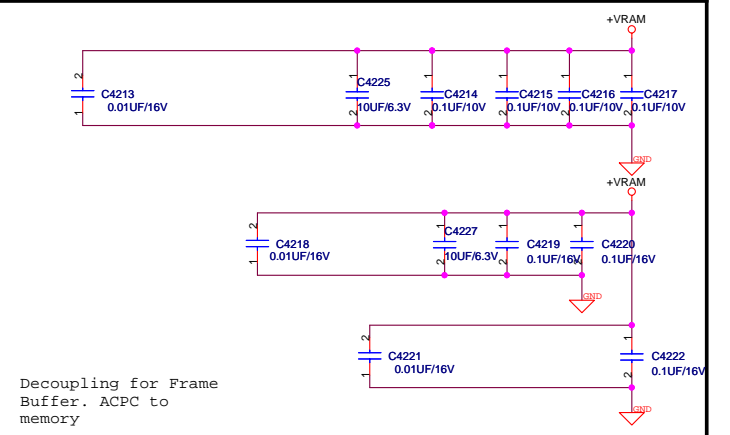
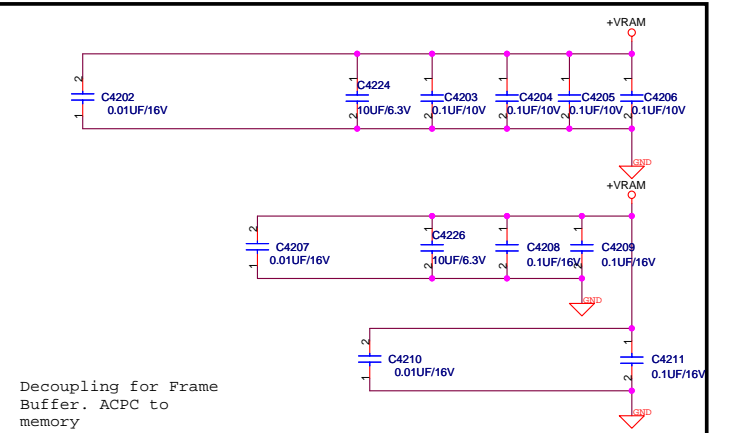
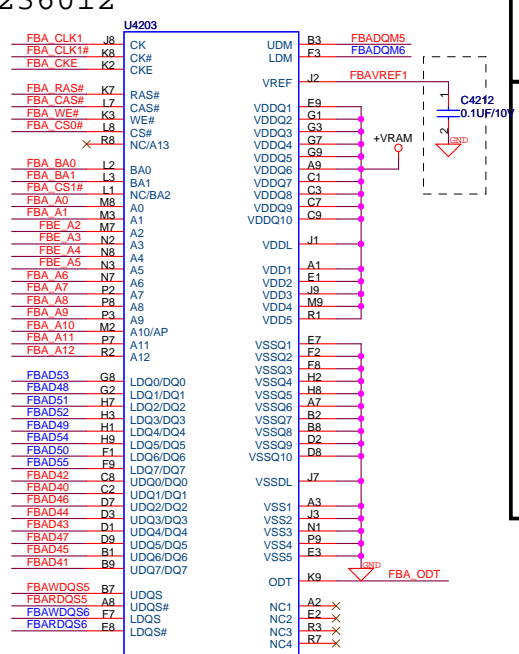
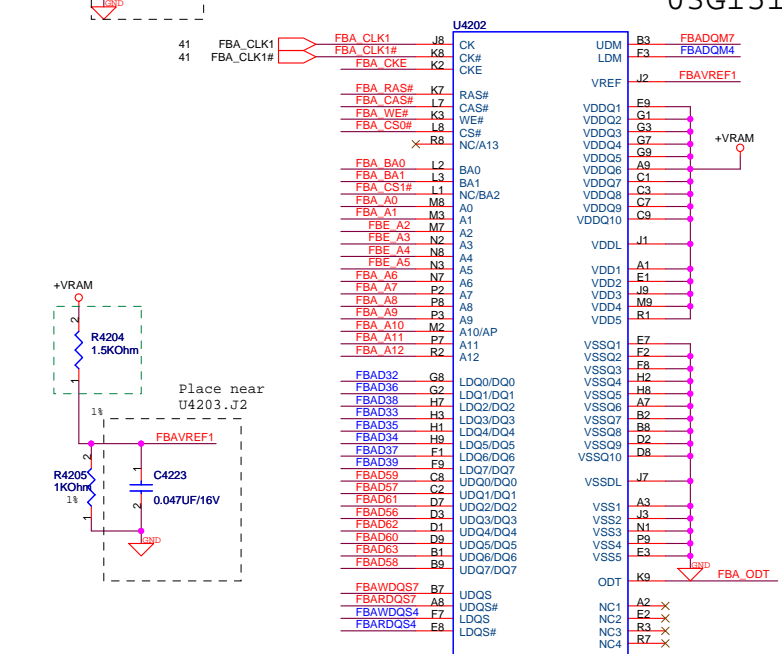
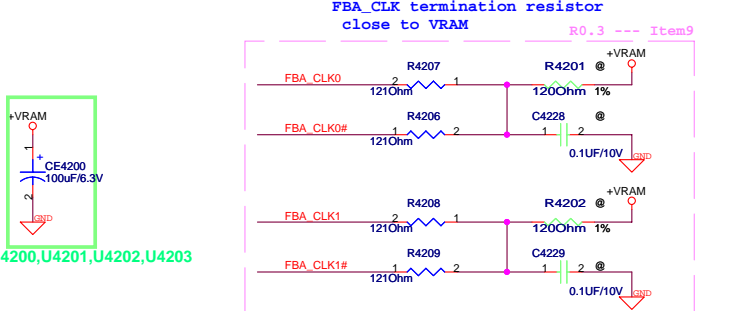
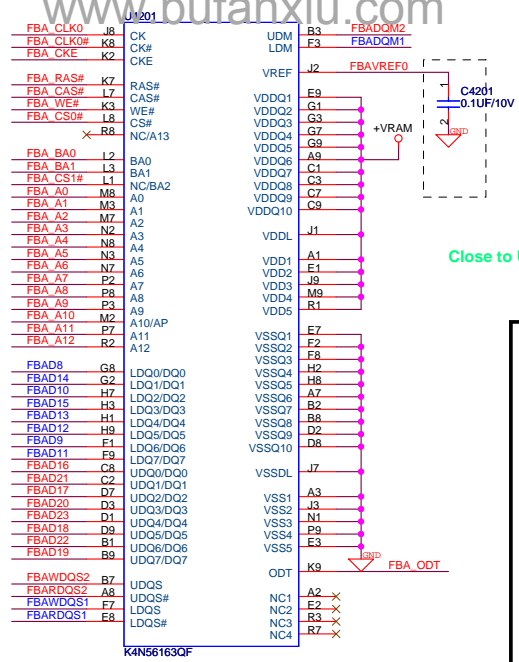
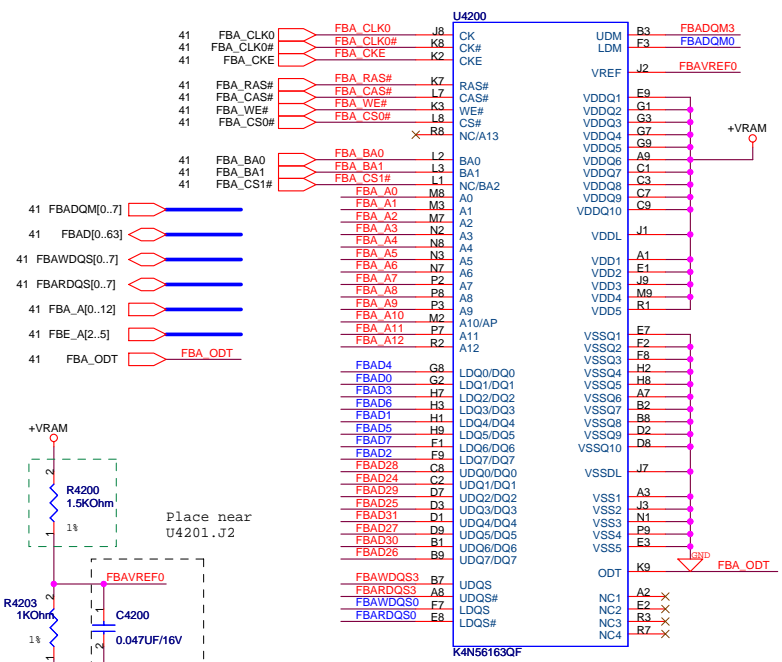
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G72M:MAX:2.075A
G72M-V:MAX:1A

GDDR2 16x16 FBVDDQ 1.8V 84PIN

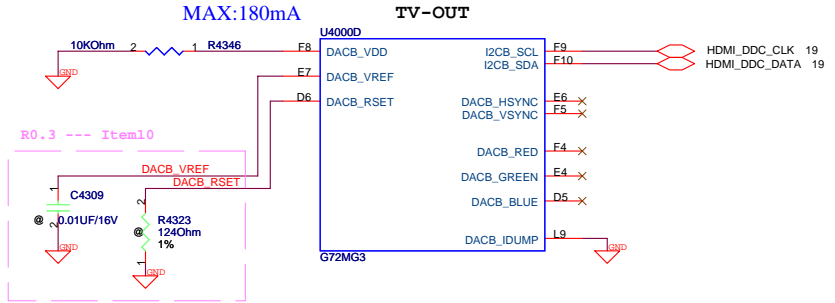
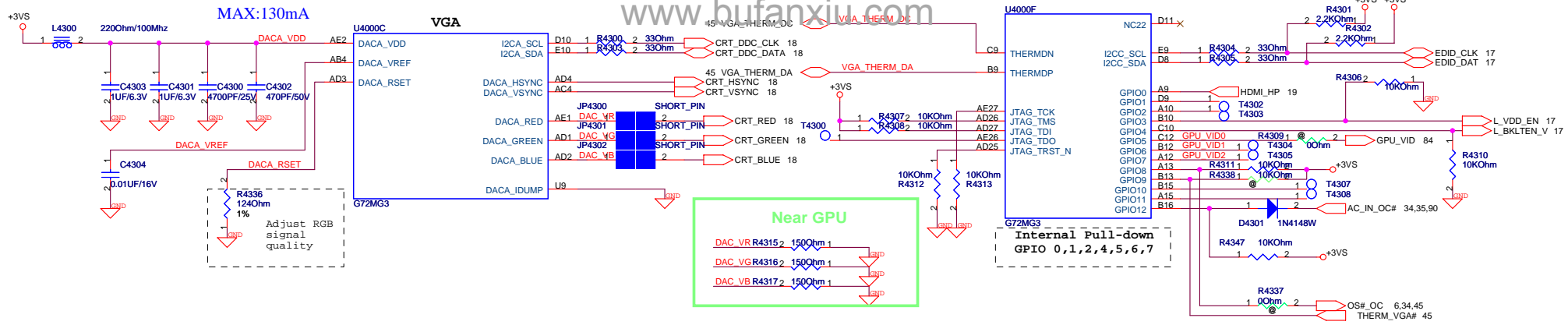


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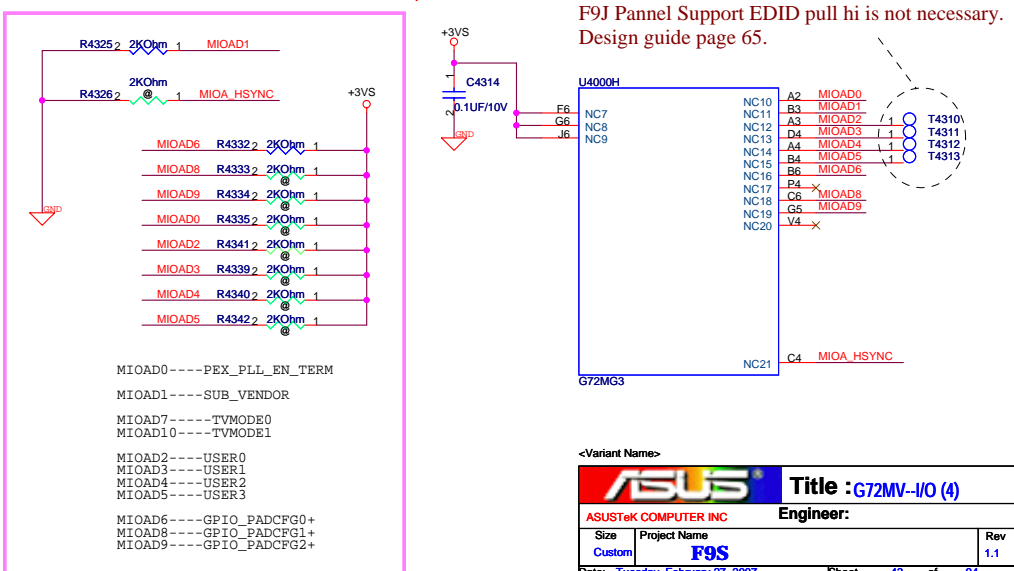
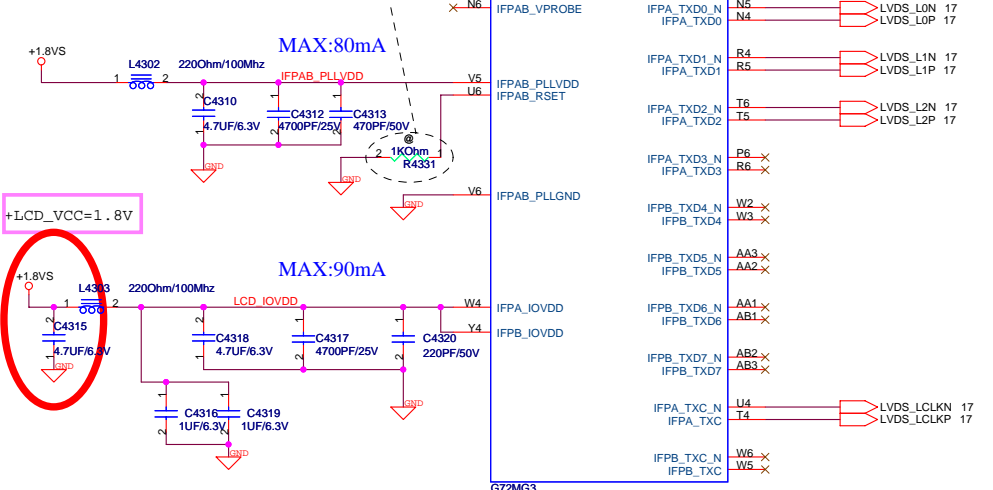
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ASUSTek COMPUTER INC		Engineer:	
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03G151236012

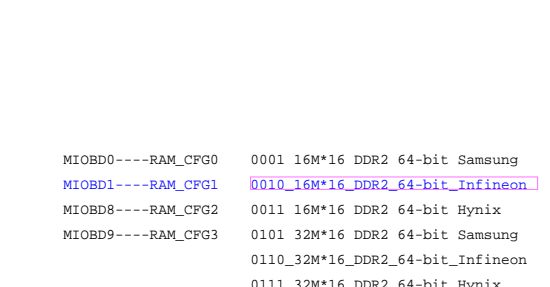
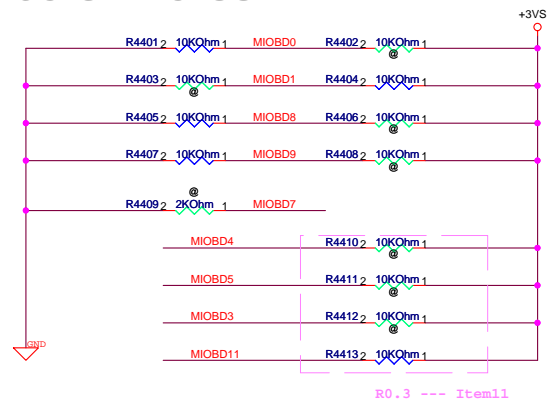
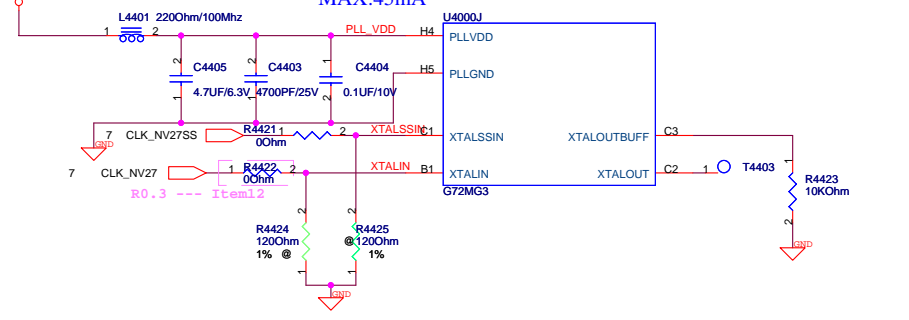
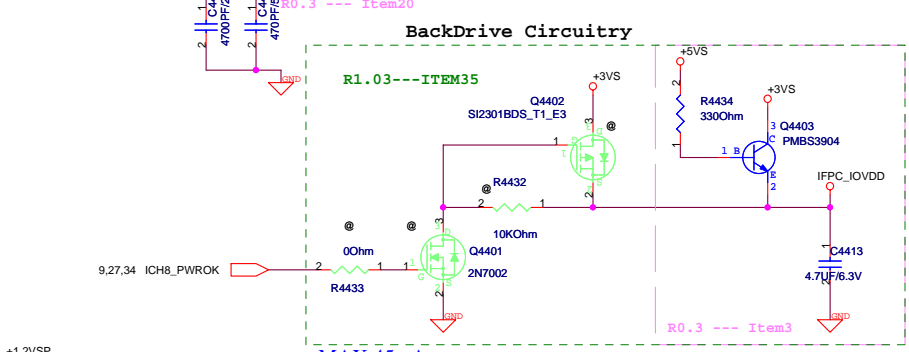
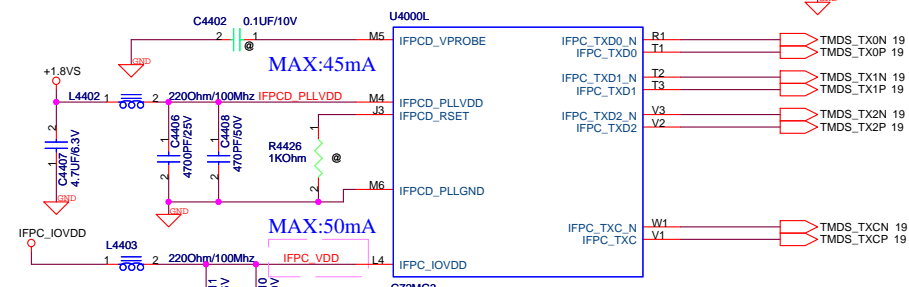
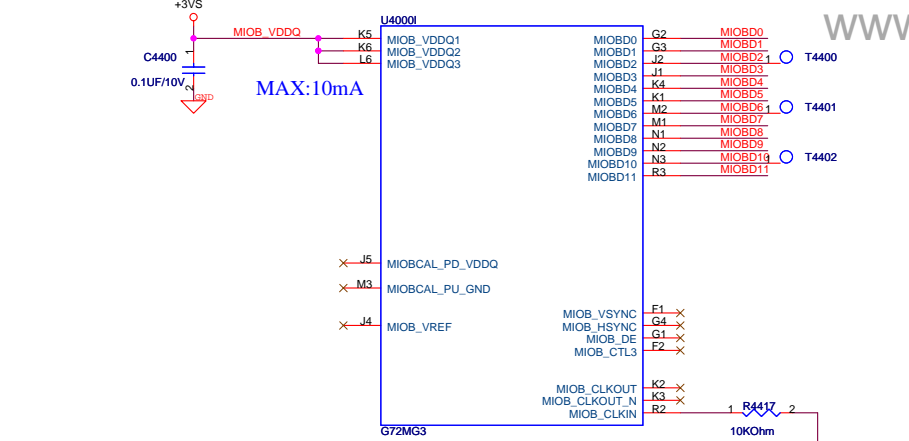


Design Guide Page80: IFPAB_RSET should be no stuff.

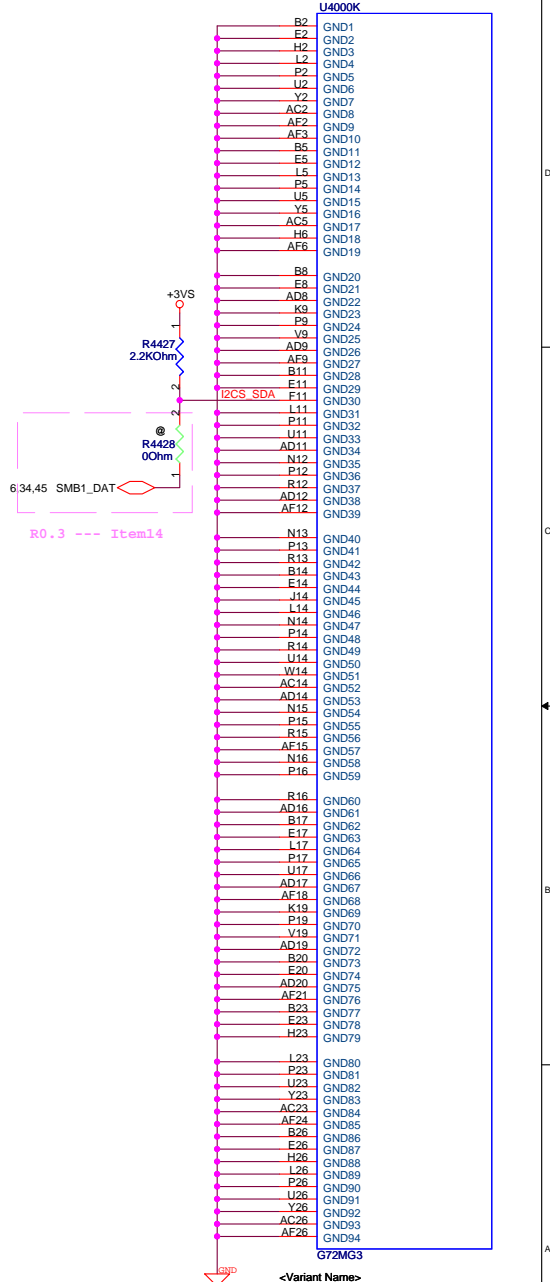


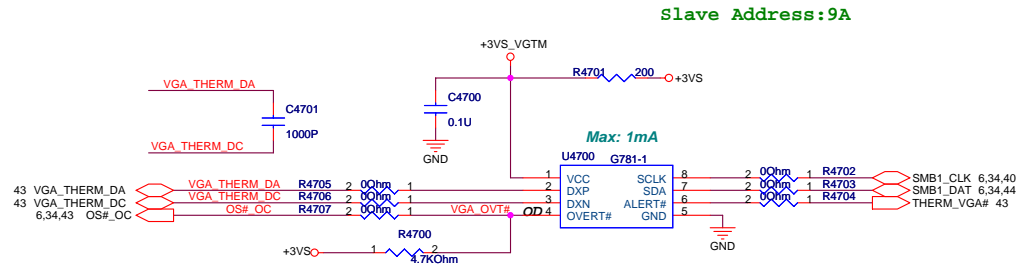
<Variant Name>

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ASUSTek COMPUTER INC		Engineer:	
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MIOBD0----	RAM_CFG0	0001	16M*16	DDR2	64-bit	Samsung
MIOBD1----	RAM_CFG1	0010	16M*16	DDR2	64-bit	Infineon
MIOBD8----	RAM_CFG2	0011	16M*16	DDR2	64-bit	Hynix
MIOBD9----	RAM_CFG3	0101	32M*16	DDR2	64-bit	Samsung
		0110	32M*16	DDR2	64-bit	Infineon
		0111	32M*16	DDR2	64-bit	Hynix
MIOBD9----	RAM_CFG3	0	Full width of the frame buffer			
		1	Half width of the frame buffer			
MIOBD2----	CRYSTAL0	00	13.5MHZ			
MIOBD6----	CRYSTAL1	01	14.318MHZ			
		10	27MHZ(Default)			
		11	RESERVED			
MIOBD4----	PCI_DEVID0	1000	NB8M-SE			
MIOBD5----	PCI_DEVID1					
MIOBD3----	PCI_DEVID2					
MIOBD11----	PCI_DEVID3					
MIOBD10----	ROMTYPE0	00	PARALLEL			
MIOB_VSYNC-	ROMTYPE1	01	SERIAL AT25F			
		10	RESERVED			
		11	LPC			
MIOBD7----	MOBILE_MODE					

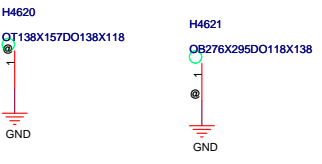
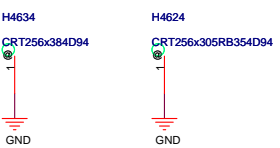
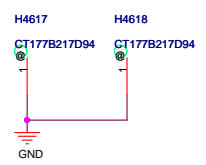
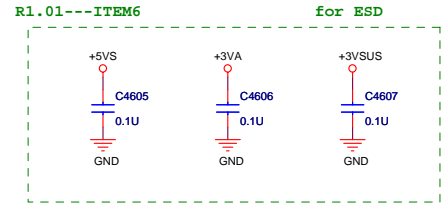
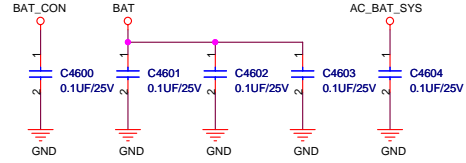
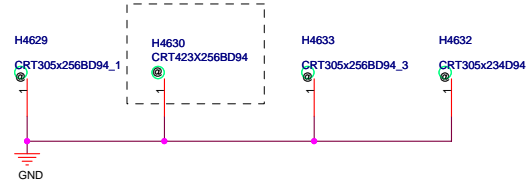
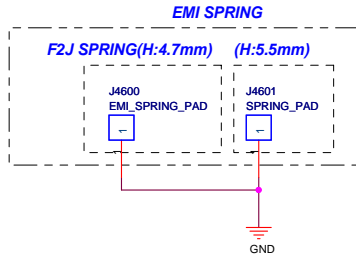
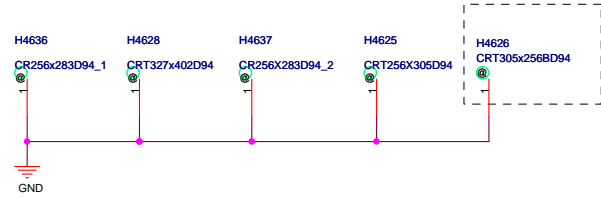


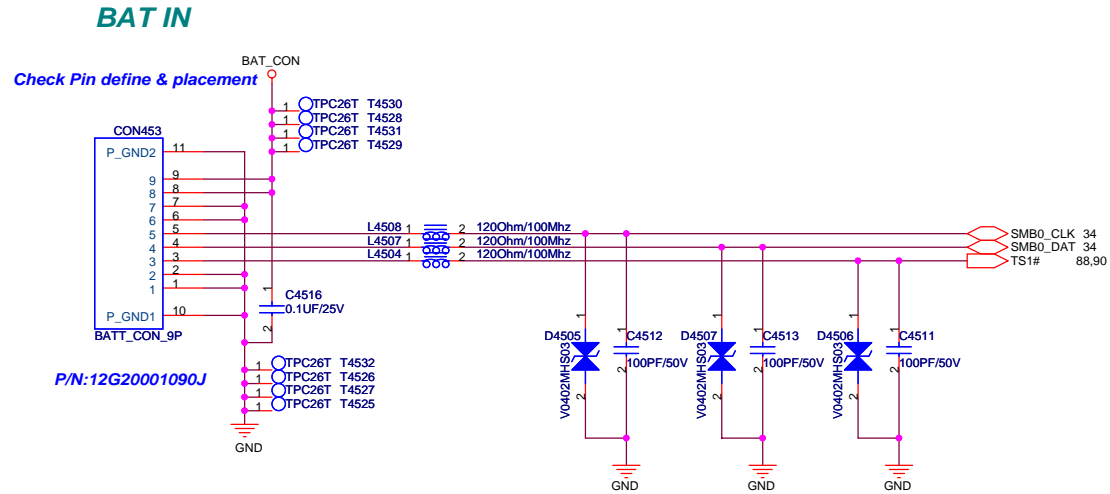
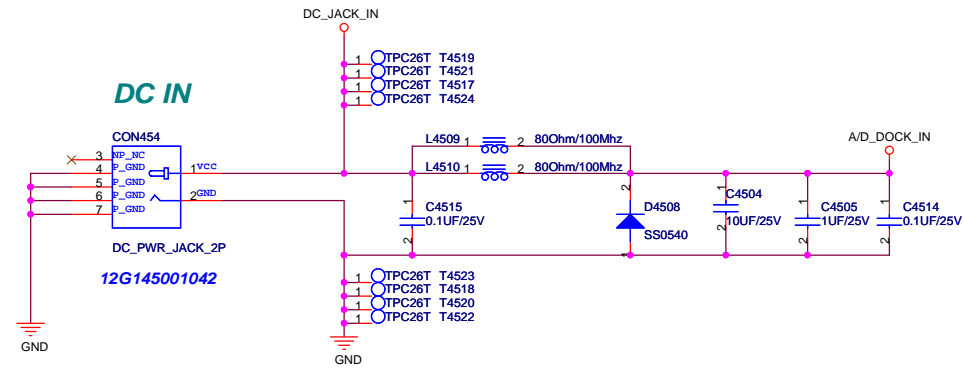


For frame buffer address/command lines those external pull up resistor can be removed for easy layout from Nvidia FAE

<Variant Name>

ASUS		Title G72MV-VRAM_TERM	
ASUSTeK COMPUTER INC		Engineer:	
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F9S SR_1128(R0.1---->R0.2)

- (1)Delete R0930,R0931 to follow Intel spec.---page9
- (2)Mount R1301 for DMI x2 ---page13
- (3)Modify netname USBP1 to USBP2 ---page17
- (4)Modify U1803,U1804 to N/A and R1817,R1818 connect to CRT_VSYNC,CRT_HSYNC ---page18
- (5)change TMDS pull high from +3VS to IFPC_IOVDD ---page19
- (6)Modify netname SUS_STAT# to PM_SUS_STAT# ---page21
- (7)Add signal for 1G LAN, ---page22
Delete R2201,R2202,Q2201,Q2202 and Modify netname ----- page22
- (8)Modify netname to IRQ14 ---page23
- (9)Delete E-SATA signal and add R2532,R2533 ---page25
- (10)Add test point T2717,T2719 ---page27
- (11)change 10/100 LAN to 10/100/1000 LAN(RTL811B) ---page29
- (12)Modify debug circuit ---page33
- (13)Modify single netname ---page34
- (14)Modify F3601 to 0.5A ---page36
- (15)Add C4066 ,D4001 for SPDIF_HDMI ---page40
- (16)Add R4434 to N/A ---page44
- (17)Add R0785,R0786,R0787 to follow Intel for CPU_BSEL ---page7
- (18)Add D3902,R3914,Q3906,R3912 for WLAN,WWAN LED(reserve) ---page39
- (19)Delete R0765,R0766,R0781,R0782,R0761,R0763 ---page7
- (20)Change CON2201 pin9 from +1.8V_LAN to GND---page22

F9S SR_1130(R0.2---->R0.3)

- (1)Delete CN1500 and add C1515~C1518---page15
- (2)DMI change to 2X---page9,26
- (3)Modify backdrive circuitry ---page44
- (4)Modify F1701 from 0.2A to 0.5A ---page17
- (5)Add R1702,C1714,Q1703 to reserve it for LCD power---page17
- (6)Delete R0719,R0721,R0723---page7
- (7)Modify L2902,L2903,L2904 size and add L2905,L2906 ---page29
- (8)R4105 change to 40ohm instead of 30ohm,and R4106 to N/A ---page41
- (9)Reserve FBA_CLKx clock terminator for NB8M-SE memory tuning---page42
- (10)Due to without TV function,C4309 and R4323 to N/A---page43
- (11)PCI_DEVICEID please set to "1000" for NB8M-SE---page44
- (12)For NB8M-SE ext. 27Mhz can connect directly without level shift,
R4422 use 0 ohm is ok---page44
- (13)For frame buffer address/command lines those external pull up resistor
can be removed for easy layout.---page45
- (14)I2CS_SCL and I2C_SDA to EC to access NB8M-SE internal thermal sensor---page40,44
- (15)Delete power limit circuit due to EC change to IT8511TE---page35
- (16)BT_DET# connect 3Vs to avoid the leakage-----Page27
- (17)Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request.
(Board lock hole:1.8mm; 3.0H)---Page23
- (18)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.--Page36
- (19)Add R1210,R1211 connect to GND for intel recommendation Rev1.5---page12
- (20)To modify duplicated netname from IFPC_IOVDD to IFPC_VDD ---page44
- (21)To modify duplicated netname of PCIE signal ---page29,33
- (22)Change RN2700 to 0402 size and no mount R2756 for Intel recommendation---page27
- (23)Change C2812,R2803 size from 0805 to 0603 for layout request.---page28
- (24)DDR SWAP for layout request---page14,15
- (25)Delete R3708,Q3710 due to +2.5VS power no use---page37
- (26)Add Q1802 to avoid current leakage from CRT device---page18

F9S SR_1130(R0.3---->R0.4 same as R1.0)

- (1)Change Newcard header H=3.2 and card ejector for F9S/E---page33
- (2)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.---page36
- (3)No Mount R3806,to avoid +3VA_EC leakage to +3Vs---page38
- (4)Add C2843,C2844 connect to GND for intel recommendation---page28
- (5)Change C06XX from 10U to 22U for intel recommendation---page06
- (6)Change C3412 from 1U to 2.2U and delay EC_RST#---page34

- (7)R2208 reserve high change to pull low for intel recommendation. ---page23
- (8)Add R2106 33ohm for checklist ---page24
- (9)Add Q1901,R1928,R1929 to avoid leakage for HDMI DDC clk, and Data---page19
- (10)Add R3660,R3661,C3667,C3668(SD and MS CLK) for EMI request ---page36

F9S ER_0122(R1.0---->R1.01)

- (1)Add C2201 ~ C2208 for EMI request ---page22
- (2)Change +VCCP discharge by SUSB_ON for the correspondence with
power enable ----page37
- (3)Change RES. 4R8P RN3403 to single RES R3429, R3434 for uncertain
PMTHERM# leakag ---page34
- (4)Delete D1901 and add Q1902 and R1926,R1927 change to 1.8K ohm for HDMI
spec. ---page19
- (5)+5VS_CRT change to +5VS_HDMI_CRT and D1806 to DNI ---page18
- (6)Add C4605,C4606,C4607 0.1uf cap. for ESD ---page46
- (7)R3660,R3661 mount 33 Ohm and C3667,C3668 mount 10p for EMI issue---page36
- (8)Power change to AC_BAT_SYS_INV for layout improve---page17
- (9)Change D2401 ,D2400 part from RSB6.8S to EGA10603V05A1---page24

F9S ER_0125(R1.01---->R1.02)

- (10)Add C2108 0.1uf cap. for ESD---page21
- (11)Add USB Port Charging Function on S4/ S5---page24
- (12)Add OS#_OC to FAN---page6
- (13)Change R0402 from 68 ohm to 1k ohm 1% because it can fixes the PROCHOT#
failure when driven by thermal sensor on the CRB.----page4
- (14)Delete C0401 for intel recommend.---page4
- (15)Change WLAN SW pull up to +3VA_EC for leakage prevention.---page38
- (16)Del D0701,D0702 and add R785,R786 because there is no leakage at S3/S4 or
card insertion.---page7
- (17)Power add BATSEL_3S# connect to EC.---page34
- (18)DNI useless U2603 and C2606.---page26
- (19)Reserve a RES R2754 to pull up PM_RSMRST# to +3VSUS.---page27
- (20)Change net name PM_RSMRST# to PM_RSMRST#_SB to pull up +3VSUS & add
D2701 for leakage prevention.---page27

F9S ER_0126(R1.02---->R1.03 same as R1.1)

- (21)Add PLT_RST#_BUF for Sierra card modern reset signal MDL_RESET#.---page22
- (22)Change C2500,C2502 from 22pF to 15pF to meet XTAL requirement---page25
- (23)C3656/C3655 change from 18pF to 27pF to meet XTAL requirement---page36
- (24)Change R0712 from 220 ohm to 270 ohm for clock signal quality
improvement.--page07
- (25)Change L1811,L1812,L1813 from BEAD 120ohm to 82nH and C1832,C1834,C1836
from 22p to 10p for CRT signal quality---page18
- (26)Change Q2405,Q2407 2N7002 to UM6K1N ---page24
- (27)Add R2409,R2410 to reserve +5VSUS for SN74CBTD3306 5V power. ---page24
- (28)PWRLMT Circuit: For Battery 1P ---page35
- (29)SWAP +3V and +3VS power for 3G requirement ---page22
- (30)Add C0719,C0721 for 3G requirement ---page07
- (31)Mount L1709 common mode choke for 3G requirement---page17
- (32)Add C1715,C1716 for 3G requirement---page17
- (33)To combine UM6K1N for cost down :delete Q3706,Q9202,Q9203---page37
- (34)R1705 from 100 ohm change to 390 ohm for LCD power off sequence---page17
- (35)Mount Q4403 and remove Q4402,Q4401,R4432,R4433 for cost down---page44

F9S ER_0207(R1.1---->R1.2)

- (36)LVDS conn. pin modification for LVDS coaxial cable---page17

F9S ER_0215(R1.2---->R1.3)

- (37)Power Team modify +1.5VS power rating to 3.5A ---page82
- (38)Add CN3501~CN3506 for 3G
requirement---page35
- (39)Change CLK_TPMPICI R0707 from 33 ohm
to 27 ohm and mount C0725(10p) to meet
edge rate spec---page36

		Title : History(1)	
ASUSTeK COMPUTER INC		Engineer:	
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change list:

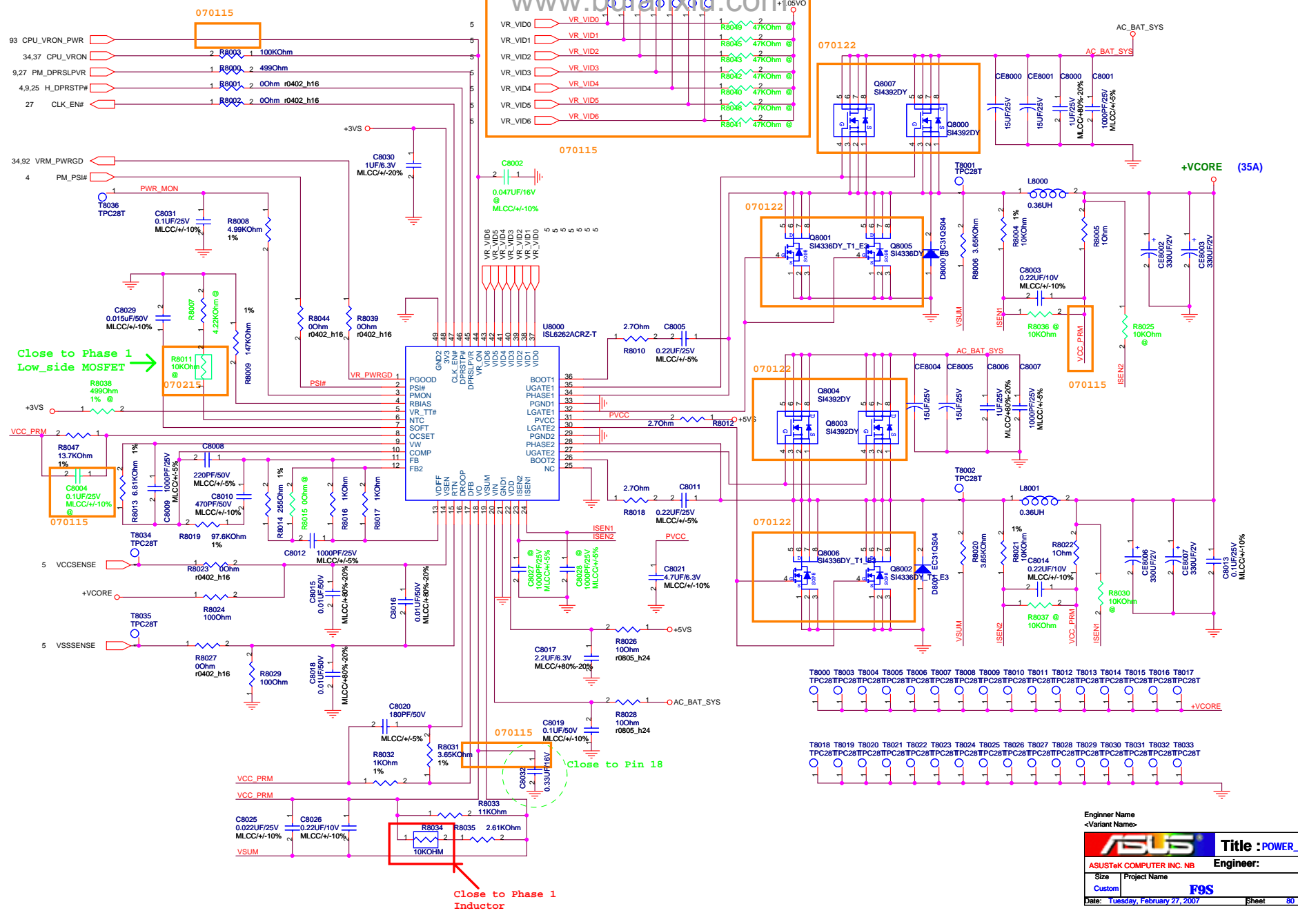
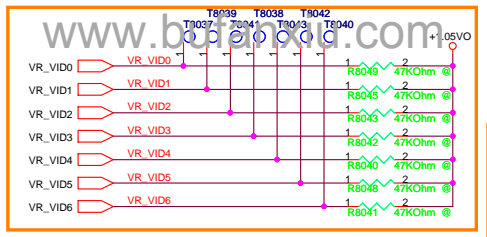
1. Delete R8046.
2. Change C8004(DNI) to U8000 pin8.
3. Change C8032 to U8000 pin18.
4. Add test point T8037~T8042.
5. For power sequency, change R8400 from 0 to 20K ohm.
6. For OCP adjust, change R8407 from 200K to 30K ohm.
7. For output voltage adjust, change R8406 from 20K to 4.22K, change R8409 from 100K to 20K ohm.
8. To Increase the saturation crrent of L8400, change L8400 from 09G02X103022 to 09G02X103U00.
9. DNI Q8404 and R8408.
10. Delete Q8505 and Q8501.
11. Change L8500 from 0.56uH to 1uH.
12. For OCP adjust, change R8508 from 100K to 51K.
13. For PWM oscillation issue, change output capacitor to 150uF/2V(ESR=18m ohm) *2.
14. For power sequency, change R8504 from 0 to 120K, change C8504 from DNI to 0.1uF, change C8515 from 0.033uF to 0.1uF.
15. Add JP8805 for layout improve.
16. Add 3S/4S selector circuit(DNI).
17. Add U9001 colay to U9000.
18. For power sequency, change R9108 and R9107 to 47K, change R9109 and R9110 to 22K, Delete R9106 and R9112.
19. Change Schematic_Part at Q8000,Q8001,Q8002,Q8003,Q8004 Q8005,Q8006,Q8007,Q8300,Q8301,Q8401,Q8403.
20. Change L8101 from 3.3uH/CYNTEC to 3.8uH/SUMIDA.
21. Change R8120 from 21K to 20K for OCP adjust.
22. For spec. change.Chagne Q8004 from SI4392 to SI4800, Change Q8006 from SI4336to SI4800, Change R8524 from 30K to 174K, Change L8500 from 1uH/18A to 1.8uH/9A. DNI CE8506, CE8504.

F9S ER_0215(R1.1 --> R1.3)-----POWER

23. Power team modify +1.5VS power rating to 3.5A ---page82

<Variant Name>

		Title : History(2)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F9S		1.1
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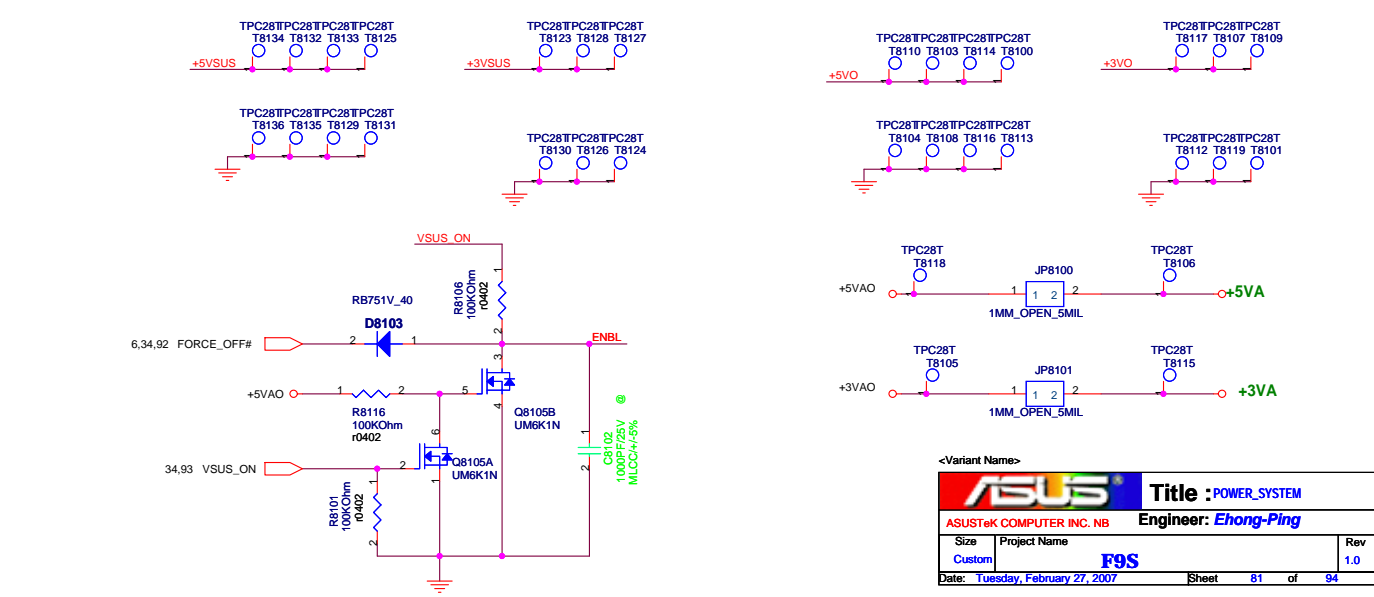
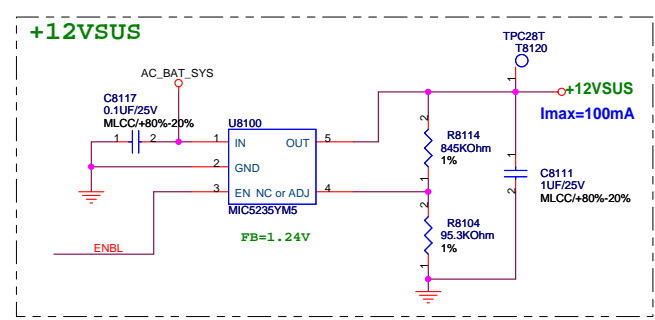
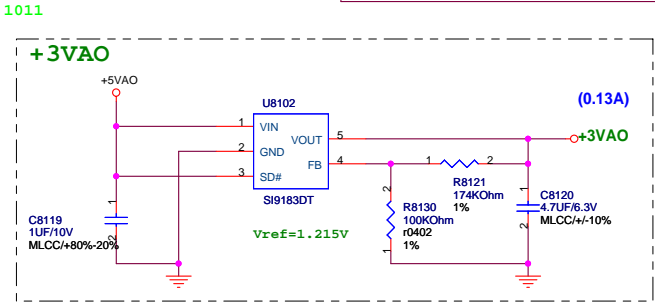
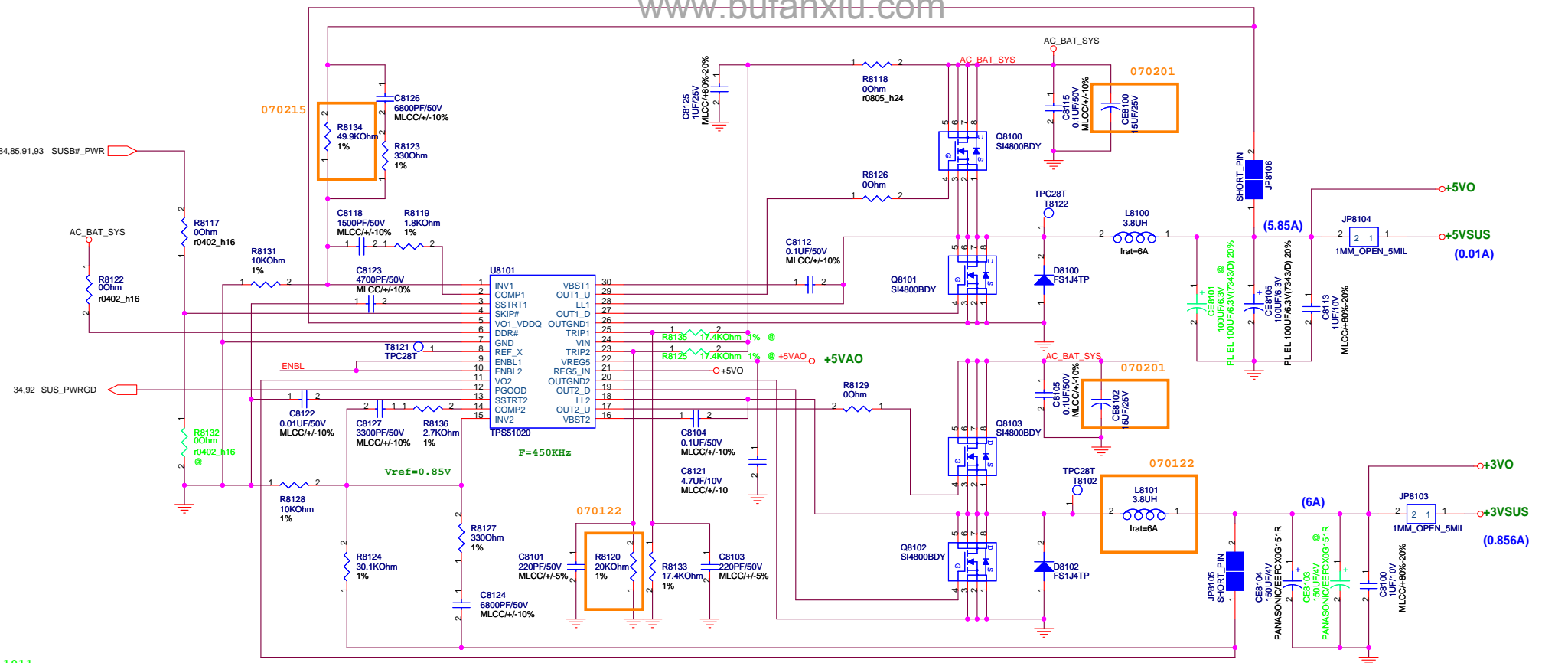
Close to Phase 1 Low_side MOSFET

Close to Pin 18

Close to Phase 1 Inductor

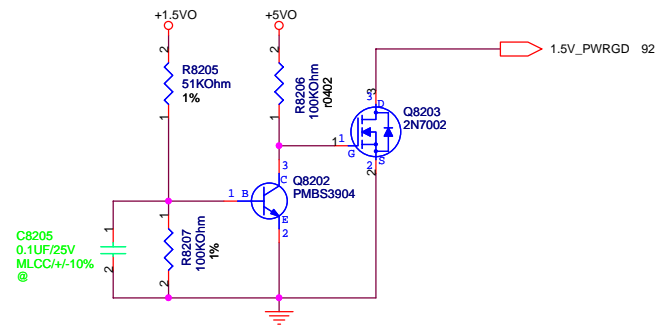
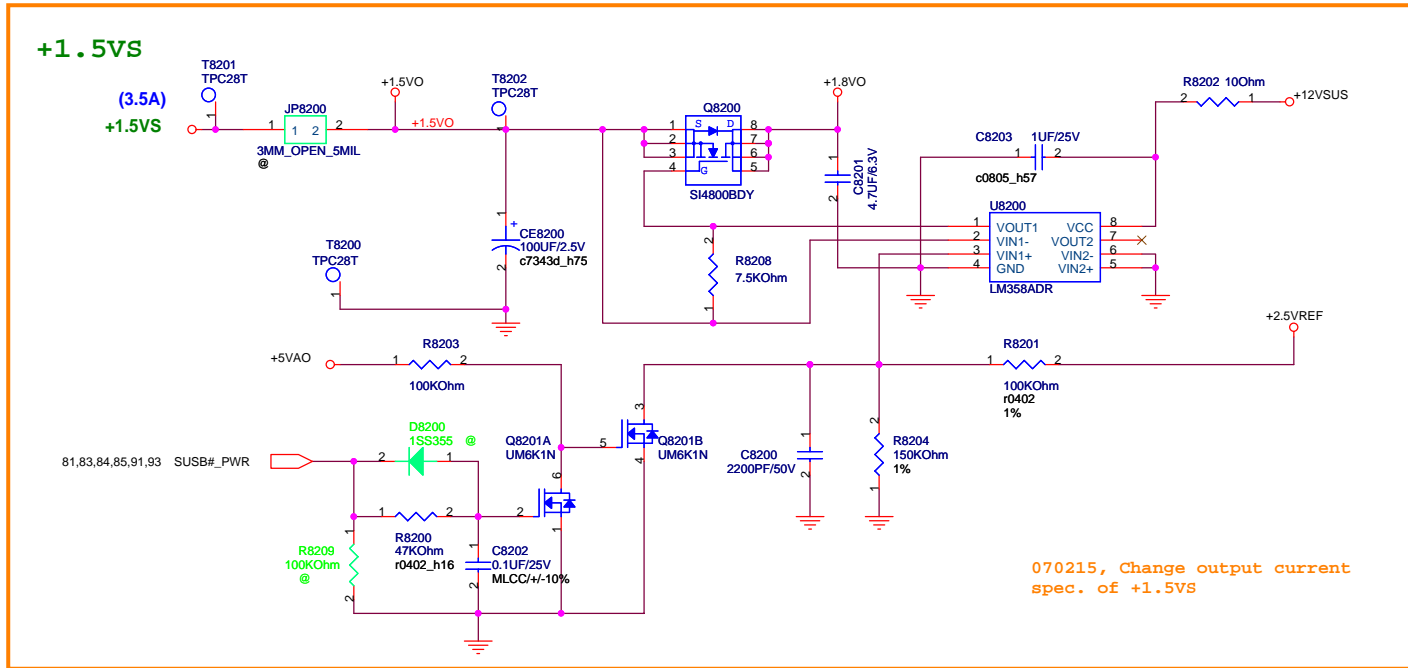
Engineer Name
-Variant Name-

		Title : POWER_VCORE	
		ASUSTek COMPUTER INC. NB	Engineer:
Size	Project Name	F9S	Rev
Custom			1.0
Date: Tuesday, February 27, 2007		Sheet	80 of 94



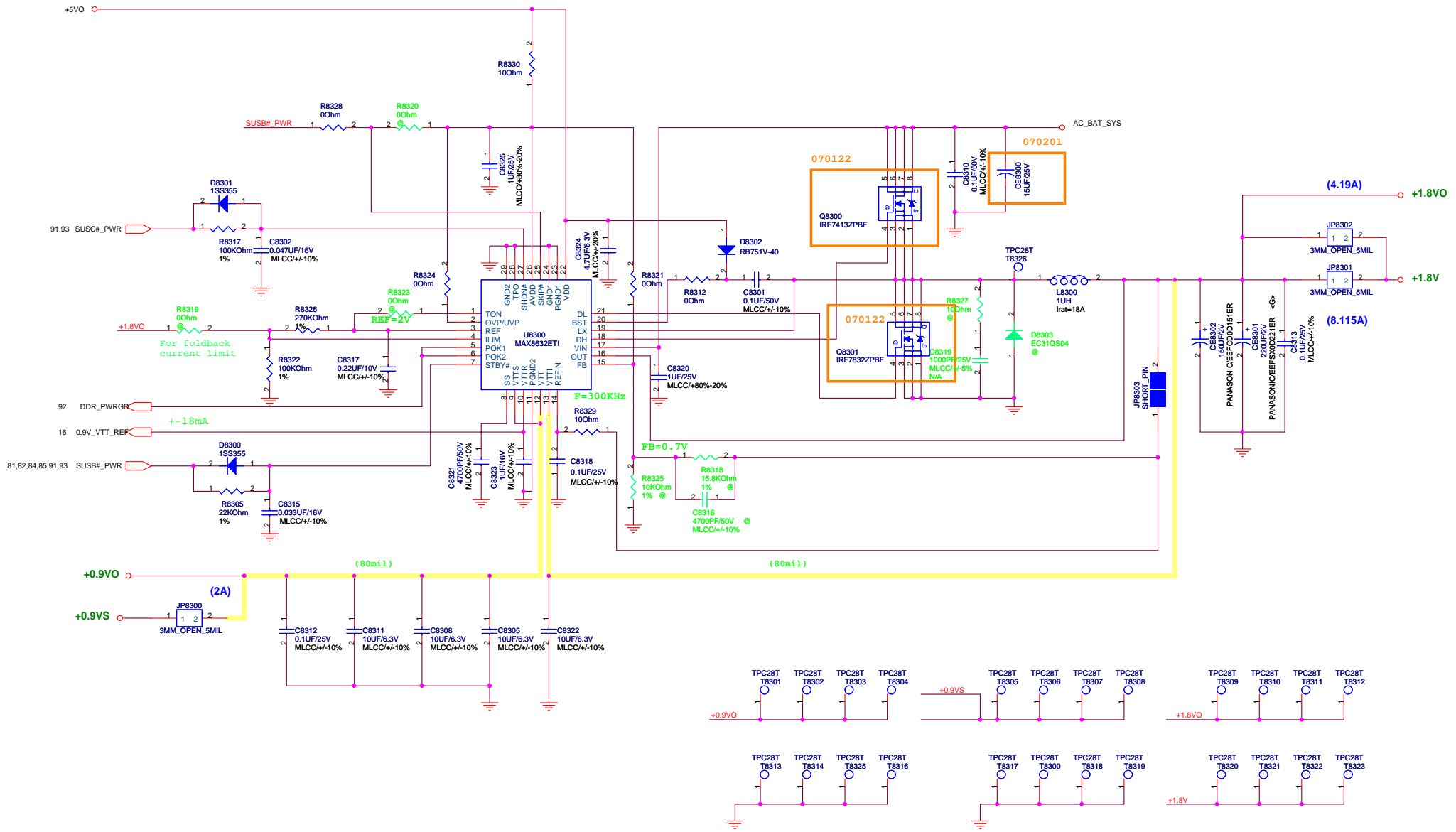
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		Title : POWER_SYSTEM	
ASUSTek COMPUTER INC. NB		Engineer: Hong-Ping	
Size	Project Name		Rev
Custom	F9S		1.0
Date: Tuesday, February 27, 2007	Sheet	81	of 94



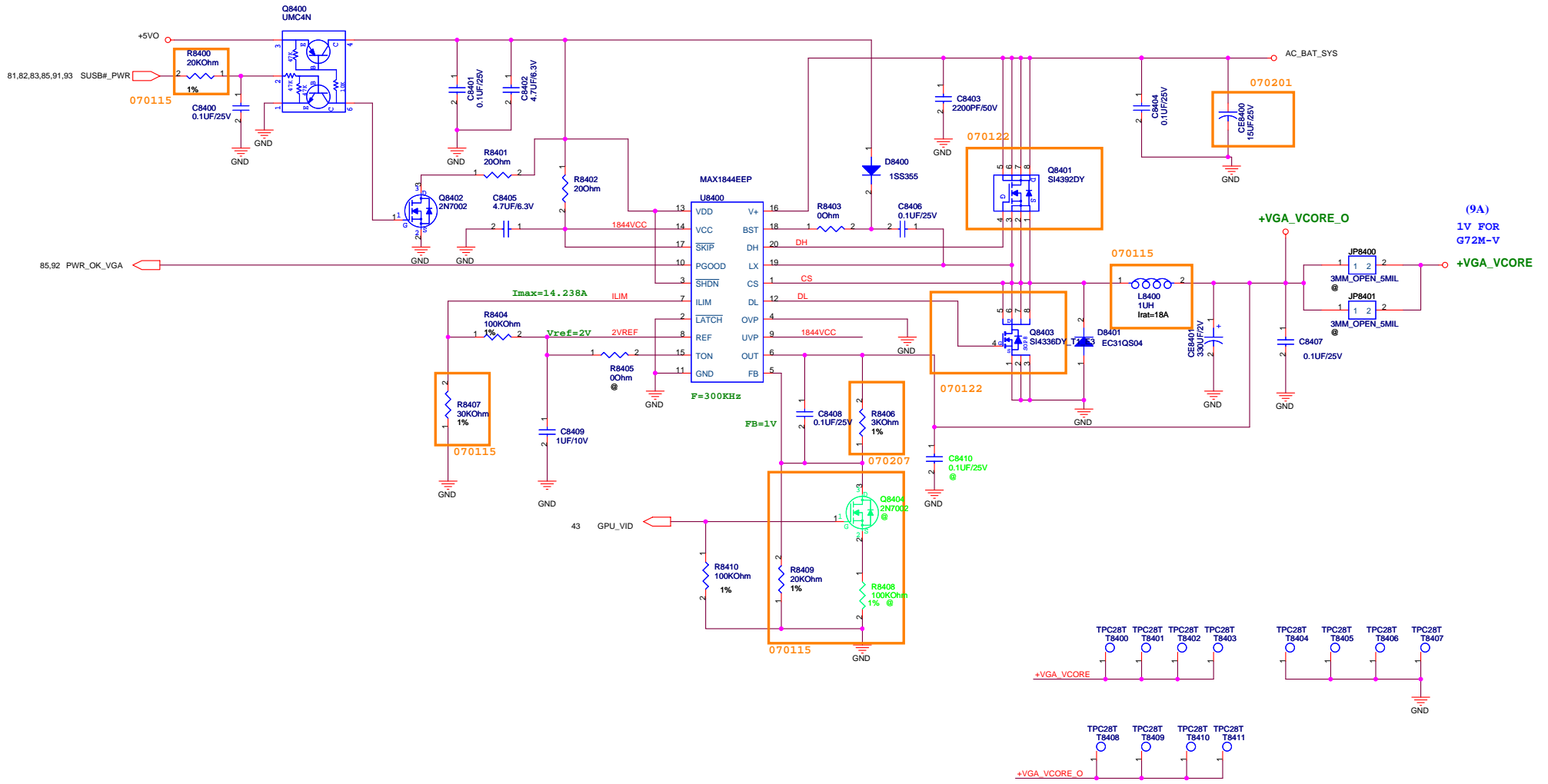
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ASUS		Title : POWER_I/O_1.5VS & 1.05VS	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ehong-Ping</i>	
Size B	Project Name F9S		Rev 1.0
Date: Tuesday, February 27, 2007		Sheet	82 of 94



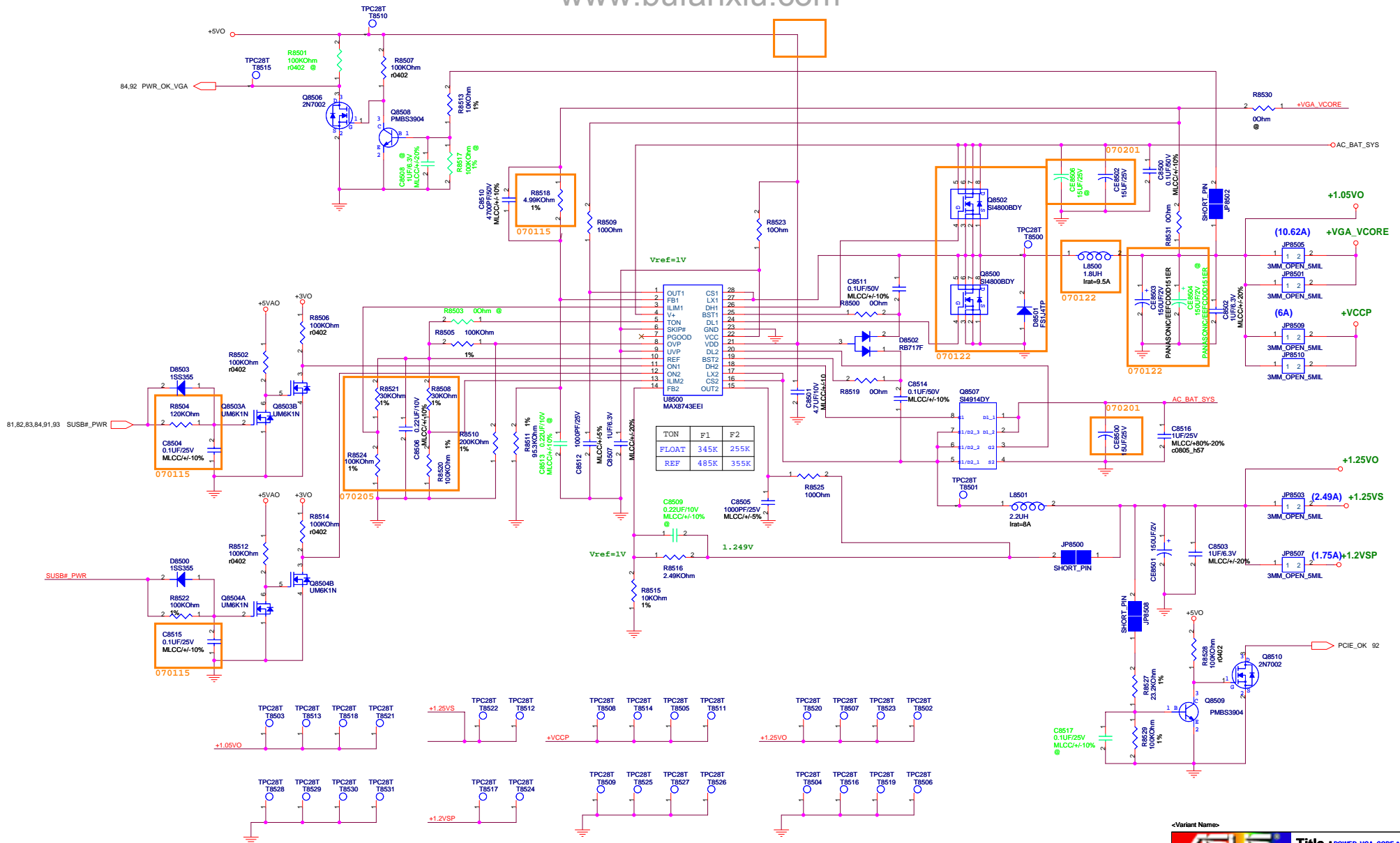
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		Title : POWER_I/O_DDR & VTT	
ASUSTeK COMPUTER INC. NB		Engineer: Hong-Ping	
Size	Project Name	Rev	
Custom	F9S	1.0	
Date: Tuesday, February 27, 2007		Sheet	83 of 94



<Variant Name>


ASUS		Title : POWER_IO_+2.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name		Rev
Custom	F9S		1.0
Date: Tuesday, February 27, 2007	Sheet	84	of 94

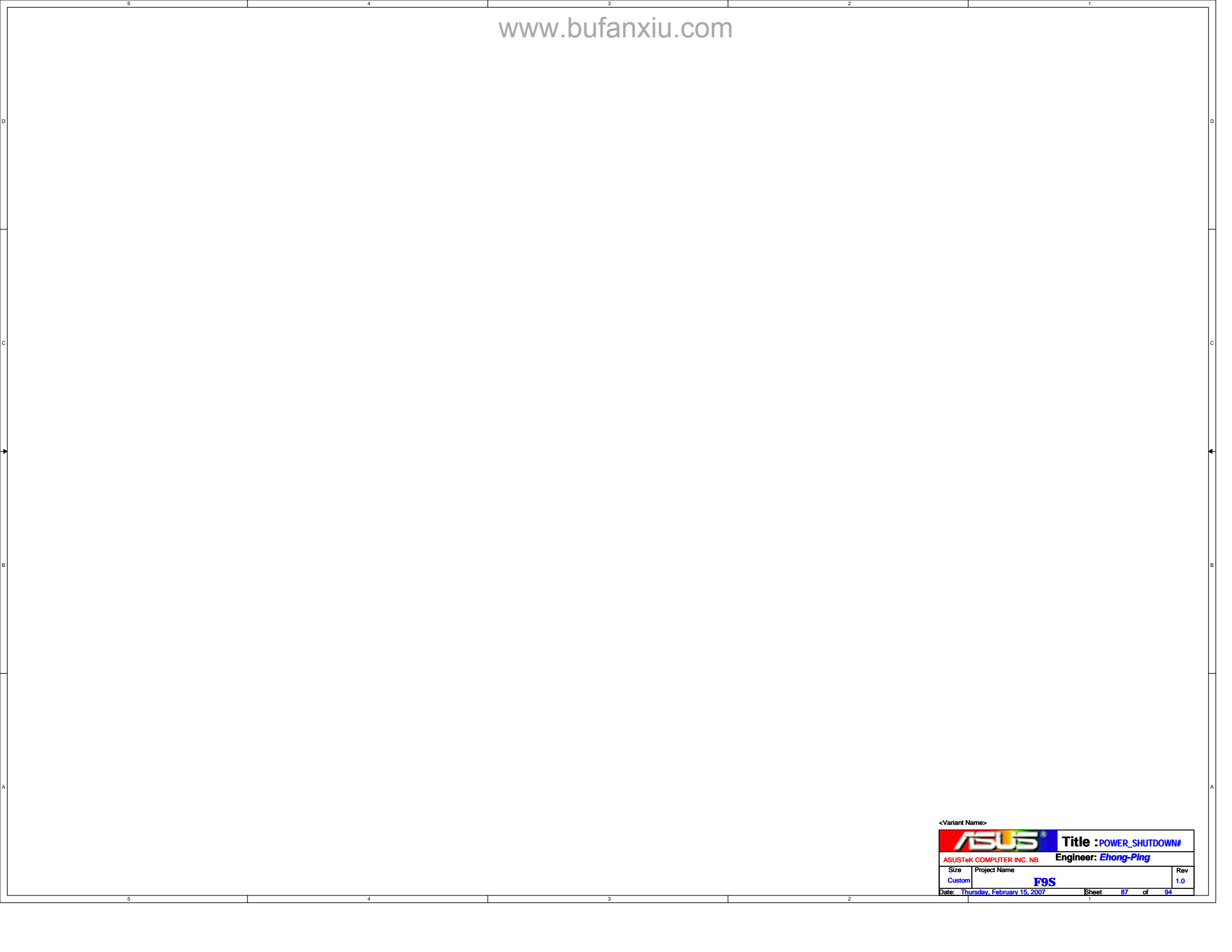


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ASUS		Title : POWER_VGA_CORE & RAM	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name	Rev	1.0
Custom	F9S	Sheet	65 of 94
Date:	Tuesday, February 27, 2007	Sheet	65 of 94

<Variant Name>

		Title : <i>N/A</i>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ehong-Ping</i>	
Size	Project Name		Rev
B	F9S		1.0
Date: <i>Thursday, February 15, 2007</i>		Sheet	86 of 94



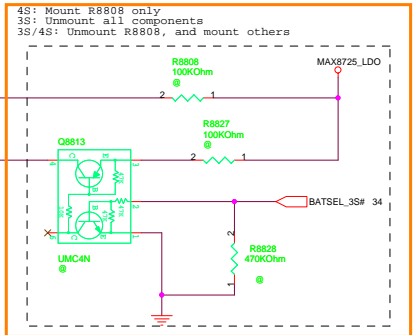
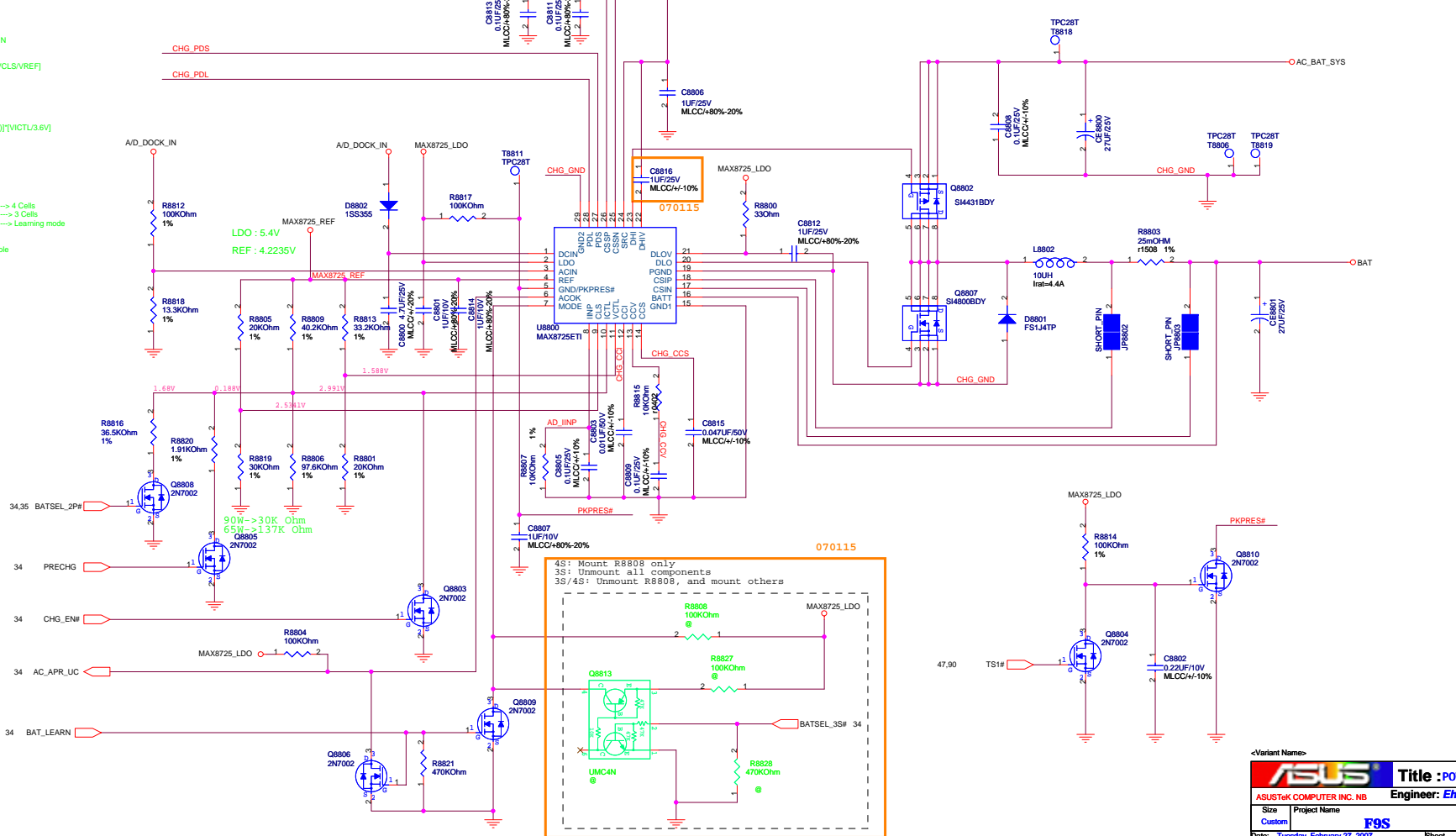
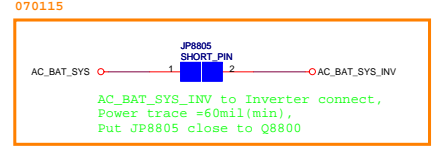
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		Title :POWER_SHUTDOWN#
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping
Size	Project Name	Rev
Custom	F9S	1.0
Date: Thursday, February 15, 2007		Sheet 87 of 94

POWER PATH & BAT_LEARN

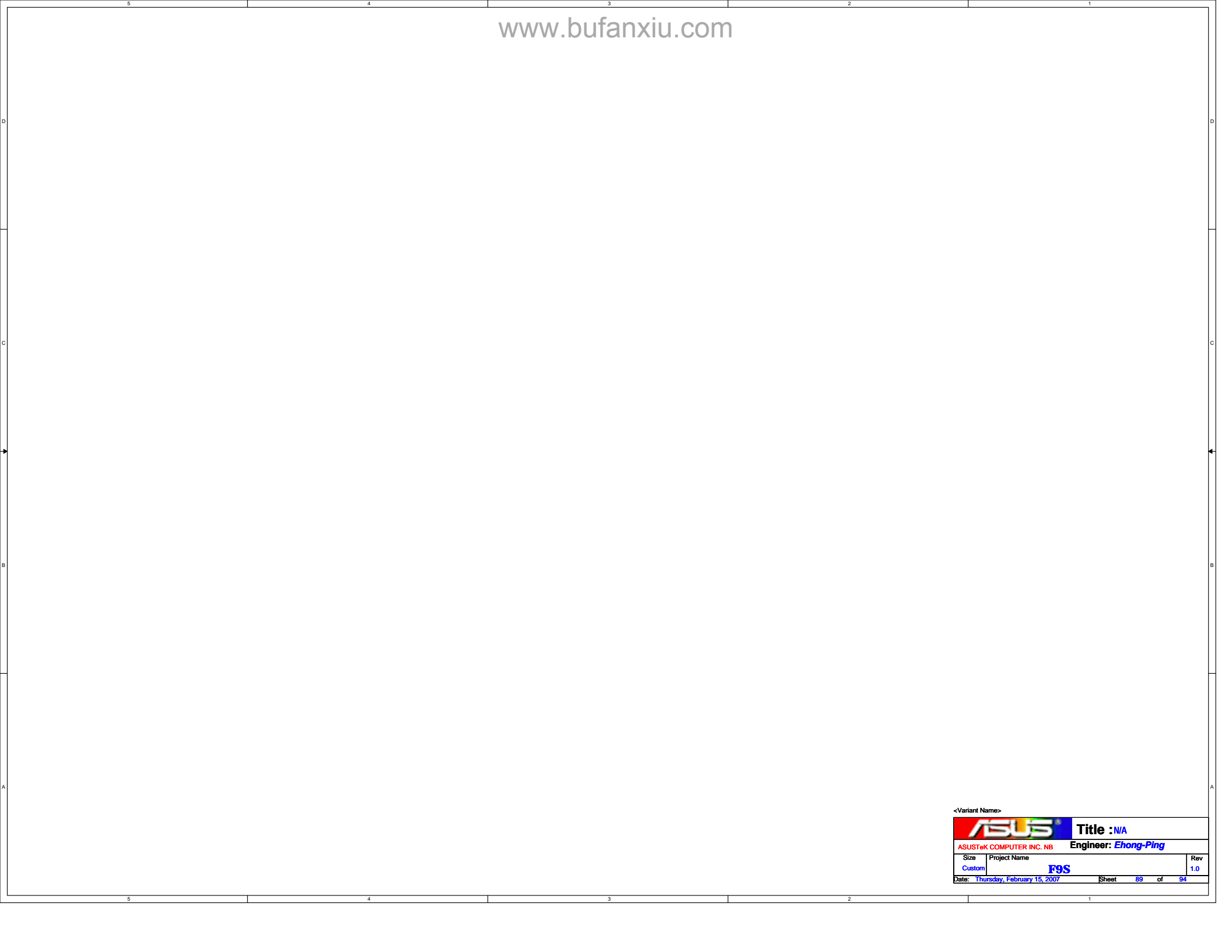
90 WATT

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Rsense(ADIN)=0.010ohm
 VCLS=2.5341V
 => Iin(max)=4.5A
 => Constant Power = 19 * 4.5 = 85.5W
 => R5710=20K, R5715=30K
 Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
 Rsense(CHG)=0.025 ohm
 VICTL= 3V => Ichg = 2.5A
 VICTL= 1.68V => Ichg = 1.4A
 Vbatt = Cell * (Vref + (VCTL - 1.8V) / 9.52)
 VCTL = 1.588V
 => Vbatt = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
 2.0 > Vmode > 1.6V (floating) -> 3 Cells
 0.8 > Vmode (tie to GND) -> Learning mode
 VICTL < 0.8V or DCIN < 7V -> Charger Disable
 Precharge current=150mA




<Variant Name>

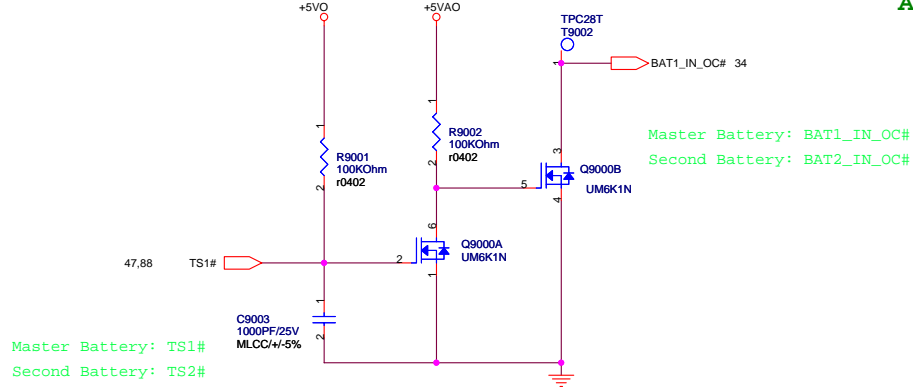
ASUS		Title : POWER_CHARGER	
ASUSTek COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name	Rev	
Custom	F9S	1.0	
Date: Tuesday, February 27, 2007	Sheet	68	of 94



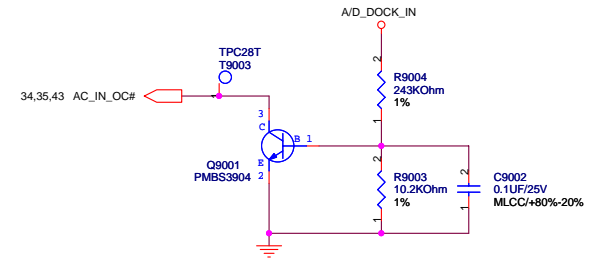
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		Title : <i>N/A</i>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Ehong-Ping</i>	
Size	Project Name		Rev
Custom	F9S		1.0
Date: <i>Thursday, February 15, 2007</i>		Sheet	89 of 94

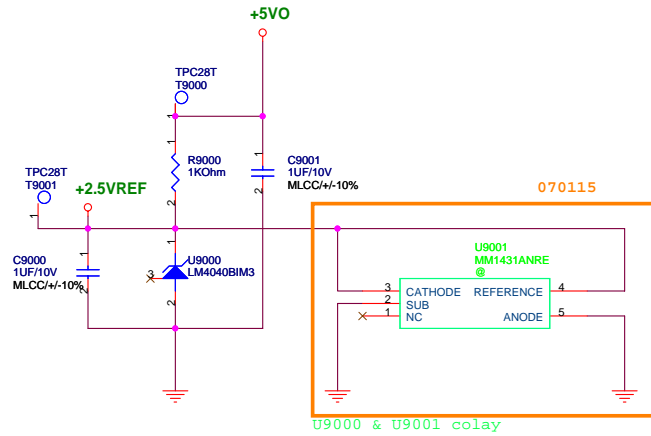
BATTERY IN DETECT



ADAPTER IN DETECT

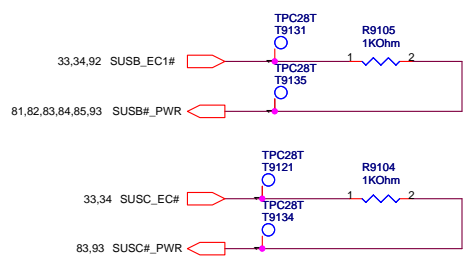
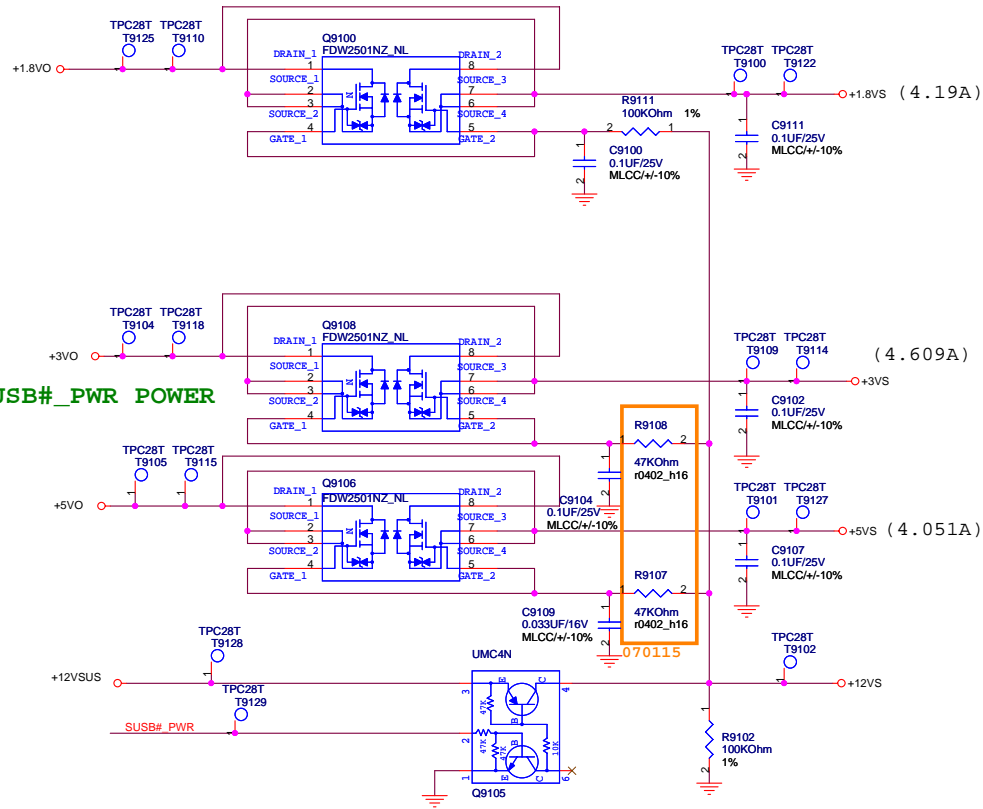
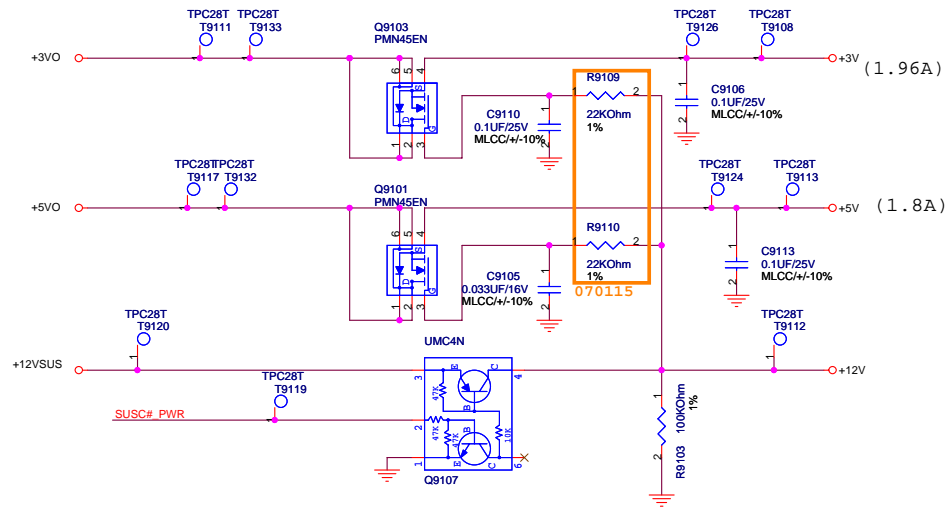


+2.5VREF

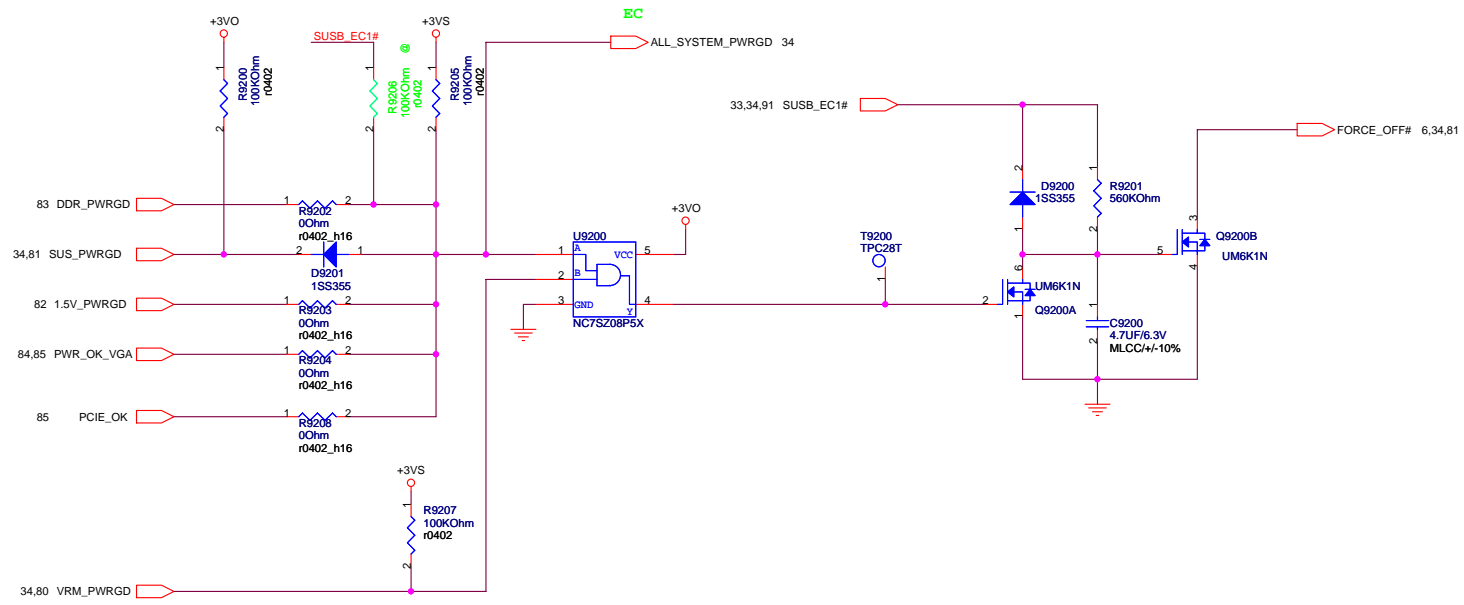


<Variant Name>

ASUS		Title :POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Ehong-Ping	
Size	Project Name		Rev
Custom	F9S		1.0
Date: Tuesday, February 27, 2007		Sheet	90 of 94

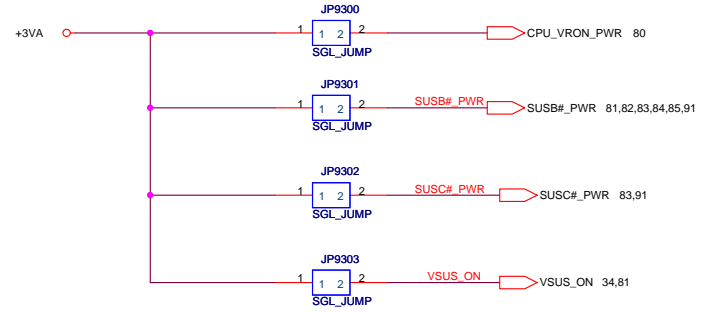


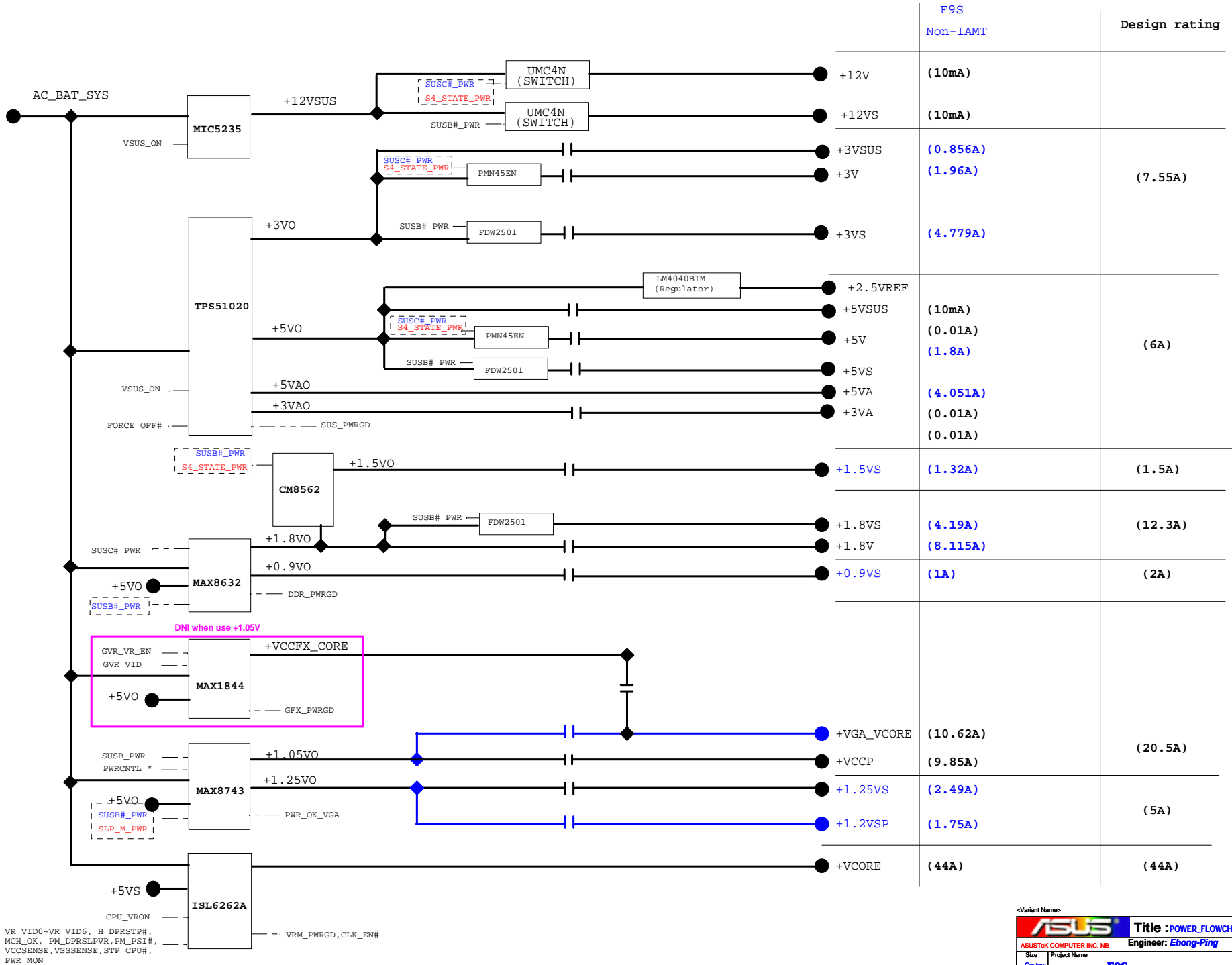
POWER GOOD DETECTER





FOR POWER TEST





VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON