SYSTEM PAGE REF.

K42Jr SCHEMATIC Revision 2.0

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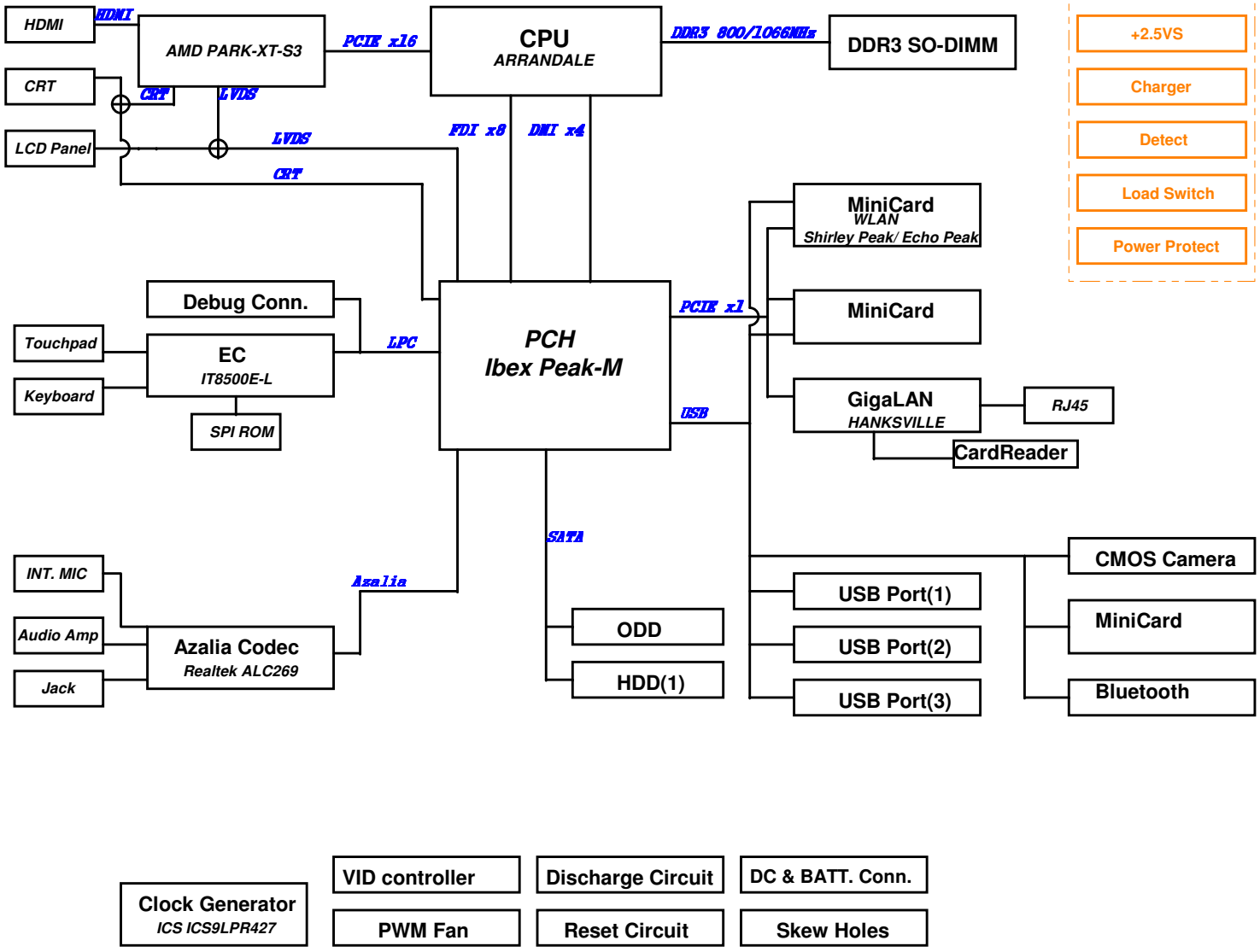
BLOCK DIAGRAM



ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: Nic

Size	Project Name	Rev
C	K42Jr	1.1

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PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	–	–	+3VS
GPIO 01	GPO	–	INT TBD	+3VS
GPIO [2:5]	Native	–	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	–	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAYPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	–	–	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	–	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	–	–	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	–	–	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	–	–	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	–	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	–	–	+3VS
GPIO 34	Native	STP_PCI#	–	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	–	–	+3VS
GPIO 49	GPO	GPU_RST#	–	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	–	–	+5VS
GPIO 53	GPO	–	INT PU	+3VS
GPIO 54	GPO	–	–	+5VS
GPIO 55	GPO	–	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	–	–	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	–	+3VSUS
GPIO 62	Native	SUS_CLK	–	+3VSUS
GPIO 63	Native	PM_SLP_S5#	–	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	–	–	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	–	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC IT8512

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		–
GPA3		–
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		–
GPA7		–
GPB0	O	SUSC_EC#
GPB1	O	SUSB_EC#
GPB2		–
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RC_IN#
GPB7	O	PM_RSMRST#
GPC0		–
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5		OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0		–
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		–
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		–
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPF0		–
GPF1		–
GPF2	I	EXP_GATE#
GPF3		–
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7		–
GPG0		–
GPG1	I	PM_SUSB#
GPG2		–
GPG6		–
GPH0	IO	PM_CLKRUN#
GPH1		–
GPH2	O	GFX_VR_ON
GPH3	O	BAT_LEARN
GPH4		–
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		–
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6		–
GPI7		–
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	TP_LED
GPJ5		–

EC IT8301

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2		–
GPIO3		–
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		–
GPIO8		–
GPIO9		–
GPIO10		–
GPIO11		–
GPIO12	O	ME_PWROK
GPIO13		–
GPIO14	O	ME_SLP_M_EC#
GPIO15		–
GPIO16		–
GPIO17		–
GPIO18		–
GPIO19		–
GPIO20		–
GPIO21		–
GPIO22		–
GPIO23		–
GPIO24		–
GPIO25		–
GPIO26		–
GPIO27		–
GPIO28		–
GPIO29		–
GPIO30		–
GPIO31		–
GPIO32		–
GPIO33		–
GPIO34		–
GPIO35		–
GPIO36		–
GPIO37		–

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LPR362)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
VID Controller(ASM8272)	0011011x (36)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
CPU Thermal Sensor(G780)	1001100x (98)	
VGA Thermal IC(G781-1)	1001101x (9A)	

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	ESATA (for pre-ES1)
PCIE 6	GLAN
PCIE 7	
PCIE 8	

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	NewCard
USB 6	Minicard TV Tuner
USB 7	
USB 8	
USB 9	WLAN
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

ASUSTeK COMPUTER INC. NB4

Title : System Setting

Engineer: CH_Lin

Size	Project Name	Rev
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U0301A

DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3

FDI_TXN[7:0]
FDI_TXP[7:0]
FDI_FSYNC0 FDI_FSYNC1
FDI_INT
FDI_LSYNC0 FDI_LSYNC1

For Intel GFX display

PEG_ICOMPI PEG_ICOMPO PEG_RCOMPO PEG_RBIAS
R0301 49.9Ohm 1%
R0302 750Ohm 1%

PEG_RX[0:15] PCIENB_RXN[15:0] (75)
PEG_TX[0:15] PCIENB_TXN[15:0] CX0316–CX0301 0.1UF/16V PCIEG_RXN[15:0] (75)
PCIENB_TXP[15:0] CX0332–CX0317 0.1UF/16V PCIEG_RXP[15:0] (75)

R0370,R0371,R0372 near U0301

For EC request, to read PECI via EC.
Connection: R0317.2-->Q0301.1-->U3001.118

SOCKET989

U0301B

R0303 R0304 20Ohm H_COMP3 AT23 / H_COMP2 AT24
R0305 49.9Ohm H_COMP1 G16
R0306 49.9Ohm H_COMP0 AT26
+VTT_CPU R0307 49.9Ohm H_CATERR# AK14
(25) H_PECI AT15
H_PROCHOT_S# AN26
(32) H_THRMTRIP# AK15
(7) H_XDPRST# AP26
(22) PM_SYNC# AL15
(7,25) H_CPUPWRGD AN14 / AN27
(22) H_DRAM_PWRGD AK13
(32) H_VTTPWRGD AM15
(7) H_PWRGD_XDP AM26
(24,30,32,41,53,75) BUF_PLT_RST# R0318 1.5KOhm 1% PLT_RST#_R AL14
R0319 750Ohm 1% C0304 0.1UF/10V

COMP3 COMP2 COMP1 COMP0 SKTOCC# CATERR# PECI PROCHOT# THERMTRIP# RESET_OBS# PM_SYNC VCCPWRGOOD_1 VCCPWRGOOD_0 SM_DRAMPWROK VTTPWRGOOD TAPPWRGOOD RSTIN#

MISC THERMAL CLOCKS DDR3 MISC JTAG & BPM PWR MANAGEMENT

SOCKET989

BCLK BCLK# → BCLK_CPU_P_PCH (25) BCLK_CPU_N_PCH (25)
BCLK_ITP BCLK_ITP# → CLK_ITP_BCLK (7) CLK_ITP_BCLK# (7)
PEG_CLK PEG_CLK# → CLK_DMI_PCH (21) CLK_DMI#_PCH (21)
DPLL_REF_SSCLK DPLL_REF_SSCLK# CLKDREF R0366 1KOhm CLKDREF# R0367 1KOhm

SM_DRAMRST# → M_DRAMRST# (16,17)
SM_RCOMP0 R0331 100Ohm 1%
SM_RCOMP1 R0332 24.9Ohm 1%
SM_RCOMP2 R0333 130Ohm 1%
PM_EXT_TS#[0] PM_EXT_TS#[1] PM_EXTTS#1 → PM_EXTTS#0 (16,17)
+VTT_CPU RN0301A RN0301B 49.9Ohm RN0301C RN0301D 10KOhm
PRDY# PREQ# → XDP_PRDY# (7) XDP_PREQ# (7) IPU
TCK TMS TRST# → XDP_TCLK (7) XDP_TMS (7) XDP_TRST# (7) IPU
TDI TDO TDI_M TDO_M → XDP_TDI_R XDP_TDO_R XDP_TDI_M XDP_TDO_M IPU
DBR# → XDP_DBRESET# (7,22)
BPM#[0:7] → XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7 → XDP_OBS[7:0] (7) IPU

Stuff these resistors for disable IGPU

FDI_FSYNC0 R0398 1KOhm
FDI_FSYNC1 R0397 1KOhm
FDI_LSYNC0 R0396 1KOhm
FDI_LSYNC1 R0395 1KOhm
FDI_INT R0399 1KOhm

H_CPUPWRGD C0301 0.1UF/10V
H_DRAM_PWRGD C0302 0.1UF/10V
H_VTTPWRGD C0303 0.1UF/10V

+VTT_CPU
H_XDPRST# R0313 68OHM
XDP_TMS R0345 51Ohm
XDP_TDI_R R0346 51Ohm
XDP_PREQ# R0347 51Ohm
XDP_TCLK R0348 51Ohm
XDP_TRST# R0354 1% 49.9Ohm

JTAG MAPPING
XDP_TDI_R R0349 /XDP 0Ohm → XDP_TDI (7)
XDP_TDO_M R0350 0Ohm → XDP_TDO (7)
R0351 0Ohm /XDP
XDP_TDI_M R0352 0Ohm
XDP_TDO_R R0353 /XDP 0Ohm

DRAMPWROK: (WW35 MoW)
Choose either one solution: -->Choose solution 2

1. This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
2. Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.

+1.5V
R0320 1% 1.1KOHM
H_DRAM_PWRGD
R0321 1% 3KOhm

+VTT_CPU
R0322 68OHM
H_PROCHOT_S#
Q0301 2N7002
THRO_CPU (30)

ASUSTeK COMPUTER INC. NB1

Title : CPU(1)_DMI,PEG,FDI,CLK,MISC
Engineer: CH_Lin

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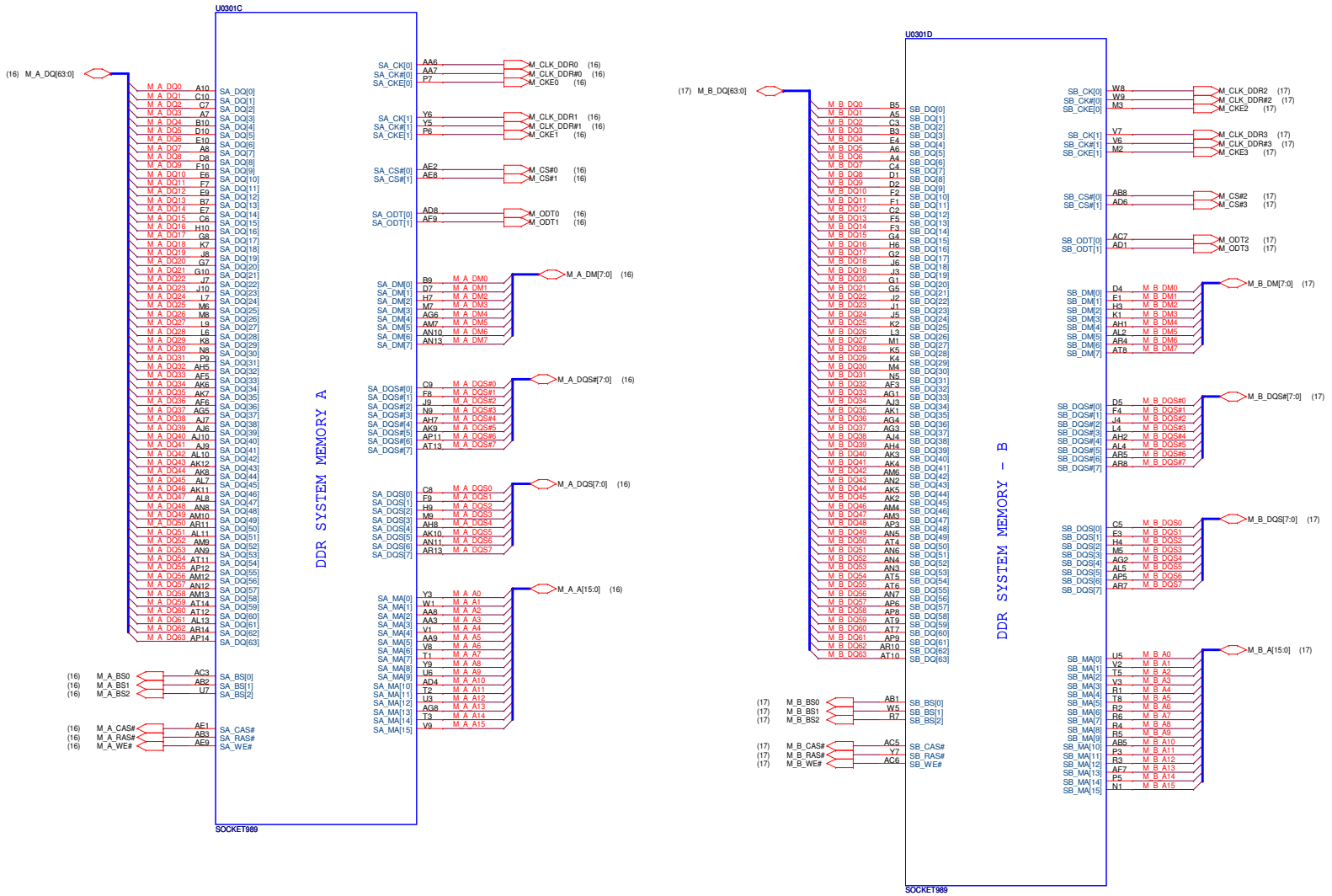

ASUSTeK COMPUTER INC. NB1	Title : CPU(2)_DDR3	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
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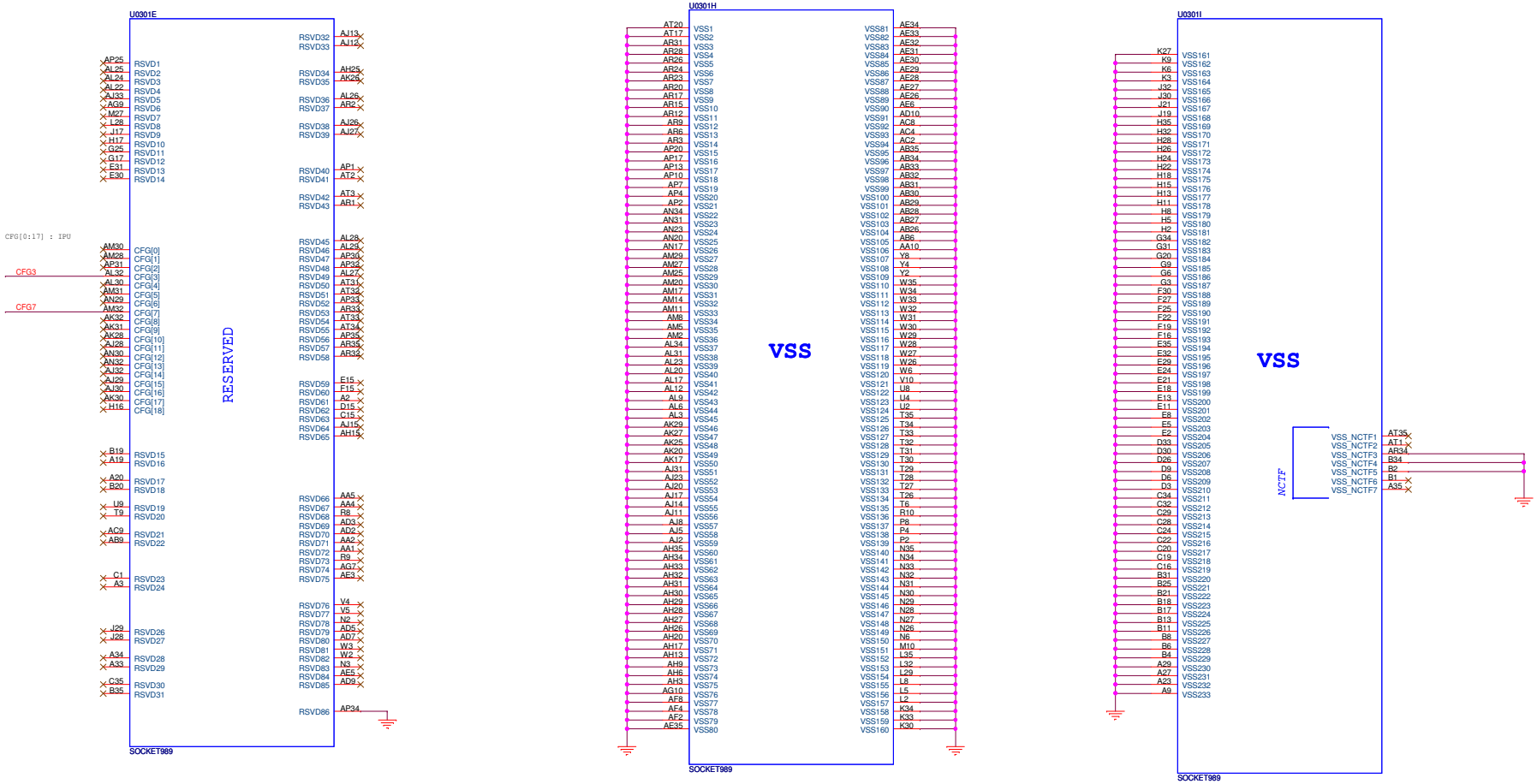

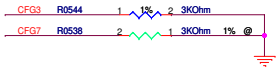

CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal.(Arrandale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.

CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.
CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.
CFG[17:5] - Reserved configuration pins.
Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifucation:
- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.
CFG[3] – Reserved (Used by Arrandale Pporcessors for PCI Express* Static Lane Numbering Reversal)
CFG[11:4] - Reserved configuration pins.
CFG[12] - N/A on Clarksfield processors.
CFG[17:13] - Reserved configuration pins.
Note: Hardware straps are sampled after RSTIN# de-assertion.

ASUSTeK COMPUTER INC. NB1

Title : CPU(3)_CFG,RSVD,GND

Engineer: CH_Lin

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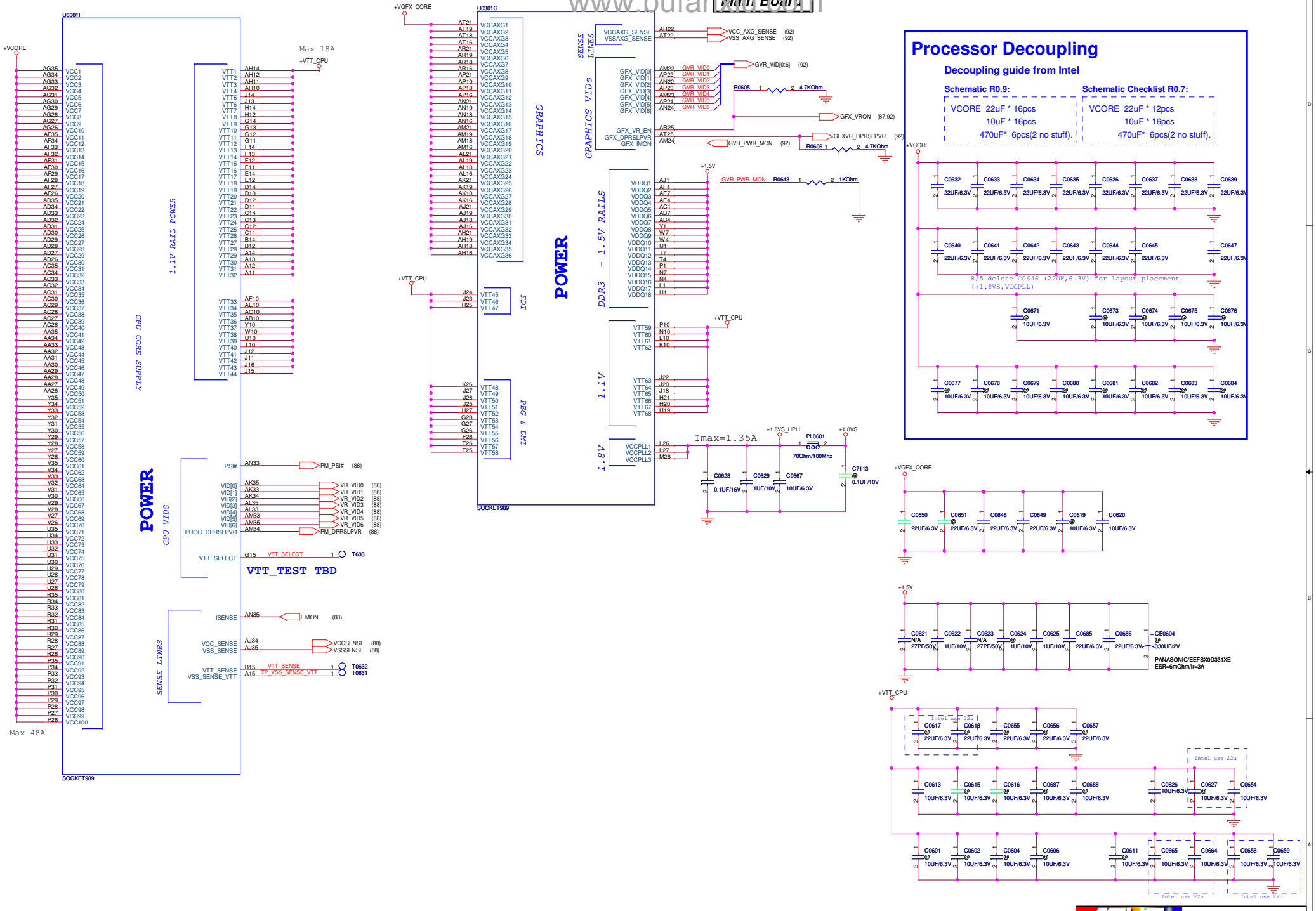
Main Board



Processor Decoupling

Decoupling guide from Intel

Schematic R0.9:

VCORE 22uF * 16pcs
10uF * 16pcs
470uF* 6pcs(2 no stuff).

Schematic Checklist R0.7:

VCORE 22uF * 12pcs
10uF * 16pcs
470uF* 6pcs(2 no stuff).

8/5 delete C0646 (22UF,6.3V) for layout placement.
(+1.8VS,VCCPLL)

PANASONIC/EEFSX0D331XE
ESR=6mOhm/Ir=3A

Intel use 22u

ASUSTeK COMPUTER INC. NB1	Title : CPU(4)_PWR		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
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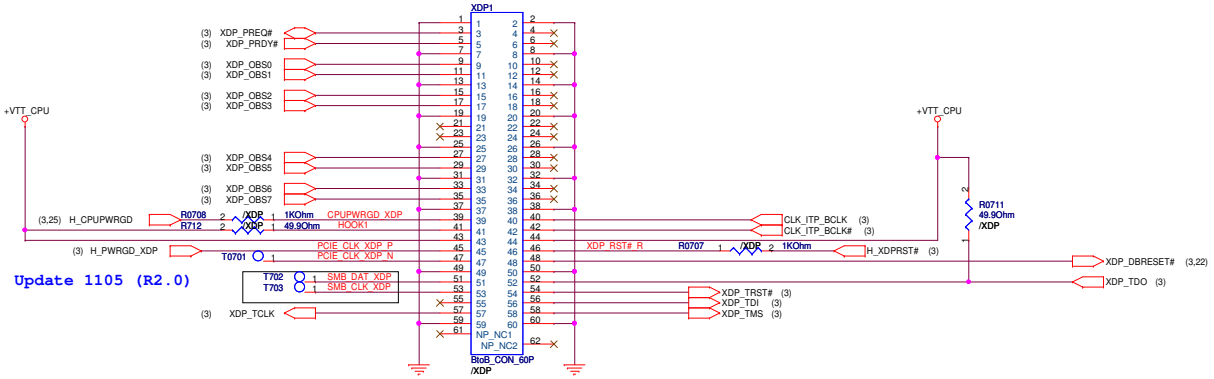
CPU XDP connector



Update 1105 (R2.0)

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
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ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: M60JV		Rev: 1.01
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: M60JV	Rev: 1.01
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: M60JV	Rev: 1.01
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: M60JV		Rev: 1.01
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: M60JV	Rev: 1.01
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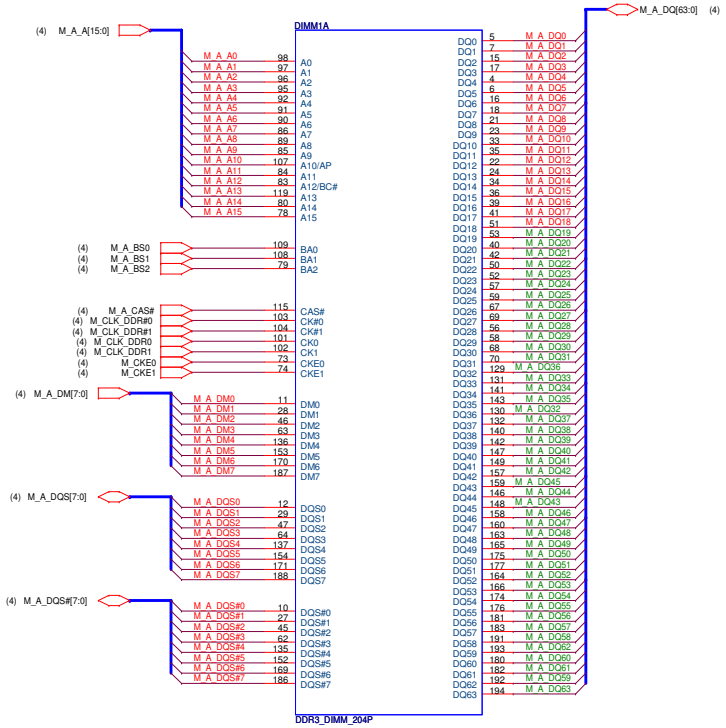
Main Board

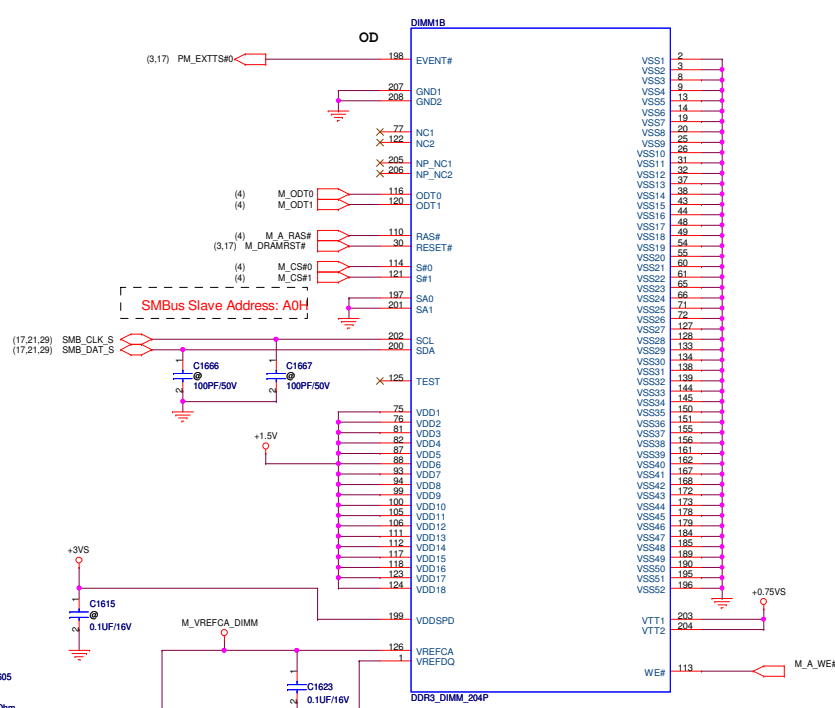
ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: CH_Lin	
Size: Custom	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 13 of 96	

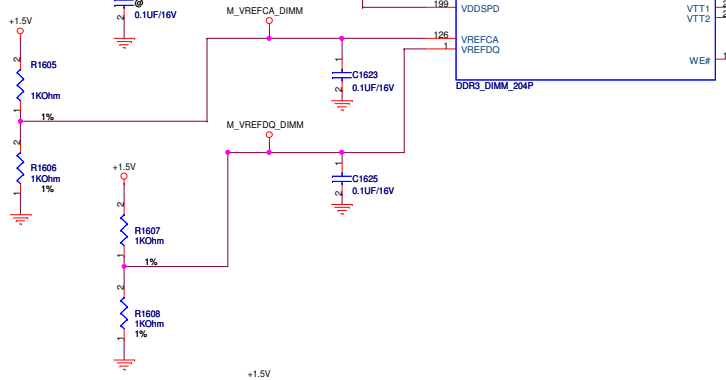
ASUSTeK COMPUTER INC. NB6	Title :	Engineer: CH_Lin
Size: A	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 14 of 96	

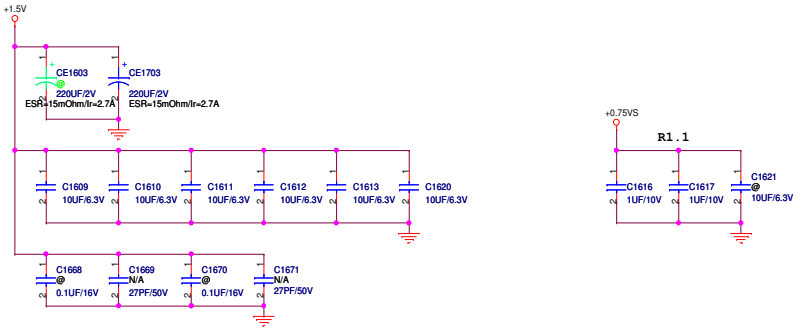
ASUSTeK COMPUTER INC. NB6	Title :	Engineer: CH_Lin
Size: A	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 15 of 96	



REV 9.2mm

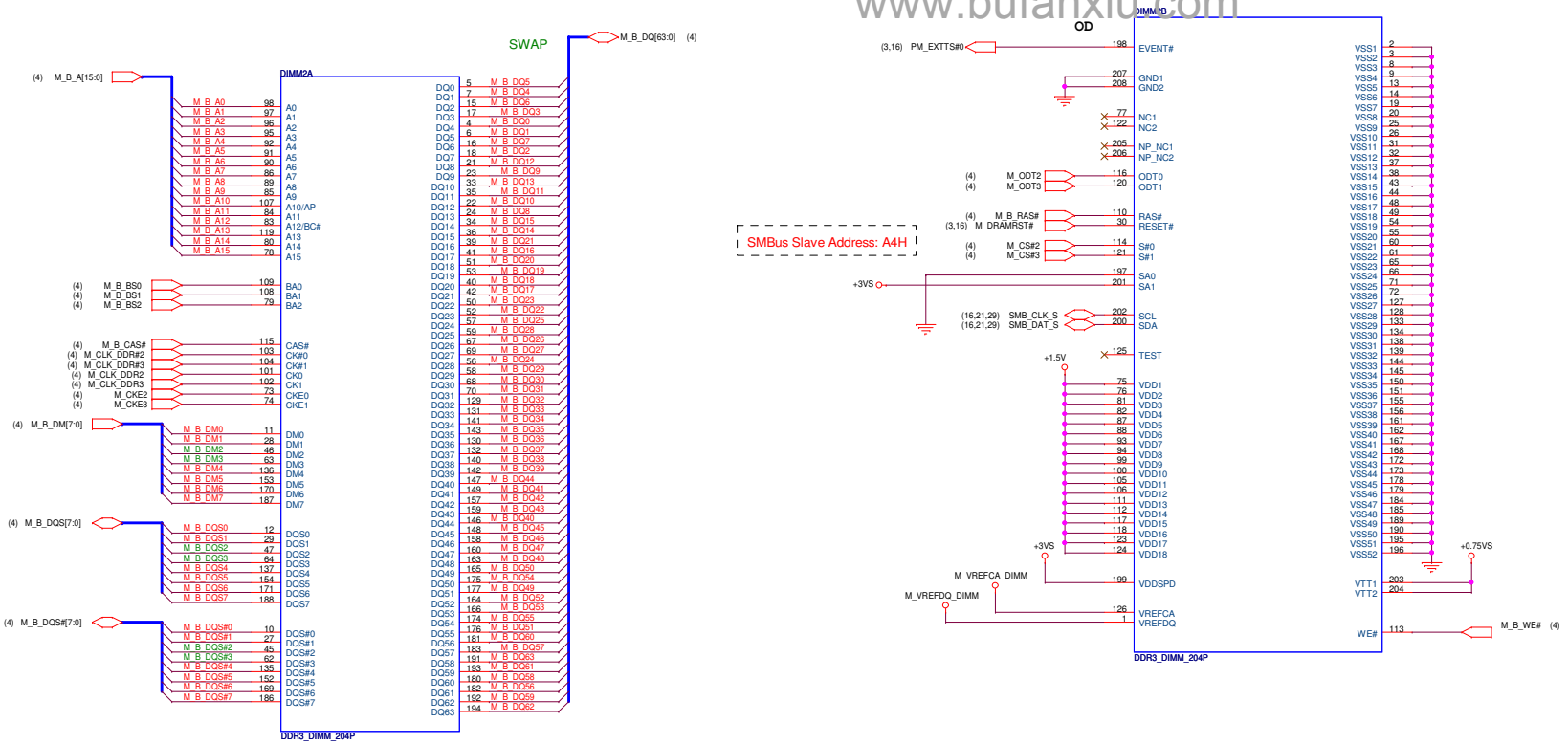






Layout Note: Place these caps near SO DIMMS

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_0	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 16 of 96	



STD 5.2mm

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1		
	Engineer: CH_Lin		
Size C	Project Name M60JV		Rev 1.01
Date: Thursday, November 12, 2009	Sheet 17 of 96		

Title DDR3 CA_DQ VOLTAGE

ASUSTeK COMPUTER INC. NB6

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

Date: Thursday, November 12, 2009 Sheet 18 of 96

Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. **NOTE:** This signal should not be pulled low.
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts.If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination:** 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDATA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDATA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination:** 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high

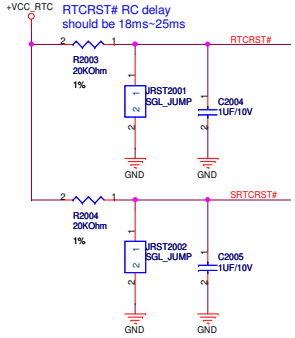
Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN#/GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. **NOTE:** Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. **NOTE:** This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. **NOTE:** A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

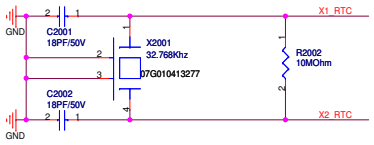
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

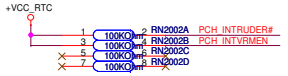


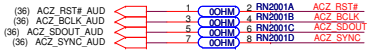
DG2.0 P297
RTCRST# and SRTCRST# can not be shorted together

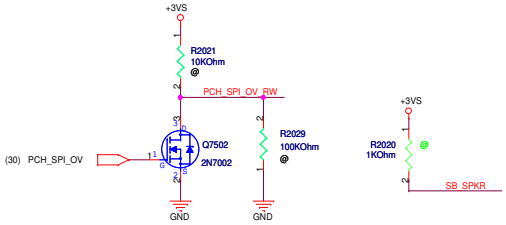
Strap information:

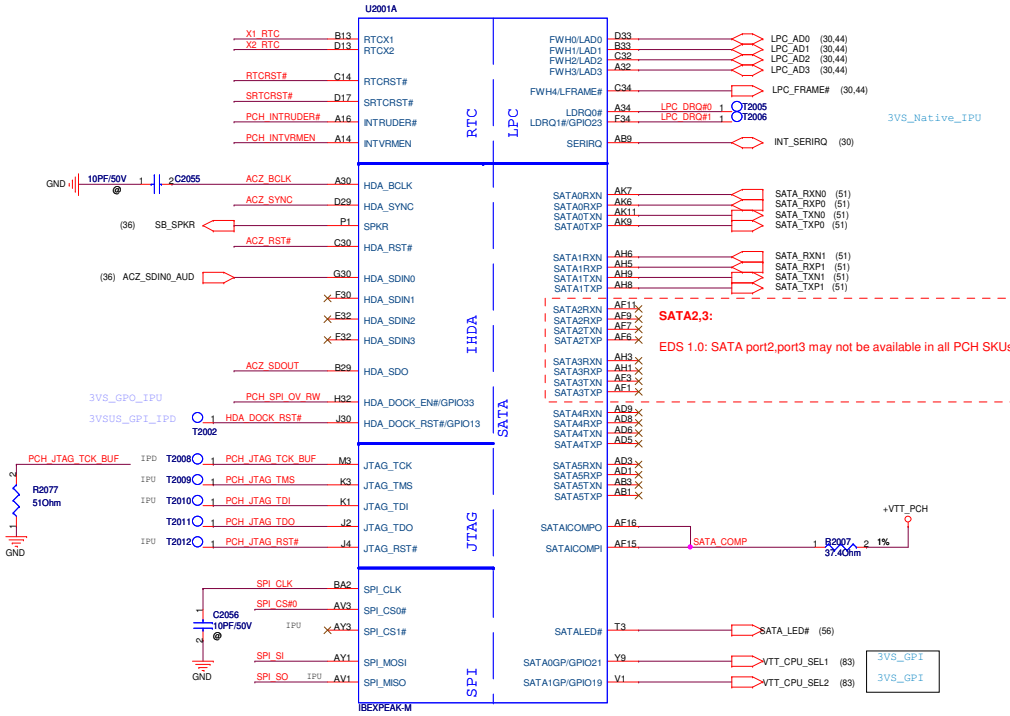
	H	L
ACZ_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_SI: iTPM strap. (IPD)	Enable	Disable
PCH_INTVRMEN Integrated 1.05 V VRM Enable /Disable	Enable	Disable



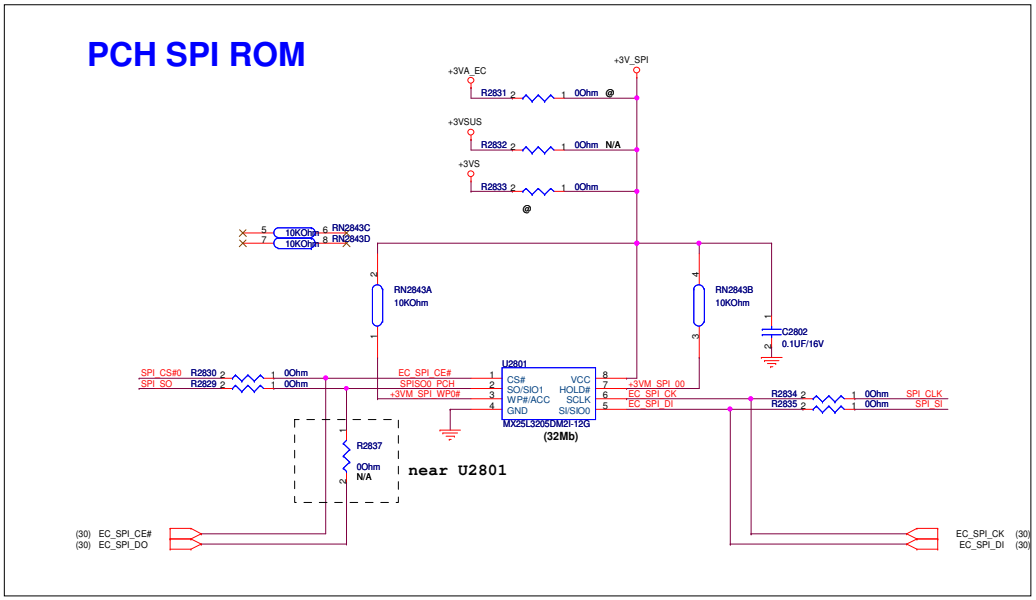


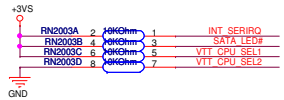






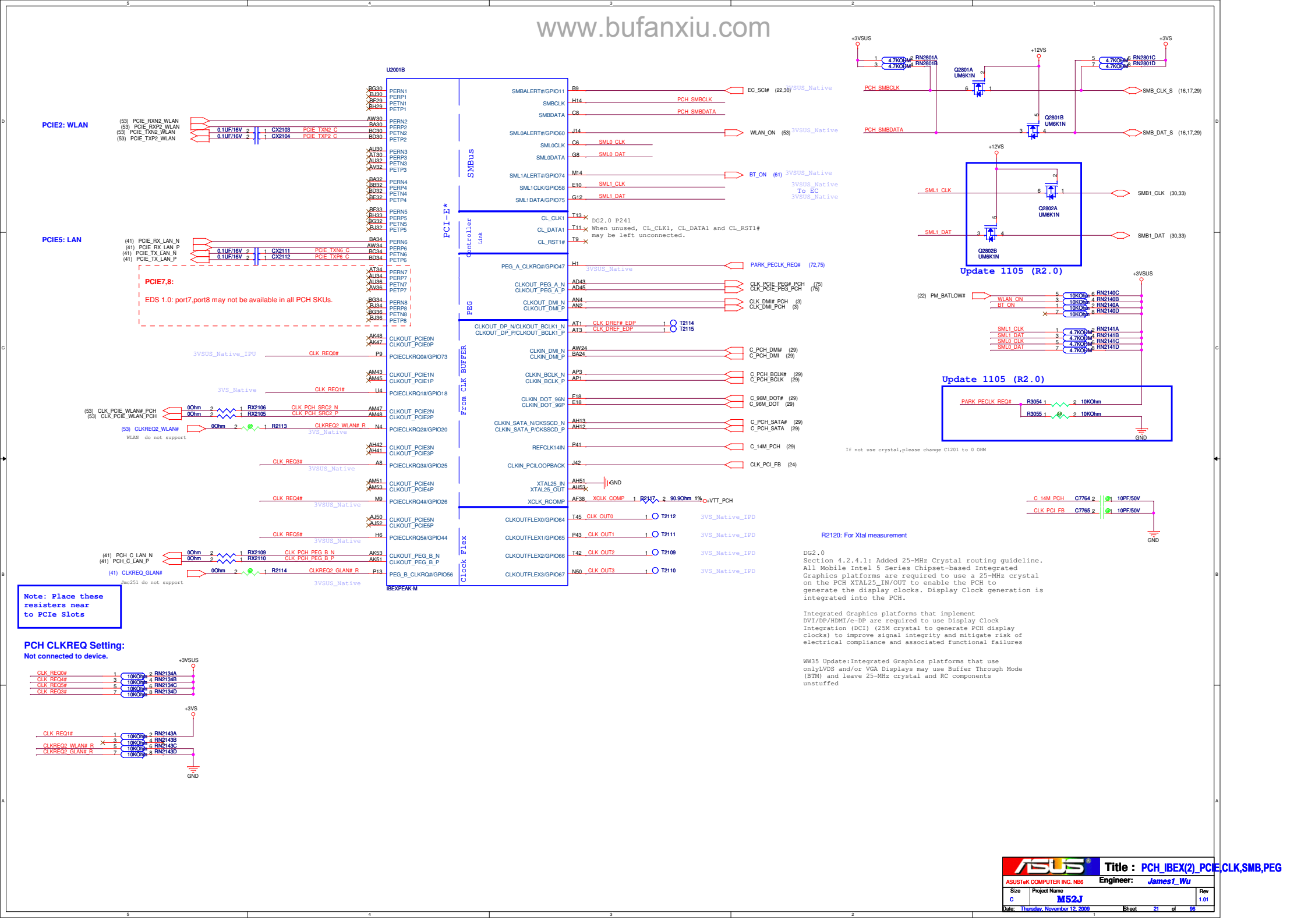
PCH SPI ROM





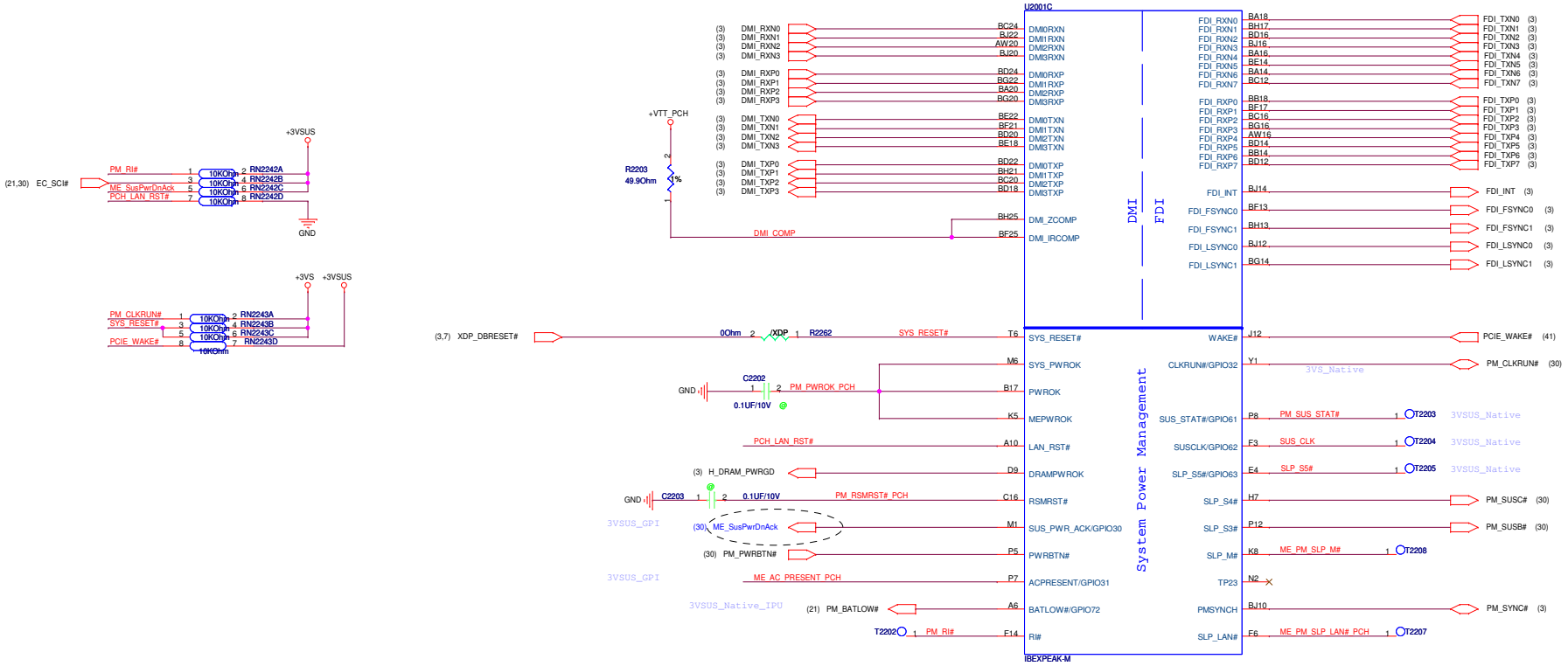
Update 1105 (R2.0)

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(1)SATA,IHDA,RTC,LPC		
	Engineer: James1_Wu		
Size: C	Project Name: M52J		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 20 of 96		



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG		
	Engineer: James1_Wu		
Size: C	Project Name: M52J		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 21 of 96		

pre-ES1 not support
Reversal Feature



R1.1,item L15

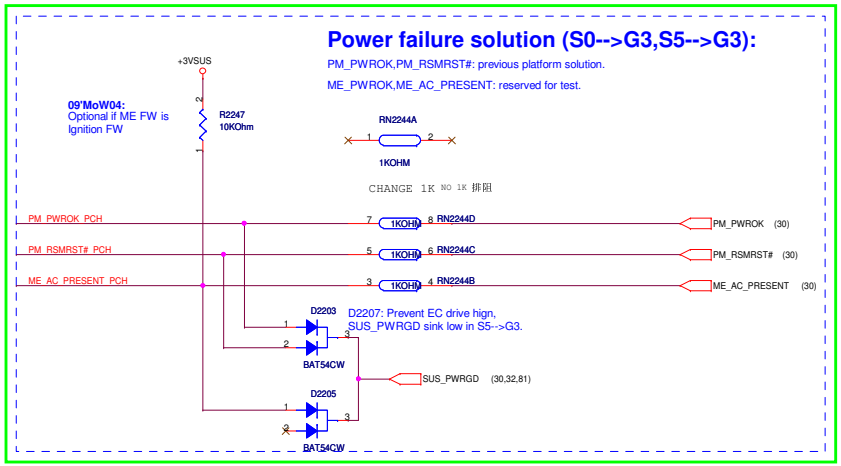


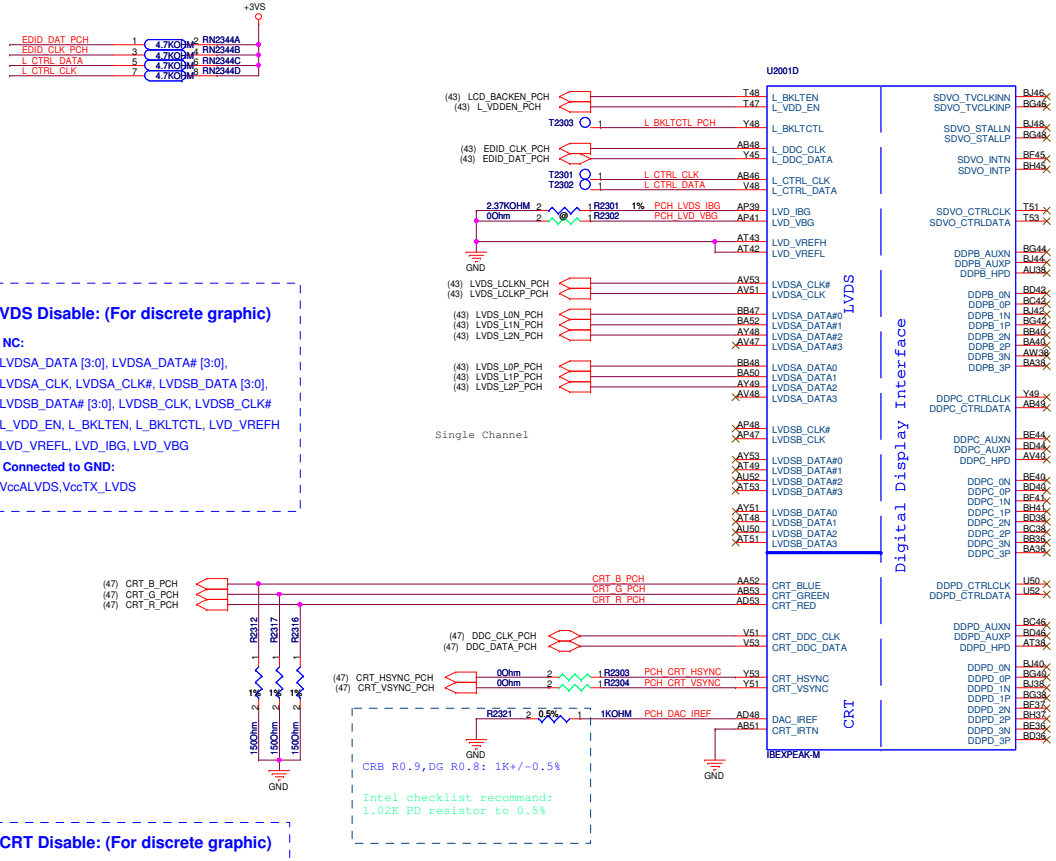
Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required **Note:** Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) **Note:** If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required **Note:** If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(3)_FDI,DMI,SYS PWR	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 22 of 96	



LVDS Disable: (For discrete graphic)

1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

ASUSTeK COMPUTER INC. NB6

Title : PCH_IBEX(4)_DP,LVDS,CRT

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

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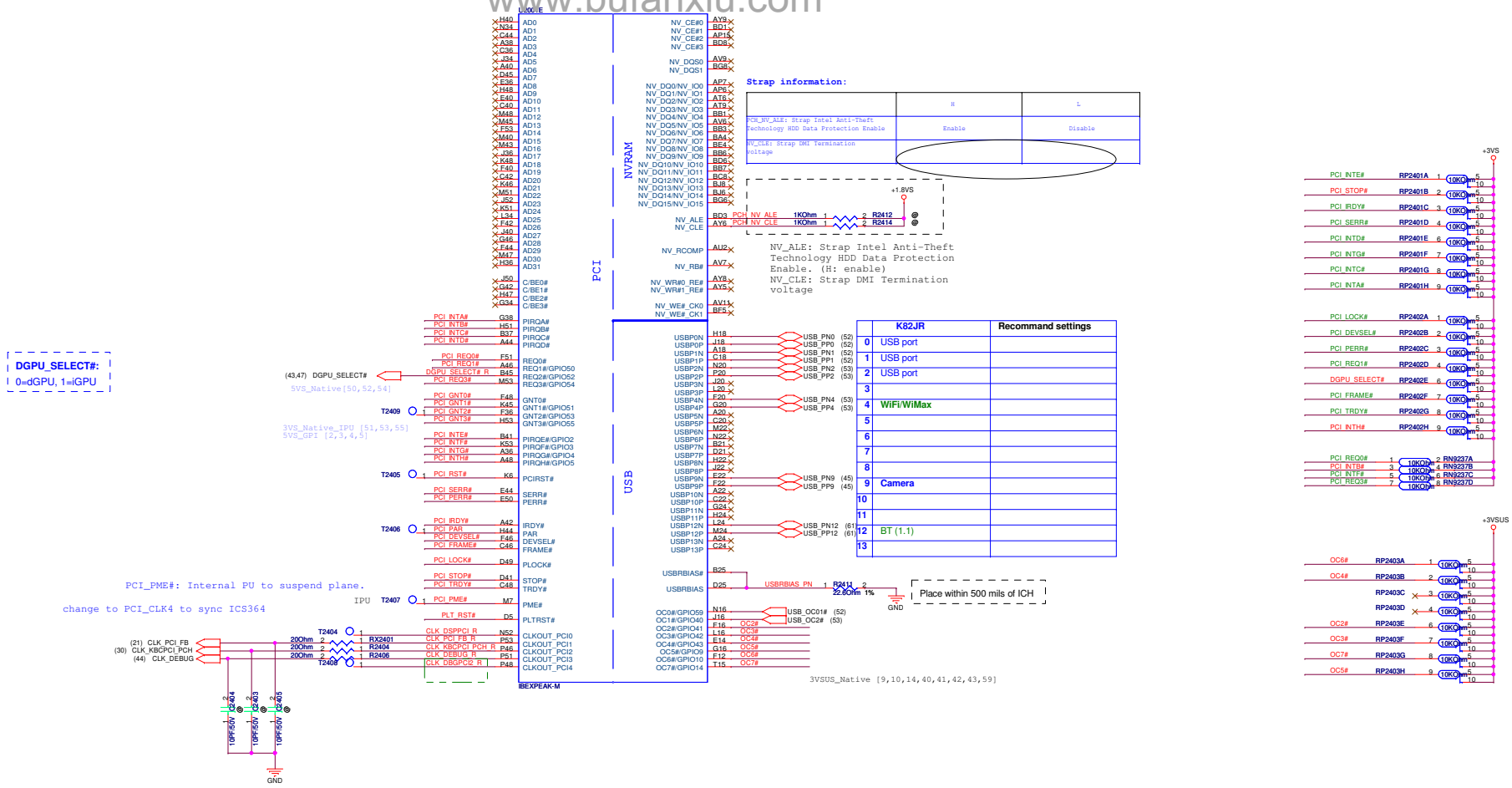


	K82JR	Recommand settings
0	USB port	
1	USB port	
2	USB port	
3		
4	WiFi/WiMax	
5		
6		
7		
8		
9	Camera	
10		
11		
12	BT (1.1)	
13		

GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

Sampled on rising edge of PWROK.

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

Project Name	M60JV	Rev 1.01
Engineer:	CH_Lin	
Title :	PCH_IBEX(5)_PCI,NVRAM,U	
Sheet	24 of 98	

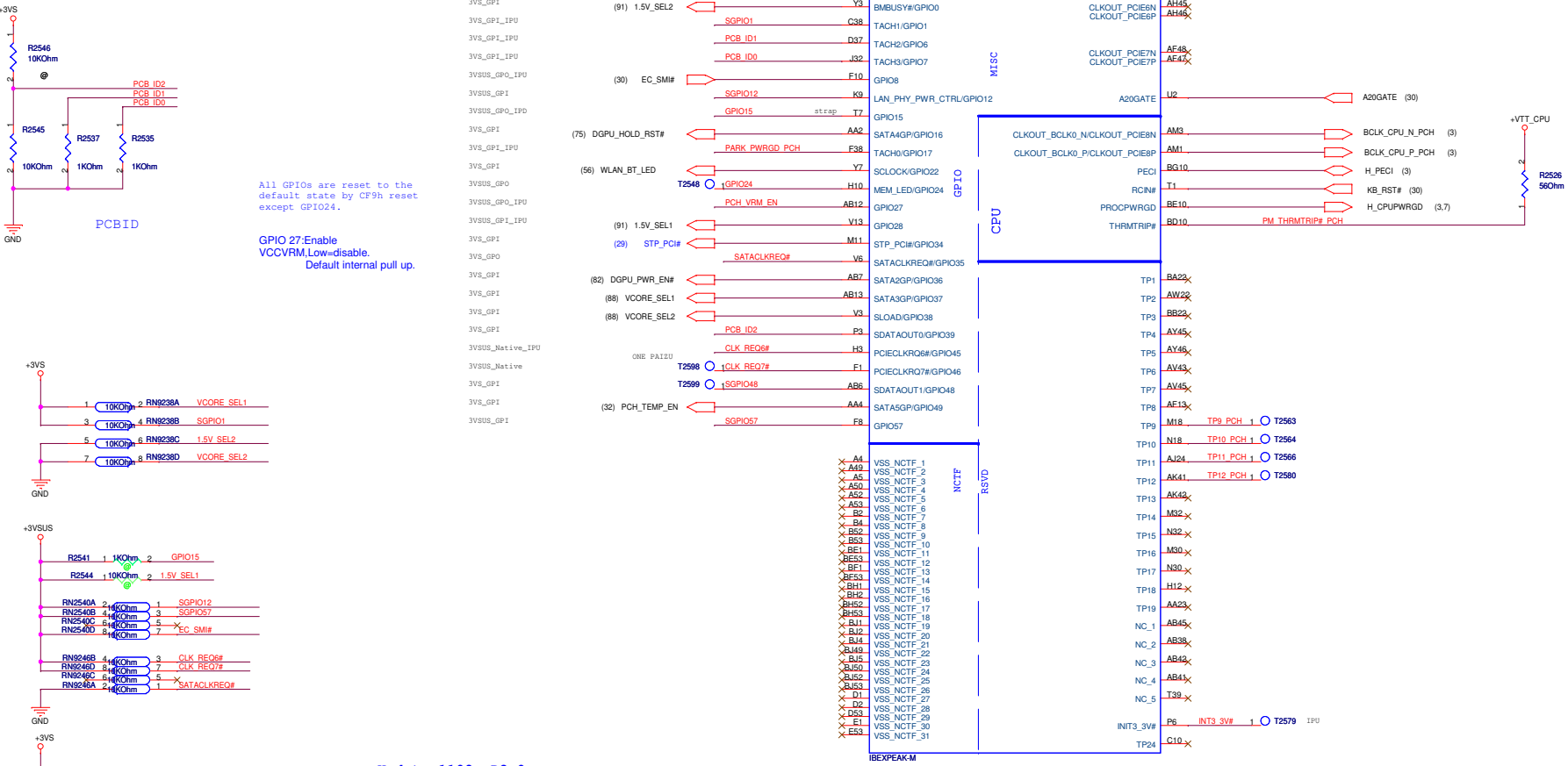
POWER按照提供的default值調節電壓

PCBID

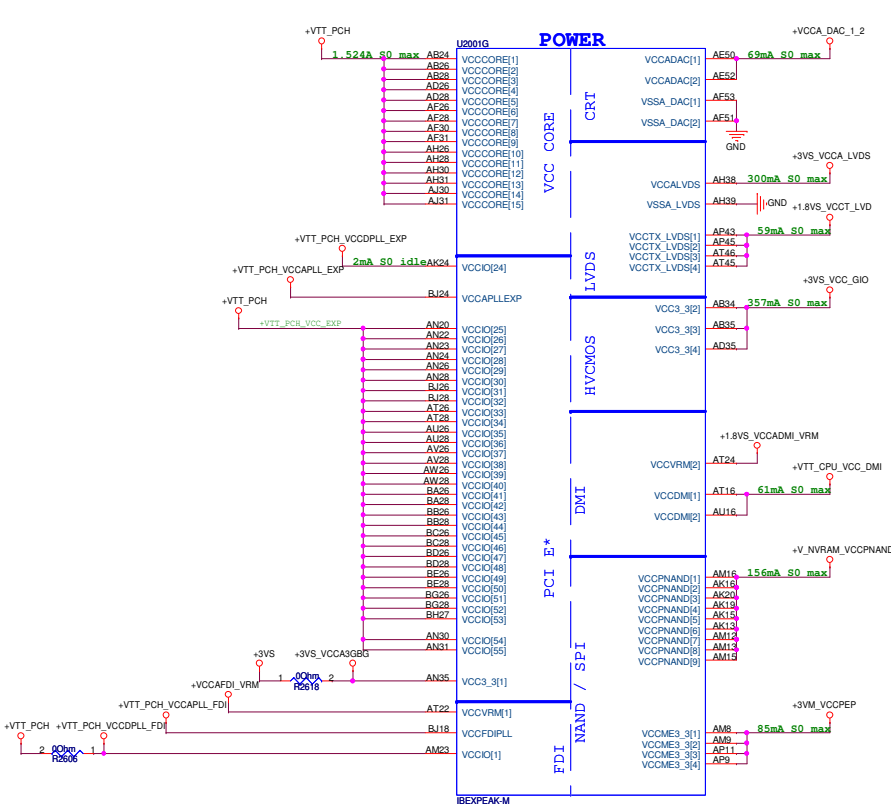
All GPIOs are reset to the default state by CF9h reset except GPIO24.

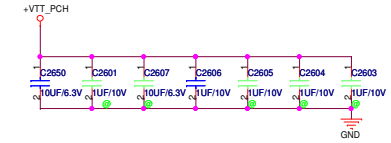
GPIO 27:Enable
VCCVRM,Low=disable.
Default internal pull up.

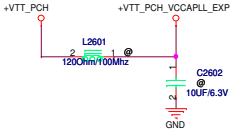
Update 1109, R2.0

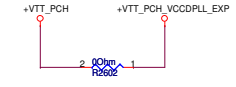


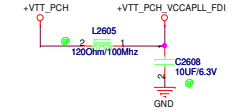
ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(6)CPU,GPIO,MISC		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 25 of 96		

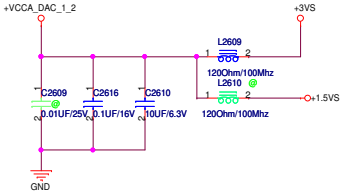


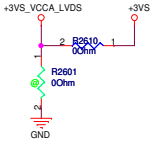


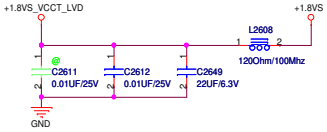


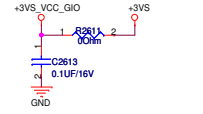


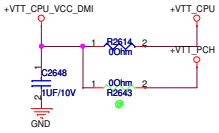


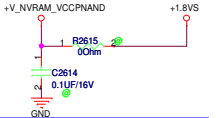


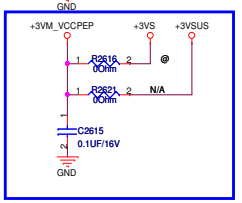






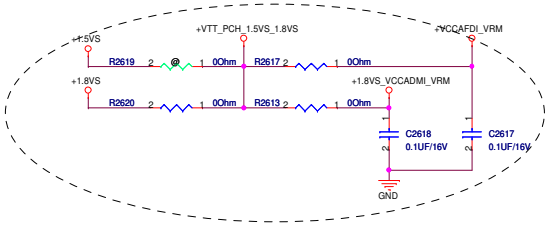




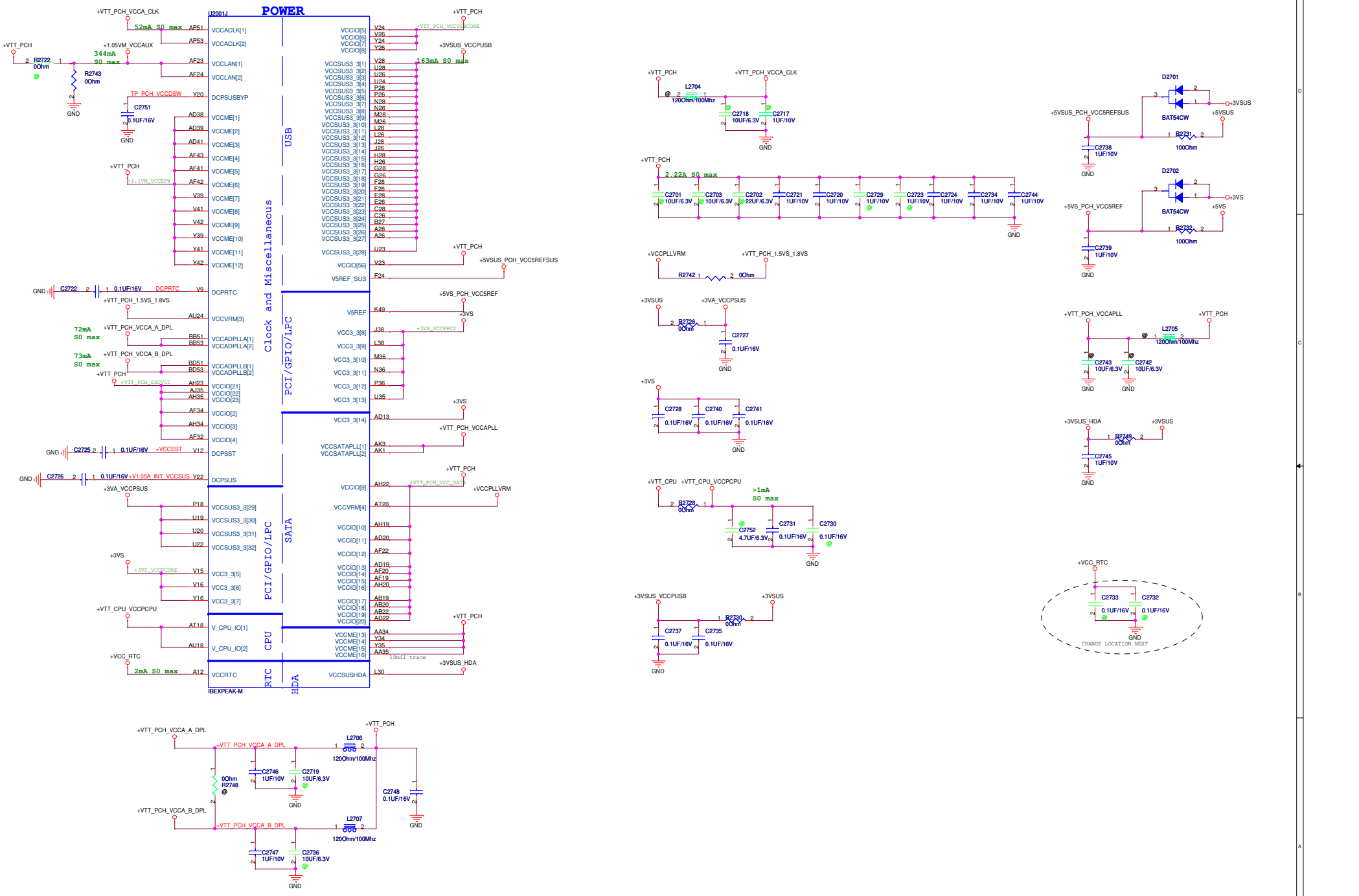


Update 1105 (R2.0)

HDA_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)
Low: 1.8V
High: 1.5V



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(7)_POWER,GND	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 26 of 96	



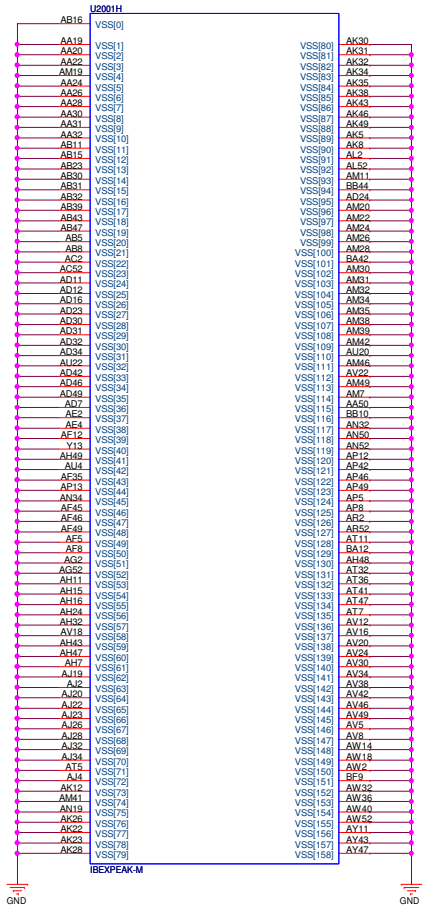
ASUSTeK COMPUTER INC. NB6

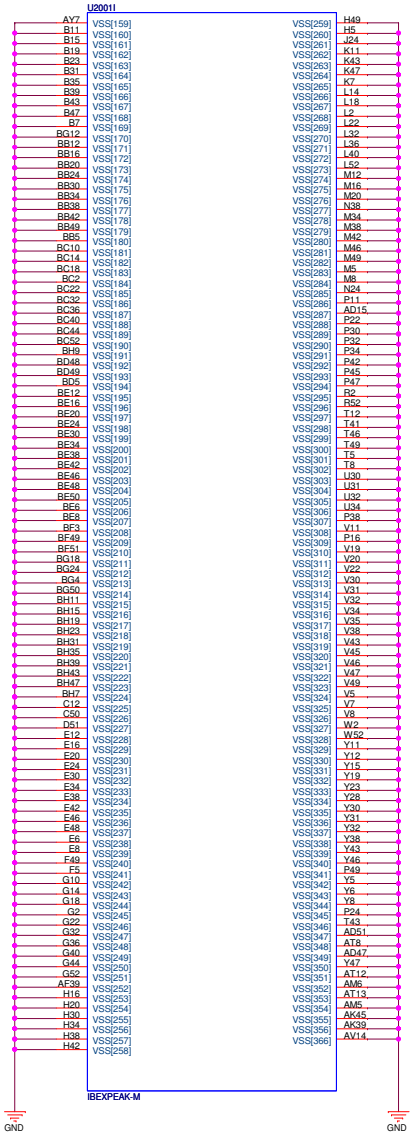
Title :PCH_IBEX(8)_POWER,GND

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

Date: Thursday, November 12, 2009 Sheet 27 of 96





ASUSTeK COMPUTER INC. NB6	Title : PCH GND	
	Engineer: James1_Wu	
Size: C	Project Name: M52J	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 28 of 96	

1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

CR1 1MOhm /X
CX1 14.31818Mhz
C_XIN
C_XOUT
CC4 12PF/50V
CC5 12PF/50V
GND

+3VS
CL1 120Ohm/100Mhz
+3V_CLK
CC9 0.1UF/16V @
CC13 10UF/6.3V c0805_h57
CC12 0.1UF/16V
CC14 0.1UF/16V
CC15 0.1UF/16V
CC16 0.1UF/16V
CC17 0.1UF/16V
CC18 0.1UF/16V
CC19 0.1UF/16V
CC20 0.1UF/16V
CL3 120Ohm/100Mhz
+3V_CLK_VDDA
CC22 0.1UF/16V

VDDxx
min:3.135V max: 3.465V
I: 135mV

CU1
ICS9LPRS427CGLFT

1	VDD1	25MHz/FREERUN	56
2	GND1	PCI&PCIEX_STOP#	55
3	PEREQ1#	CPU_STOP#	54
4	PEREQ2#	REF0/FSLC	53
5	FS4/PCICLK0	DOC_PEREQ3#	52
6	GND2	GND4	51
7	VDDPCI	X1	50
8	ITP_EN/PCICLK_F0	X2	49
9	SEL12_48#/12_48MHz	VDDREF	48
10	Vtt_PwrGd/PD#	SDATA	47
11	VDD2	SCLK	46
12	FSLA/USB_48MHz	GND5	45
13	GND3	CPUT_LR0	44
14	DOTT_96MHzLR	CPUC_LR0	43
15	DOTC_96MHzLR	VDDCPU	42
16	FSLB	CPUT_LR1	41
17	PCIeT_LR0	CPUC_LR1	40
18	PCIeC_LR0	RESET#	39
19	PCIeT_LR1	GNDA	38
20	PCIeC_LR1	VDDA	37
21	VDDPCIEX1	CPUITPT_LR2/PCIeT_LR6	36
22	PCIeT_LR2	CPUITPC_LR2/PCIeC_LR6	35
23	PCIeC_LR2	VDDPCIEX3	34
24	PCIeT_LR3	PCIeT_LR5	33
25	PCIeC_LR3	PCIeC_LR5	32
26	SATACLKT_LR	PCIeT_LR4	31
27	SATACLKC_LR	PCIeC_LR4	30
28	VDDPCIEX2	GND6	29

PEREQ1#
C_REQ#_WLAN
FS4
C_PCI_SB_R
C_48M_R
CLK_EN
C_FSLA
C_FSLB
(21) C_96M_DOT
(21) C_96M_DOT#
(21) C_PCH_DMI
(21) C_PCH_DMI#
(21) C_PCH_SATA
(21) C_PCH_SATA#

C_25M_LAN_R 33Ohm CR6 /X → C_25M_LAN (41), STP_PCI# (25)
STP_CPU#
C_FSLC 33Ohm CR3 → C_14M_PCH (21)
C_REQ#_LAN
C_XIN
C_XOUT
SMB_DAT_S (16,17,21)
SMB_CLK_S (16,17,21)
C_PCH_BCLK (21)
C_PCH_BCLK# (21)
C_DXP CT1
C_DXP# CT2

C2933 /EMI/X 10PF/50V
C2934 /EMI/X 10PF/50V
C_25M_LAN_R
C_FSLC

+3VS
CR14 10KOhm
CLK_EN
CR16 100KOhm
CC31 0.1UF/16V /X
CQ2 2N7002
(88) CLK_EN#

C_FSLA CR10 10KOhm
CR12 10KOhm @
C_FSLB CR13 10KOhm @
CR15 10KOhm
C_FSLC CR17 10KOhm

STP_CPU# CR19 10KOhm
C_48M_R CR11 10KOhm @

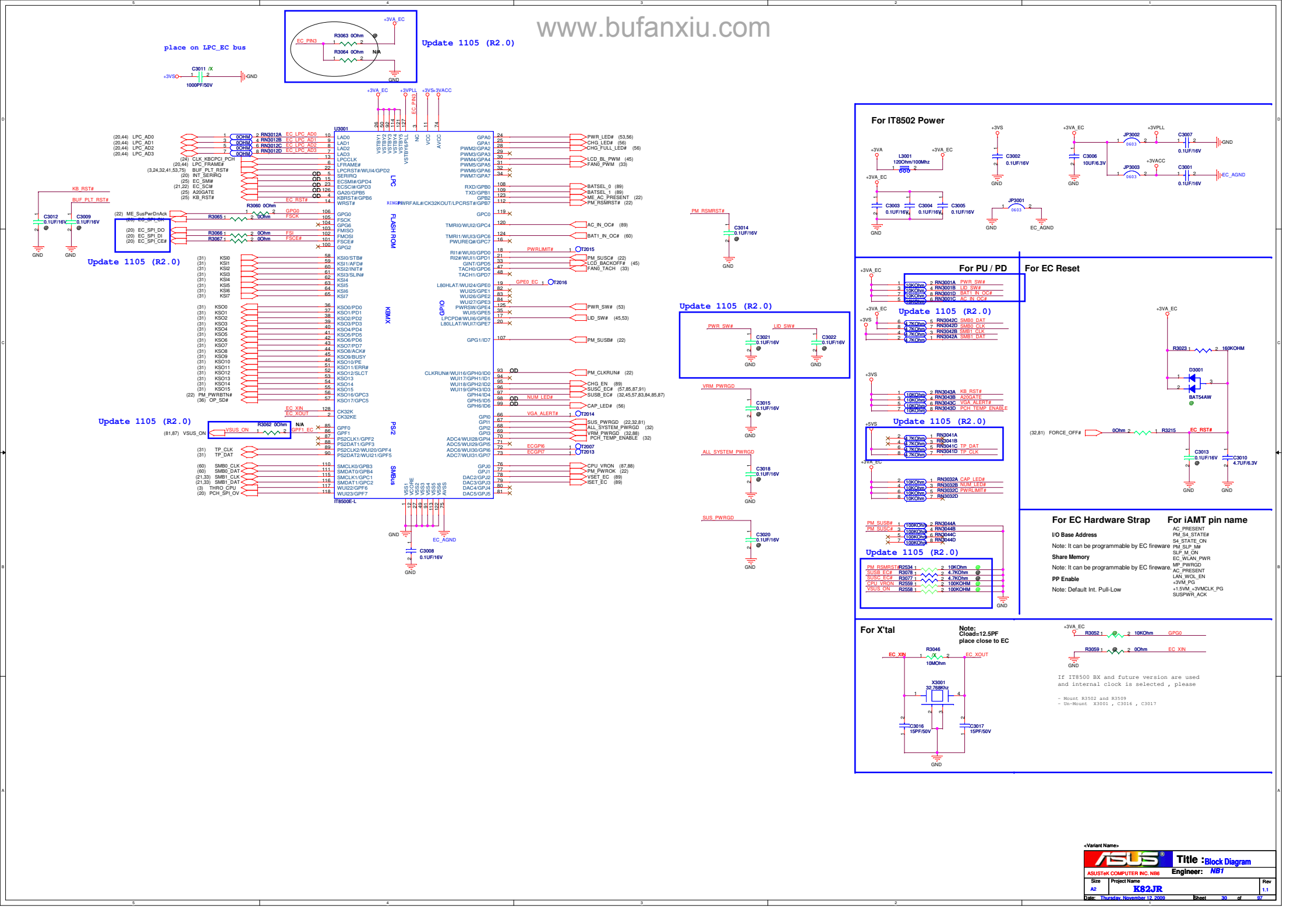
FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133
0	1	0	200

C_REQ#_LAN 10KOhm CRN2A
C_REQ#_WLAN 10KOhm CRN2B
PEREQ1# 10KOhm CRN2C
C_PCI_SB_R 10KOhm CRN2D

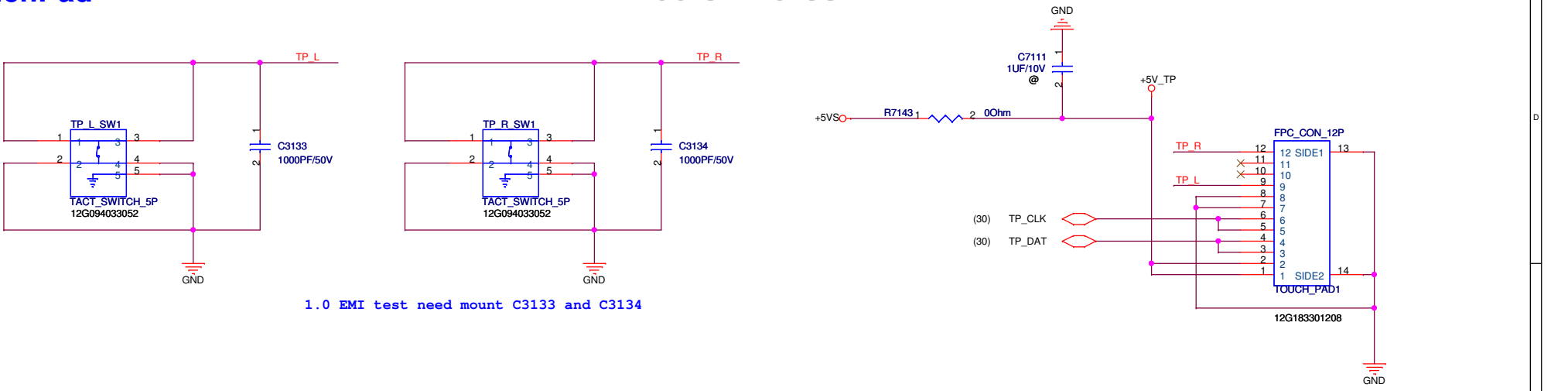
FS4 CR23 /X 10KOhm
CR18 10KOhm

<Variant Name>

ASUSTek Computer INC.
Title : ICS9LPRS427C
Engineer: Nic_wang
Size A3
Project Name 1008P
Rev 1.0G
Date: Thursday, November 12, 2009
Sheet 29 of 96



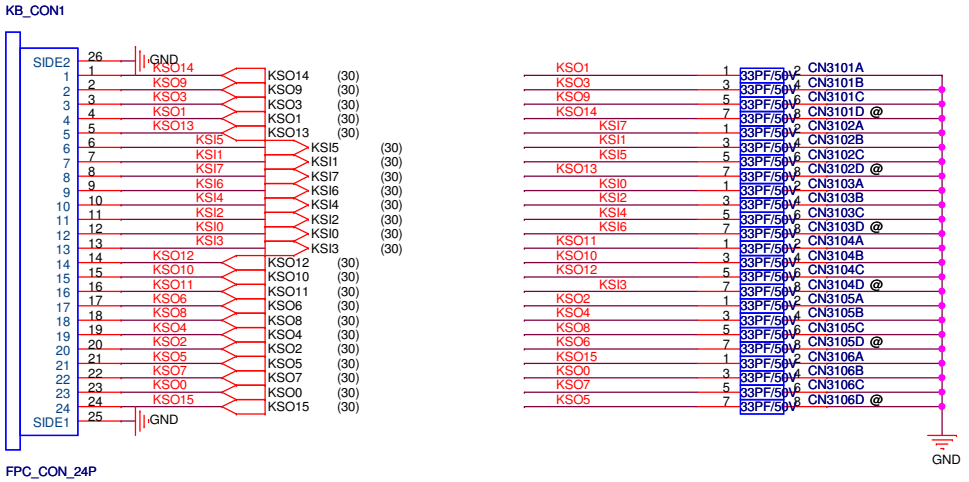
TouchPad



1.0 EMI test need mount C3133 and C3134

Keyboard Connector

EMI Request



<Variant Name>

Title : Block Diagram

ASUSTeK COMPUTER INC. NB6

Engineer: Jeff Kao

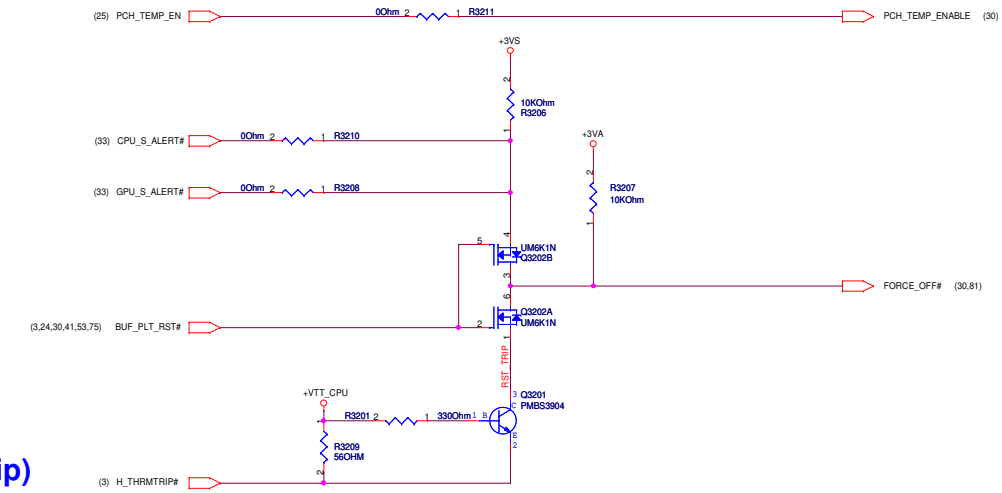
Size	Project Name	Rev
Custom	K70SC	1.1

Date: Thursday, November 12, 2009 Sheet 31 of 97

Thermal Policy

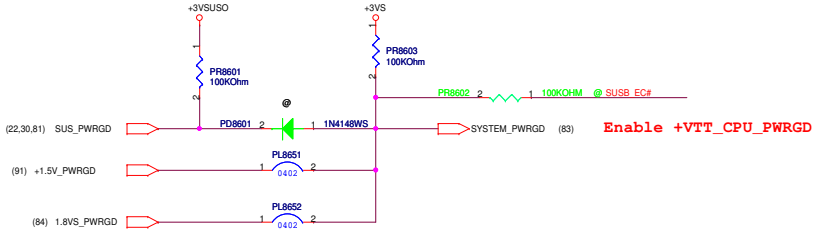
Input 1(sensor)

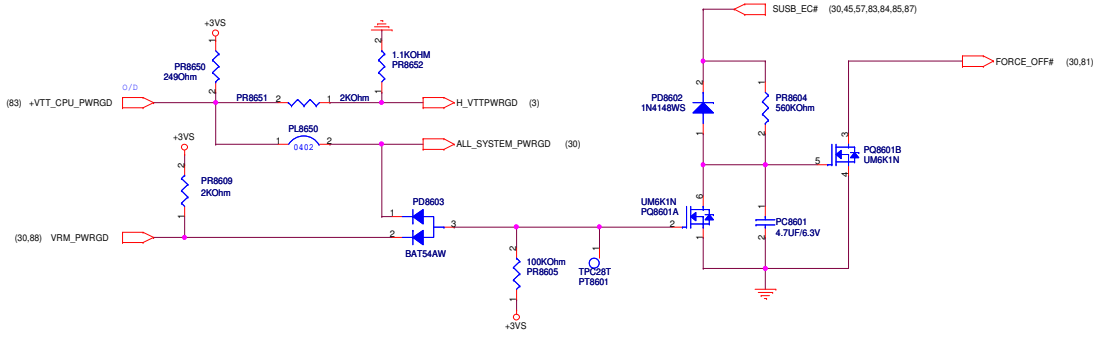
Input 2(thermtrip)



Output (shut down)

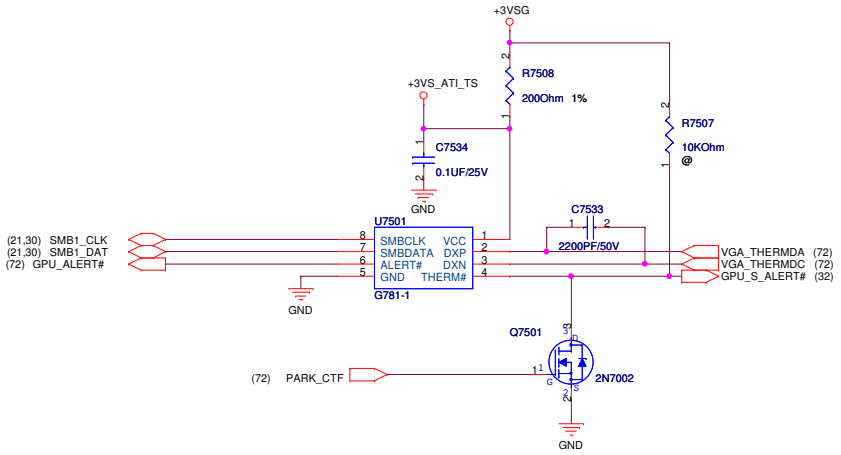
POWER GOOD DETECTER





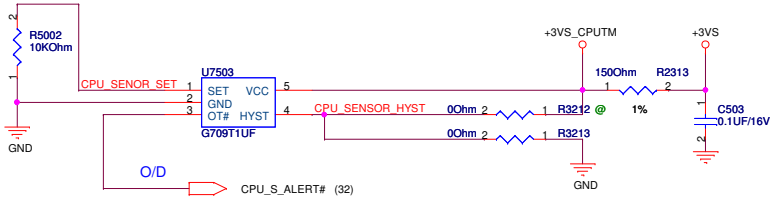
ASUSTeK COMPUTER INC. NB4	Title : Forceoff#_PWRGD_Thermal		
	Engineer: NB1		
Size: C	Project Name: K82JR		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 32 of 96		

GPU Thermal Sensor



CPU Thermal Sensor

Update 1108 (R2.0)

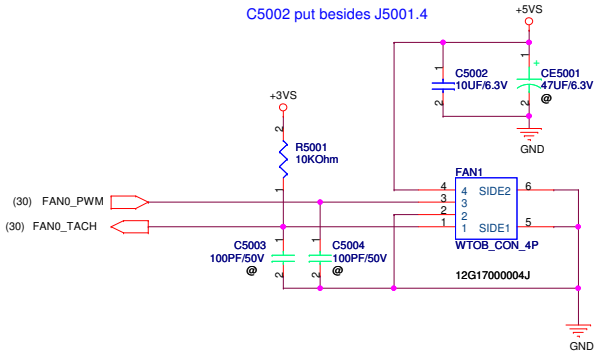


HYST=VCC : 10 degree
HYST=GND : 10 degree C

U7503 under CPU socket

PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.



ASUSTeK COMPUTER INC

Title : AR8131

Engineer:

Size	Project Name	Rev
Custom	LAN Design IP	108

Date: Thursday, November 12, 2009 Sheet 33 of 96

移至 USB BOARD

<Variant Name>

Title : 8131

ASUSTeK COMPUTER INC

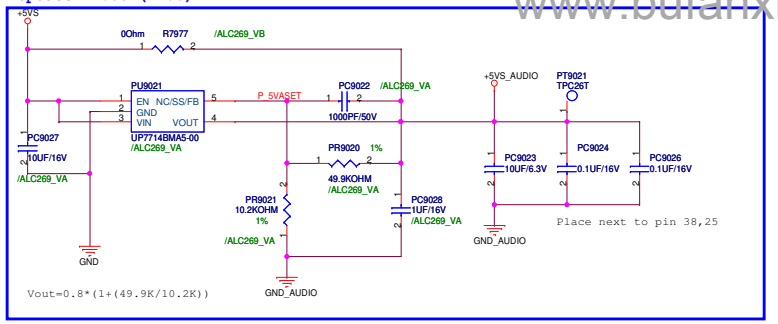
Engineer:

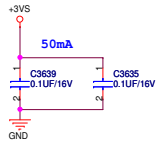
Size	Project Name	Rev
Custom	LAN Design IP	108

Date: Thursday, November 12, 2009 Sheet 34 of 96

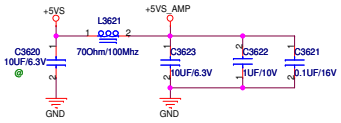
ASUSTeK COMPUTER INC. NB4	Title : MDC_****		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 35 of 96		

Update 11.08 (R2.0)

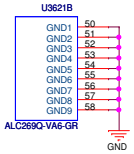




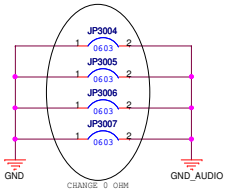
Close to pin1, 9



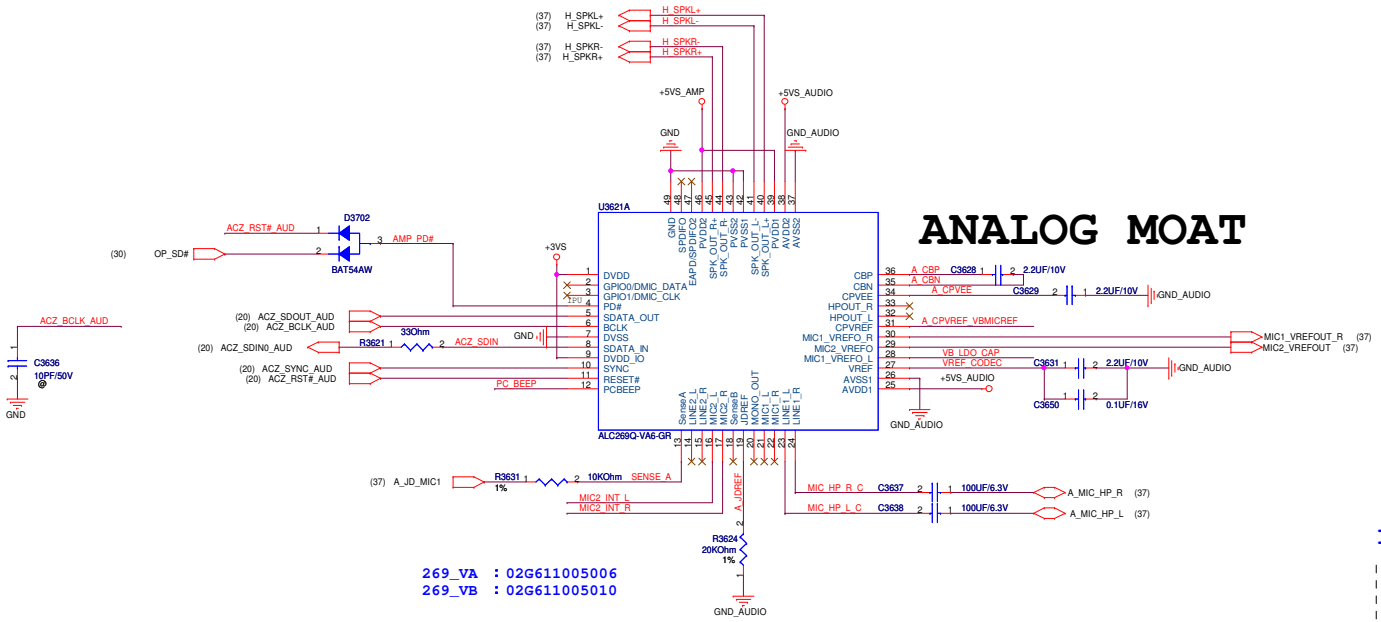
Place next to pin 39,46



For EMI

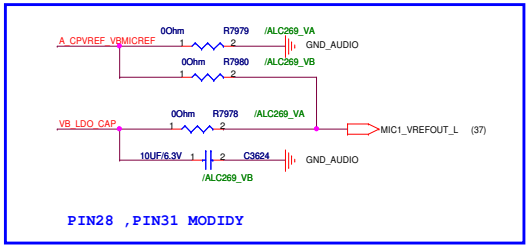


ANALOG MOAT

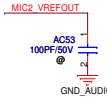


269_VA : 02G611005006
269_VB : 02G611005010

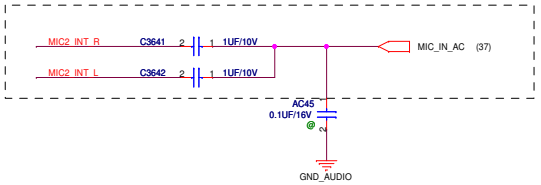
Update 11.08 (R2.0)



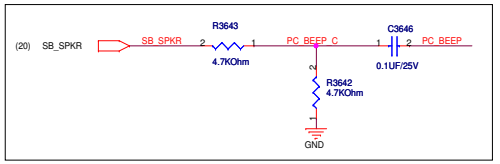
PIN28 ,PIN31 MODIDY



INTERNAL MIC



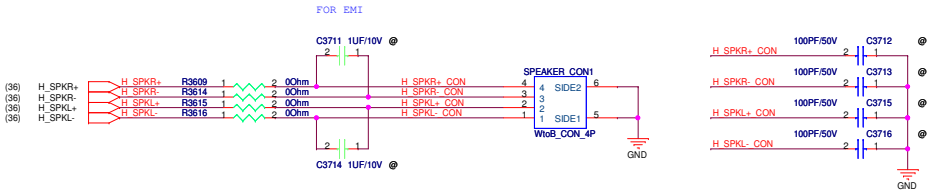
PC BEEP



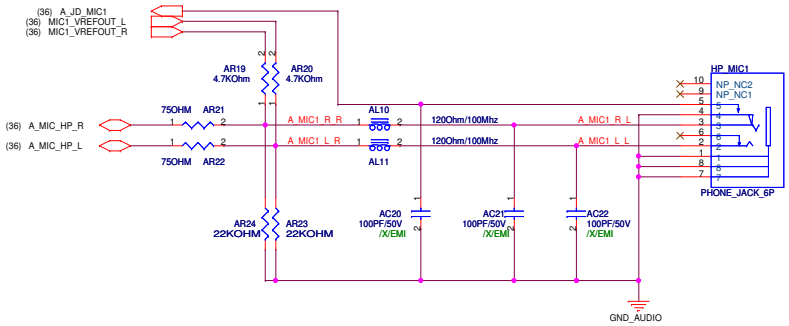
<Variant Name>

ASUSTeK COMPUTER INC. NB2	Title : CODEC ALC 269	
	Engineer: NB1	
Size: C	Project Name: K82JR	Rev: 1.01
Date: Friday, November 13, 2009	Sheet 36 of 96	

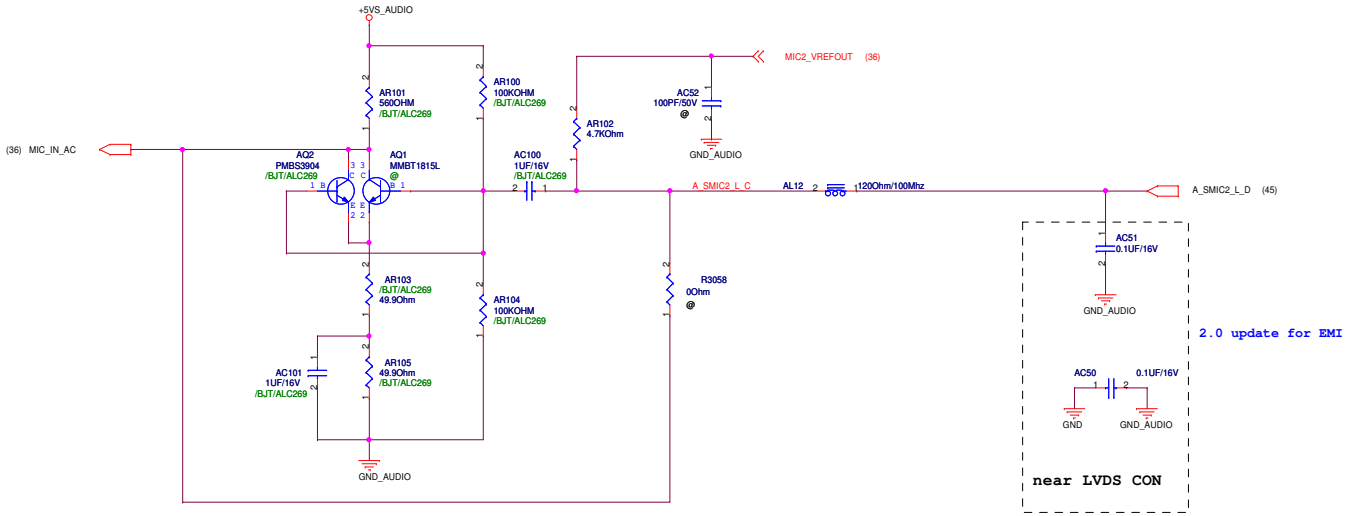
SPEAKER



HP and MIC



Internal MIC and AMP



ASUSTeK COMPUTER INC. NB2	Title :	
	Engineer:	
Size: C	Project Name: K82JR	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 37 of 96	

ASUSTeK COMPUTER INC. NB4	Title : AUD_FM2010		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 38 of 96		

ASUSTeK COMPUTER INC. NB4	Title : AUD_****		
	Engineer: CH_Lin		
Size: Custom	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 39 of 96		

Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.

<Variant Name>

Title : AU6433D53-GLF

ASUSTek Computer Inc.

Engineer: Fehling_Wang

Size	Project Name	Rev
A3	1008P Card Reader	1.0G

Date: Thursday, November 12, 2009 Sheet 40 of 96

Reference Resistance

LAN_REXT — R3301 12KOhm — GND

D3E Enable/Disable

R3309	R3308	D3E
Unmount	Mount	Enable
Mount	Unmount	Disable

+VDD33 — R3309 0Ohm @ — 0Ohm R3308 — BUF_PLT_RST# — LAN_MPD

U3301 JMC251-V10

+VDD33, +1.2V_DVDD, GND

LAN_REXT, LANXIN, LANXOUT, LAN_LX, LAN_FB12

(21) PCH_C_LAN_N, (21) PCH_C_LAN_P

(21) PCIE_TX_LAN_P, (21) PCIE_TX_LAN_N

(21) PCIE_RX_LAN_N, (21) PCIE_RX_LAN_P

0.1UF/16V C3315, 0.1UF/16V C3316, LAN_TXN_JMC, LAN_TXP_JMC

(3,24,30,32,53,75) BUF_PLT_RST#

(22) PCIE_WAKE#

(21) CLKREQ_GLAN#

LAN_MPD, LAN_SCL, MS_XD_DETECT#, SD_MMC_DETECT#

MDIO13/XDRB, LAN_SDA

+VDD33, +CR_CARD_POWER (>20mil)

SDD0, SDD1, SDD2, SDD3, SDCMD, JMSDCLK, SDWP

JMSDCLK — R3723 0Ohm — SDCLK — C3321 10PF/50V @ — GND

L_TRDN3 (53), L_TRDP3 (53), L_TRDN2 (53), L_TRDP2 (53), L_TRDN1 (53), L_TRDP1 (53), L_TRDN0 (53), L_TRDP0 (53)

LAN_LED1 — T3302 TPC26T, LAN_LED0 — T3301 TPC26T

+CR_CARD_POWER / +CR_POWER_CON

F3301 0.35A/6V

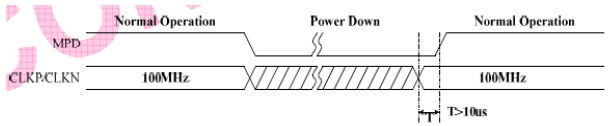
C3322 10UF/6.3V @, C3325 0.1UF/16V, C3324 0.1UF/16V — GND

+CR_POWER_CON — SD_CON1 — SD_SOCKET_9P

SDD2, SDD3, SDCMD, SDCLK, SDD0, SDD1

P_GND2, P_GND1, SDWP, SD_MMC_DETECT#

Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.



BUF_PLT_RST# — C3320 0.1UF/16V — GND

Switch Regulator

LAN_FB12 — JP3302 0603 — +1.2V_DVDD

LAN_LX (>20mil) — L3301 4.7UH — (>20mil)

C3319 10UF/6.3V, C3317 0.1UF/16V, C3305 0.1UF/16V, C3303 0.1UF/16V — GND

Serial EEPROM

+VDD33 — C3323 0.1UF/10V @ — GND

U3302 AT24C08BN-SH-T: A0, A1, A2, GND, VCC, WP, SCL, SDA

R3721 4.7KOhm @, R3722 4.7KOhm @ — LAN_SCL, LAN_SDA

+3VSUS — JP3301 0603 — +VDD33

C3318 10UF/6.3V, C3301 0.1UF/16V, C3310 0.1UF/16V, C3308 0.1UF/16V, C3309 0.1UF/16V — GND

(29) C_25M_LAN — C4122 10PF/50V @ — LANXIN, LANXOUT

X3301 25Mhz — C3312 27PF/50V, C3313 27PF/50V — R7976 33Ohm @ — GND

+VDD33, +CR_POWER_CON

RN4143A SDCMD, RN4143B SDWP, RN4143C SD_MMC_DETECT#, RN4143D MS_XD_DETECT#

+CR_POWER_CON — R3306 1KOhm — MDIO13/XDRB

ASUSTeK COMPUTER INC. NB4	Title : LAN-AR8131	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 1.3
Date: Thursday, November 12, 2009	Sheet 41 of 99	

ASUSTeK COMPUTER INC. NB4	Title : LAN_RJ45	
	Engineer: James1_Wu	
Size: Custom	Project Name: M52J	Rev: 1.3
Date: Thursday, November 12, 2009	Sheet 42 of 99	

(45) LVDS_L0N
(45) LVDS_L0P
(45) LVDS_L1N
(45) LVDS_L1P
(45) LVDS_L2N
(45) LVDS_L2P
(45) LVDS_LCLKN
(45) LVDS_LCLKP

LVDS_LCLKP_VGA @1 0OHM 2 RN4501A LVDS_LCLKP
LVDS_LCLKN_VGA @3 0OHM 4 RN4501B LVDS_LCLKN
LVDS_L0P_VGA @1 0OHM 2 RN4502A LVDS_L0P
LVDS_L0N_VGA @3 0OHM 4 RN4502B LVDS_L0N
LVDS_L1P_VGA @1 0OHM 2 RN4503A LVDS_L1P
LVDS_L1N_VGA @3 0OHM 4 RN4503B LVDS_L1N
LVDS_L2P_VGA @1 0OHM 2 RN4504A LVDS_L2P
LVDS_L2N_VGA @3 0OHM 4 RN4504B LVDS_L2N

PARK_BLON 0Ohm 2 1 R4534 @ LCD_BACKEN
PARK_VDD_EN 0Ohm 2 1 R4535 @ L_VDDEN

U7104 TS5V330CDBQR
(24,47) DGPU_SELECT#
(75) LVDS_LCLKP_VGA
(23) LVDS_LCLKP_PCH
LVDS_LCLKP
(75) LVDS_LCLKN_VGA
(23) LVDS_LCLKN_PCH
LVDS_LCLKN
LVDS_L0P_VGA (75) LVDS_L0P_PCH (23)
LVDS_L0N_VGA (75) LVDS_L0N_PCH (23)
+5VS GND

U7101 TS5V330CDBQR
DGPU_SELECT#
(75) LVDS_L1P_VGA
(23) LVDS_L1P_PCH
LVDS_L1P
(75) LVDS_L1N_VGA
(23) LVDS_L1N_PCH
LVDS_L1N
LVDS_L2P_VGA (75) LVDS_L2P_PCH (23)
LVDS_L2N_VGA (75) LVDS_L2N_PCH (23)
+5VS GND

U7106 PI5C3257QE
DGPU_SELECT#
(72) PARK_BLON
(23) LCD_BACKEN_PCH
(45) LCD_BACKEN
(75) PARK_VDD_EN
(23) L_VDDEN_PCH
(45) L_VDDEN
EDID_DAT_VGA (72) EDID_DAT_PCH (23)
EDID_CLK_VGA (72) EDID_CLK_PCH (23)
EDID_DAT (45)
EDID_CLK (45)
+5VS GND

Update 1110 (R2.0)

+3VS +3VSG
RN9247A EDID_DAT_VGA
RN9247B EDID_CLK_VGA
RN9247C EDID_DAT
RN9247D EDID_CLK
4.7KOHM

+5VS GND
C7106 0.1UF/16V
C7107 0.1UF/16V
C7108 0.1UF/16V
C7109 0.1UF/16V

ASUSTeK COMPUTER INC. NB4

Title : CB_NewCard
Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

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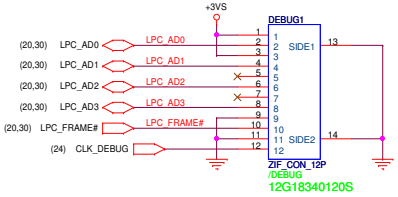
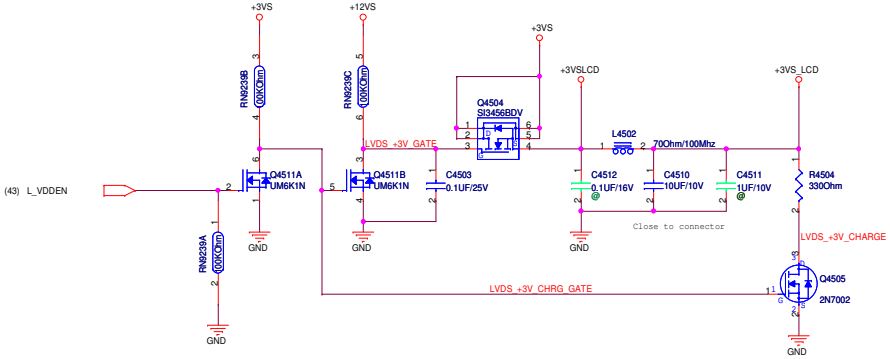
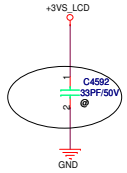
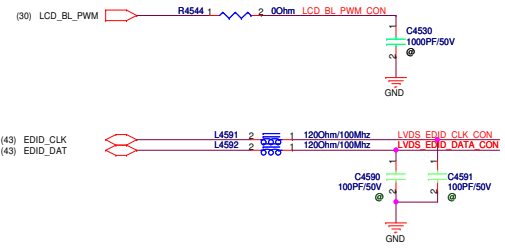
LPC Debug Port

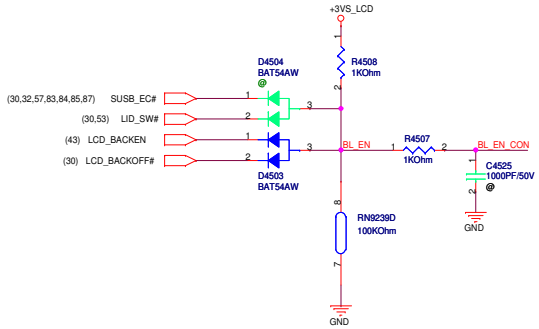


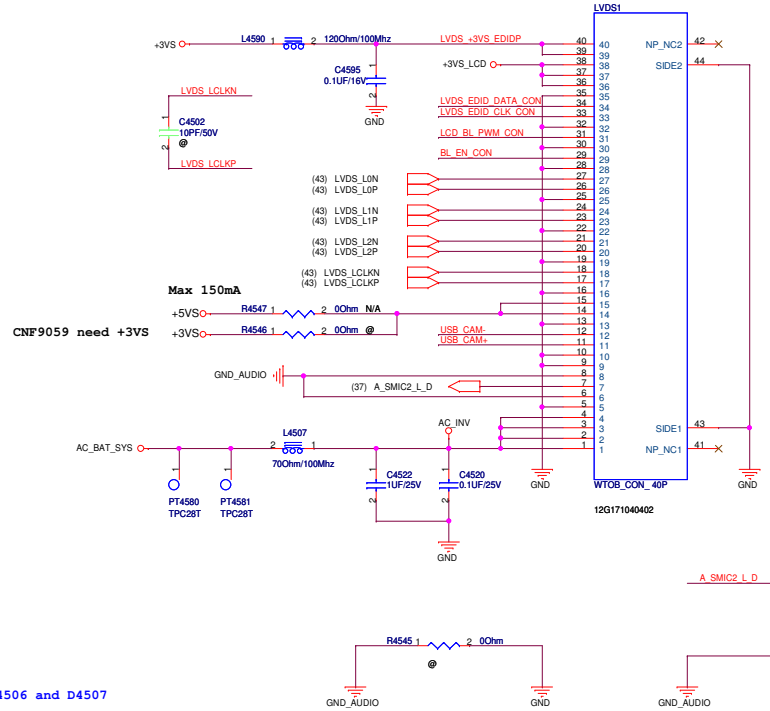
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 44 of 96	

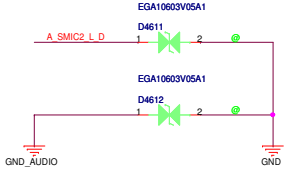


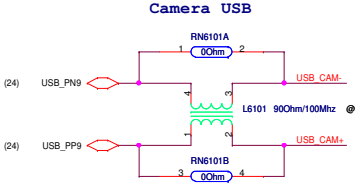


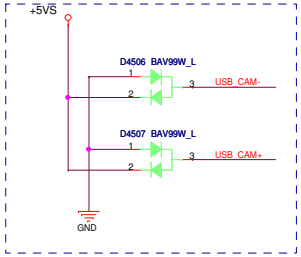












ASUSTeK COMPUTER INC. NB1

Title: LVDS & Inverter CON

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	K40AA	1.00

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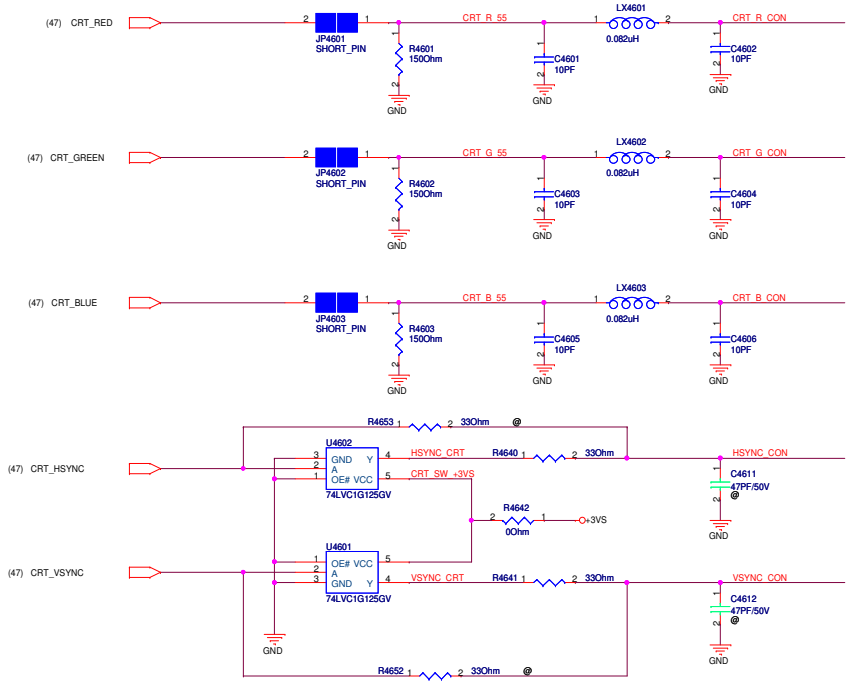
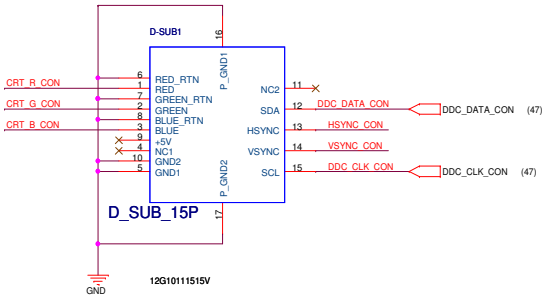
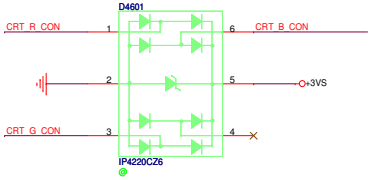
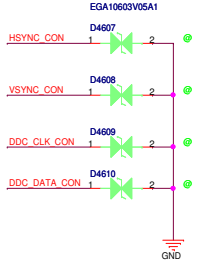
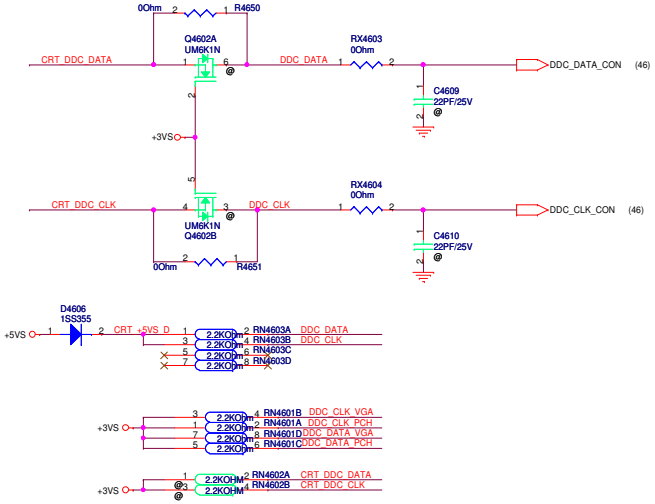


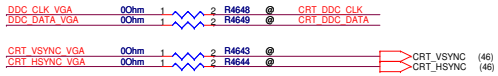


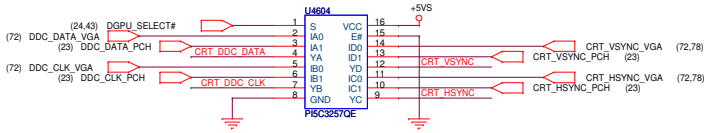




ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 46 of 96	

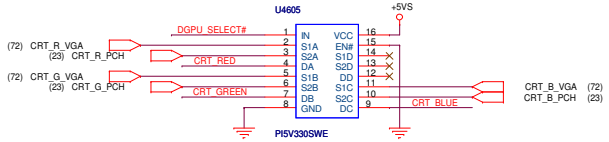






change pin define
A0 TO A1

S=0 for VGA output
S=1 for PCH output



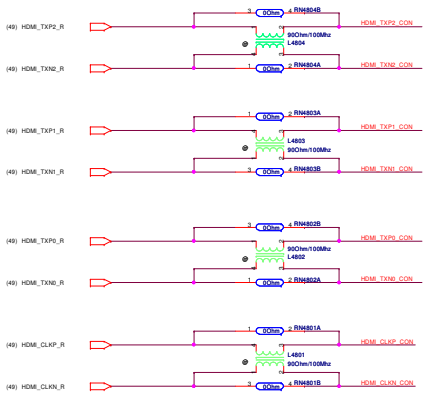
PI5V330SWE bandwidth=570MHz

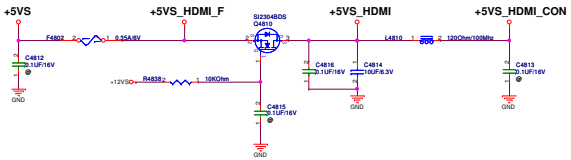
PCH analog RAMDAC=350MHz.
(2048x1536 with 32bit color at 75Hz)

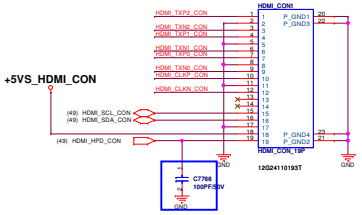
S=0 for VGA output
S=1 for PCH output

ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 47 of 96	

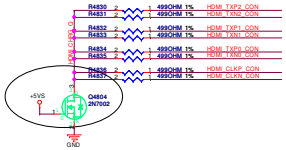
Near CON J4801



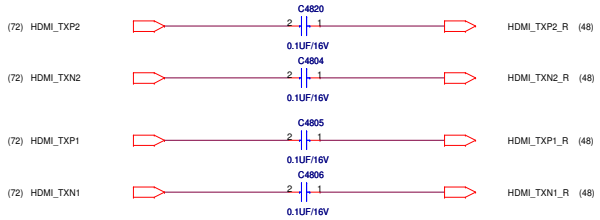


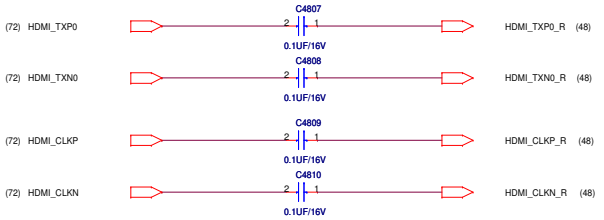


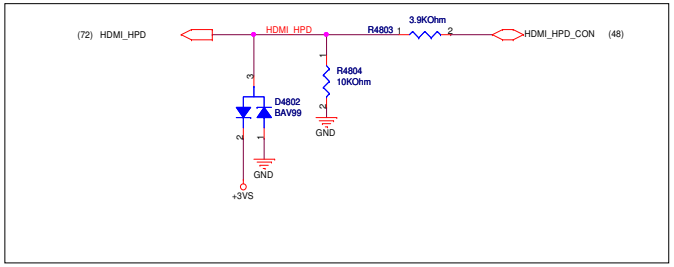
Update 1108 (2.0) EMI Add

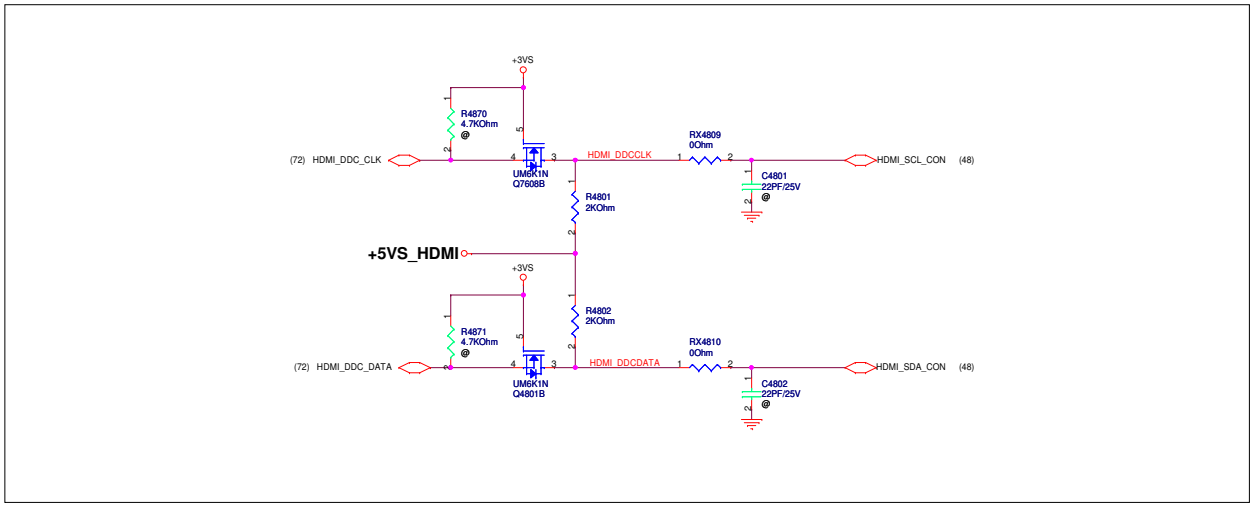


Title : TV_HDMI		
ASUSTeK COMPUTER INC. NB4	Engineer: CH_Lin	
Size: D	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 48 of 96	





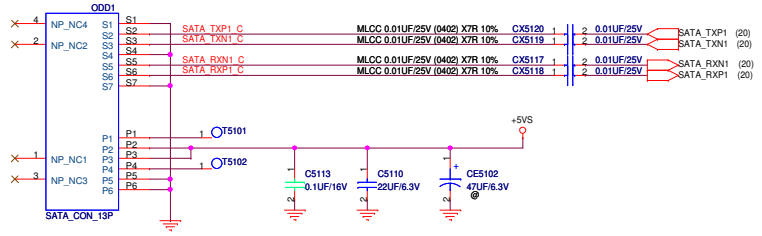




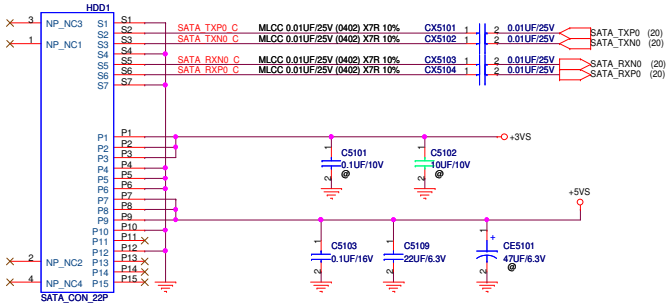
ASUSTeK COMPUTER INC. NB4	Title : TV ****	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Friday, November 13, 2009	Sheet 49 of 96	

ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 50 of 96		

ODD

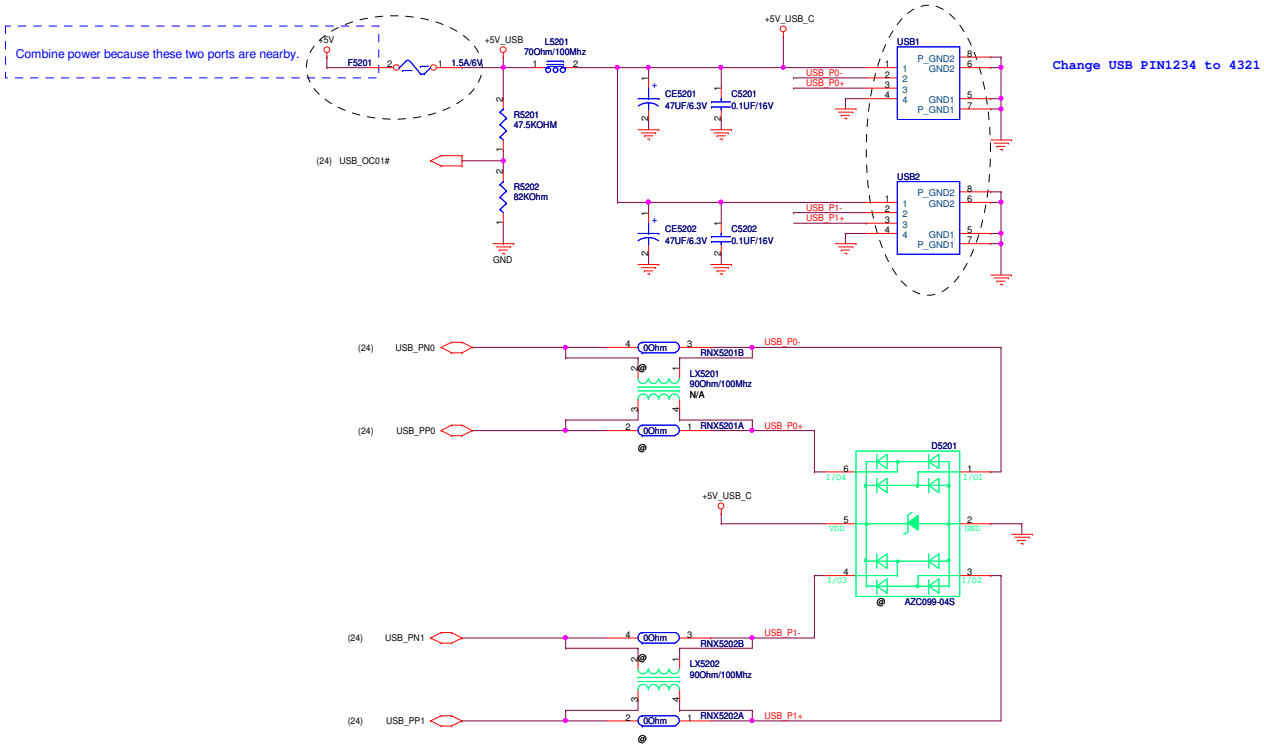


HDD (1st)



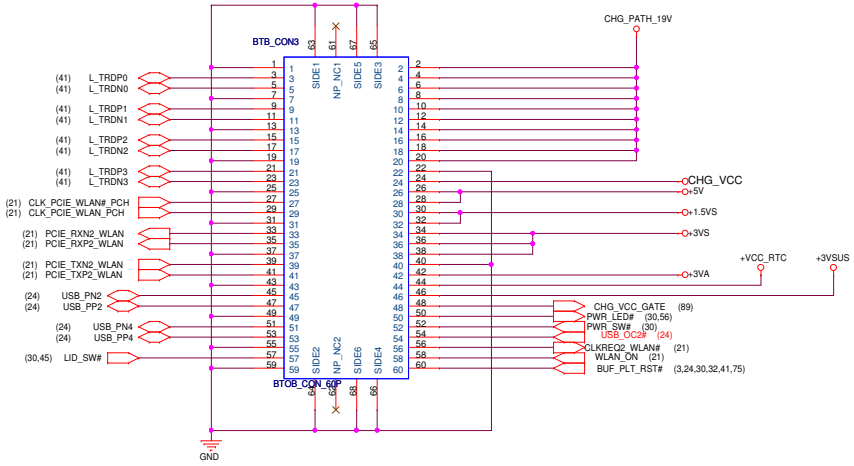
ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 51 of 96	

USB ports



Change USB PIN1234 to 4321

ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *2		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 52 of 96		



ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 53 of 96	

ASUSTeK COMPUTER INC. NB4	Title : BAR_****		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 54 of 96		

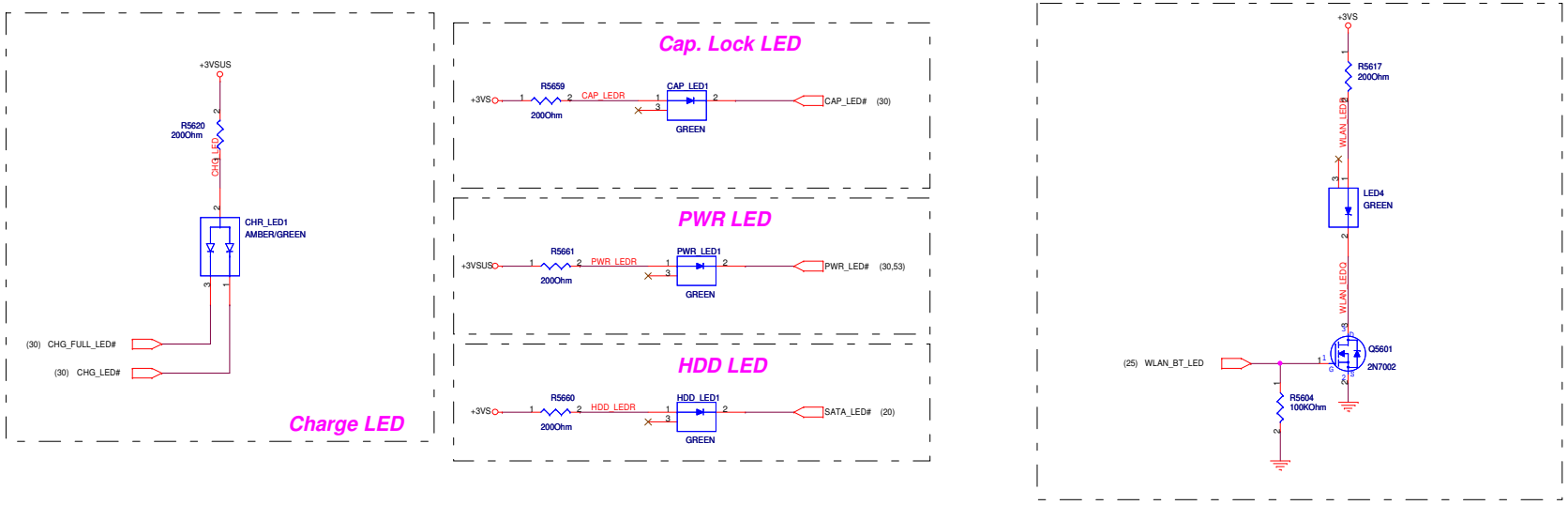
Title : SIO_****

ASUSTeK COMPUTER INC. NB4

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

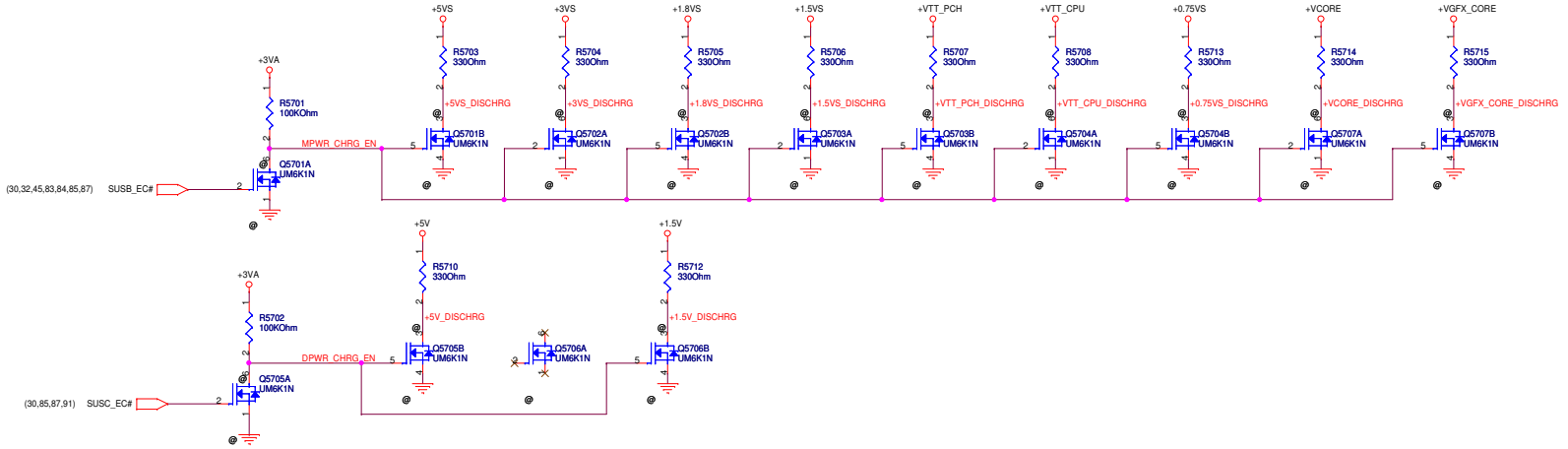
Date: Thursday, November 12, 2009 Sheet 55 of 96



Change LED part number

ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 56 of 96	

Remove +2.5Vs in for ACT_SEX



ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 57 of 96	

Title : PCI_****

ASUSTeK COMPUTER INC. NB4

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

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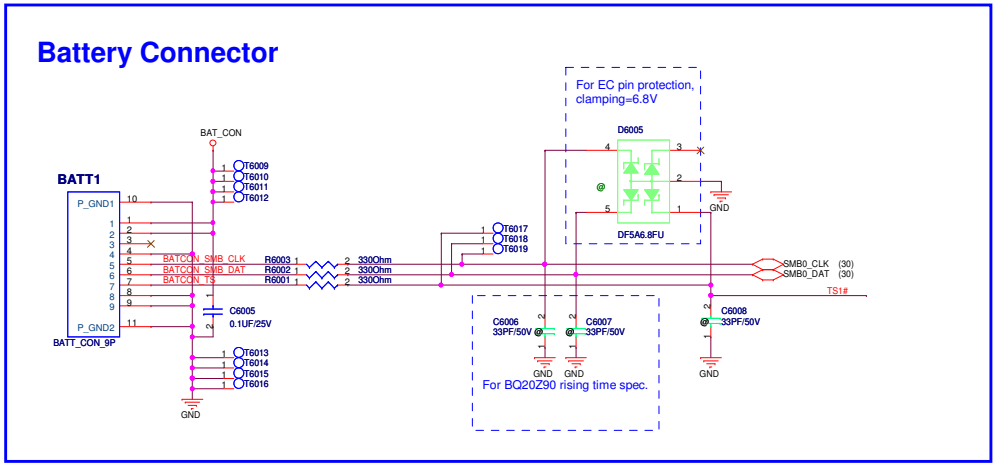
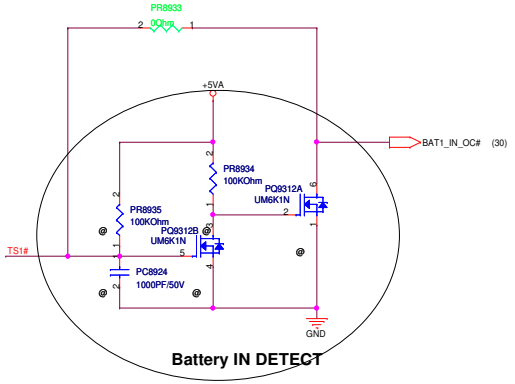
Main Board

ASUSTeK COMPUTER INC. NB4	Title : DJ_****	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 59 of 96	

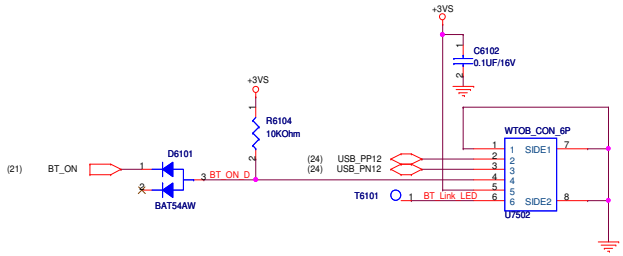
Battery Connector





ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 60 of 96	

BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 61 of 96		

Title : TPM_****

ASUSTeK COMPUTER INC. NB4

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

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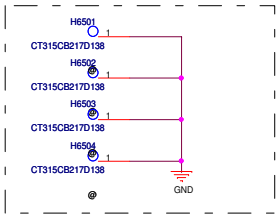
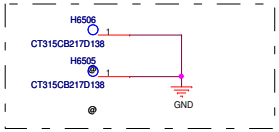
ASUSTeK COMPUTER INC. NB4	Title : FP_FP Conn		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 63 of 96		

ASUSTeK COMPUTER INC. NB4	Title : TUN_TV Tuner		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 64 of 96		

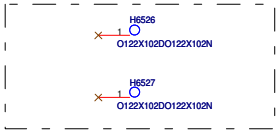
For CPU



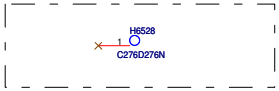
For GPU

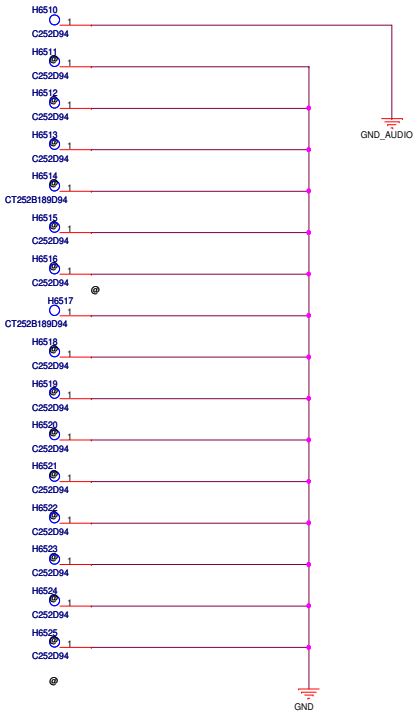


For 橢圓定位孔

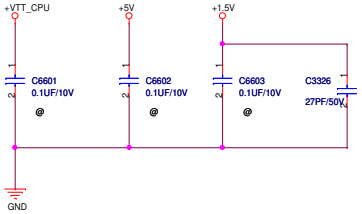


HHD 呼吸孔





ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 65 of 96	



ASUSTeK COMPUTER INC. NB4

Title : EMI

Engineer: CH_Lin

Size	Project Name	Rev
C	M60JV	1.01

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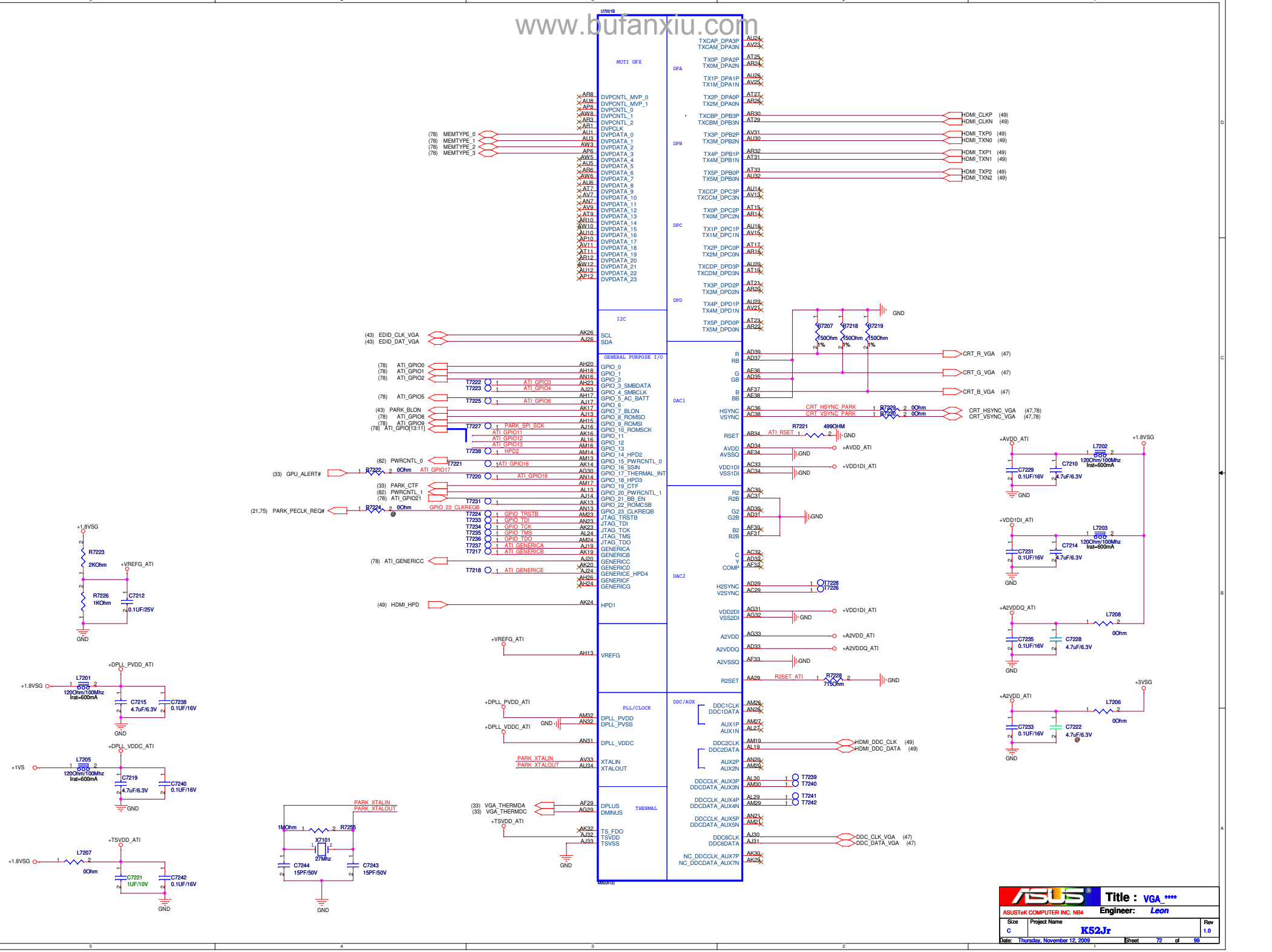
ASUSTeK COMPUTER INC. NB4	Title : PCH_XDP, ONFI		
	Engineer: Ed_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 67 of 96		

ASUSTeK COMPUTER INC. NB4		Title : OTH_LCM	
		Engineer: CH_Lin	
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009		Sheet 68 of 96	

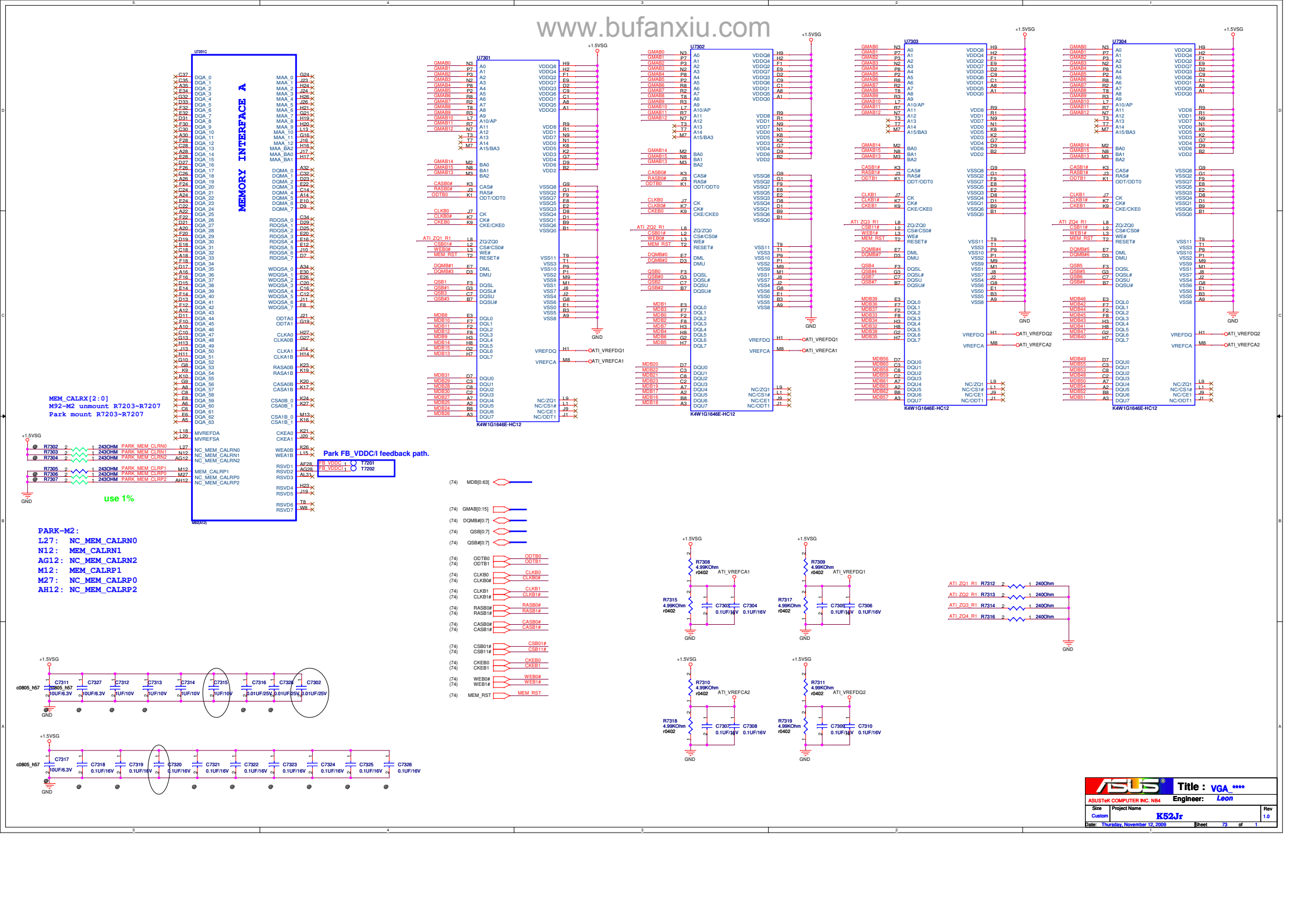
ASUSTeK COMPUTER INC. NB4	Title : OTH_GAME-LED*****		
	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 69 of 96		

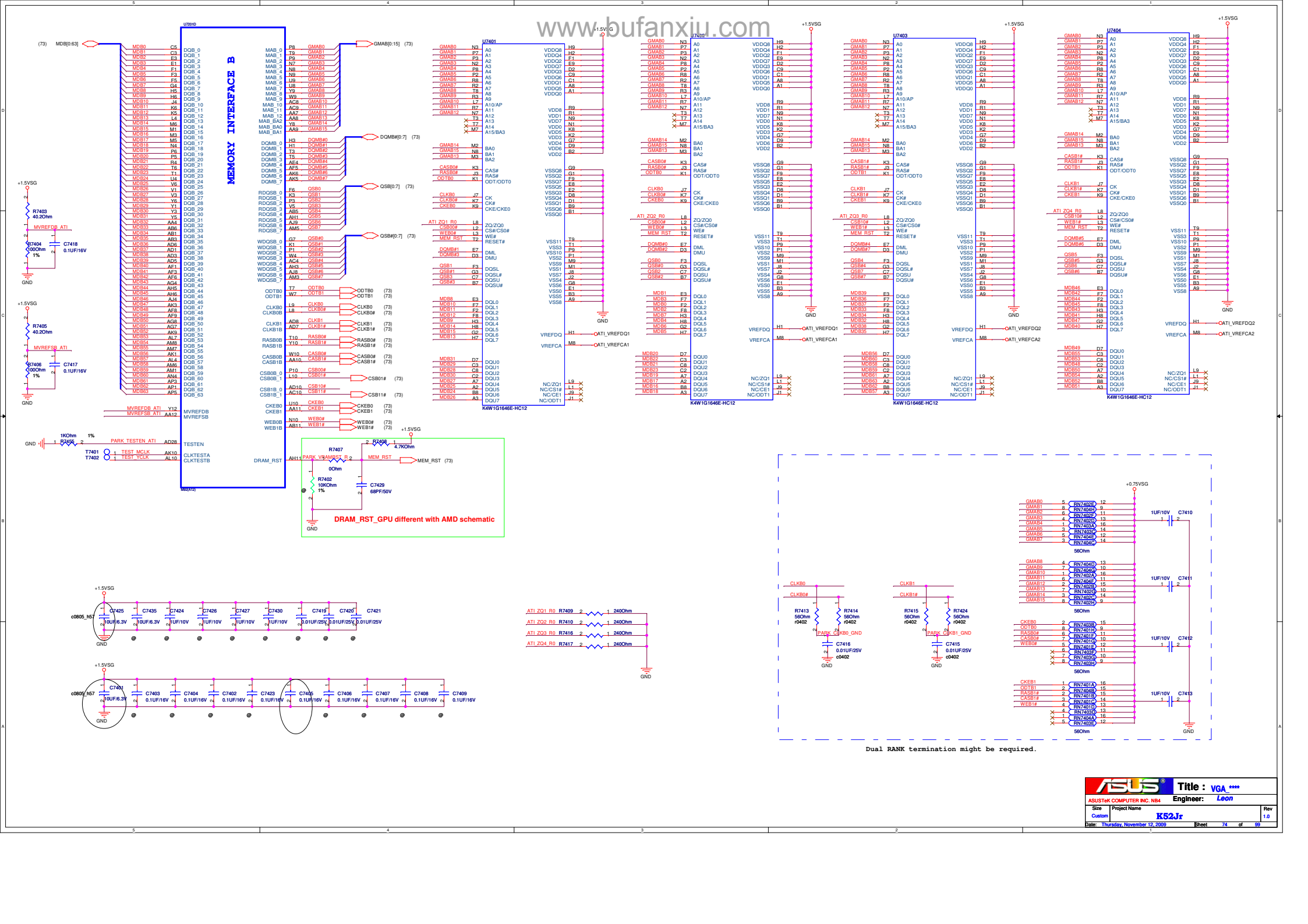
ASUSTeK COMPUTER INC. NB4		Title :	
		Engineer:	
Size: Custom	Project Name: M60JV		Rev: 1.01
Date: Thursday, November 12, 2009		Sheet 70 of 96	

ASUSTeK COMPUTER INC. NB4	Title :	
	Engineer:	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 71 of 96	



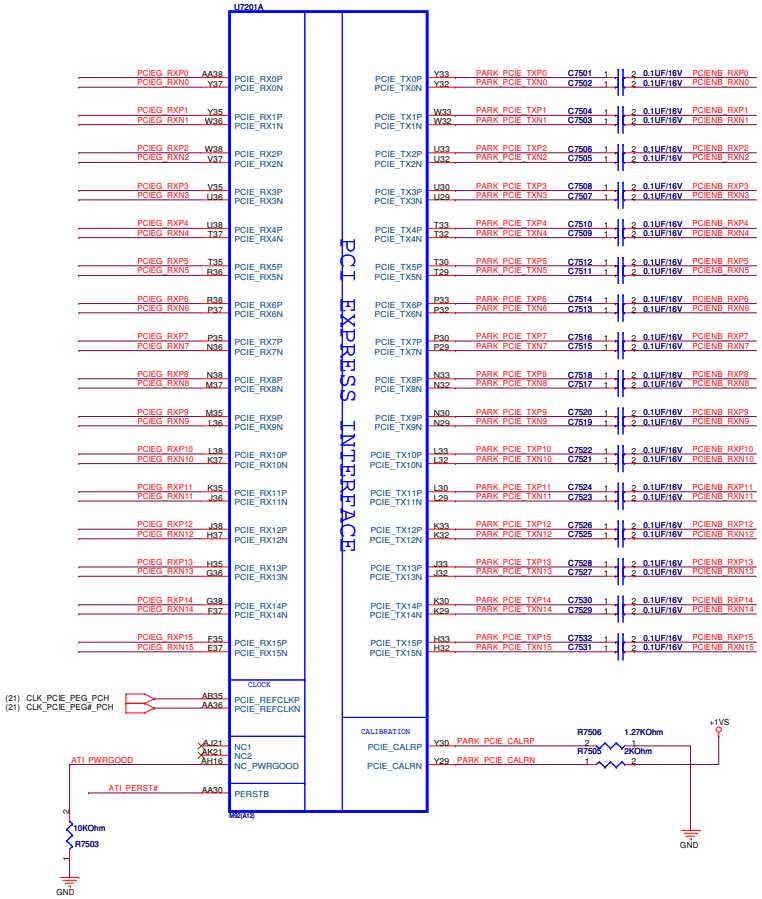
Title : VGA_****			
ASUSTeK COMPUTER INC. NB4	Engineer: Leon		
Size: C	Project Name: K52Jr	Rev: 1.0	
Date: Thursday, November 12, 2009	Sheet 72 of 99		

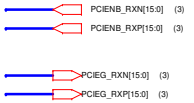


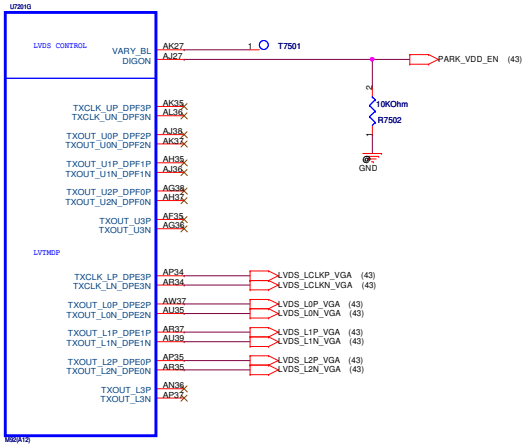


ASUSTeK COMPUTER INC. NB4	Title : VGA ****		
	Engineer: Leon		
Size: Custom	Project Name: K52Jr		Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 74 of 99		

PCI EXPRESS

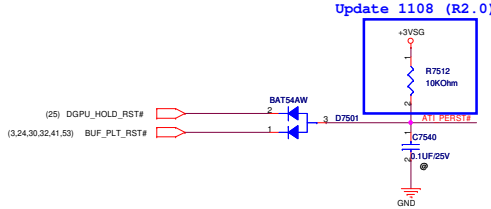




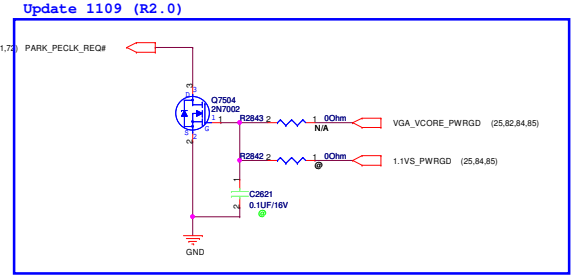


For switchable graphic

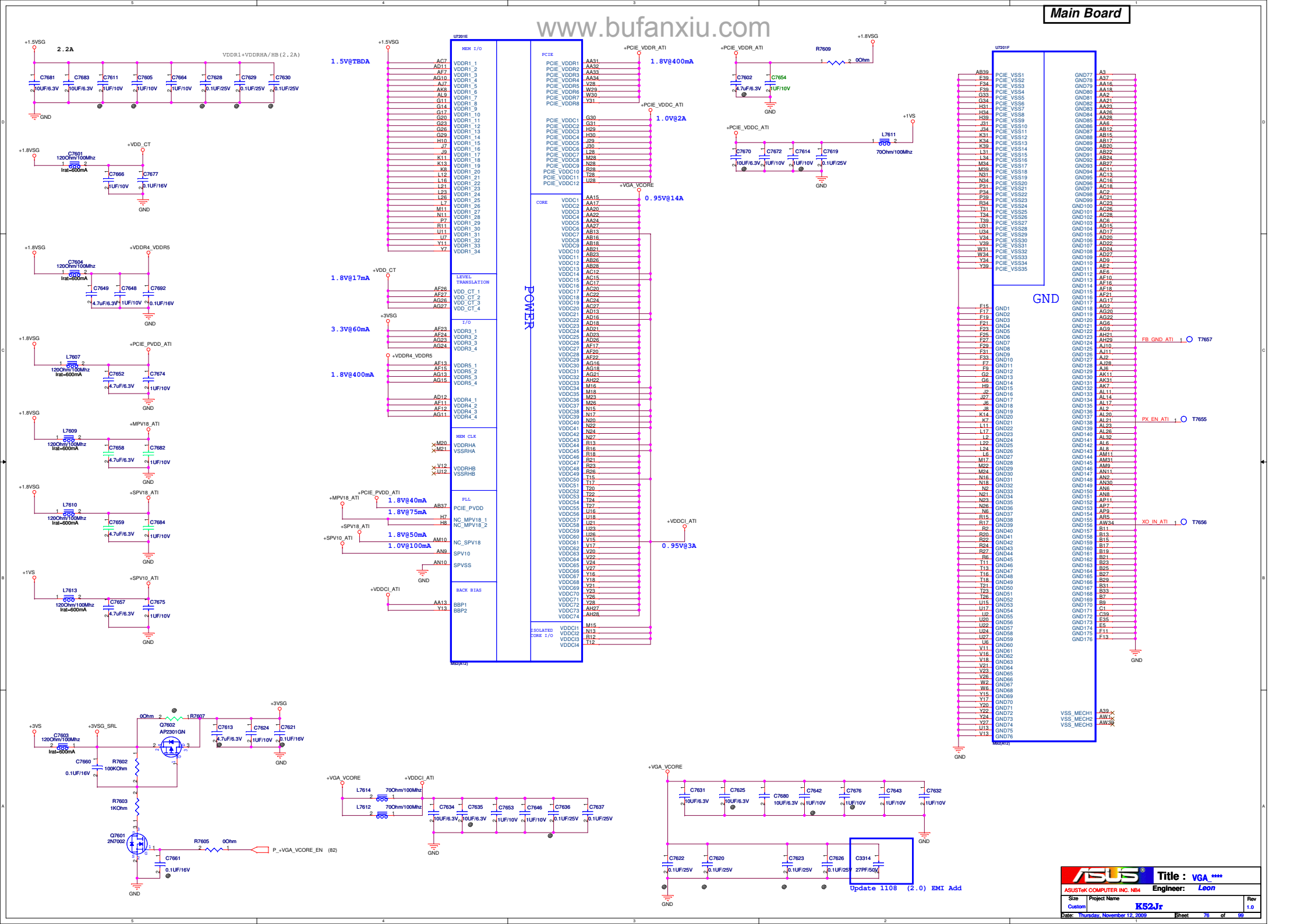
Update 1108 (R2.0)



Update 1109 (R2.0)

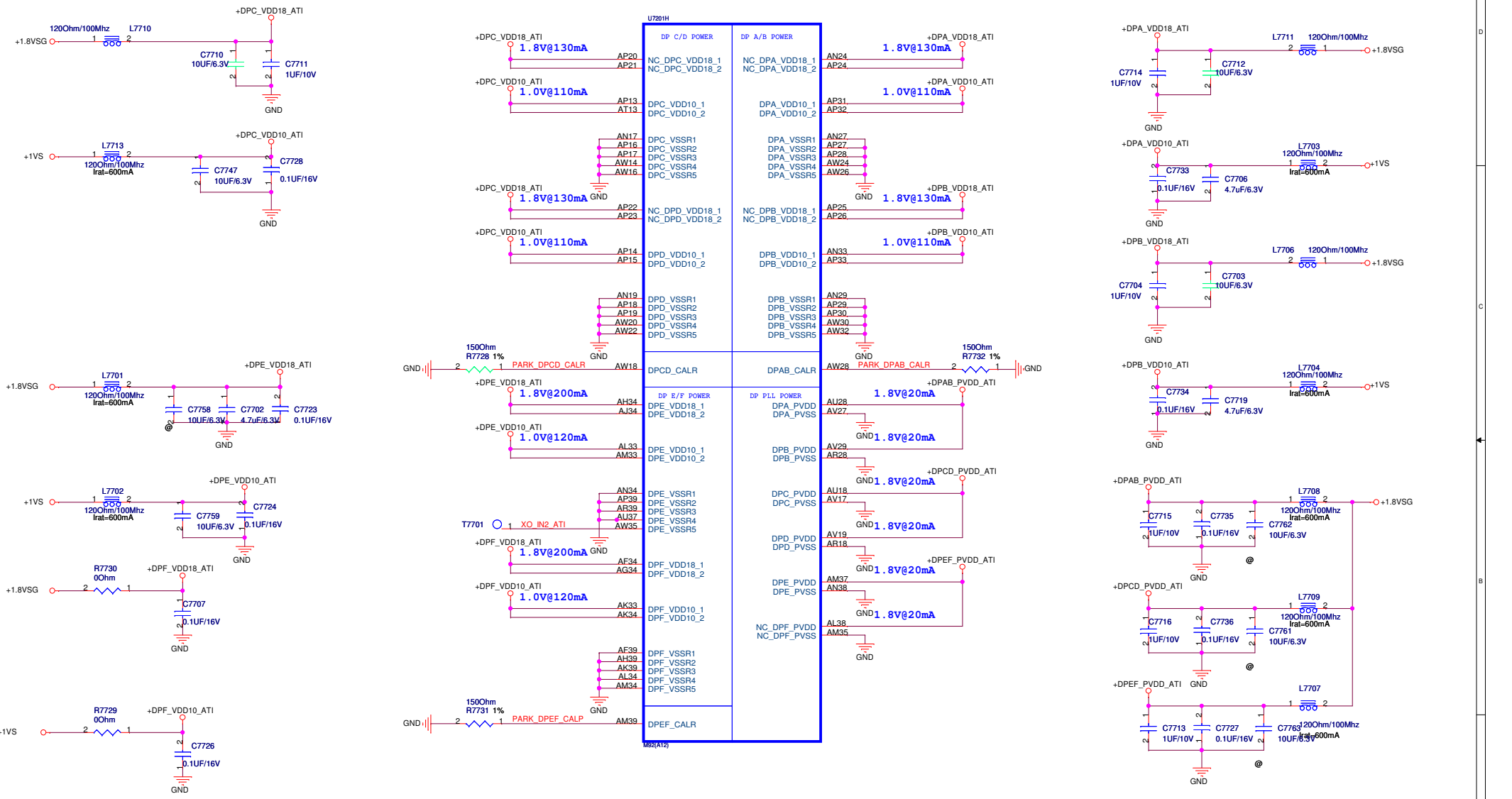


ASUSTeK COMPUTER INC. NB4	Title : VGA ****	
	Engineer: Leon	
Size: A2	Project Name: K52Jr	Rev: 1.0
Date: Friday, November 13, 2009	Sheet 75 of 99	

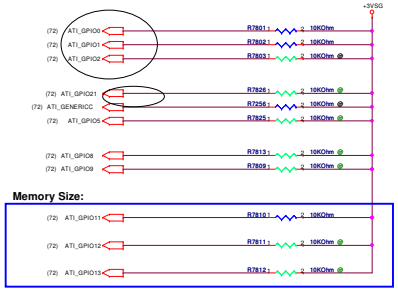


Title :	VGA ****
ASUSTeK COMPUTER INC. NB4	Engineer: Leon
Size: Custom	Project Name: K52Jr
Rev: 1.0	
Date: Thursday, November 12, 2009	Sheet 76 of 99

DPE: LVDS
DPB: HDMI
DAC1: CRT

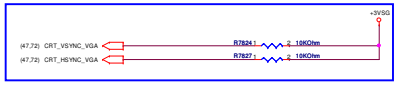


ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: Leon	
Size: Custom	Project Name: K52Jr	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 77 of 99	

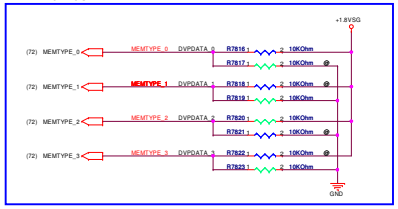


Memory Size:

Audio function:



Memory Type:



Dual Rank DDR3 1GB need AMD check pull low or high for following DDR3 VRAM
03G151638020 DDR3 64M*16-1.2 FBGA-96 SAMSUNG/K4W1G1646E-HC12
03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	0	32M*16 (256M)	A channel(M92-S2), B channel(M96-M2)
	0001	1	32M*16 (512M)	2-AB channel
	0010	2	64M*16 (512M)	A channel(M92-S2), B channel(M96-M2)
	0011	3	64M*16 (1G)	2-AB channel
Samsung	0100	4	64M*16 (512M)	A channel(M92-S2), B channel(M96-M2)
	0101	5	64M*16 (1G)	2-AB channel
	0110	6	32M*16 (256M)	A channel(M92-S2), B channel(M96-M2)
	0111	7	32M*16 (512M)	2-AB channel
Hynix	1000	8	32M*16 (256M)	A channel(M92-S2), B channel(M96-M2)
	1001	9	32M*16 (512M)	2-AB channel
	1010	10	64M*16 (512M)	A channel(M92-S2), B channel(M96-M2)
	1011	11	64M*16 (1G)	2-AB channel
	1100	12		
	1101	13	TBD	TBD
	1110	14		
Elpida	1111	15	64M*16 (1G)	2-AB channel

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Qimonda	0000	0	32M*16 (256M)	B channel
	0001	1	32M*16 (512M)	B channel dual-link
	0010	2	64M*16 (512M)	B channel
	0011 M92-M2	3	64M*16 (1G)	B channel dual-link
Samsung	0100	4	64M*16 (512MB)	B channel
	0101 M92-M2	5	64M*16 (1G)	B channel dual-link
	0110	6	32M*16 (256MB)	B channel M92-M2 only support B channel
	0111	7	32M*16 (512MB)	B channel dual-link
Hynix	1000	8	32M*16 (256M)	B channel
	1001	9	32M*16 (512M)	B channel dual-link
	1010	10	64M*16 (512M)	B channel
	1011 M92-M2	11	64M*16 (1G)	B channel dual-link
	1100	12		
	1101	13	TBD	
	1110	14		
Elpida	1111	15	64M*16 (1G)	B channel dual-link

TX_PWRS_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing. Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.) 1: Full Tx output swing.	0 (Internal pull-down)	0 (If the PCIe bus design meets the "Low Loss Interconnect" requirements) Otherwise: 1 Must be pulled to 3.3 V at reset using ~3-K (5%) resistor
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled. Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.) 1: Tx de-emphasis enabled.	0 (Internal pull-down)	0 (if the PCIe bus design meets the "Low Loss Interconnect" requirements. e.g. motherboard implementations.) Otherwise: 1 Must be pulled to 3.3 V at reset using ~3-K (5%) resistor (e.g. MXM and add-in boards).
BIF_GEN2_EN_A	GPIO_2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on. Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CBB (compliance base board).	0 (Internal pull-down)	0 5.0 GT/s capability will be controlled by software.
VGA_DIS	GPIO_9_ROMSI	VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO_13 GPIO_12 GPIO_11	a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. See *"ROM Configurations" on page 3-33* b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. See *"Primary Memory Aperture size requested at PCI Configuration" on page 3-33*	0 (Internal pull-down)	Design dependent. See description for more information.

POWERPLAY Interface

Pin Name	Type	PD/PU	Description
GPIO_5_AC_BATT	I/O	PD-reset	GPIO_5_AC_BATT is an **optional** input which allows the system to request a fast power reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods only in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_16_SSIN GPIO_20_PWRCNTL_1	I/O 3.3 V VDDR3	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At Reset, these signals will be inputs with weak internal pull-down resistors. VBIOS can define all voltage control signals to be either 3.3-V or open drain outputs (all signals must be the same type). The output state (high/low) of these signals is programmable for each PowerPlay state.
GPIO_21_BB_EN	I/O		(Optional) Voltage control signal for memory voltage regulator. Note that this signal must be low (0 V) at reset (failure to do so will prevent booting).

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	X
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC	GPIO2	GPIO21

BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device Note that when an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	0 (Internal pull-down)	Design dependent. See description for more information.
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	0 (Internal pull-down)	Design dependent. See description for more information.
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it should try to sense whether or not a VIP device is connected on the VIP Host interface. 0 - Driver would ignore the value sampled on VHAD_0 during reset 1 - Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no). According to the VIP 1.1 standard, VHAD_0 is tied high, and VIP slave devices are required to drive this signal low during reset. This scheme allows for a VIP device to be connected to the graphics adapter via a daughter card. Note: If the strap is needed, it must be placed between the ball and the VSYNC output buffer. This output buffer prevents monitors from affecting the value at reset.	0 (Internal pull-down)	Design dependent. See description for more information.

RESERVED CONFIGURATION STRAPS

Allow for pull-up pads for these straps and if these GPIOs are used, they must not conflict during reset

RESERVED	H2SYNC	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (Internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).

Pull-up pads are not required for these straps but if these GPIOs are used, they must not conflict during reset.

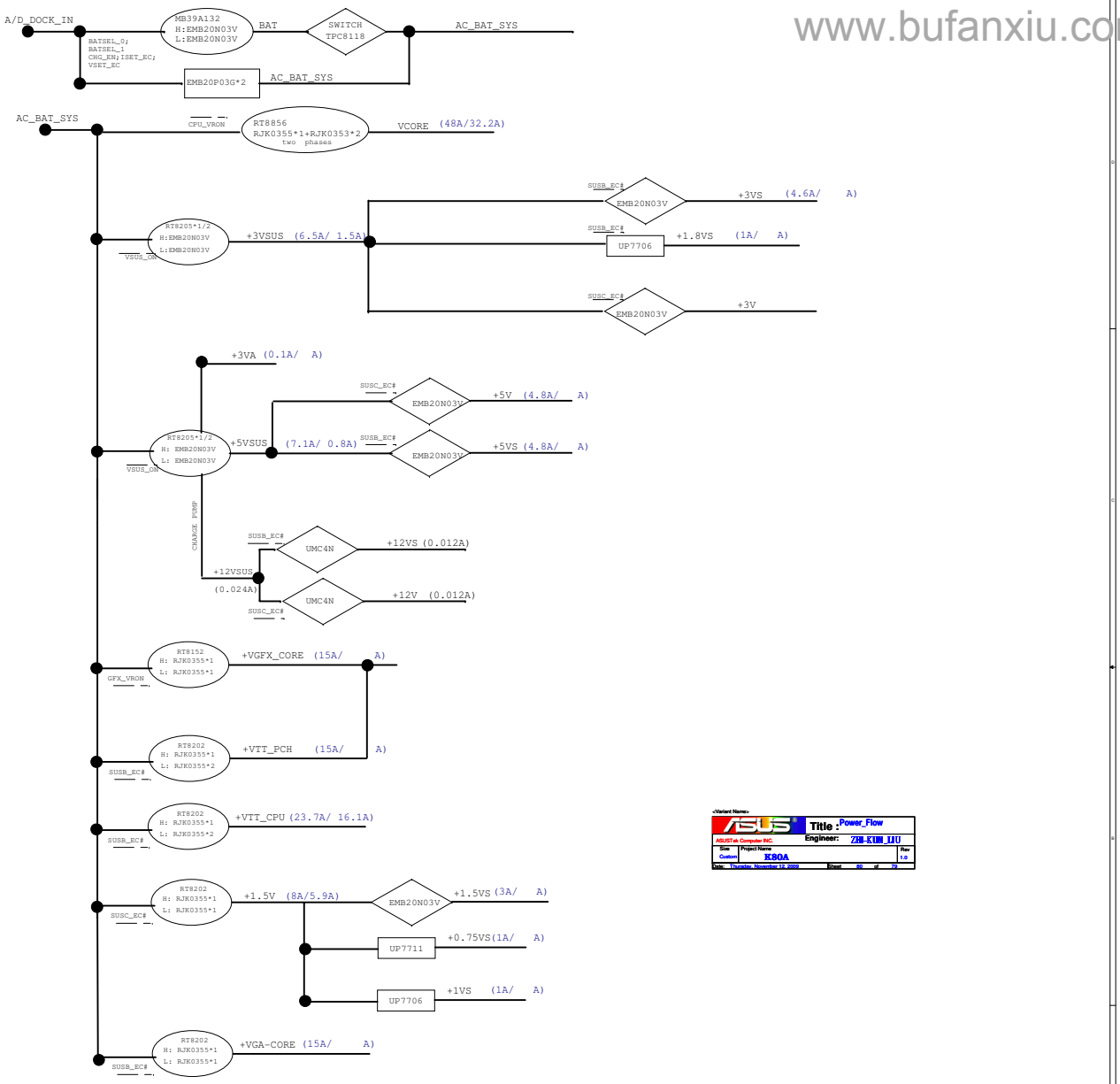
RESERVED	GPIO_8_ROMSO GPIO_21_BB_EN	Internal use only. THESE PADS HAVE INTERNAL PULL-DOWNS AND MUST BE 0 V AT RESET. These pads may be left unconnected, however, if they are connected to additional logic on the board, the logic must not allow these signals to be driven or pulled to any value except GND at reset.	0 (Internal pulldown)	No PAD required. Ensure that no logic conflicts with these signals during Reset.

64 MB	010
32 MB	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

ASUSTeK COMPUTER INC. NB4

Title : VGA_M96_STRAP
Engineer: Leon
Size: D | Project Name: K52Jr | Rev: 1.0
Date: Thursday, November 12, 2009 | Sheet 76 of 99

Title :	VGA_M96_STRAP
ASUSTeK COMPUTER INC. NB4	Engineer: Leon
Size: A3	Project Name: K52Jr
Rev: 1.0	
Date: Thursday, November 12, 2009	Sheet 79 of 99



<Variant Name>

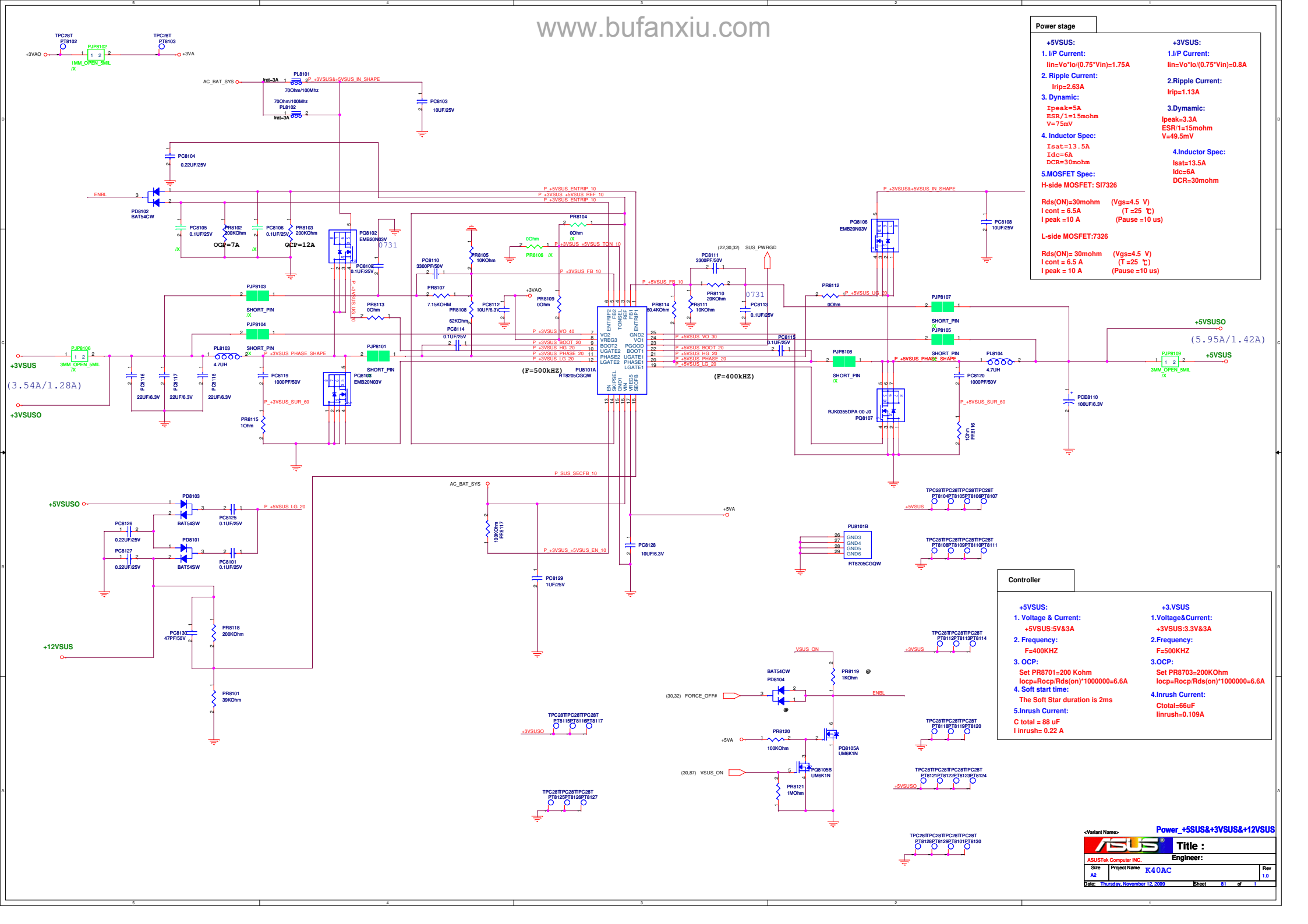
Title : Power_Flow

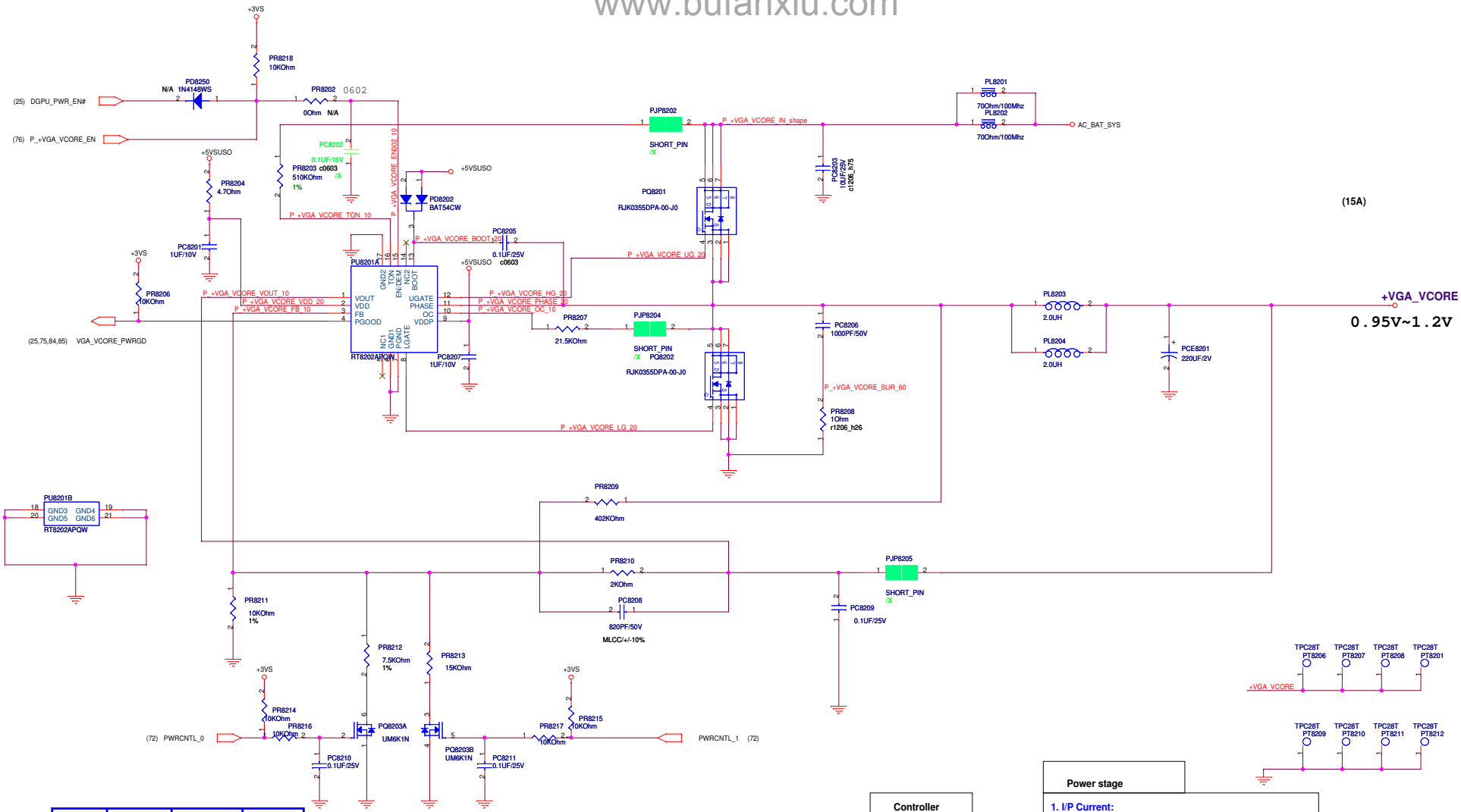
ASUSTeK Computer INC.

Engineer: ZHI-KUN_LIU

Size: Custom | Project Name: K80A | Rev: 1.0

Date: Thursday, November 12, 2009 | Sheet 60 of 79





PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	0.9	-5%
0	1	1.0	Normal
1	0	1.1	+5%
1	1	1.2	+10%

Controller

1. Voltage & Current:

   +1.2VSUS: 16A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

Set PR8107=21.5kohm
Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5.Inrush Current:

   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:

   Iripple=3.74A

3.ripple voltage:

   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV

4. Inductor Spec: 3. OCP:

   Isat=25A
   Idc=15.5A
   DCR=5.5mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

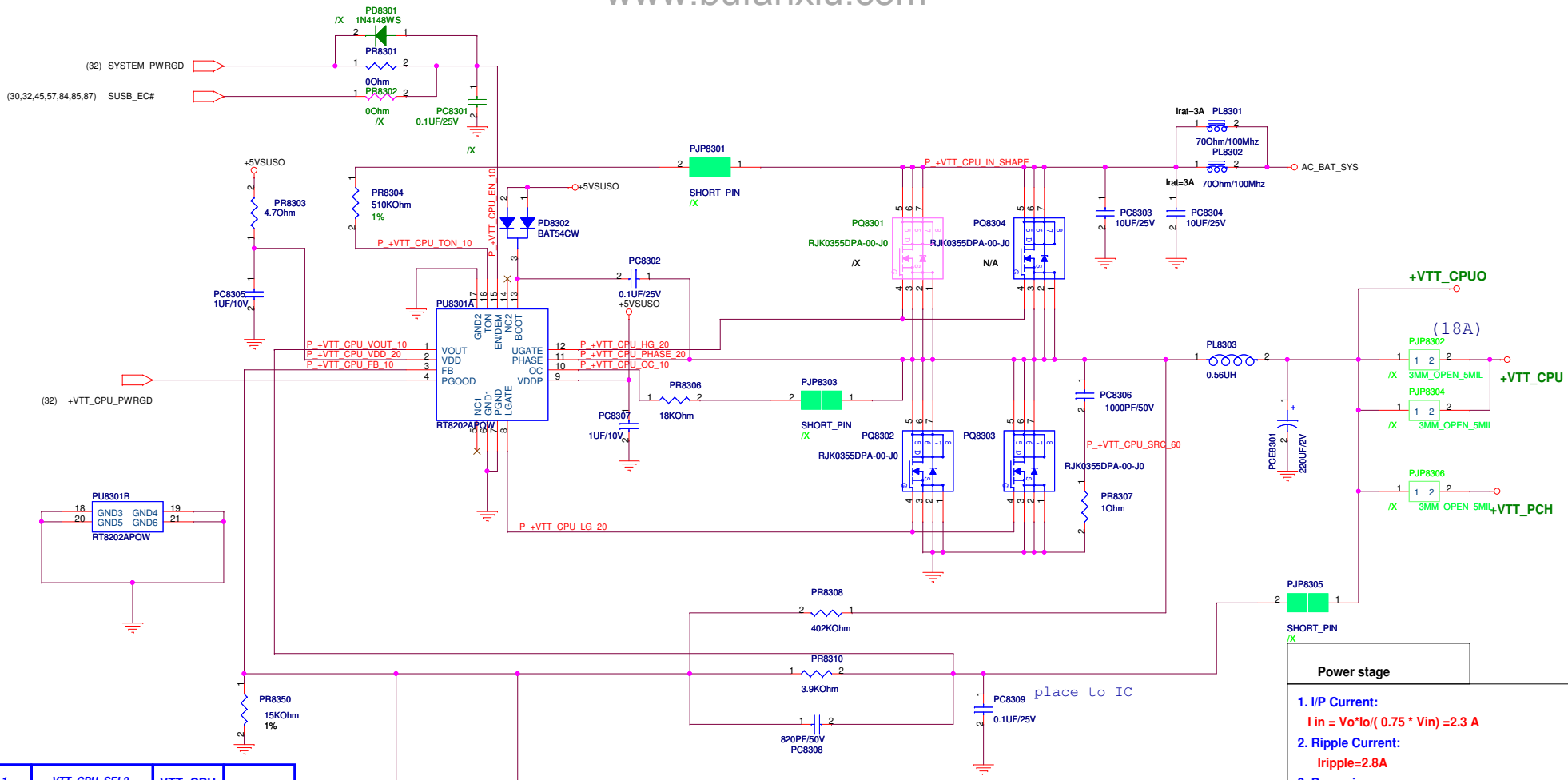
ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Thursday, November 12, 2009 Sheet 82 of 1



VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

Controller

1. Voltage & Current:

   +VCCP:1.05V@10A

2. Frequency:

   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   Set PR7343=18KOhm
   Iocp=Rocp*20/Rds(on)=22A

4. Soft start time:

   Soft-Star duration is 1.35ms

5. Inrush Current:

   C total = 200 uF
   I inrush= 0.16 A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =2.3 A

2. Ripple Current:

   Iripple=2.8A

3. Dynamic:

   Ipeak=1.98A
   DCR=3.3mohm
   V=6.534mV

4. Inductor Spec:

   Isat=16A
   Idc=11A
   DCR=9mOhm

5. MOSFET Spec:

   H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

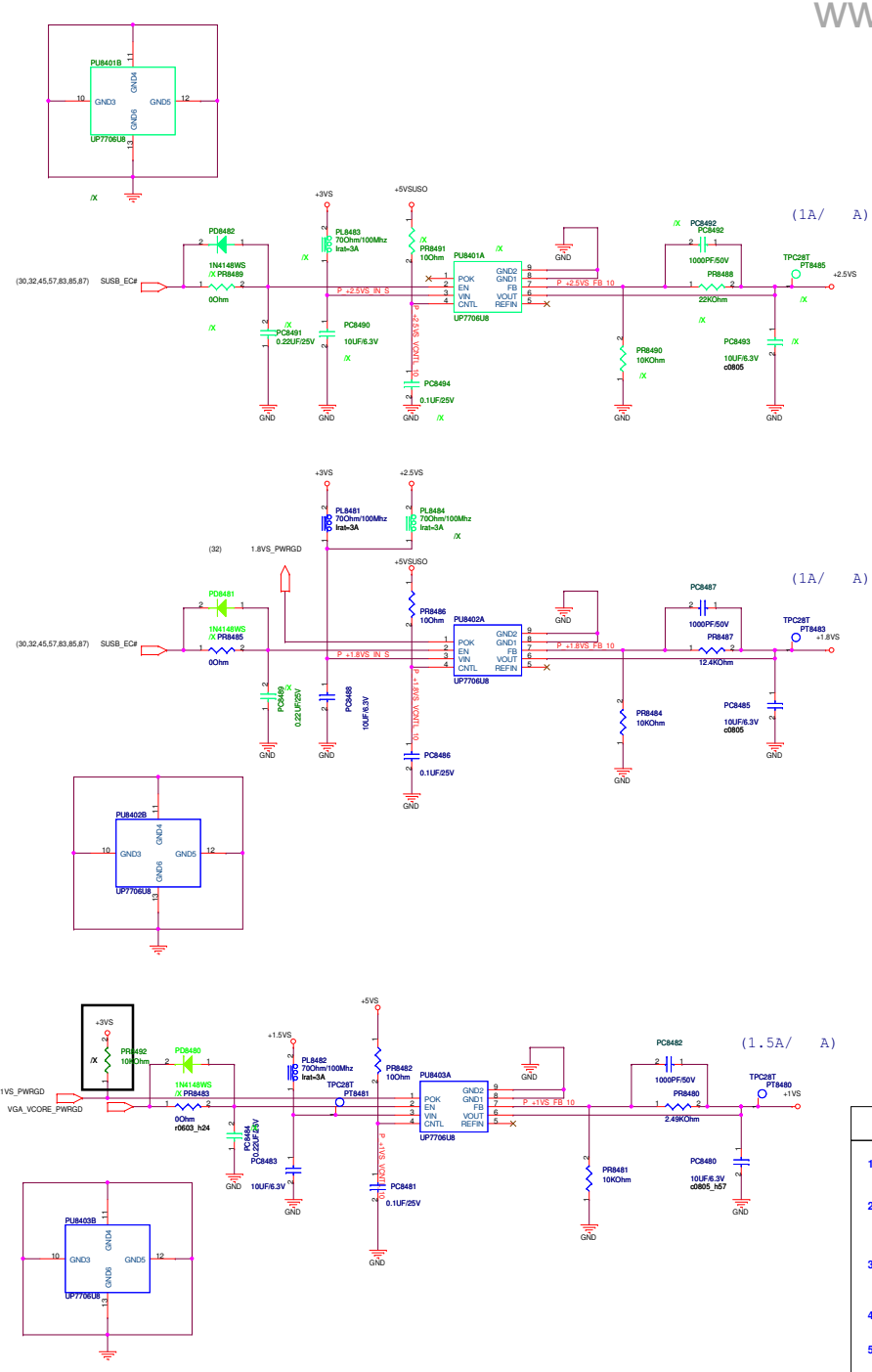
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009 Sheet 83 of 1



Controller

1. Voltage & Current:
   +1.8V:+1.8V&12A
2. Frequency:
   Ton=3.85p*Rt(on)*Vo/Vin-05
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR7343=18kohm
   Iocp=Rocp*20/Rds(on)
   =20*1.5/16.5=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =100uF
   I
   inrush=0.133A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.947A
2. Ripple Current:
   Iripple=2.342A
3. Ripple Voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=3.25A
   DCR=3.3mohm
   V=10.75mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

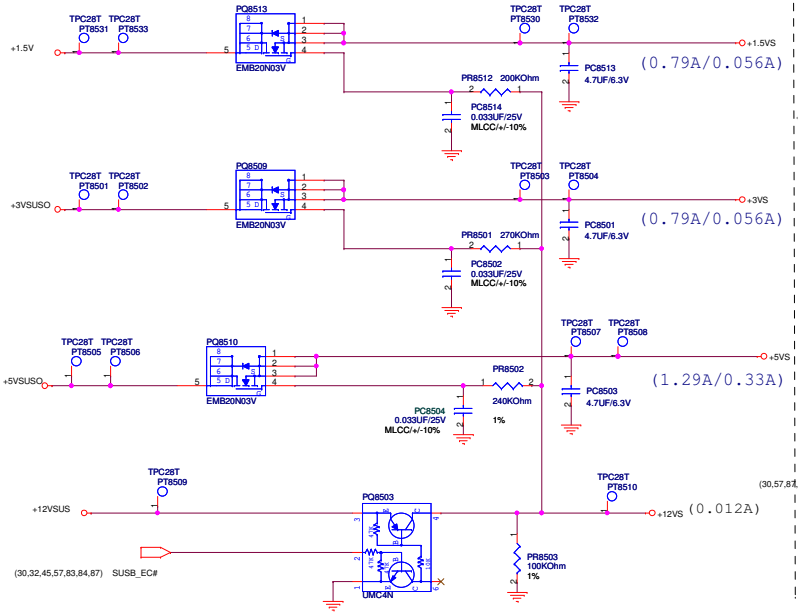
Title : Power_+1.8V&+0.9V

Engineer:

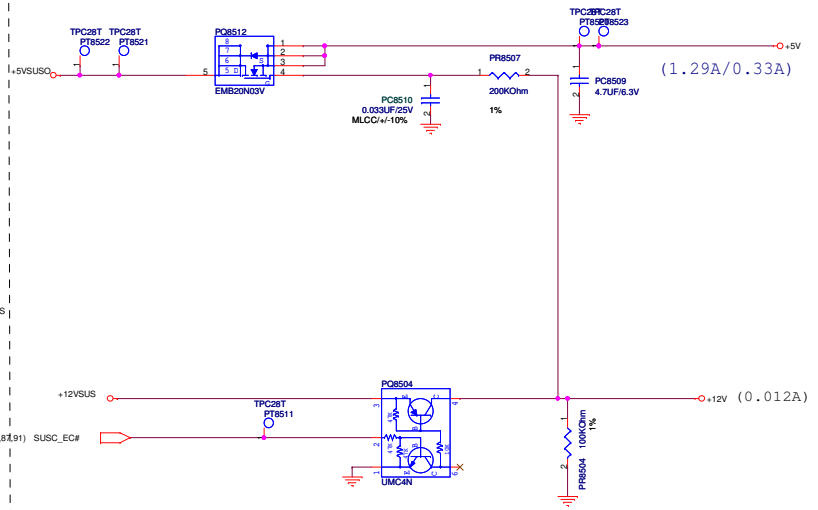
Size	Project Name	Rev
Custom		1.0

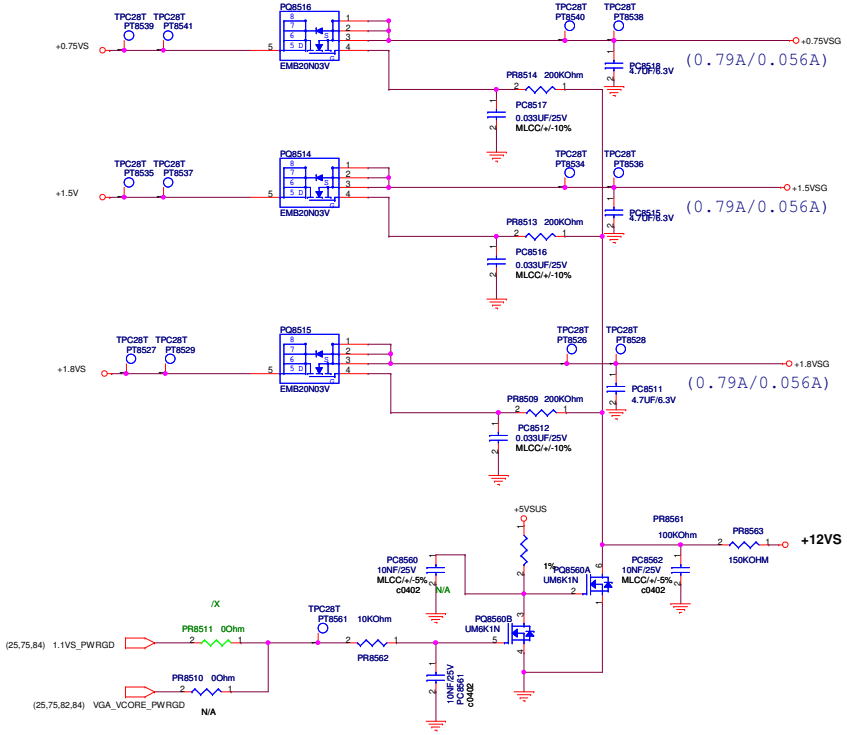
Date: Thursday, November 12, 2009 Sheet 84 of 1

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_Load_Switch

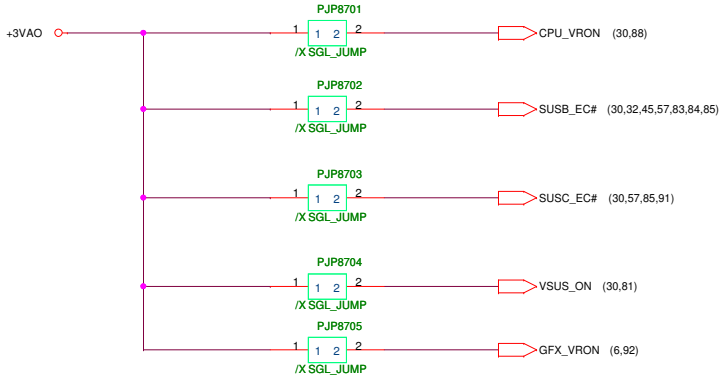
Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009 Sheet 85 of 1

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_good_detecter
	Engineer:
Size: Custom	Project Name
Rev: 1.0	
Date: Thursday, November 12, 2009	Sheet 86 of 1



<Variant Name>

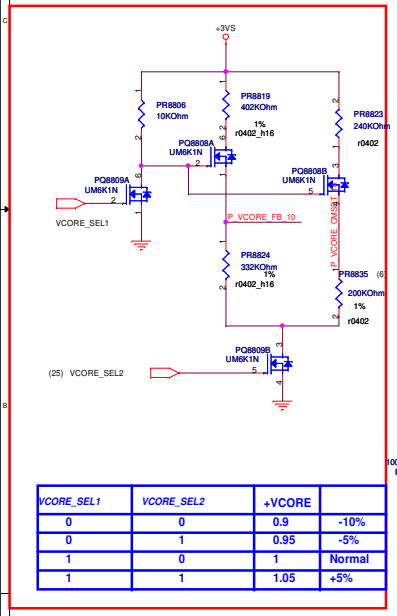
ASUSTeK COMPUTER INC

Title : Power_for_test

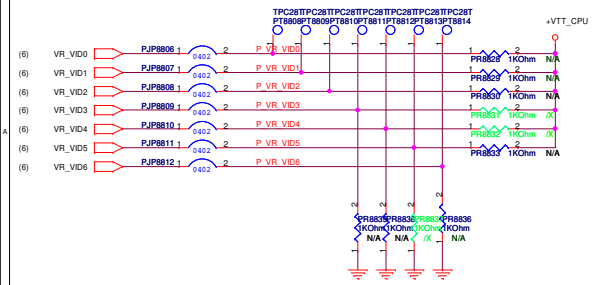
Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, November 12, 2009 Sheet 87 of 1



VCORE_SEL1	VCORE_SEL2	+VCORE	
0	0	0.9	-10%
0	1	0.95	-5%
1	0	1	Normal
1	1	1.05	+5%



CPU SKU, $I_{CC\_CORE-MAX}$ Maximum CPU Core Current	I_{MAX} (IMON=900 mV min) [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
$I_{CC\_CORE-MAX}$ ≤20 A	20	001	45.0
20A< $I_{CC\_CORE-MAX}$ ≤30 A	30	010	30.0
30A< $I_{CC\_CORE-MAX}$ ≤40 A	40	011	22.5
40A< $I_{CC\_CORE-MAX}$ ≤50 A	50	100	18.0
50A< $I_{CC\_CORE-MAX}$ ≤60 A	60	101	15.0
60A< $I_{CC\_CORE-MAX}$ ≤70 A	70	110	12.9
70A< $I_{CC\_CORE-MAX}$ ≤90 A	90	111	10.0

1. VID[2:0] "Reserved " - default VID[2:0]='111' - option to change default should be provided on the motherboard.
2. VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
3. VID[6] "Reserved" - default VID [6]='0' - option to change default should be provided on the motherboard.
4. DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR='1' for IMVP-6.5-compliant controller.
5. PSI# - "Reserved" - default PSI#='0' - option to change default should be provided on the motherboard.

Power stage

1. I/P Current:
   I in = Vo*Io/(0.85 * Vin) =2.93 A
2. Ripple Current:
   Iripple=7.04A Vrip=15.85mV
3. Dynamic:
   Ipeak=45A
   ESR=2.25mohm
   V=91.1mV
4. Inductor Spec:
   Idc=38.8A
   Itemp=32.5A
   DCR=1.1mOhm
5. MOSFET Spec:
   H-side MOSFET: RJK0355
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)
   L-side MOSFET: RJK0353
   Rds(on)=7.6mOhm (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)
6. CPU MLCC: 16*10uF

Controller

1. Voltage & Current:
   Vcore:1.05V/45A
2. Frequency:
   CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
   Vocset=25*Ilim*Rsense
   Ilim=35.5*2=71A
4. Slew rate:
   Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5. Inrush Current:
   C total = 880 uF
   I inrush= 0.154 A
6. Droop Resistance:
   Rdroop=R1/R2*10*Rsense=2mohm

<Variant Name>

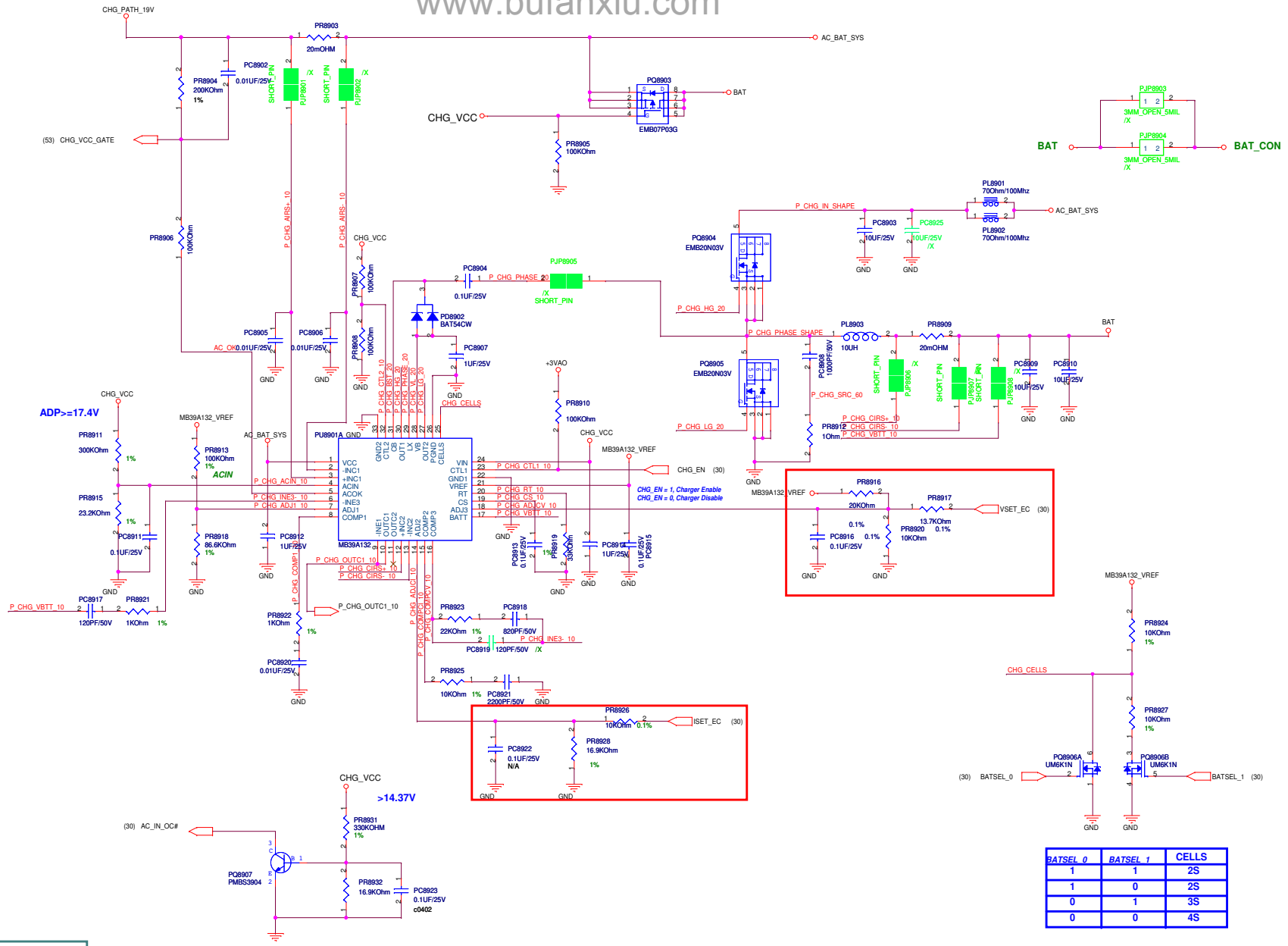
ASUSTeK Computer INC.

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
Custom	K82	1.0

Date: Thursday, November 12, 2009 Sheet 88 of 1



BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

1. Adapter Threshold: 17.41V

17.41=(PR9213+PR9216)/PR9216*1.25

2. AP4835 ID=-9.2A

3. MB39A132_VREF= 5.0V

4. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25/0.02=3.14A
330K--162K

90W: 100K--86.6K :Ilimit_current=4.49A

5. Charging Voltage

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

6. Charging current

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:

fosc(KHz) = 17000 / RT (KOhm)

fosc(KHz) = 17000/33K=515KHz

2. OCP:

Ioc=0.2/Rs = 10A

3. Soft start time:

ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms

4. Inrush current(3S):

Iinrush = C*V/t=9.7mA

Power stage

1. I/P Current(3S2P):

I in = Vo*Io/(0.75 * Vin) =2.21A

2. Ripple Current(3S2P):

Iripple=1.18A

3. Inductor Spec:

Isat=4.4A
Idc=3.8A
DCR=35mohm

4. MOSFET Spec:

Idc= 6.5A/5.0A
Rdcon=22/30mohm
Vgsth=0.8~1.8V

EC Code: 202

<Variant Name>

Title : Power_Charger

ASUSTek Computer INC.

Engineer: Limy_li

Size	Project Name	Rev
C		1.0

Date: Thursday, November 12, 2009 Sheet 89 of 1

<Variant Name>

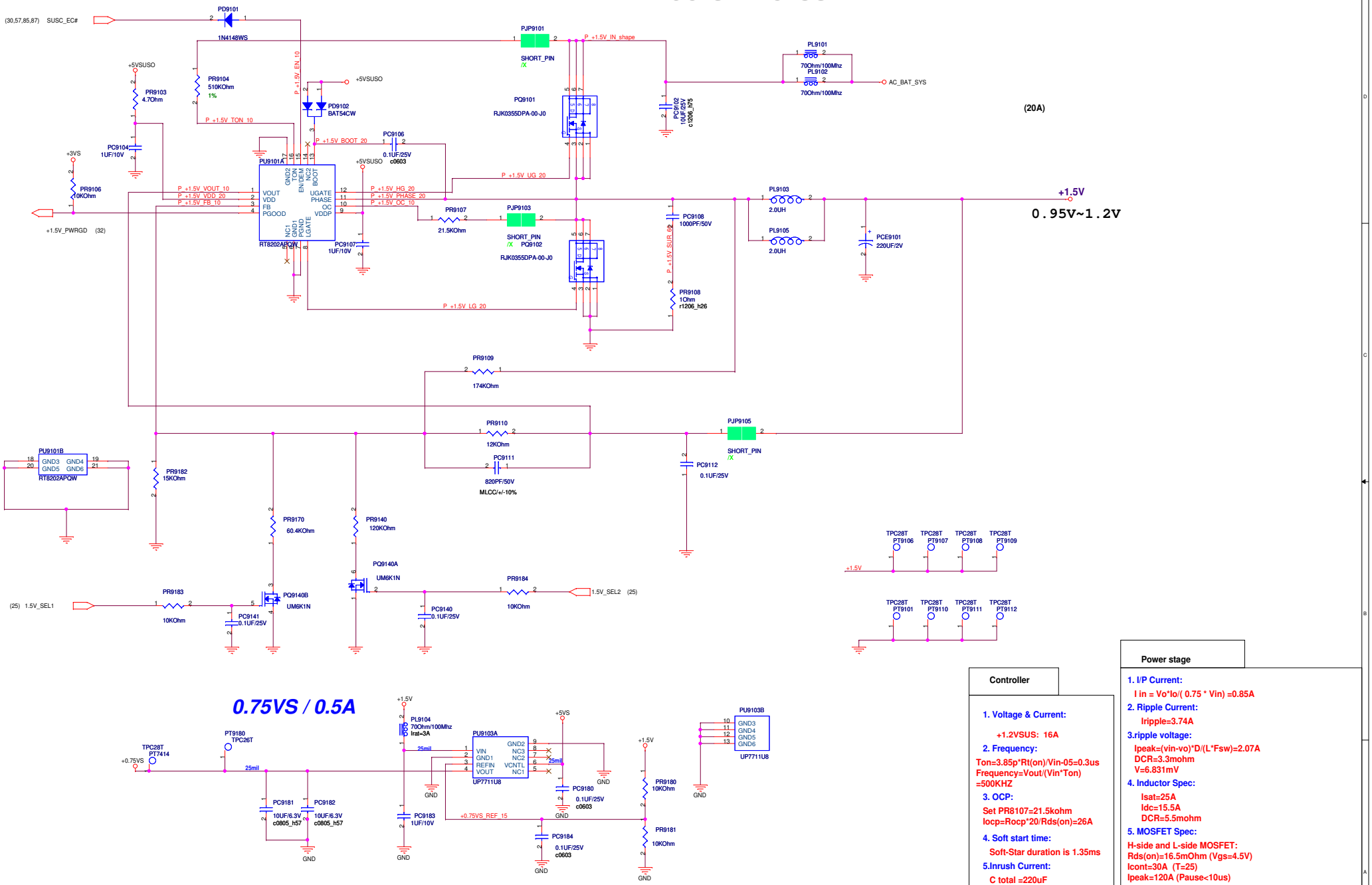
Title : Power_Charger

ASUSTek Computer INC.

Engineer: Limy_li

Size	Project Name	Rev
A3	F83T	2.1G

Date: Thursday, November 12, 2009 Sheet 90 of 1



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

Controller

1. Voltage & Current:

   +1.2VSUS: 16A

2. Frequency:

   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   Set PR8107=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5. Inrush Current:

   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:

   Iripple=3.74A

3. ripple voltage:

   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV

4. Inductor Spec:

   Isat=25A
   Idc=15.5A
   DCR=5.5mohm

5. MOSFET Spec:

   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : +1.5V

Engineer:

Size	Project Name	Rev
C	K80A	1.0

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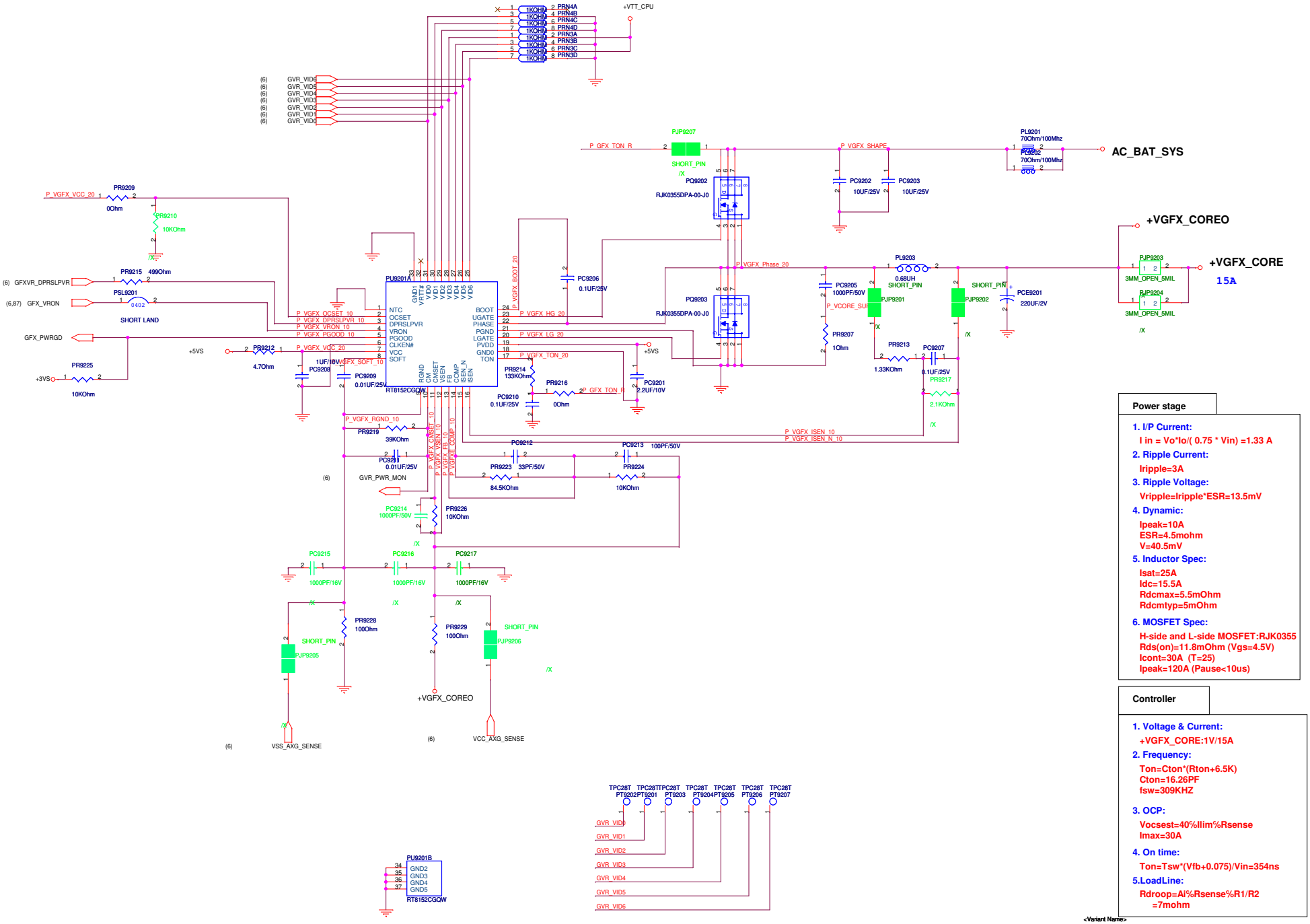


Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=10A
   ESR=4.5mohm
   V=40.5mV
5. Inductor Spec:
   Isat=25A
   Idc=15.5A
   Rdcmax=5.5mOhm
   Rdcmtyp=5mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

Controller

1. Voltage & Current:
   +VGFX_CORE:1V/15A
2. Frequency:
   Ton=Cton*(Rton+6.5K)
   Cton=16.26PF
   fsw=309KHZ
3. OCP:
   Vocsest=40%Ilim%Rsense
   Imax=30A
4. On time:
   Ton=Tsw*(Vfb+0.075)/Vin=354ns
5. LoadLine:
   Rdroop=Ai%Rsense%R1/R2
   =7mohm

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
C	UX21	1.0

Date: Thursday, November 12, 2009 Sheet 92 of 1

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_+VCCP	
	Engineer:	
Size: C	Project Name	Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 93 of 1	

<Variant Name>

Title : Power_+VCCP

ASUSTeK COMPUTER INC

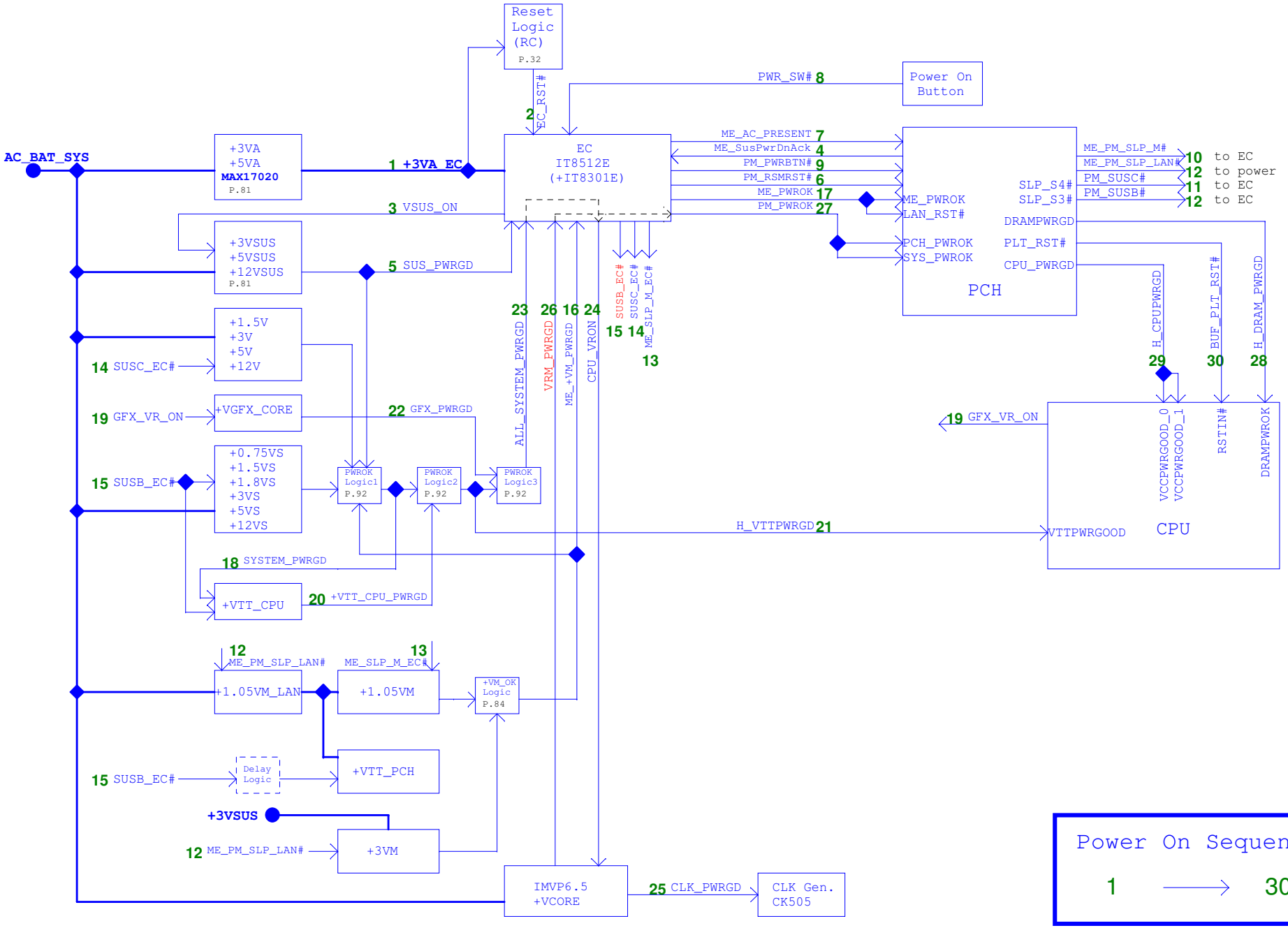
Engineer:

Size	Project Name	Rev
A3		1.0

Date: Thursday, November 12, 2009 Sheet 94 of 1

AC-IN Mode

M52J Power On Sequence Diagram Rev. 0.31



ASUSTeK COMPUTER INC	Title : POWER SEQUENCE	
	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 95 of 96	

M52J Power-On Sequence Timing Diagram Rev.0.31

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 ME_AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 ME_PM_SLP_M#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/ME_PM_SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) 13 ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 14 SUSC_EC#

+1.5V/+3V/+5V

(EC to power) 15 SUSB_EC#

+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS

(power to EC) 16 ME_+VM_PWRGD

(EC to PCH) 17 ME_PWROK

18 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) 19 GFX_VR_ON

20 +VTT_CPU_PWRGD/ 21 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

22 GFX_PWRGD

(power to EC)

23 ALL_SYSTEM_PWRGD

(EC to power) 24 CPU_VRON

+VCORE

25 CLK_PWRGD

(inversion of CLK_EN#)

(power to EC) 26 VRM_PWRGD

(EC to PCH) 27 PM_PWROK

(PCH to CPU) 28 H_DRAM_PWRGD

(PCH to CPU) 29 H_CPUPWRGD

(PCH to CPU) 30 BUF_PLT_RST#

(pull up to +3VSUS)

T0=20ms(spec.>=10ms)

T1<200ms(check)

(falling edge)

T2=50ms

T3=2ms(spec.>=1ms)

T4=1.25ms

T5=60us(typ.)

T6=110ms (spec.>=99ms)

T7=10~100us

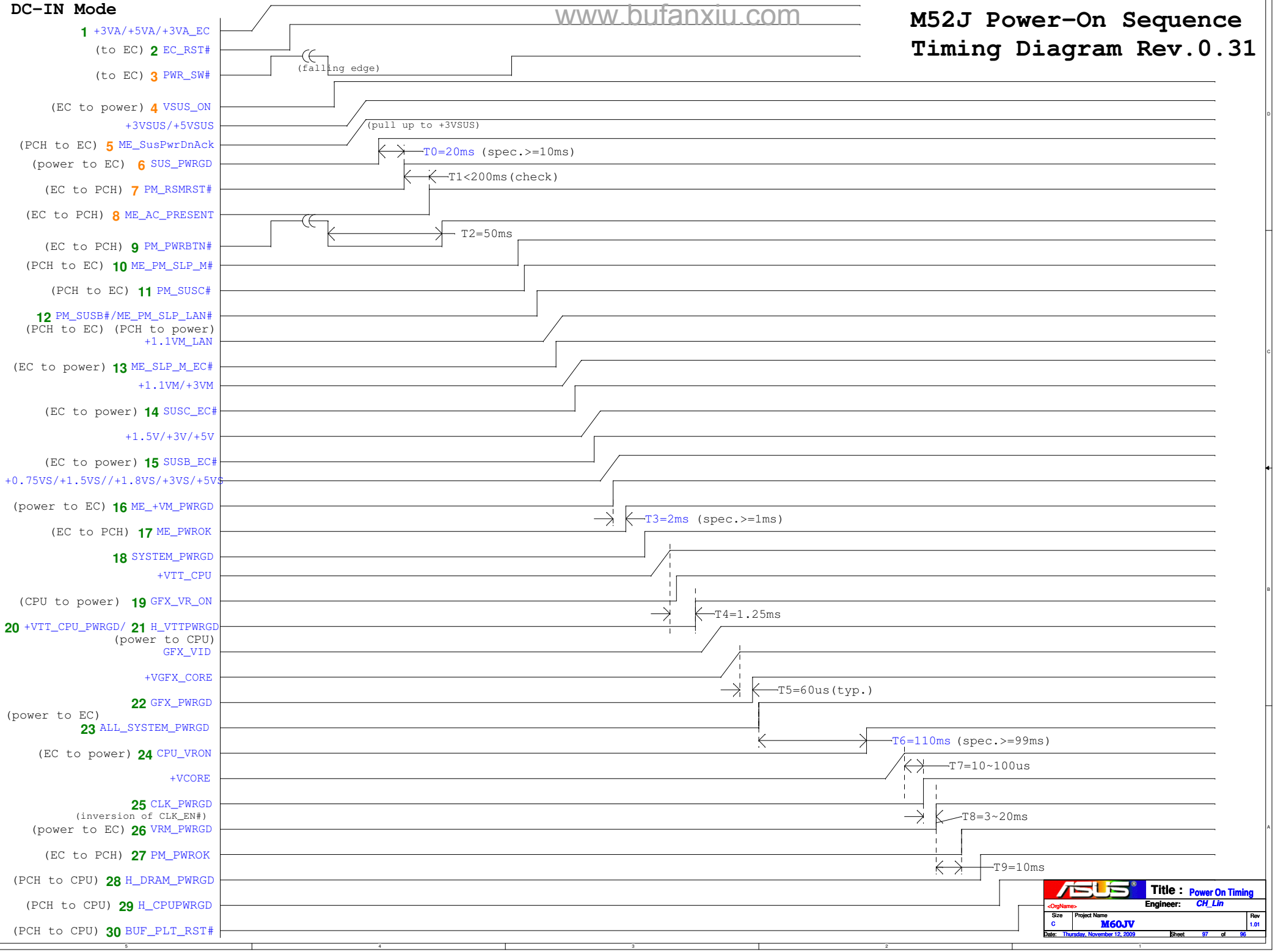
T8=3~20ms

T9=10ms

Title : Power On Timing		
<OrgName>	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 96 of 96	

M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode



Title :	Power On Timing
<OrgName>	Engineer: CH_Lin
Size: C	Project Name: M60JV
Rev: 1.01	
Date: Thursday, November 12, 2009	Sheet 97 of 96