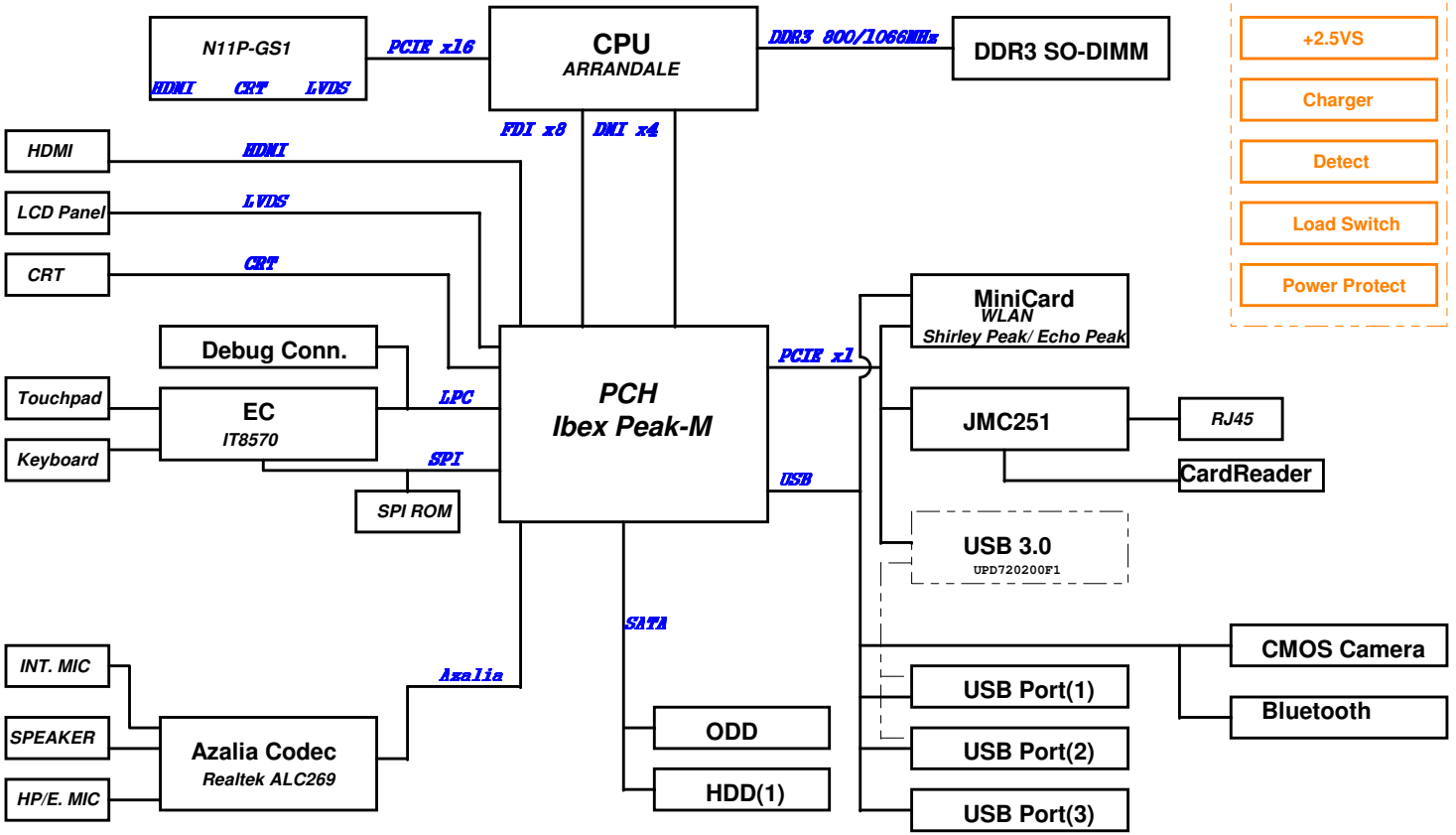
K42Jv SCHEMATIC Revision 2.0

SYSTEM PAGE REF.

BLOCK DIAGRAM



Power
- VCORE
- System
- 1.5VS & 1.05VS
- DDR & VTT
- +2.5VS
- Charger
- Detect
- Load Switch
- Power Protect

Clock Generator
ICS9LVS3162

VID controller | Discharge Circuit | DC & BATT. Conn.

PWM Fan | Reset Circuit | Skew Holes

ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.1

Date: Thursday, February 11, 2010 Sheet 1 of 96

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	-	INT TBD	+3VS
GPIO 07	GPI	USB30_SMIB	EXT PU	+3VS
GPIO 08	GPI	EC_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	OC5#	EXT PU	+3VSUS
GPIO 10	Native	OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EC_SCI#	EXT PU	+3VSUS
GPIO 12	Native	-	EXT PU	+3VSUS
GPIO 13	GPO	-		+3VSUS
GPIO 14	Native	OC7#	EXT PU	+3VSUS
GPIO 15	GPO	-	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWRGD_PCH	EXT PD	+3VS
GPIO 18	Native	CLK_REQ1#	EXT PU	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2_WLAN#_R	EXT PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_BT_LED	EXT PD	+3VS
GPIO 23	Native	LPC_DRQ#1		+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLK_REQ3#	EXT PU	+3VSUS
GPIO 26	Native	CLK_REQ4#(USB 3.0)	EXT PU	+3VSUS
GPIO 27	Native	PCH_VRM_EN	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON	-	+3VSUS
GPIO 29	GPO		-	+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	PCH_SPI_OV_RW	INT WEAK PU	+3VS
GPIO 34	Native	STP_PCI#	EXT PU	+3VS
GPIO 35	Native	SATACLKREQ#	EXT PD	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PD	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC2#	EXT PU	+3VSUS
GPIO 41	Native	OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	PECLK_REQ#	EXT PU	+3VSUS
GPIO 48	GPO	-	EXT PU	+3VS
GPIO 49	GPO	PCH_TEMP_EN	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#	EXT PU	+5VS
GPIO 53	GPO	PCI_GNT2#	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	Native	CLKREQ2_GLAN#_R	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC01#	EXT PU	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	EDID_SELECT#	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	PM_BATLOW#	EXT PU (Not used)	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU	+3VSUS

EC IT8570

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	KB_RST#
GPB7	O	PM_RSMRST#
GPC0	O	CLK_UC
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7		-
GPD0		-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EC_SCI#
GPD4	O	EC_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	I	HDMI_HPD
GPE0		-
GPE1		-
GPE2		-
GPE3		-
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0		-
GPF1	O	VSUS_ON
GPF2	O	VTT_DRAM_PWR_SEL1
GPF3	O	VTT_DRAM_PWR_SEL2
GPF4	IO	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	VGA_DEEPIDLE (TBD)
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5		-
GPH6	O	CAP_LED#
GPI0	I	GPU_ALERT#
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ENABLE
GPI5	I	CPU_VCORE_I_SEN
GPI6	I	DGPU_VCORE_I_SEN
GPI7		-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	V_DA_EC/VCORE_SEL1
GPJ5	O	VCORE_SEL2

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LVS3162)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A4)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
VGA Thermal IC(G781-1)	1001101x (9A)	

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	
USB 4	
USB 5	
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	

ASUSTeK COMPUTER INC. NB4

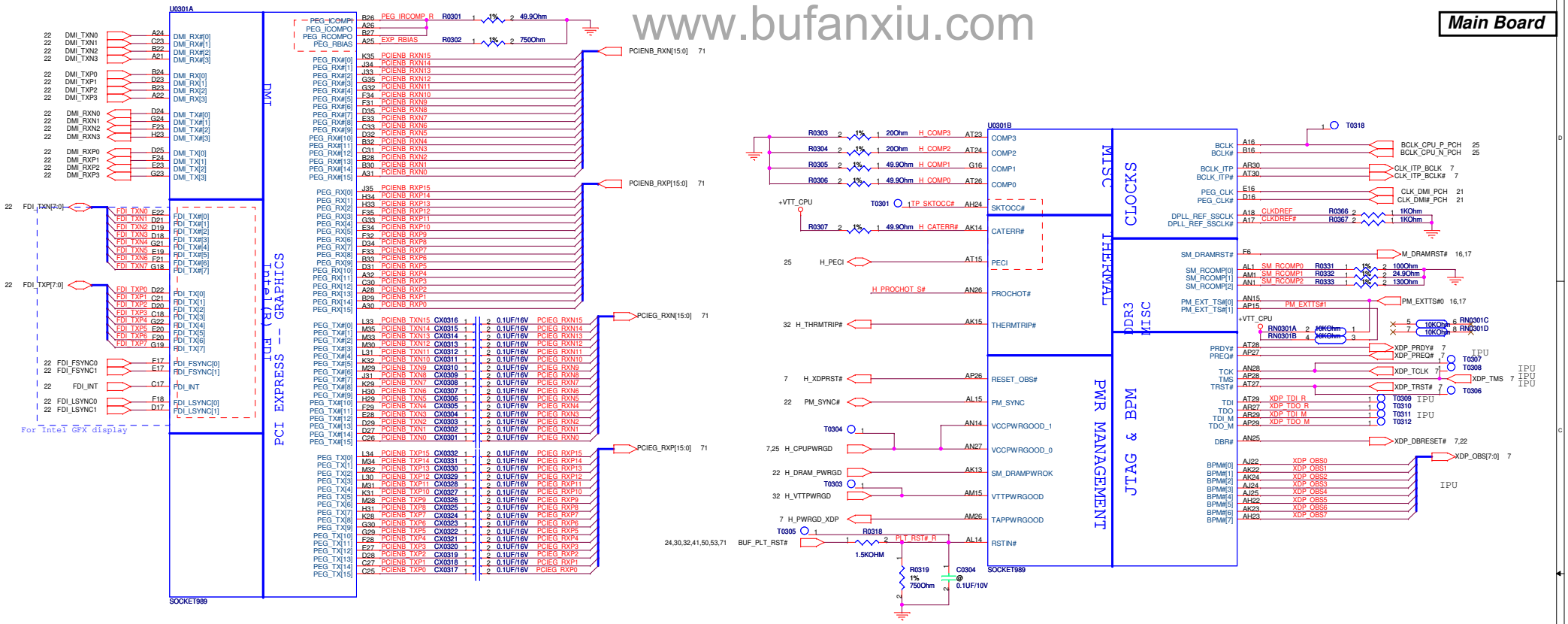
Title : System Setting

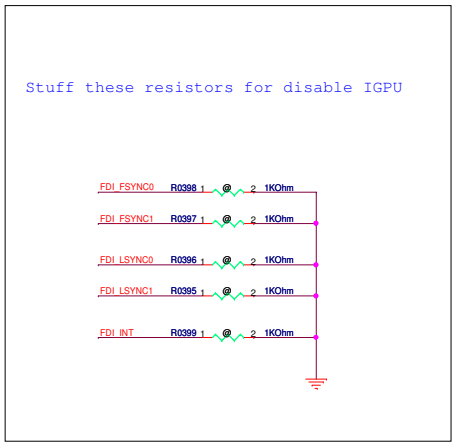
Engineer: JAY_TSAI

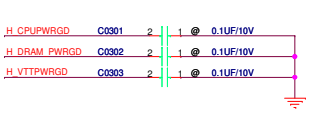
Size	Project Name	Rev
C	K42Jv	1.01

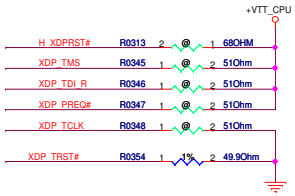
Date: Thursday, February 11, 2010 Sheet 2 of 96

Main Board

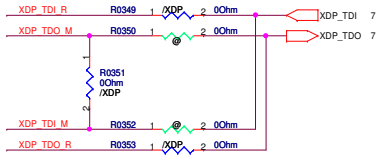








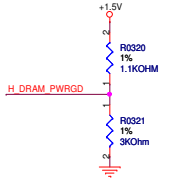
JTAG MAPPING

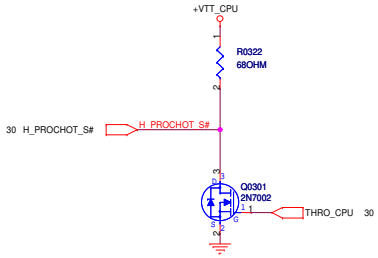


DRAMPWROK: (WW35 MoW)

Choose either one solution: -->Choose solution 2

1. This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
2. Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.





ASUSTeK COMPUTER INC. NB1	Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC	
	Engineer:	JAY_TSAI	
Size: C	Project Name: K42Jv		Rev: 1.01
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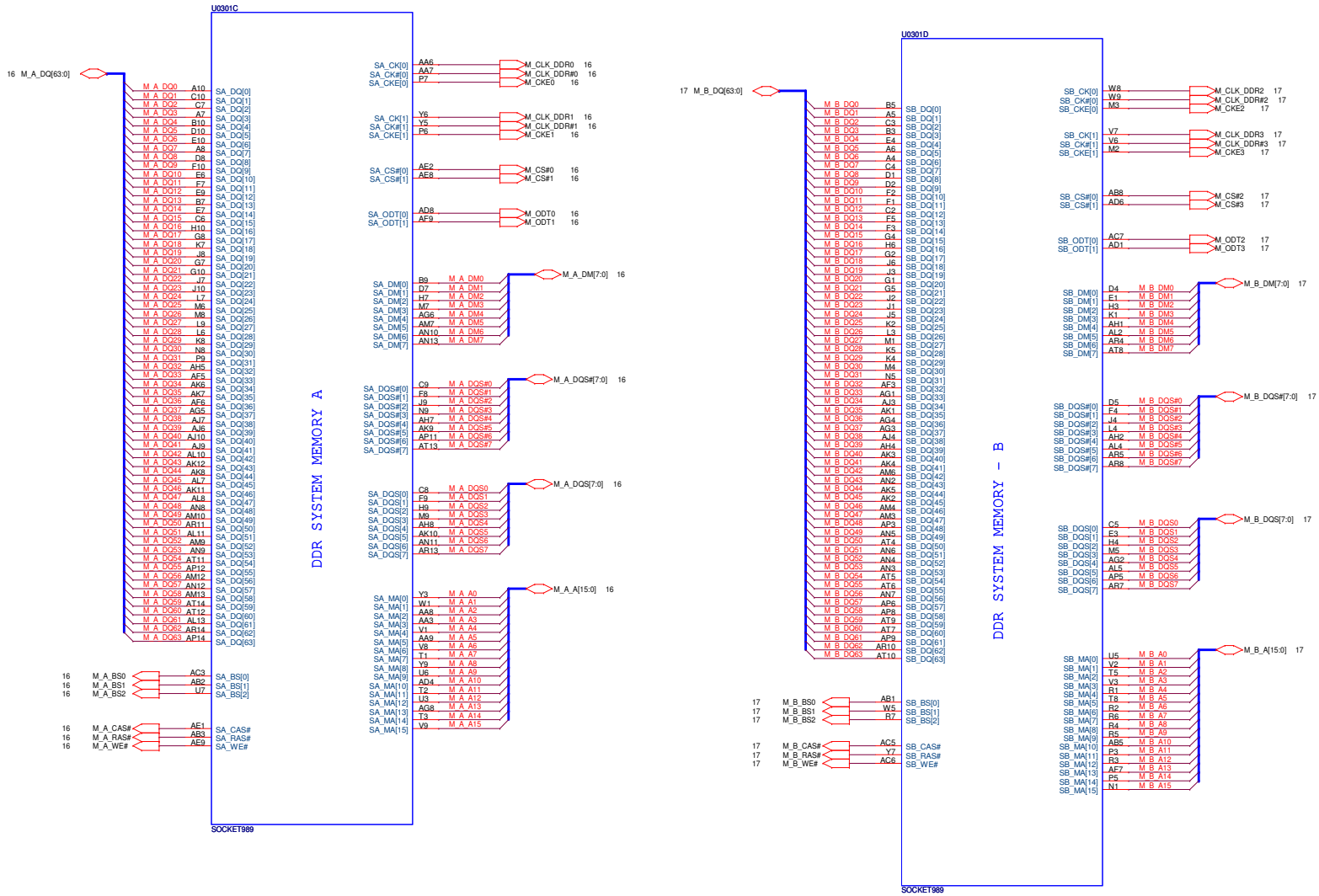
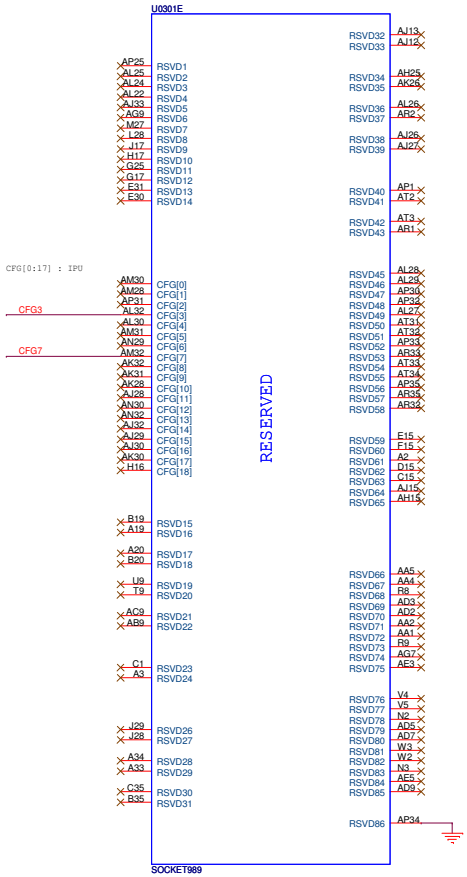
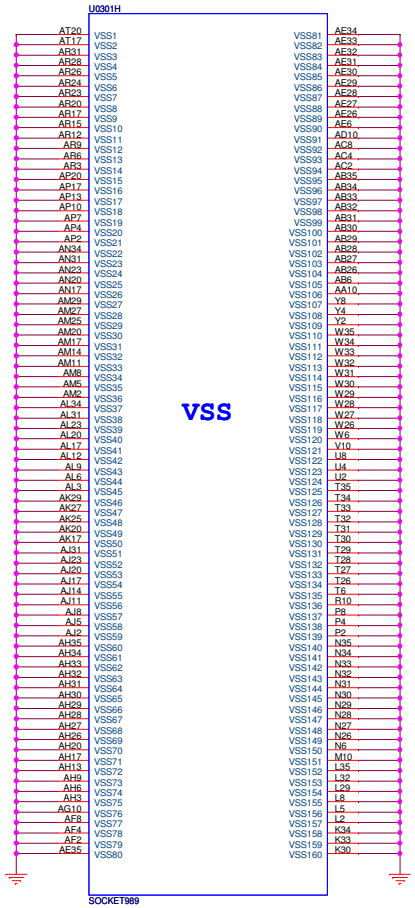
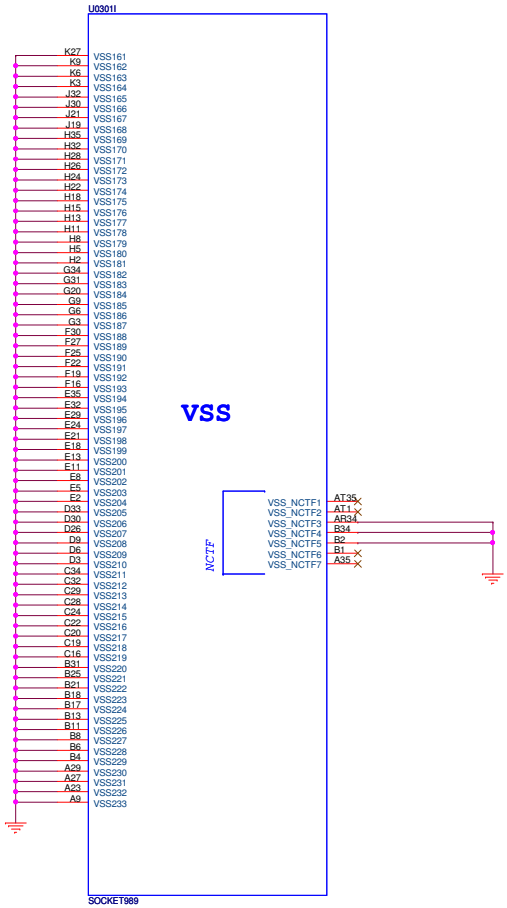


ASUSTeK COMPUTER INC. NB1	Title : CPU(2)_DDR3	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 4 of 96	







CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal.(Arrandale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Arrandale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.

CFG3 R0544 1 1% 2 3KOhm
CFG7 R0538 2 1 3KOhm 1%
@

CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.
CFG[3] – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.
- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort.
CFG[17:5] - Reserved configuration pins.
Note: Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifucation:
- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.
CFG[3] – Reserved (Used by Arrandale Ppercessors for PCI Express* Static Lane Numbering Reversal)
CFG[11:4] - Reserved configuration pins.
CFG[12] - N/A on Clarksfield processors.
CFG[17:13] - Reserved configuration pins.
Note: Hardware straps are sampled after RSTIN# de-assertion.

ASUSTeK COMPUTER INC. NB1

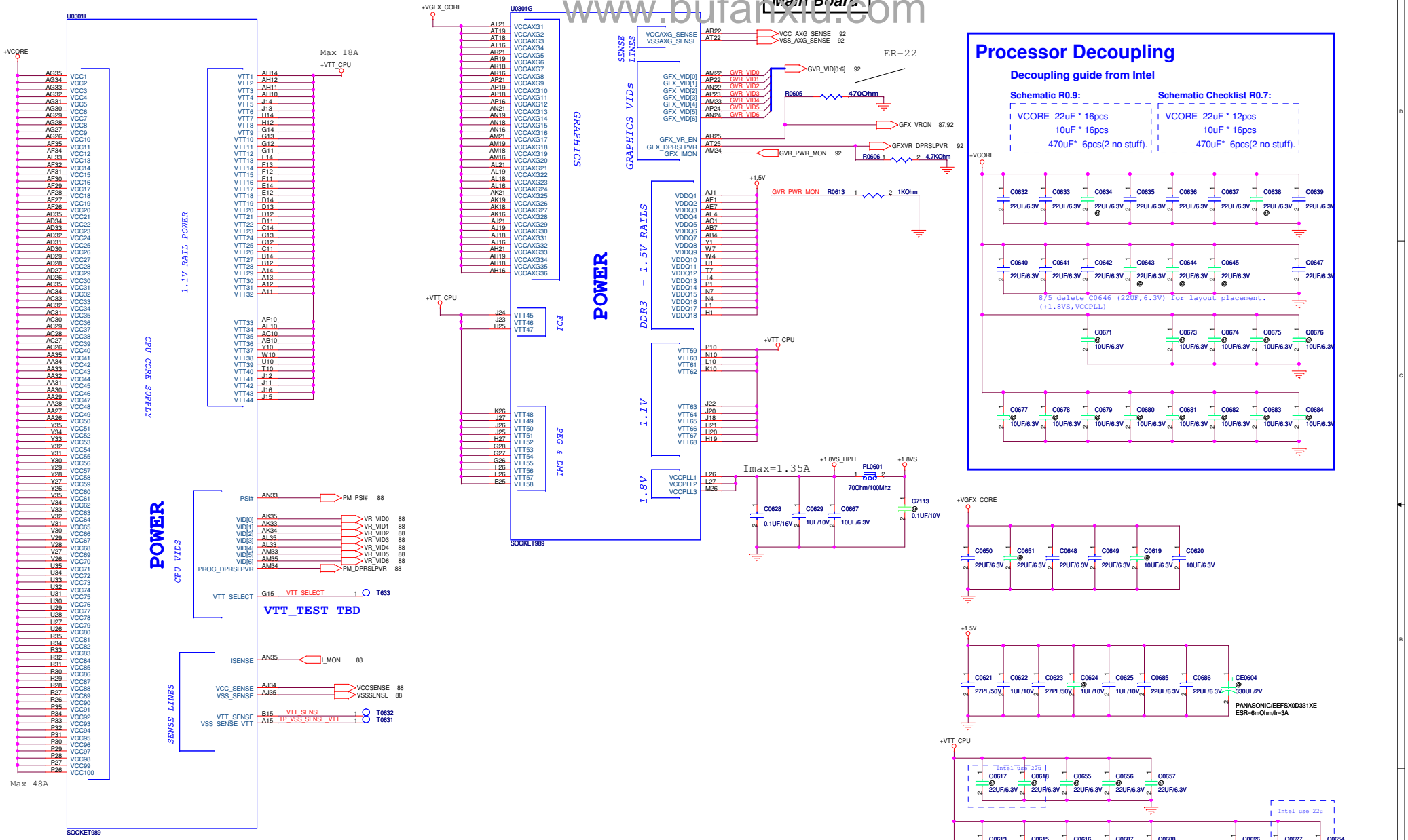
Title : CPU(3)_CFG,RSVD,GND

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 5 of 96

Main Board



Processor Decoupling

Decoupling guide from Intel

Schematic R0.9:	Schematic Checklist R0.7:
VCORE 22uF * 16pcs	VCORE 22uF * 12pcs
10uF * 16pcs	10uF * 16pcs
470uF* 6pcs(2 no stuff).	470uF* 6pcs(2 no stuff).

8/5 delete C0646 (22UF,6.3V) for layout placement.
(+1.8VS,VCCPLL)

PANASONIC/EEFSX0D331XE
ESR=6mOhm/Ir=3A

Intel use 22u

ASUSTeK COMPUTER INC. NB1	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
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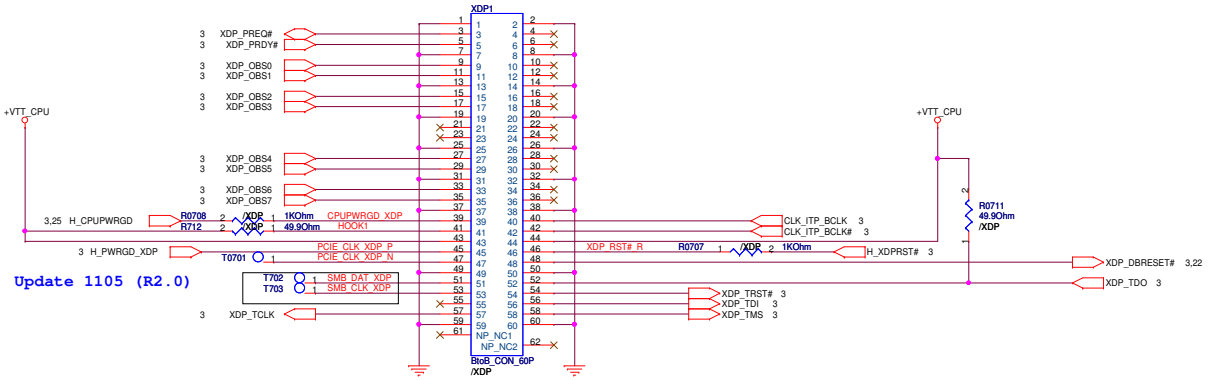
Title : CPU(4)_PWR

CPU XDP connector



Update 1105 (R2.0)

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 7 of 96		

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 8 of 96		

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 9 of 96		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer:	
Size: Custom	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 10 of 96	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer:	
Size: Custom	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 11 of 96	

Main Board

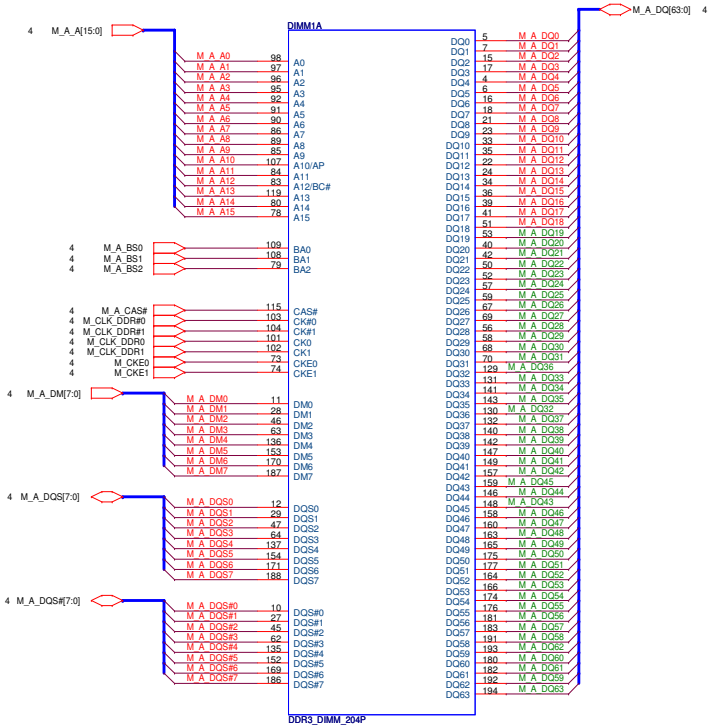
ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer:	
Size: Custom	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 12 of 96	

Main Board

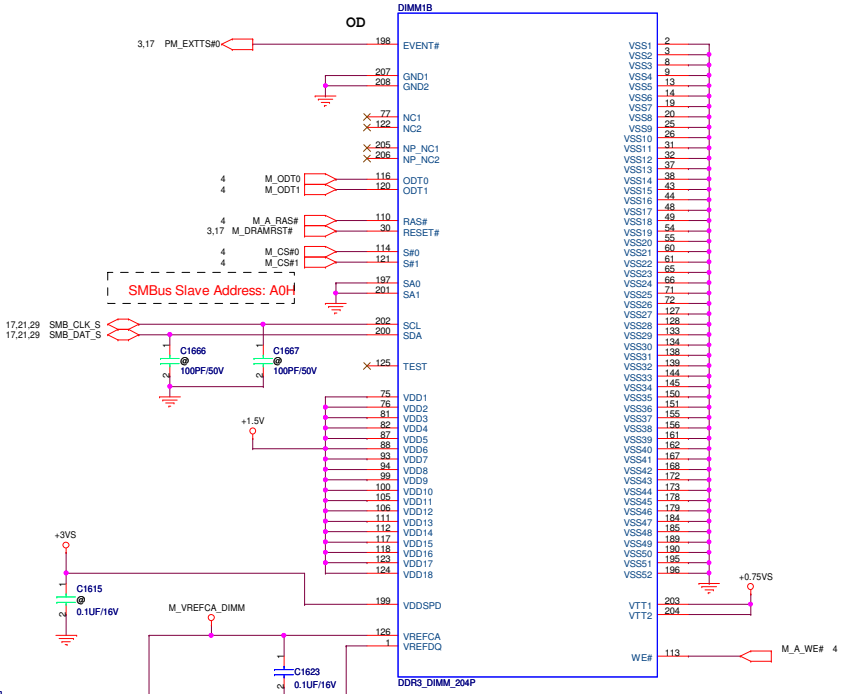
ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer:		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 13 of 96		

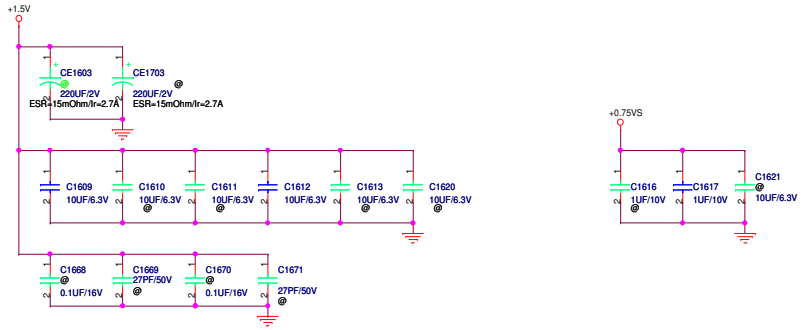
ASUSTeK COMPUTER INC. NB6	Title :	
	Engineer:	
Size: A	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 14 of 96	

ASUSTeK COMPUTER INC. NB6	Title :	
	Engineer:	
Size: A	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 15 of 96	



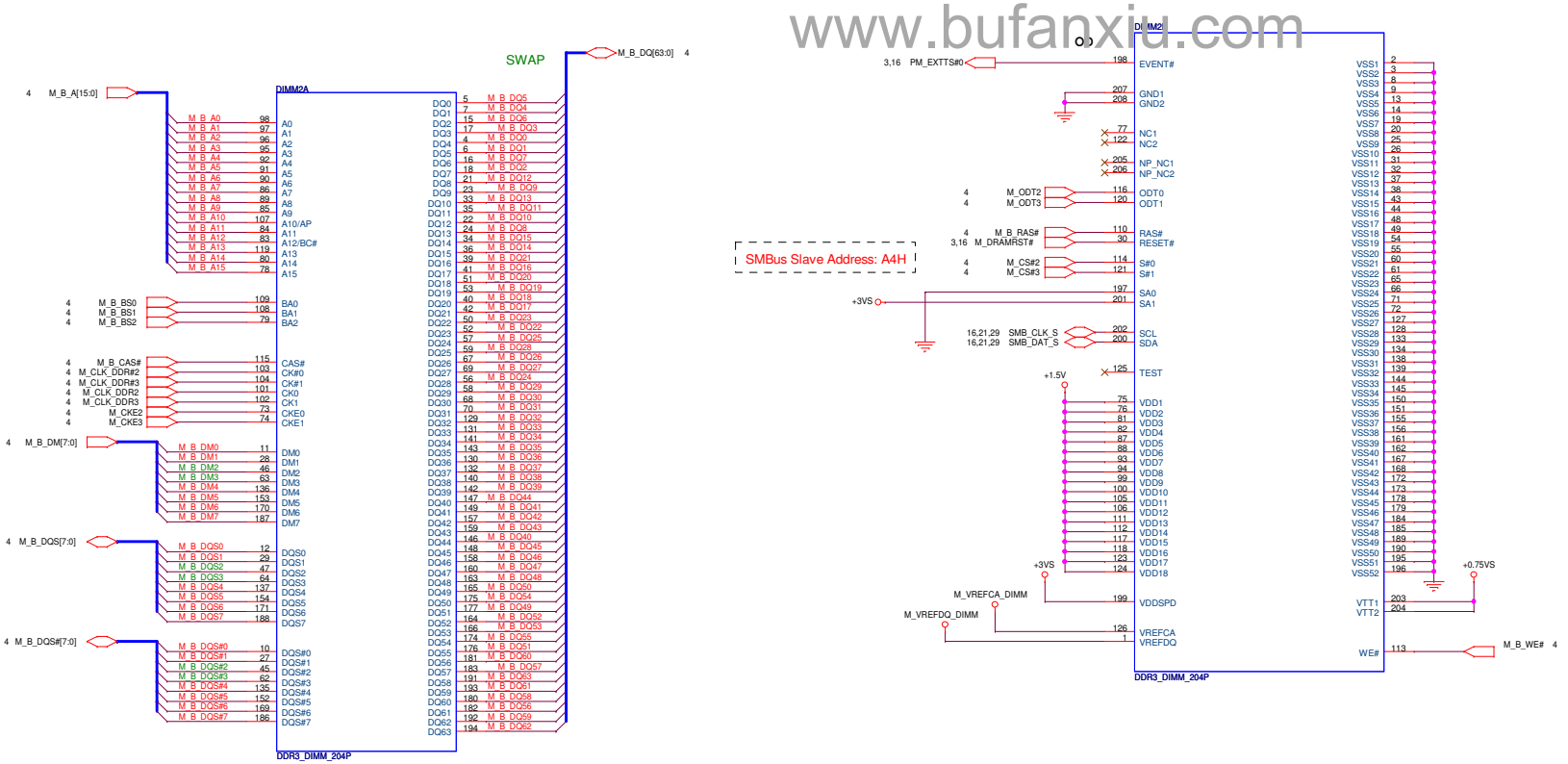
REV 9.2mm





Layout Note: Place these caps near SO DIMMS

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_0	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 16 of 96	



STD 5.2mm

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1		
	Engineer: JAY_TSAI		
Size C	Project Name K42Jv		Rev 1.01
Date: Thursday, February 11, 2010	Sheet 17 of 96		

ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 18 of 96		

Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. Note: the internal pull-up is disabled after PLTRST# de-asserts. **NOTE:** This signal should not be pulled low.
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts.If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination**: 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GbE LAN.

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDATA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDATA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDATA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination**: 0 1 Reserved; 1 0 PCI; 1 1 SPI; 0 0 LPC **NOTE:** If option 00 LPC is selected, BIOS may still be placed on LPC; however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high

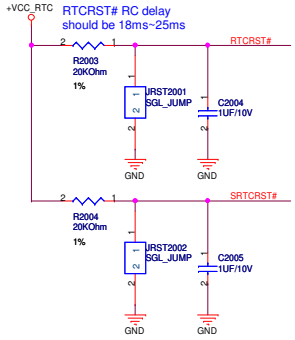
Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_EN#/GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. **NOTE:** Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. **NOTE:** This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. **NOTE:** This signal should not be pulled low
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. **NOTE:** A strong pull up may be needed for GPIO functionality
L_DDC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

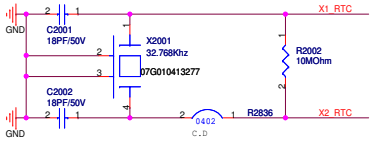
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

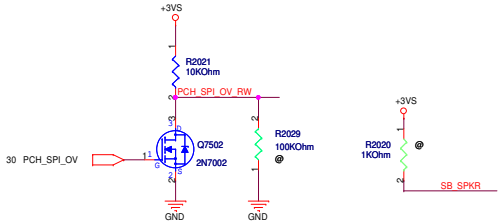


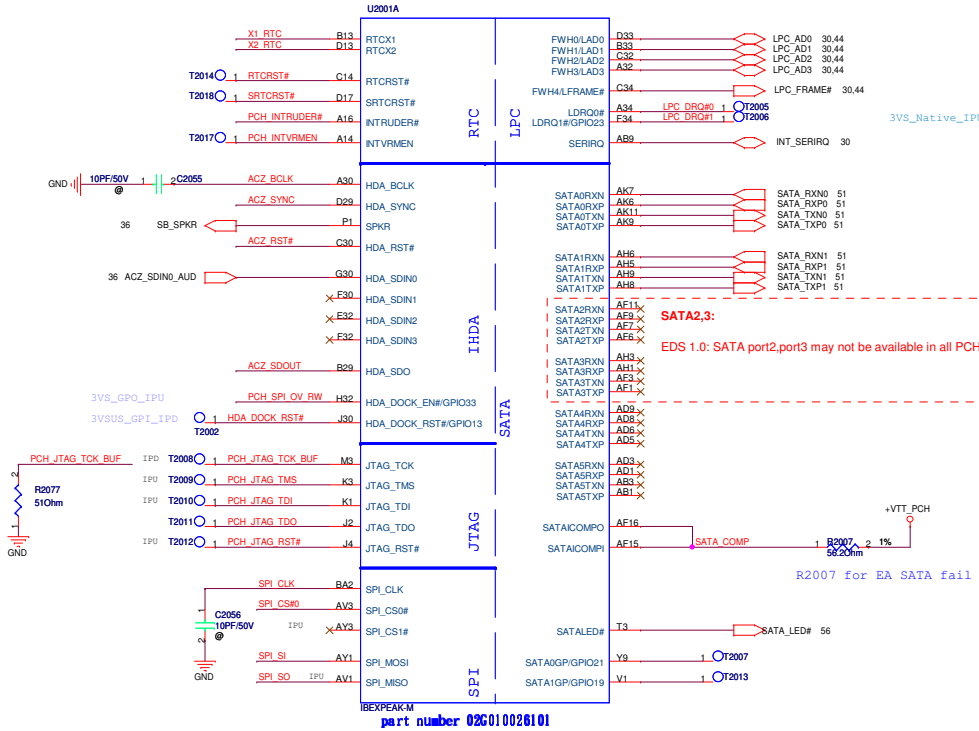
DG2.0 P297
RTCRST# and SRTCRST# can not be shorted together

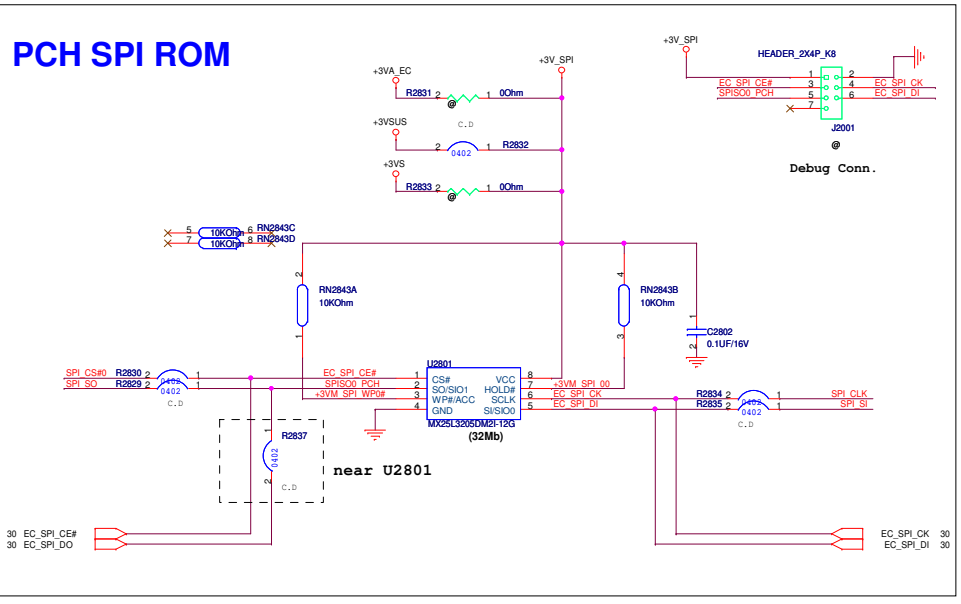
Strap information:

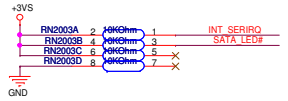
	H	L
ACZ_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)	1.5V	1.8V
SB_SPKR: No reboot strap (IPD)	No reboot	Disable No reboot
PCH_SPI_OV_RW: (IPU)	No Flash ME FW	Flash ME FW
SPI_SI: iTPM strap. (IPD)	Enable	Disable
PCH_INTVRMEN Integrated 1.05 V VRM Enable /Disable	Enable	Disable

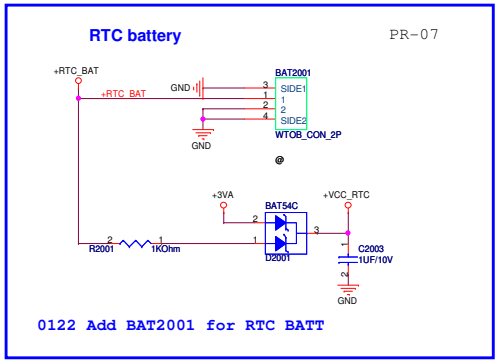




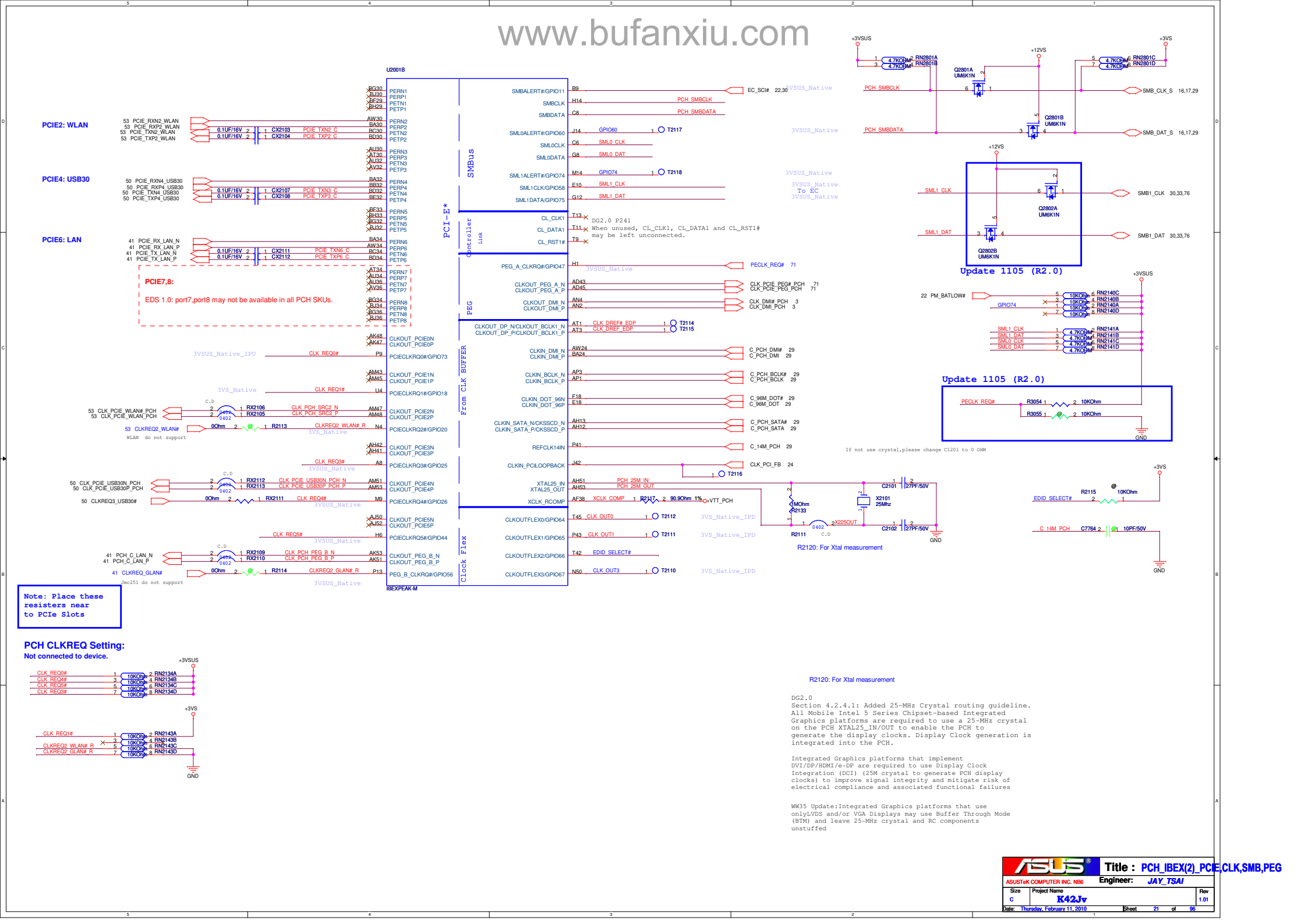




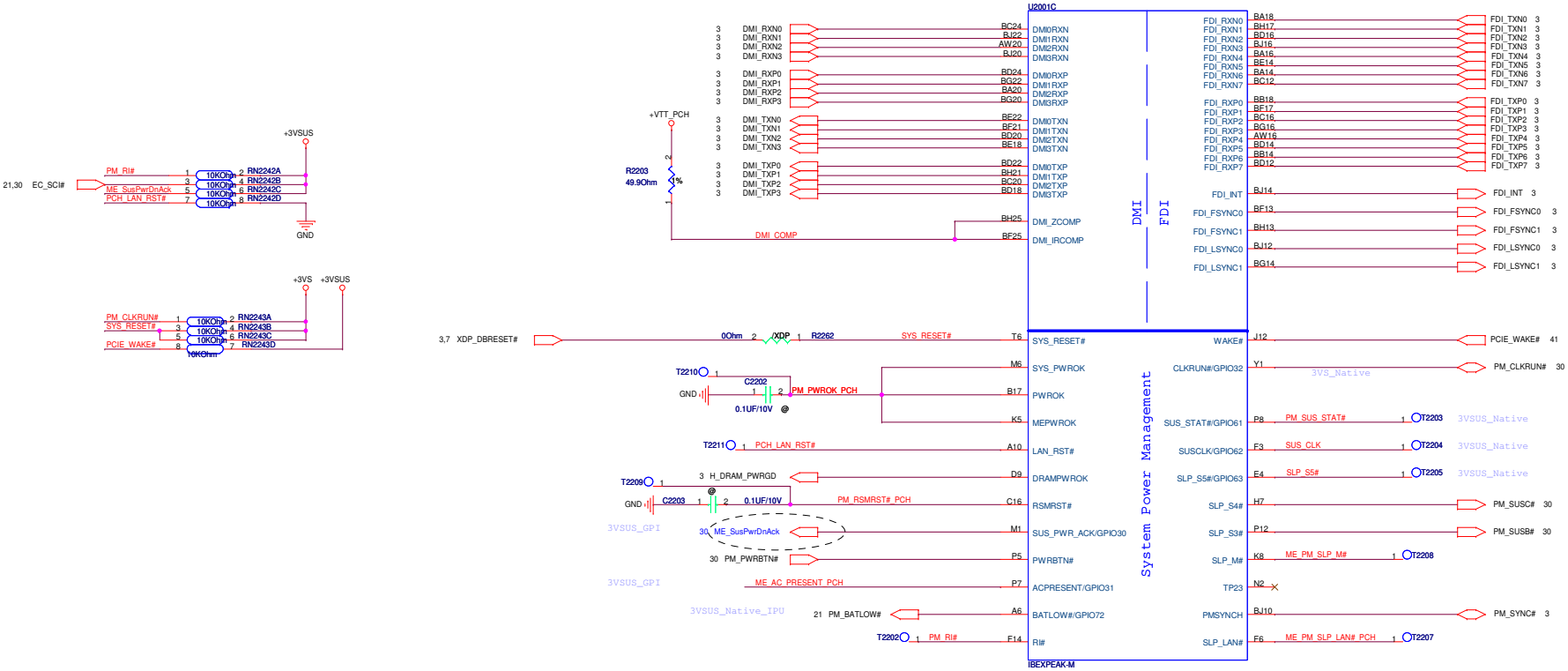




ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(1)SATA,IHDA,RTC,LPC		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 20 of 96		



pre-ES1 not support
Reversal Feature



R1.1,item L15

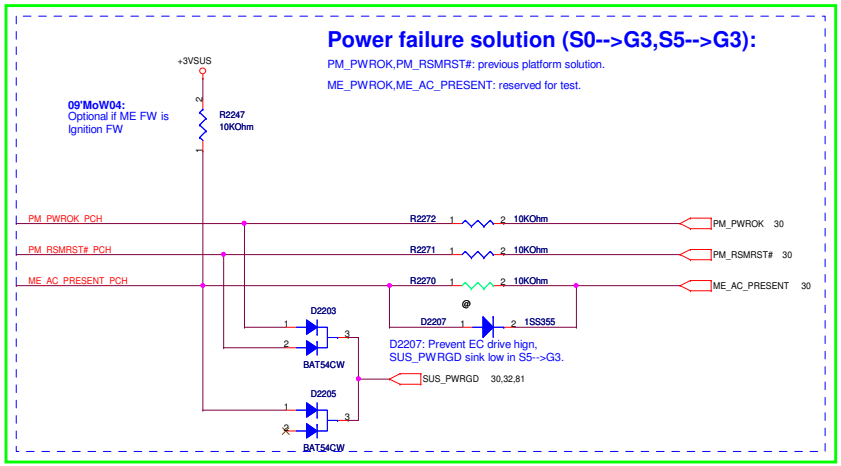


Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required **Note:** Optional if Intel ME FW is Intel® ME Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) **Note:** If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel® ME-EC perspective.
SLP_S3#	Optional	Required **Note:** If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.

ASUSTeK COMPUTER INC. NB6

Title : PCH_IBEX(3)_FDI,DMI,SYS PWR

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

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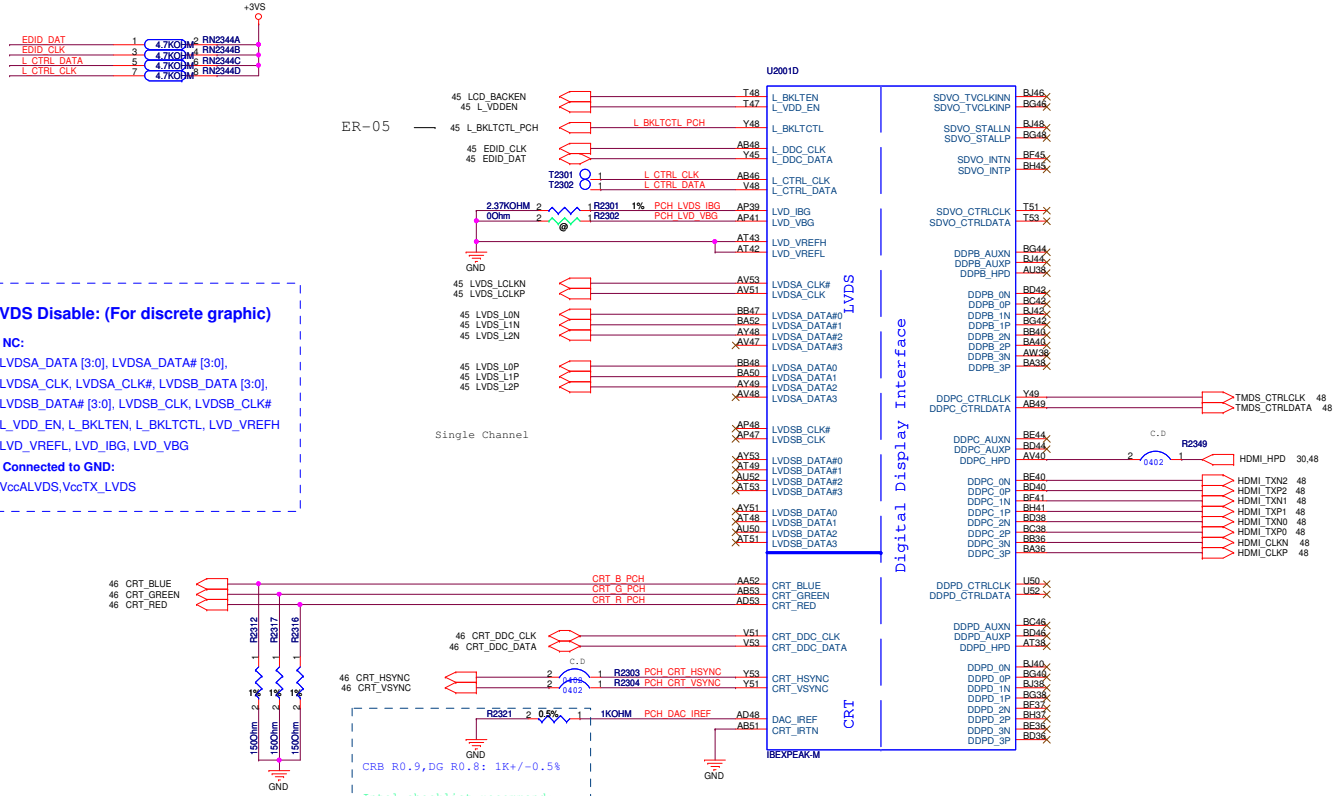

LVDS Disable: (For discrete graphic)

1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(4)_DP,LVDS,CRT	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
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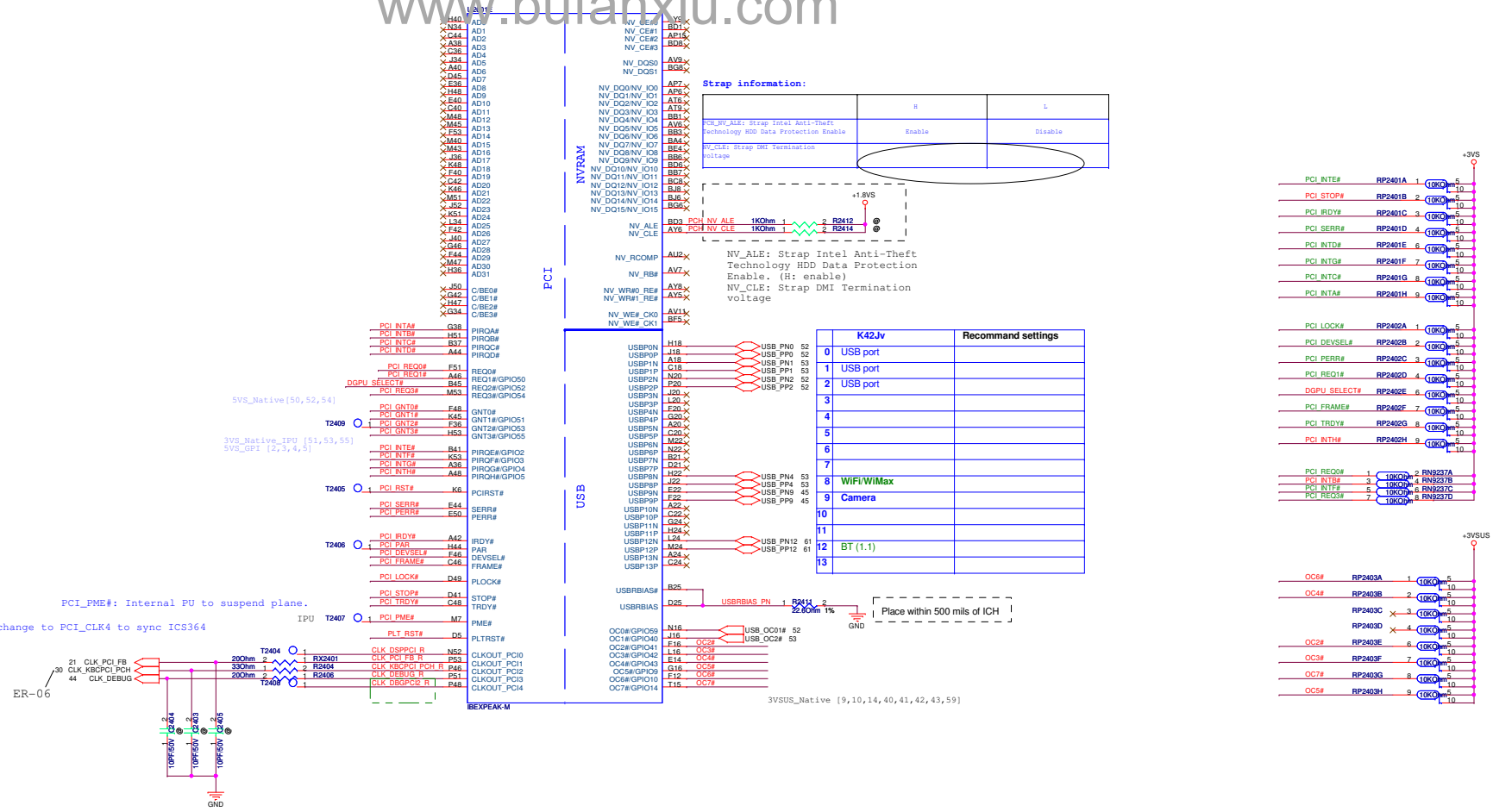


GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap		
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

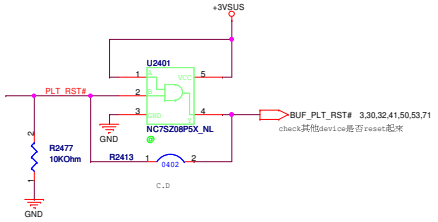
Sampled on rising edge of PWROK.

PCI_GNT0# R2440 1KOhm
PCI_GNT1# R2441 1KOhm
GND

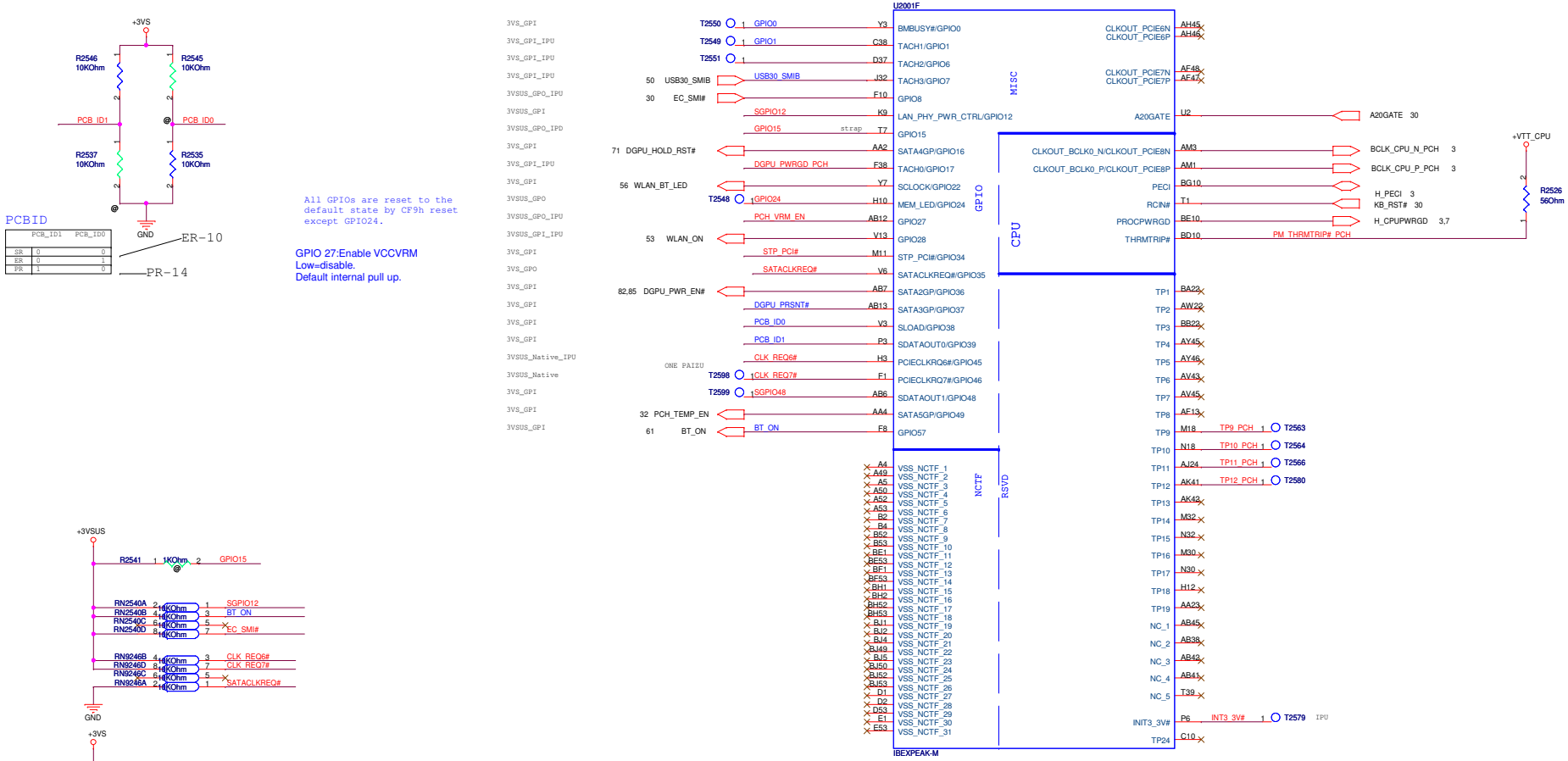
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

PCI_GNT3# R2444 1KOhm
GND



POWER按照提供的default值調節電壓



Title : PCH_IBEX(6)CPU,GPIO,MISC		
ASUSTeK COMPUTER INC. NB6	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
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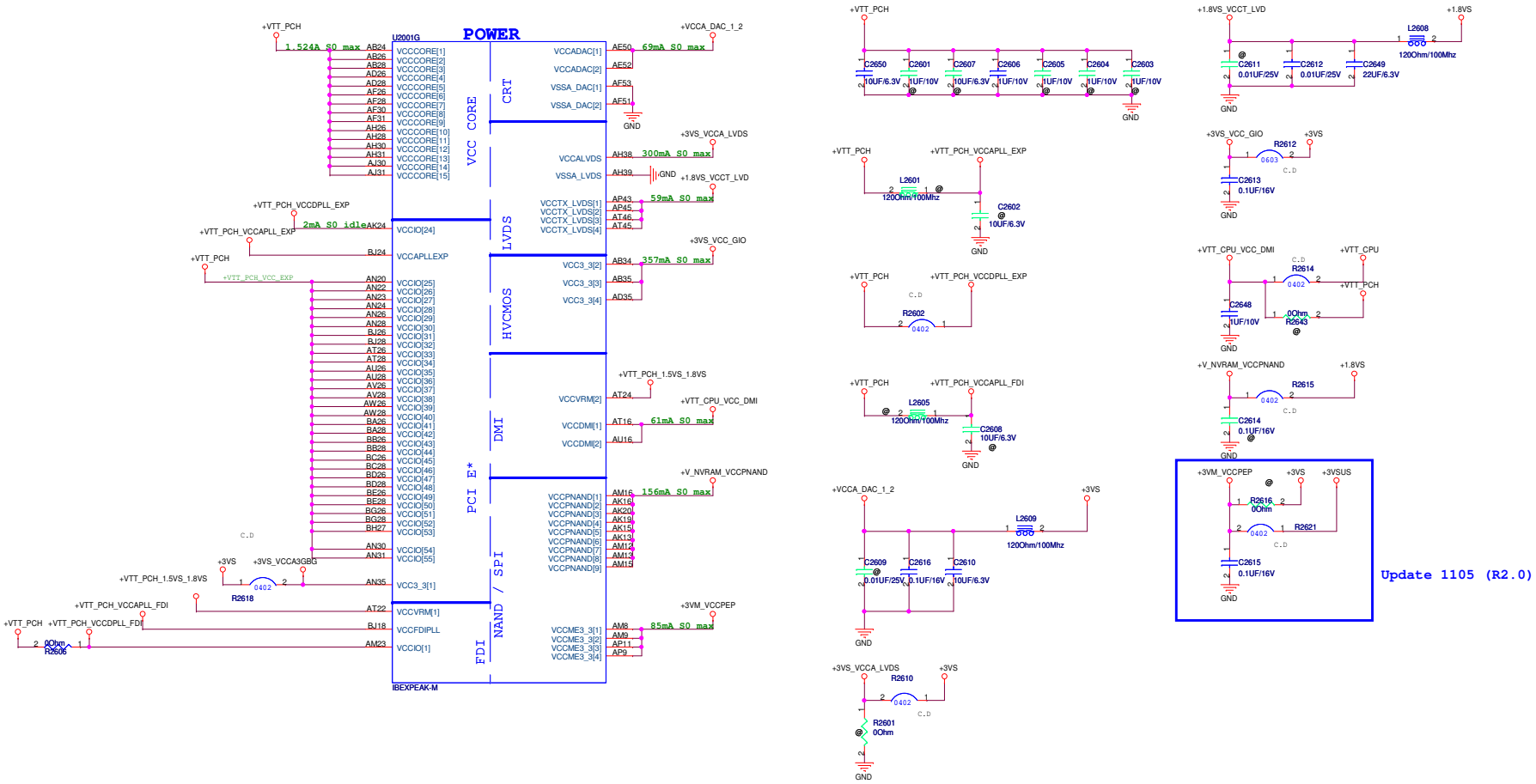
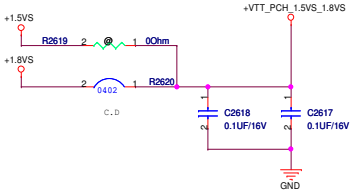


Update 1105 (R2.0)

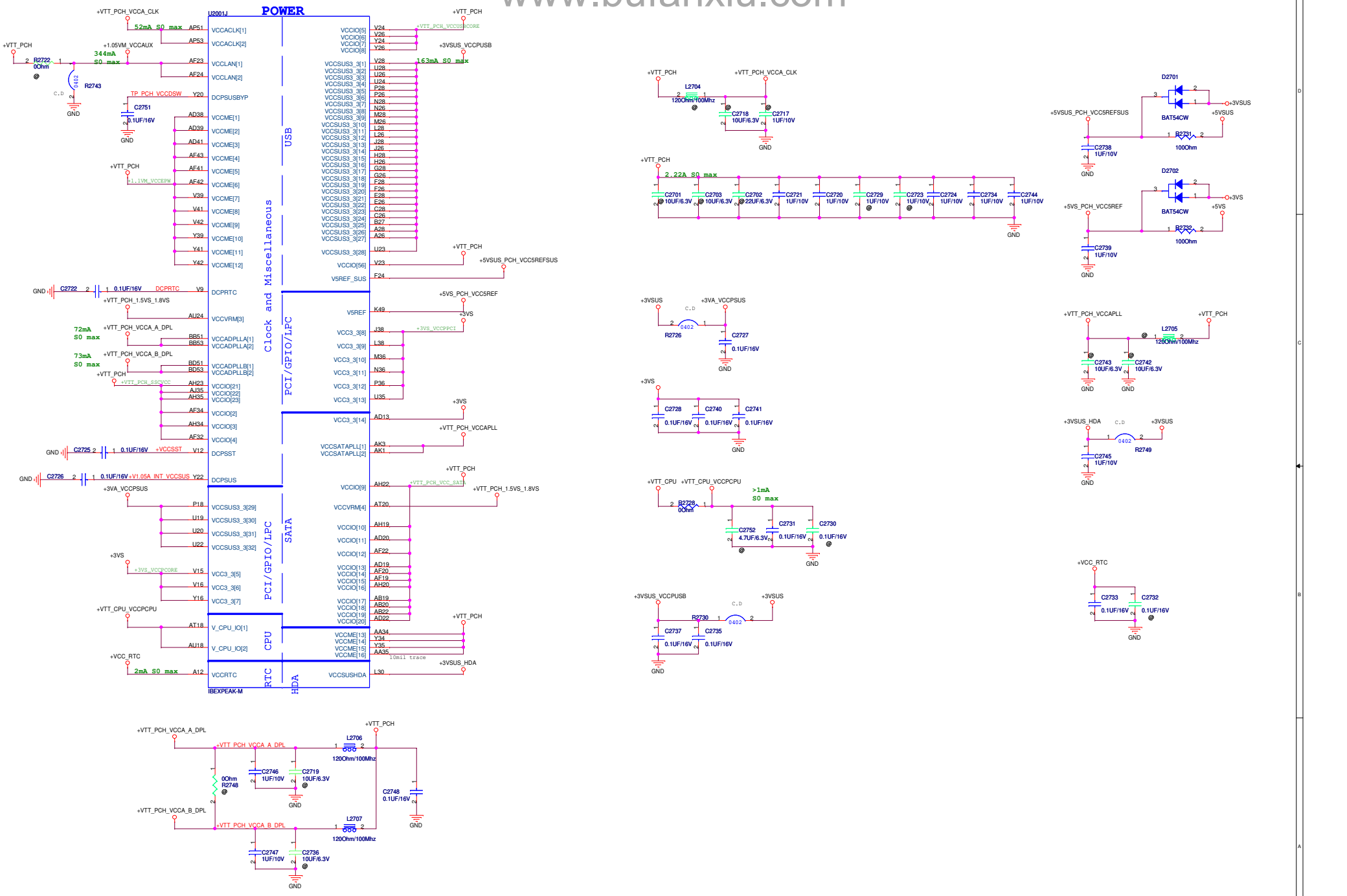


HDA_SYNC: Select VCCVRM 1.5V or 1.8V (IPD)
Low: 1.8V
High: 1.5V

GPIO27 NC:enable internal regulator for:

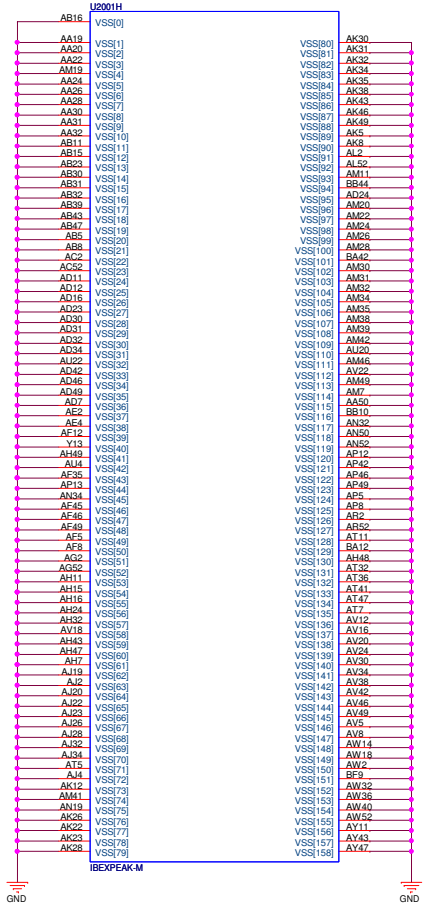
VccAClk	VccapllEXP
VccFDIPLL	VccSATAPLL

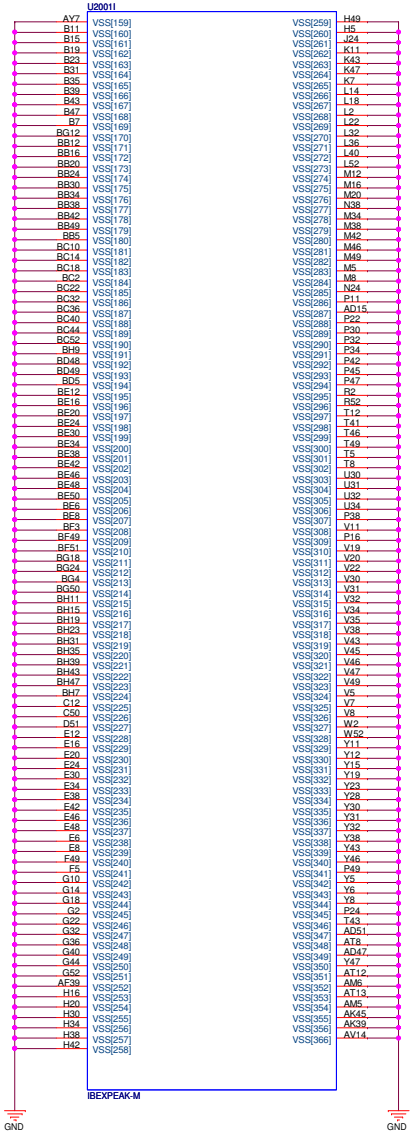
ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(7)_POWER,GND	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 26 of 96	



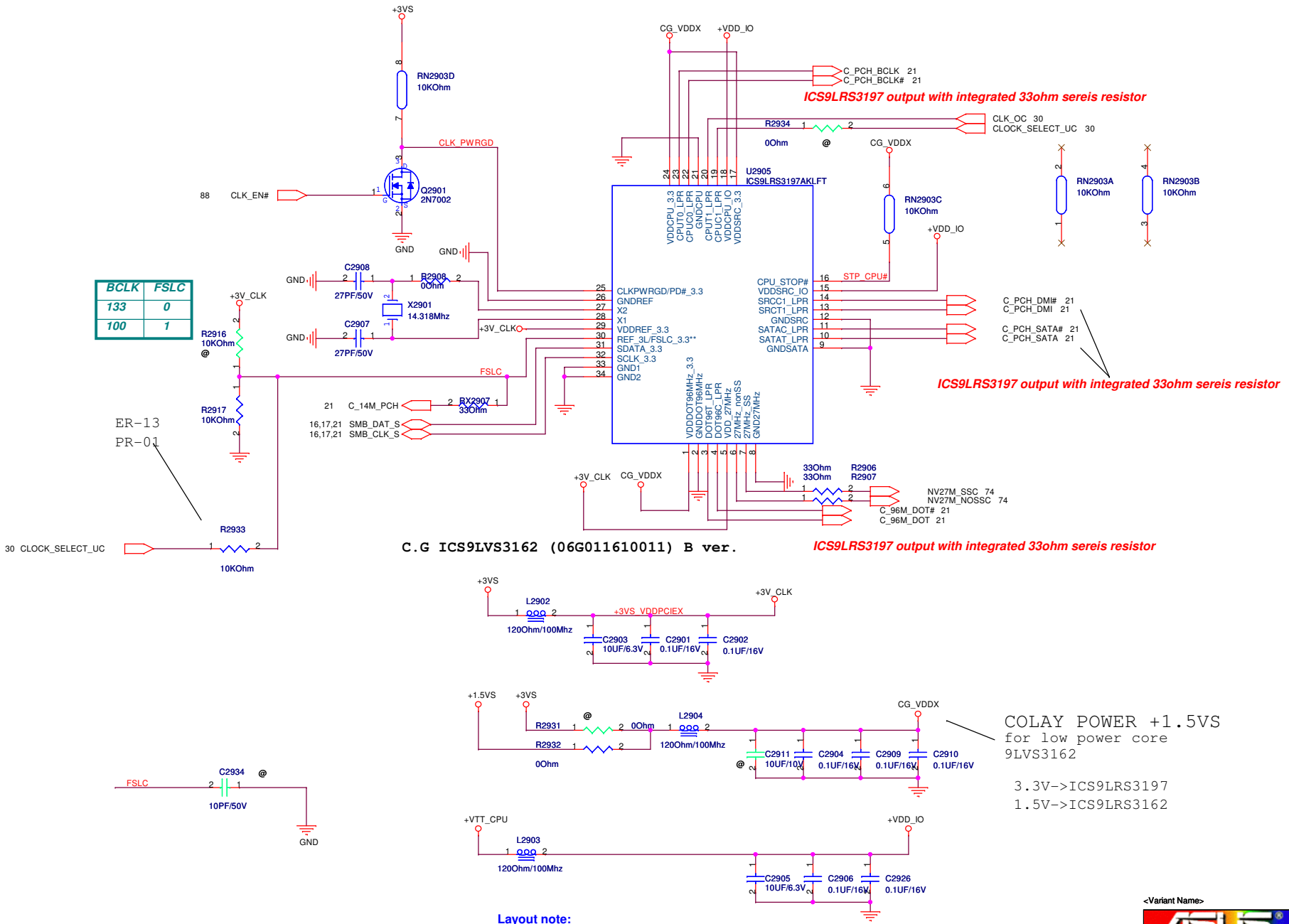
ASUSTeK COMPUTER INC. NB6	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 27 of 96	

Title :PCH_IBEX(8)_POWER,GND



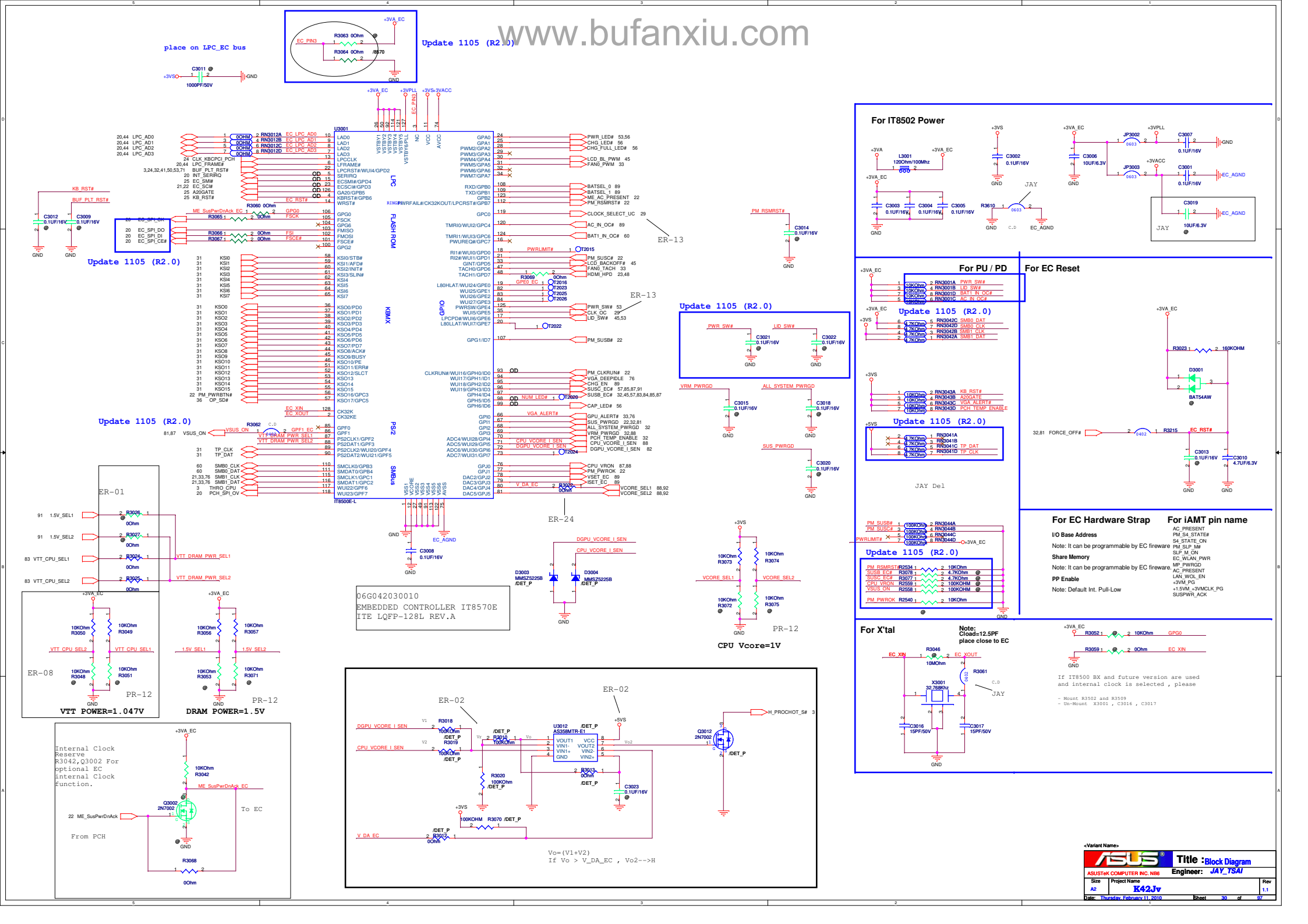


ASUSTeK COMPUTER INC. NB6	Title :PCH GND	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 28 of 96	

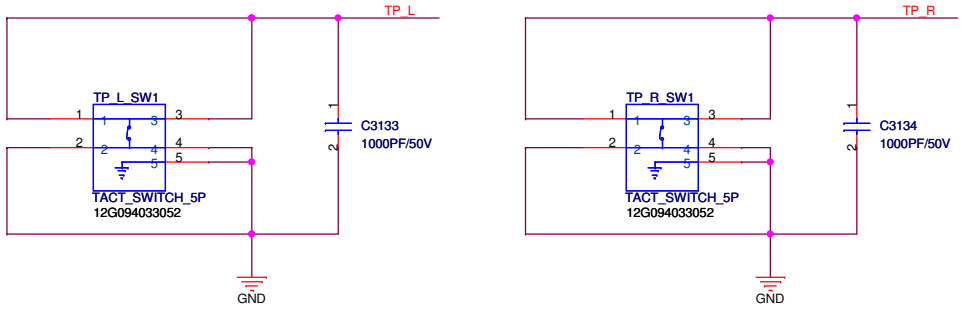


<Variant Name>

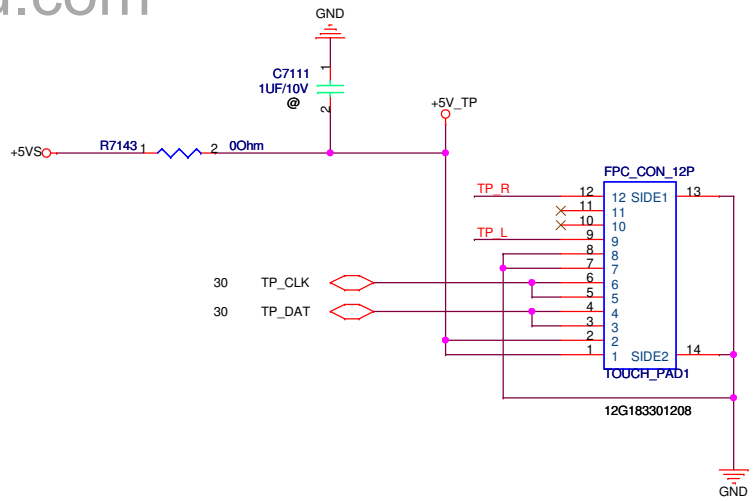
Title :	ICS9LRS3197
ASUSTek Computer INC.	Engineer: JAY_TSAI
Size: A3	Project Name: K42Jv
Rev: 1.0G	
Date: Thursday, February 11, 2010	Sheet 29 of 96



TouchPad

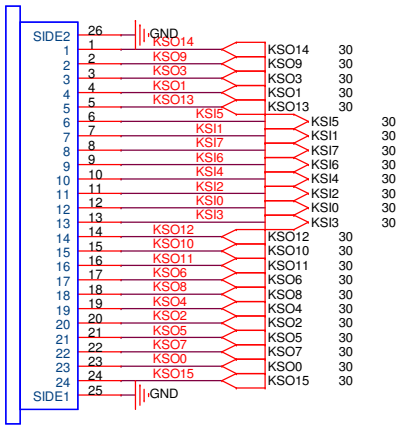


1.0 EMI test need mount C3133 and C3134



Keyboard Connector

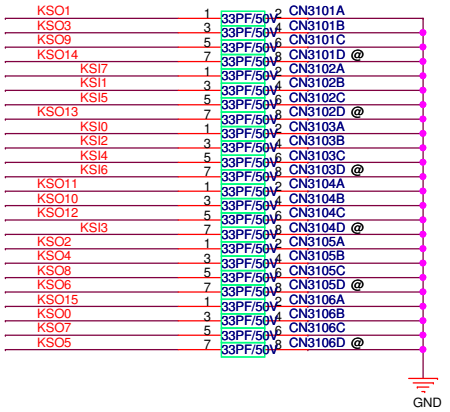
KB_CON1



FPC_CON_24P

12G182102402

EMI Request



<Variant Name>

ASUSTeK COMPUTER INC. NB6	Title : Block Diagram	
	Engineer: JAY_TSAI	
Size: Custom	Project Name: K42Jv	Rev: 1.1
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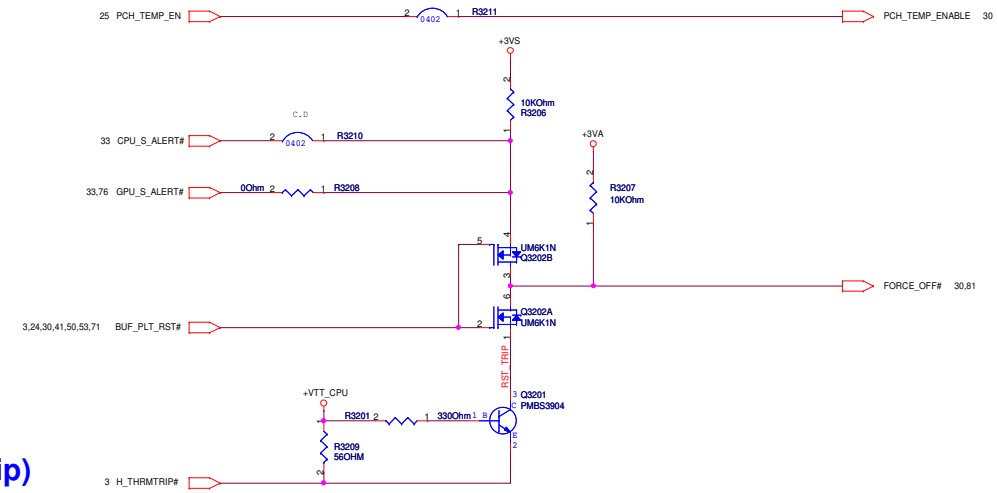
Thermal Policy

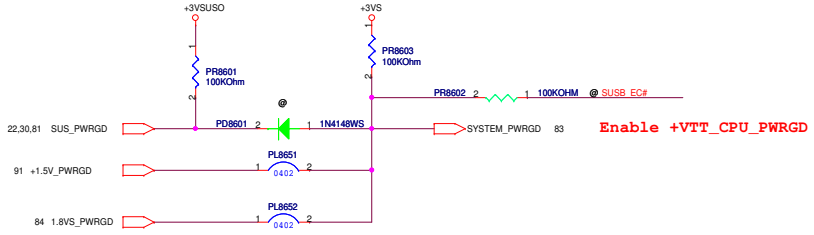
Input 1(sensor)

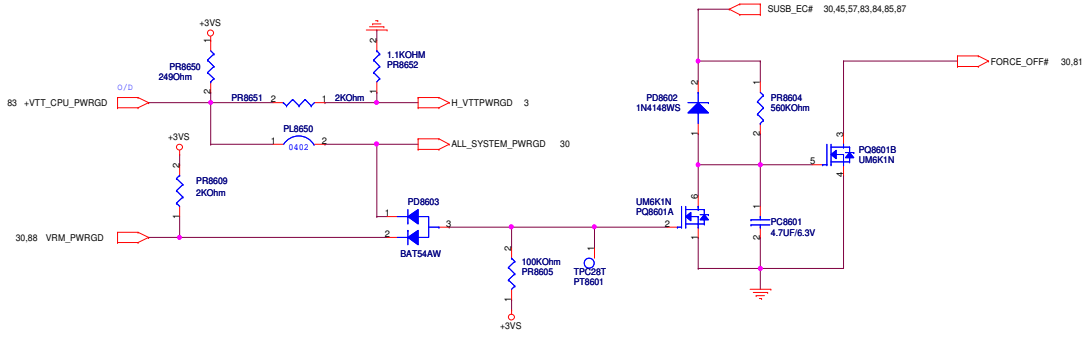
Input 2(thermtrip)



Output (shut down)

POWER GOOD DETECTER





ASUSTeK COMPUTER INC. NB4	Title : Forceoff#_PWRGD_Thermal	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
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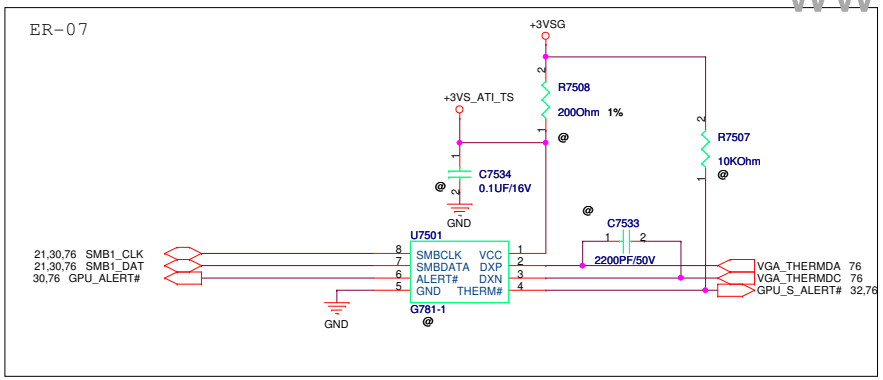
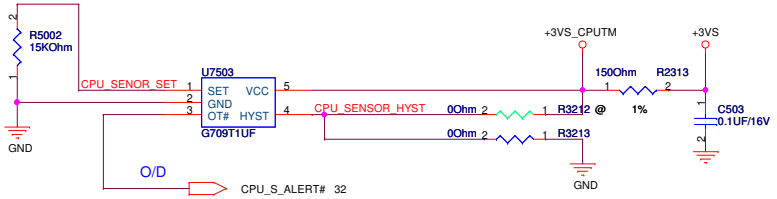
GPU Thermal Sensor



CPU Thermal Sensor

Update 1108 (R2.0)

R5002 for thermal 96C

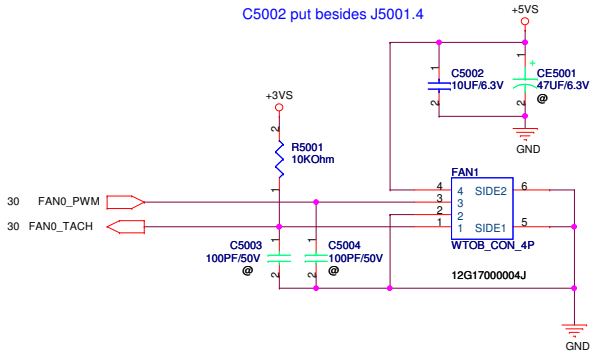


HYST=VCC : 10 degree
HYST=GND : 10 degree C

U7503 under CPU socket

PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.



ASUSTeK COMPUTER INC

Title : FAN_Thermal

Engineer: JAY_TSAI

Size	Project Name	Rev
Custom	K42Jv	108

Date: Thursday, February 11, 2010 Sheet 33 of 96

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	K42Jv	108

Date: Thursday, February 11, 2010 Sheet 34 of 96

ASUSTeK COMPUTER INC. NB4	Title : ****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 35 of 96		

ANALOG MOAT

Update 11.08 (R2.0)

+3VS 50mA
C3639 0.1UF/16V
C3635 0.1UF/16V
GND
Close to pin1,9

0Ohm R7977 /ALC269_VB
PU9021 UP7714BMA5-00 /ALC269_VA
EN NC/SS/FB GND VIN VOUT
P_5VASET
PC9027 10UF/16V /ALC269_VA
PC9022 /ALC269_VA 1000PF/50V
PR9020 1% 49.9KOHM /ALC269_VA
PR9021 10.2KOHM 1% /ALC269_VA
PC9028 1UF/16V /ALC269_VA
+5VS_AUDIO PT9021 TPC26T
PC9023 10UF/6.3V /ALC269_VA
PC9024 0.1UF/16V
PC9026 0.1UF/16V
GND_AUDIO
Place next to pin 38,25
Vout=0.8*(1+(49.9K/10.2K))

+5VS L3621 70Ohm/100Mhz +5VS_AMP
C3620 10UF/6.3V
C3623 10UF/6.3V
C3622 1UF/10V
C3621 0.1UF/16V
GND
Place next to pin 39,46

U3621B ALC269Q-VA6-GR
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9
50 51 52 53 54 55 56 57 58
GND

For EMI
JP3004 JP3005 JP3006 JP3007 0603
GND GND_AUDIO
CHANGE 0 OHM

PR-04
+3VS +5VS
R3623 100KOhm
R3622 10KOhm /ALC269_VB
ER-11
D3702 BAT54AW
Q3605 2N7002
ACZ_RST#_AUD AMP_PD#_Q OP_SD#
AMP_PD#
ACZ_BCLK_AUD C3636 10PF/50V
20 ACZ_SDOUT_AUD 20 ACZ_BCLK_AUD 20 ACZ_SDIN0_AUD 20 ACZ_SYNC_AUD 20 ACZ_RST#_AUD
R3621 33Ohm ACZ_SDIN
PC_BEEP
ER-15 PR-03
R3631 0402
37 A_JD_MIC1
SENSE_A
MIC2_INT_L MIC2_INT_R

U3621A ALC269Q-VA6-GR
DVDD GPIO0/DMIC_DATA GPIO1/DMIC_CLK PD# SDATA_OUT BCLK DVSS SDATA_IN DVDD_IO SYNC RESET# PCBEEP
GND SPDIFO DVDD2 SPK_OUT_R+ SPK_OUT_R- SPK_OUT_L+ SPK_OUT_L- AVDD2 AVSS2
SPK_OUT_R+ SPK_OUT_R- SPK_OUT_L+ SPK_OUT_L- PVDD1 PVSS1
CBP CBN CPVEE HPOUT_R HPOUT_L CPVREF MIC1_VREFO_R MIC2_VREFO MIC1_VREFO_L VREF AVSS1 AVDD1
SPKR#A LINE2_R LINE2_L MIC2_L MIC2_R JDREF MONO_OUT MIC1_R MIC1_L LINE1_L LINE1_R

H_SPKL+ H_SPKL- H_SPKR- H_SPKR+
EAPD +5VS_AMP +5VS_AUDIO GND GND_AUDIO
A_CBP A_CBN C3628 2.2UF/10V
A_CPVEE C3629 2.2UF/10V
A_CPVREF_VBMICREF
VB_LDO_CAP VB_LDO_CAP
MIC1_VREFOUT_R MIC2_VREFOUT MIC1_VREFOUT_L
C3631 C3650 2.2UF/10V 0.1UF/16V
PR-02
R3624 20KOhm 1%
A_JDREF
AC_MIC_HP_R AC_MIC_HP_L

PR-13
269_VB2 : 02G611005010
269_VB5 : 02G611005015

Update 11.08 (R2.0)
A_CPVREF_VBMICREF 0Ohm R7979 /ALC269_VA GND_AUDIO
0Ohm R7980 /ALC269_VB
VB_LDO_CAP 0Ohm R7978 /ALC269_VA MIC1_VREFOUT_L 37
10UF/6.3V C3624 /ALC269_VB GND_AUDIO
PIN28 ,PIN31 MODIDY

MIC2_VREFOUT AC53 100PF/50V GND_AUDIO

PC BEEP

20 SB_SPKR R3643 4.7KOhm SB_SPKR PC_BEEP_C C3646 0.1UF/16V PC_BEEP
R3642 4.7KOhm GND

INTERNAL MIC

MIC2_INT_R C3641 1UF/10V MIC_IN_AC 37
MIC2_INT_L C3642 1UF/10V
AC45 0.1UF/16V GND_AUDIO

EXT. MIC

MIC1_INT_R C3644 1UF/10V EX_MIC_IN_AC 37
MIC1_INT_L C3643 1UF/10V
AC46 0.1UF/16V GND_AUDIO

PR-06

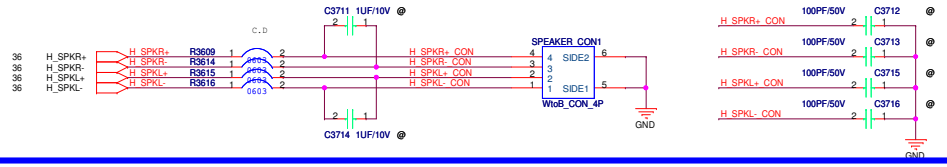
MUTE
+3VSUS +12V
R3625 10KOhm
R3627 2.2MOhm
R3626 10KOhm MUTE_POP#
Q3608A UM6K1N Q3608B UM6K1N
C3647 0.1UF/16V
EAPD OP_SD# D3703 BAT54AW
ACZ_RST#_AUD R3644 100KOhm
GND

Option 1
Q3606A UM6K1N Q3607A UM6K1N
AC_MIC_HP_R AC_MIC_HP_R_Q
MUTE_POP#
AC_MIC_HP_L AC_MIC_HP_L_Q
Q3606B UM6K1N Q3607B UM6K1N
C3637 100UF/6.3V A_MIC_HP_R 37
C3638 100UF/6.3V A_MIC_HP_L 37

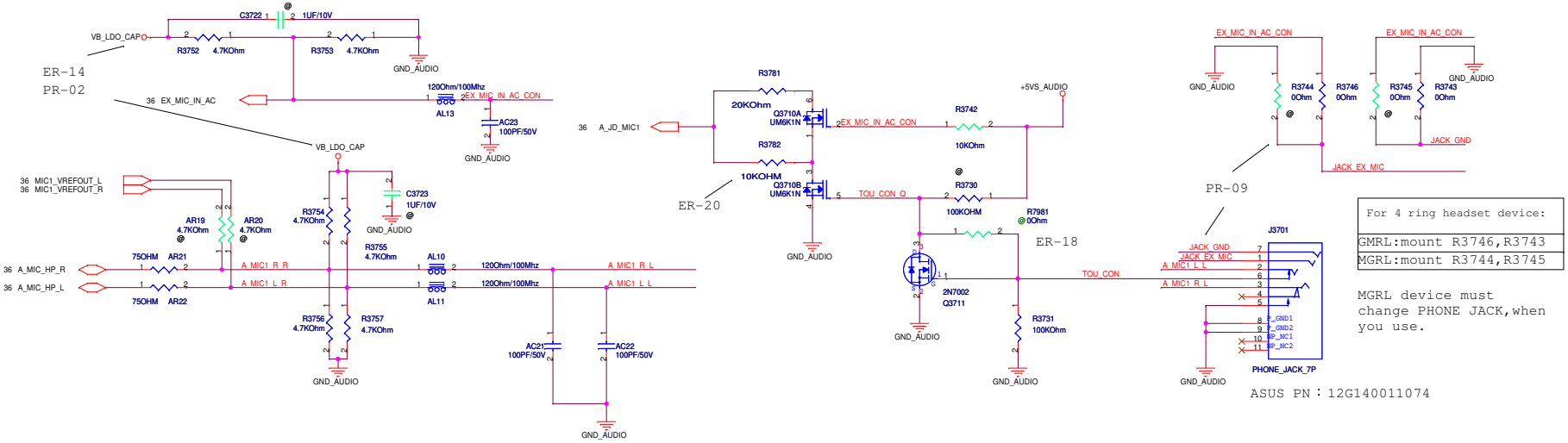
bypass Q3606,3607
AC_MIC_HP_R 0Ohm R3628 @ AC_MIC_HP_R_Q
AC_MIC_HP_L 0Ohm R3629 @ AC_MIC_HP_L_Q
Option 2

<Variant Name>
ASUSTeK COMPUTER INC. NB2
Title : CODEC ALC 269
Engineer: JAY_TSAI
Size C | Project Name K42Jv | Rev 1.01
Date: Thursday, February 11, 2010 | Sheet 36 of 96

SPEAKER



HP and MIC

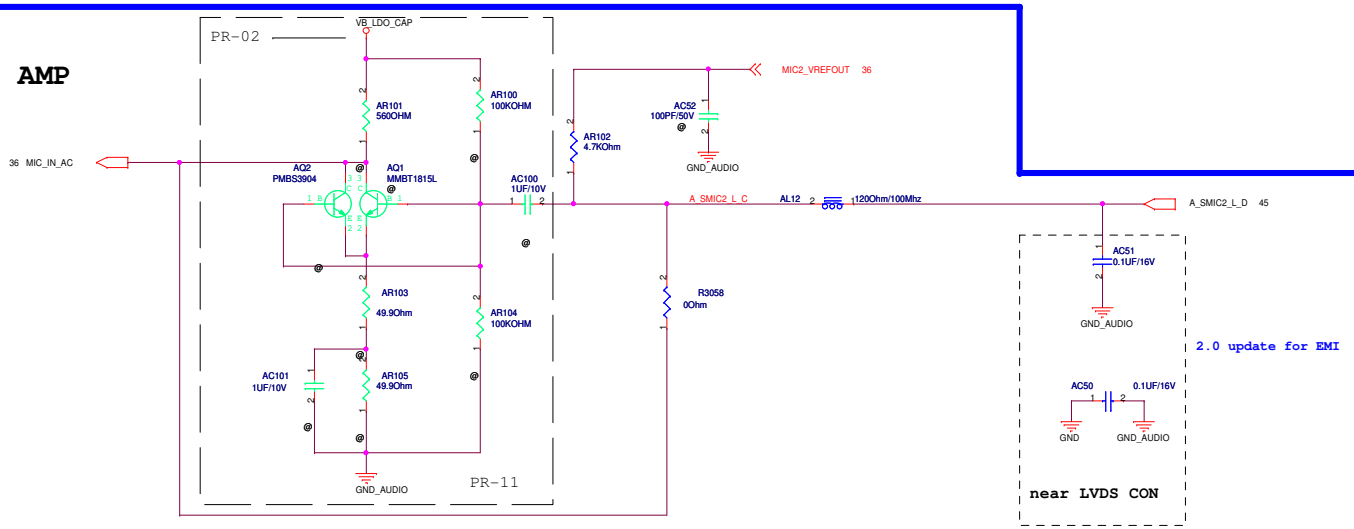


For 4 ring headset device:
GMRL:mount R3746,R3743
MGRL:mount R3744,R3745

MGRL device must change PHONE JACK,when you use.

ASUS PN：12G140011074

Internal MIC and AMP



ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 37 of 96		

ASUSTeK COMPUTER INC. NB4	Title :	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 38 of 96	

ASUSTeK COMPUTER INC. NB4	Title : AUD_****		
	Engineer: JAY_TSAI		
Size: Custom	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 39 of 96		

<Variant Name>

ASUSTek Computer Inc.	Title : ***	
	Engineer: JAY_TSAI	
Size: A3	Project Name: K42Jv	Rev: 1.0G
Date: Thursday, February 11, 2010	Sheet 40 of 96	

Reference Resistance

LAN_REXT — R3301 12KOhm — GND

D3E Enable/Disable

R3309	R3308	D3E
Unmount	Mount	Enable
Mount	Unmount	Disable

+VDDIO — R3309 0Ohm @ — 0Ohm R3308 — BUF_PLT_RST# — LAN_MPD

U3301 JMC251-V10

+VDD33, +1.2V_DVDD, GND

LAN_REXT, LANXIN, LANXOUT, LAN_LX, LAN_FB12

21 PCH_C_LAN_N, 21 PCH_C_LAN_P

21 PCIE_TX_LAN_P, 21 PCIE_TX_LAN_N

21 PCIE_RX_LAN_N, 21 PCIE_RX_LAN_P

0.1UF/16V C3315, 0.1UF/16V C3316, LAN_TXN_JMC, LAN_TXP_JMC

3,24,30,32,50,53,71 BUF_PLT_RST#

22 PCIE_WAKE#

21 CLKREQ_GLAN#

LAN_MPD, LAN_SCL, MS_XD_DETECT#, SD_MMC_DETECT#

MDIO13/XDRB, LAN_SDA

L_TRIN3 53, L_TRIP3 53, L_TRIN2 53, L_TRDP2 53, L_TRDN1 53, L_TRDP1 53, L_TRDN0 53, L_TRDP0 53

LAN_LED1 T3302 TPC26T, LAN_LED0 T3301 TPC26T

SDD0, SDD1, SDD2, SDD3, SDCMD, JMSDCLK, SDWP

JMSDCLK

JMSDCLK — R3723 0Ohm — SDCLK; C3321 10PF/50V @ — GND

+CR_CARD_POWER / +CR_POWER_CON

+CR_CARD_POWER — F3301 0.35A/6V — +CR_POWER_CON

C3322 10UF/6.3V @, C3325 0.1UF/16V, C3324 0.1UF/16V — GND

SD_CON1 SD_SOCKET_9P

SDD2, SDD3, SDCMD, SDCLK, SDD0, SDD1

P_GND2, P_GND1, SDWP, SD_MMC_DETECT#

Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.

MPD / CLKP/CLKN

Normal Operation | Power Down | Normal Operation

MPD

CLKP/CLKN 100MHz | 100MHz

T>10us

BUF_PLT_RST#

BUF_PLT_RST# — C3320 0.1UF/16V — GND

Switch Regulator

LAN_FB12 — JP3302 0603 — +1.2V_DVDD

LAN_LX (>20mil) — L3301 4.7UH — (>20mil) +1.2V_DVDD

C3319 10UF/6.3V, C3317 0.1UF/16V, C3305 0.1UF/16V, C3303 0.1UF/16V — GND

Serial EEPROM

+VDD33 — C3323 0.1UF/10V @ — GND

U3302 AT24C08BN-SH-T: A0 A1 A2 GND, VCC WP SCL SDA

R3721 4.7KOhm @, R3722 4.7KOhm @ — LAN_SCL, LAN_SDA

+3VSUS / +VDD33

JP3301 0603

C3318 10UF/6.3V, C3301 0.1UF/16V, C3310 0.1UF/16V, C3308 0.1UF/16V, C3309 0.1UF/16V — GND

LANXIN / LANXOUT

X3301 25Mhz

C3312 27PF/50V, C3313 27PF/50V — GND

+VDD33 / +CR_POWER_CON

RN4143A SDCMD, RN4143B SDWP, RN4143C SD_MMC_DETECT#, RN4143D MS_XD_DETECT#

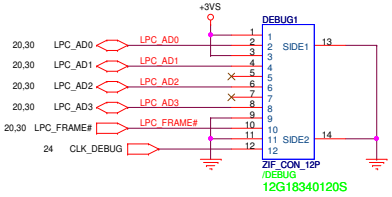
R3306 1KOhm — MDIO13/XDRB

Title : LAN-JMC251		
ASUSTeK COMPUTER INC. NB4	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.3
Date: Thursday, February 11, 2010	Sheet 41 of 99	

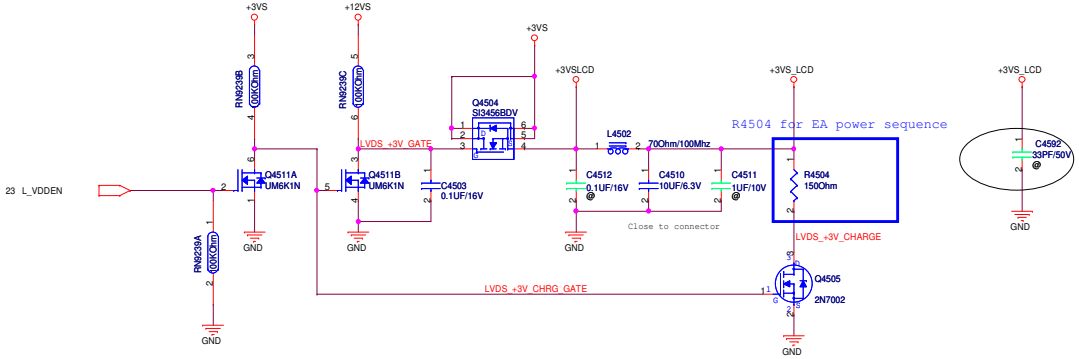
ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: JAY_TSAI	
Size: Custom	Project Name: K42Jv	Rev: 1.3
Date: Thursday, February 11, 2010	Sheet 42 of 99	

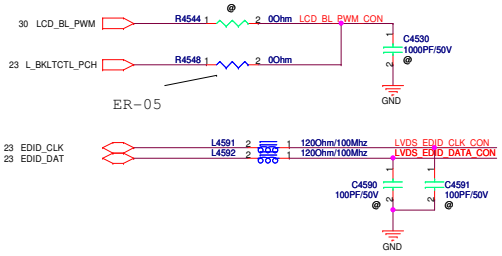
ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 43 of 96	

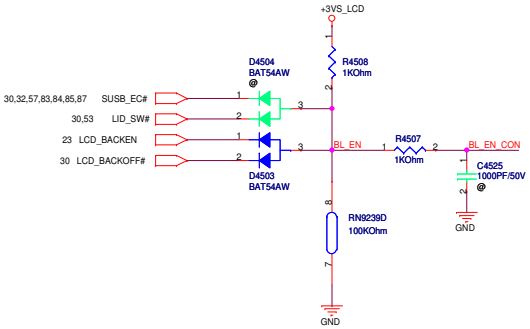
LPC Debug Port

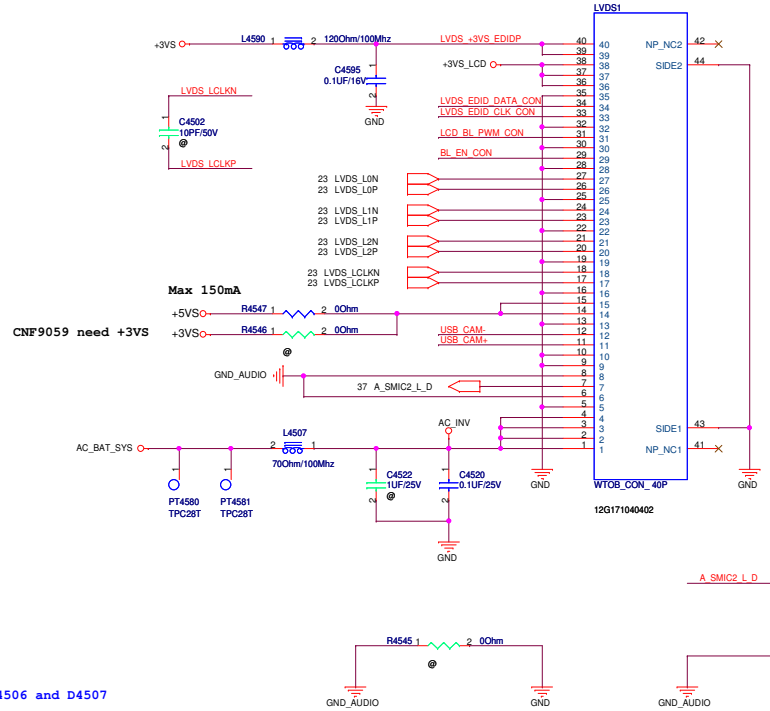


ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 44 of 96	

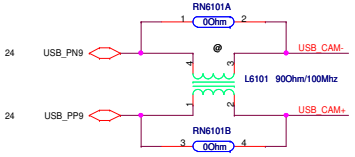




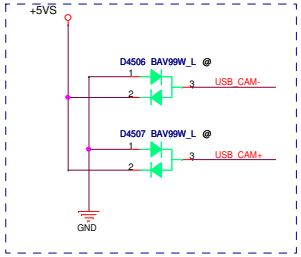




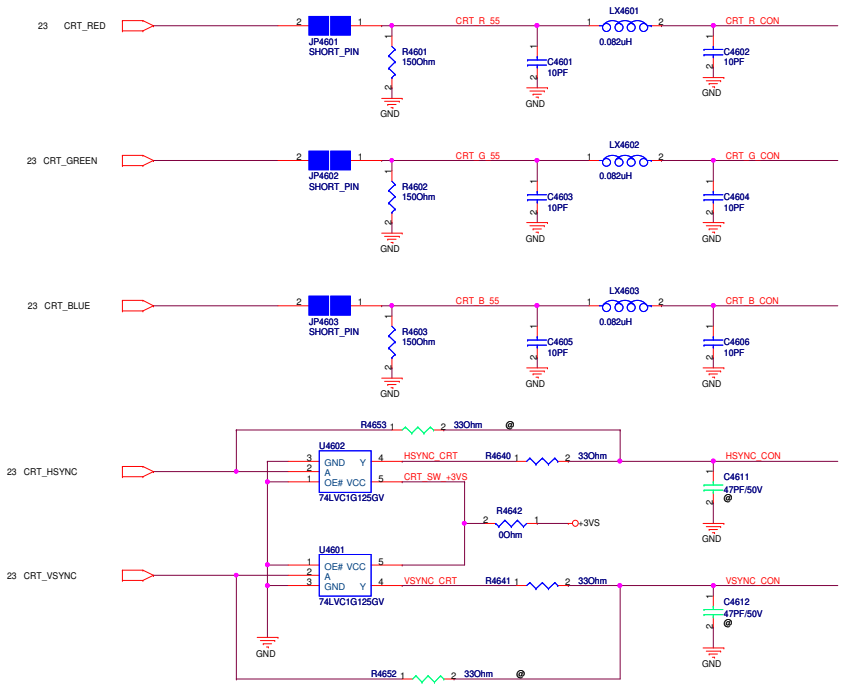
Camera USB

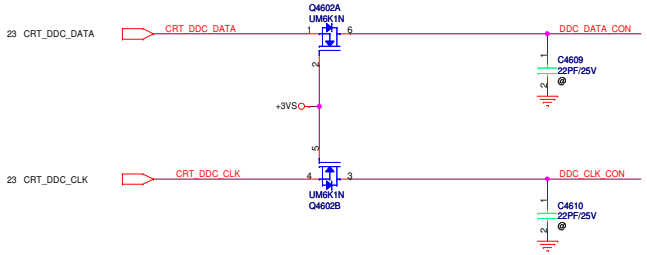


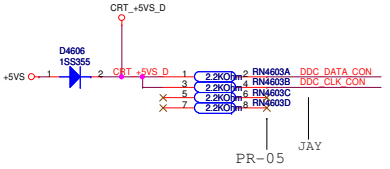
1.0 EMI test need mount D4506 and D4507

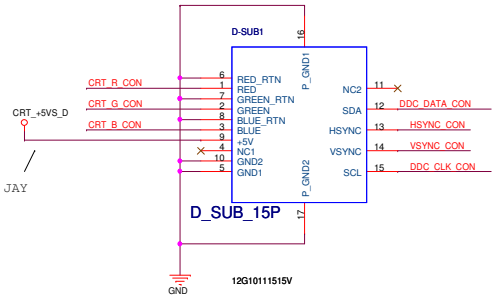


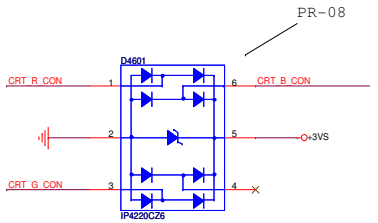
ASUSTeK COMPUTER INC. NB1	Title: LVDS & Inverter CON	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.00
Date: Thursday, February 11, 2010	Sheet 45 of 94	

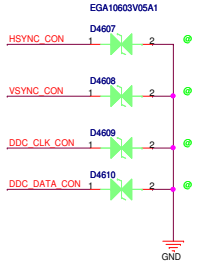






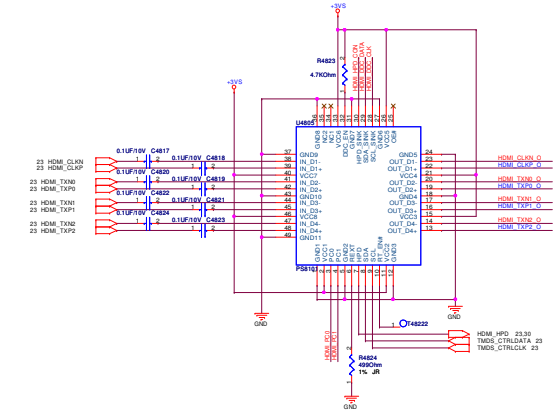


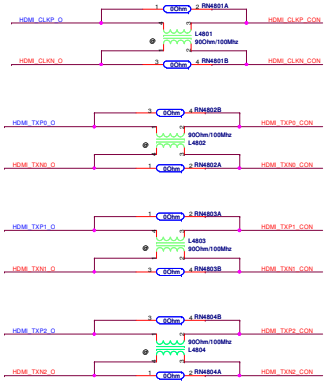


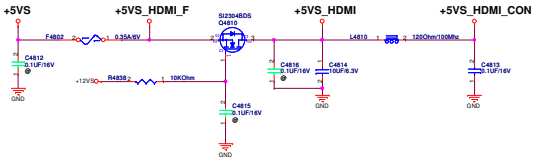


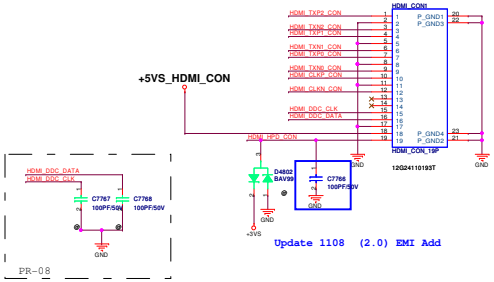
ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 46 of 96	

ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 47 of 96	

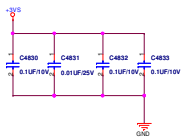


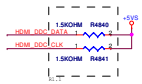


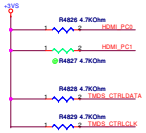




Update 1108 (2.0) EMI Add







ASUSTeK COMPUTER INC. NB4	Title : TV_HDMI	
	Engineer: JAY_TSAI	
Size: D	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 48 of 96	

Main Board

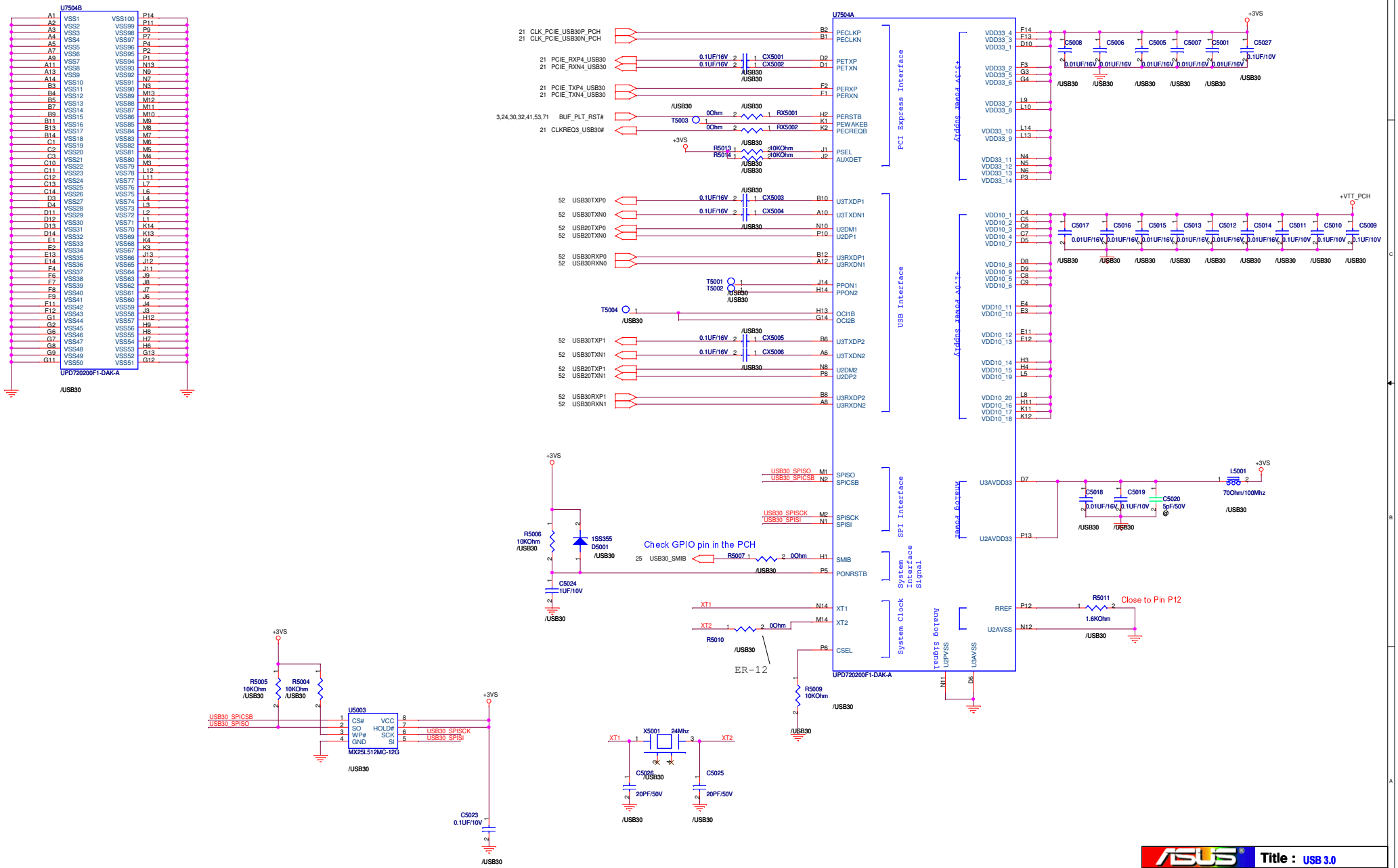
Title : TV_****

ASUSTeK COMPUTER INC. NB4

Engineer: JAY_TSAI

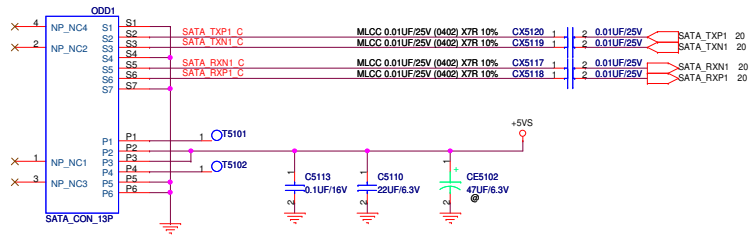
Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 49 of 96

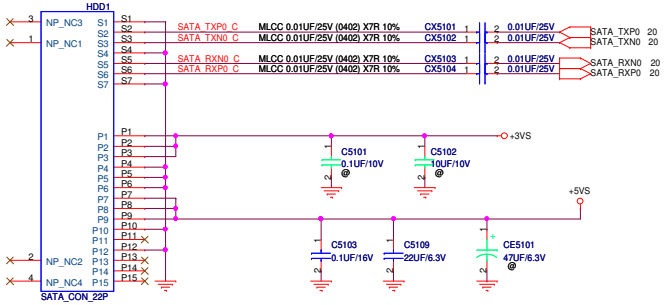


ASUSTeK COMPUTER INC. NB4	Title : USB 3.0		
	Engineer: Frank_Ma		
Size: C	Project Name: K42JV		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 50 of 96		

ODD



HDD (1st)



ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 51 of 96	

USB2.0 CON PN:12G131030042
Change USB PIN1234 to 4321

For USB3.0, change 3A fuse

ER-19

Combine power because these two ports are nearby.

USB ports

+5V
F5201 1.5A/6V
+5V_USB
L5201 70Ohm/100Mhz
+5V_USB_C
CE5203 47UF/6.3V
C5201 0.1UF/16V
R5201 47.5KOHM
24 USB_OC01#
R5203 82KOhm
GND
USB1
USB_P0-
USB_P0+
P_GND2
GND2
GND1
P_GND1
CE5204 47UF/6.3V
C5202 0.1UF/16V
USB2
USB_P2-
USB_P2+

ER-19

24 USB_PN0
USB_PN0_R
0Ohm RNX5201B
USB_P0-
LX5201 90Ohm/100Mhz
24 USB_PP0
USB_PP0_R
0Ohm RNX5201A
USB_P0+
50 USB20TXN0
R5205 0Ohm
50 USB20TXP0
R5206 0Ohm

PR-08

D5201
I/O4
I/O1
VDD
GND
I/O3
I/O2
AZC099-04S
+5V_USB_C

ER-19

24 USB_PN2
USB_PN2_R
0Ohm RNX5202A
USB_P2-
LX5202 90Ohm/100Mhz
24 USB_PP2
USB_PP2_R
0Ohm RNX5202B
USB_P2+
50 USB20TXN1
R5209 0Ohm
50 USB20TXP1
R5210 0Ohm

U5201
USB30TXP0
USB30TXN0
USB30RXP0
USB30RXN0
I/O1
I/O2
I/O3
I/O4
VDD
GND
I/O6
I/O5
AZ1065-06Q
+5V_USB
USB_P0+
USB_P0-

U7506
USB30TXP1
USB30TXN1
USB30RXP1
USB30RXN1
AZ1065-06Q
USB_P2+
USB_P2-

50 USB30RXN0
50 USB30RXP0
USB30RXN0
USB30RXP0
50 USB30TXP0
50 USB30TXN0
USB30TXP0
USB30TXN0

50 USB30RXN1
50 USB30RXP1
USB30RXN1
USB30RXP1
50 USB30TXP1
50 USB30TXN1
USB30TXP1
USB30TXN1

ASUSTeK COMPUTER INC. NB4

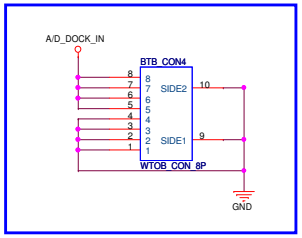
Title : USB_USB Port *2

Engineer: Frank_Ma

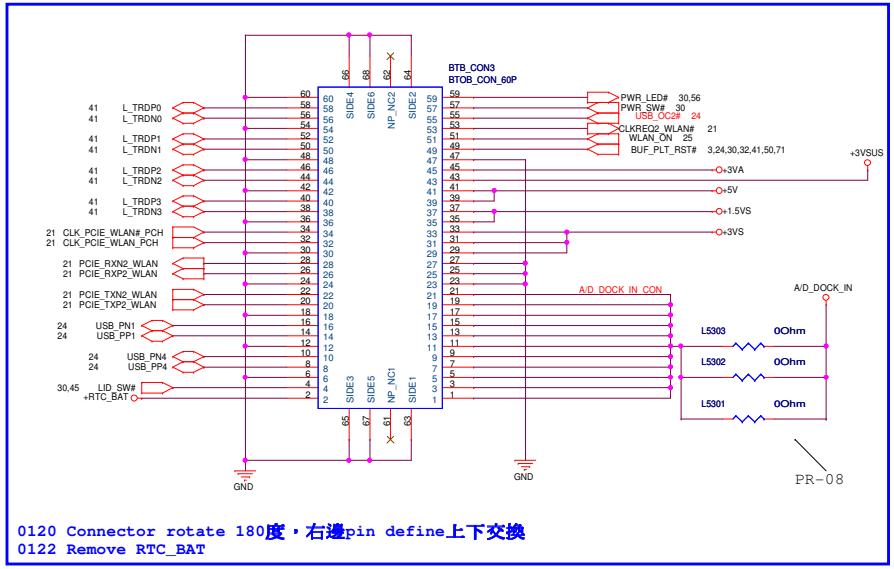
Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 52 of 96

0125 Add 8 pin WtoB connector



PR-07

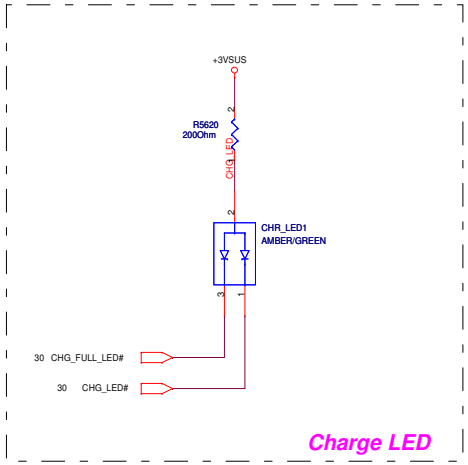


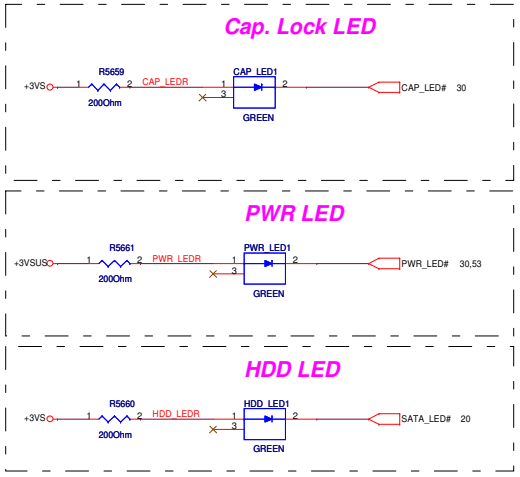
0120 Connector rotate 180度，右邊pin define上下交換
0122 Remove RTC_BAT

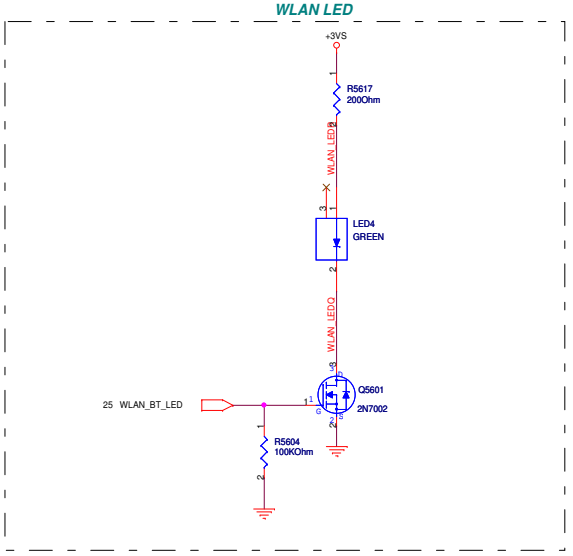
ASUSTeK COMPUTER INC. NB6		Title : B TO B	
		Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010		Sheet 53 of 96	

ASUSTeK COMPUTER INC. NB4	Title : BAR_****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 54 of 96		

ASUSTeK COMPUTER INC. NB4	Title : SIO_****		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 55 of 96		





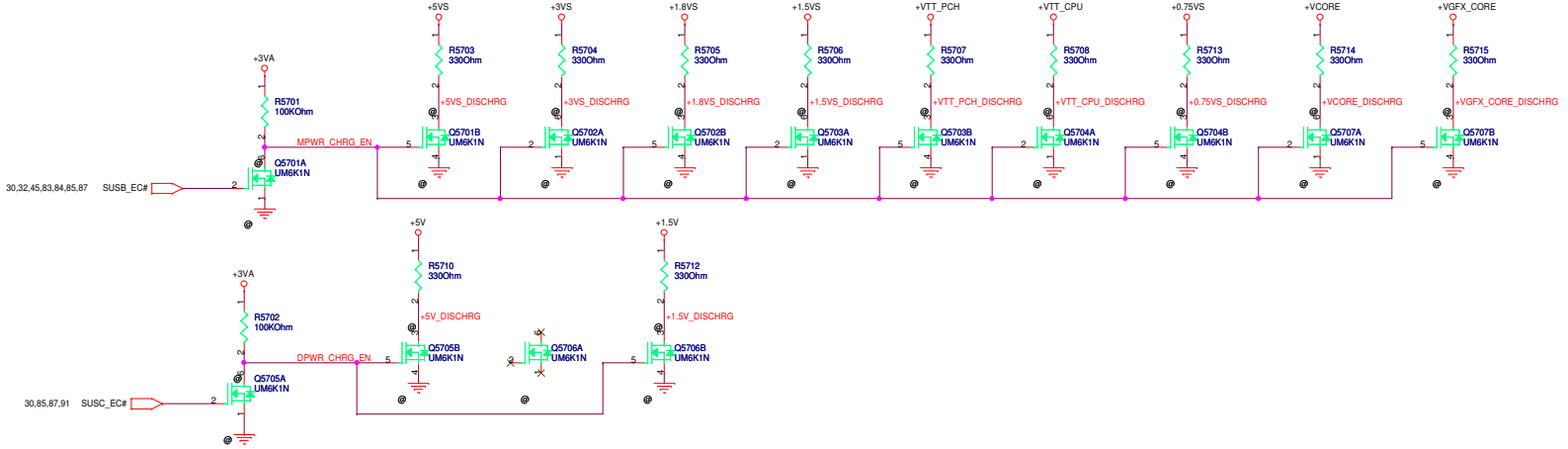


Change LED part number

ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 56 of 96	

Main Board

Remove +2.5Vs is for DIS GFX

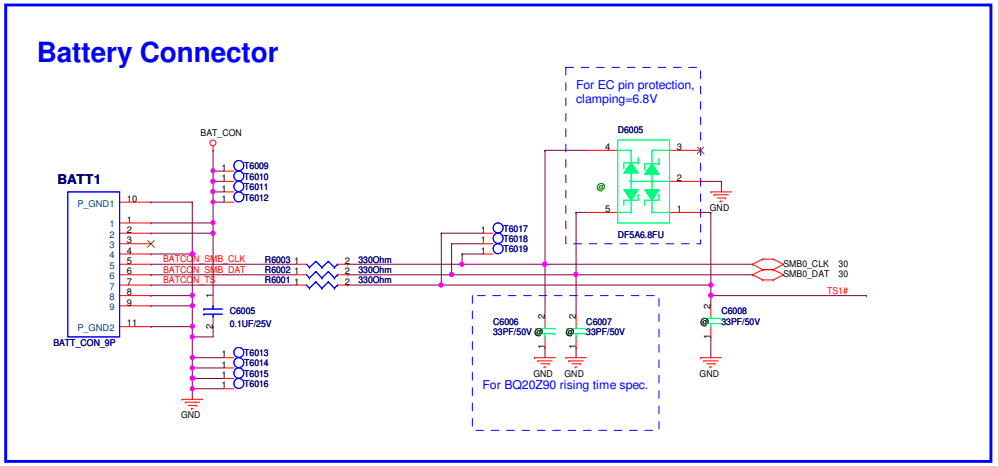


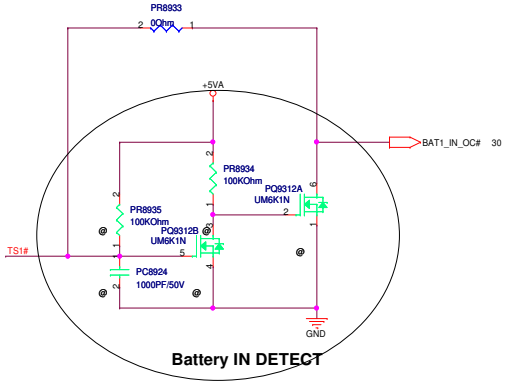
ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 57 of 96	

ASUSTeK COMPUTER INC. NB4	Title : PCI_****	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 58 of 96	

ASUSTeK COMPUTER INC. NB4	Title : DJ_****	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 59 of 96	

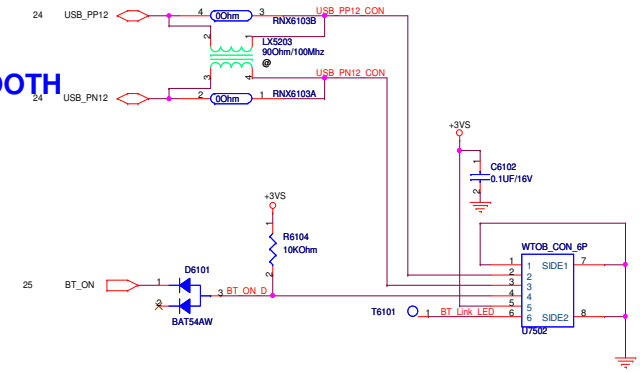
Battery Connector





ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 60 of 96	

BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 61 of 96		

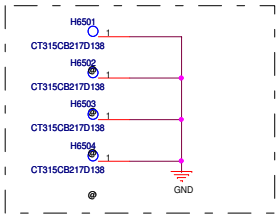
ASUSTeK COMPUTER INC. NB4	Title : TPM_****	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 62 of 96	

Main Board

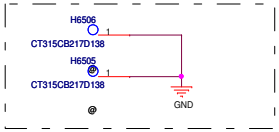
ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 63 of 96	

ASUSTeK COMPUTER INC. NB4	Title : ***		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 64 of 96		

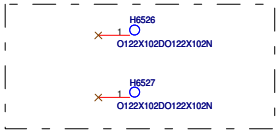
For CPU



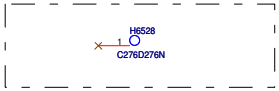
For GPU

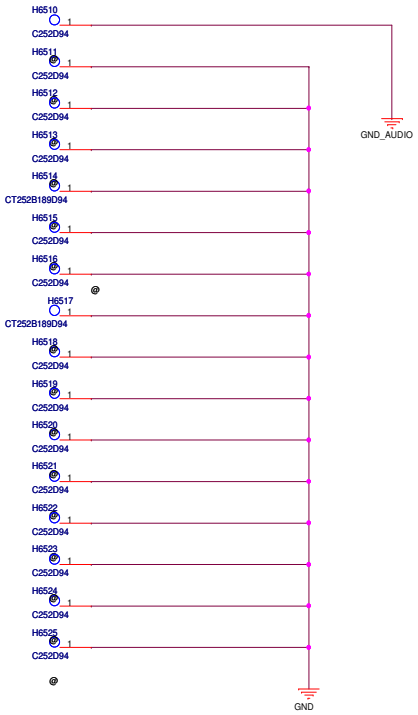


For 橢圓定位孔

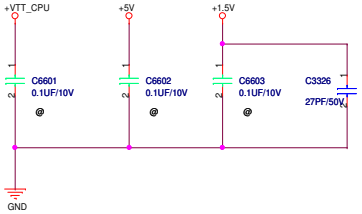


HHD 呼吸孔





ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 65 of 96	



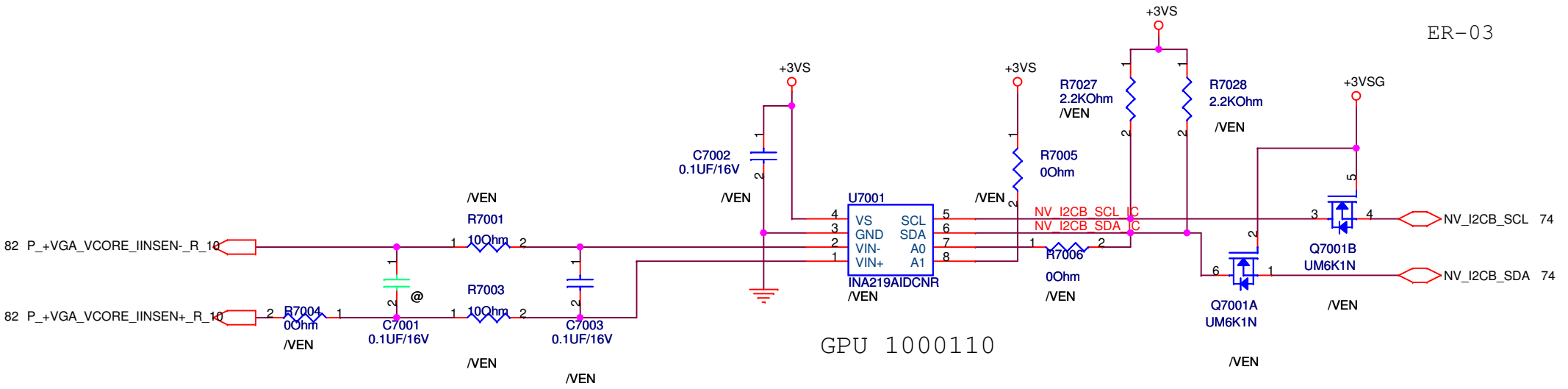
ASUSTeK COMPUTER INC. NB4	Title : EMI	
	Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 66 of 96	

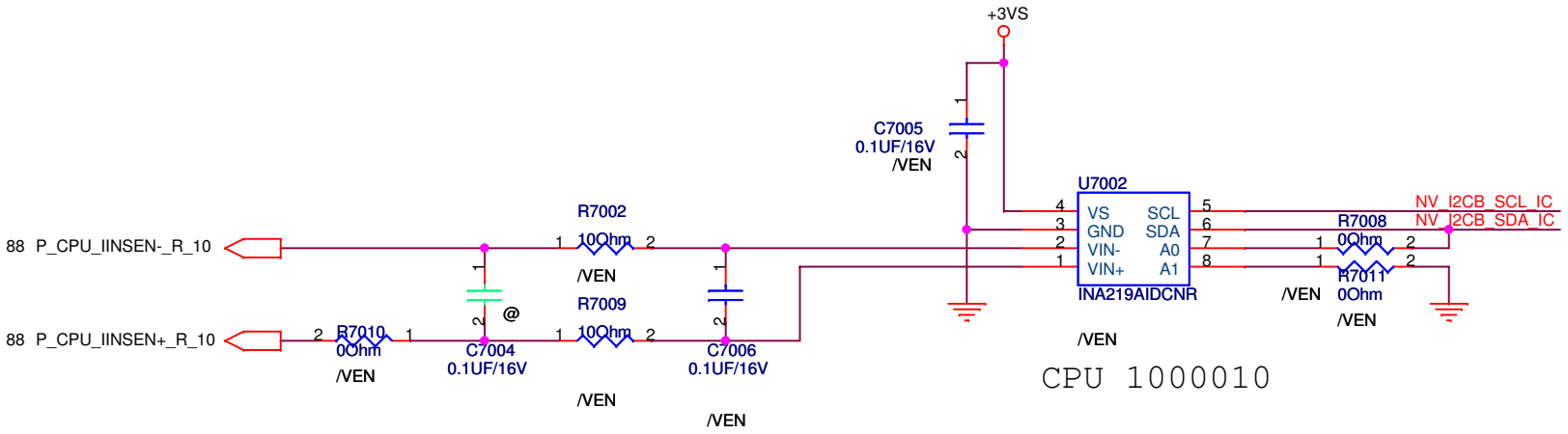
ASUSTeK COMPUTER INC. NB4	Title : ***		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 67 of 96		

ASUSTeK COMPUTER INC. NB4	Title : OTH_LCM		
	Engineer: JAY_TSAI		
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 68 of 96		

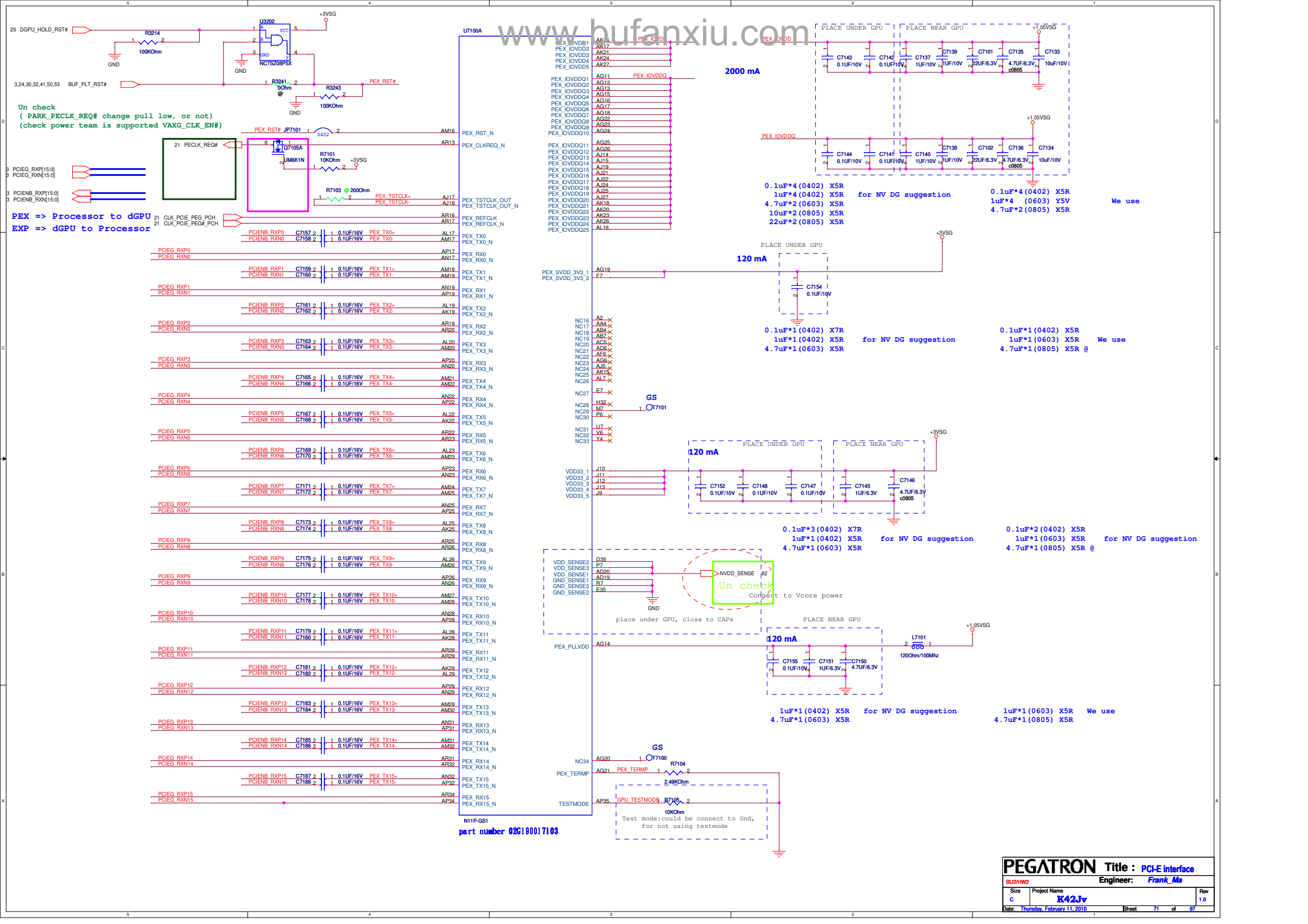
ASUSTeK COMPUTER INC. NB4		Title : OTH_GAME-LED*****	
		Engineer: JAY_TSAI	
Size: C	Project Name: K42Jv		Rev: 1.01
Date: Thursday, February 11, 2010		Sheet 69 of 96	

ER-03

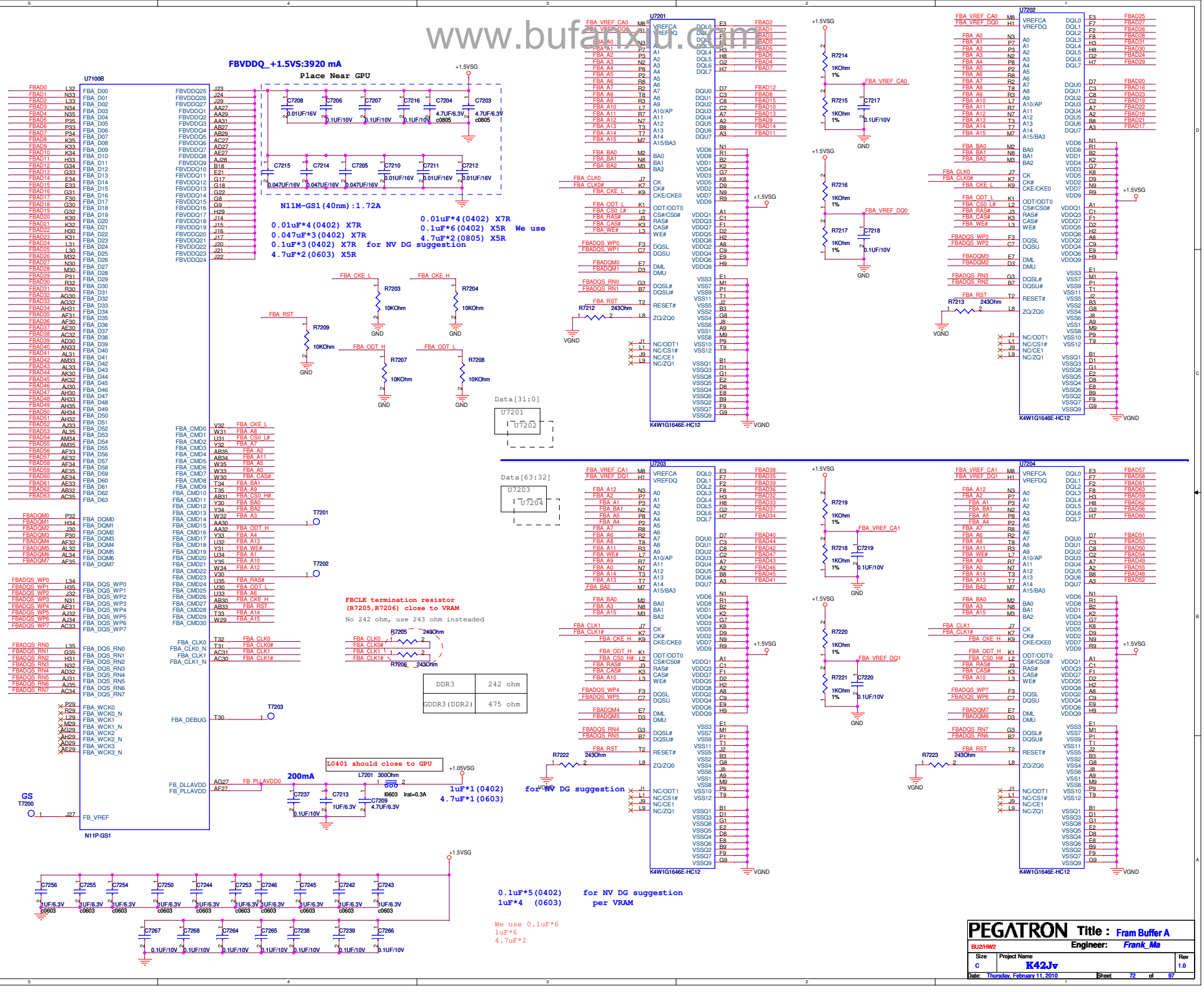


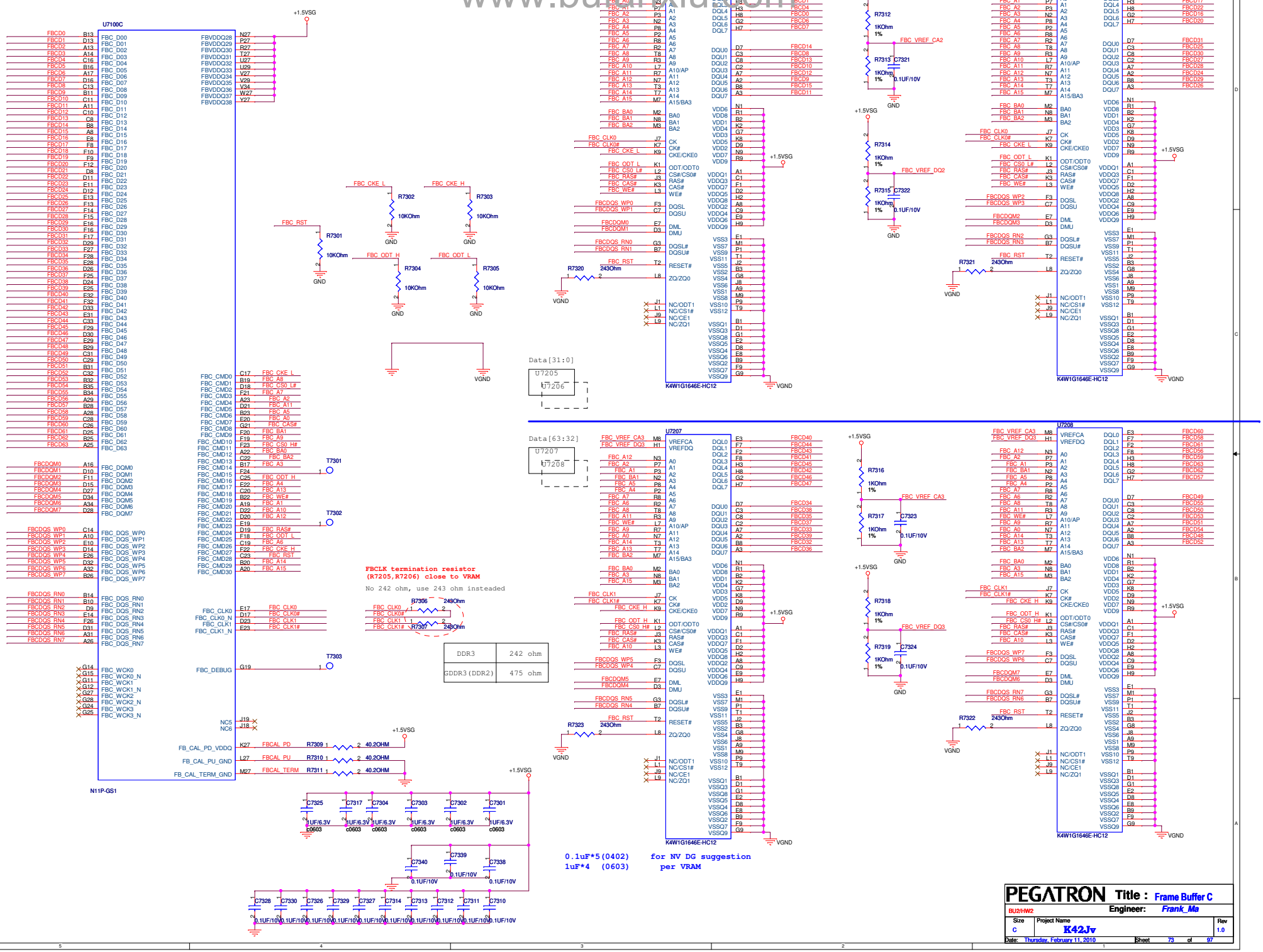


ASUSTeK COMPUTER INC. NB4	Title : VENTURA	
	Engineer: JAY_TSAI	
Size: A4	Project Name: K42JV	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 70 of 96	



PEGATRON	Title : PCI-E interface		
BU2/HW2	Engineer: Frank_Ma		
Size: C	Project Name: K42Jv	Rev: 1.0	
Date: Thursday, February 11, 2010	Sheet 71 of 97		



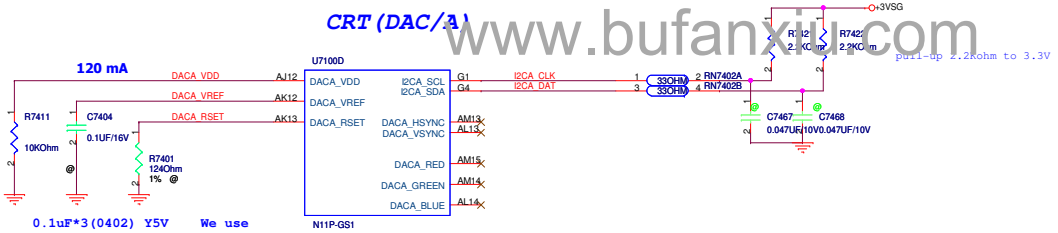


DDR3	242 ohm
GDDR3(DDR2)	475 ohm

0.1uF*5(0402) for NV DG suggestion
1uF*4 (0603) per VRAM

PEGATRON	Title : Frame Buffer C		
BU2/HW2	Engineer: Frank_Ma		
Size: C	Project Name: K42Jv		Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 73 of 97		

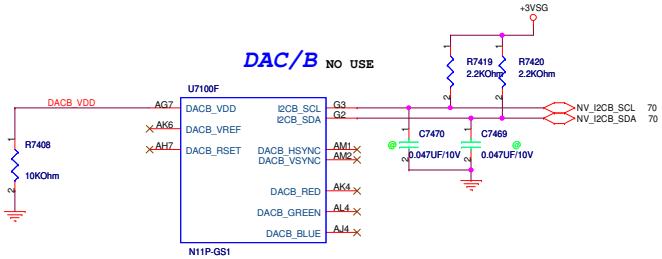
CRT (DAC/A)

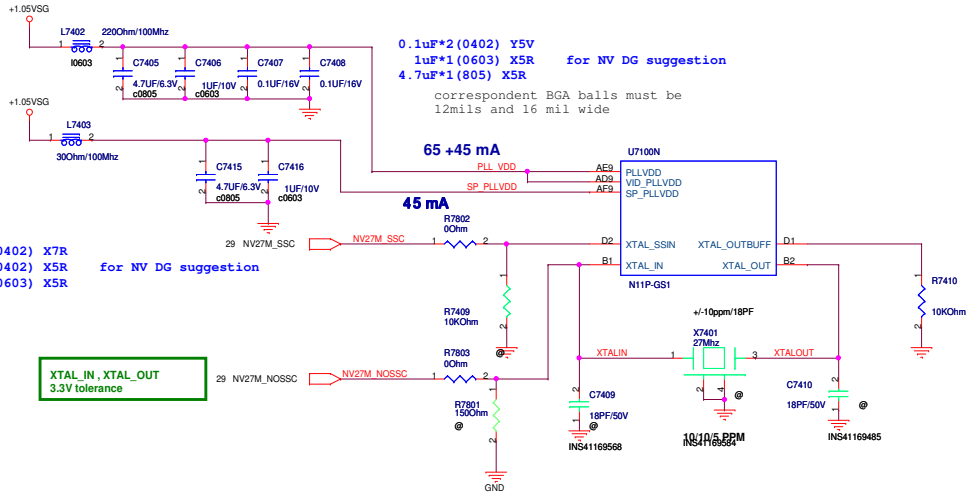


470pF*1(0402) X7R
4700pF*1(0402) X7R
100nF*3(0402) X7R for NV DG suggestion
1uF*1(0402) X5R
4.7uF*1(0603) X5R

0.1uF*3(0402) Y5V We use
4.7uF*1(0805) X5R

DAC/B NO USE





0.1uF*2(0402) Y5V
1uF*1(0603) X5R for NV DG suggestion
4.7uF*1(805) X5R

correspondent BGA balls must be
12mils and 16 mil wide

0.1uF*2(0402) X7R
1uF*2(0402) X5R for NV DG suggestion
4.7uF*2(0603) X5R

XTAL_IN , XTAL_OUT
3.3V tolerance

Option /SSC and /XTAL unmount

Ask to FAE if necessary or not

PEGATRON	Title : DACs, CLK GEN	
BU2/HW2	Engineer: Frank_Ma	
Size: C	Project Name: K42Jv	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 74 of 97	

GPU	IFP A	IFP B	IFP C	IFP D
GB1-128	LVDS (Single Link)	LVDS (Dual Link)	HDMI	DisplayPort (unused)

LVDS (IFPAB)

U7100G

220 mA

R7501 1KOhm @
R7525 10KOhm

220 mA

R7524 10KOhm

IFPA_TXD0_N, IFPA_TXD0, IFPA_TXD1_N, IFPA_TXD1, IFPA_TXD2_N, IFPA_TXD2, IFPA_TXD3_N, IFPA_TXD3, IFPA_TXC_N, IFPA_TXC, IFPB_TXD4_N, IFPB_TXD4, IFPB_TXD5_N, IFPB_TXD5, IFPB_TXD6_N, IFPB_TXD6, IFPB_TXD7_N, IFPB_TXD7, IFPB_TXC_N, IFPB_TXC

IFPAB_PLLVDD, IFPAB_RSET, IFPA_IOVDD, IFPB_IOVDD, GPIO0

T7525

N11P-GS1

0.1uF*2(0402) for NV DG suggestion
1uF*1(0402)
4.7uF*1(0603)

Follow K42Jr and NV pull up 4.7k ohm to 3.3 (please chenk page 49)

HDMI (IFPC)

U7100H

285 mA

R7522 10KOhm
R7502 1KOhm @

220 mA

R7523 10KOhm

IFPC_PLLVDD, IFPC_RSET, IFPC_AUX_I2CW_SDA_N, IFPC_AUX_I2CW_SCL, IFPC_L3_N, IFPC_L3, IFPC_L2_N, IFPC_L2, IFPC_L1_N, IFPC_L1, IFPC_L0_N, IFPC_L0, IFPC_IOVDD, GPIO1

IFPC_AUX#, IFPC_AUX

+3VSG

Reserved for pull-up 2.2Kohm to 3.3V

R7520 2.2KOhm @
R7521 2.2KOhm @

C7567 @ 0.047UF/10V
C7568 @ 0.047UF/10V

ER-17

T7526

N11P-GS1

0.1uF*2(0402) for NV DG suggestion
1uF*1(0402)
4.7uF*1(0603)

DP (IFPD)

U7100E

R7518 10KOhm
R7519 10KOhm

GND

IFPD_PLLVDD, IFPD_RSET, IFPD_AUX_I2CX_SDA_N, IFPD_AUX_I2CX_SCL, IFPD_L3_N, IFPD_L3, IFPD_L2_N, IFPD_L2, IFPD_L1_N, IFPD_L1, IFPD_L0_N, IFPD_L0, IFPD_IOVDD, GPIO19

N11P-GS1

IFPEF is unused

U7100I

R7504 10KOhm
R7505 10KOhm

GND

IFPE_AUX_I2CY_SDA_N, IFPE_AUX_I2CY_SCL, IFPE_L3_N, IFPE_L3, IFPE_L2_N, IFPE_L2, IFPE_L1_N, IFPE_L1, IFPE_L0_N, IFPE_L0, GPIO15

IFPEF_PLLVDD, IFPEF_RSET, IFPE_IOVDD, IFPF_AUX_I2CZ_SDA_N, IFPF_AUX_I2CZ_SCL, IFPF_IOVDD, IFPF_L3_N, IFPF_L3, IFPF_L2_N, IFPF_L2, IFPF_L1_N, IFPF_L1, IFPF_L0_N, IFPF_L0, GPIO21

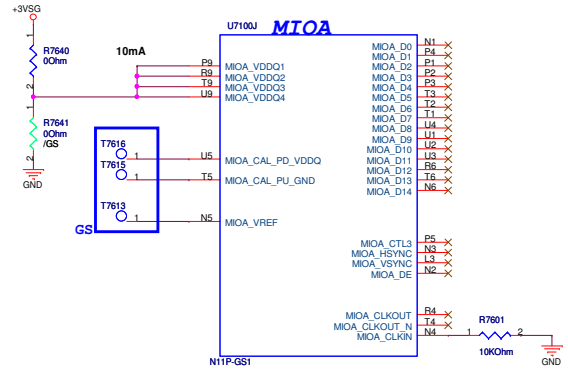
N11P-GS1

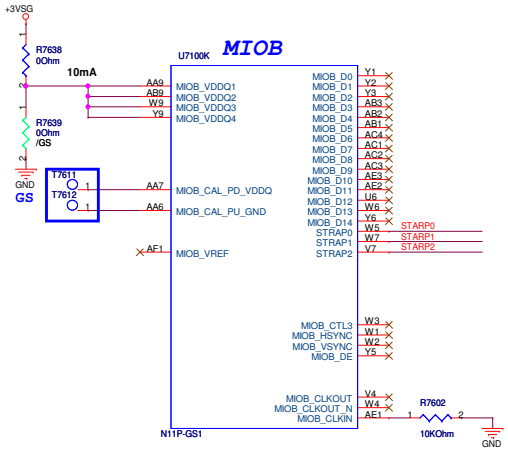
PEGATRON Title : LVDS/HDMI/DP

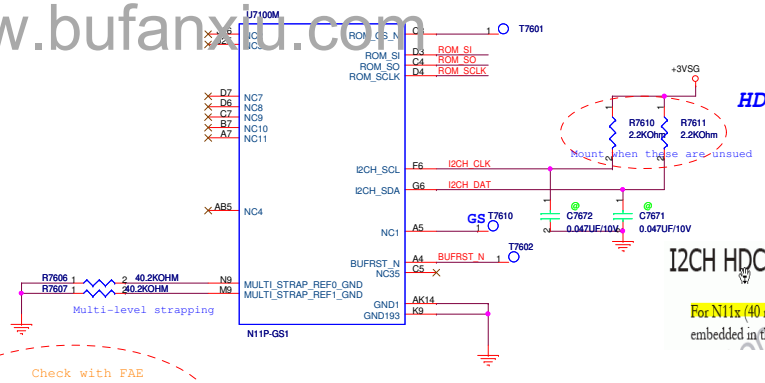
BU2/HW2 Engineer: Frank_Ma

Size	Project Name	Rev
C	K42Jv	1.0

Date: Thursday, February 11, 2010 Sheet 75 of 97







I2CH HDCP Interface

For N11x (40 nm), an external HDCP ROM is not required. HDCP functionality is embedded in the GPU. External connections are not required to support HDCP.

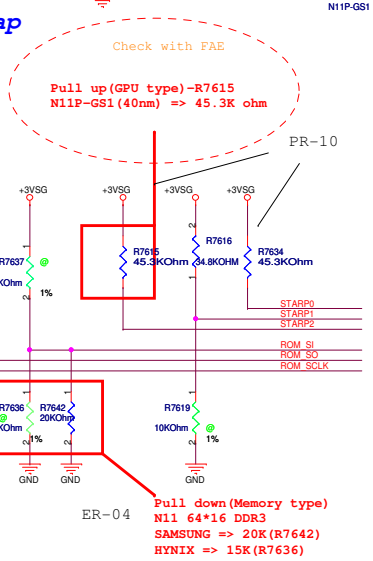
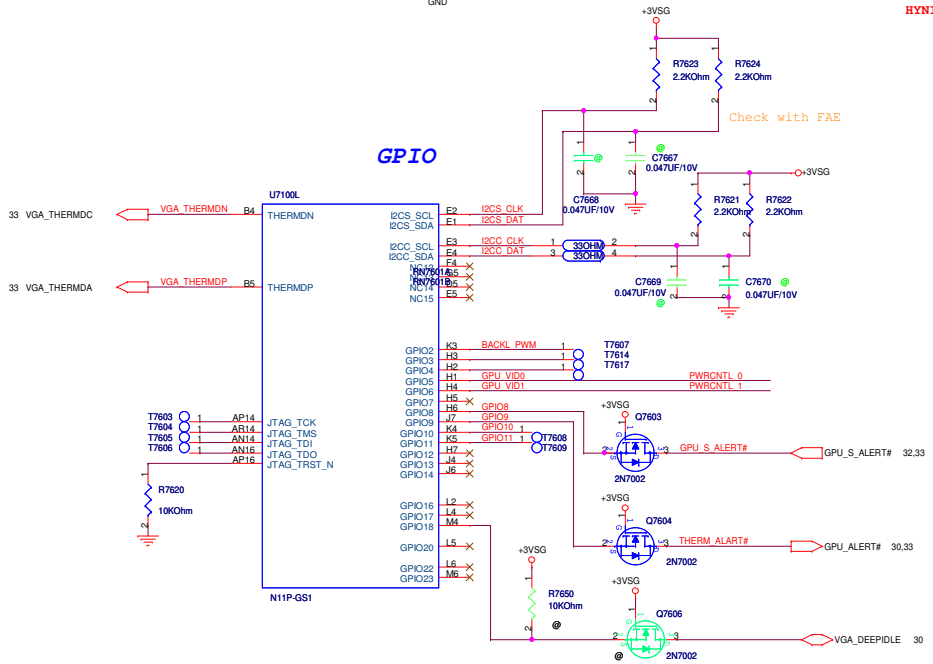
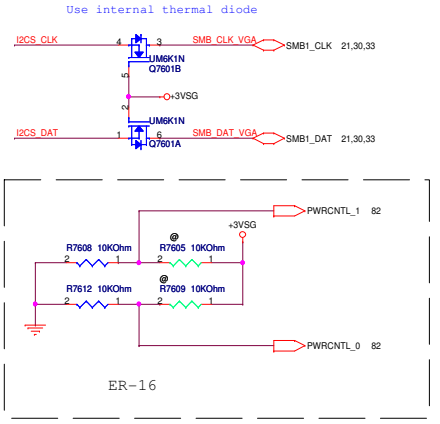


Table 13-5. Multilevel Strapping Options

Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]





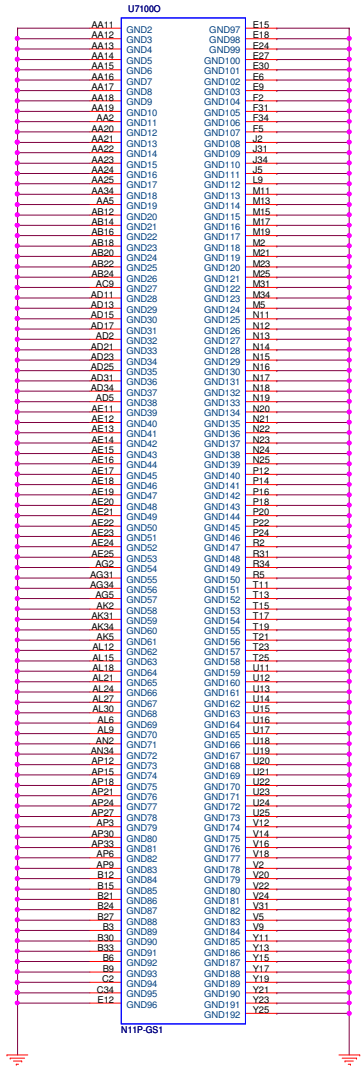
I2C ASSIGNMENTS

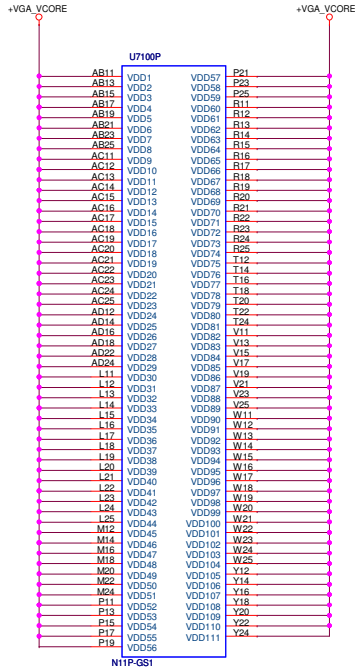
I2CA: CRT --3V
I2CB: N/A
I2CC: LVDS(EDID)
I2CS: Slave for GPU internal thermal
I2CH: HDCP
IFPC_AUX_I2CW: HDMI --3 V
IFPD_AUX_I2CX: DP --3 V
IFPE_AUX_I2CY: N/A
IFPF_AUX_I2CZ: N/A

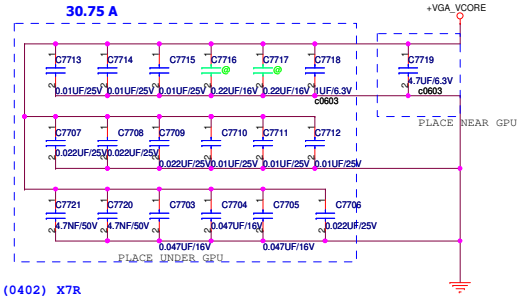
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	n/a	n/a	p.75
1	IN	-	IFPC HPD-C (HDMI) p.75
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	-	NVVDD VID 0
6	OUT	-	NVVDD VID 1
7	OUT	-	NVVDD VID 2
8	I/O	LOW	OVERT
9	I/O	LOW	THERMAL ALERT
10	OUT		Memory VREF switch
11	I/O	LOW	SLI raster sync
12	IN	-	AC DETECT
13	OUT	-	MEM_VID
14	OUT	-	PWR_CRT1
15	IN	-	IFPE HPD-E
16	OUT	-	FAN_PWM
17	IN	-	Reserved
18	IN	-	Reserved
19	IN	-	IFPD HPD-D (DP) P.75
20	IN	-	Reserved
21	IN	-	IFPF HPD-F
22	IN	-	SLI swap ready signal
23	I/O		

PEGATRON Title : Strap, GPIO
BU2/HW2 Engineer: Frank_Ma
Size C | Project Name K42Jv | Rev 1.0
Date: Thursday, February 11, 2010 | Sheet 76 of 97








```
4700pF*2   (0402) X7R
0.01uF*6   (0402) X7R
0.022uF*4  (0402) X7R
0.047uF*3  (0402) X7R    for NV DG suggestion
0.22uF*2   (0603) X7R
1uF*1      (0603) X5R
4.7uF*1    (0603) X5R

0.1uF*15   (0402) X5R
0.22uF*2   (0603) X7R @      We use
1uF*1      (0603) X5R
4.7uF*1    (0603) X5R
```

PEGATRON	Title : PWR&GND		
BU2/HW2	Engineer: Frank_Ma		
Size: C	Project Name: K42Jv		Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 77 of 97		

ER Modify list:

ER-01 : For VTT Power adjustable and DRAM power fix

ER-02 : Exchange PIN 2 and PIN 3 connection and Power rail chagne from +3VS to +5VS.

ER-03 : Add /Ven lable for Ventura option.

ER-04 : According GPU strap define setting to P.D.

ER-05 : LCD backlight control change to accord DESIGN IP.

ER-06 : Change R2404 to 33OHM for EA measurement.

ER-07 : Unmount External thermal sensor change to use DGPU internal thermal sensor.

ER-08 : According for VTT power default setting.

ER-09 : To change from +1.8VSG to +1.5VSG.

ER-10 : PCB ID change from SR to ER setting.

ER-11 : ALC269 ver B. must add 10K P.U for PD# pin.

ER-12 : Modify Crystal Rd location and add /USB30 lable.

ER-13 : For Smart33 Down freq. and reserve over clock design.
R2933 mount 4.7K 0603 at ER stage.

ER-14 : Modify power rail to +5VS_AUDIO.

ER-15 : R3631 change from 10K to 0R.

ER-16 : Setting DGPU Vcore default power to 0.8V.

ER-17 : Unmount R7520,R7521 from vendor suggestion.

ER-18 : Reserve vendor solution add 0R for bypass other circuit.

ER-19 : Change USB port to 2.0 connector and design only for USB 2.0.

ER-20 : For line-in channel ,HP jack sensor must change to 10K.

ER-22 : To resolve "3622146 A Voltage Spike on Graphics Core Rail (Vaxg) to 1.5V seen during system shutdown"change from 4.7K to 470 OHM.

ER-23 : Follow Design IP,change to P.D.

ER-24 : Change mount for smart 33 control Vcore power.

For cost down and short jump ,Please search "C.D"

PR Modify list:

PR-01 : Change R2933 to 10K 0402.

PR-02 : Mic bias voltage change from +5VS_AUDIO to CODEC's PIN28(integreated regulator).To avoid MIC noise by drity power.

PR-03 : Change R3631 from 0R to short jump.

PR-04 : Add level shift circuit.

PR-05 : Del RN9250.

PR-06 : Add for pop and click sounds.

PR-07 : Change for B to B re-design.(copy from K42JC schematic)

PR-08 : EMI/ESD request.

PR-09 : Add MGRL of headset device design.

PR-10 : According to vendor suggestion.(45K change to 45.3K)

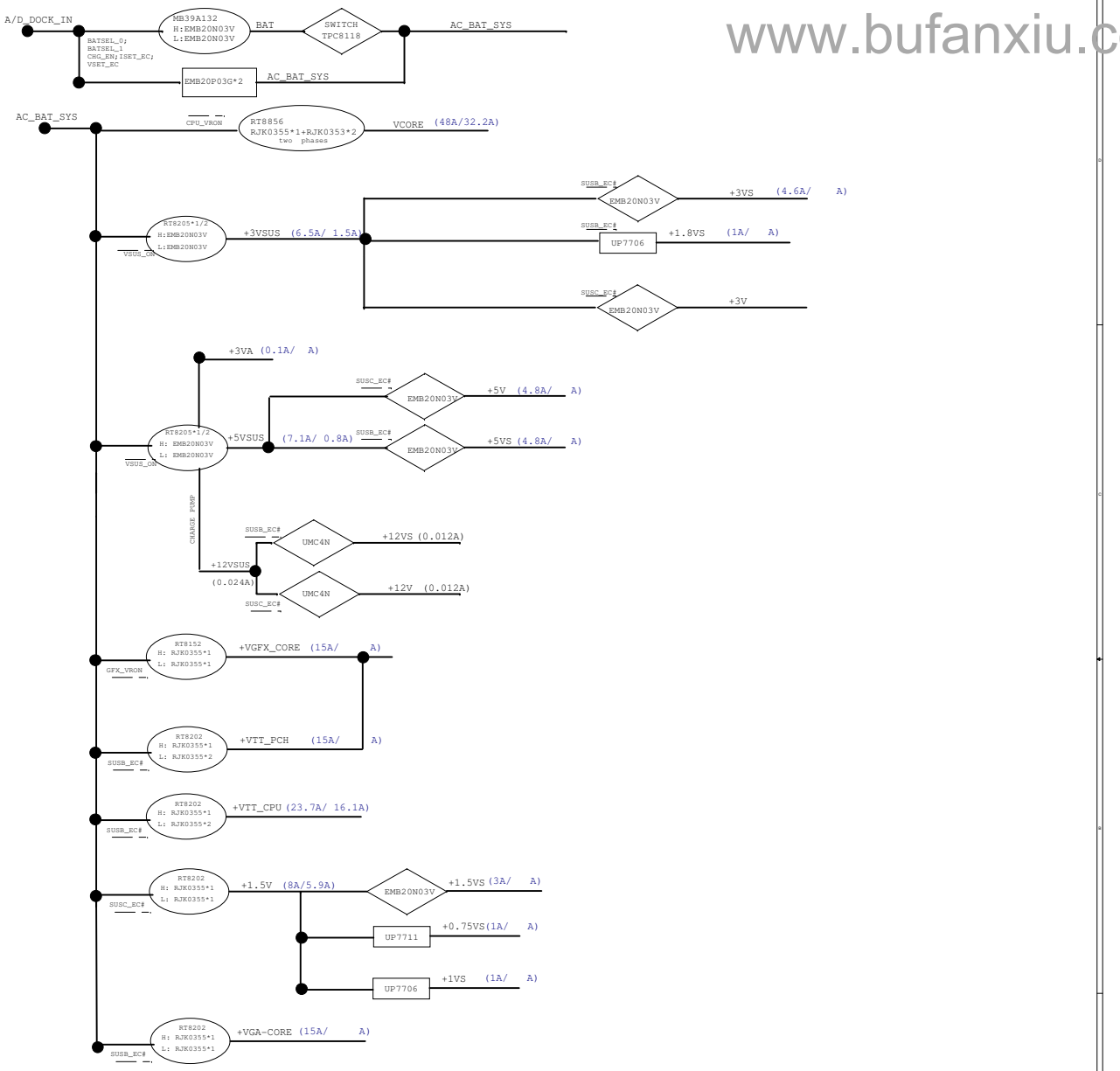
PR-11 : Bypass INT. MIC amplifier.

PR-12 : VTT,+1.5V,VCORE power set to default normal power rails.

PR-13 : Codec IC(ALC269) change from VB2 to VB5.

PR-14 : PCB ID change from ER to PR setting.

ASUSTeK COMPUTER INC. NB4	Title : ***	
	Engineer: Frank_Ma	
Size: C	Project Name: K42Jv	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 79 of 99	



<Variant Name>

ASUSTek Computer INC.

Title : Power_Flow

Engineer: ZHI-KUN_LIU

Size	Project Name	Rev
Custom	K80A	1.0

Date: Thursday, February 11, 2010 Sheet 80 of 79

Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.75A
2. Ripple Current:
   Irip=2.63A
3. Dynamic:
   Ipeak=5A
   ESR/1=15mohm
   V=75mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   H-side MOSFET: SI7326
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 6.5A (T =25 ℃)
   I peak =10 A (Pause =10 us)
   L-side MOSFET:7326
   Rds(ON)= 30mohm (Vgs=4.5 V)
   I cont = 6.5 A (T =25 ℃)
   I peak = 10 A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=0.8A
2. Ripple Current:
   Irip=1.13A
3. Dymamic:
   Ipeak=3.3A
   ESR/1=15mohm
   V=49.5mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm

Controller

+5VSUS:

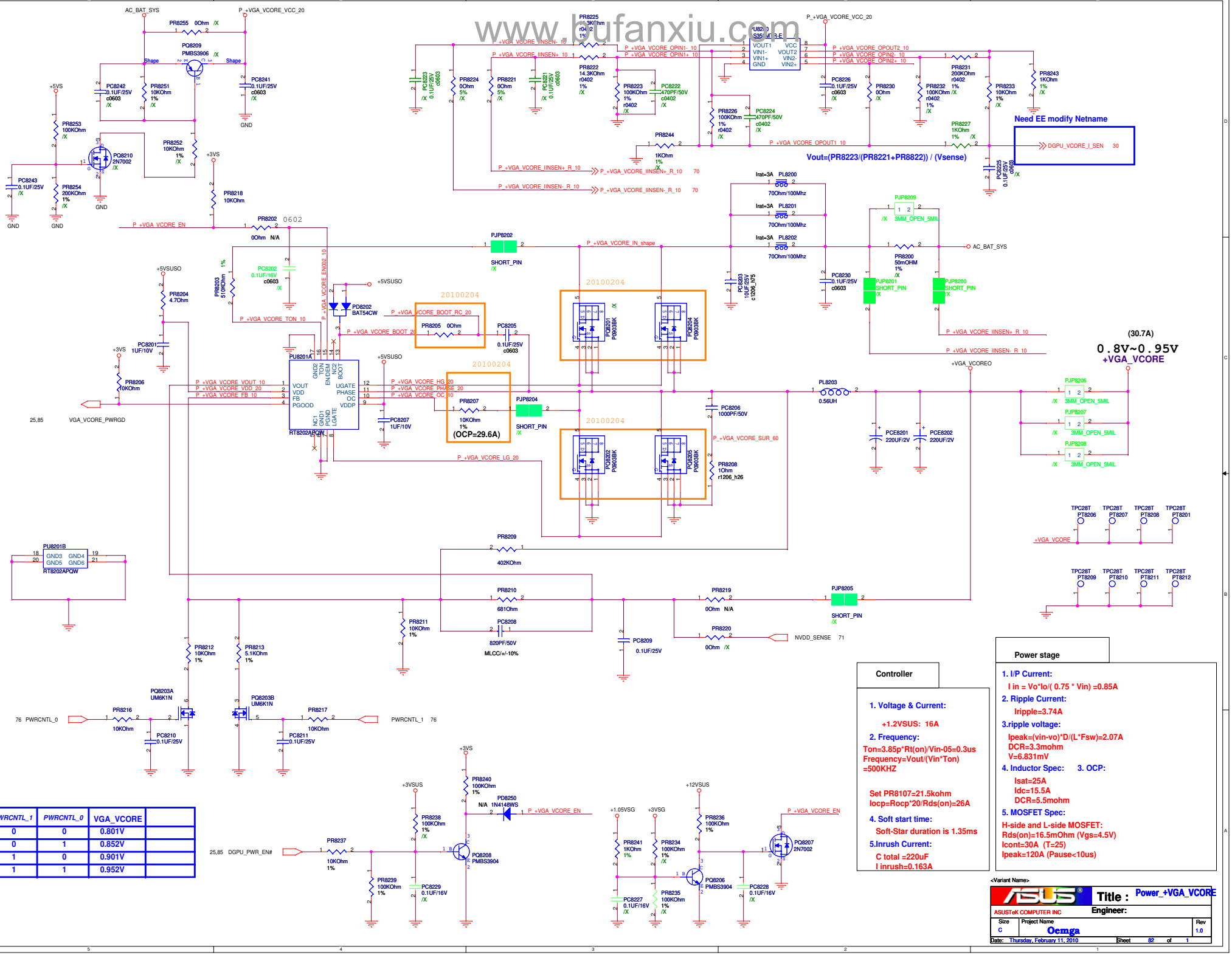
1. Voltage & Current:
   +5VSUS:5V&3A
2. Frequency:
   F=400KHZ
3. OCP:
   Set PR8701=200 Kohm
   Iocp=Rocp/Rds(on)*1000000=6.6A
4. Soft start time:
   The Soft Star duration is 2ms
5. Inrush Current:
   C total = 88 uF
   I inrush= 0.22 A

+3.VSUS

1. Voltage&Current:
   +3VSUS:3.3V&3A
2. Frequency:
   F=500KHZ
3. OCP:
   Set PR8703=200KOhm
   Iocp=Rocp/Rds(on)*1000000=6.6A
4. Inrush Current:
   Ctotal=66uF
   Iinrush=0.109A

+3VA / 100mA

<Variant Name>	Power_+5SUS&+3VSUS&+12VSUS
ASUSTek Computer INC.	Title :
	Engineer:
Size: A2	Project Name: K40AC
Rev: 1.0	
Date: Thursday, February 11, 2010	Sheet 81 of 1



PWRCNTL_1	PWRCNTL_0	VGA_VCORE	
0	0	0.801V	
0	1	0.852V	
1	0	0.901V	
1	1	0.952V	

Controller

1. Voltage & Current:
   +1.2VSUS: 16A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ

   Set PR8107=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=3.74A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV
4. Inductor Spec:
5. OCP:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
6. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

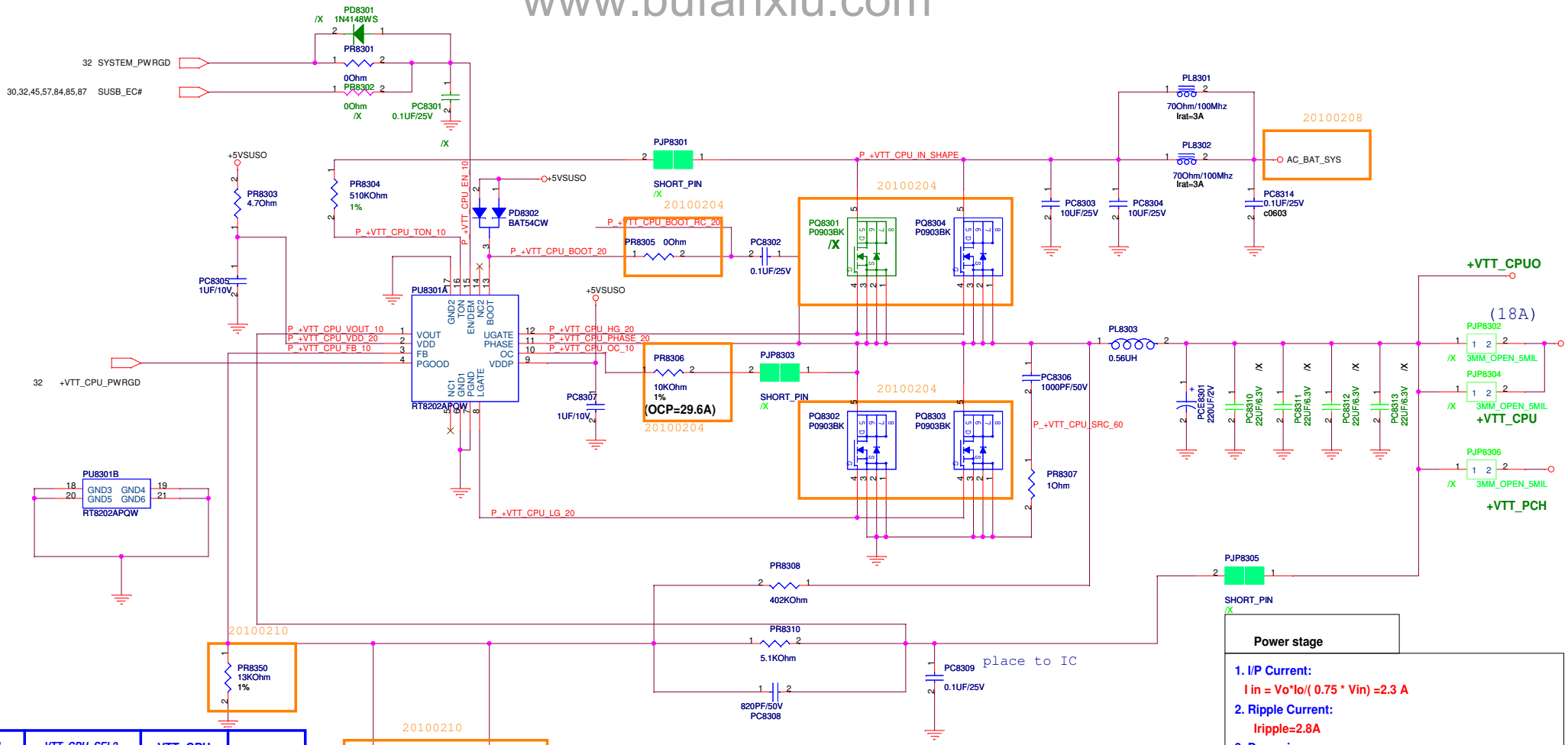
ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Thursday, February 11, 2010 Sheet 82 of 1



VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	1.041V	DV3
0	1	1.059V	DV2
1	0	1.078V	DV1
1	1	1.097V	Normal

Controller

1. Voltage & Current:
   +VCCP:1.05V@10A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR7343=18KOhm
   Iocp=Rocp*20/Rds(on)=22A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total = 200 uF
   I inrush= 0.16 A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.3 A
2. Ripple Current:
   Iripple=2.8A
3. Dynamic:
   Ipeak=1.98A
   DCR=3.3mohm
   V=6.534mV
4. Inductor Spec:
   Isat=16A
   Idc=11A
   DCR=9mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

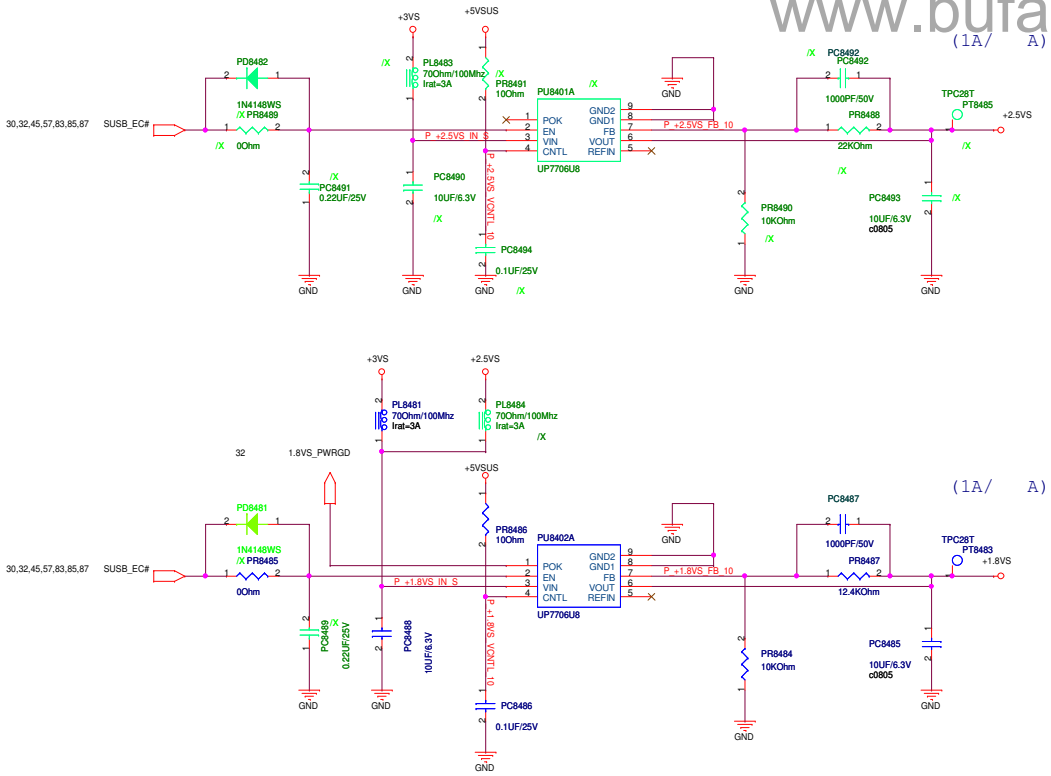
ASUSTeK COMPUTER INC

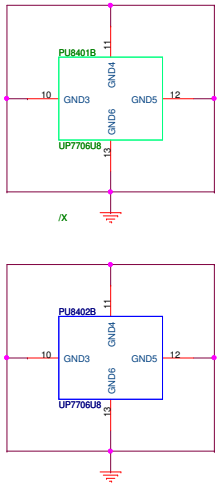
Title : Power_+VCCP

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, February 11, 2010 Sheet 83 of 1





Controller

1. Voltage & Current:

   +1.8V:+1.8V&12A

2. Frequency:

   Ton=3.85p*Rt(on)*Vo/Vin-05
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   Set PR7343=18kohm
   Iocp=Rocp*20/Rds(on)
   =20*21.5/16.5=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5.Inrush Current:

   C total =100uF
   I
   inrush=0.133A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.8 * Vin) =0.947A

2. Ripple Current:

   Iripple=2.342A

3. Ripple Voltage:

   Ipeak=(vin-vo)*D/(L*Fsw)=3.25A
   DCR=3.3mohm
   V=10.75mV

4. Inductor Spec:

   Isat=36A
   Idc=18A
   DCR=3.3mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_+1.8V&+0.9V	
	Engineer:	
Size: C	Project Name	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 84 of 1	

SUSB#_PWR POWER

20100204

PQ8513 P2003BEA — +1.5V → +1.5VS (0.79A/0.056A)
PR8512 200KOhm, PC8514 0.033UF/25V MLCC/+/-10%, PC8513 4.7UF/6.3V

20100204

PQ8509 P2003BEA — +3VSUSO → +3VS (0.79A/0.056A)
PR8501 270KOhm, PC8502 0.033UF/25V MLCC/+/-10%, PC8501 4.7UF/6.3V

20100204

PQ8510 P2003BEA — +5VSUSO → +5VS (1.29A/0.33A)
PR8502 240KOhm 1%, PC8504 0.033UF/25V MLCC/+/-10%, PC8503 4.7UF/6.3V

PQ8503 UMC4N — +12VSUS → +12VS (0.012A)
PR8503 100KOhm 1%
30,32,45,57,83,84,87 SUSB_EC#

20100204

PQ8517 P2003BEA — +3VS → +3VSG (VDD33 / +3VSG) (1.38A)
3VSG_RC_10, PR8515 200KOhm, PC8519 0.033UF/25V MLCC/+/-10%, PC8520 4.7UF/6.3V

20100204

PQ8516 P2003BEA — +VTT_CPU → +1.05VSG (PEX_VDD / +1.05VSG) (3.83A)
1.05VSG_RC_10, PR8514 200KOhm, PC8517 0.033UF/25V MLCC/+/-10%, PC8518 4.7UF/6.3V

20100204

PQ8514 RJK0355DPA-00-J0 — +1.5V → +1.5VSG (PBVDDQ / +1.5VSG) (5.85A)
1.5VSG_RC_10, PR8513 200KOhm, PC8516 0.033UF/25V MLCC/+/-10%, PC8515 4.7UF/6.3V

20100204

PQ8515 P2003BEA /X — +1.8VS → +1.8VSG (IFPAB_IOVDD / +1.8VSG) (0.3A)
1.8VSG_RC_10, PR8509 200KOhm /X, PC8512 0.033UF/25V MLCC/+/-10% /X, PC8511 4.7UF/6.3V /X

+5VSUS
PR8561 100KOhm 1%, PC8560 10NF/25V MLCC/+/-5% c0402 N/A, PQ8560A UM6K1N
PR8563 150KOHM, PC8562 10NF/25V MLCC/+/-5% c0402 → +12VS
PR8516 0Ohm /X
30,32,45,57,83,84,87 SUSB_EC#
PR8510 0Ohm, GPU_LS_EN_10
TPC28T PT8561, PR8562 10KOhm, PQ8560B UM6K1N
PC8561 10NF/25V c0402

SUSC#_PWR POWER

PQ8512 P2003BEA — +5VSUSO → +5V (1.29A/0.33A)
PR8507 200KOhm 1%, PC8510 0.033UF/25V MLCC/+/-10%, PC8509 4.7UF/6.3V

PQ8504 UMC4N — +12VSUS → +12V (0.012A)
30,57,87,91 SUSC_EC#
PR8504 100KOhm 1%

+12VSUS
+3VSG: PR8526 100KOhm 1%, PR8524 100KOhm 1%, PR8525 100KOhm 1% /X, PC8525 0.1UF/16V, PQ8521A UM6K1N, PQ8521B UM6K1N, PC8526 0.1UF/16V /X — 1.05VSG_RC_10

+12VSUS
+3VSG: PR8520 100KOhm 1%, PR8518 100KOhm 1% /X, PR8519 100KOhm 1% /X, PC8521 0.1UF/16V, PQ8518A UM6K1N, PQ8518B UM6K1N, PC8522 0.1UF/16V /X — 1.5VSG_RC_10
25,82 VGA_VCORE_PWRGD → PR8517 0Ohm

+12VSUS
+1.5VSG: PR8523 100KOhm 1% /X, PR8521 100KOhm 1% /X, PR8522 100KOhm 1% /X, PC8523 0.1UF/16V /X, PQ8519 PMBS3904 /X, PQ8520 2N7002 /X, PC8524 0.1UF/16V /X — 1.8VSG_RC_10

+3VSUS
PR8530 100KOhm 1%, PR8529 100KOhm 1% /X, PR8528 100KOhm 1% /X, PC8527 0.1UF/16V /X, PQ8522 2N7002 — GPU_LS_EN_10
25,82 DGPU_PWR_EN# → PR8527 0Ohm

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_Load_Switch

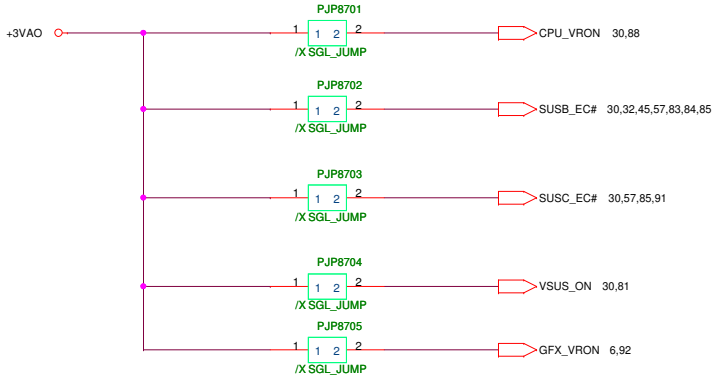
Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, February 11, 2010 Sheet 85 of 1

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_good_detecter	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 86 of 1	



<Variant Name>

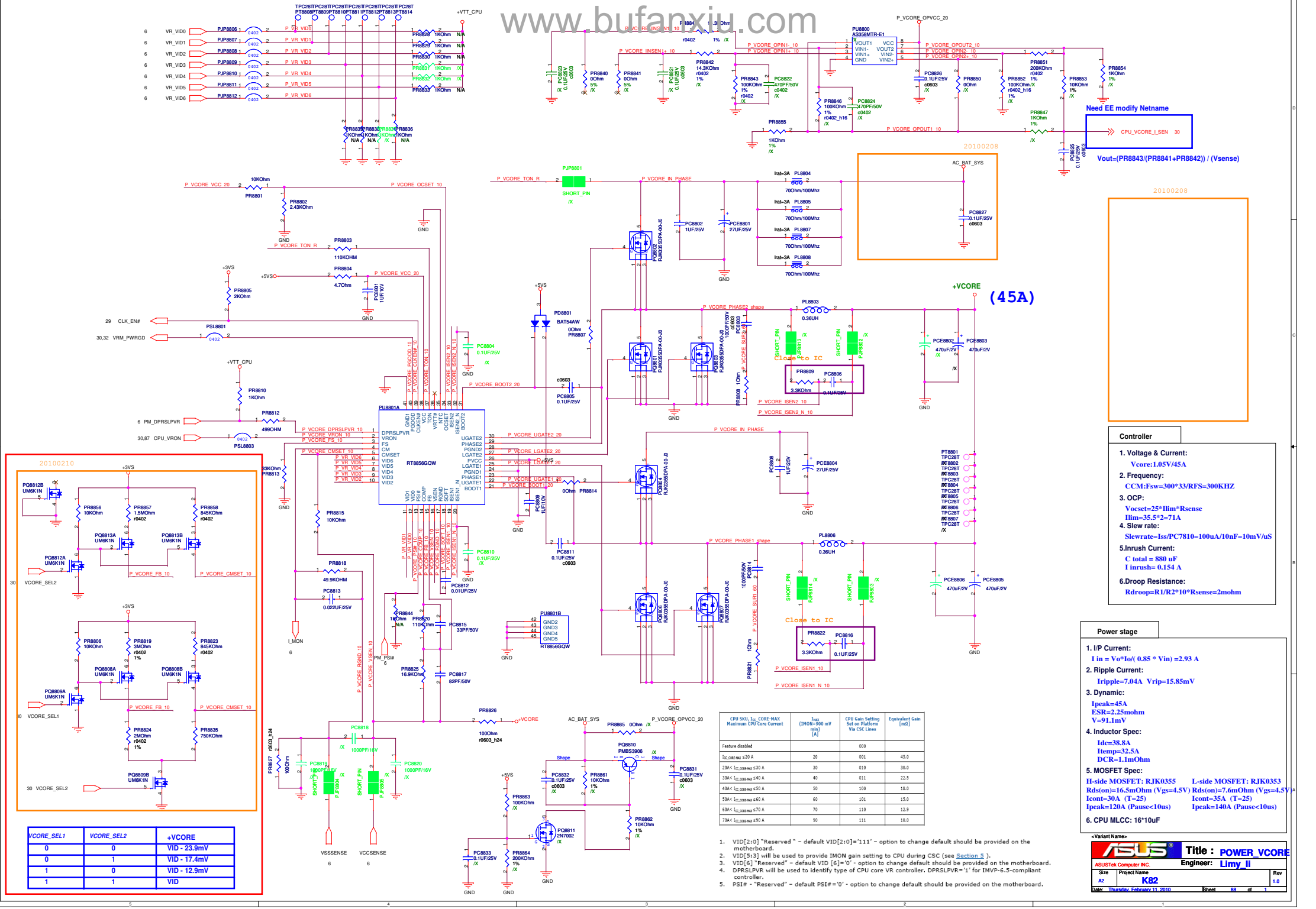
ASUSTeK COMPUTER INC

Title : Power_for_test

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Thursday, February 11, 2010 Sheet 87 of 1



VCORE_SEL1	VCORE_SEL2	+VCORE
0	0	VID - 23.9mV
0	1	VID - 17.4mV
1	0	VID - 12.9mV
1	1	VID

CPU SKU, $I_{CC\_CORE\_MAX}$ Maximum CPU Core Current	I_{MAX} (IMON=900 mV min) [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
$I_{CC\_CORE\_MAX}$ ≤20 A	20	001	45.0
20A< $I_{CC\_CORE\_MAX}$ ≤30 A	30	010	30.0
30A< $I_{CC\_CORE\_MAX}$ ≤40 A	40	011	22.5
40A< $I_{CC\_CORE\_MAX}$ ≤50 A	50	100	18.0
50A< $I_{CC\_CORE\_MAX}$ ≤60 A	60	101	15.0
60A< $I_{CC\_CORE\_MAX}$ ≤70 A	70	110	12.9
70A< $I_{CC\_CORE\_MAX}$ ≤90 A	90	111	10.0

1. VID[2:0] "Reserved " – default VID[2:0]='111' – option to change default should be provided on the motherboard.
2. VID[5:3] will be used to provide IMON gain setting to CPU during CSC (see Section 5).
3. VID[6] "Reserved" – default VID [6]='0' - option to change default should be provided on the motherboard.
4. DPRSLPVR will be used to identify type of CPU core VR controller. DPRSLPVR='1' for IMVP-6.5-compliant controller.
5. PSI# - "Reserved" – default PSI#='0' - option to change default should be provided on the motherboard.

Controller

1. Voltage & Current:
   Vcore:1.05V/45A
2. Frequency:
   CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
   Vocset=25*Ilim*Rsense
   Ilim=35.5*2=71A
4. Slew rate:
   Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5. Inrush Current:
   C total = 880 uF
   I inrush= 0.154 A
6. Droop Resistance:
   Rdroop=R1/R2*10*Rsense=2mohm

Power stage

1. I/P Current:
   I in = Vo*Io/(0.85 * Vin) =2.93 A
2. Ripple Current:
   Iripple=7.04A Vrip=15.85mV
3. Dynamic:
   Ipeak=45A
   ESR=2.25mohm
   V=91.1mV
4. Inductor Spec:
   Idc=38.8A
   Itemp=32.5A
   DCR=1.1mOhm
5. MOSFET Spec:
   H-side MOSFET: RJK0355 L-side MOSFET: RJK0353
   Rds(on)=16.5mOhm (Vgs=4.5V) Rds(on)=7.6mOhm (Vgs=4.5V)
   Icont=30A (T=25) Icont=35A (T=25)
   Ipeak=120A (Pause<10us) Ipeak=140A (Pause<10us)
6. CPU MLCC: 16*10uF

<Variant Name>

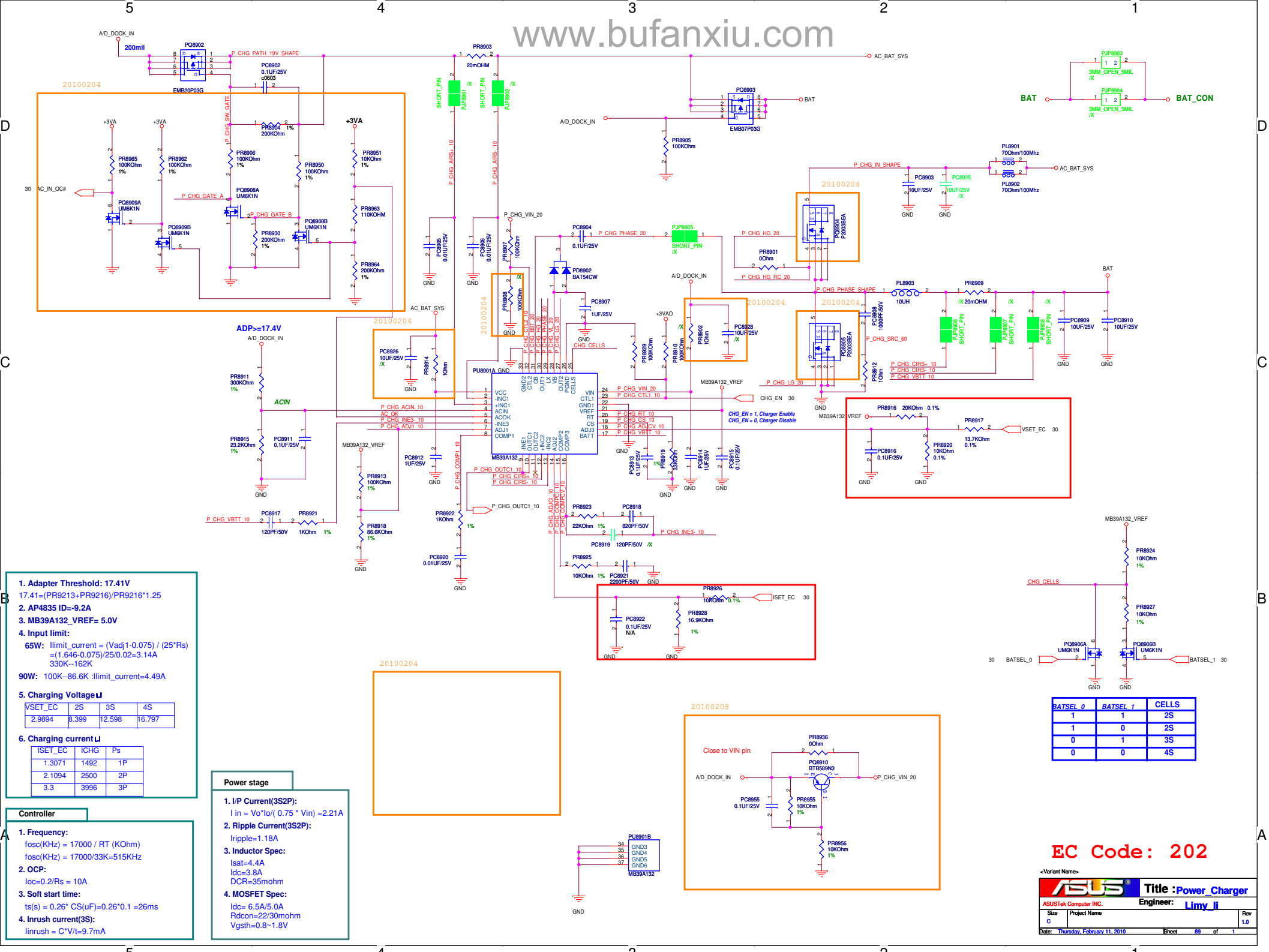
ASUSTek Computer INC.

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
A2	K82	1.0

Date: Thursday, February 11, 2010 Sheet 88 of 1



1. Adapter Threshold: 17.41V

17.41=(PR9213+PR9216)/PR9216*1.25

2. AP4835 ID=-9.2A

3. MB39A132_VREF= 5.0V

4. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25/0.02=3.14A
330K--162K

90W: 100K--86.6K :Ilimit_current=4.49A

5. Charging Voltage

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

6. Charging current

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:

fosc(KHz) = 17000 / RT (KOhm)

fosc(KHz) = 17000/33K=515KHz

2. OCP:

Ioc=0.2/Rs = 10A

3. Soft start time:

ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms

4. Inrush current(3S):

Iinrush = C*V/t=9.7mA

Power stage

1. I/P Current(3S2P):

I in = Vo*Io/(0.75 * Vin) =2.21A

2. Ripple Current(3S2P):

Iripple=1.18A

3. Inductor Spec:

Isat=4.4A
Idc=3.8A
DCR=35mohm

4. MOSFET Spec:

Idc= 6.5A/5.0A
Rdcon=22/30mohm
Vgsth=0.8~1.8V

BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

EC Code: 202

<Variant Name>

ASUSTek Computer INC.

Title : Power_Charger

Engineer: Limy_li

Size	Project Name	Rev
C		1.0

Date: Thursday, February 11, 2010 Sheet 89 of 1

<Variant Name>

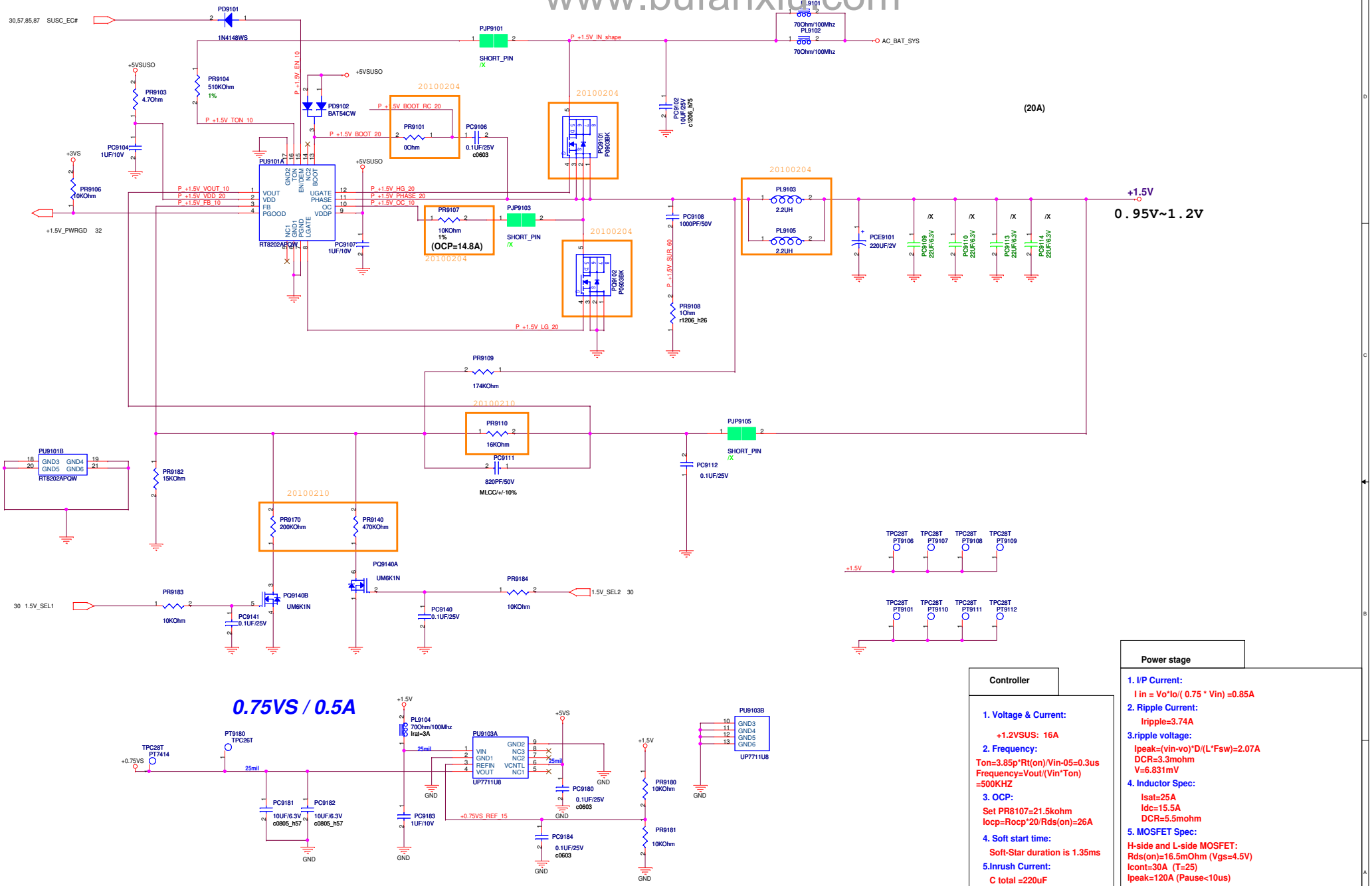
Title : Power_Charger

ASUSTek Computer INC.

Engineer: Limy_li

Size	Project Name	Rev
A3	F83T	2.1G

Date: Thursday, February 11, 2010 Sheet 90 of 1



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.483V	DV3
0	1	1.506V	DV2
1	0	1.538V	DV1
1	1	1.561V	Normal

Controller

1. Voltage & Current:
   +1.2VSUS: 16A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8107=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=3.74A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=3.3mohm
   V=6.831mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

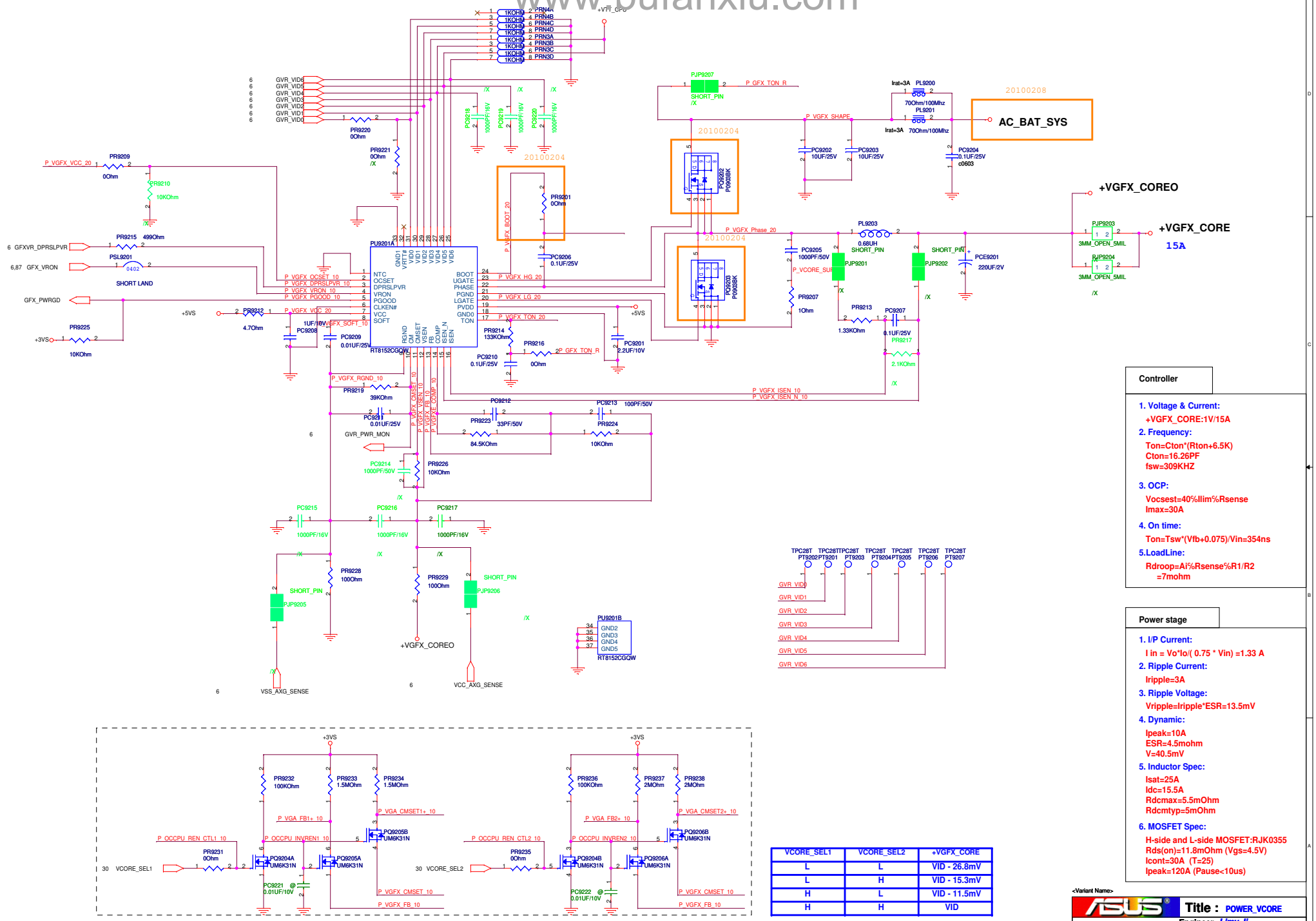
ASUSTeK COMPUTER INC

Title : +1.5V

Engineer:

Size	Project Name	Rev
C	K80A	1.0

Date: Thursday, February 11, 2010 Sheet 91 of 91



VCORE_SEL1	VCORE_SEL2	+VGFX_CORE
L	L	VID - 26.8mV
L	H	VID - 15.3mV
H	L	VID - 11.5mV
H	H	VID

Controller

1. Voltage & Current:
   +VGFX_CORE:1V/15A
2. Frequency:
   Ton=Cton*(Rton+6.5K)
   Cton=16.26PF
   fsw=309KHZ
3. OCP:
   Vocsest=40%Ilim%Rsense
   Imax=30A
4. On time:
   Ton=Tsw*(Vfb+0.075)/Vin=354ns
5. LoadLine:
   Rdroop=Ai%Rsense%R1/R2
   =7mohm

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=10A
   ESR=4.5mohm
   V=40.5mV
5. Inductor Spec:
   Isat=25A
   Idc=15.5A
   Rdcmax=5.5mOhm
   Rdcmtyp=5mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Limy_li

Size	Project Name	Rev
C	UX21	1.0

Date: Thursday, February 11, 2010 Sheet 92 of 1

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_+VCCP	
	Engineer:	
Size: C	Project Name	Rev: 1.0
Date: Thursday, February 11, 2010	Sheet 93 of 1	

<Variant Name>

Title : Power_+VCCP

ASUSTeK COMPUTER INC

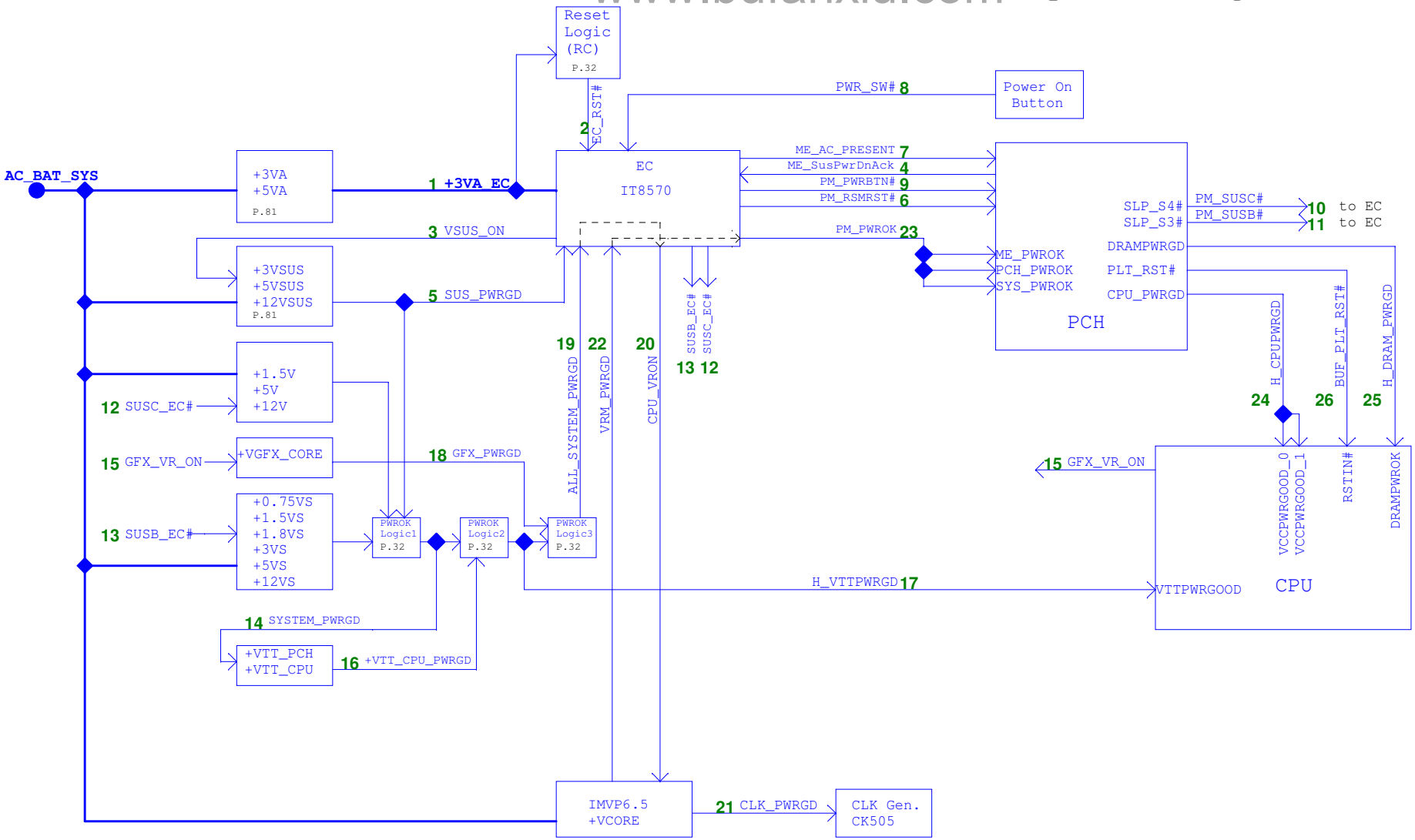
Engineer:

Size	Project Name	Rev
A3		1.0

Date: Thursday, February 11, 2010 Sheet 94 of 1

AC-IN Mode

k42Jv Power On Sequence Diagram Rev. 0.31



Power On Sequence

1 → 26

ASUSTeK COMPUTER INC

Title : POWER SEQUENCE

Engineer: JAY_TSAI

Size	Project Name	Rev
C	K42Jv	1.01

Date: Thursday, February 11, 2010 Sheet 95 of 96

M52J Power-On Sequence Timing Diagram Rev.0.31

AC-IN Mode

1 +3VA/+5VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 VSUS_ON

+3VSUS/+5VSUS

(pull up to +3VSUS)

(PCH to EC) 4 ME_SusPwrDnAck

(power to EC) 5 SUS_PWRGD

T0=20ms(spec.>=10ms)

T1<200ms(check)

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 ME_AC_PRESENT

(falling edge)

(to EC) 8 PWR_SW#

T2=50ms

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 ME_PM_SLP_M#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/ME_PM_SLP_LAN#

(PCH to EC) (PCH to power)

+1.1VM_LAN

(EC to power) 13 ME_SLP_M_EC#

+1.1VM/+3VM

(EC to power) 14 SUSC_EC#

+1.5V/+3V/+5V

(EC to power) 15 SUSB_EC#

+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS

(power to EC) 16 ME_+VM_PWRGD

T3=2ms(spec.>=1ms)

(EC to PCH) 17 ME_PWROK

18 SYSTEM_PWRGD

+VTT_CPU

(CPU to power) 19 GFX_VR_ON

T4=1.25ms

20 +VTT_CPU_PWRGD/ 21 H_VTTPWRGD

(power to CPU)

GFX_VID

+VGFX_CORE

T5=60us(typ.)

22 GFX_PWRGD

(power to EC)

23 ALL_SYSTEM_PWRGD

T6=110ms (spec.>=99ms)

(EC to power) 24 CPU_VRON

T7=10~100us

+VCORE

25 CLK_PWRGD

(inversion of CLK_EN#)

T8=3~20ms

(power to EC) 26 VRM_PWRGD

(EC to PCH) 27 PM_PWROK

T9=10ms

(PCH to CPU) 28 H_DRAM_PWRGD

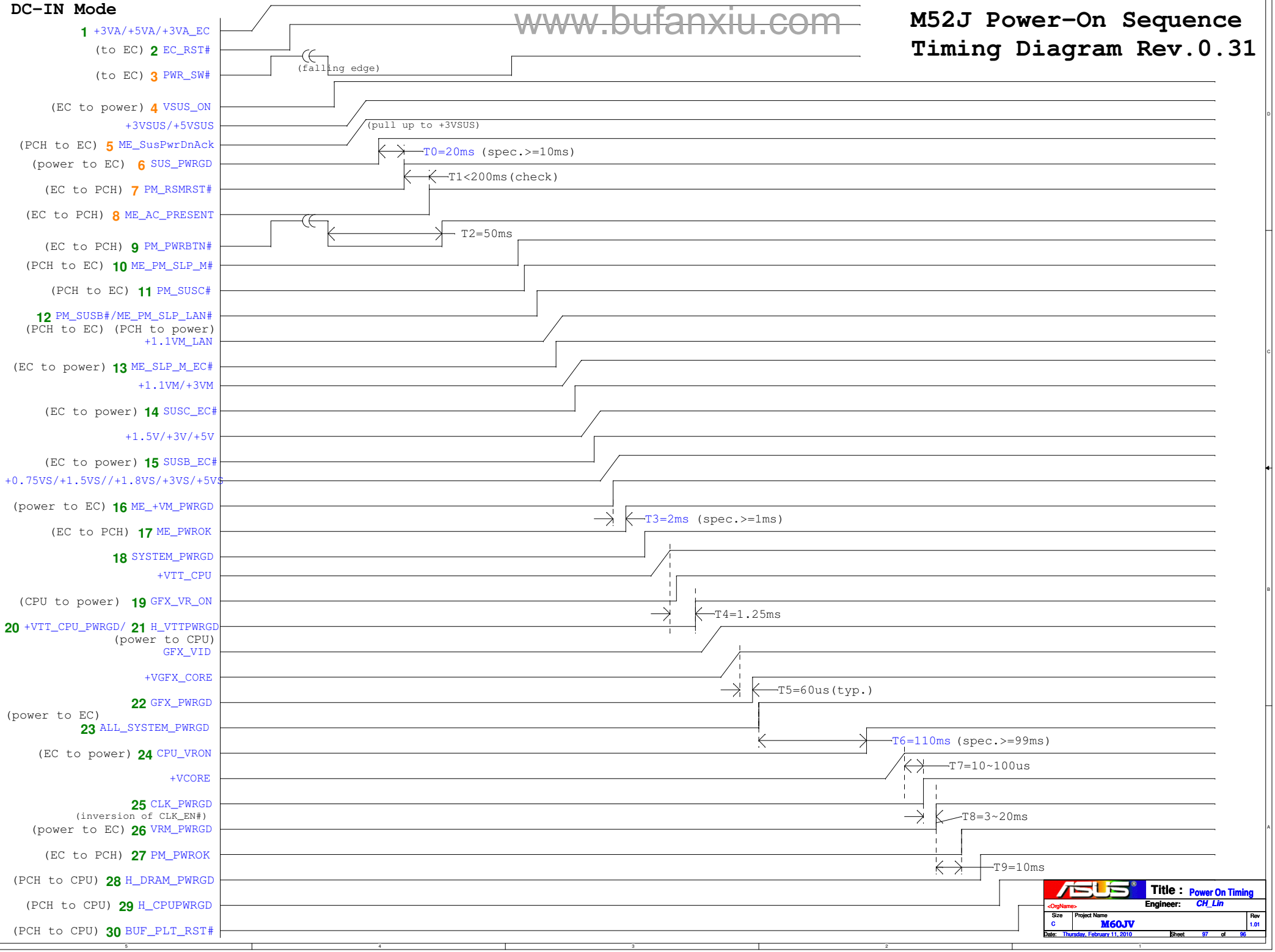
(PCH to CPU) 29 H_CPUPWRGD

(PCH to CPU) 30 BUF_PLT_RST#

Title : Power On Timing		
<OrgName>	Engineer: CH_Lin	
Size: C	Project Name: M60JV	Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 96 of 96	

M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode



Title : Power On Timing			
<OrgName>	Engineer: CH_Lin		
Size: C	Project Name: M60JV		Rev: 1.01
Date: Thursday, February 11, 2010	Sheet 97 of 96		