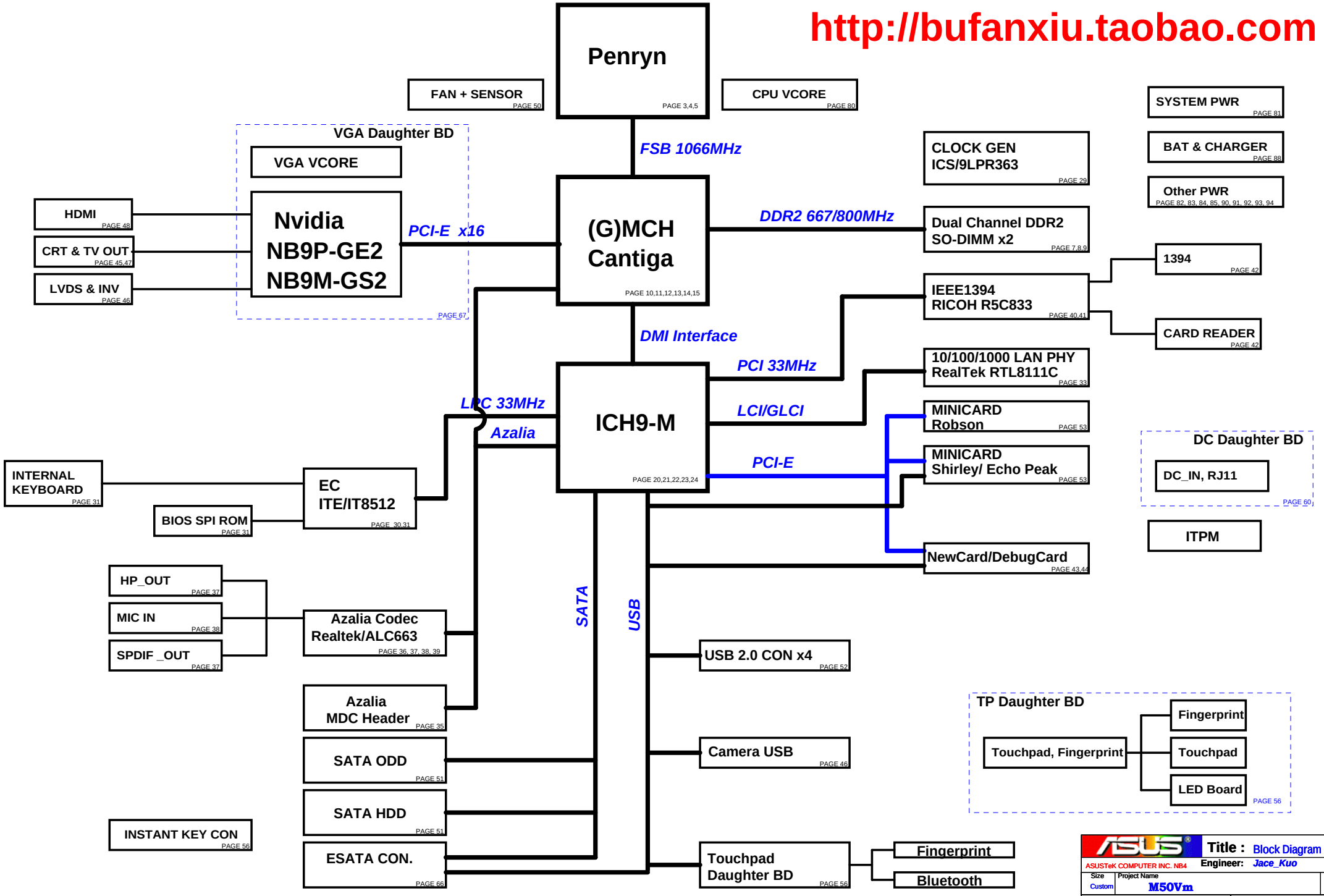
M50Vm Montevina Block Diagram



ASUSTeK COMPUTER INC. NB4	Title : Block Diagram		
	Engineer: Jace_Kuo		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 1 of 96		

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ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI	SIO_SMI#	+3VS
GPIO 07	GPI	WLAN_LED_ON	+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	GPI	LAN_WOL_EN	+3VSUS
GPIO 10	GPI	SUSPWR_ACK	+3VSUS
GPIO 11	GPI	EXT_SCI#	+3VSUS
GPIO 12	GPO		+3VSUS
GPIO 13	GPI		+3VSUS
GPIO 14	GPI	AC_PRESENT	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_ON#	+3VS
GPIO 18	GPO	PD_RST#	+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	-	+3VS
GPIO 23	Native	LPC_DRQ1#	+3VS
GPIO 24	GPO	PD_EN	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	CB_SD#	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	EMAIL_LED#	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC#1	+3VSUS
GPIO 41	Native	USB_OC#2	+3VSUS
GPIO 42	Native	USB_OC#3	+3VSUS
GPIO 43	Native	USB_OC#4	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDTV_EN#	**+3VS**
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native		+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native		+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native		+3VS
GPIO 56			+3VSUS
GPIO 57	GPI		+3VSUS
GPIO 58	GPI	SPI_CS#1	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native		+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	

ASUSTeK COMPUTER INC. NB6

Title : Schematic Information

Engineer: Raphael_Chen

Size	Project Name	Rev
Custom	M50Vm	1.1

Date: Wednesday, February 13, 2008 Sheet 2 of 96

10 H_D#[63:0] — H_D#[63:0]

10 H_A#[35:3] — H_A#[35:3]

10 H_REQ#[4:0] — H_REQ#[4:0]

U0301A

ADDR GROUP 0

H_A#3 J4 A[3]#
H_A#4 L5 A[4]#
H_A#5 L4 A[5]#
H_A#6 K5 A[6]#
H_A#7 M3 A[7]#
H_A#8 N2 A[8]#
H_A#9 J1 A[9]#
H_A#10 N3 A[10]#
H_A#11 P5 A[11]#
H_A#12 P2 A[12]#
H_A#13 L2 A[13]#
H_A#14 P4 A[14]#
H_A#15 P1 A[15]#
H_A#16 R1 A[16]#
10 H_ADSTB#0 M1 ADSTB[0]#

H_REQ#0 K3 REQ[0]#
H_REQ#1 H2 REQ[1]#
H_REQ#2 K2 REQ[2]#
H_REQ#3 J3 REQ[3]#
H_REQ#4 L1 REQ[4]#

ADDR GROUP 1

H_A#17 Y2 A[17]#
H_A#18 U5 A[18]#
H_A#19 R3 A[19]#
H_A#20 W6 A[20]#
H_A#21 U4 A[21]#
H_A#22 Y5 A[22]#
H_A#23 U1 A[23]#
H_A#24 R4 A[24]#
H_A#25 T5 A[25]#
H_A#26 T3 A[26]#
H_A#27 W2 A[27]#
H_A#28 W5 A[28]#
H_A#29 Y4 A[29]#
H_A#30 U2 A[30]#
H_A#31 V4 A[31]#
H_A#32 W3 A[32]#
H_A#33 AA4 A[33]#
H_A#34 AB2 A[34]#
H_A#35 AA3 A[35]#
10 H_ADSTB#1 V1 ADSTB[1]#

H_A20M# A6 A20M#
H_FERR# A5 FERR#
H_IGNNE# C4 IGNNE#

H_STPCLK# D5 STPCLK#
H_INTR C6 LINT0
H_NMI B4 LINT1
H_SMI# A3 SMI#

RESERVED

M4 RSVD1
N5 RSVD2
T2 RSVD3
V3 RSVD4
B2 RSVD5
C3 RSVD6
D2 RSVD7
D22 RSVD8
D3 RSVD9
F6 RSVD10

H_TDO_M
H_TDI_M

SOCKET478B

CONTROL

ADS# H1 H_ADS# 10
BNR# E2 H_BNR# 10
BPRI# G5 H_BPRI# 10

DEFER# H5 H_DEFER# 10
DRDY# F21 H_DRDY# 10
DBSY# E1 H_DBSY# 10

BR0# F1 H_BR0# 10

IERR# D20 H_IERR#
INIT# B3 H_INIT# 20

LOCK# H4 H_LOCK# 10

RESET# C1 H_CPURST# 10
RS[0]# F3 H_RS#0 10
RS[1]# F4 H_RS#1 10
RS[2]# G3 H_RS#2 10
TRDY# G2 H_TRDY# 10

HIT# G6 H_HIT# 10
HITM# E4 H_HITM# 10

T0318
T0319

+VCCP_CPU
R0309 1 2 56Ohm

XDP/ITP SIGNALS

BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2
PREQ# AC1 H_PREQ#
TCK AA6 H_TCK
TDI AB3 H_TDI
TDO AB5 H_TDO
TMS AB6 H_TMS
TRST# C20 H_TRST#
DBR# H_DBR#

THERMAL

PROCHOT# D21 H_PROCHOT_S#
THRMDA A24 CPU_THRM_DA 50
THRMDC B25 CPU_THRM_DC 50
THERMTRIP# C7 H_THRMTRIP# 5,20,32

H CLK

BCLK[0] A22 CLK_CPU_BCLK 29
BCLK[1] A21 CLK_CPU_BCLK# 29

T0302
T0303

T0313
T0314
GTL_REF2

U0301B

DATA GRP 0

H_D#0 E22 D[0]#
H_D#1 F24 D[1]#
H_D#2 E26 D[2]#
H_D#3 G22 D[3]#
H_D#4 E23 D[4]#
H_D#5 G25 D[5]#
H_D#6 E25 D[6]#
H_D#7 E23 D[7]#
H_D#8 K24 D[8]#
H_D#9 G24 D[9]#
H_D#10 J24 D[10]#
H_D#11 J23 D[11]#
H_D#12 H22 D[12]#
H_D#13 F26 D[13]#
H_D#14 K22 D[14]#
H_D#15 H23 D[15]#
10 H_DSTBN#0 J26 DSTBN[0]#
10 H_DSTBP#0 H26 DSTBP[0]#
10 H_DINV#0 H25 DINV[0]#

DATA GRP 2

Y22 D[32]# H_D#32
AB24 D[33]# H_D#33
V24 D[34]# H_D#34
V26 D[35]# H_D#35
V23 D[36]# H_D#36
T22 D[37]# H_D#37
U25 D[38]# H_D#38
U23 D[39]# H_D#39
Y25 D[40]# H_D#40
W22 D[41]# H_D#41
Y23 D[42]# H_D#42
W24 D[43]# H_D#43
W25 D[44]# H_D#44
AA23 D[45]# H_D#45
AA24 D[46]# H_D#46
AB25 D[47]# H_D#47
Y26 DSTBN[2]# H_DSTBN#2 10
AA26 DSTBP[2]# H_DSTBP#2 10
U22 DINV[2]# H_DINV#2 10

DATA GRP 1

H_D#16 N22 D[16]#
H_D#17 K25 D[17]#
H_D#18 P26 D[18]#
H_D#19 R23 D[19]#
H_D#20 L23 D[20]#
H_D#21 M24 D[21]#
H_D#22 L22 D[22]#
H_D#23 M23 D[23]#
H_D#24 P25 D[24]#
H_D#25 P23 D[25]#
H_D#26 P22 D[26]#
H_D#27 T24 D[27]#
H_D#28 R24 D[28]#
H_D#29 L25 D[29]#
H_D#30 T25 D[30]#
H_D#31 N25 D[31]#
10 H_DSTBN#1 L26 DSTBN[1]#
10 H_DSTBP#1 M26 DSTBP[1]#
10 H_DINV#1 N24 DINV[1]#

DATA GRP 3

D[48]# AE24 H_D#48
D[49]# AD24 H_D#49
D[50]# AA21 H_D#50
D[51]# AB22 H_D#51
D[52]# AB21 H_D#52
D[53]# AC26 H_D#53
D[54]# AD20 H_D#54
D[55]# AE22 H_D#55
D[56]# AF23 H_D#56
D[57]# AC25 H_D#57
D[58]# AE21 H_D#58
D[59]# AD21 H_D#59
D[60]# AC22 H_D#60
D[61]# AD23 H_D#61
D[62]# AF22 H_D#62
D[63]# AC23 H_D#63
DSTBN[3]# AE25 H_DSTBN#3 10
DSTBP[3]# AF24 H_DSTBP#3 10
DINV[3]# AC20 H_DINV#3 10

MISC

GTLREF AD26
TEST1 C23
TEST2 D25
TEST3 C24
TEST4 AF26
TEST5 AF1
TEST6 A26

BSEL[0] B22
BSEL[1] B23
BSEL[2] C21

COMP[0] R26 H_COMP0 R0311 1 2 27.4Ohm 1%
COMP[1] U26 H_COMP1 R0312 1 2 54.9Ohm 1%
COMP[2] AA1 H_COMP2 R0313 1 2 27.4Ohm 1%
COMP[3] Y1 H_COMP3 R0314 1 2 54.9Ohm 1%

DPRSTP# E5 H_DPRSTP# 11,20,80
DPSLP# B5 H_DPSLP# 20
DPWR# D24 H_DPWR# 10
PWRGOOD D6
SLP# D7 H_CPUSLP# 10
PSI# AE6 PM_PSI# 80

SOCKET478B

+VCCP_CPU
R0315 1KOhm 1%
R0316 2KOhm 1%
C0301 0.1UF/10V @

GTL_REF
R0317 @ 1% 1KOhm
R0318 @ 1% 1KOhm
T0304
T0305
T0306
T0307

29 CPU_BSEL0
29 CPU_BSEL1
29 CPU_BSEL2

Zo=55 Ohm, 0.5" max for GTL_REF

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

H_PWRGD 20

R0319 2 1 200Ohm @ +VCCP_CPU

Pin B2 M4 N5 left as NC for QC design (BPM_2# [2] BPM_2#[1] BPM_2[0])

Pin T2 V3 change to QC Thermal Diode detect (THRMDA_2 THRMDC_2)

T0320
T0321

+VCCP_CPU
R0335 1KOhm @ 1%
R0301 2KOhm @ 1%
C0302 0.1UF/10V @

DC

Default Strapping When Not Used

+VCCP_CPU

H_PREQ# R0302 54.9Ohm 1%
H_TDI R0303 54.9Ohm 1%
H_TDO R0304 @ 54.9Ohm 1%
H_TMS R0305 54.9Ohm 1%
H_DBR# R0306 @ 1KOhm 1% +3VS
H_TCK R0307 54.9Ohm 1%
H_TRST# R0308 54.9Ohm 1%

Place R0304 & R0306 for XDP function

QC

Default Strapping When Not Used

+VCCP_CPU

H_TDO_M R0330 @ 54.9Ohm 1%
H_TDI_M R0331 @ 54.9Ohm 1%

+VCCP_CPU
R0310 68Ohm
H_PROCHOT_S#
30,88 PWRLIMIT# D0301 RB751V-40
Q0301 H2N7002
THRO_CPU 30

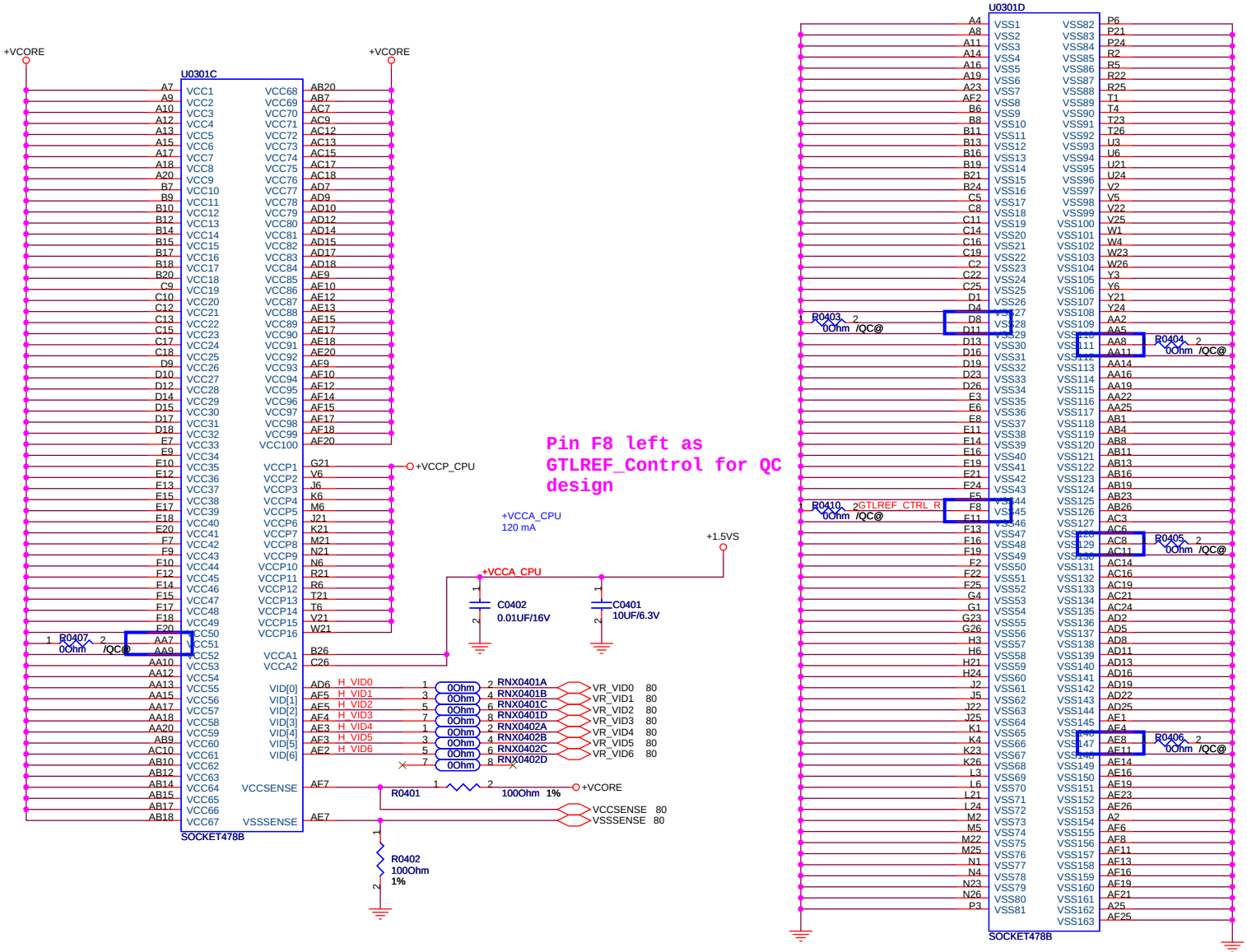
/QC only QC mount
/QC@ DC mount

ASUSTeK COMPUTER INC. NB4

Title : Penryn CPU (1)
Engineer: Jace_Kuo

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Tuesday, March 04, 2008 Sheet 3 of 96



Pin AA7 left NC for QC design (QC BR1#)

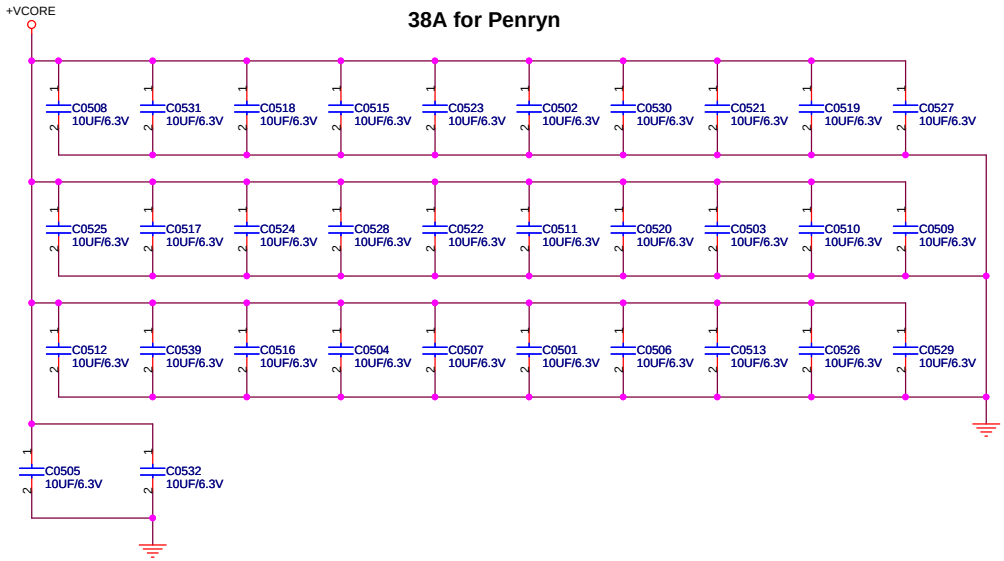
Pin F8 left as GTLREF_Control for QC design

Pin AA8 AC8 D8 left as reserved for QC design

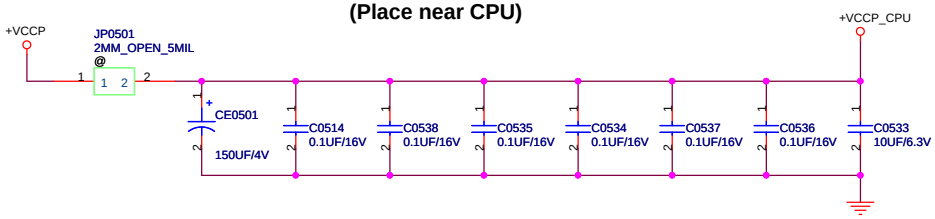
Pin AE8 left as NC for QC design (BPM_2#[3])

ASUSTeK COMPUTER INC. NB4	Title : Penryn CPU (2)	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 4 of 96	

38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)

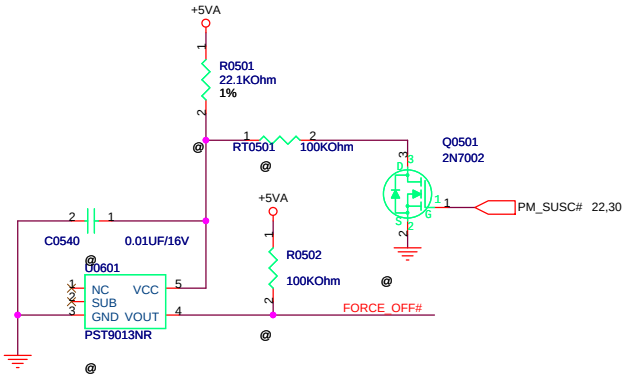


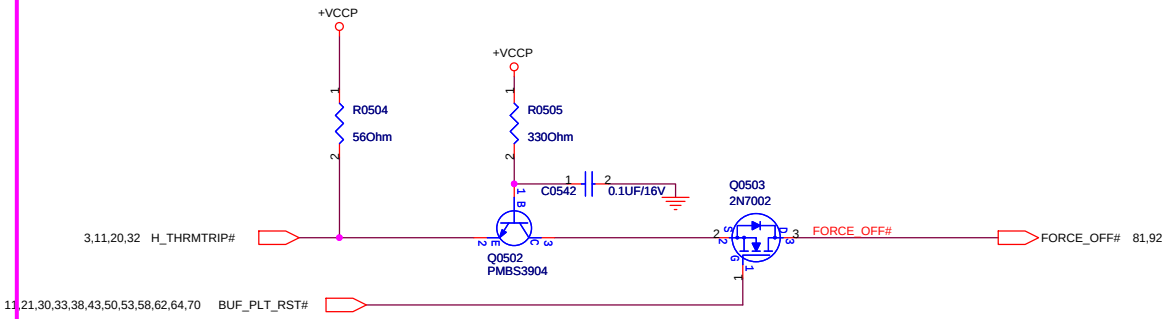
Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?

? DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU

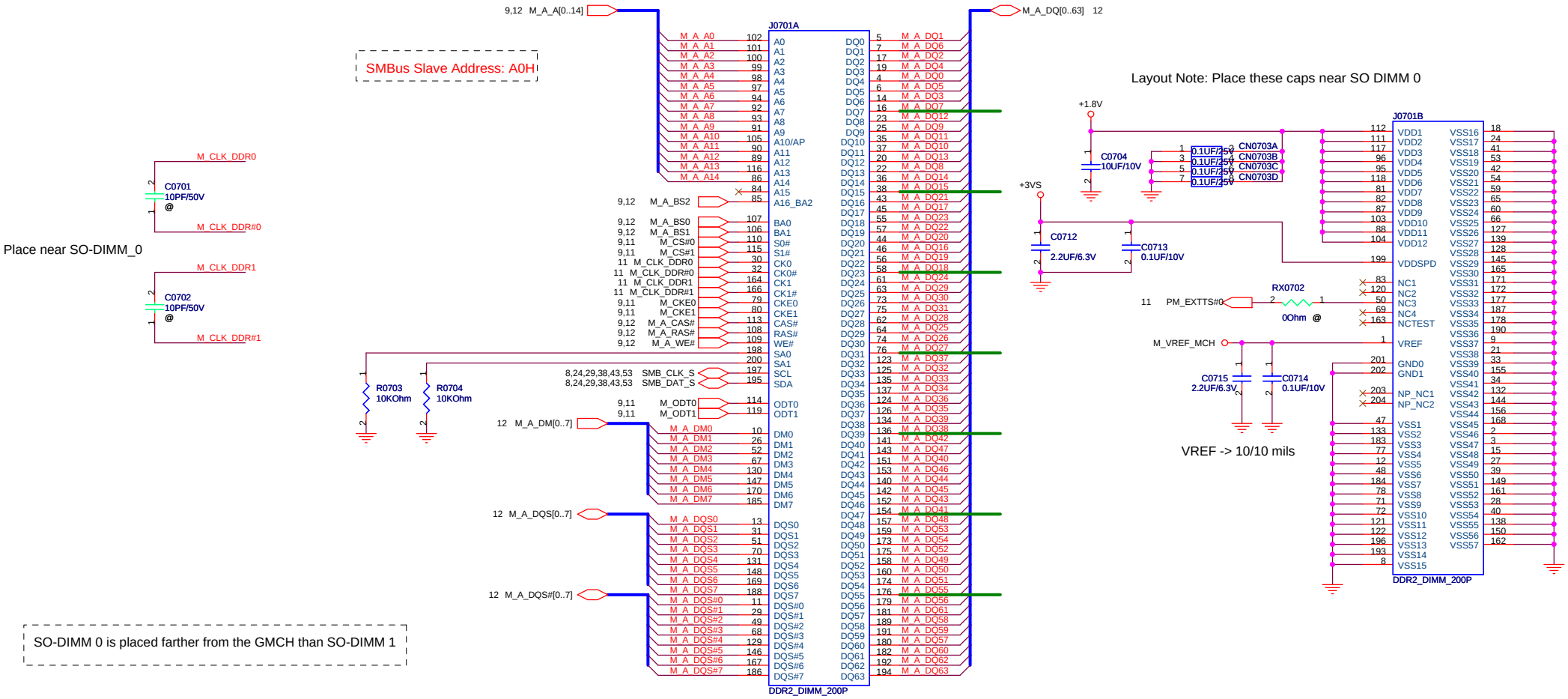




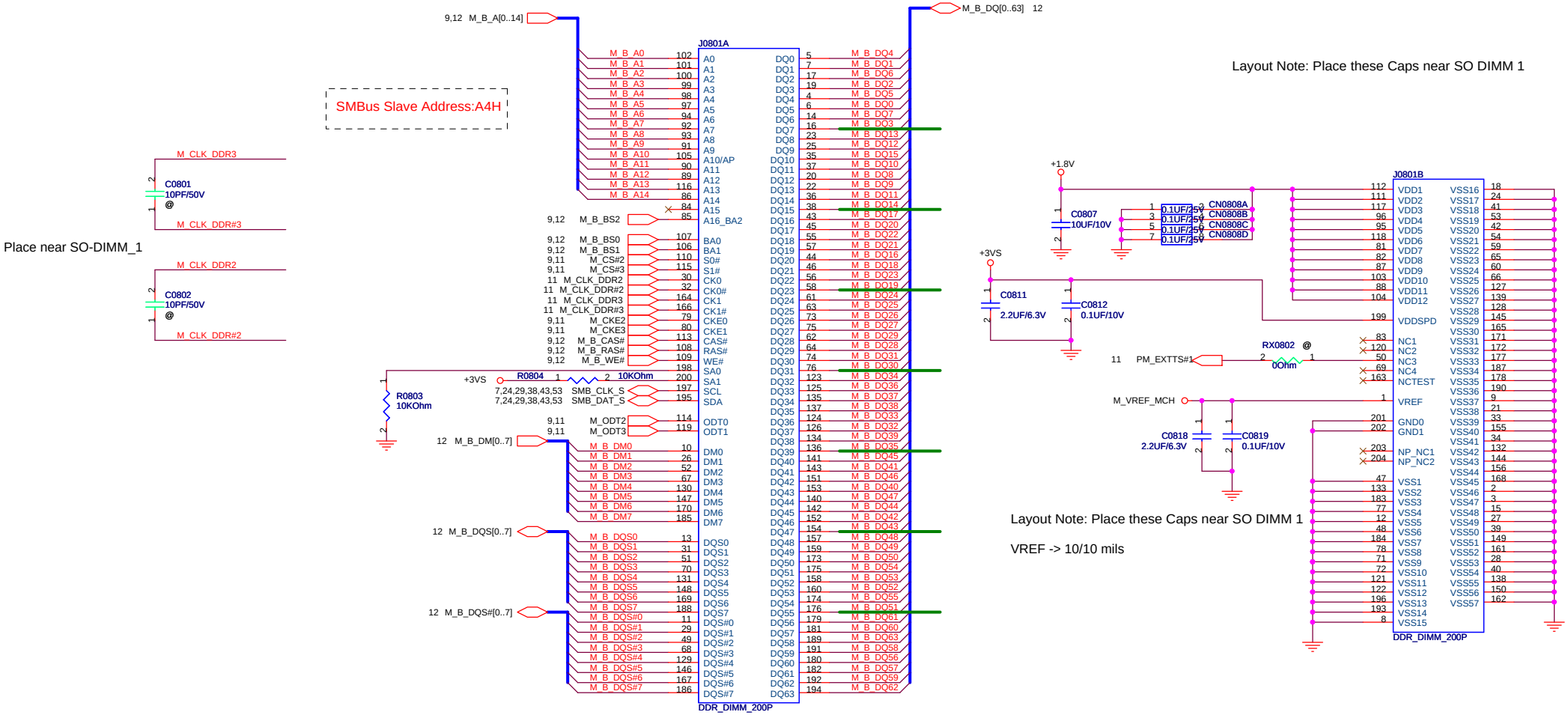
Thermal Trip signal (From CPU to ICH-9M and sequence)

ASUSTeK COMPUTER INC. NB4	Title : CPU CAPS	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 5 of 96	

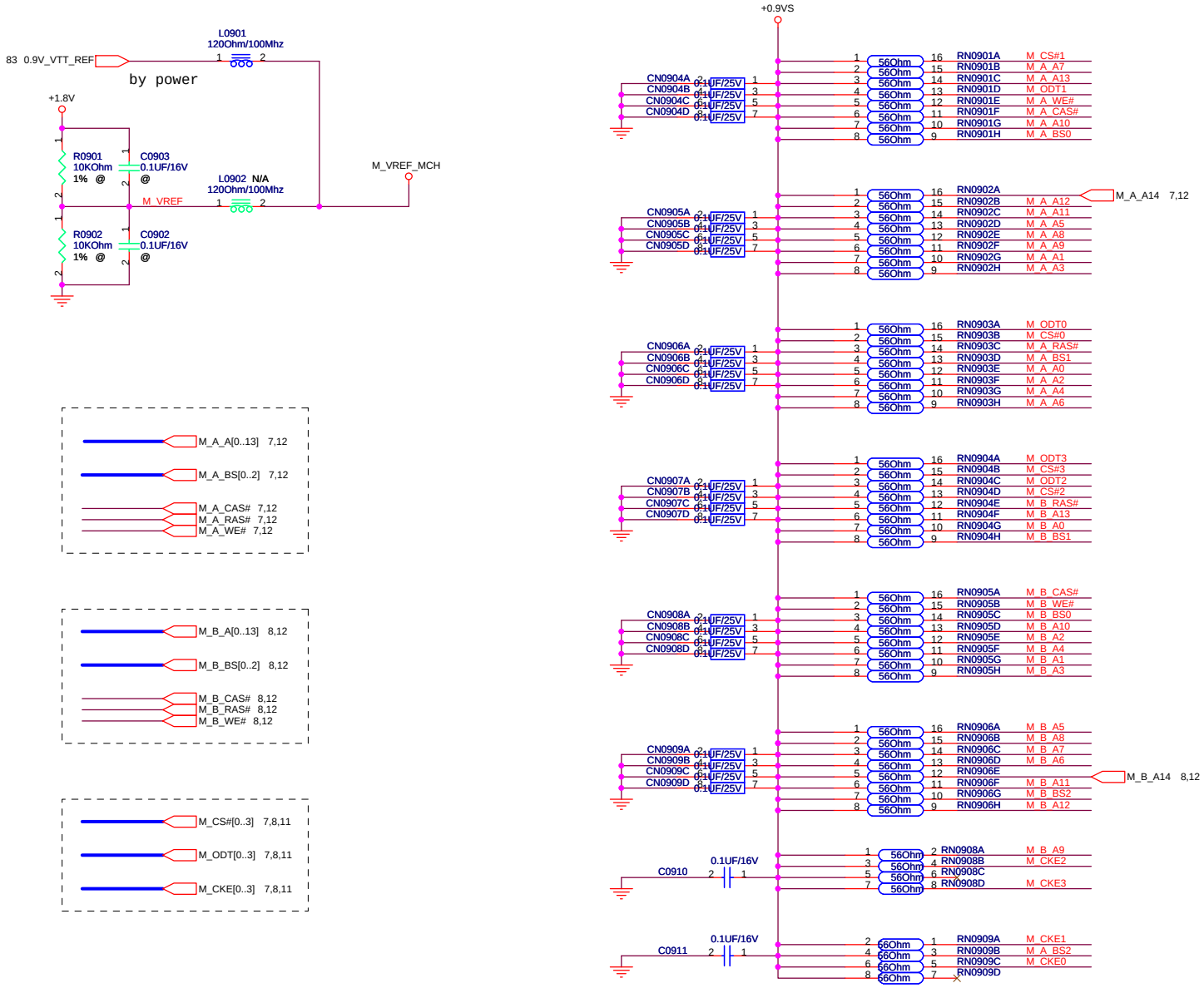
ASUSTeK COMPUTER INC. NB6	Title : Engineer:	
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 6 of 96	



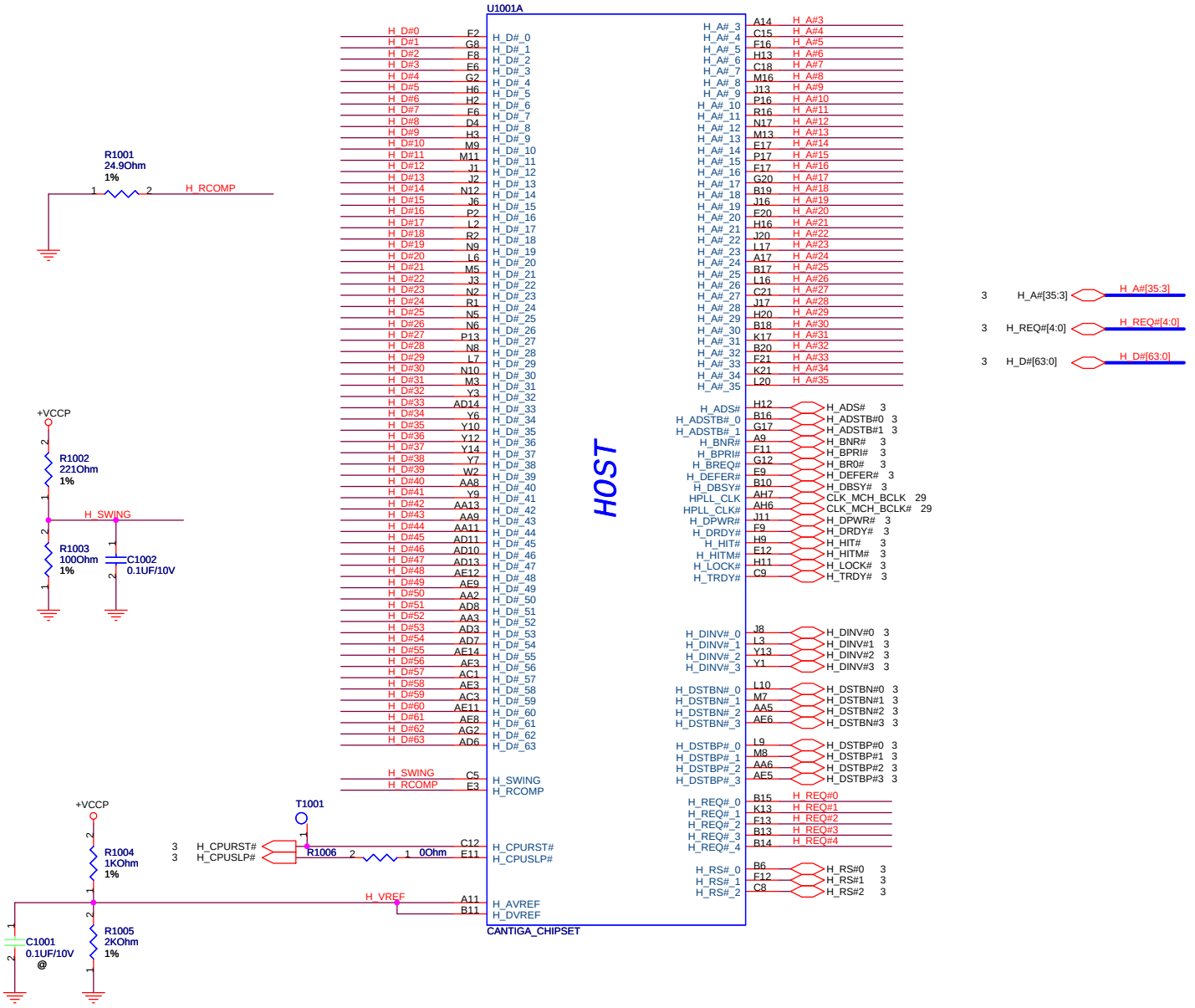
ASUSTeK COMPUTER INC. NB4	Title : DDR2 SO-DIMM_0	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 7 of 96	



ASUSTeK COMPUTER INC. NB4	Title : DDR2 SO-DIMM_1		
	Engineer: Jace_Kuo		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Friday, March 07, 2008	Sheet 8 of 96		



ASUSTeK COMPUTER INC. NB4	Title : DDR2 termination	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, March 04, 2008	Sheet 9 of 96	



Cap 0.1uF within 500 mils from GMCH

ASUSTeK COMPUTER INC. NB4	Title : Cantiga - CPU (1)	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 10 of 96	

LVDS signals CRT signals
PM:NC PM:GND
OTH Hsync and Vsync NC

U1001B

RSVD
DDR CONTROL/COMPENSATION
CLK
DMI
GRAPHICS VID
PM
ME
MISC
HDA
NC

U1001C

LVDS
PCI-EXPRESS GRAPHICS
VGA

R1.1 SWAP LVDS Chanel A B

change CRT part-number to 0 Ohm
10G212000004010
R1112

R1112: 0 ohm for PM

change CRT part-number to 0 Ohm 10G212000004010 R1109 R1120 R1111

PM: 0Ohm
GM disable: 0Ohm
GM: 150Ohm

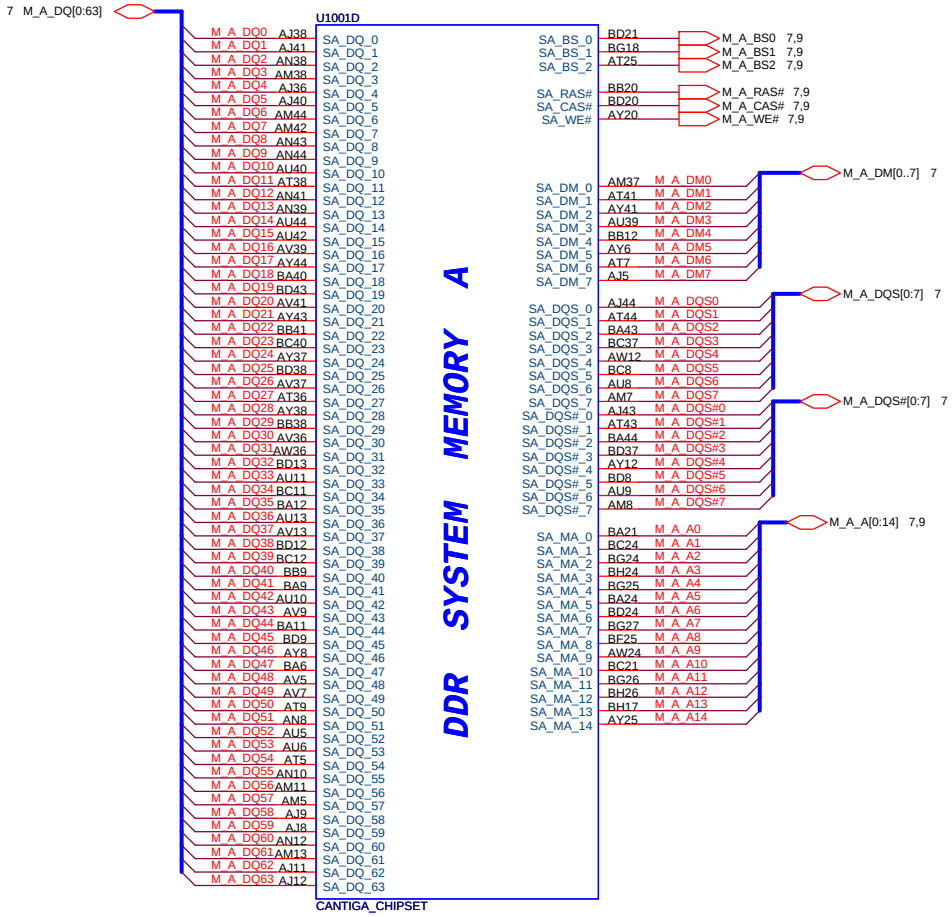
FOLLOW INTEL Design

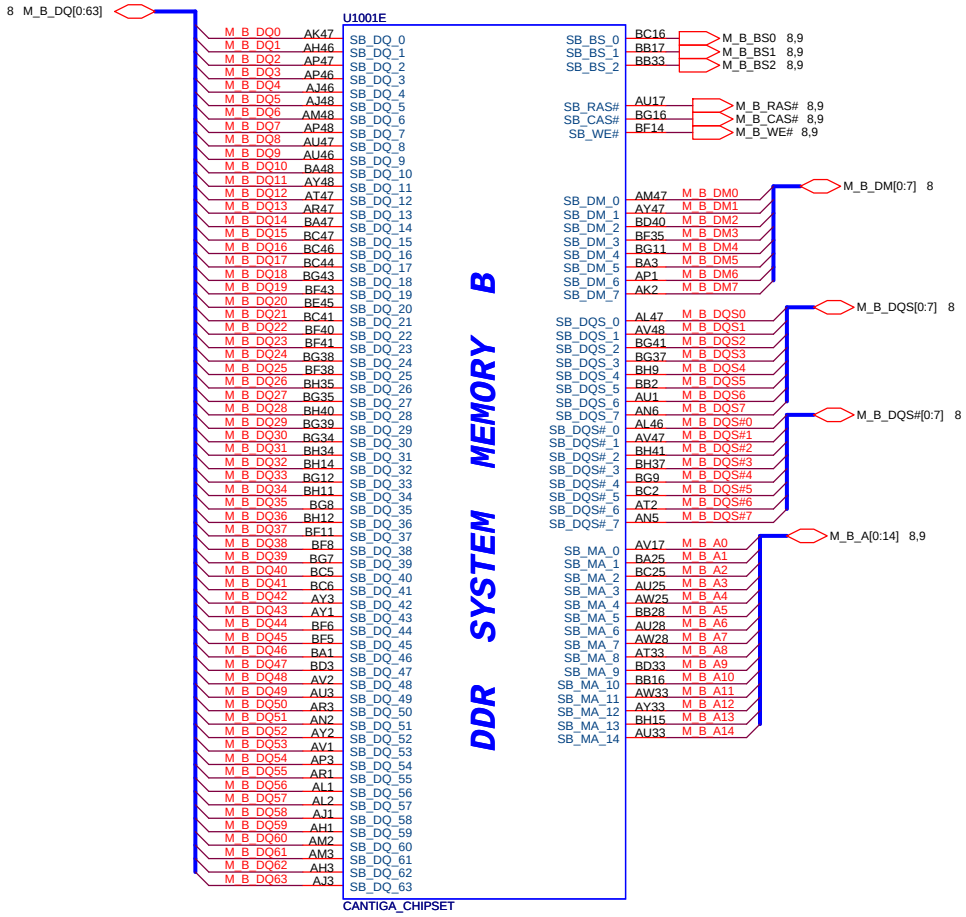
To EC(THERM.)

PM_NC_AUD_side

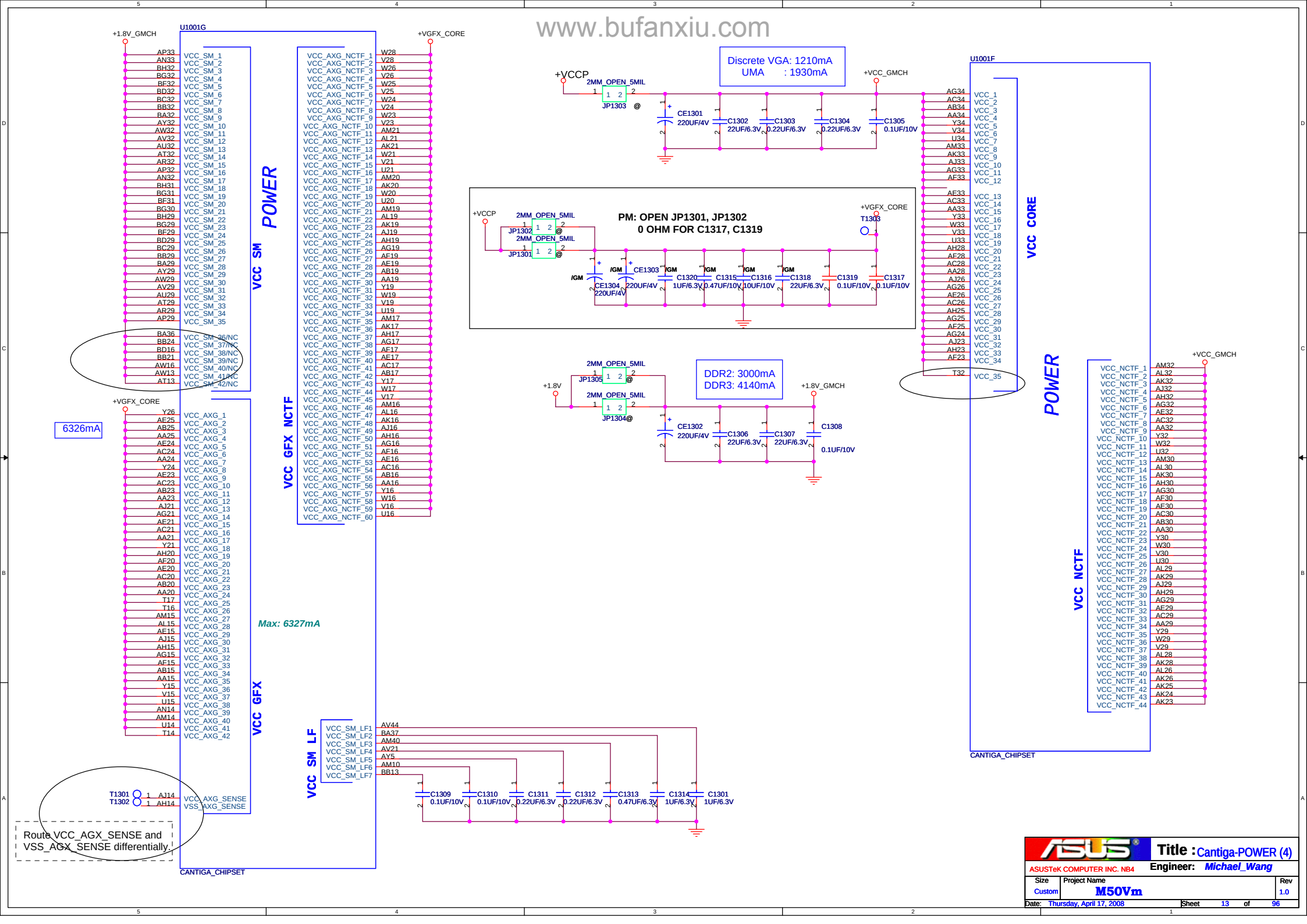
CANTIGA_CHIPSET

Title : Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB4
Engineer: Michael_Wang
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Friday, March 07, 2008
Sheet 11 of 96

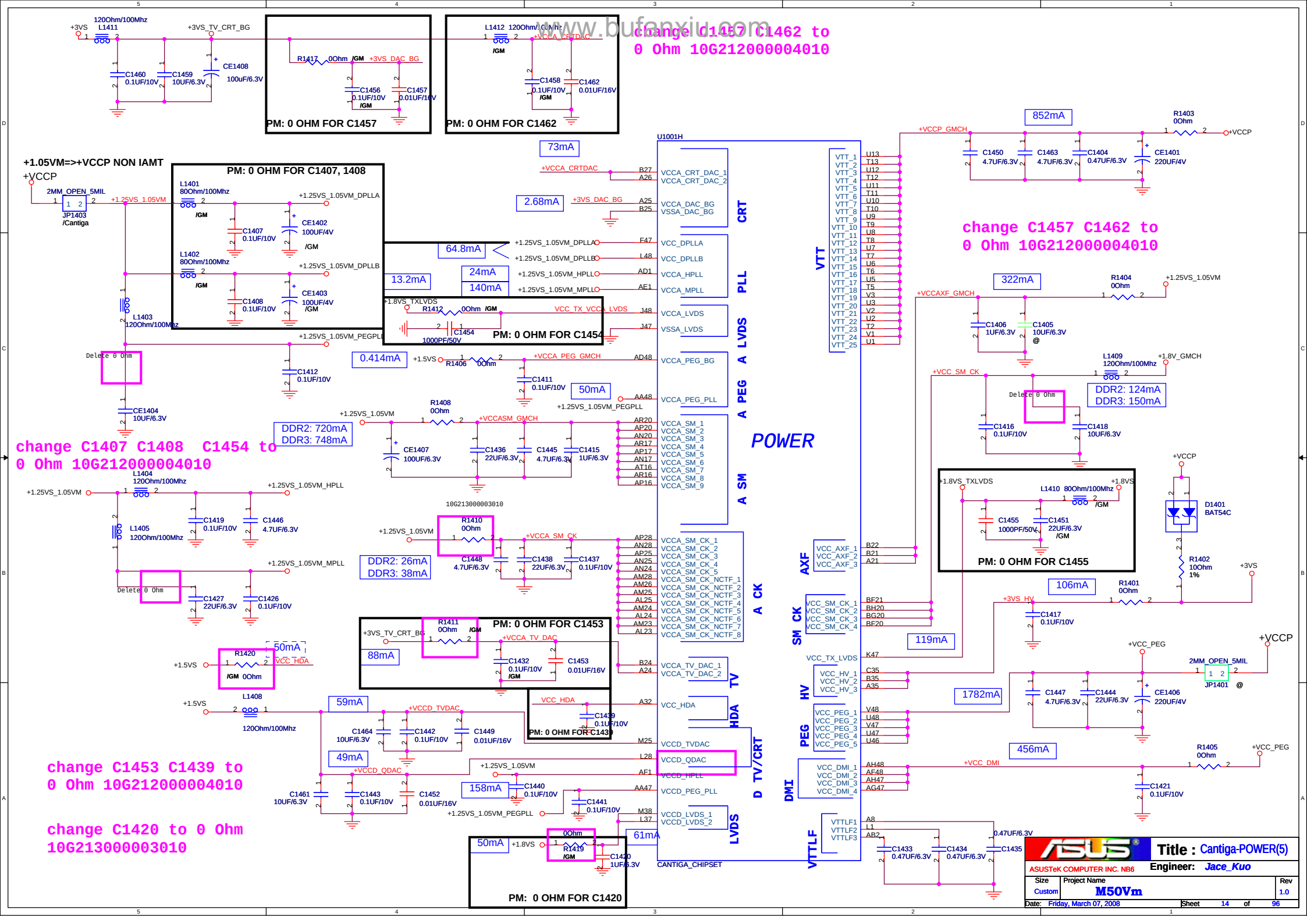




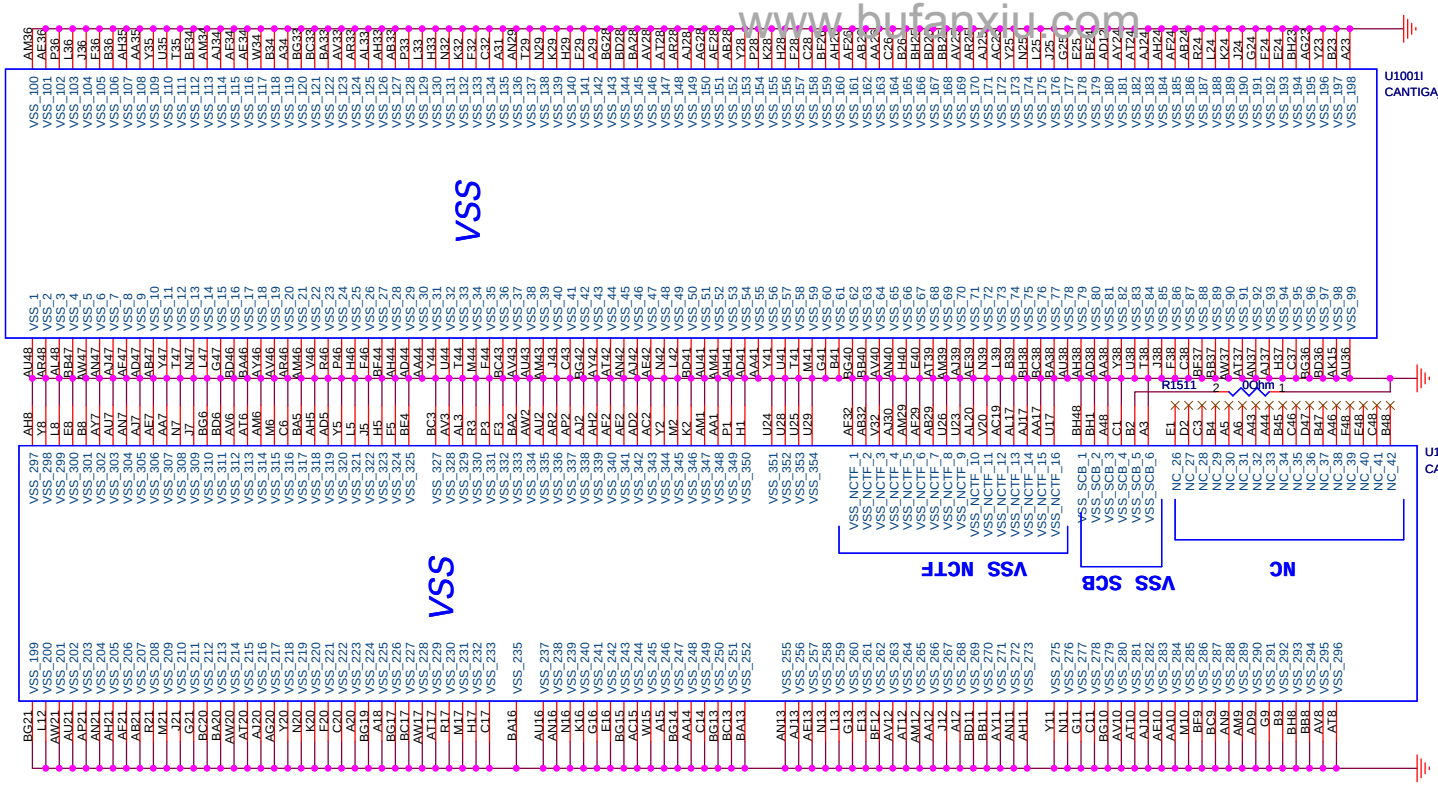
ASUSTeK COMPUTER INC. NB4	Title : Cantiga-DDR2 bus (3)	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 12 of 96	



ASUSTeK COMPUTER INC. NB4	Title : Cantiga-POWER (4)	
	Engineer: Michael_Wang	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 13 of 96	



Title : Cantiga-POWER(5)		
ASUSTeK COMPUTER INC. NB6	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 14 of 96	



11 MCH_CFG_5

R1505 2.21KOhm @

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

11 MCH_CFG_6

R1510 2.21KOhm @

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

11 MCH_CFG_7

R1507 2.21KOhm @

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

11 MCH_CFG_9

R1508 2.21KOhm @

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

11 MCH_CFG_16

R1503 2.21KOhm @

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

11 MCH_CFG_10

R1504 2.21KOhm @

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

11 MCH_CFG_12

R1509 2.21KOhm @

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

11 MCH_CFG_13

R1506 2.21KOhm @

+3VS

R1501 4.02KOHM @

11 MCH_CFG_19

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

+3VS

R1502 4.02KOHM @

11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

ASUSTeK COMPUTER INC. NB4

Title : Cantiga-GND

Engineer: Michael_Wang

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Tuesday, March 04, 2008 Sheet 15 of 96

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 16 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 17 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 18 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 19 of 96	

Time delay 18~25 ms

Place Near the Open Door

LCI/GLCI disable guidelines
Design guide 4.11.19

check memory ID 0

output 24MHz

check MDC series 33 Ohm close to MDC connector

SATA AC coupling Capacitors should be placed at connector side. Design Guide 4.1.5

Delete

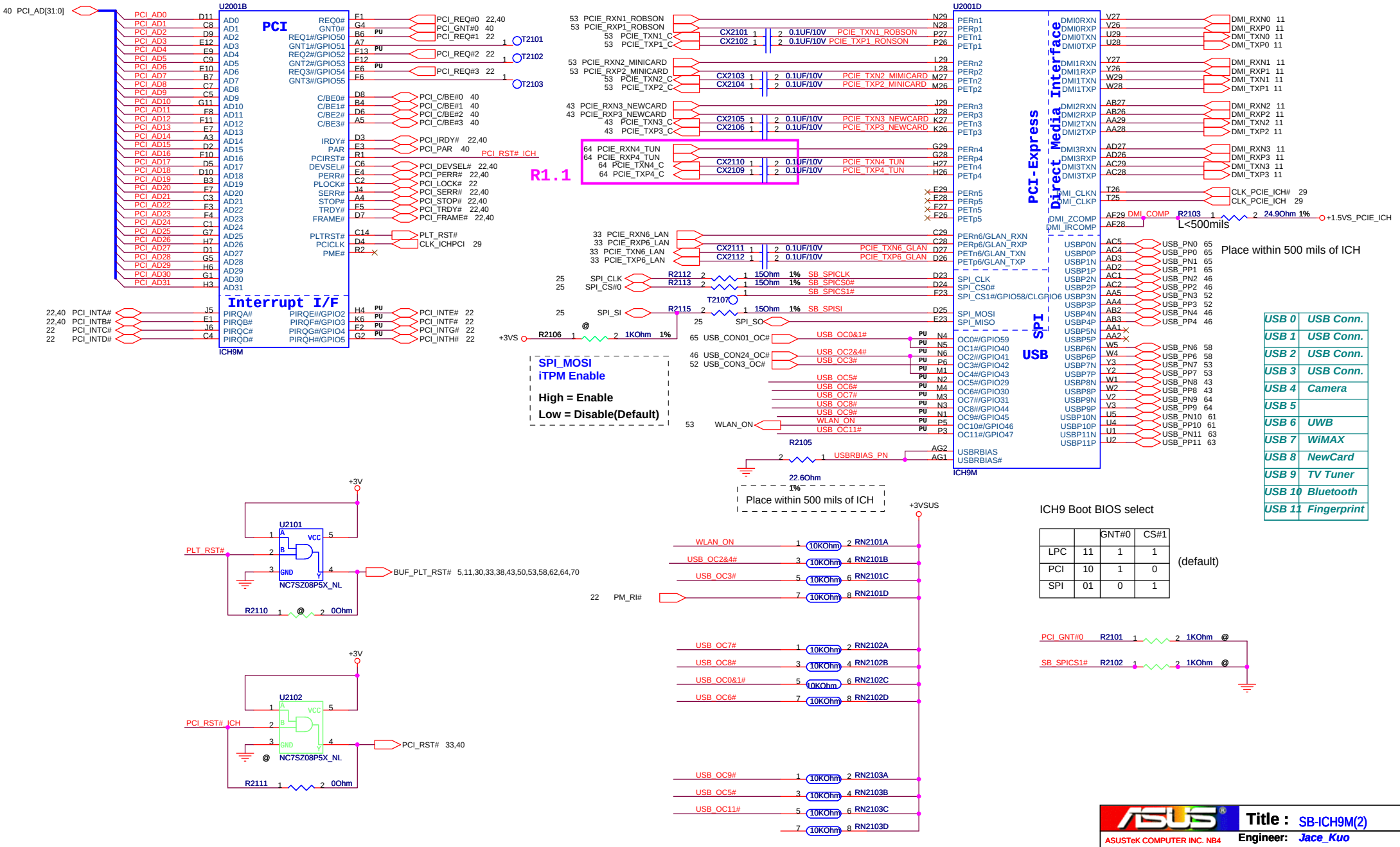
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable

VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1

Change Battery Holder to N1S

Title :	SB-ICH9M(1)		
ASUSTeK COMPUTER INC. NB4	Engineer:	Jace_Kuo	
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 20 of 96		



		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

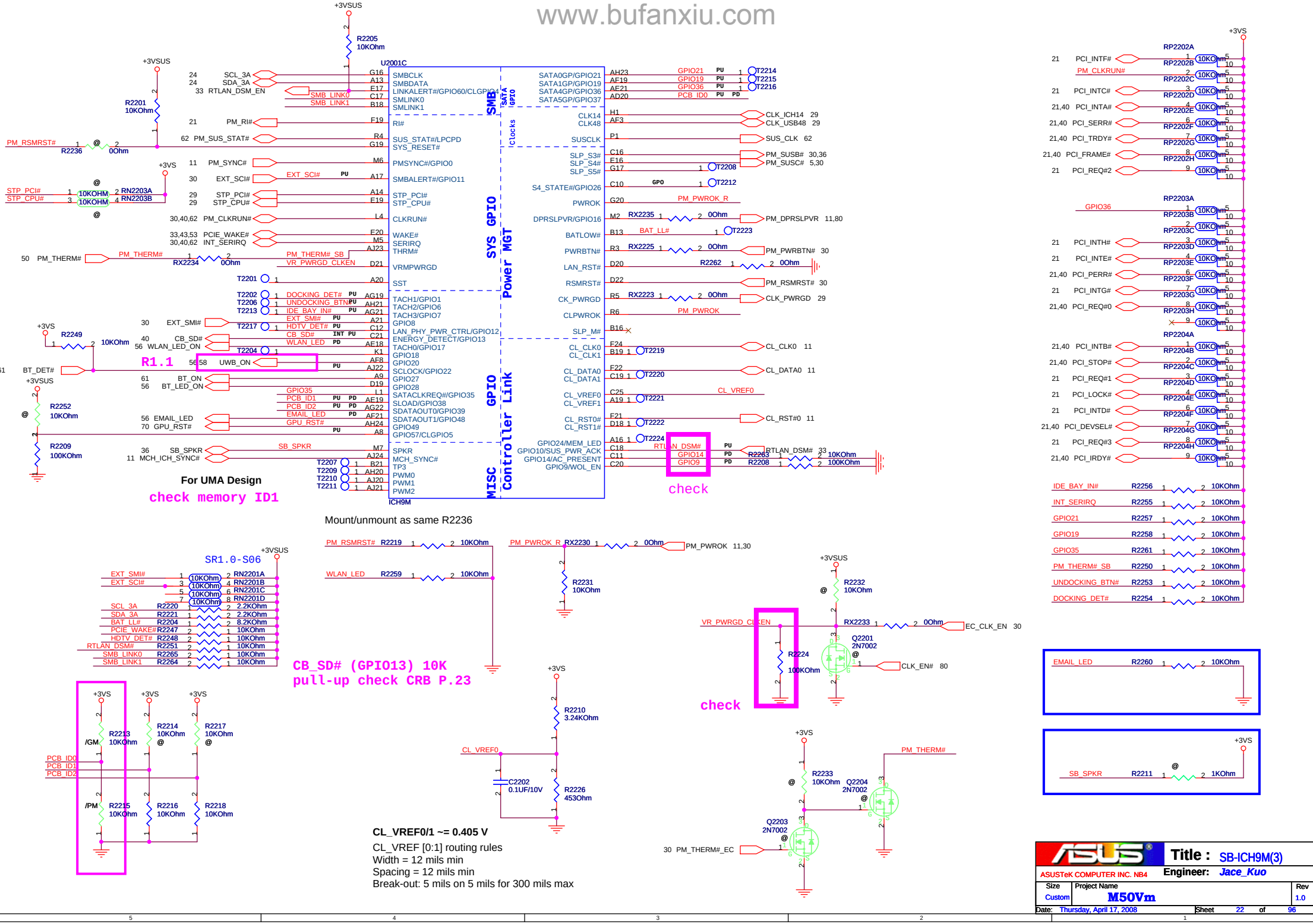
ASUSTeK COMPUTER INC. NB4

Title : SB-ICH9M(2)

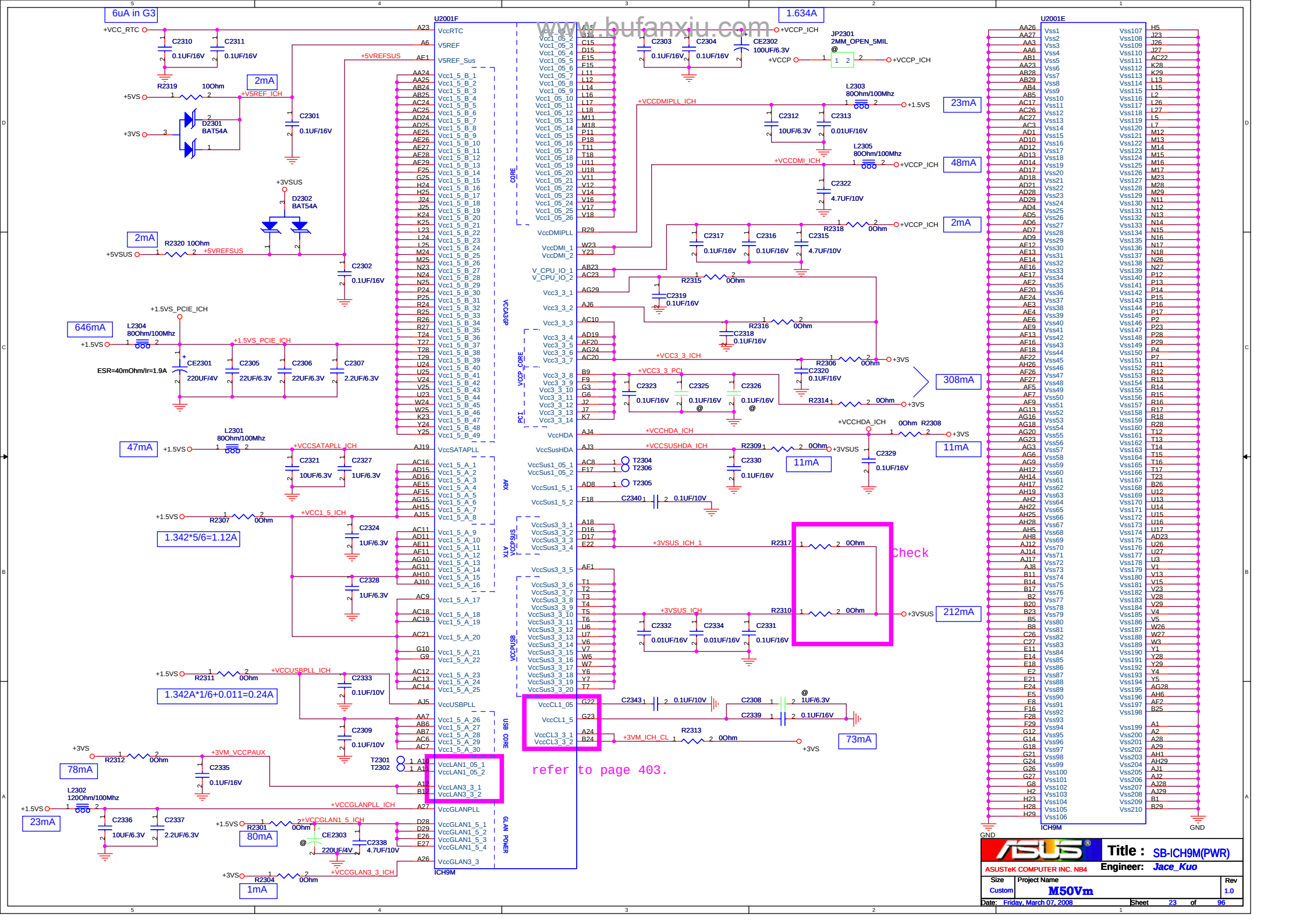
Engineer: Jace_Kuo

Size	Project Name	Rev
Custom	M50Vm	1.0

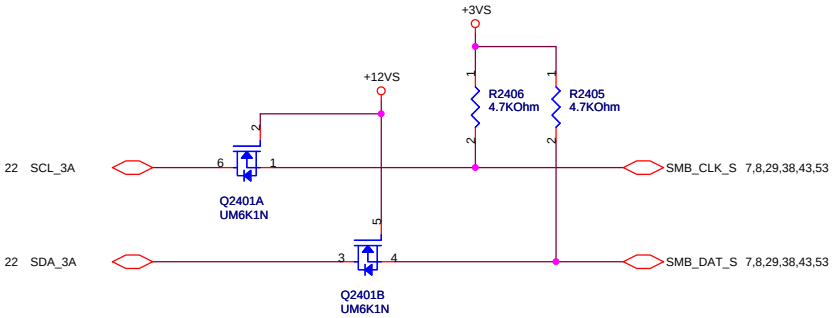
Date: Friday, March 07, 2008 Sheet 21 of 96



Title :	SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB4	Engineer: Jace_Kuo
Size: Custom	Project Name: M50Vm
Rev: 1.0	
Date: Thursday, April 17, 2008	Sheet 22 of 96


6uA in G3
1.634A
2mA
2mA
2mA
646mA
47mA
1.342*5/6=1.12A
1.342A*1/6+0.011=0.24A
78mA
23mA
80mA
1mA
23mA
48mA
2mA
308mA
11mA
11mA
212mA
73mA
Check
refer to page 403.
www.bufanxiu.com
U2001F
U2001E
ICH9M
Title : SB-ICH9M(PWR)
ASUSTeK COMPUTER INC. NB4
Engineer: Jace_Kuo
Project Name M50Vm
Date: Friday, March 07, 2008
Sheet 23 of 96

ICH9-M

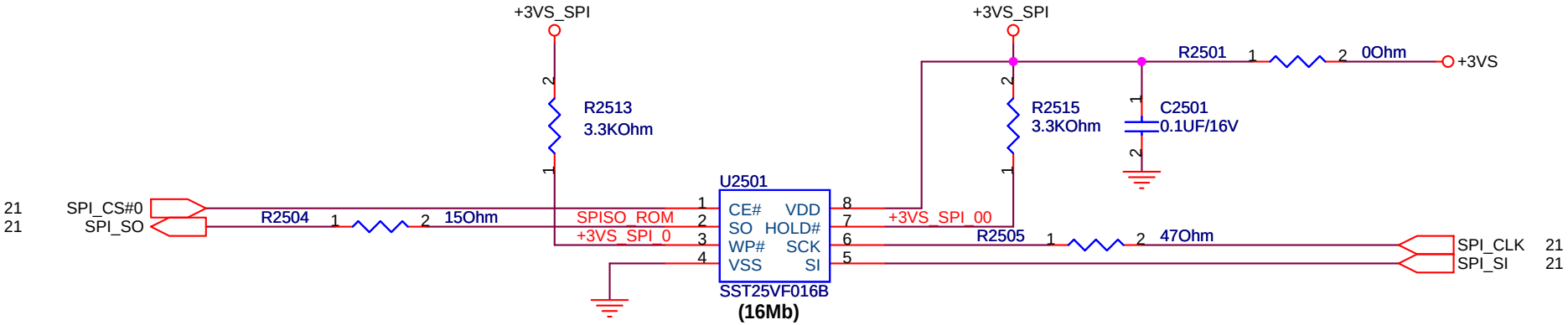


7 SO-DIMM0
8 SO-DIMM1
29 CLK-GEN
39 AUD-DSP
43 NEWCARD
53 WLAN

EC-IT8752

Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S SMB_DAT_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card B. SMB_CLK_M SMB_DAT_M → CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor

ASUSTeK COMPUTER INC. NB4	Title : ICH9M-Other	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 24 of 96	



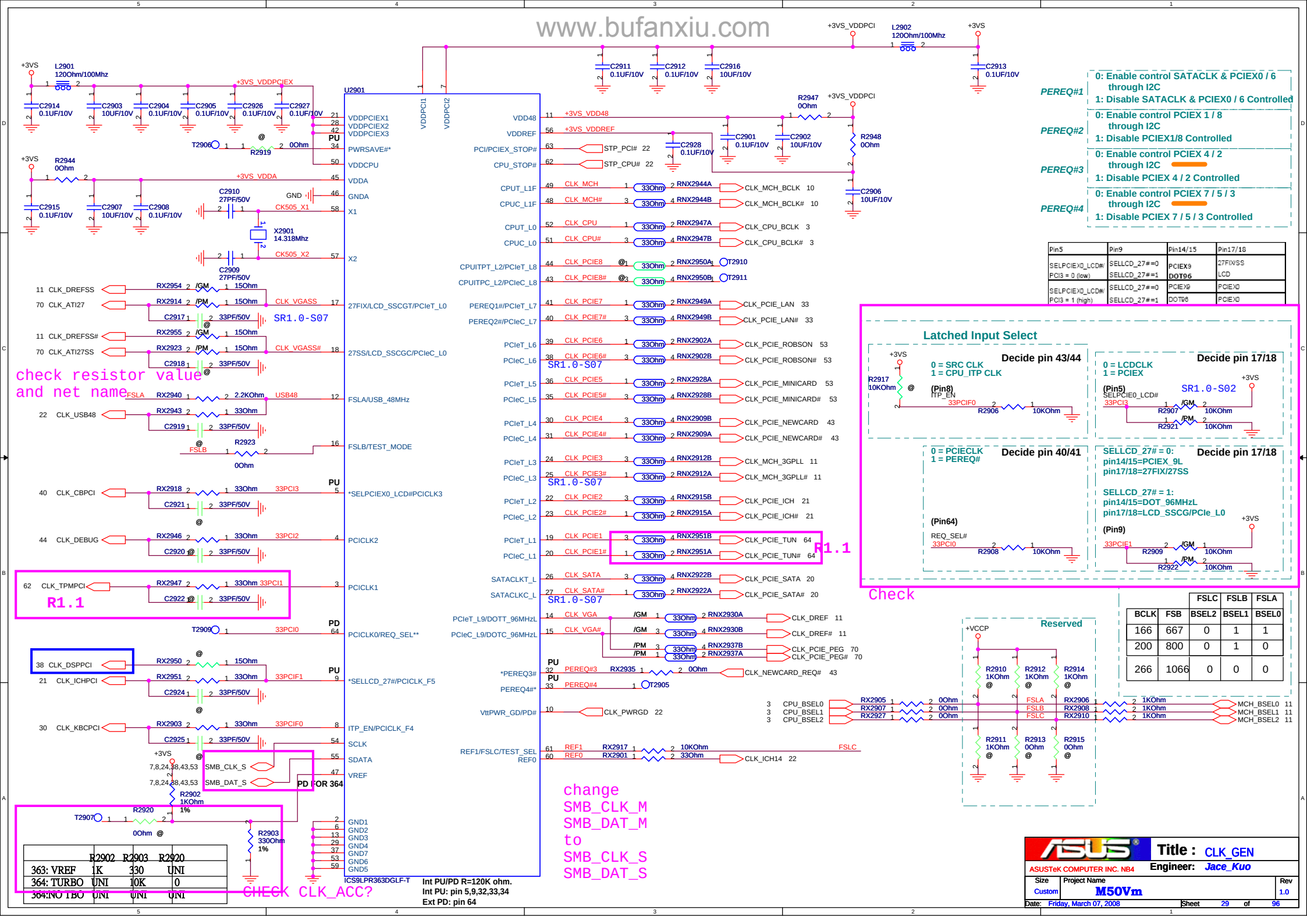
FOR iTPM

ASUSTeK COMPUTER INC. NB4	Title : SPI ROM	
	Engineer: Jace_Kuo	
Size: A	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 25 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 26 of 96	

ASUSTeK COMPUTER INC. NB6	Title :	Engineer: Raphael_Chen
Size: A	Project Name: M50Vm	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 27 of 96	

ASUSTeK COMPUTER INC. NB6	Title :	Engineer: Raphael_Chen
Size: A	Project Name: M50Vm	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 28 of 96	

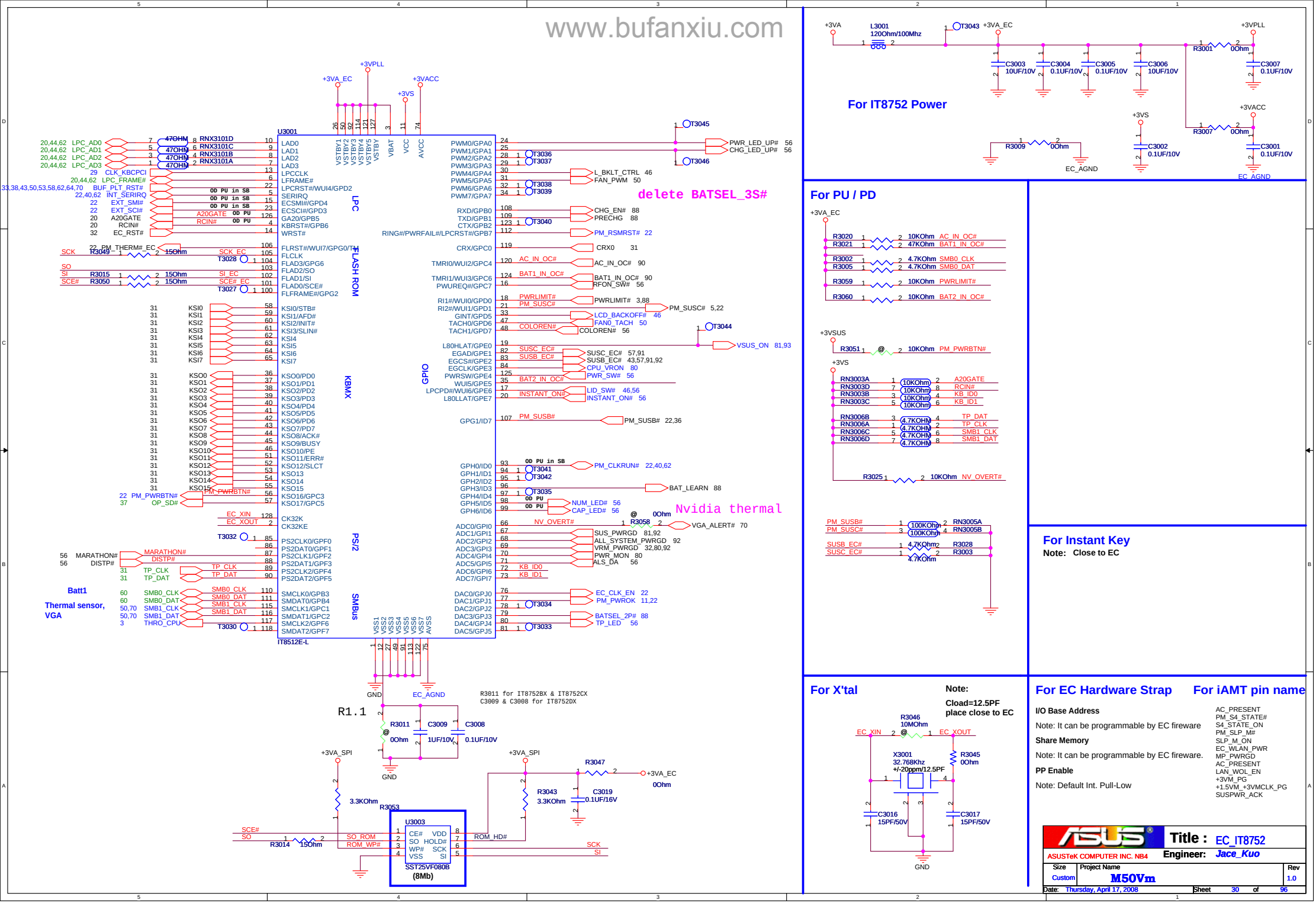


Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD# PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9 DOT96	27FIXSS LCD
	SELLCD_27#=1		
SELPCIEX0_LCD# PCI3 = 1 (high)	SELLCD_27#=0	PCIEX9	PCIEX0
	SELLCD_27#=1	DOT96	PCIEX0

BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO	UNI	10K	0
364:NO TBO	UNI	UNI	UNI

Title :	CLK_GEN
Engineer:	Jace_Kuo
ASUSTeK COMPUTER INC. NB4	
Size: Custom	Project Name: M50Vm
Rev:	1.0
Date: Friday, March 07, 2008	Sheet 29 of 96



ASUSTeK COMPUTER INC. NB4

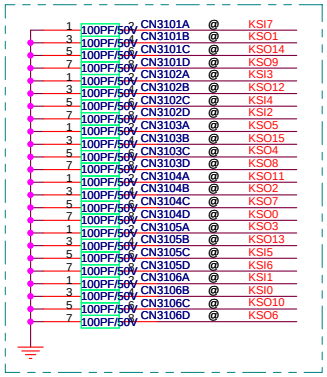
Title : EC_IT8752

Engineer: Jace_Kuo

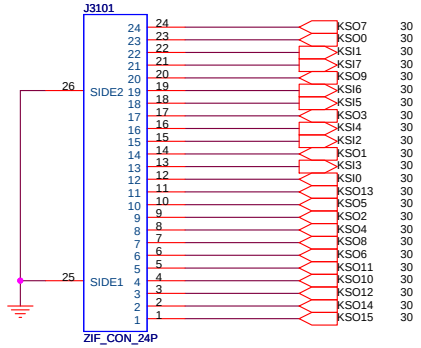
Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Thursday, April 17, 2008 Sheet 30 of 96

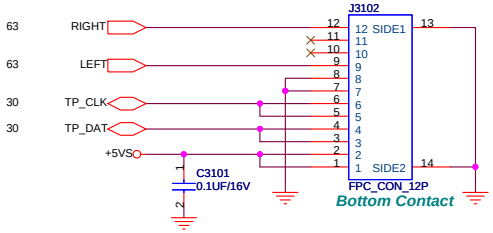
EMI



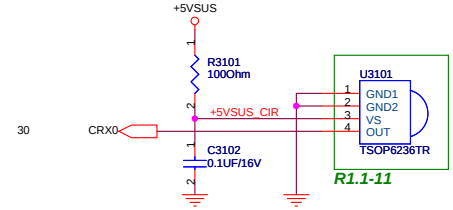
Keyboard



Touchpad



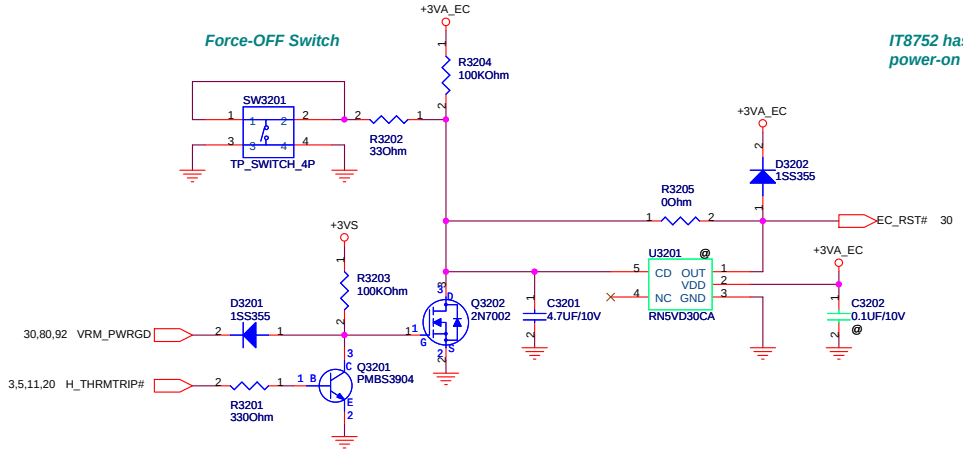
CIR



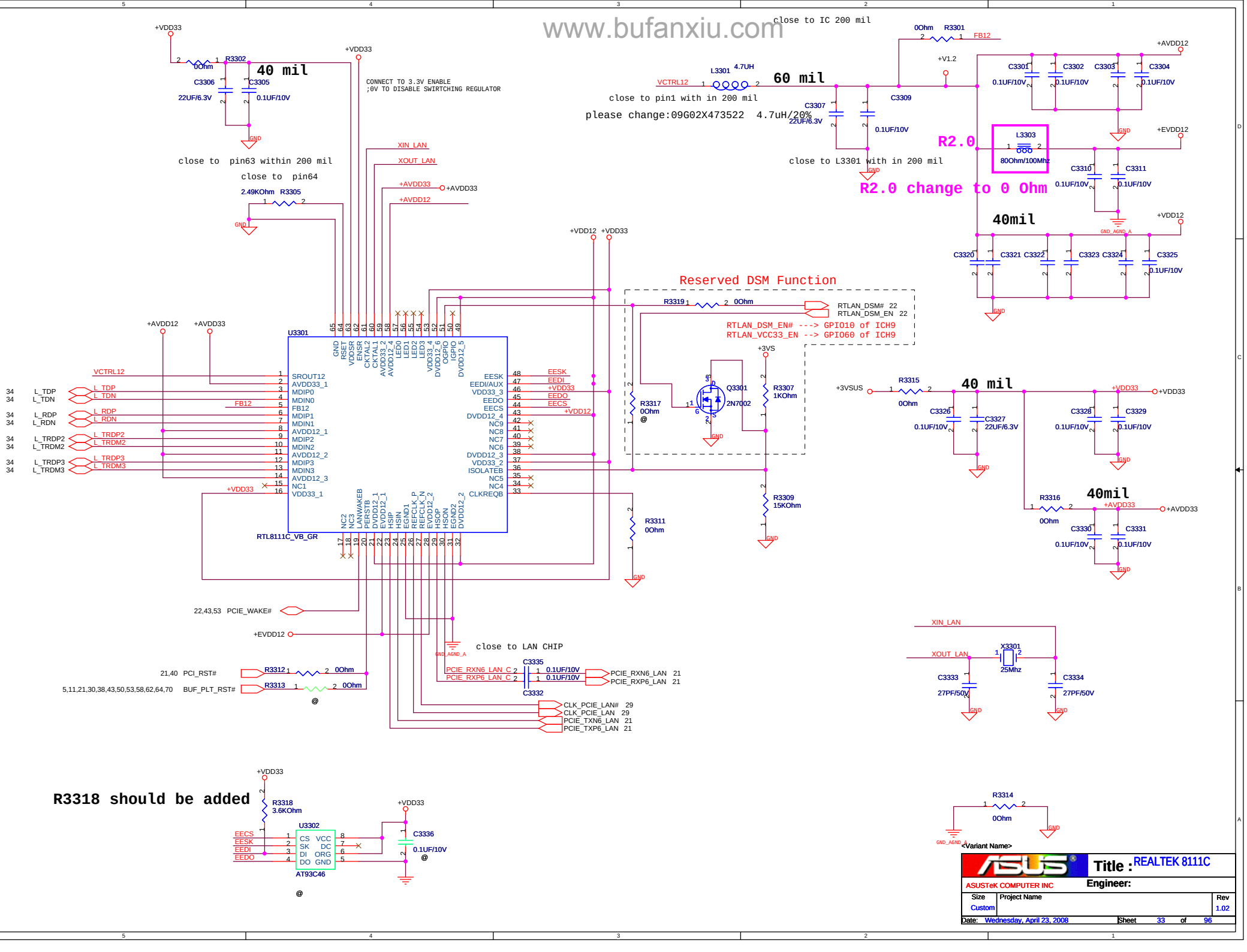
ASUSTeK COMPUTER INC. NB1	Title : KBC_KB, TP & CIR	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 31 of 96	

Force-OFF Switch

IT8752 has built-in level detection for power-on reset circuit



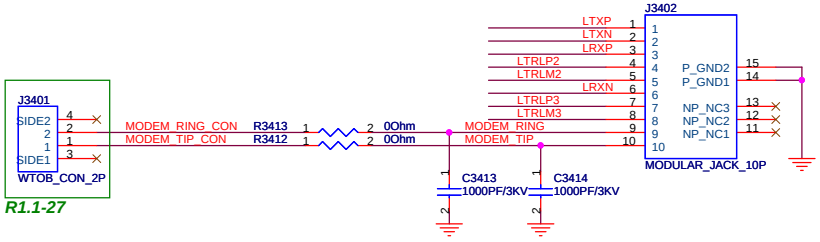
ASUSTeK COMPUTER INC. NB1	Title : RST_Reset Circuit	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 32 of 96	



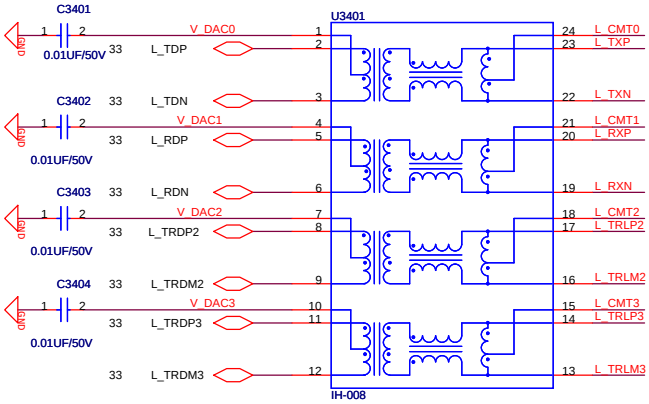
<Variant Name>

ASUSTeK COMPUTER INC	Title : REALTEK 8111C	
	Engineer:	
Size: Custom	Project Name	Rev: 1.02
Date: Wednesday, April 23, 2008	Sheet 33 of 96	

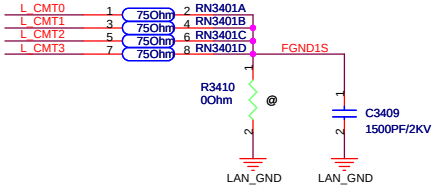
N1S Check connector to follow N1S or not

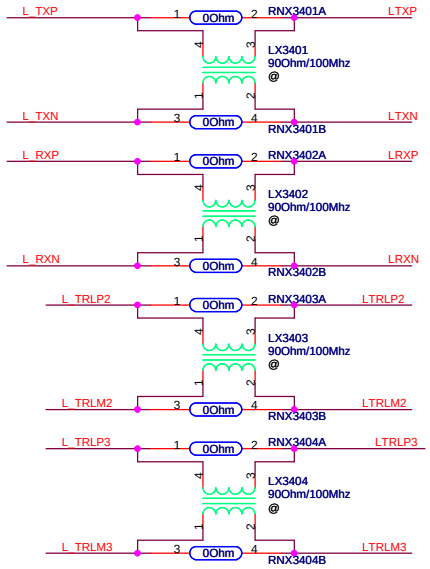


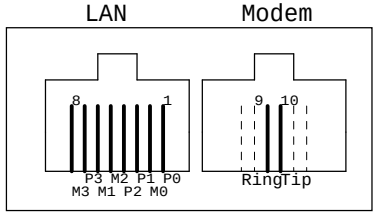
R1.1-27

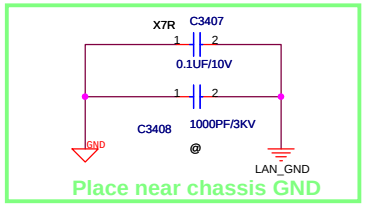


Transformer close CN3402









<Variant Name>

Title : IO

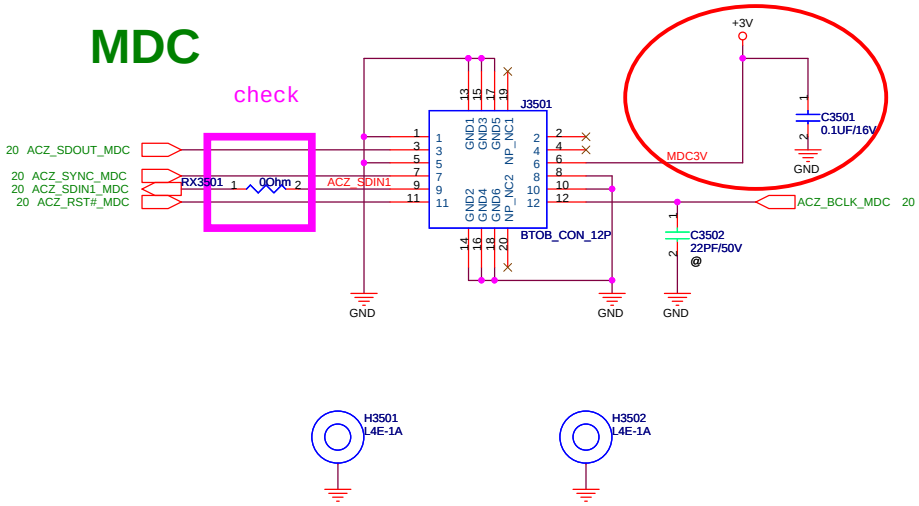
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom		1.01

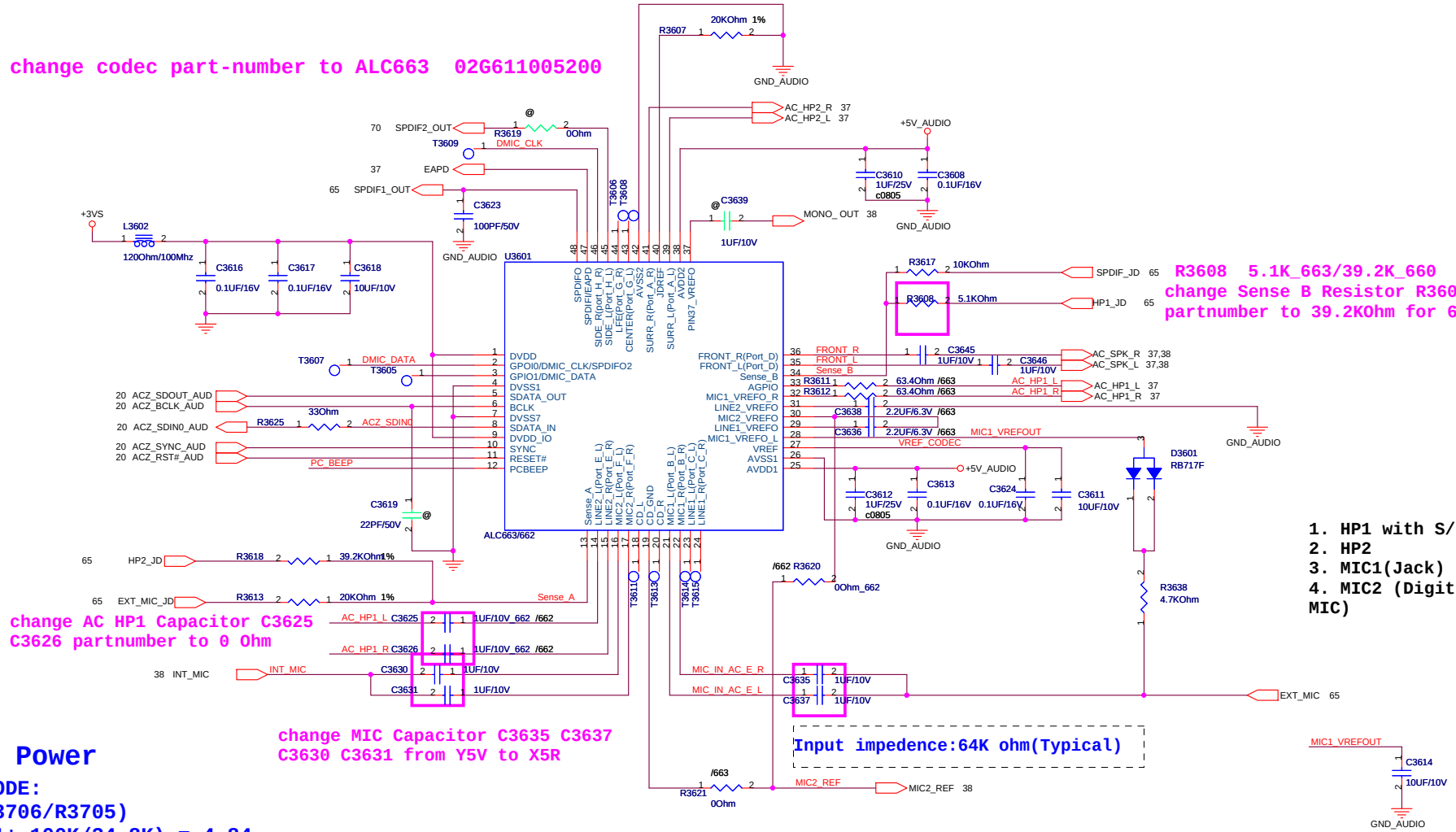
Date: Wednesday, April 16, 2008 Sheet 34 of 96

MDC



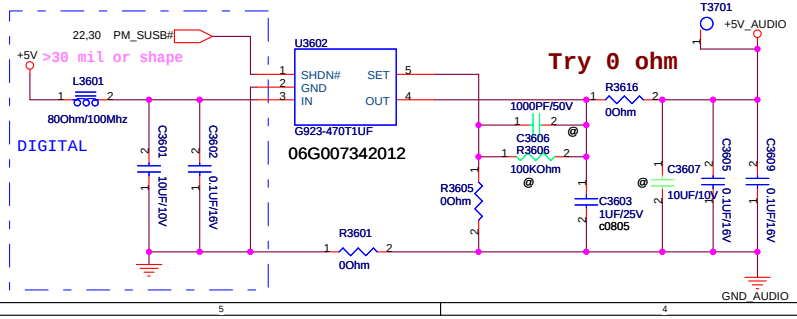
ASUSTeK COMPUTER INC	Title : MDC	
	Engineer: Borland_Huang	
Size: Custom	Project Name: M50Vm	Rev: 1.01
Date: Friday, March 07, 2008	Sheet 35 of 96	

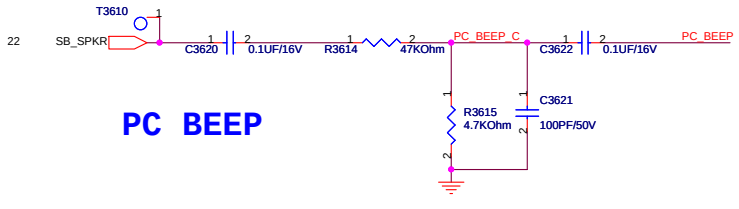
change codec part-number to ALC663 02G611005200

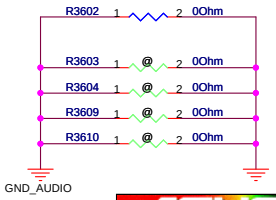


Audio Power

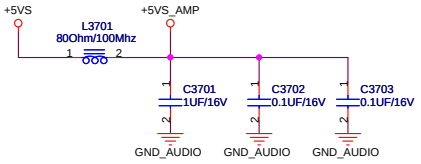
FOR ADJUST MODE:
Vo=1.25*(1+R3706/R3705)
= 1.25*(1+ 100K/34.8K) = 4.84

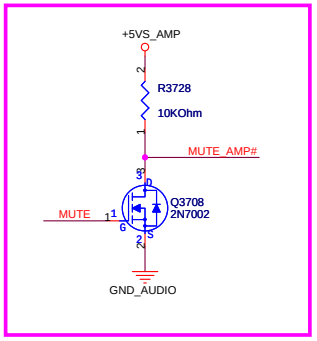




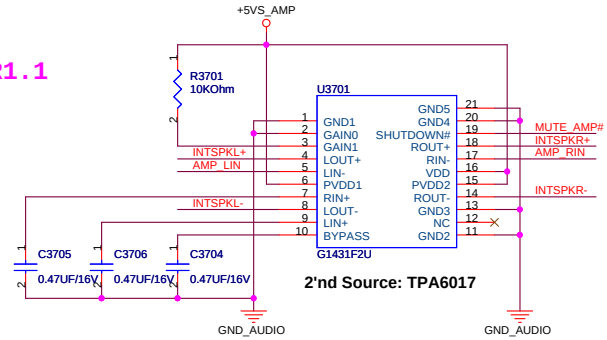


Title : CODEC ALC663		
Engineer:		
Size: Custom	Project Name	Rev: 1.1
Date: Thursday, April 17, 2008	Sheet 36 of 96	





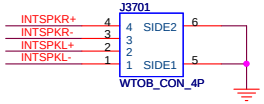
R1.1



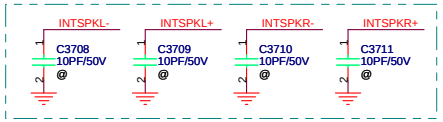
2'nd Source: TPA6017

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

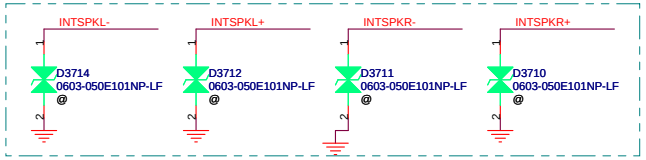
Internal Speaker Conn.

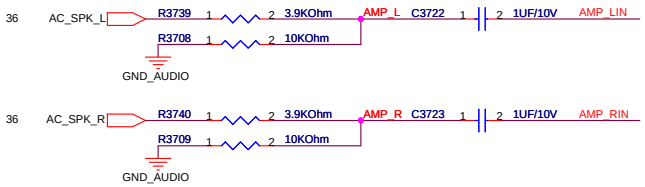


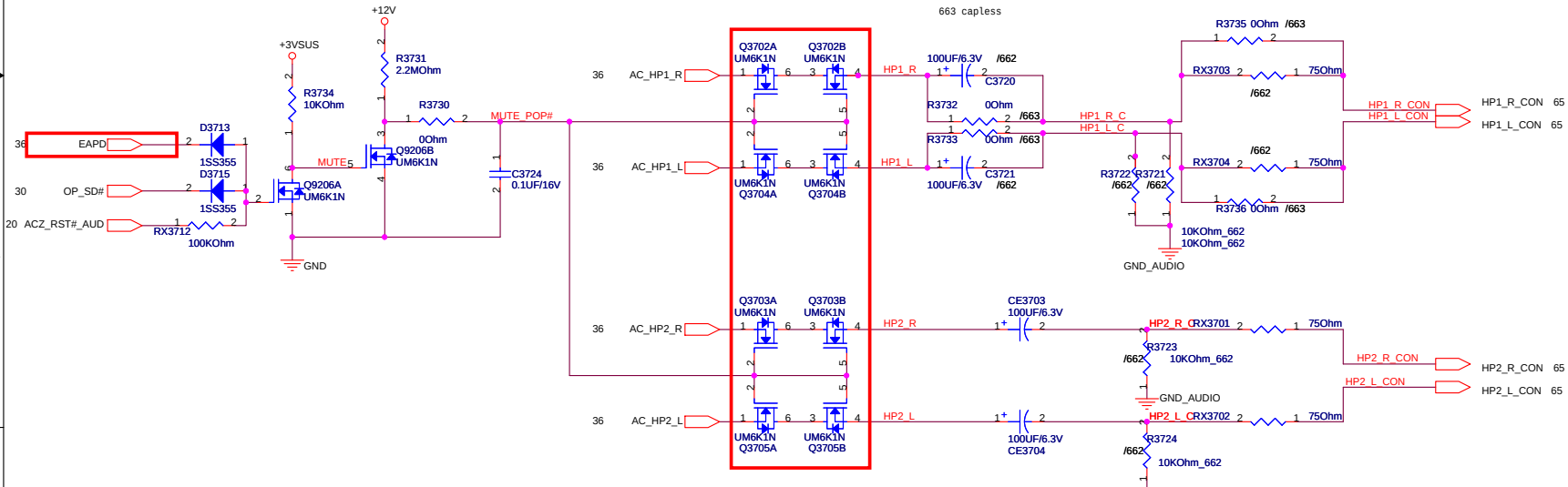
Reserved for 3G



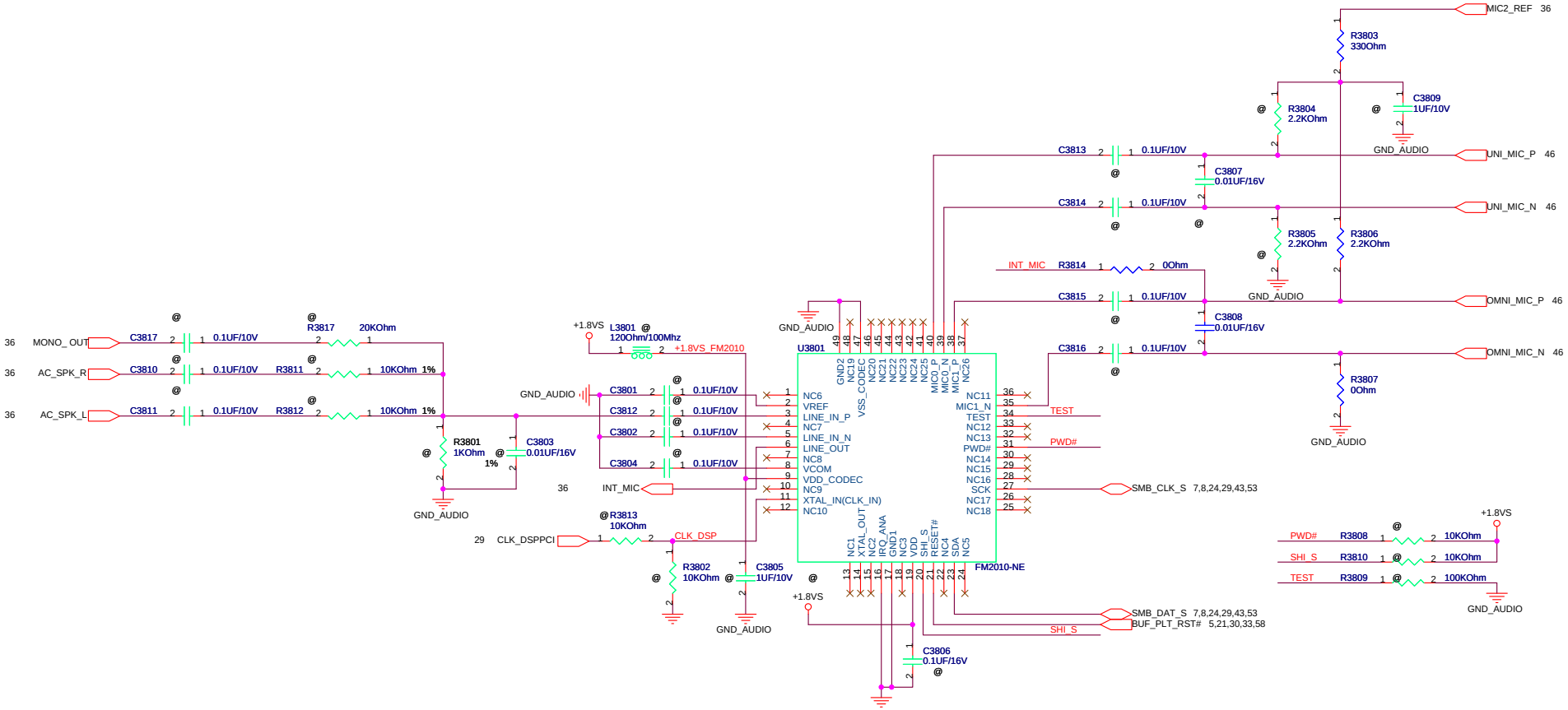
Reserved for EMI







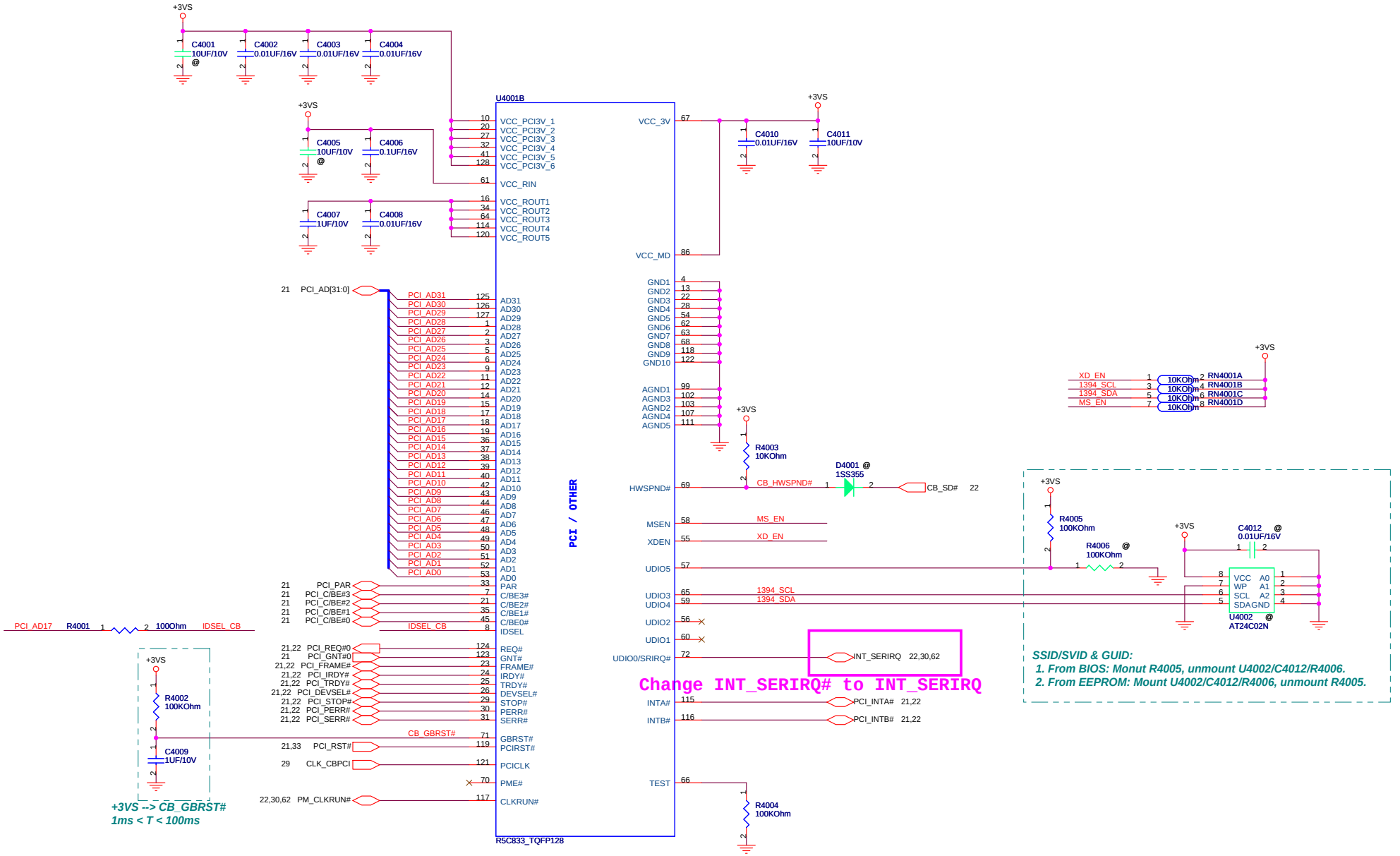
ASUS	Title : AUD_Amp & Jack		
	Engineer:		
Size: Custom	Project Name		Rev: 1.0
Date: Friday, March 07, 2008	Sheet 37 of 96		



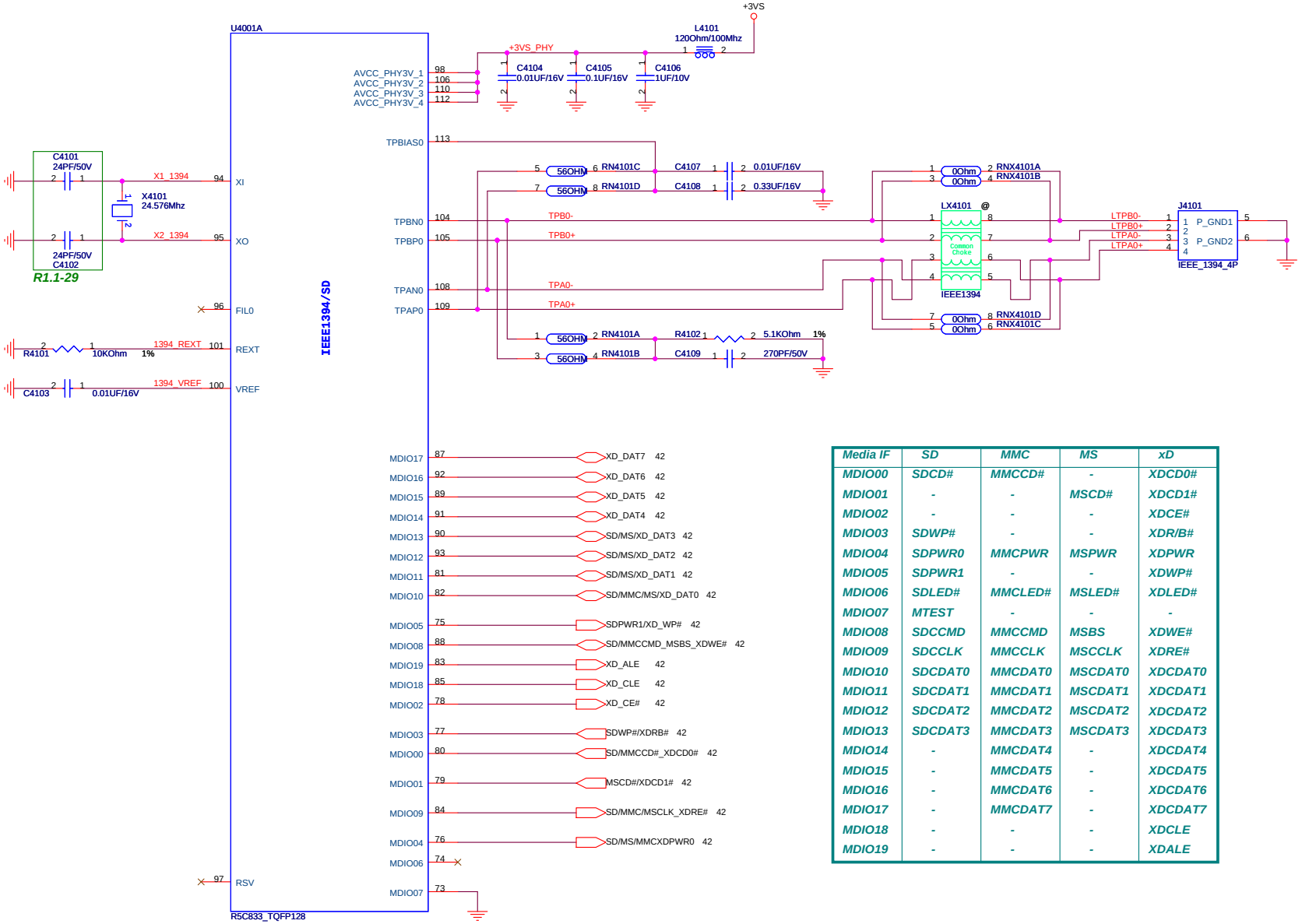
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 38 of 96	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : AUD_****	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 39 of 96	

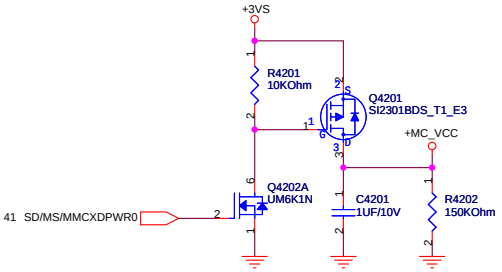


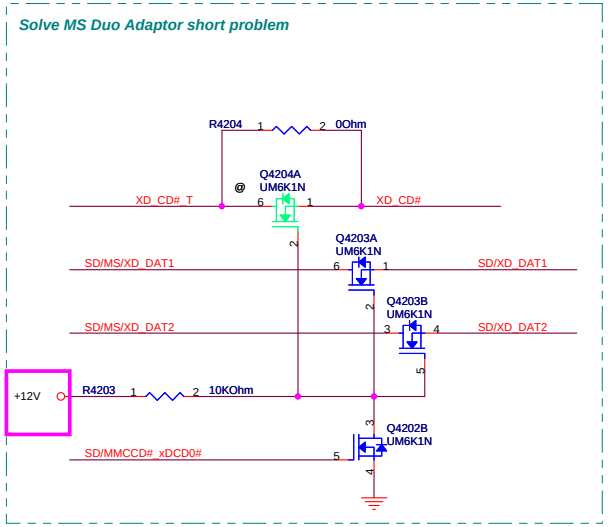
ASUSTeK COMPUTER INC. NB1	Title : CB_R5C833	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 40 of 96	

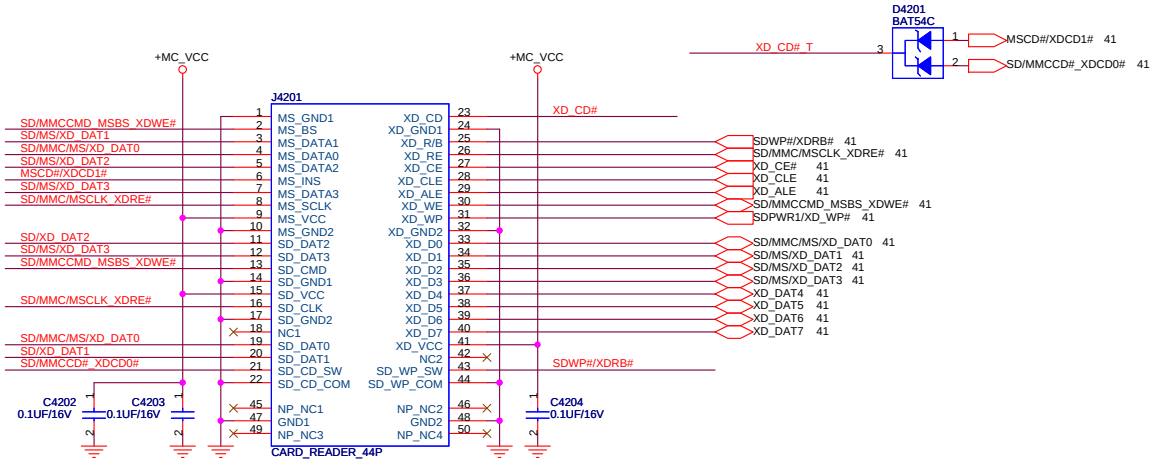


Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XDCLE
MDIO19	-	-	-	XDALE

Title : CB_R5C833		
ASUSTeK COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 41 of 96	







ASUSTeK COMPUTER INC. NB1

Title : CB_4in1 CardReader

Engineer: John Hung

Size	Project Name	Rev
Custom	M50Vm	1.0

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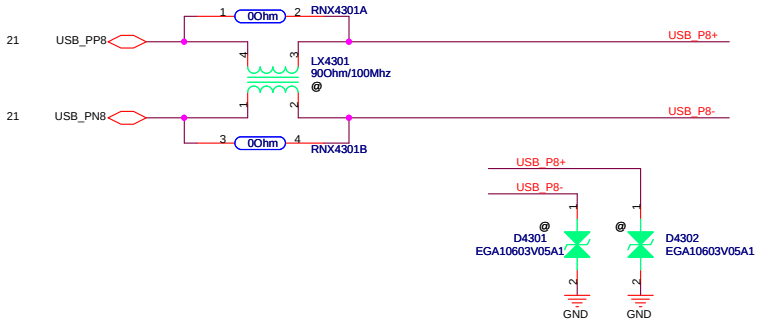
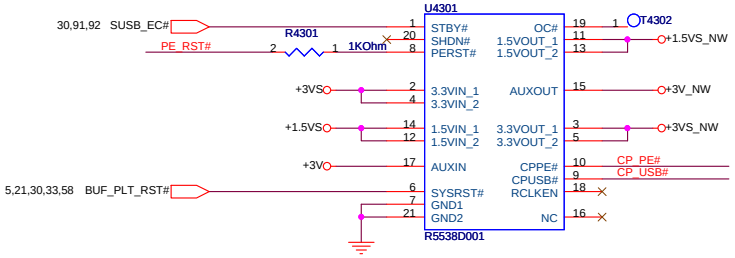
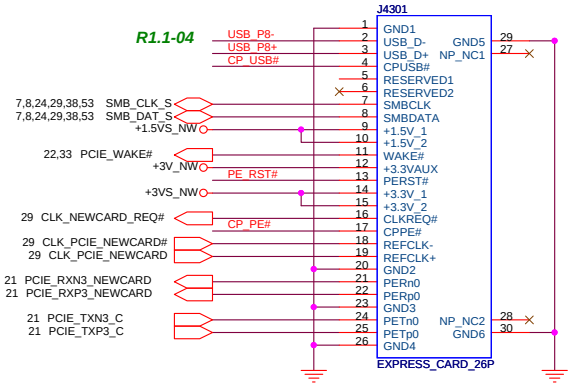


R1.1-04

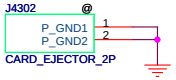


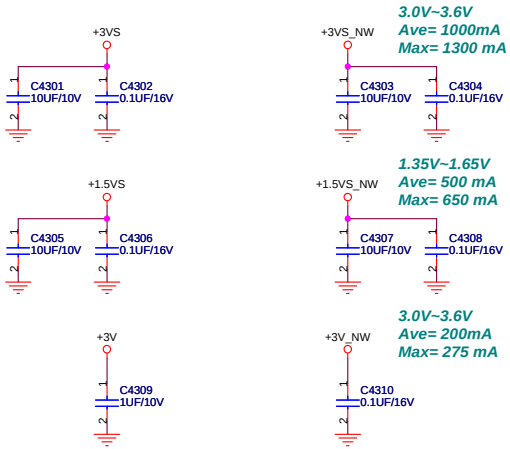
NewCard Header

R1.1-04



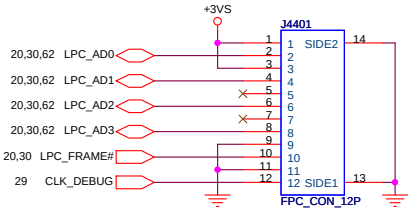
NewCard Ejecter





ASUSTeK COMPUTER INC. NB1	Title : CB_NewCard	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 43 of 96	

LPC Debug Port



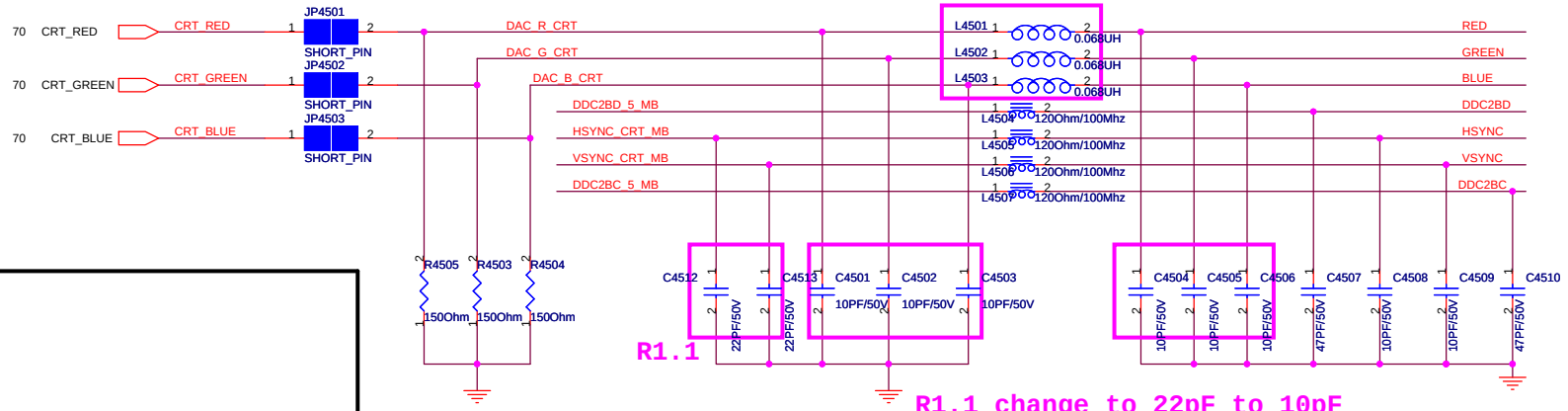
Bottom Contact

For NewCard Debug Card

Delete

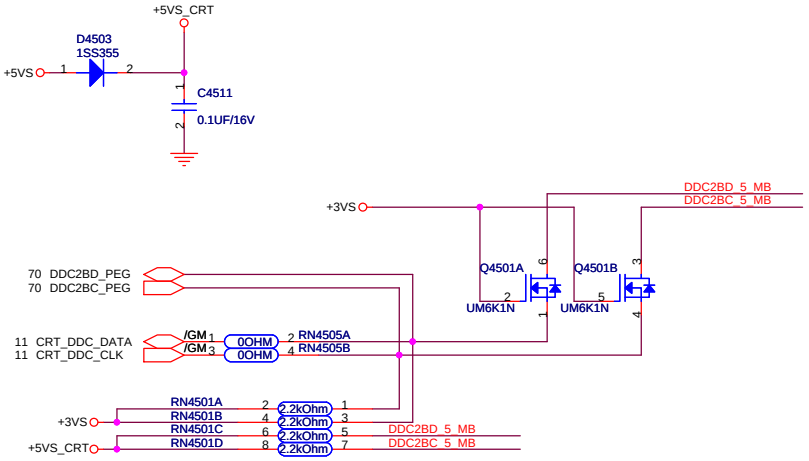
ASUSTeK COMPUTER INC. NB1	Title : BUG_LPC Debug	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 44 of 96	

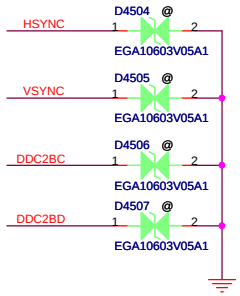
R1.1 change to 0.068uH



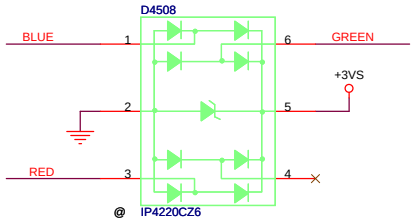
R1.1 change to 22pF to 10pF

MXM CONNECTOR SIDE

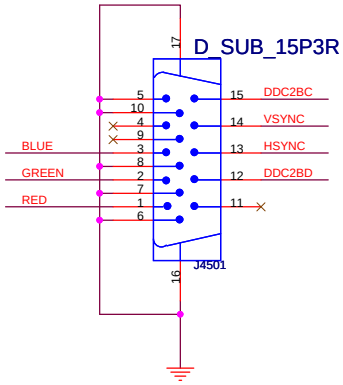


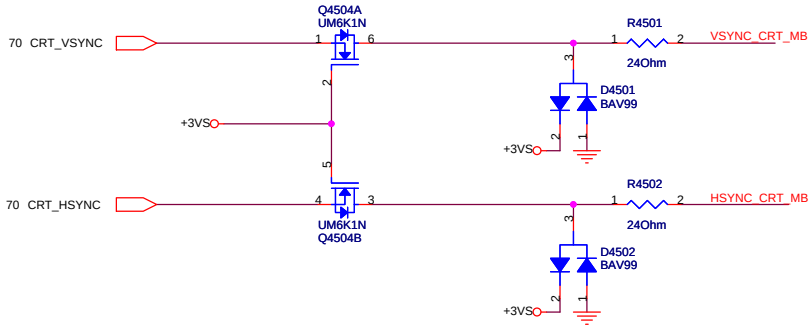


PLACE ESD Diodes near VGA port

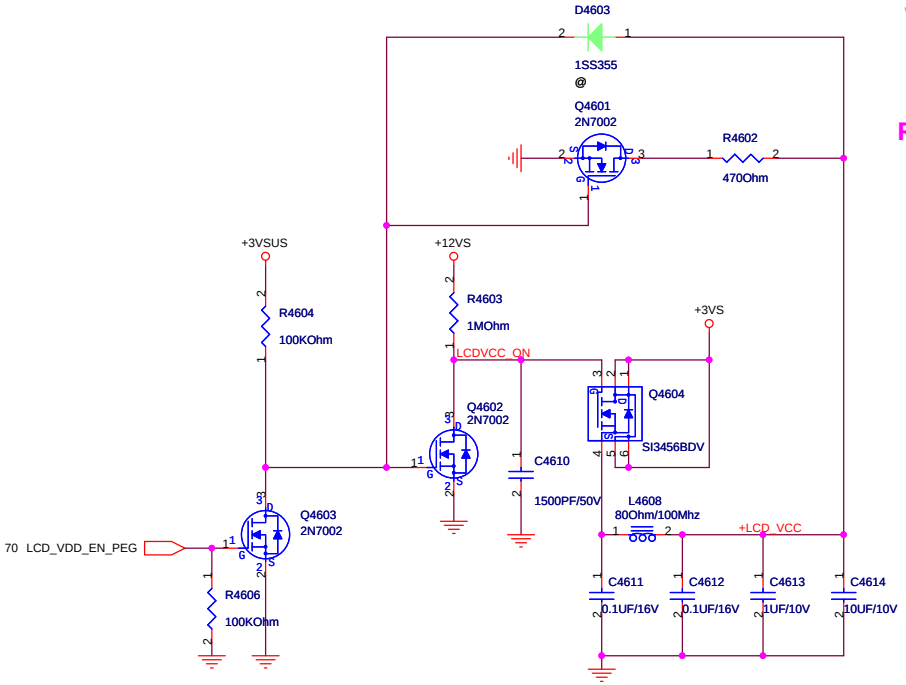


12G101102155

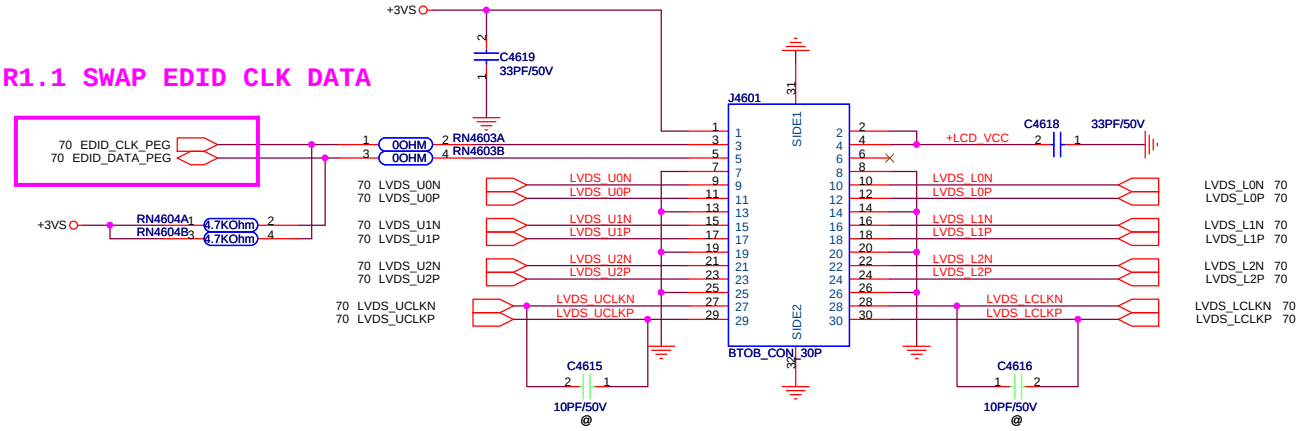




ASUSTeK COMPUTER INC. NB6	Title : CRT	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 45 of 96	

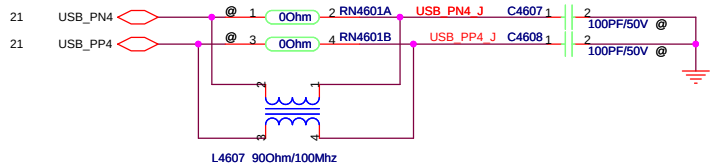


R1.1 SWAP EDID CLK DATA

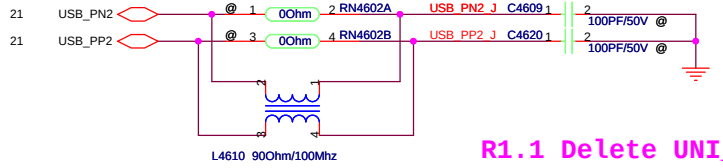


LVDS CNT

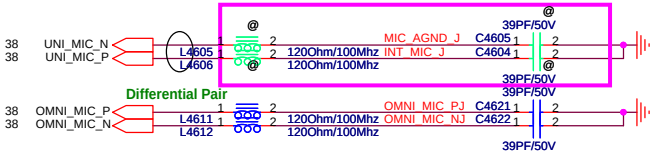
CAMERA MODULE



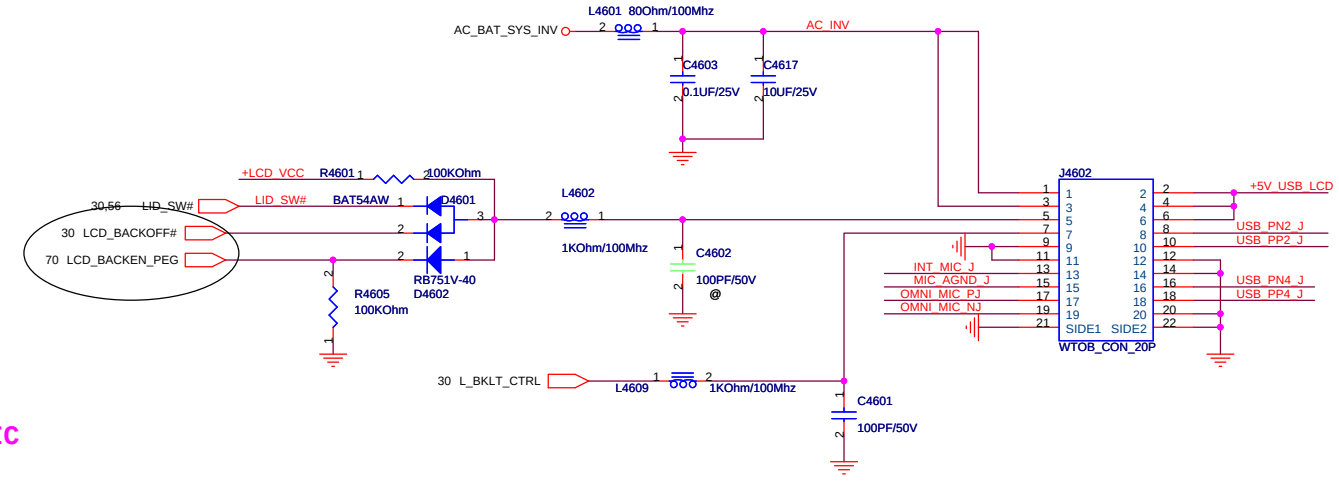
CAMERA MODULE

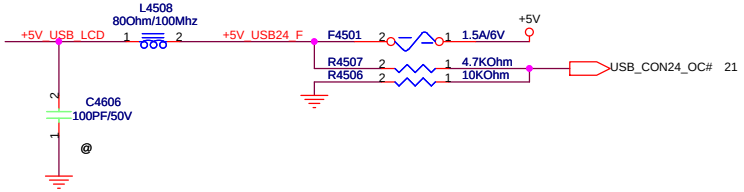


R1.1 Delete UNI_MIC



INVERTOR CNT





ASUSTeK COMPUTER INC. NB6	Title: LVDS & Inverter CON	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 46 of 96	

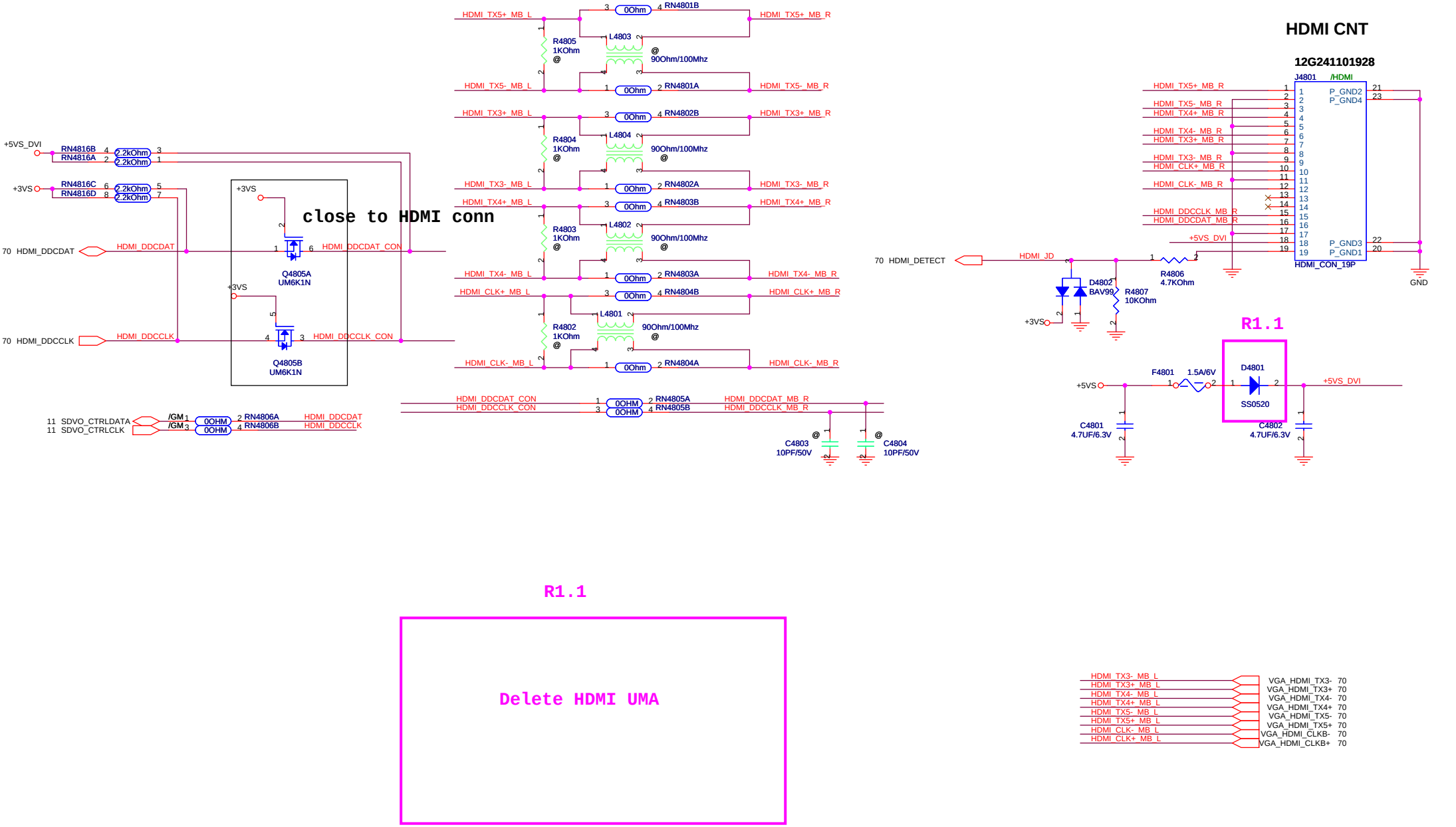
Title : TV_OUT CON

ASUSTeK COMPUTER INC. NB6

Engineer: Jace_Kuo

Size	Project Name	Rev
Custom	M50Vm	1.0

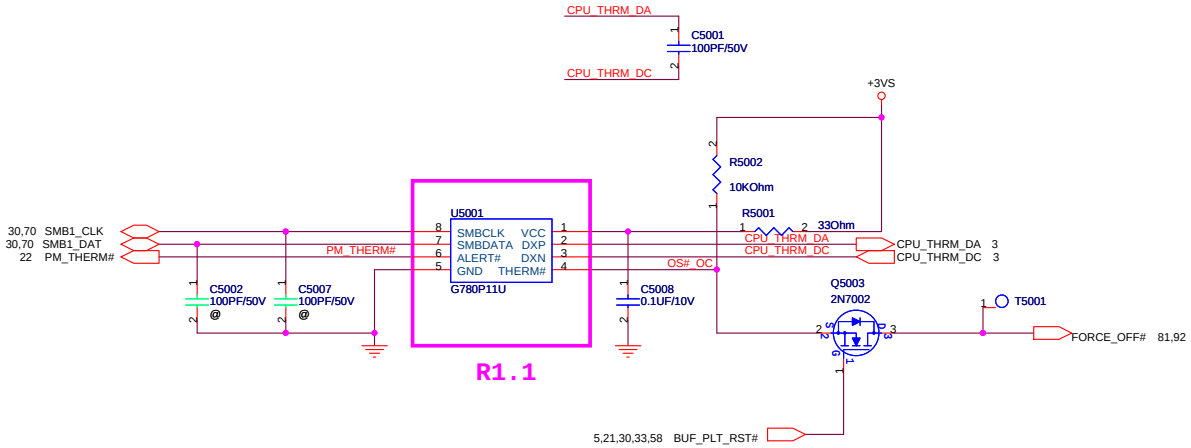
Date: Wednesday, February 13, 2008 Sheet 47 of 96



ASUSTeK COMPUTER INC. NB6	Title: LVDS & Inverter CON	
	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 48 of 96	

ASUSTeK COMPUTER INC. NB6	Title :	Engineer: Jace_Kuo	
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 49 of 96		

Thermal Sensor

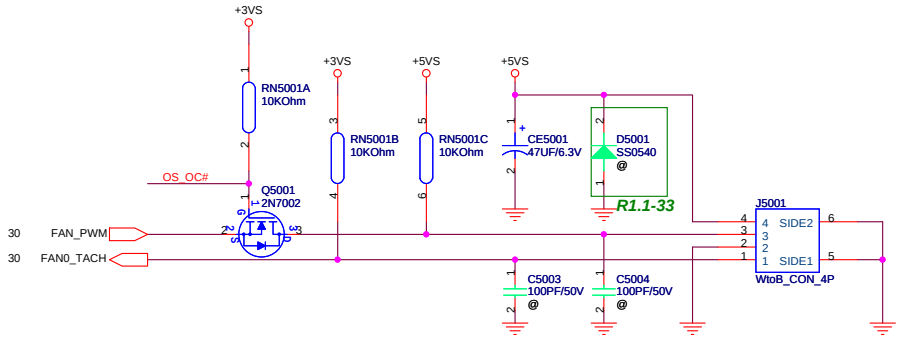


R1.1

SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1
degree

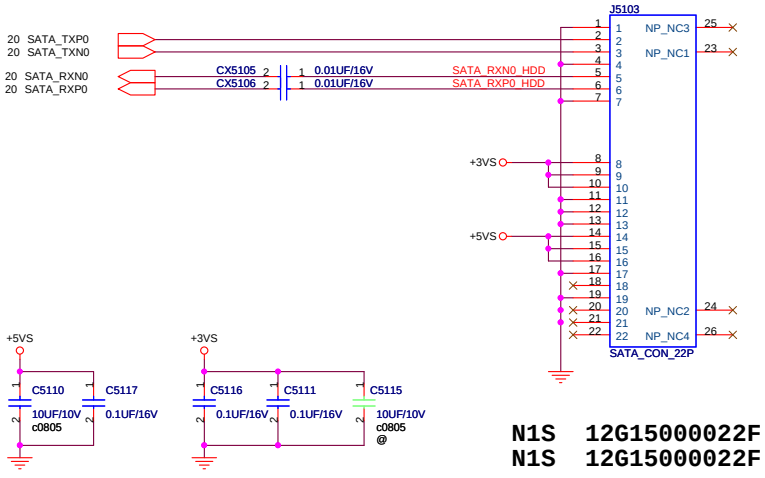
SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1
degree

PWM Fan



ASUSTeK COMPUTER INC. NB1	Title : FAN_Fan & Sensor	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 50 of 96	

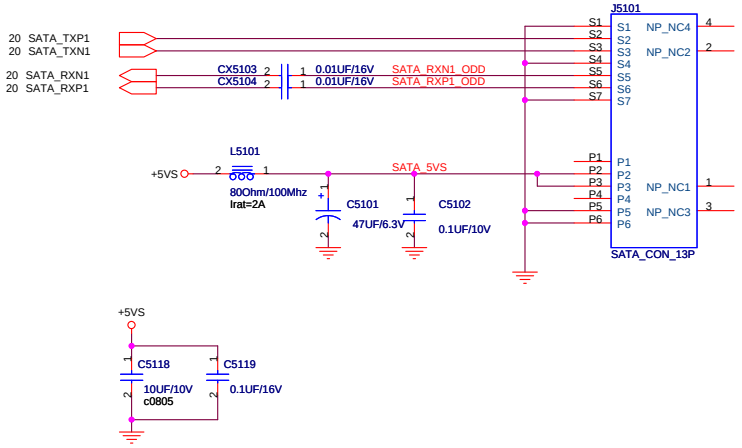
SATA0 HDD CON



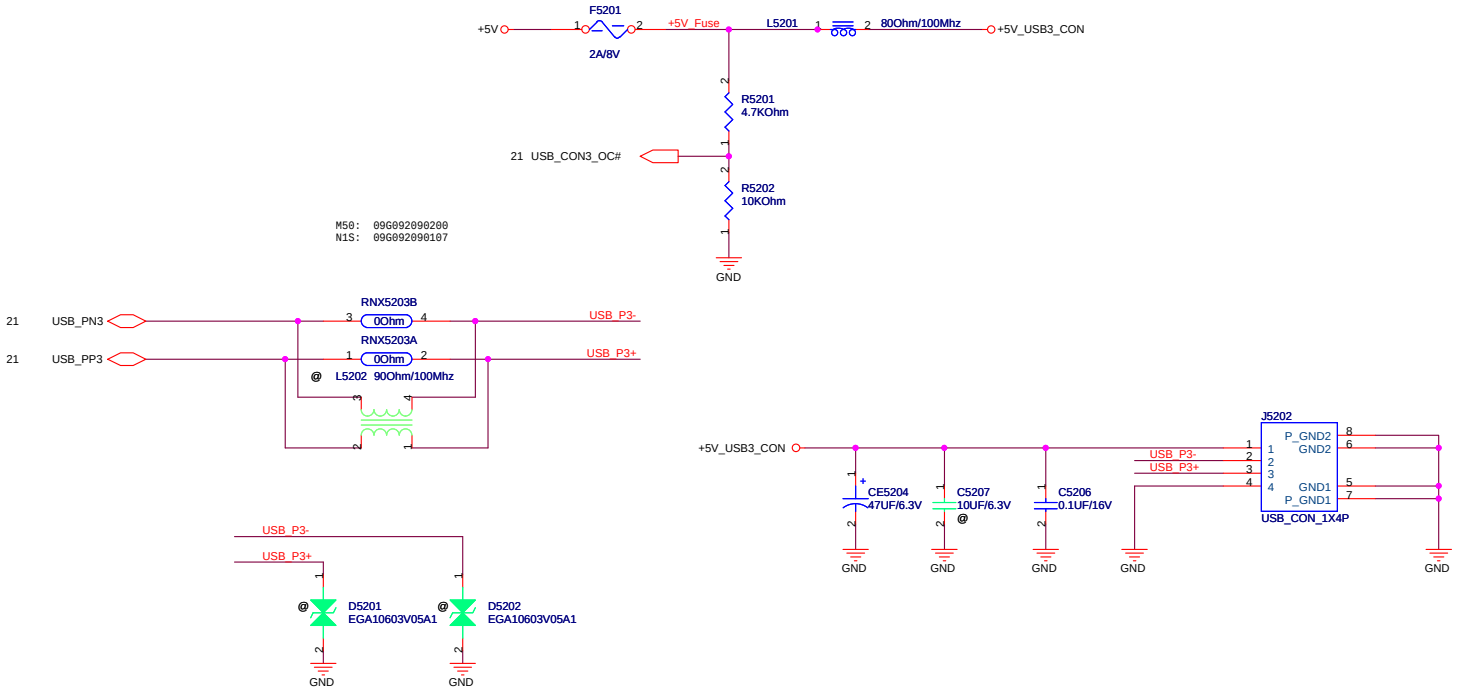
N1S 12G15000022F
N1S 12G15000022F

LAYOUT NOTE:
Two Strobes : Matched within 100 mils of each other
D[0:15] : Matched within +/- 450 mils of two strobes

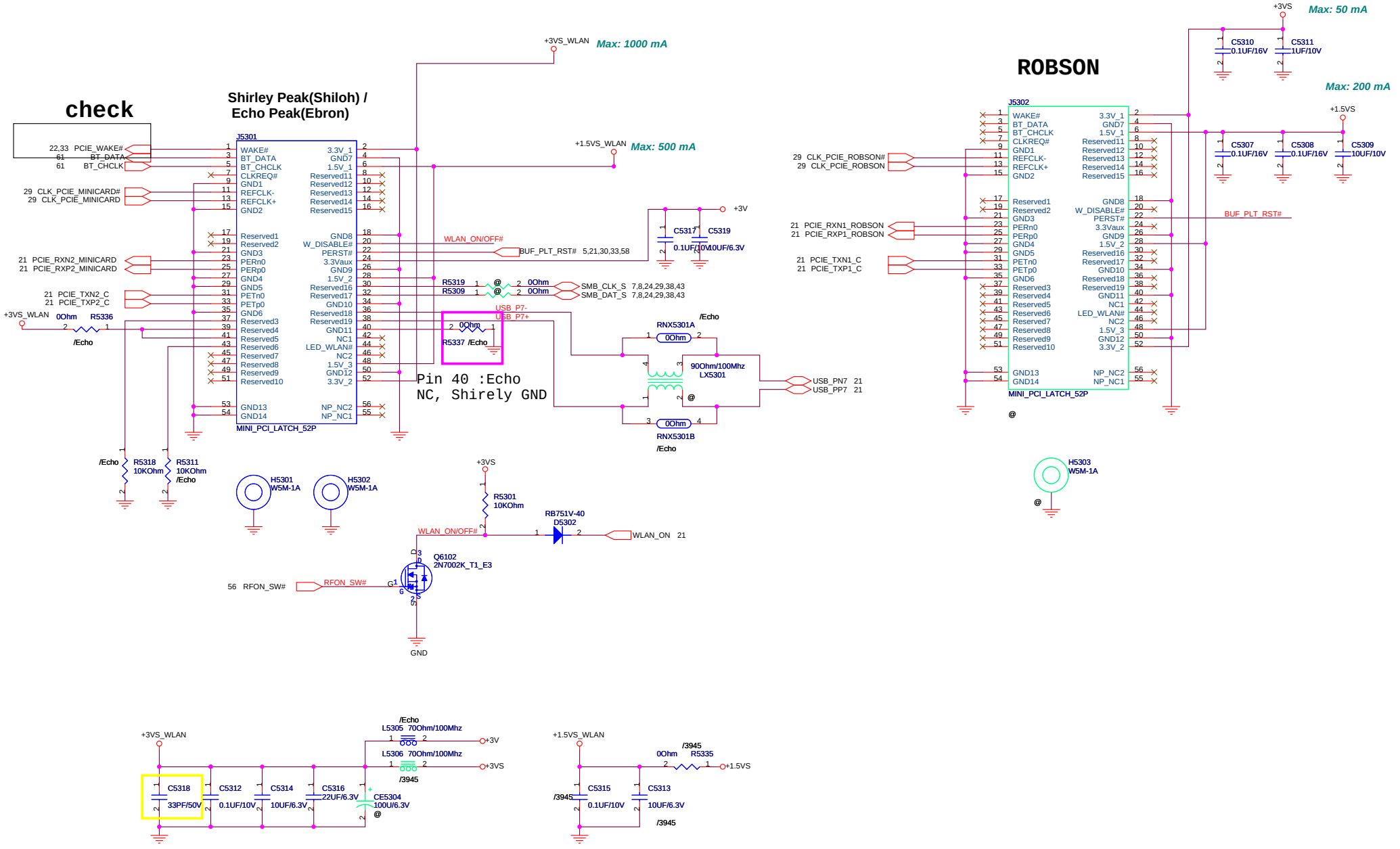
ODD CNT



ASUS	Title : HDD & ODD CONN.	
	Engineer:	
Size: Custom	Project Name	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 51 of 96	



ASUSTeK COMPUTER INC. NB1	Title : USB_USB Ports	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 52 of 96	



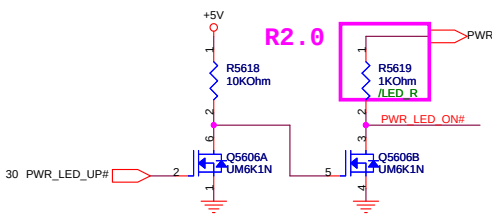
ASUSTeK COMPUTER INC. NB1	Title : PCI_WLAN	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 53 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 54 of 96	

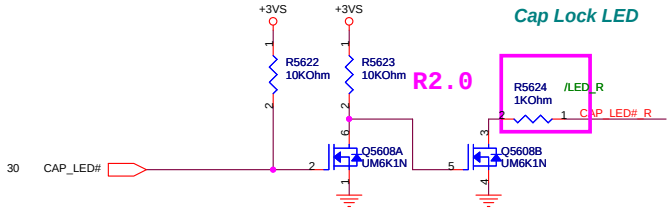
ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 55 of 96	

Rear

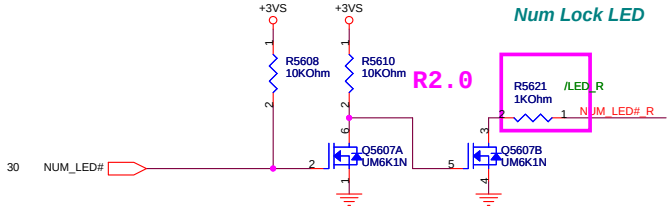
Power LED



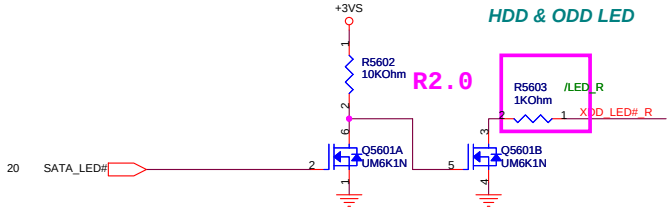
Cap Lock LED



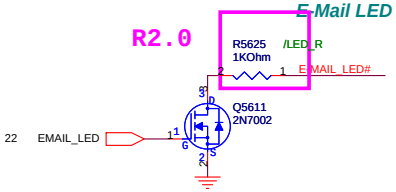
Num Lock LED



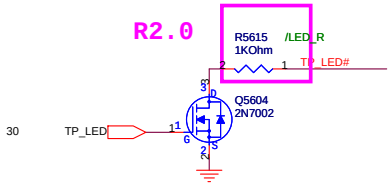
HDD & ODD LED

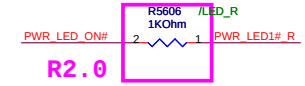


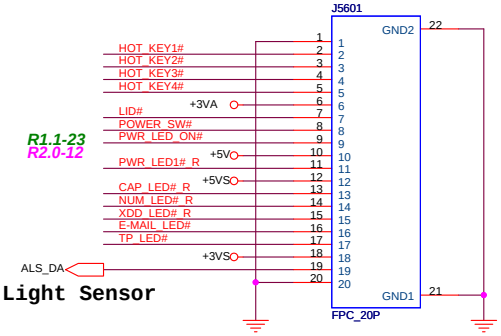
E-Mail LED

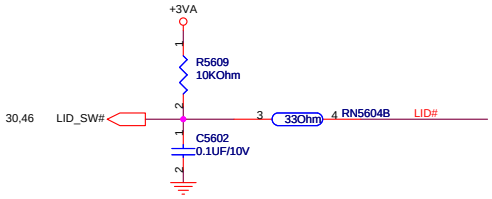


Touch-pad Lock LED

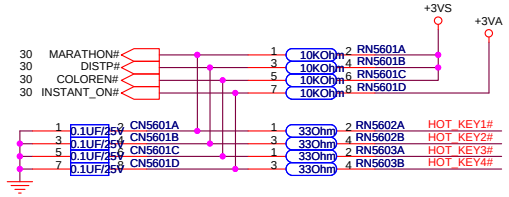


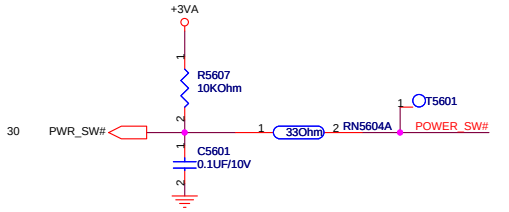




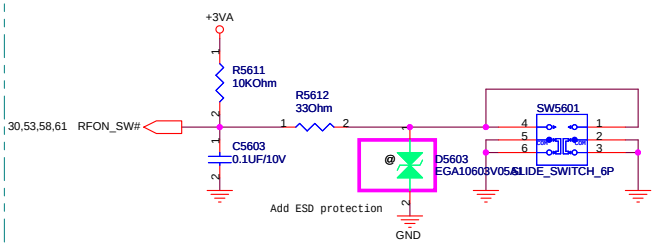


1. Power4Gear
2. Touch-Pad ON/OFF
3. Splendid
4. Instant Fun Plus
5. Power Button

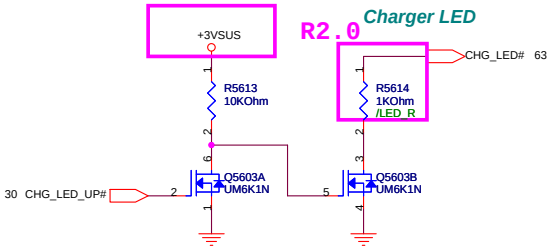




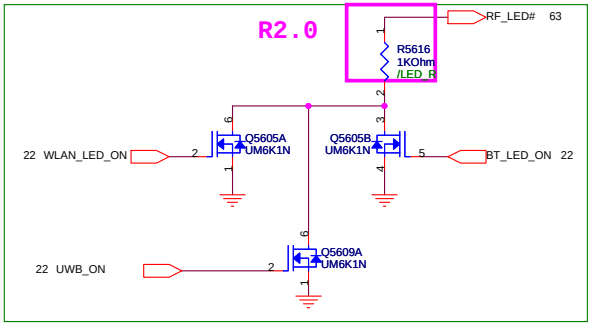
Main Board



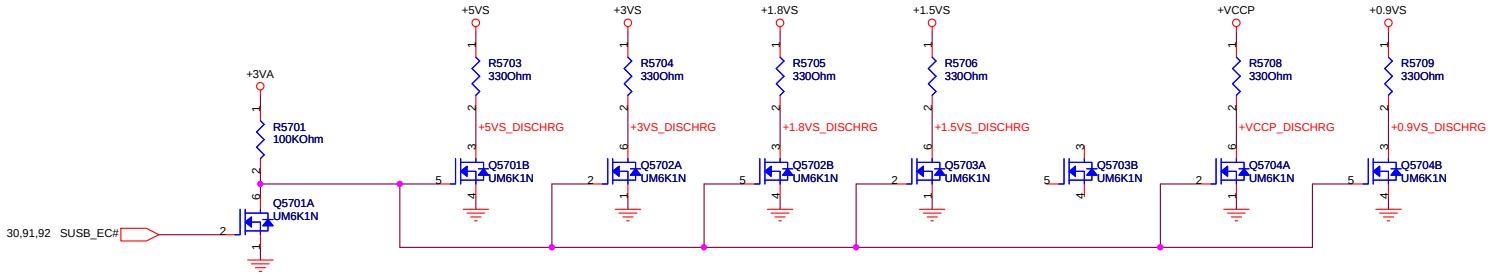
Charger LED

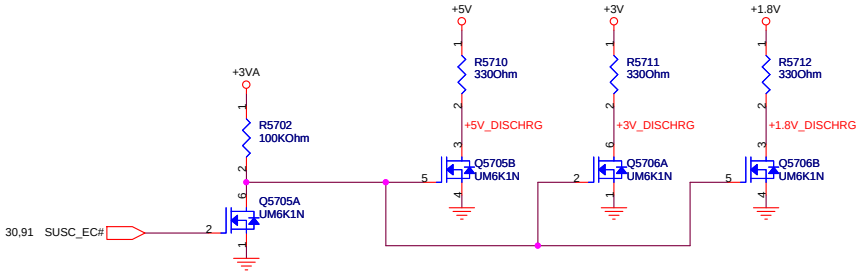


WLAN LED

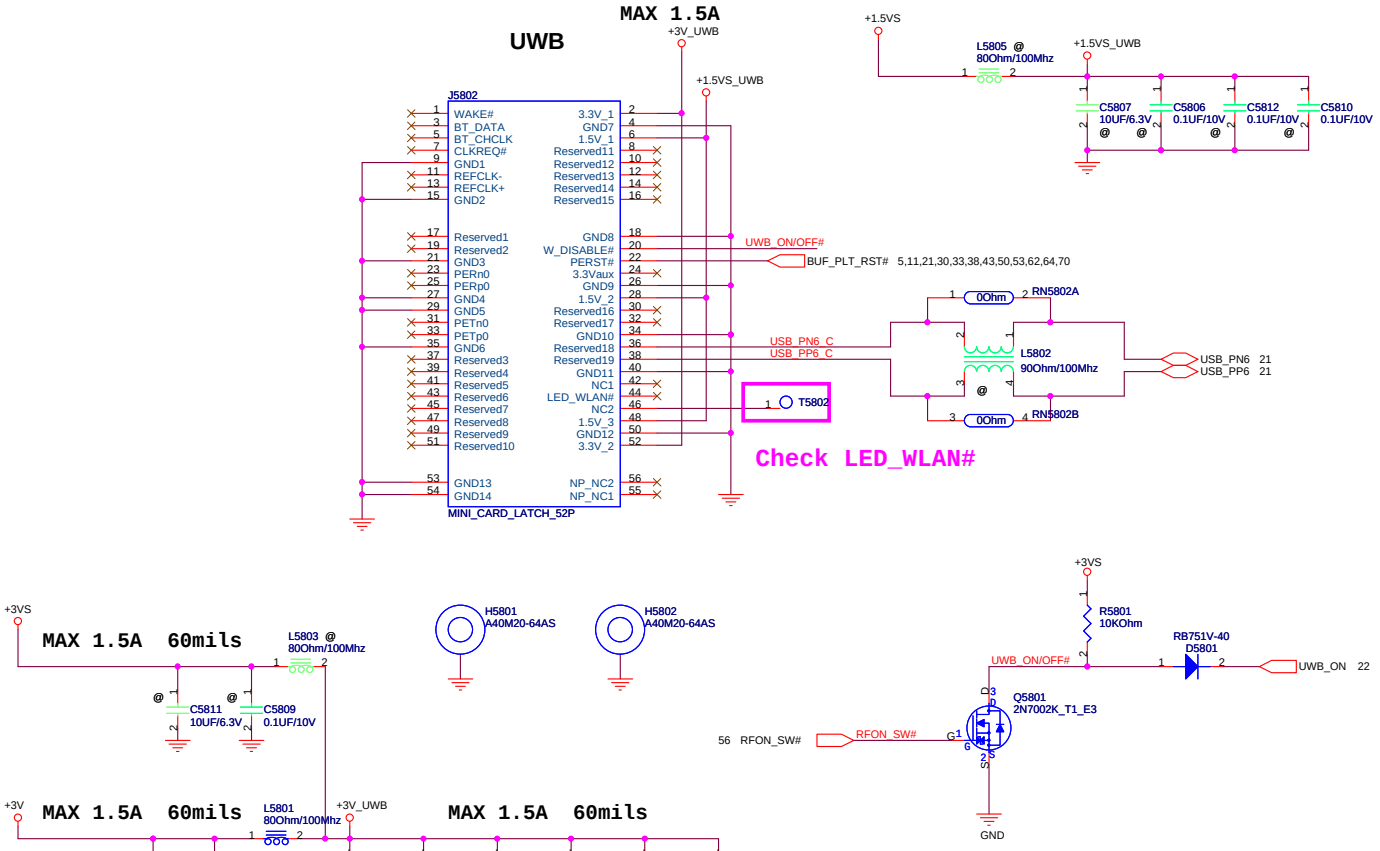


ASUSTeK COMPUTER INC. NB1	Title : LED_Indicator	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 2.0
Date: Wednesday, April 23, 2008	Sheet 56 of 96	





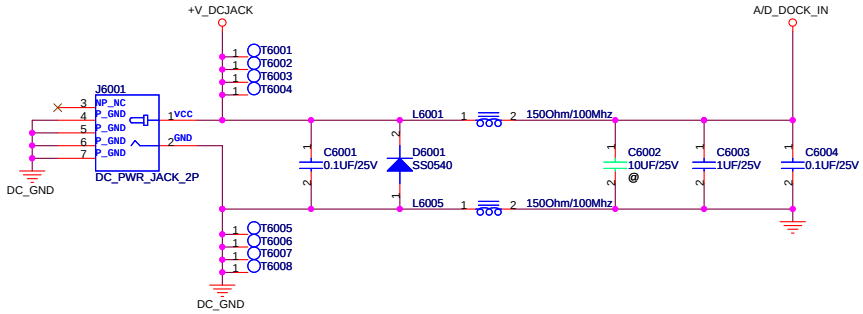
ASUSTeK COMPUTER INC. NB1	Title : DSG_Discharge	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 57 of 96	



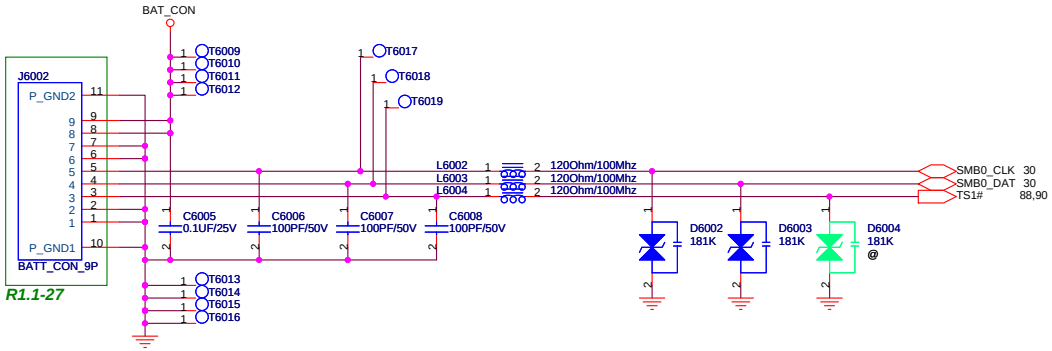
ASUSTeK COMPUTER INC. NB6	Title : UWB Minicard card	
	Engineer: Raphael_Chen	
Size: Custom	Project Name: V1V	Rev: 1.1
Date: Friday, March 07, 2008	Sheet 58 of 94	

ASUSTeK COMPUTER INC. NB6	Title : Engineer:	
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 59 of 96	

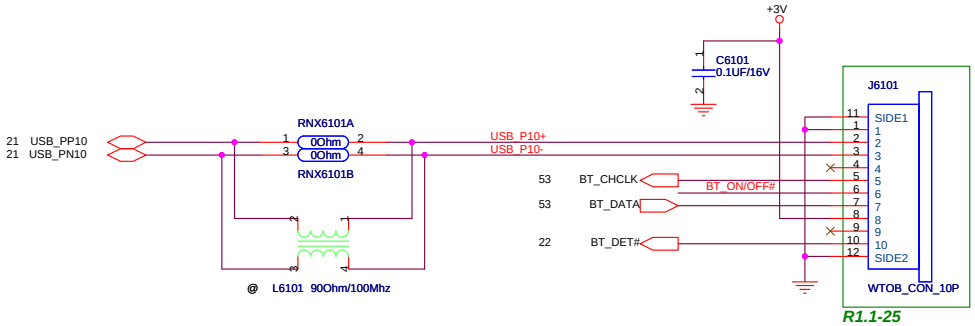
DC Jack



Battery Connector

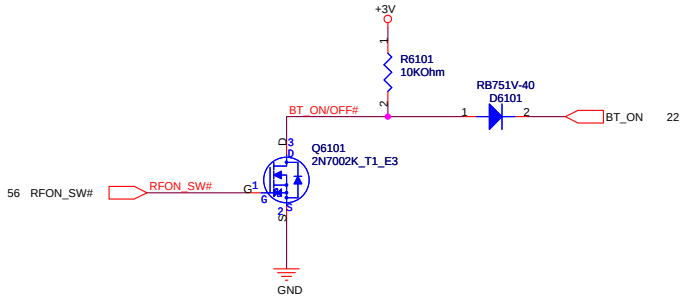


ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT Conn.	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Thursday, April 17, 2008	Sheet 60 of 96	

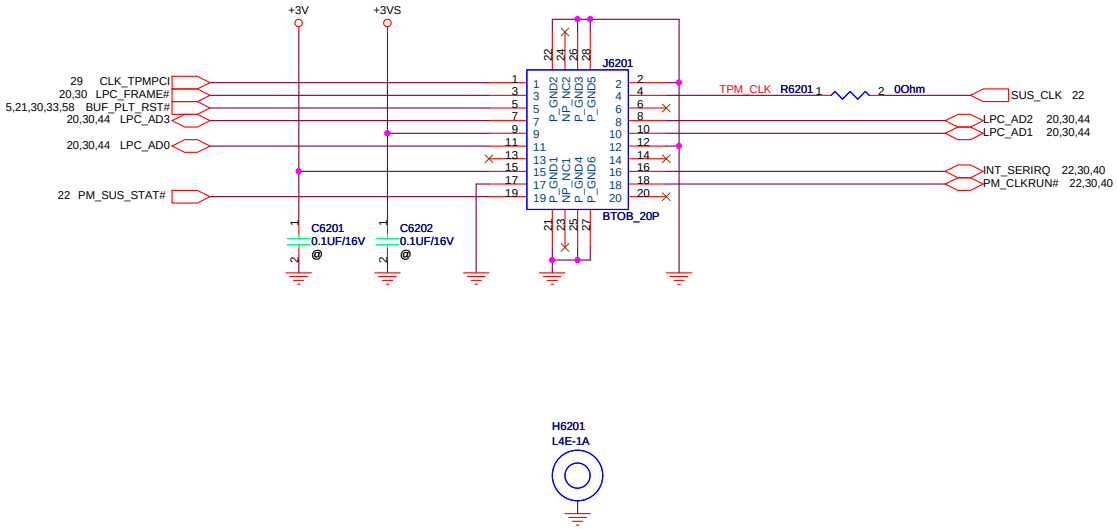


R1.1-25

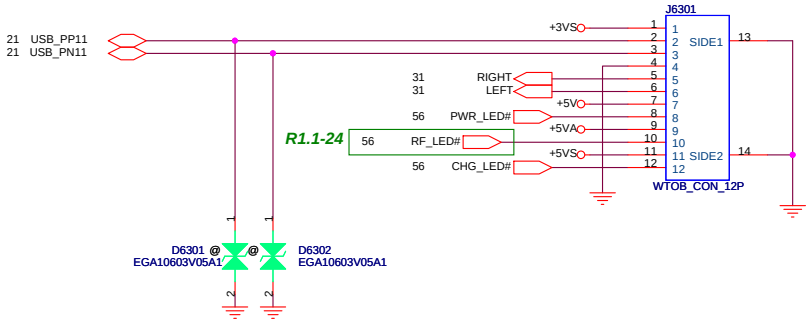
BT change from 2.0 to 2.1



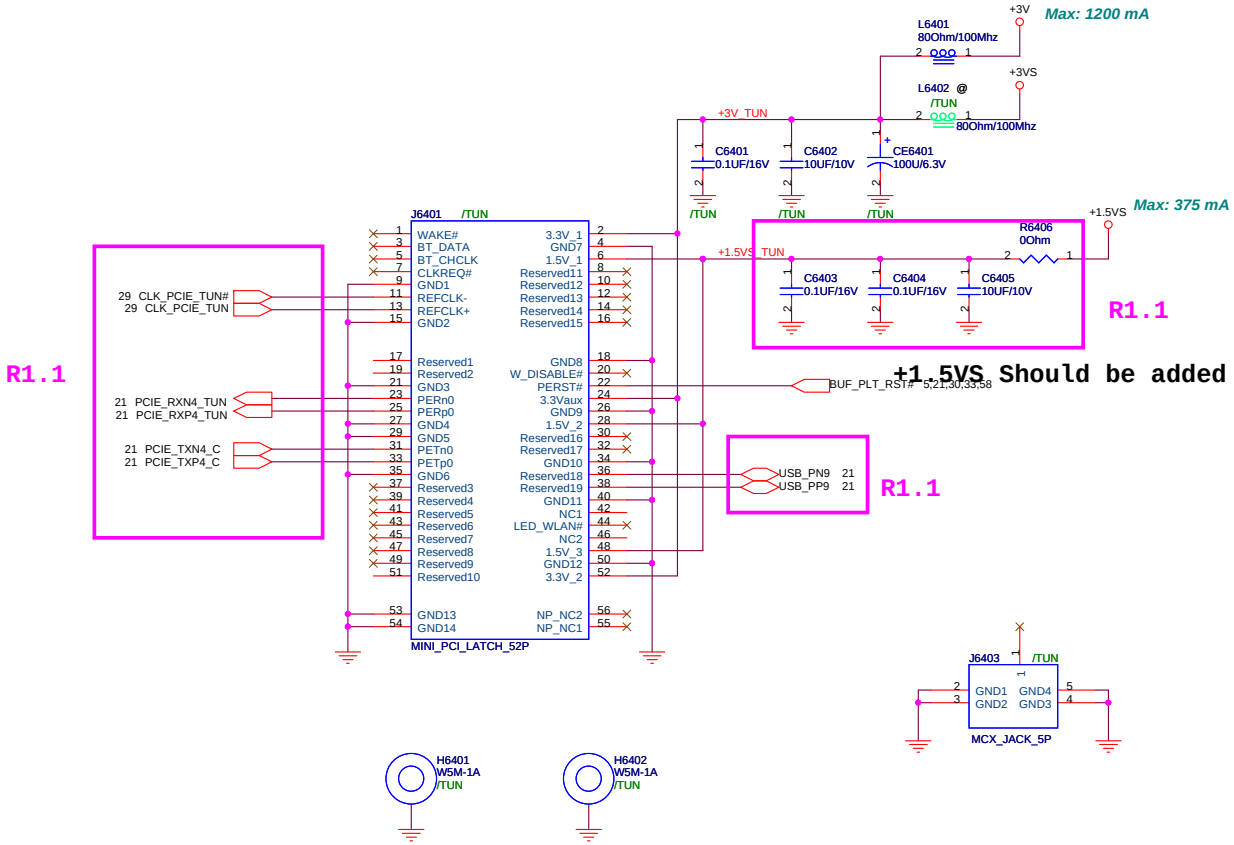
ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 61 of 96	



ASUSTeK COMPUTER INC. NB1	Title : TPM_TPM 1.2	
	Engineer:	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 62 of 96	

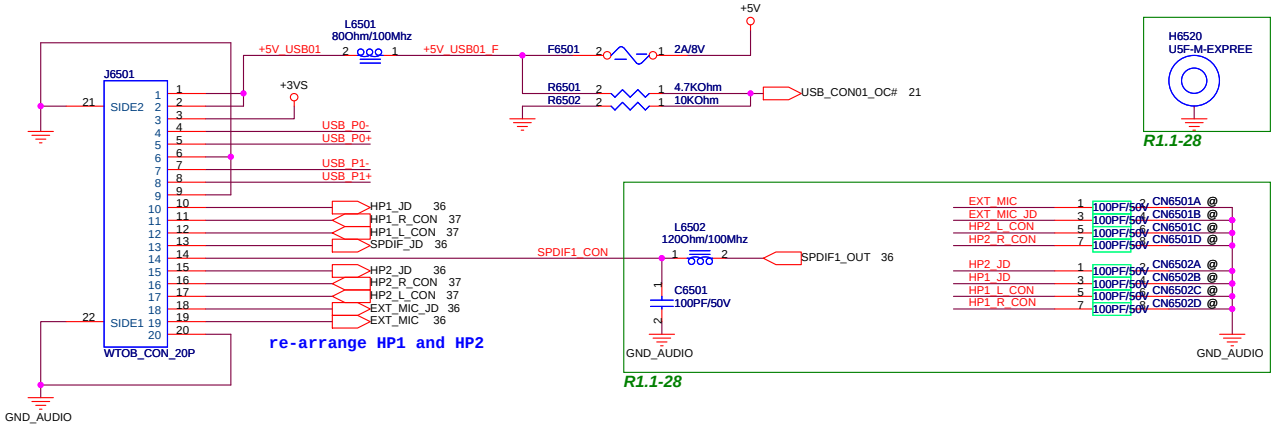


ASUSTeK COMPUTER INC. NB1	Title : FP_Fingerprint Conn.	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 63 of 96	

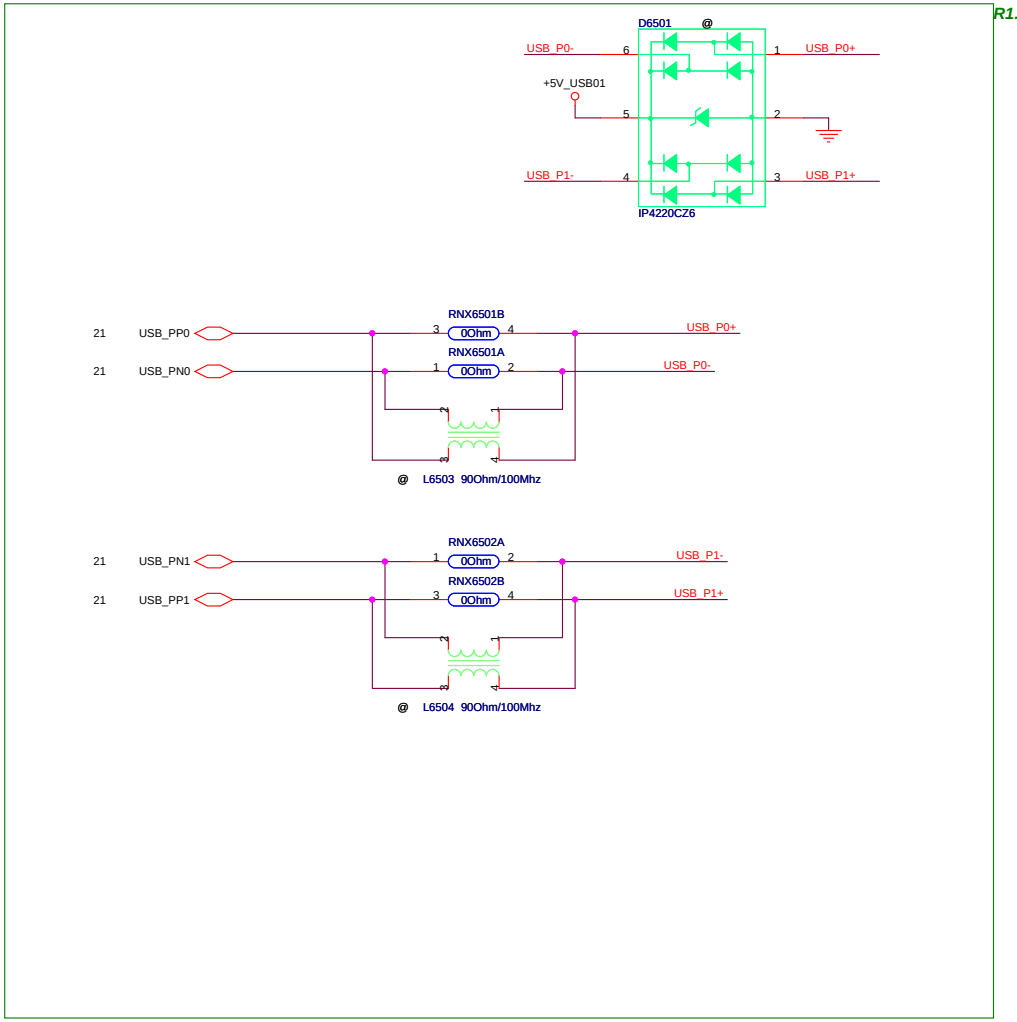


ASUSTeK COMPUTER INC. NB1	Title : TUN_TV Tuner	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 64 of 96	

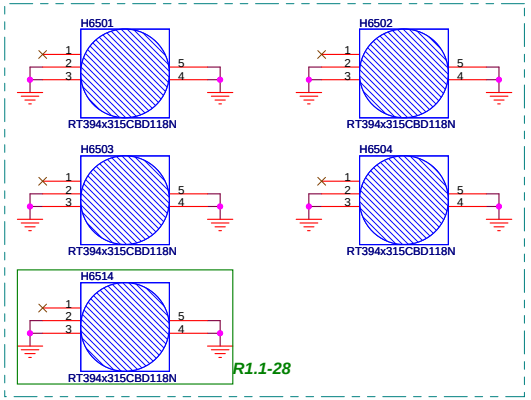
Main Board



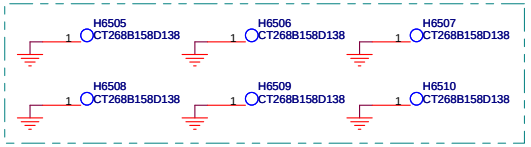
R1.1-09



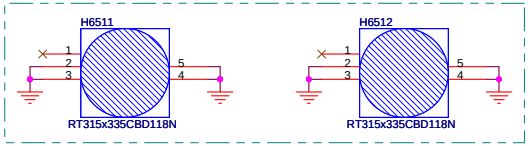
Screw Hole A



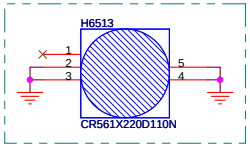
Screw Hole B



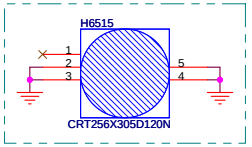
Screw Hole C



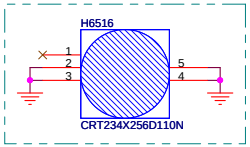
Screw Hole F



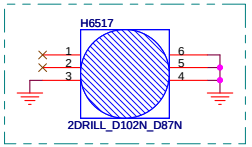
Screw Hole H



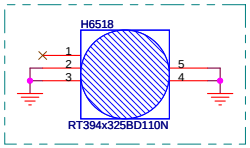
Screw Hole I



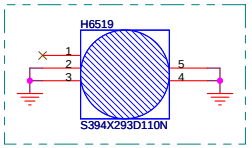
Screw Hole J



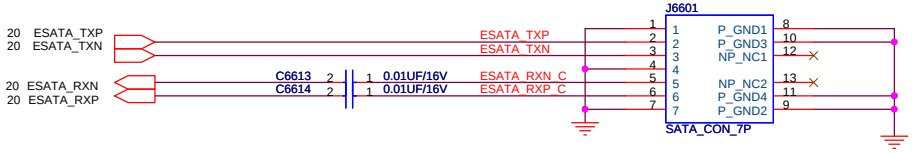
Screw Hole K



Screw Hole L



ASUSTeK COMPUTER INC. NB1	Title : ME_Conn & Screw Holes	
	Engineer: John Hung	
Size: Custom	Project Name: M50Vm	Rev: 1.0
Date: Tuesday, April 15, 2008	Sheet 65 of 96	



Title : E-SATA		
Engineer:		
Size: Custom	Project Name	Rev: 1.0
Date: Friday, March 07, 2008	Sheet 66 of 96	

ASUSTeK COMPUTER INC. NB1	Title : PCI_WWAN		
	Engineer: John Hung		
Size: Custom	Project Name: M50Vm		Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 67 of 96		

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 68 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.0
Date: Wednesday, February 13, 2008	Sheet 69 of 96	

RESISTERS CLOSE TO MXM

CON7001A

DVI
DVI_A_TX0
DVI_A_TX0#
DVI_A_TX1
DVI_A_TX1#
DVI_A_TX2
DVI_A_TX2#
DVI_A_CLK
DVI_A_CLK#
DVI_A_HPD
DVI_B_HPD/GND
48 HDMI_DETECT

CRT DDC
DDCB_CLK
DDCB_DAT
45 DDC2BC_PEG
45 DDC2BD_PEG
DDCA_CLK
DDCA_DAT

VGA
45 CRT_BLUE
45 CRT_RED
45 CRT_GREEN
45 CRT_HSYNC
45 CRT_VSYNC
VGA_BLU
VGA_RED
VGA_GRN
VGA_HSYNC
VGA_VSYNC

LVDS
46 LCD_VDD_EN_PEG
46 LCD_BACKEN_PEG
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
46 LVDS_L0P
46 LVDS_L0N
46 LVDS_L1P
46 LVDS_L1N
46 LVDS_L2P
46 LVDS_L2N
LVDS_UTX0
LVDS_UTX0#
LVDS_UTX1
LVDS_UTX1#
LVDS_UTX2
LVDS_UTX2#
LVDS_UTX3
LVDS_UTX3#
46 LVDS_LCLKP
46 LVDS_LCLKN
LVDS_UCLK
LVDS_UCLK#
46 LVDS_U0P
46 LVDS_U0N
46 LVDS_U1P
46 LVDS_U1N
46 LVDS_U2P
46 LVDS_U2N
LVDS_LTX0
LVDS_LTX0#
LVDS_LTX1
LVDS_LTX1#
LVDS_LTX2
LVDS_LTX2#
LVDS_LTX3
LVDS_LTX3#
46 LVDS_UCLKP
46 LVDS_UCLKN
LVDS_LCLK
LVDS_LCLK#

R1.1 SWAP LVDS Channel A B

Reserve to GDDR3 sequence

IGP
+0.9VS
36 SPDIF2_OUT
20 ACZ_RST#_VGA
20 ACZ_SDOUT#_VGA
20 ACZ_SDIN2_VGA
20 ACZ_SYNC_VGA
20 ACZ_BCLK_VGA
IGP_UTX0
IGP_UTX0#
IGP_UTX1
IGP_UTX1#
IGP_UTX2
IGP_UTX2#
IGP_UCLK
IGP_UCLK#

HDMI
48 VGA_HDMI_TX3+
48 VGA_HDMI_TX3-
48 VGA_HDMI_TX4+
48 VGA_HDMI_TX4-
48 VGA_HDMI_TX5+
48 VGA_HDMI_TX5-
48 VGA_HDMI_CLKB+
48 VGA_HDMI_CLKB-
IGP_LTX0/DVI_B_TX0
IGP_LTX0#/DVI_B_TX0#
IGP_LTX1/DVI_B_TX1
IGP_LTX1#/DVI_B_TX1#
IGP_LTX2/DVI_B_TX2
IGP_LTX2#/DVI_B_TX2#
IGP_LCLK/DVI_B_CLK
IGP_LCLK#/DVI_B_CLK#

TV-OUT
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb

SMBUS
LVDS DDC
46 EDID_CLK_PEG
46 EDID_DATA_PEG
DDCC_CLK
DDCC_DAT
30,50 SMB1_CLK
30,50 SMB1_DAT
SMB_CLK
SMB_DAT
thermal
RN7001A
RN7001B

MXM_230P

B TO B : Height = 7mm

PEX
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
CLK_REQ#
PEX_RST#
PEX_REFCLK
PEX_REFCLK#

PCIEG_RXP0 11
PCIEG_RXN0 11
PCIENB_RXP0 11
PCIENB_RXN0 11
PCIEG_RXP1 11
PCIEG_RXN1 11
PCIENB_RXP1 11
PCIENB_RXN1 11
PCIEG_RXP2 11
PCIEG_RXN2 11
PCIENB_RXP2 11
PCIENB_RXN2 11
PCIEG_RXP3 11
PCIEG_RXN3 11
PCIENB_RXP3 11
PCIENB_RXN3 11
PCIEG_RXP4 11
PCIEG_RXN4 11
PCIENB_RXP4 11
PCIENB_RXN4 11
PCIEG_RXP5 11
PCIEG_RXN5 11
PCIENB_RXP5 11
PCIENB_RXN5 11
PCIEG_RXP6 11
PCIEG_RXN6 11
PCIENB_RXP6 11
PCIENB_RXN6 11
PCIEG_RXP7 11
PCIEG_RXN7 11
PCIENB_RXP7 11
PCIENB_RXN7 11
PCIEG_RXP8 11
PCIEG_RXN8 11
PCIENB_RXP8 11
PCIENB_RXN8 11
PCIEG_RXP9 11
PCIEG_RXN9 11
PCIENB_RXP9 11
PCIENB_RXN9 11
PCIEG_RXP10 11
PCIEG_RXN10 11
PCIENB_RXP10 11
PCIENB_RXN10 11
PCIEG_RXP11 11
PCIEG_RXN11 11
PCIENB_RXP11 11
PCIENB_RXN11 11
PCIEG_RXP12 11
PCIEG_RXN12 11
PCIENB_RXP12 11
PCIENB_RXN12 11
PCIEG_RXP13 11
PCIEG_RXN13 11
PCIENB_RXP13 11
PCIENB_RXN13 11
PCIEG_RXP14 11
PCIEG_RXN14 11
PCIENB_RXP14 11
PCIENB_RXN14 11
PCIEG_RXP15 11
PCIEG_RXN15 11
PCIENB_RXP15 11
PCIENB_RXN15 11

R7014 1 @ 2 0Ohm GPU_RST# 22
R7015 1 2 0Ohm BUF_PLT_RST# 5,21,30,33,58
CLK_PCIE_PEG# 29
CLK_PCIE_PEG# 29

OTHER
THERM#
PRSNT1#
PRSNT2#
RUNPWROK
NP_NC1
NP_NC2
GND_1
GND_2
PRSNT2#
PWR_OK_VGA 92
BUF_PLT_RST#
VGA_OVT#
R7001 1 @ 2 0Ohm FORCE_OFF# 81,92
VGA_ALERT# 30
Q7002
2N7002@

LVDS_U0P /GM 3 0OHM 4 RN7002B LVDS_U0P_GM 11
LVDS_U0N /GM 1 0OHM 2 RN7002A LVDS_U0N_GM 11
LVDS_U1P /GM 3 0OHM 4 RN7003B LVDS_U1P_GM 11
LVDS_U1N /GM 1 0OHM 2 RN7003A LVDS_U1N_GM 11
LVDS_U2P /GM 1 0OHM 2 RN7004A LVDS_U2P_GM 11
LVDS_U2N /GM 3 0OHM 4 RN7004B LVDS_U2N_GM 11
LVDS_UCLKP /GM 1 0OHM 2 RN7005A LVDS_UCLKP_GM 11
LVDS_UCLKN /GM 3 0OHM 4 RN7005B LVDS_UCLKN_GM 11
LVDS_L0P /GM 3 0OHM 4 RN7006B LVDS_L0P_GM 11
LVDS_L0N /GM 1 0OHM 2 RN7006A LVDS_L0N_GM 11
LVDS_L1P /GM 3 0OHM 4 RN7007B LVDS_L1P_GM 11
LVDS_L1N /GM 1 0OHM 2 RN7007A LVDS_L1N_GM 11
LVDS_L2P /GM 3 0OHM 4 RN7008B LVDS_L2P_GM 11
LVDS_L2N /GM 1 0OHM 2 RN7008A LVDS_L2N_GM 11
LVDS_LCLKP /GM 1 0OHM 2 RN7009A LVDS_LCLKP_GM 11
LVDS_LCLKN /GM 3 0OHM 4 RN7009B LVDS_LCLKN_GM 11

LCD_VDD_EN_PEG 0Ohm 1 /GM 2 R7005 L_VDDEN 11
LCD_BACKEN_PEG 0Ohm 1 /GM 2 R7006 L_BKLTEN 11
EDID_DATA_PEG 0Ohm 1 /GM 2 R7008 EDID_DAT 11
EDID_CLK_PEG 0Ohm 1 /GM 2 R7009 EDID_CLK 11

MXM Heatsink Stand-Off
H7001 /PM CT217B67D47
H7002 /PM CT217B67D47
H7003 /PM U5F-M-EXPREE
H7004 /PM U5F-M-EXPREE

CON7001B
AC_BAT_SYS
max 3A?
+1.5VS 3.15A
max 3.5A
+3VS 850mA
max 1.5A
PWR_SRC1
PWR_SRC2
PWR_SRC3
PWR_SRC4
PWR_SRC5
PWR_SRC6
PWR_SRC7
PWR_SRC8
1V8RUN_1
1V8RUN_2
1V8RUN_3
1V8RUN_4
1V8RUN_5
1V8RUN_6
1V8RUN_7
3V3RUN_1
3V3RUN_2
3V3RUN_3
5VRUN
2V5RUN
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44 GND45 GND46 GND47 GND48 GND49 GND50 GND51 GND52 GND53 GND54
MXM_230P

HDMI DDC
48 HDMI_DDCCLK
48 HDMI_DDCDAT
29 CLK_ATI27SS
29 CLK_ATI27
+5V
+12VS
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
AC/BATT#
+1.8VS
SUSB# PWR VGA
GND66 GND65 GND64 GND63 GND62 GND61 GND60 GND59 GND58 GND57 GND56 GND55

+3VSUS
R7002 100KOhm
U7001 NC7SZ14P5_NL
SUSB# PWR VGA
81,82,83,91,93 SUSB#_PWR
R7003 10KOhm
Q7001 PMBS3904
+12VSUS
R7004 100KOhm
PRSNT2#
ATI : Low
NV : High
Q7003 2N7002
C7001 0.1UF/16V

ASUSTeK COMPUTER INC. NB6
Title : VGA CON
Engineer: Raphael_Chen
Size: Custom
Project Name: M50Vm
Rev: 1.0
Date: Friday, March 07, 2008
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ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 71 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 72 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 73 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 74 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 75 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 76 of 96	

ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 77 of 96	

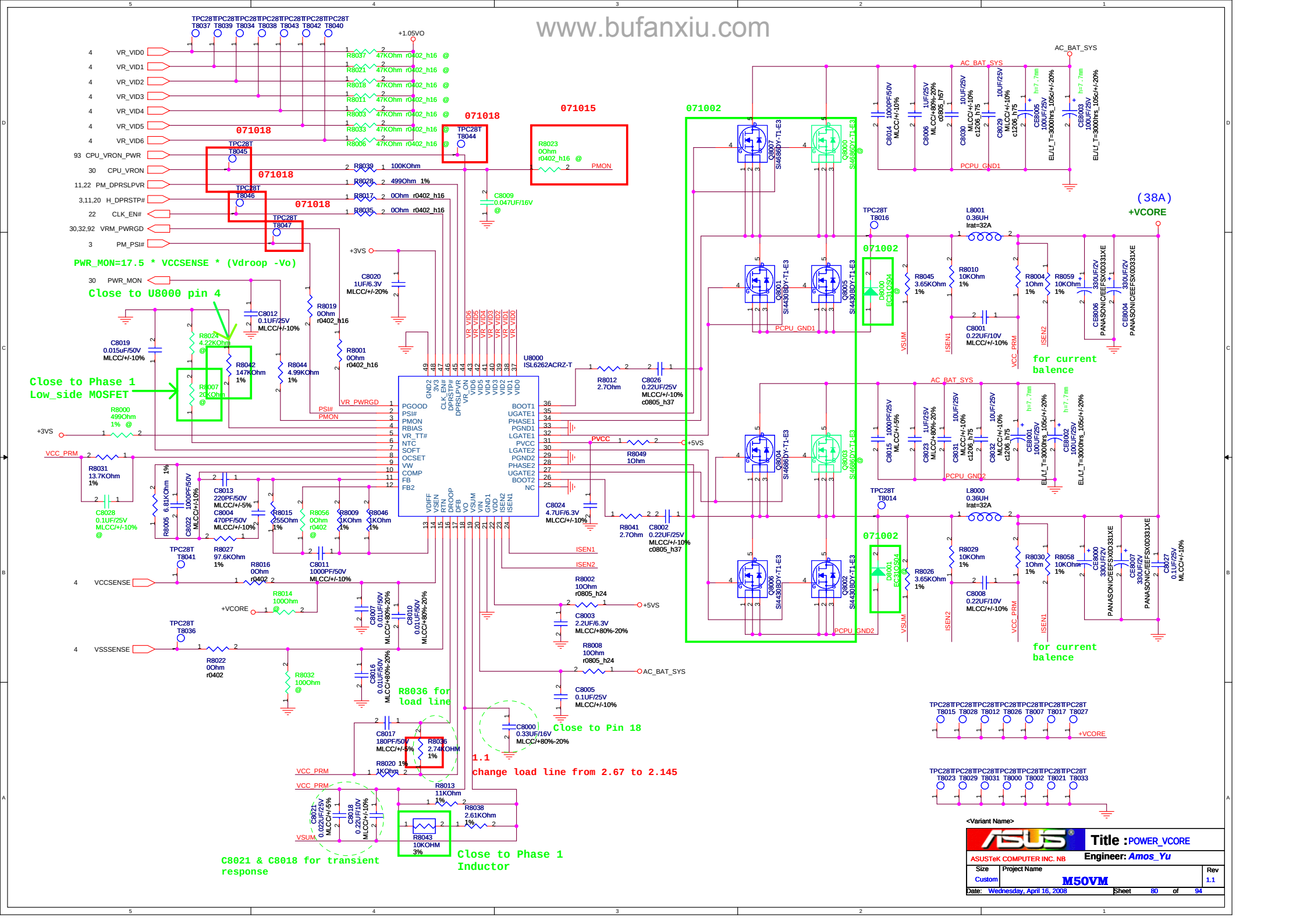
ASUS	Title :	
Engineer:		
Size: A	Project Name	Rev: 1.1
Date: Wednesday, February 13, 2008	Sheet 78 of 96	

History

20070820 R1.01:

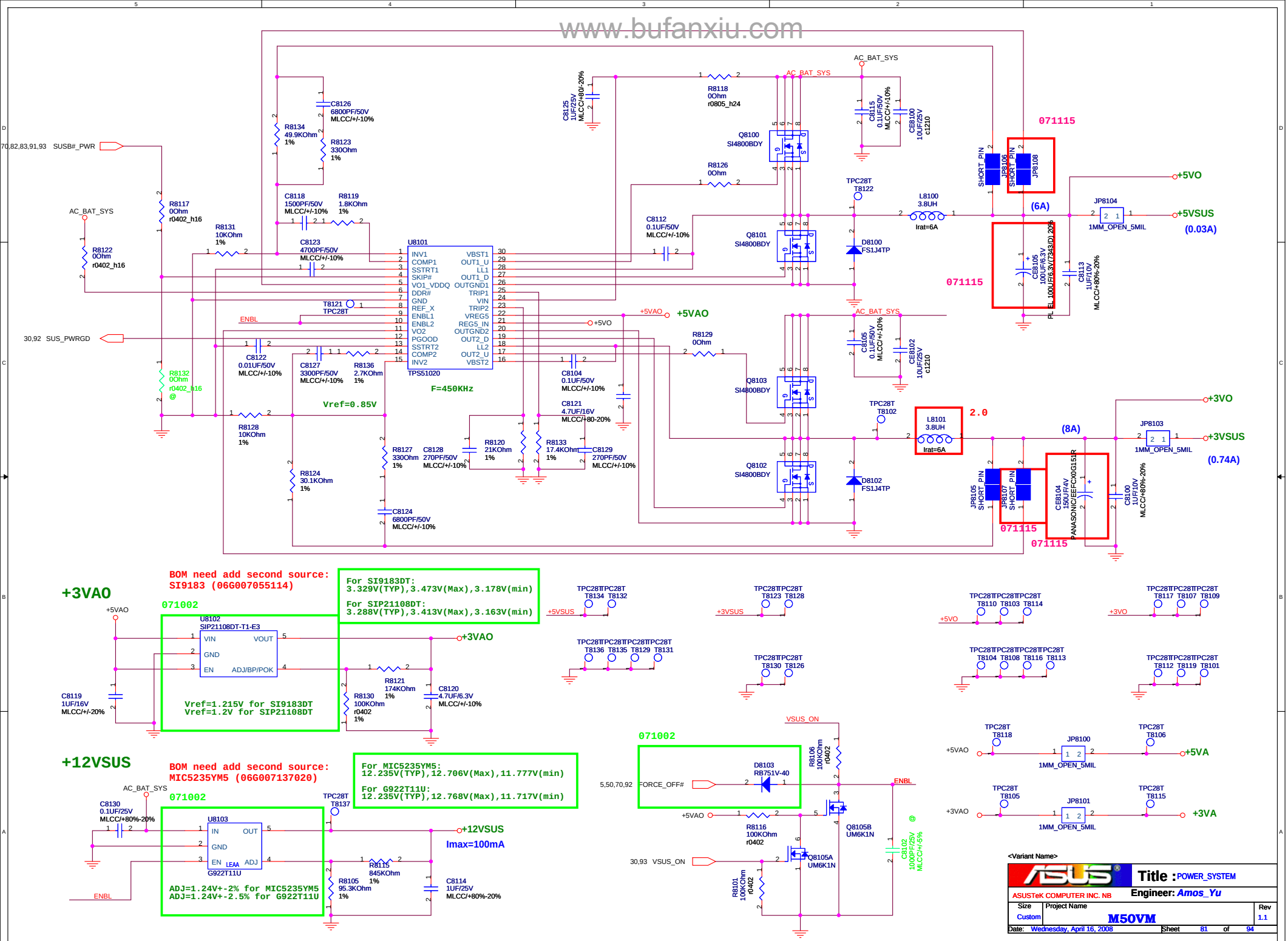
1. RTL8111C first release.
2. Remove RTL8111B co-lay circuit.
3. Change the L3404 part-name for the same part reference.

ASUSTeK COMPUTER INC	Title : History	
	Engineer:	
Size: Custom	Project Name	Rev: 1.01
Date: Wednesday, February 13, 2008	Sheet 79 of 96	



Title :	POWER_VCORE
ASUSTeK COMPUTER INC. NB	Engineer: Amos_Yu
Size: Custom	Project Name: M50VM
Rev: 1.1	
Date: Wednesday, April 16, 2008	Sheet 80 of 94

<Variant Name>



+3VA0

BOM need add second source:
SI9183 (06G007055114)

071002

U8102 SIP21108DT-T1-E3 (VIN, VOUT, GND, EN, ADJ/BP/POK)

For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)

For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)

Vref=1.215V for SI9183DT
Vref=1.2V for SIP21108DT

+5VAO → +3VAO

C8119 1UF/16V MLCC/+/-20%
R8121 174KOhm 1%
R8130 100KOhm r0402 1%
C8120 4.7UF/6.3V MLCC/+/-10%

+12VSUS

BOM need add second source:
MIC5235YM5 (06G007137020)

071002

U8103 (IN, OUT, GND, EN, ADJ) G922T11U

For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)

For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)

ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U

Imax=100mA

C8130 0.1UF/25V MLCC/+80%-20%
R8115 845KOhm 1%
R8105 95.3KOhm 1%
C8114 1UF/25V MLCC/+80%-20%

FORCE_OFF# / VSUS_ON

5,50,70,92 FORCE_OFF#
30,93 VSUS_ON
D8103 RB751V-40
Q8105B UM6K1N
Q8105A UM6K1N
R8106 100KOhm r0402
R8116 100KOhm r0402
R8101 100KOhm r0402
C8102 1000PF/25V MLCC/+/-5%

TPC28T T8118 JP8100 TPC28T T8106 +5VA
TPC28T T8105 JP8101 TPC28T T8115 +3VA

<Variant Name>

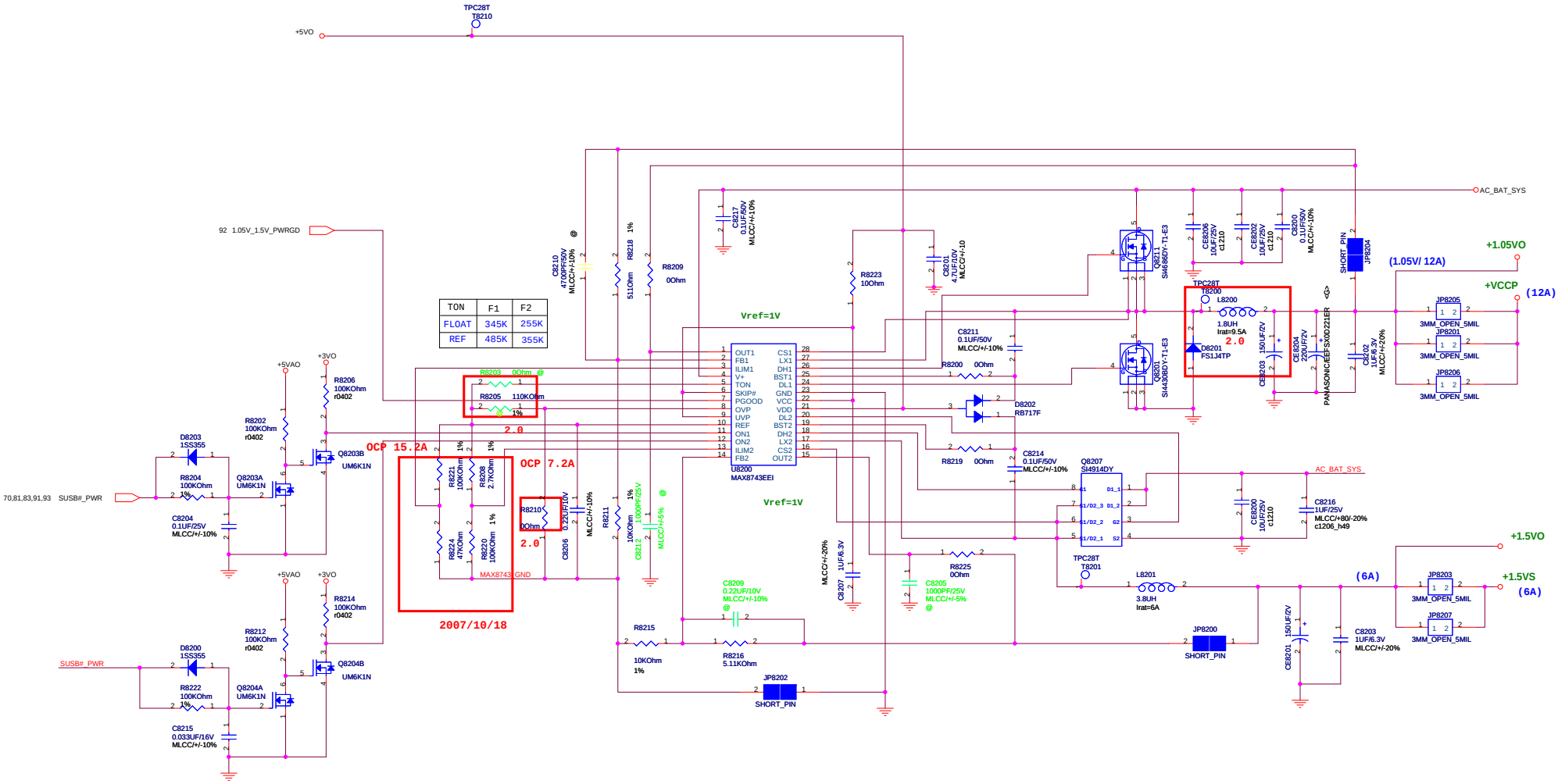
ASUSTeK COMPUTER INC. NB

Title : POWER_SYSTEM

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 81 of 94



<Variant Name>

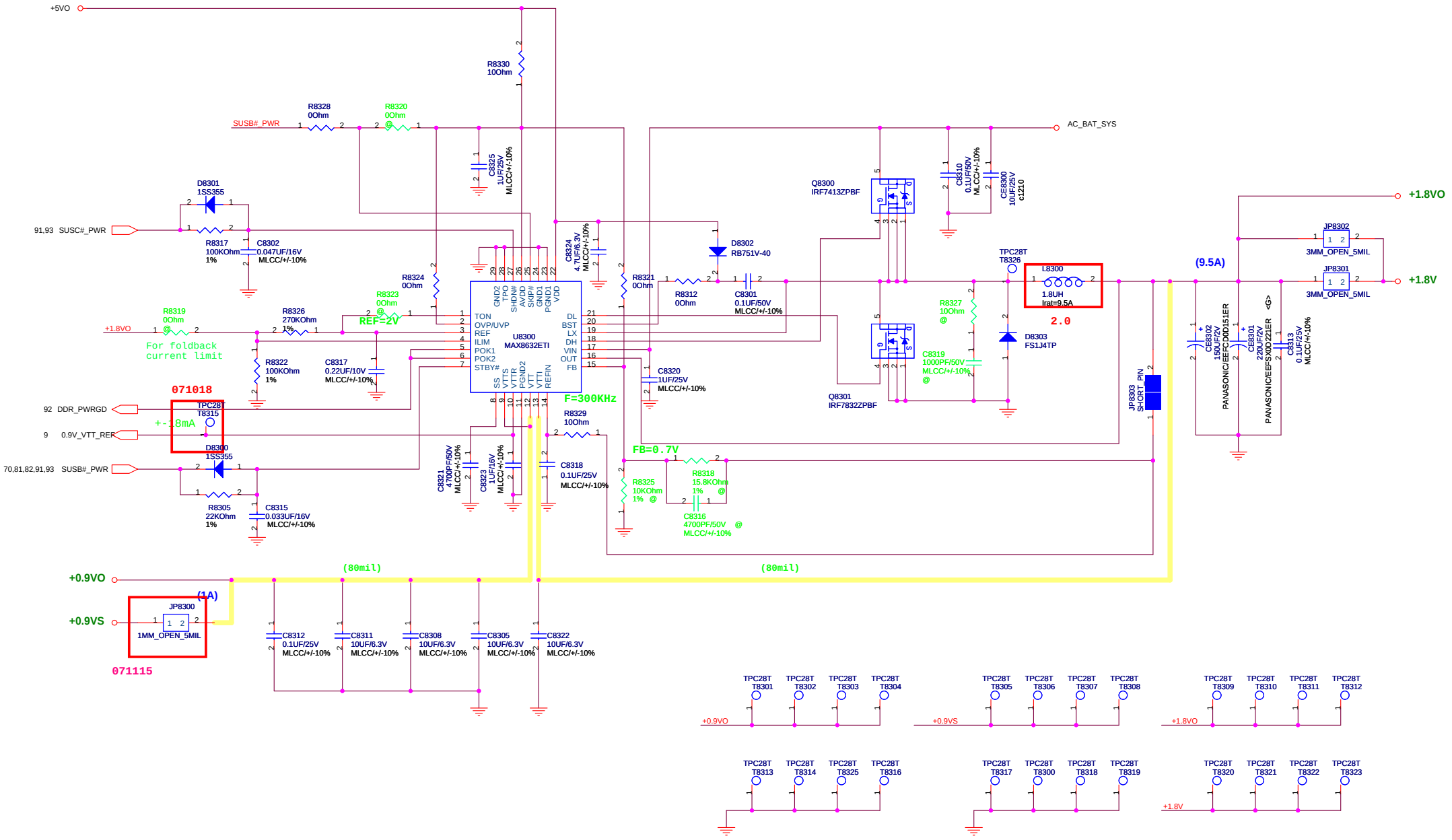
ASUSTeK COMPUTER INC. NB

Title : POWER_VGA_CORE & RAM

Engineer: Amos_Yu

Size	Project Name	Rev
C	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 82 of 94



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_DDR & VTT	
	Engineer: Amos_Yu	
Size: Custom	Project Name: M50VM	Rev: 1.1
Date: Wednesday, April 16, 2008	Sheet 83 of 94	

071002

<Variant Name>

Title : POWER_I/O_ +2.5VS

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 84 of 94

071002

<Variant Name>

Title : POWER_I/O_1.5VS & 1.05VS

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 85 of 94

071002

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
B	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 86 of 94

071002

<Variant Name>

071002

Title : POWER_SHUTDOWN#

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 87 of 94

POWER PATH & BAT_LEARN

add second source

add second source

90W->10m Ohm
65W->20m Ohm

071112

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R8805=20K,R8819=30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA

LDO : 5.4V
REF : 4.2235V

1.SI4431BDY-> 07G005140011
2.SI9435BDY-> 07G005921010
3.FDS9435A -> 07G005720010

90W->30K Ohm
65W->137K Ohm

071018

071002

For EC(ITE8752):
Delete net AC_APR_UC, R8804, Q8806

071018

071018

071018

071002

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_CHARGER

Engineer: Amos_Yu

Size	Project Name	Rev
C	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 88 of 94

071002

<Variant Name>

Title : N/A

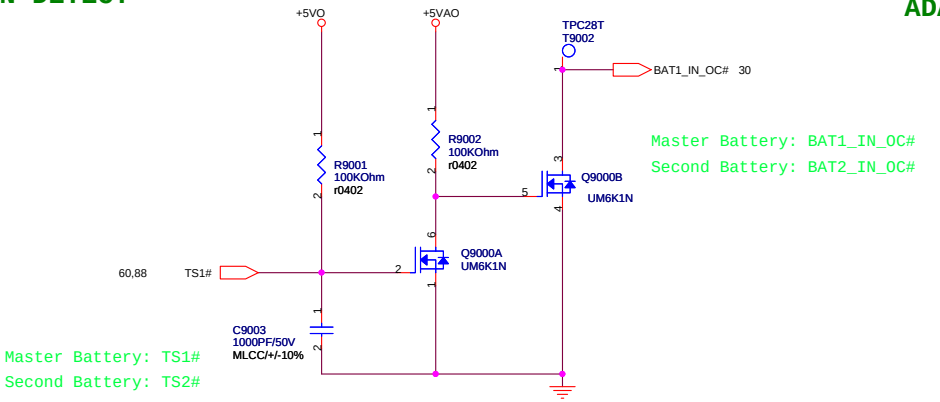
ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

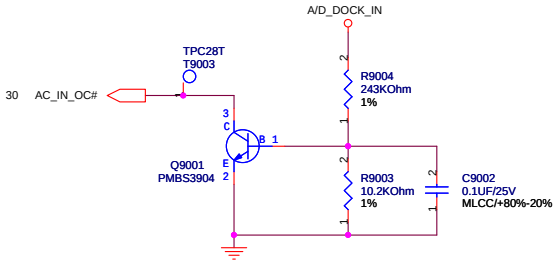
Size	Project Name	Rev
Custom	M50VM	1.0

Date: Wednesday, April 16, 2008 Sheet 89 of 94

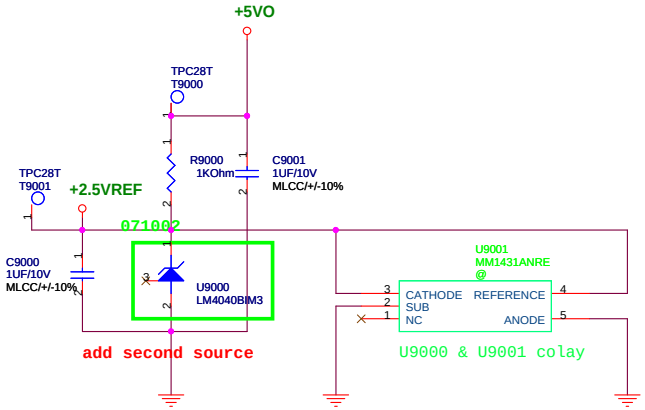
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



U9000 06G006002412 (tolerence:0.2%) add second source 06G006002610 (tolerence:1%) and 06G006002414(tolerence:1%)

<Variant Name>

Title : POWER_DETECT

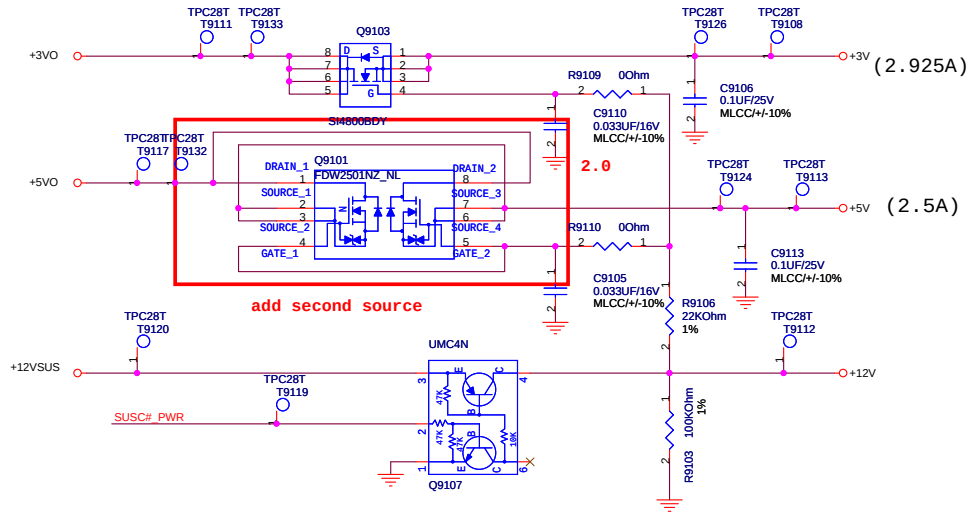
ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

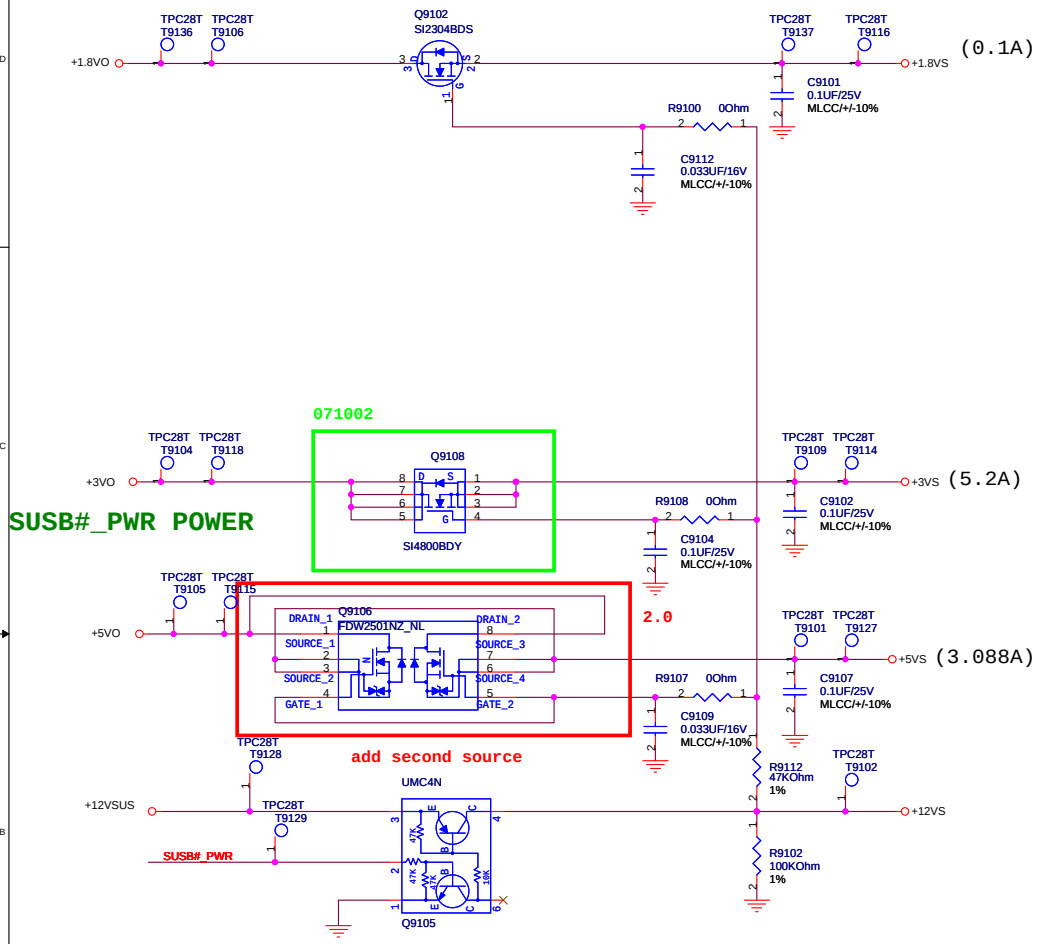
Size	Project Name	Rev
Custom	M50VM	1.1

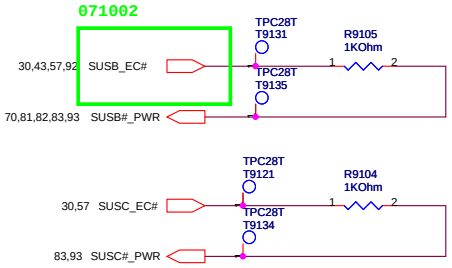
Date: Wednesday, April 16, 2008 Sheet 90 of 94

SUSC#_PWR POWER



SUSB#_PWR POWER





<Variant Name>

ASUSTeK COMPUTER INC. NB

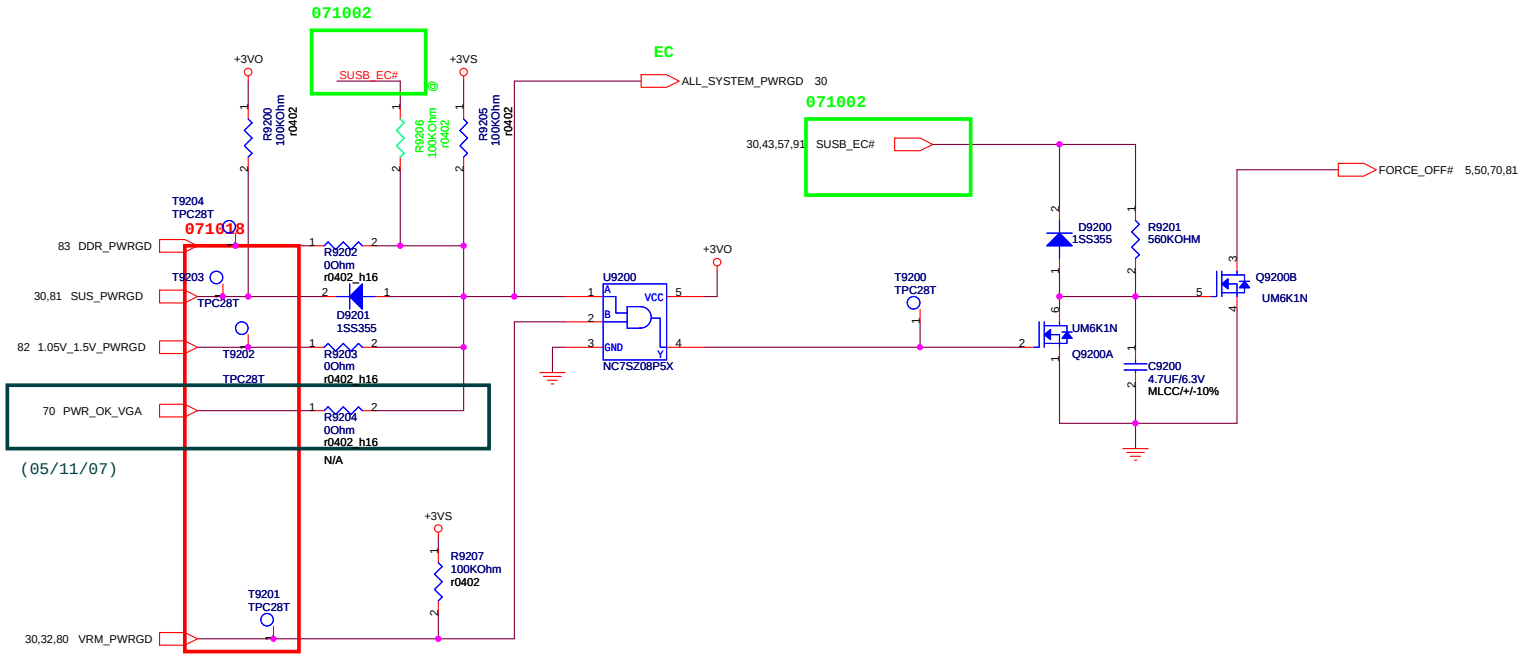
Title : POWER_LOAD SWITCH

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_PROTECT

Engineer: Amos_Yu

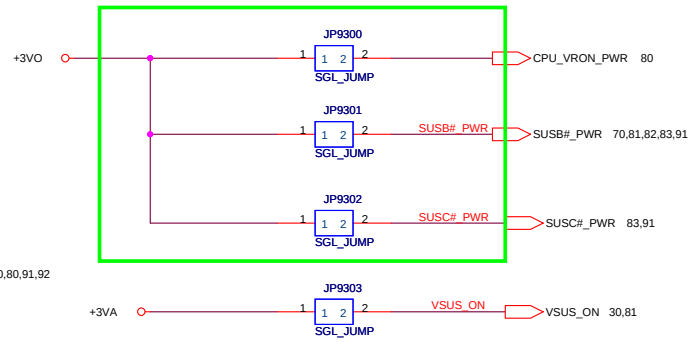
Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 92 of 94

AC_BAT_SYS	AC_BAT_SYS	70,80,81,82,83,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	88,90
+3VA	+3VA	20,30,56,57,81
+5VAO	+5VAO	81,82,90
+5VO	+5VO	81,82,83,88,90,91
+5VSUS	+5VSUS	23,31,81
+5V	+5V	36,46,52,56,57,63,65,70,91
+5VS	+5VS	23,31,37,45,48,50,51,56,57,63,80,91
+3VO	+3VO	81,82,91,92
+3VSUS	+3VSUS	20,21,22,23,30,33,37,46,56,70,81
+3V	+3V	21,35,43,53,57,61,64,91
+3VS	+3VS	3,7,8,11,14,15,20,21,22,23,24,25,29,30,32,33,36,37,40,41,42,43,44,45,46,48,50,51,53,56,57,63,64,65,70,80,91,92
+12VSUS	+12VSUS	70,81,91
+12V	+12V	37,91
+12VS	+12VS	24,42,46,70,91
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	7,8,9,11,13,57,83
+1.8VS	+1.8VS	14,20,38,57,70,91
+0.9VS	+0.9VS	9,57,70,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	80,82
+VCCP	+VCCP	5,10,11,13,14,20,23,29,57,82
+1.5VO	+1.5VO	82
+1.5VS	+1.5VS	4,14,20,23,43,53,57,64,70,82
+VCORE	+VCORE	4,5,80

FOR POWER TEST

1017



<Variant Name>

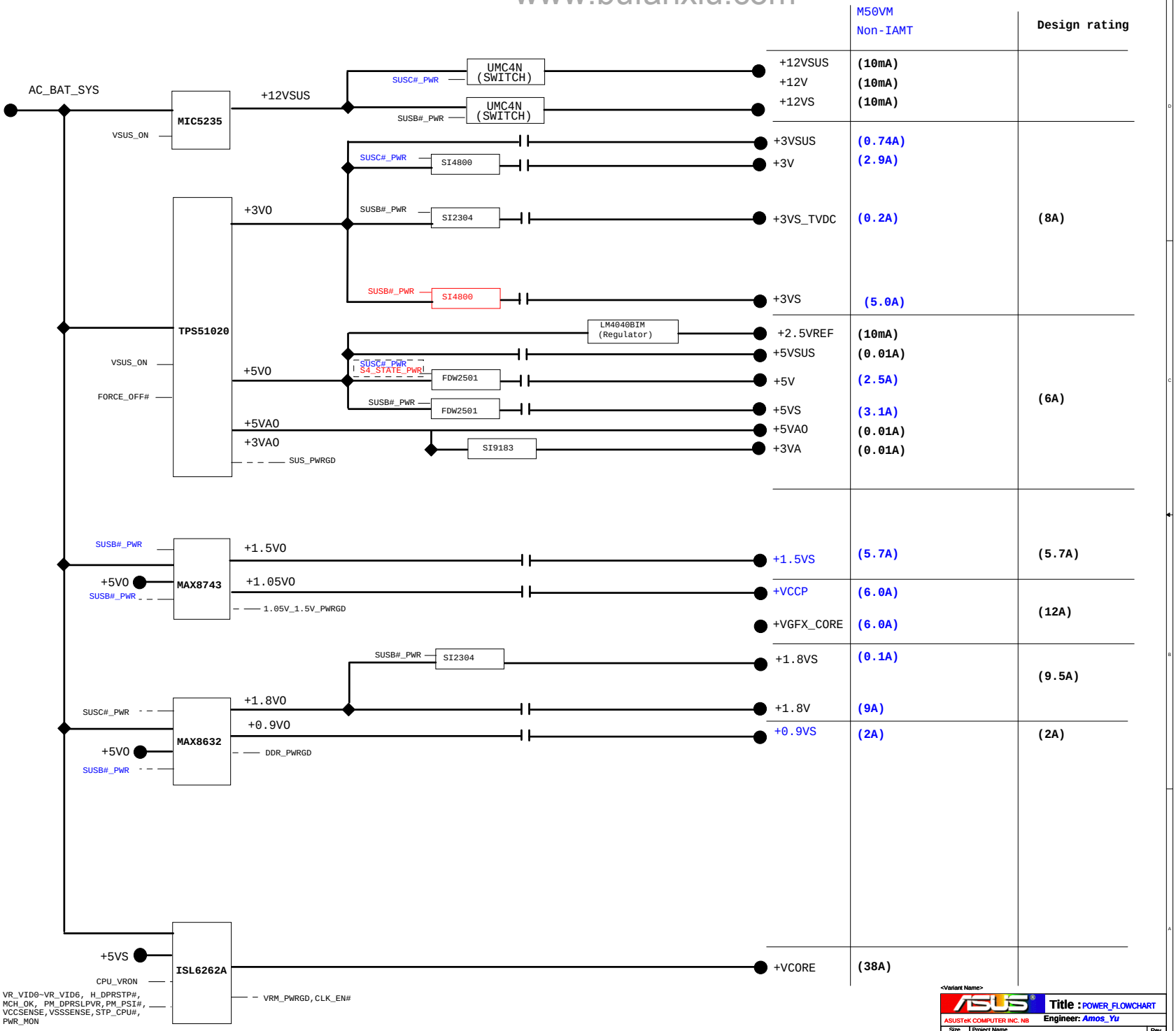
Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 93 of 94



	M50VM Non-IAMT	Design rating
+12VSUS	(10mA)	
+12V	(10mA)	
+12VS	(10mA)	
+3VSUS	(0.74A)	
+3V	(2.9A)	
+3VS_TVDC	(0.2A)	(8A)
+3VS	(5.0A)	
+2.5VREF	(10mA)	
+5VSUS	(0.01A)	
+5V	(2.5A)	
+5VS	(3.1A)	(6A)
+5VA0	(0.01A)	
+3VA	(0.01A)	
+1.5VS	(5.7A)	(5.7A)
+VCCP	(6.0A)	
+VGFX_CORE	(6.0A)	(12A)
+1.8VS	(0.1A)	
+1.8V	(9A)	(9.5A)
+0.9VS	(2A)	(2A)
+VCORE	(38A)	

<Variant Name>

ASUSTeK COMPUTER INC. NB

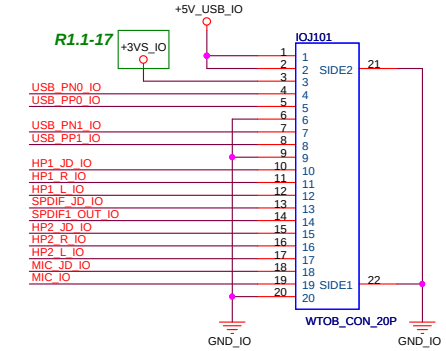
Title : POWER_FLOWCHART

Engineer: Amos_Yu

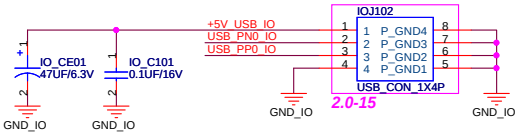
Size	Project Name	Rev
Custom	M50VM	1.1

Date: Wednesday, April 16, 2008 Sheet 94 of 94

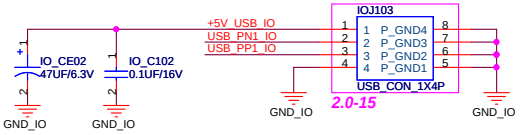
I/O Board

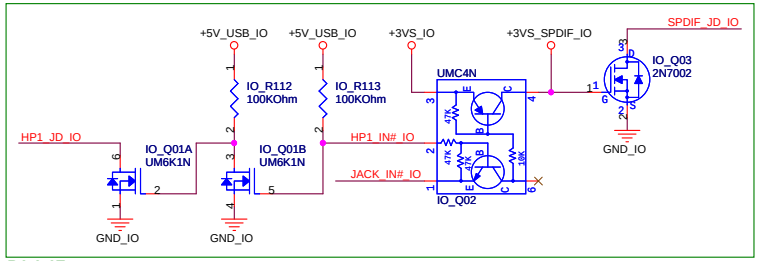


USB Port 0

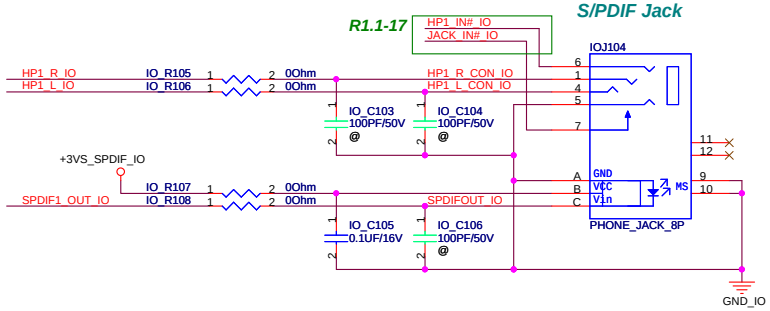


USB Port 1

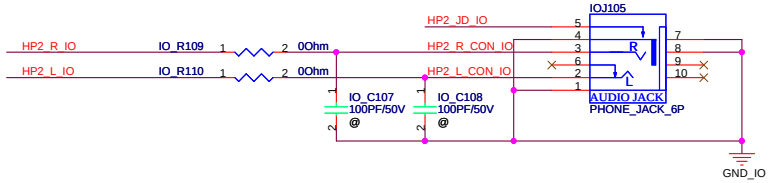




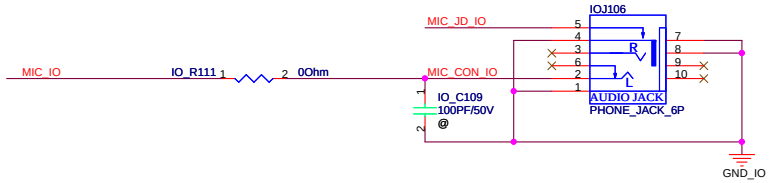
Headphone & S/PDIF Jack



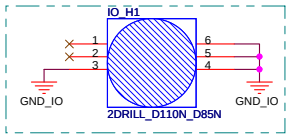
Headphone Jack



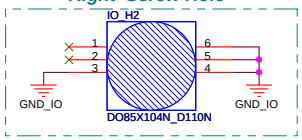
MIC In Jack



Left Screw Hole



Right Screw Hole



ASUSTeK COMPUTER INC. NB1

Title : USB & Audio Jack

Engineer: Wenchi_Shen

Size	Project Name	Rev
Custom	M50Vm	2.0

Date: Tuesday, April 15, 2008 Sheet 95 of 96

Rev	Date	Description
R1.0		First Release!
R1.1 Green Block		** Merge IO board into main board PCB. Page 95. 01.Remove VR_VID[6:0] testing series 0 0hm. Page 4. 02.Change 6pcs +VCORE capacitors to No-Stuff for cost down. Page 5. 03.Change 3pcs +0.9VS capacitors to No-Stuff for cost down. Page 9. 04.Change N1Sv USB port to follow N2Sv, and modify USB_OC#. Page 21,43,45. 05.PM Request: Change Bluetooth LED tp E-Mail LED. Page 22,56. 06.Follow Intel to change C2304 to 1uF/16V(XR). Page 23. 07.Follow R1E to change R2904 to 270ohm. Page 29. 08.Follow IT8752/8512 EC Common Hardware Pin Assignment v0.005, change GPE7 to INSTANT_ON# and GPG0 to PM_THERM#. Page 30. 09.PM REquest: Remove USB port charger function. Page 30,65. 10.PM change WWAN LED to touch-pad lock LED. Page 30,56. 11.Change IR to 36KHz to meet Vista remote control Min. range requirement. Page 31. 12.Remove testing 2nd CIR design. Page 31. 13.Change X3301 to 49S type for cost down. Page 33. 14.LAN chip version change. Page 33. 15.Audio codec chip change version. Page 36. 16.N1Sv/X55 will not supprot 3G function. Page 36,67. 17.Add S/PDIF & HDMI jack detect by Realtek sugesstion. Page 36,65,70,95. 18.Modify audio de-pop circuit. Page 36,37. 19.Modify LVDS power sequence failed bug. Page 45. 20.Modify LCD abnormal display bug due to LVDS pair mismatch. Page 45,70. 21.Remove HDTV support function. Page 47,70. 22.Remove HDMI EMI filter design. Page 48. 23.X55 need two pwer LEDs. Page 56. 24.PM change WLAN LED to RF LED. Page 56,63. 25.Bluetooth pin define error. Page 61. 26.Remove co-layout sequence logic control circuit. Page 68. 27.ME change parts: J3401,J5102,J6002,J6501. Page 34,51,60,65. 28.EMI modification. Page 34,36,65. 29.Crystal accuracy fine-tune. Page 30.USB droop test fail. Page 65. 31.Remove IO board USB common choke design. Page 95. 32.Speaker fine-tune. Page 37. 33.Cost down for 4-wire PWM fan. Page 50. 34.Cost down: Change RB717F to BAT54AW. Page 37,45,48,56.
R2.0 Pink Block		01.Change +1.25VS_MPLL, +1.25VS_PEGPLL & +1.8V_SM_CK PLL design. Page 15. 02.Add CMOS crack protection circuit. Page 22. 03.Reserve C2337 (10UF/16V) for +5VREF_ICH. Page 23. 04.With EMI RD's confirmation, remove reserved LAN common choke circuit. Page 34. 05.With EMI RD's confirmation, change R3612, R3614, R3615, R3616, R3622, R3624,R3626 to short-pad. Page 36. 06.With EMI RD's confirmation, remove reserved 1394 common choke circuit. Page 41. 07.With EMI RD's confirmation, remove reserved NewCard USB common choke circuit. Page 43. 08.Add NewCard debug card co-layout circuit. Page 44. 09.EMI modification: change reserved common choke circuit from USB port to internal camera port. Page 45. 10.HDMI jack detection modification. Page 48,70. 11.Change FAN capacitors to 10UF. Page 50. 12.Modify X55 power LED design. Page 56.

Rev	Date	Description
		13.With EMI RD's confirmation, remove reserved e-SATA/USB combo port USB common choke circuit. Page 41. 14.Reserve R8023 for shortage issue of ISL6262A. Page 80. 15.QTR USB plug test failed, change USB connector. Page 95.

ASUSTeK COMPUTER INC. NB1

Title : Revision History

Engineer: John Hung

Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Wednesday, February 13, 2008 Sheet 96 of 96