PROJECT N10I

Revision 2008/04/24

Revision History

R1.0	S R	2008/01

SMB Signals

Host	Name	Devices	Address
Chipset	SMBCK,SMBDA	ICH7-M	0001 000X b
		ADT7473(Thermal)	0101 110X b
		ICS954310(Clock Genertor)	D2h
		DDR2 SO-DIMM	A0h

Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+*VALWAYSP	+*V	+*VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCI Devices

Bus#	Device#	Function#	REQ/GNT#	IDSEL	APIC Interrupts	Device Function
Bus0	Device00	Function0				Intel 945GMS Host Bridge
Bus0	Device02	Function0				VGA-Comptible Controller
Bus0	Device1C	Function0				PCI to PCI Bridge
Bus0	Device27	Function0			A#	Azalia Controller
Bus0	Device29	Function0			H#	Intel UHCI USB Cotroller
Bus0	Device29	Function1			D#	Intel UHCI USB Cotroller
Bus0	Device29	Function2			C#	Intel UHCI USB Cotroller
Bus0	Device29	Function3			A#	Intel UHCI USB Cotroller
Bus0	Device29	Function7			H#	Intel EHCI USB Cotroller
Bus0	Device31	Function1			C#	PATA
Bus0	Device31	Function2			B#	SATA
Bus5	Device08	Function0		AD17	B#	CarBus Brige

Voltage Rail

Net Name	Voltage	On During These ACPI States	Description
+3VAO,+3VA,+3VALWAYS_P	+3.3V	S0 - S5	Always ON.
+5VCHG	+5V		
+VCC_RTC	+5V		
+3VO,+3VSUS,+3VALWAYS	+3V	S0,S3,S4*,S5*	Power supply for ICH7M, RTL8111B.
+5VO,+5VSUS	+5V		
+1.8VO,+1.8V	+1.8V	S0 - S3	Power supply for 945GMS,DDRII,ICH7M,M38857 R5C801.
+3V	+3V		
+5V	+5V		
+1.05VO,+VCCP	+1.05V	S0	0.9V DDR2 termination voltage
+1.5VO,+1.5VS	+1.5V		
+0.9VO,+0.9VS	+0.9V		Core voltage for processor
+2.5VO,+2.5VS,VCCA3GBG	+2.5VS		
VCCALVDS,VCCSYNC,VCCTXLVDS			
+3VS	+3V		
+5VS	+5V		
+VCORE_O,+VCORE	Variable		

ASUSTeK COMPUTER INC

Title : Table of Contens

Engineer: ENGINEER

Size	Project Name	Rev
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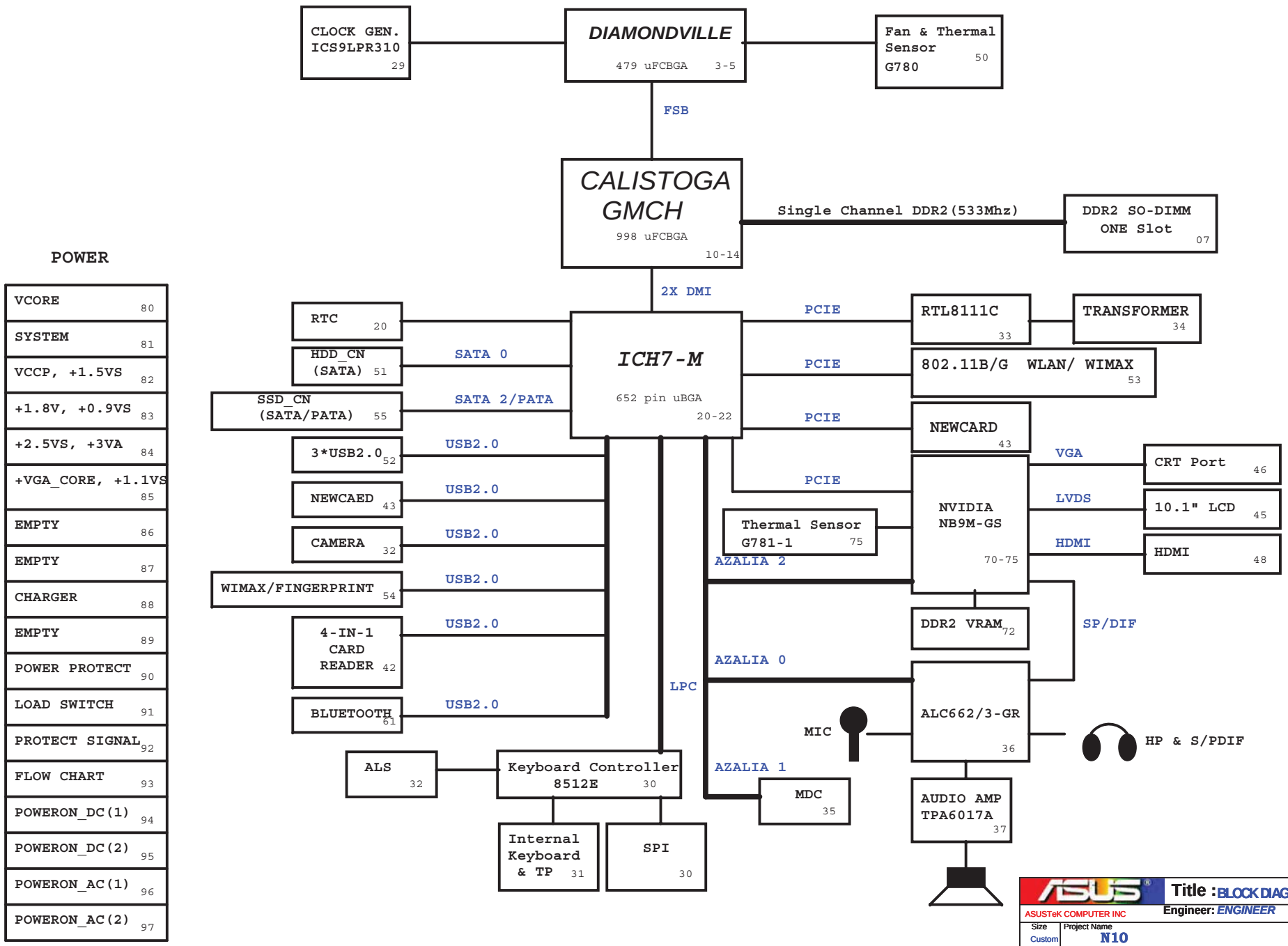
DIAMONDVILLE/CALISTOGA(945GSE) BLOCK DIAGRAM



POWER

VCORE	80
SYSTEM	81
VCCP, +1.5VS	82
+1.8V, +0.9VS	83
+2.5VS, +3VA	84
+VGA_CORE, +1.1VS	85
EMPTY	86
EMPTY	87
CHARGER	88
EMPTY	89
POWER PROTECT	90
LOAD SWITCH	91
PROTECT SIGNAL	92
FLOW CHART	93
POWERON_DC(1)	94
POWERON_DC(2)	95
POWERON_AC(1)	96
POWERON_AC(2)	97

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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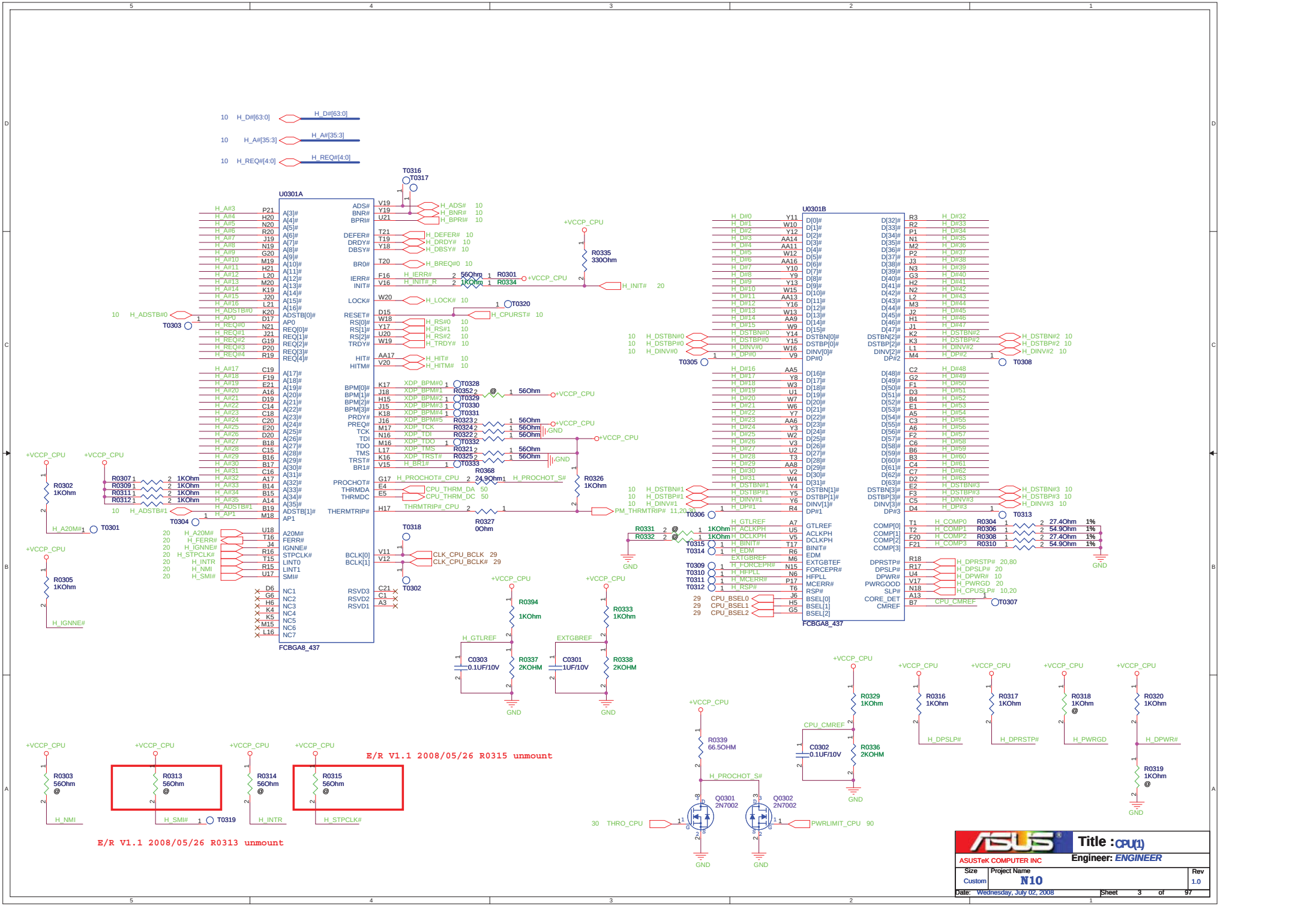
H_D#[63:0]
H_A#[35:3]
H_REQ#[4:0]
U0301A
FCBGA8_437
U0301B
FCBGA8_437
E/R V1.1 2008/05/26 R0315 unmount
E/R V1.1 2008/05/26 R0313 unmount
Title : CPU(1)
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size: Custom
Project Name: N10
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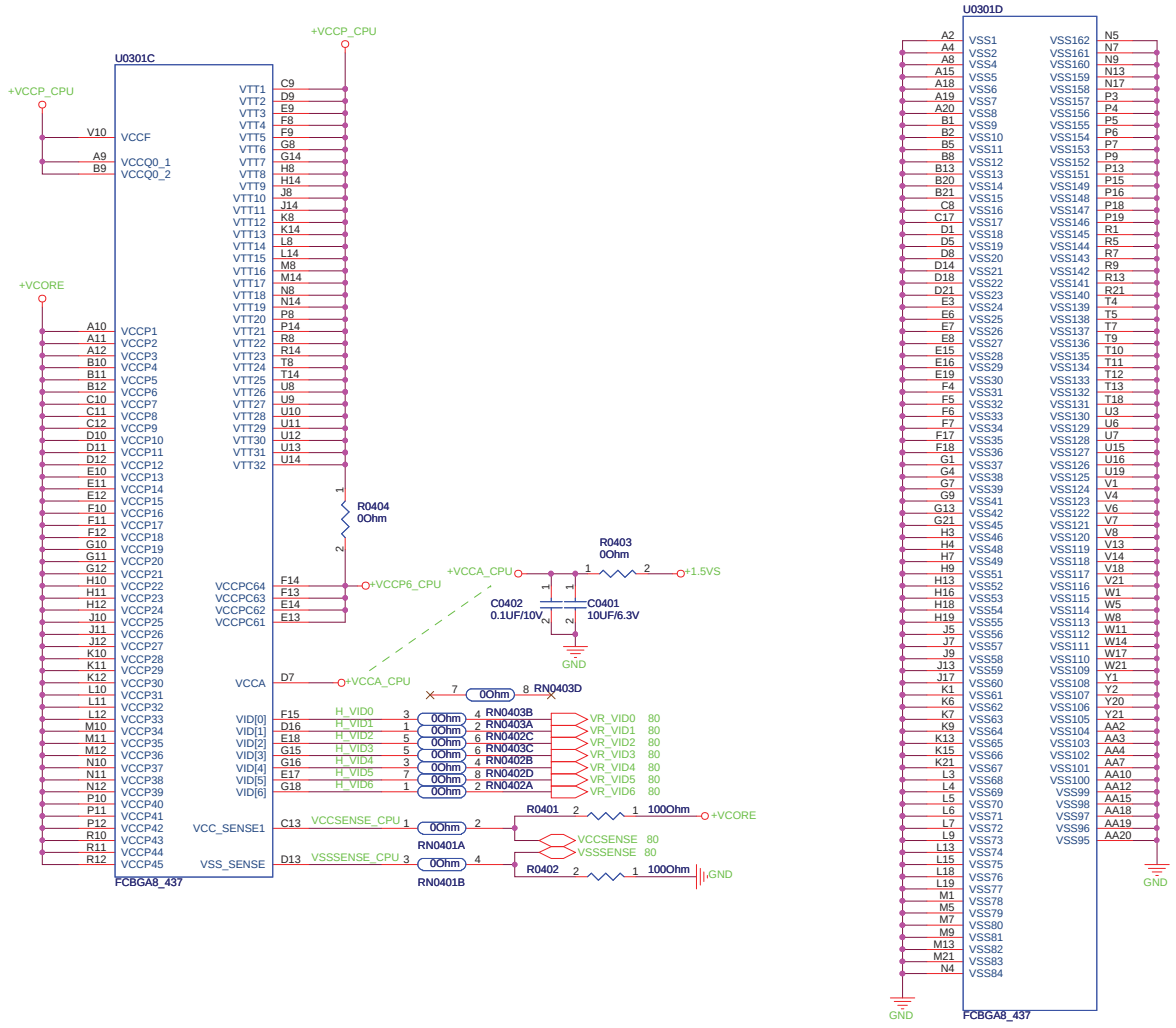

ASUSTeK COMPUTER INC

Title : CPU(2)

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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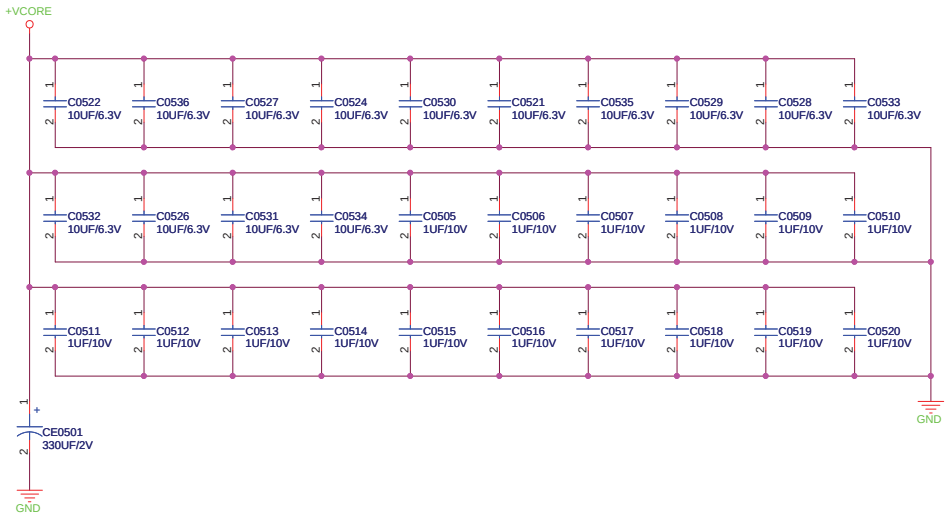
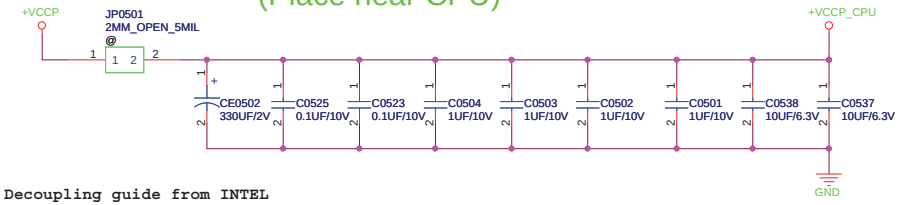


+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from INTEL

VCORE	1uF/10V	* 16pcs for CPU
	10uF/6.3V	*14pcs for CPU
	330uF/2V	* 1pcs for CPU
VCCP	0.1uF	* 2pcs for CPU
	1uF	* 4 pcs for CPU
	10uF	* 2 pcs for CPU
	330uF	* 1pcs for CPU

ASUSTeK COMPUTER INC

Title : CPU CAPS

Engineer: ENGINEER

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Title :	EMPTY
ASUSTeK COMPUTER INC	Engineer: ENGINEER
Size: Custom	Project Name: N10
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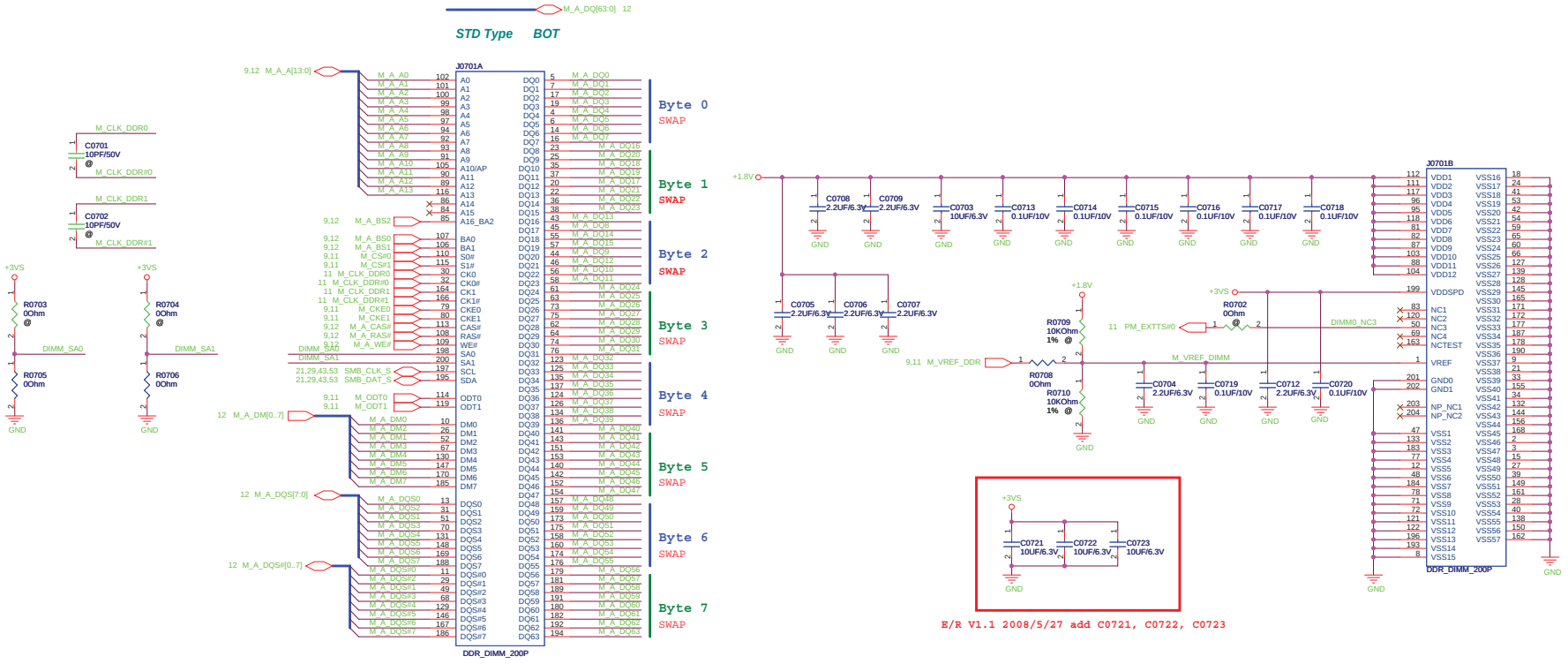

ASUSTeK COMPUTER INC	Title : DIMM		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
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Title :	EMPTY
ASUSTeK COMPUTER INC	Engineer: ENGINEER
Size: Custom	Project Name: N10
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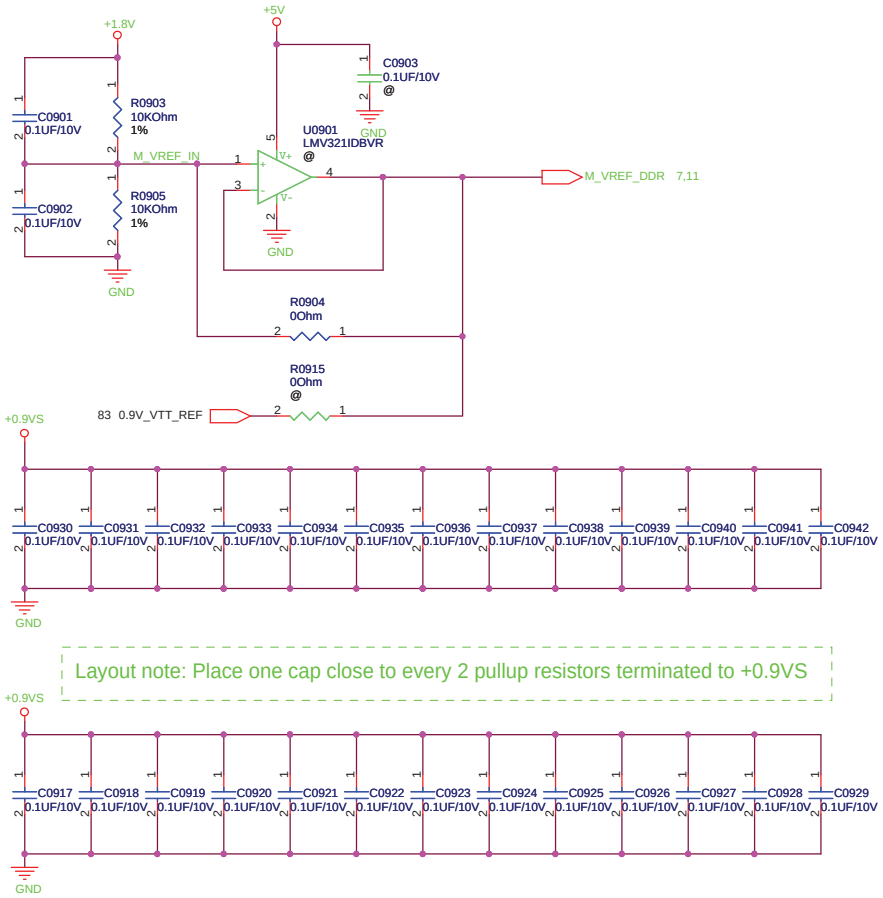
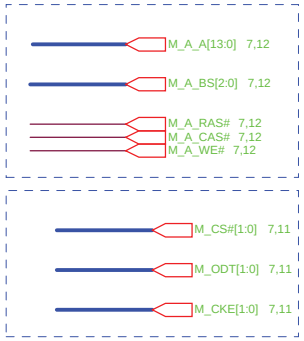
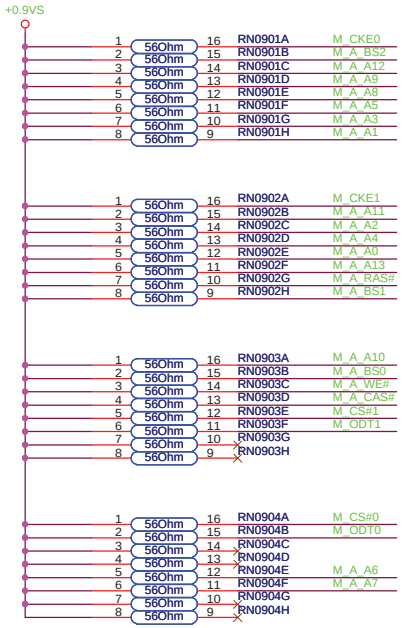


+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve SUSB# and SUSC#



HAD SWAPED



ASUSTeK COMPUTER INC

Title : DDR2 TERM

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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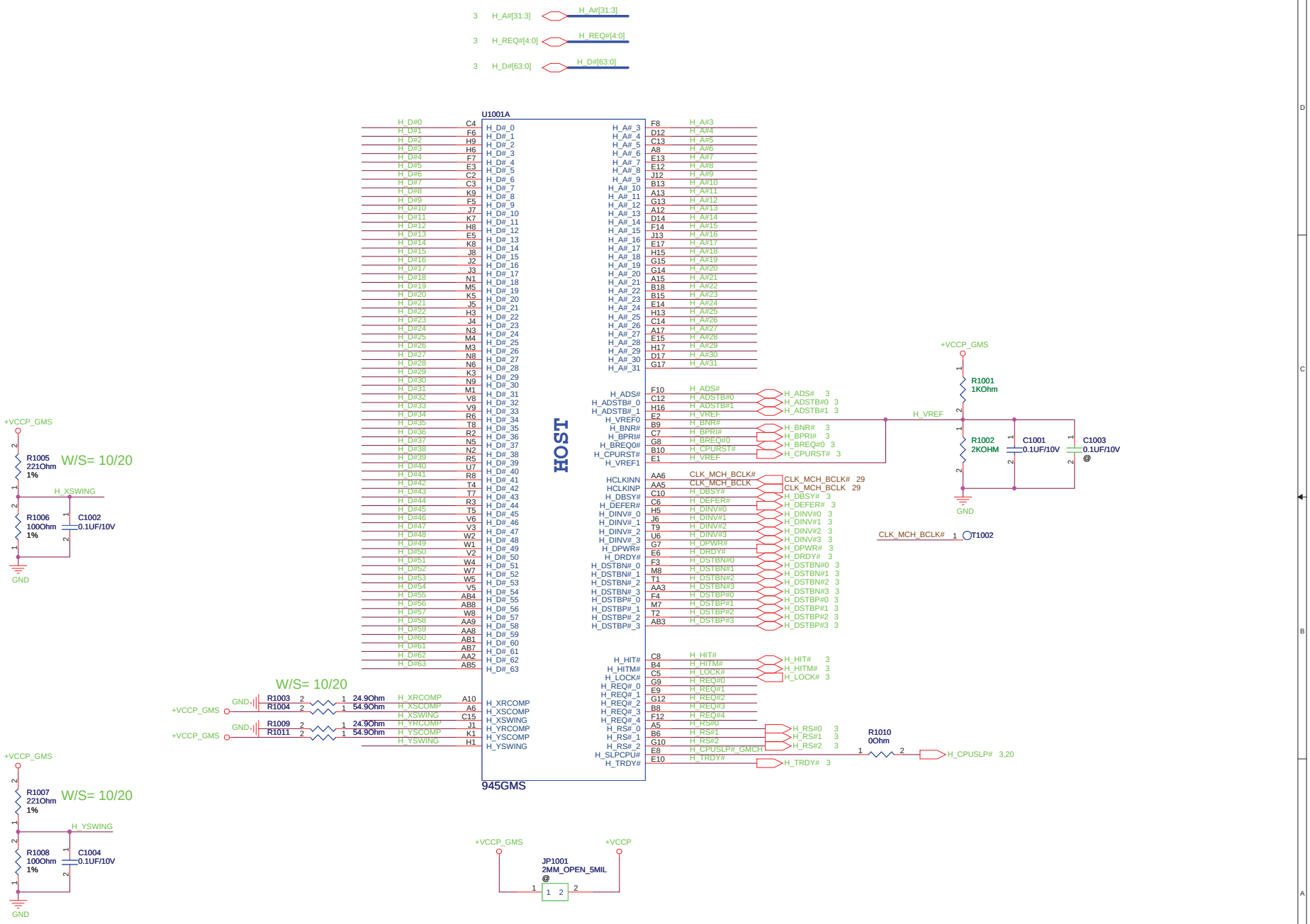

ASUSTeK COMPUTER INC	Title : Calistoga GMCH(1)		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
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TX/RX of DMI is viewed from ICH7M

Lane Reversal of DMI is not supported in 945GMS

CFG[2:0] :
001=FSB533
011=FSB667

CFG5 : DMI STRAP
LOW = DMI X 2
HIGH =RSVD

CFG[3,6] :
Reserved

U1001B

DMI_TXN0 Y29 / DMI_TXN1 Y32 / DMI_TXP0 Y28 / DMI_TXP1 Y31 / DMI_RXN0 V28 / DMI_RXN1 V31 / DMI_RXP0 V29 / DMI_RXP1 V32

M_CLK_DDR0 AF33 / M_CLK_DDR1 AG1 / AJ1 / AM30 / M_CLK_DDR#0 AG33 / M_CLK_DDR#1 AF1 / AK1 / AN30

M_CKE0 AN21 / M_CKE1 AN22 / AF26 / AF25

M_CS#0 AG14 / M_CS#1 AF12 / AK14 / AH12

M_ODT0 AE12 / M_ODT1 AE14 / AJ14 / AJ12

R1114 40.2Ohm M_OCDCOMP0 AJ21 / R1126 40.2Ohm M_OCDCOMP1 AF11

R1111 80.6Ohm M_RCOMP0 AN12 / R1112 80.6Ohm M_RCOMP AN14

M_VREF_MCH AA33 / AE1

DMI_RXN_0 DMI_RXN_1 DMI_RXP_0 DMI_RXP_1 DMI_TXN_0 DMI_TXN_1 DMI_TXP_0 DMI_TXP_1

SM_CK_0 SM_CK_1 SM_CK_2 SM_CK_3 SM_CK#_0 SM_CK#_1 SM_CK#_2 SM_CK#_3 SM_CKE_0 SM_CKE_1 SM_CKE_2 SM_CKE_3 SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 SM_OCDCOMP_0 SM_OCDCOMP_1 SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 SM_RCOMPN SM_RCOMPP SM_VREF_0 SM_VREF_1

DMI / DDR2 MUXING

CFG_0 CFG_1 CFG_2 CFG_3 CFG_5 CFG_6

C18 MCH_BSEL0 → MCH_BSEL0 29
E18 MCH_BSEL1 → MCH_BSEL1 29
G20 MCH_BSEL2 → MCH_BSEL2 29
G18 MCH_CFG3 — R1131 @ 2.2KOhm
J20 MCH_CFG5 — R1129 2.2KOhm
J18 MCH_CFG6 — R1130 @ 2.2KOhm → GND

RESERVED1 K32 / RESERVED2 K31 / RESERVED7 C17 / RESERVED8 F18 / RESERVED9 A33 — MCH_RSVD9 — R1133 0Ohm → GND

CFG/RSVD

E31 MCH_SYNC# → MCH_SYNC# 21
G21 PM_BMBUSY# → PM_BMBUSY# 21
F26 PM_EXTTS#0
H26 PM_EXTTS#1 — R1118 0Ohm @
J15 THRMTRIP# GMCH — R1125 0Ohm
AB29 PM_PWROK_MCH — R1127 0Ohm → PM_PWROK 21,30
W27 PLT_RST#_MCH — R1102 100Ohm → PLT_RST# 21,33,42

ICH_SYNC# PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 THRMTRIP# PWROK RSTIN#

PM

A27 CLK_DREFCLK# 29
A26 CLK_DREFCLK 29
J33 CLK_DREFSS# 29
H33 CLK_DREFSS 29
J22 CLK_MCH_REQ# 29

D_REFCLKINN D_REFCLKINP D_REFSSCLKINN D_REFSSCLKINP CLKREQ#

CLK

945GMS

+1.8V
R1116 10KOhm 1% @
R1113 0Ohm → M_VREF_DDR 7,9
C1102 0.1UF/10V @
C1101 0.1UF/10V @
C1103 2.2UF/6.3V @
R1121 10KOhm 1% @
GND

+3VS
R1119 10KOhm PM_EXTTS#0 → PM_EXTTS#0 7
R1120 10KOhm PM_EXTTS#1
使用 FAST C4E EXIT R1120 內有PU 不可以上
不用 FAST C4E EXIT R1120 就必須上

R1109 10KOhm
T1102 SDVO_CRTLDATA / SDVO_CRTLCLK
29 CLK_MCH_3GPLL# / 29 CLK_MCH_3GPLL

R1137 10KOhm CRT_DDCCLK_MCH
R1138 10KOhm CRT_DDCDAT_MCH
47 CRT_DDCCLK_MCH / 47 CRT_DDCDAT_MCH
47 CRT_BLUE_MCH
R1139 1% 150Ohm CRT_BLUE_MCH
47 CRT_GREEN_MCH
R1140 1% 150Ohm CRT_GREEN_MCH
47 CRT_RED_MCH
R1141 1% 150Ohm CRT_RED_MCH
47 CRTVSYNC_MCH
47 CRTHSYNC_MCH
R1128 1% 255Ohm CRT_IREF

R1123 10KOhm
R1124 10KOhm
47 LCD_BLADJ_MCH
47 LCD_BLEN_MCH
L_CTLA_CLK
L_CTLB_DATA
47 EDIDCLK_MCH
47 EDIDDAT_MCH
47 LCD_VDDEN_MCH
R1122 1.5KOhm L_IBG L_VBG
T1103

R1135 10KOhm EDIDCLK_MCH
R1136 10KOhm EDIDDAT_MCH

47 LVDS_LCLKN_MCH
47 LVDS_LCLKP_MCH
47 LVDS_L0N_MCH
47 LVDS_L1N_MCH
47 LVDS_L2N_MCH
47 LVDS_L0P_MCH
47 LVDS_L1P_MCH
47 LVDS_L2P_MCH

U1001F

SDVO_CTRLDATA H27 / SDVO_CTRLCLK J27 / G_CLKINN Y26 / G_CLKINP AA26

CRT_DDC_CLK H20 / CRT_DDC_DATA H22 / CRT_BLUE A24 / CRT_BLUE# A23 / CRT_GREEN E25 / CRT_GREEN# F25 / CRT_RED C25 / CRT_RED# D25 / CRT_VSYNC F27 / CRT_HSYNC D27 / CRT_IREF H25

L_BKLTCTL H30 / L_BKLTEN G29 / L_CLKCTLA F28 / L_CTLBDATA E28 / L_DDC_CLK G28 / L_DDC_DATA H28 / L_VDDEN K30 / L_IBG K27 / L_VBG J29 / L_VREFH J30 / L_VREFL K29

LA_CLKN D30 / LA_CLKP C30 / LB_CLKN A30 / LB_CLKP A29

LA_DATAN_0 G31 / LA_DATAN_1 F32 / LA_DATAN_2 D31

LA_DATAP_0 H31 / LA_DATAP_1 G32 / LA_DATAP_2 C31

LB_DATAN_0 F33 / LB_DATAN_1 D33 / LB_DATAN_2 F30

LB_DATAP_0 E33 / LB_DATAP_1 D32 / LB_DATAP_2 F29

MISC / VGA / LVDS

945GMS

EXP_A_COMPI R28 / EXP_A_ICOMPO M28 → PEG_COMP
SDVO_TVCLKIN# N30 / SDVOB_INT# R30 / SDVO_FLDSTALL# T29
SDVO_TVCLKIN M30 / SDVO_INT P30 / SDVO_FLDSTALL T30

SDVO DISABLE:
SIGNAL BE
LEFT NC

SDVO_RED# P28 / SDVO_GREEN# N32 / SDVO_BLUE# P32 / SDVO_CLKN T32
SDVO_RED N28 / SDVO_GREEN M32 / SDVO_BLUE P33 / SDVO_CLKP R32

TV_DACA_OUT A21 / TV_DACB_OUT C20 / TV_DACC_OUT E20 / TV_IREF G23 / TV_IRTNA B21 / TV_IRTNB C21 / TV_IRTNC D21

TV_DCONSEL0 G26 / TV_DCONSEL1 J26

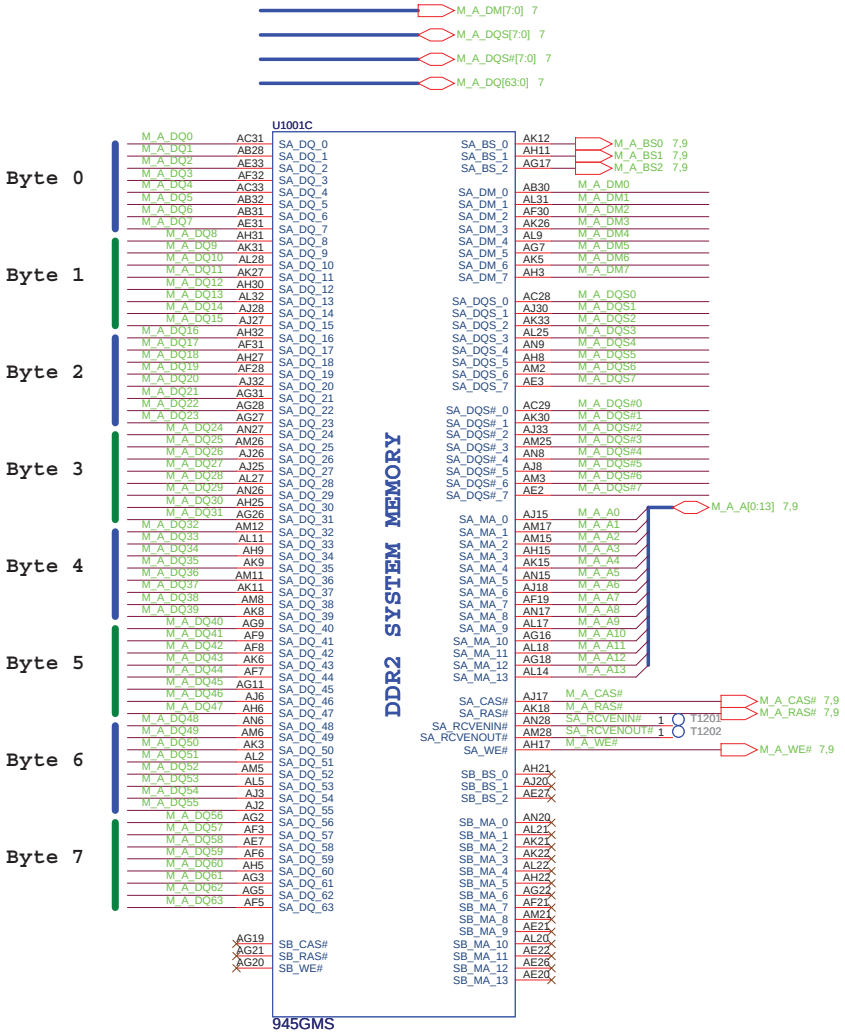
TV-OUT
DISABLE:
SIGNAL/POWER
TO 1.5V

+1.5VS_PCIE
R1101 24.9Ohm 1%

+1.5VS

SDVO

TV



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Title : Calistoga GMCH (3)

Engineer: ENGINEER

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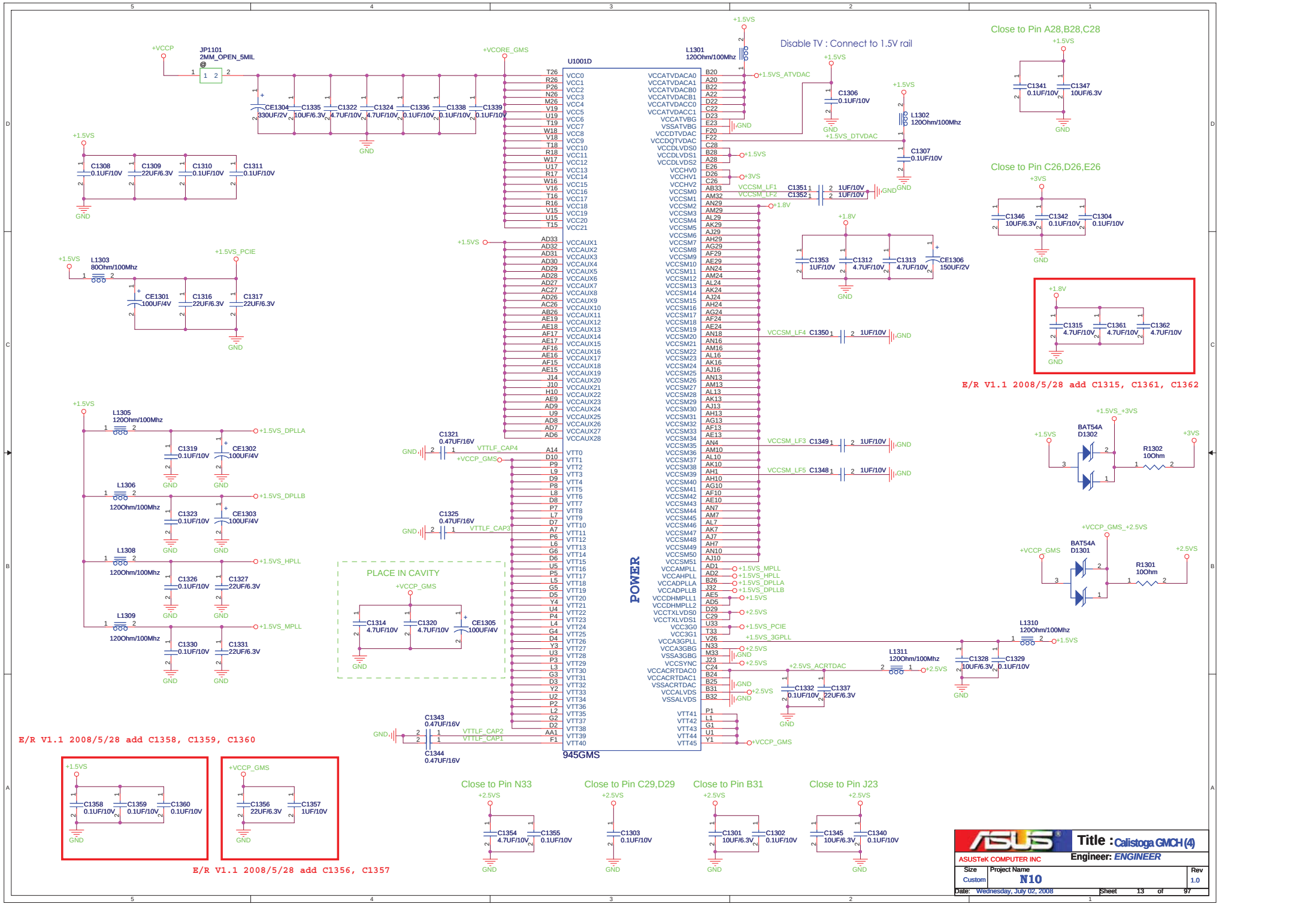
U1001D
945GMS
POWER
Disable TV : Connect to 1.5V rail
Close to Pin A28,B28,C28
Close to Pin C26,D26,E26
E/R V1.1 2008/5/28 add C1315, C1361, C1362
E/R V1.1 2008/5/28 add C1358, C1359, C1360
E/R V1.1 2008/5/28 add C1356, C1357
PLACE IN CAVITY
Close to Pin N33
Close to Pin C29,D29
Close to Pin B31
Close to Pin J23
Title : Calistoga GMCH (4)
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Project Name N10
Size Custom
Rev 1.0
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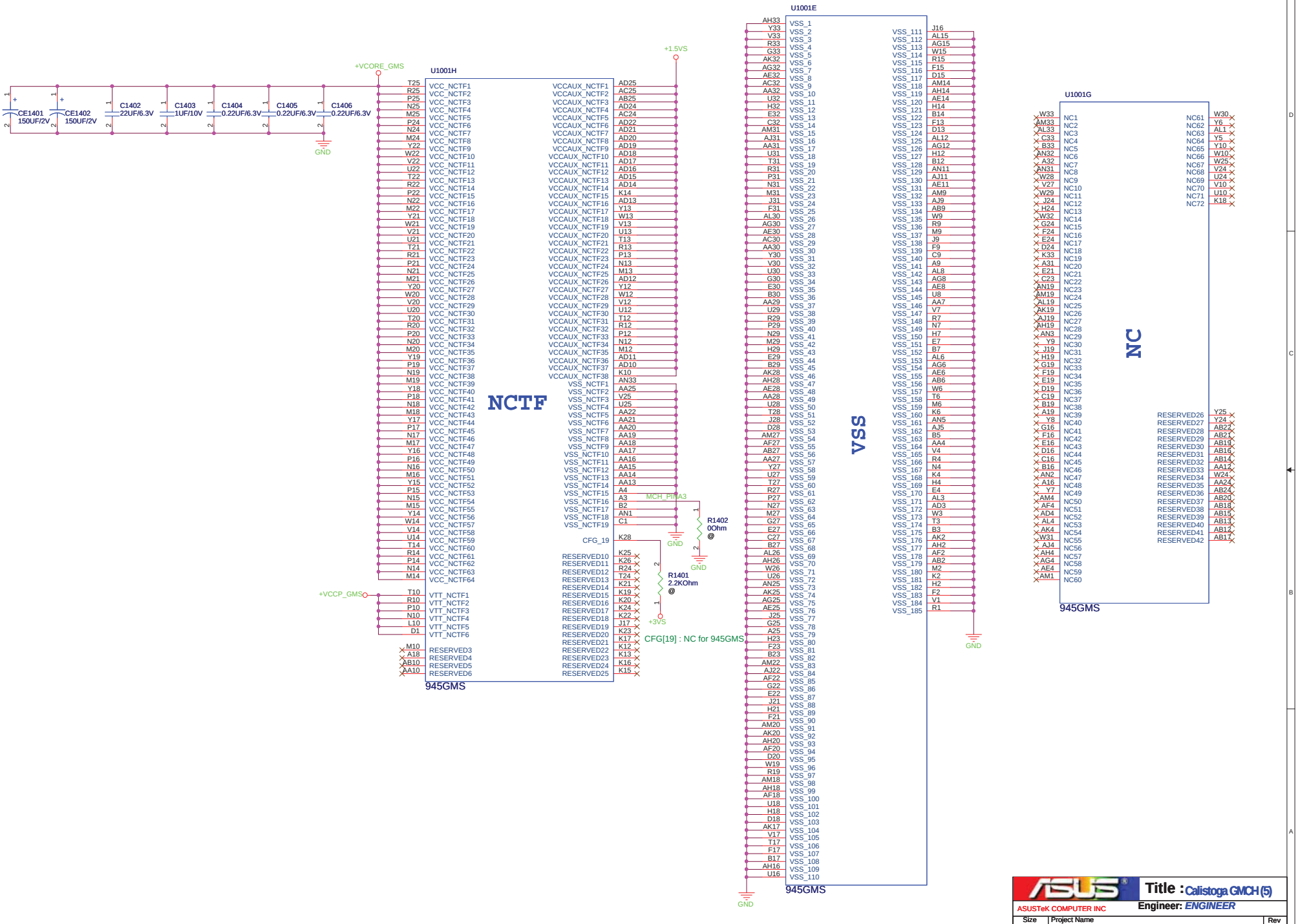
+VCORE_GMS
CE1401 150UF/2V
CE1402 150UF/2V
C1402 22UF/6.3V
C1403 1UF/10V
C1404 0.22UF/6.3V
C1405 0.22UF/6.3V
C1406 0.22UF/6.3V
GND
U1001H
NCTF
945GMS
+1.5VS
MCH_PWRA3
R1402 0Ohm @
R1401 2.2KOhm @
+3VS
CFG_19
CFG[19] : NC for 945GMS
+VCCP_GMS
U1001E
VSS
945GMS
U1001G
NC
945GMS
ASUSTeK COMPUTER INC
Title : Calistoga GMCH (5)
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

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	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

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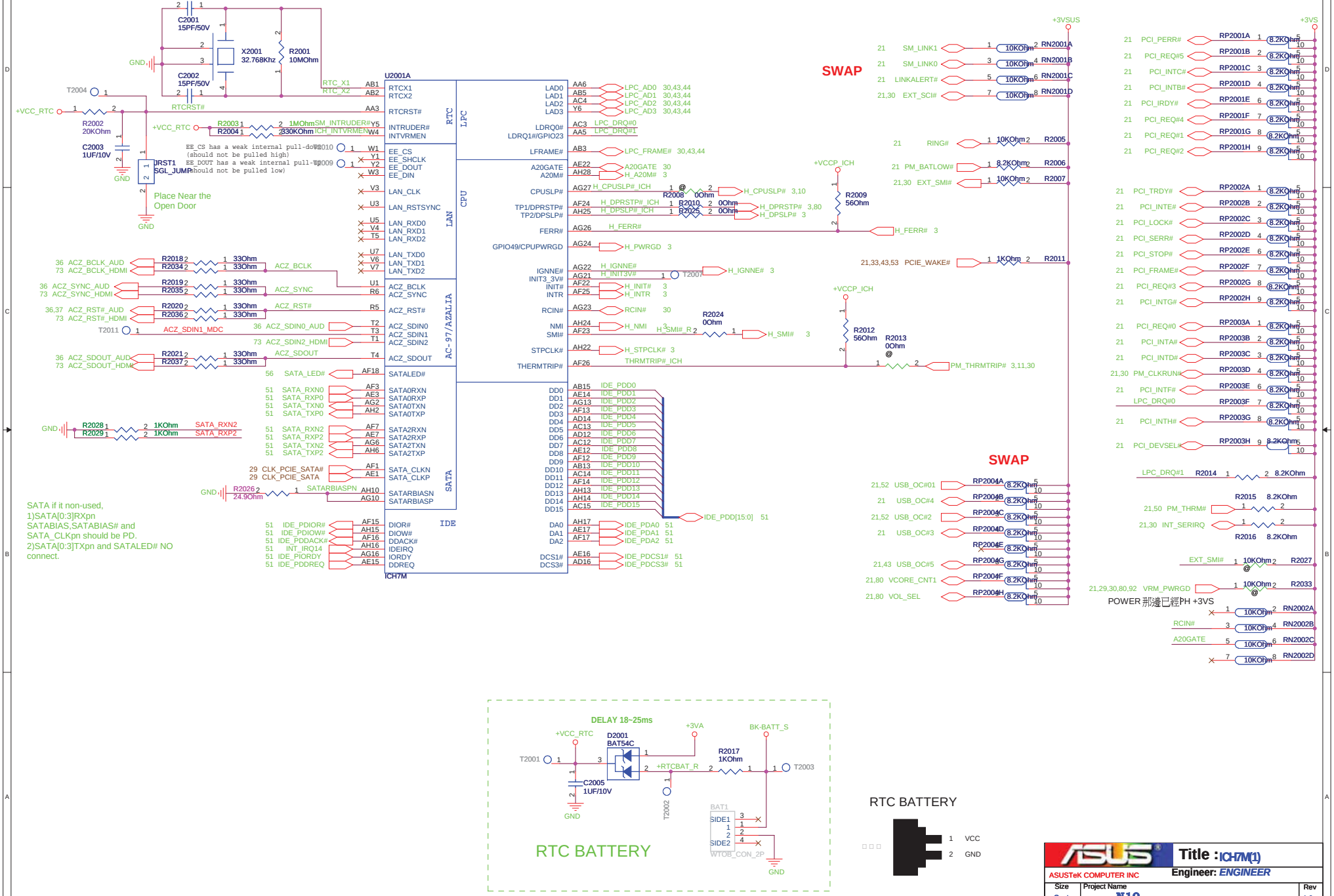

C2001 15PF/50V
X2001 32.768Khz
R2001 10MOhm
C2002 15PF/50V
GND
RTC_X1
RTC_X2
T2004
+VCC_RTC
RTCRST#
R2002 20KOhm
R2003 1MOhm
R2004 330KOhm
SM_INTRUDER#
ICH_INTVRMEN
C2003 1UF/10V
JRST1
SGL_JUMP
EE_CS has a weak internal pull-down (should not be pulled high)
EE_DOUT has a weak internal pull-up (should not be pulled low)
Place Near the Open Door
U2001A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH7M
RTC
LPC
CPU
LAN
AC-97/AZALIA
SATA
IDE
R2018 33Ohm ACZ_BCLK
R2019 33Ohm ACZ_SYNC
R2020 33Ohm ACZ_RST#
R2021 33Ohm ACZ_SDOUT
ACZ_SDIN0_AUD
ACZ_SDIN1_MDC
ACZ_SDIN2_HDMI
SATA_LED#
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
R2028 1KOhm SATA_RXN2
R2029 1KOhm SATA_RXP2
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
CLK_PCIE_SATA#
CLK_PCIE_SATA
R2026 24.9Ohm
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
INT_IRQ14
IDE_PIORDY
IDE_PDDREQ
SATA if it non-used,
1)SATA[0:3]RXpn
SATABIAS,SATABIAS# and
SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO
connect.
LAD0 LPC_AD0 30,43,44
LAD1 LPC_AD1 30,43,44
LAD2 LPC_AD2 30,43,44
LAD3 LPC_AD3 30,43,44
LDRQ0# LPC_DRQ#0
LDRQ1#/GPIO23 LPC_DRQ#1
LFRAME# LPC_FRAME# 30,43,44
A20GATE A20GATE 30
A20M# H_A20M# 3
CPUSLP# H_CPUSLP#_ICH
H_CPUSLP# 3,10
TP1/DPRSTP# H_DPRSTP#_ICH
TP2/DPSLP# H_DPSLP#_ICH
H_DPRSTP# 3,80
H_DPSLP# 3
FERR# H_FERR#
GPIO49/CPUPWRGD H_PWRGD 3
IGNNE# H_IGNNE#
INIT3_3V# H_INIT3V#
INIT# H_INIT#
INTR H_INTR
RCIN# RCIN#
NMI H_NMI
SMI# H_SMI#
STPCLK# H_STPCLK#
THERMTRIP# THRMTRIP#_ICH
R2008 0Ohm
R2010 0Ohm
R2025 0Ohm
R2024 0Ohm
R2009 56Ohm
R2012 56Ohm
R2013 0Ohm
+VCCP_ICH
H_FERR# 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
H_SMI# 3
H_STPCLK# 3
PM_THRMTRIP# 3,11,30
DD0 IDE_PDD0
DD1 IDE_PDD1
DD2 IDE_PDD2
DD3 IDE_PDD3
DD4 IDE_PDD4
DD5 IDE_PDD5
DD6 IDE_PDD6
DD7 IDE_PDD7
DD8 IDE_PDD8
DD9 IDE_PDD9
DD10 IDE_PDD10
DD11 IDE_PDD11
DD12 IDE_PDD12
DD13 IDE_PDD13
DD14 IDE_PDD14
DD15 IDE_PDD15
IDE_PDD[15:0] 51
DA0 IDE_PDA0 51
DA1 IDE_PDA1 51
DA2 IDE_PDA2 51
DCS1# IDE_PDCS1# 51
DCS3# IDE_PDCS3# 51
SWAP
+3VSUS
SM_LINK1 10KOhm RN2001A
SM_LINK0 10KOhm RN2001B
LINKALERT# 10KOhm RN2001C
EXT_SCI# 10KOhm RN2001D
RING# 10KOhm R2005
PM_BATLOW# 8.2KOhm R2006
EXT_SMI# 10KOhm R2007
PCIE_WAKE# 1KOhm R2011
USB_OC#01 RP2004A
USB_OC#4 RP2004B
USB_OC#2 RP2004C
USB_OC#3 RP2004D
USB_OC#5 RP2004E
VCORE_CNT1 RP2004F
VOL_SEL RP2004H
SWAP
+3VS
PCI_PERR# RP2001A
PCI_REQ#5 RP2001B
PCI_INTC# RP2001C
PCI_INTB# RP2001D
PCI_IRDY# RP2001E
PCI_REQ#4 RP2001F
PCI_REQ#1 RP2001G
PCI_REQ#2 RP2001H
PCI_TRDY# RP2002A
PCI_INTE# RP2002B
PCI_LOCK# RP2002C
PCI_SERR# RP2002D
PCI_STOP# RP2002E
PCI_FRAME# RP2002F
PCI_REQ#3 RP2002G
PCI_INTG# RP2002H
PCI_REQ#0 RP2003A
PCI_INTA# RP2003B
PCI_INTD# RP2003C
PM_CLKRUN# RP2003D
PCI_INTF# RP2003E
LPC_DRQ#0 RP2003F
PCI_INTH# RP2003G
PCI_DEVSEL# RP2003H
LPC_DRQ#1 R2014 8.2KOhm
R2015 8.2KOhm
R2016 8.2KOhm
PM_THRM#
INT_SERIRQ
EXT_SMI# R2027
VRM_PWRGD R2033
POWER 那邊已經PH +3VS
RN2002A
RN2002B
RN2002C
RN2002D
RCIN#
A20GATE
DELAY 18~25ms
+VCC_RTC
D2001 BAT54C
+3VA
BK-BATT_S
T2001
R2017 1KOhm
+RTCBAT_R
T2003
C2005 1UF/10V
T2002
BAT1
SIDE1
SIDE2
WTOB_CON_2P
RTC BATTERY
RTC BATTERY
1 VCC
2 GND
ASUSTeK COMPUTER INC
Title : ICH7M(1)
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
Sheet 20 of 97

ICH7 Boot BIOS select

GNT#5	GNT#4	
LPC	11	(default)
PCI	10	
SPI	01	

GNT#3 without PD, if NOT top-block swap(inter high)

PCIE TX/RX 方向命名是以ICH7M 爲中心

TX/RX of DMI is viewed from ICH7M
Lane Reversal of DMI is not supported in 945GMS

U2001B

PCI

Interrupt I/F

MISC

ICH7M

U2001D

PCI-Express

Direct Media Interface

SPI

USB

ICH7M

E/R 20080519

E/R 20080514 超頻

E/R V1.1 2008/5/28 R2137 100k ohm change to 10k ohm

P/R V2.0 2008/7/01 when mount R2151 --> N10J

P/R V2.0 2008/7/01 when mount R2152 --> N10E

SPKR signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

SWAP

U2001C

SMB

Clocks

SYS GPIO

Power MGT

GPIO

ICH7M

E/R 20080522 F/P on-off

POWER 那邊已經PH +3VS
R2128 如果上會形成分壓

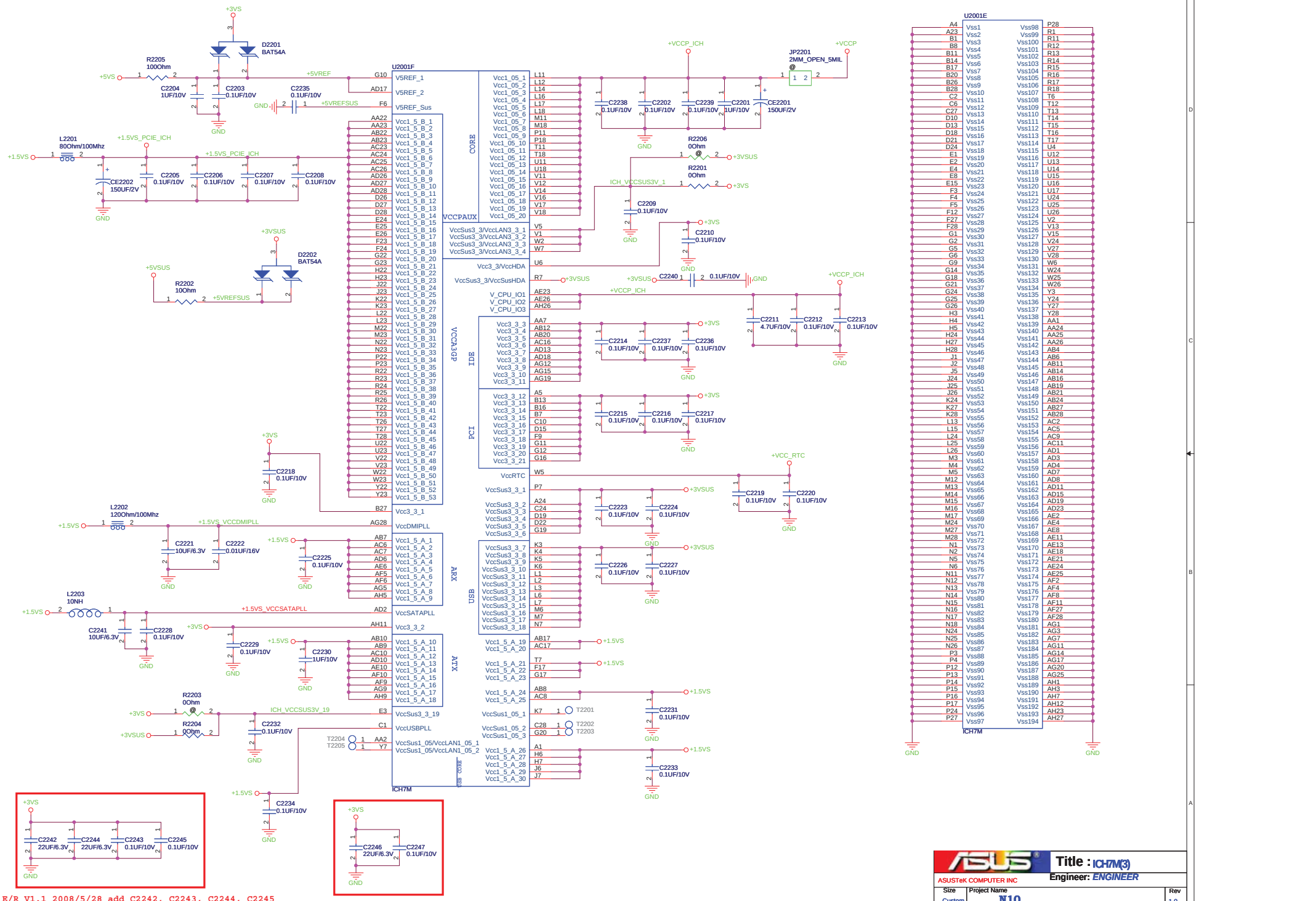
GPIO[25] is a reserved signal.
The signal has a weak internal pull-up
and should not be pulled low

ICH7 GPIO	PCB_ID
GPIO39	PCB_ID2
GPIO38	PCB_ID1
GPIO37	PCB_ID0

E/R V1.1 2008/5/28 R2136 100k ohm change to 10k ohm

P/R V2.0 2008/6/29 GPIO25 change to FP_ON

ASUSTeK COMPUTER INC	Title : ICH7M(2)	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 21 of 97	


U2001F
ICH7M
U2001E
ICH7M
D2201
BAT54A
D2202
BAT54A
JP2201
2MM_OPEN_5MIL
R2205
100Ohm
R2206
0Ohm
R2201
0Ohm
R2202
10Ohm
R2203
0Ohm
R2204
0Ohm
L2201
80Ohm/100Mhz
L2202
120Ohm/100Mhz
L2203
10NH
+3VS
+5VS
+1.5VS
+5VSUS
+3VSUS
+VCCP_ICH
+VCCP
+VCC_RTC
+5VREF
+5VREFSUS
+1.5VS_PCIE_ICH
+1.5VS_VCCDMIPLL
+1.5VS_VCCSATAPLL
ICH_VCCSUS3V_1
ICH_VCCSUS3V_19
GND
CORE
VCCPAUX
VCCA3GP
IDE
PCI
ARX
USB
ATX
E/R V1.1 2008/5/28 add C2242, C2243, C2244, C2245
E/R V1.1 2008/5/28 add C2246, C2247
ASUSTeK COMPUTER INC
Title : ICH7M(3)
Engineer: ENGINEER
Size: Custom
Project Name: N10
Rev: 1.0
Date: Wednesday, July 02, 2008
Sheet 22 of 97

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 23 of 97

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 24 of 97		

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 25 of 97

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 26 of 97

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 27 of 97

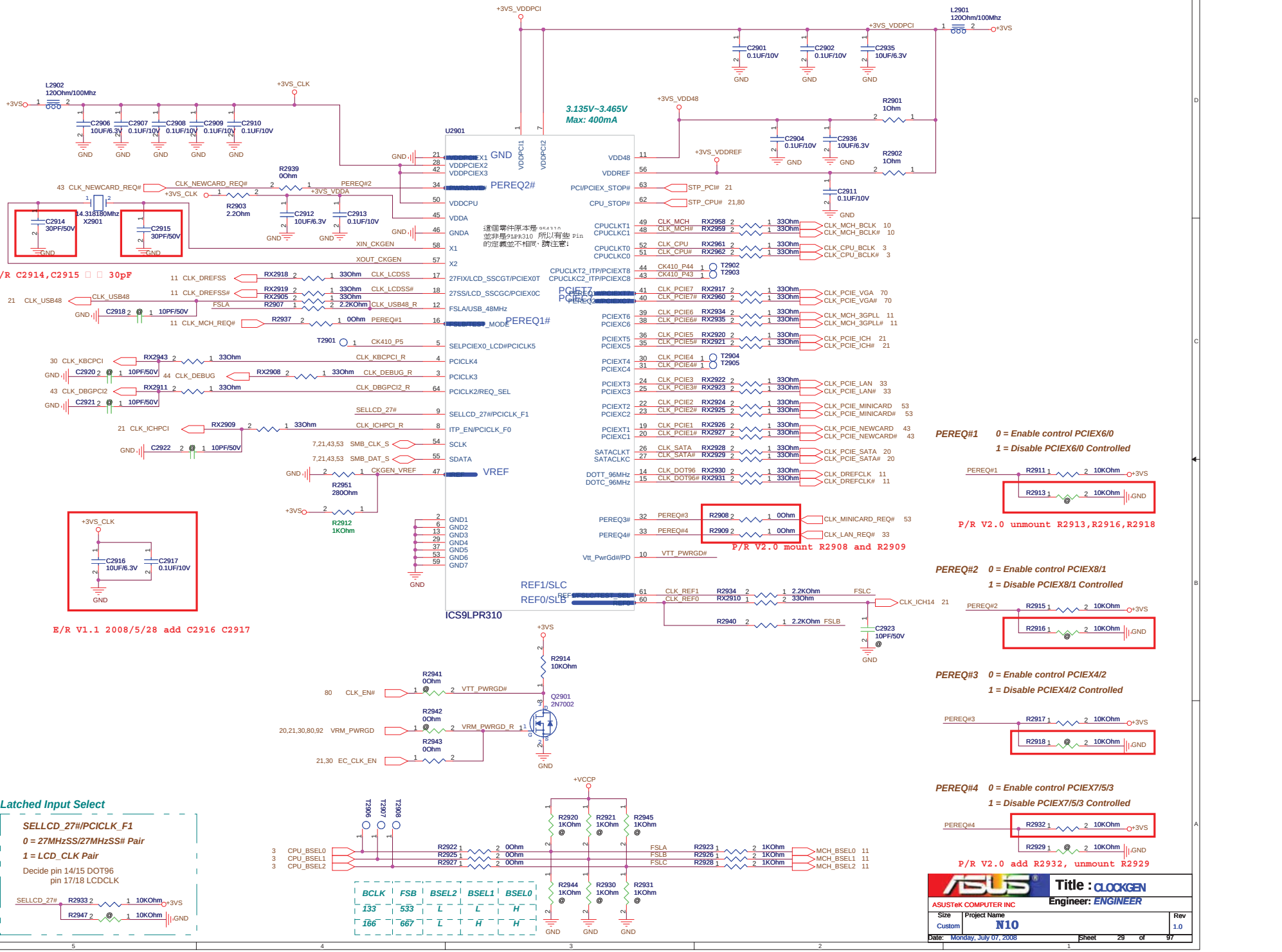
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 28 of 97


U2901
ICS9LPR310
3.135V~3.465V
Max: 400mA
E/R C2914,C2915 30pF
E/R V1.1 2008/5/28 add C2916 C2917
PEREQ#1 0 = Enable control PCIEX6/0
1 = Disable PCIEX6/0 Controlled
P/R V2.0 unmount R2913,R2916,R2918
PEREQ#2 0 = Enable control PCIEX8/1
1 = Disable PCIEX8/1 Controlled
PEREQ#3 0 = Enable control PCIEX4/2
1 = Disable PCIEX4/2 Controlled
PEREQ#4 0 = Enable control PCIEX7/5/3
1 = Disable PCIEX7/5/3 Controlled
P/R V2.0 mount R2908 and R2909
P/R V2.0 add R2932, unmount R2929
Latched Input Select
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
Decide pin 14/15 DOT96
pin 17/18 LCDCLK
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCKGEN
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Project Name N10
Size Custom
Rev 1.0
Date: Monday, July 07, 2008
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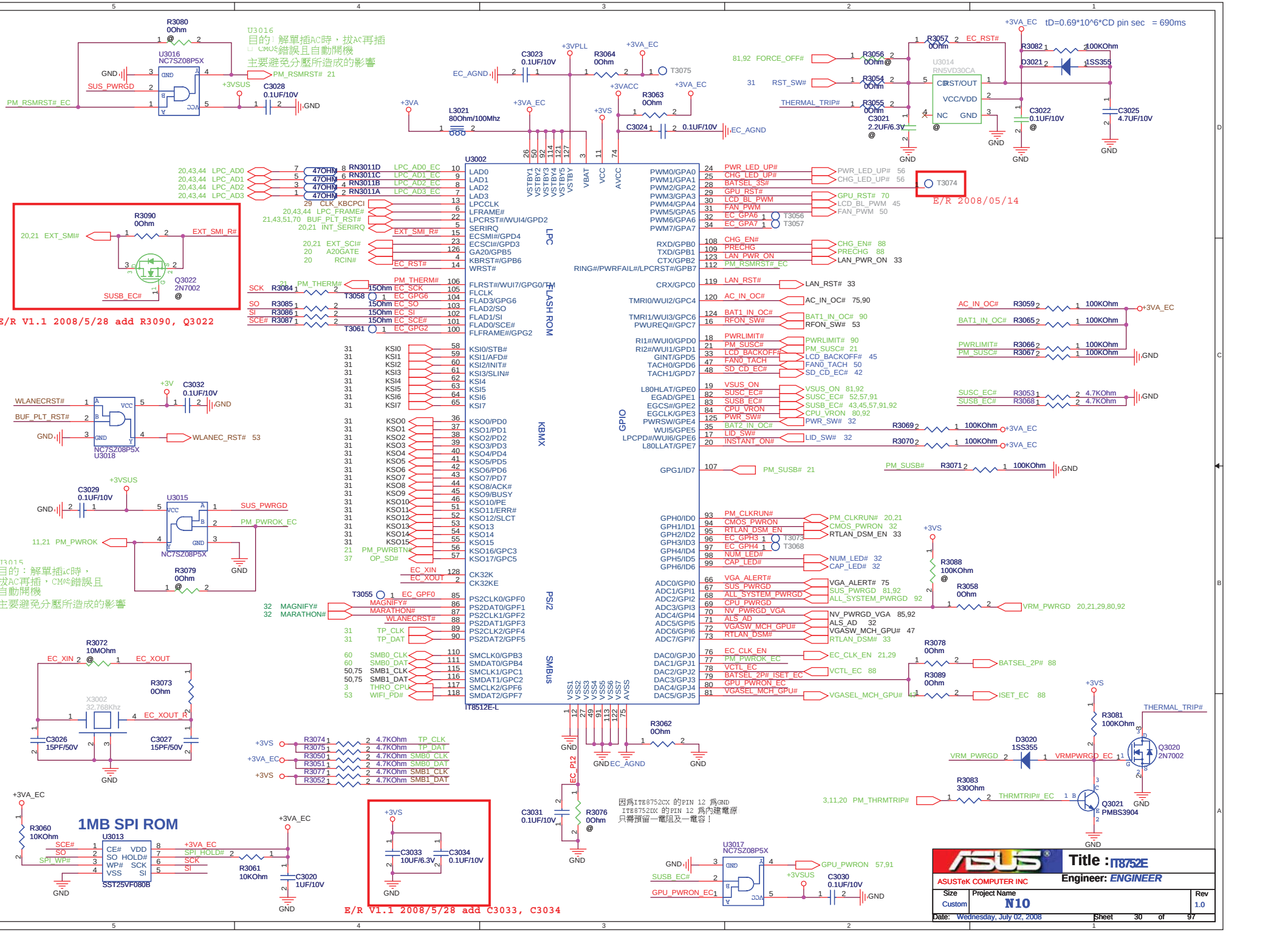
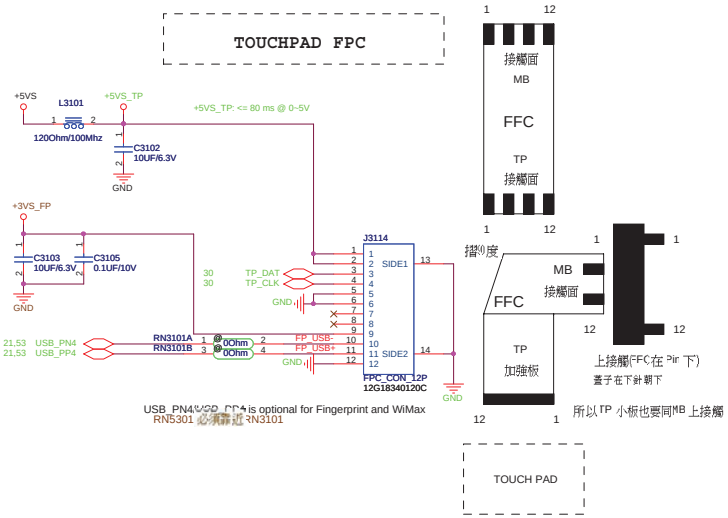

U3016
目的：解單插AC時，拔AC再插
CMOS錯誤且自動開機
主要避免分壓所造成的影響
R3080 0Ohm
U3016 NC7SZ08P5X
PM_RSMRST# 21
PM_RSMRST# EC
SUS_PWRGD
+3VSUS
C3028 0.1UF/10V
C3023 0.1UF/10V
+3VPLL
R3064 0Ohm
+3VA_EC
T3075
EC_AGND
+3VA
L3021 80Ohm/100Mhz
+3VACC
R3063 0Ohm
+3VS
C3024 0.1UF/10V
81,92 FORCE_OFF#
R3056 0Ohm
R3057 0Ohm
EC_RST#
31 RST_SW#
R3054 0Ohm
THERMAL_TRIP#
R3055 0Ohm
U3014 RN5VD30CA
CE
RST/OUT
VCC/VDD
NC
GND
C3021 2.2UF/6.3V
C3022 0.1UF/10V
C3025 4.7UF/10V
R3082 100KOhm
D3021 1SS355
tD=0.69*10^6*CD pin sec = 690ms
U3002
LAD0
LAD1
LAD2
LAD3
LPCCLK
LFRAME#
LPCRST#/WUI4/GPD2
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
GA20/GPB5
KBRST#/GPB6
WRST#
LPC
20,43,44 LPC_AD0
20,43,44 LPC_AD1
20,43,44 LPC_AD2
20,43,44 LPC_AD3
RN3011D LPC_AD0_EC
RN3011C LPC_AD1_EC
RN3011B LPC_AD2_EC
RN3011A LPC_AD3_EC
47OHM
29 CLK_KBCPCI
20,43,44 LPC_FRAME#
21,43,51,70 BUF_PLT_RST#
20,21 INT_SERIRQ
EXT_SMI_R#
20,21 EXT_SCI#
20 A20GATE
20 RCIN#
EC_RST#
R3090 0Ohm
20,21 EXT_SMI#
Q3022 2N7002
SUSB_EC#
E/R V1.1 2008/5/28 add R3090, Q3022
FLASH ROM
FLRST#/WUI7/GPG0/TM
FLCLK
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE#
FLFRAME#/GPG2
SCK R3084 15Ohm EC_SCK
SO R3085 15Ohm EC_SO
SI R3086 15Ohm EC_SI
SCE# R3087 15Ohm EC_SCE#
T3058 EC_GPG6
T3061 EC_GPG2
PM_THERM#
KBMX
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSO16/GPC3
KSO17/GPC5
21 PM_PWRBTN#
37 OP_SD#
EC_XIN
EC_XOUT
CK32K
CK32KE
PS/2
PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5
T3055 EC_GPF0
32 MAGNIFY#
32 MARATHON#
WLANECRST#
31 TP_CLK
31 TP_DAT
SMBus
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7
60 SMB0_CLK
60 SMB0_DAT
50,75 SMB1_CLK
50,75 SMB1_DAT
3 THRO_CPU
53 WIFI_PD#
IT8512E-L
VSTBY1
VSTBY2
VSTBY3
VSTBY4
VSTBY5
VBAT
VCC
AVCC
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
AVSS
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7
PWR_LED_UP#
CHG_LED_UP#
BATSEL_3S#
GPU_RST#
LCD_BL_PWM
FAN_PWM
EC_GPA6 T3056
EC_GPA7 T3057
T3074
E/R 2008/05/14
RXD/GPB0
TXD/GPB1
CTX/GPB2
RING#/PWRFAIL#/LPCRST#/GPB7
CHG_EN#
PRECHG
LAN_PWR_ON
PM_RSMRST# EC
CRX/GPC0
LAN_RST#
TMRI0/WUI2/GPC4
AC_IN_OC#
TMRI1/WUI3/GPC6
PWUREQ#/GPC7
BAT1_IN_OC#
RFON_SW#
RI1#/WUI0/GPD0
RI2#/WUI1/GPD1
GINT/GPD5
TACH0/GPD6
TACH1/GPD7
PWRLIMIT#
PM_SUSC#
LCD_BACKOFF#
FAN0_TACH
SD_CD_EC#
GPIO
L80HLAT/GPE0
EGAD/GPE1
EGCS#/GPE2
EGCLK/GPE3
PWRSW/GPE4
WUI5/GPE5
LPCPD#/WUI6/GPE6
L80LLAT/GPE7
VSUS_ON
SUSC_EC#
SUSB_EC#
CPU_VRON
PWR_SW#
BAT2_IN_OC#
LID_SW#
INSTANT_ON#
GPG1/ID7
PM_SUSB# 21
GPH0/ID0
GPH1/ID1
GPH2/ID2
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
PM_CLKRUN#
CMOS_PWRON
RTLAN_DSM_EN
EC_GPH3 T3073
EC_GPH4 T3068
NUM_LED#
CAP_LED#
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7
VGA_ALERT#
SUS_PWRGD
ALL_SYSTEM_PWRGD
CPU_PWRGD
NV_PWRGD_VGA
ALS_AD
VGASW_MCH_GPU#
RTLAN_DSM#
DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5
EC_CLK_EN
PM_PWROK_EC
VCTL_EC
BATSEL_2P# ISET_EC
GPU_PWRON_EC
VGASEL_MCH_GPU#
R3059 100KOhm
R3065 100KOhm
R3066 100KOhm
R3067 100KOhm
R3053 4.7KOhm
R3068 4.7KOhm
R3069 100KOhm
R3070 100KOhm
R3071 100KOhm
R3088 100KOhm
R3058 0Ohm
VRM_PWRGD 20,21,29,80,92
R3078 0Ohm
R3089 0Ohm
BATSEL_2P# 88
ISET_EC 88
R3081 100KOhm
D3020 1SS355
Q3020 2N7002
VRMPWRGD_EC
3,11,20 PM_THRMTRIP#
R3083 330Ohm
Q3021 PMBS3904
R3062 0Ohm
R3076 0Ohm
C3031 0.1UF/10V
因爲ITE8752CX 的PIN 12 爲GND
ITE8752DX 的PIN 12 爲內建電源
只需預留一電阻及一電容！
R3074 4.7KOhm TP_CLK
R3075 4.7KOhm TP_DAT
R3050 4.7KOhm SMB0_CLK
R3051 4.7KOhm SMB0_DAT
R3077 4.7KOhm SMB1_CLK
R3052 4.7KOhm SMB1_DAT
R3072 10MOhm
R3073 0Ohm
X3002 32.768Khz
C3026 15PF/50V
C3027 15PF/50V
1MB SPI ROM
U3013 SST25VF080B
R3060 10KOhm
R3061 10KOhm
C3020 1UF/10V
C3033 10UF/6.3V
C3034 0.1UF/10V
E/R V1.1 2008/5/28 add C3033, C3034
U3017 NC7SZ08P5X
GPU_PWRON 57,91
C3030 0.1UF/10V
U3015 NC7SZ08P5X
C3029 0.1UF/10V
SUS_PWRGD
PM_PWROK_EC
11,21 PM_PWROK
R3079 0Ohm
IT3015
目的：解單插AC時，
拔AC再插，CMOS錯誤且
自動開機
主要避免分壓所造成的影響
U3018 NC7SZ08P5X
C3032 0.1UF/10V
WLANEC_RST# 53
ASUSTeK COMPUTER INC
Title : IT8752E
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
Sheet 30 of 97

TOUCHPAD FPC

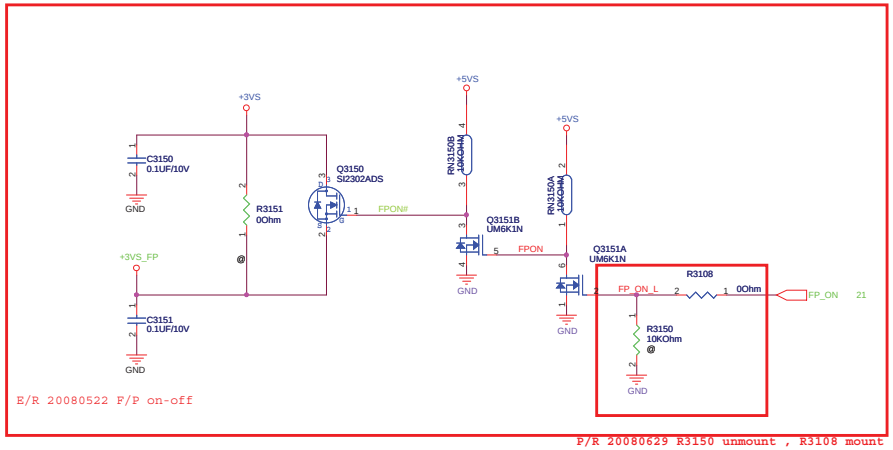


USB_PN4/USB_PP4 is optional for Fingerprint and WiMax

RN5301 必須靠近 RN3101

TOUCH PAD

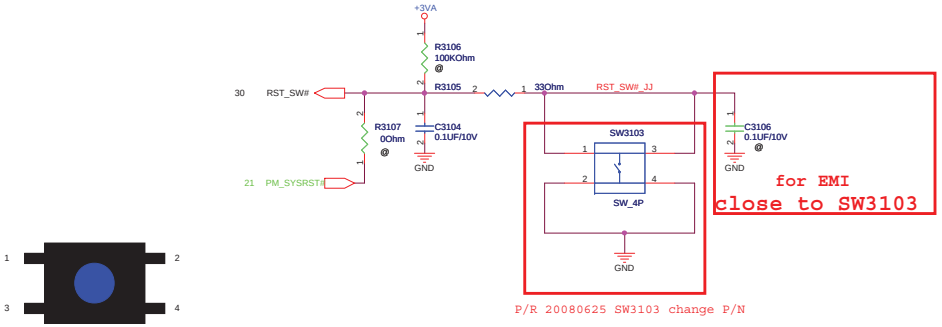
製作FFC 時要提醒ME標示TP/MB 文字面以利組裝



E/R 20080522 F/P on-off

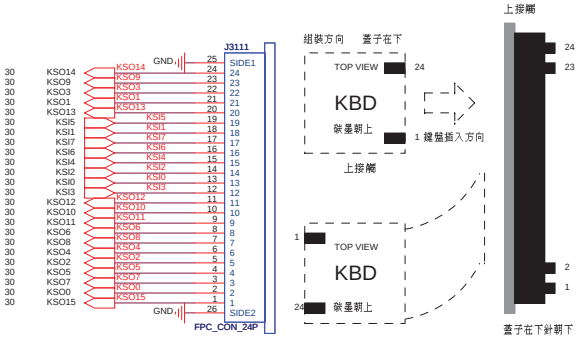
P/R 20080629 R3150 unmount , R3108 mount

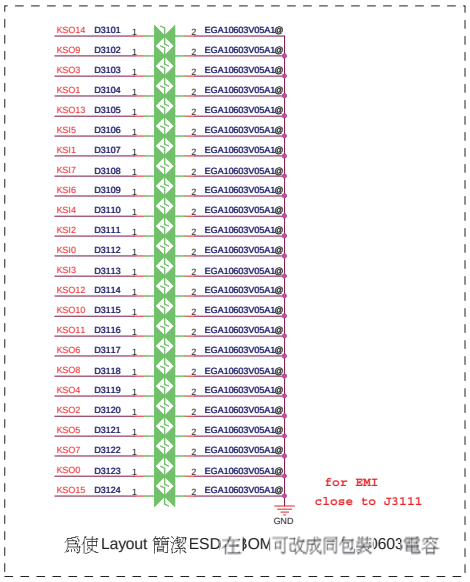
RESET BUTTON



P/R 20080625 SW3103 change P/N

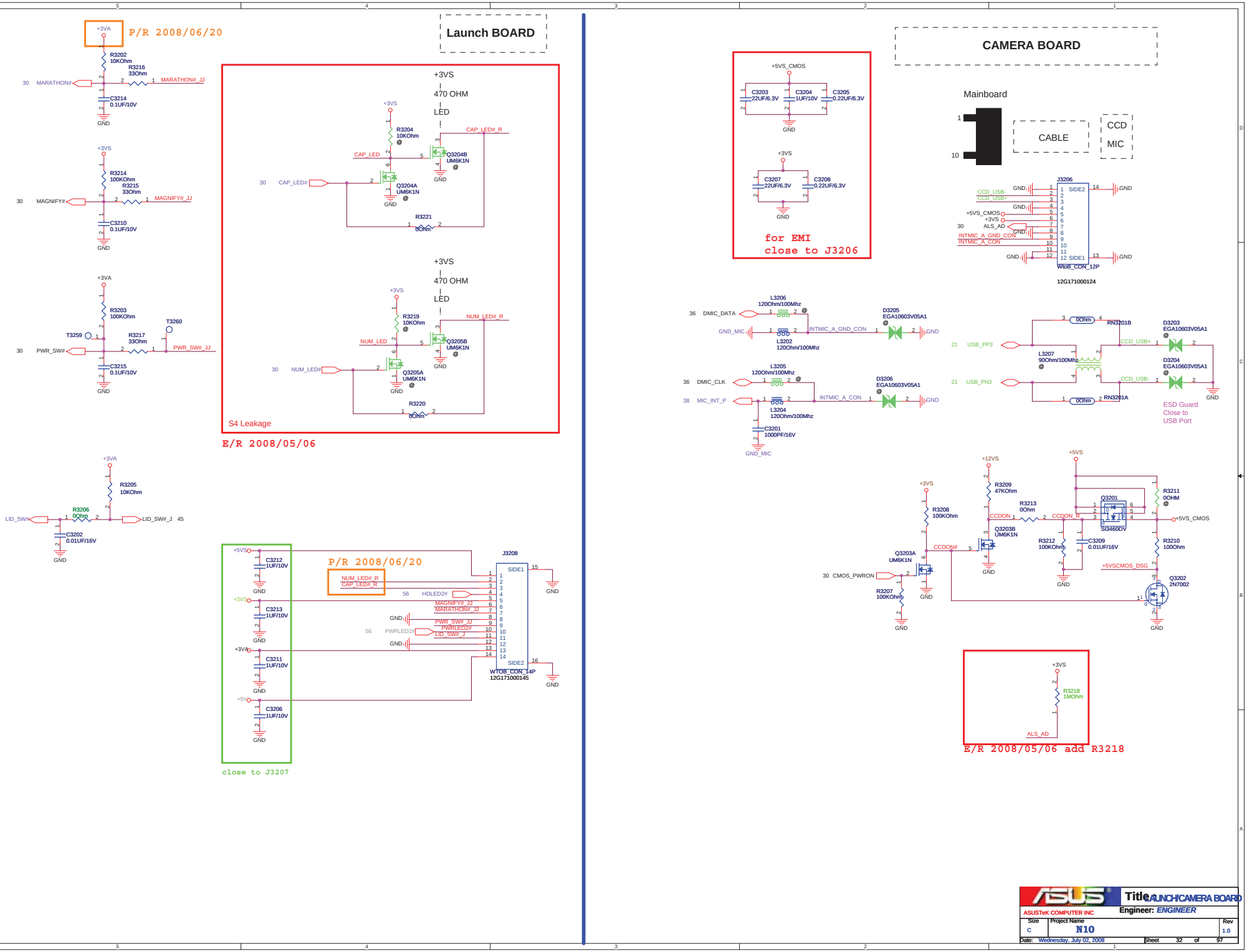
INTERNAL KEYBOARD





爲使Layout 簡潔ESD在POM可改成同包裝0603電容

ASUSTeK COMPUTER INC	Title : KEYBOARD	
	Engineer: ENGINEER	
Size: C	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 31 of 97	


Launch BOARD
P/R 2008/06/20
+3VA
R3202 10KOhm
R3216 33Ohm
30 MARATHON#
MARATHON#_JJ
C3214 0.1UF/10V
GND
+3VS
R3214 100KOhm
R3215 33Ohm
30 MAGNIFY#
MAGNIFY#_JJ
C3210 0.1UF/10V
R3203 100KOhm
T3259
T3260
R3217 33Ohm
30 PWR_SW#
PWR_SW#_JJ
C3215 0.1UF/10V
+3VS
470 OHM
LED
R3204 10KOhm @
CAP_LED
CAP_LED#_R
Q3204B UM6K1N @
30 CAP_LED#
Q3204A UM6K1N @
R3221 0Ohm
R3219 10KOhm @
NUM_LED
NUM_LED#_R
Q3205B UM6K1N @
30 NUM_LED#
Q3205A UM6K1N @
R3220 0Ohm
S4 Leakage
E/R 2008/05/06
R3205 10KOhm
R3206 0Ohm
LID_SW#
LID_SW#_J 45
C3202 0.01UF/16V
+5VS
C3212 1UF/10V
C3213 1UF/10V
C3211 1UF/10V
C3206 1UF/10V
P/R 2008/06/20
NUM_LED#_R
CAP_LED#_R
56 HDLED2#
MAGNIFY#_JJ
MARATHON#_JJ
PWR_SW#_JJ
56 PWRLED2#
LID_SW#_J
J3208
SIDE1
SIDE2
WTOB_CON_14P
12G171000145
close to J3207
CAMERA BOARD
+5VS_CMOS
C3203 22UF/6.3V
C3204 1UF/10V
C3205 0.22UF/6.3V
C3207 22UF/6.3V
C3208 0.22UF/6.3V
for EMI
close to J3206
Mainboard
CABLE
CCD
MIC
J3206
CCD_USB-
CCD_USB+
+5VS_CMOS
+3VS
30 ALS_AD
INTMIC_A_GND_CON
INTMIC_A_CON
WtoB_CON_12P
12G171000124
36 DMIC_DATA
GND_MIC
L3206 120Ohm/100Mhz
D3205 EGA10603V05A1
INTMIC_A_GND_CON
L3202 120Ohm/100Mhz
36 DMIC_CLK
38 MIC_INT_P
L3205 120Ohm/100Mhz
D3206 EGA10603V05A1
INTMIC_A_CON
L3204 120Ohm/100Mhz
C3201 1000PF/16V
21 USB_PP3
21 USB_PN3
0Ohm
RN3201B
RN3201A
L3207 90Ohm/100Mhz
D3203 EGA10603V05A1
D3204 EGA10603V05A1
CCD_USB+
CCD_USB-
ESD Guard Close to USB Port
+12VS
+5VS
R3209 47KOhm
R3213 0Ohm
CCDON
CCDON_R
Q3201 SI3460DV
R3211 0OHM @
+5VS_CMOS
R3208 100KOhm
Q3203B UM6K1N
Q3203A UM6K1N
CCDON#
30 CMOS_PWRON
R3212 100KOhm
C3209 0.01UF/16V
R3210 100Ohm
+5VSCMOS_DSG
R3207 100KOhm
Q3202 2N7002
R3218 1MOhm
ALS_AD
E/R 2008/05/06 add R3218
Title LAUNCH CAMERA BOARD
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size C
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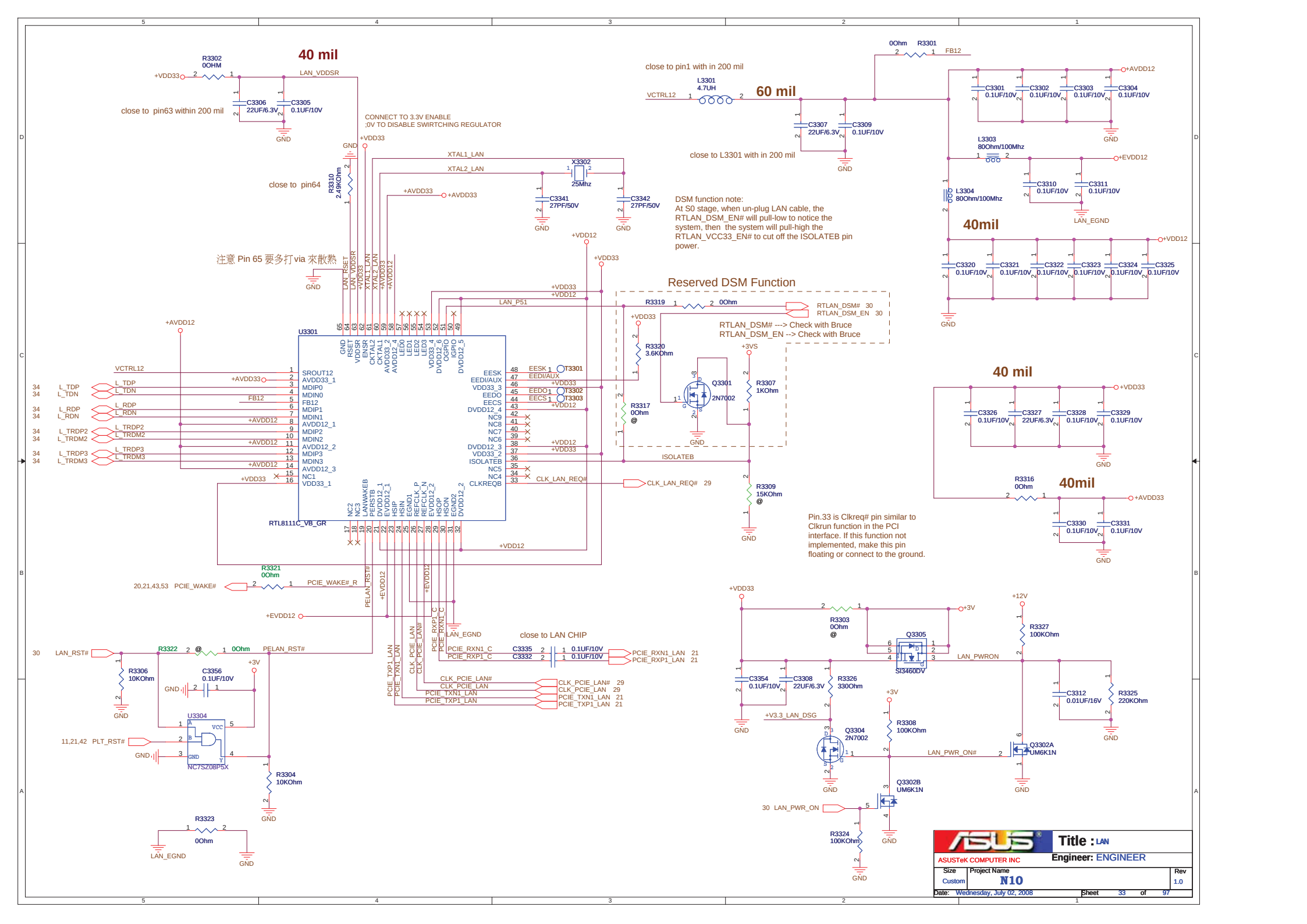
40 mil
R3302 0OHM
+VDD33
LAN_VDDSR
close to pin63 within 200 mil
C3306 22UF/6.3V
C3305 0.1UF/10V
GND
CONNECT TO 3.3V ENABLE
;0V TO DISABLE SWIRTCHING REGULATOR
close to pin64
R3310 2.49KOhm
XTAL1_LAN
XTAL2_LAN
X3302
25Mhz
C3341 27PF/50V
C3342 27PF/50V
+AVDD33
+AVDD12
注意 Pin 65 要多打via 來散熱
LAN_RSET
+VDD12
LAN_P51
U3301
RTL8111C_VB_GR
SROUT12
AVDD33_1
MDIP0
MDIN0
FB12
MDIP1
MDIN1
AVDD12_1
MDIP2
MDIN2
AVDD12_2
MDIP3
MDIN3
AVDD12_3
NC1
VDD33_1
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
DVDD12_4
NC9
NC8
NC7
NC6
DVDD12_3
VDD33_2
ISOLATEB
NC5
NC4
CLKREQB
L_TDP
L_TDN
L_RDP
L_RDN
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
VCTRL12
FB12
T3301
T3302
T3303
CLK_LAN_REQ#
CLK_LAN_REQ# 29
Reserved DSM Function
R3319 0Ohm
RTLAN_DSM# 30
RTLAN_DSM_EN 30
RTLAN_DSM# ---> Check with Bruce
RTLAN_DSM_EN --> Check with Bruce
R3320 3.6KOhm
R3317 0Ohm @
Q3301 2N7002
R3307 1KOhm
+3VS
R3309 15KOhm @
ISOLATEB
Pin.33 is Clkreq# pin similar to Clkrun function in the PCI interface. If this function not implemented, make this pin floating or connect to the ground.
R3321 0Ohm
20,21,43,53 PCIE_WAKE#
PCIE_WAKE#_R
PELAN_RST#
+EVDD12
LAN_EGND
close to LAN CHIP
PCIE_RXN1_C
PCIE_RXP1_C
C3335
C3332
0.1UF/10V
PCIE_RXN1_LAN 21
PCIE_RXP1_LAN 21
CLK_PCIE_LAN#
CLK_PCIE_LAN
PCIE_TXN1_LAN
PCIE_TXP1_LAN
CLK_PCIE_LAN# 29
CLK_PCIE_LAN 29
PCIE_TXN1_LAN 21
PCIE_TXP1_LAN 21
30 LAN_RST#
R3322 @ 0Ohm
PELAN_RST#
R3306 10KOhm
C3356 0.1UF/10V
+3V
U3304
NC7SZ08P5X
11,21,42 PLT_RST#
R3304 10KOhm
R3323 0Ohm
close to pin1 with in 200 mil
L3301 4.7UH
60 mil
close to L3301 with in 200 mil
C3307 22UF/6.3V
C3309 0.1UF/10V
0Ohm R3301
FB12
C3301 0.1UF/10V
C3302 0.1UF/10V
C3303 0.1UF/10V
C3304 0.1UF/10V
+AVDD12
L3303 80Ohm/100Mhz
+EVDD12
C3310 0.1UF/10V
C3311 0.1UF/10V
L3304 80Ohm/100Mhz
LAN_EGND
40mil
C3320 0.1UF/10V
C3321 0.1UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
40 mil
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 0.1UF/10V
C3329 0.1UF/10V
R3316 0Ohm
40mil
C3330 0.1UF/10V
C3331 0.1UF/10V
R3303 0Ohm @
Q3305 SI3460DV
+12V
R3327 100KOhm
LAN_PWRON
C3354 0.1UF/10V
C3308 22UF/6.3V
R3326 330Ohm
+V3.3_LAN_DSG
C3312 0.01UF/16V
R3325 220KOhm
Q3304 2N7002
R3308 100KOhm
LAN_PWR_ON#
Q3302A UM6K1N
Q3302B UM6K1N
30 LAN_PWR_ON
R3324 100KOhm
ASUSTeK COMPUTER INC
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Engineer: ENGINEER
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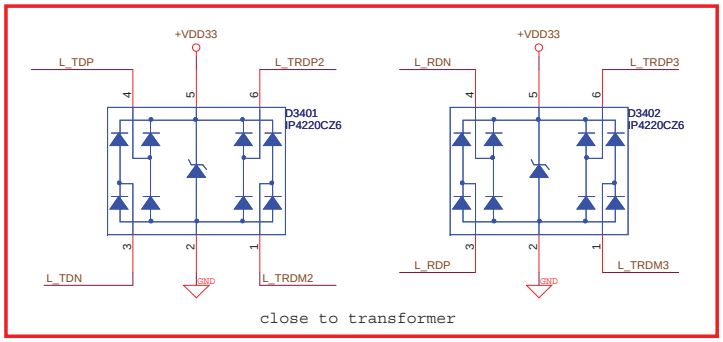
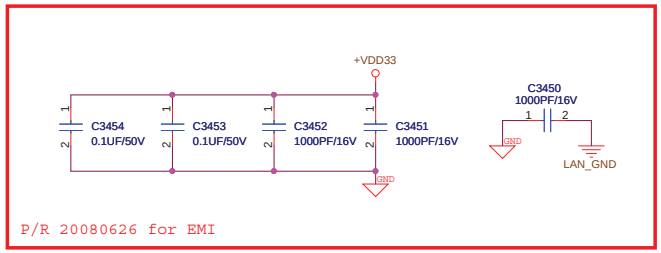
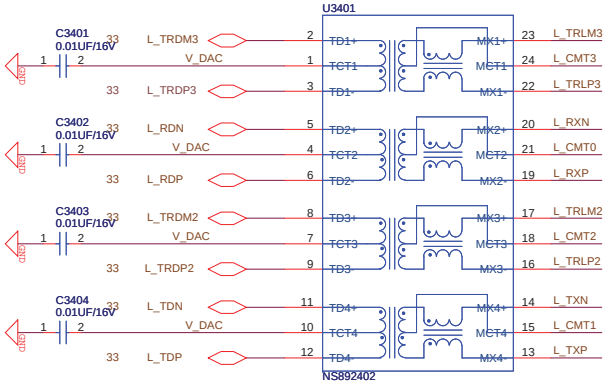
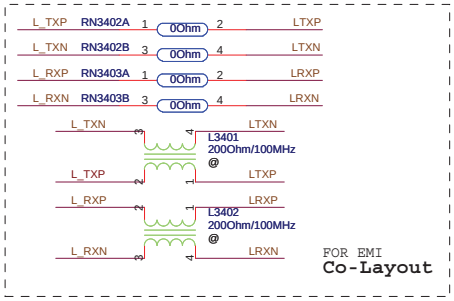
P/R 20080630 SWAP D3401(pin1,pin6) and D3402(pin3,pin4)

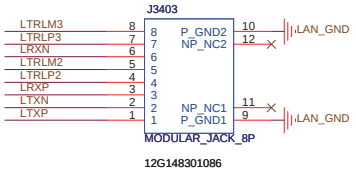


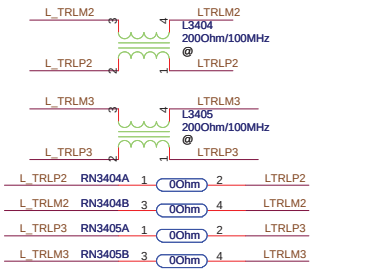


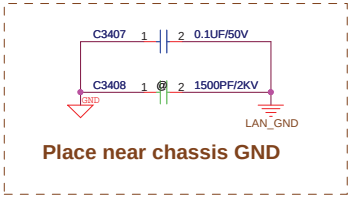


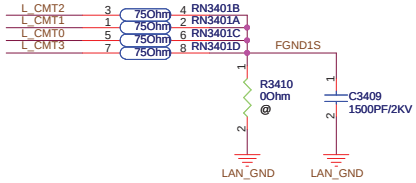
Transformer close to J401

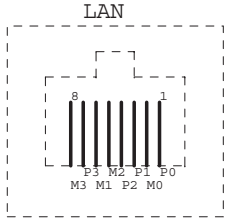












ASUSTeK COMPUTER INC	Title : LAN	
	Engineer: ENGINEER	
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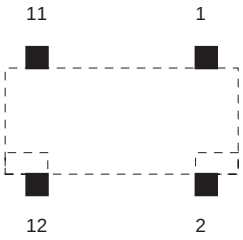
MDC



ASUSTeK COMPUTER INC	Title : MDC Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
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Digital

SPDIF_GPU is reserved for ALC663

依PM 指示 ALC662/ALC663 變 Layout
猫殺先上 ALC662 及 Analog MIC

U3601 ALC662/663

AUD_SHDN# For ALC663 power-on sequence

R3601 is 34KOHM(10G213340213010) for MAX8863
R3601 is 0 OHM(10G213340213010) for GMT923

For EMI

ASUSTeK COMPUTER INC	Title : AUDIO CODEC		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
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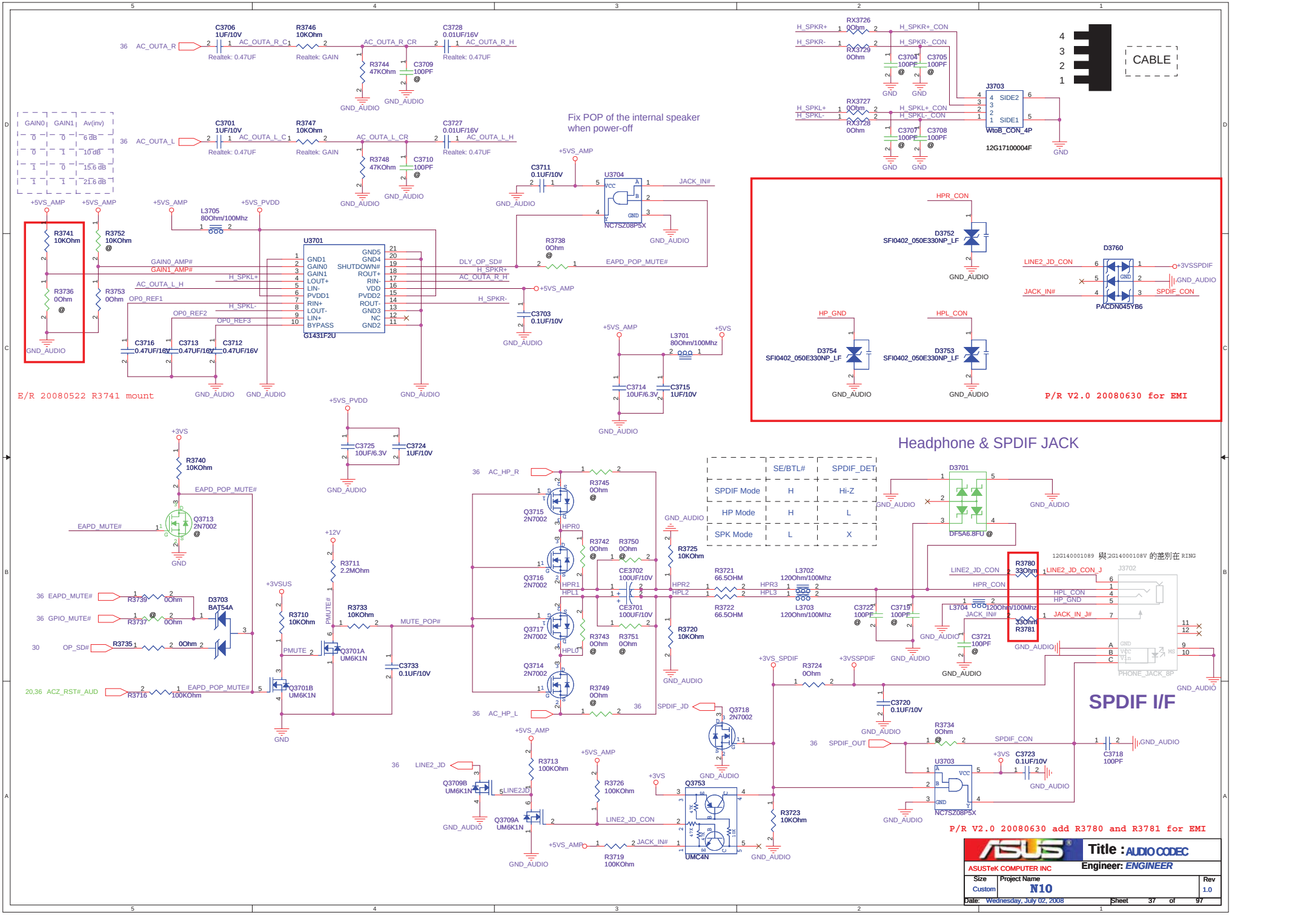
C3706 1UF/10V
R3746 10KOhm
C3728 0.01UF/16V
AC_OUTA_R
AC_OUTA_R_C
AC_OUTA_R_CR
AC_OUTA_R_H
Realtek: 0.47UF
Realtek: GAIN
R3744 47KOhm
C3709 100PF
GND_AUDIO
C3701 1UF/10V
R3747 10KOhm
C3727 0.01UF/16V
AC_OUTA_L
AC_OUTA_L_C
AC_OUTA_L_CR
AC_OUTA_L_H
R3748 47KOhm
C3710 100PF
GAIN0 GAIN1 Av(inv)
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
Fix POP of the internal speaker when power-off
H_SPKR+
H_SPKR-
RX3726 0Ohm
RX3729 0Ohm
H_SPKR+_CON
H_SPKR-_CON
C3704 100PF
C3705 100PF
H_SPKL+
H_SPKL-
RX3727 0Ohm
RX3728 0Ohm
H_SPKL+_CON
H_SPKL-_CON
C3707 100PF
C3708 100PF
J3703
SIDE2
SIDE1
WtoB_CON_4P
12G17100004F
CABLE
+5VS_AMP
+5VS_PVDD
L3705 80Ohm/100Mhz
R3741 10KOhm
R3752 10KOhm @
R3736 0Ohm @
R3753 0Ohm
U3701
G1431F2U
GAIN0_AMP#
GAIN1_AMP#
H_SPKL+
H_SPKL-
AC_OUTA_L_H
OP0_REF1
OP0_REF2
OP0_REF3
C3716 0.47UF/16V
C3713 0.47UF/16V
C3712 0.47UF/16V
C3711 0.1UF/10V
U3704
NC7SZ08P5X
JACK_IN#
R3738 0Ohm @
DLY_OP_SD#
EAPD_POP_MUTE#
H_SPKR+
AC_OUTA_R_H
H_SPKR-
C3703 0.1UF/10V
L3701 80Ohm/100Mhz
+5VS
C3714 10UF/6.3V
C3715 1UF/10V
E/R 20080522 R3741 mount
HPR_CON
D3752 SFI0402_050E330NP_LF
D3760
LINE2_JD_CON
JACK_IN#
PACDN045YB6
+3VSSPDIF
SPDIF_CON
HP_GND
HPL_CON
D3754 SFI0402_050E330NP_LF
D3753 SFI0402_050E330NP_LF
P/R V2.0 20080630 for EMI
Headphone & SPDIF JACK
+3VS
R3740 10KOhm
EAPD_POP_MUTE#
EAPD_MUTE#
Q3713 2N7002
GND
+5VS_PVDD
C3725 10UF/6.3V
C3724 1UF/10V
+12V
R3711 2.2MOhm
+3VSUS
R3710 10KOhm
PMUTE#
R3733 10KOhm
MUTE_POP#
C3733 0.1UF/10V
Q3701A UM6K1N
Q3701B UM6K1N
D3703 BAT54A
R3739 0Ohm
R3737 0Ohm
R3735 0Ohm
R3716 100KOhm
GPIO_MUTE#
OP_SD#
ACZ_RST#_AUD
AC_HP_R
AC_HP_L
R3745 0Ohm @
Q3715 2N7002
Q3716 2N7002
Q3717 2N7002
Q3714 2N7002
HPR0
HPR1
HPL1
HPL0
R3742 0Ohm @
R3750 0Ohm @
R3743 0Ohm @
R3751 0Ohm @
R3749 0Ohm @
CE3702 100UF/10V
CE3701 100UF/10V
R3725 10KOhm
R3720 10KOhm
HPR2
HPL2
HPR3
HPL3
R3721 66.5OHM
R3722 66.5OHM
L3702 120Ohm/100Mhz
L3703 120Ohm/100Mhz
SE/BTL#
SPDIF_DET
SPDIF Mode H Hi-Z
HP Mode H L
SPK Mode L X
D3701 DF5A6.8FU @
R3780 33Ohm
R3781 33Ohm
C3722 100PF @
C3715 100PF @
L3704 120Ohm/100Mhz
C3721 100PF @
12G14001089 與2G14000108V 的差別在 RING
J3702
PHONE_JACK_8P
SPDIF I/F
+3VS_SPDIF
+3VSSPDIF
R3724 0Ohm
C3720 0.1UF/10V
SPDIF_JD
Q3718 2N7002
SPDIF_OUT
R3734 0Ohm @
SPDIF_CON
C3718 100PF
U3703
NC7SZ08P5X
C3723 0.1UF/10V
LINE2_JD
Q3709B UM6K1N
Q3709A UM6K1N
R3713 100KOhm
R3726 100KOhm
LINE2_JD_CON
JACK_IN#
R3719 100KOhm
Q3753
UMC4N
R3723 10KOhm
P/R V2.0 20080630 add R3780 and R3781 for EMI
ASUSTeK COMPUTER INC
Title : AUDIO CODEC
Engineer: ENGINEER
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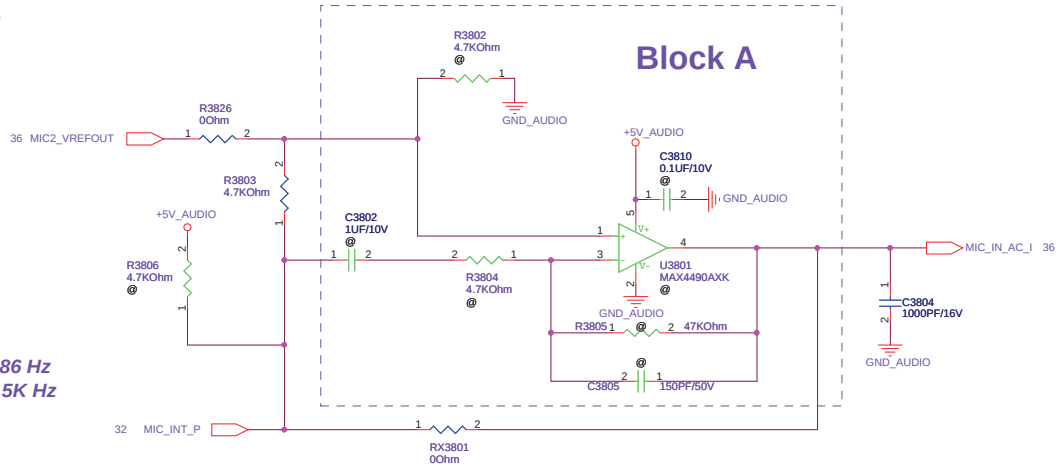
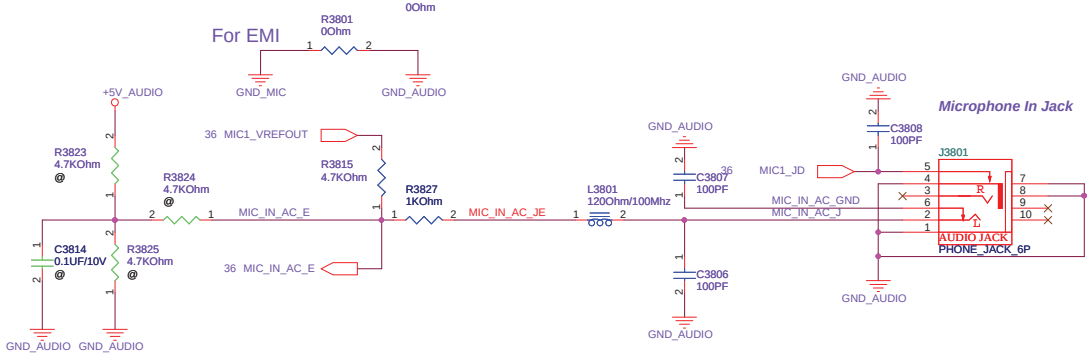
Internal MIC Pre-Amplifier



(Microphone)FL = 33.86 Hz
(Microphone)FH = 22.5K Hz

External MIC



ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

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Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

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xD Pin-assignment

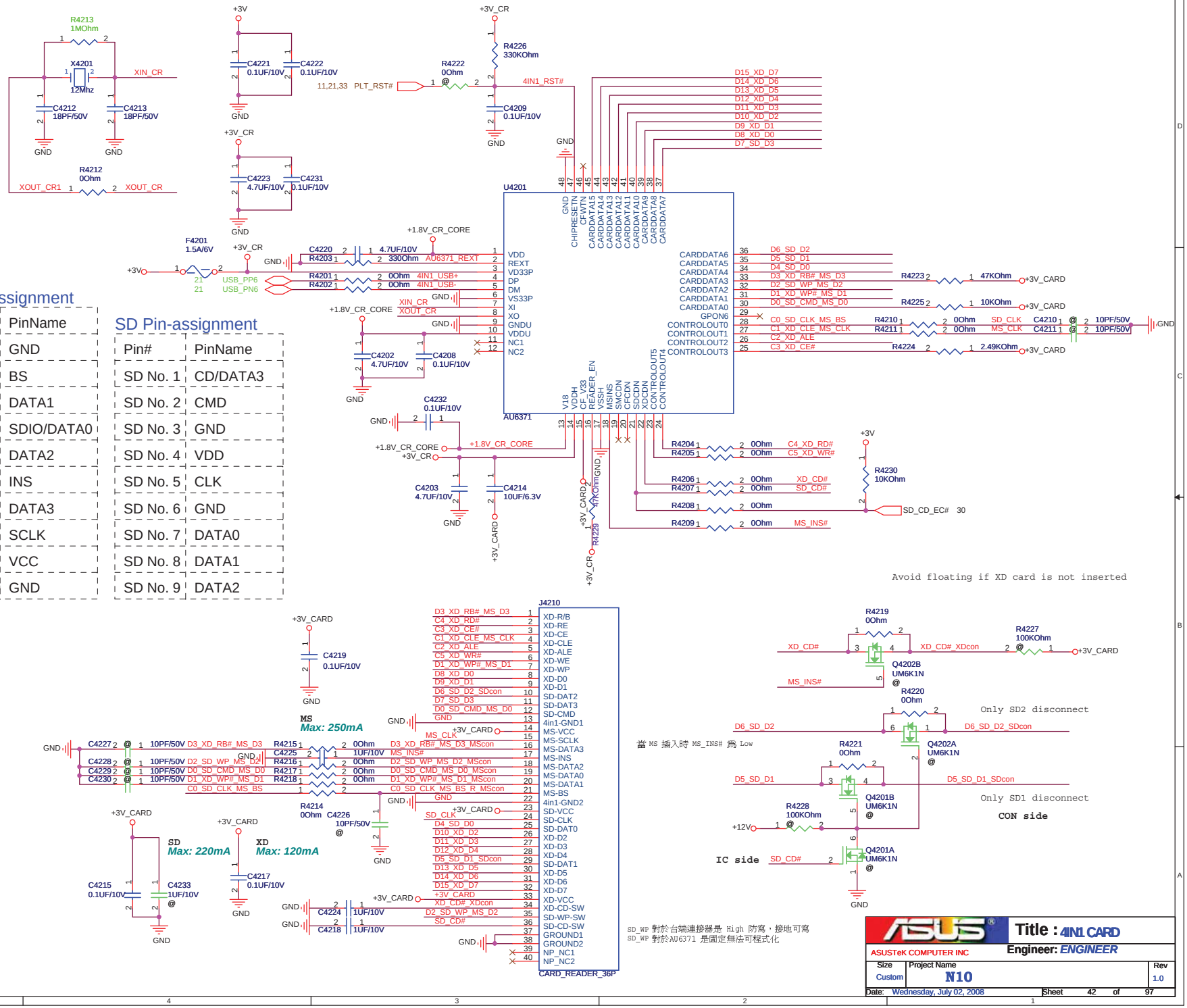
Pin#	PinName
Xd No. 0	CD
Xd No. 1	GND
Xd No. 2	R/-B
Xd No. 3	-RE
Xd No. 4	-CE
Xd No. 5	CLE
Xd No. 6	ALE
Xd No. 7	-WE
Xd No. 8	-WP
Xd No. 9	GND
Xd No.10	D0
Xd No.11	D1
Xd No.12	D2
Xd No.13	D3
Xd No.14	D4
Xd No.15	D5
Xd No.16	D6
Xd No.17	D7
Xd No.18	VCC

MS Pin-assignment

Pin#	PinName
MS No. 1	GND
MS No. 2	BS
MS No. 3	DATA1
MS No. 4	SDIO/DATA0
MS No. 5	DATA2
MS No. 6	INS
MS No. 7	DATA3
MS No. 8	SCLK
MS No. 9	VCC
MS No.10	GND

SD Pin-assignment

Pin#	PinName
SD No. 1	CD/DATA3
SD No. 2	CMD
SD No. 3	GND
SD No. 4	VDD
SD No. 5	CLK
SD No. 6	GND
SD No. 7	DATA0
SD No. 8	DATA1
SD No. 9	DATA2



ASUSTeK COMPUTER INC

Title : 4IN1 CARD

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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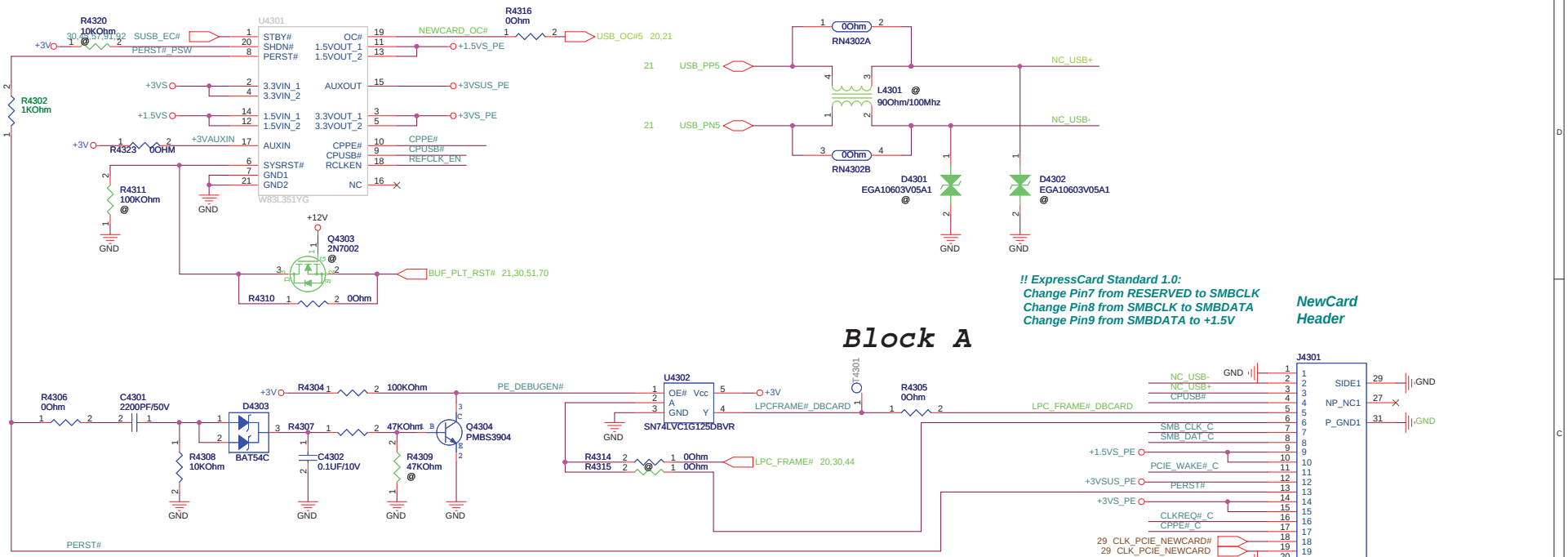

在編 BOM時 請將鑑殼 12G21C20001X 加在 50 階

ASUSTeK COMPUTER INC	Title : NEWCARD	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
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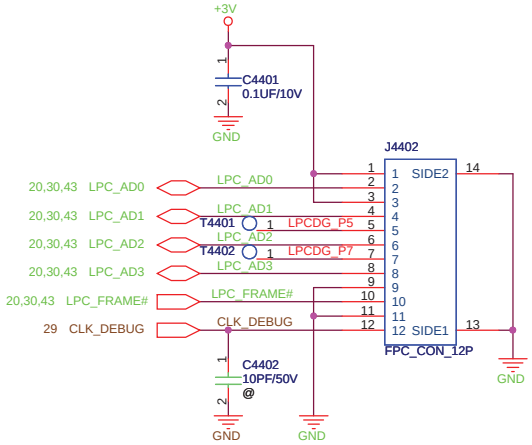
LPC DEBUG PORT



ASUSTeK COMPUTER INC	Title : LPC DEBUG	
	Engineer: ENGINEER	
Size: B	Project Name: N10	Rev: 1.0
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LCD LVDS Interface

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Backlight Control
LCD Power

E/R V1.1 2008/5/28 add C4514, C4515

47 EDID_CLK — LX4502 120Ohm/100Mhz — EDIDCLK_J — C4520 1000PF/16V @ — GND
47 EDID_DAT — LX4504 120Ohm/100Mhz — EDIDDAT_J — C4521 1000PF/16V @ — GND
+3VS_EDID — C4507 0.1UF/10V — GND
+3VS — L4503 80Ohm/100Mhz — +3VS_EDID

+3VS — C4512 0.1UF/10V — C4514 10UF/6.3V — C4515 10UF/6.3V — GND

+12VS — R4503 100KOhm — Q4501 SI3460DV — +3VSLCD — L4502 80Ohm/100Mhz — +3VS_LCD

+3VSUS — R4506 100KOhm — Q4503B UM6K1N — C4503 0.01UF/16V — R4507 220KOhm — LCDVDD_EN

47 L_VDDEN — Q4503A UM6K1N — R4505 100KOhm — GND

C4504 10UF/6.3V — C4505 1UF/10V — C4506 0.1UF/10V — C4510 0.01UF/16V — C4511 0.01UF/16V — GND

R4504 100Ohm — +3VSLCD_DIS — Q4502 2N7002 — LCDVDD_DIS

C4551 0.1UF/10V @ — GND
close to J4502 for EMI

+LED_VCC

J4502 — WTOB_CON_30P
GND1 NP_NC1 NP_NC2 GND2

CPT CLAA102NA0ACW LCD 正視圖

SWAP

47 LVDS_L0N — LVDS_L0N
47 LVDS_L0P — LVDS_L0P
47 LVDS_L1N — LVDS_L1N
47 LVDS_L1P — LVDS_L1P
47 LVDS_L2N — LVDS_L2N
47 LVDS_L2P — LVDS_L2P
47 LVDS_LCLKN — LVDS_LCLKN
47 LVDS_LCLKP — LVDS_LCLKP
EDIDDAT_J
EDIDCLK_J
LED_BKLTCTL
+3VS_EDID
+3VS_LCD

30 LCD_BL_PWM — L4504 120Ohm/100Mhz — C4518 1000PF/16V — GND
47 L_BKLTCTL_V — L4501 120Ohm/100Mhz @ — GND

C4550 0.1UF/10V @ — GND
close to J4502 for EMI

CABLE

Backlight Interface

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

+3VS_LCD — R4511 10KOhm — D4505 BAT54A
+5VS — R4515 100KOhm — Q4515A UM6K1N — BL_EN
+12VS — R4508 100KOhm — Q4515B UM6K1N — BL_EN#
+5VS — Q4505 SI3460DV — +LEDVCC — R4509 220KOhm — C4509 0.01UF/16V — GND

32 LID_SW#_J
30 LCD_BACKOFF#
47 L_BKLTEN_V
30,43,57,91,92 SUSB_EC#

D4504 BAT54A
R4514 100KOhm @ — R4516 100KOhm — GND

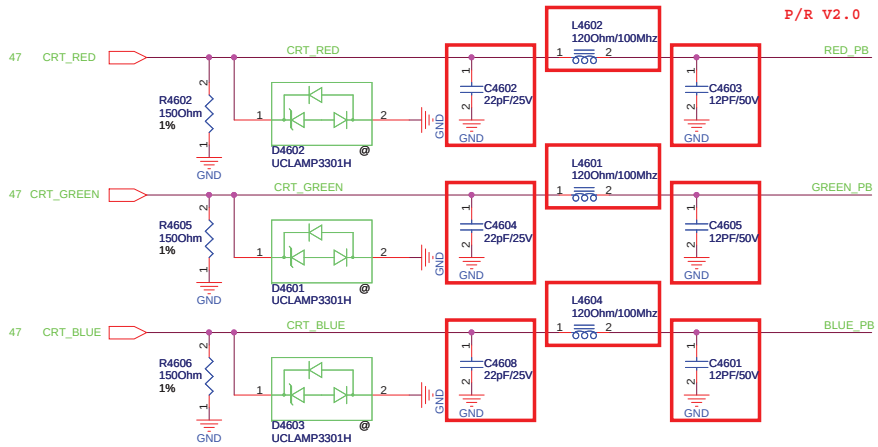
L4505 80Ohm/100Mhz — +LED_VCC
C4508 0.1UF/10V — C4501 1UF/10V — C4513 10UF/6.3V — R4510 100Ohm — GND

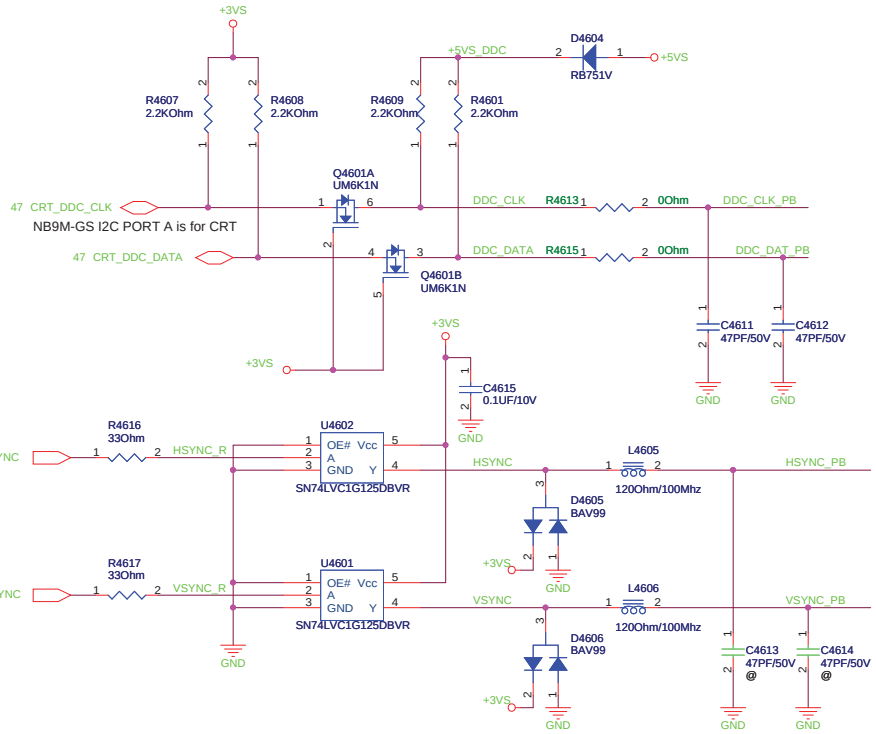
+LED_VCC_DSG — Q4504 2N7002 — BL_EN#

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 45 of 97	

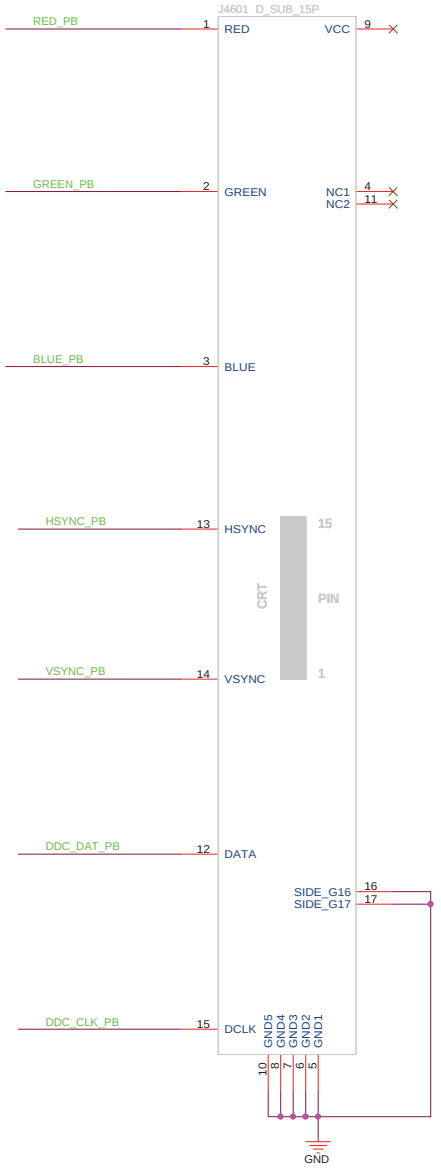
P/R V2.0 L4601,L4602,L4604 change to P/N:09G023681002 (0.068UH/300mA 0603 5%)

P/R V2.0 C4601,C4602,C4603,C4604,C4605,C4608 change to P/N:11G232010004150 (10pF 0402)





Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.



ASUSTek COMPUTER INC		Title : CRT	
		Engineer: ENGINEER	
Size: Custom	Project Name: N10		Rev: 1.0
Date: Monday, July 07, 2008		Sheet 46 of 97	

LCD/BL Enable Switch

E/R V1.1 2008/5/28 add R4753,R4754

MCH

GPU

LVDS Switch

MCH

GPU

E/R V1.1 2008/5/28 add C4715

E/R V1.1 2008/5/28 add C4713, C4714

CRT RGB Switch

DAC_SEL
L: Dx=S1x (MCH)
H: Dx=S2x (GPU)

EDID Switch

MCH

GPU

CRT DDC Switch

MCH

GPU

BL PWM Switch

MCH

GPU

VGASW_MCH_GPU#=High INTEL OFF(2,3)

VGASW_MCH_GPU#=Low ON(1,3) NB9M-GS

VGA SW 在板下

VGA SW 透視圖

N10
TOP

ON(1,3)

OFF(2,3)

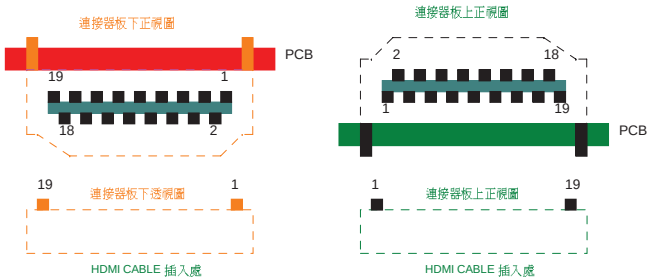
CRT SYNC Switch

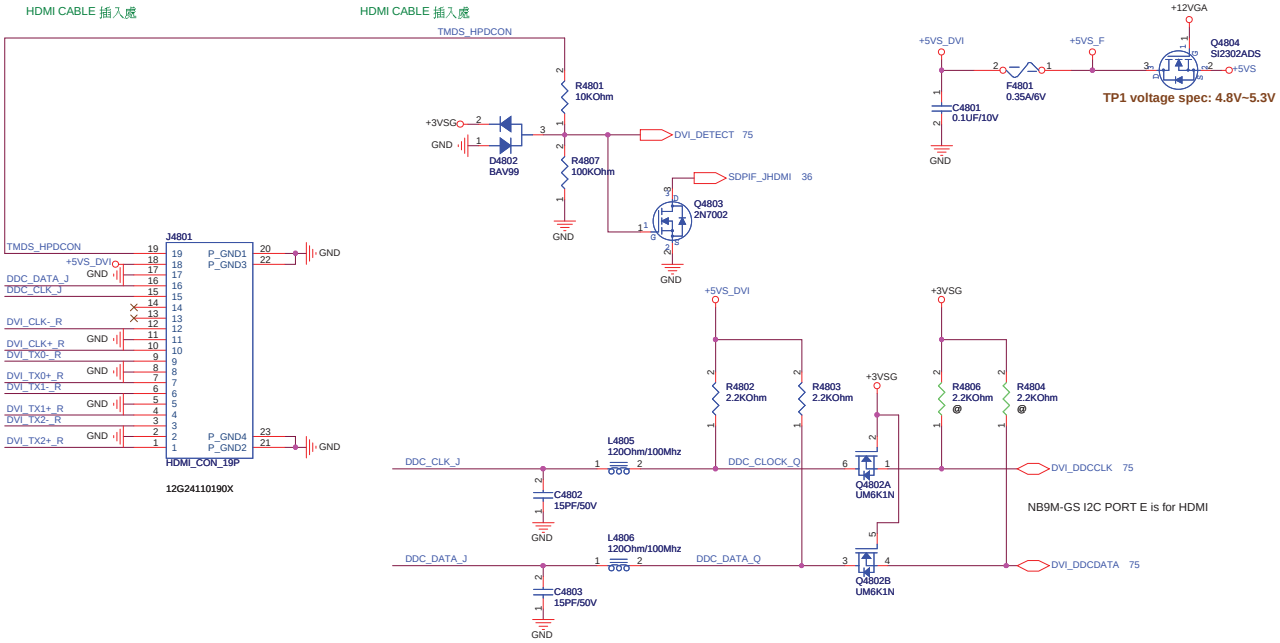
MCH

GPU

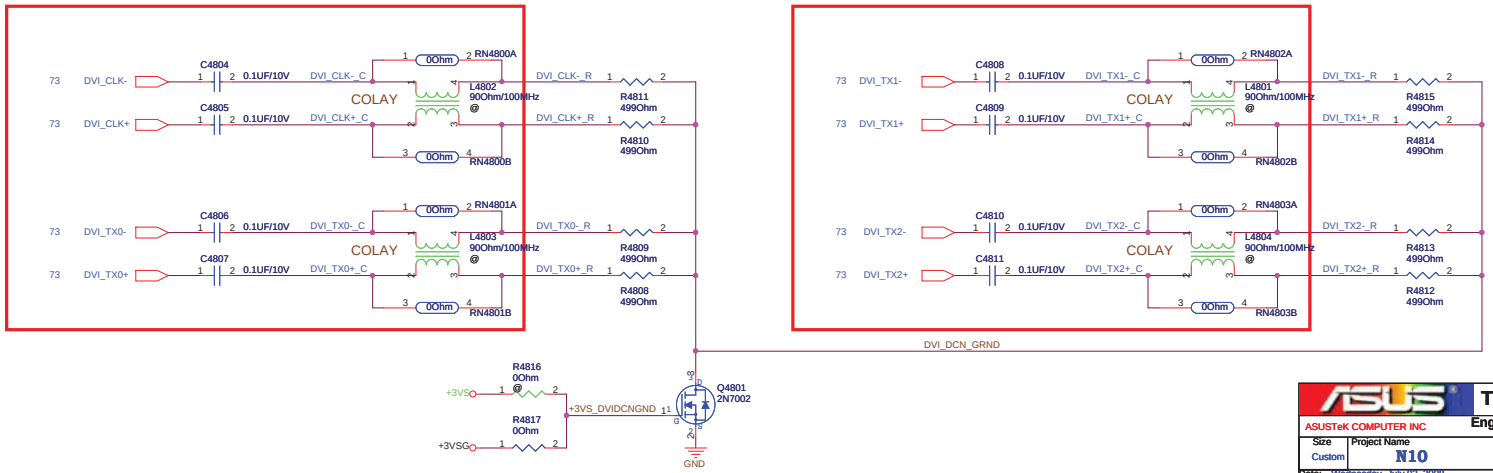
P/R V2.0 2008/7/01 change +3VS to +3VA, umount R4718

ASUSTeK COMPUTER INC. NB1	Title : Hybrid-Switch	
	Engineer: C.W._Lin	
Size: Custom	Project Name: H17	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 47 of 97	





E/R V1.1 20080526 for EMI



ASUSTeK COMPUTER INC	Title : HDMI	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 48 of 97	

Title : EMPTY

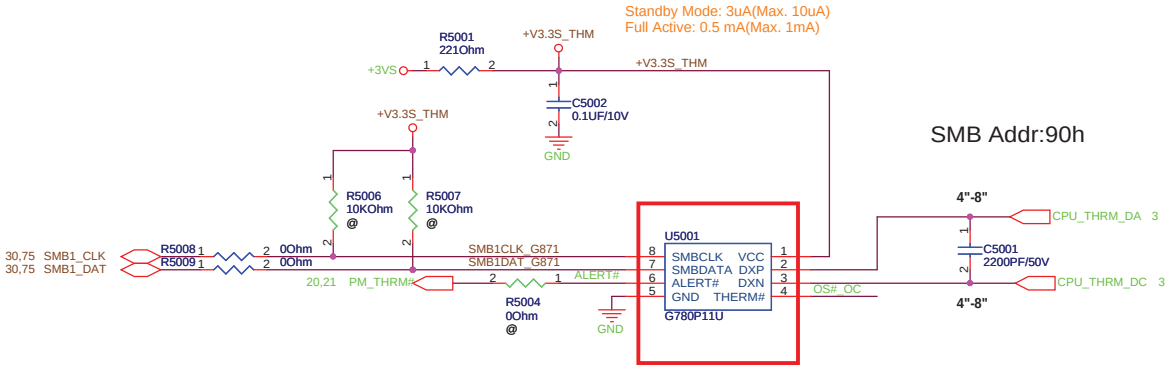
ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 49 of 97

Thermal Sensor



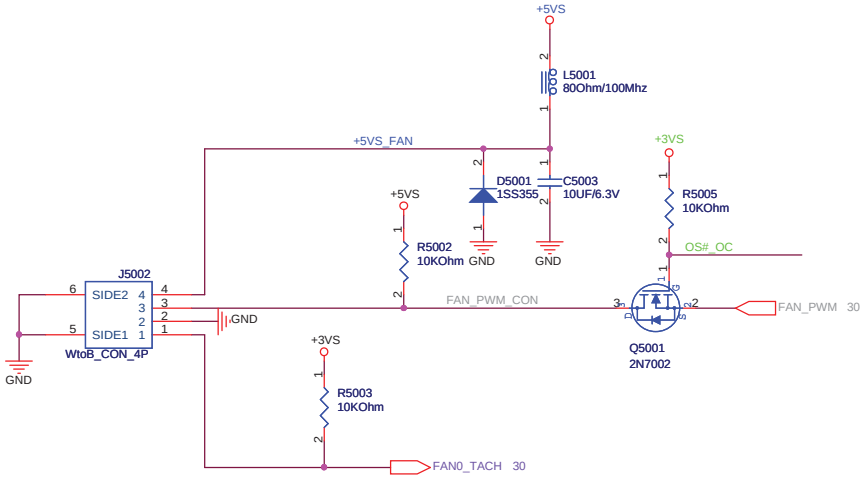
U5001 於3OM變更P/N:06G023064020 E/R 2008/05/19

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

FAN connector



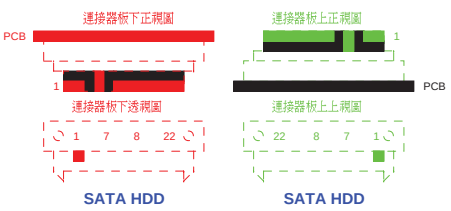
TOP

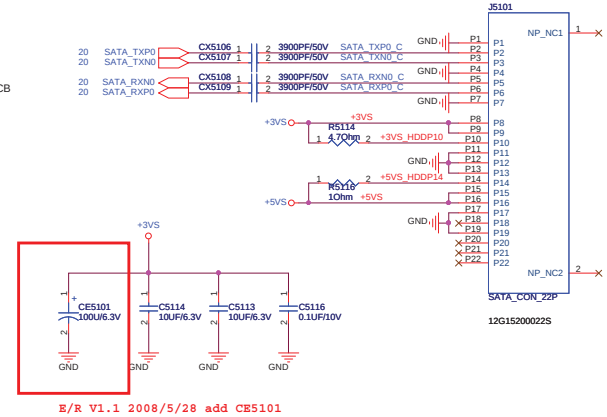
FAN

ASUSTeK COMPUTER INC	Title : THER-SENSOR/FAN	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 50 of 97	

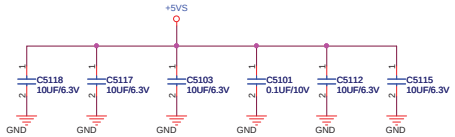
SATA HDD

J5101 變更P/N:12G15200022S (DIP)



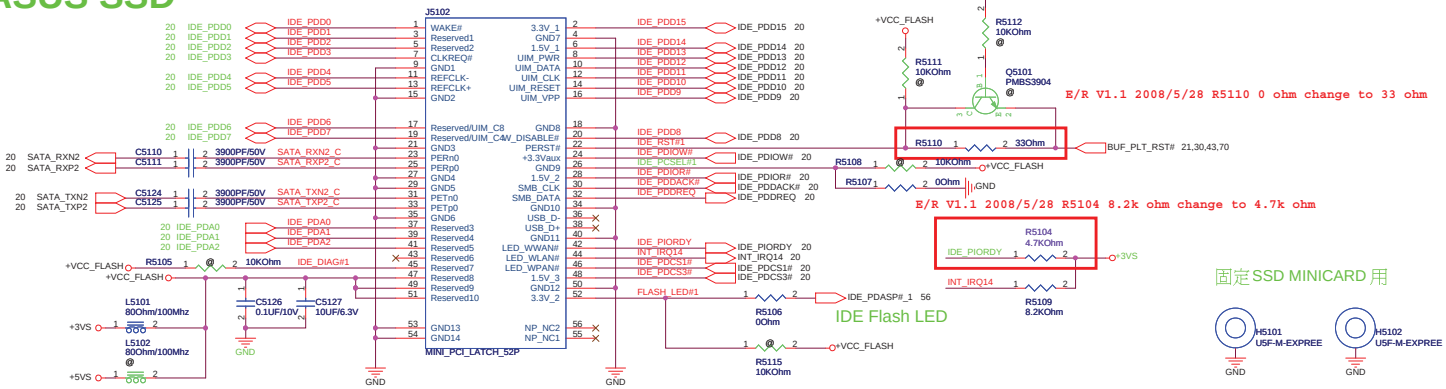


E/R V1.1 2008/5/28 add CE5101



E/R H5103,H5104 Delete

ASUS SSD



E/R V1.1 2008/5/28 R5110 0 ohm change to 33 ohm

E/R V1.1 2008/5/28 R5104 8.2k ohm change to 4.7k ohm

IDE Flash LED

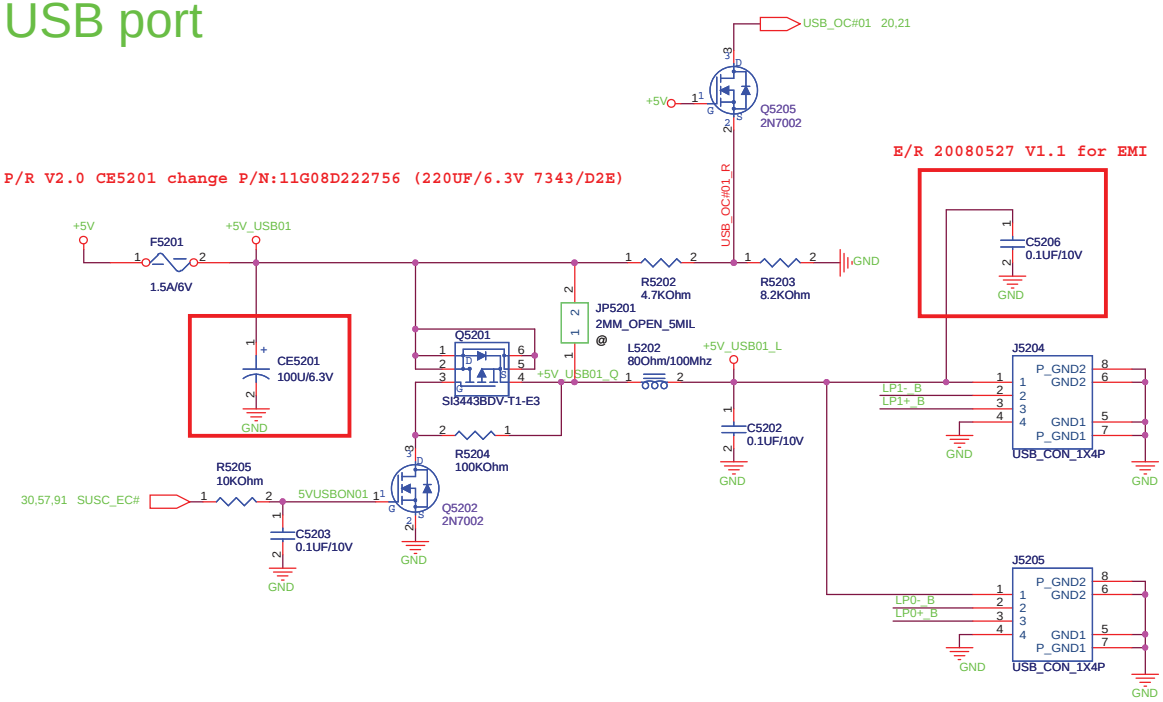
固定SSD MINICARD 用

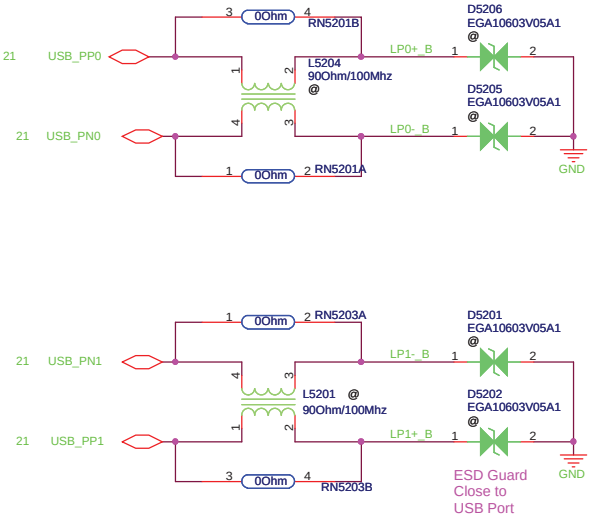
ASUSTeK COMPUTER INC	Title : HDD	
	Engineer: ENGINEER	
Size: C	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 51 of 97	

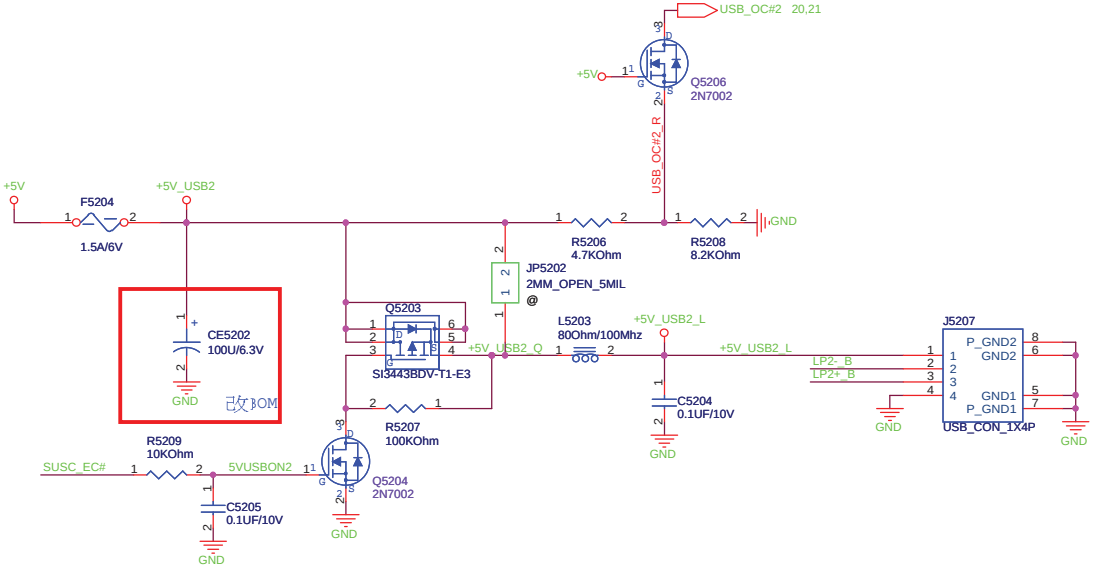
USB port

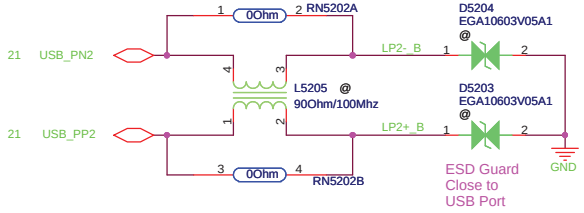
P/R V2.0 CE5201 change P/N:11G08D222756 (220UF/6.3V 7343/D2E)

E/R 20080527 V1.1 for EMI

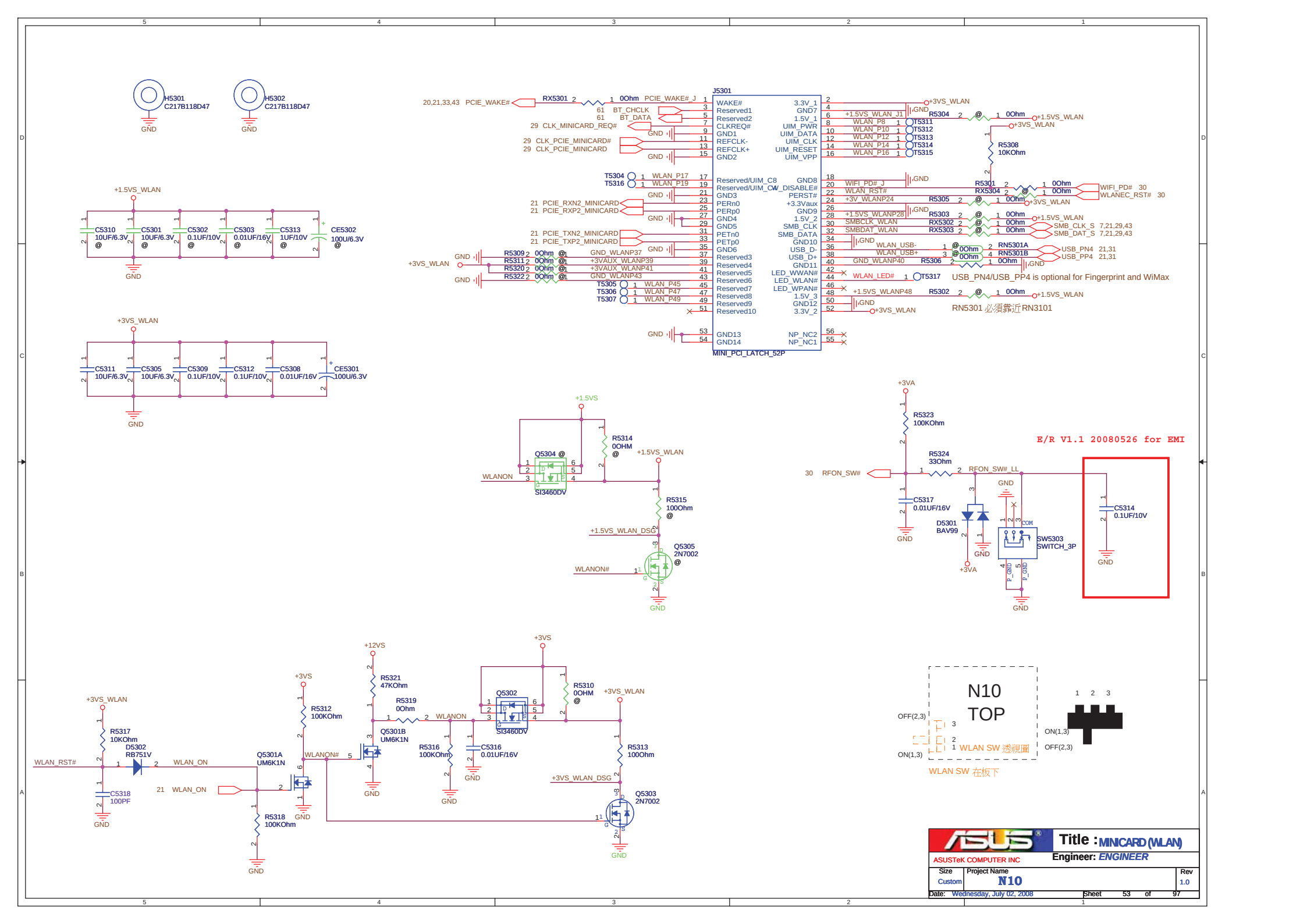








ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Monday, July 07, 2008	Sheet 52 of 97	


H5301
C217B118D47
H5302
C217B118D47
GND
J5301
MINI_PCI_LATCH_52P
WAKE#
Reserved1
Reserved2
CLKREQ#
GND1
REFCLK-
REFCLK+
GND2
3.3V_1
GND7
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
Reserved/UIM_C8
Reserved/UIM_C9
GND3
PERn0
PERp0
GND4
GND5
PETn0
PETp0
GND6
Reserved3
Reserved4
Reserved5
Reserved6
Reserved7
Reserved8
Reserved9
Reserved10
GND8
W_DISABLE#
PERST#
+3.3Vaux
GND9
1.5V_2
SMB_CLK
SMB_DATA
GND10
USB_D-
USB_D+
GND11
LED_WWAN#
LED_WLAN#
LED_WPAN#
1.5V_3
GND12
3.3V_2
GND13
GND14
NP_NC2
NP_NC1
20,21,33,43 PCIE_WAKE#
RX5301 0Ohm PCIE_WAKE# J
BT_CHCLK
BT_DATA
CLK_MINICARD_REQ#
CLK_PCIE_MINICARD#
CLK_PCIE_MINICARD
WLAN_P17
WLAN_P19
PCIE_RXN2_MINICARD
PCIE_RXP2_MINICARD
PCIE_TXN2_MINICARD
PCIE_TXP2_MINICARD
GND_WLANP37
+3VAUX_WLANP39
+3VAUX_WLANP41
GND_WLANP43
WLAN_P45
WLAN_P47
WLAN_P49
+3VS_WLAN
+1.5VS_WLAN_J1
WLAN_P8
WLAN_P10
WLAN_P12
WLAN_P14
WLAN_P16
WIFI_PD# J
WLAN_RST#
+3V_WLANP24
+1.5VS_WLANP28
SMBCLK_WLAN
SMBDAT_WLAN
WLAN_USB-
WLAN_USB+
GND_WLANP40
WLAN_LED#
+1.5VS_WLANP48
R5304 0Ohm
R5308 10KOhm
R5301 0Ohm
RX5304 0Ohm
R5305 0Ohm
R5303 0Ohm
RX5302 0Ohm
RX5303 0Ohm
R5306 0Ohm
R5302 0Ohm
RN5301A
RN5301B
T5311
T5312
T5313
T5314
T5315
T5317
WIFI_PD# 30
WLANEC_RST# 30
SMB_CLK_S 7,21,29,43
SMB_DAT_S 7,21,29,43
USB_PN4 21,31
USB_PP4 21,31
USB_PN4/USB_PP4 is optional for Fingerprint and WiMax
RN5301 必須靠近 RN3101
+1.5VS_WLAN
C5310 10UF/6.3V @
C5301 10UF/6.3V @
C5302 0.1UF/10V @
C5303 0.01UF/16V @
C5313 1UF/10V @
CE5302 100U/6.3V @
+3VS_WLAN
C5311 10UF/6.3V
C5305 10UF/6.3V
C5309 0.1UF/10V
C5312 0.1UF/10V
C5308 0.01UF/16V
CE5301 100U/6.3V
+1.5VS
Q5304 @
SI3460DV
R5314 0OHM @
WLANON
R5315 100Ohm @
+1.5VS_WLAN_DSG
Q5305 2N7002 @
WLANON#
+3VA
R5323 100KOhm
R5324 33Ohm
30 RFON_SW#
RFON_SW#_LL
C5317 0.01UF/16V
D5301 BAV99
SW5303 SWITCH_3P
C5314 0.1UF/10V
E/R V1.1 20080526 for EMI
+12VS
R5321 47KOhm
R5319 0Ohm
Q5301B UM6K1N
R5316 100KOhm
C5316 0.01UF/16V
Q5302
SI3460DV
R5310 0OHM @
R5313 100Ohm
+3VS_WLAN_DSG
Q5303 2N7002
R5312 100KOhm
Q5301A UM6K1N
R5317 10KOhm
D5302 RB751V
C5318 100PF
R5318 100KOhm
WLAN_RST#
WLAN_ON
21 WLAN_ON
N10
TOP
OFF(2,3)
ON(1,3)
WLAN SW 透視圖
WLAN SW 在板下
ASUSTeK COMPUTER INC
Title : MINICARD (WLAN)
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
Sheet 53 of 97

Title : EMPTY

ASUSTek COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 54 of 97

Title : EMPTY

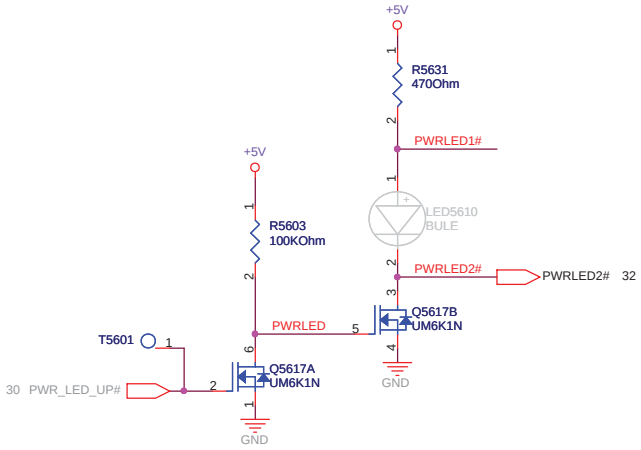
ASUSTeK COMPUTER INC

Engineer: ENGINEER

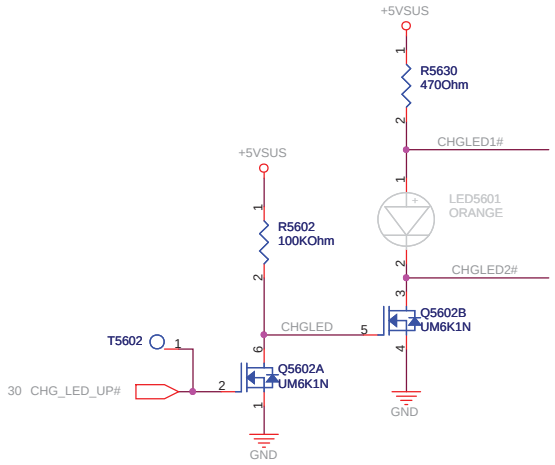
Size	Project Name	Rev
A	N10	1.0

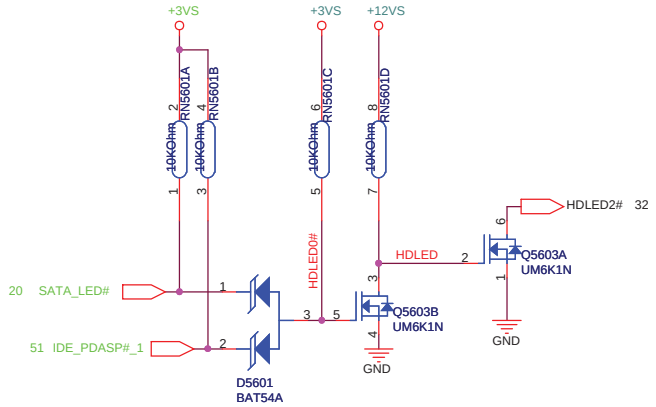
Date: Wednesday, July 02, 2008 Sheet 55 of 97

POWER LED



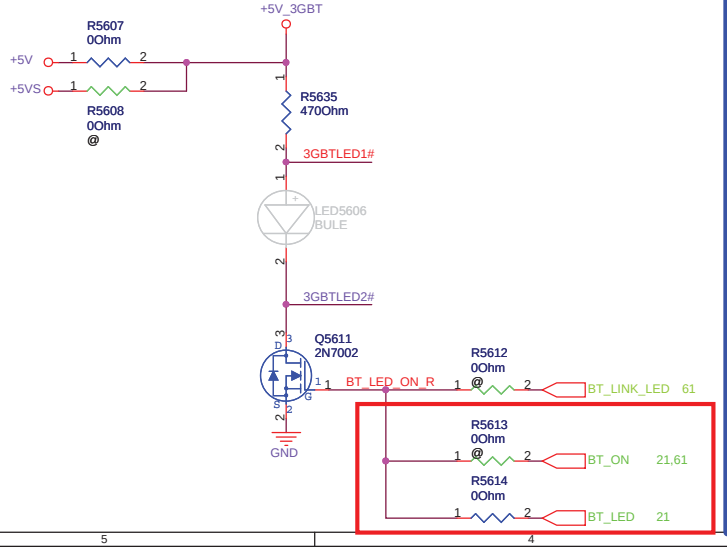
CHARGE LED



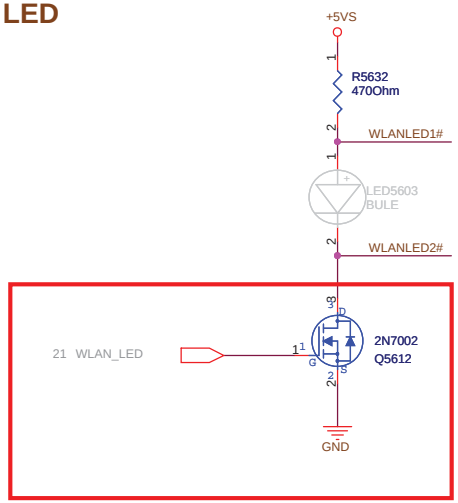


BT LED

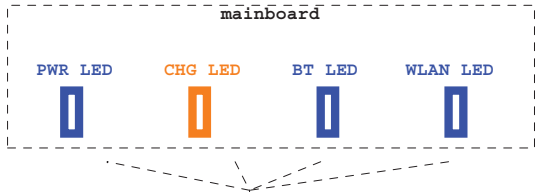
P/R V2.0 2008/6/29 R5613 unmount, R5614 mount

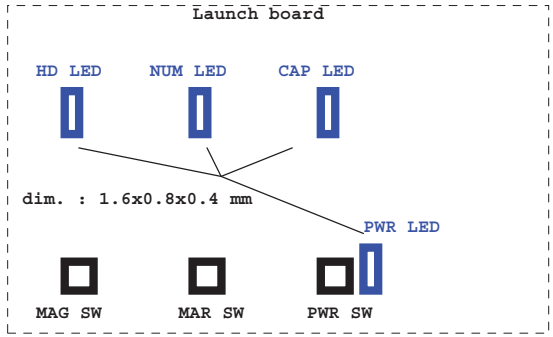


WLAN LED

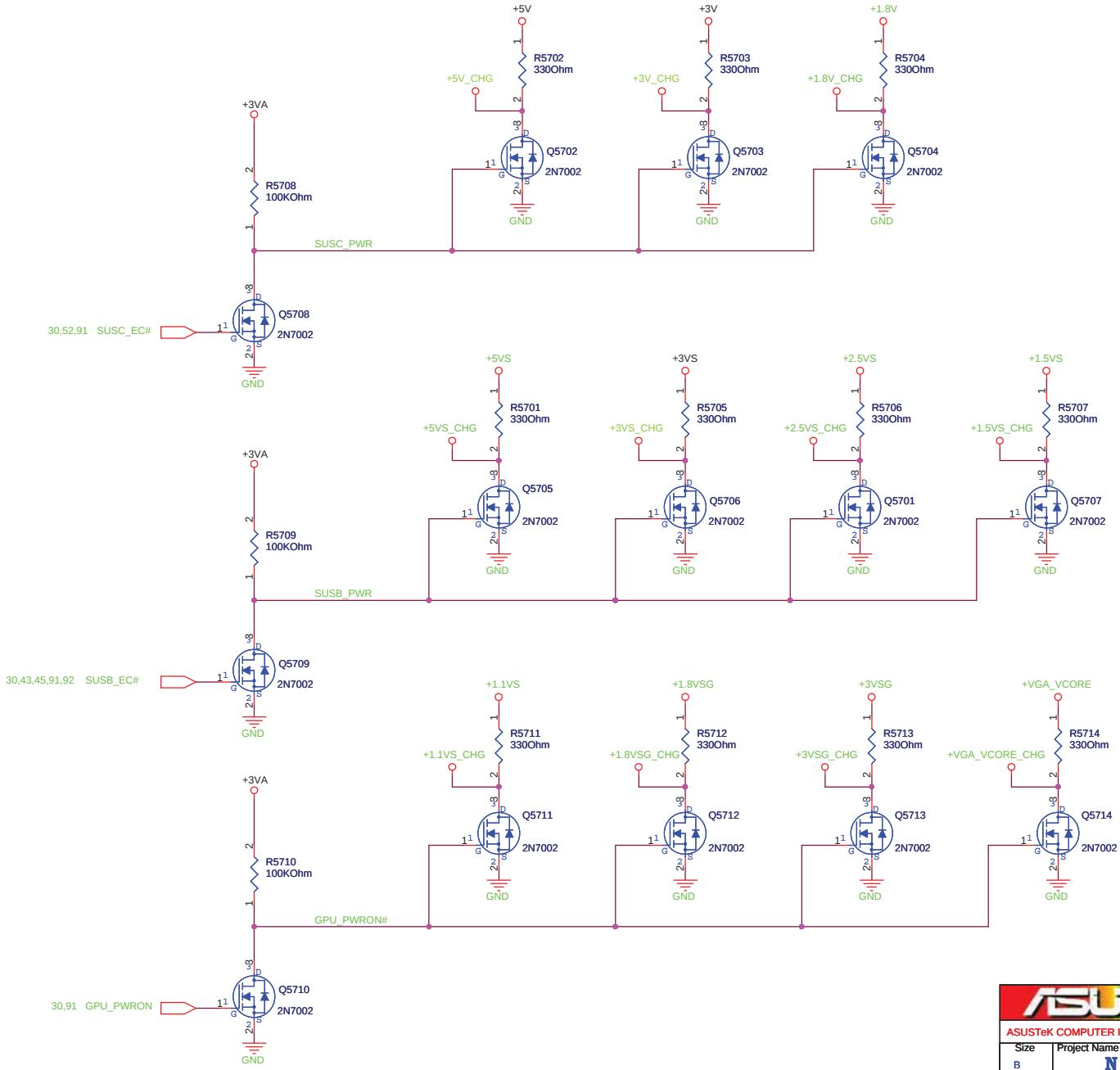


P/R V2.0 2008/6/29 mount Q5612





ASUSTek COMPUTER INC	Title : LED	
	Engineer: ENGINEER	
Size: B	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 56 of 97	



ASUSTeK COMPUTER INC

Title : Discharge Circuit

Engineer: ENGINEER

Size	Project Name	Rev
B	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 57 of 97

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
B	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 58 of 97

Title : EMPTY

ASUSTeK COMPUTER INC

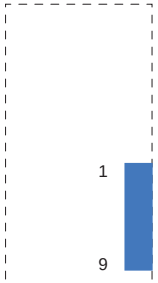
Engineer: ENGINEER

Size	Project Name	Rev
B	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 59 of 97

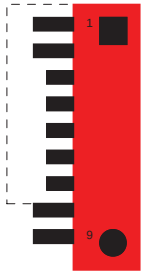
BAT1 JACK

Pin	Signal
1	P+
2	P+
3	CNT1
4	CNT2
5	SMBC
6	SMBD
7	ID
8	GND
9	GND

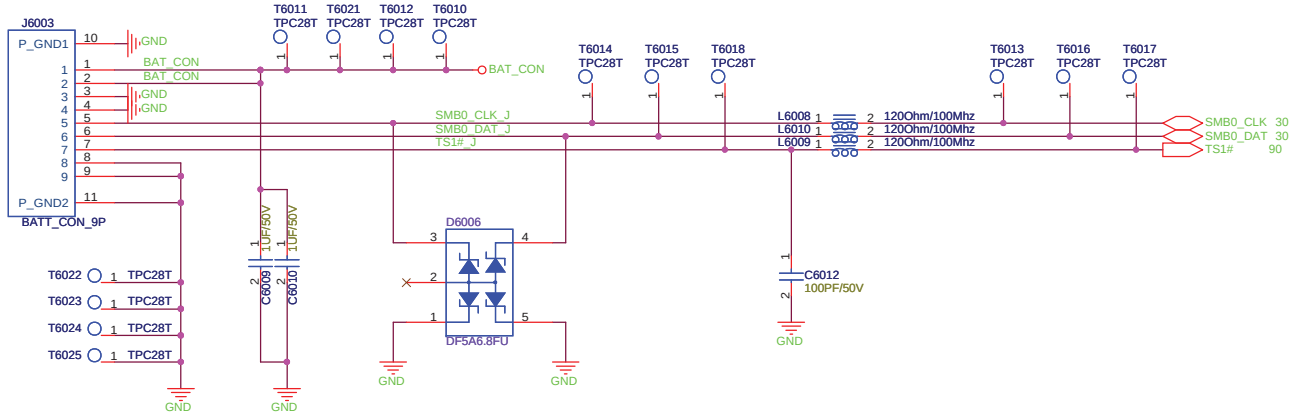


主電池上視圖

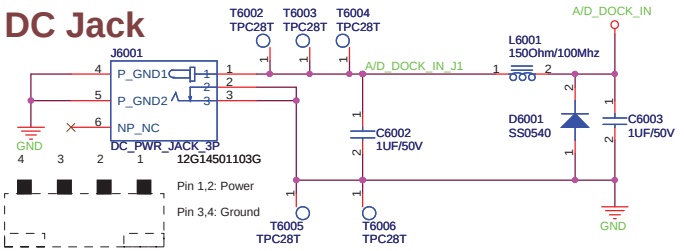
TOP VIEW(板上



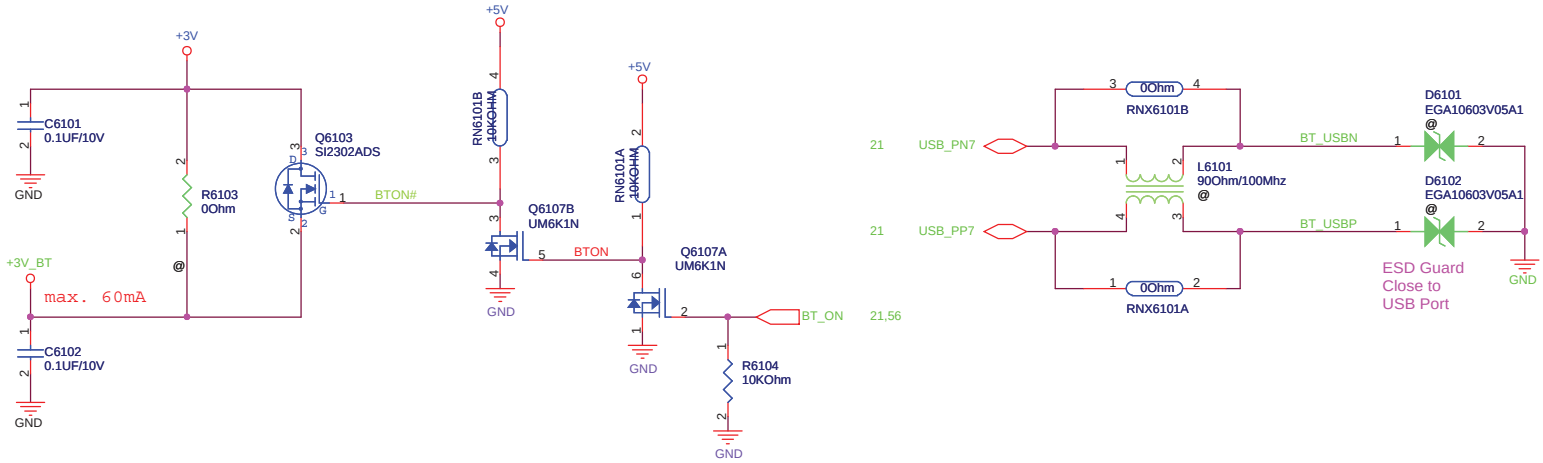
BOT VIEW(板下

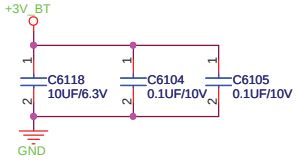


DC Jack

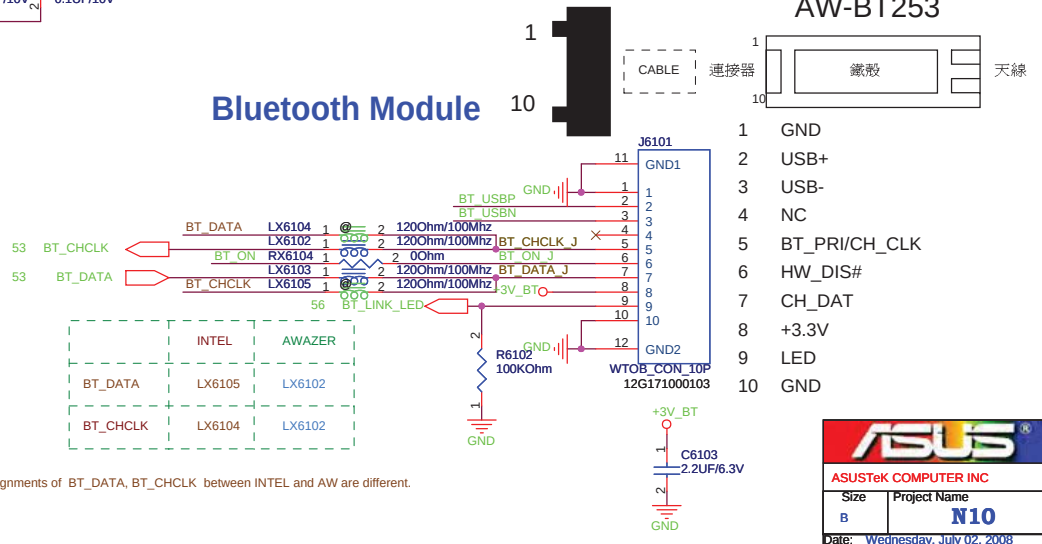


ASUSTeK COMPUTER INC	Title : DC/BATT Conn.	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 60 of 97	





Bluetooth Module



1	GND
2	USB+
3	USB-
4	NC
5	BT_PRI/CH_CLK
6	HW_DIS#
7	CH_DAT
8	+3.3V
9	LED
10	GND

Pin-assignments of BT_DATA, BT_CHCLK between INTEL and AW are different.

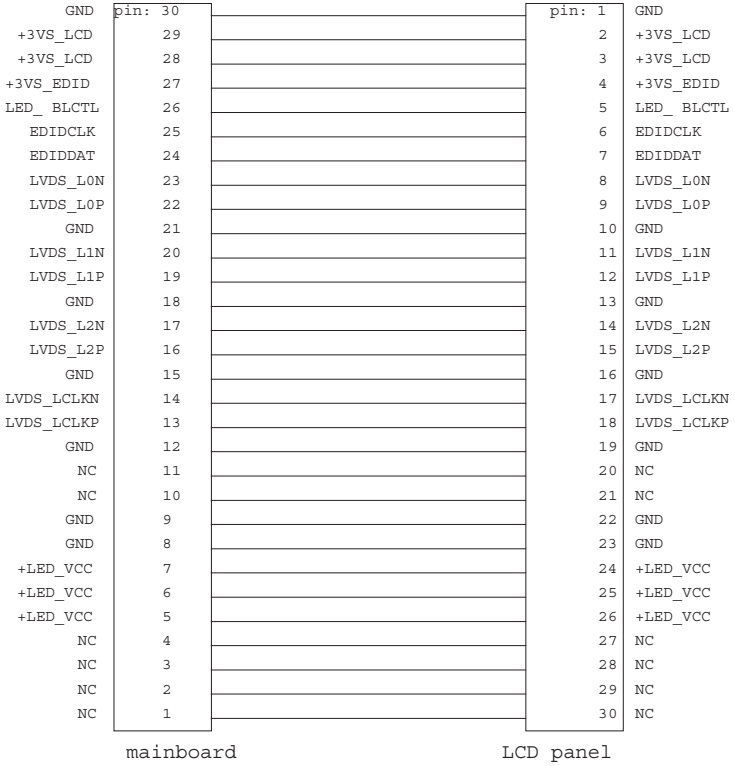
ASUSTeK COMPUTER INC

Title : BLUETOOTH

Engineer: ENGINEER

Size	Project Name	Rev
B	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 61 of 97



ASUSTeK COMPUTER INC

Title : EMPTY

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 62 of 97

Title :	EMPTY
ASUSTeK COMPUTER INC	Engineer: ENGINEER
Size: Custom	Project Name: N10
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 63 of 97

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

IC	REFERENCE	VENID	DEVID	VERSION	MARK
NB9M-GS			0x06E9		Current Version: A2

ASUSTeK COMPUTER INC

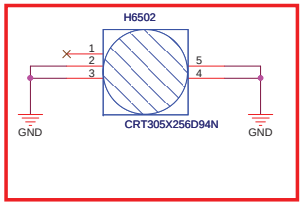
Title : RESOURCE

Engineer: ENGINEER

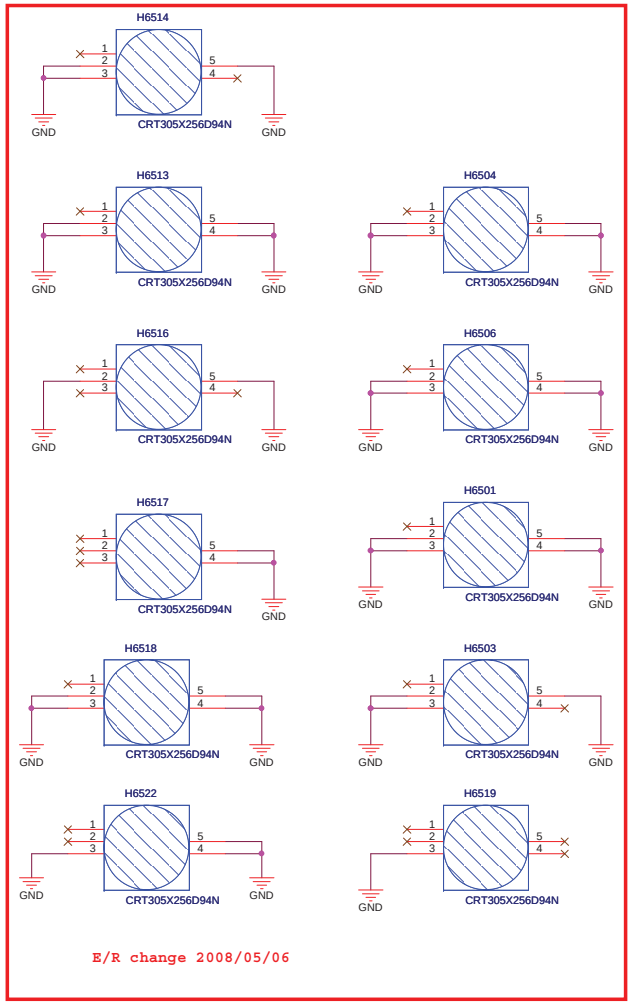
Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 64 of 97

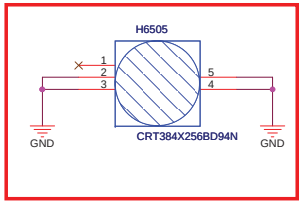
A+E



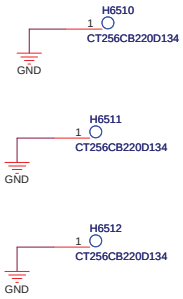
A+B



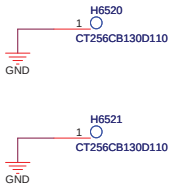
O+B



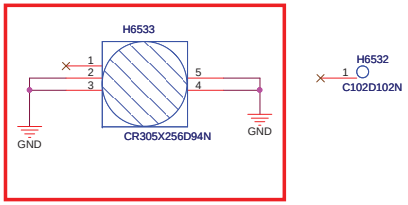
G+H



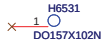
D



A+A

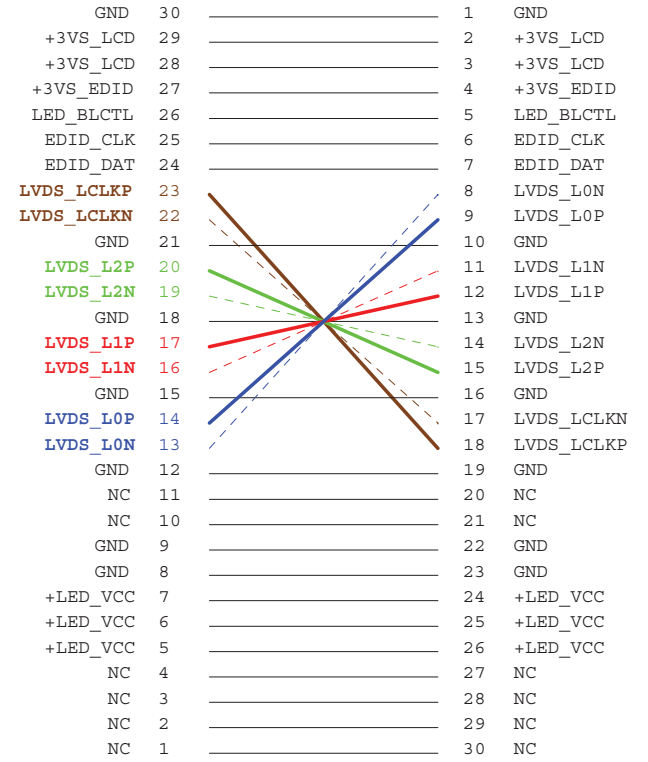


L



ASUSTeK COMPUTER INC	Title : ME-SKEW HOLE	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 65 of 97	

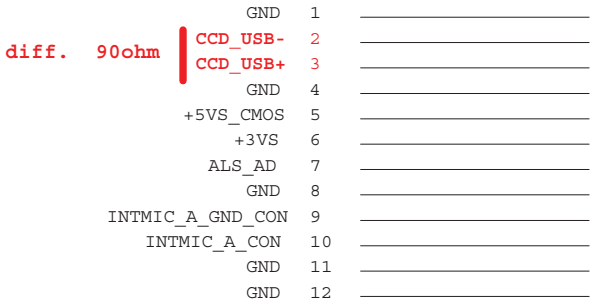
LVDS CABLE (WTB)



MAINBOARD CONNECT LCD PANEL CONNECT

P/N: 12G171040305

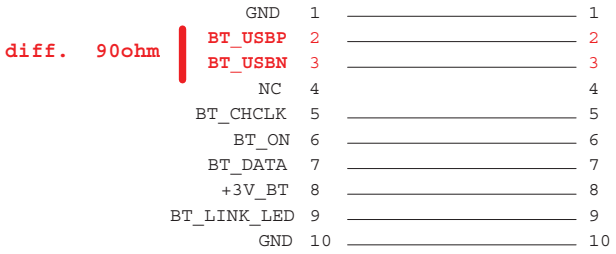
MIC., CCD, ALS CABLE(WTB)



MAINBOARD CONNECT

P/N: 12G171000124

BLUETOOTH CABLE(WTB)



MAINBOARD CONNECT BlueTooth

P/N: 12G171000103

ASUSTeK COMPUTER INC

Title : EMPTY

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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LAUNCH CABLE(WTB)

+5V	14	———	14	+5V
+3VA	13	———	13	+3VA
GND	12	———	12	GND
LID_SW#	11	———	11	LID_SW#
PWRLED#	10	———	10	PWRLED#
PWR_SW#	9	———	9	PWR_SW#
GND	8	———	8	GND
MARATHON_SW#	7	———	7	MARATHON_SW#
MAGNIFY_SW#	6	———	6	MAGNIFY_SW#
+3VS	5	———	5	+3VS
HDLED#	4	———	4	HDLED#
NUM_LED#	3	———	3	NUM_LED#
CAP_LED#	2	———	2	CAP_LED#
+5VS	1	———	1	+5VS

MAINBOARD CONNECT

P/N: 12G171000145

LAUNCH BOARD CONNECT

P/N: 12G171030140

MODEM CABLE(WTB)

RING	1	———	1	RING
TIP	2	———	2	TIP

MAINBOARD CONNECT

MODEM CONNECT

FINGER-PRINTER CABLE(FFC)

GND	12	———	12	GND
FP_USB+	11	———	11	FP_USB+
FP_USB-	10	———	10	FP_USB-
+3VS	9	———	9	+3VS
NC	8	———	8	NC
NC	7	———	7	NC
GND	6	———	6	GND
GND	5	———	5	GND
TP_CLK	4	———	4	TP_CLK
TP_DAT	3	———	3	TP_DAT
+5VS_TP	2	———	2	+5VS_TP
+5VS_TP	1	———	1	+5VS_TP

MAINBOARD CONNECT

P/N: 12G18340120C

下接觸

FINGER-PRINTER BOARD CONNECT

P/N: 12G18340120C

下接觸

Touch-Pad CABLE(FFC)

+5VS	12	———	12	+5VS
+5VS	11	———	11	+5VS
TP_DAT	10	———	10	TP_DAT
TP_CLK	9	———	9	TP_CLK
GND	8	———	8	GND
GND	7	———	7	GND
NC	6	———	6	NC
NC	5	———	5	NC
NC	4	———	4	NC
SWL	3	———	3	SWL
SWR	2	———	2	SWR
NC	1	———	1	NC

FINGER-PRINTER BOARD CONNECT

P/N: 12G183301208

上接觸

Touch-Pad BOARD CONNECT

上接觸

ASUSTeK COMPUTER INC

Title : EMPTY

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 67 of 97

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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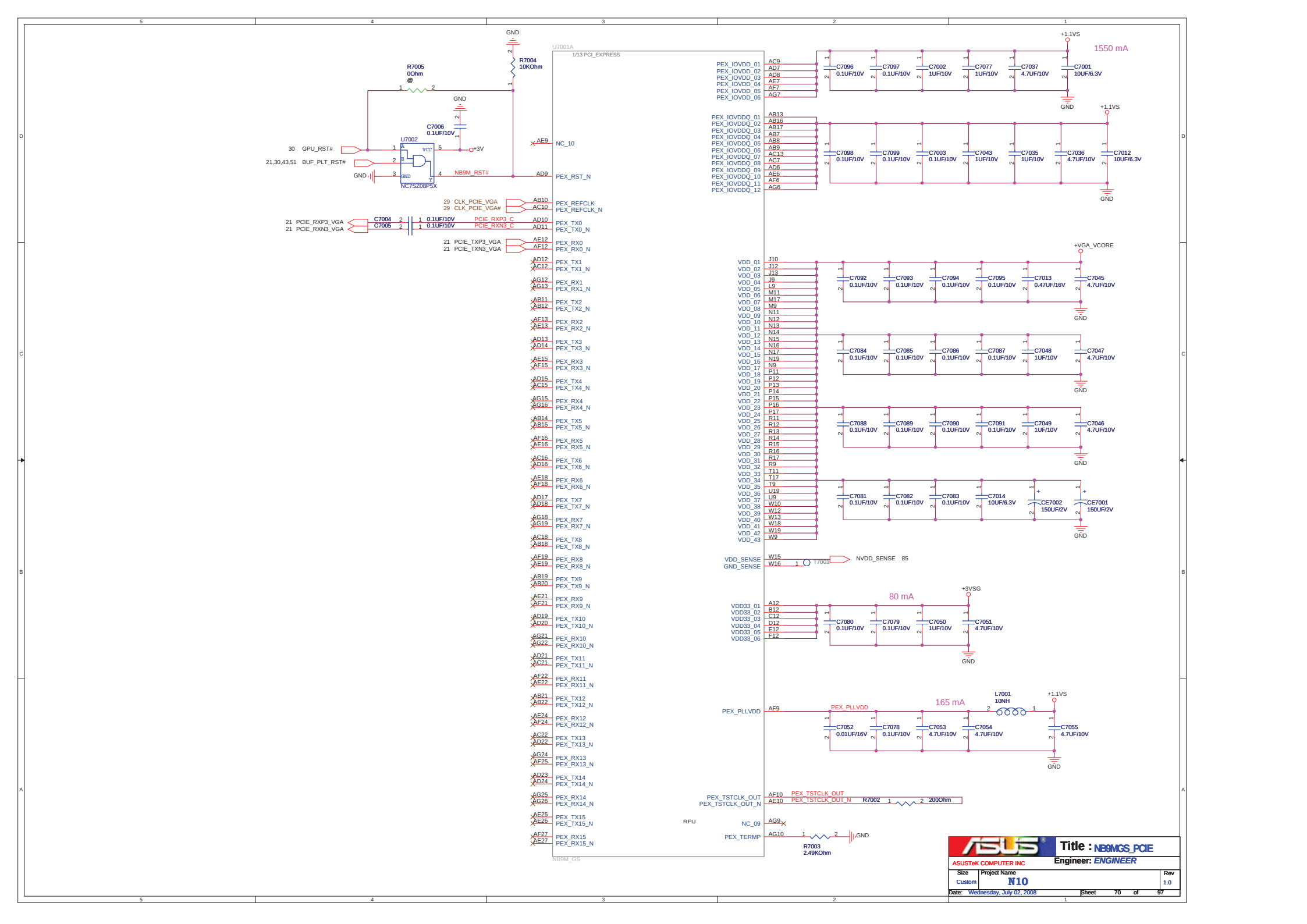
1.0 SR(2006/11/29)

ASUSTeK COMPUTER INC	Title : HISTORY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 69 of 97	


U7001A
1/13 PCI_EXPRESS
R7004 10KOhm
R7005 0Ohm @
C7006 0.1UF/10V
U7002 NC7SZ08P5X
GPU_RST#
BUF_PLT_RST#
NB9M_RST#
+3V
NC_10
PEX_RST_N
CLK_PCIE_VGA
CLK_PCIE_VGA#
PEX_REFCLK
PEX_REFCLK_N
PCIE_RXP3_VGA
PCIE_RXN3_VGA
C7004 0.1UF/10V
C7005 0.1UF/10V
PCIE_RXP3_C
PCIE_RXN3_C
PEX_TX0
PEX_TX0_N
PCIE_TXP3_VGA
PCIE_TXN3_VGA
PEX_RX0
PEX_RX0_N
PEX_TX1
PEX_TX1_N
PEX_RX1
PEX_RX1_N
PEX_TX2
PEX_TX2_N
PEX_RX2
PEX_RX2_N
PEX_TX3
PEX_TX3_N
PEX_RX3
PEX_RX3_N
PEX_TX4
PEX_TX4_N
PEX_RX4
PEX_RX4_N
PEX_TX5
PEX_TX5_N
PEX_RX5
PEX_RX5_N
PEX_TX6
PEX_TX6_N
PEX_RX6
PEX_RX6_N
PEX_TX7
PEX_TX7_N
PEX_RX7
PEX_RX7_N
PEX_TX8
PEX_TX8_N
PEX_RX8
PEX_RX8_N
PEX_TX9
PEX_TX9_N
PEX_RX9
PEX_RX9_N
PEX_TX10
PEX_TX10_N
PEX_RX10
PEX_RX10_N
PEX_TX11
PEX_TX11_N
PEX_RX11
PEX_RX11_N
PEX_TX12
PEX_TX12_N
PEX_RX12
PEX_RX12_N
PEX_TX13
PEX_TX13_N
PEX_RX13
PEX_RX13_N
PEX_TX14
PEX_TX14_N
PEX_RX14
PEX_RX14_N
PEX_TX15
PEX_TX15_N
PEX_RX15
PEX_RX15_N
NB9M_GS
PEX_IOVDD_01
PEX_IOVDD_02
PEX_IOVDD_03
PEX_IOVDD_04
PEX_IOVDD_05
PEX_IOVDD_06
C7096 0.1UF/10V
C7097 0.1UF/10V
C7002 1UF/10V
C7077 1UF/10V
C7037 4.7UF/10V
C7001 10UF/6.3V
1550 mA
PEX_IOVDDQ_01
PEX_IOVDDQ_02
PEX_IOVDDQ_03
PEX_IOVDDQ_04
PEX_IOVDDQ_05
PEX_IOVDDQ_06
PEX_IOVDDQ_07
PEX_IOVDDQ_08
PEX_IOVDDQ_09
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
C7098 0.1UF/10V
C7099 0.1UF/10V
C7003 0.1UF/10V
C7043 1UF/10V
C7035 1UF/10V
C7036 4.7UF/10V
C7012 10UF/6.3V
VDD_01
VDD_02
VDD_03
VDD_04
VDD_05
VDD_06
VDD_07
VDD_08
VDD_09
VDD_10
VDD_11
VDD_12
VDD_13
VDD_14
VDD_15
VDD_16
VDD_17
VDD_18
VDD_19
VDD_20
VDD_21
VDD_22
VDD_23
VDD_24
VDD_25
VDD_26
VDD_27
VDD_28
VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36
VDD_37
VDD_38
VDD_39
VDD_40
VDD_41
VDD_42
VDD_43
C7092 0.1UF/10V
C7093 0.1UF/10V
C7094 0.1UF/10V
C7095 0.1UF/10V
C7013 0.47UF/16V
C7045 4.7UF/10V
C7084 0.1UF/10V
C7085 0.1UF/10V
C7086 0.1UF/10V
C7087 0.1UF/10V
C7048 1UF/10V
C7047 4.7UF/10V
C7088 0.1UF/10V
C7089 0.1UF/10V
C7090 0.1UF/10V
C7091 0.1UF/10V
C7049 1UF/10V
C7046 4.7UF/10V
C7081 0.1UF/10V
C7082 0.1UF/10V
C7083 0.1UF/10V
C7014 10UF/6.3V
CE7002 150UF/2V
CE7001 150UF/2V
VDD_SENSE
GND_SENSE
T7001
NVDD_SENSE 85
VDD33_01
VDD33_02
VDD33_03
VDD33_04
VDD33_05
VDD33_06
80 mA
C7080 0.1UF/10V
C7079 0.1UF/10V
C7050 1UF/10V
C7051 4.7UF/10V
PEX_PLLVDD
165 mA
L7001 10NH
C7052 0.01UF/16V
C7078 0.1UF/10V
C7053 4.7UF/10V
C7054 4.7UF/10V
C7055 4.7UF/10V
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
R7002 200Ohm
RFU
NC_09
PEX_TERMP
R7003 2.49KOhm
GND
+1.1VS
+VGA_VCORE
+3VSG
Title : NB9MGS_PCIE
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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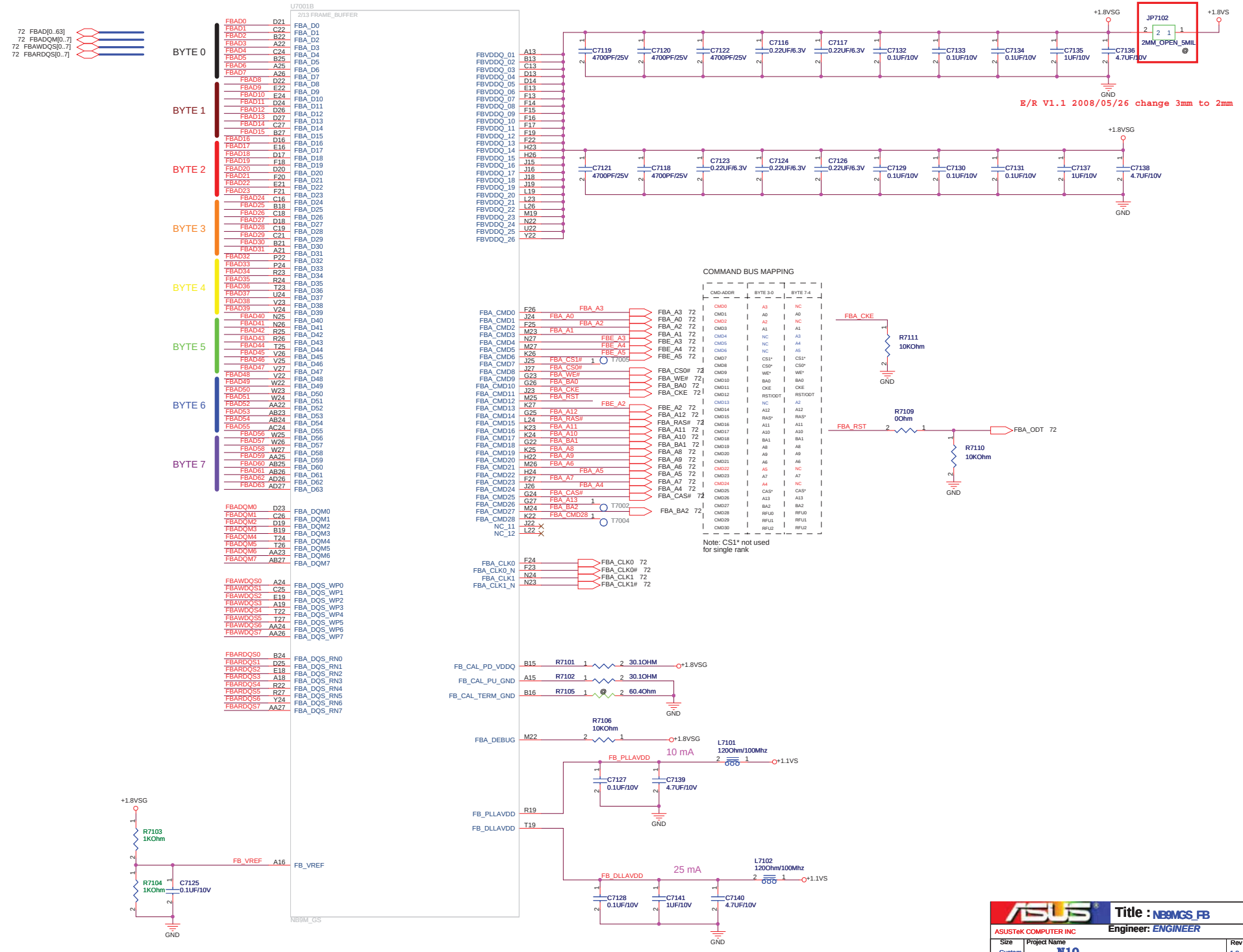
72 FBAD[0..63]
72 FBADQM[0..7]
72 FBAWDQS[0..7]
72 FBARDQS[0..7]
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
U7001B
2/13 FRAME_BUFFER
NB9M_GS
FBVDDQ_01 FBVDDQ_02 FBVDDQ_03 FBVDDQ_04 FBVDDQ_05 FBVDDQ_06 FBVDDQ_07 FBVDDQ_08 FBVDDQ_09 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26
+1.8VSG
C7119 4700PF/25V
C7120 4700PF/25V
C7122 4700PF/25V
C7116 0.22UF/6.3V
C7117 0.22UF/6.3V
C7132 0.1UF/10V
C7133 0.1UF/10V
C7134 0.1UF/10V
C7135 1UF/10V
C7136 4.7UF/10V
JP7102
2MM_OPEN_5MIL
@
+1.8VS
GND
E/R V1.1 2008/05/26 change 3mm to 2mm
C7121 4700PF/25V
C7118 4700PF/25V
C7123 0.22UF/6.3V
C7124 0.22UF/6.3V
C7126 0.22UF/6.3V
C7129 0.1UF/10V
C7130 0.1UF/10V
C7131 0.1UF/10V
C7137 1UF/10V
C7138 4.7UF/10V
COMMAND BUS MAPPING
CMD-ADDR
BYTE 3-0
BYTE 7-4
Note: CS1* not used for single rank
FBA_CKE
R7111 10KOhm
R7109 0Ohm
FBA_RST
FBA_ODT 72
R7110 10KOhm
T7009
T7002
T7004
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R7101 30.1OHM
R7102 30.1OHM
R7105 @ 60.4Ohm
R7106 10KOhm
FBA_DEBUG
FB_PLLAVDD
FB_DLLAVDD
10 mA
25 mA
L7101 120Ohm/100Mhz
L7102 120Ohm/100Mhz
+1.1VS
C7127 0.1UF/10V
C7139 4.7UF/10V
C7128 0.1UF/10V
C7141 1UF/10V
C7140 4.7UF/10V
R7103 1KOhm
R7104 1KOhm
C7125 0.1UF/10V
FB_VREF
Title : NB9MGS_FB
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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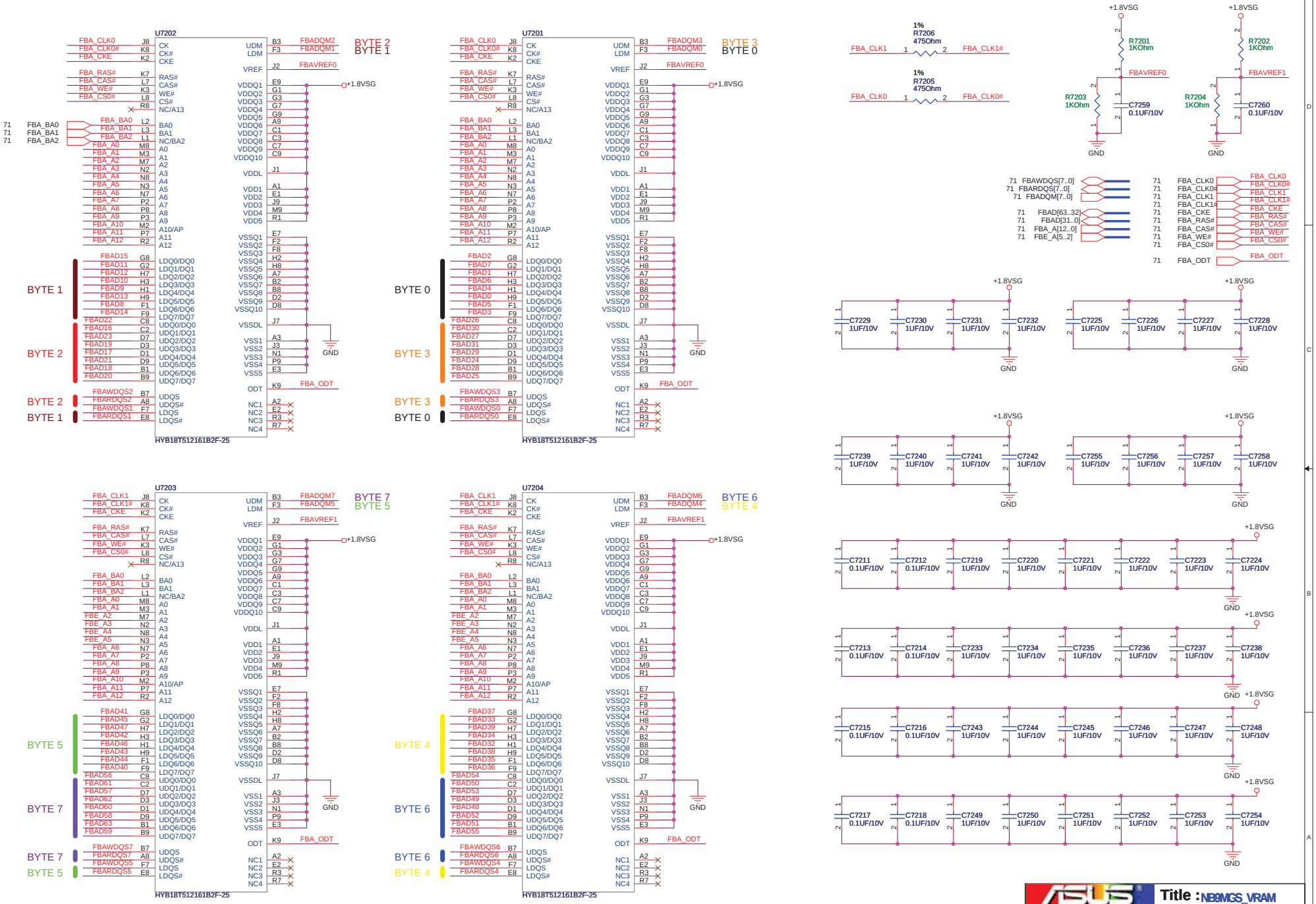

ASUSTeK COMPUTER INC

Title : NB9MGS_VRAM

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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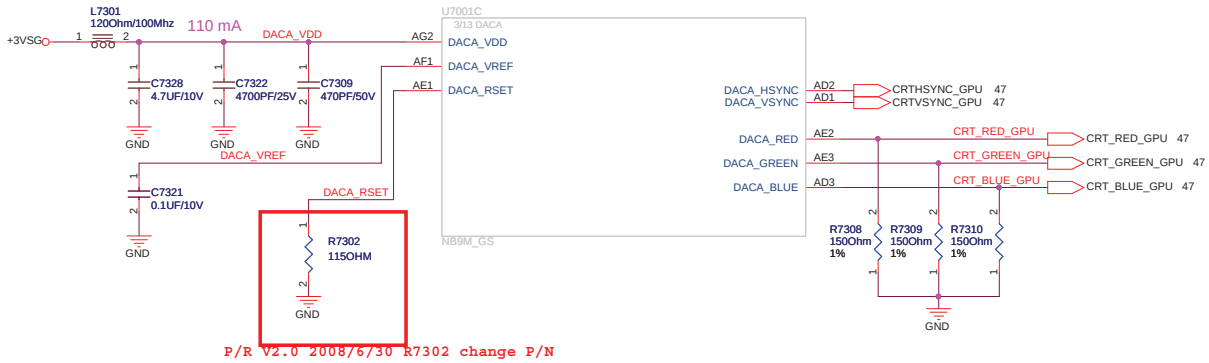
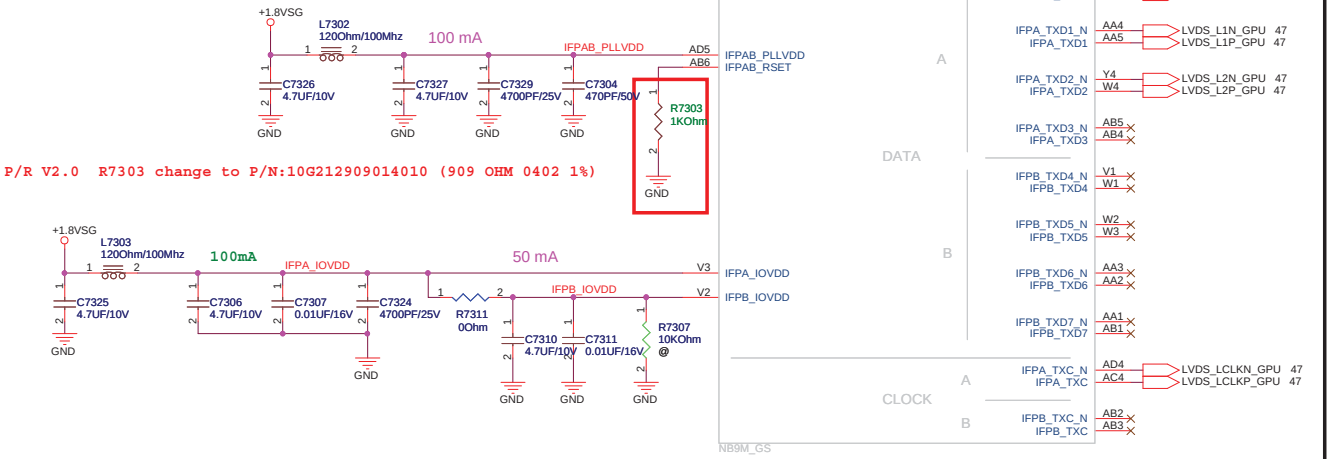
VGA

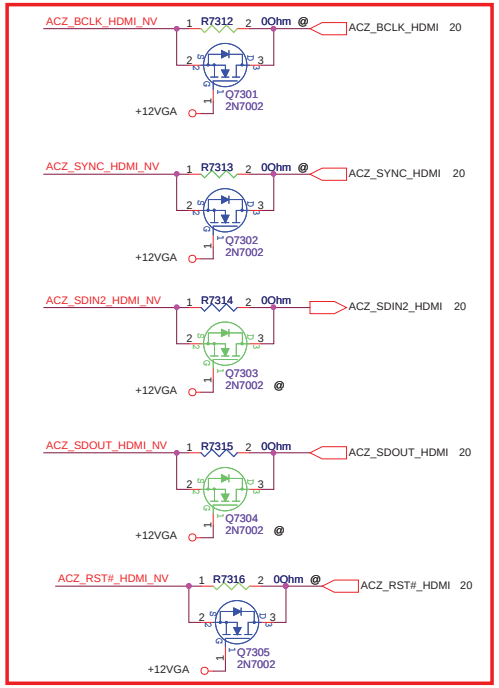


P/R V2.0 2008/6/30 R7302 change P/N

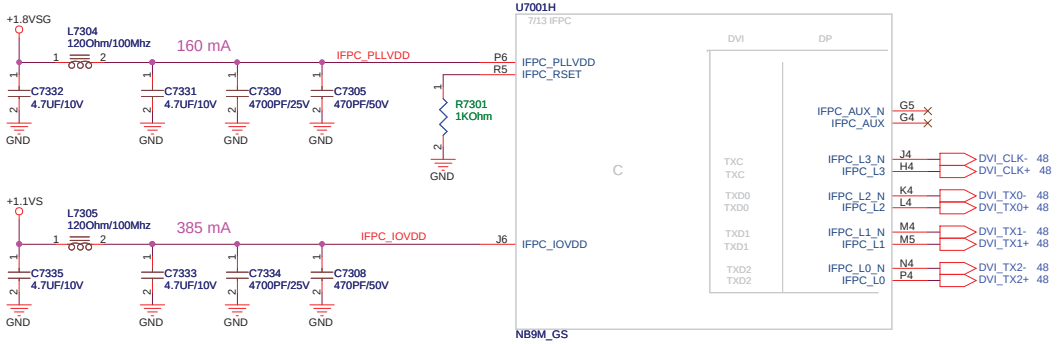
LVDS

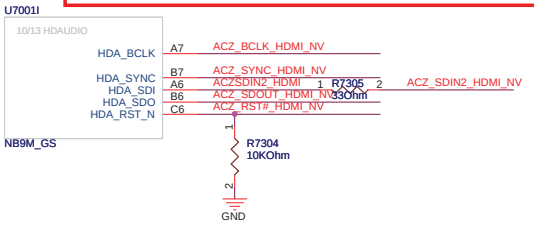


P/R V2.0 R7303 change to P/N:10G212909014010 (909 OHM 0402 1%)



HDMI





ASUSTeK COMPUTER INC

Title : NB9MGS_DISPLAY

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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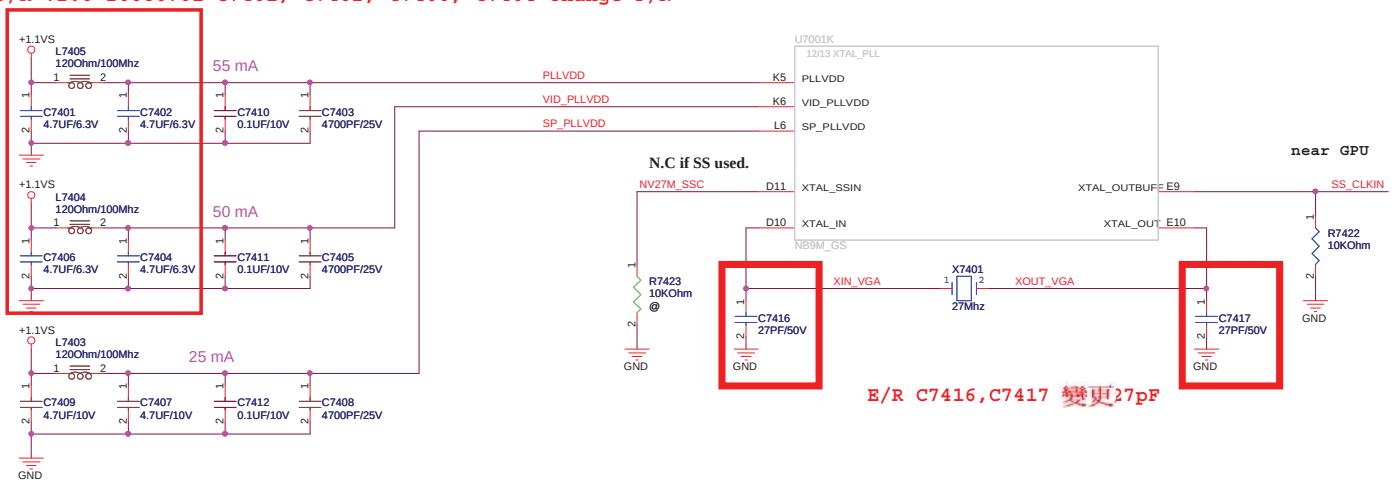
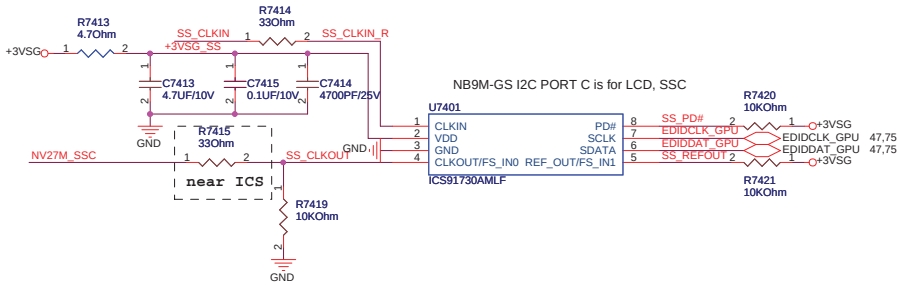
Xtal

P/R V2.0 20080701 C7401, C7402, C7406, C7404 change P/N

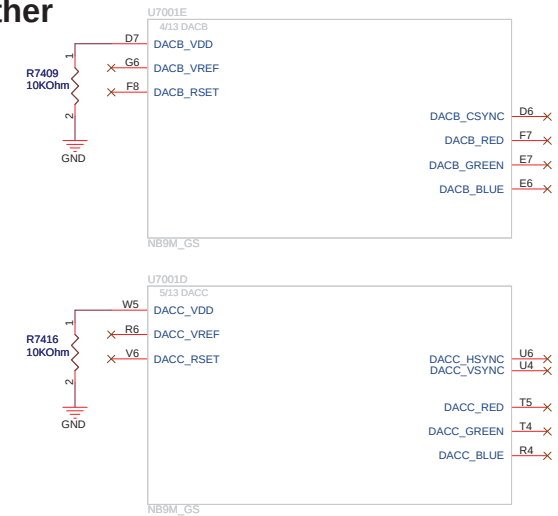


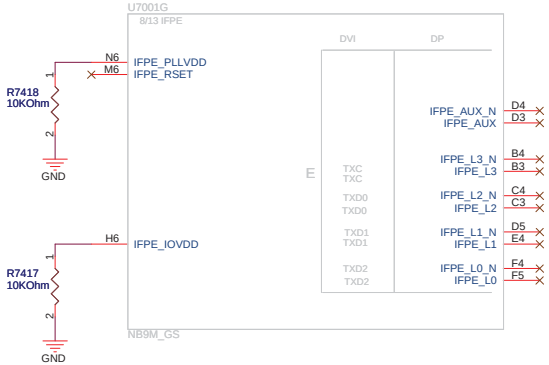
E/R C7416,C7417 變更27pF

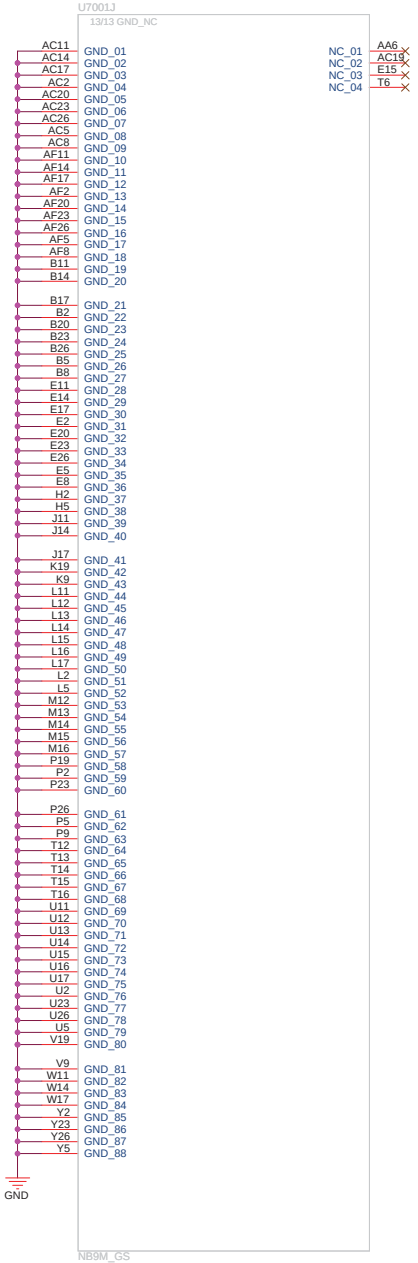
EXTERNAL SPREAD SPECTRUM



Other







ASUSTeK COMPUTER INC

Title : NB9MGS_XTAL

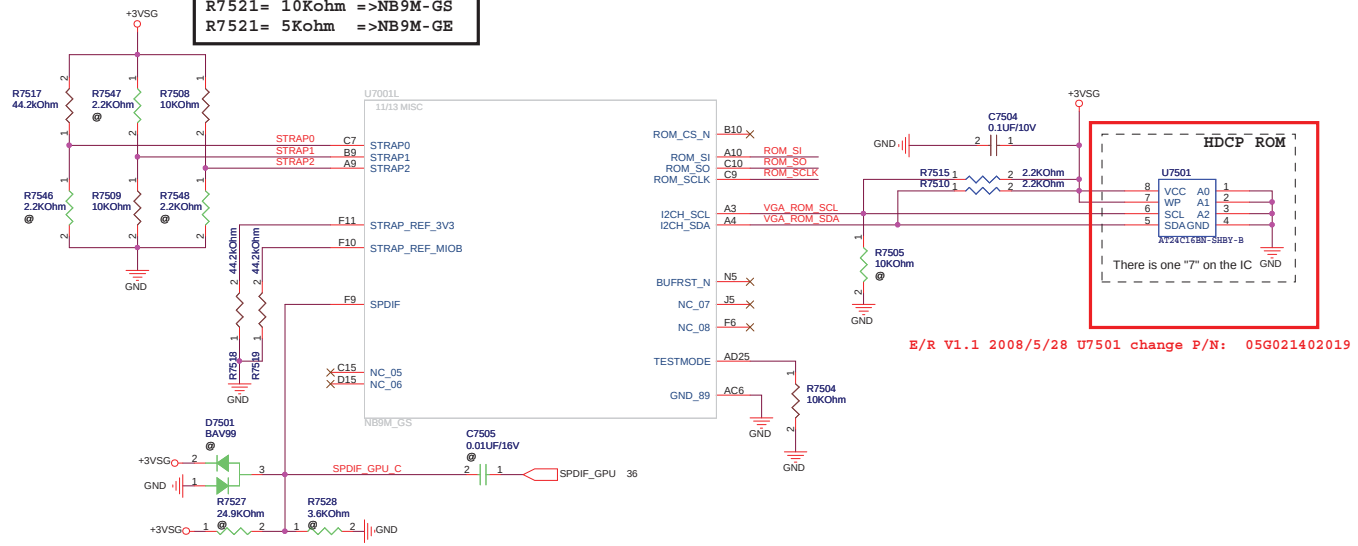
Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

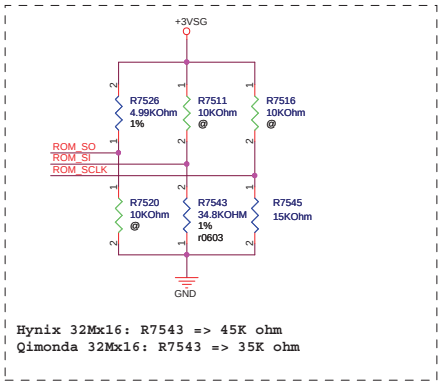
Date: Wednesday, July 02, 2008 Sheet 74 of 97

ROM

R7521= 10Kohm =>NB9M-GS
R7521= 5Kohm =>NB9M-GE



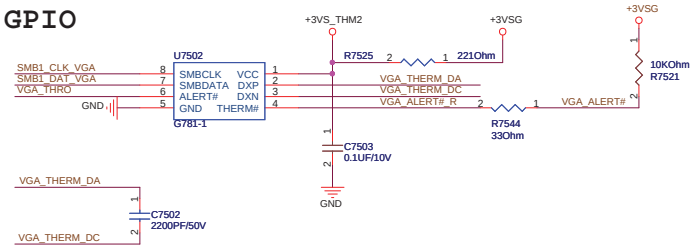
E/R V1.1 2008/5/28 U7501 change P/N: 05G021402019

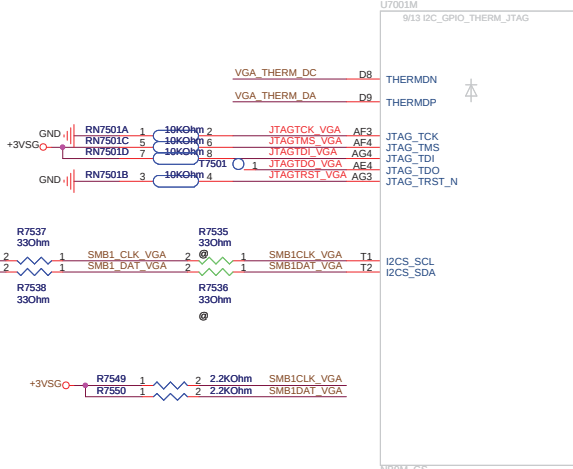


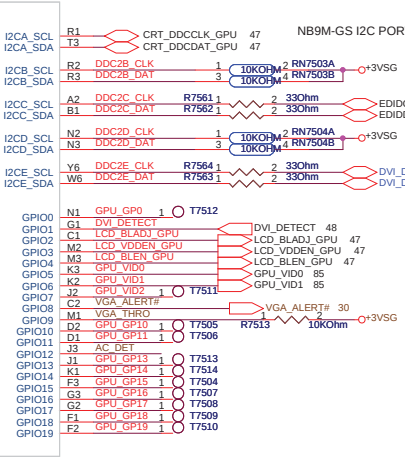
Hynix 32Mx16: R7543 => 45K ohm
Qimonda 32Mx16: R7543 => 35K ohm

External thermal sensor

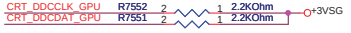
GPIO







NB9M-GS I2C PORT A is for CRT

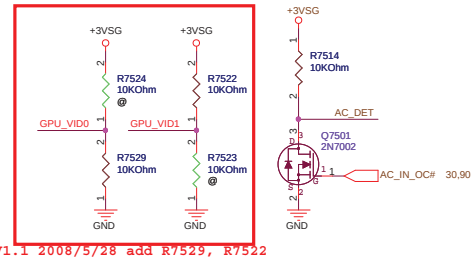


NB9M-GS I2C PORT C is for LCD, SSC

NB9M-GS I2C PORT E is for HDMI

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL



E/R V1.1 2008/5/28 add R7529, R7522

ASUSTeK COMPUTER INC	Title : NB9MGS_ROM		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 75 of 97		

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: ENGINEER

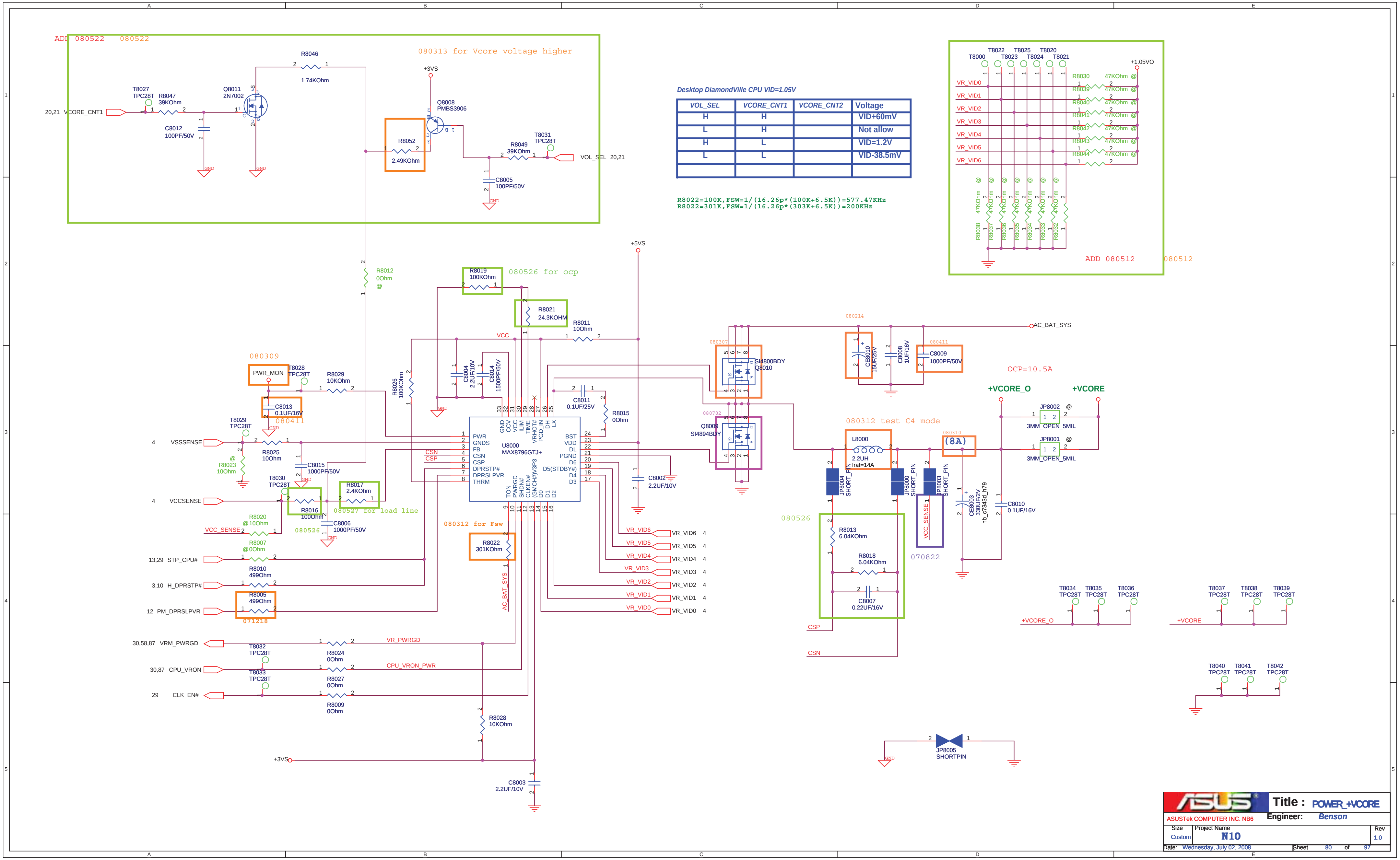
Size	Project Name	Rev
A	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 76 of 97

ASUSTeK COMPUTER INC			Title : ****	
			Engineer: ENGINEER	
Size: Custom	Project Name: N10			Rev: 1.0
Date: Wednesday, July 02, 2008		Sheet 77 of 97		

Title : ****	
ASUSTeK COMPUTER INC	Engineer: *ENGINEER*
Size: B	Project Name: N10 FUNC BOARD
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 78 of 97

Title : ****	
ASUSTeK COMPUTER INC	Engineer: *ENGINEER*
Size: B	Project Name: N10 POWER SW
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 79 of 97


ADD 080522 080522
080313 for Vcore voltage higher
R8046 1.74KOhm
+3VS
T8027 TPC28T R8047 39KOhm
Q8011 2N7002
20,21 VCORE_CNT1
C8012 100PF/50V
Q8008 PMBS3906
R8052 2.49KOhm
R8049 39KOhm
T8031 TPC28T
VOL_SEL 20,21
C8005 100PF/50V
Desktop DiamondVille CPU VID=1.05V
R8022=100K,FSW=1/(16.26p*(100K+6.5K))=577.47KHz
R8022=301K,FSW=1/(16.26p*(303K+6.5K))=200KHz
+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
ADD 080512 080512
+5VS
R8012 0Ohm
R8019 100KOhm
080526 for ocp
R8021 24.3KOHM
R8011 10Ohm
AC_BAT_SYS
080309
PWR_MON
T8028 TPC28T
R8029 10KOhm
C8013 0.1UF/16V
080411
R8026 100KOhm
C8004 2.2UF/10V
C8014 1500PF/50V
C8011 0.1UF/25V
R8015 0Ohm
U8000 MAX8796GTJ+
SI4800BDY Q8010
Q8009 SI4894BDY
CE8010 15UF/25V
C8008 1UF/16V
C8009 1000PF/50V
OCP=10.5A
+VCORE_O
+VCORE
JP8002 3MM_OPEN_5MIL
JP8001 3MM_OPEN_5MIL
080312 test C4 mode
L8000 2.2UH Irat=14A
(8A)
VSSSENSE
VCCSENSE
R8025 10Ohm
R8023 10Ohm
C8015 1000PF/50V
R8017 2.4KOhm
R8016 100Ohm
080527 for load line
C8006 1000PF/50V
C8002 2.2UF/10V
R8020 10Ohm
R8007 0Ohm
13,29 STP_CPU#
3,10 H_DPRSTP#
12 PM_DPRSLPVR
R8010 499Ohm
R8005 499Ohm
071218
080312 for Fsw
R8022 301KOhm
30,58,87 VRM_PWRGD
30,87 CPU_VRON
29 CLK_EN#
R8024 0Ohm
R8027 0Ohm
R8009 0Ohm
VR_PWRGD
CPU_VRON_PWR
R8028 10KOhm
C8003 2.2UF/10V
080526
R8013 6.04KOhm
R8018 6.04KOhm
C8007 0.22UF/16V
CSP
CSN
070822
CE8003 330UF/2V
C8010 0.1UF/16V
JP8005 SHORTPIN

Desktop DiamondVille CPU VID=1.05V

VOL_SEL	VCORE_CNT1	VCORE_CNT2	Voltage
H	H		VID+60mV
L	H		Not allow
H	L		VID=1.2V
L	L		VID-38.5mV

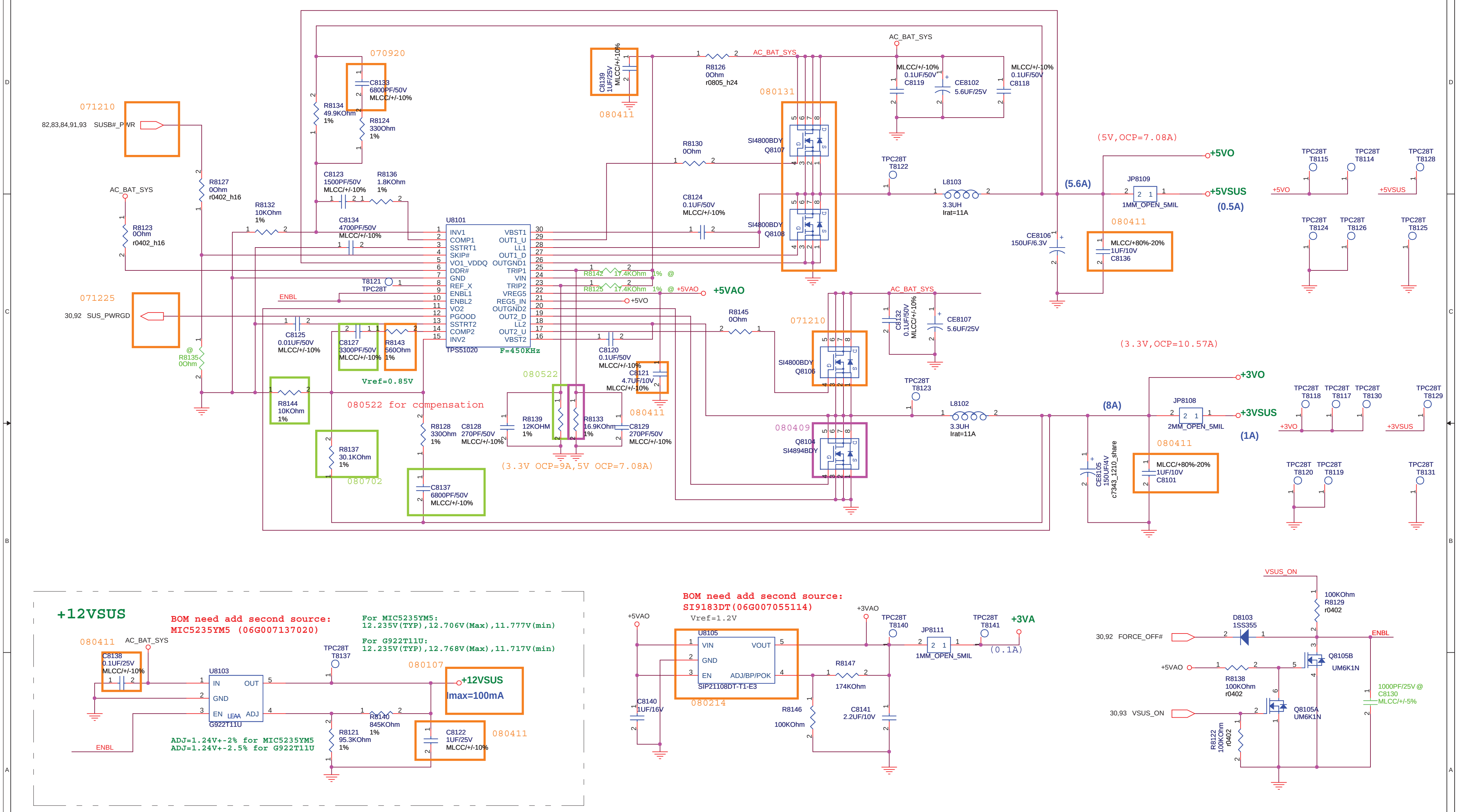
ASUSTek COMPUTER INC. NB6

Title : POWER_+VCORE

Engineer: Benson

Size: Custom | Project Name: N10 | Rev: 1.0

Date: Wednesday, July 02, 2008 | Sheet 80 of 97



070920
071210
82,83,84,91,93 SUSB#_PWR
C8133 6800PF/50V MLCC/+/-10%
R8134 49.9KOhm 1%
R8124 330Ohm 1%
C8139 1UF/25V MLCC/+/-10%
080411
R8126 0Ohm r0805_h24
AC_BAT_SYS
080131
MLCC/+/-10% 0.1UF/50V C8119
CE8102 5.6UF/25V
MLCC/+/-10% 0.1UF/50V C8118
R8127 0Ohm r0402_h16
AC_BAT_SYS
R8123 0Ohm r0402_h16
R8132 10KOhm 1%
C8123 1500PF/50V MLCC/+/-10%
R8136 1.8KOhm 1%
C8134 4700PF/50V MLCC/+/-10%
R8130 0Ohm
SI4800BDY Q8107
C8124 0.1UF/50V MLCC/+/-10%
SI4800BDY Q8108
TPC28T T8122
L8103 3.3UH Irat=11A
(5V,OCP=7.08A)
+5VO
JP8109 1MM_OPEN_5MIL
+5VSUS
(5.6A)
(0.5A)
CE8106 150UF/6.3V
080411
MLCC/+80%-20% 1UF/10V C8136
TPC28T T8115
TPC28T T8114
TPC28T T8128
TPC28T T8124
TPC28T T8126
TPC28T T8125
U8101
INV1 COMP1 SSTRT1 SKIP# VO1_VDDQ DDR# GND REF_X ENBL1 ENBL2 VO2 PGOOD SSTRT2 COMP2 INV2
VBST1 OUT1_U LL1 OUT1_D OUTGND1 TRIP1 VIN TRIP2 VREG5 REG5_IN OUTGND2 OUT2_D LL2 OUT2_U VBST2
TPS51020
F=450KHz
T8121 TPC28T
R8142 17.4KOhm 1% @
R8125 17.4KOhm 1% @ +5VAO
+5VAO
+5VO
R8145 0Ohm
ENBL
071225
30,92 SUS_PWRGD
C8125 0.01UF/50V MLCC/+/-10%
C8127 3300PF/50V MLCC/+/-10%
R8143 560Ohm 1%
C8120 0.1UF/50V MLCC/+/-10%
C8121 4.7UF/10V MLCC/+/-10%
071210
SI4800BDY Q8106
AC_BAT_SYS
C8132 0.1UF/50V MLCC/+/-10%
CE8107 5.6UF/25V
(3.3V,OCP=10.57A)
@ R8135 0Ohm
Vref=0.85V
080522
R8144 10KOhm 1%
080522 for compensation
R8128 330Ohm 1%
C8128 270PF/50V MLCC/+/-10%
R8139 12KOHM 1%
R8133 16.9KOhm 1%
C8129 270PF/50V MLCC/+/-10%
080411
080409
Q8104 SI4894BDY
TPC28T T8123
L8102 3.3UH Irat=11A
+3VO
JP8108 2MM_OPEN_5MIL
+3VSUS
(8A)
(1A)
R8137 30.1KOhm 1%
080702
(3.3V OCP=9A,5V OCP=7.08A)
C8137 6800PF/50V MLCC/+/-10%
CE8105 150UF/4V c7343_1210_share
080411
MLCC/+80%-20% 1UF/10V C8101
TPC28T T8118
TPC28T T8117
TPC28T T8130
TPC28T T8129
TPC28T T8120
TPC28T T8119
TPC28T T8131
+12VSUS
BOM need add second source:
MIC5235YM5 (06G007137020)
For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)
For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)
080411
AC_BAT_SYS
C8138 0.1UF/25V MLCC/+/-10%
U8103
IN OUT GND EN ADJ
G922T11U
TPC28T T8137
080107
+12VSUS
Imax=100mA
R8140 845KOhm 1%
R8121 95.3KOhm 1%
C8122 1UF/25V MLCC/+/-10%
080411
ENBL
ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U
BOM need add second source:
SI9183DT(06G007055114)
Vref=1.2V
+5VAO
U8105
VIN VOUT GND EN ADJ/BP/POK
SIP21108DT-T1-E3
080214
C8140 1UF/16V
+3VAO
TPC28T T8140
JP8111 1MM_OPEN_5MIL
TPC28T T8141
+3VA
(0.1A)
R8147 174KOhm
R8146 100KOhm
C8141 2.2UF/10V
VSUS_ON
100KOhm R8129 r0402
D8103 1SS355
30,92 FORCE_OFF#
ENBL
Q8105B UM6K1N
+5VAO
R8138 100KOhm r0402
1000PF/25V @ C8130 MLCC/+/-5%
30,93 VSUS_ON
Q8105A UM6K1N
R8122 100KOhm r0402

ASUSTek COMPUTER INC. NB6

Title : POWER_SYSTEM

Engineer: Benson

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 81 of 97

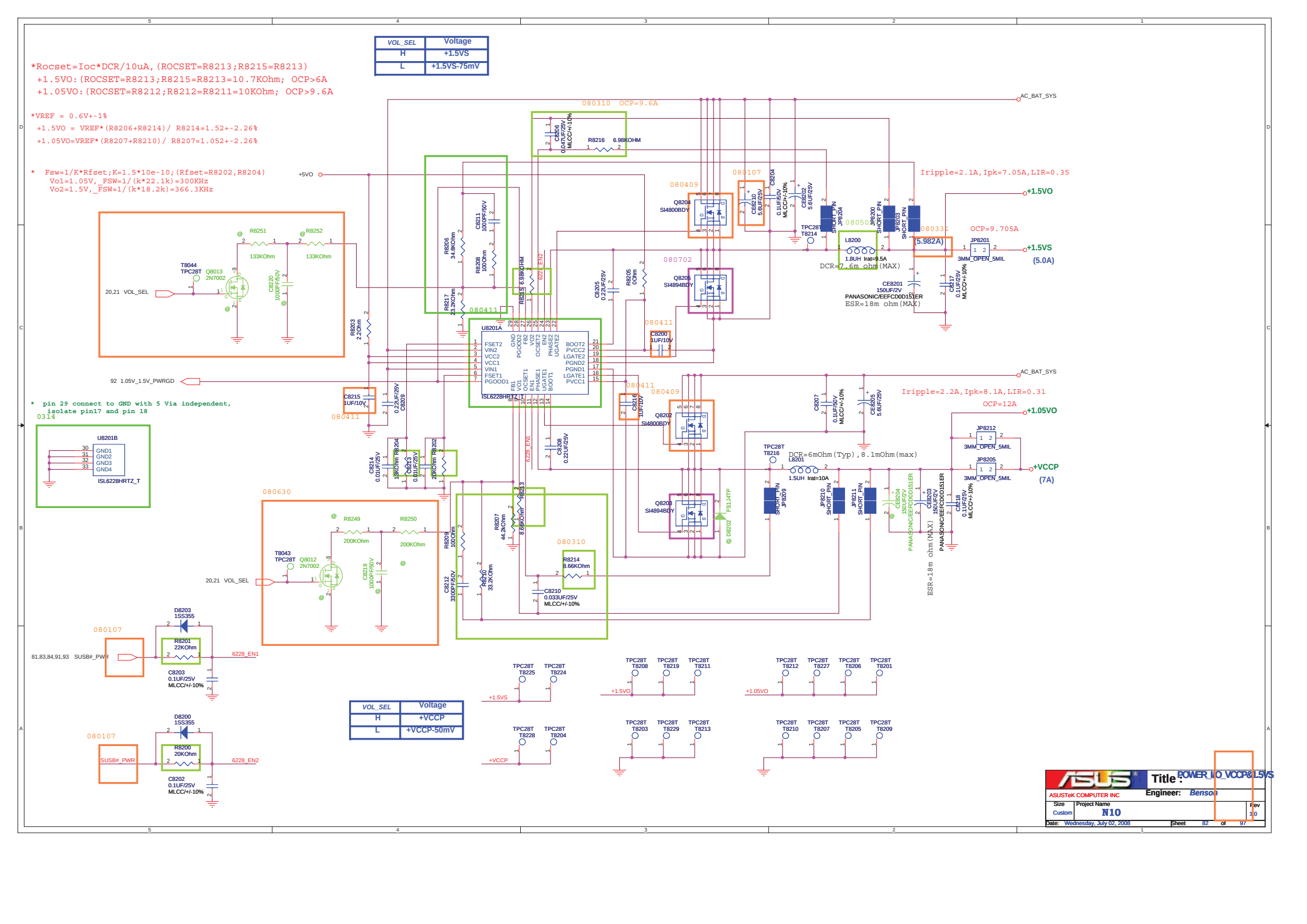
VOL_SEL	Voltage
H	+1.5VS
L	+1.5VS-75mV

*Rocset=Ioc*DCR/10uA,(ROCSET=R8213;R8215=R8213)
+1.5VO:(ROCSET=R8213;R8215=R8213=10.7KOhm; OCP>6A
+1.05VO:(ROCSET=R8212;R8212=R8211=10KOhm; OCP>9.6A

*VREF = 0.6V+-1%
+1.5VO = VREF*(R8206+R8214)/ R8214=1.52+-2.26%
+1.05VO=VREF*(R8207+R8210)/ R8207=1.052+-2.26%

* Fsw=1/K*Rfset;K=1.5*10e-10;(Rfset=R8202,R8204)
Vo1=1.05V,_FSW=1/(k*22.1k)=300KHz
Vo2=1.5V,_FSW=1/(k*18.2k)=366.3KHz

* pin 29 connect to GND with 5 Via independent, isolate pin17 and pin 18



VOL_SEL	Voltage
H	+VCCP
L	+VCCP-50mV

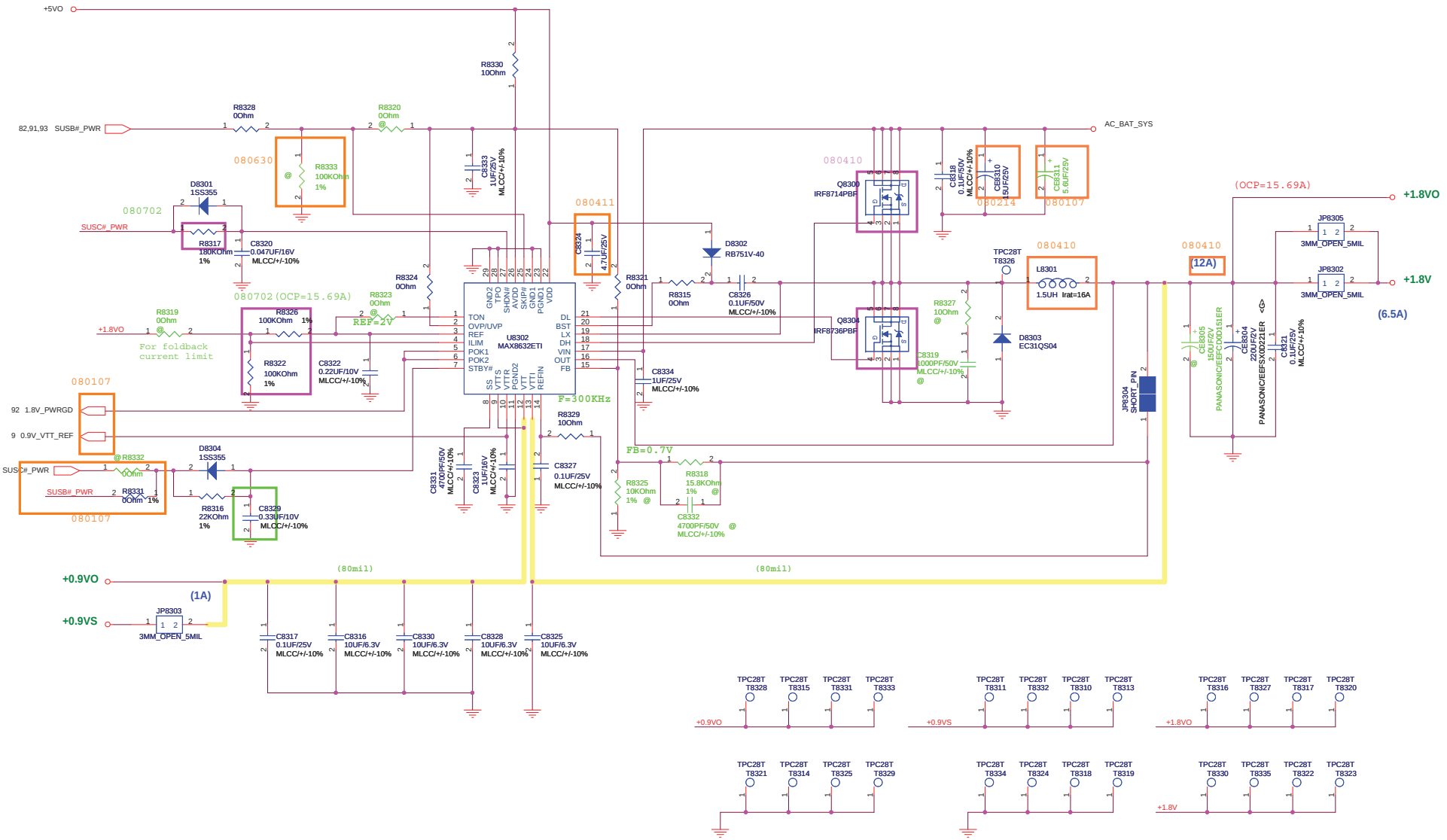
ASUSTeK COMPUTER INC

Title : POWER I/O VCCP&1.5VS

Engineer: Benson

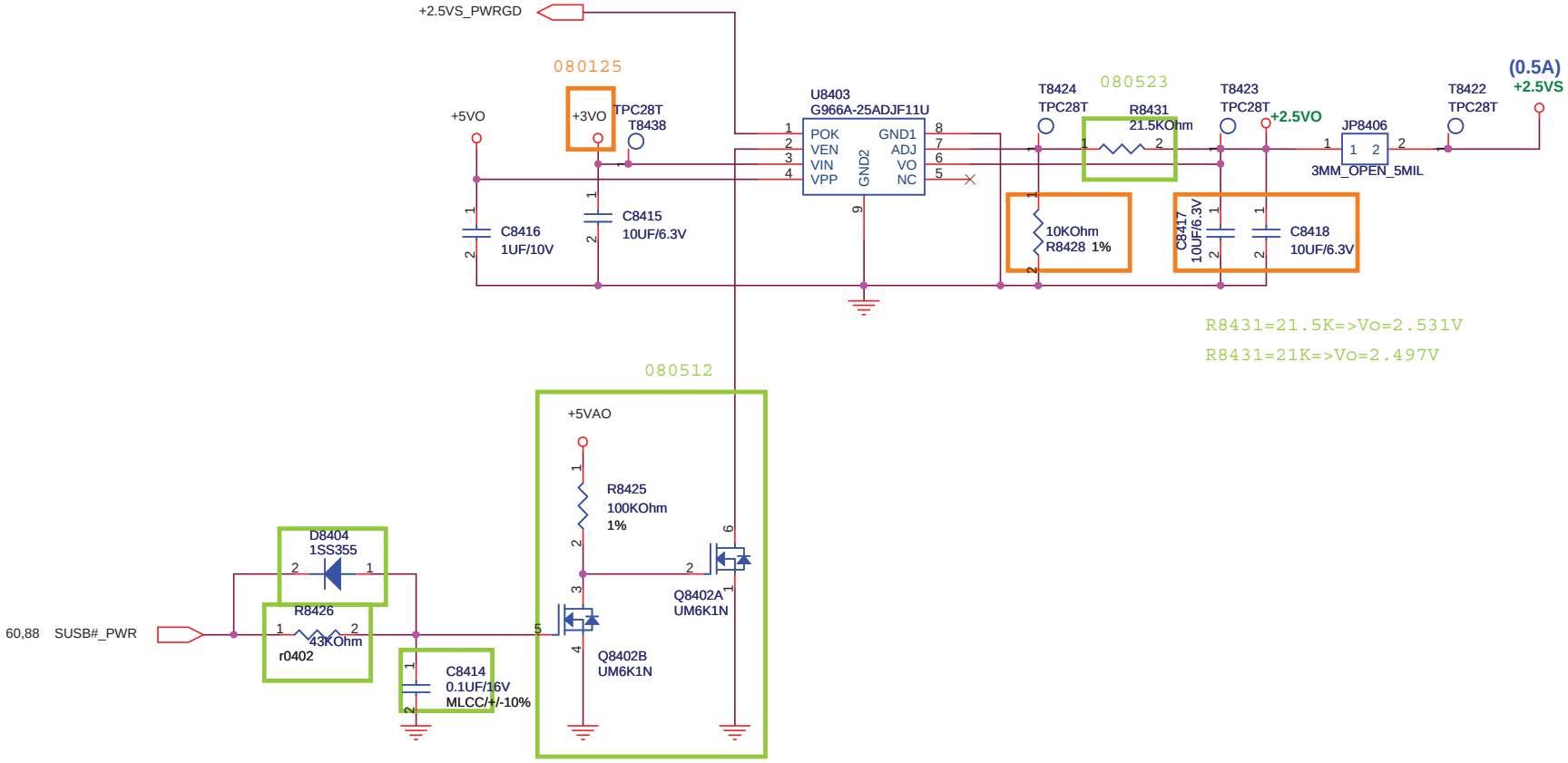
Size: Custom | Project Name: N10 | Rev: 1.0

Date: Wednesday, July 02, 2008 | Sheet 82 of 97

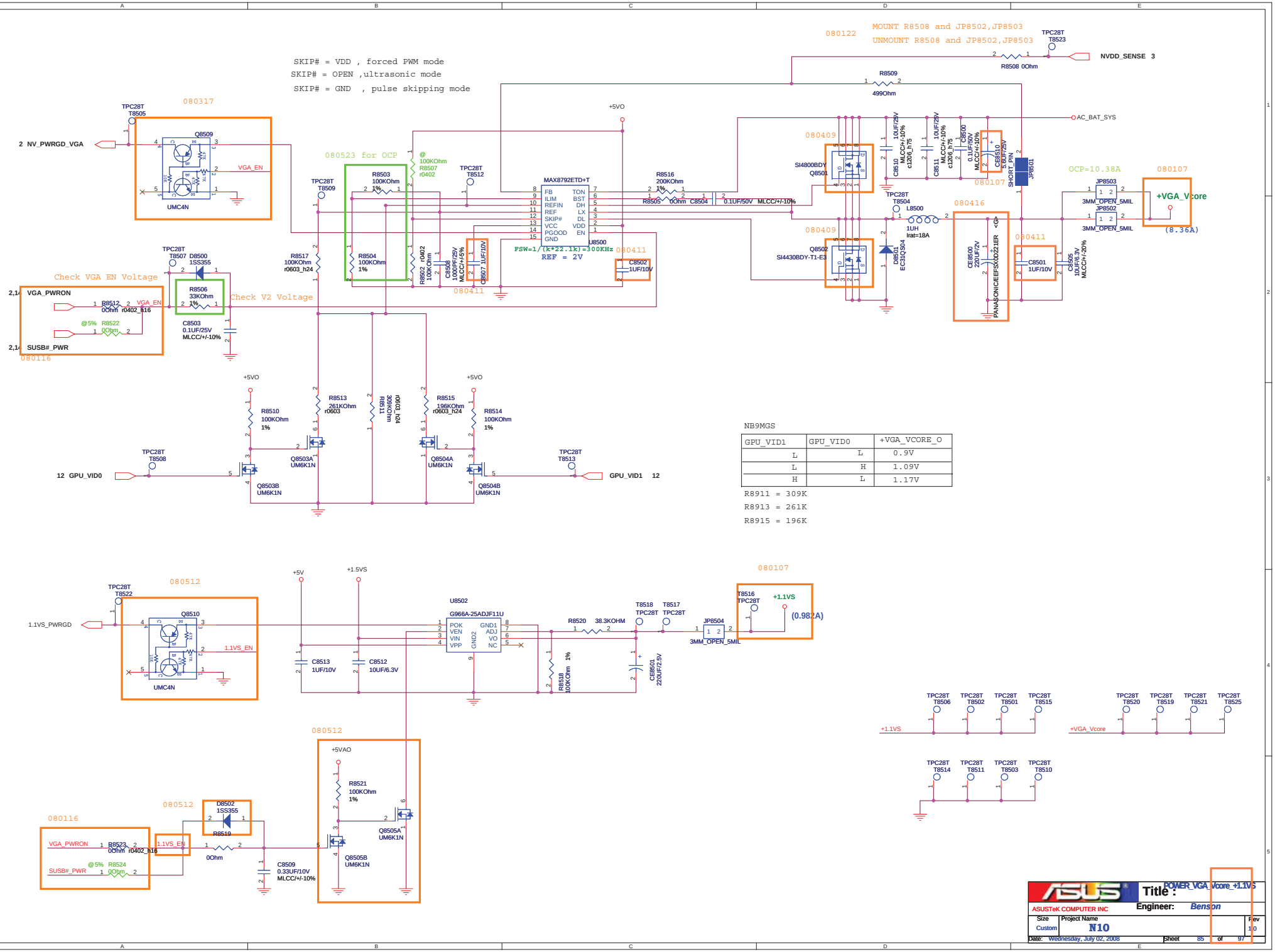


ASUSTeK COMPUTER INC	Title : POWER_IO_1.8V & 0.9VS		
	Engineer: Benson		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 83 of 97		

+2.5VS



ASUSTeK COMPUTER INC	Title : POWER_2.5VS&3VA	
	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 84 of 97	


080122
MOUNT R8508 and JP8502,JP8503
UNMOUNT R8508 and JP8502,JP8503
TPC28T T8523
R8508 0Ohm
NVDD_SENSE 3
SKIP# = VDD , forced PWM mode
SKIP# = OPEN ,ultrasonic mode
SKIP# = GND , pulse skipping mode
R8509 499Ohm
080317
TPC28T T8505
Q8509
2 NV_PWRGD_VGA
VGA_EN
UMC4N
080523 for OCP
@ 100KOhm R8507 r0402
TPC28T T8509
R8503 100KOhm 1%
TPC28T T8512
MAX8792ETD+T
FB ILIM REFIN REF SKIP# VCC PGOOD GND
TON BST DH LX DL VDD EN
U8500
FSW=1/(k*22.1k)=300KHz
REF = 2V
+5VO
R8516 200KOhm 1%
R8505 0Ohm C8504 0.1UF/50V MLCC/+/-10%
080409
SI4800BDY Q8501
SI4430BDY-T1-E3 Q8502
C8510 10UF/25V MLCC/+/-10% c1206_h75
C8511 10UF/25V MLCC/+/-10% c1206_h75
C8500 0.1UF/50V MLCC/+/-10%
CE8510 150UF/25V
SHORT PIN
JP8501
AC_BAT_SYS
OCP=10.38A
080107
JP8503 3MM_OPEN_5MIL
JP8502 3MM_OPEN_5MIL
+VGA_Vcore
(8.36A)
TPC28T T8504
L8500 1UH Irat=18A
080416
D8501 EC31QS04
CE8500 220UF/2V PANASONICEEFSX0D221ER
080411
C8501 1UF/10V
C8525 10UF/6.3V MLCC/+/-20%
TPC28T T8507
D8500 1SS355
Check VGA EN Voltage
Check V2 Voltage
2,14 VGA_PWRON
2,14 SUSB#_PWR
R8512 0Ohm r0402_h16
@5% R8522 0Ohm
R8506 33KOhm 1%
C8503 0.1UF/25V MLCC/+/-10%
080116
R8517 100KOhm r0603_h24
R8504 100KOhm 1%
R8502 r0402 100KOhm
C8508 100PF/25V MLCC/+/-5%
C8507 1UF/10V
C8502 1UF/10V
080411
R8510 100KOhm 1%
R8513 261KOhm r0603
R8515 196KOhm r0603_h24
R8514 100KOhm 1%
Q8503A UM6K1N
Q8504A UM6K1N
Q8503B UM6K1N
Q8504B UM6K1N
TPC28T T8508
TPC28T T8513
12 GPU_VID0
GPU_VID1 12
NB9MGS
GPU_VID1 | GPU_VID0 | +VGA_VCORE_O
L | L | 0.9V
L | H | 1.09V
H | L | 1.17V
R8911 = 309K
R8913 = 261K
R8915 = 196K
080512
TPC28T T8522
Q8510
1.1VS_PWRGD
1.1VS_EN
UMC4N
+5V
+1.5VS
U8502
G966A-25ADJF11U
POK VEN VIN VPP GND2 GND1 ADJ VO NC
C8513 1UF/10V
C8512 10UF/6.3V
R8520 38.3KOHM
R8518 100KOhm 1%
CE8501 220UF/2.5V
T8518 TPC28T
T8517 TPC28T
JP8504 3MM_OPEN_5MIL
080107
T8516 TPC28T
+1.1VS
(0.982A)
080512
+5VAO
R8521 100KOhm 1%
Q8505A UM6K1N
Q8505B UM6K1N
080116
D8502 1SS355
R8519
VGA_PWRON
SUSB#_PWR
R8523 0Ohm r0402_h16
@5% R8524 0Ohm
1.1VS_EN
0Ohm
C8509 0.33UF/10V MLCC/+/-10%
TPC28T T8506
TPC28T T8502
TPC28T T8501
TPC28T T8515
+1.1VS
TPC28T T8520
TPC28T T8519
TPC28T T8521
TPC28T T8525
+VGA_Vcore
TPC28T T8514
TPC28T T8511
TPC28T T8503
TPC28T T8510
ASUSTeK COMPUTER INC
Title : POWER VGA_Vcore +1.1VS
Engineer: Benson
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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Title :	N/A
ASUSTeK COMPUTER INC	Engineer: Benson
Size: A	Project Name: N10
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 86 of 97

Title :	POWER_SHUTDOWN#
ASUSTeK COMPUTER INC	Engineer: Benson
Size: A	Project Name: N10
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 87 of 97

POWER PATH & BAT_LEARN

for delete BAT_LEARN function

120W&90W:R8801=15mOHM(10G21DR01515110)
65W: R8801=20mOHM(10G21DR02015110)

080214 Snubber

1.10 Ohm,0.1uF/50V(p)
2.4.7Ohm,1uF/50V(s)
3.10 Ohm,1uF/50V

080512

(240mV/15mOhm)*VSET/4.2V=ICHG=2.5A--->VSET=0.655

EC not ready OK--->R8836 unmount,others mount

EC ready OK--->unmount R883S.R8830.Q8806.R8844.Q8807.Q8808; mount R8836

120W: R8832 = 1.82K
90W: R8832 = 6.98K
65W: R8832 = 17.8K

AC_BAT_SYS_INV to inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [60mV/Rsense(ADin)]*[1+(Rb/Ra)]
Rsense(ADin)=20m ohm
Ra=R8822=17.8K ohm,Rb=R8843=1K ohm
=> Iin(max)=3.168A
=> Constant Power = 19V * 3.168A = 60.2W

Charge Current Ichg = [240mV/Rsense(CHG)]*[VISET/VAA]
Rsense(CHG)=R8842=10m ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Precgarge current=150mA

2.4V<VCTL<4.2V=>3cell=>Vcell =4.2V+(4.2V-VVCTL)/6
3 cell=>VCTL= 3.9V => Vcell = 4.635V
0V<VCTL<1.8V=>4cell=>Vcell =4.2V+(VVCTL/6)
4 cell=>VCTL= 0.3V => Vcell = 4.635V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

VCTL = 3.9V; CHG VOLTAGE = 4.25/CELL(3 CELL)

MAX17005=>R8831=1MOhm(@)
MAX17015=>R8831=0 Ohm

MAX17015 change MAX17005 List
R8820=100K 0.1%--->0 ohm
R8826=20K 0.1%--->@
R8831=0 ohm--->1.69M ohm
R8833=@--->130K ohm

080512

EC ready OK--->R8821=20KOhm,
R8826=20KOhm,R8823=49.9KOHM

EC not ready OK--->unmount 8821=20KOhm,
R8826=20KOhm,R8823=100KOHM

BAT=2.1V===>BAT=12.6V

Title : POWER_CHARGER			
<OrgName>	Engineer: Benson		
Size: Custom	Project Name: M10		Rev: 1.0
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ASUSTeK COMPUTER INC	Title : N/A Engineer: Benson	
Size: A	Project Name: N10	Rev: 1.0
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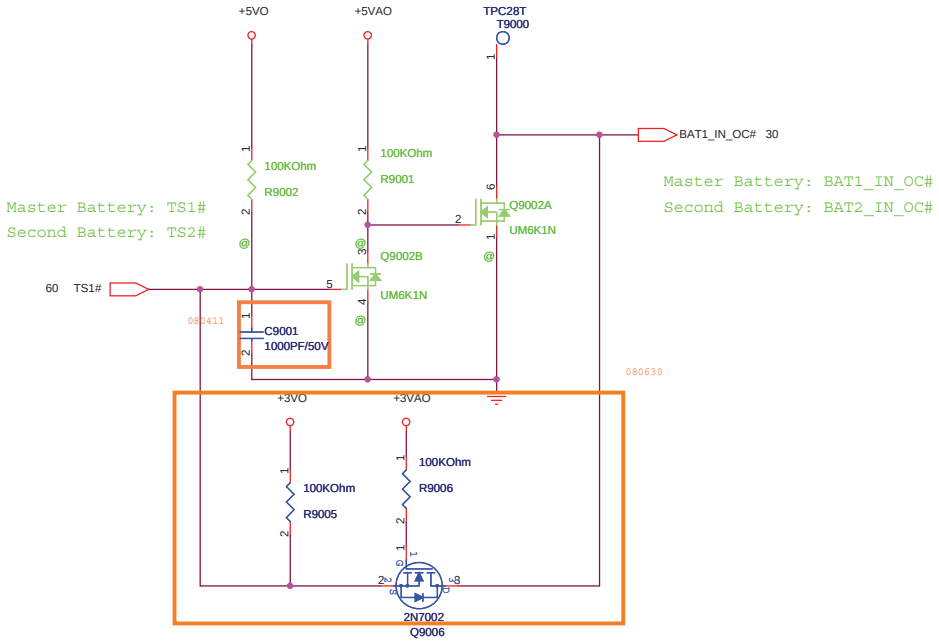
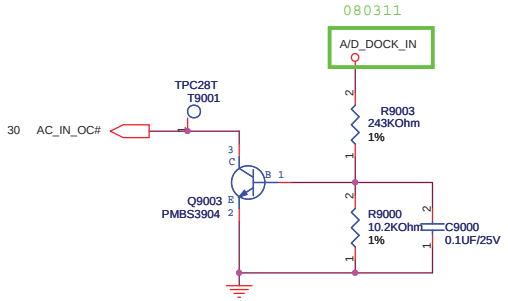
BATTERY IN DETECT



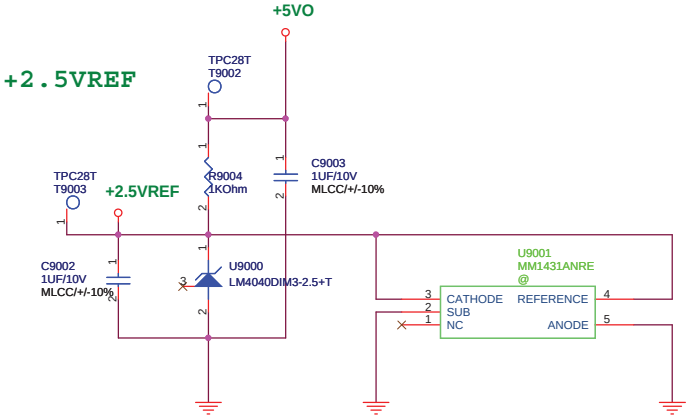
Master Battery: TS1#
Second Battery: TS2#

Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

ADAPTER IN DETECT



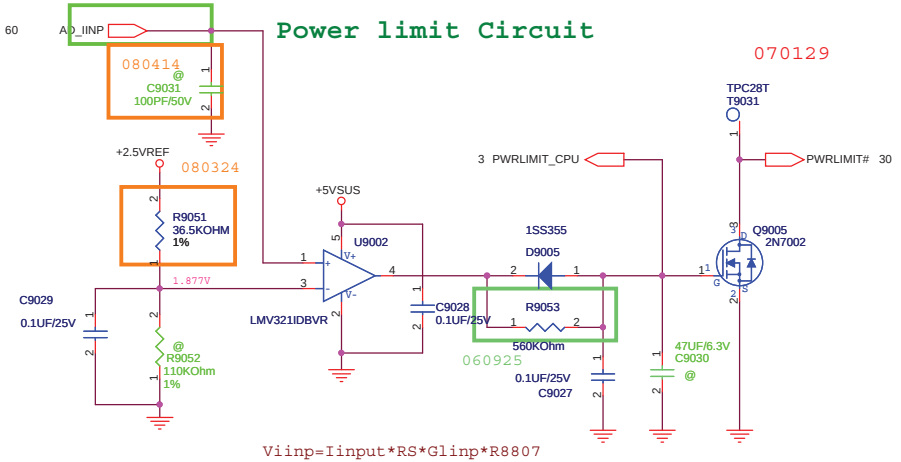
+2.5VREF



U8600 & U8601 colay

U8600 Main source change to 06G006002414(tolerence:1%).
Add second source 06G006002610 (tolerence:1%),
06G006002412 (tolerence:0.2%) and
06G006002020(tolerence:0.2%)

Power limit Circuit



Viinp=Iinput*RS*Glinp*R8807
Viinp=1.877V, RS=20mohm,
Glinp=2.8uA/mV,Pinput=63.65W

R8839=10K----->Iinput=3.35A

ASUSTeK COMPUTER INC	Title : POWER_DETECT	
	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
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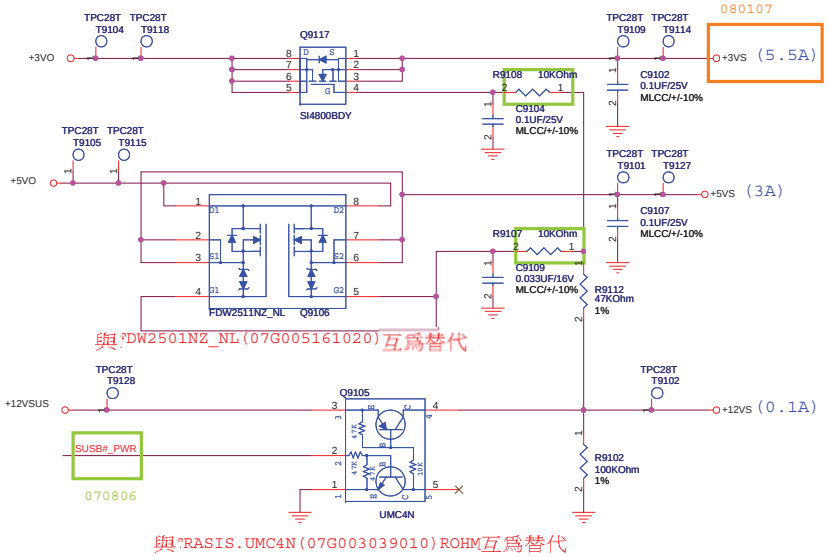
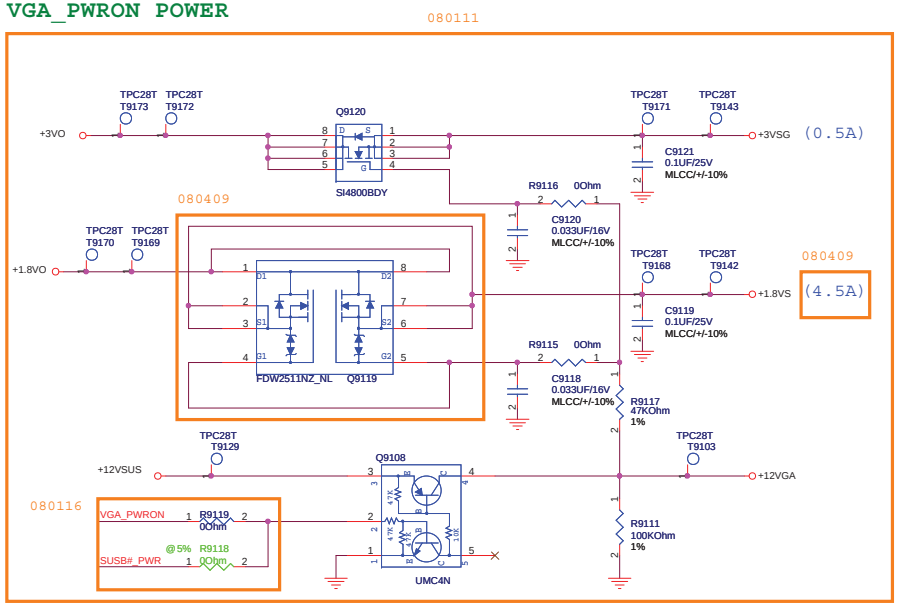
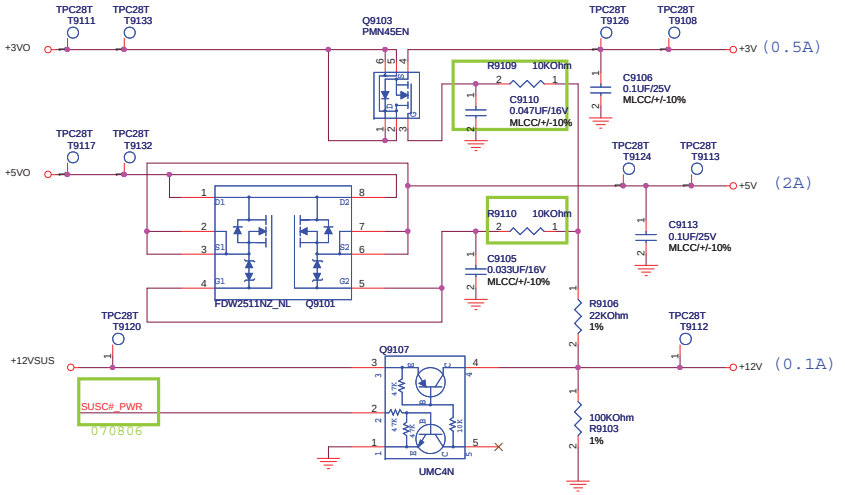
SUSB#_PWR POWER

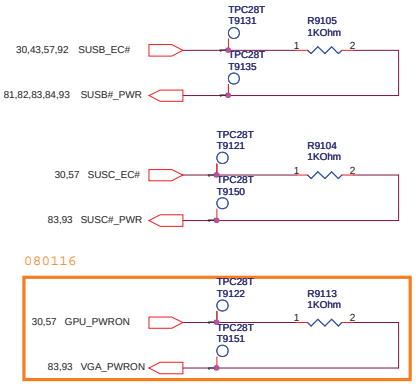


VGA_PWRON POWER



SUSC#_PWR POWER





ASUSTeK COMPUTER INC	Title : POWER_LOAD SWITCH	
	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
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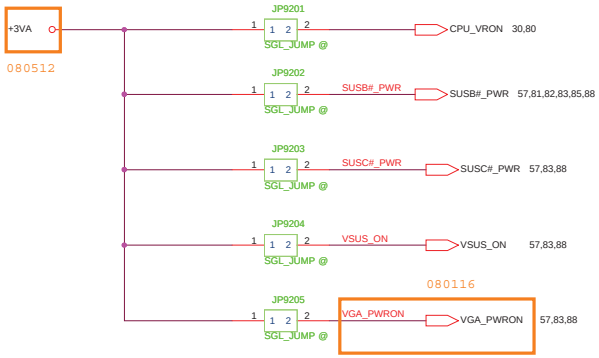
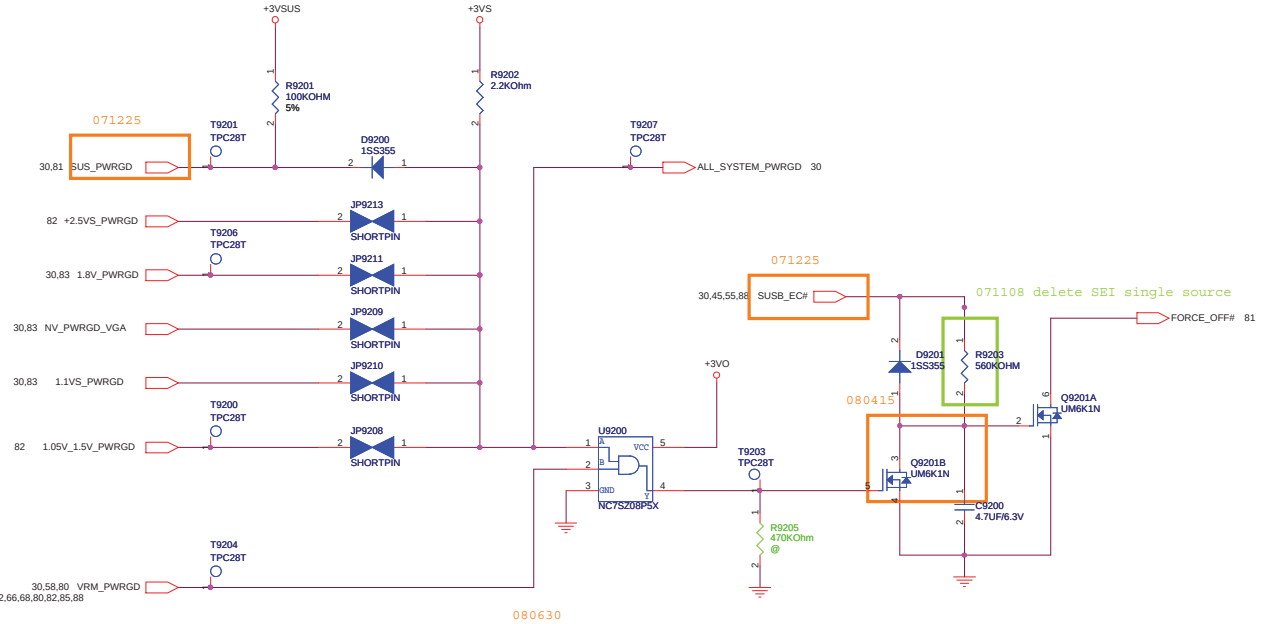
FOR POWER TEST



AC_BAT_SYS	AC_BAT_SYS	80,81,82,83,84
BAT	BAT	60,84
BAT_CON	BAT_CON	60,84
+3VA	+3VA	12,30,57,85,86
+5VO	+5VO	81,82,83,85,88
+5VSUS	+5VSUS	56,62,81
+3VO	+3VO	53,81,88
+3VSUS	+3VSUS	30,37,81
+5V	+5V	9,14,39,52,56,57,65,69,88
+5VS	+5VS	14,36,37,45,48,50,56,57,61,62,69,80,82,88
+3V	+3V	13,14,30,45,52,54,57,62,65,88
+3VS	+3VS	7,12,13,14,29,30,35,36,37,42,44,45,48,50,51,53,54,55,56,57,58,61,62,66,68,80,82,85,88
+12V	+12V	48,57,66,81
+12VS	+12VS	48,57,66,81
+2.5VS	+2.5VS	48,57,66,81
+1.8VO	+1.8VO	83
+1.8V	+1.8V	7,9,11,14,57,83,85
+1.8VS	+1.8VS	7,9,11,14,57,83,85
+0.9VS	+0.9VS	7,9,11,83
+VCCP	+VCCP	4,10,13,14,29,53,57,85
+1.05VO	+1.05VO	82
+1.5VS	+1.5VS	4,10,13,14,29,53,57,85
+VCORE	+VCORE	4,80
+VGA_Vcore	+VGA_Vcore	4,10,13,14,29,53,57,85
+1.1VS	+1.1VS	60,84
GPU_VID0	GPU_VID0	60,84
GPU_VID1	GPU_VID1	60,84
NVDD_SENSE	NVDD_SENSE	60,84

POWER GOOD DETECTER



R2.0 080331 Add Q9201, R9204 and un-mount U9200 for cost down with R9209 change from 100kohm to 10 kohm
080401 Change Q9201 from 2N7002 to BSS138.
080402 Un-Mount Q9201 and R9204, mount U9200. Recover R9209 from 10Kohm to 100Kohm

ASUSTeK COMPUTER INC	Title : Power_PROTECT_SIGNA		
	Engineer: Benson		
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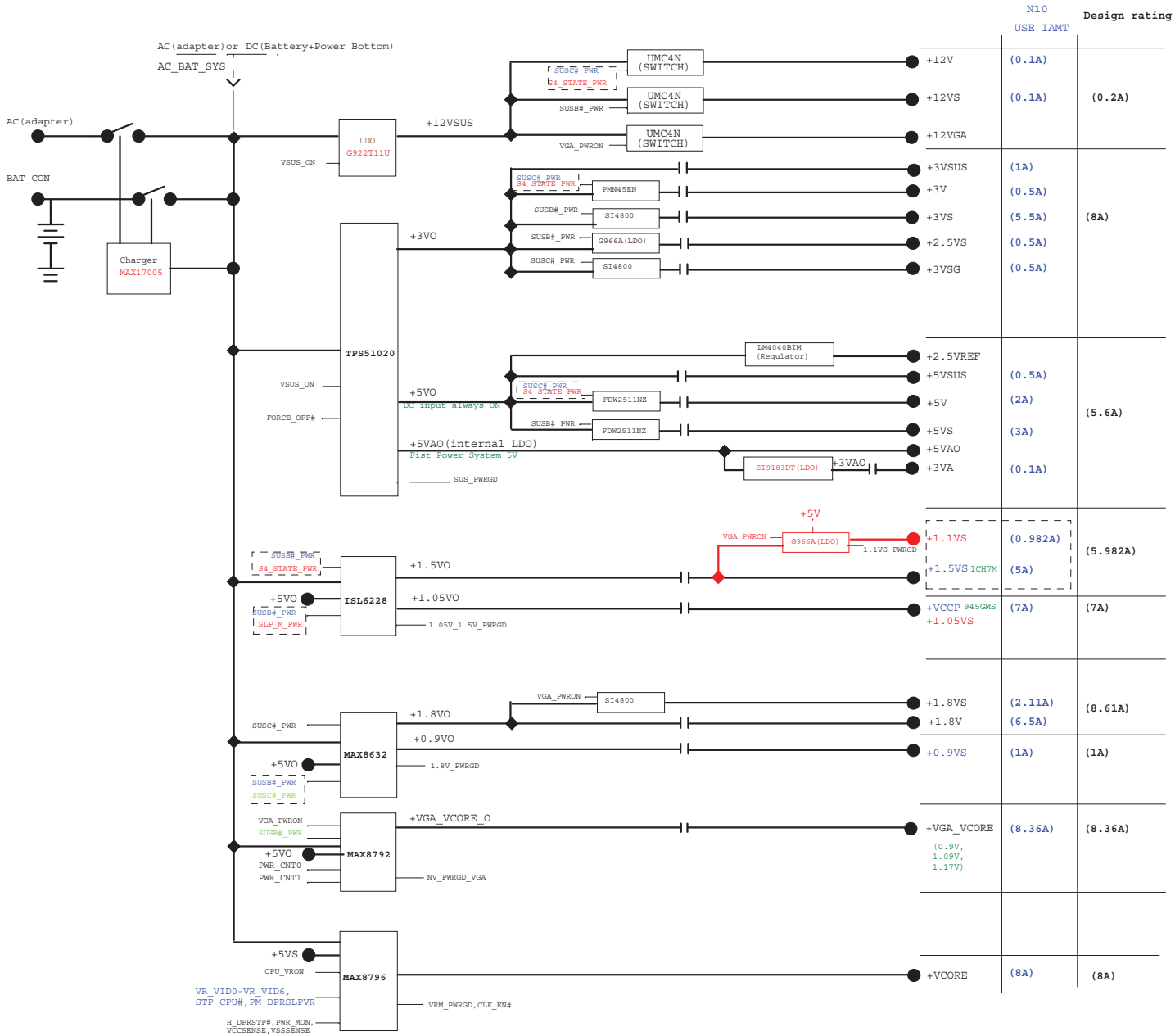

ASUSTeK COMPUTER INC

Title : POWER_FLOWCHART

Engineer: Benson

Size: Custom | Project Name: N10 | Rev: 1.0

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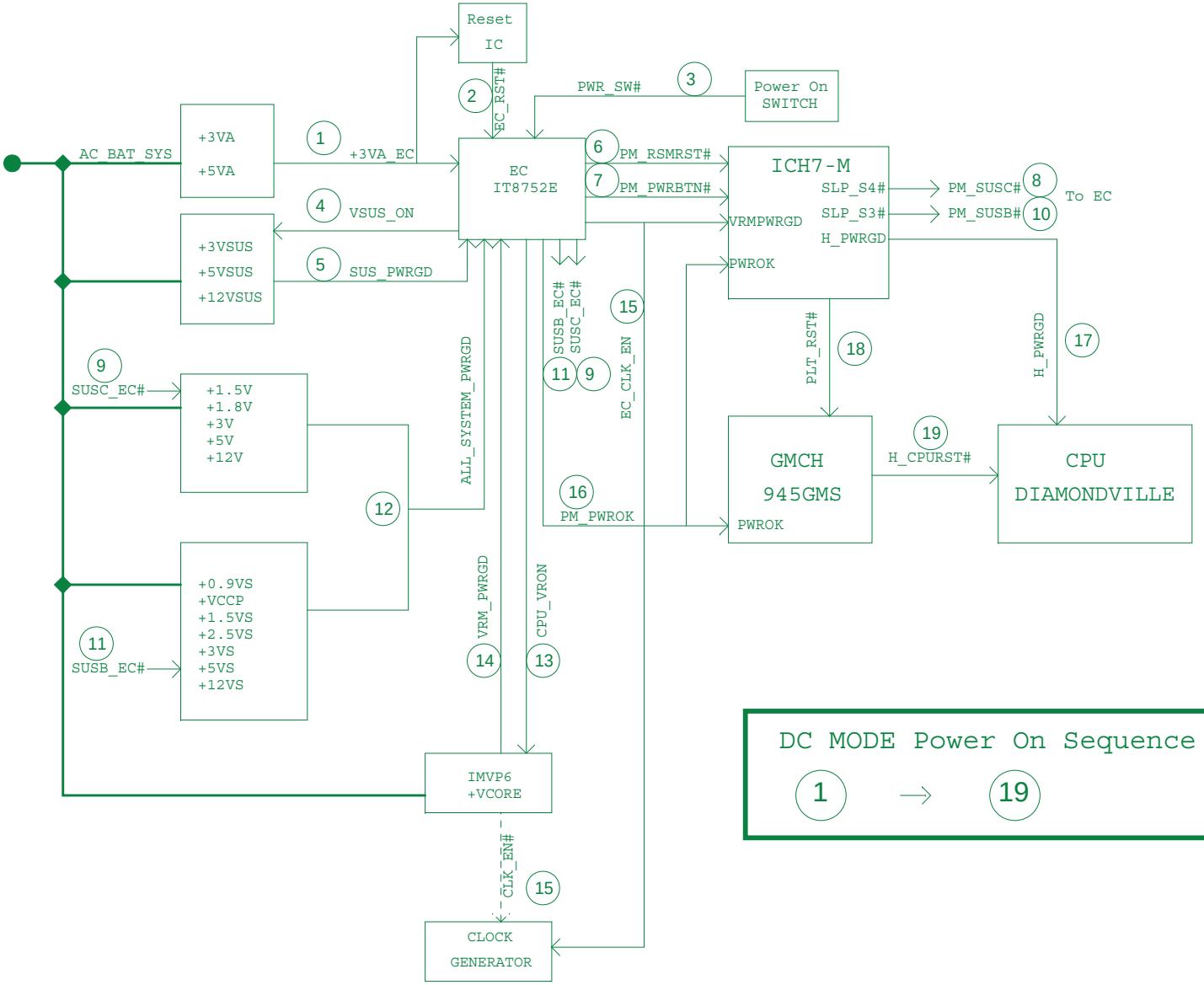
N10 POWER-ON SEQUENCE UNDER BATTERY MODE



1. Battery is plugged in only and +3VA_EC is on
2. EC_RST# is de-asserted
3. Power button is pressed
4. EC asserts VSUS_ON to turn SUS power on
5. SUS_PWRGD is asserted to indicate SUS power is OK
6. EC de-asserts PM_RSMRST# to reset RTC well of ICH7M
7. EC asserts PM_PWRBTN# to ICH7M from G2 to G0
8. ICH7M de-asserts PM_SUSC# to EC
9. EC de-asserts SUSC_EC# to turn +V power on
10. ICH7M de-asserts PM_SUSB# to EC
11. EC de-asserts SUSB_EC# to turn +VS power on
12. EC waits for ALL_SYSTEM_PWRGD
13. EC asserts CPU_VRON to turn CPU power on
14. EC waits for VRM_PWRGD
15. EC asserts EC_CLK_EN to enable clock generator
16. EC asserts PM_PWROK to 945GMS and ICH7M
17. ICH7M asserts H_PWRGD to CPU
18. ICH7M asserts PLT_RST# to reset 945GMS
19. 945GMS asserts H_CPURST# to reset CPU

DC MODE Power On Sequence

1 → 19

ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	
	Engineer: ENGINEER	
Size: C	Project Name: N10	Rev: 0.1
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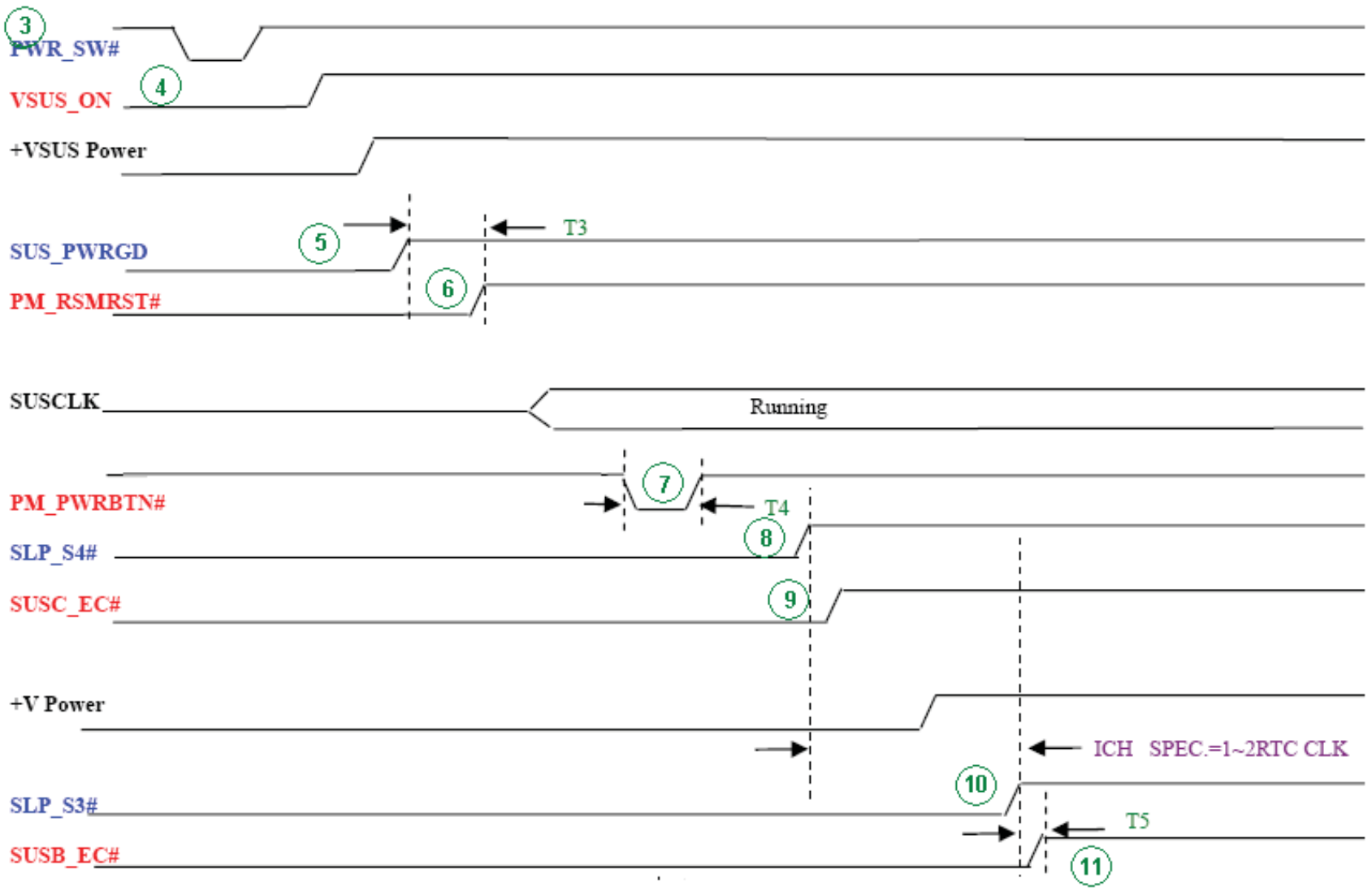
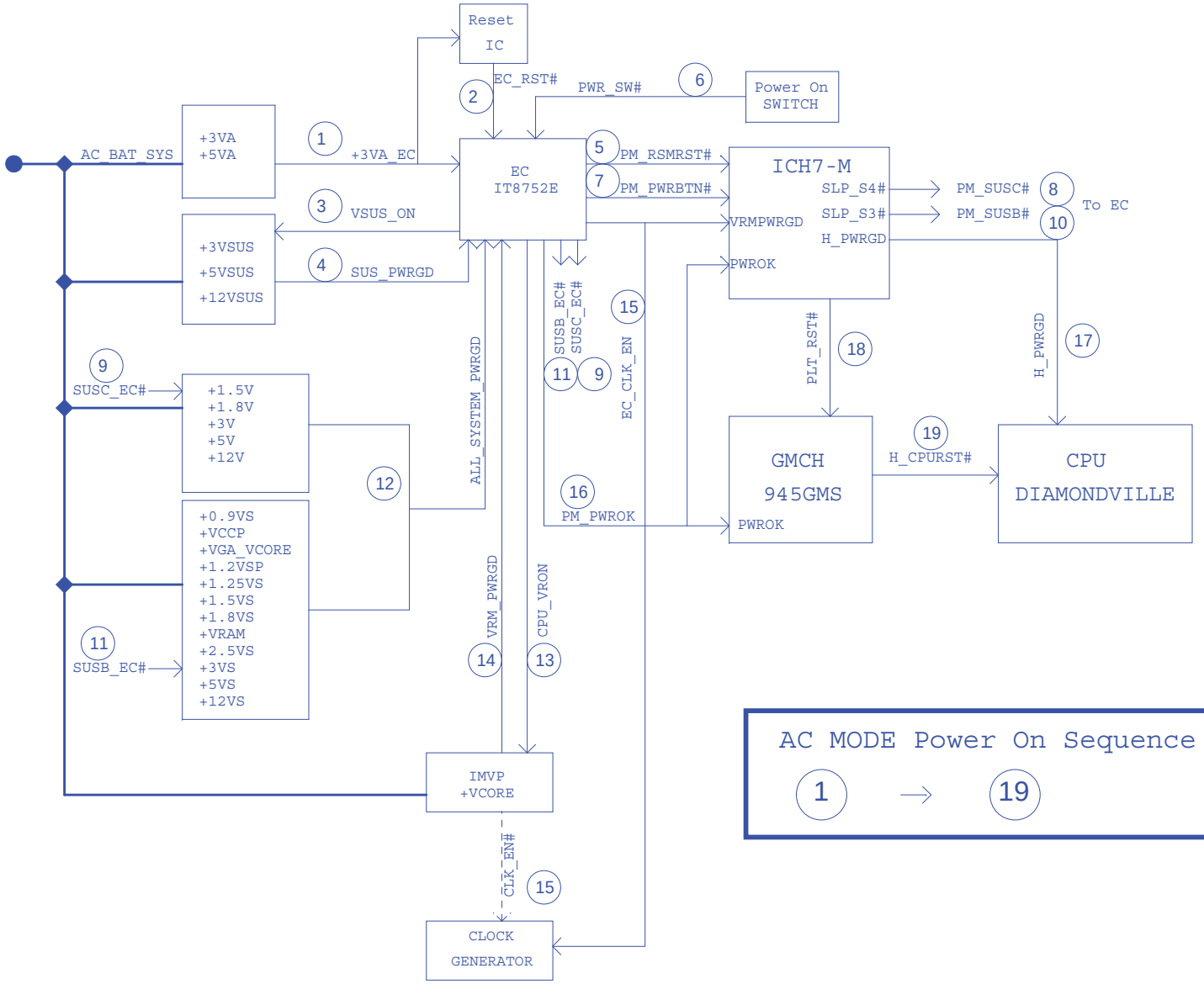


ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 0.1
Date: Wednesday, July 02, 2008	Sheet 95 of 97	

N10 POWER-ON SEQUENCE UNDER BATTERY MODE



1. Battery is plugged in only and +3VA_EC is on
2. EC_RST# is de-asserted
3. Power button is pressed
4. EC asserts VSUS_ON to turn SUS power on
5. SUS_PWRGD is asserted to indicate SUS power is OK
6. EC de-asserts PM_RSMRST# to reset RTC well of ICH7M
7. EC asserts PM_PWRBTN# to ICH7M from G2 to G0
8. ICH7M de-asserts PM_SUSC# to EC
9. EC de-asserts SUSC_EC# to turn +V power on
10. ICH7M de-asserts PM_SUSB# to EC
11. EC de-asserts SUSB_EC# to turn +VS power on
12. EC waits for ALL_SYSTEM_PWRGD
13. EC asserts CPU_VRON to turn CPU power on
14. EC waits for VRM_PWRGD
15. EC asserts EC_CLK_EN to enable clock generator
16. EC asserts PM_PWROK to 945GMS and ICH7M
17. ICH7M asserts H_PWRGD to CPU
18. ICH7M asserts PLT_RST# to reset 945GMS
19. 945GMS asserts H_CPURST# to reset CPU

AC MODE Power On Sequence

1 → 19

ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	
	Engineer: ENGINEER	
Size: C	Project Name: N10	Rev: 0.1
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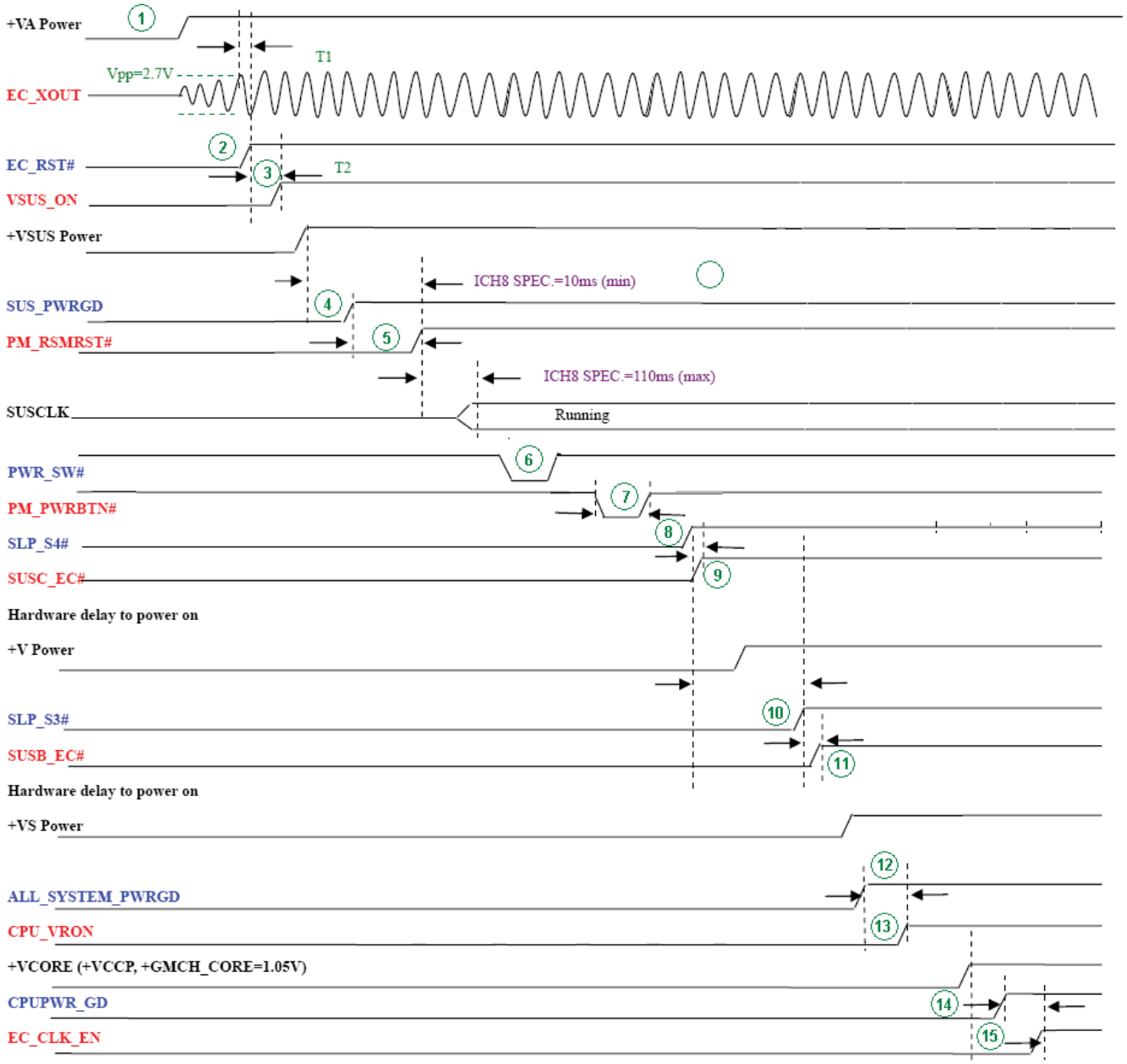

ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	
	Engineer: ENGINEER	
Size: B	Project Name: N10	Rev: 0.1
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