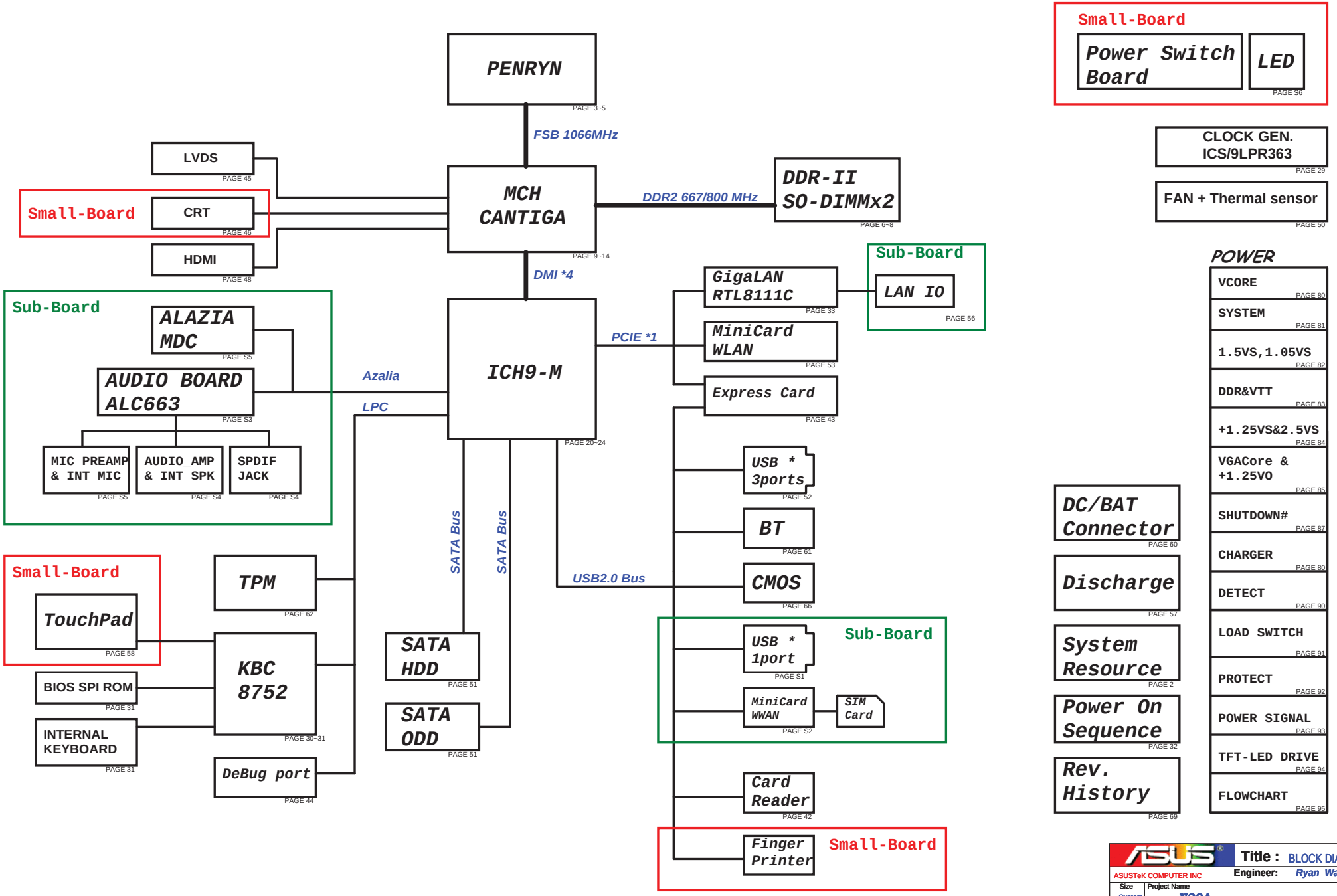
N20A: PENRYN/CANTIGA/ICH9-M BLOCK DIAGRAM



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 02, 2008	Sheet 1 of 101	

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44	Debug
45	LVDS & INVERTER CONNECTOR
46	CRT
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50	THER SENSOR & FAN
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52	USB Port x 4
53	MINICARD(Ebron/Robson/3G/TV)
54	PORT Docking
55	Super I/O & FIR
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58	UMB
60	DC power jack, Batter conn.
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62	TPM
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80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.5V & 1.05VM
83	POWER_I/O_DDR & VTT
84	NONE
85	POWER_VGA_VCORE & 1.1VO
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

GPIO33 Internal Pull High, Go Low= Flash Descriptor Security will be overriden

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]# EXT PU	+5VS
GPIO 06	GPI	- EXT PU	+3VS
GPIO 07	GPI	- EXT PU	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	SUS_PWR_ACK EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	- INT PD*	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	NEWCARD_OC#	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	**+3VS**
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	LINKALERT#	+3VSUS

INT PU*: PU or PD in special time

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	

ASUSTeK COMPUTER INC. NB1

Title : Schematic Information

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

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Reserved for the S3 reboot issue

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

Zo=55 Ohm, 0.5" max for GTL_REF

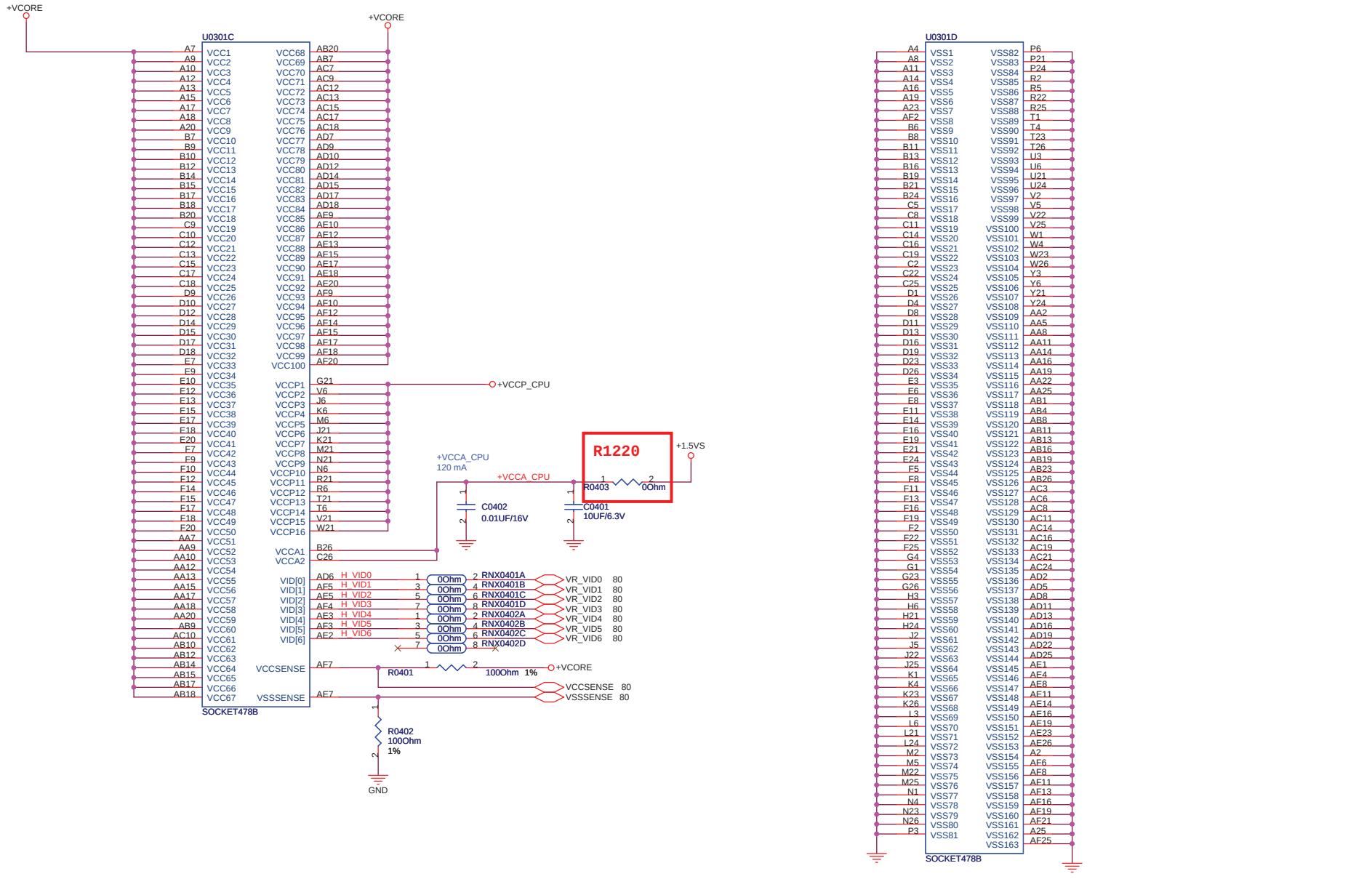
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Default Strapping When Not Used

Place R0304 & R0306 for XDP function

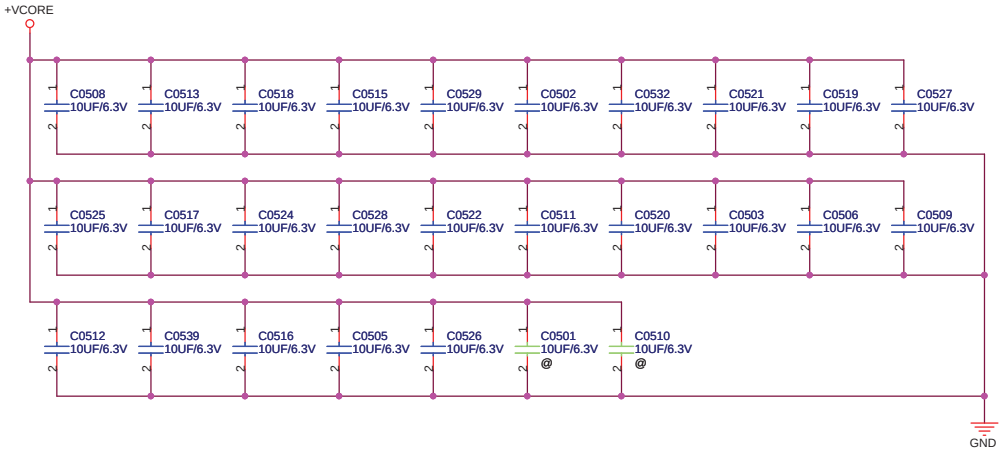
R1215

Title :	CLOCK GEN-ICS9LPR363
ASUSTeK COMPUTER INC. NB1	Engineer: Ryan_Wang
Size: Custom	Project Name: N20A
Rev: 1.20	
Date: Monday, June 02, 2008	Sheet 3 of 101

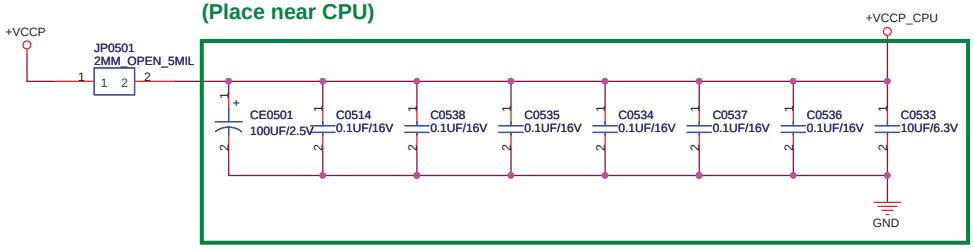


ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn(2)		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 02, 2008	Sheet 4 of 101		

38A for Penryn



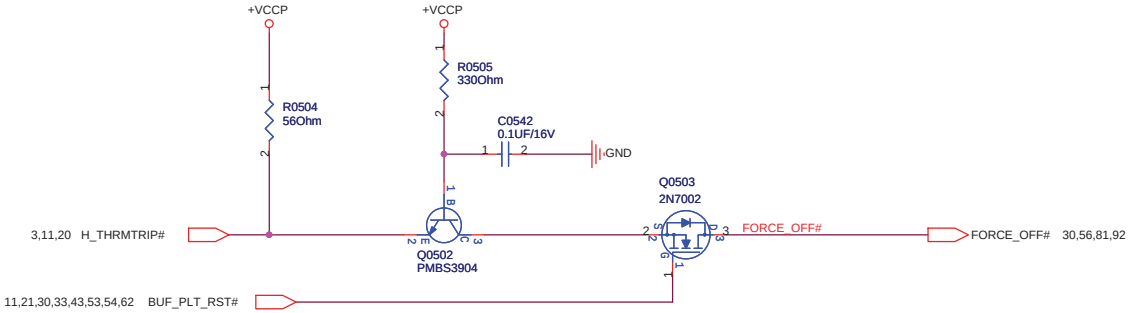
+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from Intel

CORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

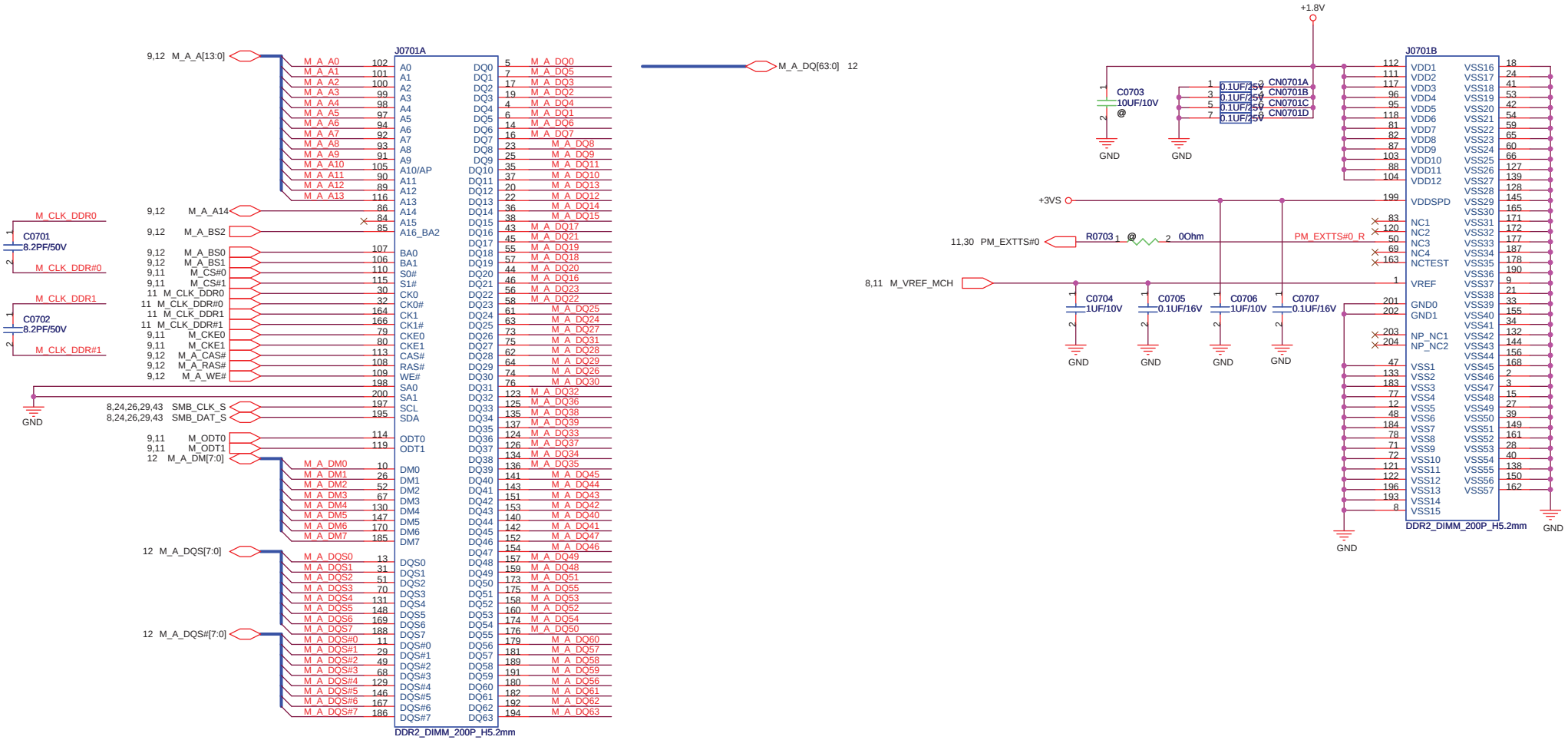
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
F3S: 10UF *16
A7S: 10UF *10 ....11/17
V1V: ?
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
F3S: 100UF *1, 0.1UF *4
V1V: ?



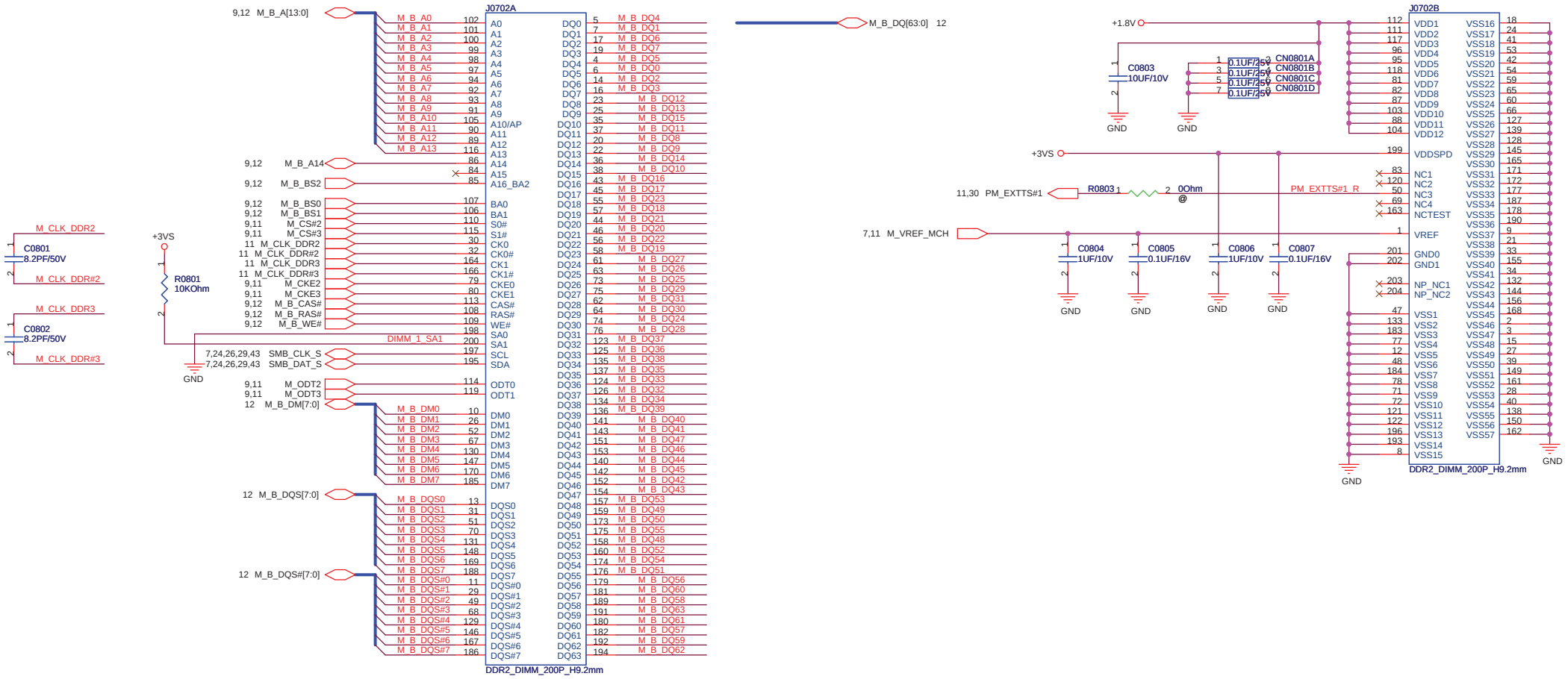
Thermal Trip signal (From CPU to ICH-9M and sequence)

ASUSTeK COMPUTER INC. NB1		Title : CPU CAPS	
		Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 02, 2008		Sheet 5 of 101	

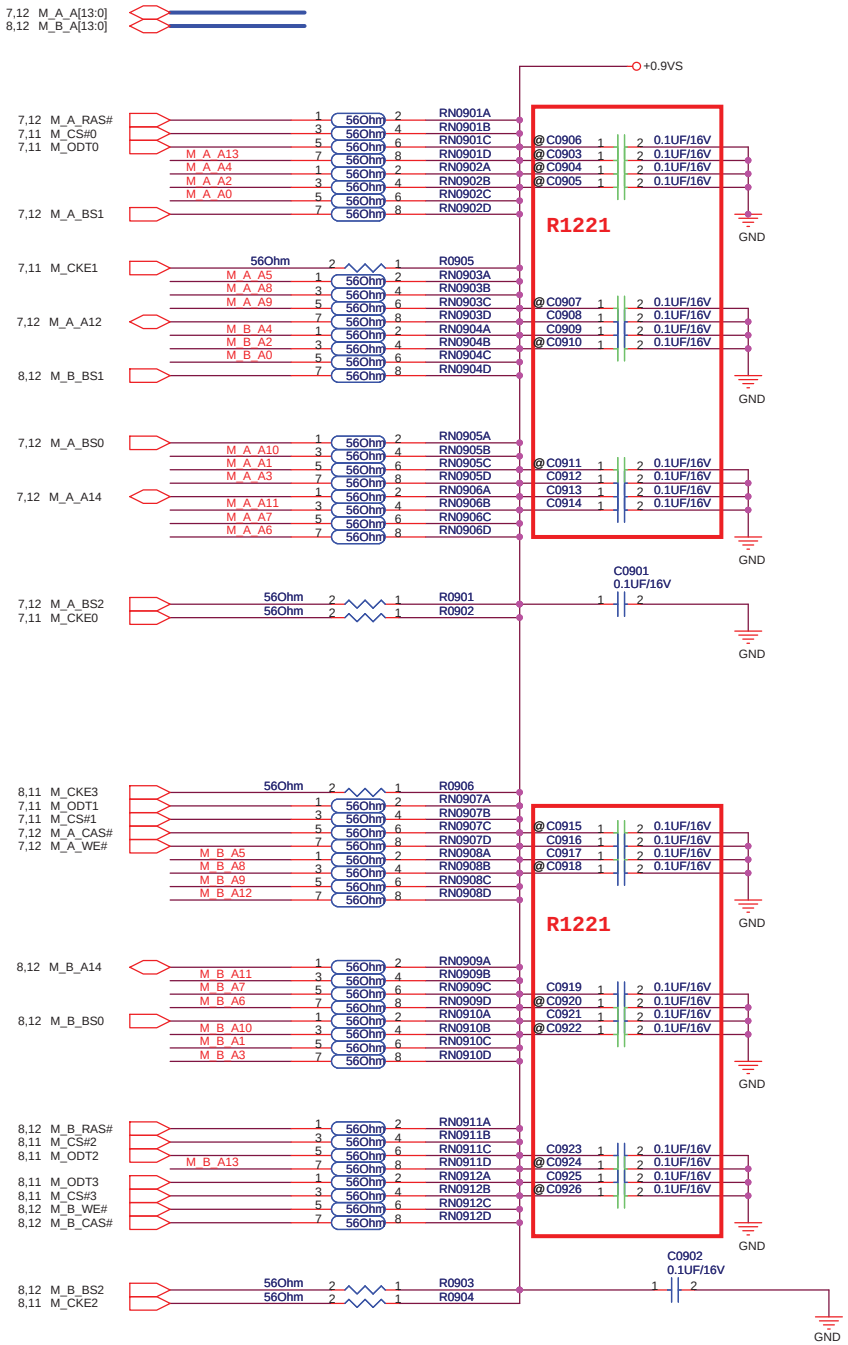
Title :	CPU CAPS
ASUSTeK COMPUTER INC. NB1	Engineer: Ryan_Wang
Size: Custom	Project Name: N20A
Rev: 1.20	
Date: Monday, June 02, 2008	Sheet 6 of 101



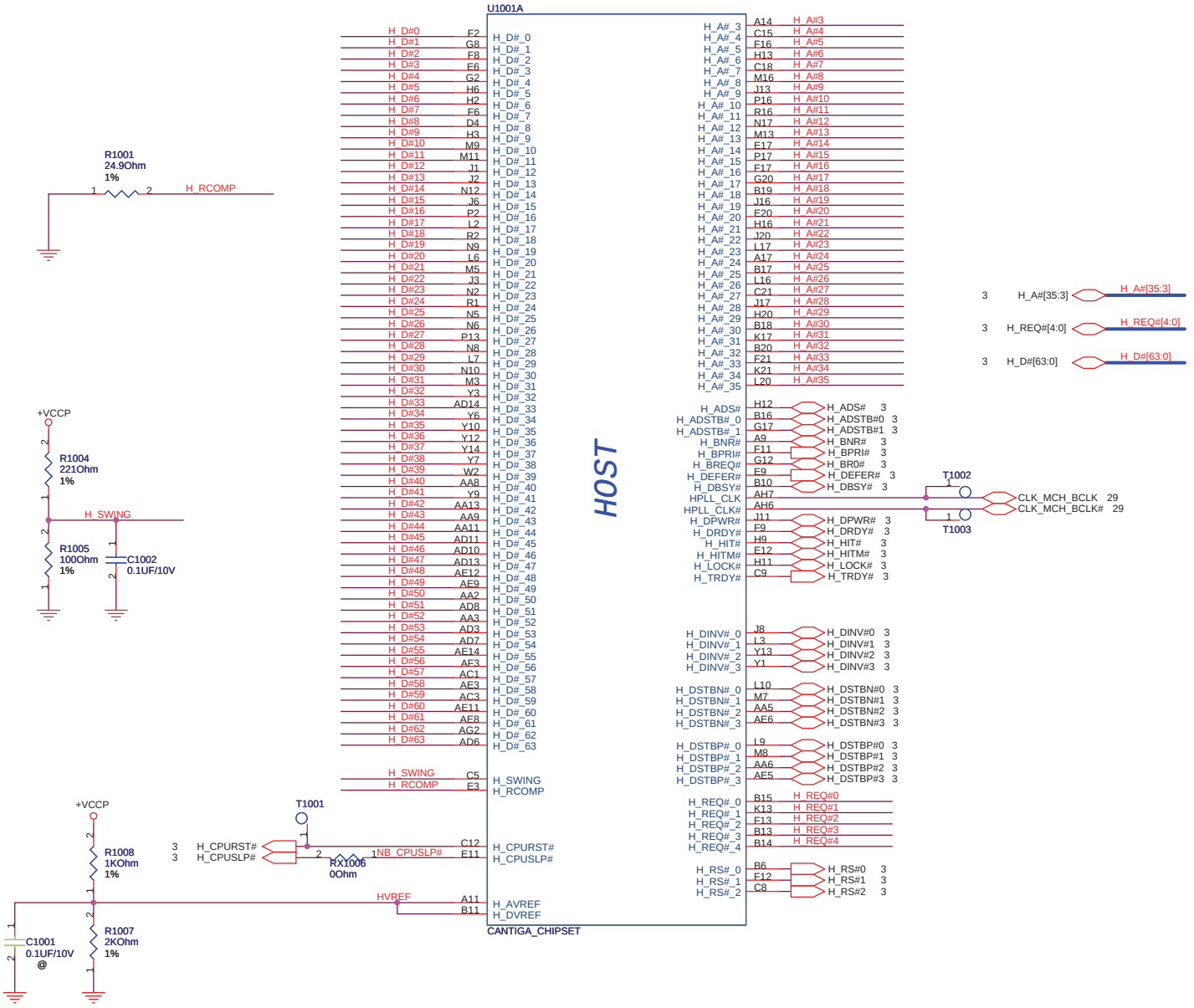
ASUSTeK COMPUTER INC	Title : SO-DIMM0 (1/3)		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 02, 2008	Sheet 7 of 101		



ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM_1	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 02, 2008	Sheet 8 of 101	



ASUSTeK COMPUTER INC. NB1	Title DDR2 termination	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 02, 2008	Sheet 9 of 101	



Cap 0.1uF within 100 mils from GMCH

ASUSTeK COMPUTER INC. NB1	Title : Cantiga -- CPU (1)	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
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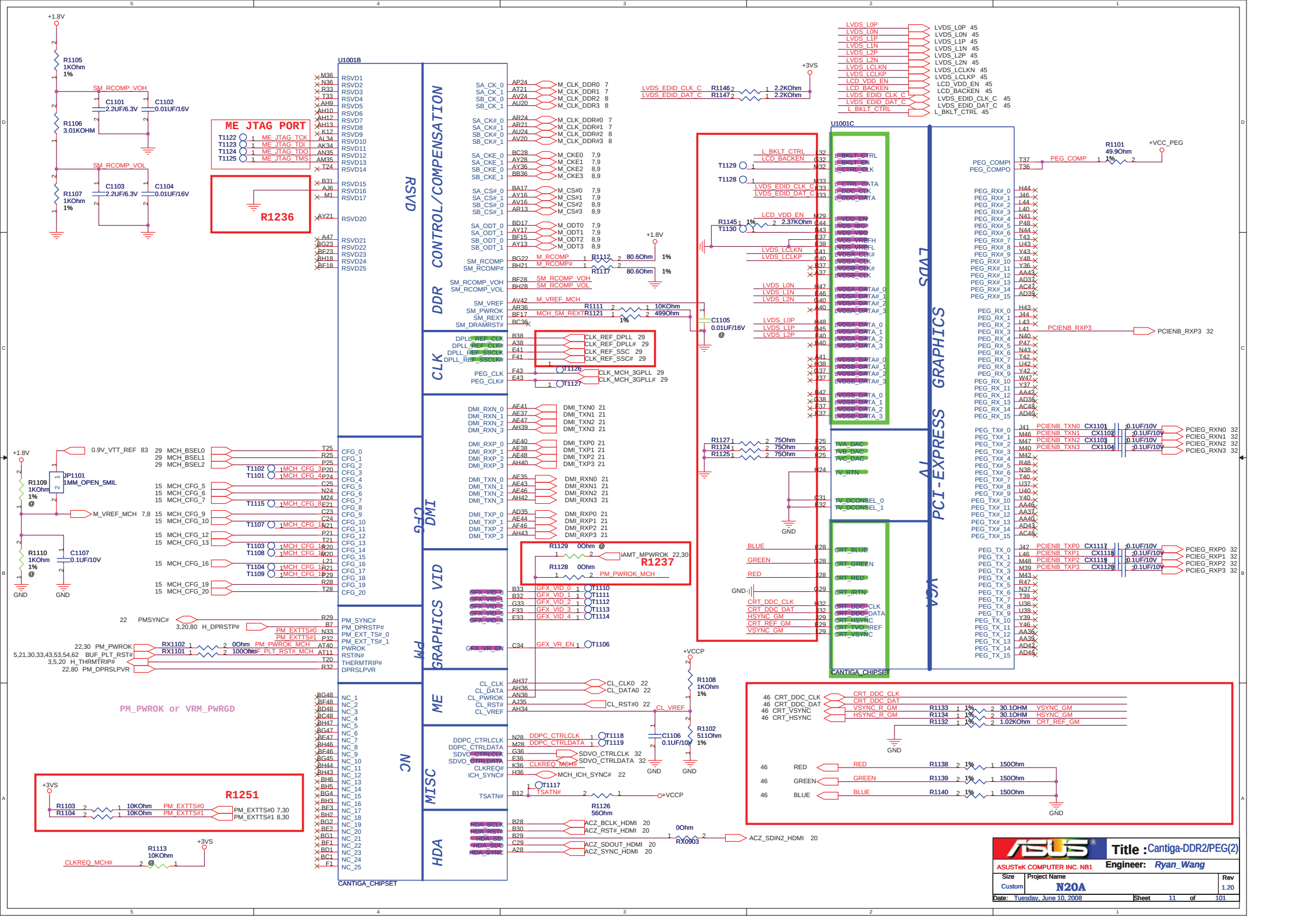
U1001B
U1001C
RSVD
CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
HDA
NC
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA_CHIPSET
ME JTAG PORT
R1236
R1237
R1251
PM_PWROK or VRM_PWRGD
Title : Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan_Wang
Size: Custom
Project Name: N20A
Rev: 1.20
Date: Tuesday, June 10, 2008
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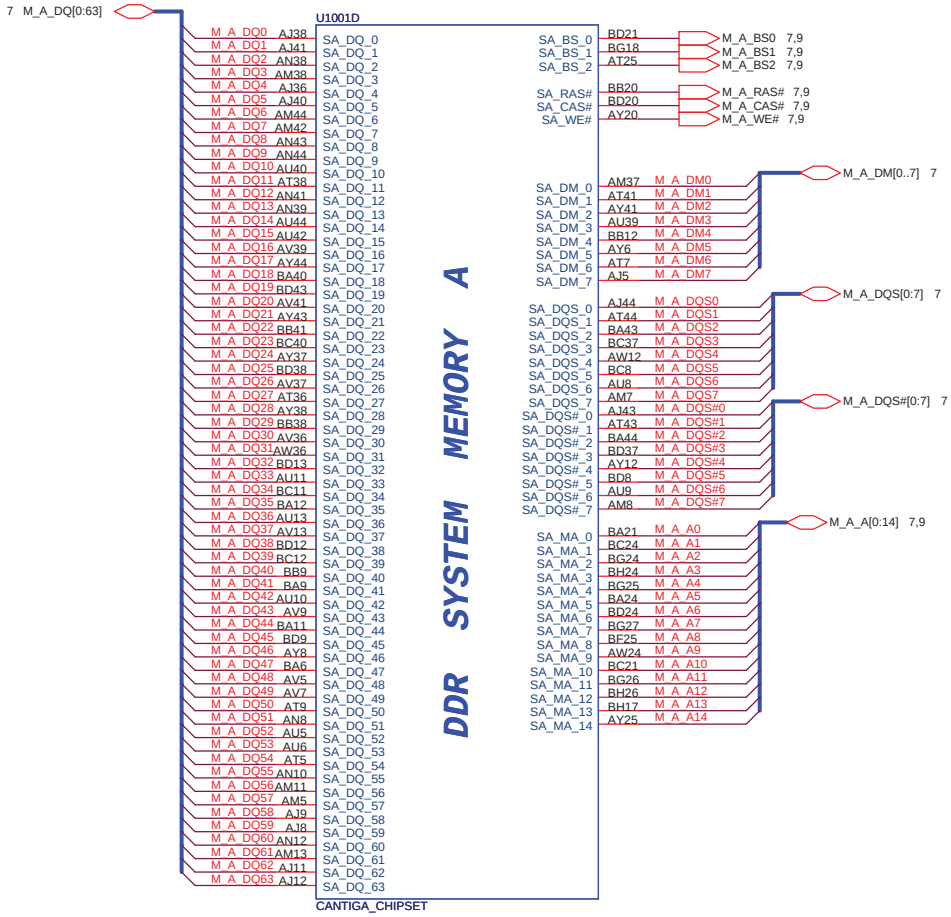

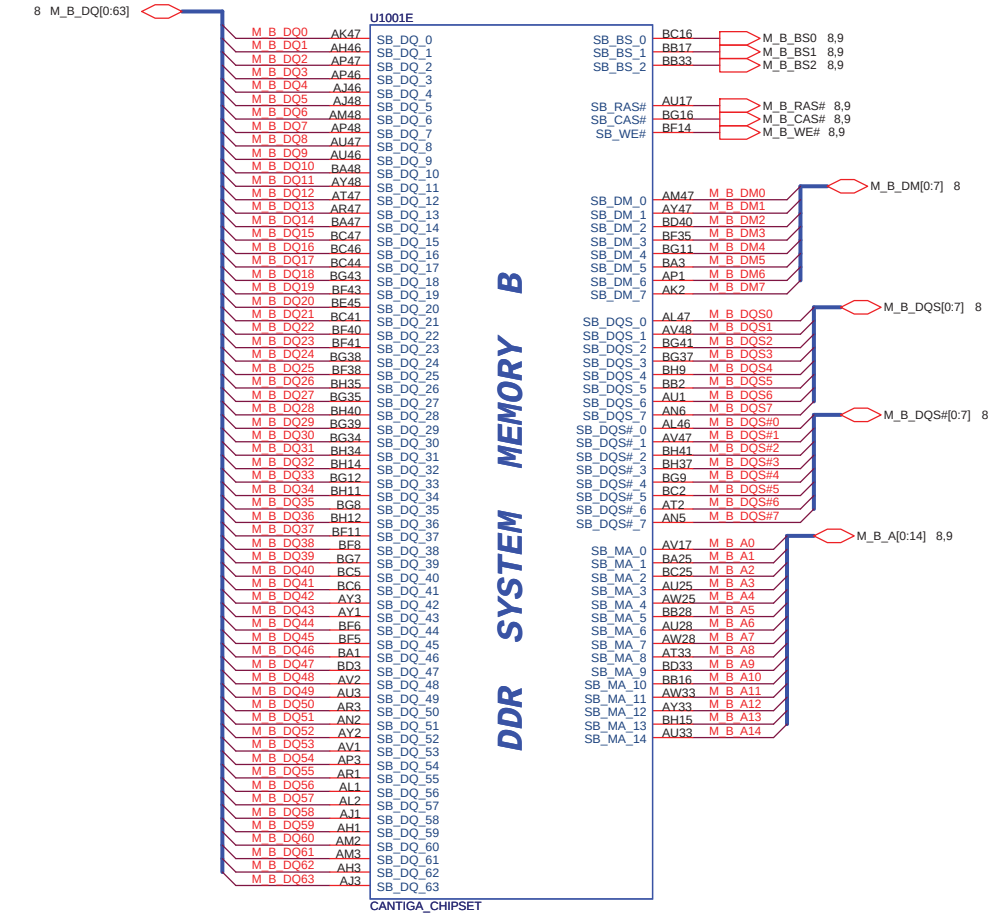

ASUSTeK COMPUTER INC. NB1

Title : Cantiga--DDR2 bus(3)

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

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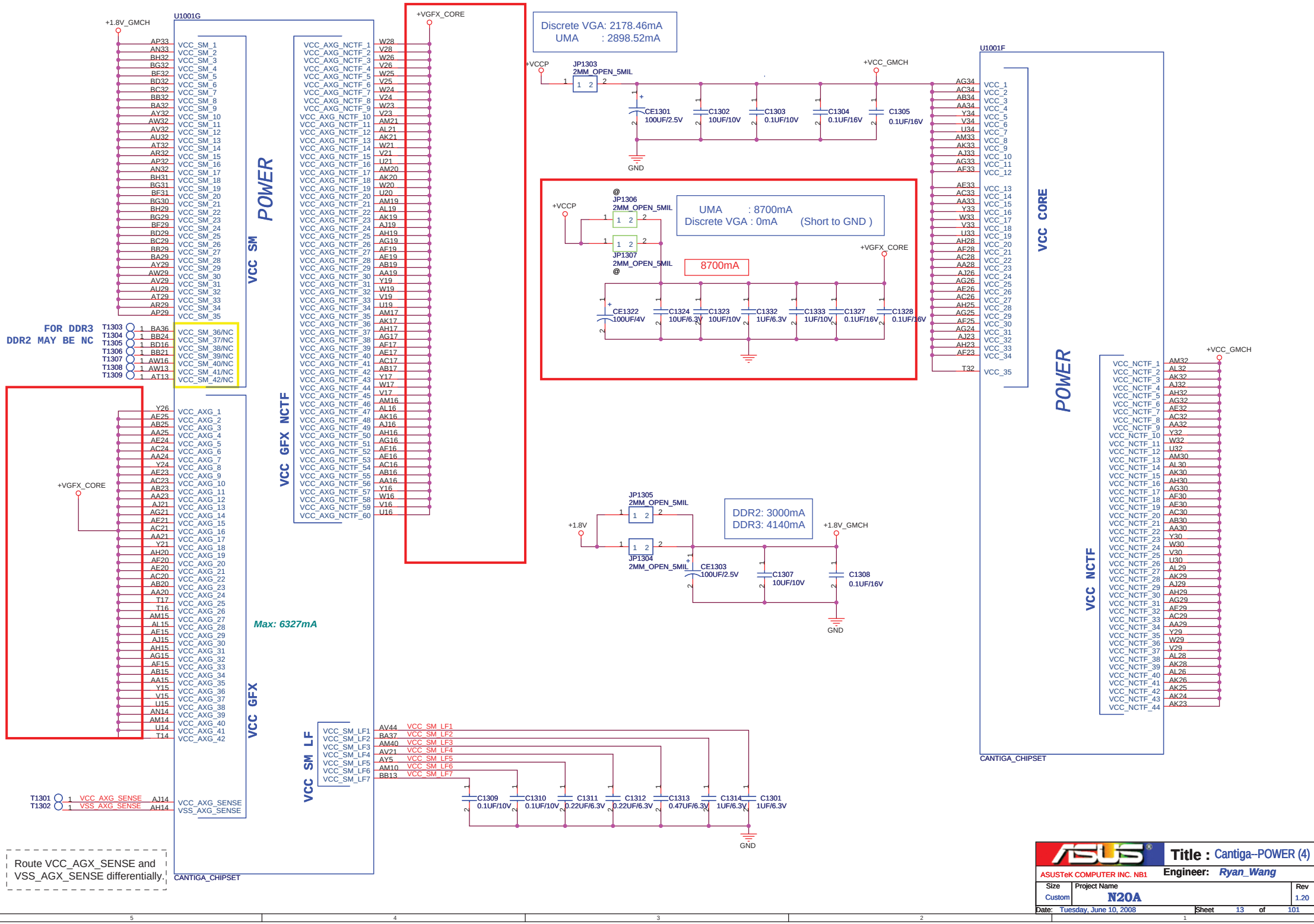
U1001G
+1.8V_GMCH
VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35
VCC SM
POWER
FOR DDR3
DDR2 MAY BE NC
T1303 T1304 T1305 T1306 T1307 T1308 T1309
VCC_SM_36/NC VCC_SM_37/NC VCC_SM_38/NC VCC_SM_39/NC VCC_SM_40/NC VCC_SM_41/NC VCC_SM_42/NC
+VGFX_CORE
VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42
VCC GFX
Max: 6327mA
VCC_AXG_SENSE VSS_AXG_SENSE
T1301 T1302
VCC_AXG_NCTF_1 ... VCC_AXG_NCTF_60
VCC GFX NCTF
+VGFX_CORE
VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7
VCC SM LF
C1309 0.1UF/10V C1310 0.1UF/10V C1311 0.22UF/6.3V C1312 0.22UF/6.3V C1313 0.47UF/6.3V C1314 1UF/6.3V C1301 1UF/6.3V
GND
CANTIGA_CHIPSET
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.
Discrete VGA: 2178.46mA
UMA : 2898.52mA
+VCCP
JP1303 2MM_OPEN_5MIL
+VCC_GMCH
CE1301 100UF/2.5V C1302 10UF/10V C1303 0.1UF/10V C1304 0.1UF/16V C1305 0.1UF/16V
GND
@ JP1306 2MM_OPEN_5MIL
JP1307 2MM_OPEN_5MIL @
UMA : 8700mA
Discrete VGA : 0mA (Short to GND)
8700mA
+VGFX_CORE
CE1322 100UF/4V C1324 10UF/6.3V C1323 10UF/10V C1332 1UF/6.3V C1333 1UF/10V C1327 0.1UF/16V C1328 0.1UF/16V
JP1305 2MM_OPEN_5MIL
JP1304 2MM_OPEN_5MIL
+1.8V
DDR2: 3000mA
DDR3: 4140mA
+1.8V_GMCH
CE1303 100UF/2.5V C1307 10UF/10V C1308 0.1UF/16V
GND
U1001F
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35
VCC CORE
POWER
VCC NCTF
+VCC_GMCH
VCC_NCTF_1 ... VCC_NCTF_44
CANTIGA_CHIPSET
ASUSTeK COMPUTER INC. NB1
Title : Cantiga--POWER (4)
Engineer: Ryan_Wang
Size: Custom
Project Name: N20A
Rev: 1.20
Date: Tuesday, June 10, 2008
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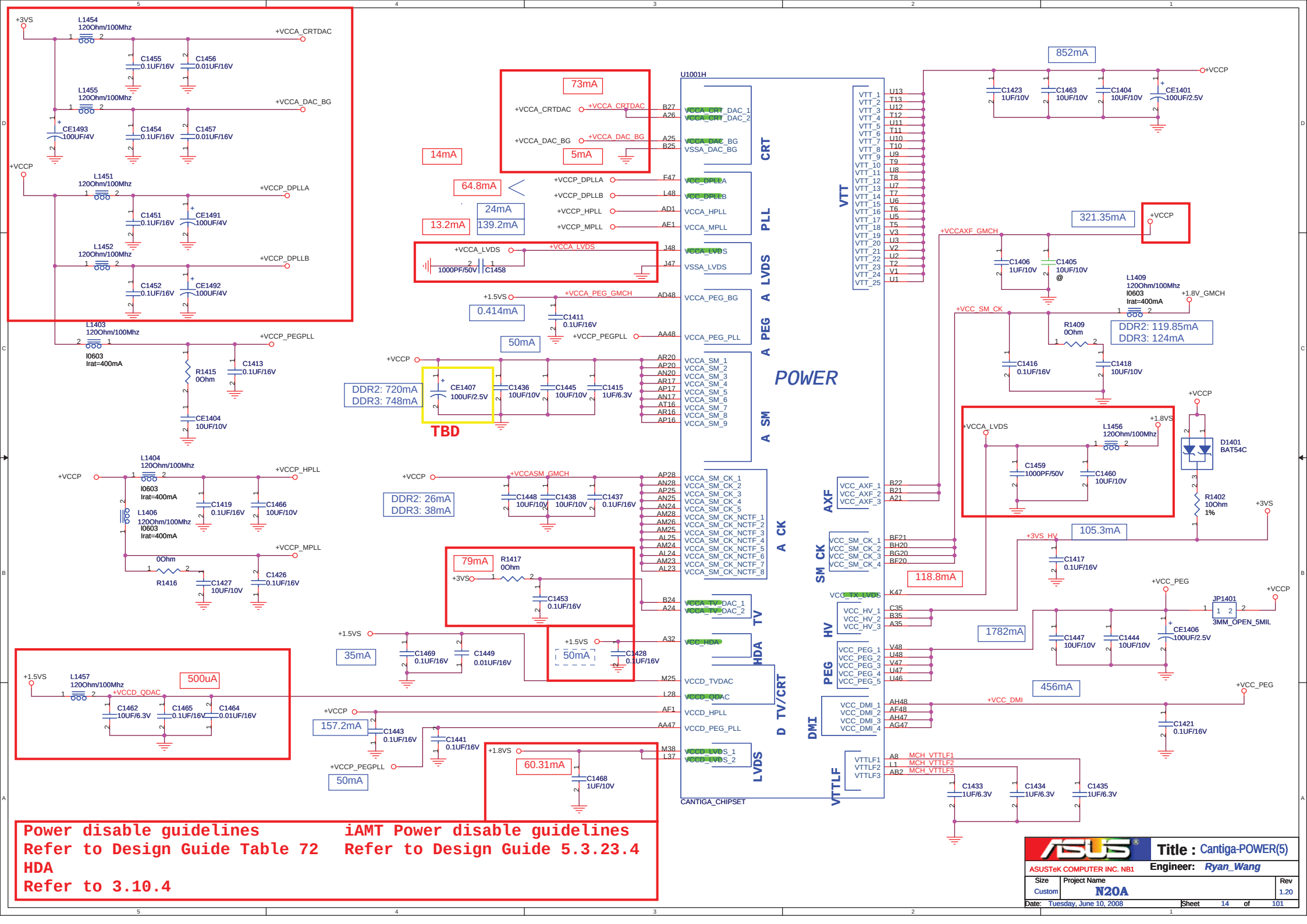
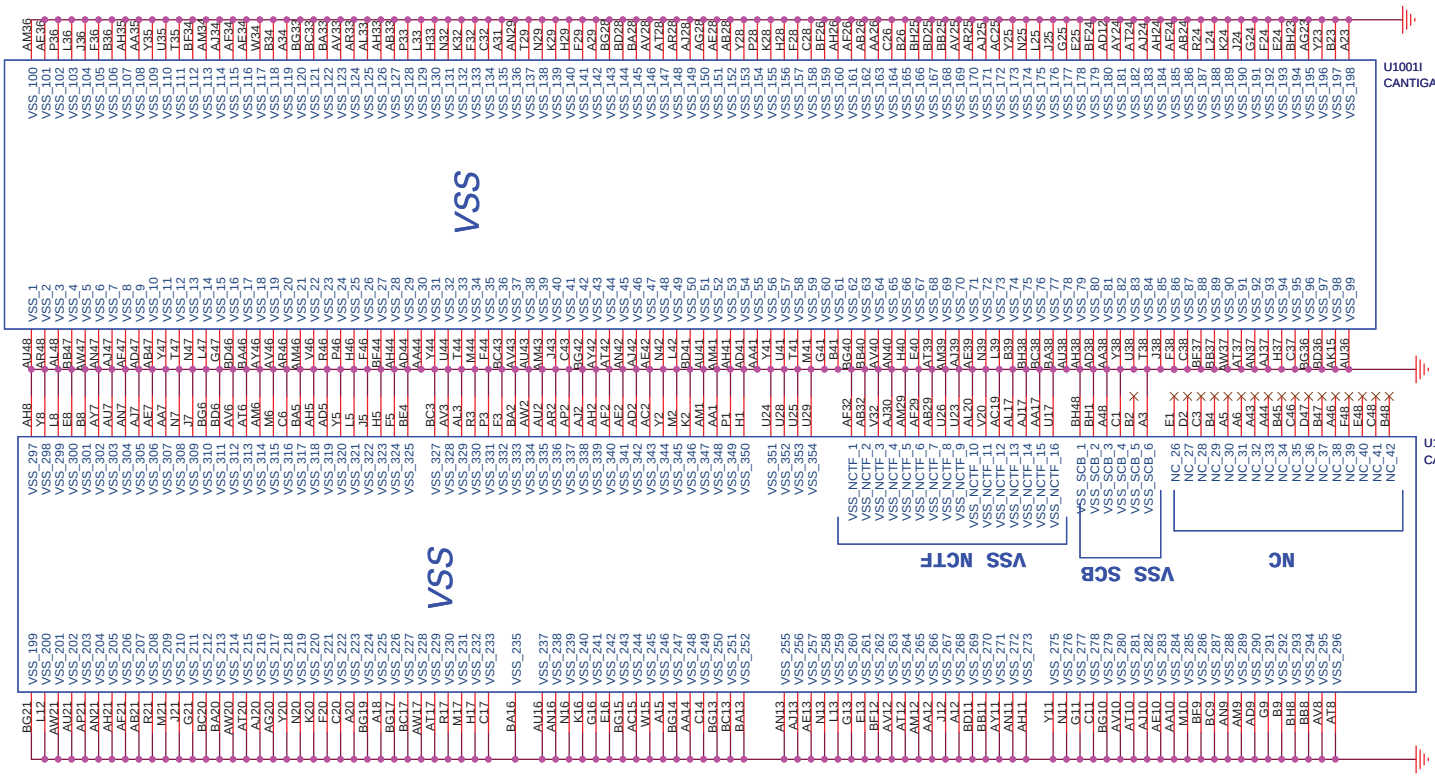

+3VS
L1454 120Ohm/100Mhz
+VCCA_CRTDAC
C1455 0.1UF/16V
C1456 0.01UF/16V
L1455 120Ohm/100Mhz
+VCCA_DAC_BG
CE1493 100UF/4V
C1454 0.1UF/16V
C1457 0.01UF/16V
+VCCP
L1451 120Ohm/100Mhz
+VCCP_DPLLA
C1451 0.1UF/16V
CE1491 100UF/4V
L1452 120Ohm/100Mhz
+VCCP_DPLLB
C1452 0.1UF/16V
CE1492 100UF/4V
L1403 120Ohm/100Mhz
+VCCP_PEGPLL
l0603
Irat=400mA
R1415 0Ohm
C1413 0.1UF/16V
CE1404 10UF/10V
L1404 120Ohm/100Mhz
+VCCP_HPLL
l0603
Irat=400mA
C1419 0.1UF/16V
C1466 10UF/10V
L1406 120Ohm/100Mhz
l0603
Irat=400mA
+VCCP_MPLL
0Ohm
R1416
C1427 10UF/10V
C1426 0.1UF/16V
+1.5VS
L1457 120Ohm/100Mhz
+VCCD_QDAC
500uA
C1462 10UF/6.3V
C1465 0.1UF/16V
C1464 0.01UF/16V
73mA
+VCCA_CRTDAC
+VCCA_CRTDAC
+VCCA_DAC_BG
+VCCA_DAC_BG
5mA
14mA
64.8mA
24mA
139.2mA
13.2mA
+VCCP_DPLLA
+VCCP_DPLLB
+VCCP_HPLL
+VCCP_MPLL
+VCCA_LVDS
+VCCA_LVDS
1000PF/50V
C1458
+1.5VS
+VCCA_PEG_GMCH
0.414mA
C1411 0.1UF/16V
+VCCP_PEGPLL
50mA
+VCCP
DDR2: 720mA
DDR3: 748mA
CE1407 100UF/2.5V
C1436 10UF/10V
C1445 10UF/10V
C1415 1UF/6.3V
TBD
+VCCP
+VCCASM_GMCH
DDR2: 26mA
DDR3: 38mA
C1448 10UF/10V
C1438 10UF/10V
C1437 0.1UF/16V
79mA
R1417 0Ohm
+3VS
C1453 0.1UF/16V
+1.5VS
35mA
C1469 0.1UF/16V
C1449 0.01UF/16V
+1.5VS
50mA
C1428 0.1UF/16V
+VCCP
157.2mA
C1443 0.1UF/16V
C1441 0.1UF/16V
+VCCP_PEGPLL
50mA
+1.8VS
60.31mA
C1468 1UF/10V
U1001H
CRT
PLL
LVDS
PEG
SM
CK
TV
HDA
TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
POWER
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
VCCA_DAC_BG
VSSA_DAC_BG
VCC_DPLLA
VCC_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
VCCA_TVDAC_1
VCCA_TVDAC_2
VCC_HDA
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1
VCCD_LVDS_2
CANTIGA_CHIPSET
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
VCC_TX_LVDS
VCC_HV_1
VCC_HV_2
VCC_HV_3
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
VTTLF1
VTTLF2
VTTLF3
852mA
+VCCP
C1423 1UF/10V
C1463 10UF/10V
C1404 10UF/10V
CE1401 100UF/2.5V
321.35mA
+VCCP
+VCCAXF_GMCH
C1406 1UF/10V
C1405 10UF/10V
@
L1409 120Ohm/100Mhz
l0603
Irat=400mA
+1.8V_GMCH
+VCC_SM_CK
R1409 0Ohm
DDR2: 119.85mA
DDR3: 124mA
C1416 0.1UF/16V
C1418 10UF/10V
+VCCP
+VCCA_LVDS
+1.8VS
L1456 120Ohm/100Mhz
C1459 1000PF/50V
C1460 10UF/10V
D1401 BAT54C
R1402 10Ohm 1%
+3VS
105.3mA
+3VS_HV
C1417 0.1UF/16V
118.8mA
+VCC_PEG
+VCCP
JP1401
3MM_OPEN_5MIL
1782mA
C1447 10UF/10V
C1444 10UF/10V
CE1406 100UF/2.5V
456mA
+VCC_PEG
+VCC_DMI
C1421 0.1UF/16V
MCH_VTTLF1
MCH_VTTLF2
MCH_VTTLF3
C1433 1UF/6.3V
C1434 1UF/6.3V
C1435 1UF/6.3V
Power disable guidelines
Refer to Design Guide Table 72
HDA
Refer to 3.10.4
iAMT Power disable guidelines
Refer to Design Guide 5.3.23.4
ASUSTeK COMPUTER INC. NB1
Title : Cantiga-POWER(5)
Engineer: Ryan_Wang
Size Custom
Project Name N20A
Rev 1.20
Date: Tuesday, June 10, 2008
Sheet 14 of 101



11 MCH_CFG_5

R1509 2.21KOhm @

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

11 MCH_CFG_6

R1514 2.21KOhm @

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

11 MCH_CFG_7

R1511 2.21KOhm @

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

11 MCH_CFG_9

R1512 2.21KOhm @

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

11 MCH_CFG_16

R1507 2.21KOhm @

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

11 MCH_CFG_10

R1508 2.21KOhm @

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

11 MCH_CFG_12

R1513 2.21KOhm @

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

11 MCH_CFG_13

R1510 2.21KOhm @

+3VS

R1503 4.02KOHM @

11 MCH_CFG_19

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

+3VS

R1506 4.02KOHM @

11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

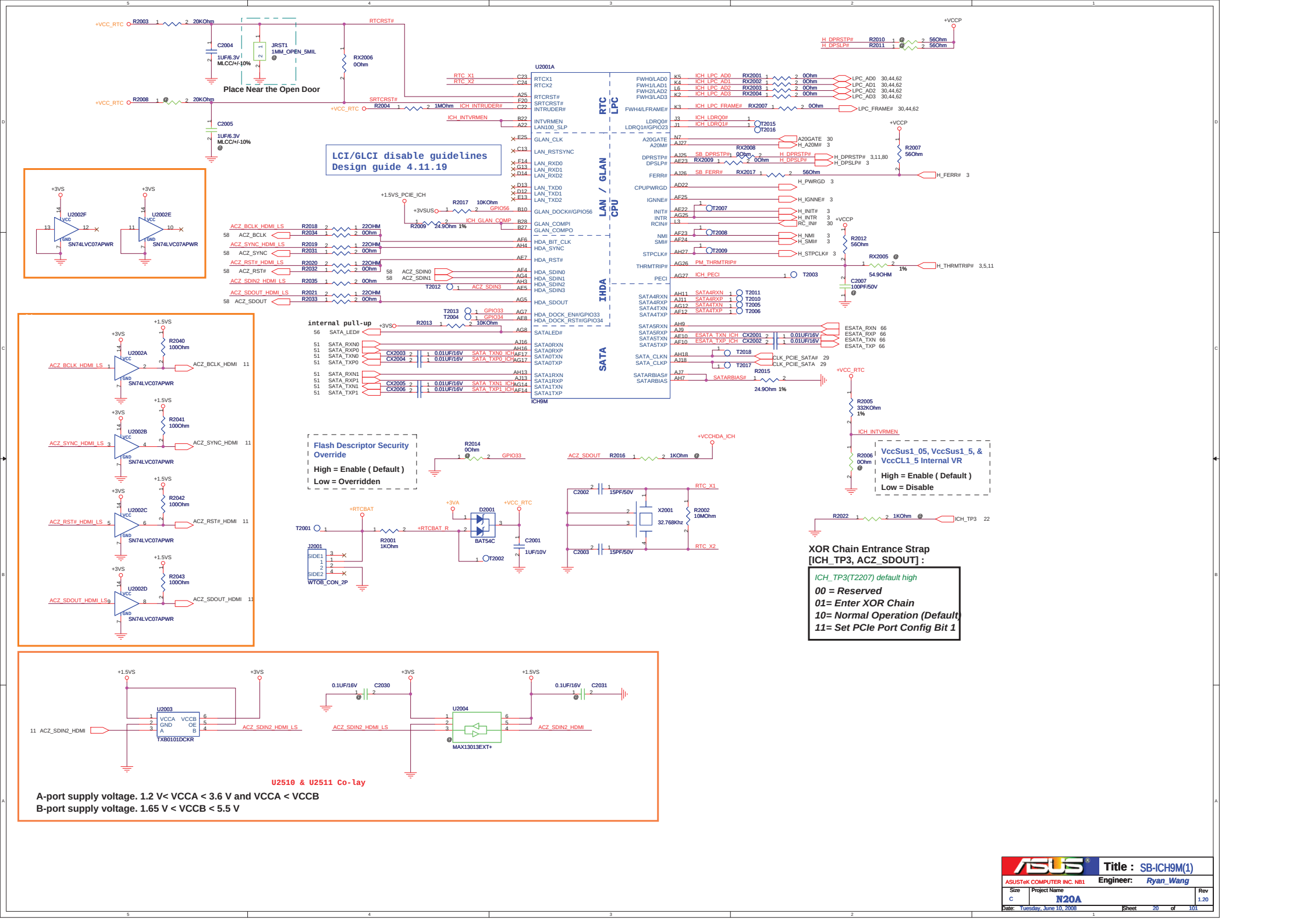
ASUSTeK COMPUTER INC. NB1	Title : Cantiga-GND	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Tuesday, June 10, 2008	Sheet 15 of 101	

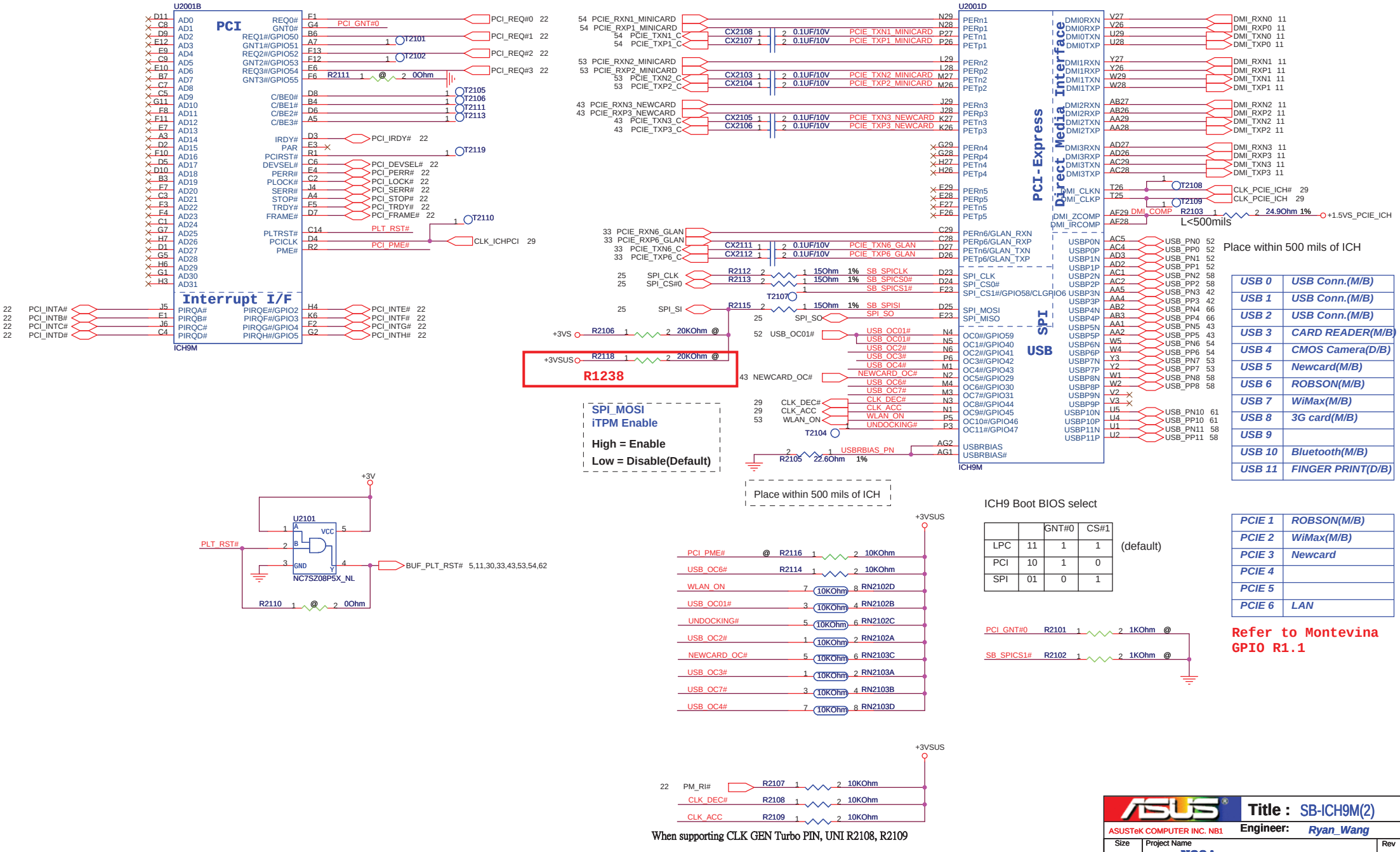
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Tuesday, June 10, 2008	Sheet 16 of 101	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Tuesday, June 10, 2008	Sheet 17 of 101	

ASUSTeK COMPUTER INC. NB1		Title :	
		Engineer: Ryan_Wang	
Size: A	Project Name: N20A		Rev: 1.20
Date: Tuesday, June 10, 2008		Sheet 18 of 101	

ASUSTeK COMPUTER INC. NB1		Title :	
		Engineer: Ryan_Wang	
Size: A	Project Name: N20A		Rev: 1.20
Date: Tuesday, June 10, 2008		Sheet 19 of 101	


LCI/GLCI disable guidelines
Design guide 4.11.19
Place Near the Open Door
U2001A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
internal pull-up
Flash Descriptor Security Override
High = Enable (Default)
Low = Overridden
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable
XOR Chain Entrance Strap [ICH_TP3, ACZ_SDOUT] :
ICH_TP3(T2207) default high
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
U2510 & U2511 Co-lay
A-port supply voltage. 1.2 V< VCCA < 3.6 V and VCCA < VCCB
B-port supply voltage. 1.65 V < VCCB < 5.5 V
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan_Wang
Size C
Project Name N20A
Rev 1.20
Date: Tuesday, June 10, 2008
Sheet 20 of 101

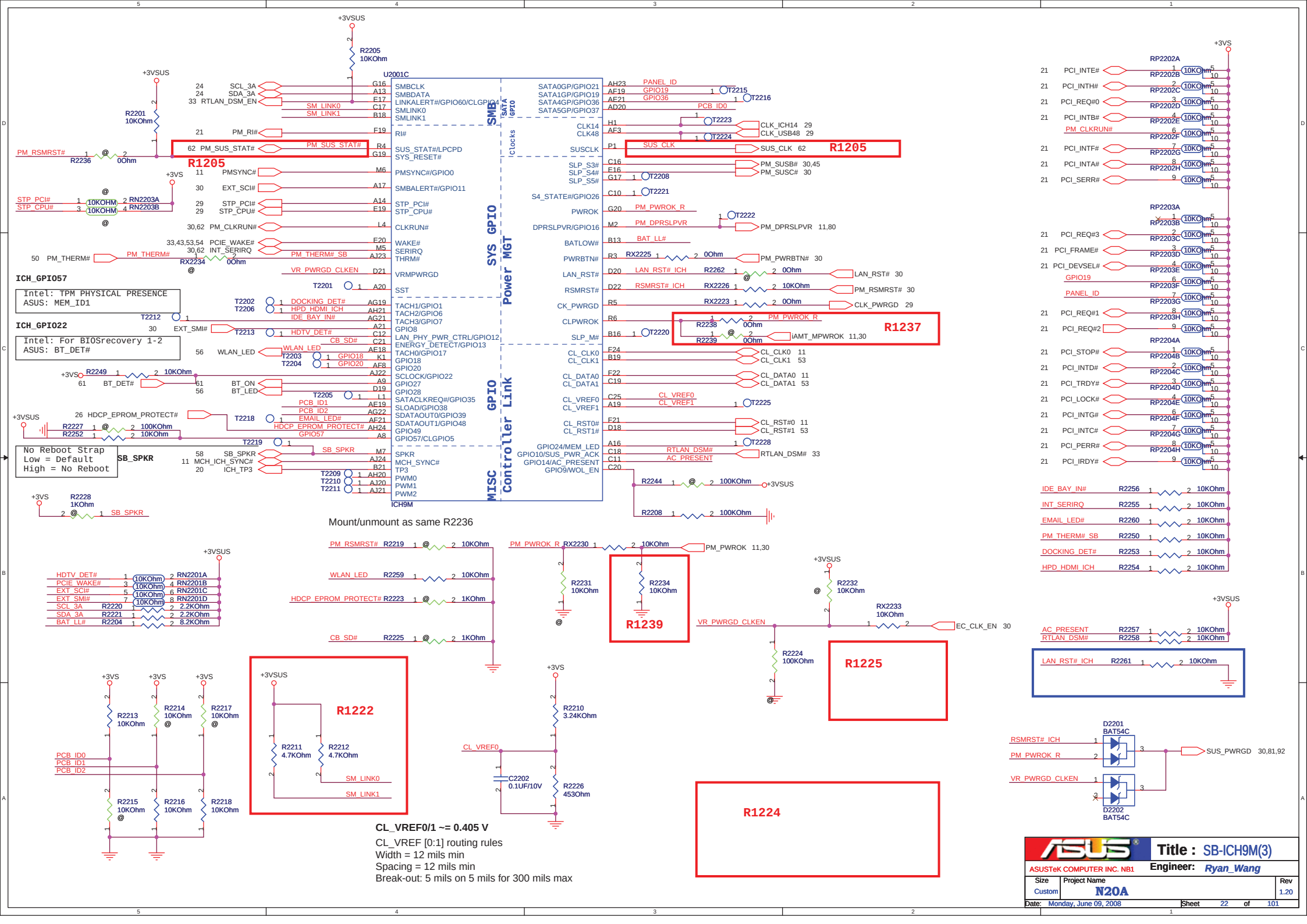


USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	CARD READER(M/B)
USB 4	CMOS Camera(D/B)
USB 5	Newcard(M/B)
USB 6	ROBSON(M/B)
USB 7	WiMax(M/B)
USB 8	3G card(M/B)
USB 9	
USB 10	Bluetooth(M/B)
USB 11	FINGER PRINT(D/B)

		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

PCIE 1	ROBSON(M/B)
PCIE 2	WiMax(M/B)
PCIE 3	Newcard
PCIE 4	
PCIE 5	
PCIE 6	LAN

Title : SB-ICH9M(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan_Wang
Size: Custom | Project Name: N20A | Rev: 1.20
Date: Tuesday, June 10, 2008 | Sheet 21 of 101


U2001C
ICH9M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
R1205
R1237
R1239
R1225
R1222
R1224
ICH_GPIO57
Intel: TPM PHYSICAL PRESENCE
ASUS: MEM_ID1
ICH_GPIO22
Intel: For BIOSrecovery 1-2
ASUS: BT_DET#
No Reboot Strap
Low = Default
High = No Reboot
SB_SPKR
Mount/unmount as same R2236
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
Title : SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan_Wang
Size: Custom
Project Name: N20A
Rev: 1.20
Date: Monday, June 09, 2008
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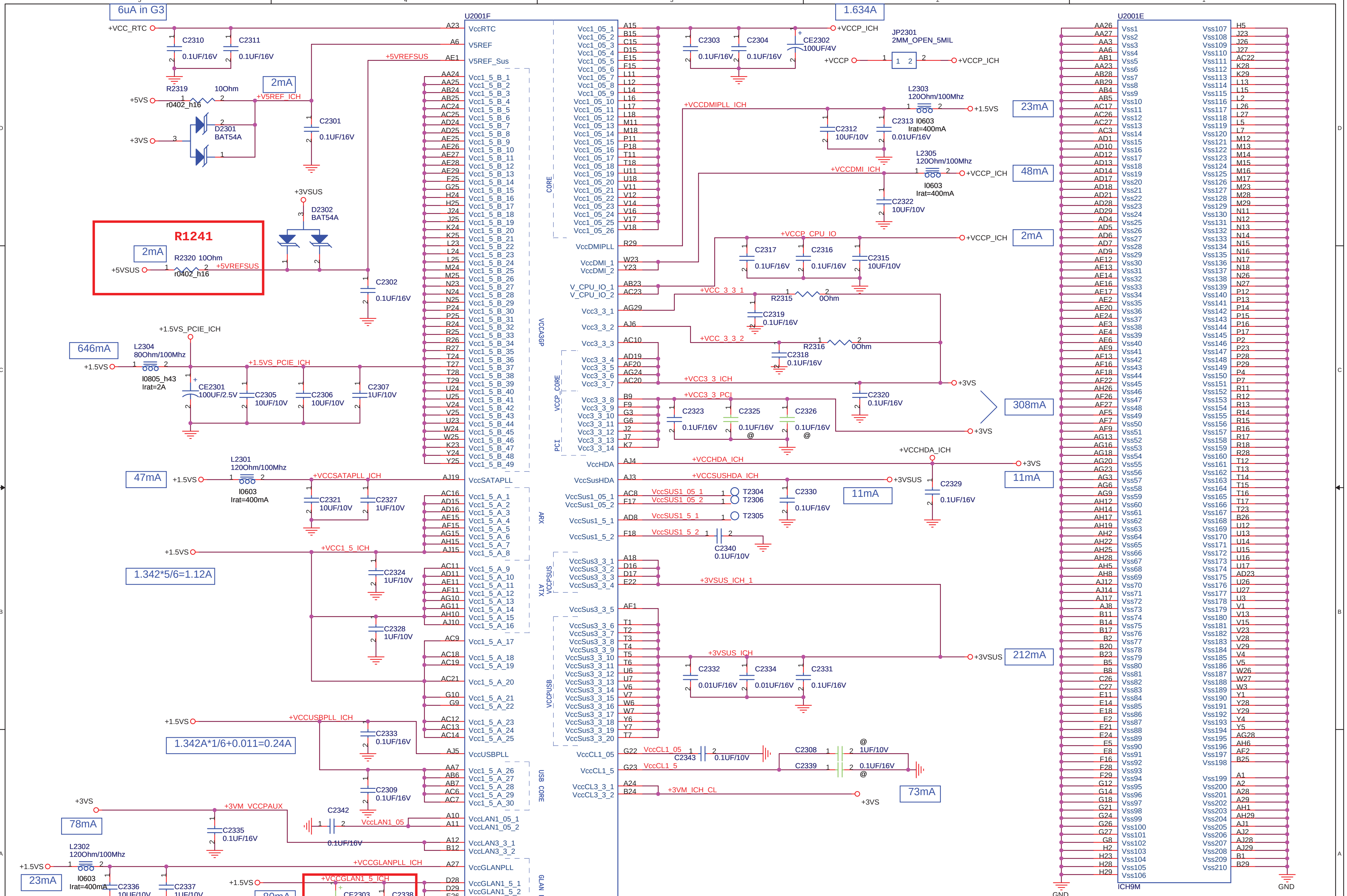


6uA in G3
+VCC_RTC
C2310 0.1UF/16V
C2311 0.1UF/16V
U2001F
VccRTC
V5REF
V5REF_Sus
+5VREFSUS
2mA
R2319 10Ohm r0402_h16
+5VS
+V5REF_ICH
+3VS
D2301 BAT54A
C2301 0.1UF/16V
+3VSUS
D2302 BAT54A
R1241
2mA
R2320 10Ohm r0402_h16
+5VSUS
C2302 0.1UF/16V
+1.5VS_PCIE_ICH
646mA
L2304 80Ohm/100Mhz l0805_h43 Irat=2A
+1.5VS
CE2301 100UF/2.5V
C2305 10UF/10V
C2306 10UF/10V
C2307 1UF/10V
47mA
L2301 120Ohm/100Mhz l0603 Irat=400mA
+VCCSATAPLL_ICH
VccSATAPLL
C2321 10UF/10V
C2327 1UF/10V
+VCC1_5_ICH
1.342*5/6=1.12A
C2324 1UF/10V
C2328 1UF/10V
+VCCUSBPLL_ICH
VccUSBPLL
1.342A*1/6+0.011=0.24A
C2333 0.1UF/16V
C2309 0.1UF/16V
+3VS
78mA
+3VM_VCCPAUX
C2335 0.1UF/16V
C2342 0.1UF/16V
VccLAN1_05
VccLAN1_05_1
VccLAN1_05_2
VccLAN3_3_1
VccLAN3_3_2
L2302 120Ohm/100Mhz l0603 Irat=400mA
23mA
+VCCGLANPLL_ICH
VccGLANPLL
C2336 10UF/10V
C2337 1UF/10V
80mA
+VCCGLAN1_5_ICH
CE2303 220UF/4V
C2338 10UF/10V
VccGLAN1_5_1
VccGLAN1_5_2
VccGLAN1_5_3
VccGLAN1_5_4
+VCCGLAN3_3_ICH
VccGLAN3_3
1mA
R1240
ICH9M
1.634A
+VCCP_ICH
C2303 0.1UF/16V
C2304 0.1UF/16V
CE2302 100UF/4V
JP2301 2MM_OPEN_5MIL
+VCCP
+VCCDMIPLL_ICH
VccDMIPLL
L2303 120Ohm/100Mhz
+1.5VS
23mA
C2312 10UF/10V
C2313 l0603 Irat=400mA 0.01UF/16V
L2305 120Ohm/100Mhz l0603 Irat=400mA
+VCCDMI_ICH
48mA
C2322 10UF/10V
VccDMI_1
VccDMI_2
+VCCP_CPU_IO
2mA
C2317 0.1UF/16V
C2316 0.1UF/16V
C2315 10UF/10V
V_CPU_IO_1
V_CPU_IO_2
+VCC_3_3_1
R2315 0Ohm
C2319 0.1UF/16V
+VCC_3_3_2
R2316 0Ohm
C2318 0.1UF/16V
+VCC3_3_ICH
C2320 0.1UF/16V
+VCC3_3_PCI
C2323 0.1UF/16V
C2325 0.1UF/16V
C2326 0.1UF/16V
308mA
+VCCHDA_ICH
VccHDA
11mA
C2329 0.1UF/16V
+VCCSUSHDA_ICH
VccSusHDA
+3VSUS
VccSUS1_05_1
VccSUS1_05_2
T2304
T2306
C2330 0.1UF/16V
11mA
VccSUS1_5_1
T2305
VccSUS1_5_2
C2340 0.1UF/10V
+3VSUS_ICH_1
+3VSUS_ICH
212mA
C2332 0.01UF/16V
C2334 0.01UF/16V
C2331 0.1UF/16V
VccCL1_05
C2343 0.1UF/10V
C2308 1UF/10V
C2339 0.1UF/16V
VccCL1_5
+3VM_ICH_CL
73mA
VccCL3_3_1
VccCL3_3_2
U2001E
GND

Title : SB-ICH9M(PWR)

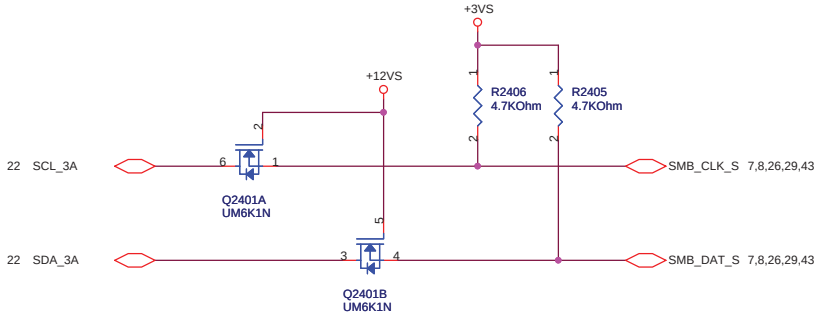
ASUSTeK COMPUTER INC. NB1

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 23 of 101

ICH9-M



Master	Slave
SCL_3A SDA_3A (ICH9M)	SMB_CLK_S SMB_DAT_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor

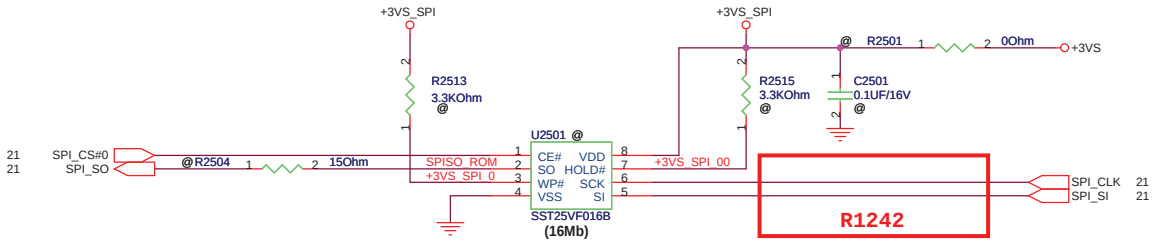
ASUSTeK COMPUTER INC. NB1

Title : ICH9M-Other

Engineer: Ryan_Wang

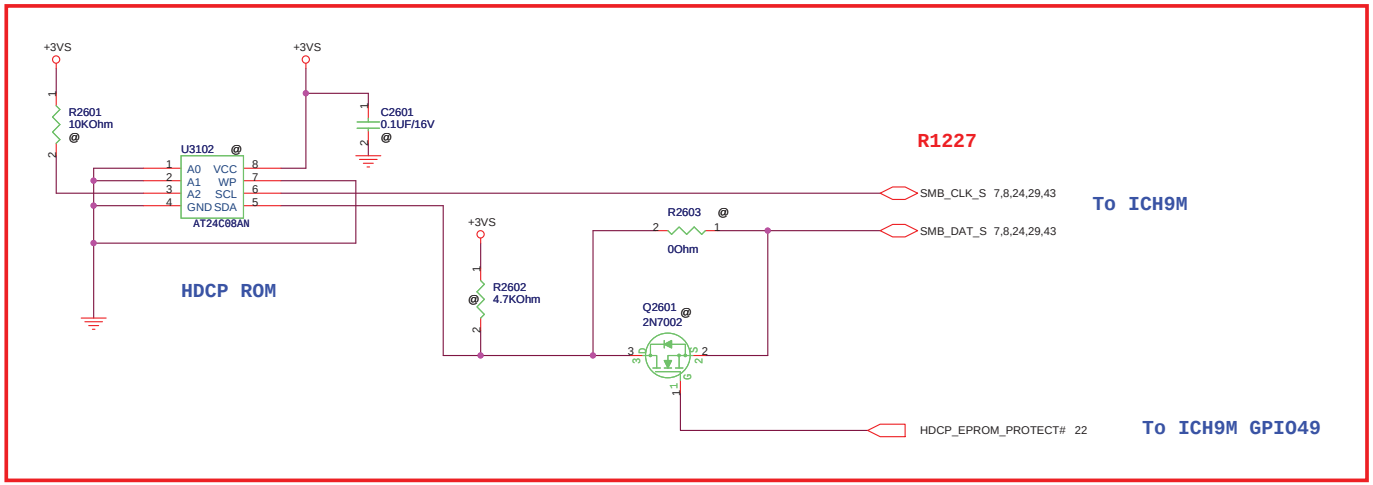
Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 24 of 101



FOR iTPM
8Mb 05G00120A010

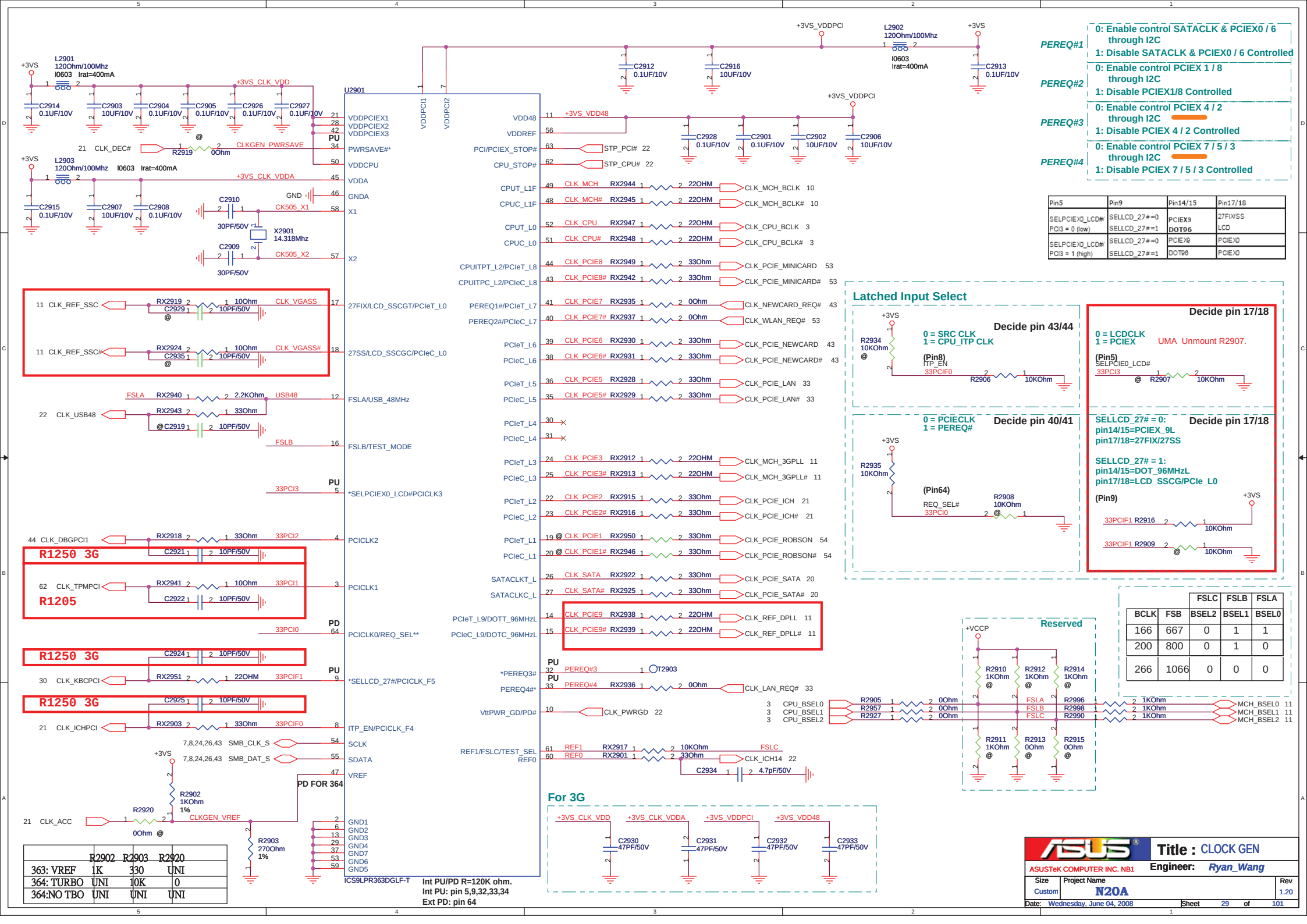
ASUSTeK COMPUTER INC. NB1	Title : SPI ROM	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Tuesday, June 10, 2008	Sheet 25 of 101	

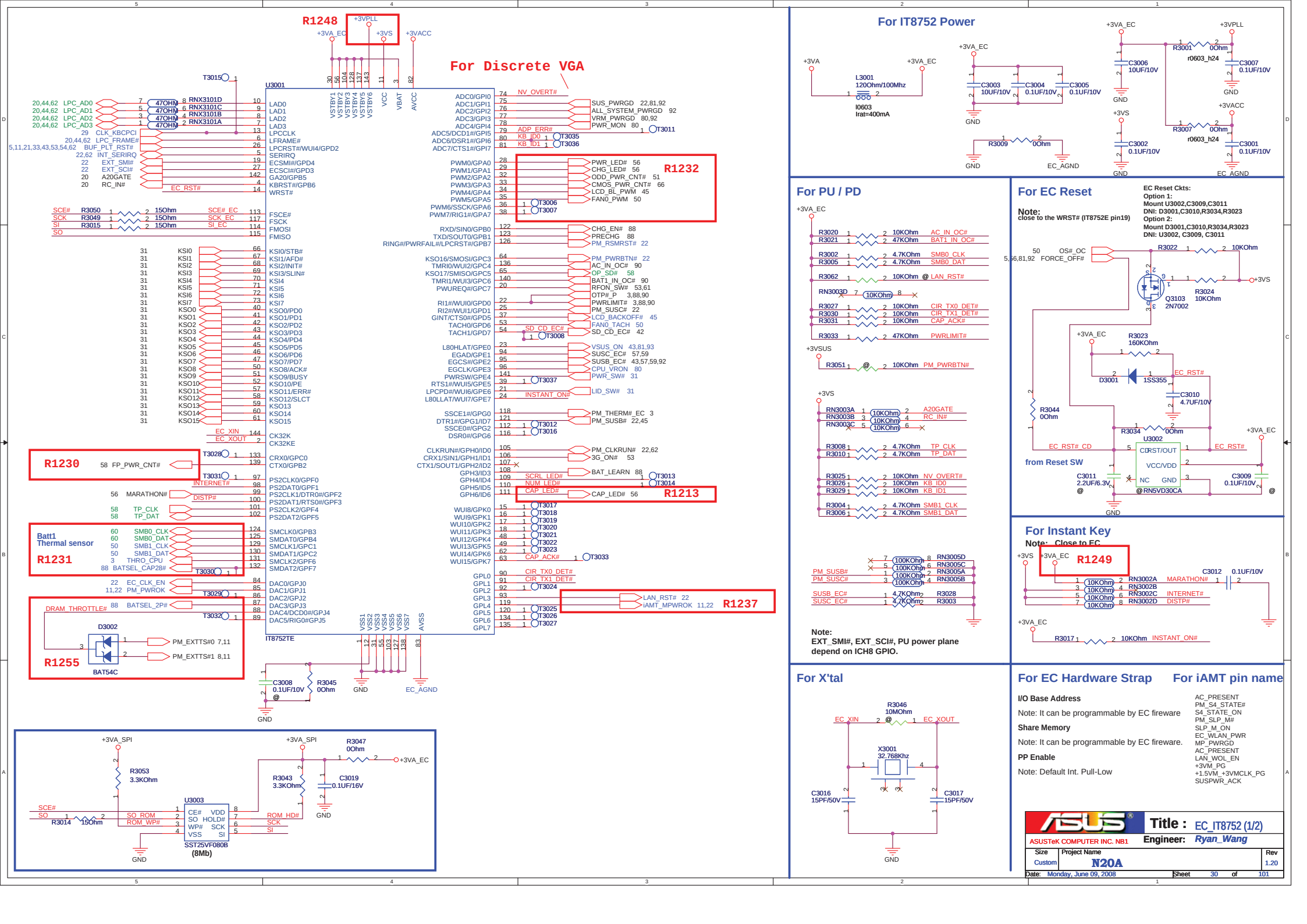


ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 26 of 101	

ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: Ryan_Wang		
Size: A	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 27 of 101		

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 28 of 101	


U2901
ICS9LPR363DGLF-T
+3VS_VDDPCI
+3VS_CLK_VDD
+3VS_CLK_VDDA
+3VS_VDD48
L2901 120Ohm/100Mhz l0603 Irat=400mA
L2902 120Ohm/100Mhz l0603 Irat=400mA
L2903 120Ohm/100Mhz l0603 Irat=400mA
PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled
PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled
PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled
PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled
Pin5 | Pin9 | Pin14/15 | Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low) | SELLCD_27#=0 | PCIEX9 | 27FIXSS
SELLCD_27#=1 | DOT96 | LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high) | SELLCD_27#=0 | PCIEX9 | PCIEX0
SELLCD_27#=1 | DOT96 | PCIEX0
Latched Input Select
0 = SRC CLK
1 = CPU_ITP CLK
(Pin8) ITP_EN 33PCIF0
Decide pin 43/44
0 = LCDCLK
1 = PCIEX
UMA Unmount R2907.
(Pin5) SELPCIE0_LCD# 33PCI3
Decide pin 17/18
0 = PCIECLK
1 = PEREQ#
(Pin64) REQ_SEL# 33PCI0
Decide pin 40/41
SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS
SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0
(Pin9) 33PCIF1 R2916 10KOhm
33PCIF1 R2909 10KOhm
Decide pin 17/18
Reserved
FSLC | FSLB | FSLA
BCLK | FSB | BSEL2 | BSEL1 | BSEL0
166 | 667 | 0 | 1 | 1
200 | 800 | 0 | 1 | 0
266 | 1066 | 0 | 0 | 0
R2902 | R2903 | R2920
363: VREF | 1K | 330 | UNI
364: TURBO | UNI | 10K | 0
364:NO TBO | UNI | UNI | UNI
For 3G
Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64
ASUSTeK COMPUTER INC. NB1
Title : CLOCK GEN
Engineer: Ryan_Wang
Size: Custom
Project Name: N20A
Rev: 1.20
Date: Wednesday, June 04, 2008
Sheet 29 of 101


For Discrete VGA
R1248
U3001
IT8752TE
R1232
R1213
R1237
R1230
R1231
R1255
Batt1
Thermal sensor
For IT8752 Power
For PU / PD
For EC Reset
For Instant Key
For X'tal
For EC Hardware Strap
For iAMT pin name
R1249
Note:
EXT_SMI#, EXT_SCI#, PU power plane
depend on ICH8 GPIO.
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
Title : EC_IT8752 (1/2)
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan_Wang
Project Name N20A
Date: Monday, June 09, 2008
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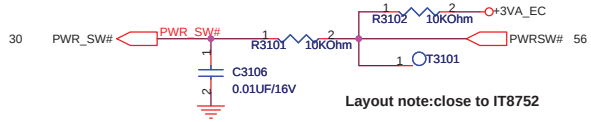
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

In Page 60

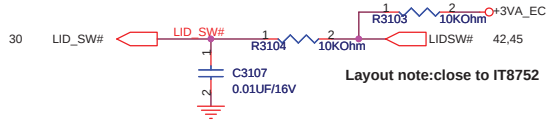
For Switch

PWR SWITCH

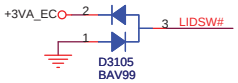


Layout note:close to IT8752

LID SWITCH



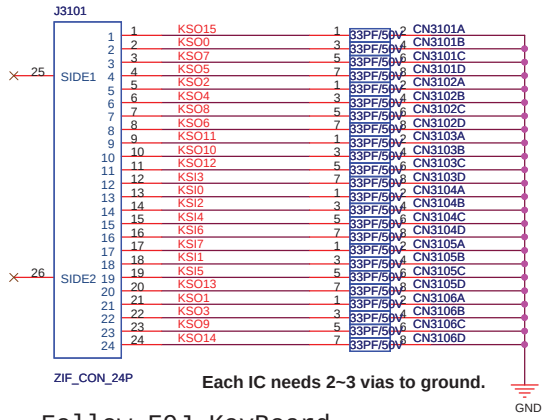
Layout note:close to IT8752



close to connector

Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

Keyboard Connector



Each IC needs 2~3 vias to ground.

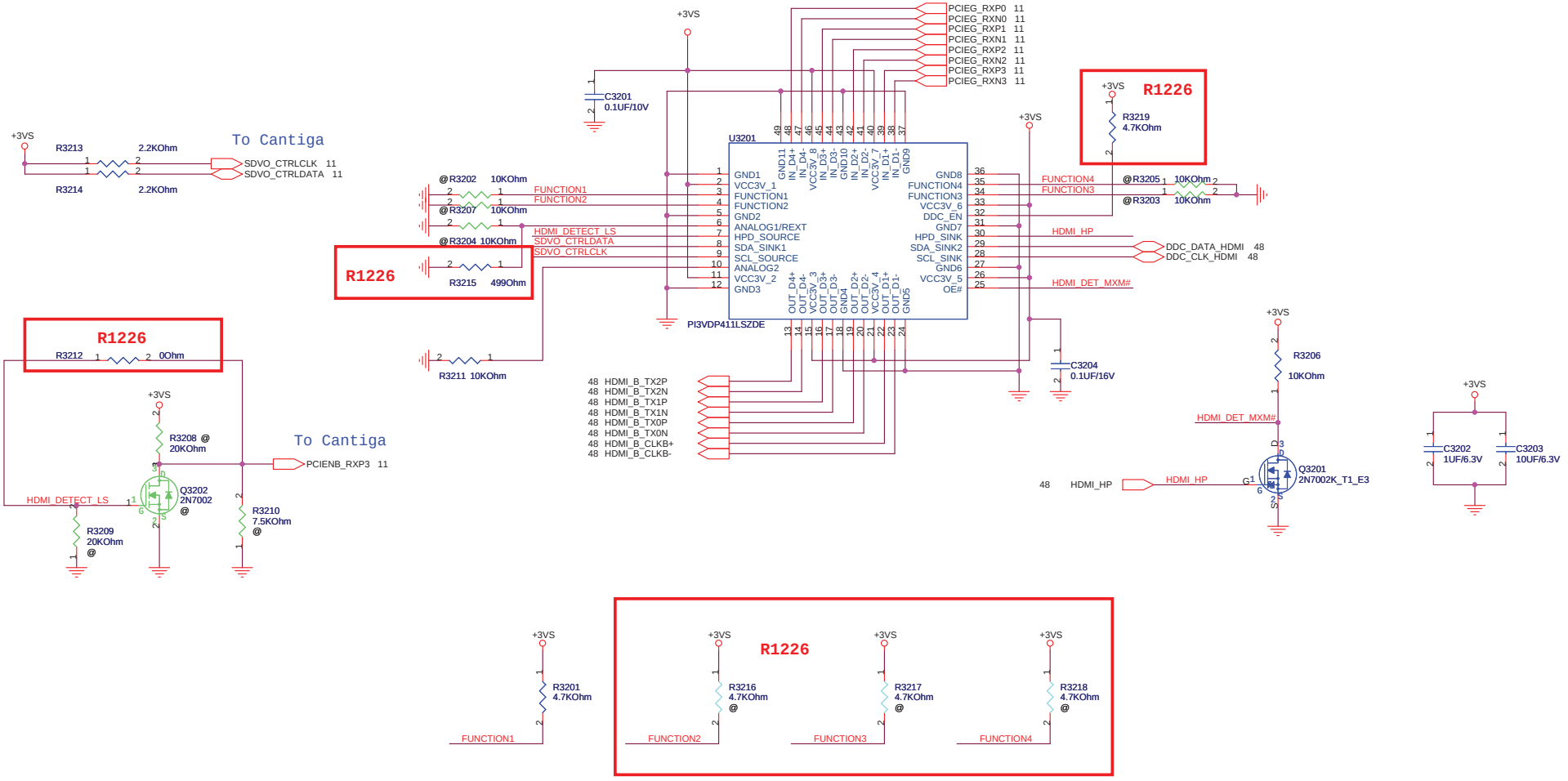
KSO[15:0] 30

KSI[7:0] 30

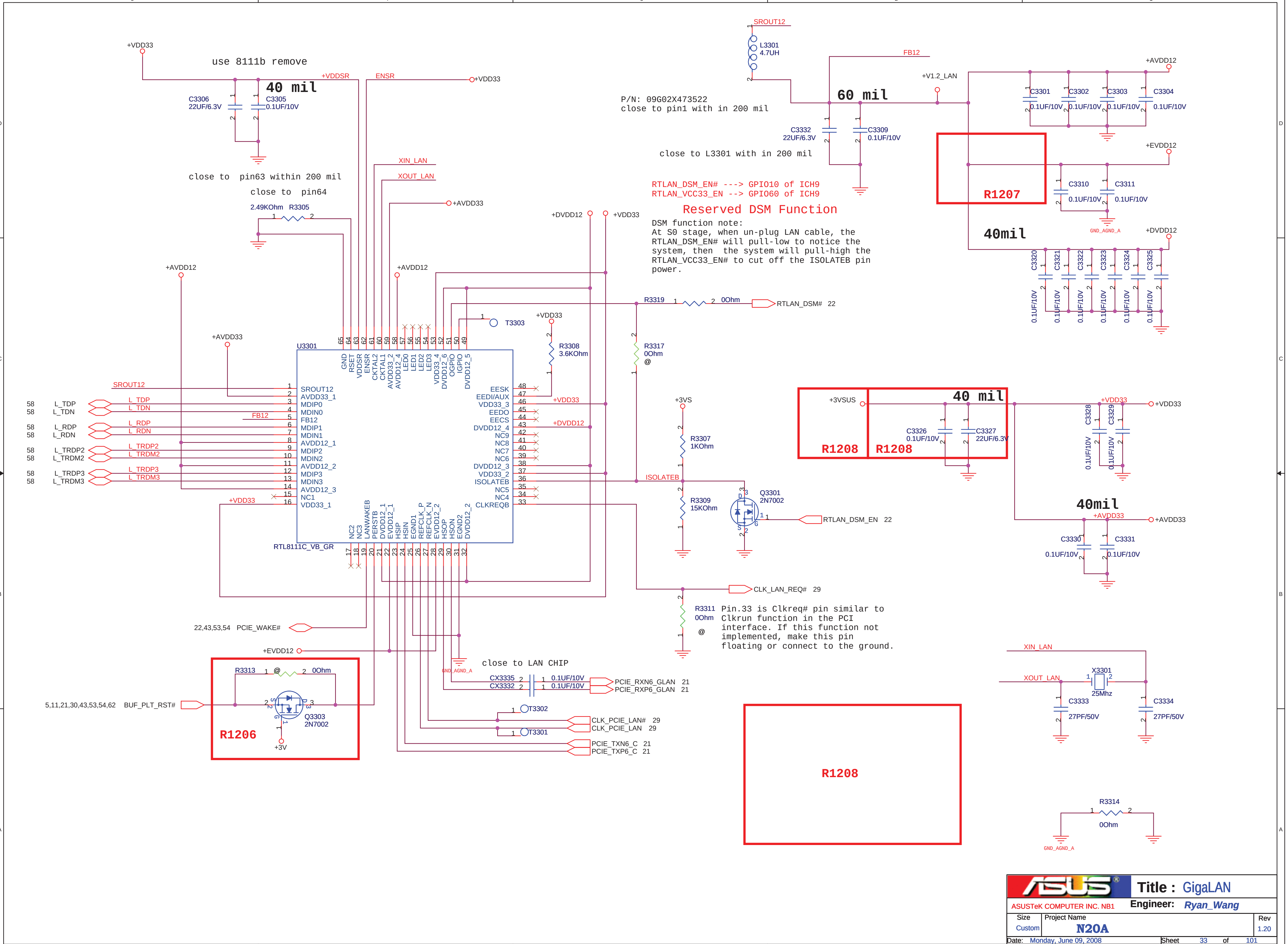
EMI decoupling recommandation.
Need put between KB connector and KBC, and close to the connector as possible.

Follow F9J KeyBoard

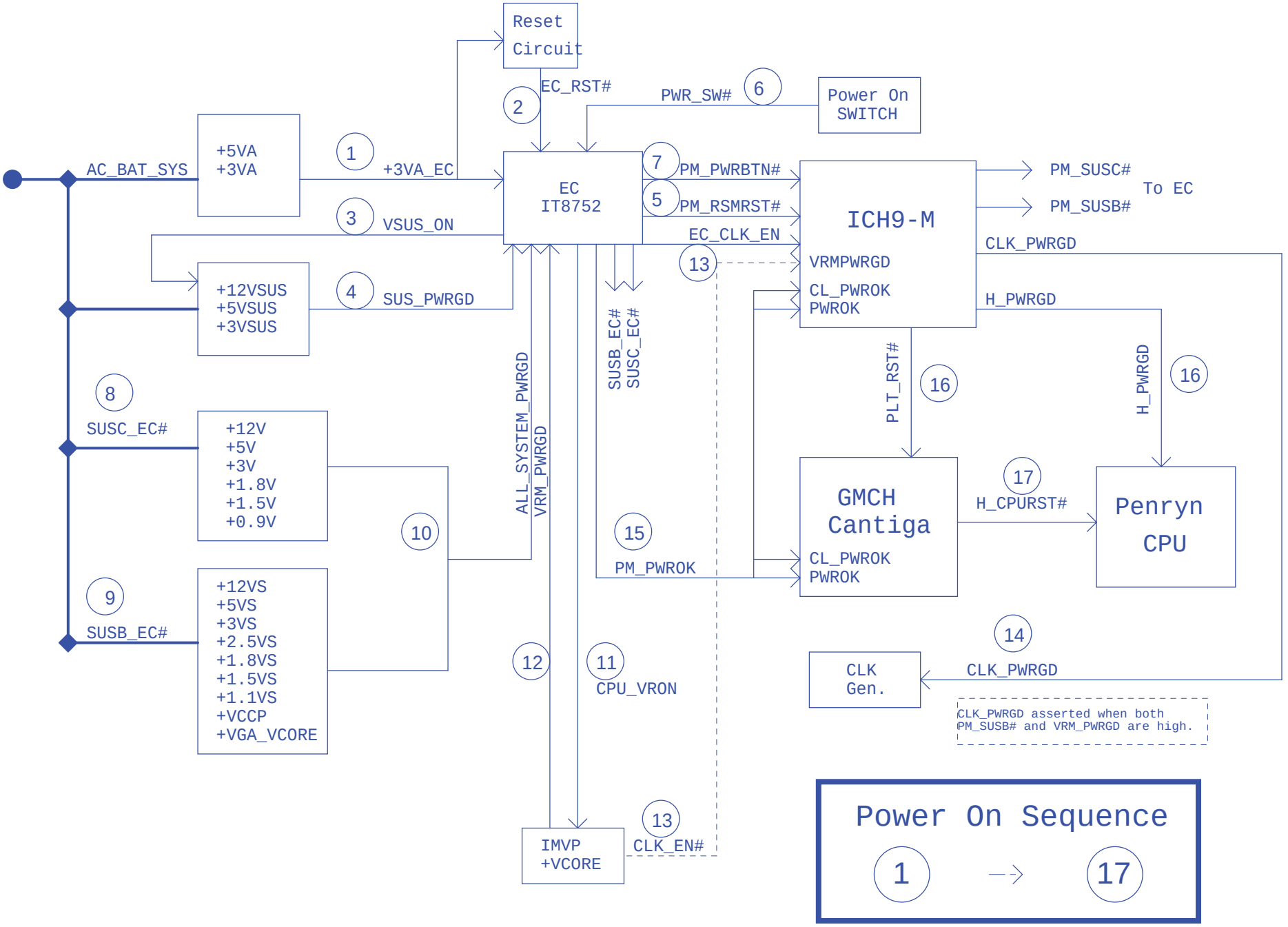
ASUSTeK COMPUTER INC. NB1	Title : EC_IT8511 (2/2)		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 31 of 101		



ASUSTeK COMPUTER INC. NB1	Title : HDMI Level Shifter	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 32 of 101	


use 8111b remove
40 mil
close to pin63 within 200 mil
close to pin64
P/N: 09G02X473522
close to pin1 with in 200 mil
60 mil
close to L3301 with in 200 mil
RTLAN_DSM_EN# ---> GPIO10 of ICH9
RTLAN_VCC33_EN --> GPIO60 of ICH9
Reserved DSM Function
DSM function note:
At S0 stage, when un-plug LAN cable, the
RTLAN_DSM_EN# will pull-low to notice the
system, then the system will pull-high the
RTLAN_VCC33_EN# to cut off the ISOLATEB pin
power.
R1207
40mil
40 mil
R1208
R1208
40mil
U3301
RTL8111C_VB_GR
Pin.33 is Clkreq# pin similar to
Clkrun function in the PCI
interface. If this function not
implemented, make this pin
floating or connect to the ground.
close to LAN CHIP
R1206
R1208
PCIE_RXN6_GLAN 21
PCIE_RXP6_GLAN 21
CLK_PCIE_LAN# 29
CLK_PCIE_LAN 29
PCIE_TXN6_C 21
PCIE_TXP6_C 21
CLK_LAN_REQ# 29
RTLAN_DSM# 22
RTLAN_DSM_EN 22
22,43,53,54 PCIE_WAKE#
5,11,21,30,43,53,54,62 BUF_PLT_RST#
X3301
25Mhz
ASUSTeK COMPUTER INC. NB1
Title : GigaLAN
Engineer: Ryan_Wang
Size Custom
Project Name N20A
Rev 1.20
Date: Monday, June 09, 2008
Sheet 33 of 101

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 34 of 101	



ASUSTeK COMPUTER INC. NB1	Title : POWER-ON SEQUENCE	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 35 of 101	

Title :

ASUSTeK COMPUTER INC. NB1

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 36 of 101

Title :

ASUSTeK COMPUTER INC. NB1

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 37 of 101

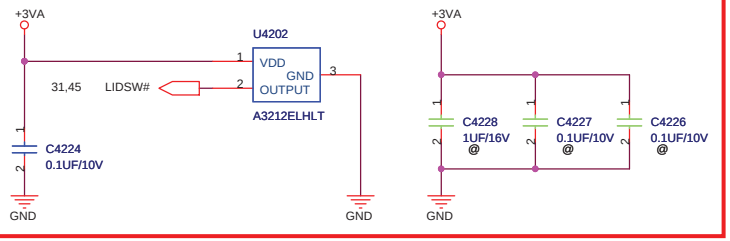
Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: Ryan_Wang
Size: Custom	Project Name: N20A
Rev: 1.20	
Date: Monday, June 09, 2008	Sheet 38 of 101

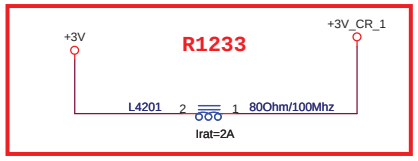
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 39 of 101	

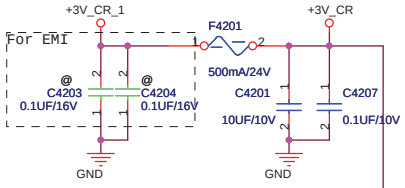
ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: Ryan_Wang
Size: Custom	Project Name: N20A
	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 40 of 101

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: Ryan_Wang
Size: Custom	Project Name: N20A
Rev: 1.20	
Date: Monday, June 09, 2008	Sheet 41 of 101

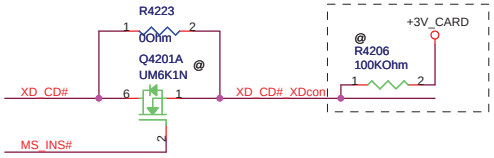
LID SENSER

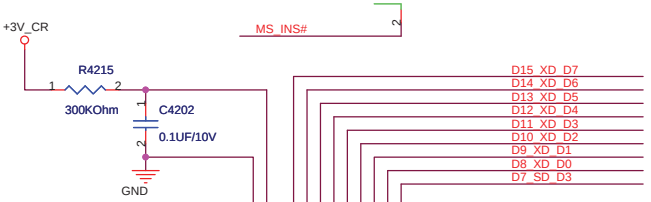


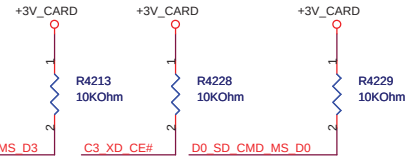


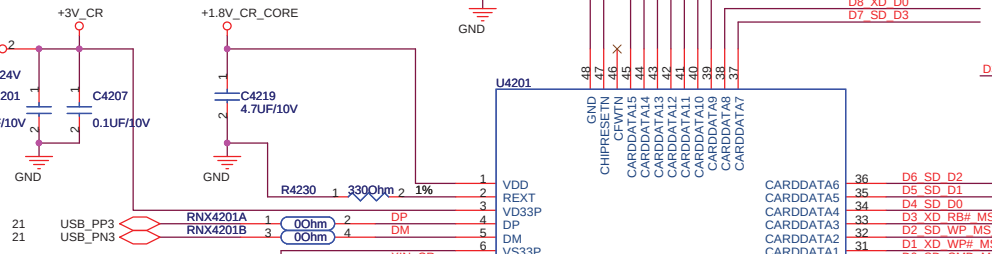


Avoid floating if XD card is not inserted

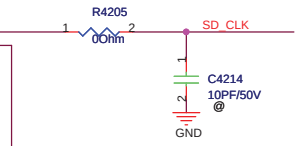


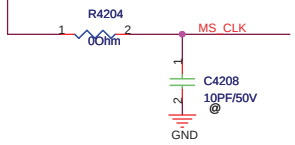


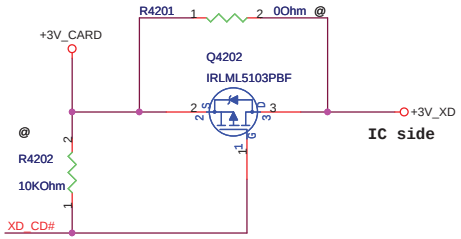


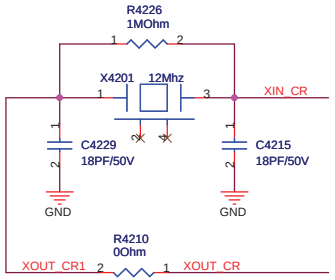


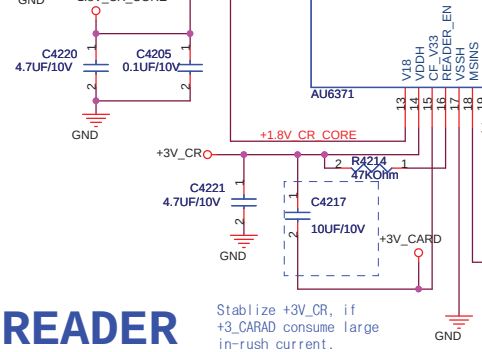
Placement near CR_CON2

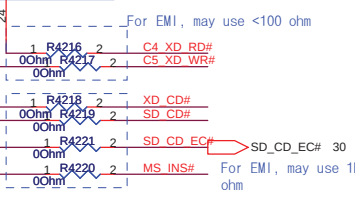






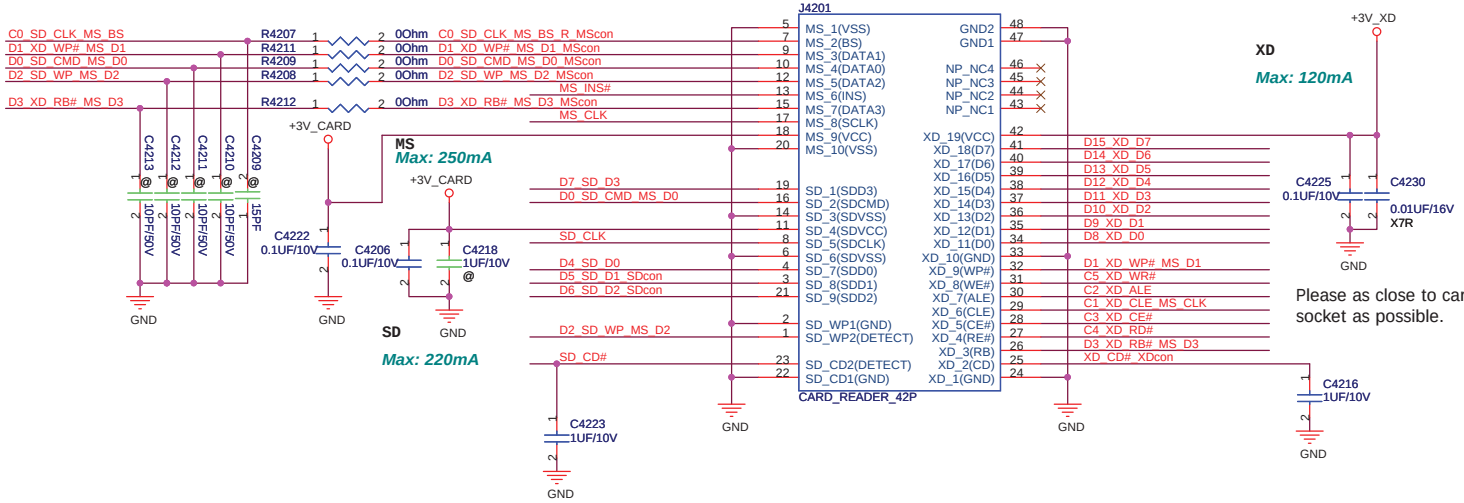






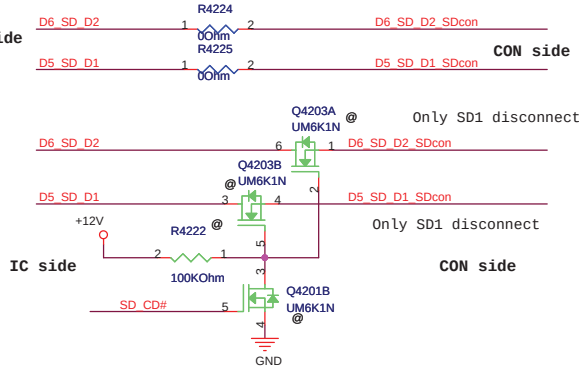
CARD READER

Stablize +3V_CR, if +3_CARAD consume large in-rush current.



Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

Only SD2 disconnect



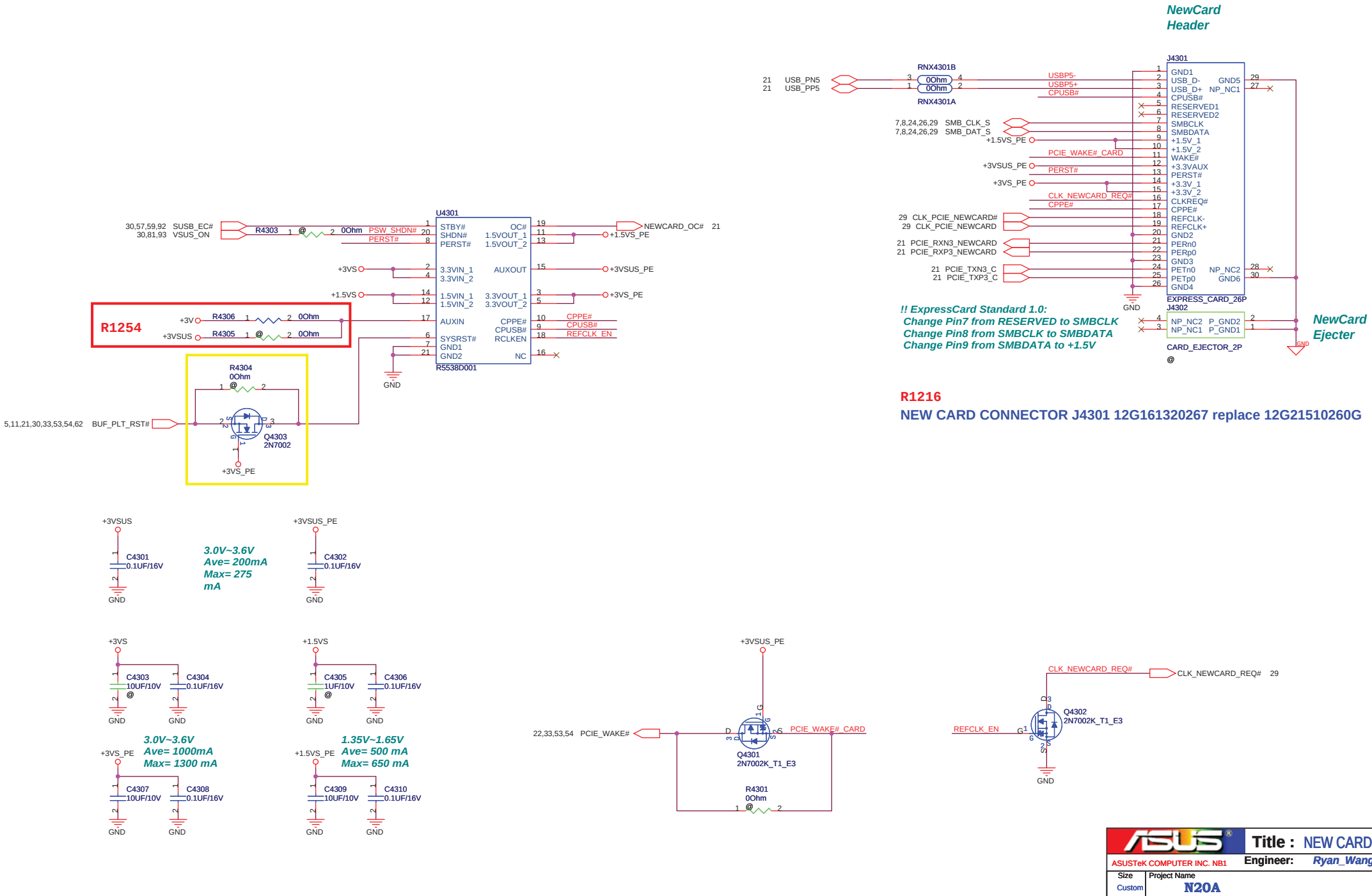
ASUSTeK COMPUTER INC. NB1

Title : CARD READER & LID

Engineer: Ryan_Wang

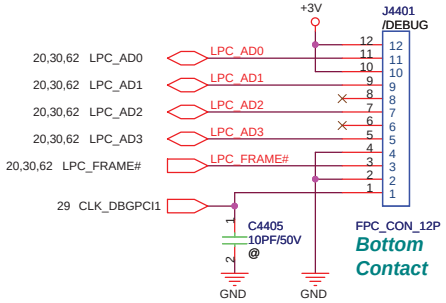
Size	Project Name	Rev
Custom	N20A	1.20

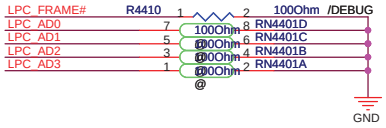
Date: Monday, June 09, 2008 Sheet 42 of 101



ASUSTeK COMPUTER INC. NB1	Title : NEW CARD	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 43 of 101	

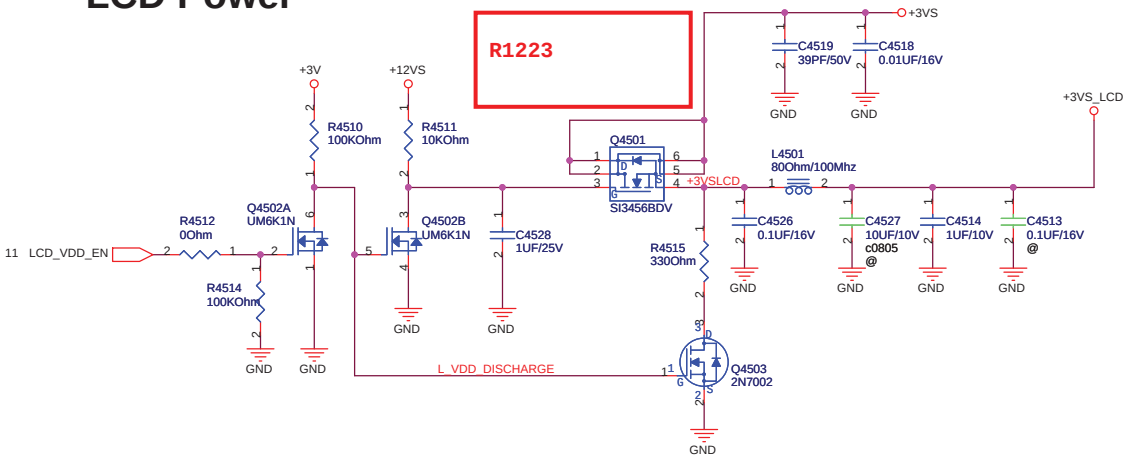
LPC DEBUG PORT

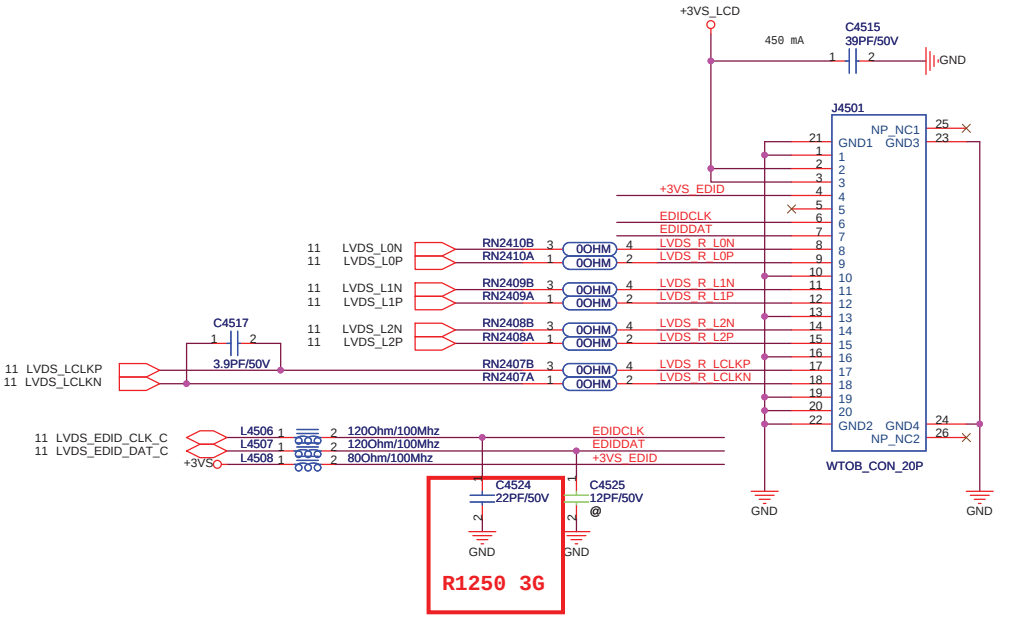


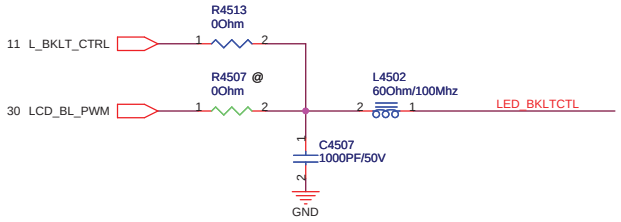


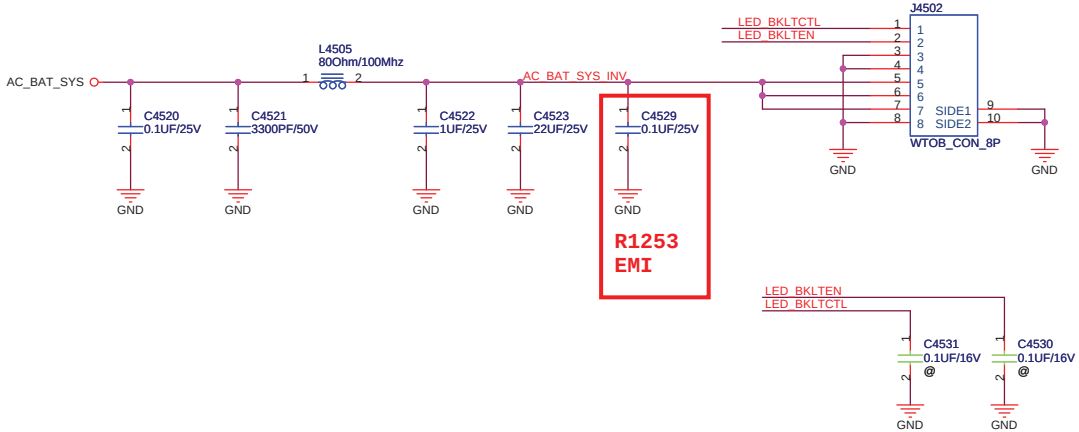
ASUSTeK COMPUTER INC. NB1	Title : DEBUG	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 44 of 101	

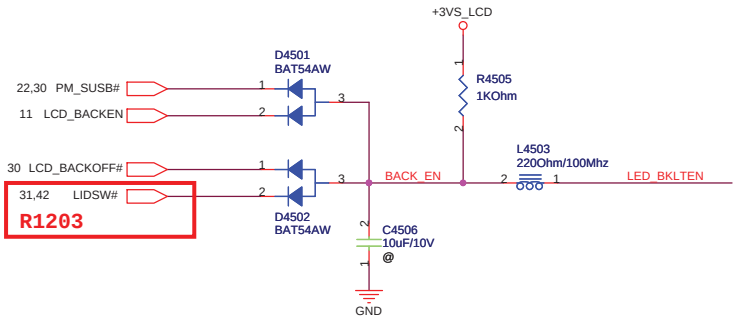
LCD Power





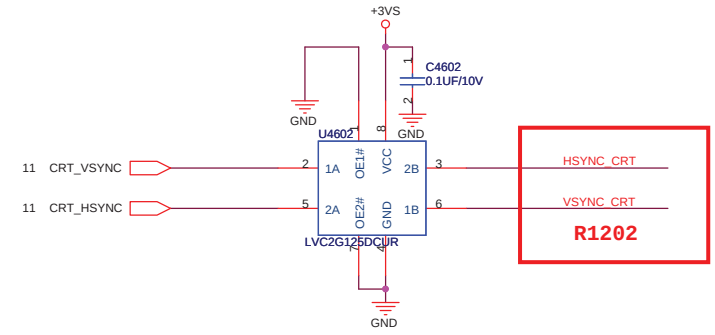


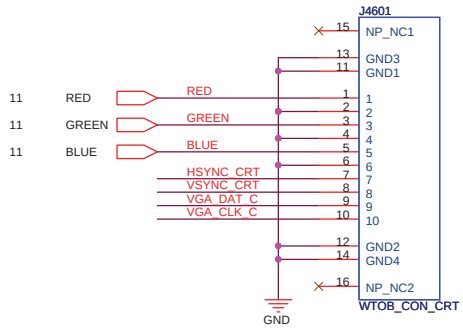


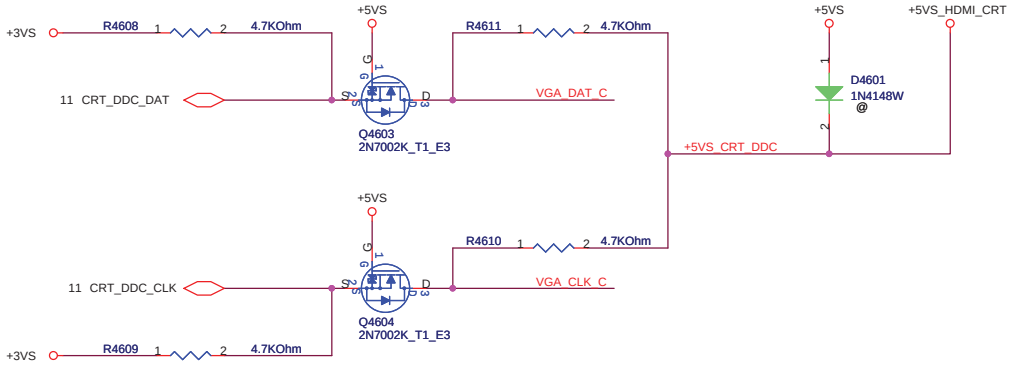


7S6P LED PANEL
+LED_VCC=3.3Vx7=23.1V
I=20mAx6=0.12A

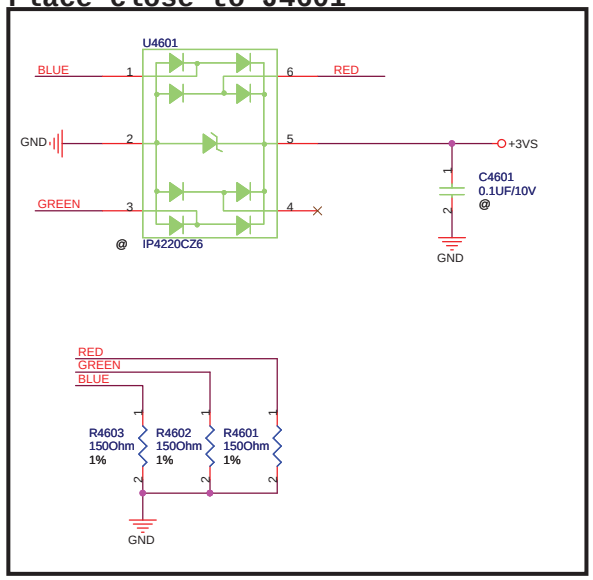
ASUSTeK COMPUTER INC	Title : LVDS (1/3)	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 45 of 101	







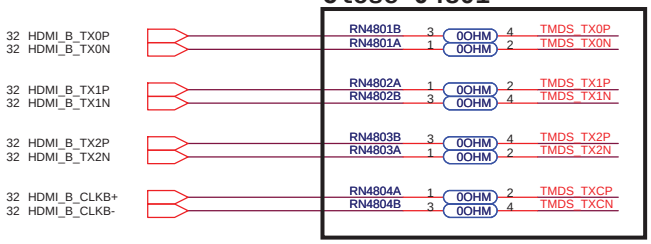
Place close to J4601

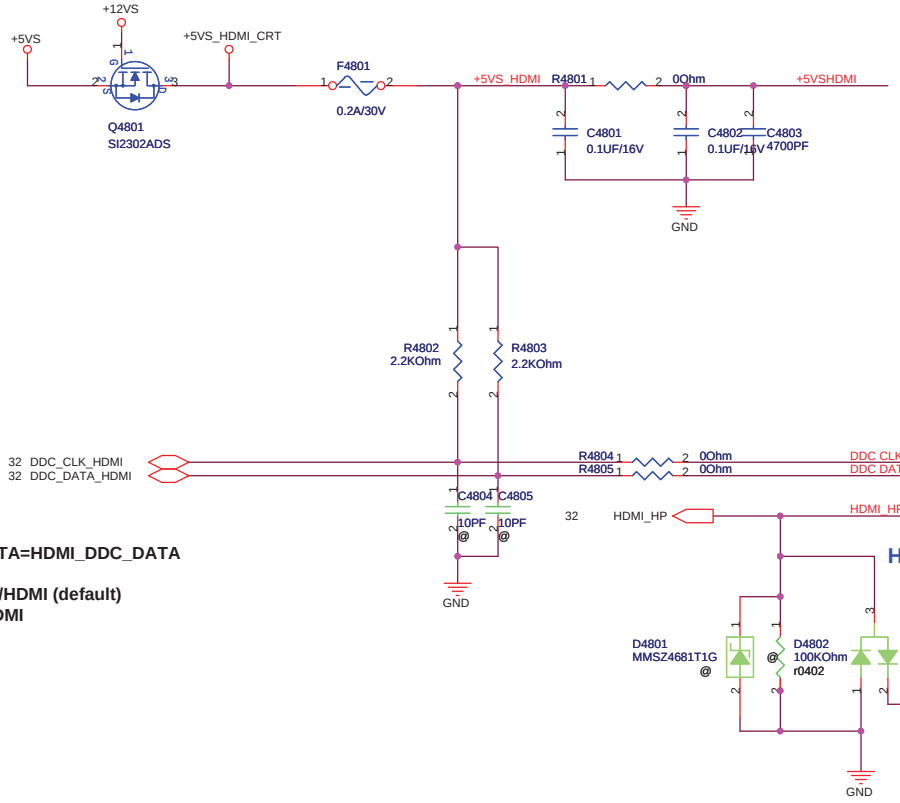


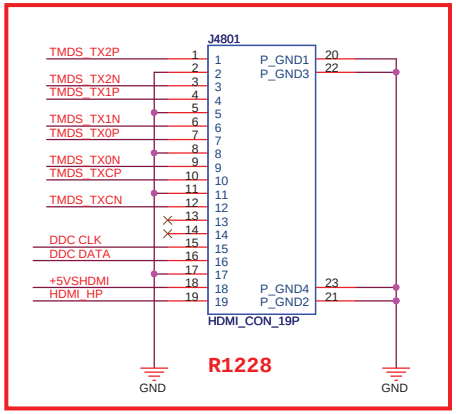
ASUSTeK COMPUTER INC	Title : CRT (2/3)	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 46 of 101	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 47 of 101	

Close J4801







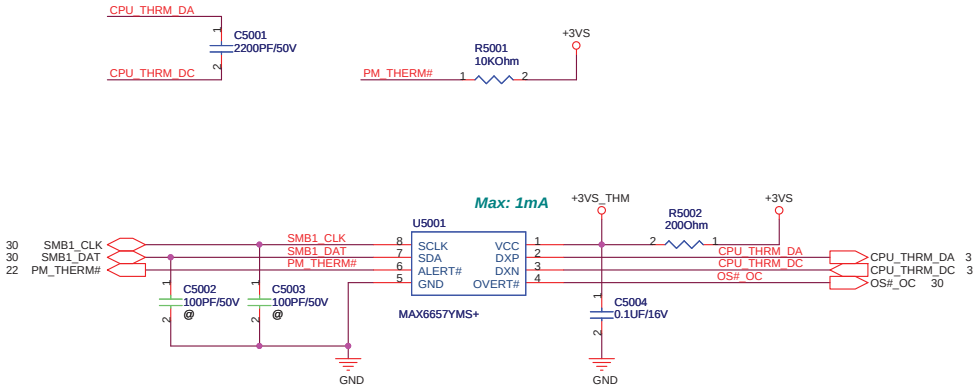
SDVO_CTRLDATA=HDMI_DDC_DATA
Strapping:
Low = No SDVO/HDMI (default)
High = SDVO/HDMI

HDMI CONNECTOR J4801 12G24110193T replace 12G24110191L.

ASUSTeK COMPUTER INC	Title : HDMI (3/3)		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 48 of 101		

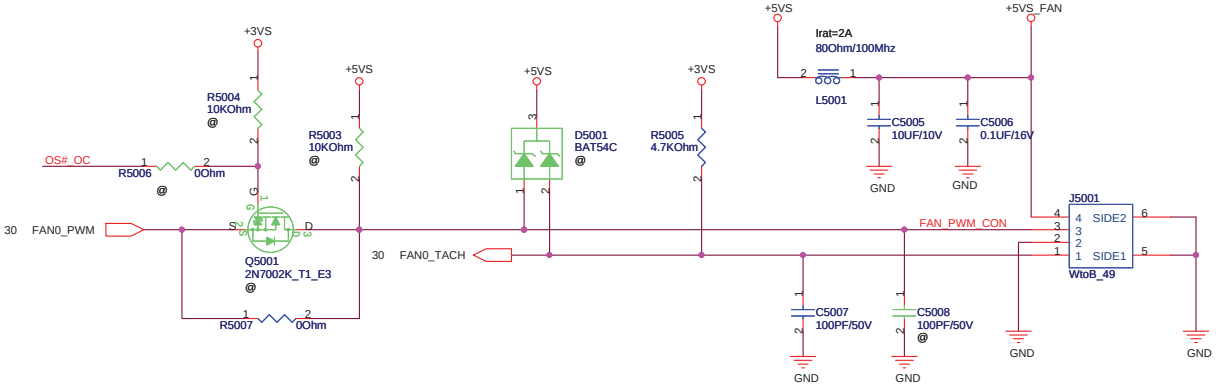
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 49 of 101	

Thermal Sensor



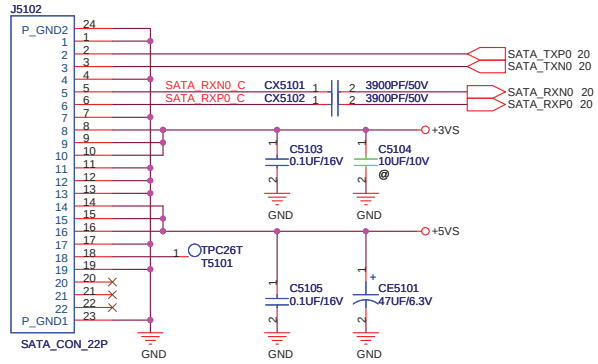
1st source: 06G023096010	TEMP.SENSOR G780P11U SOP-8	GMT
2nd source: 06G023026012	TEMP SENSOR MAX6657YMS+ SOP-8	MAXIM

DC FAN Control



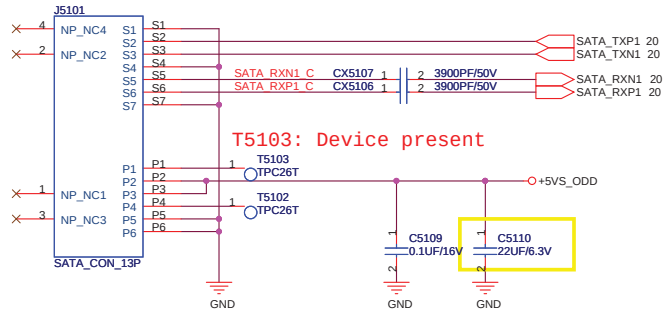
ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 50 of 101		

SATA HDD

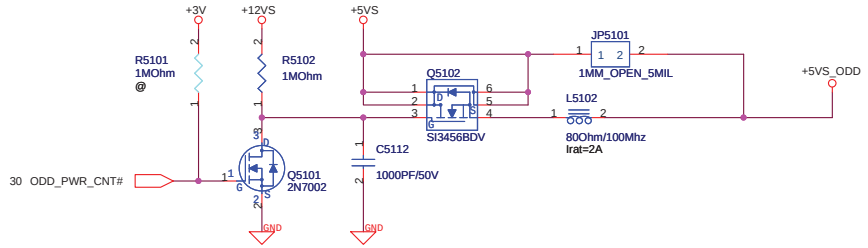


ODD

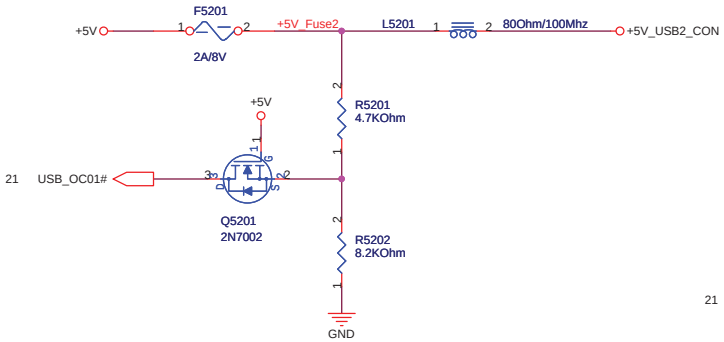
CHANGE NEW PART NUMBER

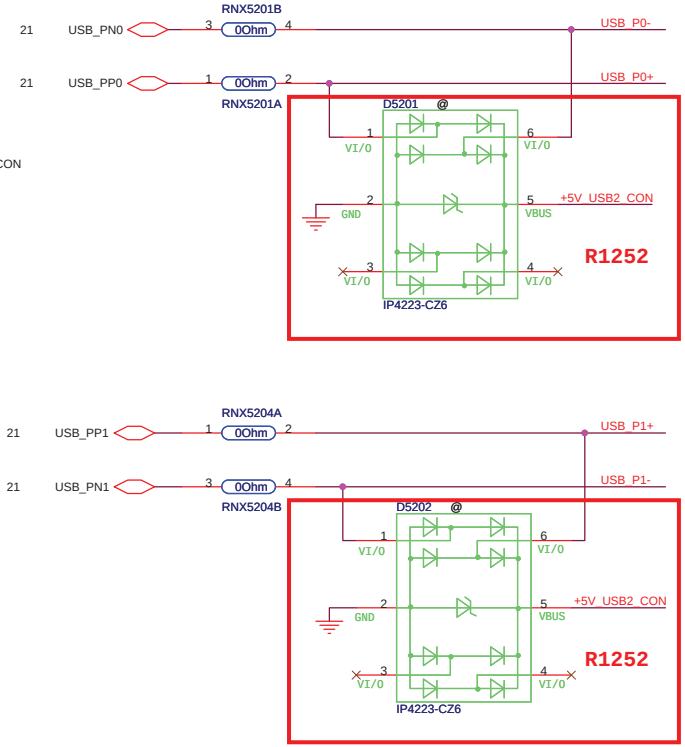


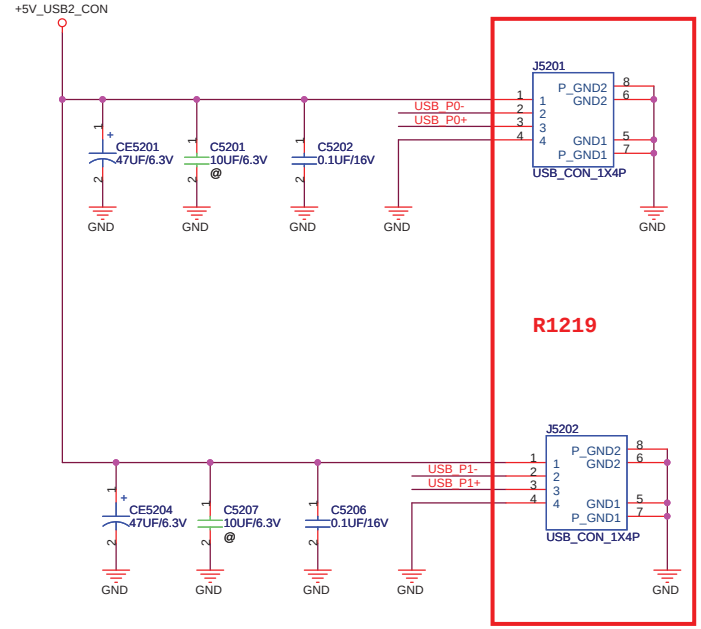
T5102 : Manufacturing Diagnostic



ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 51 of 101	

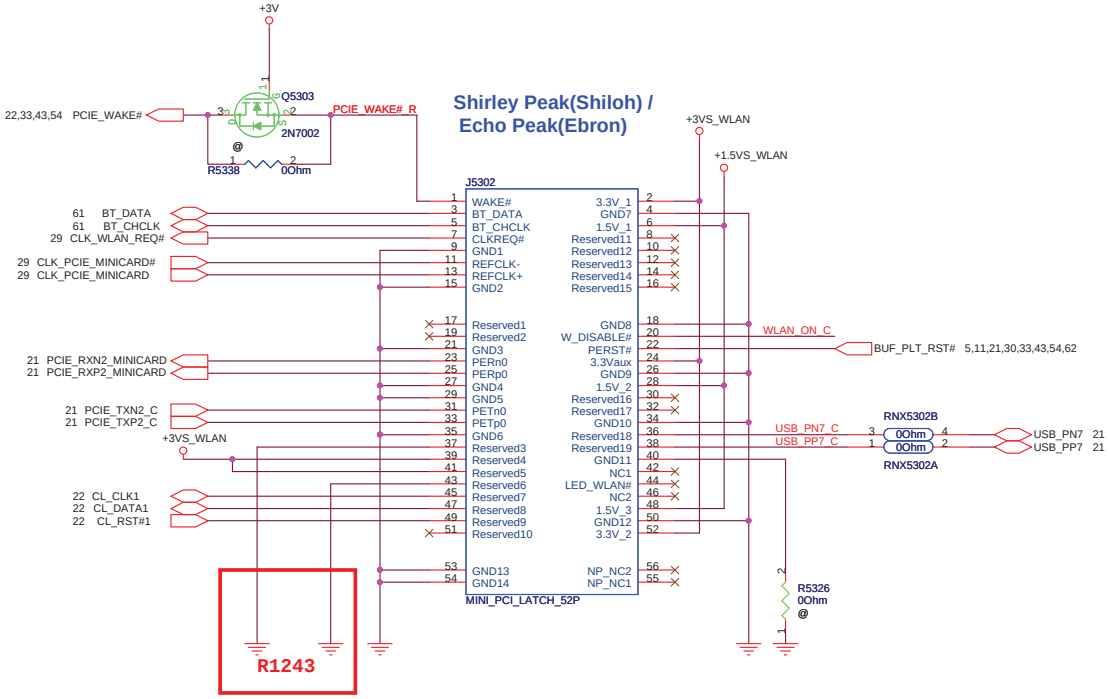


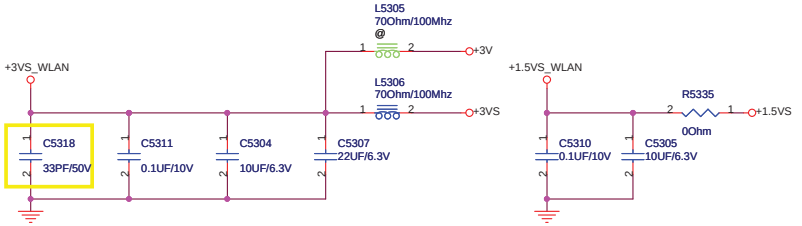


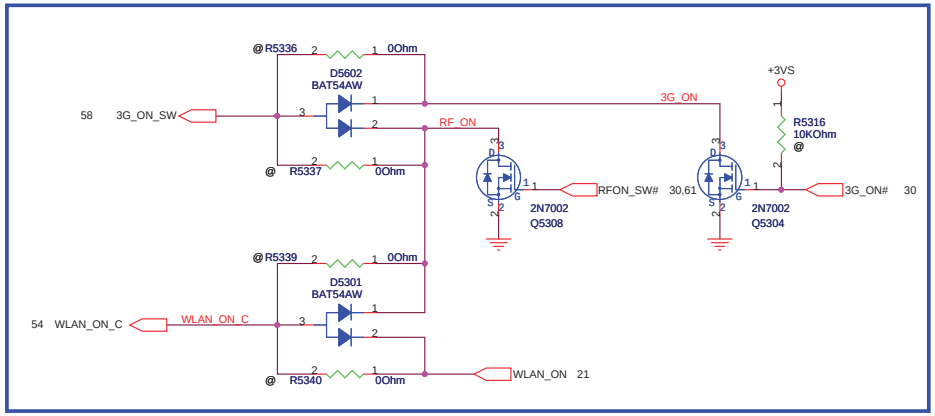


USB CONNECTOR J5201 & J5202 12G13101004Y replace 12G130011045.

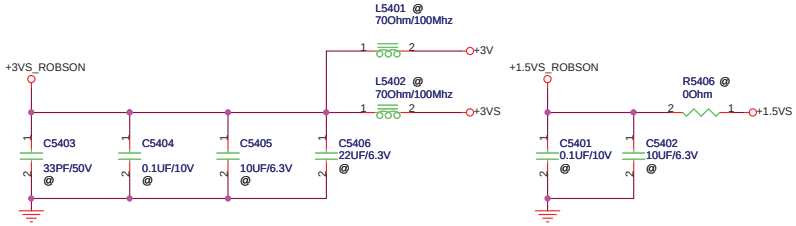
ASUSTeK COMPUTER INC. NB1	Title : USB CONN X 2	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 52 of 101	

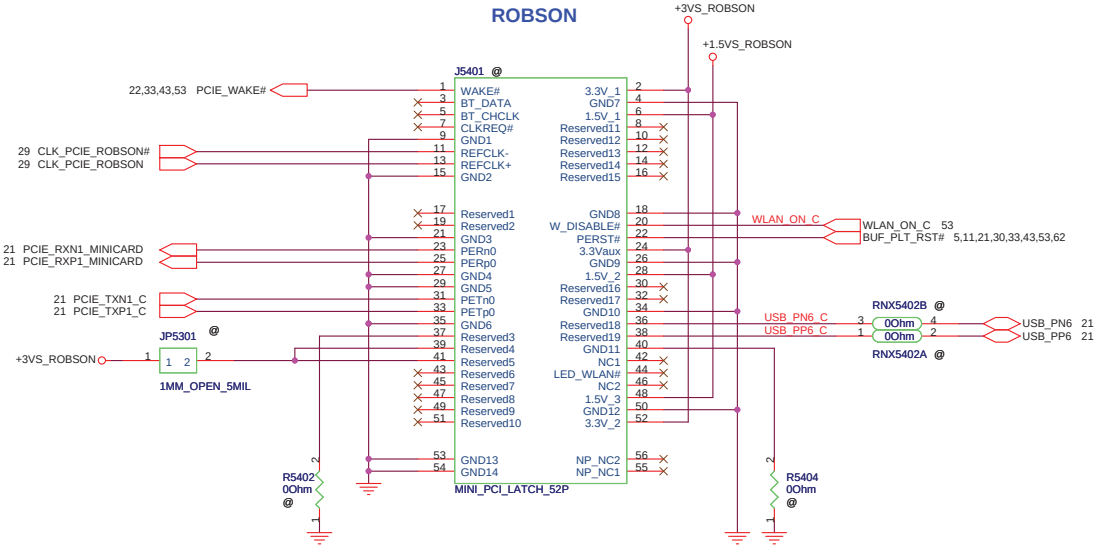






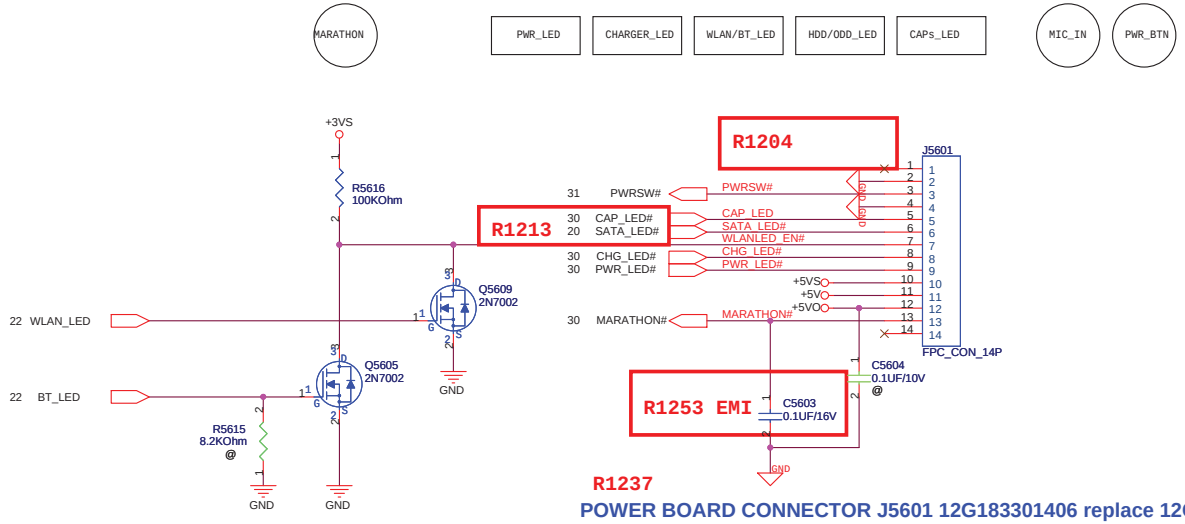
ASUSTeK COMPUTER INC. NB1	Title : Minicard card	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 53 of 101	



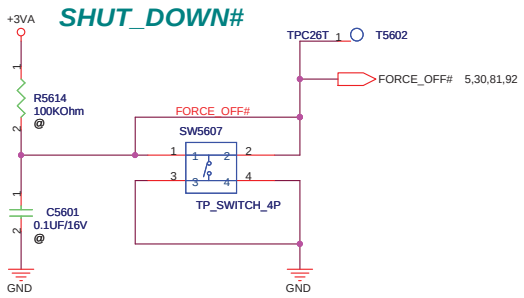


ASUSTeK COMPUTER INC. NB1	Title : Minicard card	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 54 of 101	

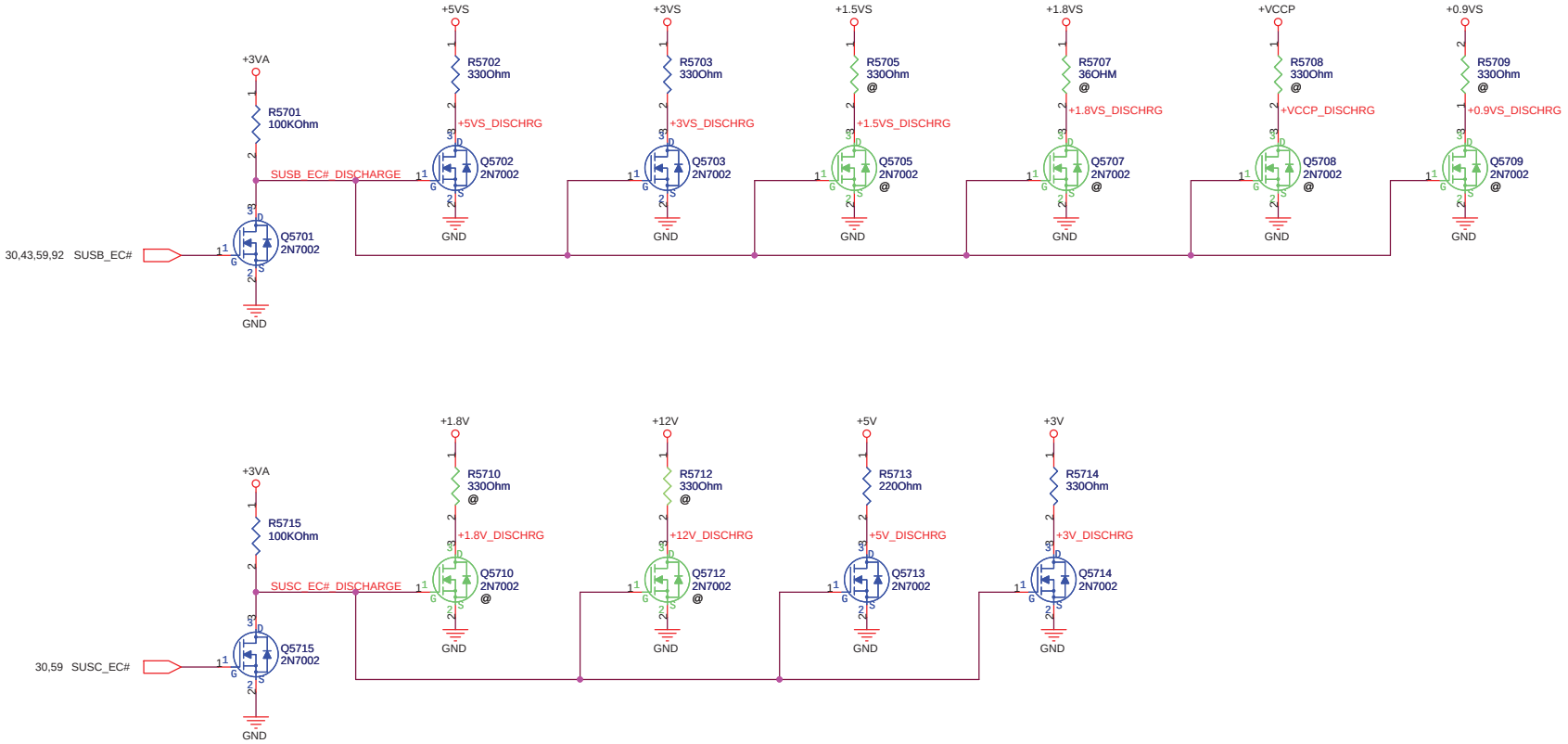
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 55 of 101	



POWER BOARD CONNECTOR J5601 12G183301406 replace 12G183301404



ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 56 of 101	



ASUSTeK COMPUTER INC. NB1

Title : DISCHARGE

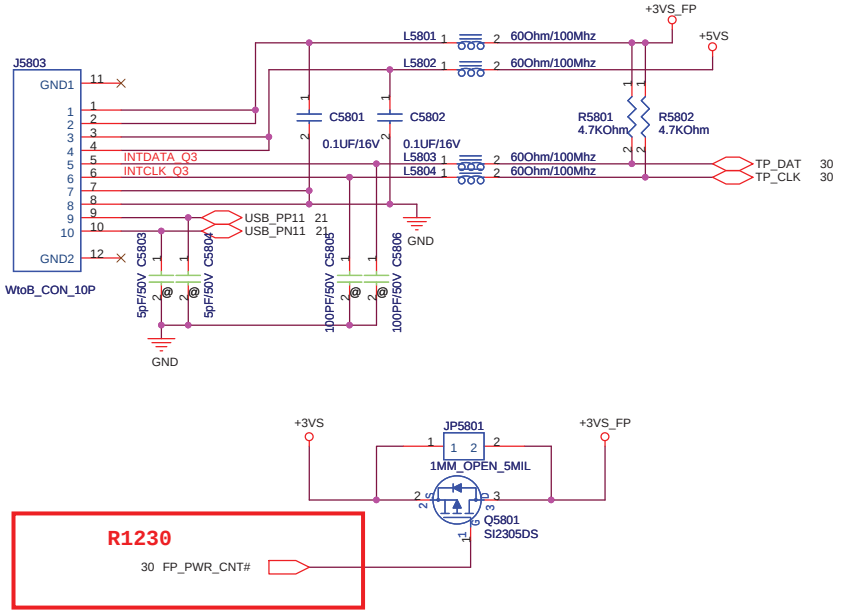
Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

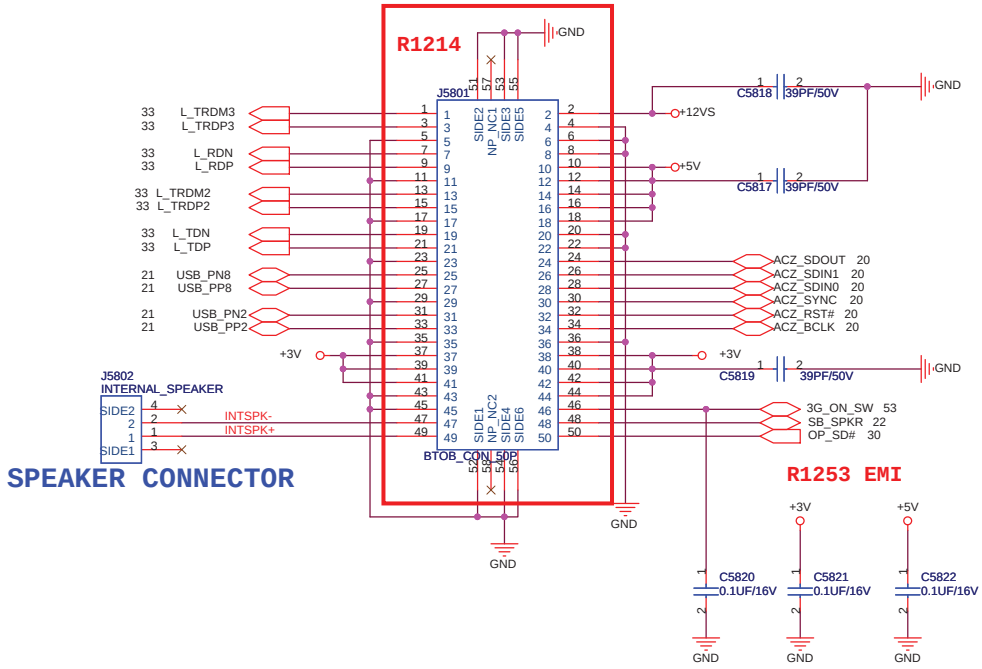
Date: Monday, June 09, 2008 Sheet 57 of 101

SUBSYS CONN

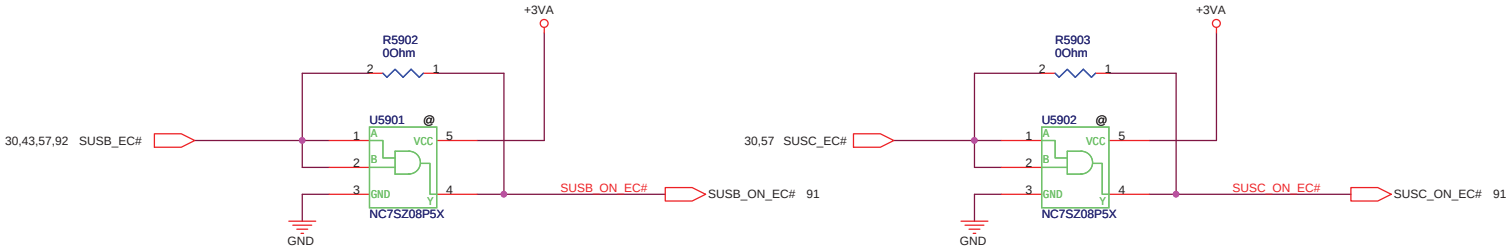
Touch Pad Connector & Finger Printer



Audio Chip & 3G Card & GigaLAN & USB Connector

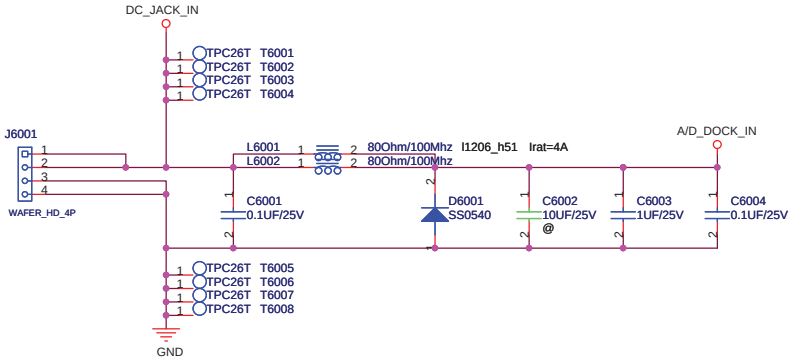


ASUSTeK COMPUTER INC. NB1	Title : SUB BOARD	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 58 of 101	



ASUSTeK COMPUTER INC. NB1	Title : Sequence Control Logic	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 59 of 101	

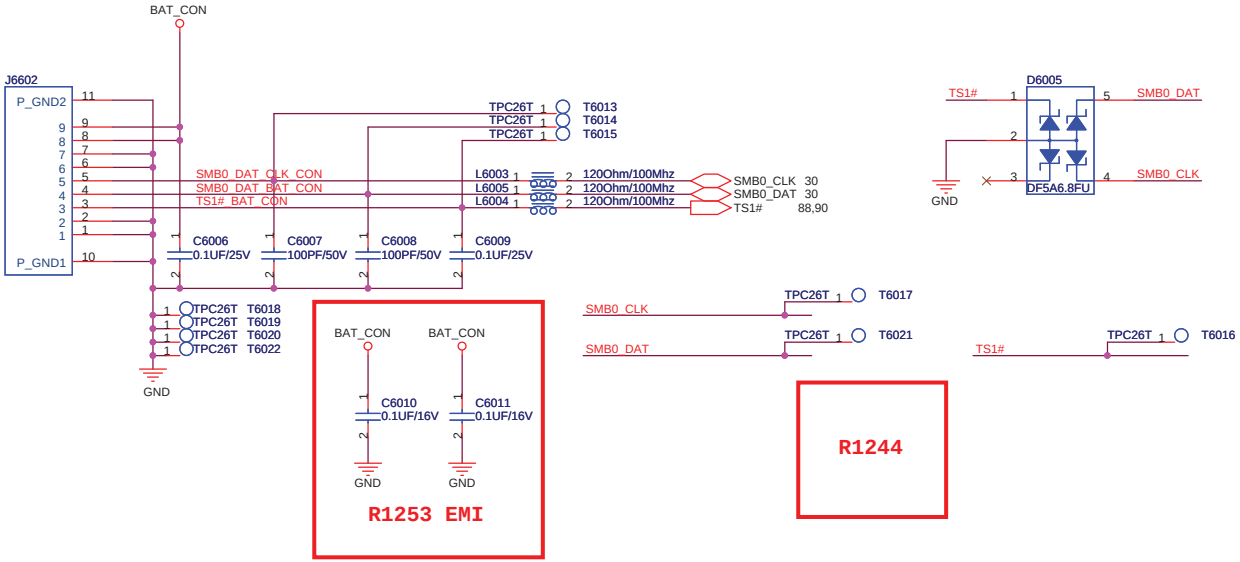
DC IN



R1218

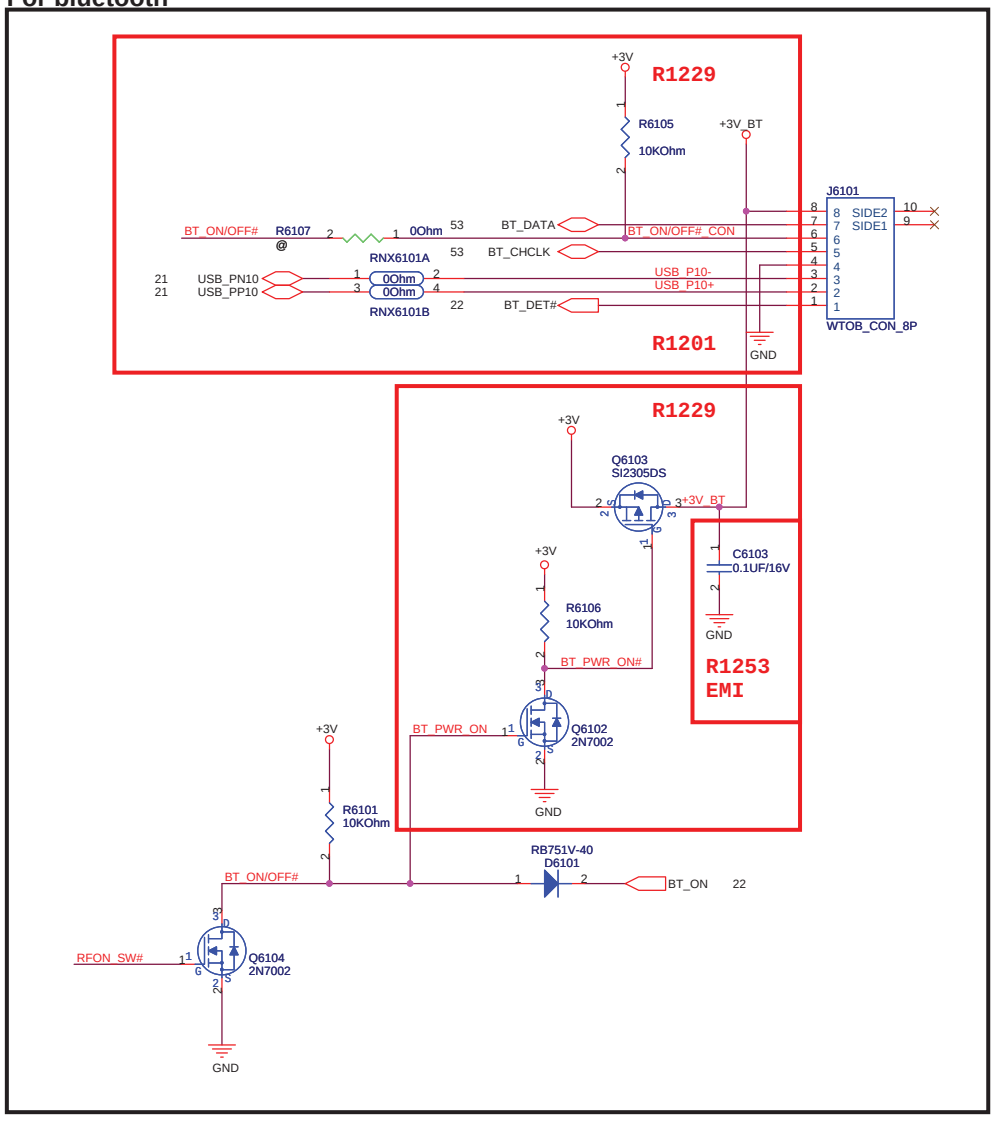
DC-IN CONNECTOR J6001 12G171020041 replace 12G080310046

BAT IN

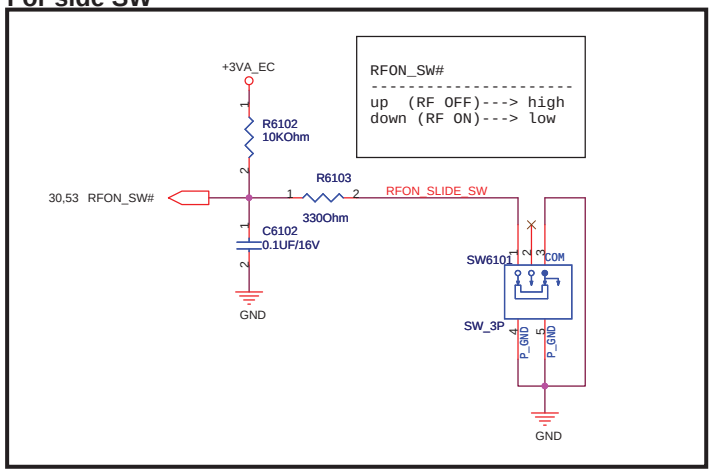


ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 60 of 101		

For bluetooth

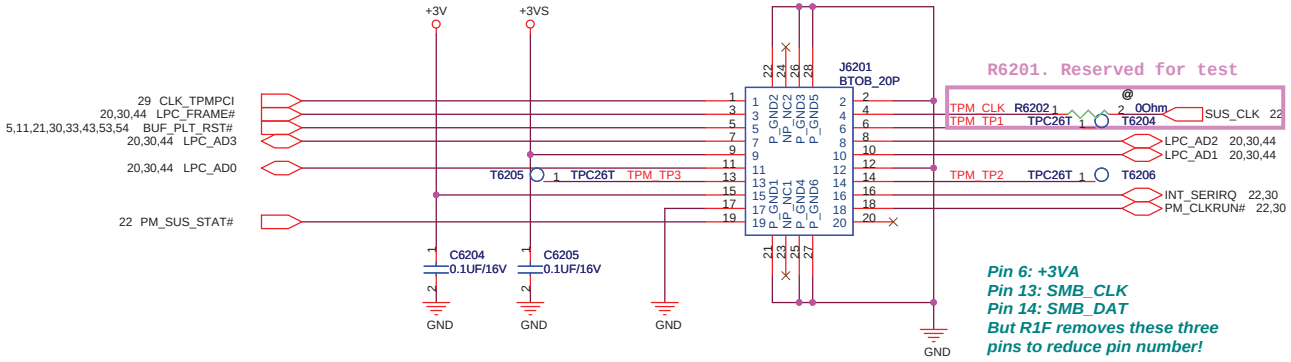


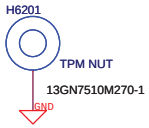
For side SW



ASUSTeK COMPUTER INC. NB1	Title : BlueTooth	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 61 of 101	

For TPM module





ASUSTeK COMPUTER INC. NB1	Title : TPM	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 62 of 101	

Title :

ASUSTeK COMPUTER INC. NB1

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 63 of 101

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Ryan_Wang	
Size: A	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 64 of 101	

FOR WLAN (TOP)

H5303
U5F-M-EXPREE

H5304
U5F-M-EXPREE

GND

GND

FOR WLAN (BOTTOM)

H5401 @
U5F-M-EXPREE

GND

H6506 1 @ CR303X260D110
H6507 1 @ C236D110
H6508 1 @ CR260X276D110
H6509 1 @ C236D110
H6510 1 @ C236D110
H6511 1 @ C236D110
H6512 1 @ CR303X260D110
H6513 1 @ CR303X260D110
H6514 1 @ C236D110

GND

H6517 1 @ CT307CRB341X299D110
H6526 1 @ CR236X258D110
H6527 1 @ CR236X258D110
H6528 1 @ CR236X258D110

GND

H6501 1 @ C102D102N
H6502 1 @ C102D102N

H6518 1 @ CT260CB170D150
H6519 1 @ CT260CB170D150
H6520 1 @ CT260CB170D150
H6521 1 @ CT260CB170D150

CPU SCREW HOLE

GND

H6530 1 @ HOLE_NPTH

GPU SCREW NUT

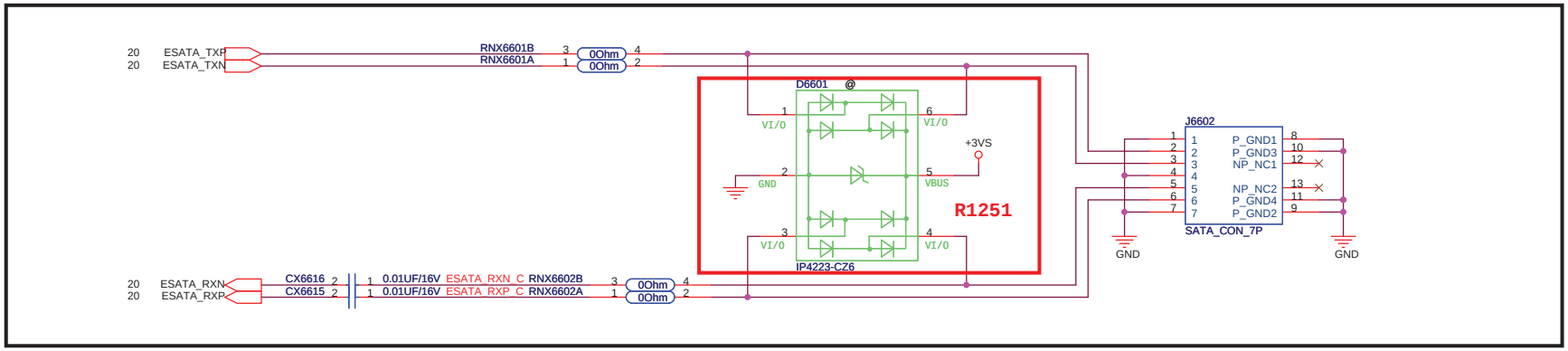
H6522 @ 1 CT236B276X295D110

GND

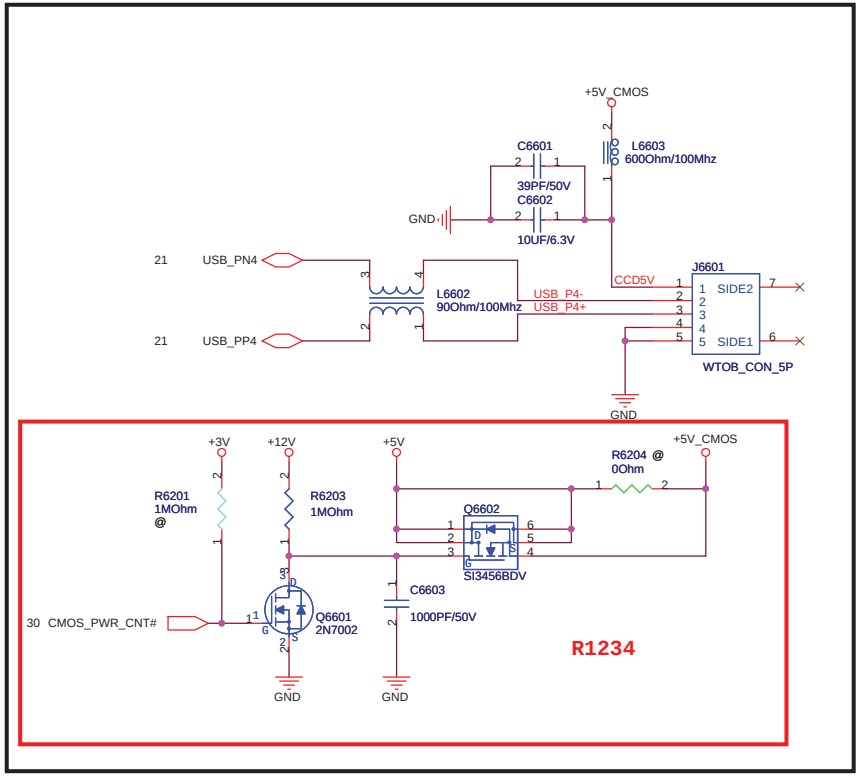
GPU NUT P/N: 13G021036001
H22 SCREW HOLE P/N: S01907
H23 SCREW HOLE P/N: S01821

ASUSTeK COMPUTER INC. NB1	Title: MDC NUT & Hinksink NUT	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 65 of 101	

E-SATA Connector



CMOS Camera Connector



ASUSTeK COMPUTER INC. NB1	Title : E-SATA & CMOS		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 66 of 101		

C6701
+3VA — 2 — 1 — GND
0.1UF/10V

C6702
+3VA — 2 — 1 — GND
0.1UF/10V

C6703
+3VSUS — 2 — 1 — GND
0.1UF/10V

C6704
+VCORE — 2 — 1 — GND
0.1UF/10V

C6705
+VCORE — 2 — 1 — GND
0.1UF/10V

C6706
+VCORE — 2 — 1 — GND
0.1UF/10V

C6707
+3VSUS — 2 — 1 — GND
0.1UF/10V

C6708
+VCCP — 2 — 1 — GND
0.1UF/10V

C6709
+VCCP — 2 — 1 — GND
0.1UF/10V

C6710
+VCCP — 2 — 1 — GND
0.1UF/10V

C6711
+3VSUS — 2 — 1 — GND
0.1UF/10V

C6712
+5V — 2 — 1 — GND
0.1UF/10V

C6713
+5V — 2 — 1 — GND
0.1UF/10V

C6714
+VCORE — 2 — 1 — GND
0.1UF/10V

C6715
+VCORE — 2 — 1 — GND
0.1UF/10V

C6716
+VCORE — 2 — 1 — GND
0.1UF/10V

C6717
+3V — 2 — 1 — GND
0.1UF/10V

C6718
+1.5VS — 2 — 1 — GND
0.1UF/10V

C6719
+1.5VS — 2 — 1 — GND
0.1UF/10V

C6720
+3VSUS — 2 — 1 — GND
0.1UF/10V

C6721
+1.8V — 2 — 1 — GND
0.1UF/10V

C6731
+5VS — 2 — 1 — +3V
0.1UF/10V

C6732
+5VS — 2 — 1 — +3V
0.1UF/10V

C6733
+VCCP — 2 — 1 — +3V
0.1UF/10V

C6734
+VCCP — 2 — 1 — +3VS
0.1UF/10V

C6735
+VCCP — 2 — 1 — +3VS
0.1UF/10V

C6736
+5VS — 2 — 1 — +3V
0.1UF/10V

C6737
+VCCP — 2 — 1 — +3VS
0.1UF/10V

C6738
+VCCP — 2 — 1 — +3VS
0.1UF/10V

C6739
+5VS — 2 — 1 — +3VS
0.1UF/10V

C6740
+5VS — 2 — 1 — +3VS
0.1UF/10V

C6741
+5VS — 2 — 1 — +3VS
0.1UF/10V

C6742
+VCCP — 2 — 1 — +3V
0.1UF/10V

C6747
+5VS — 2 — 1 — +3V
0.1UF/10V

C6748
+5VS — 2 — 1 — +3V
0.1UF/10V

C6749
+5VS — 2 — 1 — +3V
0.1UF/10V

C6750
+1.8V — 2 — 1 — +3VS
0.1UF/10V

C6751
+3V — 2 — 1 — +3VS
0.1UF/10V

C6752
+3V — 2 — 1 — +3VS
0.1UF/10V

C6753
+3V — 2 — 1 — +3VS
0.1UF/10V

C6754
+3V — 2 — 1 — +3VS
0.1UF/10V

+0.9VS — C6755 0.1UF/16V — GND
+0.9VS — C6757 0.1UF/16V — GND

R1253 EMI

ASUSTeK COMPUTER INC. NB1

Title : EMI CAPS

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 67 of 101

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: Ryan_Wang
Size: Custom	Project Name: N20A
Rev: 1.20	
Date: Monday, June 09, 2008	Sheet 68 of 101

N20A Revision History

Rev	Date	Description
1.1	2008/3/1	S/R Release
1.2	2008/6/10	E/R Release 1. Modify BT253 pin1 and pin4 assignment with new BT253 cable. (P61) 2. Exchange CRT buffer output VSYNC & HSNC signal. (P46) 3. Modify signal net from LID_SW# to LIDSW#. (P45) 4. Delete Power Board connector J5601 pin1 LID_SW# signal . (P56) 5. Add LPC TPM Module schematic . (P22,P29,P62) 6. Mount Q3303 for RTL8111C BUF_PLT_RST# leakage voltage. (P33) 7. Exchange +EVDD12 R3321 from bead to 0 Ohm for RTL8111C. (P33) 8. Add C3326 0.1uF for design IP and delete power control for LAN IC (P33) 9. Modify SCX338 & SCX339c ap value from 0.01 to 0.22uF for GMT suggestion. (P98) 10. Modify SC403 & SC405 cap value from 1uF and 0.47uF for GMT suggestion. (P99) 11. Modify SR408 & SR406 value from 47K to 24K Ohm for Gain suggestion. (P99) 12. Modify ACZ_RST# control signal for AMP mute function. (P99) 13.Delete CAP_LED MOS for costdown issue . (P30,P56) 14.Change Part Number 12G16022050S for ME request . (P58 & P96) 15.Unmount control THRO_CPU schematic from EC PM_THERM#_EC. (P3) 16. NEW CARD CONNECTOR J4301 12G161320267 replace 12G21510260G.(P43) 17.POWER BOARD CONNECTOR J5601 12G183301406 replace 12G183301404. (P56) 18.DC-IN CONNECTOR J6001 12G171020041 replace 12G080310046.(P60) 19.USB CONNECTOR J5201 & J5202 12G13101004Y replace 12G130011045. (P52) 20. Modify L0401 to 0Ohm for Intel schematic suggestion.(P4) 21. Modify DDRII DIMM 0.1uF capacitor location for layout issue.(P9) 22. Modify SM_LINK0 and SM_LINK1 schematic from P24 to P22.(P22,P24) 23. Delete Old LCD discharge schematic D4503 and R4509.(P45) 24. Delete unmount control signal PM_THERM# from CPU & ECschematic.(P22) 25. Delete unmount control signal CLK_EN# from +VCORE ICschematic.(P22) 26. Modify HDMI level shifter schematic for second source request.(P32) 27. Unmount HDCP BOM.(P26) 28. HDMI CONNECTOR J4801 12G24110193T replace 12G24110191L..(P48) 29. Modify BT253 power control function for power saving. (P61) 30. Modify FINGER PRINTER GPIO power control function for power saving. (P30,P58) 31. Exchange BATSEL_CAP28# GPIO power control function for power saving. (P30) 32. Modify GPIO netname CMOS_PWR_CNT# . (P30) 33. Delete Card Reader power control function for power saving. (P42) 34. Modify power control function for power saving. (P66) 35. Delete LAN RTL8111C power control function for power saving. (P33) 36. Modify Intel GM45 pin B2 to NC and pin AJ6 to GND.(P15,P11) 37. Modify iAMT_MPWROK signal for Intel suggest schematic. (P11,P22,P30) 38. Modify iTPM SPI_SI connect to +3VS.(P21) 39. Add PM_PWROK R2234 10K Ohm to GND for Design IP suggestion. (P22) 40. Unmount C2328 10uF for Intel LAN IC power plane.(P23) 41. Add +5VSUS termination 10 Ohm for Intel suggested schematic .(P23) 42. Modify iTPM SPI_CLK termonation R2505 to 0 Ohm.(P25) 43. Delete resistor to GND for Shirley and Echo peak module.(P53) 44. Delete varistor for battery SMB_DAT and SMB_CLK signal.(P60) 45.Unmount SR3616 and SR315 for realtek suggestion.(P99) 46. Modify SR502 to 1K Ohm for realtek suggest 1K Ohm for ESD (P100) 47. Modify SC607 and SC608 to 100PF/250Vfor Design IP.(P101)

Rev	Date	Description
		48. Modify 0805 0Ohm betwen GND_LAN and GND_S.(P101) 49. Modify MARATHON# to +3VA power plane for express gate. (P30) 50. Add C2921 & C2924 & C2925 & C4524 for 3G request. (P45) 51. Exchange USB ESD IC D6601 to IP4223 for cost down issue.(P66) 52. Exchange USB ESD IC D5201 and D5202 to IP4223 for cost down issue.(P52) 53. Add 0.1uF C4529 & C5603 & C5821 & C5822 & C6010 & C6103 & C6103 & C6755 and C6757 for EMI request.(P45,P56,P58,P66,P61,P67) 54. Modify NEWCARD Power switch AUXIN pin17 to +3V for winbond second source.(P43) 55.Modify EC8752 pin GPJ4 to DRAM_THROTTLE# function.(P30)
1.2	2008/5/29	Power Note : 1. R9106 from 27k change to 22k. 2. R9109 from 56k change to 62k. 3. R8035 0 ohm deleted. Because EE no need CLK_EN# signal. 4. C8808 from 1206 size change to 0805 size.(11G235247512320) 5. Q8007,Q8000,Q8004,Q8003 from IRF7413ZPBF change to IRF8714PBF for cost down. 6. Q8001,Q8005,Q8006,Q8002 from IRF7836PBF change to IRF8736PBF for cost down. 7. R8214 from 95.3k change to 82.5k.

ASUSTeK COMPUTER INC. NB1

Title : HISTORY

Engineer: Ryan_Wang

Size	Project Name	Rev
Custom	N20A	1.20

Date: Tuesday, June 10, 2008 Sheet 69 of 101

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: U6V	Rev: 1.0
Date: Monday, June 02, 2008	Sheet 70 of 101	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: U6V	Rev: 1.0
Date: Monday, June 02, 2008	Sheet 71 of 101	

ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: U6V		Rev: 1.0
Date: Monday, June 02, 2008	Sheet 72 of 101		

ASUSTeK COMPUTER INC. NB1			Title :	
			Engineer:	<OrgAddr1>
Size	Project Name			Rev
Custom	U6V			1.0
Date: Monday, June 02, 2008		Sheet 73 of 101		

ASUSTeK COMPUTER INC. NB1		Title :	
		Engineer:	<OrgAddr1>
Size: Custom	Project Name: U6V		Rev: 1.0
Date: Monday, June 02, 2008		Sheet 74 of 101	

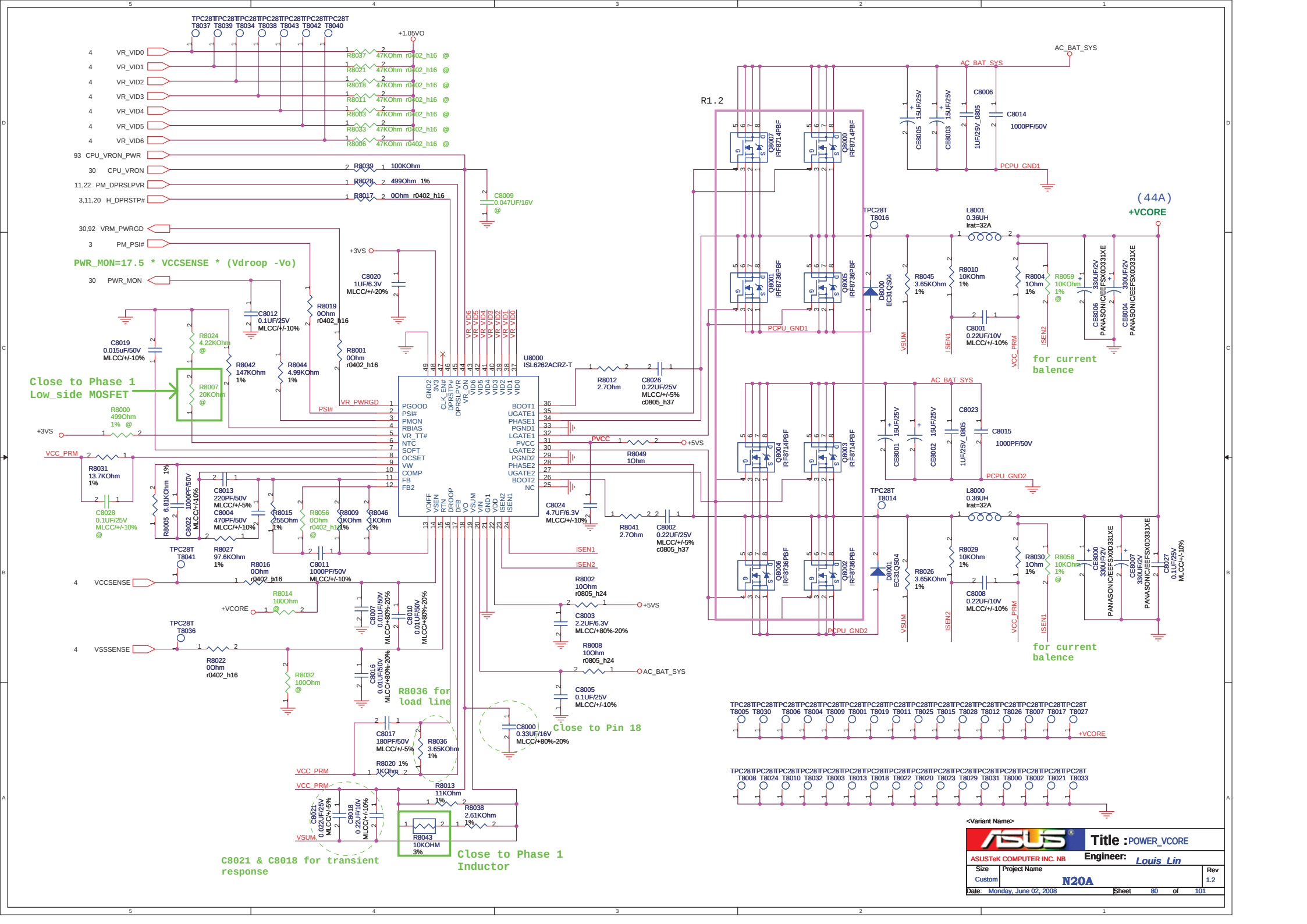
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: U6V	Rev: 1.0
Date: Monday, June 02, 2008	Sheet 75 of 101	

ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: Custom	Project Name: U6V	Rev: 2.0
Date: Monday, June 02, 2008	Sheet 76 of 101	

ASUSTeK COMPUTER INC. NB1	Title : Cantiga-POWER(5)			
	Engineer: <OrgAddr1>			
Size: A	Project Name: U6V			Rev: 1.0
Date: Monday, June 02, 2008		Sheet 77 of 101		

ASUSTeK COMPUTER INC. NB1	Title : Cantiga-POWER(5)	
	Engineer: <OrgAddr1>	
Size: A	Project Name: U6V	Rev: 1.0
Date: Monday, June 02, 2008	Sheet 78 of 101	

ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: A	Project Name: U6V		Rev: 1.0
Date: Monday, June 02, 2008	Sheet 79 of 101		


U8000 ISL6262ACRZ-T
PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to Phase 1 Low_side MOSFET
R8036 for load line
Close to Pin 18
C8021 & C8018 for transient response
Close to Phase 1 Inductor
for current balence
for current balence
(44A)
+VCORE
R1.2
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Louis Lin
Project Name N20A
Rev 1.2
Date: Monday, June 02, 2008
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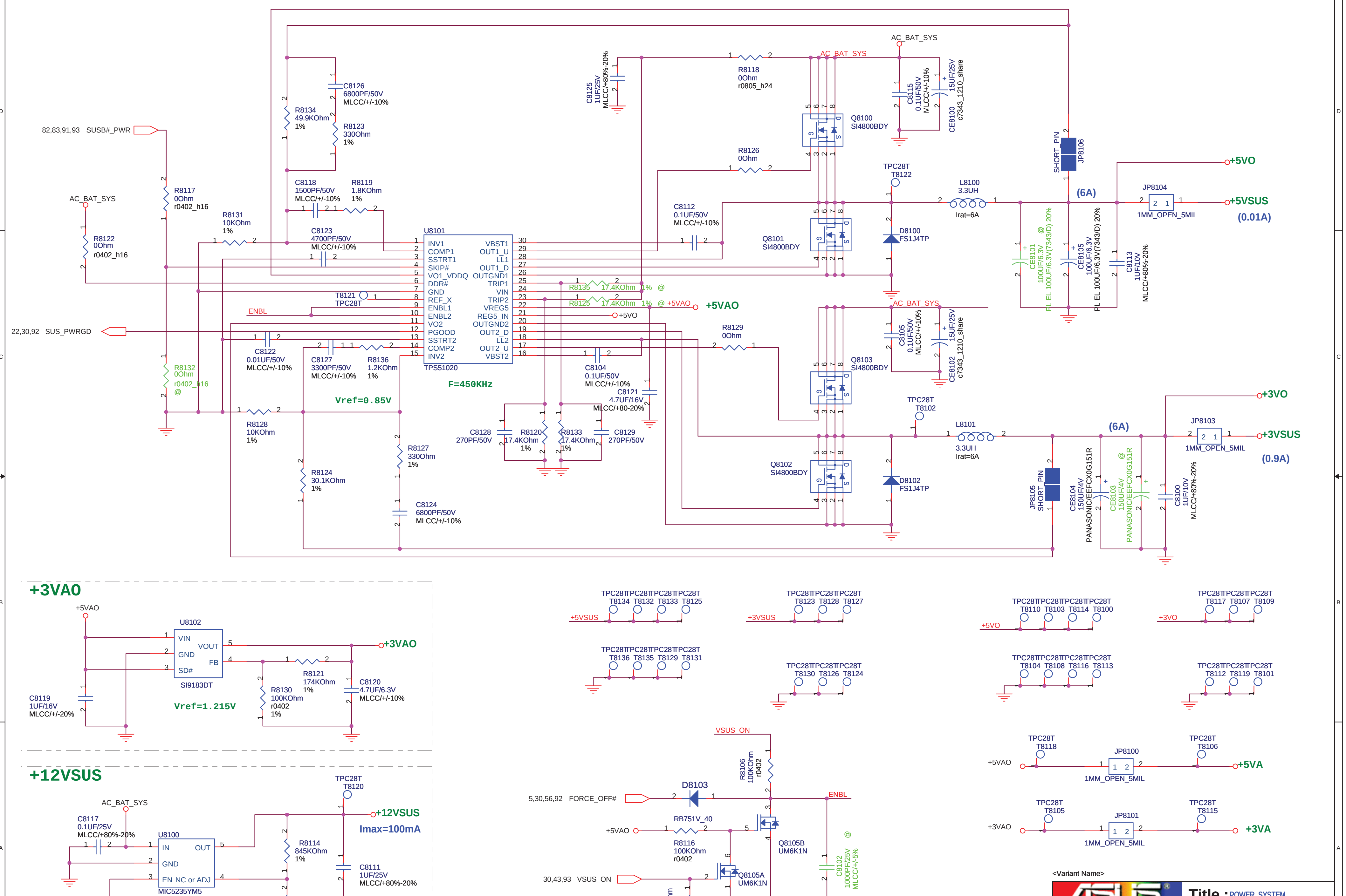


+5VO
+5VSUS
+5VAO
+3VO
+3VSUS
(6A)
(0.01A)
(0.9A)
U8101
TPS51020
F=450KHz
Vref=0.85V
82,83,91,93 SUSB#_PWR
22,30,92 SUS_PWRGD
AC_BAT_SYS
ENBL
Q8100 SI4800BDY
Q8101 SI4800BDY
Q8102 SI4800BDY
Q8103 SI4800BDY
L8100 3.3UH Irat=6A
L8101 3.3UH Irat=6A
D8100 FS1J4TP
D8102 FS1J4TP
JP8104 1MM_OPEN_5MIL
JP8103 1MM_OPEN_5MIL
JP8106 SHORT_PIN
JP8105 SHORT_PIN
+3VAO
U8102
SI9183DT
Vref=1.215V
+12VSUS
U8100
MIC5235YM5
FB=1.24V
Imax=100mA
TPC28T T8120
+5VA
+3VA
JP8100 1MM_OPEN_5MIL
JP8101 1MM_OPEN_5MIL
5,30,56,92 FORCE_OFF#
30,43,93 VSUS_ON
VSUS_ON
D8103 RB751V_40
Q8105A UM6K1N
Q8105B UM6K1N

<Variant Name>

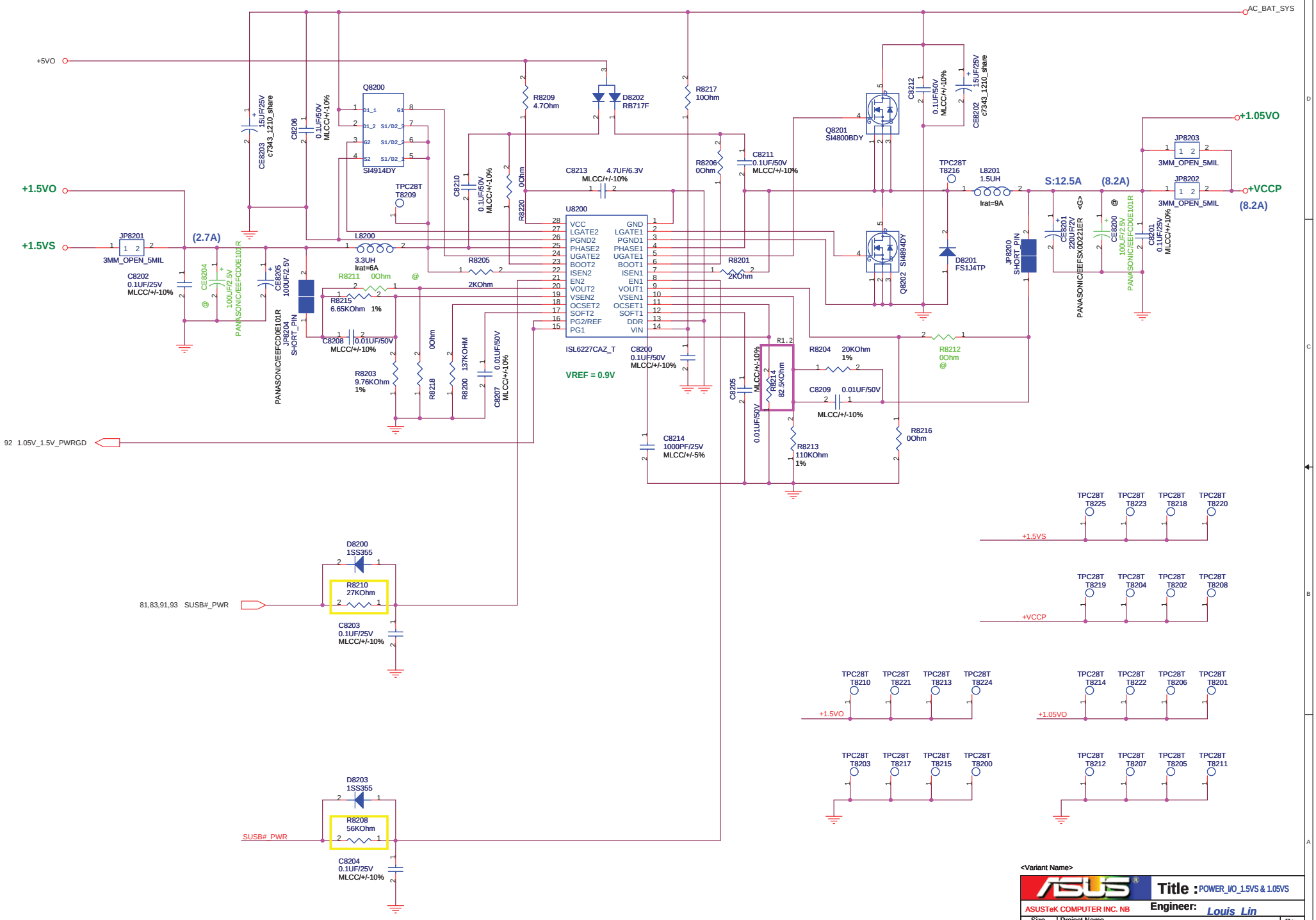
Title : POWER_SYSTEM

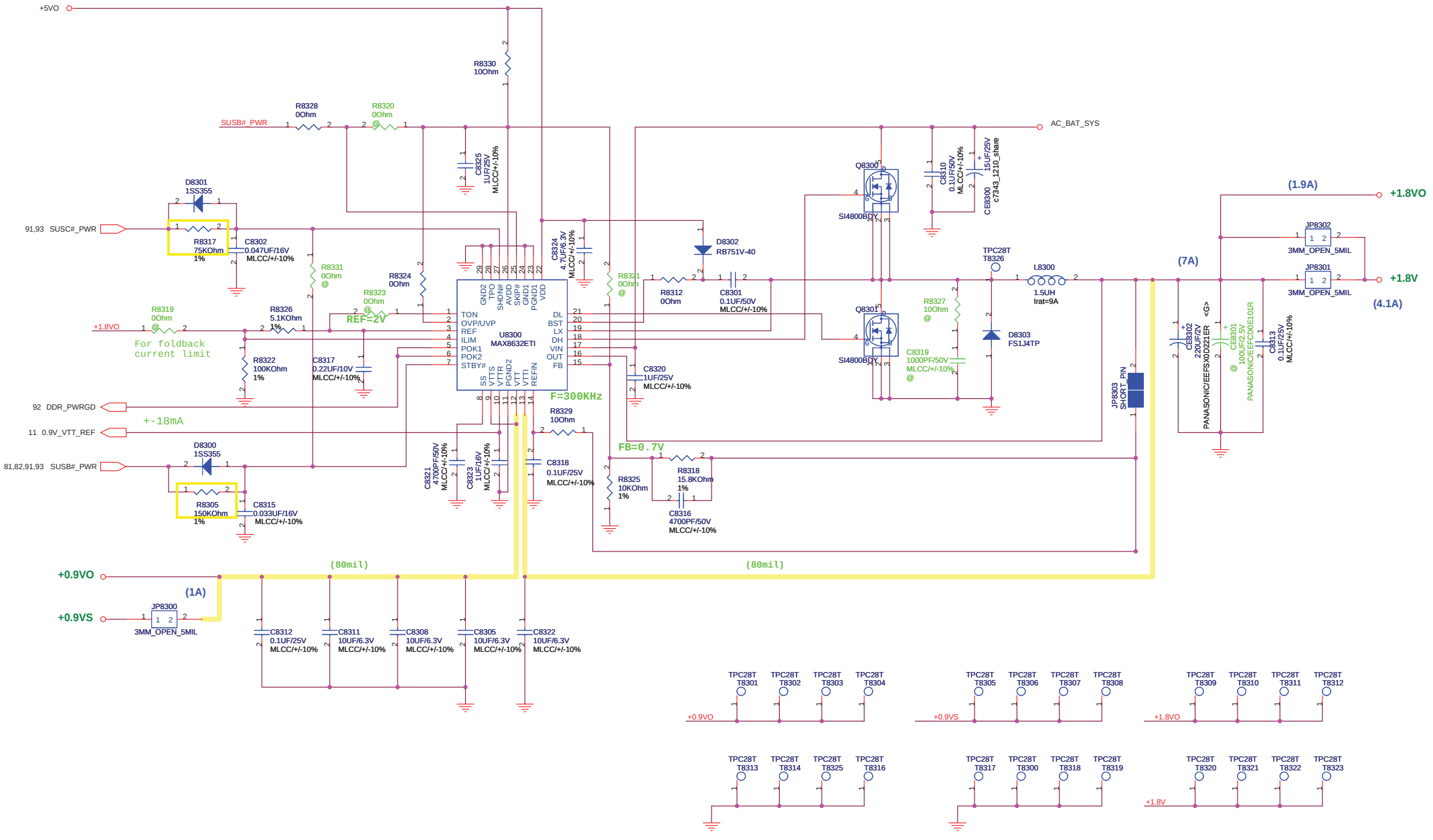
ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 81 of 101


AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
U8200
ISL6227CAZ_T
VREF = 0.9V
Q8200
SI4914DY
Q8201
SI4800BDY
Q8202
SI4894DY
L8200
3.3UH
Irat=6A
L8201
1.5UH
Irat=9A
S:12.5A
(8.2A)
(2.7A)
JP8201
JP8202
JP8203
3MM_OPEN_5MIL
JP8204
SHORT_PIN
JP8200
SHORT_PIN
D8200
1SS355
D8201
FS1J4TP
D8202
RB717F
D8203
1SS355
92 1.05V_1.5V_PWRGD
81,83,91,93 SUSB#_PWR
SUSB# PWR
TPC28T
T8209
T8216
T8225
T8223
T8218
T8220
T8219
T8204
T8202
T8208
T8210
T8221
T8213
T8224
T8214
T8222
T8206
T8201
T8203
T8217
T8215
T8200
T8212
T8207
T8205
T8211
<Variant Name>
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC. NB
Engineer: Louis_Lin
Size: Custom
Project Name: N20A
Rev: 1.2
Date: Monday, June 02, 2008
Sheet 82 of 101



<Variant Name>

Title : POWER_I/O_DDR & VTT

ASUSTeK COMPUTER INC. NB

Engineer: Louis Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 83 of 101

<Variant Name>

Title : POWER_I/O_ +1.25VS&+2.5VS

ASUSTeK COMPUTER INC. NB

Engineer: Louis Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 84 of 101

<Variant Name>

<Org Name>

Title : POWER_VGA_CORE & 1.1VSP

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 85 of 101

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
B		1.2

Date: Monday, June 02, 2008 Sheet 86 of 101

<Variant Name>

Title : POWER_SHUTDOWN#

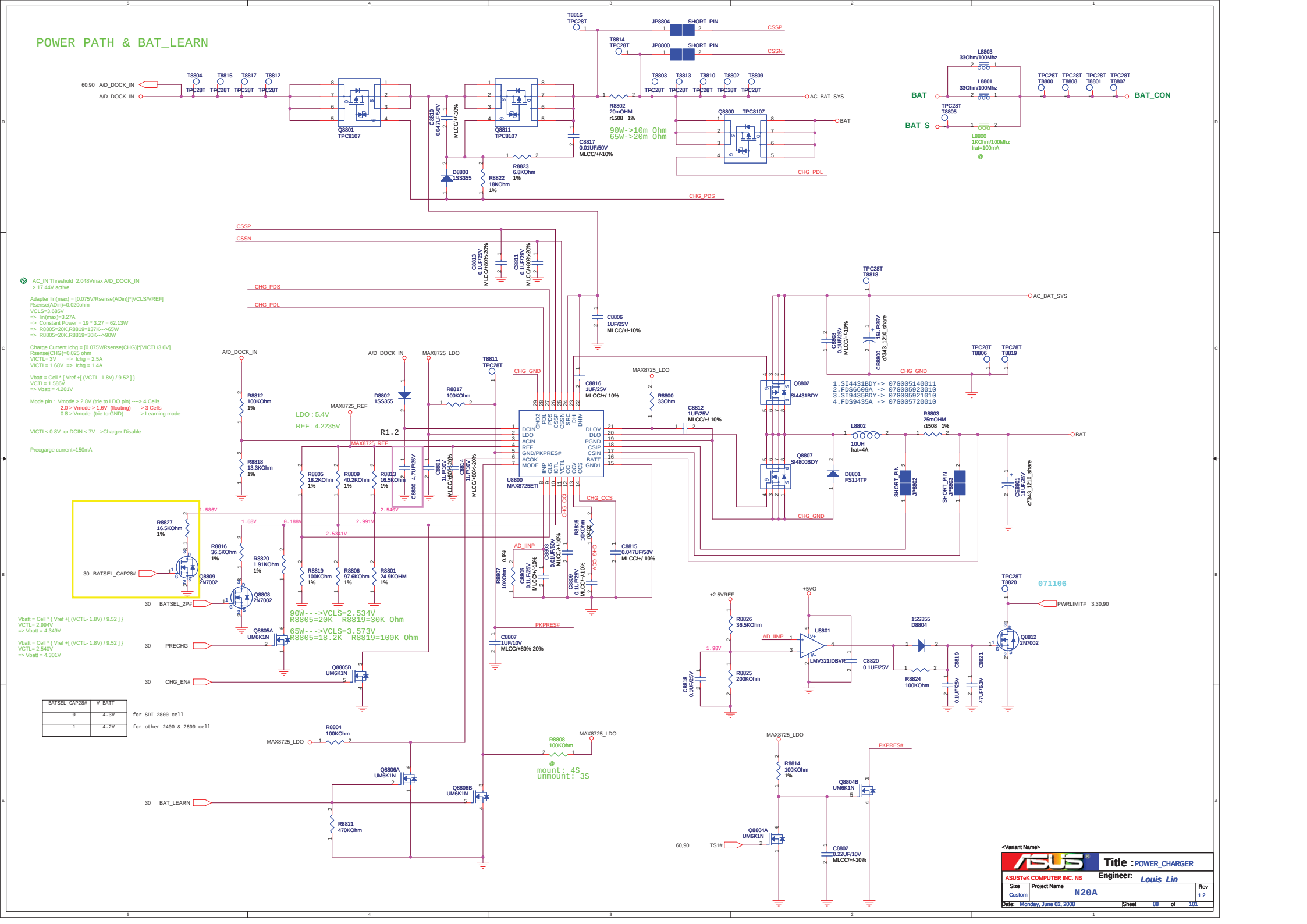
ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 87 of 101

POWER PATH & BAT_LEARN



<Variant Name>

Title : N/A

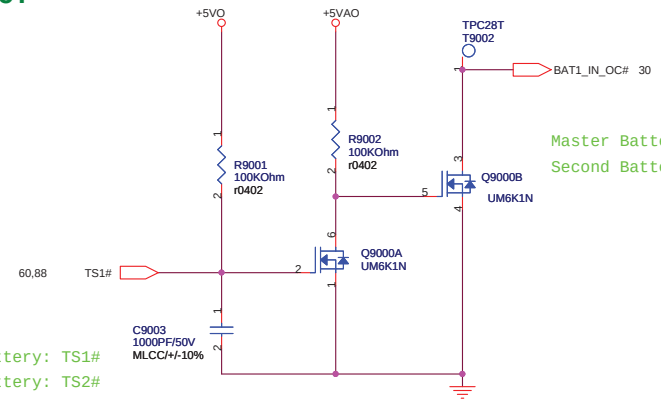
ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom		1.2

Date: Monday, June 02, 2008 Sheet 89 of 101

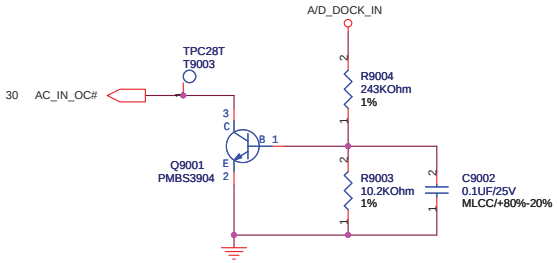
BATTERY IN DETECT



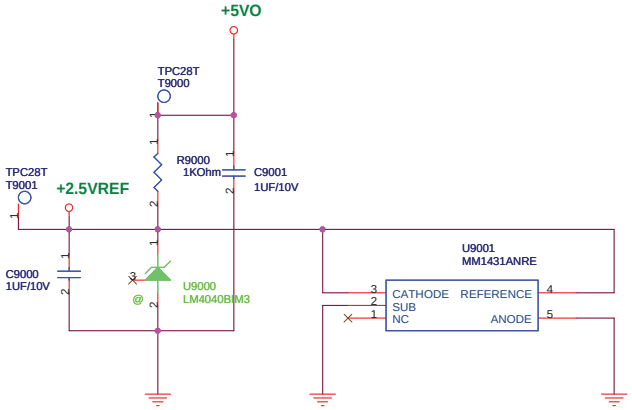
Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT

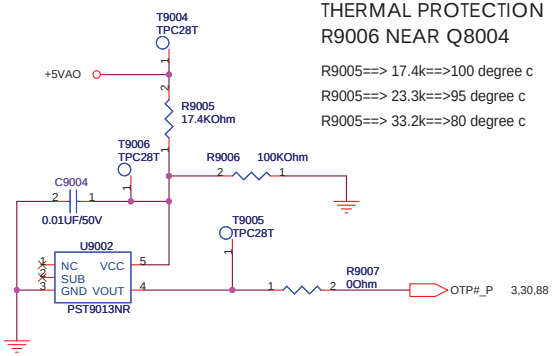


+2.5VREF



U9000 & U9001 colay

THERMAL PROTECT



95 DEGREE C

THERMAL PROTECTION
R9006 NEAR Q8004

R9005==> 17.4k==>100 degree c
R9005==> 23.3k==>95 degree c
R9005==> 33.2k==>80 degree c

<Variant Name>

ASUSTeK COMPUTER INC. NB

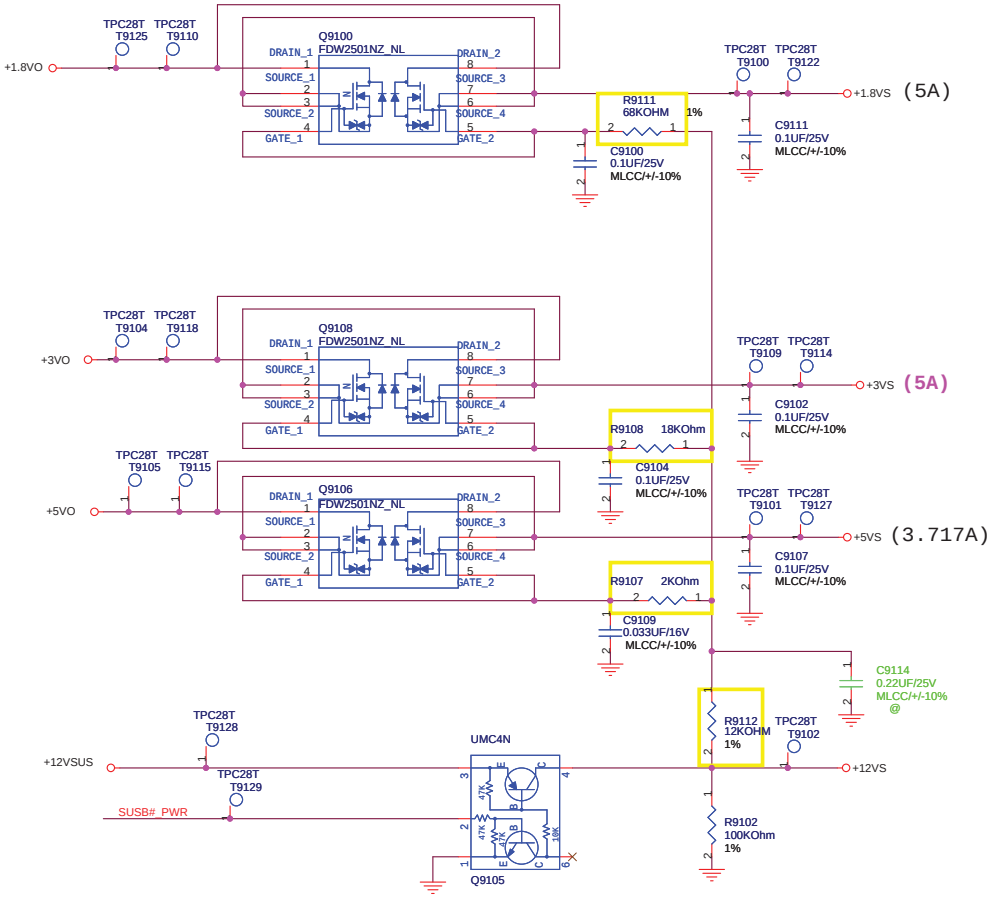
Title : POWER_DETECT

Engineer: Louis Lin

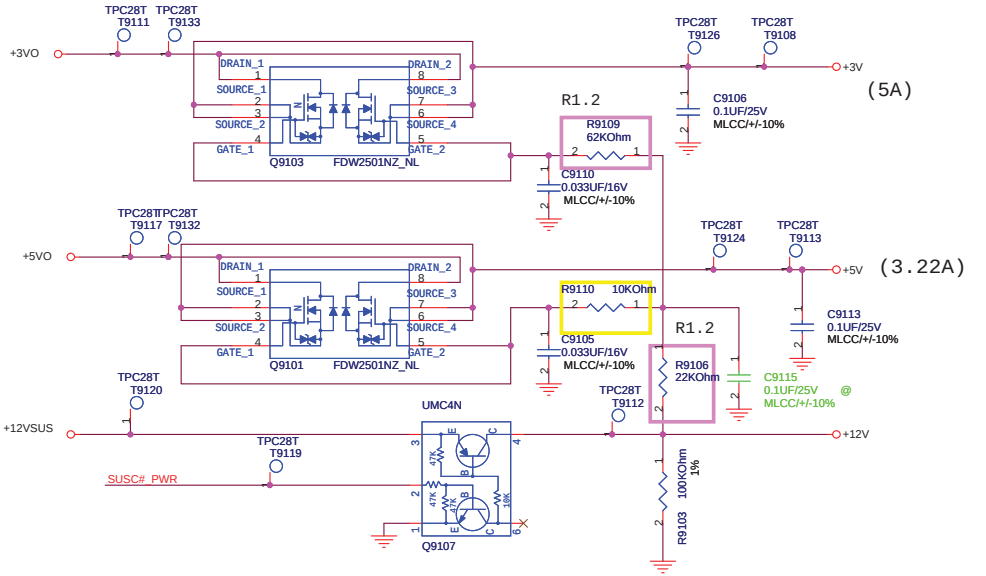
Size	Project Name	Rev
Custom	N20A	1.2

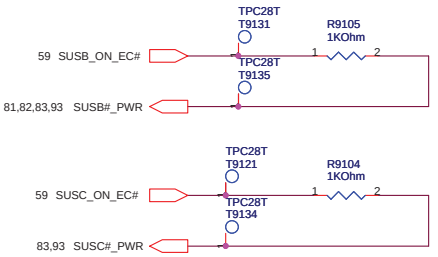
Date: Monday, June 02, 2008 Sheet 90 of 101

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

Title : POWER_LOAD SWITCH

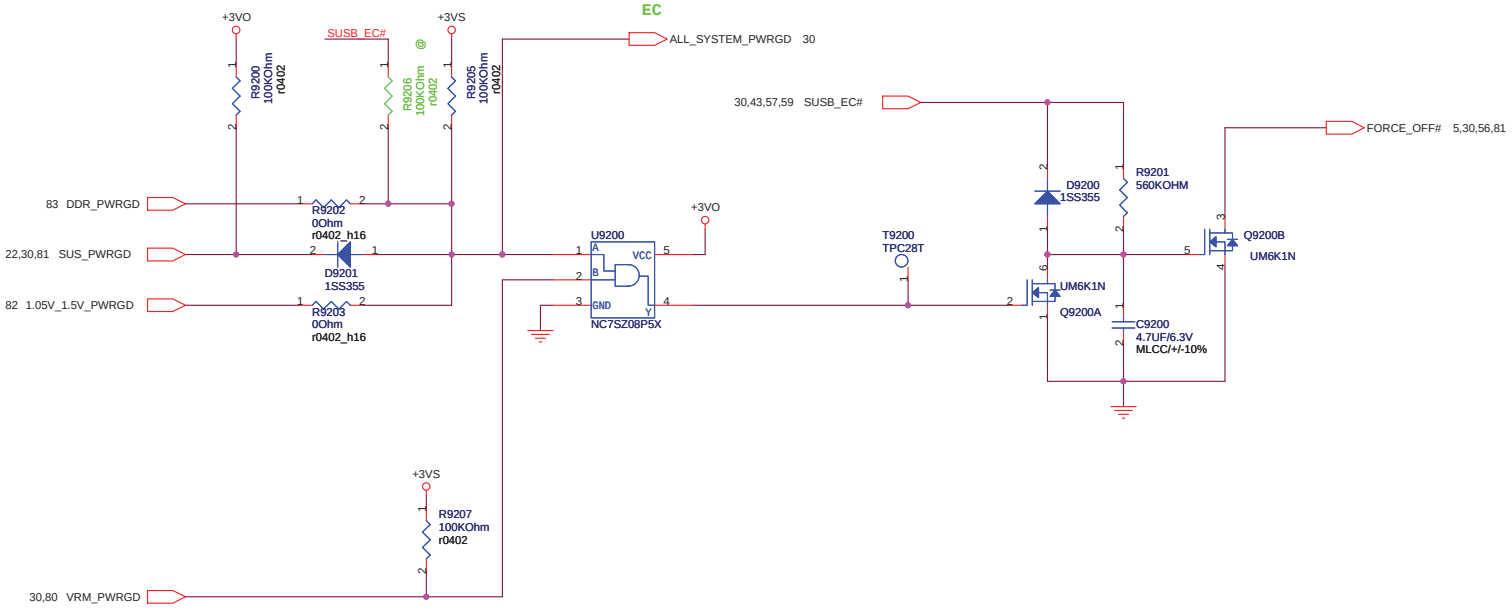
ASUSTeK COMPUTER INC. NB

Engineer: Louis Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 91 of 101

POWER GOOD DETECTER



<Variant Name>

Title : POWER_PROTECT

ASUSTeK COMPUTER INC. NB

Engineer: Louis Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 92 of 101

AC_BAT_SYS — AC_BAT_SYS 45,80,81,82,83,88

BAT — BAT 88

BAT_CON — BAT_CON 60,88

+2.5VREF — +2.5VREF 88,90

+3VA — +3VA 20,30,42,56,57,59,67,81

+5VAO — +5VAO 81,90

+5VO — +5VO 56,81,82,83,88,90,91

+5VSUS — +5VSUS 23,81

+5V — +5V 52,56,57,58,66,67,91

+5VS — +5VS 23,46,48,50,51,56,57,58,67,80,91

+3VO — +3VO 81,91,92

+3VSUS — +3VSUS 20,21,22,23,30,33,43,67,81

+3V — +3V 21,33,42,43,44,45,51,53,54,57,58,61,62,66,67,91

+3VS — +3VS 3,7,8,11,14,15,20,21,22,23,24,25,26,29,30,32,33,43,45,46,48,50,51,53,54,56,57,58,62,66,67,80,91,92

+12VSUS — +12VSUS 81,91

+12V — +12V 42,57,66,91

+12VS — +12VS 24,45,48,51,58,91

+1.8VO — +1.8VO 83,91

+1.8V — +1.8V 7,8,11,13,57,67,83

+1.8VS — +1.8VS 14,57,91

+0.9VS — +0.9VS 9,57,67,83

+0.9VO — +0.9VO 83

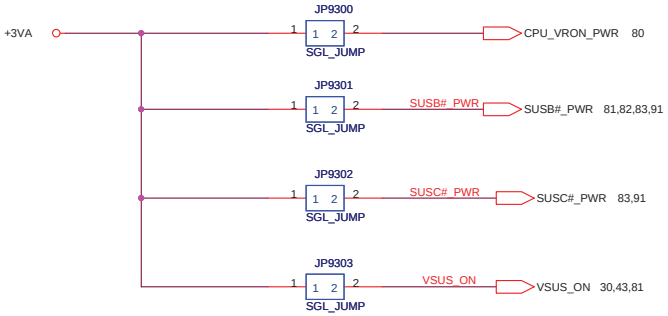
+1.05VO — +1.05VO 80,82

+VCCP — +VCCP 5,10,11,13,14,20,23,29,57,67,82

+1.5VO — +1.5VO 82

+1.5VS — +1.5VS 4,14,20,23,43,53,54,57,67,82

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Louis Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 93 of 101

<Variant Name>

Title : POWER_TFT-LED DRIVE

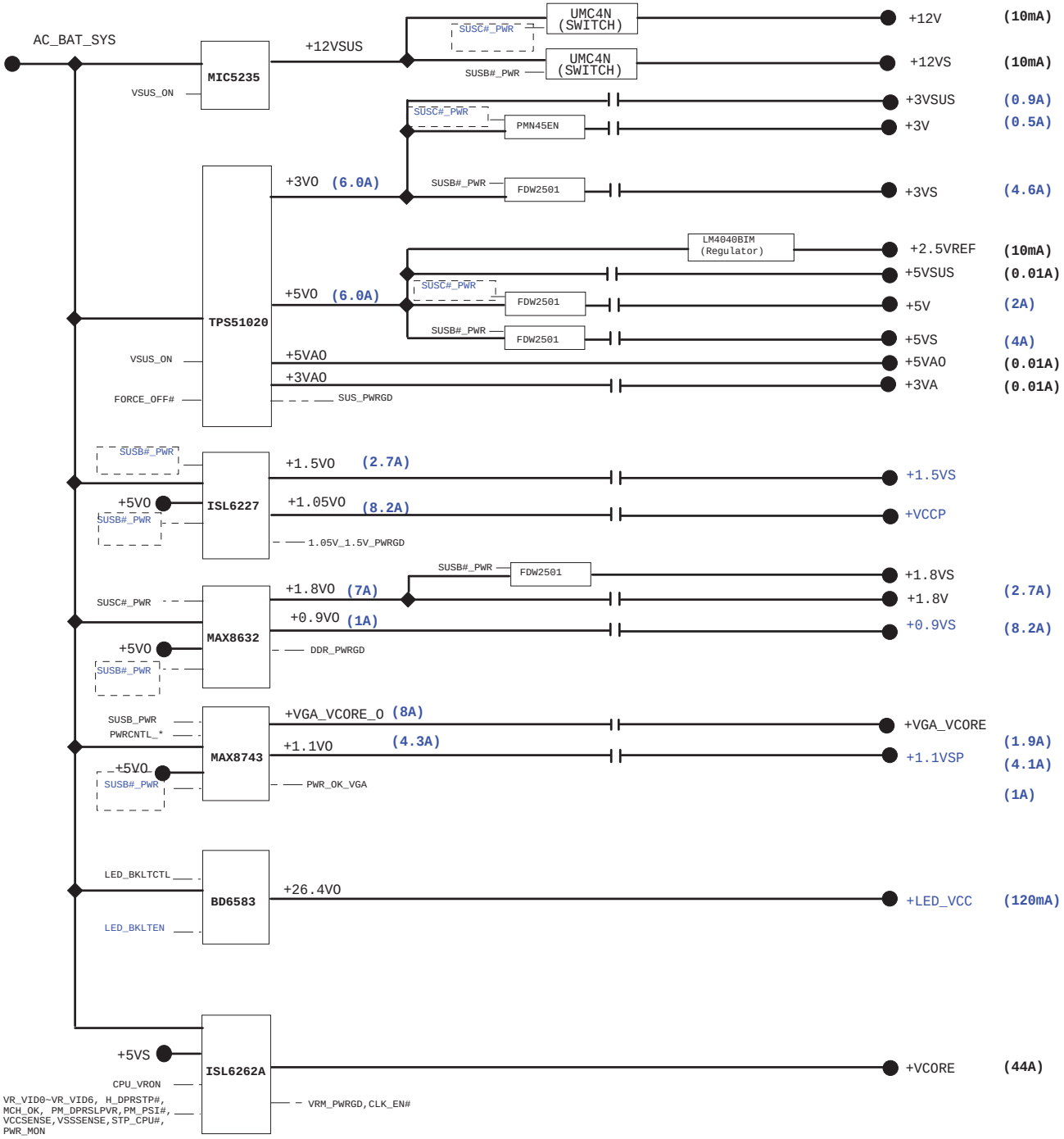
ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 94 of 101

Non-IAMT



<Variant Name>

ASUSTeK COMPUTER INC. NB

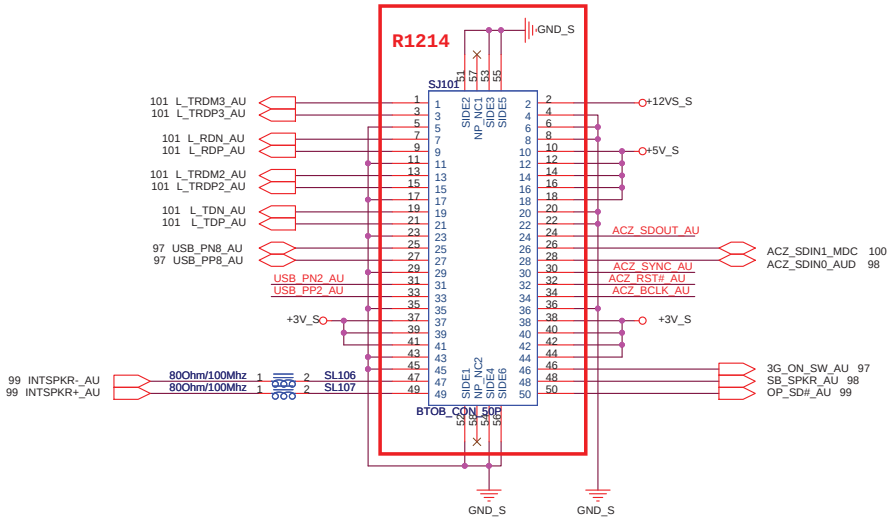
Title : POWER_FLOWCHART

Engineer: Louis_Lin

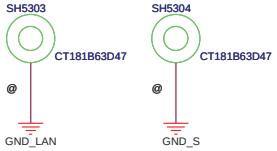
Size	Project Name	Rev
Custom	N20A	1.2

Date: Monday, June 02, 2008 Sheet 95 of 101

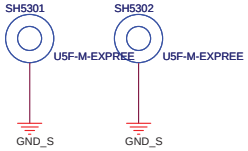
SUB CONN



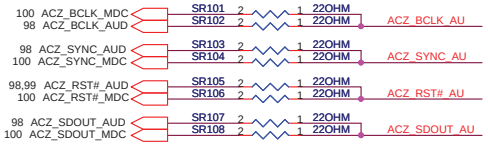
FOR MDC (TOP)

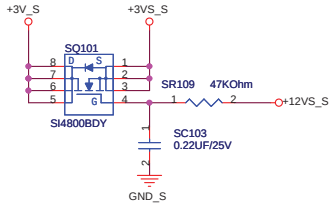


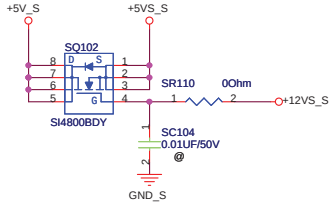
FOR 3G (TOP)

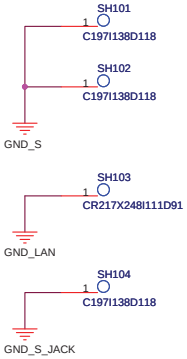


SCREW HOLE



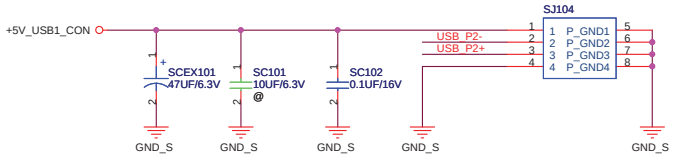


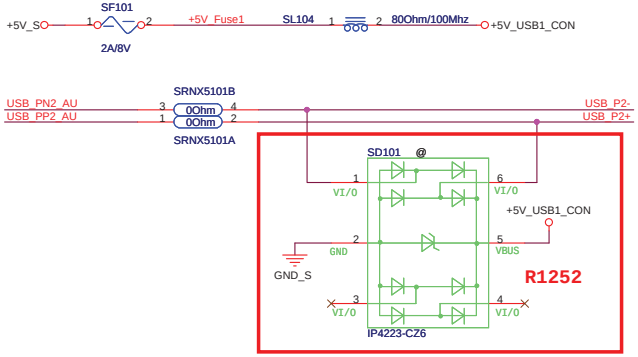




FIXED HOLES

SUB USB CONN





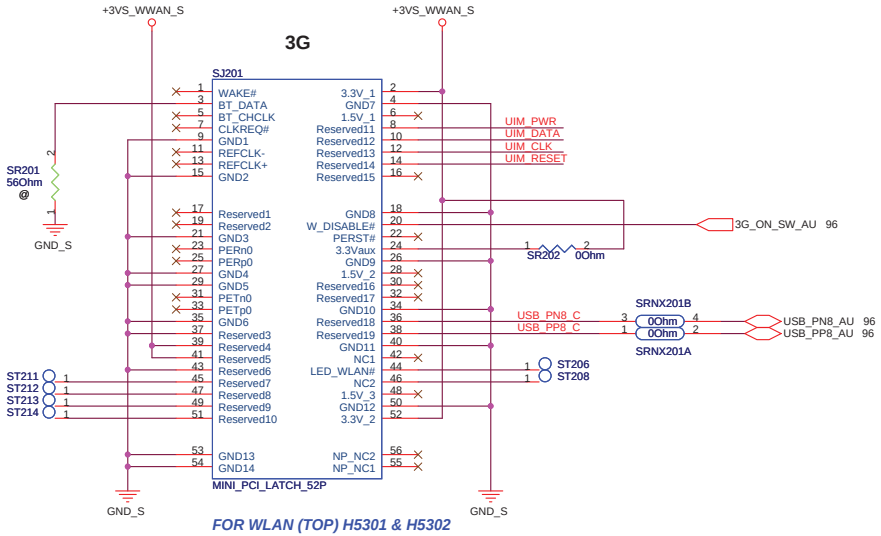
ASUSTeK COMPUTER INC. NB1

Title : SUB_CON &USB

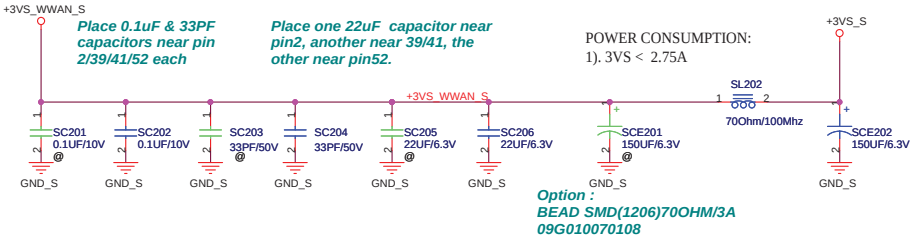
Engineer: Ryan_Wang

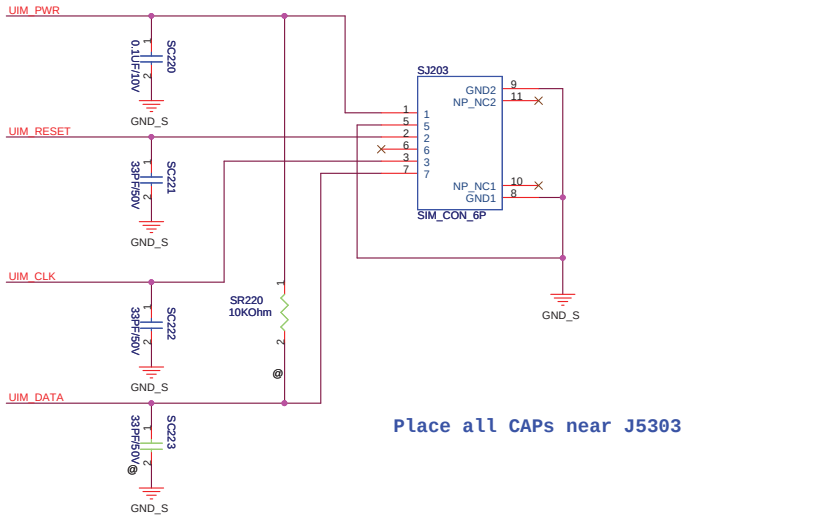
Size	Project Name	Rev
Custom	N20A	1.20

Date: Monday, June 09, 2008 Sheet 96 of 101



FOR WLAN (TOP) H5301 & H5302

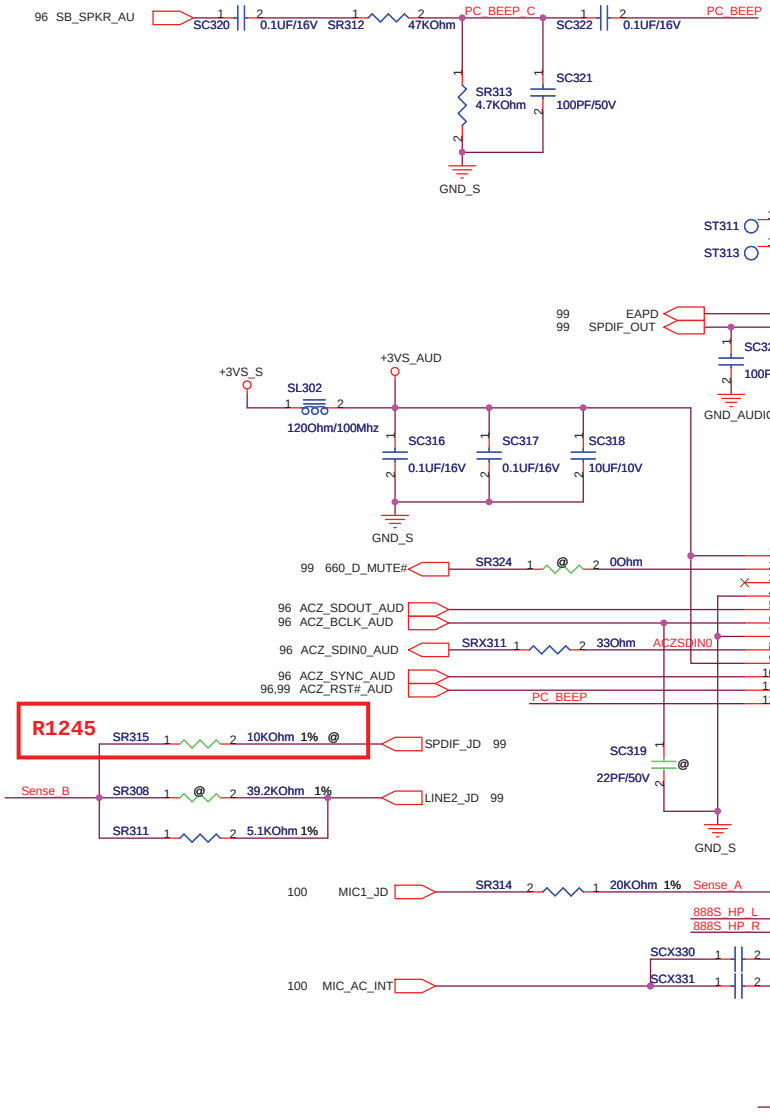




Place all CAPs near J5303

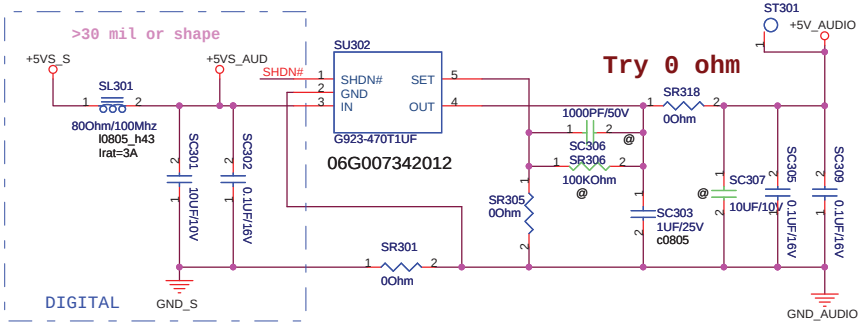
ASUSTeK COMPUTER INC. NB1	Title : WWAN & SIM	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 97 of 101	

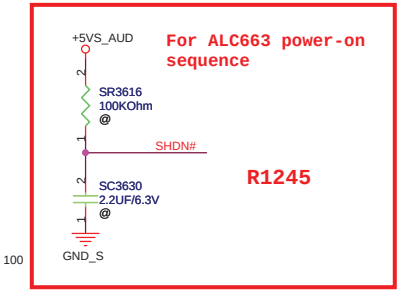
PC BEEP

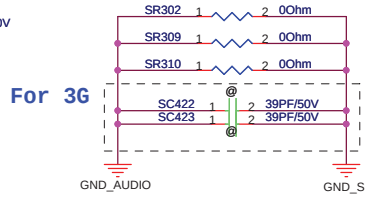


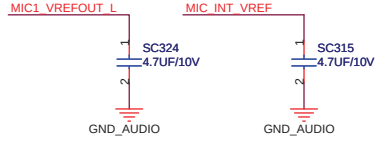
Audio Power

FOR ADJUST MODE:
Vo=1.25*(1+R3706/R3705)
= 1.25*(1+ 100K/34.8K) = 4.84





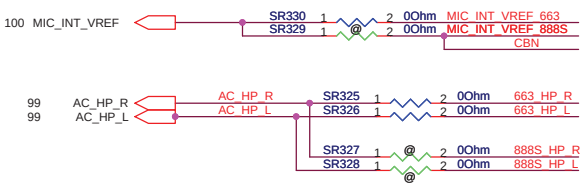


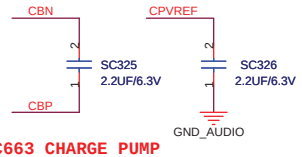


Colay ALC663 & 888S

ALC663
Mount SR325, SR326 for Headphone
SR311 for jack sense
SC325 & SC326 for CHARGE PUMP
SR330 for Internal MIC

ALC888S
Mount SR327, SR328 for Headphone
SR308 for jack sense
SR329 for Internal MIC





ALC663 CHARGE PUMP

ASUSTeK COMPUTER INC. NB1	Title : CODEC-ALC663	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 98 of 101	

MUTE CONTROL

HP & SPDIF CONN

2'nd source:
TI/TPA6205A1DGNRG4, P/N: 06G045099110

R1212

R1210

R1211

AMP POWER

FOR ALC663 CAP-LESS

FOR EMI BEAD

Colay ALC663 & 888S

ALC663
Mount SR429, SR430 for CAP less

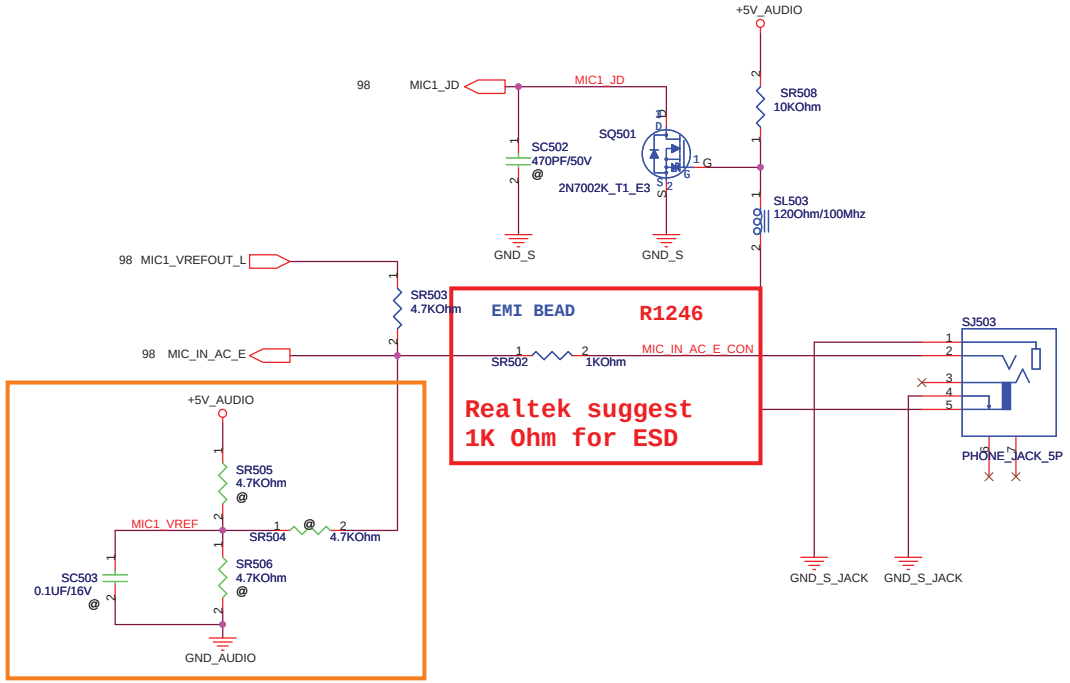
ALC888S
Mount SCEX401, SR420, SRX418
SCEX402, SR421, SRX419

Removed the SPDIF power control signal.When HP jack sense enable, the driver must turn off the SPDIF.

For 3G

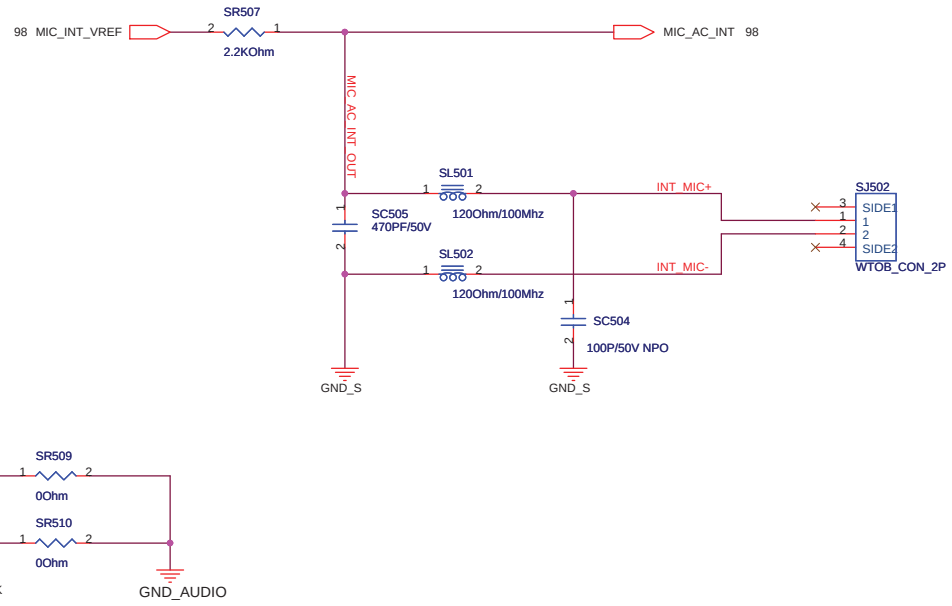
ASUSTeK COMPUTER INC. NB1	Title : AUDIO AMP & HP	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 99 of 101	

EXTERNAL MICROPHONE

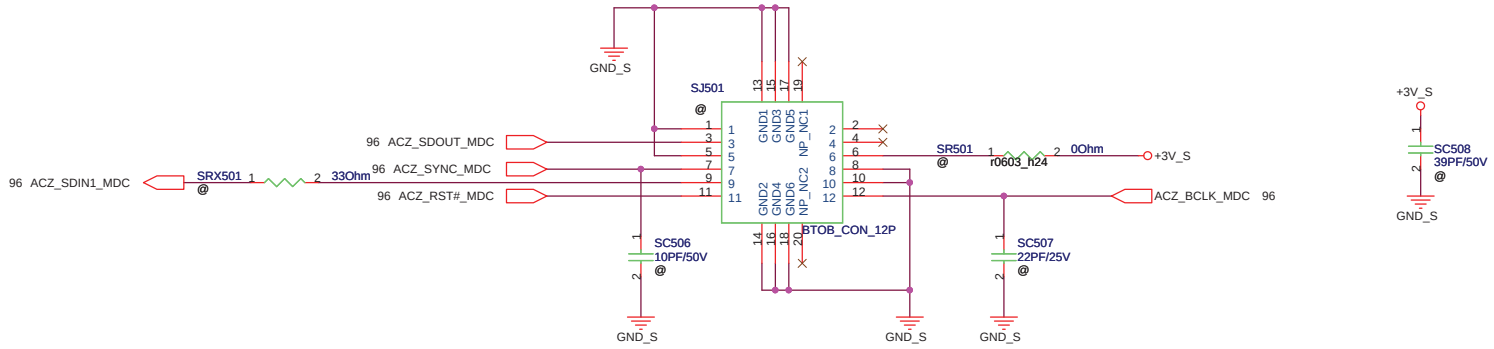


Reserved the external MIC bias(T filter).

INTERNAL MICROPHONE

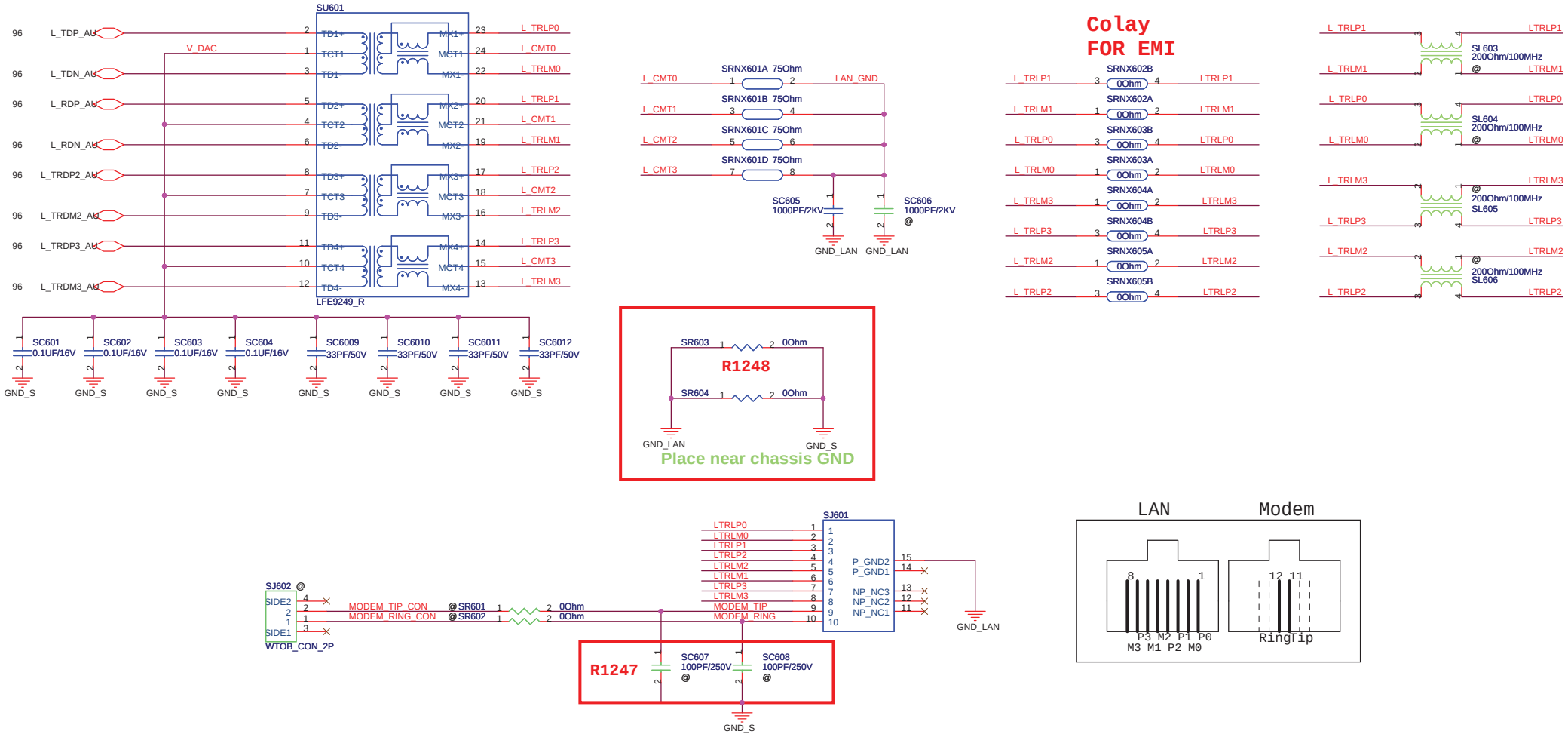


MODEM



FOR MDC (TOP) H3501 & H3502

ASUSTeK COMPUTER INC. NB1	Title : MIC & MDC	
	Engineer: Ryan_Wang	
Size: Custom	Project Name: N20A	Rev: 1.20
Date: Monday, June 09, 2008	Sheet 100 of 101	



ASUSTeK COMPUTER INC. NB1	Title : RJ11 +RJ45		
	Engineer: Ryan_Wang		
Size: Custom	Project Name: N20A		Rev: 1.20
Date: Monday, June 09, 2008	Sheet 101 of 101		