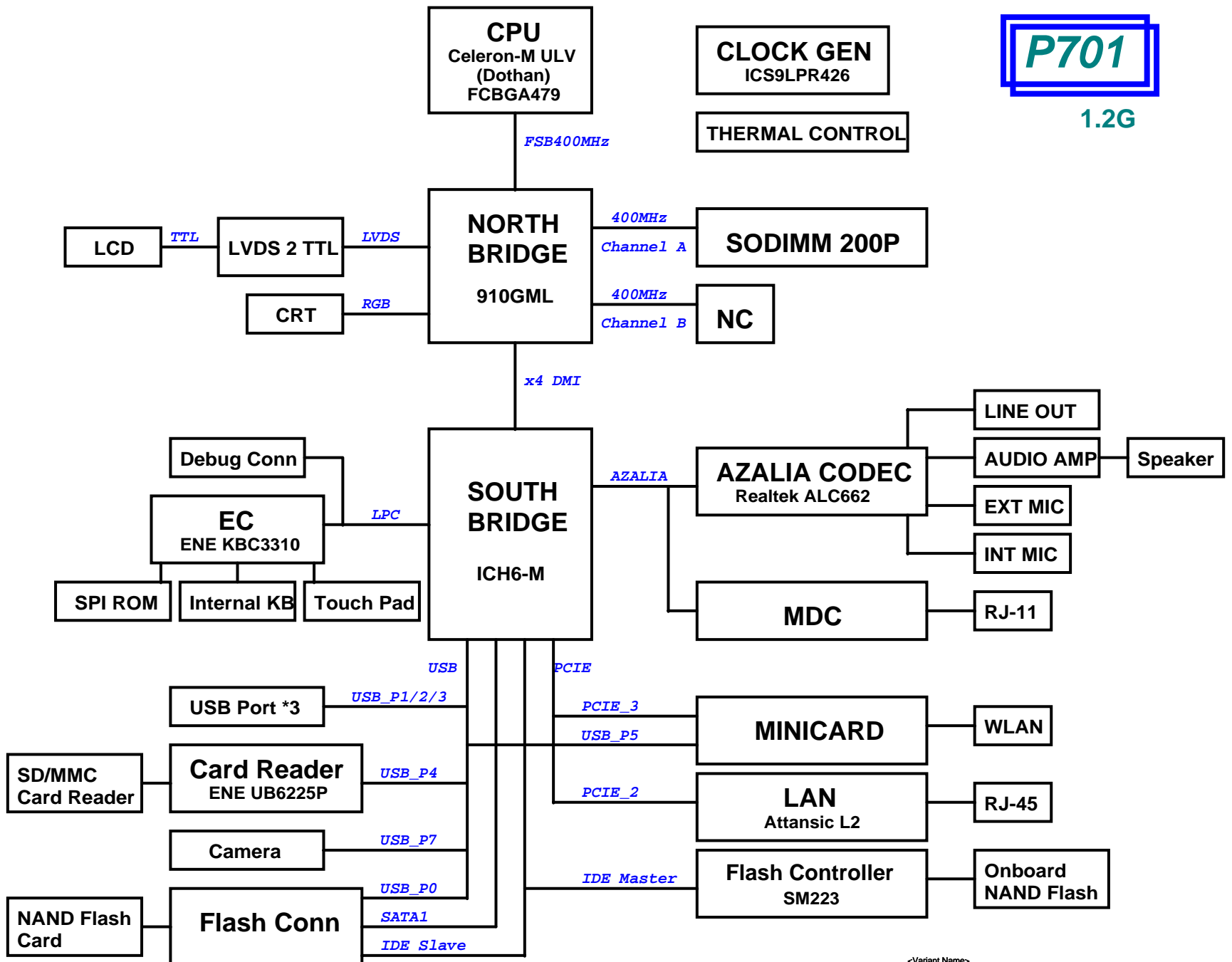


- 01_Block Diagram
- 02_System Setting
- 03_Power Sequence
- 04_EC Pin Define
- 05_History
- 06_*
- 07_Clock Gen_ICS9LPR426
- 08_Dothan_HOST
- 09_Dothan_PWR_GND
- 10_910GML_HOST_DMI
- 11_910GML_DRAM
- 12_910GML_VGA_LVDS_TV
- 13_910GML_PWR
- 14_910GML_GND
- 15_ICH6-M_Azalia_GPIO_PCI_LAN
- 16_ICH6-M_USB_PCIE_DMI_IDE_SATA
- 17_ICH6-M_PWR_GND
- 18_DDR2_SODIMM
- 19_DDR2_Termination
- 20_Onboard VGA
- 21_LCD Conn
- 22_Minicard
- 23_LAN_Atheros L2
- 24_MDC_RJ11_RJ45
- 25_Onboard Flash
- 26_Flash Conn
- 27_USB Port
- 28_Card Reader_ENE UB6225P
- 29_Camera Conn
- 30_Codec_ALC662
- 31_Audio_AMP_Jack
- 32_EC_ENE KB3310
- 33_Switch_SPI ROM_Debug Conn
- 34_KB_Touch Pad
- 35_Thermal Sensor_FAN
- 36_LED_THERMTRIP
- 37_Discharge
- 38_PWR Jack
- 39_Srew Hole
- 40_EMI
- 41_POWER FLOW
- 42_CHARGER
- 43_VCORE(7A)
- 44_POWER_3V_5V_VTT_DDR
- 45_POWER_3VA_3VSB
- 46_POWER_1.05V_1.5V_2.5V
- 47_POWER_1.8V_DUAL_5VSB



P701


1.2G

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPIO/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SC#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	10K Pull +3V	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSM#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PC#	Clock GEN STP_PC#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	NC	GPO	fixed as Output only
NA	GPIO22	NA	NA	NA
AD21	GPO23	NC	GPO	fixed as Output only
V3	GPIO24	WLAN	I/O	Output
P5	GPIO25	NC	I/O	Output

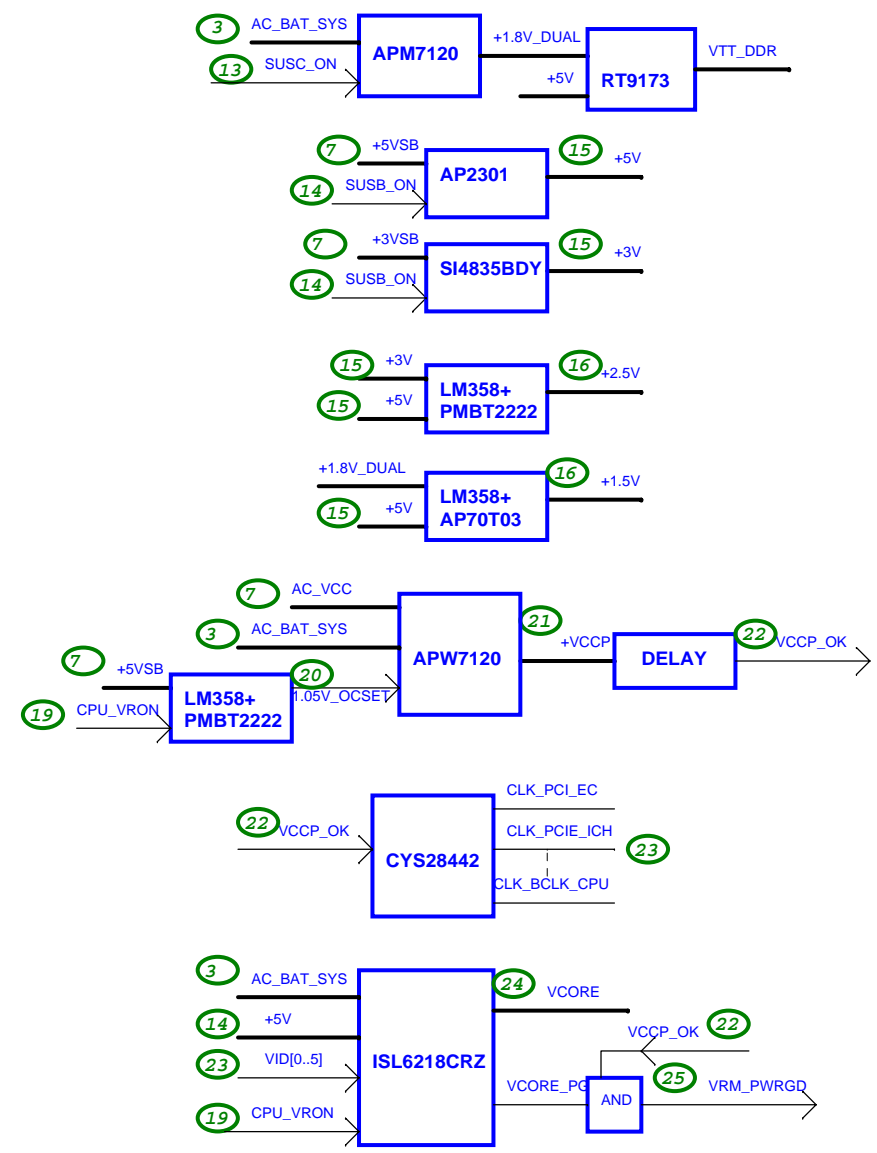
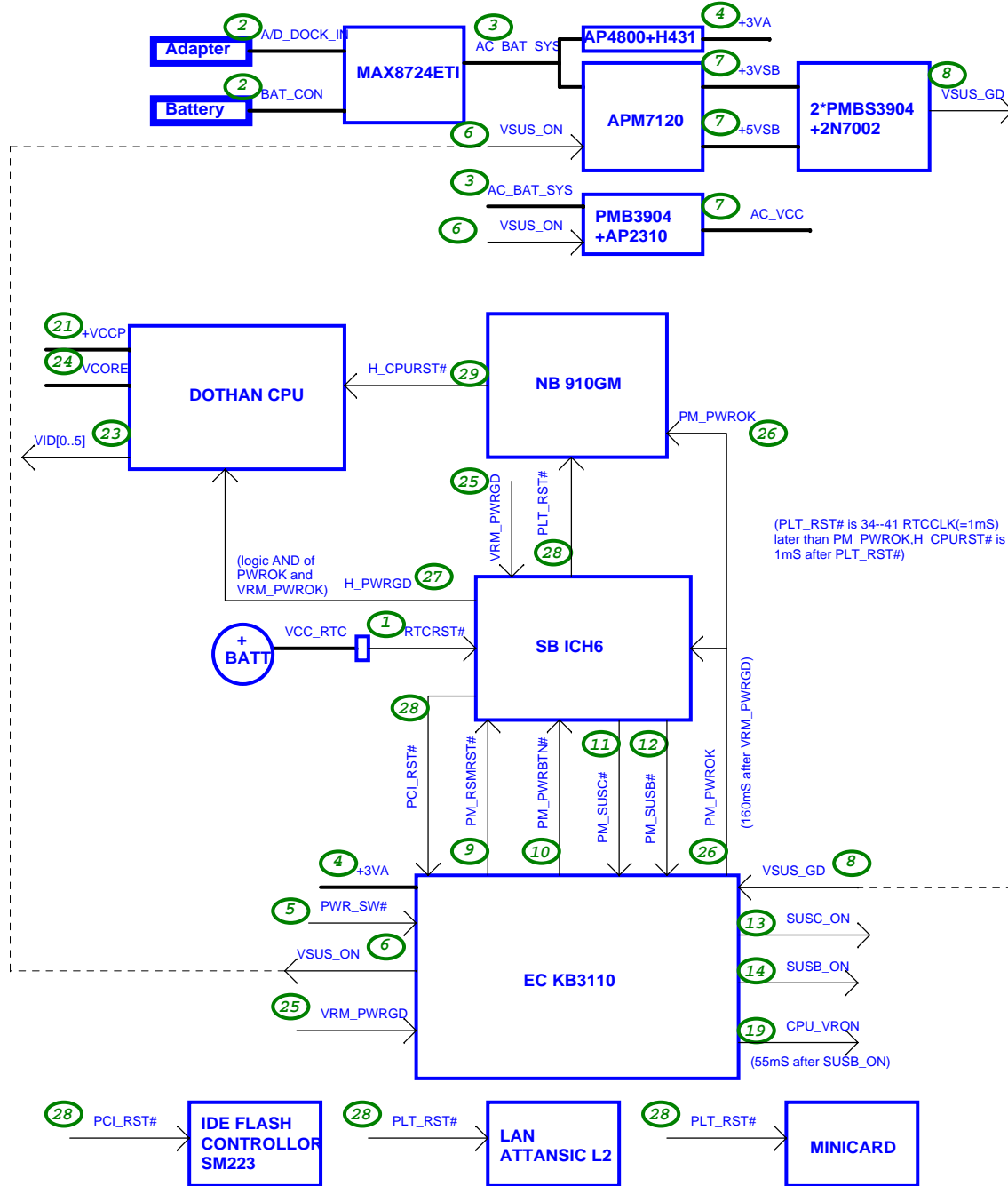
Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	NC	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	NC	I/O	Output
AC18	GPIO34	NC	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 /GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

<Variant Name>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size A3	Project Name P701	Rev 1.2G	
Date: Friday, August 24, 2007		Sheet 2 of 47	

*This sequence is for Battery Plug-in and no Adapter,
 if Adapter Plug-in, the sequence change to:
 A/D_DOCK_IN-->AC_BAT_SYS-->+3VA-->VSUS_ON-->+3VSB & +5VSB
 -->VSUS_GD-->PM_REMRST#-->PWR_SW#-->PM_PWRBTN-->PM_SUSC#-->PM_SUSB#

	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL



EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	EMAIL_SW#	I	EMAIL_SW#, *
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	N.C	O	Reserved
15	GPIO08	EXTSM#	O	EXTSM#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	LCD_CSB	O	LCD chip select
18	GPIO0C	LCD_SDA	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SC#	KBC_SC#	O	KBC_SC#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	LCD_SCL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	N.C	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	NUM_LED#	O	EC H/W controls(Unused)
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	P_PMON_10	I	Sense Power Loading
64	AD1	BAT_IN	I	sense Battery
65	AD2	N.C	I	Reserved
66	AD3	N.C	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSERVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB0_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB0_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB1_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB1_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	N.C	O	Reserved
84	PSDAT1	N.C	O	Reserved
85	PSCLK2	N.C	O	Reserved
86	PSDAT2	N.C	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CAP_LED#	O	EC H/W controls
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	*HW Strap for SPI Flash de External Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH8_PWROK	O	
103	GPXOA06	N.C	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPL_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P-3P
110	GPXID1	N.C	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is Pull Down 100K ohm to GND
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	N.C	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCL_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

<Variant Name>

		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size	Project Name		Rev
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CIRCUIT UPDATED HISTORY


Rev	Date	Description
1.0G	2007/02/26 }	S701L Schematic 1.0G Beginning
	2007/03/16	S701L 1.0G Gerber Out
1.1G	2007/03/24 }	S701L Schematic 1.1G Beginning
	2007/04/19	S701L 1.1G Gerber Out
1.0G	2007/04/24 }	P701(S701L renamed) Schematic 1.0G Beginning 1. PC8054, PR6075 /X to N/A 2. Attansic L2 change to Atheros L2(pin to pin) 3. LC1, LC33 /CAP/X to N/A 4. C87 change to X5R to cost down 5. L1, L2, L3 change to 56 NH, R5, R6 change to 75 Ohm to pass CRT EA measure 6. PR48 change to 22K Ohm, PC35 change to 4700PF to fix no VCORE issue 7. PR6074 change to 4.7K Ohm to fix +3VSB OCP issue 8. Clock Gen CY28442-2 change to ICS9LPR367 9. Phase in Power Level Reduce solution, mark "Taipei0508" 10. Card Reader Socket change to SD Socket 12G25100091E 11. Add System FAN circuit 12. Camera change to USB port 7, Minicard change to USB port 5 13. Use SB GPIO27 to Enable/Disable Card Reader UB6225P 14. Use SB GPIO28 to Enable/Disable Modem 15. Card Reader UB6225P share 48M clock from CLock Gen with SB USB part 16. Add D29 to fix LCD_CSB leakage current issue 17. LC29, LC30 change to 27PF to pass EA crystal measure 18. Change vaule of PR73, PR74, PC56 and add PC60 to adjust the power sequence timing between Stand By power and RSMRST# 19. Remove USB port 1 20. Add +5V generate +3V_LCD circuit 21. Remove +5V_CHG generate circuit 22. Use SB GPIO33, GPIO34 to controll the level of VCORE 23. U31 use APL5315BI-TRL to replace MAX8863TEUK(pin to pin, but reference voltage level different) 24. PR59 change to 130K Ohm for both 12V Adapter and 9.8V Adapter P701 1.0G Gerber Out
	2007/05/22	
1.1G	2007/05/31 }	P701 Schematic 1.1G Beginning 1. Remove the 48M clock from CLock Gen to Card Reader UB6225P 2. Clock Gen ICS9LPR367 change to ICS9LPR426 3. Flash Connector increase SATA and USB interface 4. Add Onboard Flash(SM223 + NAND Flash x4) 5. BATT_CON pin 5 connect to GND 6. Q34 pin 1 connect to +3V to fix EC reset issue 7. Remove J1, J2 8. KB pin 28 connect to GND for P701-ISP_CARD 9. Use SB GPO23 to Enable/Disable Audio Amplifier 10. Use SB GPO21 to controll Camera Power 11. Use SB GPIO24 to controll Minicard Power 12. Use SB GPIO25 to Enable/Disable WLAN Ratio 13. Atheros L2 and Minicard SMBUS interface directly pull high 14. LCD_CON pin 20 connect to AC_BAT_SYS P701 1.1G Gerber Out
	2007/06/07	

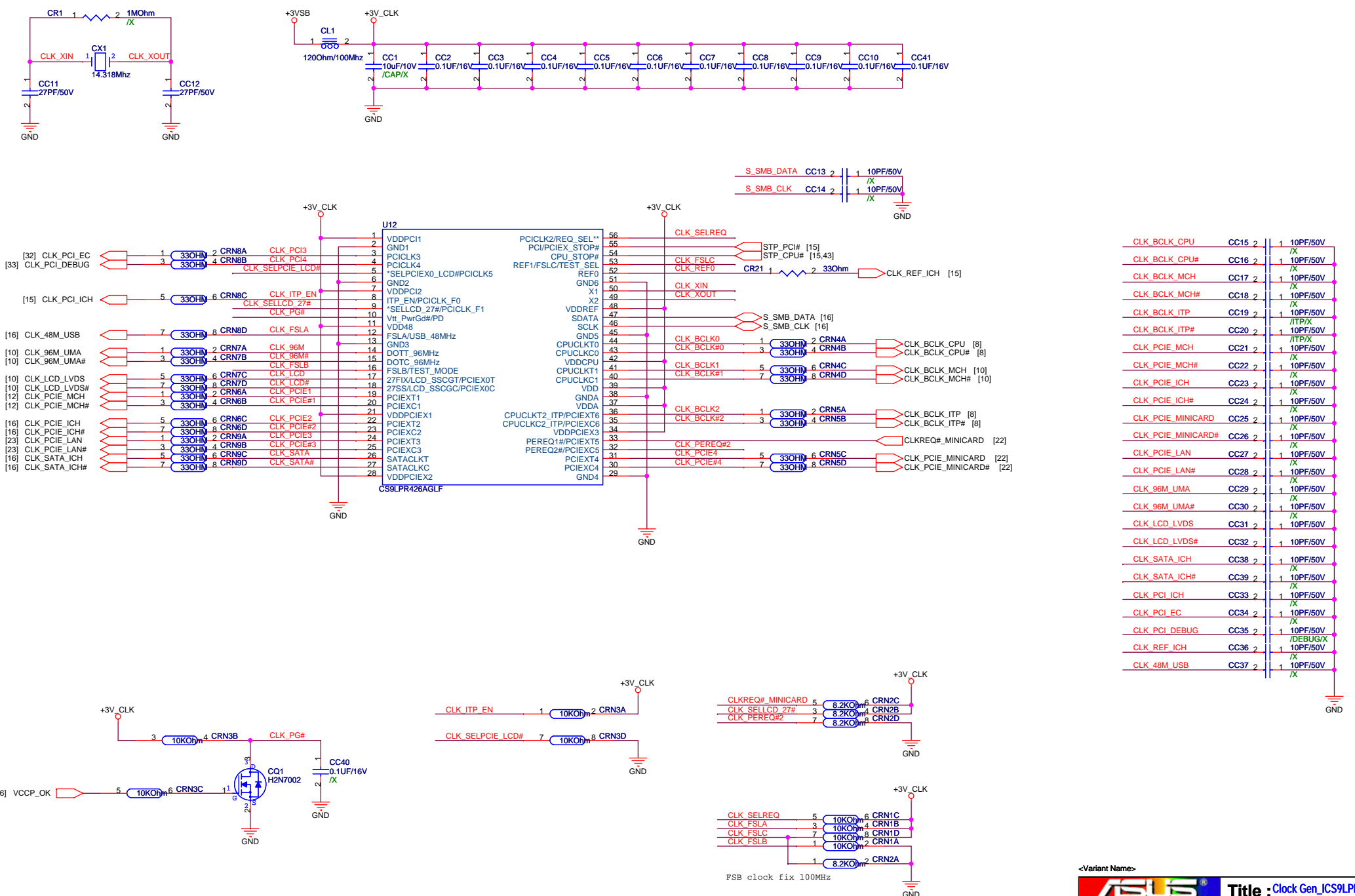
Rev	Date	Description
1.2G	2007/06/30 }	P701 Schematic 1.2G Beginning 1. Add R174 to short DASP pins of Master IDE device and SLave IDE device 2. Use SB GPIO27 to controll Card Reader UB6225P Power 3. PR606084.2 connect to +5V to fix LCD flash issue 4. Adjust SPEAKER pin define 5. Adjust CHARGE LED and WLAN LED lightness 6. Use SB GPI 26, 29, 30, 31 for PCB version 7. Change USB ESD diode for EMI request 8. Add Floating GND TP_GND and Spring TP1 & TP2 for EMI request 9. Change PM_VCOREL1, PM_VCOREL2 default level 10. Add PQ48 to controll +3V_PE to fix WLAN AW-GE780 can't detect issue 11. Power Charger part update circuit for new Adapter 12. Use SB GPI12 to detect LID signal level 13. Add H/W THERMTRIP circuit (page 36) 14. Add U40 to prevent system auto power on after clear CMOS 15. Use SB GPI7 for THRO_CPU 16. Power Charger part update circuit to prevent incorrect Adapter damage boards 17. Q1.1, Q2.1 change to +3V P701 1.2G Gerber Out
	2007/07/06	
1.2G	2007/07/26 }	P701 Schematic 1.3G Beginning 1. Add R11 for 801

<Variant Name>

		Title : History	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size A3	Project Name P701	Rev 1.2G	
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<Variant Name>

		Title : Blank	
ASUSTek Computer INC.		Engineer: <i>Keil_Huang</i>	
Size A3	Project Name P701		Rev 1.2G
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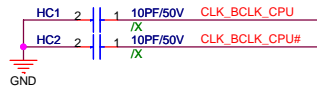


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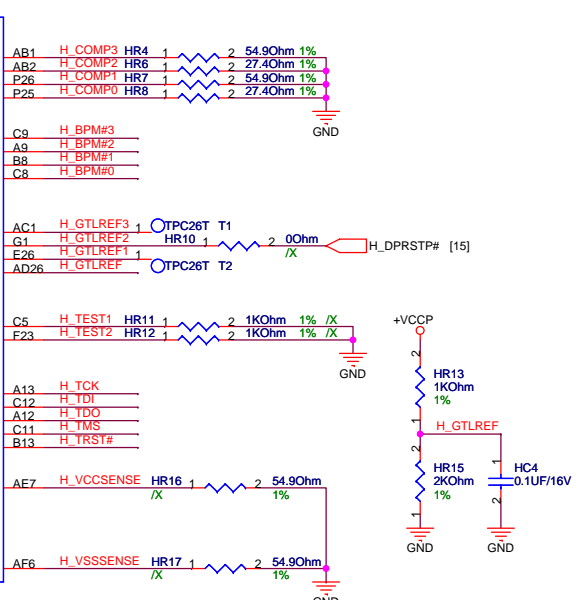
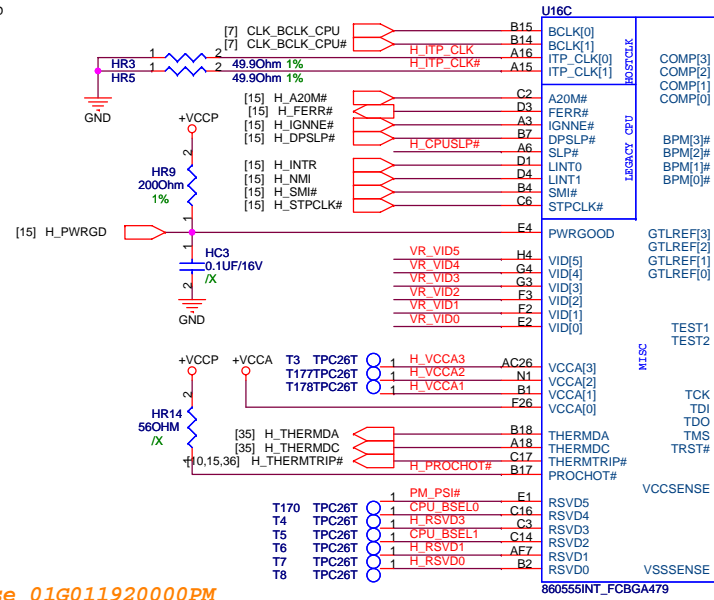
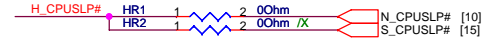
ASUS		Title : Clock Gen_ICS9LPR426	
ASUSTek Computer INC.		Engineer: Keii_Huang	
Size	Project Name		Rev
A3	P701		1.2G
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F5B clock fix 100MHz

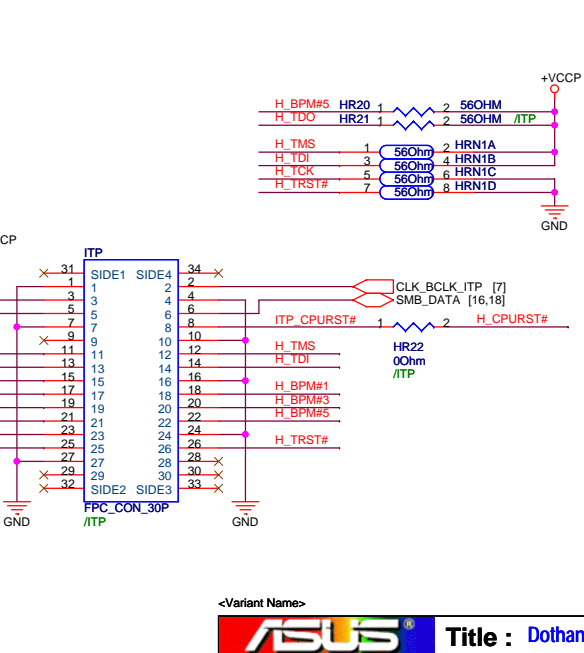
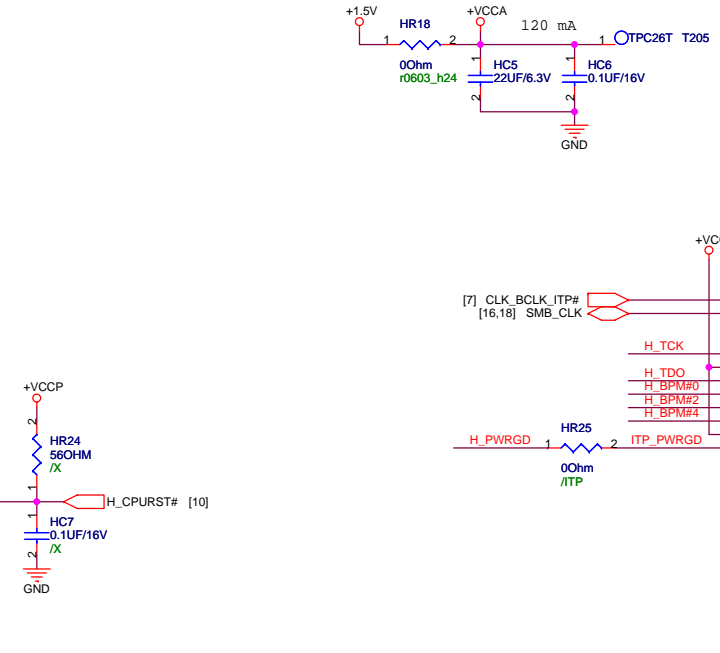
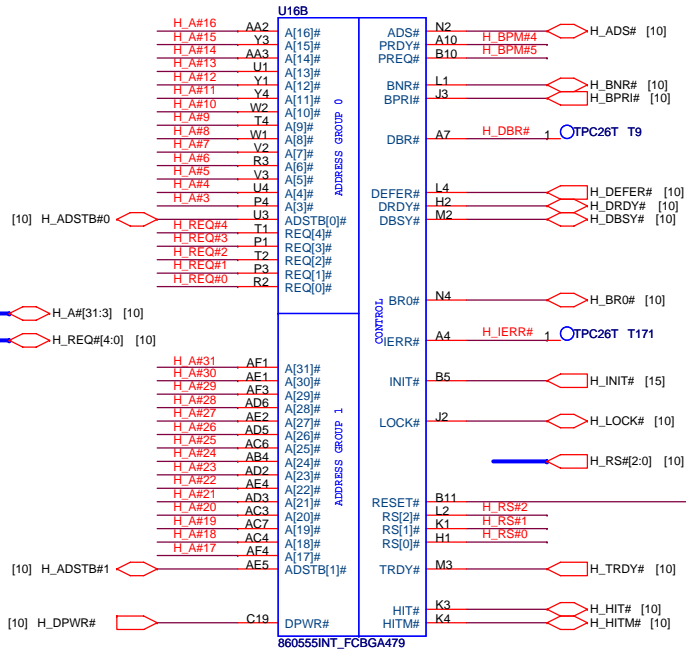
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- H_DIN##[3:0] [10]
- H_DSTBN##[3:0] [10]
- H_DSTBP##[3:0] [10]



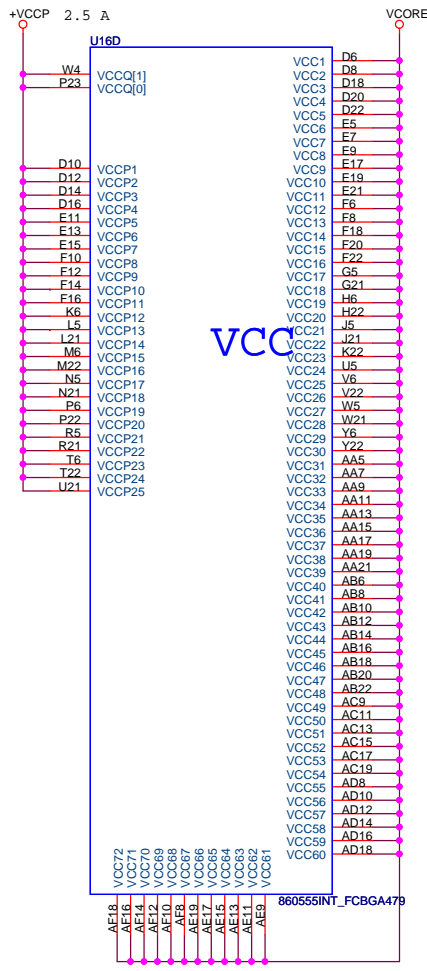
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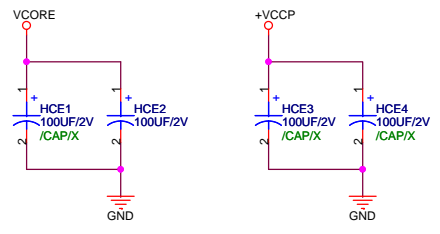
U16 use 01G011920000PM



ASUS Title : Dothan_HOST
 ASUSTek Computer INC. Engineer: Keil_Huang
 Size Project Name Rev
 A3 P701 1.2G
 Date: Saturday, September 01, 2007 Sheet 8 of 47

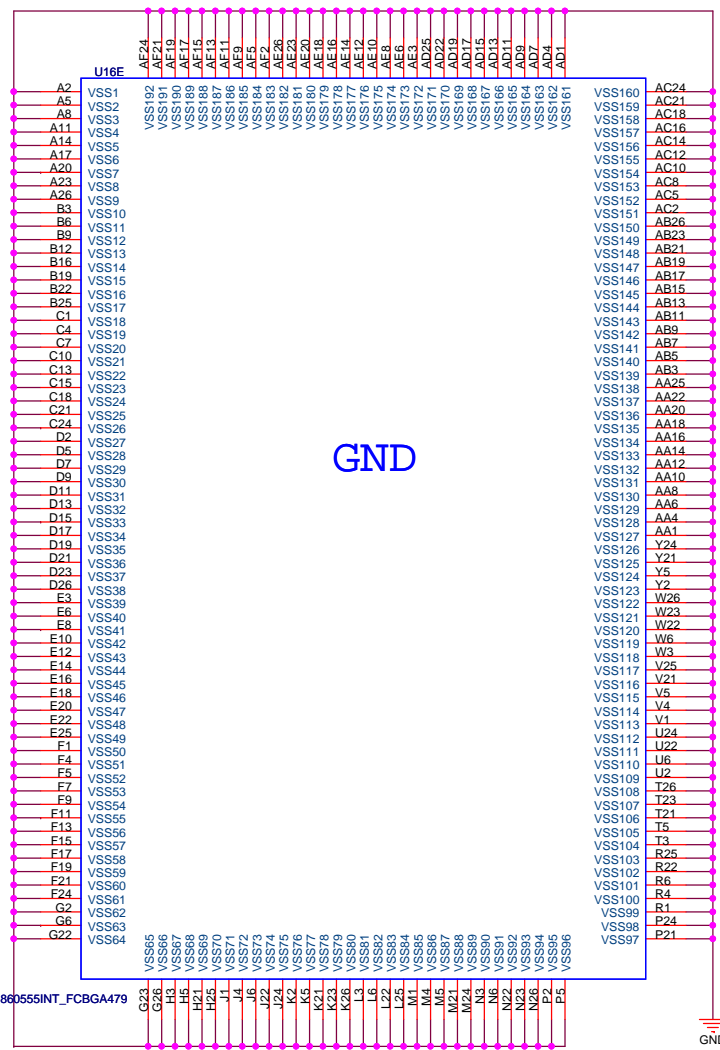
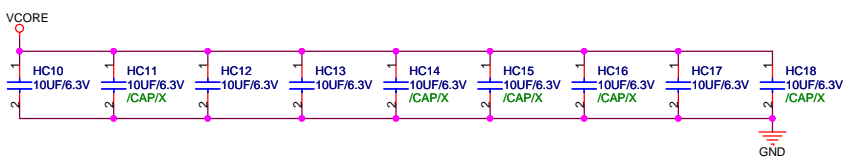
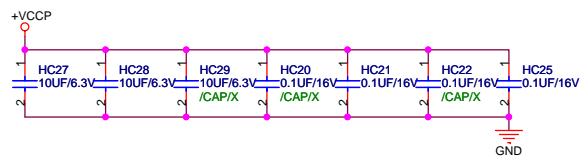
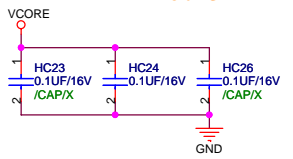


Celeron-M(Dothan) ULV max 7 A

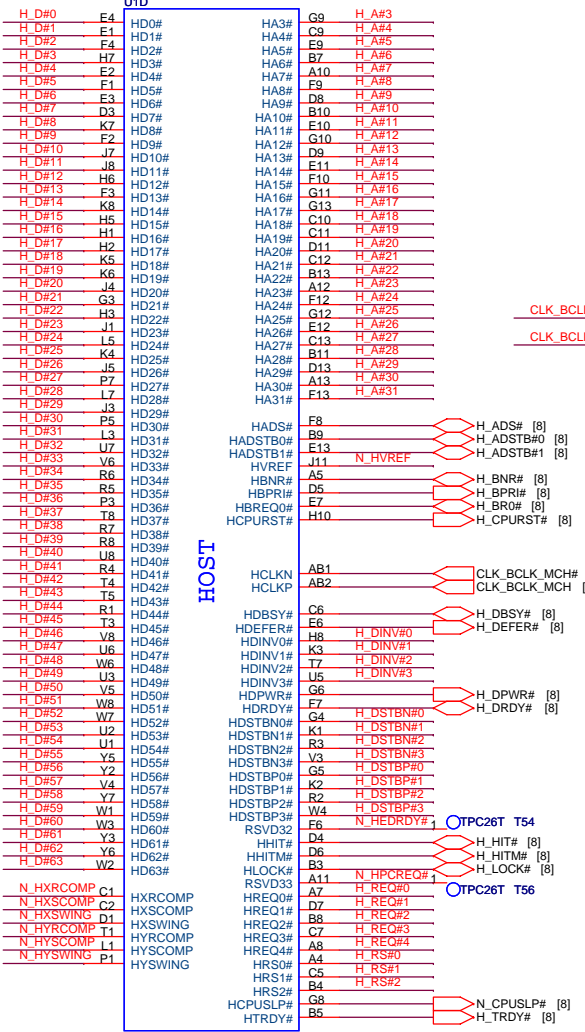
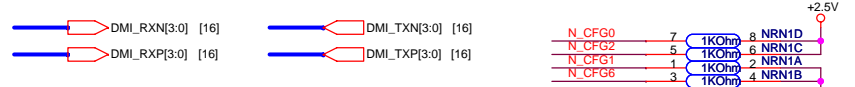


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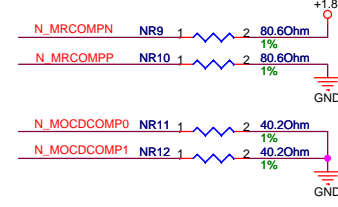
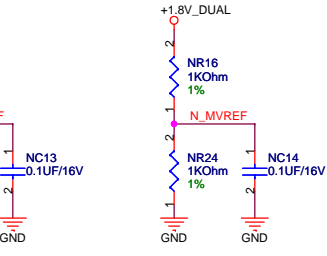
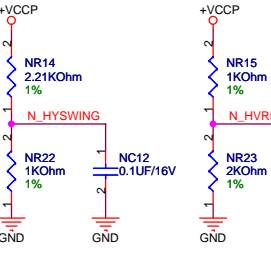
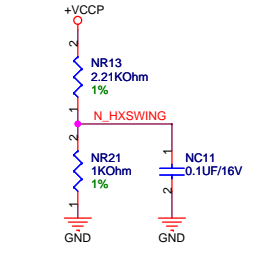
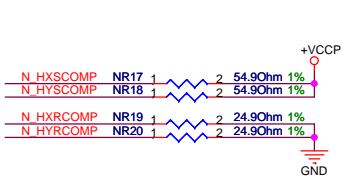
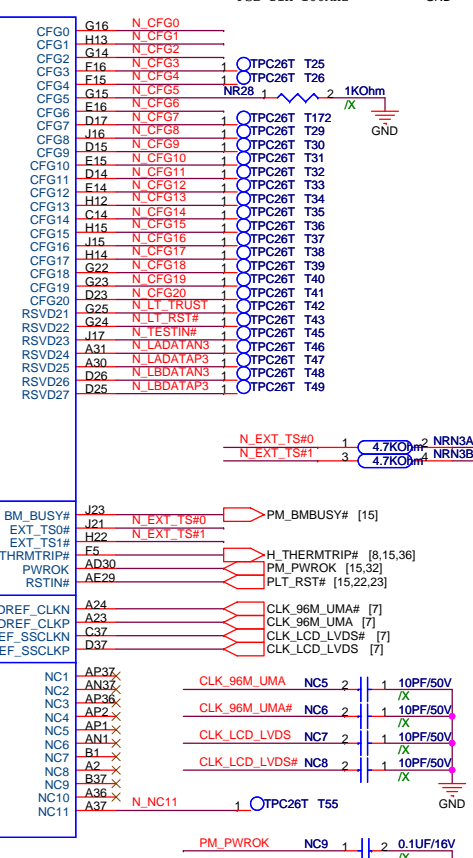
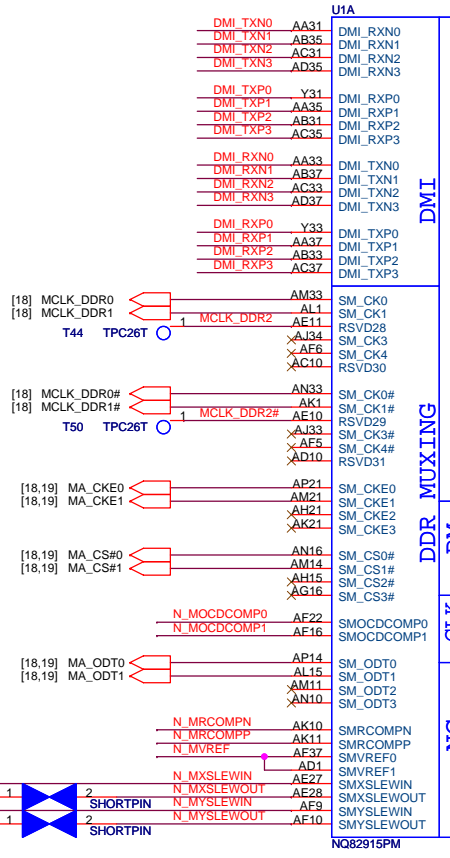
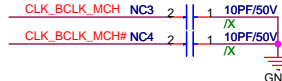
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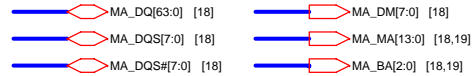
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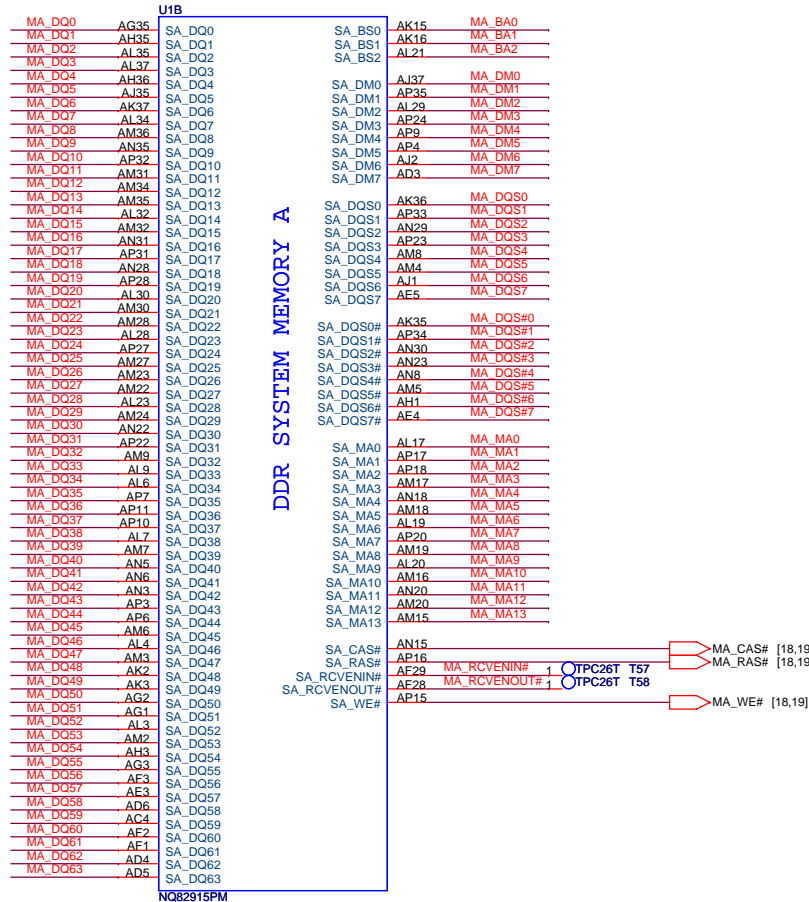
U1 use 02G010007612



ASUS logo and project information: Title: 910GML_HOST_DMI, ASUSTek Computer INC., Engineer: Kell Huang, Project Name: P701, Date: Saturday, September 01, 2007, Sheet 10 of 47, Rev 1.2G.



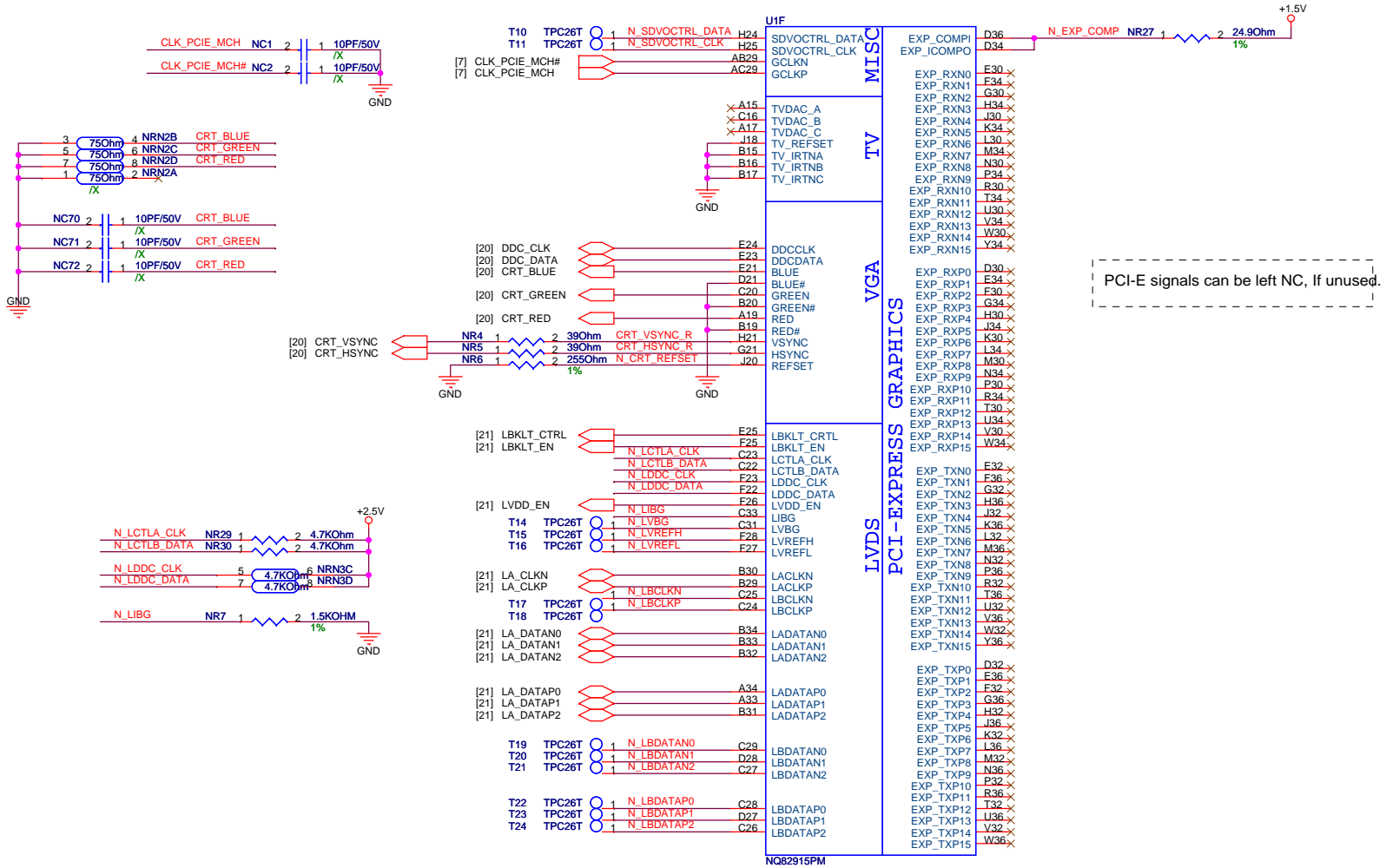
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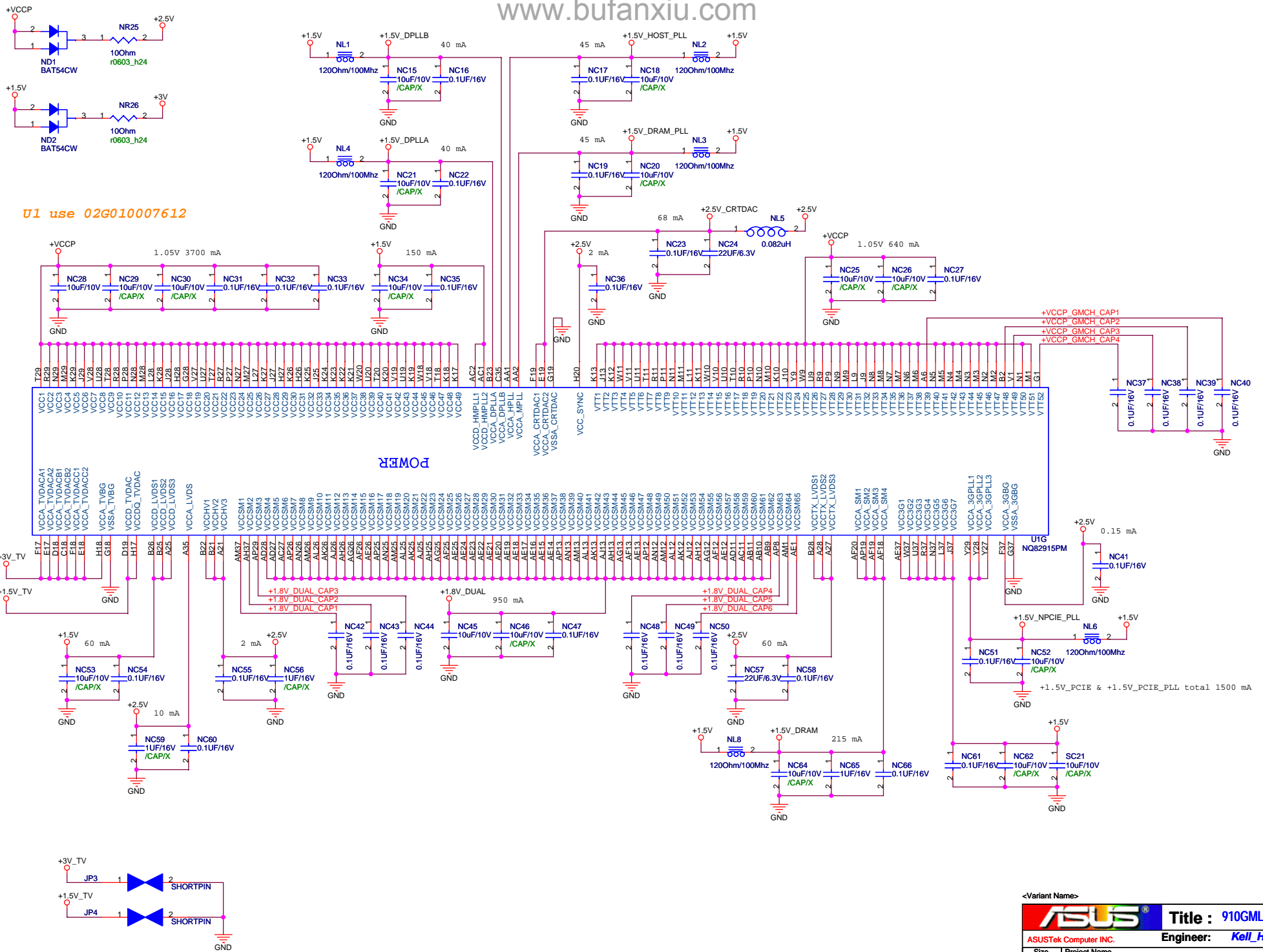
SDVO SMBus have internal pull down

SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

U1 use 02G010007612



PCI-E signals can be left NC, If unused.

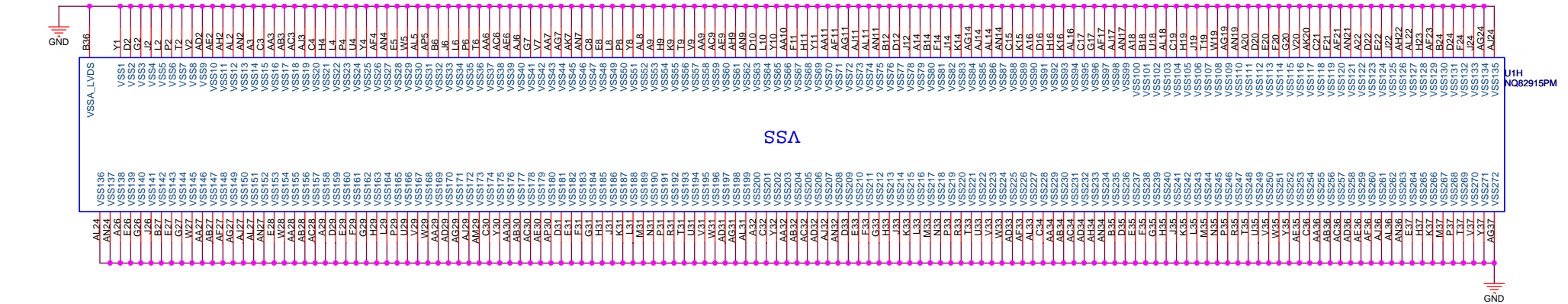
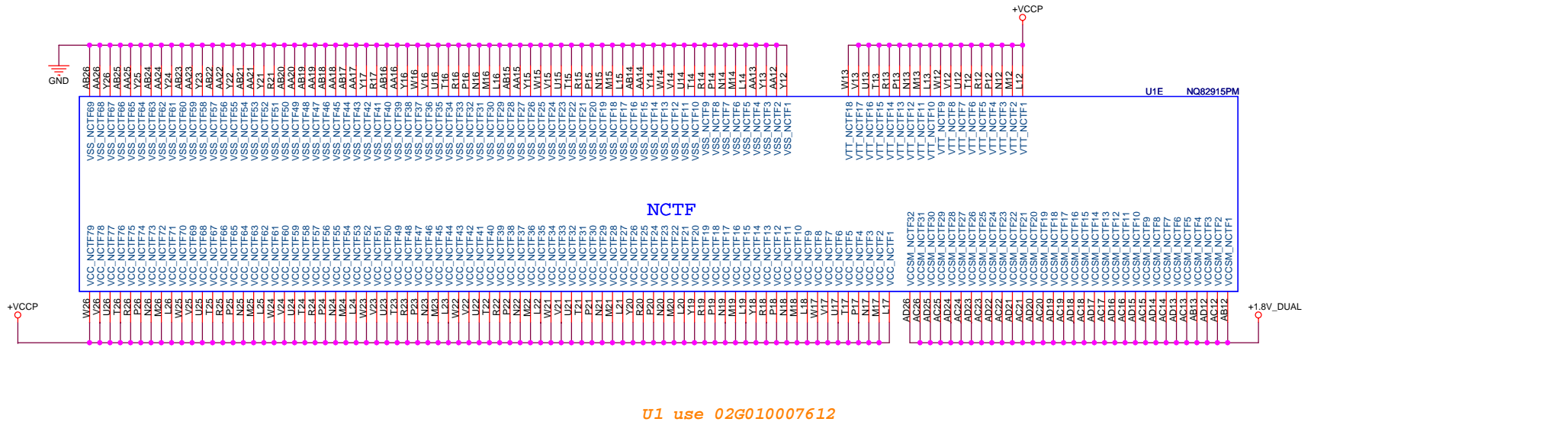


<Variant Name>

ASUS Title : 910GML_PWR

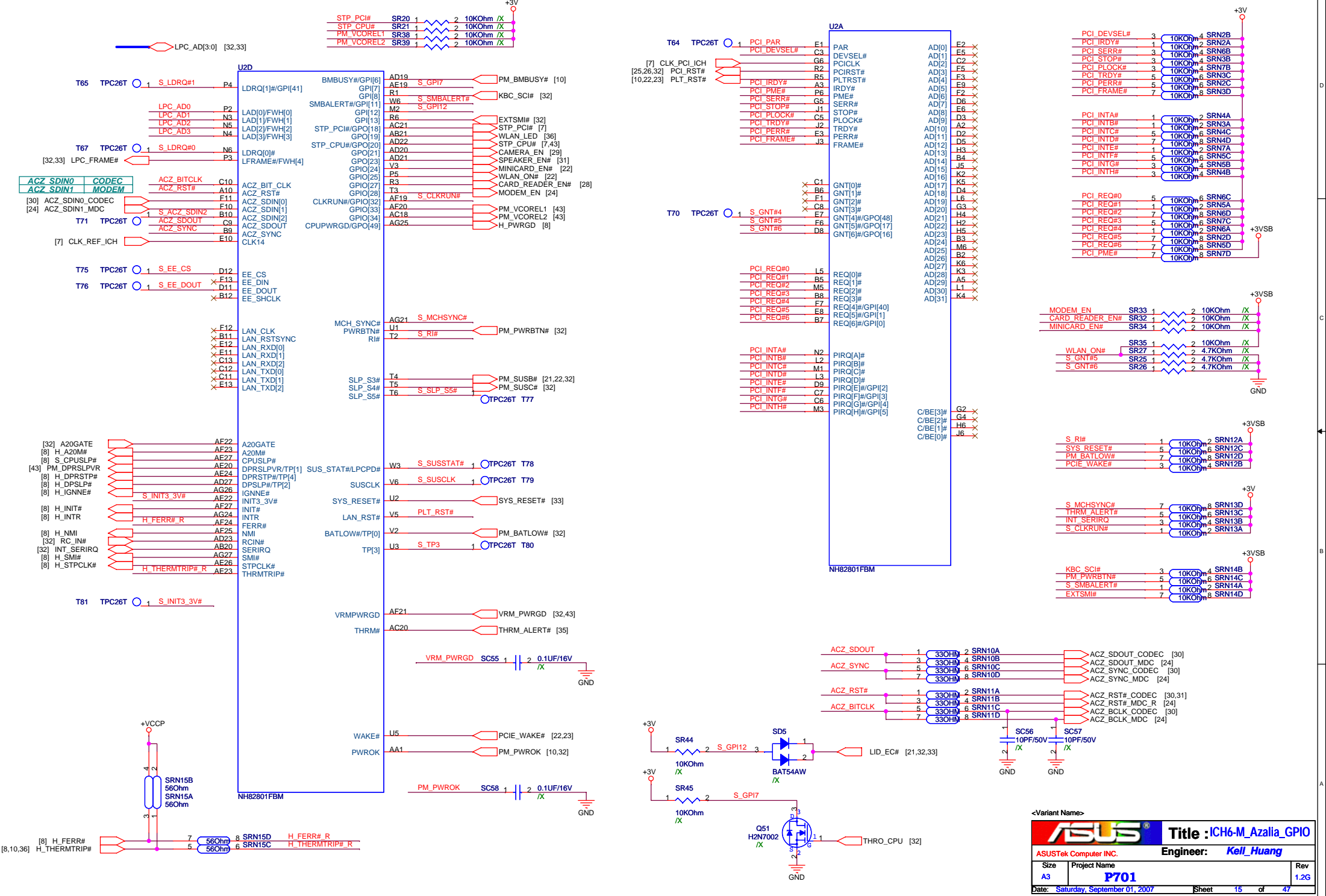
ASUSTek Computer INC. Engineer: Keil_Huang

Size	Project Name	Rev
A3	P701	1.2G
Date: Saturday, September 01, 2007	Sheet	13 of 47



<Variant Name>

		Title : 910GML_GND	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size	Project Name		Rev
A3	P701		1.2G
Date:	Friday, August 24, 2007	Sheet	14 of 47



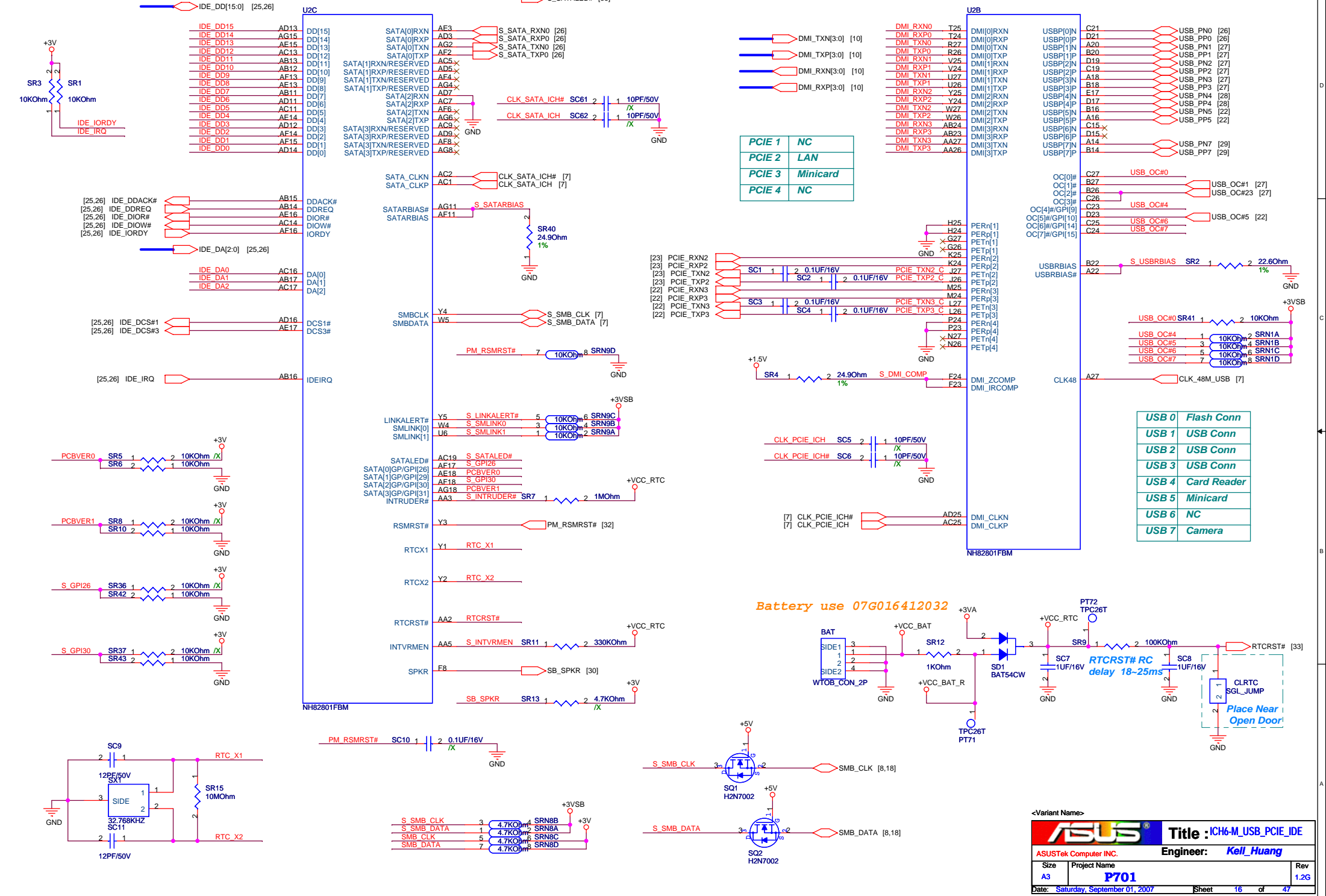
<Variant Name>

ASUS Title : ICH6-M_Azalia_GPIO

ASUSTek Computer INC. Engineer: Keil_Huang

Size	Project Name	Rev
A3	P701	1.2G

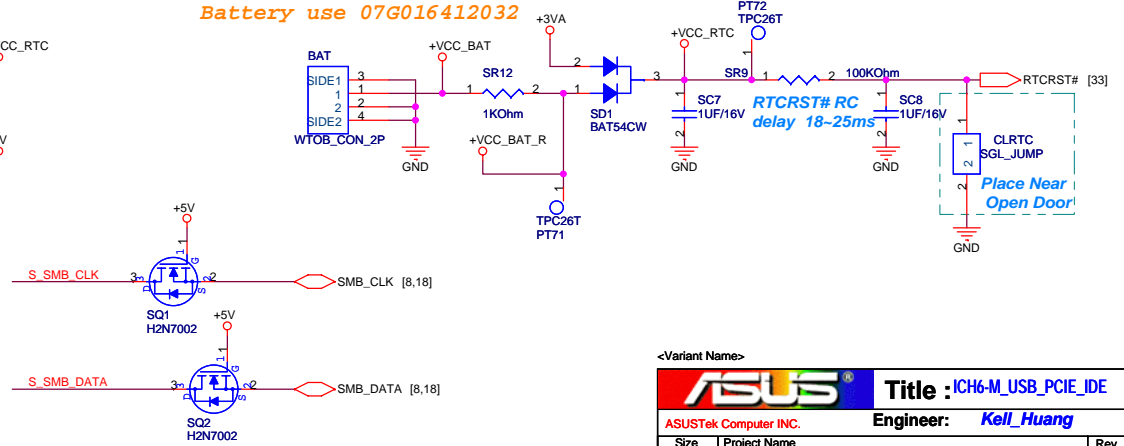
Date: Saturday, September 01, 2007 Sheet 15 of 47



PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	NC
USB 7	Camera

Battery use 07G016412032



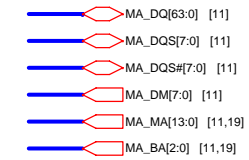
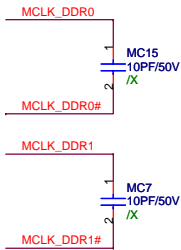
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ASUS Title : ICH6-M_USB_PCIE_IDE

ASUSTek Computer INC. Engineer: **Keil_Huang**

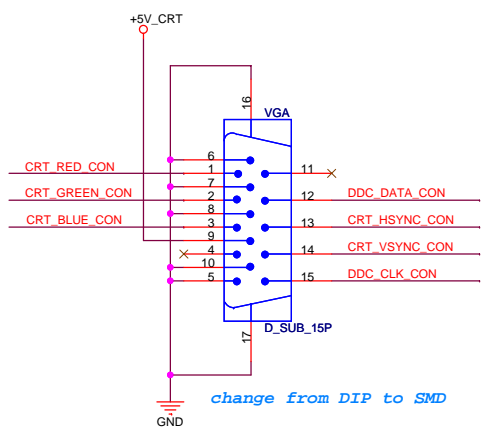
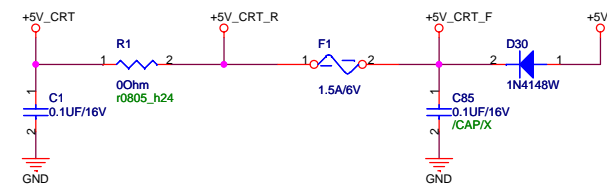
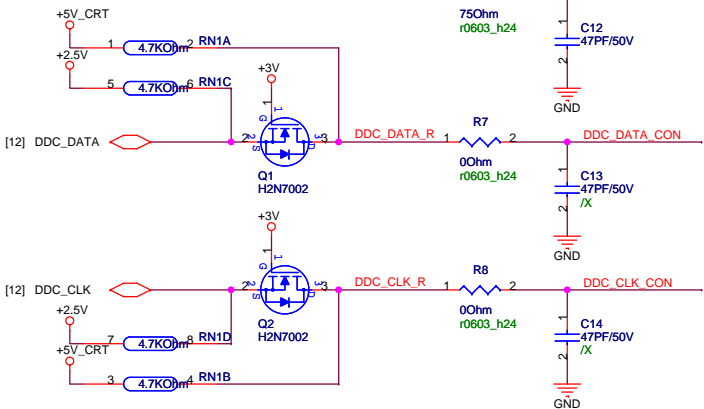
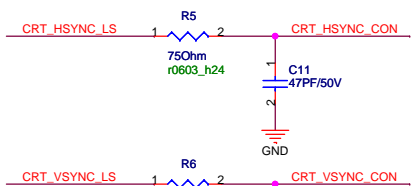
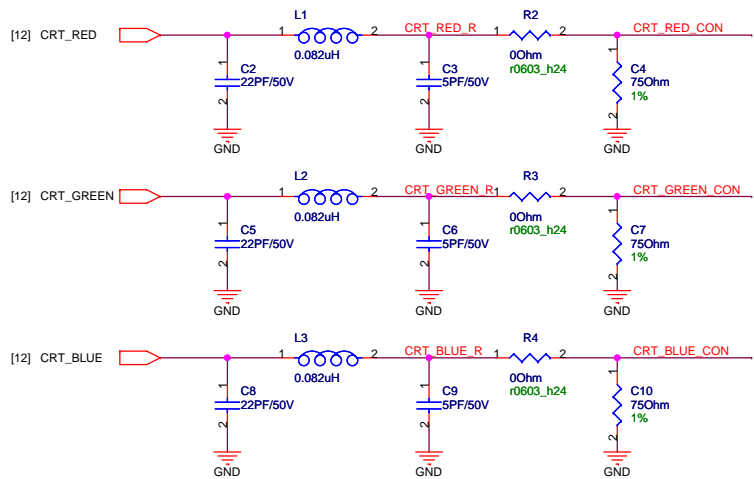
Size	Project Name	Rev
A3	P701	1.2G

Date: Saturday, September 01, 2007 Sheet 16 of 47

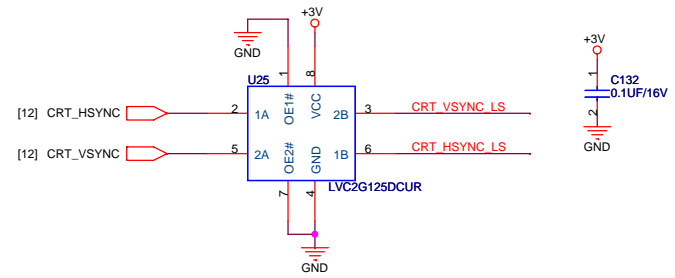
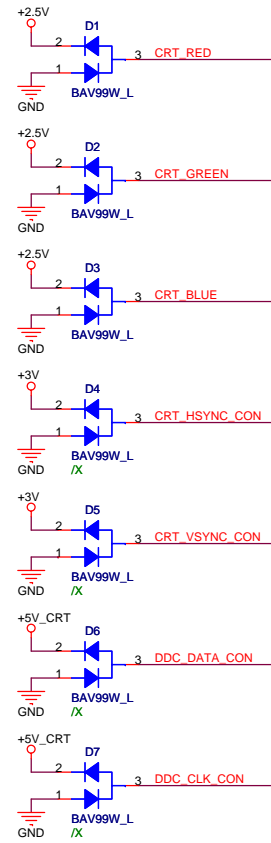


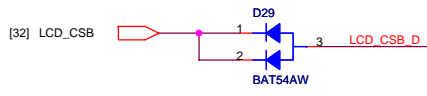
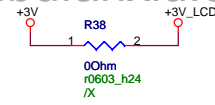
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MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	105	A9	DQ9
MA_MA10	91	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	86	A14	DQ14
	84	A15	DQ15
	85	A16_BA2	DQ16
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MA_BA1	106	BA1	DQ19
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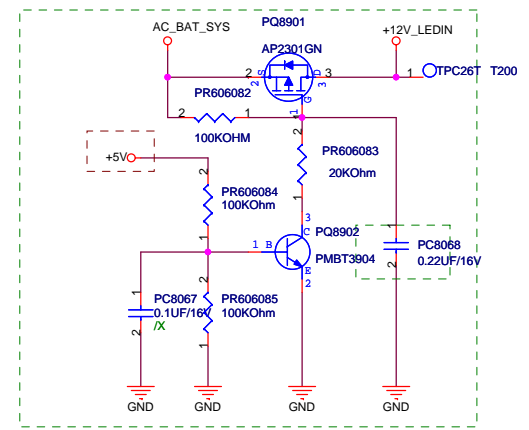
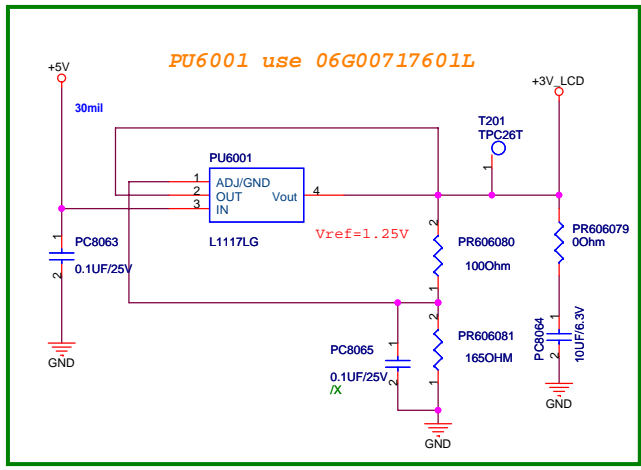
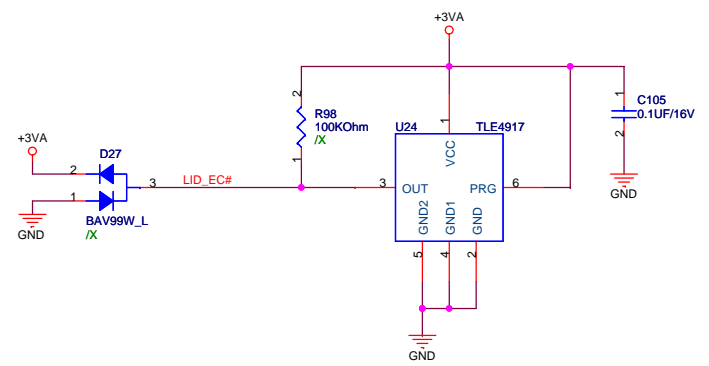
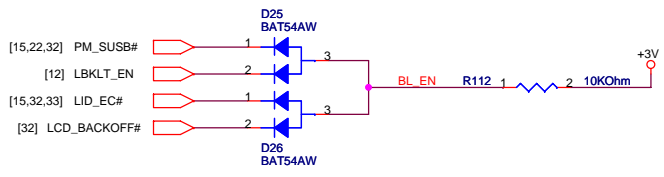
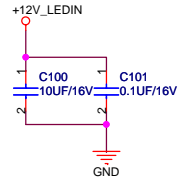
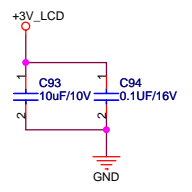
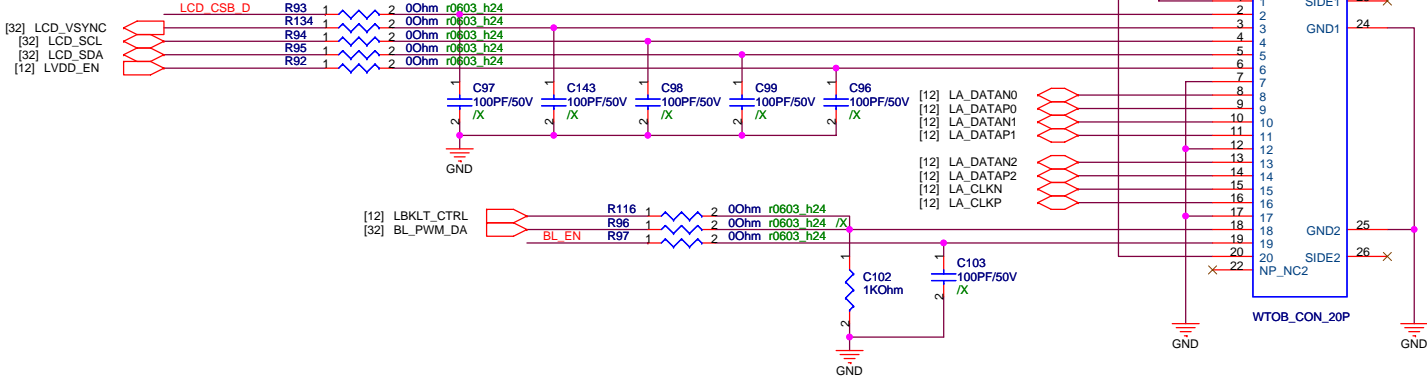


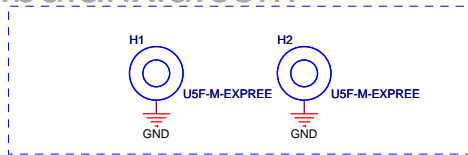
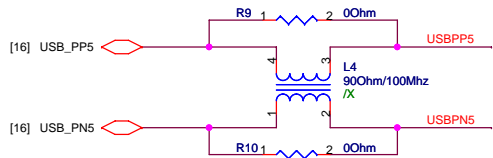
VGA use 12G10110015W & 12G10110015N



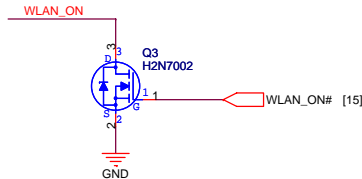
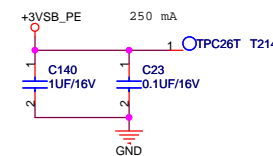
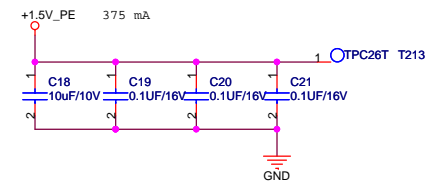
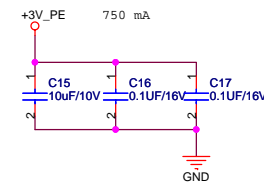


Remove R134 for LCD Board 1.4G, need rework

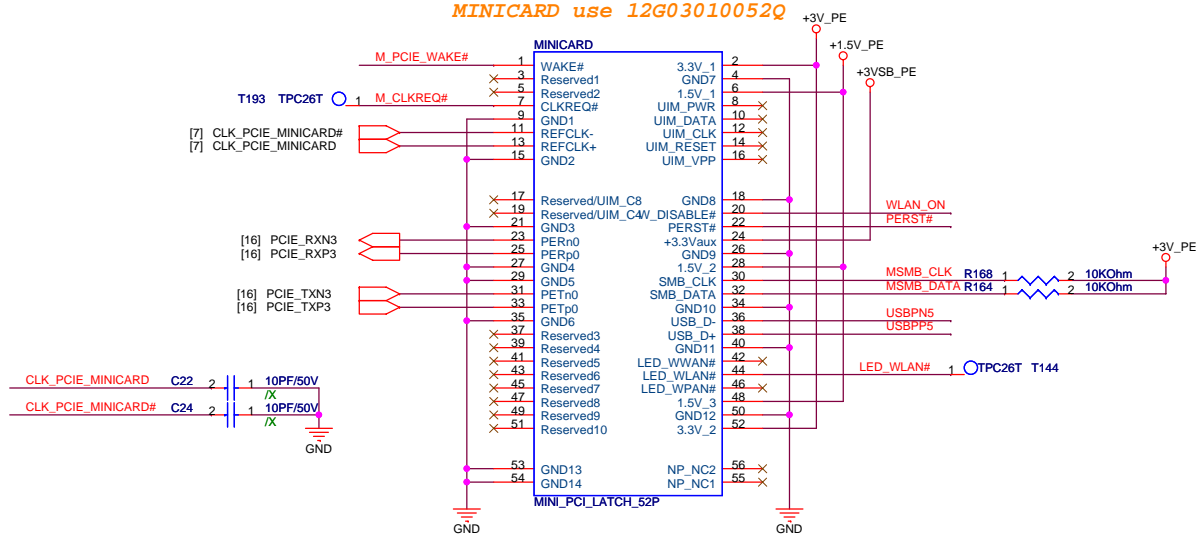




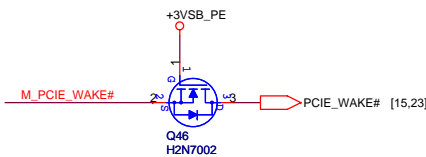
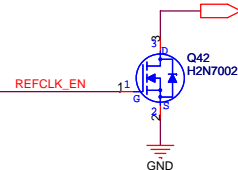
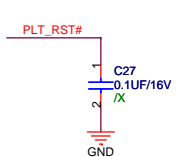
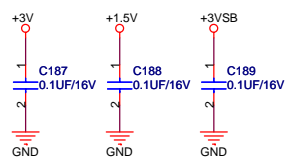
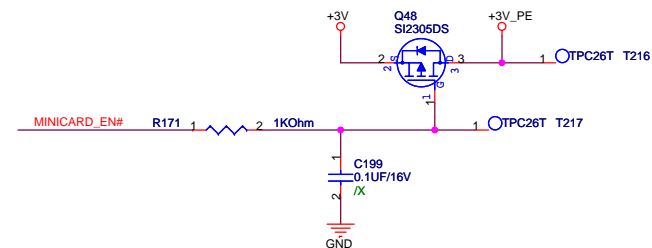
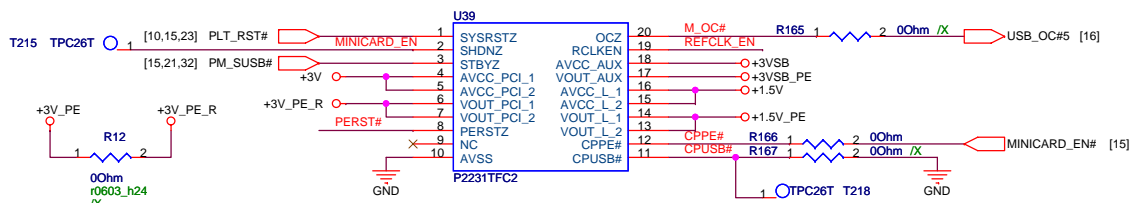
MINI CARD NUT(1.6mm) *2



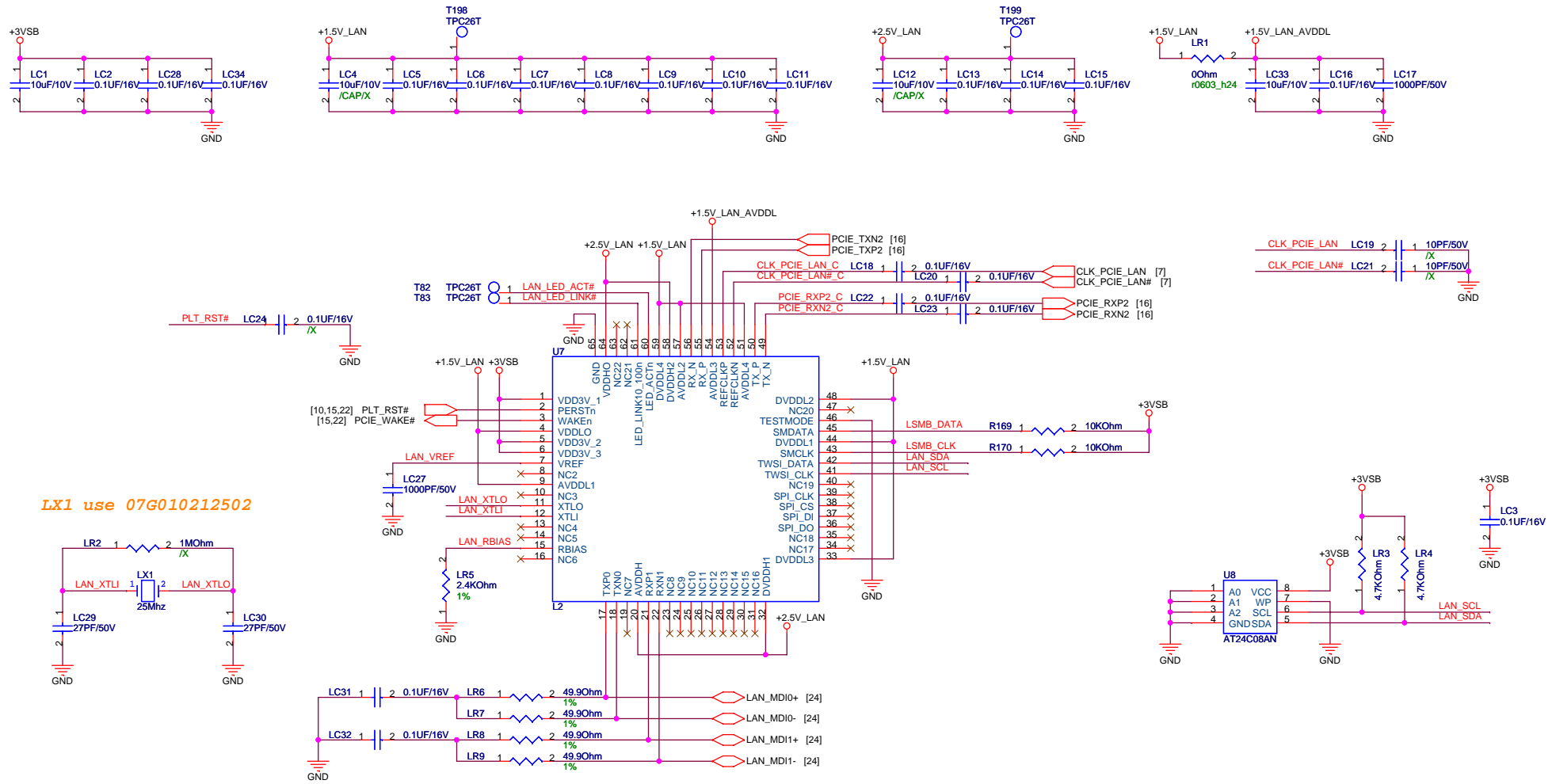
MINICARD use 12G03010052Q



U39 use 06G030057011



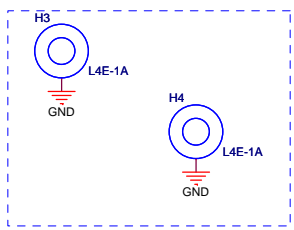
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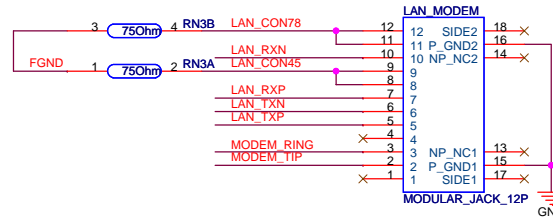
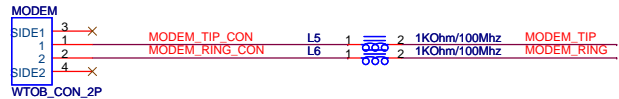
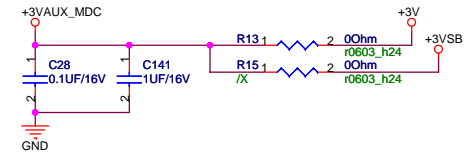
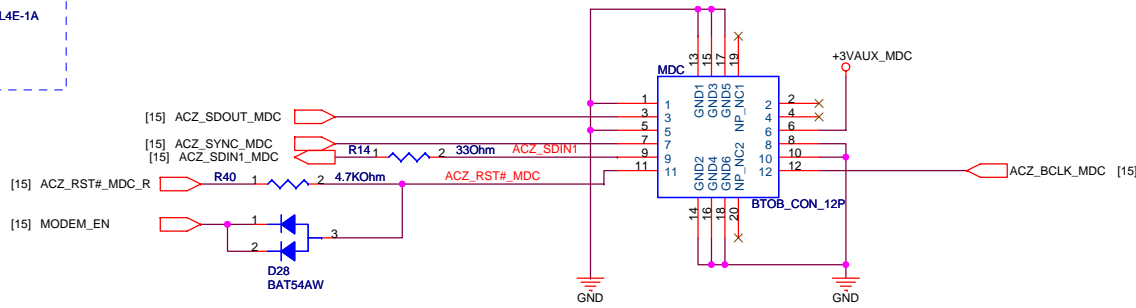
LX1 use 07G010212502

<Variant Name>

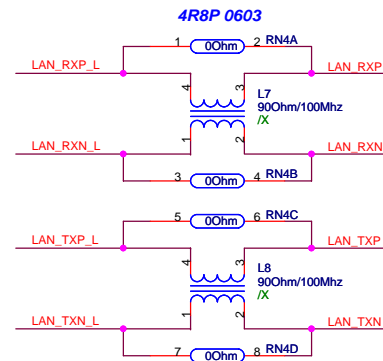
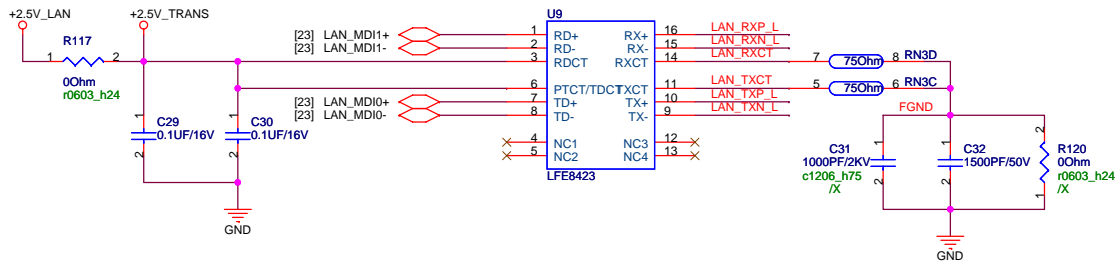
		Title : LAN_Atheros L2	
ASUSTek Computer INC.		Engineer: <i>Keil_Huang</i>	
Size	Project Name		Rev
A3	P701		1.2G
Date:	Tuesday, September 04, 2007	Sheet	23 of 47



MODEM NUT(3.0mm) *2

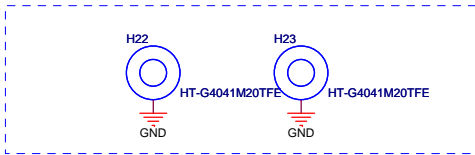


U9 use 09G051050100

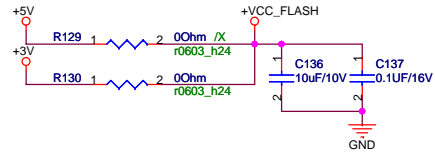


<Variant Name>

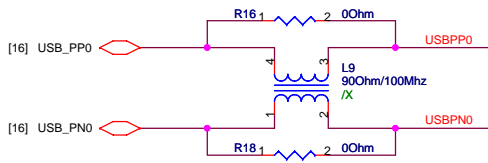
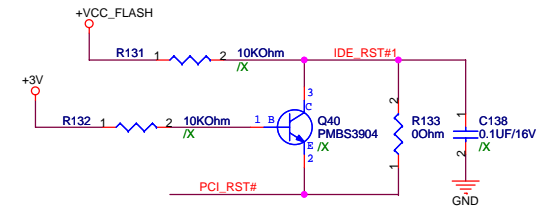
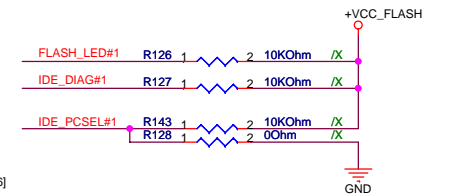
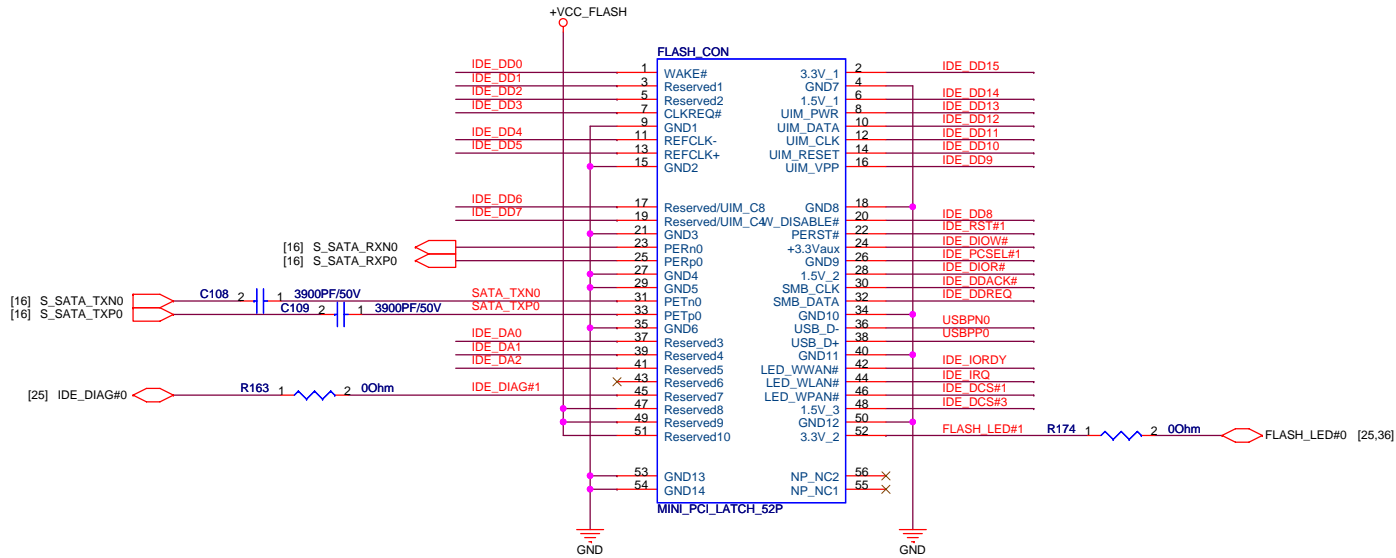
ASUS		Title : MDC_RJ11_RJ45	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size	Project Name	Rev	
A3	P701	1.2G	
Date: Saturday, September 01, 2007	Sheet	24	of 47



FLASH CARD NUT(3.3mm) *2

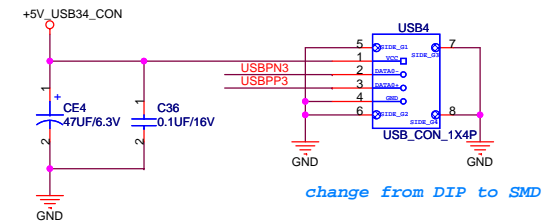
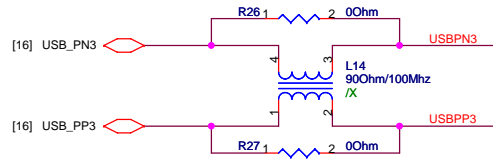
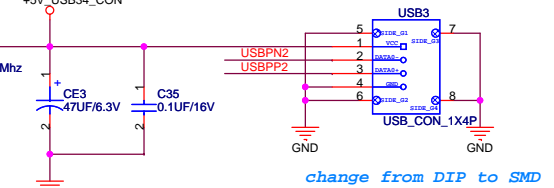
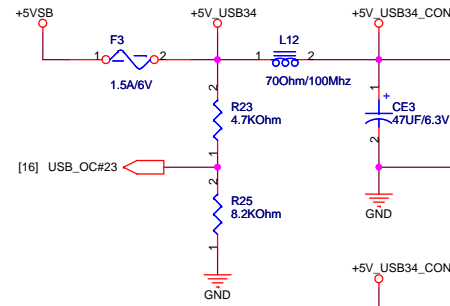
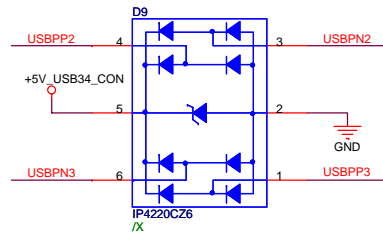
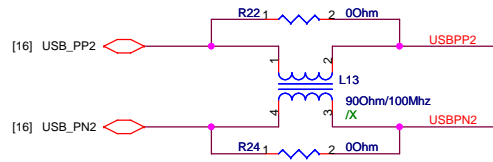
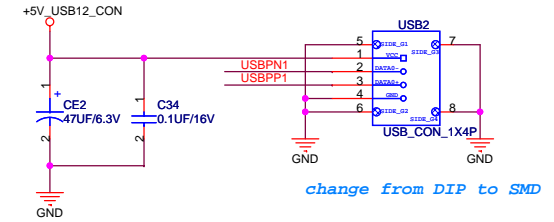
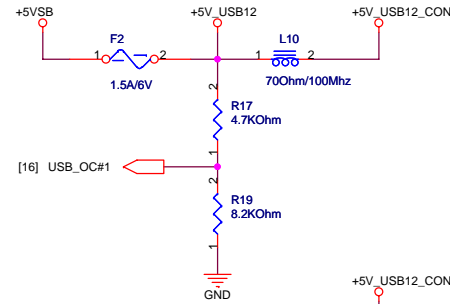
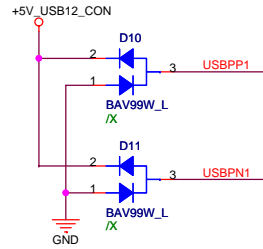
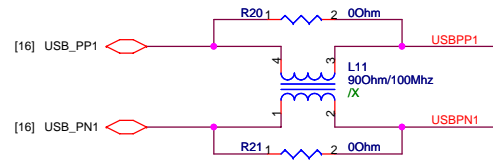


- IDE_DD[15:0] [16,25]
- IDE_DA[2:0] [16,25]
- IDE_DDACK# [16,25]
- IDE_DDREQ [16,25]
- IDE_DIOR# [16,25]
- IDE_DIOW# [16,25]
- IDE_IORDY [16,25]
- IDE_DCS#1 [16,25]
- IDE_DCS#3 [16,25]
- IDE_IRQ [16,25]
- PCI_RST# [15,25,32]
- FLASH_LED#1 [36]



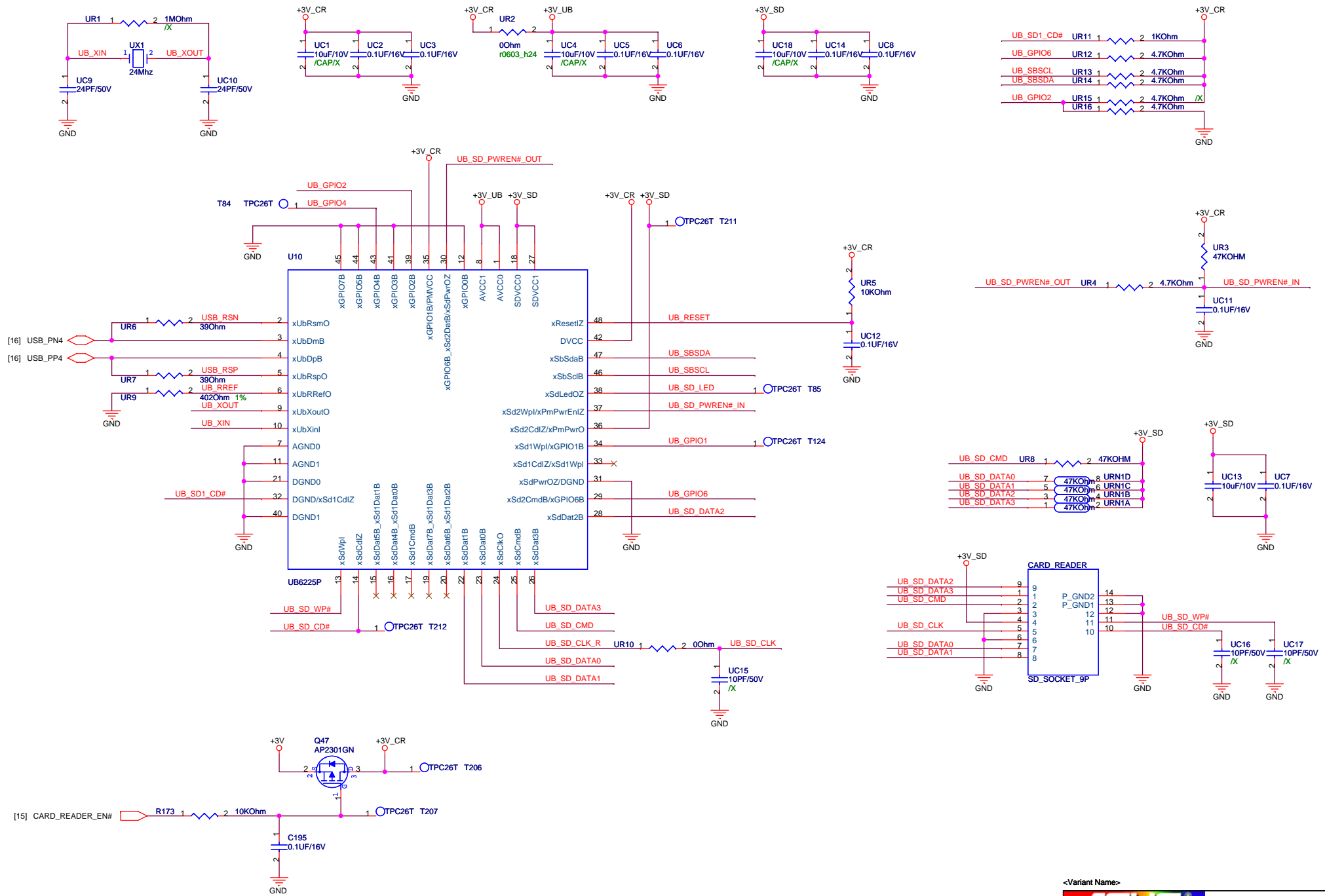
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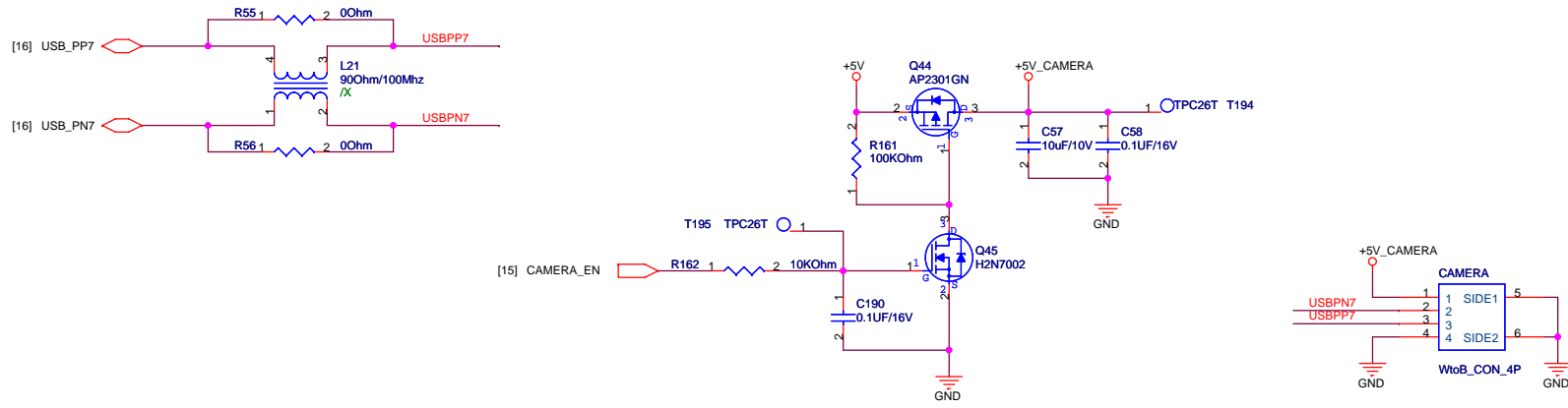
ASUS		Title : Flash Conn	
ASUSTek Computer INC.		Engineer: <i>Keil_Huang</i>	
Size	Project Name	Rev	
A3	P701	1.2G	
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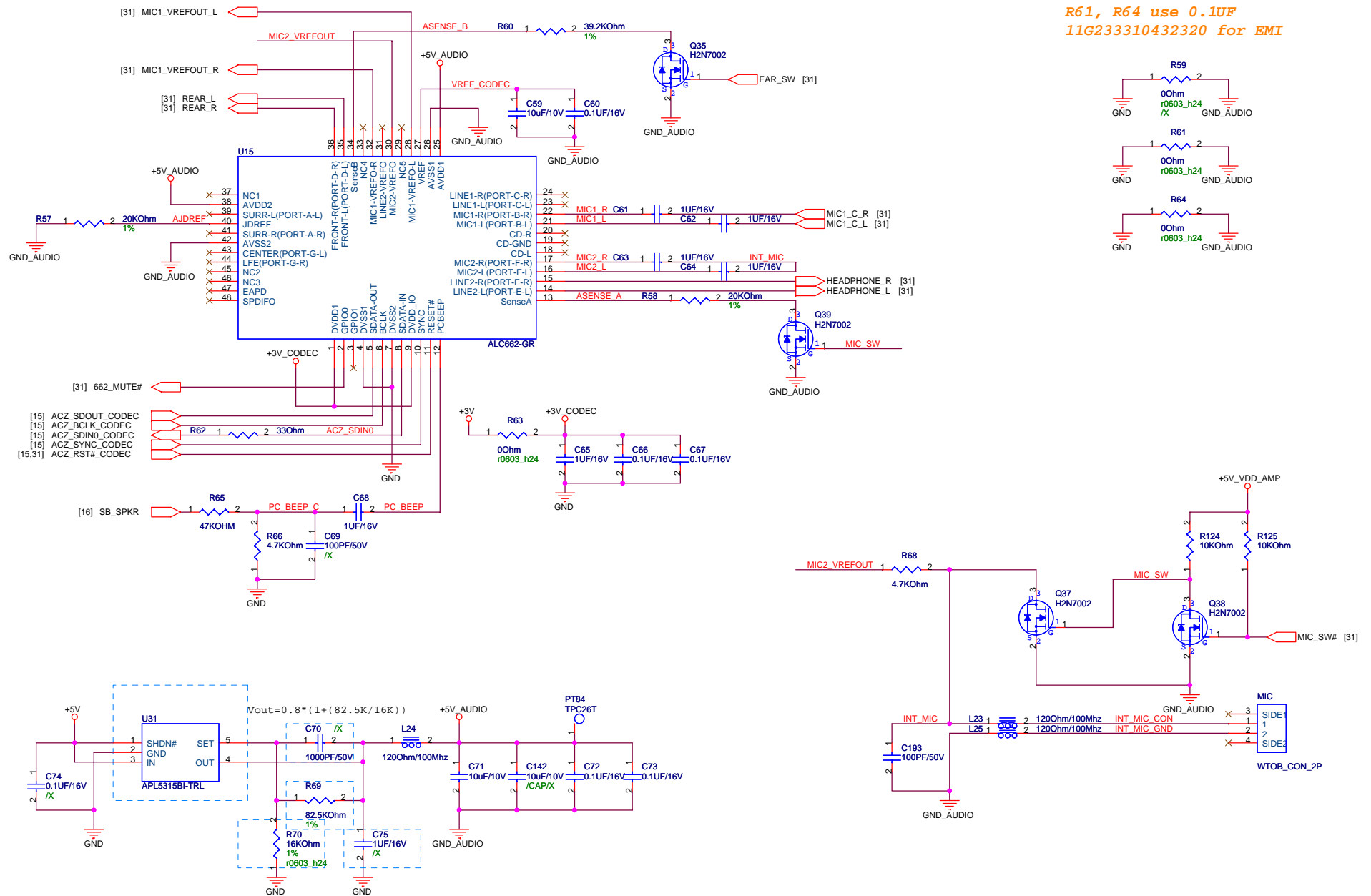


<Variant Name>

		Title : USB Port	
ASUSTek Computer INC.		Engineer: <i>Keil_Huang</i>	
Size	Project Name		Rev
A3	P701		1.2G
Date: Saturday, September 01, 2007		Sheet	27 of 47





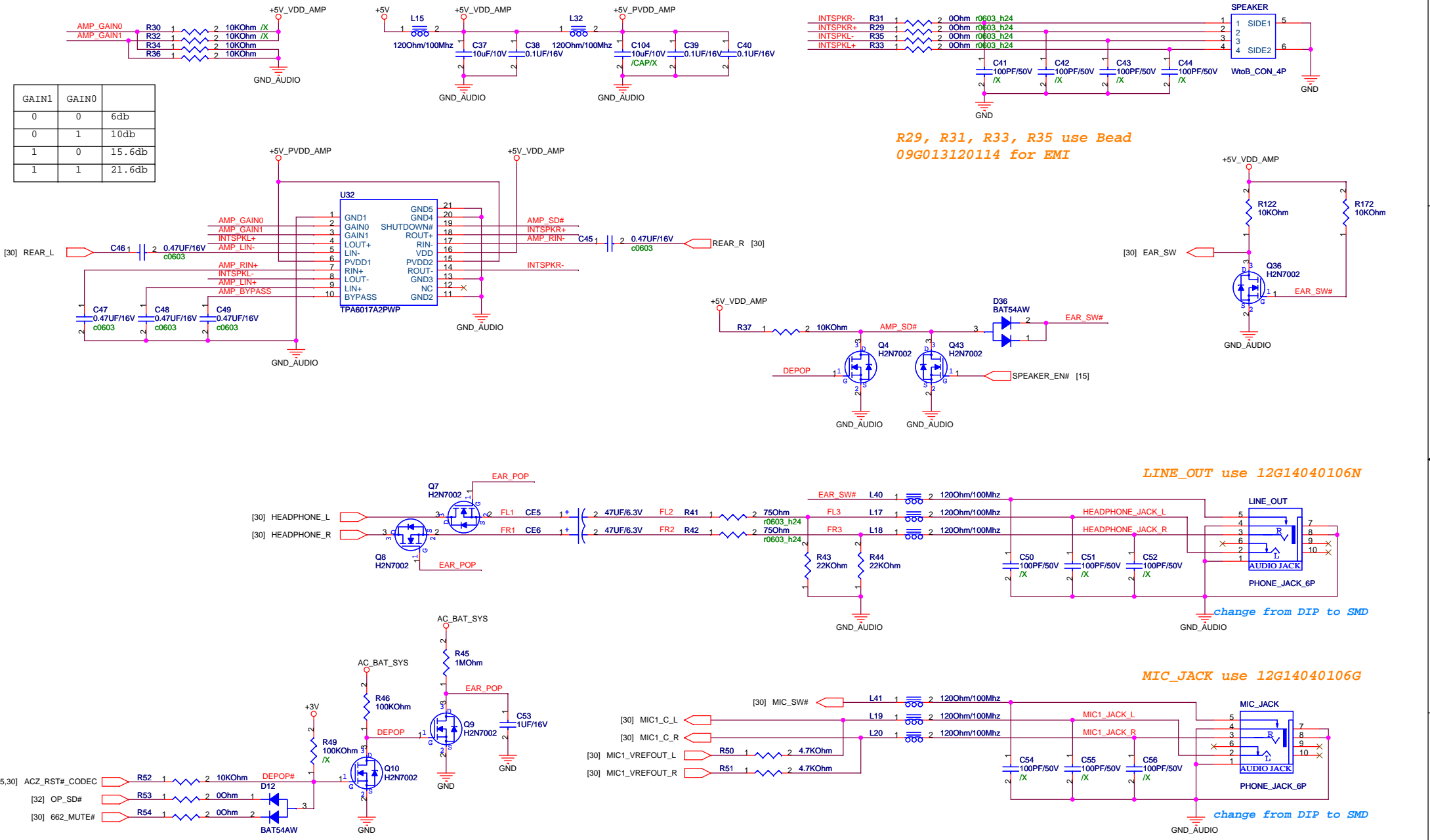


R61, R64 use 0.1uF
11G233310432320 for EMI

<Variant Name>

ASUS		Title : Codec_ALC662	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Keil_Huang</i>	
Size	Project Name		Rev
A3	P701		1.2G
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GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



R29, R31, R33, R35 use Bead 09G013120114 for EMI

LINE_OUT use 12G14040106N

MIC_JACK use 12G14040106G

change from DIP to SMD

change from DIP to SMD

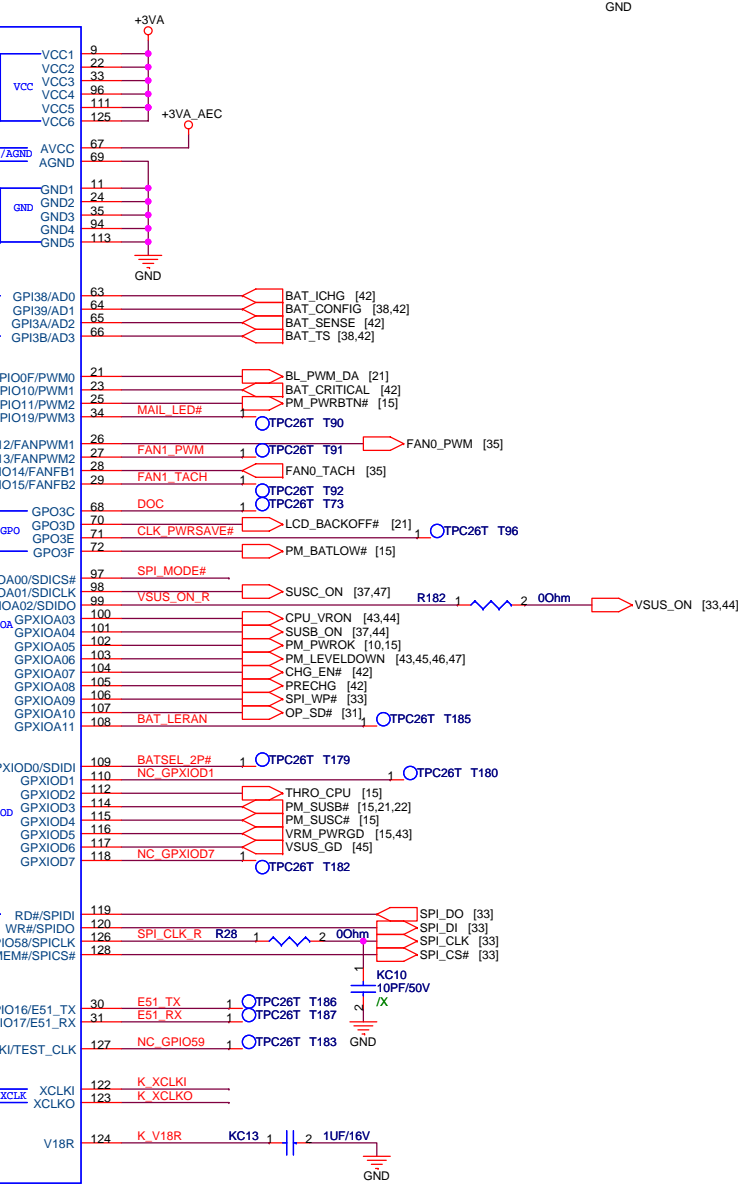
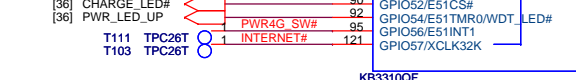
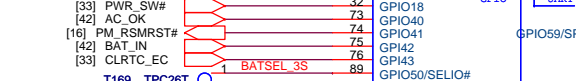
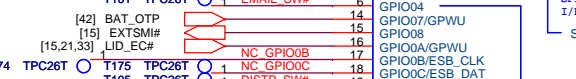
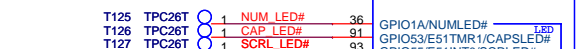
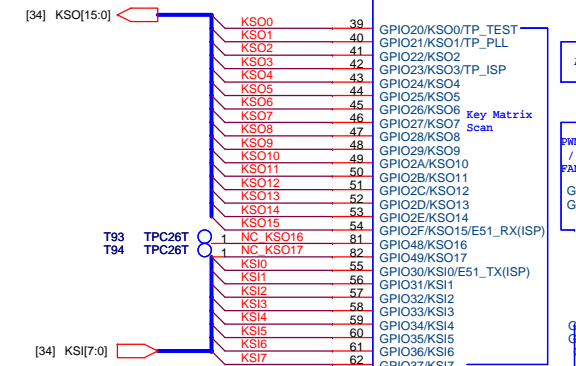
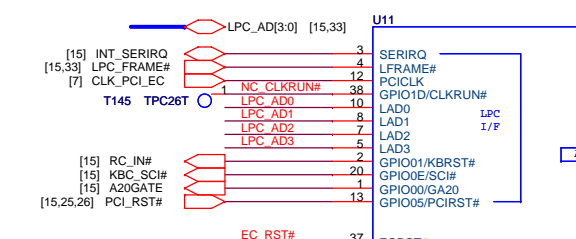
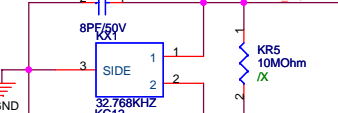
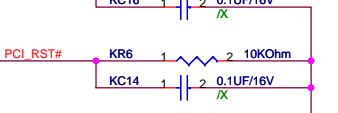
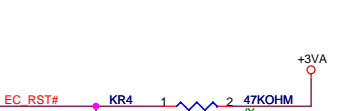
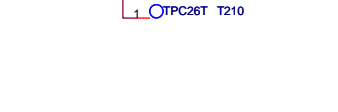
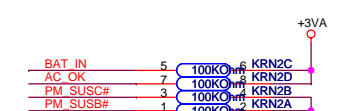
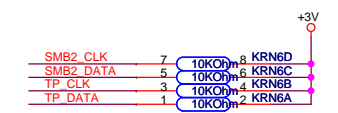
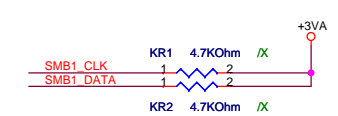
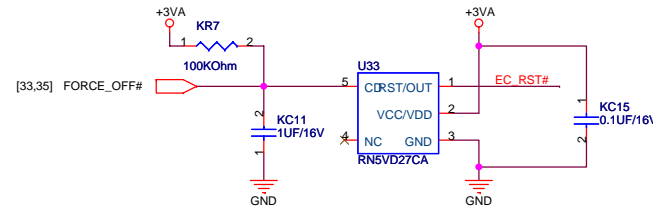
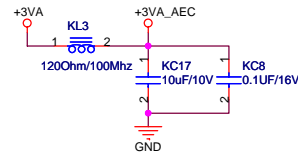
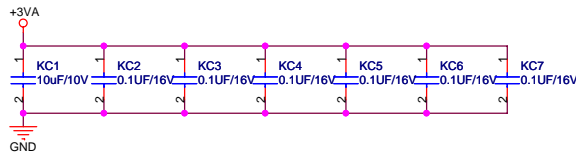
<Variant Name>

ASUS Title : Audio_AMP_Jack

ASUSTek Computer INC. Engineer: *Keil_Huang*

Size	Project Name	Rev
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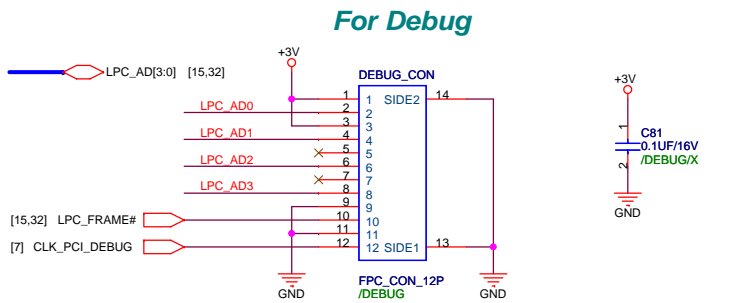
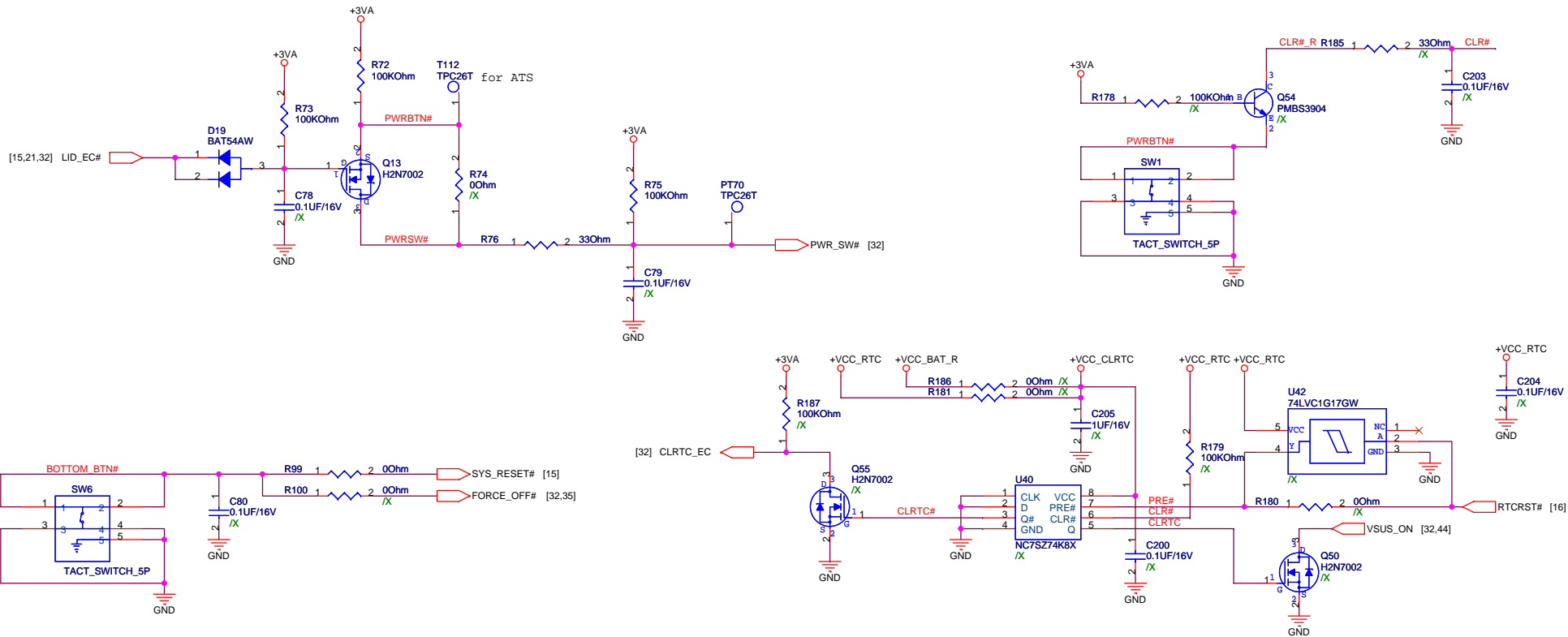
<Variant Name>

ASUS Title : EC_ENE KB3310

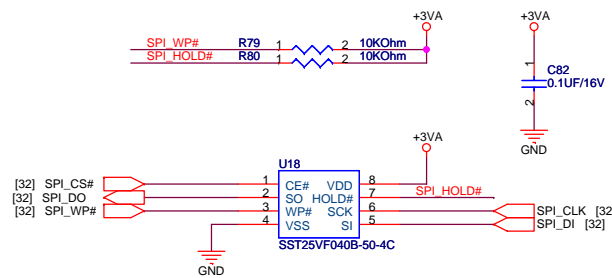
ASUSTek Computer INC. Engineer: Keil_Huang

Size	Project Name	Rev
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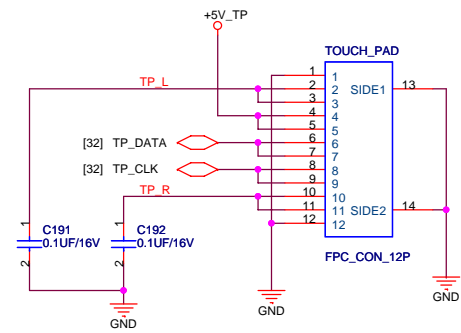


Debug Card cable use Z96 Touch Pad cable, P/N:
 14G124110126, 14G124110120, 14G124110121
 14G124110124, 14G124110125

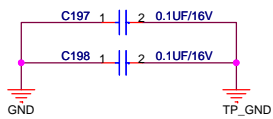
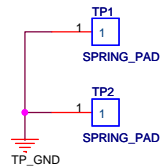
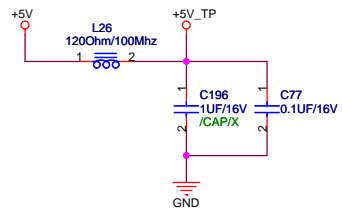
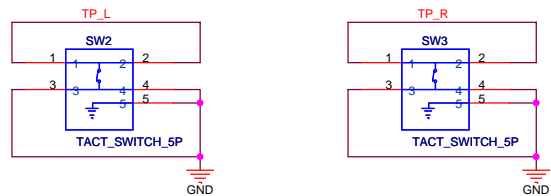


U18 use 05G001002900 & 05G00100F130

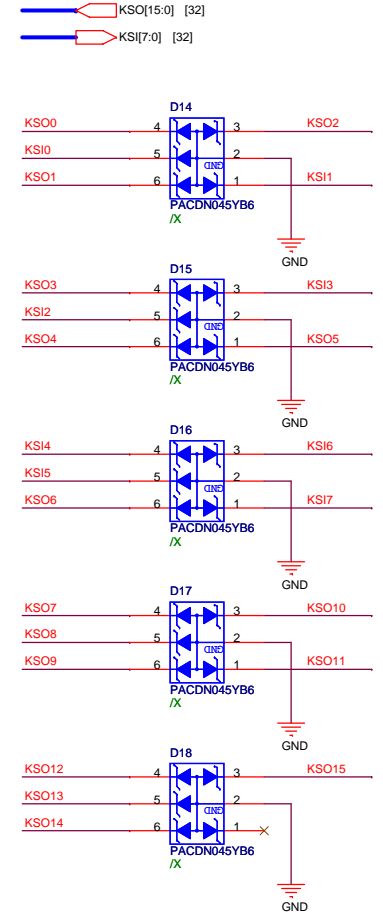
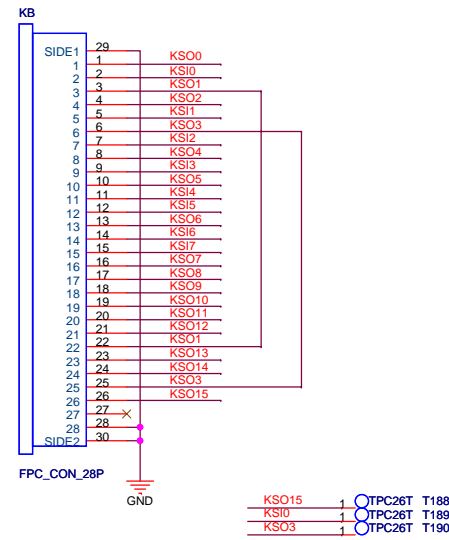
For Touch-Pad

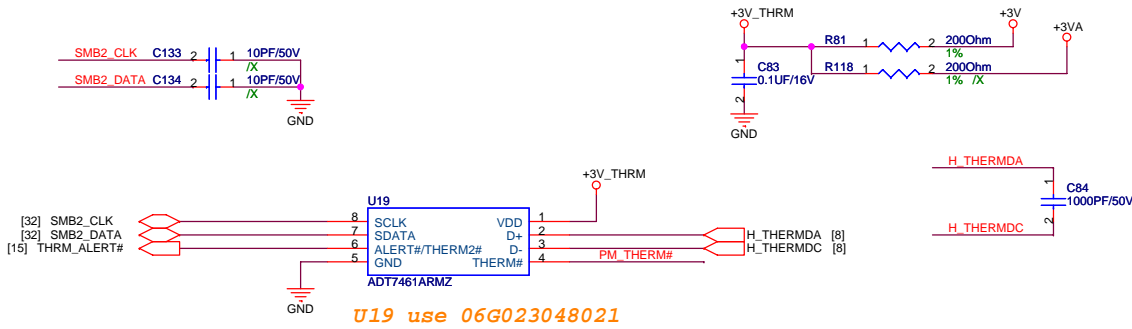


SW2, SW3 use 12G09103305N

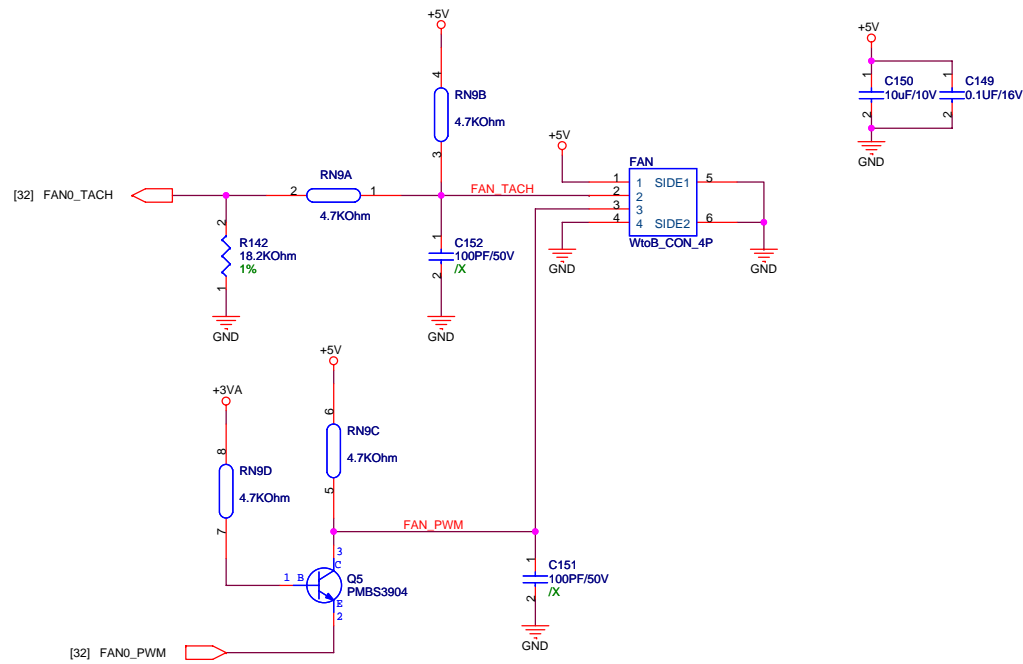
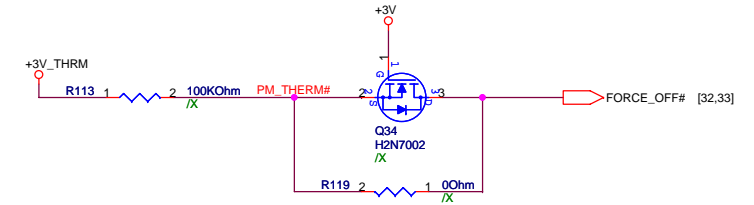


For Keyboard





U19 use 06G023048021

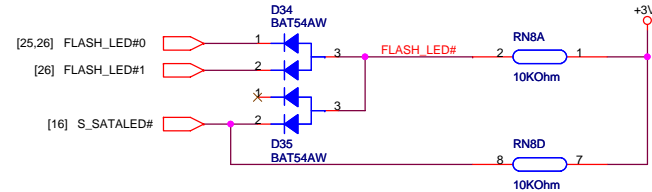
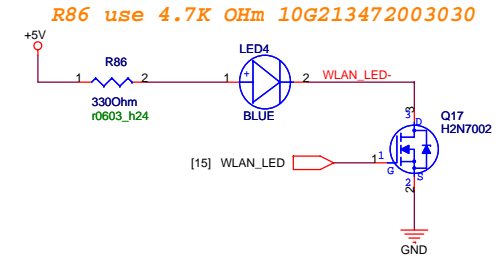
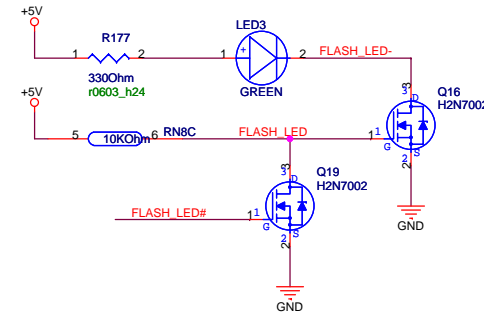
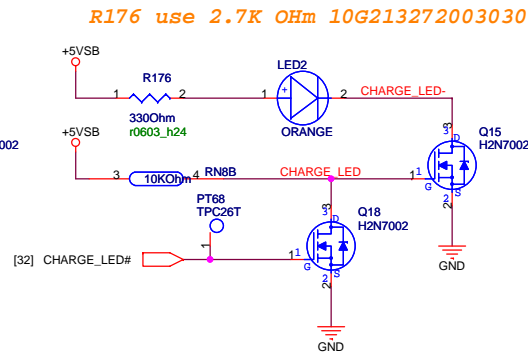
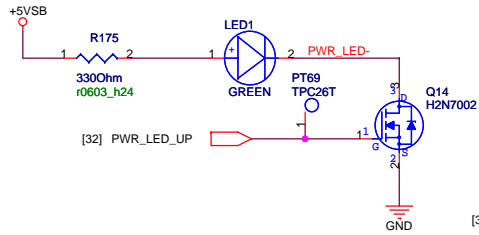


for POWER LED

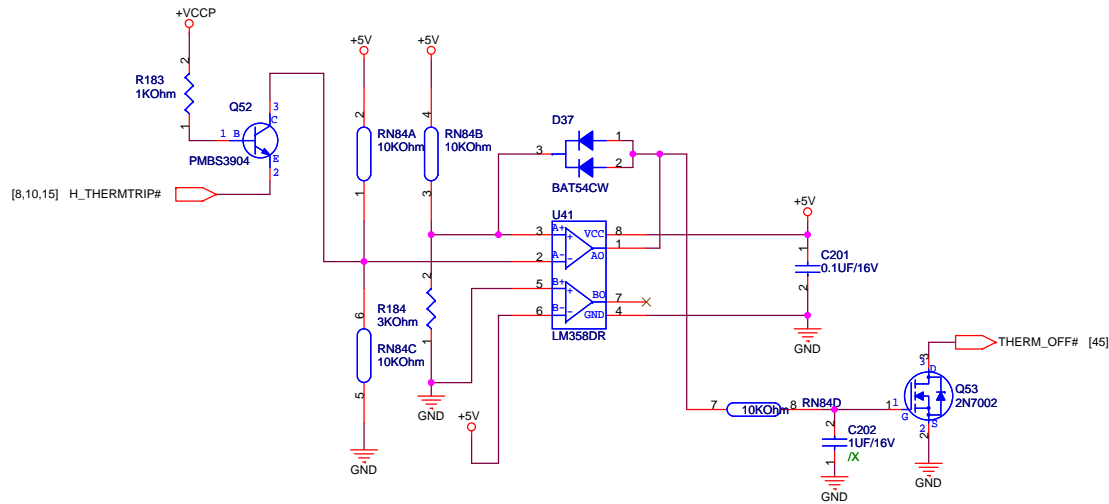
for CHARGE LED

for FLASH LED

for WLAN LED

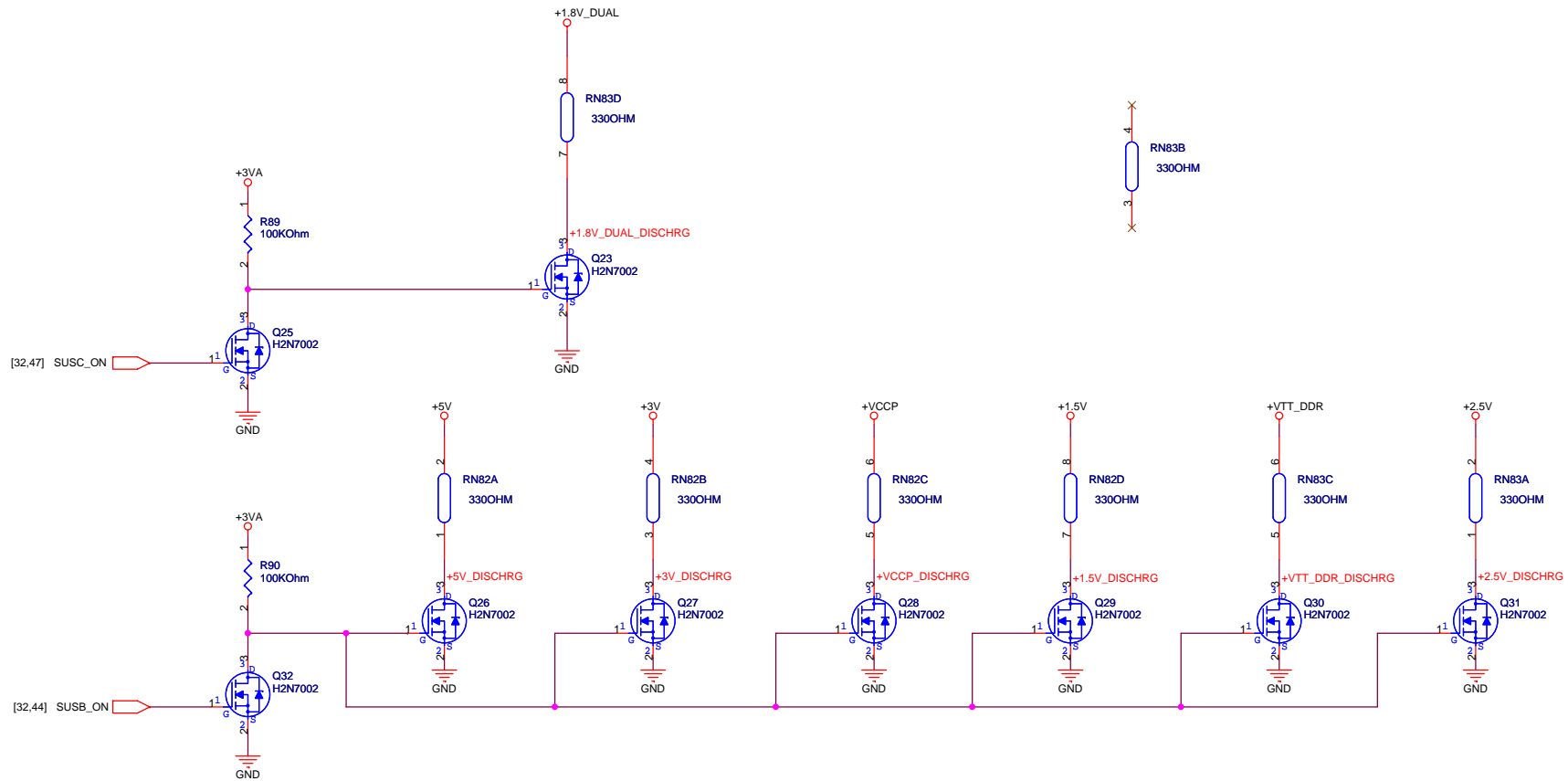


For THERMTRIP



<Variant Name>

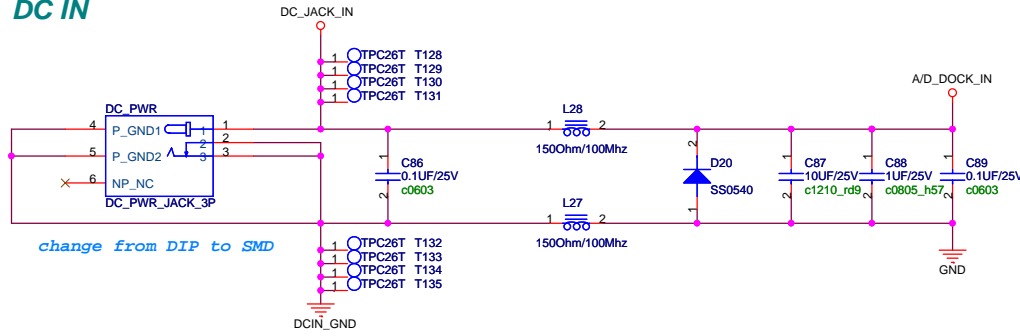
ASUS		Title : LED_THERMTRIP	
ASUSTek Computer INC.		Engineer: <i>Keil_Huang</i>	
Size	Project Name	Rev	
A3	P701	1.2G	
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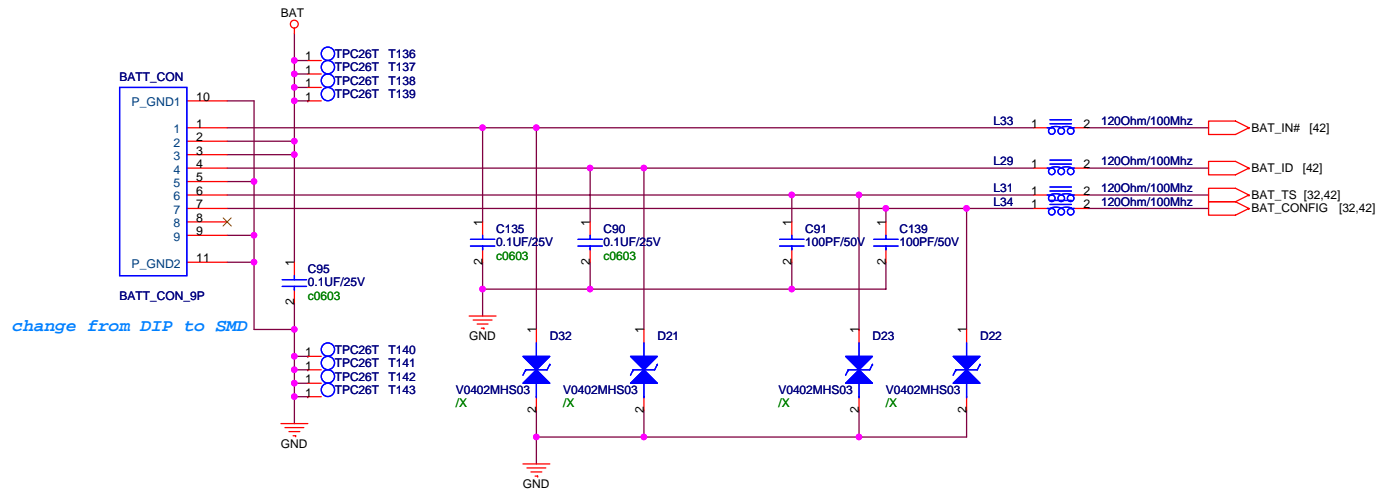
<Variant Name>

		Title : Discharge	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size	Project Name		Rev
A3	P701		1.2G
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DC IN

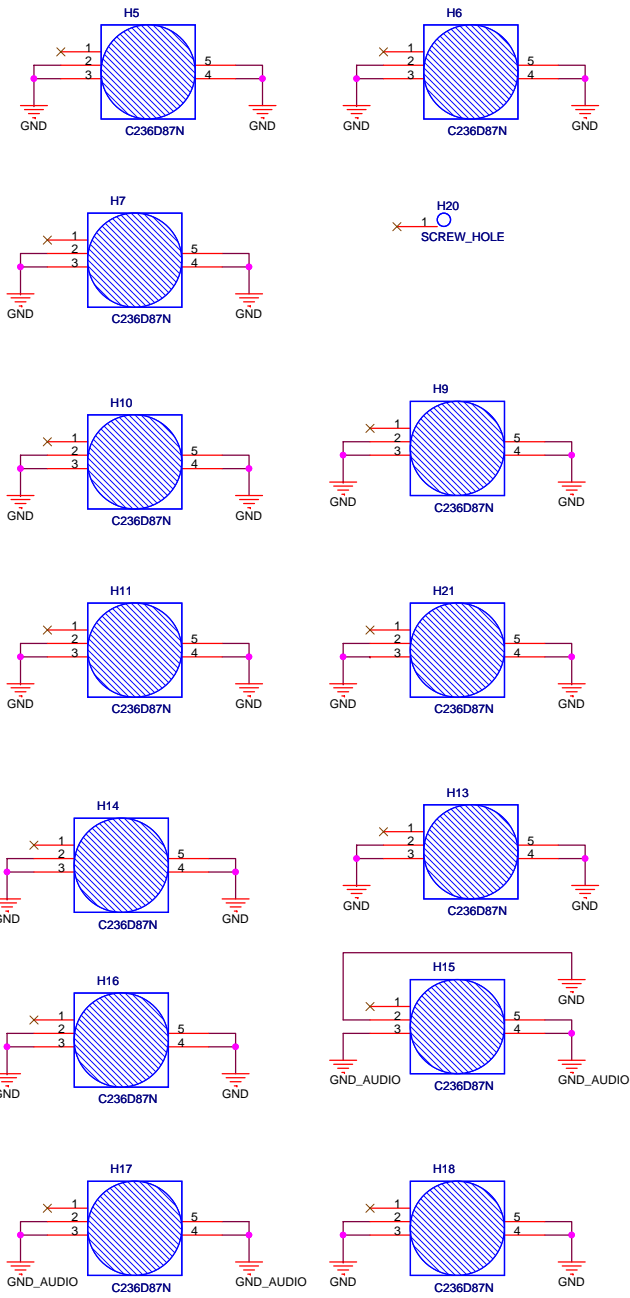


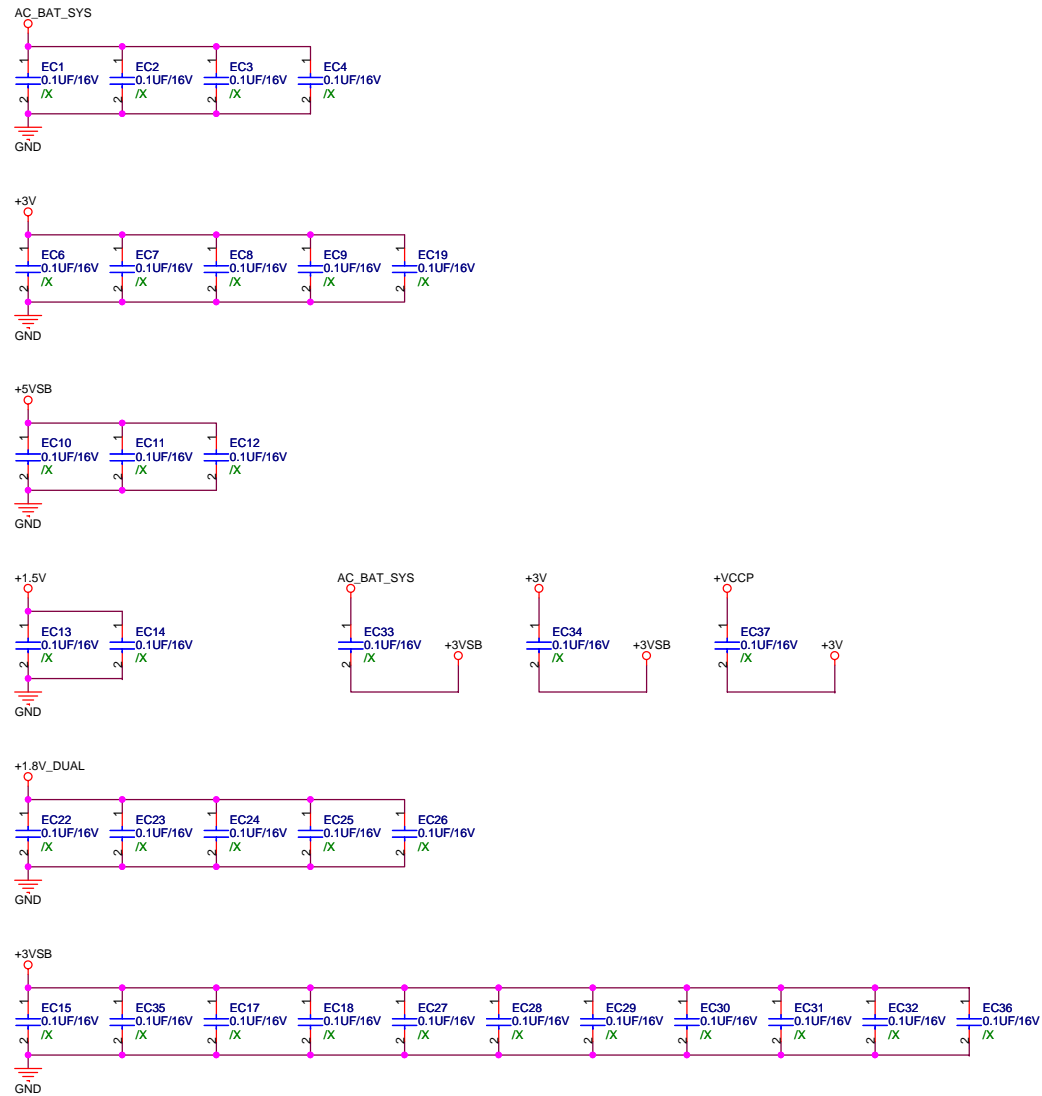
BAT IN



<Variant Name>

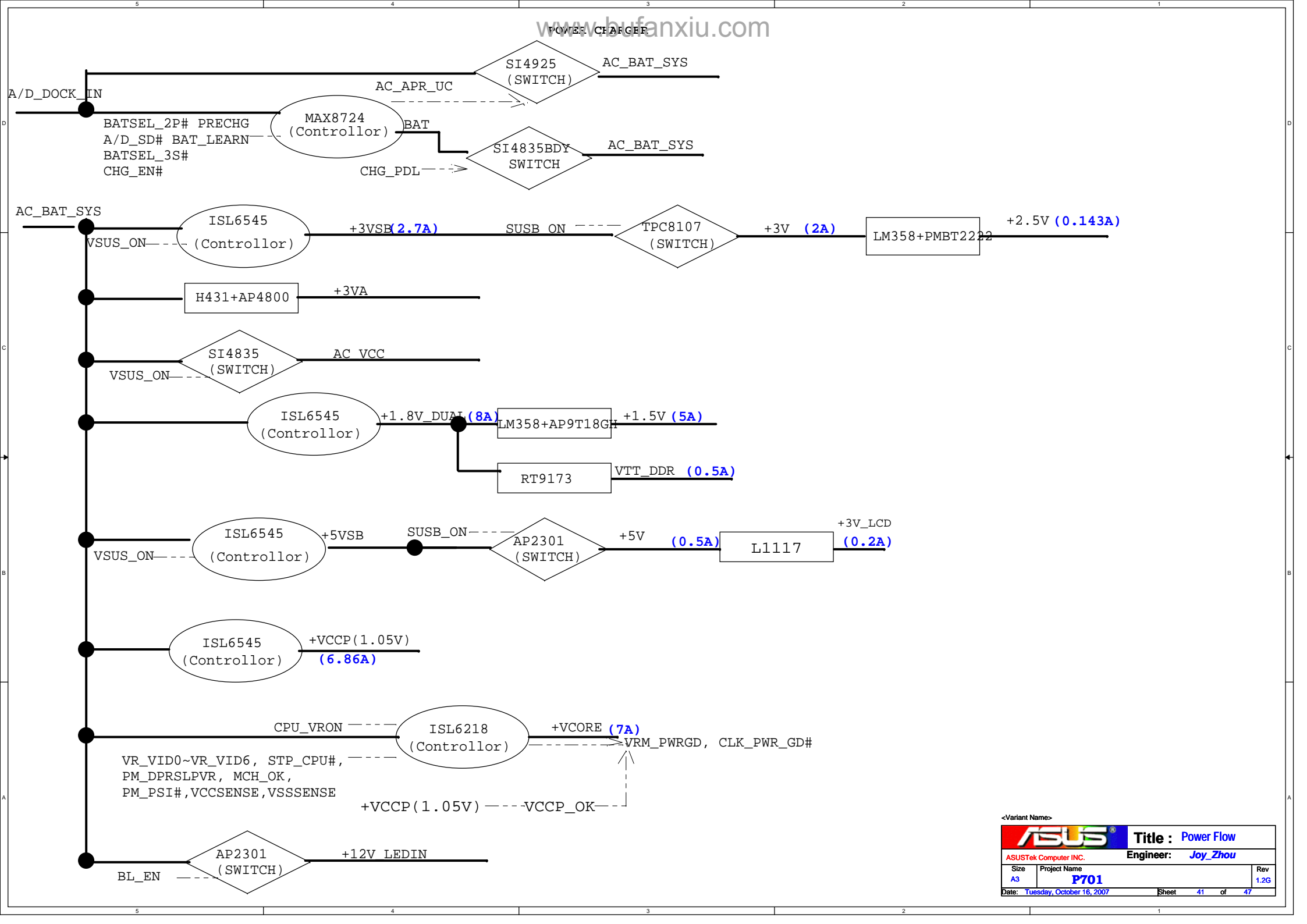
		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: <i>Keil_Huang</i>	
Size	Project Name		Rev
A3	P701		1.2G
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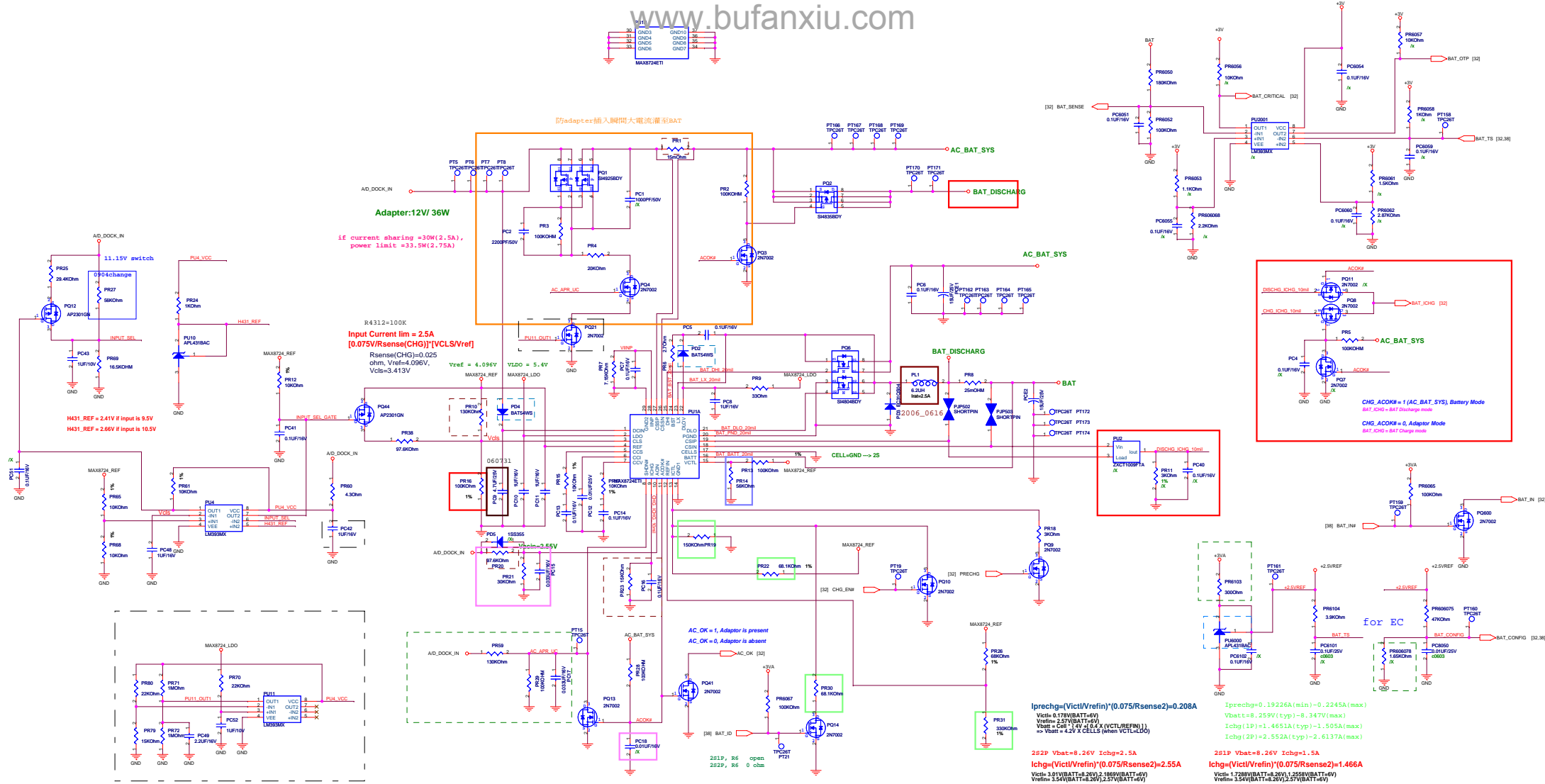




<Variant Name>

		Title : EMI	
ASUSTek Computer INC.		Engineer: Keil_Huang	
Size	Project Name		Rev
A3	P701		1.2G
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Adapter: 12V/ 36W
 if current sharing = 30W(2.5A),
 power limit = 33.5W(2.75A)

Input Current lim = 2.5A
 $[0.075V/Rsense(CHG)] \times [VCLSV/Vref]$
 $R_{sense(CHG)} = 0.025 \text{ ohm}, V_{ref} = 4.096V, V_{cls} = 3.413V$

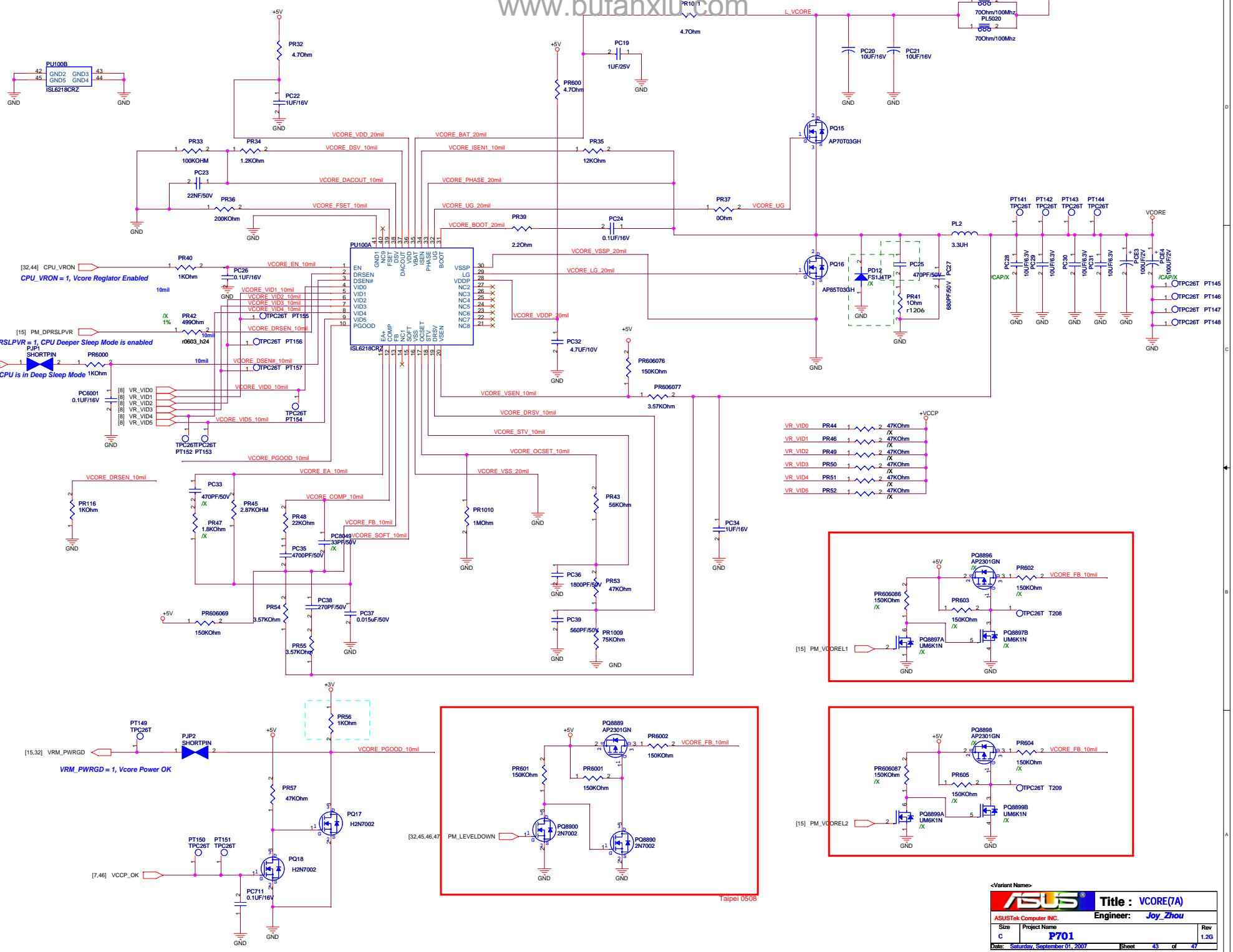
$I_{prechg} = (V_{ct1}/V_{refin}) \times (0.075/R_{sense2}) = 0.208A$

282P Vbat=8.26V Icbg=2.5A
 $I_{chg} = (V_{ct1}/V_{refin}) \times (0.075/R_{sense2}) = 2.55A$
 $V_{ct1} = 3.01V(BATT=2.5V), 2.189V(BATT=4V)$
 $V_{refin} = 3.54V(BATT=2.5V), 2.57V(BATT=4V)$
 $V_{bat} = Cell \times 4 \times [0.4 \times (V_{CTLR}/REFIN)] + 8.26$
 $\Rightarrow V_{ct1} = 1.149V(4.096 \times 39139)$
 $V_{bat} = 4.2V \times CELLS \text{ (when } V_{CTL} = LDO)$

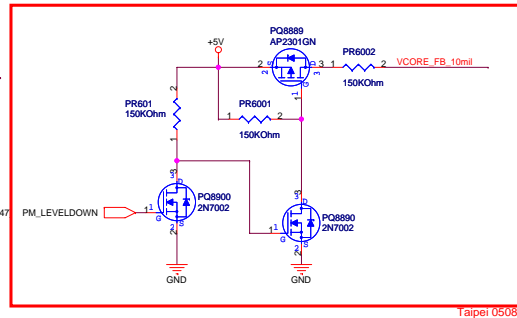
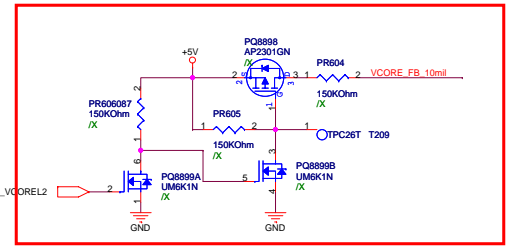
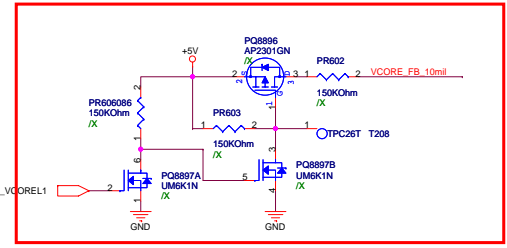
$I_{prechg} = 0.19226A \text{ (min)} - 0.2245A \text{ (max)}$
 $V_{bat} = 8.259V \text{ (typ)} - 8.347V \text{ (max)}$
 $I_{chg} (1P) = 1.4651A \text{ (typ)} - 1.505A \text{ (max)}$
 $I_{chg} (2P) = 2.552A \text{ (typ)} - 2.6137A \text{ (max)}$

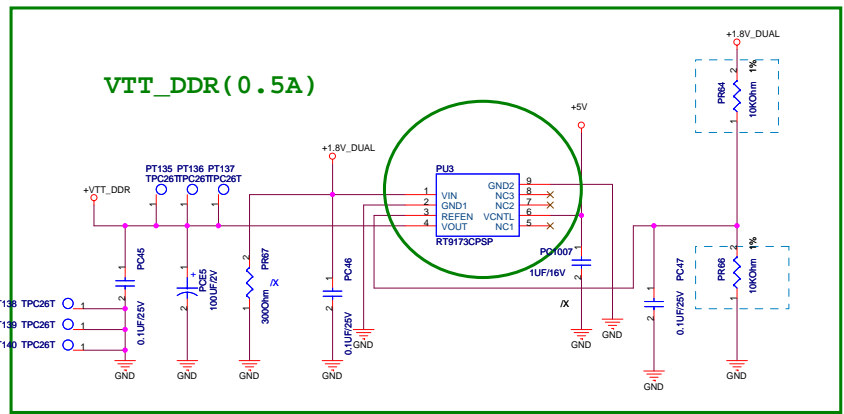
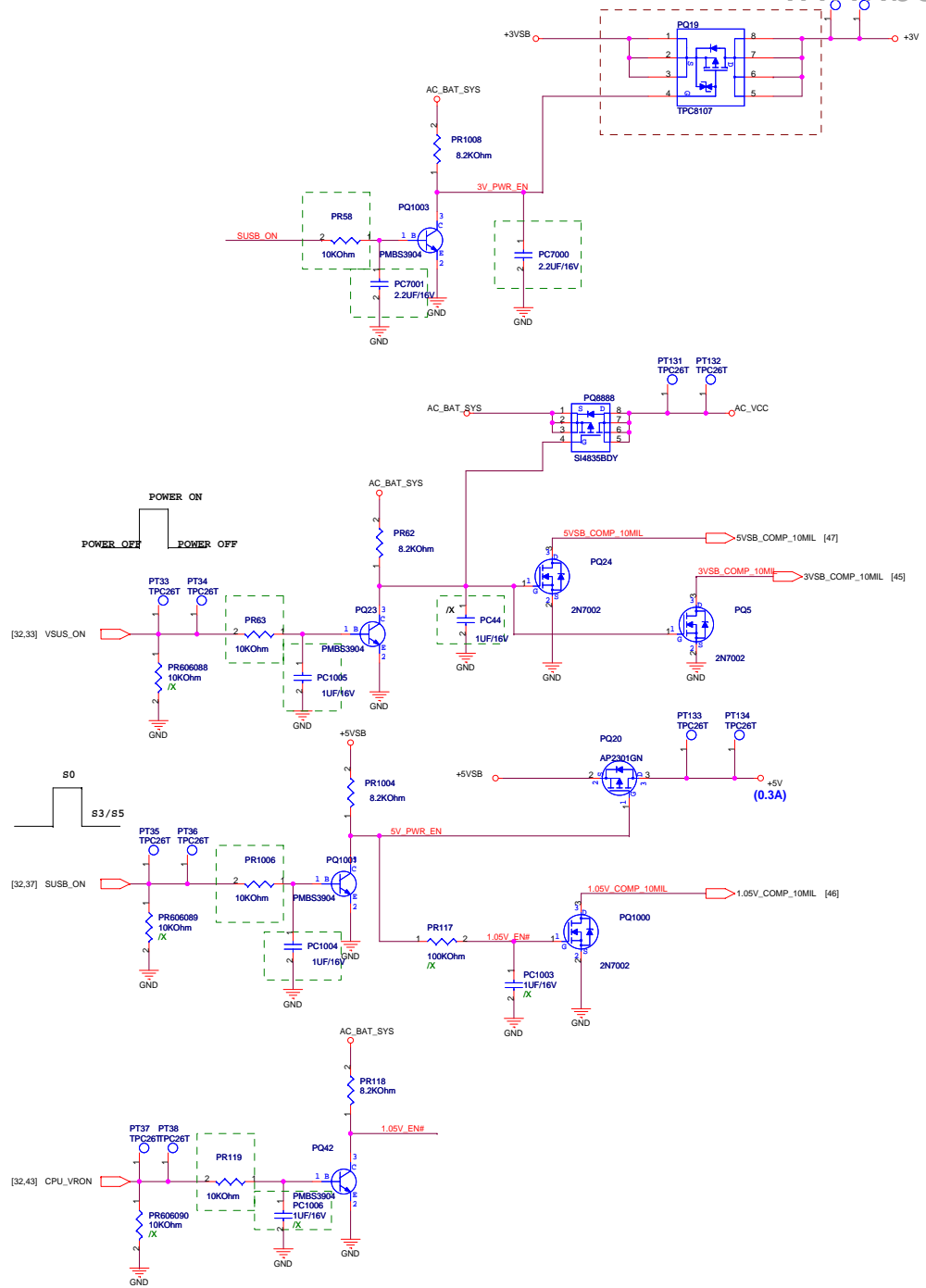
281P Vbat=8.26V Icbg=1.5A
 $I_{chg} = (V_{ct1}/V_{refin}) \times (0.075/R_{sense2}) = 1.466A$
 $V_{ct1} = 1.738V(BATT=2.5V), 1.258V(BATT=4V)$
 $V_{refin} = 3.54V(BATT=2.5V), 2.57V(BATT=4V)$
 $V_{bat} = Cell \times 4 \times [0.4 \times (V_{CTLR}/REFIN)] + 8.26$
 $\Rightarrow V_{ct1} = 1.149V(4.096 \times 39139)$
 $V_{bat} = 4.2V \times CELLS \text{ (when } V_{CTL} = LDO)$

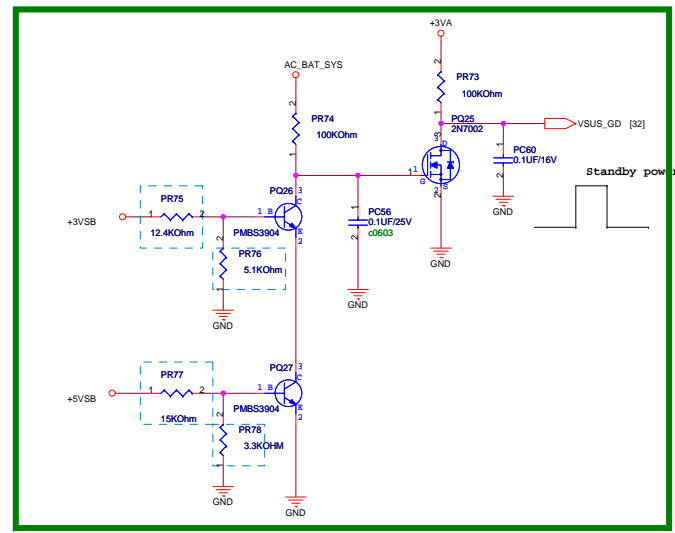
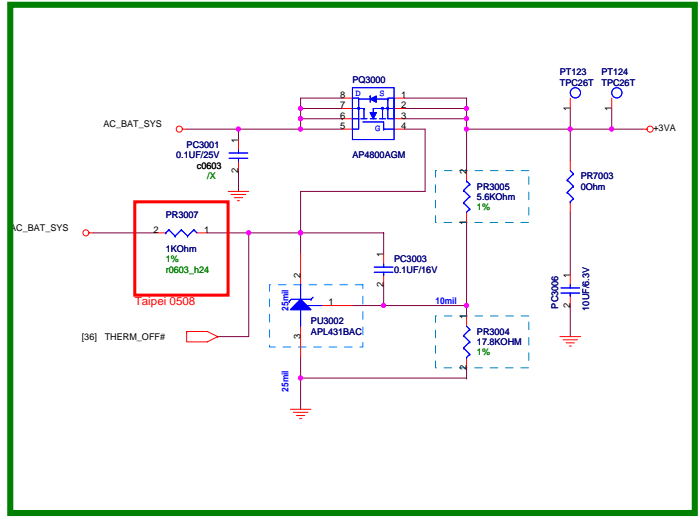
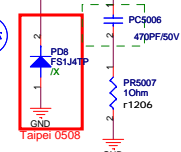
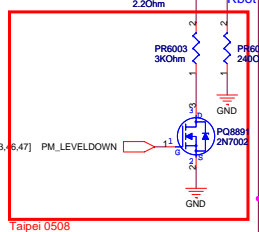
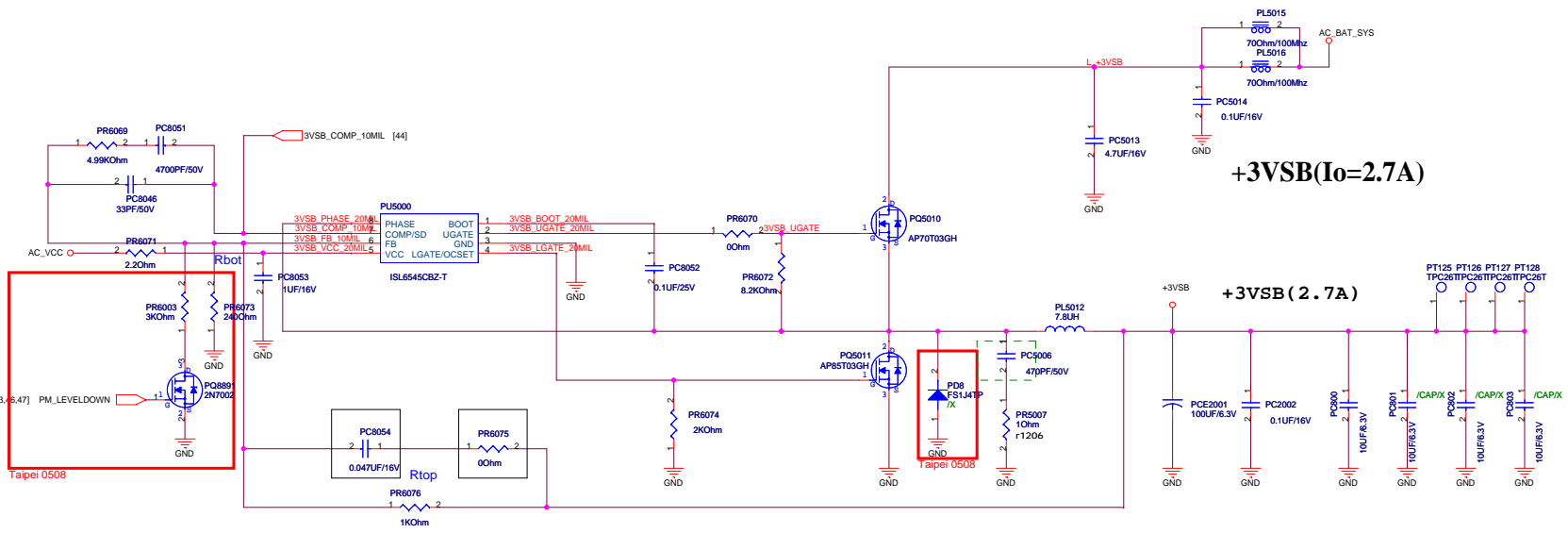
ASUS Title: CHARGER
 Project Name: Joy_Zhou
 Part: P701 Rev: 1.03
 Date: Friday, September 11, 2009 Sheet: 42 of 47

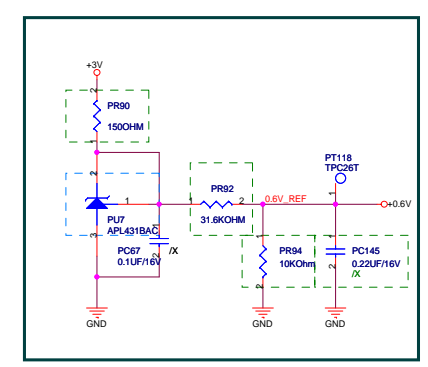
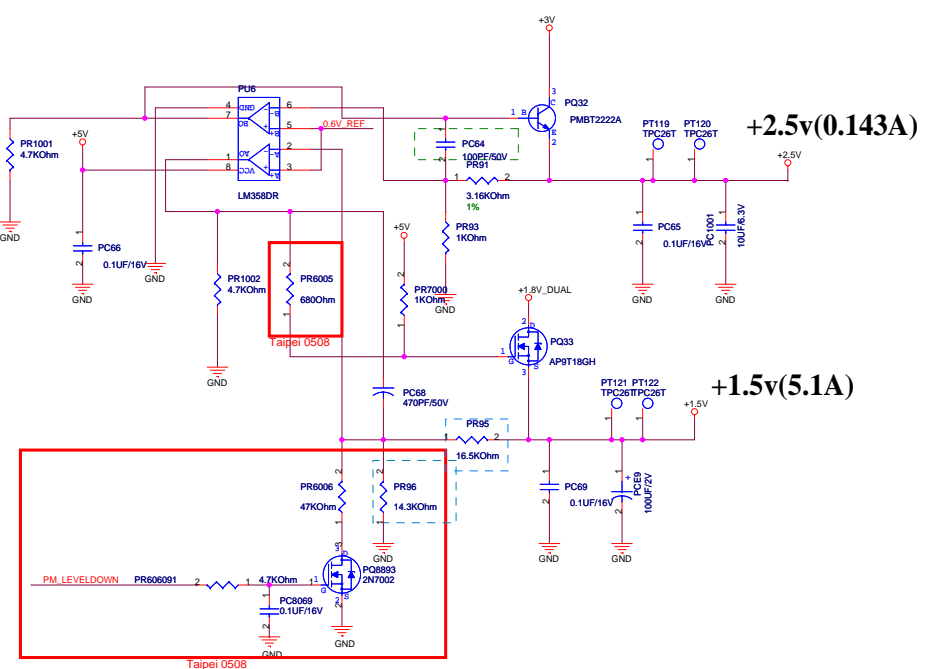
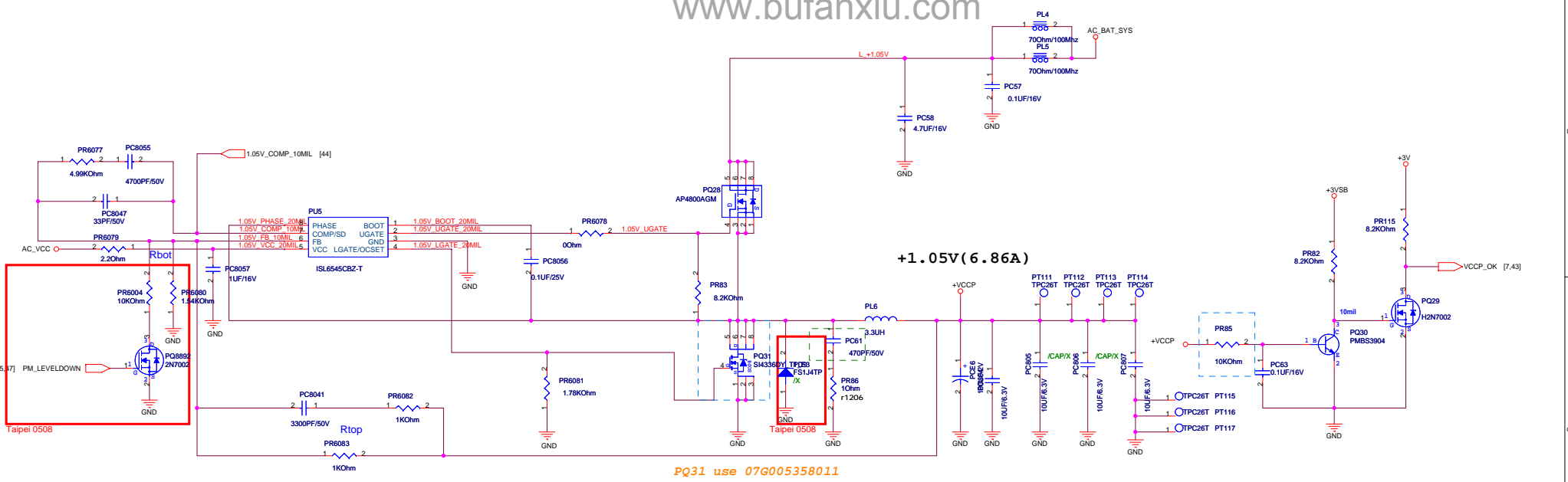


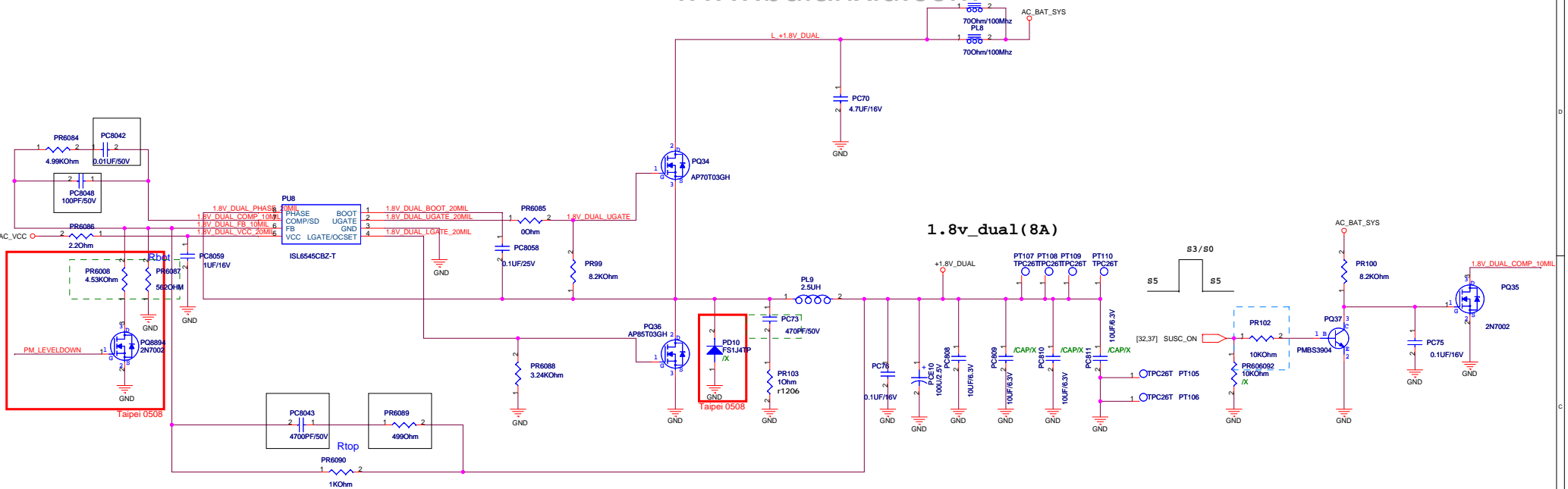
- VR_VID0 PR44 1 2 47KOhm /X
- VR_VID1 PR46 1 2 47KOhm /X
- VR_VID2 PR49 1 2 47KOhm /X
- VR_VID3 PR50 1 2 47KOhm /X
- VR_VID4 PR51 1 2 47KOhm /X
- VR_VID5 PR52 1 2 47KOhm /X



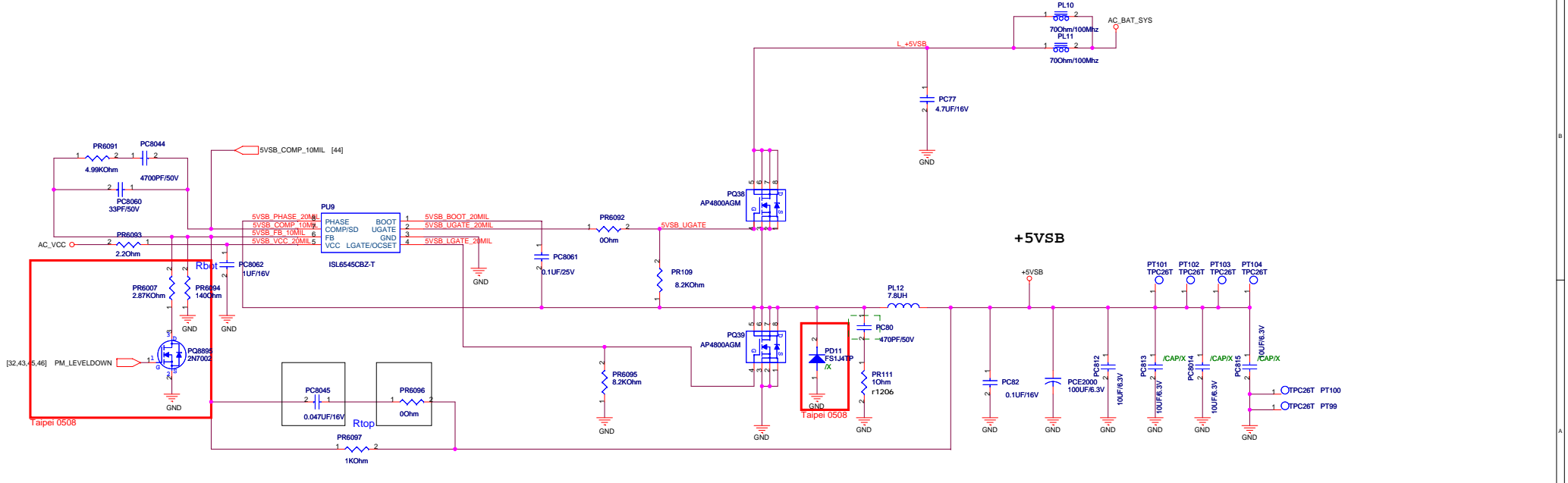








1.8v_dual (8A)



+5VSB