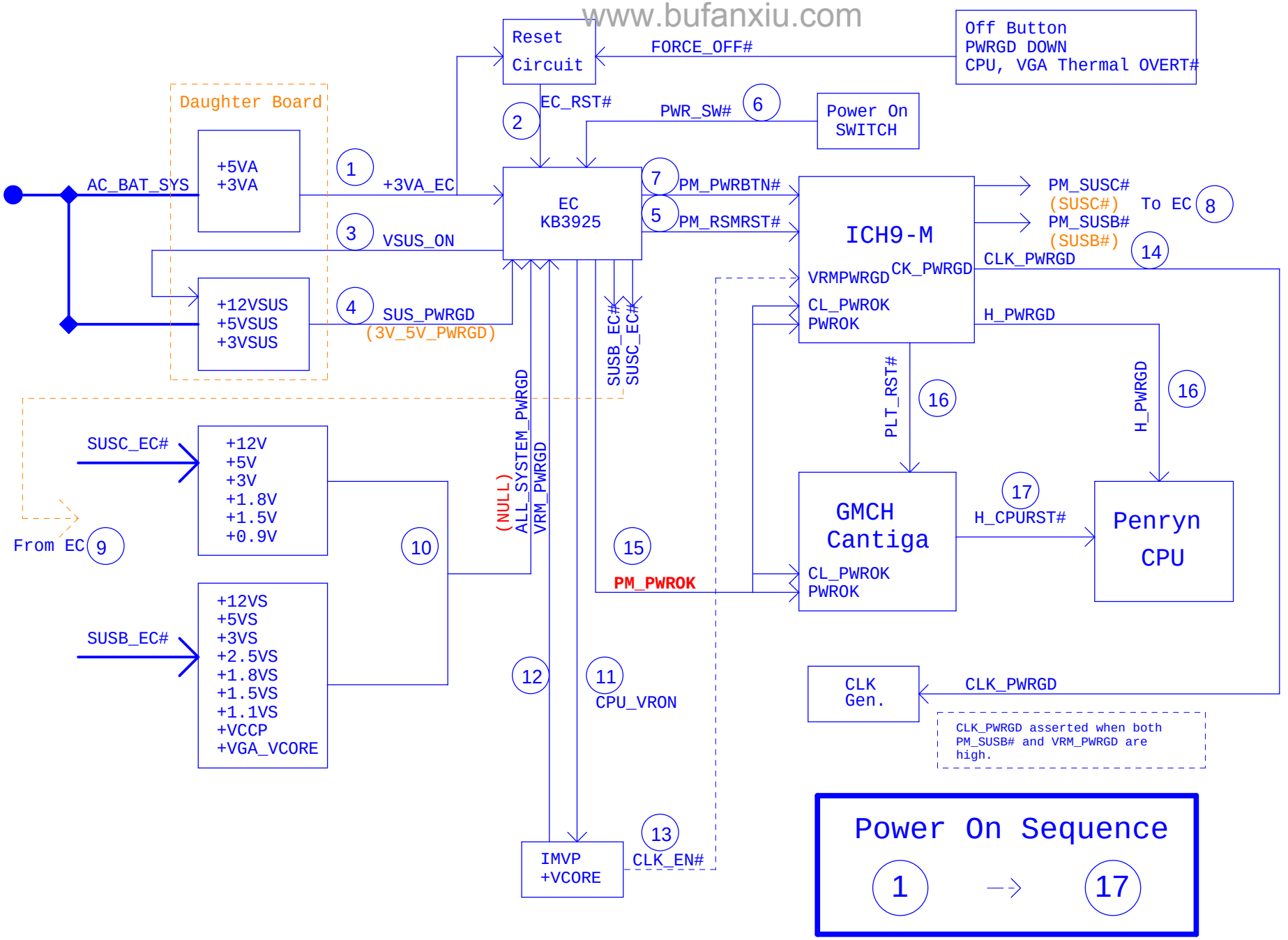
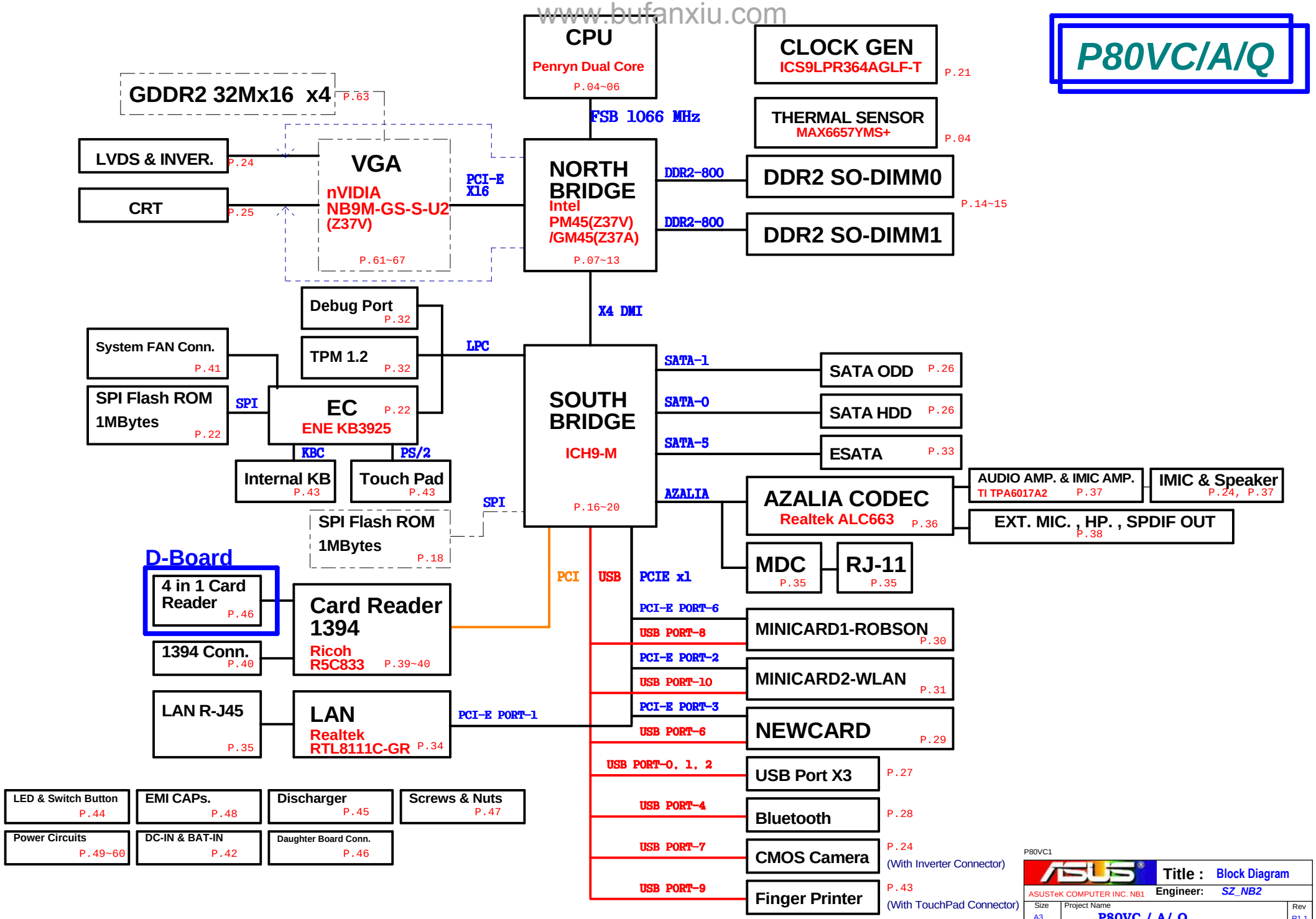


P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Power-On Sequence	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 1 of 52	

P80VC/A/Q



P80VC1

ASUSTeK COMPUTER INC. NB1

Title : Block Diagram

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 2 of 52

Z37V/A Schematic Index

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02	Schematic Information
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07-09	DDR II SO-DIMM
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29	CLK-ICS9LPR363CGLF-T
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32	POWER-ON SEQUENCE
33	Realtek RTL8111C
34	RJ45 + RJ11
35	MDC
36	ALC663 Codec
37	AUDIO_G1431 & HP
38	MICROPHONE & Array MIC
~~39~~	~~FM2010 DSP~~
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & 4 IN1 CON
43	NewCard PWR SW & CON
44	Debug
45	LVDS & INVERTER CONNECTOR
46	CRT
48	HDMI
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port x 4
53	MINICARD(Ebron/Robson/3G/TV)
~~54~~	~~PORT Docking~~
~~55~~	~~Super I/O & FIR~~
56	LED/TP/SW
57	DISCHARGE
58	UMB
60	DC power jack, Batter conn.
61	Blue Tooth
62	TPM
63	Finger Print
65	MDC NUT & Hinksink NUT
66	E-SATA
68	XDP
70-77	VGA (nVidia NB9P-GE)
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.5V & 1.05VM
83	POWER_I/O_DDR & VTT
84	NONE
85	POWER_VGA_VCORE & 1.1VO
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

GPIO33 Internal Pull High, Go Low= Flash ROM Descriptor Security will be overriden

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	Native	PMSYNC#	+3VS
GPIO 01	GPI	- EXT PU to +3VS	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+5VS
GPIO 06	GPI	WLBT_SW# EXT PU	+3VS
GPIO 07	GPI	-	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN EXT PD	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	SMBALERT# EXT PU	+3VSUS
GPIO 12	GPI	EXT_SCI# EXT PU	+3VSUS
GPIO 13	GPI	-	+3VSUS
GPIO 14	Native	AC_PRESENT EXT PU	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	-	+3VS
GPIO 18	GPO	GPU_PWR_SB EXT PU NS	+3VS
GPIO 19	GPO	BT_LED EXT PU NS	+3VS
GPIO 20	GPO	GPU_RST_SB# EXT PU NS	+3VS
GPIO 21	GPO	WLAN_LED EXT PU NS	+3VS
GPIO 22	GPI	ODC# EXT PU	+3VS
GPIO 23	Native	LPC_LDRQ1# INT PU*	+3VS
GPIO 24	GPO	-	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	-	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5# EXT PU	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7# EXT PU	+3VSUS
GPIO 32	GPO	PM_CLKRUN# EXT PU	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPO	WLAN_ON EXT PU NS	+3VS
GPIO 37	GPO	BT_ON EXT PU NS	+3VS
GPIO 38	GPI	-	+3VS
GPIO 39	GPO	CLK_PWRSAVE# EXT PU	+3VS
GPIO 40	Native	USB_CON_OC01#	+3VSUS
GPIO 41	Native	USB_CON_OC2#	+3VSUS
GPIO 42	Native	USB_OC3# EXT PU	+3VSUS
GPIO 43	Native	USB_OC4# EXT PU	+3VSUS
GPIO 44	Native	USB_OC8# EXT PU	+3VSUS
GPIO 45	Native	USB_OC9# EXT PU	+3VSUS
GPIO 46	Native	USB_OC10# EXT PU	+3VSUS
GPIO 47	Native	USB_OC11# EXT PU	+3VSUS
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	- INT PU* EXT PU to +3VS	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU* EXT PU to +3VS	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU* EXT PU to +3VS	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_CON_OC01#	+3VSUS
GPIO 60	Native	PM_LINKALERT# EXT PU	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPIO02	GPO	PM_RSMRST#	
GPIO03	GPO	LCD_BACKOFF#	
GPIO04	GPI	EMAIL_SW#	
GPIO06	-	-	
GPIO07	-	-	
GPIO08	GPO	EXT_SMI#	
GPIO09	-	-	
GPIO0A	GPI	LID_EC#	
GPIO0B			
GPIO0C			
GPIO0D	GPI	DISTP_SW#	
GPIO11	GPO		
GPIO18			
GPIO19			

EC GPIO	Use As	Signal Name	Power

INT PU*: PU or PD in special time

P80VC1

Title : System Information

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size: Custom | Project Name: P80VC / A/ Q | Rev: R1.1

Date: Tuesday, December 16, 2008 | Sheet 3 of 52

R1.1 KL99 FOR P80Q
R1.1 KL1 FOR P80VC/A

+3V KL99 120Ohm/100Mhz /woAMT
+3VM /AMT KL1 120Ohm/100Mhz
+3VS_CLK KL3 120Ohm/100Mhz
KC7 Do Not Stuff /X
KC8 10UF/6.3V
KC9 0.1UF/10V
KC10 0.1UF/10V
KC11 0.1UF/10V
KC12 0.1UF/10V
KC30 0.1UF/10V
KC31 0.1UF/10V
KC2 0.1UF/10V
+3VS_CLKA
GND

+1.5VS KL2 120Ohm/100Mhz
+1.5VS_CLK
KC1 Do Not Stuff /X
KC3 10UF/6.3V
KC4 0.1UF/10V
KC6 0.1UF/10V
R1.1
KR1 Do Not Stuff
KX1 14.318Mhz +/-30ppm/20PF
XIN_CLK XOUT_CLK
KC13 30PF/50V
KC14 30PF/50V
H = 1.2mm
GND

Tuning Cap. @ device sides

KC24 Do Not Stuff /X — CLK_27M_GPU
KC25 Do Not Stuff /X — CLK_27M_GPU_SS
KC18 Do Not Stuff /X — CLK_48M_SB
KC22 Do Not Stuff /X — CLK_33M_TPM
KC23 Do Not Stuff /X — CLK_33M_EC
KC19 Do Not Stuff /X — CLK_33M_SB
KC20 Do Not Stuff /X — CLK_33M_DBG2
KC17 Do Not Stuff /X — CLK_14M_ICH
GND

Close the end of devices

Close to CLK GEN

SMB_CLK_M
SMB_DAT_M
KC15 Do Not Stuff /X
KC16 Do Not Stuff /X
GND

+3VS_CLKA
+1.5VS_CLK
+3VS_CLK

KU1

VDDSRC_1
VDDSRC_IO1
VDDSRC_IO2
VDDPCI_1
VDDPCI_2
VDD48
VDDREF
**FUC
VDDCPU
VDDA
GNDA
X1
X2
27MHZ/LCD_SSCG/SRC-0
27MHZS/LCD_SSCG#/SRC-0#
**FSLA/USB_48MHz
**FSLB/TEST_MODE
*SELSRC0_LCD#/PCI-3
PCI-2
PCI-1
**PCI-0/REQ_SEL
*SELLCD_27#/PCIF-1
**ITP_EN/PCIF-0
SCLK
SDATA
**FOC
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
RTM875T-336-GRT

To ICH9 GPIO45
To ICH9 GPIO44

XIN_CLK
XOUT_CLK
FUC
FOC
FSLB
LCDCK_SEL
SMB_CLK_M
SMB_DAT_M

R1.1
CLK_100M_LVDS 33Ohm 2 KRN8A /GM
CLK_27M_GPU 33Ohm 2 KRN11A /PM
CLK_27M_FIX
CLK_100M_LVDS# 33Ohm 4 KRN8B /GM
CLK_27M_GPU_SS 33Ohm 4 KRN11B /PM
CLK_27M_SS
CLK_48M_CR KR29 33Ohm
CLK_48M_SB KR17 33Ohm
CLK_48M
FSLA

CLK_48M_SB,CLK_48M_CR layout 時 trace 長度相等

CLK_33M_TPM KR32 33Ohm CLK_33M2
CLK_33M_DBG2 KR26 33Ohm REQ_SEL#
SEL_27M#
CLK_33M_SB KR27 33Ohm CLK_33M_F1
EN_ITPCLK
CLK_33M_EC KR28 33Ohm CLK_33M_F0

SMB_CLK_M
SMB_DAT_M

*INT-PU 120K ohm
**INT-PD 120K ohm.

**PCI_SRC_STOP# — STP_PCI#
**CPU_STOP# — STP_CPU#
CPU-1 CPUCLK1 33OHM 2 KRN1A — CLK_MCH_BCLK
CPU-1# CPUCLK1# 33OHM 4 KRN1B — CLK_MCH_BCLK#
CPU-0 CPUCLK0 33OHM 2 KRN14A — CLK_CPU_BCLK
CPU-0# CPUCLK0# 33OHM 4 KRN14B — CLK_CPU_BCLK#
CPUITP/SRC-8 CPUCLK2 33OHM 2 KRN3A — CLK_XDP_BCLK
CPUITP#/SRC-8# CPUCLK2# 33OHM 4 KRN3B /ITP — CLK_XDP_BCLK#
*SRC_REQ1#/SRC-7 — LAN_CLKREQ#
*SRC_REQ2#/SRC-7# — MCH_CLKREQ#
SRC-6 CLK_PCIE6 33OHM 2 KRN2A — CLK_PCIE_LAN
SRC-6# CLK_PCIE6# 33OHM 4 KRN2B — CLK_PCIE_LAN#
SRC-5 CLK_PCIE5 33OHM 2 KRN6A — CLK_100M_NEW
SRC-5# CLK_PCIE5# 33OHM 4 KRN6B — CLK_100M_NEW#
SRC-4 CLK_PCIE4 33OHM 4 KRN13B — CLK_100M_MIN1
SRC-4# CLK_PCIE4# 33OHM 2 KRN13A — CLK_100M_MIN1#
SRC-3 CLK_PCIE3 33OHM 4 KRN9B — CLK_PCIE_GPU
SRC-3# CLK_PCIE3# 33OHM 2 KRN9A /PM — CLK_PCIE_GPU#
SRC-2 CLK_PCIE2 33OHM 4 KRN15B — CLK_PCIE_ICH
SRC-2# CLK_PCIE2# 33OHM 2 KRN15A — CLK_PCIE_ICH#
SRC-1 CLK_PCIE1 33OHM 4 KRN7B — CLK_PCIE_NB
SRC-1# CLK_PCIE1# 33OHM 2 KRN7A — CLK_PCIE_NB#
SATA CLK_SATA 33OHM 4 KRN16B — CLK_SATA_SB
SATA# CLK_SATA# 33OHM 2 KRN16A — CLK_SATA_SB#
SRC-9/DOT96 CLK_96M 33OHM 4 KRN10B — CLK_96M_NB
SRC-9#/DOT96# CLK_96M# 33OHM 2 KRN10A /GM — CLK_96M_NB#

R1.1 Remove 0ohm

R1.1
*SRC_REQ3# — WLAN_CLKREQ#
*SRC_REQ4# — NEW_CLKREQ#
**VtPWR_GD/PD# CLK_PWRGD KR35 0Ohm KR36 Do Not Stuff /X — SB_CLKPWRGD / EC_CLKPWRGD
**REF-1/FSLC/TEST_SEL FSLC REF-0 KR24 33Ohm — CLK_14M_ICH

PEREQ1# for SATA,SRC-0, SRC-6(LAN:PCIE6)
PEREQ2# for SRC-1, SRC-8(NC)
PEREQ3# for SRC-2,SRC-4(WLAN PCIE4)
PEREQ4# for SRC-3,SRC-5, SRC-7(NEWCARD PCIE5)

FSB Freq. Strap

FSC	FSB	FSA	CPU
0	0	0	266
0	0	1	133
0	1	0	200
0	1	1	166
1	0	0	333
1	0	1	100
1	1	0	400
1	1	1	200

FSLA KR5 10KOhm CPU_BSEL0
FSLB KR6 10KOhm CPU_BSEL1
FSLC KR7 10KOhm CPU_BSEL2

LCDCK_SEL	SEL_27M#				
PIN 5 (IPU)	PIN 9 (IPU)	PIN14, 15	PIN17	PIN18	
0	0	SRC-9	27FIX	27SS	
0	1	DOT96	DOT96SS	DOT96SS	
1	0	DOT96	27FIX	27SS	/PM
1	1	DOT96	SRC-0	SRC-0	/GM

R1.1 +3VS_CLK KR33 10KOhm /GM
SEL_27M# KR8 10KOhm /PM GND
R1.1 +3VS_CLK KR34 10KOhm
LCDCK_SEL KR9 Do Not Stuff GND

PIN 8 ITP_EN/PCIF-0
Select PIN43, 44 as CPUITP or SRC8

R1.1 +3VS_CLK KR20 10KOhm
EN_ITPCLK KR10 Do Not Stuff GND

0 :SRC8
1 :CPUITP

PIN 64 (IPD)PCI-0/REQ_SEL
Select PIN40, 41 as SRC_REQ# or SRC7

R1.1 +3VS_CLK KR15 10KOhm
REQ_SEL#

0 :SRC-7
1 :SRC_REQ#

P80VC1

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2
Title : Main Clock-1
Size A2 | Project Name P80VC / A/ Q | Rev R1.1
Date: Tuesday, December 16, 2008 | Sheet 4 of 52

CPU1A

SOCKET478B

12G010594786

CPU1B

SOCKET478B

12G010594786

AC mode : check PWRLIMT#
DC mode : check battery OTP / OCP

R1.1
Remove THRO_CPU from EC

Zo=55 Ohm, 0.5" max for GTL_REF

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1 degree

CPU Thermal Sensor

HU1
MAX6657YMS+

Place close to CPU Pin
Max: 1mA

ITP

BTOB_CON_31P
/ITP

12G161300310

Stuff when use ITP : HR12, HR13, HR14, HR17, HR18, HR19, HR20, HR21, HR22, HR23, HR24, KRN3

HR12, HR13, HR30, HR31 Place close to CPU

Route H_THERMDA and H_THERMDC in the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

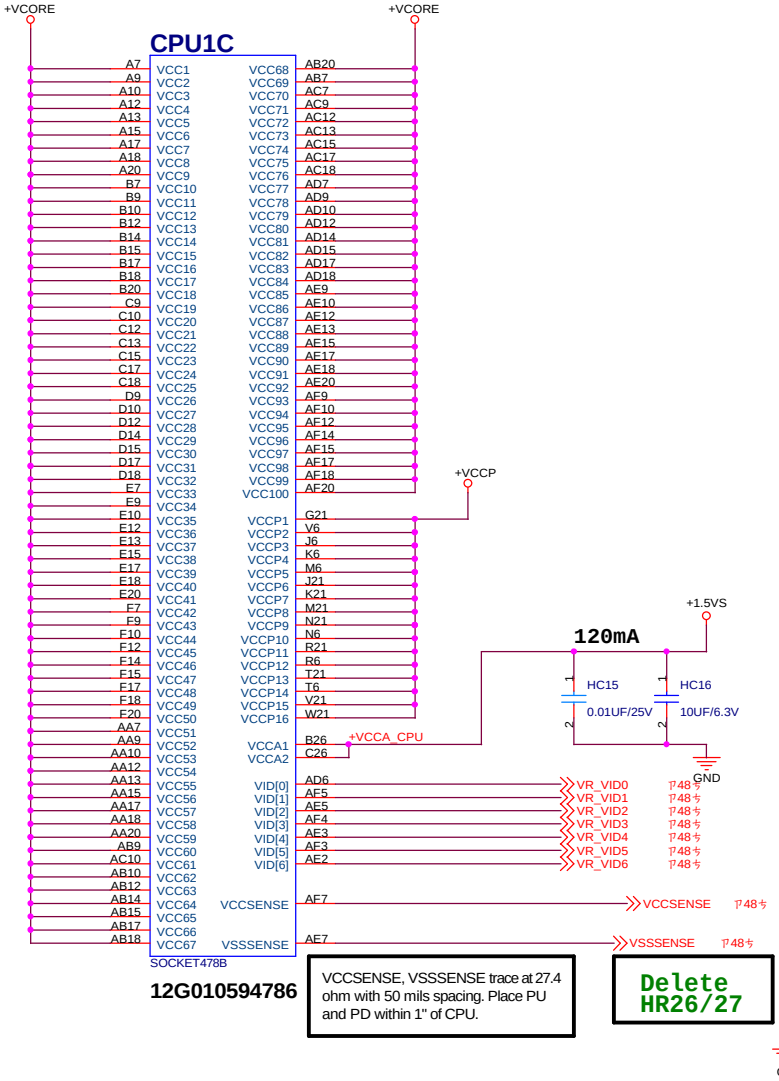
P80VC1

Title : CPU-Penryn (1)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

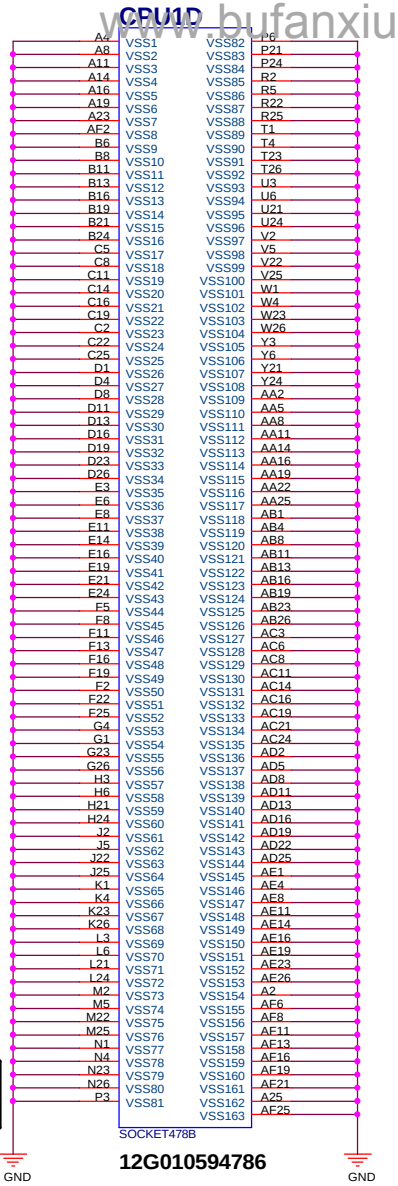
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

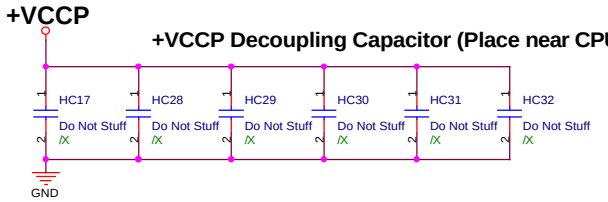
Date: Tuesday, December 16, 2008 Sheet 5 of 52

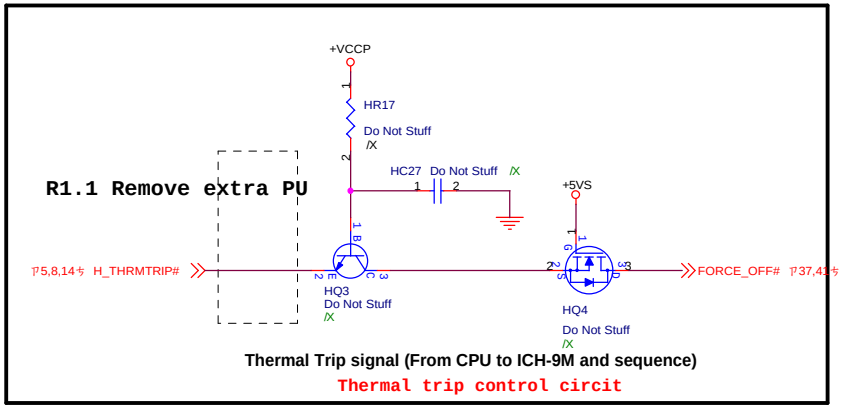


VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

Delete HR26/27

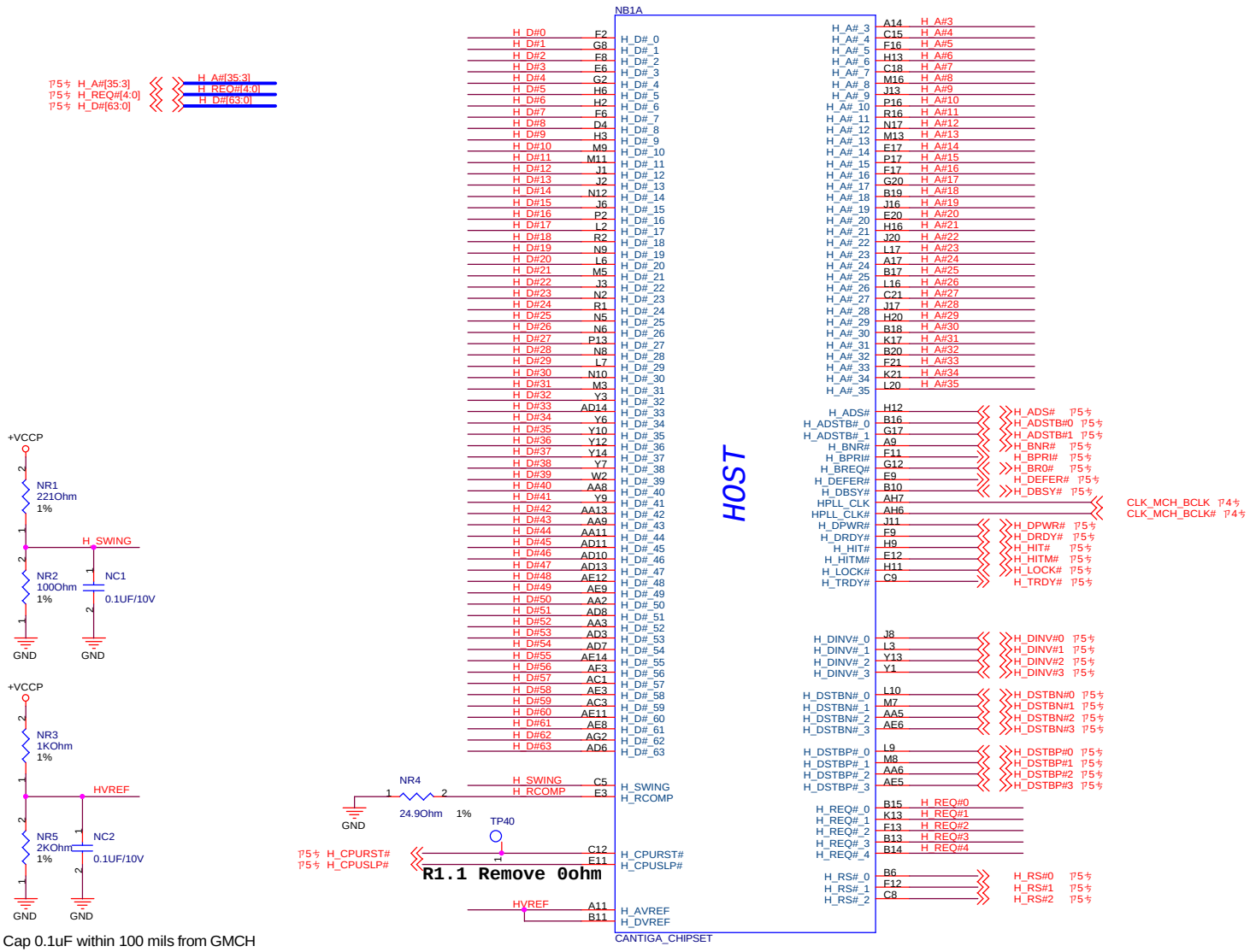






P80VC1

ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn (2)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 6 of 52	



Cap 0.1uF within 100 mils from GMCH

BOM:
GM45:02G010020030
PM45:02G010022520
GL40:02G010023900
or 02G010017532

P80VC1

Title : Cantiga - CPU(1)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 7 of 52

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2
CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable
CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality
CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes
CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable
CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)
CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable
CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes
CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

3.01K OHM -> 3K OHM

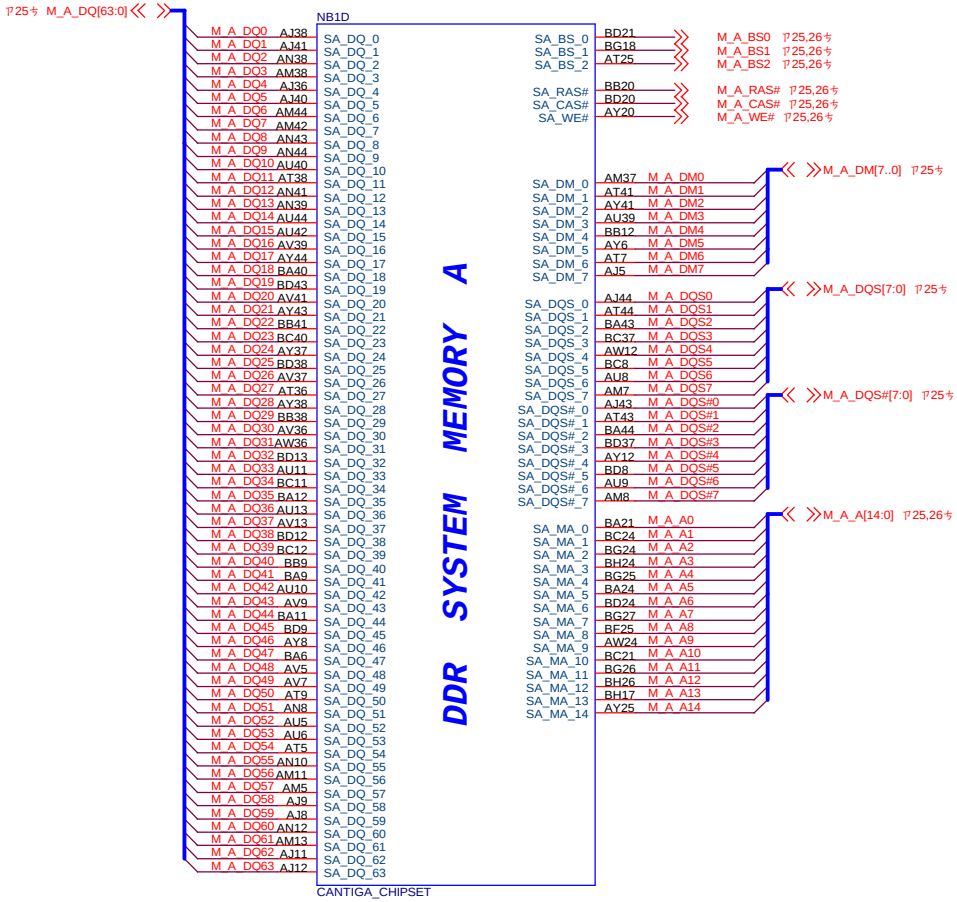
R1.1

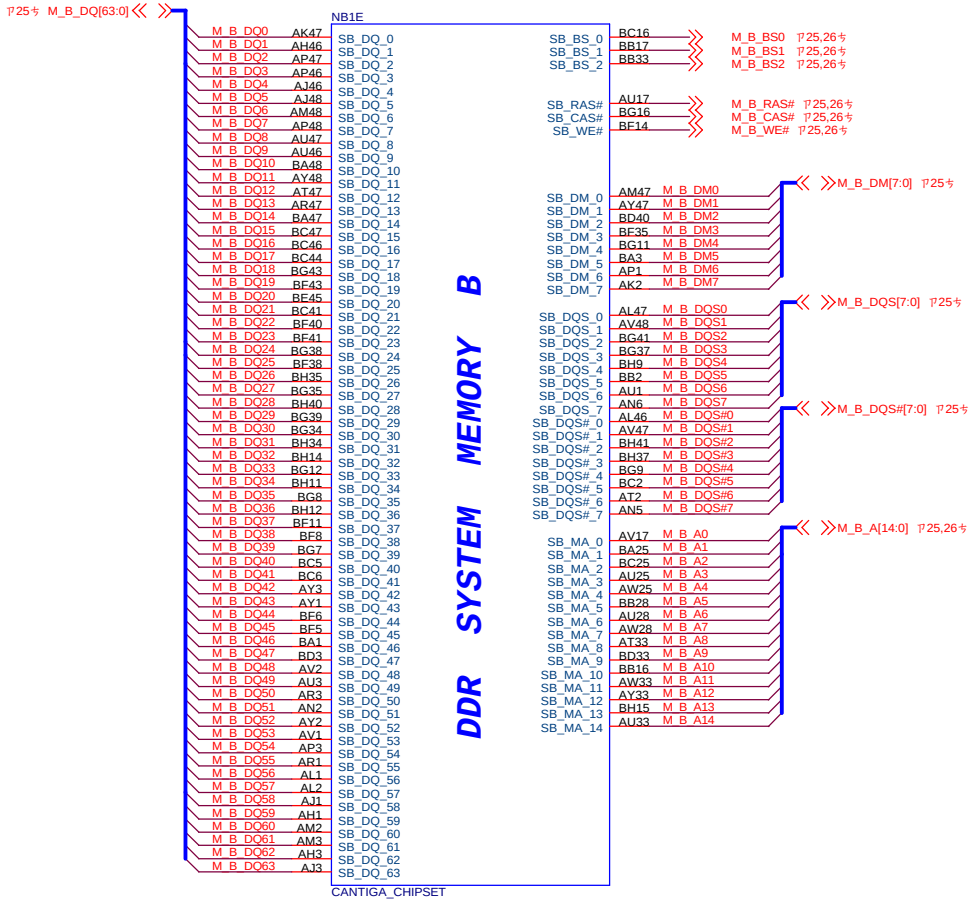
R1.1

2.2UF -> 1UF

P80VC1

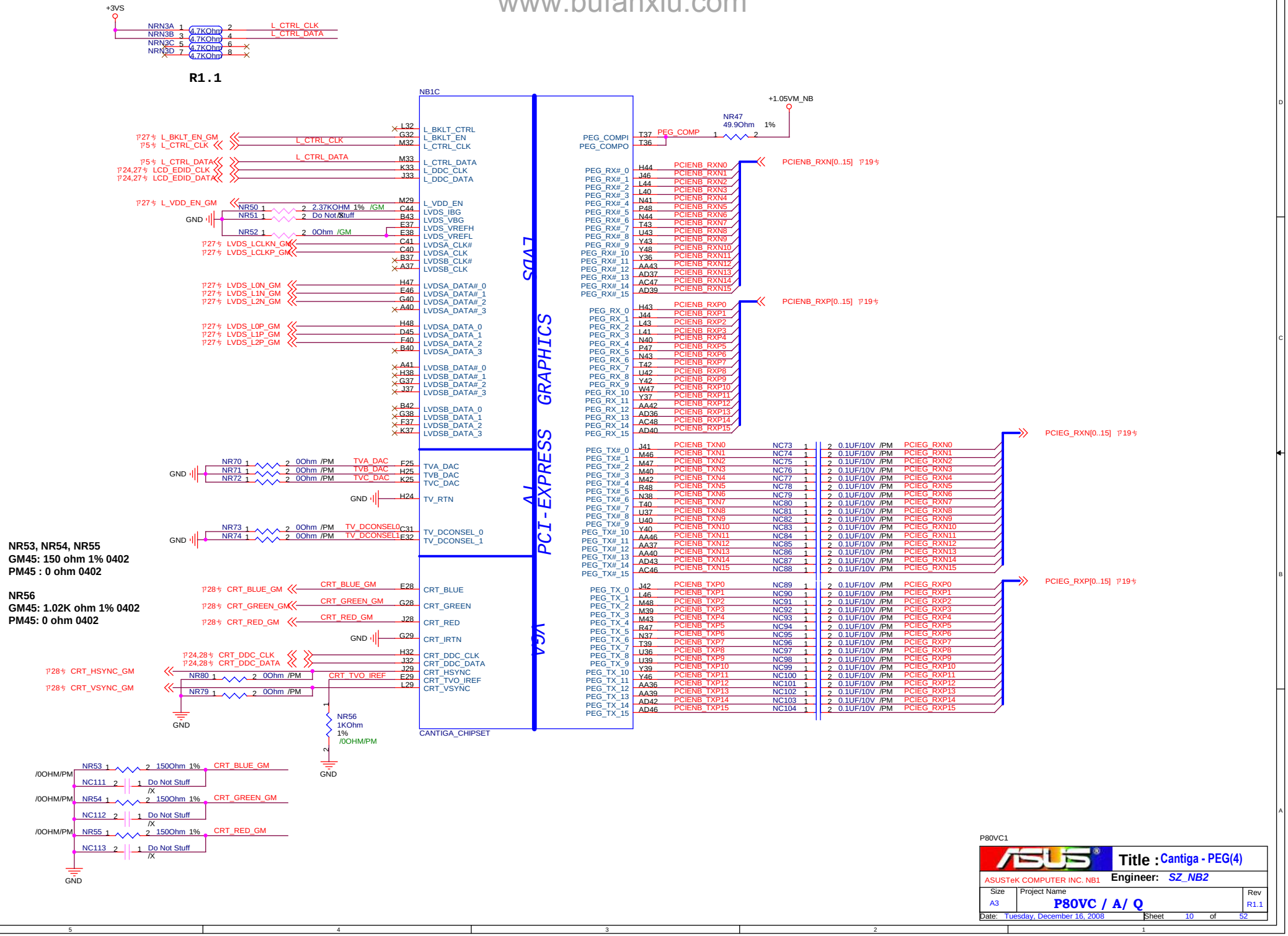
ASUSTeK COMPUTER INC. NB1	Title : Cantiga - DDR2/DMI(2)	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 8 of 52	





P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - DDR2(3)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 9 of 52	



NR53, NR54, NR55
GM45: 150 ohm 1% 0402
PM45 : 0 ohm 0402

NR56
GM45: 1.02K ohm 1% 0402
PM45: 0 ohm 0402

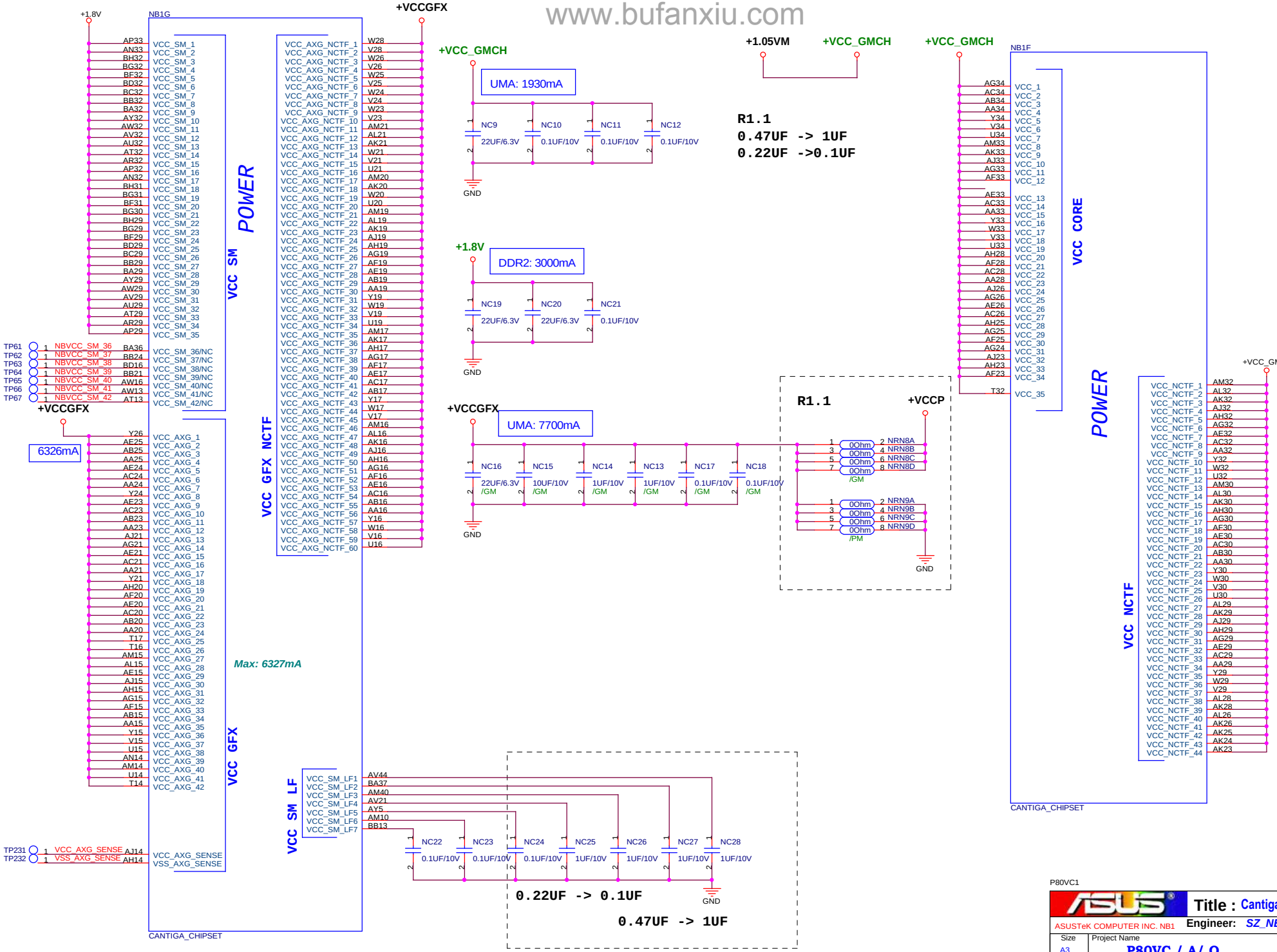
P80VC1

Title : Cantiga - PEG(4)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

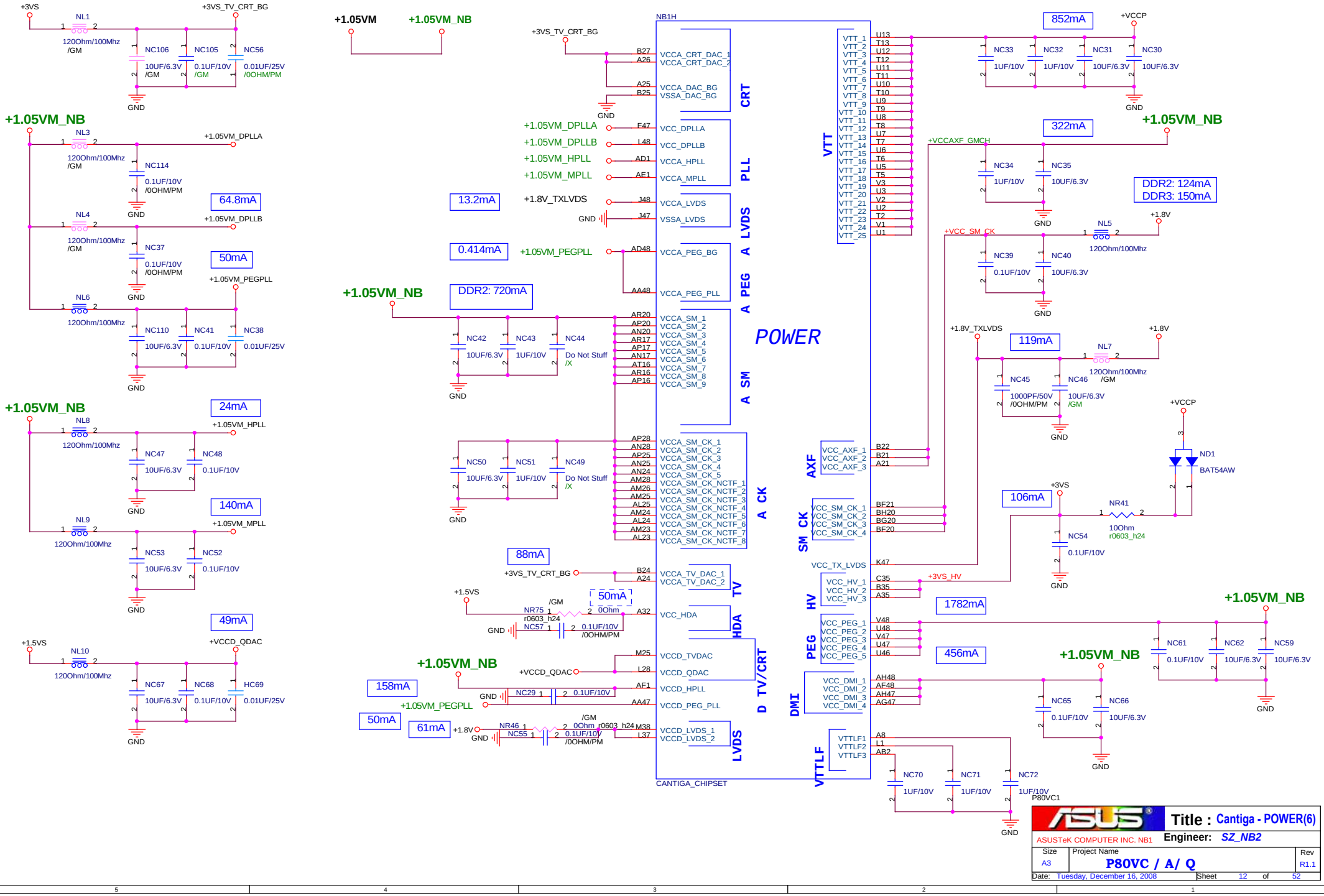
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

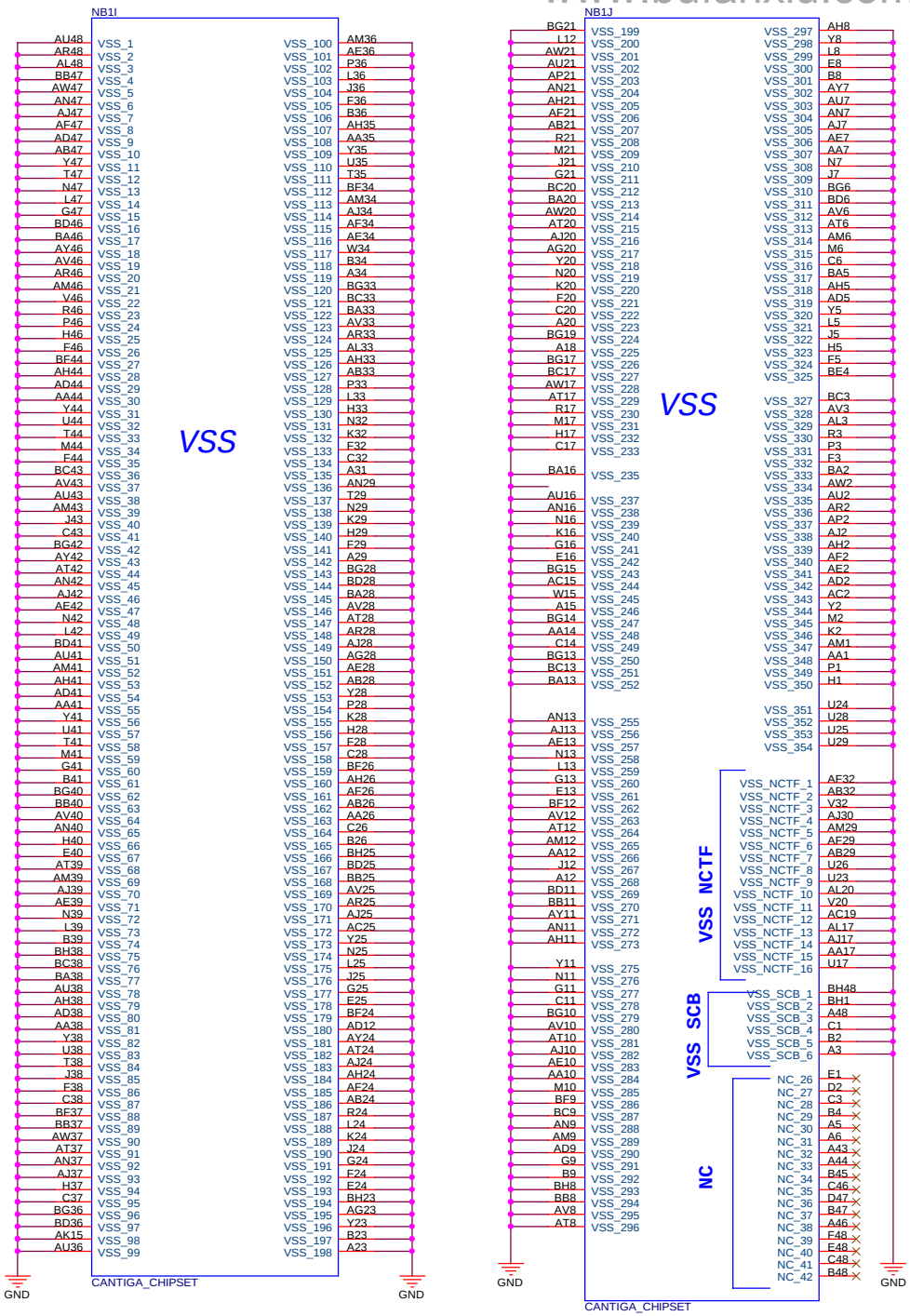
Date: Tuesday, December 16, 2008 Sheet 10 of 52



P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - POWER(5)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 11 of 52	





Change NC-26/42 to NC from GND

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - GND(7)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 13 of 52	

Place Near the Open Door

RTCRST#
SC1
1UF/10V
JRST1
Do Not Stuff
r0603_h24
/X
GND
GND

R1.1
+VCC_RTC
100KOHM SRN6A
100KOHM SRN6B
100KOHM SRN6C
100KOHM SRN6D

VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR

VccLAN1_05 & VccCL1_05 Internal VR

High = Enable (Default)

Low = Disable

BOM: 02G010015342

SB Heatsink Screwhole
SH1
SH2
13GNJ510M190-1
13GNJ510M190-1
GND
GND

SB1A
ICH9M

RTC_X1
RTC_X2
RTCRST#
INTRUDER#
ICH_INTVRMEN
ICH_LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP

RTC
LPC
LAN / GLAN
CPU
IHDA
SATA

FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3
LPC_FRAME#
LPC_DRQ0# ST68
LPC_DRQ1#
A20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
RC_IN#
H_NMI
H_SMI#
H_STPCLK#
PM_THRMTRIP#
ST80
ESATA_RXN_SB
ESATA_RXP_SB
ESATA_TXN_SB
ESATA_TXP_SB
CLK_SATA_SB#
CLK_SATA_SB
SATARBIAS#
SR38 27.4Ohm 1%
GND

Pass EA measurement

+3VSUS
SR35
10KOhm
GPIO56
+1.5VS_PCIE_ICH
SR36 24.9Ohm 1%
SB_GPIO33
ST82
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
HDD
ODD
HDD_LED#

ACZ_BCLK_AUD
ACZ_SYNC_AUD
ACZ_RST#_AUD
ACZ_SDOUT_AUD
ACZ_BCLK_MDC
ACZ_SYNC_MDC
ACZ_RST#_MDC
ACZ_SDOUT_MDC
33OHM SRN1A
33OHM SRN1D
33OHM SRN1B
33OHM SRN1C
33OHM SRN2D
33OHM SRN2B
33OHM SRN2C
33OHM SRN2A
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT

ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0_AUD
ACZ_SDIN1_MDC
ACZ_SDOUT

SC5
12PF/50V
RTC_X1
SX1
32.768kMhz
+/-20ppm/12.5PF
SR40
10MOhm
SC6
12PF/50V
RTC_X2
GND

OD signal
+VCCP
SRN4D
56OHM
H_FERR#
56OHM SRN4B
PM_THRMTRIP#
56OHM SRN4C
H_THRMTRIP#
SC72
Do Not Stuff
/X
GND

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1

Flash Descriptor Security Override

High = Enable (Default)

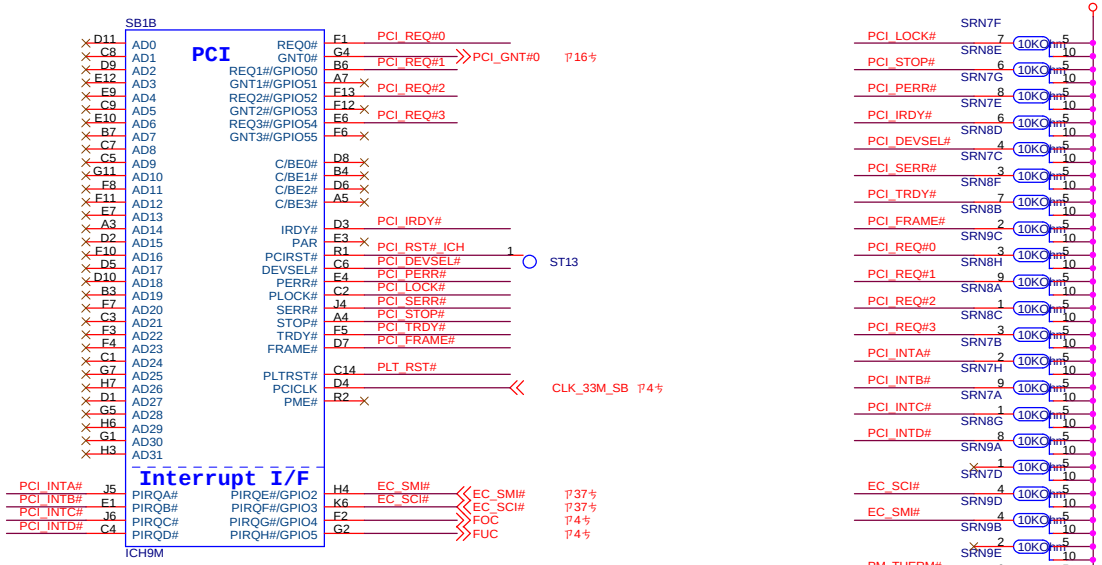
Low = Overridden

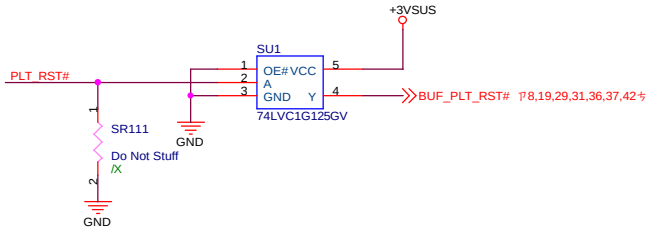
ACZ_SDOUT
SR49 Do Not Stuff 1%
SR5 Do Not Stuff 1%
+3VS
ICH_TP3
GND

SR6 Do Not Stuff
SB_GPIO33
GND

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(1)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 14 of 52	





UNUSED PCI temination

AD [31:0]	Can be left unconnected
C/BE [3:0]#	Can be left unconnected
DEVSEL#	8.2-k weak pull-up resistor to Vcc3_3
FRAME#	8.2-k weak pull-up resistor to Vcc3_3
IRDY#	8.2-k weak pull-up resistor to Vcc3_3
TRDY#	8.2-k weak pull-up resistor to Vcc3_3
STOP#	8.2-k weak pull-up resistor to Vcc3_3
PAR	Can be left unconnected
PERR#	8.2-k weak pull-up resistor to Vcc3_3
REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54	Requires a 8.2-k weak pull-up resistor to Vcc3_3. REQ [3:1] can be configured as GPIO instead.
GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55	Can be left unconnected. GNT [3:1]# can be configured as GPIO instead. GNT [3:0] is sampled as a functional strapping;
PCICLK	Should remain connected to 33-MHz clock source
PCIRST#	Can be left unconnected
PLOCK#	8.2-k weak pull-up resistor to Vcc3_3
SERR#	8.2-k weak pull-up resistor to Vcc3_3
PIRQ [D:A]# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	Requires a 8.2-k weak pull-up resistor to Vcc3_3 PIRQ [H:E]# Can be left unconfigured as GPIO instead
SERIRQ	8.2-k pull-up to Vcc3_3
PME#	Can be left unconnected. Internally pull-up
CLKRUN#	8.2-k weak pull-up resistor to Vcc3_3

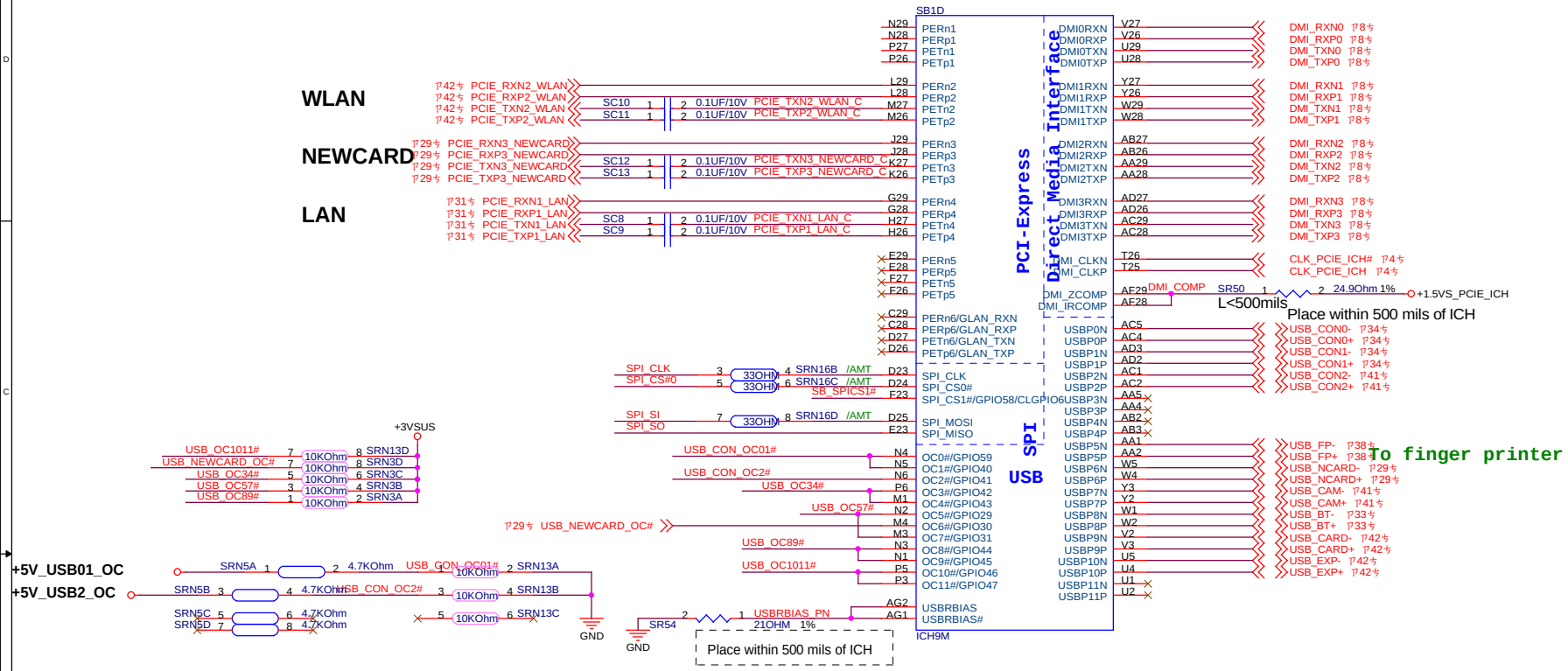
P80VC1

Title : SB-ICH9M(2)

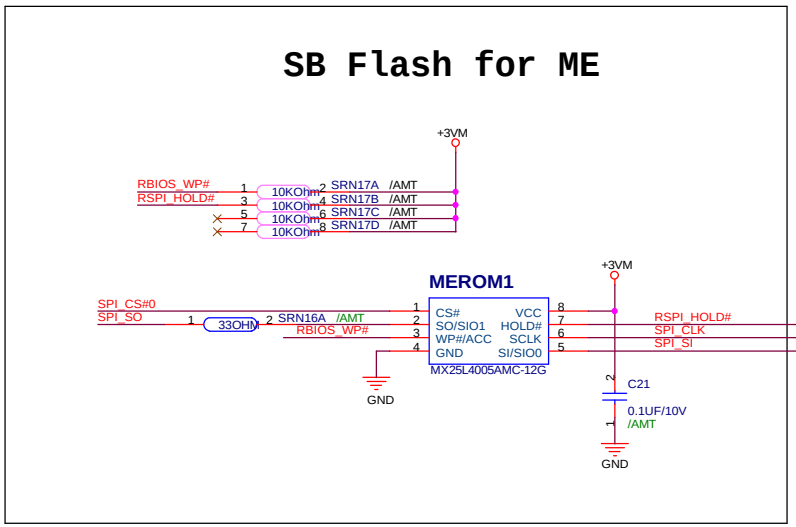
ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 15 of 52

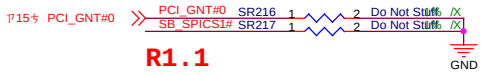


USB0	CON
USB1	CON
USB2	CON
USB3	N/A
USB4	N/A
USB5	FingerPrint
USB6	NewCard
USB7	Camera
USB8	BT
USB9	Cardreader
USB10	MC (WLAN)
USB11	N/A



ICH9 Boot BIOS select

		GNT#0	CS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	



R1.1

SPI_MOSI
iTPM
Enable
High = Enable
Low = Disable(Default)

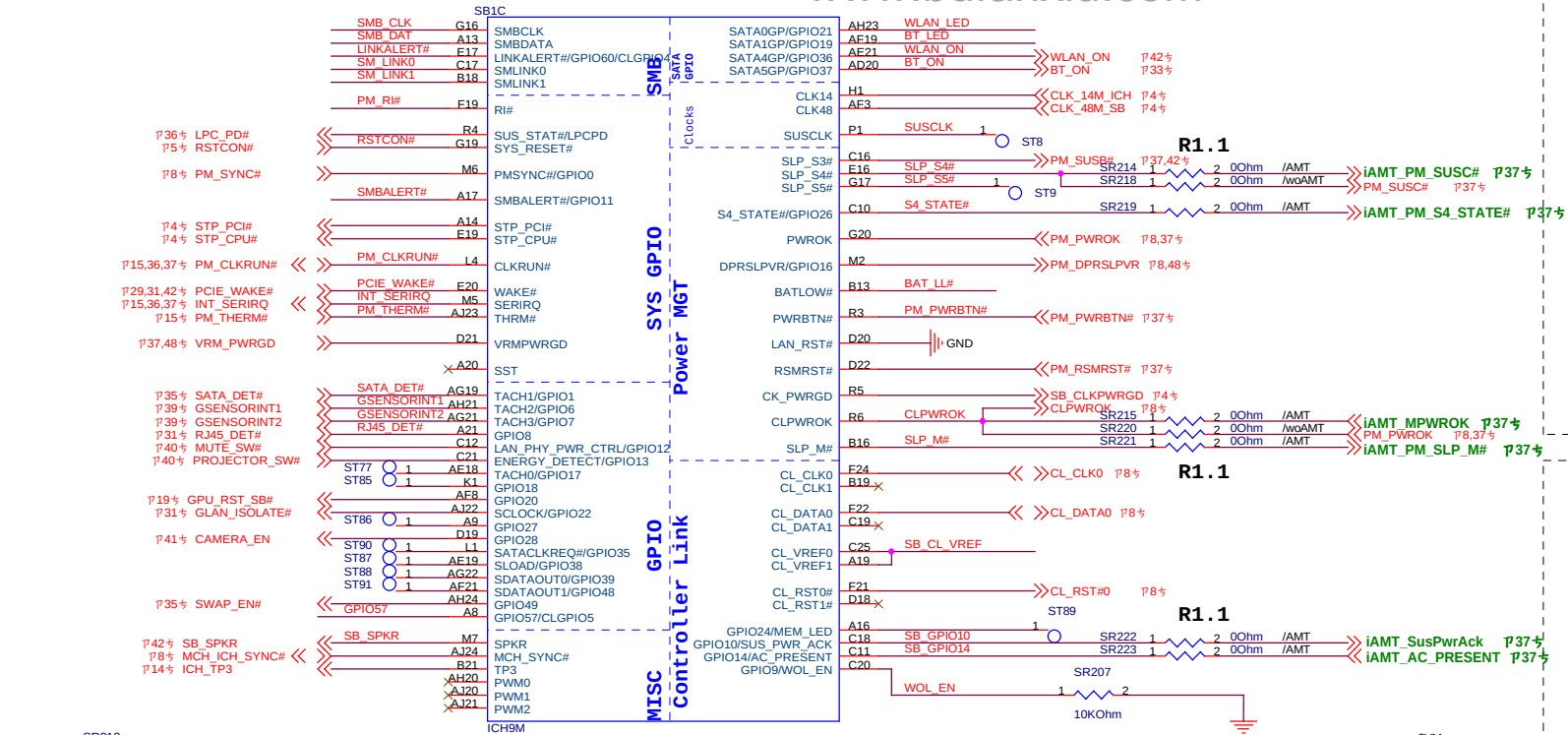
P80VC1

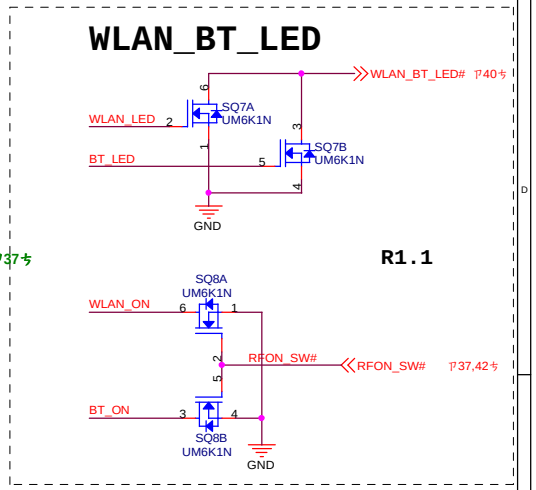
Title : SB-ICH9M(3)

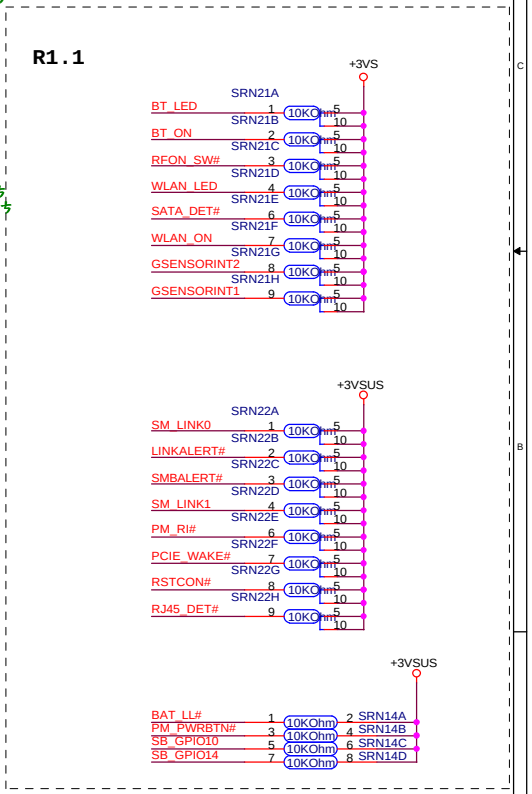
ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

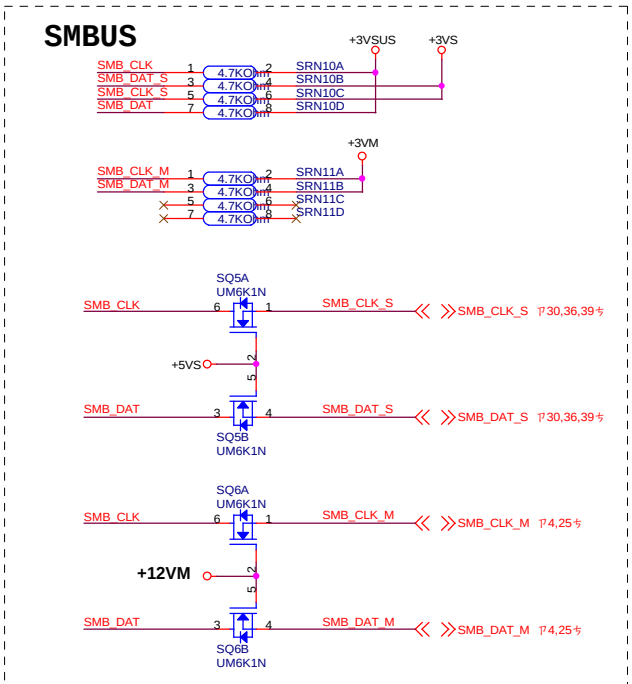
Date: Tuesday, December 16, 2008 Sheet 16 of 52

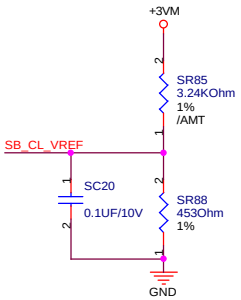






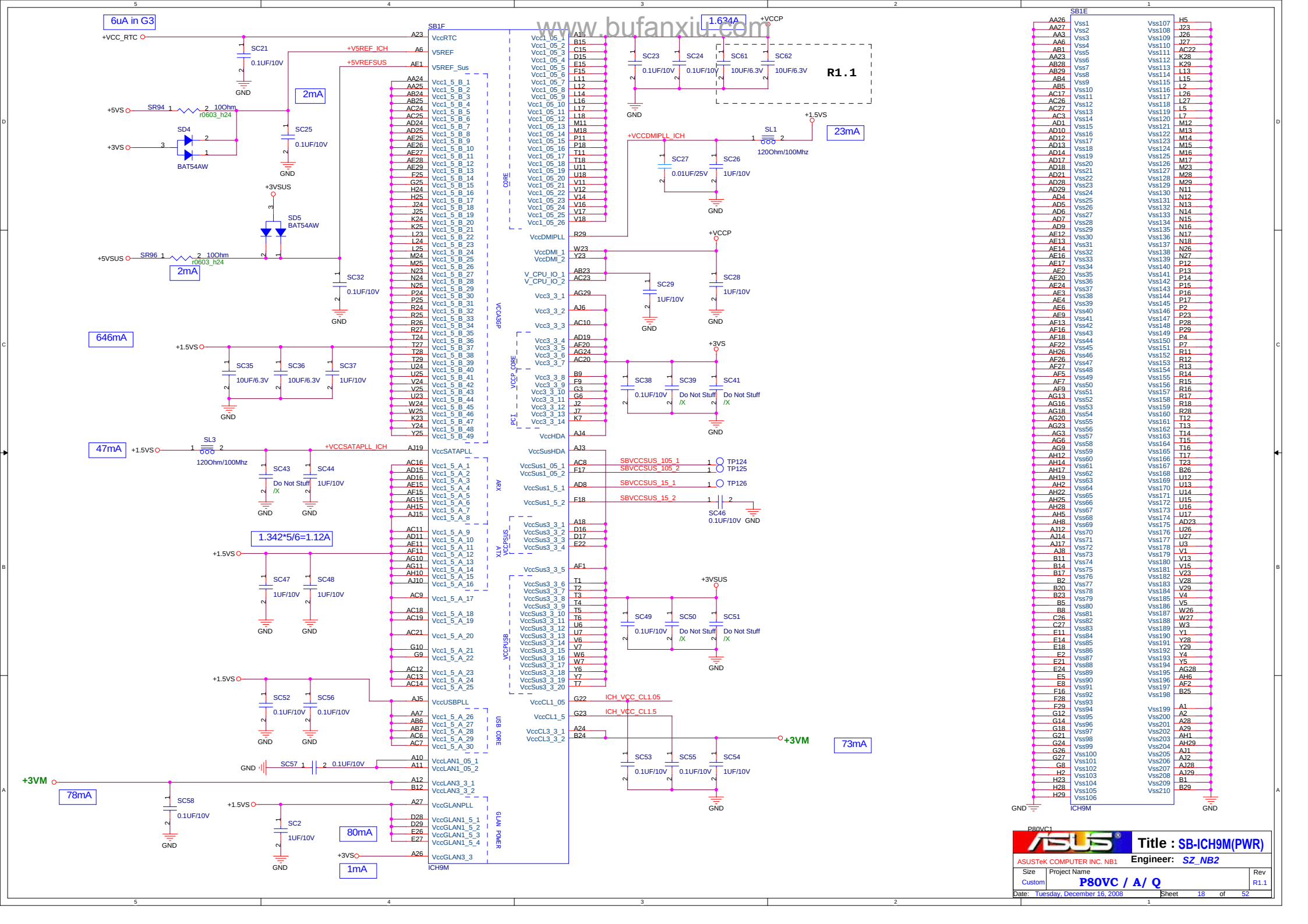
GPIO57:
PU:iTPM Physical presence
PD:100Kohm





P80VC1

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(4)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 17 of 52	



PCIEG_RXP[0..15] 于10分
PCIEG_RXN[0..15] 于10分
PCIENB_RXP[0..15] 于10分
PCIENB_RXN[0..15] 于10分

PCIENB_RXN15	GC4	1	2 0.1UF/10V /PM	PCIEG_TXN15
PCIENB_RXP15	GC5	1	2 0.1UF/10V /PM	PCIEG_TXP15
PCIENB_RXN14	GC6	1	2 0.1UF/10V /PM	PCIEG_TXN14
PCIENB_RXP14	GC7	1	2 0.1UF/10V /PM	PCIEG_TXP14
PCIENB_RXN13	GC8	1	2 0.1UF/10V /PM	PCIEG_TXN13
PCIENB_RXP13	GC9	1	2 0.1UF/10V /PM	PCIEG_TXP13
PCIENB_RXN12	GC10	1	2 0.1UF/10V /PM	PCIEG_TXN12
PCIENB_RXP12	GC11	1	2 0.1UF/10V /PM	PCIEG_TXP12
PCIENB_RXN11	GC12	1	2 0.1UF/10V /PM	PCIEG_TXN11
PCIENB_RXP11	GC17	1	2 0.1UF/10V /PM	PCIEG_TXP11
PCIENB_RXN10	GC18	1	2 0.1UF/10V /PM	PCIEG_TXN10
PCIENB_RXP10	GC19	1	2 0.1UF/10V /PM	PCIEG_TXP10
PCIENB_RXN9	GC20	1	2 0.1UF/10V /PM	PCIEG_TXN9
PCIENB_RXP9	GC21	1	2 0.1UF/10V /PM	PCIEG_TXP9
PCIENB_RXN8	GC22	1	2 0.1UF/10V /PM	PCIEG_TXN8
PCIENB_RXP8	GC23	1	2 0.1UF/10V /PM	PCIEG_TXP8
PCIENB_RXN7	GC24	1	2 0.1UF/10V /PM	PCIEG_TXN7
PCIENB_RXP7	GC25	1	2 0.1UF/10V /PM	PCIEG_TXP7
PCIENB_RXN6	GC26	1	2 0.1UF/10V /PM	PCIEG_TXN6
PCIENB_RXP6	GC27	1	2 0.1UF/10V /PM	PCIEG_TXP6
PCIENB_RXN5	GC28	1	2 0.1UF/10V /PM	PCIEG_TXN5
PCIENB_RXP5	GC29	1	2 0.1UF/10V /PM	PCIEG_TXP5
PCIENB_RXN4	GC30	1	2 0.1UF/10V /PM	PCIEG_TXN4
PCIENB_RXP4	GC31	1	2 0.1UF/10V /PM	PCIEG_TXP4
PCIENB_RXN3	GC32	1	2 0.1UF/10V /PM	PCIEG_TXN3
PCIENB_RXP3	GC33	1	2 0.1UF/10V /PM	PCIEG_TXP3
PCIENB_RXN2	GC34	1	2 0.1UF/10V /PM	PCIEG_TXN2
PCIENB_RXP2	GC35	1	2 0.1UF/10V /PM	PCIEG_TXP2
PCIENB_RXN1	GC42	1	2 0.1UF/10V /PM	PCIEG_TXN1
PCIENB_RXP1	GC43	1	2 0.1UF/10V /PM	PCIEG_TXP1
PCIENB_RXN0	GC44	1	2 0.1UF/10V /PM	PCIEG_TXN0
PCIENB_RXP0	GC45	1	2 0.1UF/10V /PM	PCIEG_TXP0

+3VSG

GR106 10KOhm /PM

GD1 BAT54AW /PM

于8,15,29,31,36,37,42分 BUF_PLT_RST#

于17分 GPU_RST_SB#

NB9M_RST# AD9

于4分 CLK_PCIE_GPU

于4分 CLK_PCIE_GPU#

GT01 /X

GT02 /X

NC_10 AE9

PEX_RST_N

CLK_PCIE_NB9M AB10
CLK_PCIE_NB9M# AC10
PEX_REFCLK
PEX_REFCLK_N

PCIEG_TXP0	AD10	PEX_TX0
PCIEG_TXN0	AD11	PEX_TX0_N
PCIEG_RXP0	AE12	PEX_RX0
PCIEG_RXN0	AE12	PEX_RX0_N
PCIEG_TXP1	AD12	PEX_TX1
PCIEG_TXN1	AC12	PEX_TX1_N
PCIEG_RXP1	AG12	PEX_RX1
PCIEG_RXN1	AG13	PEX_RX1_N
PCIEG_TXP2	AB11	PEX_TX2
PCIEG_TXN2	AB12	PEX_TX2_N
PCIEG_RXP2	AF13	PEX_RX2
PCIEG_RXN2	AE13	PEX_RX2_N
PCIEG_TXP3	AD13	PEX_TX3
PCIEG_TXN3	AD14	PEX_TX3_N
PCIEG_RXP3	AE15	PEX_RX3
PCIEG_RXN3	AF15	PEX_RX3_N
PCIEG_TXP4	AD15	PEX_TX4
PCIEG_TXN4	AC15	PEX_TX4_N
PCIEG_RXP4	AG15	PEX_RX4
PCIEG_RXN4	AG16	PEX_RX4_N
PCIEG_TXP5	AB14	PEX_TX5
PCIEG_TXN5	AB15	PEX_TX5_N
PCIEG_RXP5	AF16	PEX_RX5
PCIEG_RXN5	AE16	PEX_RX5_N
PCIEG_TXP6	AC16	PEX_TX6
PCIEG_TXN6	AD16	PEX_TX6_N
PCIEG_RXP6	AE18	PEX_RX6
PCIEG_RXN6	AF18	PEX_RX6_N
PCIEG_TXP7	AD17	PEX_TX7
PCIEG_TXN7	AD18	PEX_TX7_N
PCIEG_RXP7	AG18	PEX_RX7
PCIEG_RXN7	AG19	PEX_RX7_N
PCIEG_TXP8	AC18	PEX_TX8
PCIEG_TXN8	AB18	PEX_TX8_N
PCIEG_RXP8	AF19	PEX_RX8
PCIEG_RXN8	AE19	PEX_RX8_N
PCIEG_TXP9	AB19	PEX_TX9
PCIEG_TXN9	AB20	PEX_TX9_N
PCIEG_RXP9	AE21	PEX_RX9
PCIEG_RXN9	AF21	PEX_RX9_N
PCIEG_TXP10	AD19	PEX_TX10
PCIEG_TXN10	AD20	PEX_TX10_N
PCIEG_RXP10	AG21	PEX_RX10
PCIEG_RXN10	AG22	PEX_RX10_N
PCIEG_TXP11	AD21	PEX_TX11
PCIEG_TXN11	AC21	PEX_TX11_N
PCIEG_RXP11	AF22	PEX_RX11
PCIEG_RXN11	AE22	PEX_RX11_N
PCIEG_TXP12	AB21	PEX_TX12
PCIEG_TXN12	AB22	PEX_TX12_N
PCIEG_RXP12	AE24	PEX_RX12
PCIEG_RXN12	AF24	PEX_RX12_N
PCIEG_TXP13	AC22	PEX_TX13
PCIEG_TXN13	AD22	PEX_TX13_N
PCIEG_RXP13	AG24	PEX_RX13
PCIEG_RXN13	AF25	PEX_RX13_N
PCIEG_TXP14	AD23	PEX_TX14
PCIEG_TXN14	AD24	PEX_TX14_N
PCIEG_RXP14	AG25	PEX_RX14
PCIEG_RXN14	AG26	PEX_RX14_N
PCIEG_TXP15	AE25	PEX_TX15
PCIEG_TXN15	AE26	PEX_TX15_N
PCIEG_RXP15	AF27	PEX_RX15
PCIEG_RXN15	AE27	PEX_RX15_N

NB9M_GS /PM

+3VS +3VSG 200mA

+1.8VS +1.8VSG

+0.9VS +0.9VS_VGA

+1.1VS_GPU +VCCP 1.715A

JP4 Do Not Stuff /X

Use +1.05VS(+VCCP) for +1.1VS rail

BOM:02G190014113

9.1A
1/13 PCI_EXPRESS

PEX_IOVDD_01 AC9
PEX_IOVDD_02 AD7
PEX_IOVDD_03 AD8
PEX_IOVDD_04 AE7
PEX_IOVDD_05 AF7
PEX_IOVDD_06 AG7

PEX_IOVDDQ_01 AB13
PEX_IOVDDQ_02 AB16
PEX_IOVDDQ_03 AB17
PEX_IOVDDQ_04 AB7
PEX_IOVDDQ_05 AB8
PEX_IOVDDQ_06 AB9
PEX_IOVDDQ_07 AC13
PEX_IOVDDQ_08 AC7
PEX_IOVDDQ_09 AD6
PEX_IOVDDQ_10 AE6
PEX_IOVDDQ_11 AF6
PEX_IOVDDQ_12 AG6

+1.1VS_GPU

1.6A

GC13 10UF/10V X7R 10% /PM
GC14 1UF/10V /PM
GC15 1UF/10V /PM
GC16 1UF/10V /PM

GND

VDD_01 J10
VDD_02 J12
VDD_03 J13
VDD_04 J9
VDD_05 L9
VDD_06 M11
VDD_07 M17
VDD_08 M9
VDD_09 N11
VDD_10 N12
VDD_11 N13
VDD_12 N14
VDD_13 N15
VDD_14 N16
VDD_15 N17
VDD_16 N19
VDD_17 N9
VDD_18 P11
VDD_19 P12
VDD_20 P13
VDD_21 P14
VDD_22 P15
VDD_23 P16
VDD_24 P17
VDD_25 R11
VDD_26 R12
VDD_27 R13
VDD_28 R14
VDD_29 R15
VDD_30 R16
VDD_31 R17
VDD_32 R9
VDD_33 T11
VDD_34 T17
VDD_35 T9
VDD_36 U19
VDD_37 U9
VDD_38 W10
VDD_39 W12
VDD_40 W13
VDD_41 W18
VDD_42 W19
VDD_43 W9

+VGA_CORE_VS

GC46 10UF/6.3V /PM
GC47 1UF/10V /PM
GC48 1UF/10V /PM
GC49 1UF/10V /PM
GC50 1UF/10V /PM
GC51 1UF/10V /PM
GC41 1UF/10V /PM

GND

VDD_SENSE W15
GND_SENSE W16

NVDD_SENSE 于53分

GND

+3VSG

80mA

VDD33_01 A12
VDD33_02 B12
VDD33_03 C12
VDD33_04 D12
VDD33_05 E12
VDD33_06 F12

GC53 1UF/10V /PM

GND

+1.1VS_GPU

65mA

PEX_PLLVDD AF9

GL1 10NH I0603 /PM

GC54 Do Not Stuff /X
GC56 1UF/10V /PM

GND

PEX_TSTCLK_OUT AF10 PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N AE10 PEX_TSTCLK_OUT_N

GR1 200Ohm 1% /PM

NC_09 AG9

PEX_TERMP AG10

GR2 2.49KOhm 1% /PM

GND

PCI-E I/O Termination Calibration

P80VC1

Title :

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 19 of 52

GU1B
2/13 FRAME_BUFFER

FBAD0	D21	FBA_D0
FBAD1	C22	FBA_D1
FBAD2	B22	FBA_D2
FBAD3	A22	FBA_D3
FBAD4	C24	FBA_D4
FBAD5	B25	FBA_D5
FBAD6	A25	FBA_D6
FBAD7	A26	FBA_D7
FBAD8	D22	FBA_D8
FBAD9	E22	FBA_D9
FBAD10	E24	FBA_D10
FBAD11	D24	FBA_D11
FBAD12	D26	FBA_D12
FBAD13	D27	FBA_D13
FBAD14	C27	FBA_D14
FBAD15	B27	FBA_D15
FBAD16	D16	FBA_D16
FBAD17	E16	FBA_D17
FBAD18	D17	FBA_D18
FBAD19	F18	FBA_D19
FBAD20	D20	FBA_D20
FBAD21	F20	FBA_D21
FBAD22	F21	FBA_D22
FBAD23	F21	FBA_D23
FBAD24	C16	FBA_D24
FBAD25	B18	FBA_D25
FBAD26	C18	FBA_D26
FBAD27	D18	FBA_D27
FBAD28	C19	FBA_D28
FBAD29	C21	FBA_D29
FBAD30	B21	FBA_D30
FBAD31	A21	FBA_D31
FBAD32	P22	FBA_D32
FBAD33	P24	FBA_D33
FBAD34	R23	FBA_D34
FBAD35	R24	FBA_D35
FBAD36	T23	FBA_D36
FBAD37	U24	FBA_D37
FBAD38	V23	FBA_D38
FBAD39	V24	FBA_D39
FBAD40	N25	FBA_D40
FBAD41	N26	FBA_D41
FBAD42	R25	FBA_D42
FBAD43	R26	FBA_D43
FBAD44	T25	FBA_D44
FBAD45	V26	FBA_D45
FBAD46	V25	FBA_D46
FBAD47	V27	FBA_D47
FBAD48	V22	FBA_D48
FBAD49	W22	FBA_D49
FBAD50	W23	FBA_D50
FBAD51	W24	FBA_D51
FBAD52	AA22	FBA_D52
FBAD53	AB23	FBA_D53
FBAD54	AB24	FBA_D54
FBAD55	AC24	FBA_D55
FBAD56	W25	FBA_D56
FBAD57	W26	FBA_D57
FBAD58	W27	FBA_D58
FBAD59	AA25	FBA_D59
FBAD60	AB25	FBA_D60
FBAD61	AB26	FBA_D61
FBAD62	AD26	FBA_D62
FBAD63	AD27	FBA_D63

FBADQM0	D23	FBA_DQM0
FBADQM1	C26	FBA_DQM1
FBADQM2	D19	FBA_DQM2
FBADQM3	B19	FBA_DQM3
FBADQM4	T24	FBA_DQM4
FBADQM5	T26	FBA_DQM5
FBADQM6	AA23	FBA_DQM6
FBADQM7	AB27	FBA_DQM7

FBAWDQS0	A24	FBA_DQS_WP0
FBAWDQS1	C25	FBA_DQS_WP1
FBAWDQS2	E19	FBA_DQS_WP2
FBAWDQS3	A19	FBA_DQS_WP3
FBAWDQS4	T22	FBA_DQS_WP4
FBAWDQS5	T27	FBA_DQS_WP5
FBAWDQS6	AA24	FBA_DQS_WP6
FBAWDQS7	AA26	FBA_DQS_WP7

FBARDQS0	B24	FBA_DQS_RN0
FBARDQS1	D25	FBA_DQS_RN1
FBARDQS2	E18	FBA_DQS_RN2
FBARDQS3	A18	FBA_DQS_RN3
FBARDQS4	R22	FBA_DQS_RN4
FBARDQS5	R27	FBA_DQS_RN5
FBARDQS6	Y24	FBA_DQS_RN6
FBARDQS7	AA27	FBA_DQS_RN7

NB9M_GS
/PM

+1.8VSG

FBVDDQ_01	A13	
FBVDDQ_02	B13	
FBVDDQ_03	C13	
FBVDDQ_04	D13	
FBVDDQ_05	D14	
FBVDDQ_06	E13	
FBVDDQ_07	F13	
FBVDDQ_08	F14	
FBVDDQ_09	F15	
FBVDDQ_10	F16	
FBVDDQ_11	F17	
FBVDDQ_12	F19	
FBVDDQ_13	F22	
FBVDDQ_14	H23	
FBVDDQ_15	H26	
FBVDDQ_16	J15	
FBVDDQ_17	J16	
FBVDDQ_18	J18	
FBVDDQ_19	J19	
FBVDDQ_20	L19	
FBVDDQ_21	L23	
FBVDDQ_22	L26	
FBVDDQ_23	M19	
FBVDDQ_24	N22	
FBVDDQ_25	U22	
FBVDDQ_26	Y22	

GC57 10UF/6.3V /PM
GC58 1UF/10V /PM
GC59 1UF/10V /PM
GC60 1UF/10V /PM
GC61 1UF/10V /PM
GC62 1UF/10V /PM
GND

Mapping Mode A

FBA_CMD0	F26	FBA_A3	FBA_A3
FBA_CMD1	J24	FBA_A0	FBA_A0
FBA_CMD2	F25	FBA_A2	FBA_A2
FBA_CMD3	M23	FBA_A1	FBA_A1
FBA_CMD4	N27	FBE_A3	FBE_A3
FBA_CMD5	M27	FBE_A4	FBE_A4
FBA_CMD6	K26	FBE_A5	FBE_A5
FBA_CMD7	J25	FBA_CS1#	GT03 /X
FBA_CMD8	J27	FBA_CS0#	FBA_CS0#
FBA_CMD9	G23	FBA_WE#	FBA_WE#
FBA_CMD10	G26	FBA_BA0	FBA_BA0
FBA_CMD11	J23	FBA_CKE	FBA_CKE
FBA_CMD12	M25	FBA_RST	
FBA_CMD13	K27	FBE_A2	FBE_A2
FBA_CMD14	G25	FBA_A12	FBA_A12
FBA_CMD15	L24	FBA_RAS#	FBA_RAS#
FBA_CMD16	K23	FBA_A11	FBA_A11
FBA_CMD17	K24	FBA_A10	FBA_A10
FBA_CMD18	G22	FBA_BA1	FBA_BA1
FBA_CMD19	K25	FBA_A8	FBA_A8
FBA_CMD20	H22	FBA_A9	FBA_A9
FBA_CMD21	M26	FBA_A6	FBA_A6
FBA_CMD22	H24	FBA_A5	FBA_A5
FBA_CMD23	F27	FBA_A7	FBA_A7
FBA_CMD24	J26	FBA_A4	FBA_A4
FBA_CMD25	G24	FBA_CAS#	FBA_CAS#
FBA_CMD26	G27	FBA_A13	FBA_A13
FBA_CMD27	M24	FBA_BA2	FBA_BA2
FBA_CMD28	K22		GT04 /X
NC_11	J22		
NC_12	L22		

FBA_CKE — GR3 10KOhm /PM — GND

FBA_RST — GR4 0Ohm /PM — FBA_ODT — GR5 10KOhm /PM — GND

FBA_CLK0	F24	FBA_CLK0	FBA_CLK0
FBA_CLK0_N	F23	FBA_CLK0#	FBA_CLK0#
FBA_CLK1	N24	FBA_CLK1	FBA_CLK1
FBA_CLK1_N	N23	FBA_CLK1#	FBA_CLK1#

+1.8VSG

FB_CAL_PD_VDDQ — B15 — GR6 30.1OHM 1%
FB_CAL_PU_GND — A15 — GR7 30.1OHM 1%
FB_CAL_TERM_GND — B16 — GR8 Do Not Stuff 1% /X — GND

+1.8VSG

FBA_DEBUG — M22 — GR9 10KOhm /PM

+1.8VSG

GR10 1KOhm 1% /PM
FB_VREF — A16 — FB_VREF
GR11 1KOhm 1% /PM
GC79 0.1UF/10V /PM
GND

15mil

+1.1VS_GPU

GL2 120Ohm/100Mhz /PM

35mA

FB_PLLAVDD — R19
FB_DLLAVDD — T19

GC77 Do Not Stuff /X
GC80 1UF/10V /PM
GC81 Do Not Stuff /X
GND

P80VC1

Title :

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 20 of 52

FBAWDQS[0..7]
FBARDQS[0..7]
FBADQM[0..7]

03G15133F114:
03G15133F211

GU2

K4N1G164QQ_HC25
/PM

GU3

K4N1G164QQ_HC25
/PM

FBA_CLK1 GR14 1 2 475Ohm 1% FBA_CLK1#
/PM

FBA_CLK0 GR15 1 2 475Ohm 1% FBA_CLK0#
/PM

+1.8VSG

GR12 1KOhm 1% /PM — FBAVREF0 — GC83 0.1UF/10V /PM — GND
GR13 1KOhm 1% /PM — FBAVREF1 — GC84 0.1UF/10V /PM — GND
GR16 1KOhm 1% /PM — GND
GR17 1KOhm 1% /PM — GND

15mil

GC85 GC86 GC87 1UF/10V /PM — Do Not Stuff /X — GND
GC88 GC89 GC90 1UF/10V /PM — Do Not Stuff /X — GND
GC91 GC92 GC93 1UF/10V /PM — Do Not Stuff /X — GND
GC94 GC95 GC96 1UF/10V /PM — Do Not Stuff /X — GND

GU4

K4N1G164QQ_HC25
/PM

GU5

K4N1G164QQ_HC25
/PM

+0.9VS_VGA

GRN3C GRN3F GRN1H GRN2B GRN1F GRN1C GRN2A GRN3A — GC109 0.1UF/10V /PM — GND
GRN1A GRN2G GRN1G GRN2F GRN2H GRN1B GRN2C GRN2E — GC110 0.1UF/10V /PM — GND
GRN1D GRN2D GRN3E GRN1E GRN3B GRN3H GRN3G GRN3D — GC111 10UF/6.3V /PM — GND

P80VC1

ASUSTeK COMPUTER INC. NB1

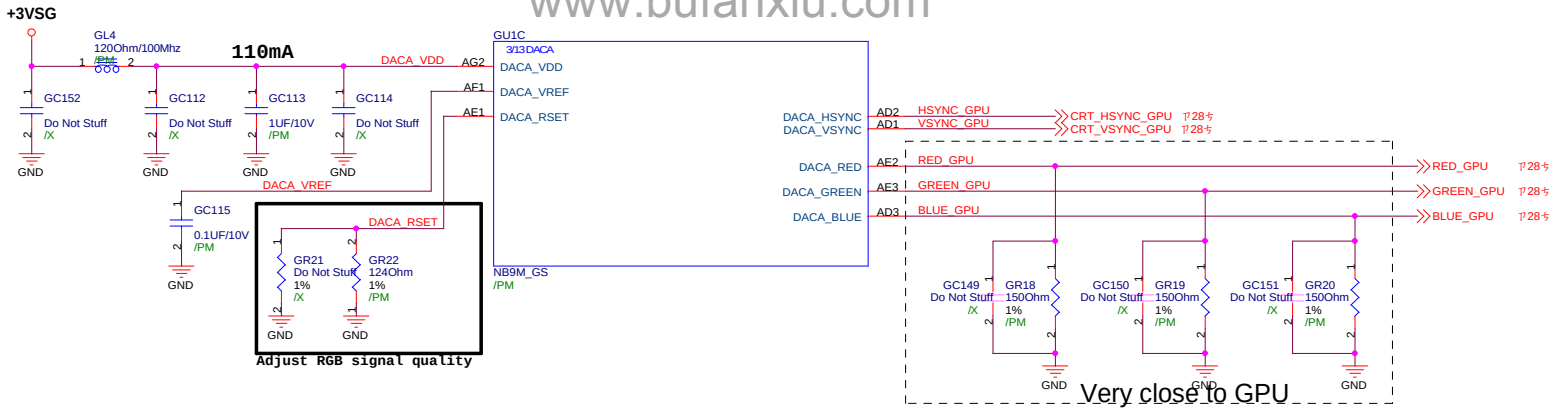
Title :

Engineer: SZ_NB2

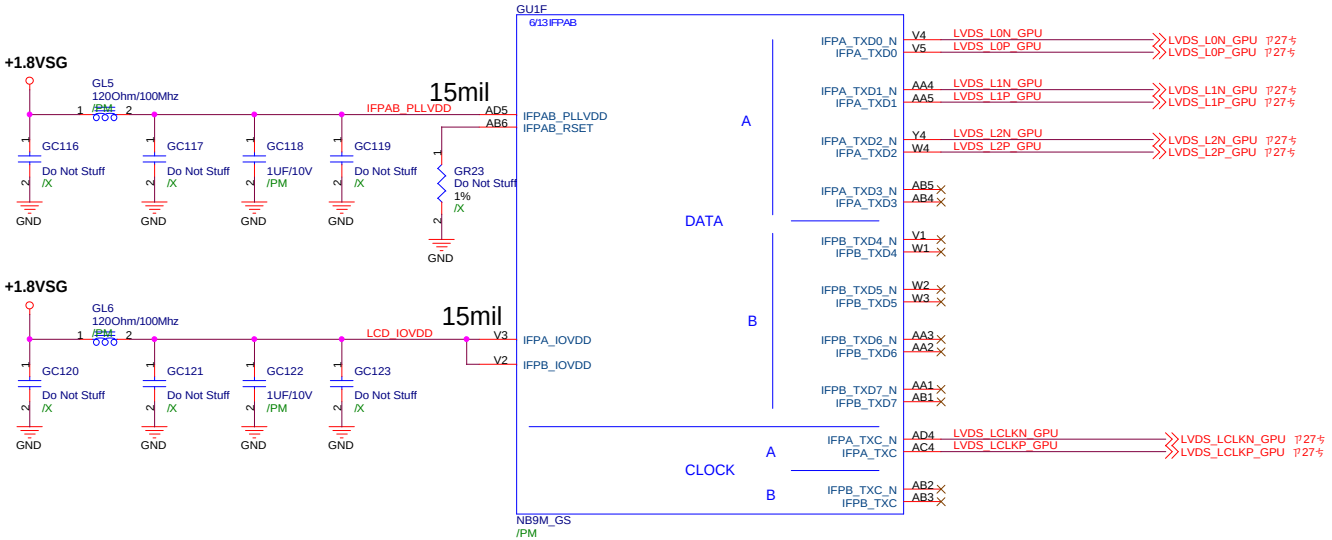
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 21 of 52

VGA

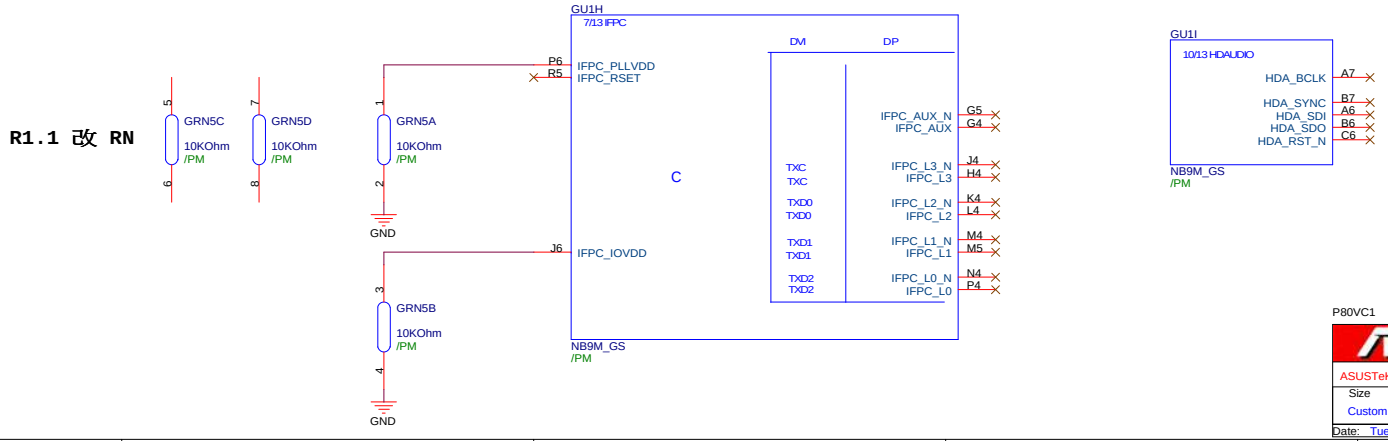


LVDS



HDMI

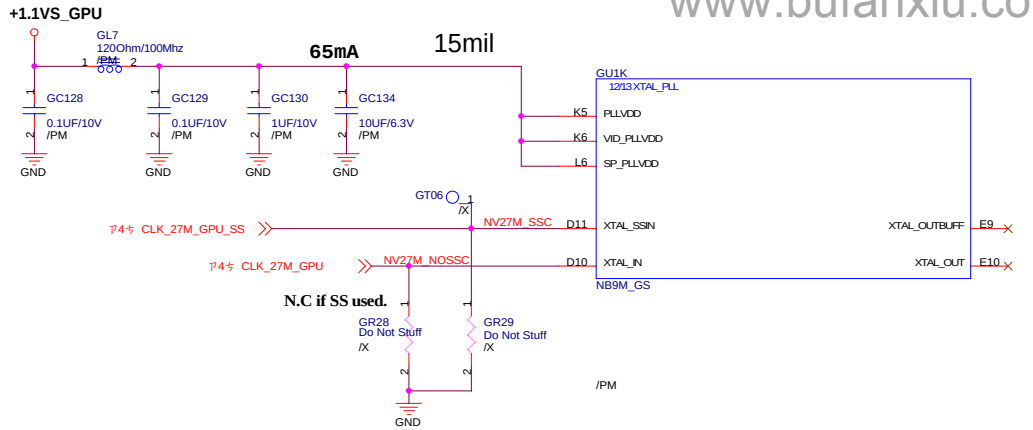
R1.1 改 RN

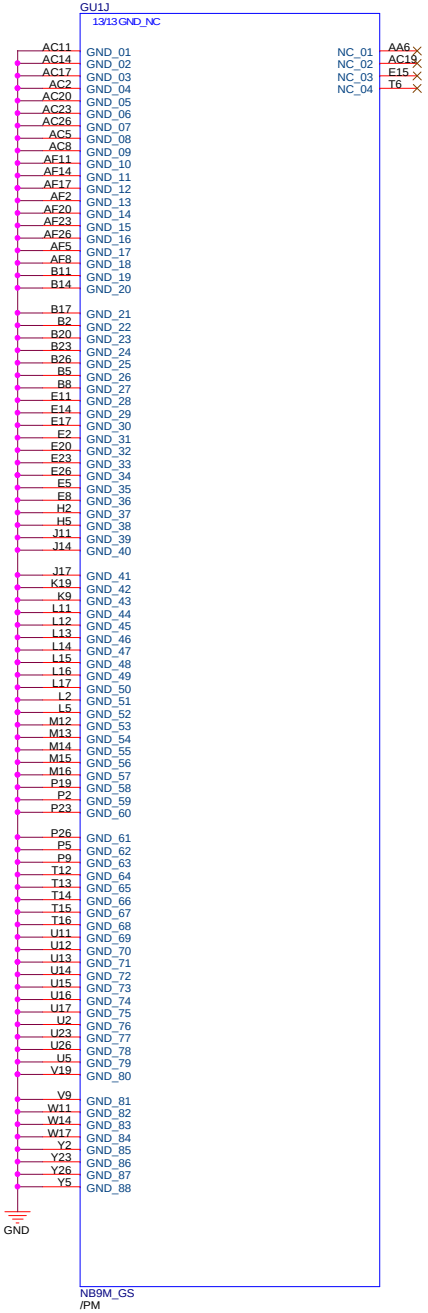


P80VC1

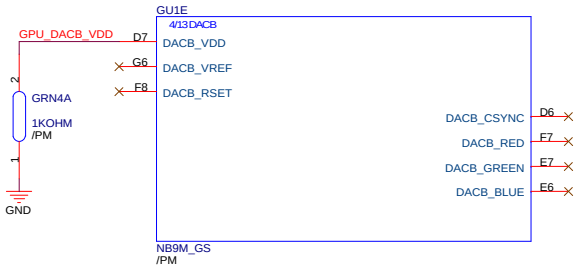
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 22 of 52	

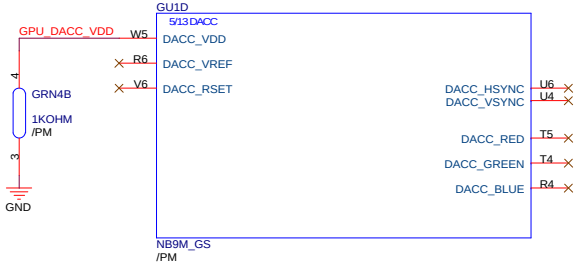
Xtal

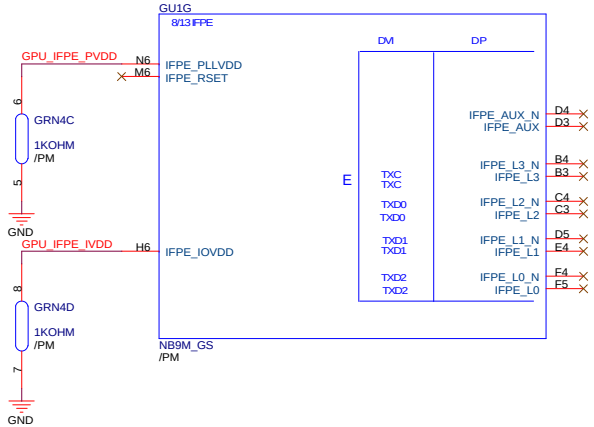




Other







P80VC1

ASUSTeK COMPUTER INC. NB1

Title :

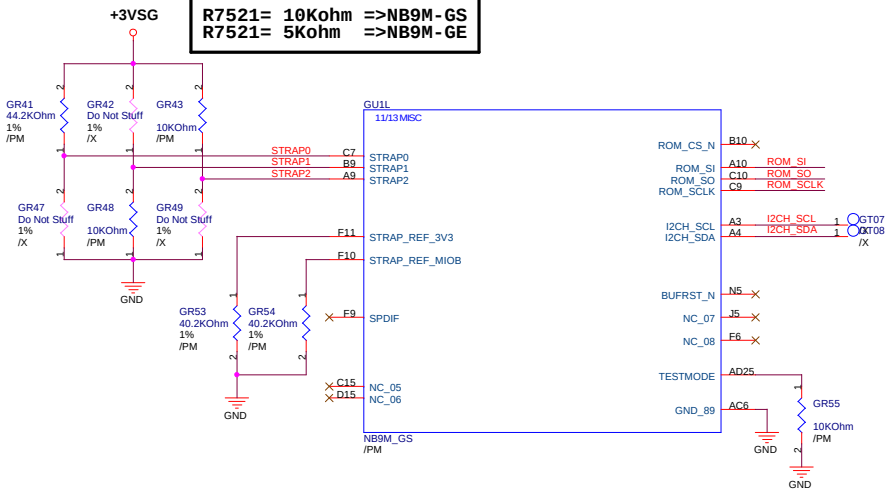
Engineer: SZ_NB2

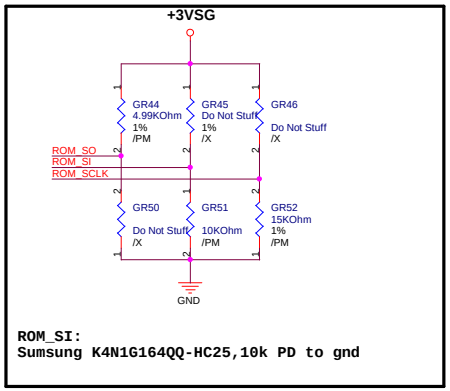
Size	Project Name	Rev
Custom	P80VC / A / Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 23 of 52

ROM

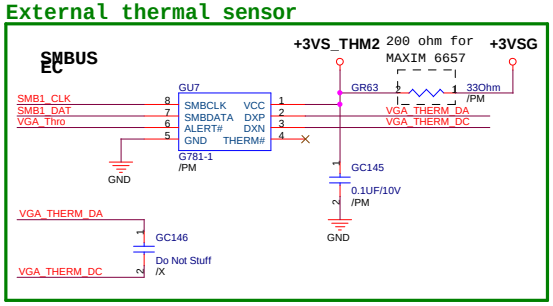
R7521= 10Kohm =>NB9M-GS
R7521= 5Kohm =>NB9M-GE

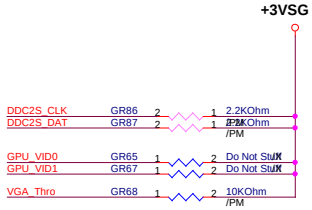


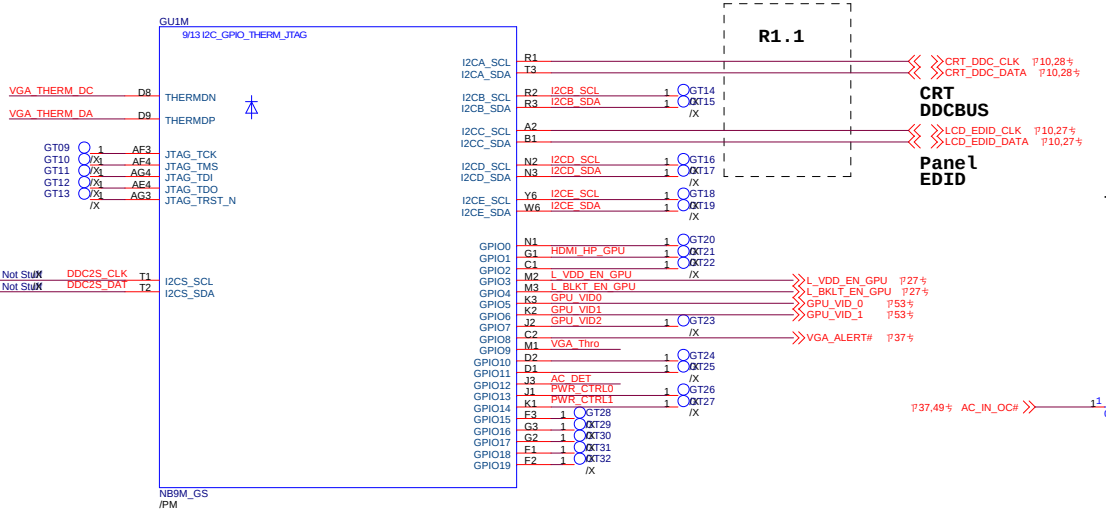


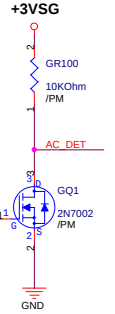
GPIO

External thermal sensor









GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL

P80VC1

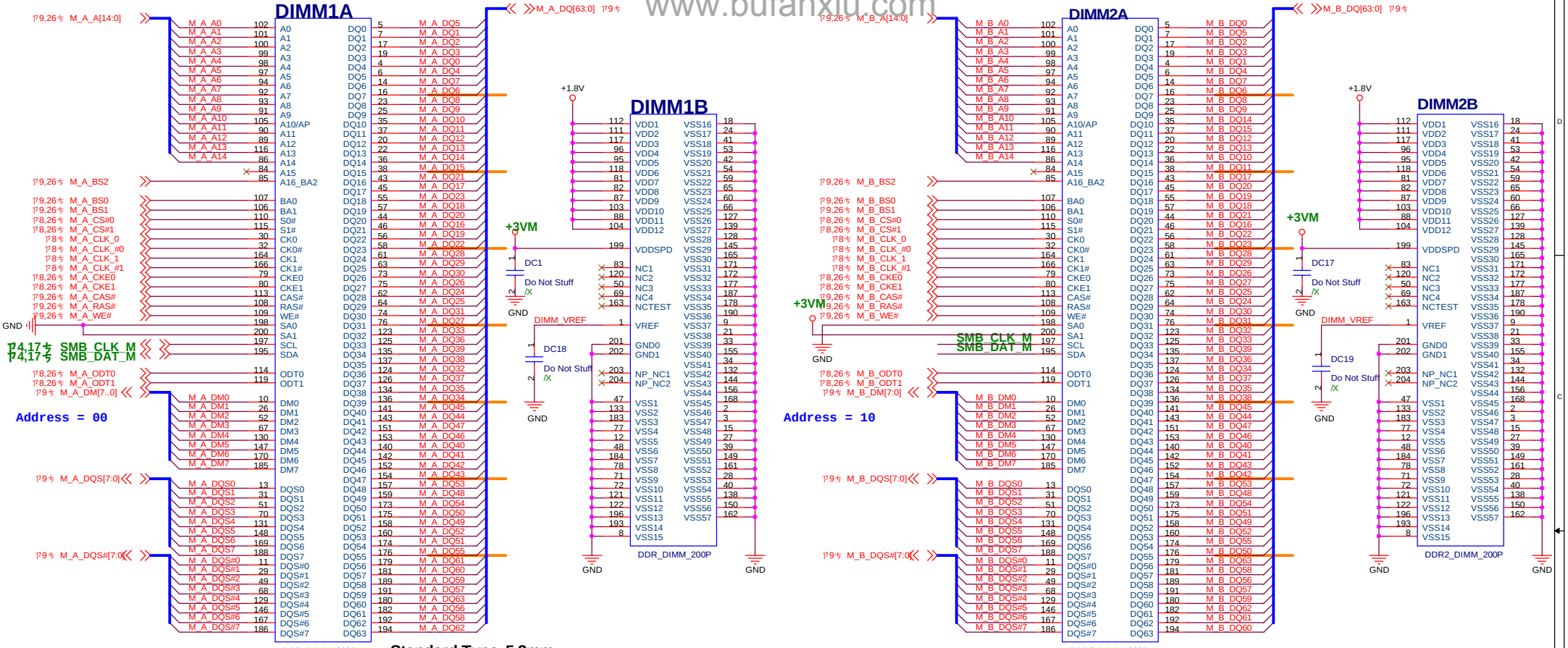
ASUSTeK COMPUTER INC. NB1

Title :

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 24 of 52



Standard Type, 5.2mm

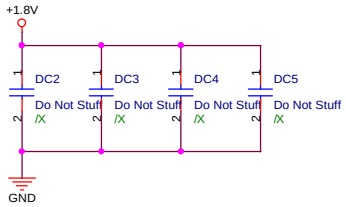
12G025122000 DDR2 Channel-A

12G025C22004

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

Power Cap

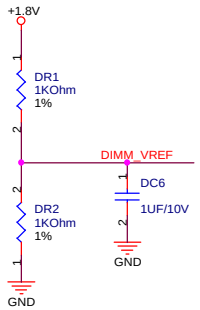
Close to DIMM



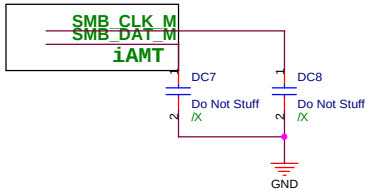
Placement at each DIMM each side by one

DIMM_VREF

Close to DIMM



Close to DIMM



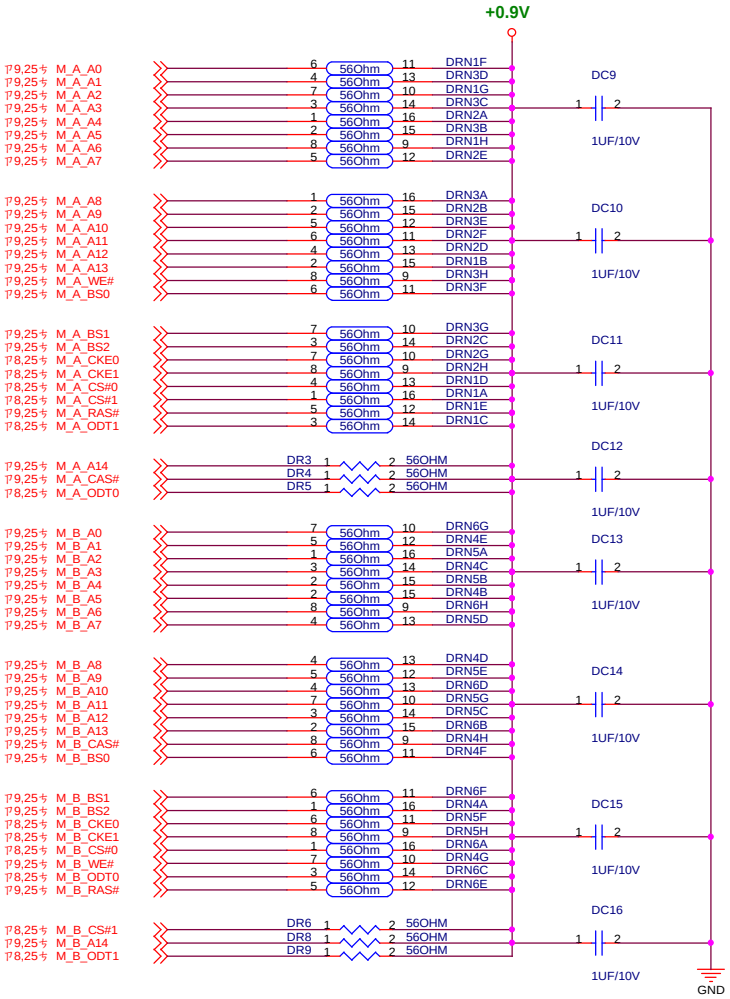
P80VC1

Title : DDR2 SO-DIMMs

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

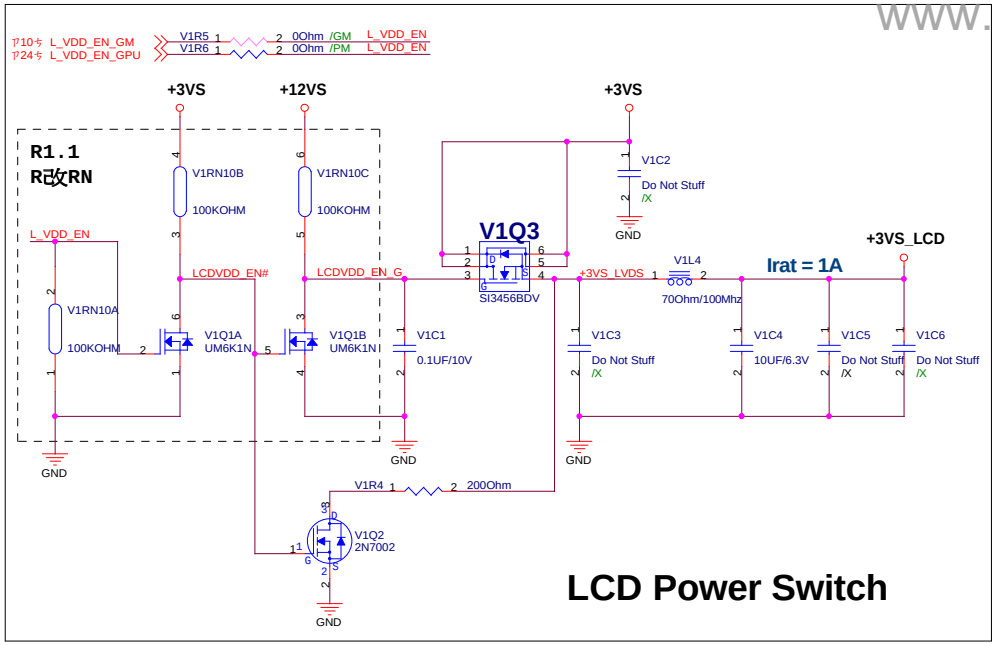
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

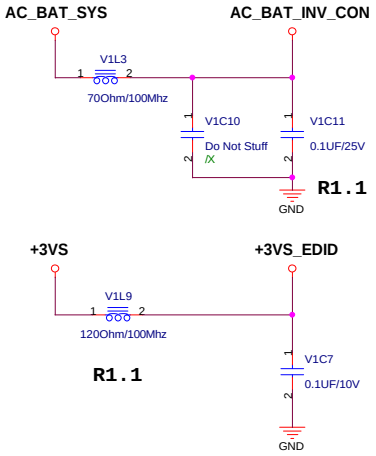
Date: Tuesday, December 16, 2008 Sheet 25 of 52

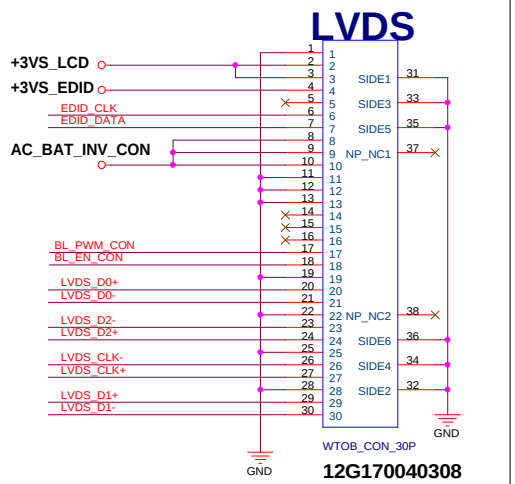


P80VC1

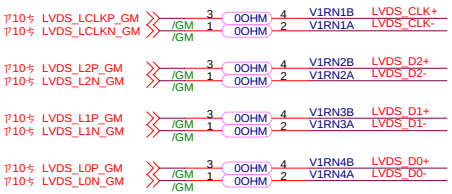
ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 26 of 52	



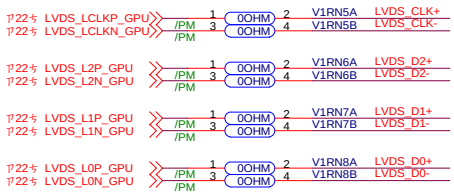


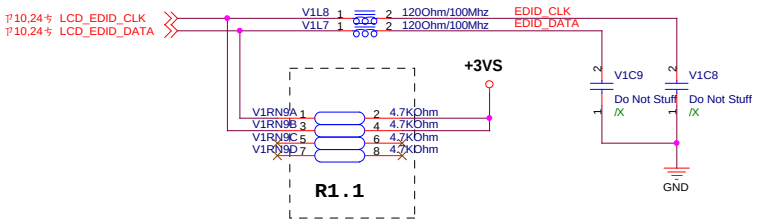


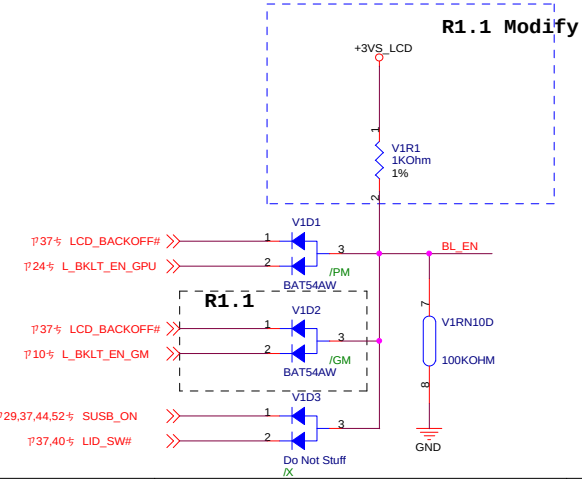
LVDS from GM

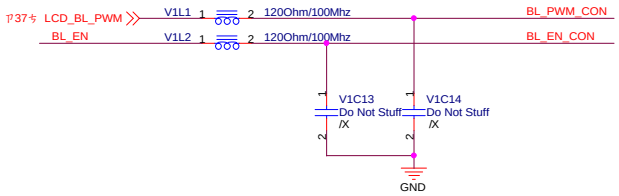


LVDS from GPU





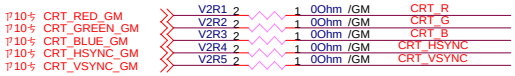




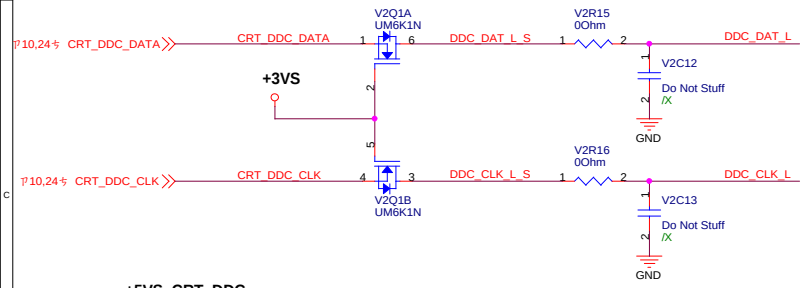
P80VC1

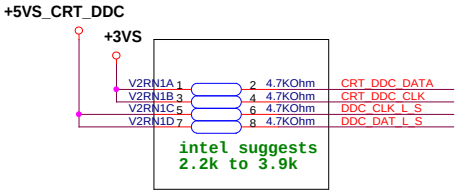
ASUSTeK COMPUTER INC. NB6	Title : LVDS conn	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 27 of 52	

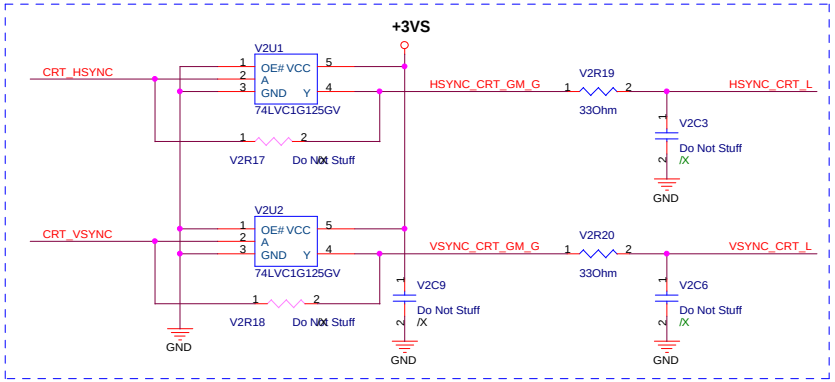
From GMCH



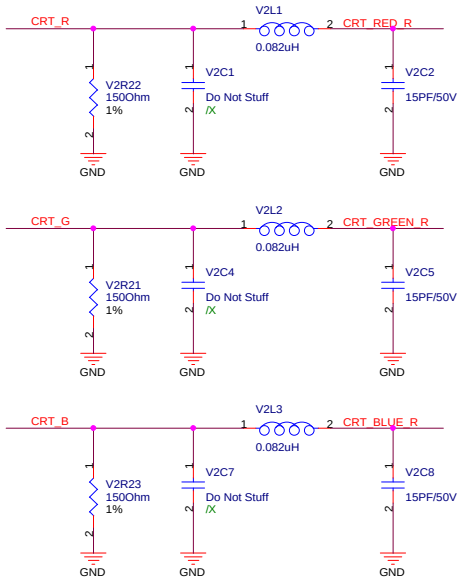
From GPU





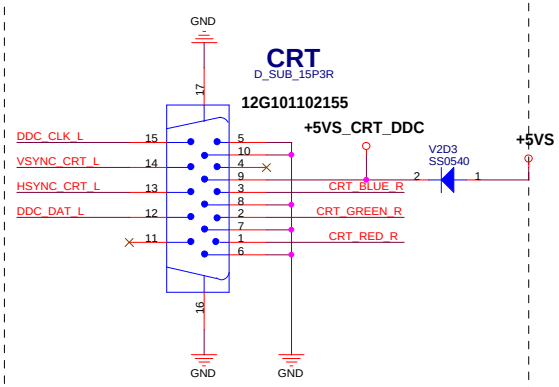


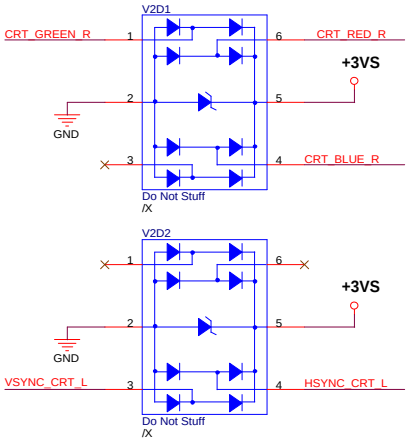
2008/12/4 : Pass EA measurement



R1.1 change P/N

CRT Connector





ESD Diodes

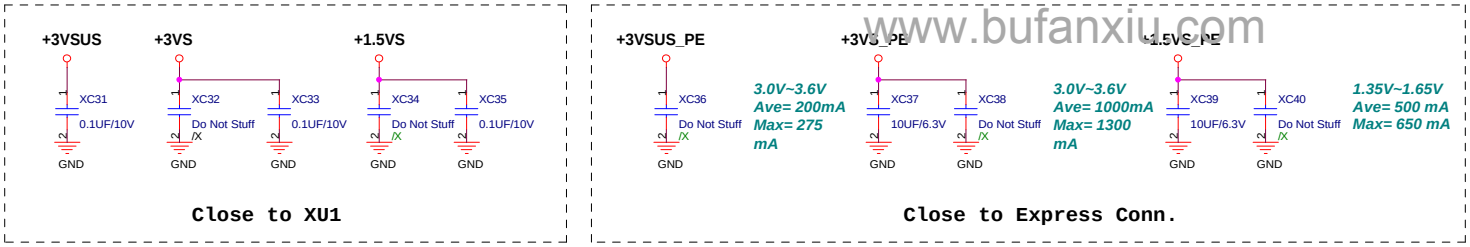
Place ESD Diodes near CRT Connector

R1.1 /X

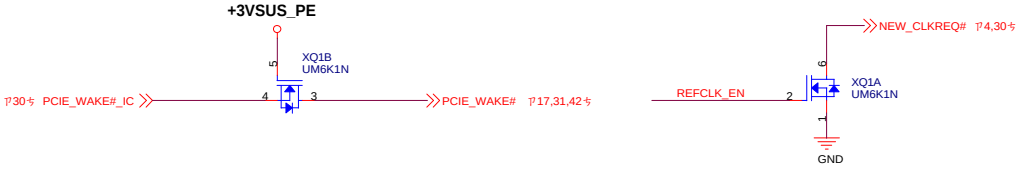
P80VC1

ASUSTeK COMPUTER INC. NB6	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A / Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 28 of 52	

Title : CRT conn

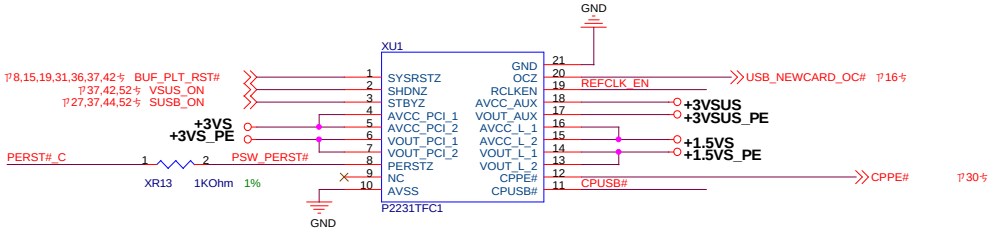


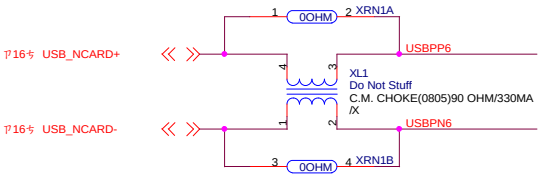
NewCard Header

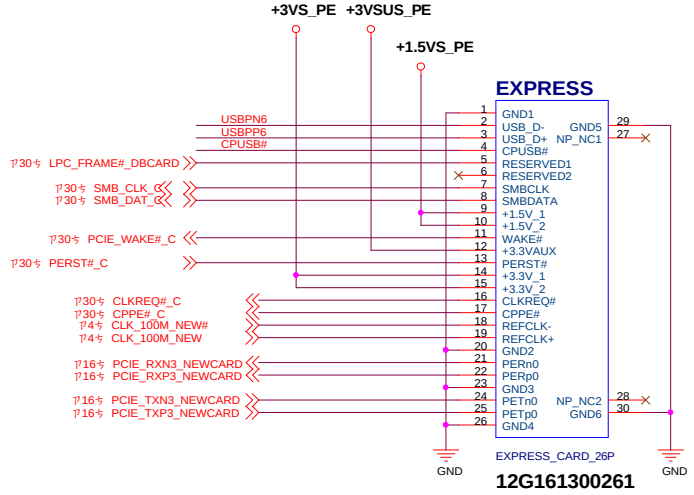


06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1

06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2



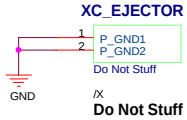




12G161300261

ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector



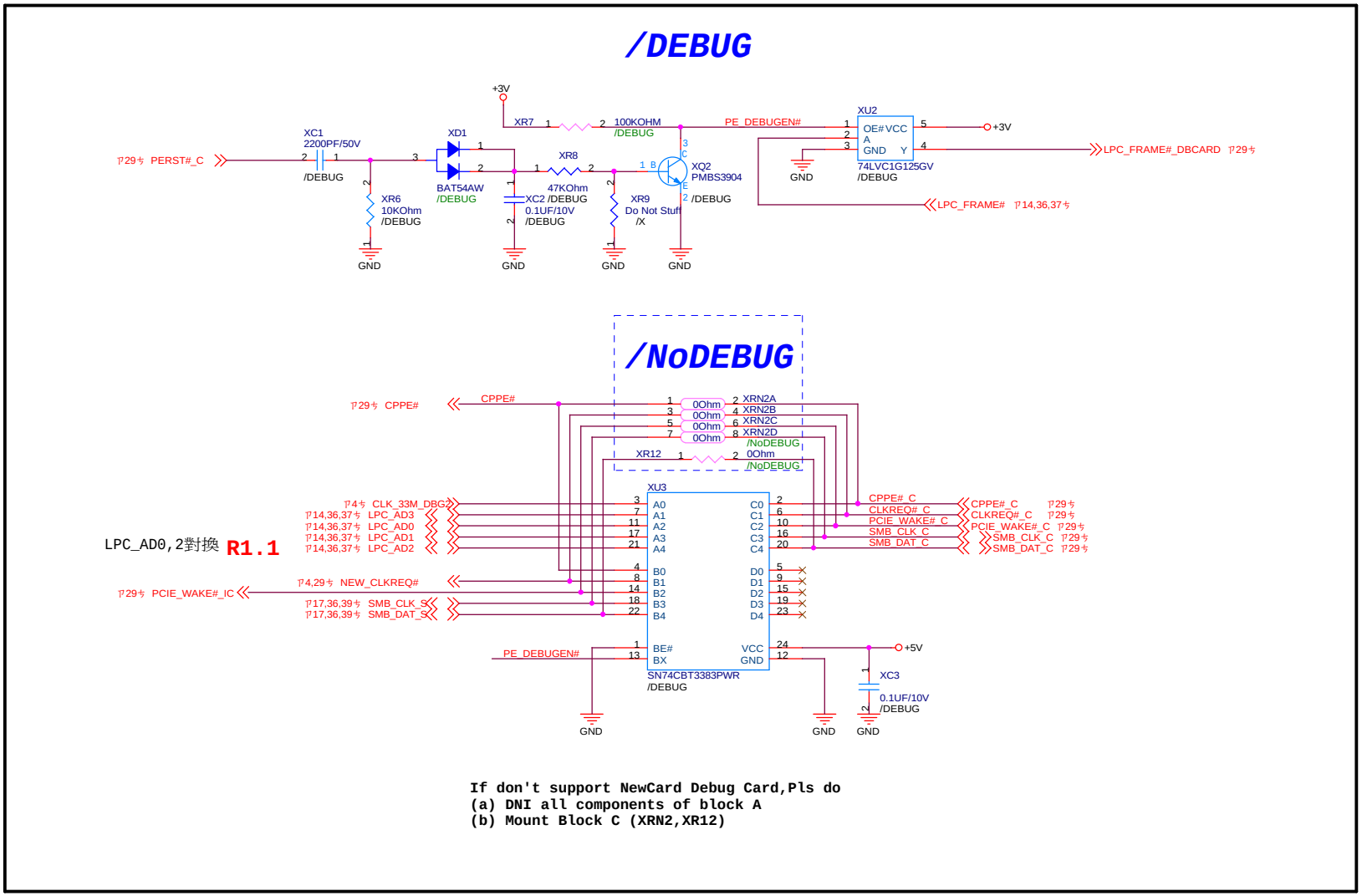
P80VC1

Title : NEWCARD

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 29 of 52



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : NEWCARD_DEBUG	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 30 of 52	

+3VSUS
LC10 0.1UF/16V
LC11 0.1UF/16V
LC12 0.1UF/16V
GND

For VDD33 pin29, pin37

+3VSUS
LL1 120Ohm/100Mhz
AVDD33_LAN
LC7 0.1UF/16V
LC8 0.1UF/16V
GND

For AVDD33 pin1, pin40

+1.2VOUT
Wider than 60mils
LL2 4.7UH
EVDD12
LC16 22UF/6.3V
LC9 0.1UF/16V
LC19 0.1UF/16V
GND
DVDD12
LC20 0.1UF/16V
LC17 0.1UF/16V
LC21 0.1UF/16V
LC22 0.1UF/16V
LC18 0.1UF/16V
LC23 0.1UF/16V
GND

Note 1: The Trace length between LL2 and 8111DL's Pin 48 must be within 0.5 cm. LC9 and LC16 to LL2 must be within 0.5cm. Refer to Layout guide for more detail.

Pass EA measurement

LR16 Do Not Stuff /X
GLAN_XTAL1 LX1 GLAN_XTAL2
25Mhz +/-30ppm/18PF
LC24 27PF/50V
LC25 27PF/50V
GND

+3VSUS
LC5 22UF/6.3V
LC6 0.1UF/16V
GND

Note : Regulator input,the Trace length between LC5 and 8111DL's Pin 44,45 must be within200mils and wider than 40mils

+3VSUS
GND LR12 2.49KOhm 1%
LC4 Do Not Stuff/X
GND

Remove LR11 if switching regulator is enabled.
Remove LR14 if external power 1.2V is used.

+1.2VOUT
GLAN_REST
AVDD33_LAN
DVDD12
+3VSUS
TP935
GND
GLAN_XTAL2
GLAN_XTAL1

+3VSUS
LR9 1KOhm 1%
LR10 Do Not Stuff 1% /X
LU2
EECS EESK EEDI EEDO
CS SK DI DO VCC DC ORG GND
Do Not Stuff /X
+3VSUS
LC3 Do Not Stuff /X
GND

DVDD12
AVDD33_LAN
LU1
SROUT12 GND4 RSET VDDSR2 VDDSR CKTAL2 CKTAL1 AVDD33_2 AVDD12_2 LED0 VDD33_2
AVDD33_1 MDIP0 MDIN0 FB12 MDIP1 MDIN1 GND1 MDIP2 MDIN2 AVDD12_1 MDIP3 MDIN3
DVDD12_3 LED1/EESK LED2/EEDI/AUX LED3/EEDO EECS GND3 DVDD12_4 VDD33_1 ISOLATEB PERSTB LANWAKEB CLKREQB
EESK EEDI EEDO EECS GND ISOLATE#
BUF_PLT_RST# 8,15,19,29,37,42
PCIE_WAKE# 17,29,42
LAN_CLKREQ# 4
LR6 Do Not Stuff
GND
DVDD12_2 GND2 HSIP HSIN PCIECLK_P PCIECLK_N EVDD12 HSOP HSON EGND GPO NC7
RTL8111DL-GR

+3VS
LR18 1KOhm 1%
GLAN_ISOLATE# 17
LR19 15KOhm 1%
GND

EVDD12
DVDD12
LR2 0Ohm
RJ45_DET# 17
LR1 0Ohm
GND

PCIE_TXP1_LAN 16
PCIE_TXN1_LAN 16
CLK_PCIE_LAN 4
CLK_PCIE_LAN# 4
PCIE_RXP1_LAN 16
PCIE_RXN1_LAN 16
LC1 0.1UF/10V
LC2 0.1UF/10V
PCIE_RXP1_LAN_C
PCIE_RXN1_LAN_C

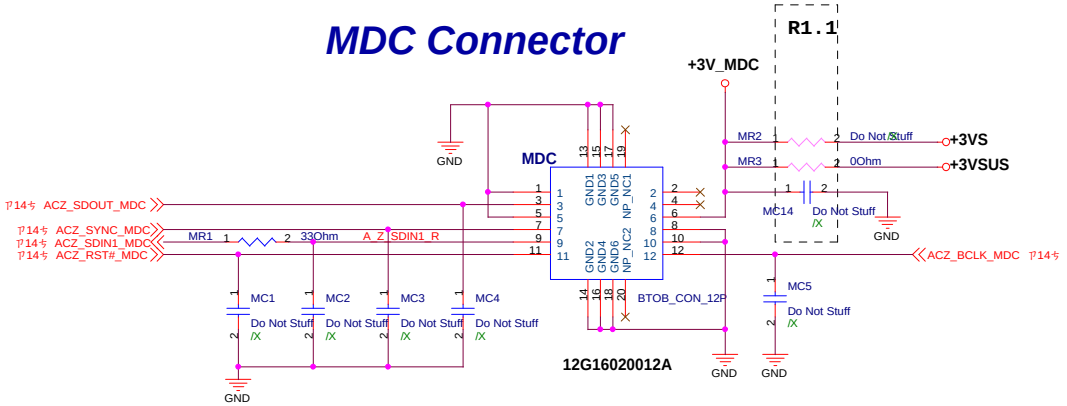
RTLAN_DSM#: ICH9 GPIO10
GLAN_DSMEN:ICH9 GPIO60

P80VC1

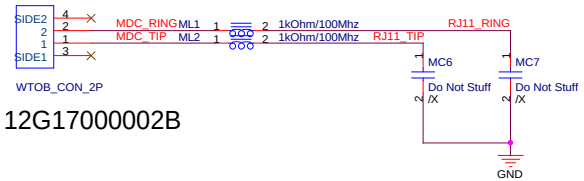
ASUSTeK COMPUTER INC. NB1

Title : SB-ICH9M(3)
Engineer: SZ_NB2
Size: Custom
Project Name: P80VC / A/ Q
Rev: R1.1
Date: Tuesday, December 16, 2008
Sheet 31 of 52

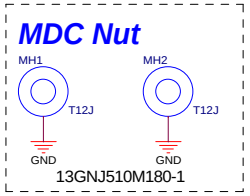
MDC Connector



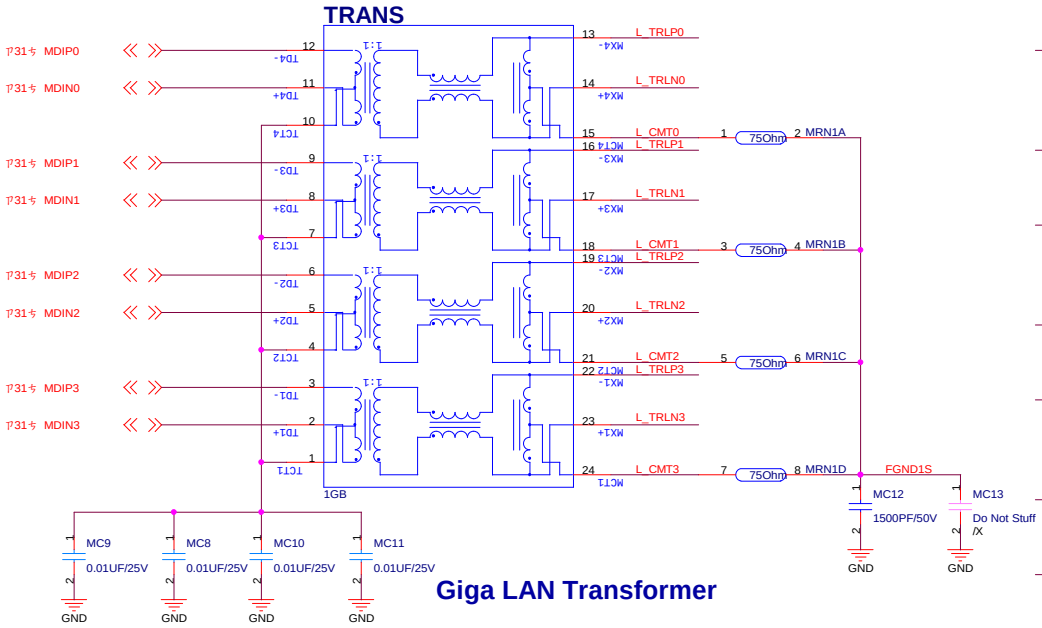
RING



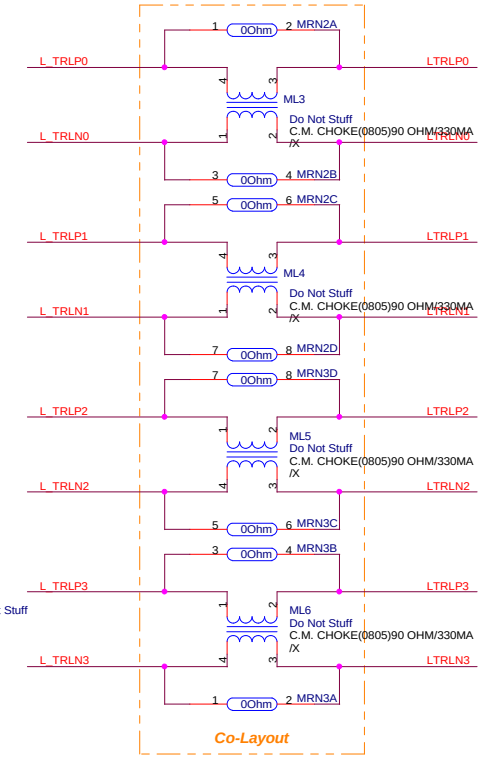
MDC Nut



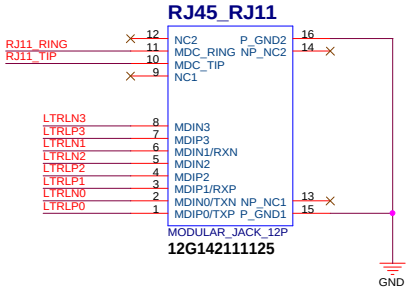
TRANS



Giga LAN Transformer



RJ45_RJ11



P80VC1

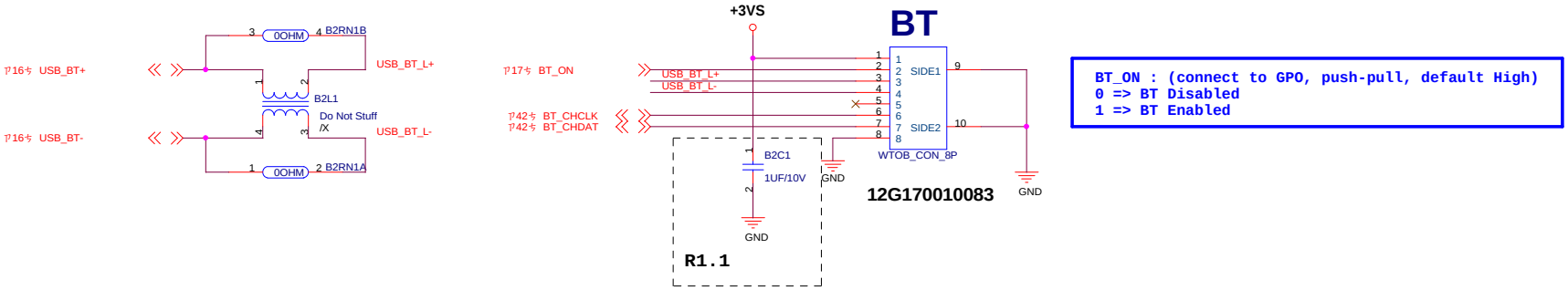
ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Title : RJ45-11&MDC

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 32 of 52

Bluetooth Connector



BT_ON : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

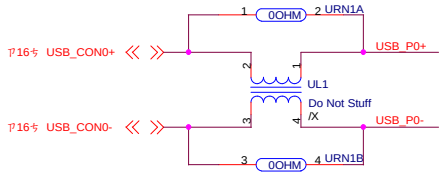
P80VC1

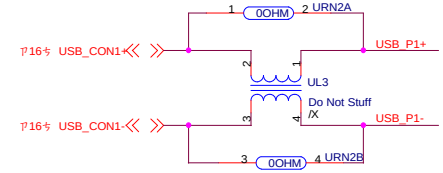
Title : BT&Launch

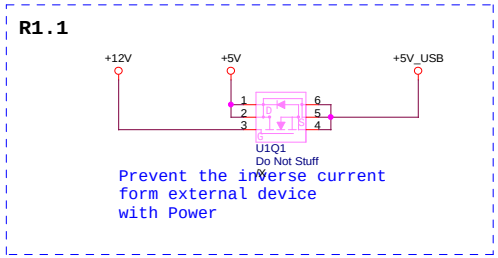
ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

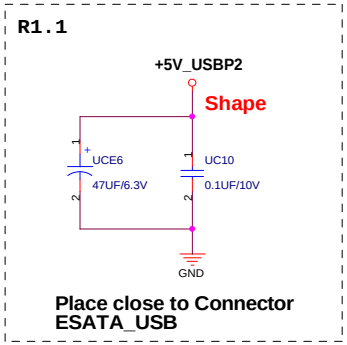
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

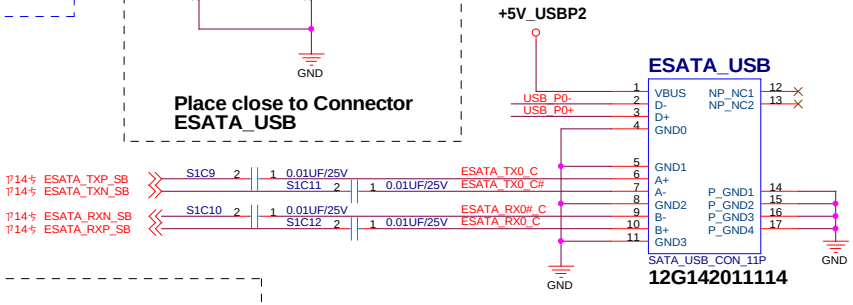
Date: Tuesday, December 16, 2008 Sheet 33 of 52

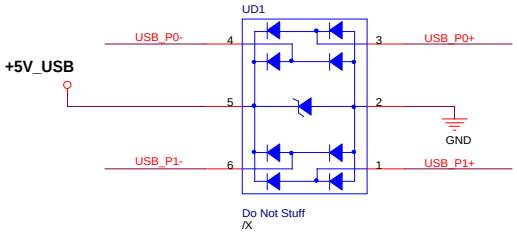


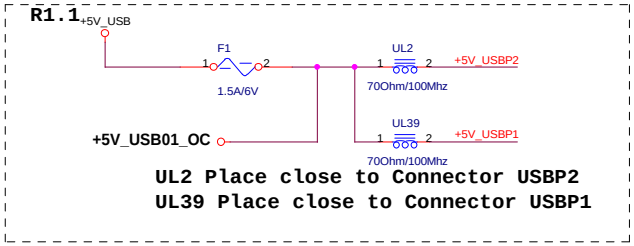


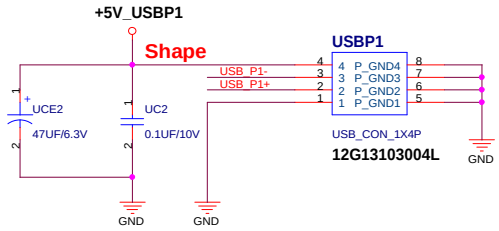








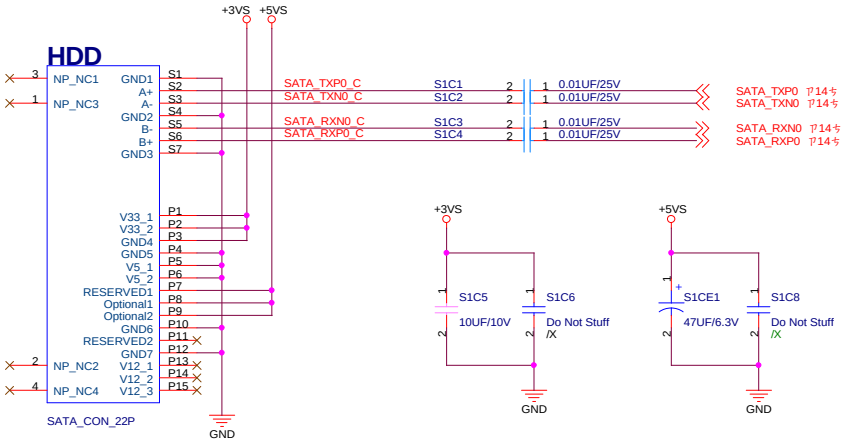




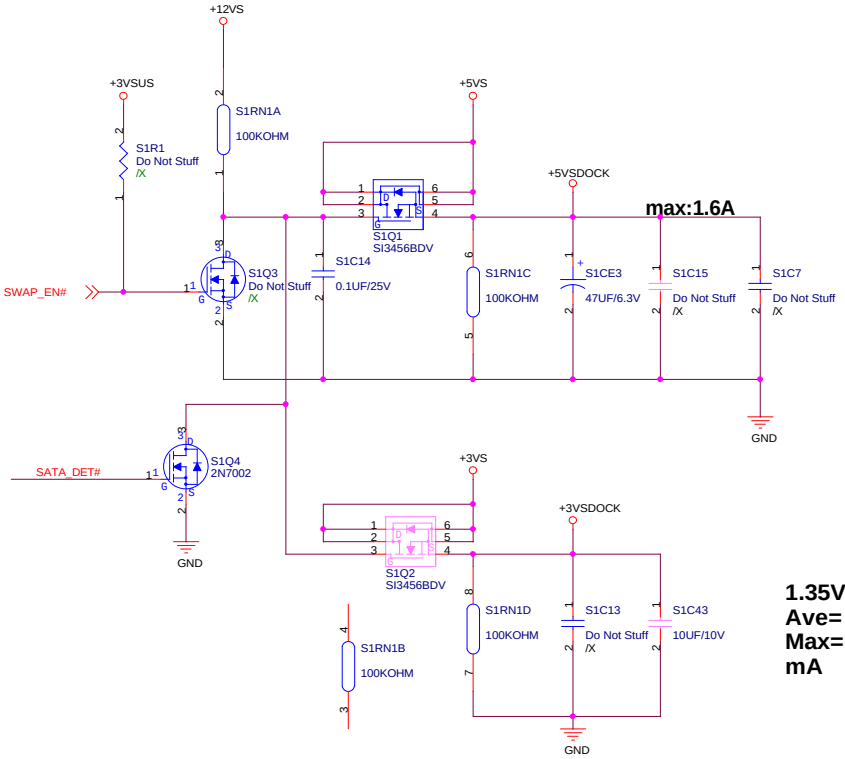
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Audio Brd con&USB x2	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 34 of 52	

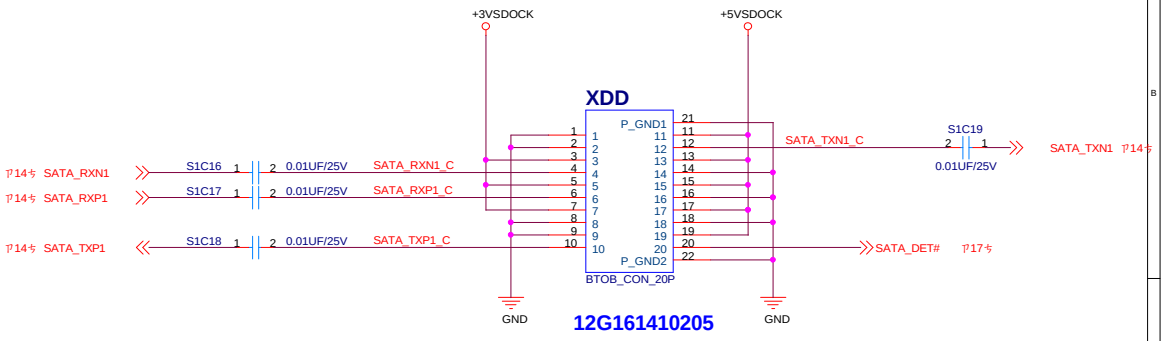
SATA HDD Connector



12G150200221



1.35V~1.65V
Ave= 500 mA
Max= 650
mA

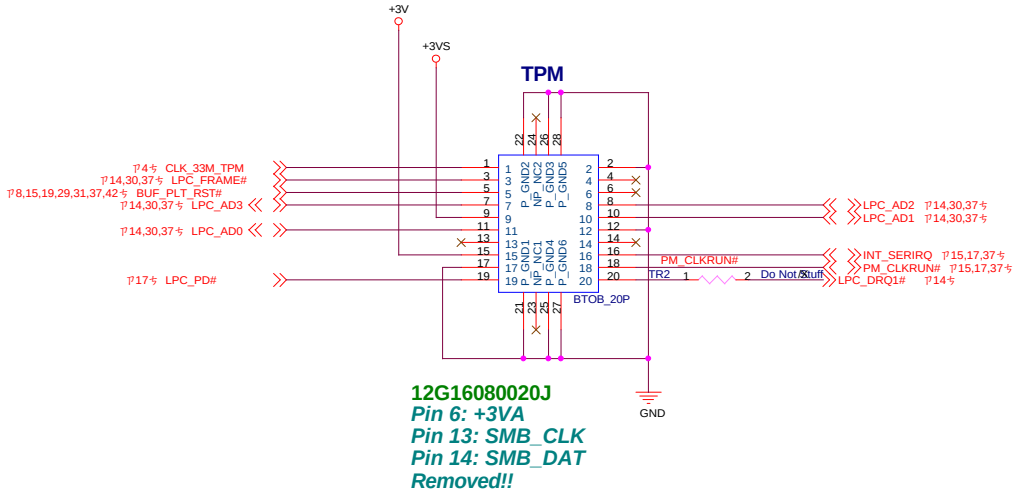


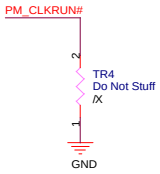
12G161410205

P80VC1

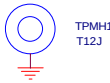
ASUSTeK COMPUTER INC. NB6	Title : SATA HDD	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 35 of 52	

TPM Connector



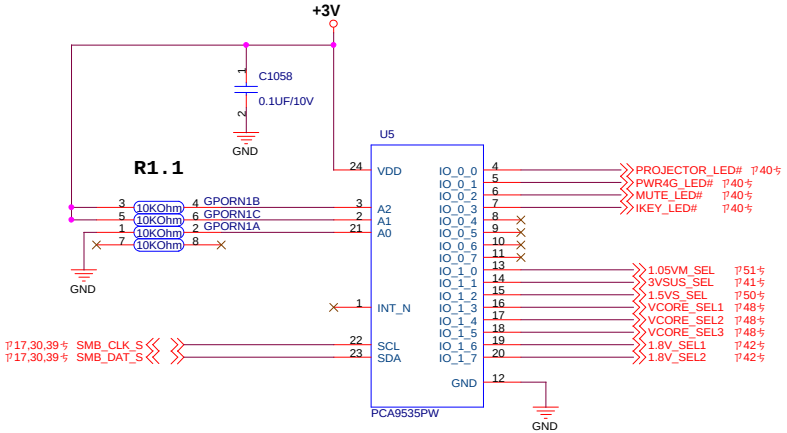


TPM Nut



13GNJ510M190-1

I2C GPIO Controller



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Debug&TPM&GPIO	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 36 of 52	

For Discrete VGA

ZU1 — IT8752E_L

R1.1 Add power Limit

SUSC_ON:For iAMT, only used to turn on +1.8V

R1.1 del learn ?

For iAMT, used to turn on +12V,+5V,+3V

For IT8512 Power

R1.1 POWER GOOD DETECT

ALL_SYSTEM_PWRGD → ZD2 BAT54AW → +1.5VS_PWRGD, NV_PWRGD_VGA
ZD3 BAT54AW → +1.8V_PWRGD, DDR_PWRGD
iAMT_+1.05VM_+3VM_PG → ZD4 BAT54AW → +1.05VM_PWRGD, +3VM_PWRGD

For EC Reset

close to the WRST# (IT8752E pin19)

Oringinal R = 160K OHM

For PU / PD

R1.1

For X'tal

Note:
Cload=12.5PF
place close to EC

ZX1 32.768kHz +/-20ppm/12.5PF

ZU3 SST25VF080B (8Mb)

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

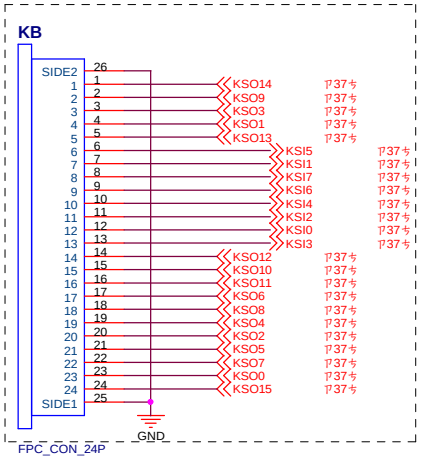
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

P80VC1

ASUSTeK COMPUTER INC. NB1

Title : EC ENE3925
Engineer: SZ_NB2
Size: Custom
Project Name: P80VC / A/ Q
Rev: R1.1
Date: Tuesday, December 16, 2008
Sheet 37 of 52

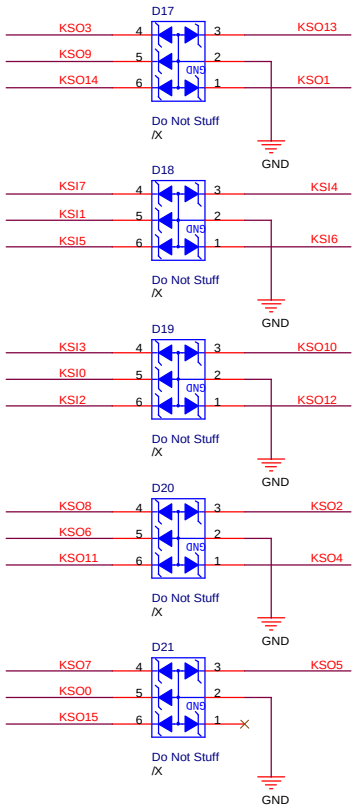
Keyboard Connector

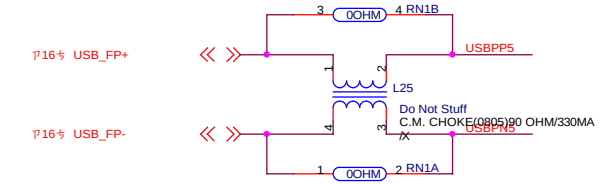


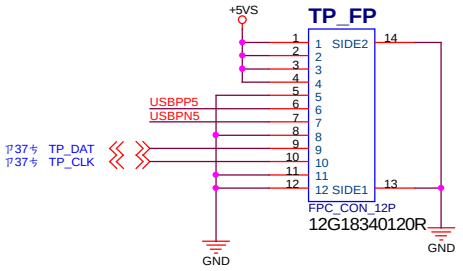
12G182102402

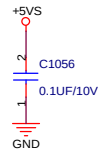
R1.1

FOR EMI/ESD

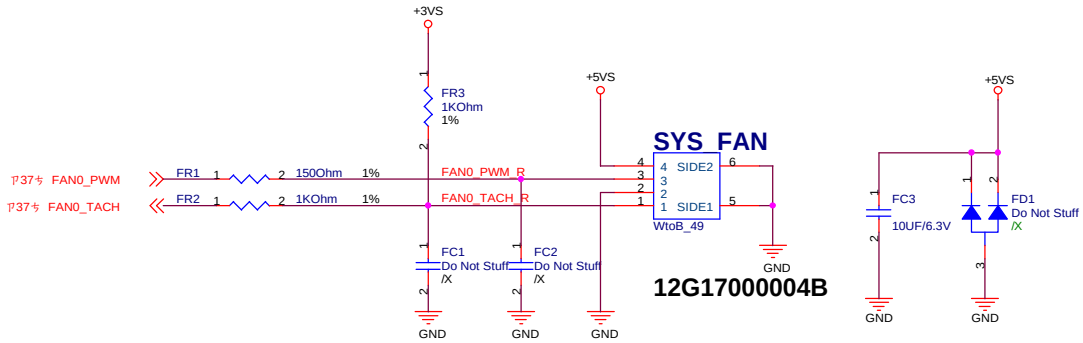








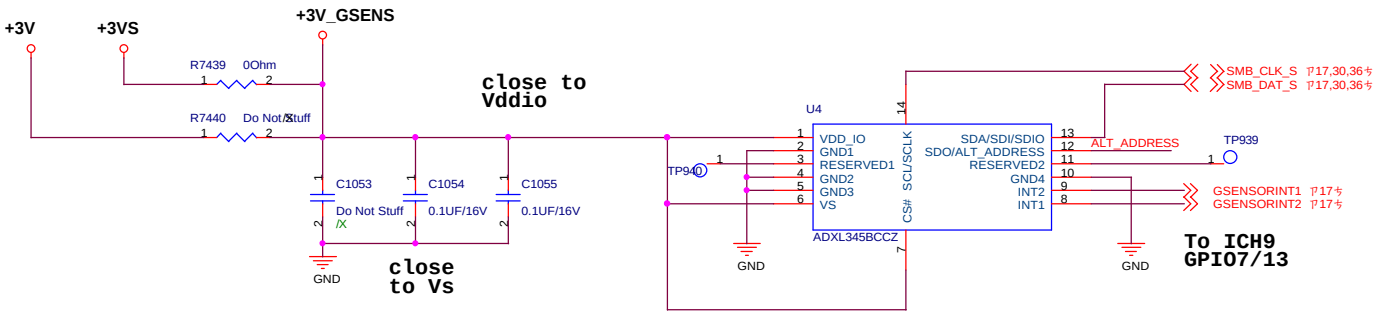
Place close to connector



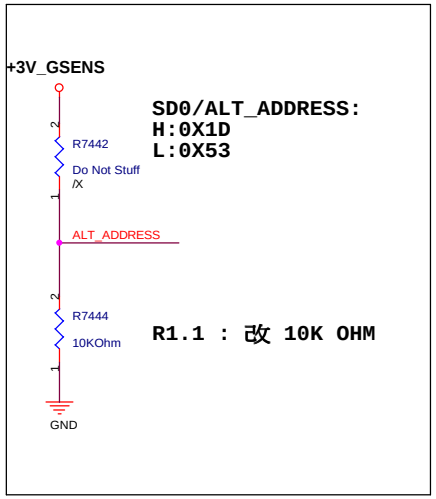
12G17000004B

P80VC1

ASUSTeK COMPUTER INC. NB6	Title : KB—TP	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 38 of 52	



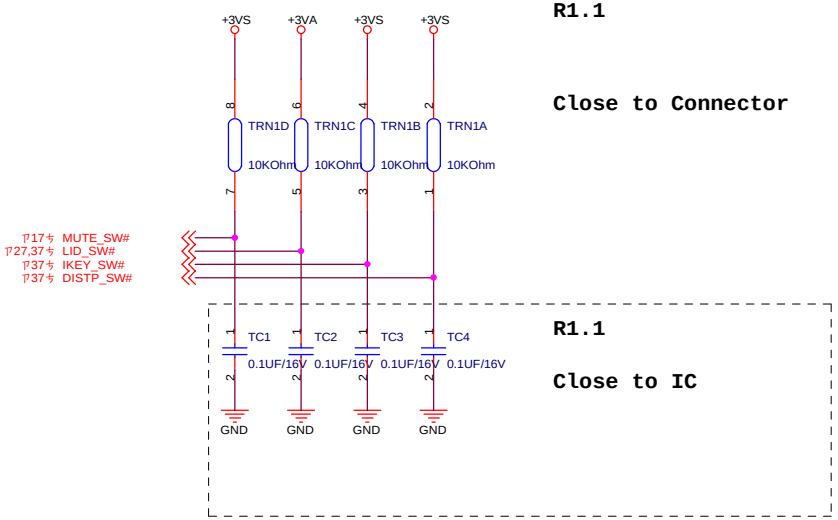
RESERVED
PIN3: connect to Vs or NC
PIN11: connect to GND or NC
CS#: Tie to Vddio to enable I2C mode.

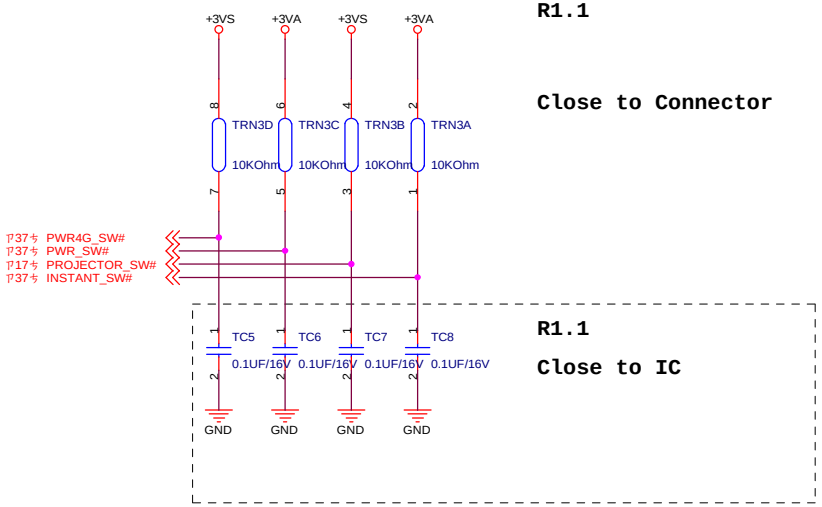


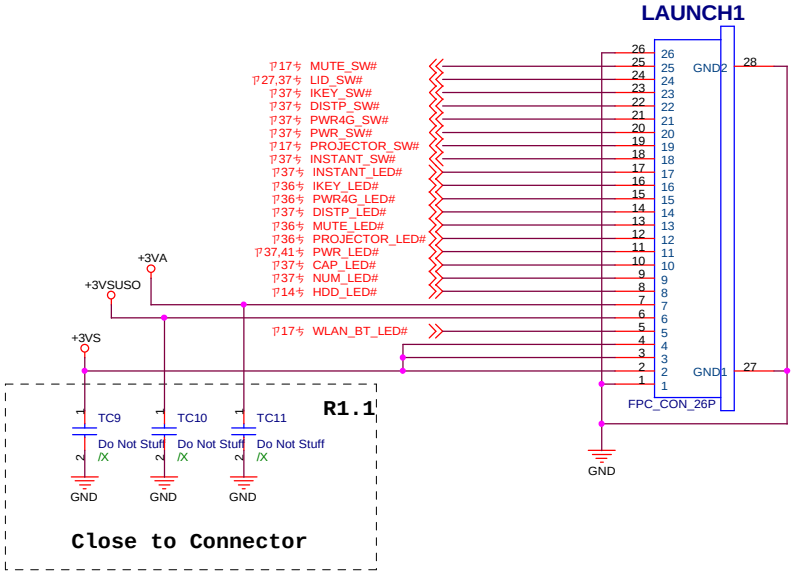
P80VC1

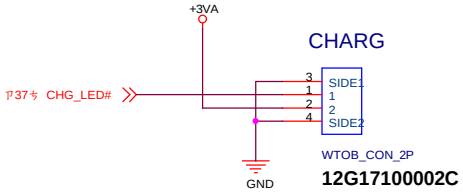
ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 39 of 52	

Debounced Circuits



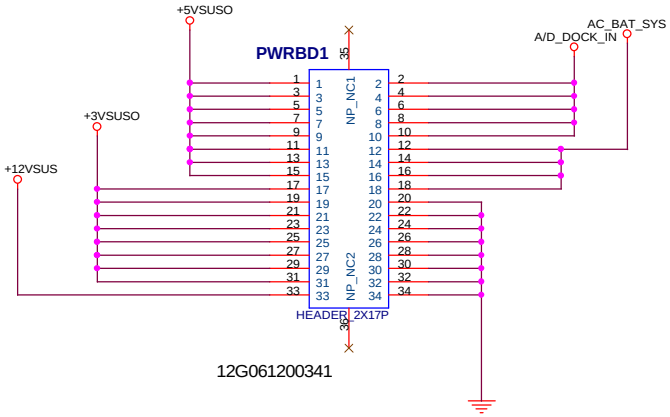




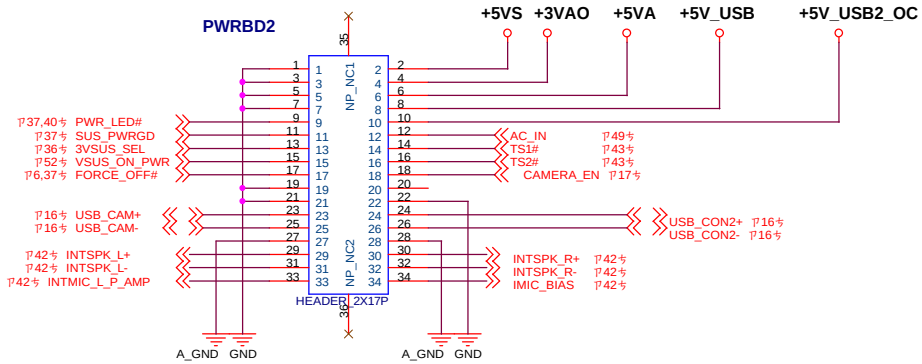


P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 40 of 52	



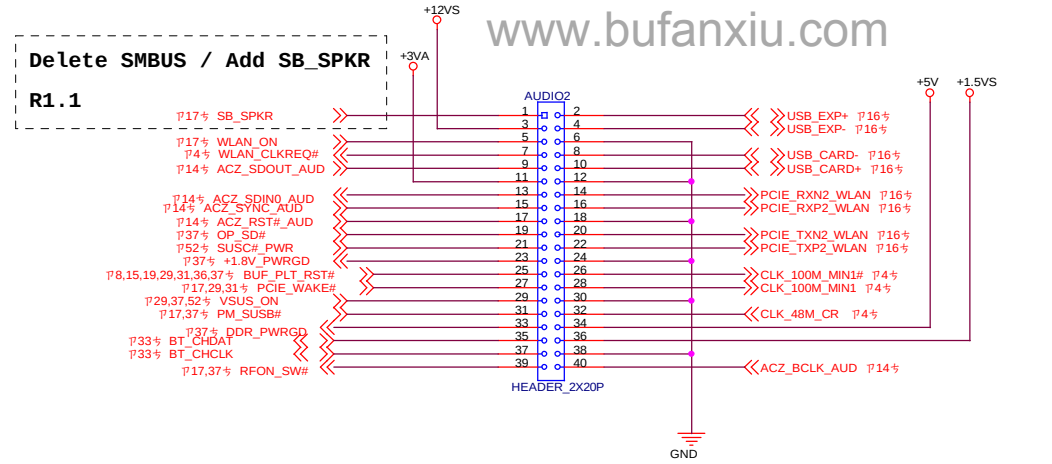
12G061200341

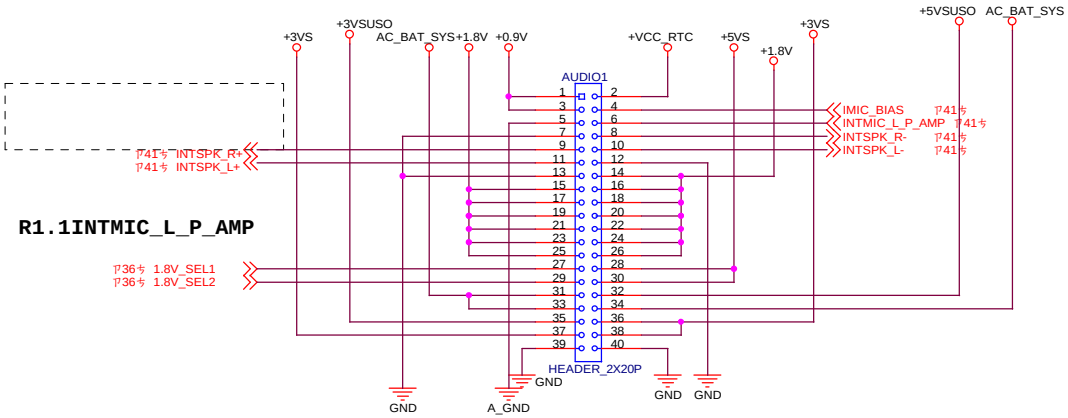


12G061200341

P80VC1

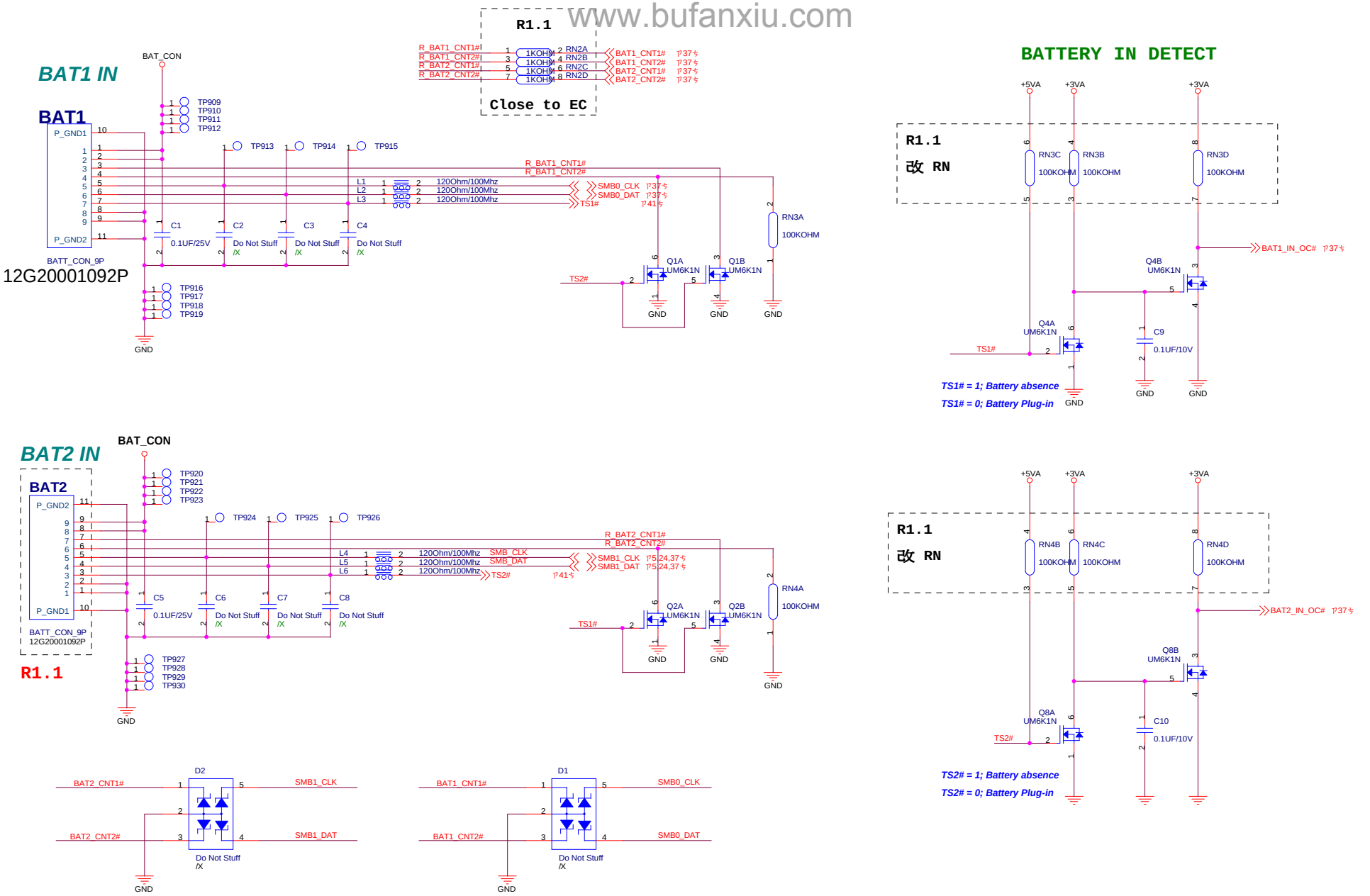
ASUSTeK COMPUTER INC. NB6	Title : other	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 41 of 52	





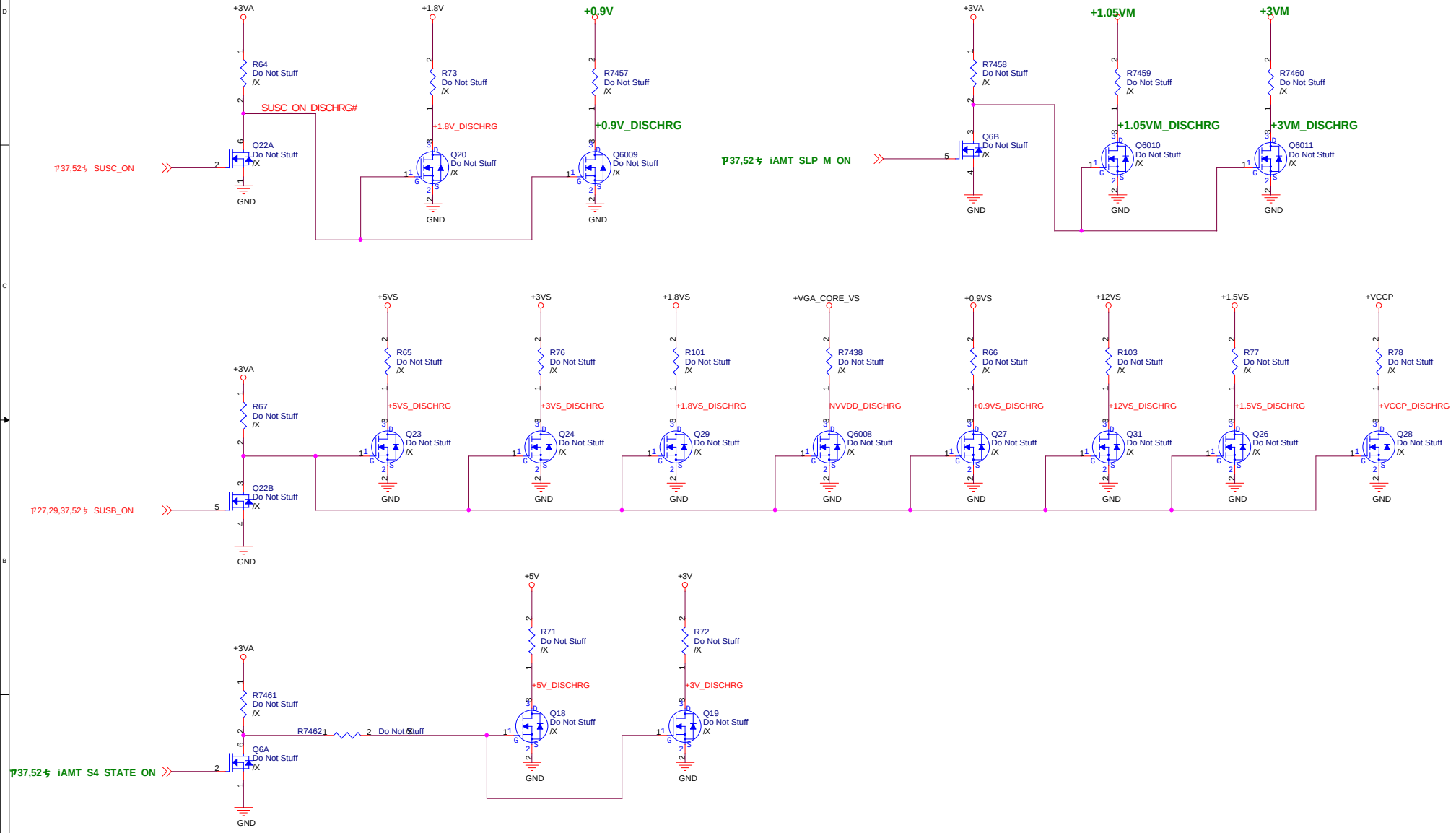
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : other	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 42 of 52	



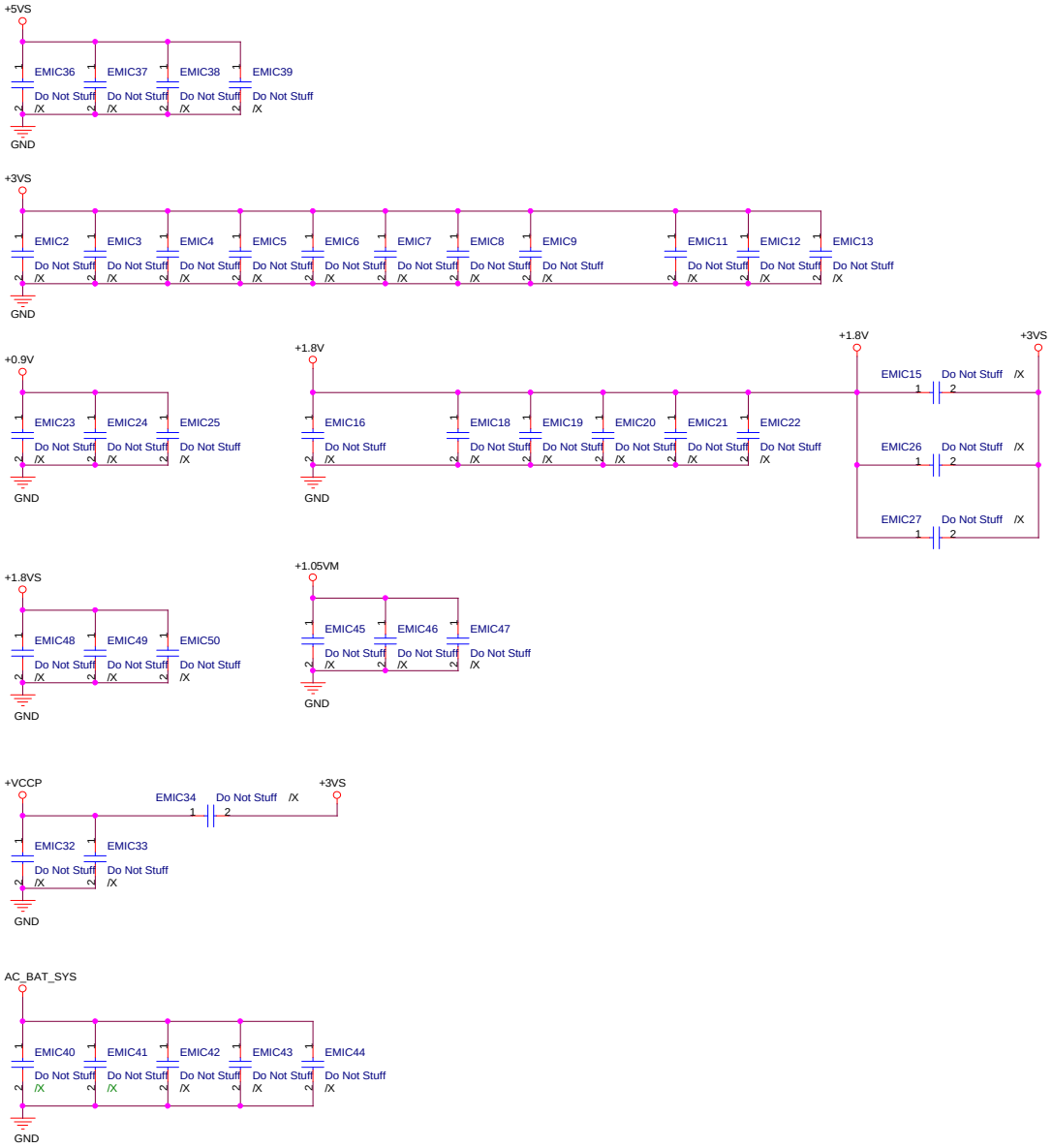
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : DC-IN&BAT-IN	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 43 of 52	



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Discharger	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A / Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 44 of 52	



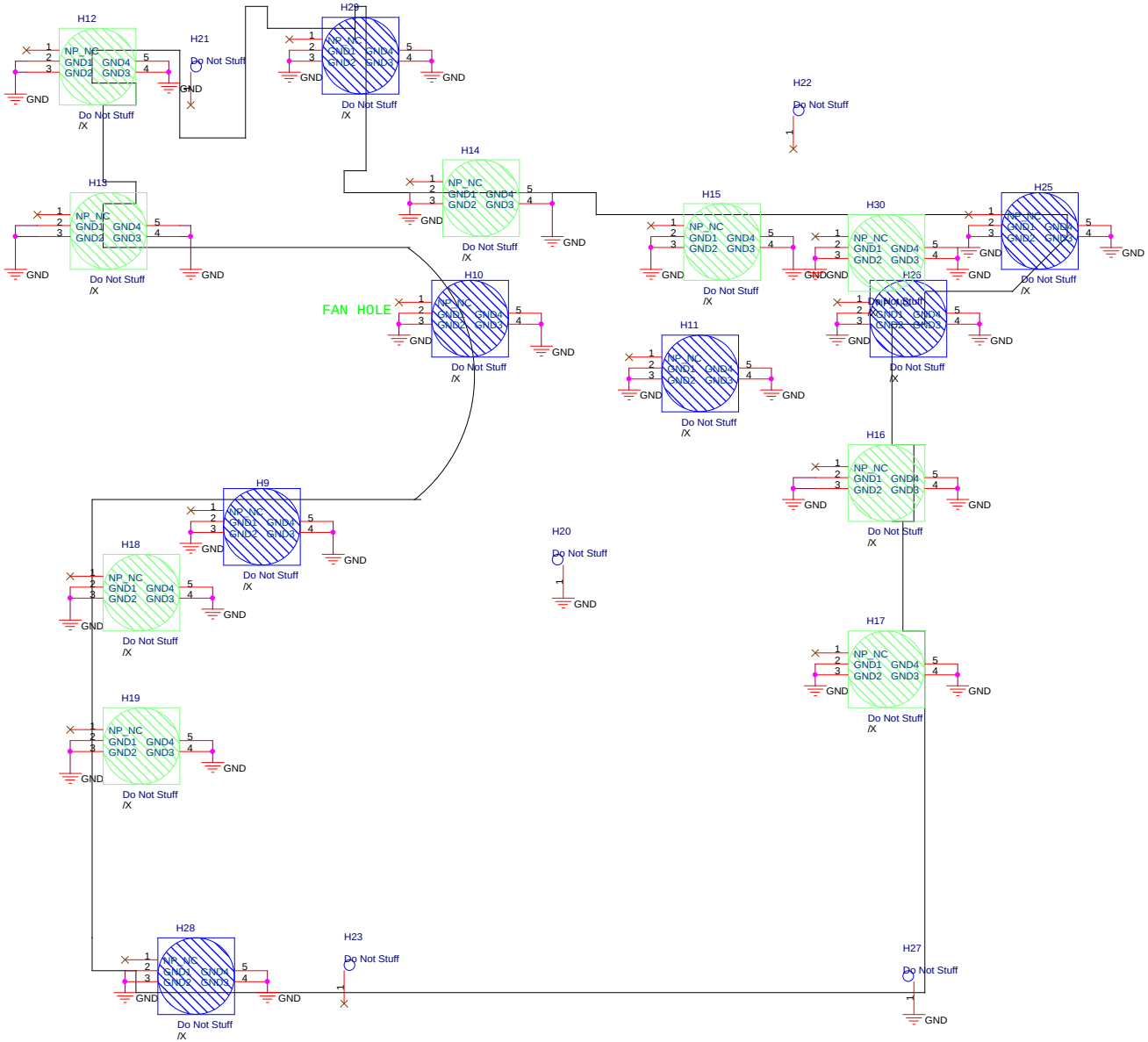
P80VC1

Title : EMI CAP

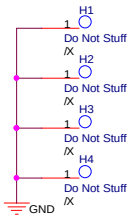
ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

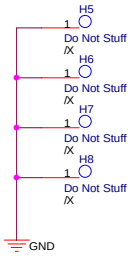
Date: Tuesday, December 16, 2008 Sheet 45 of 52



CPU HOLE

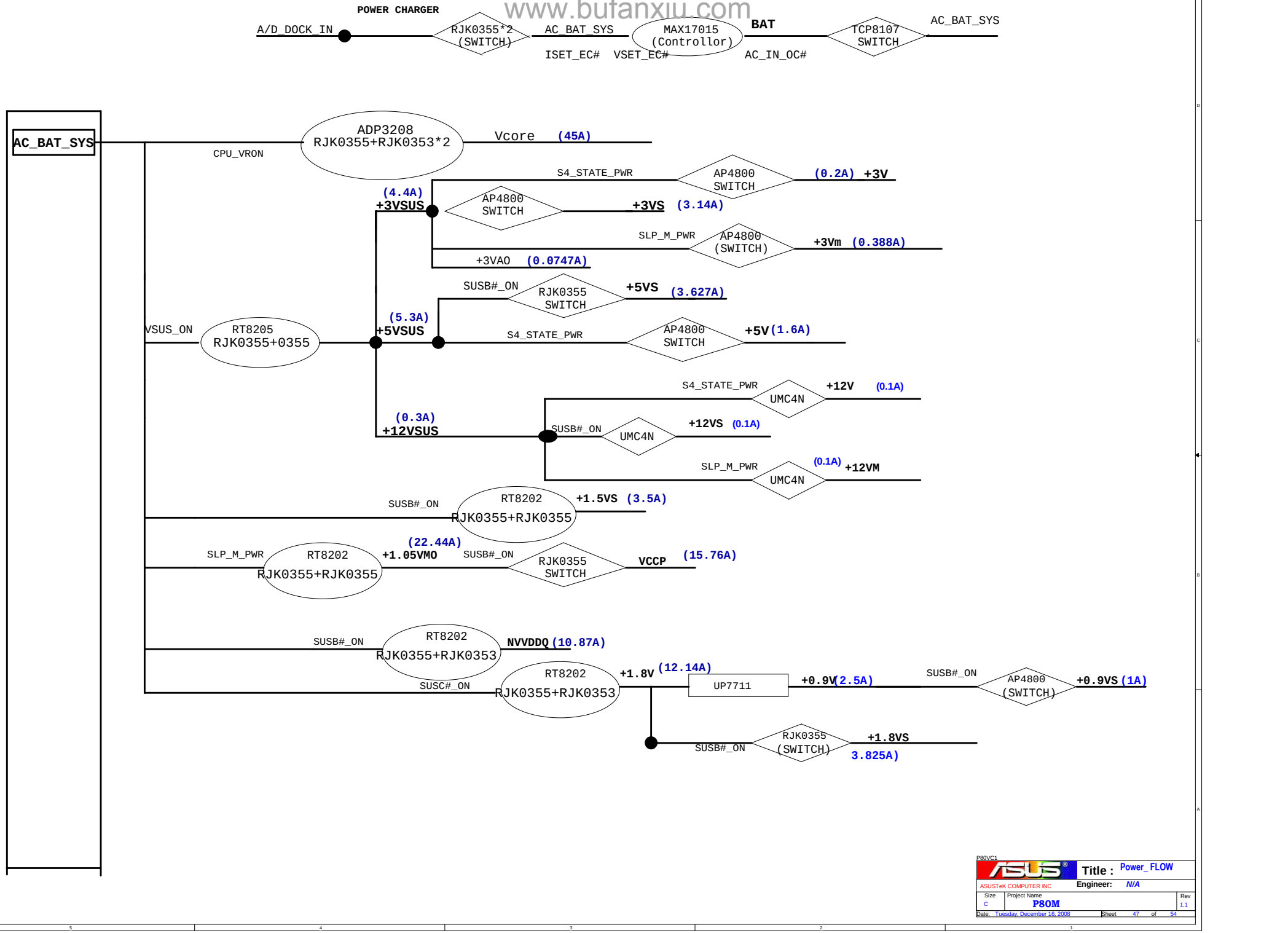


NB+GPU HOLE



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Screw Hole	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 46 of 52	



P80VC1

Title : Power_ FLOW

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
C	P80M	1.1

Date: Tuesday, December 16, 2008 Sheet 47 of 54

Power stage

1. **I/P Current:**
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. **Ripple Current:**
   Iripple=3A
3. **Ripple Voltage:**
   Vripple=Iripple*ESR=13.5mV
4. **Dynamic:**
   Ipeak=45A
   ESR=4.5mohm
   V=100mV
5. **Inductor Spec:**
   Isat=26A
   Idc=20.8A
   Rdcmax=1.09mOhm
   Rdcmtyp=1.02mOhm
6. **MOSFET Spec:**
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=4.5V)
   Icont=30/35A (T=25)/
   Ipeak=120/140A (Pause<10us)

Controller

1. **Voltage & Current:**
   +VCORE:1.1V/45A
2. **Frequency:**
   Setting the clock Frequency:
   RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
   Fsw=2.05V/(4*7.2pF*235Kohm)=303K
3. **OCP:**
   DCR*Imax*R2/(R1+R2)=22.5mV
   Imax=10.87A
4. **tss time:**
   TSS=1.8ms TSt=1.8ms
5. **LoadLine:**
   Out Droop Resistance :
   Ro=Rcs*Rsense/Rph
   =206.69Kohm*1.02mohm/120Kohm=1.76mohm

(45A)

VCORE_SEL1	VCORE_SEL2	VCORE_SEL3	Voltage
0	1	1	VID-100mV
1	0	1	VID-50mV
1	1	1	ViD
1	1	0	VID+50mV

Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
I=78.38A

Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K

Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm

P80VC1

ASUSTek Computer INC.

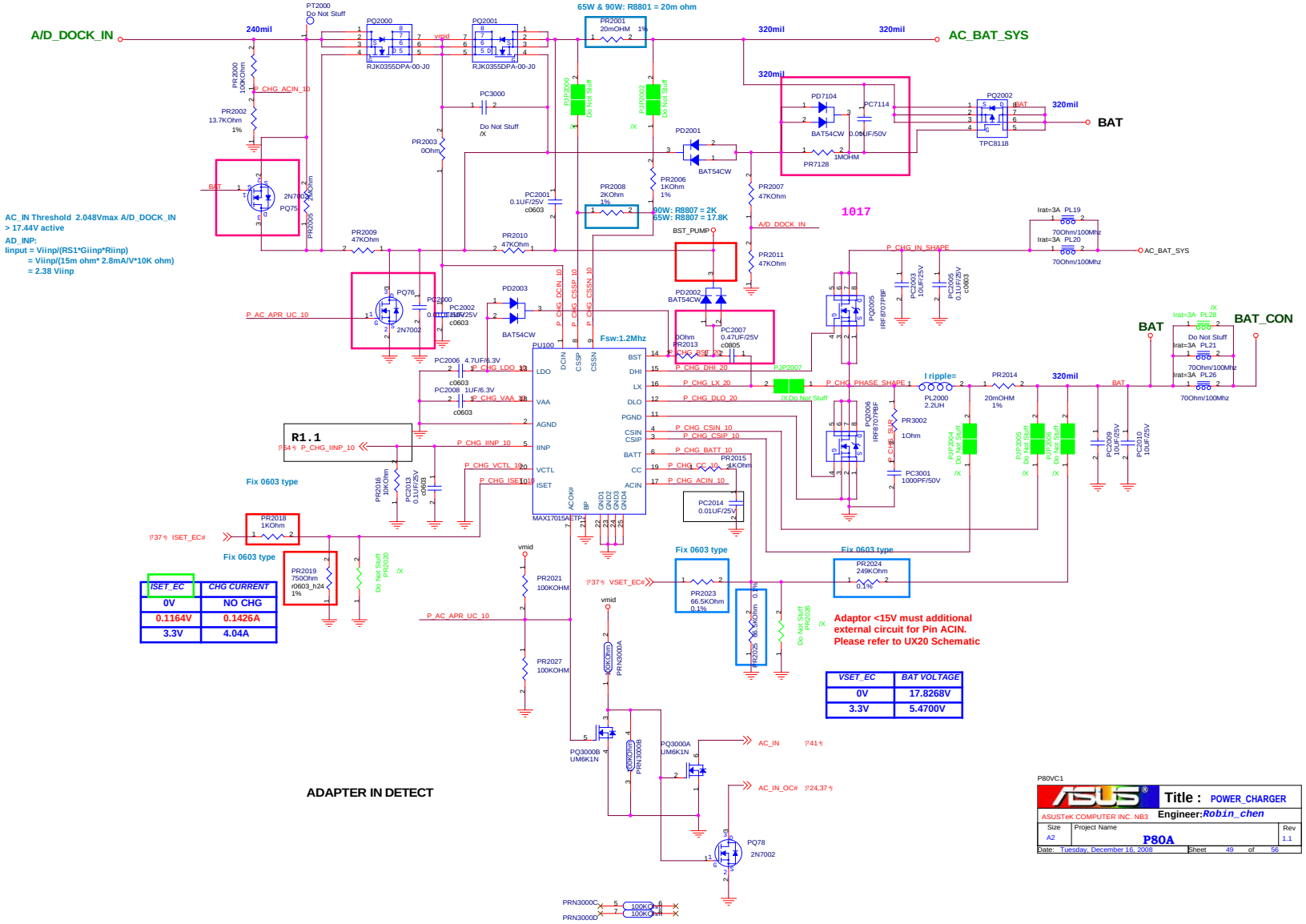
Title : POWER_VCORE

Engineer: Robin_chen

Size	Project Name	Rev
A2	P80	1.1

Date: Tuesday, December 16, 2008 Sheet 48 of 56

POWER PATH & BAT_LEARN



ISET_EC	CHG CURRENT
0V	NO CHG
0.1164V	0.1426A
3.3V	4.04A

VSET_EC	BAT VOLTAGE
0V	17.8268V
3.3V	5.4700V

Power stage

1. Ripple Current:
   Iripple=3A
2. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
3. MOSFET Spec:
   H-side and L-side MOSFET:AP4800
   Rds(on)=21mOhm (Vgs=4.5V)
   Icont=9.6 (T=25)
   Ipeak=40 (Pause<10us)

Controller

1. Frequency:
   1.2MHZ
2. Current limit
   4.5A(90W)
   3.16A(65W)

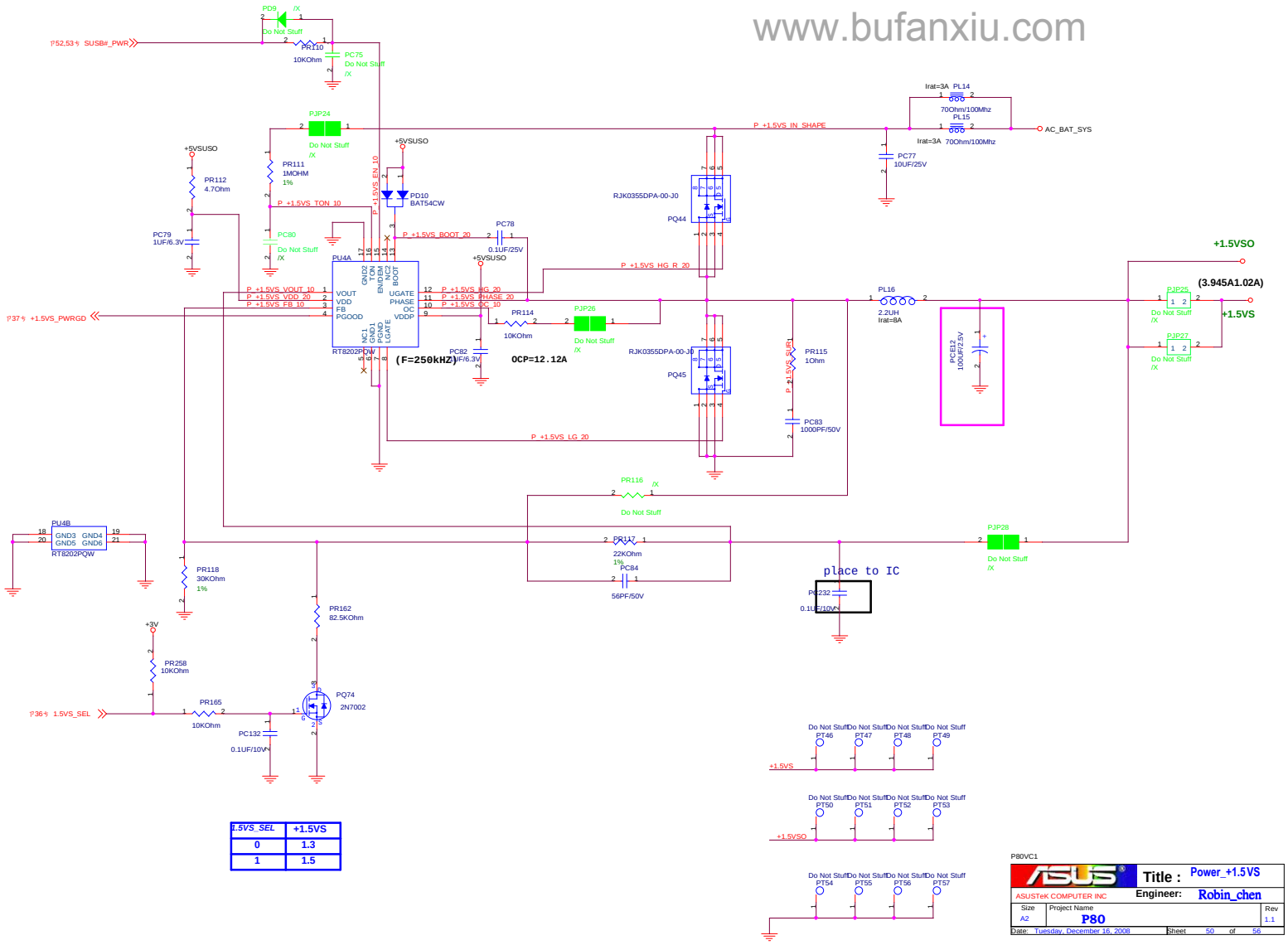
P80VC1

Title : POWER_CHARGER

ASUSTeK COMPUTER INC. NB3 Engineer:Robin_chen

Size	Project Name	Rev
A2	P80A	1.1

Date: Tuesday, December 16, 2008 Sheet 49 of 56



1.5VS_SEL	+1.5VS
0	1.3
1	1.5

Power stage

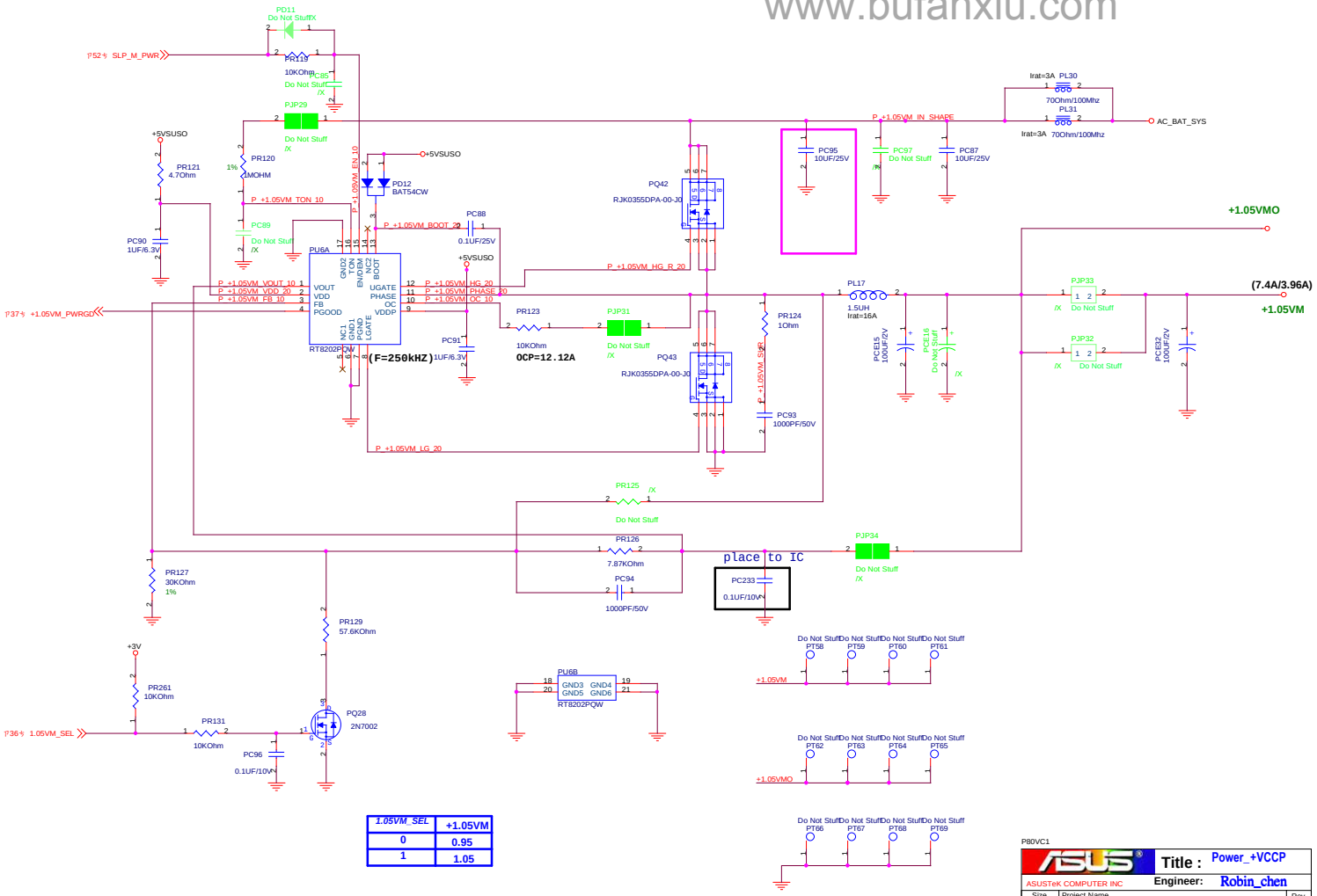
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.368A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=3.503A
   ESR/2=4.5mohm
   V=14.18mV
4. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30 (T=25)
   Ipeak=120 (Pause<10us)

Controller

1. Voltage & Current:
   +1.5V&3.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+1.5VS	
	Engineer: Robin_chen	
Size: A2	Project Name: P80	Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 50 of 56	



1.05VM_SEL	+1.05VM
0	0.95
1	1.05

Power stage

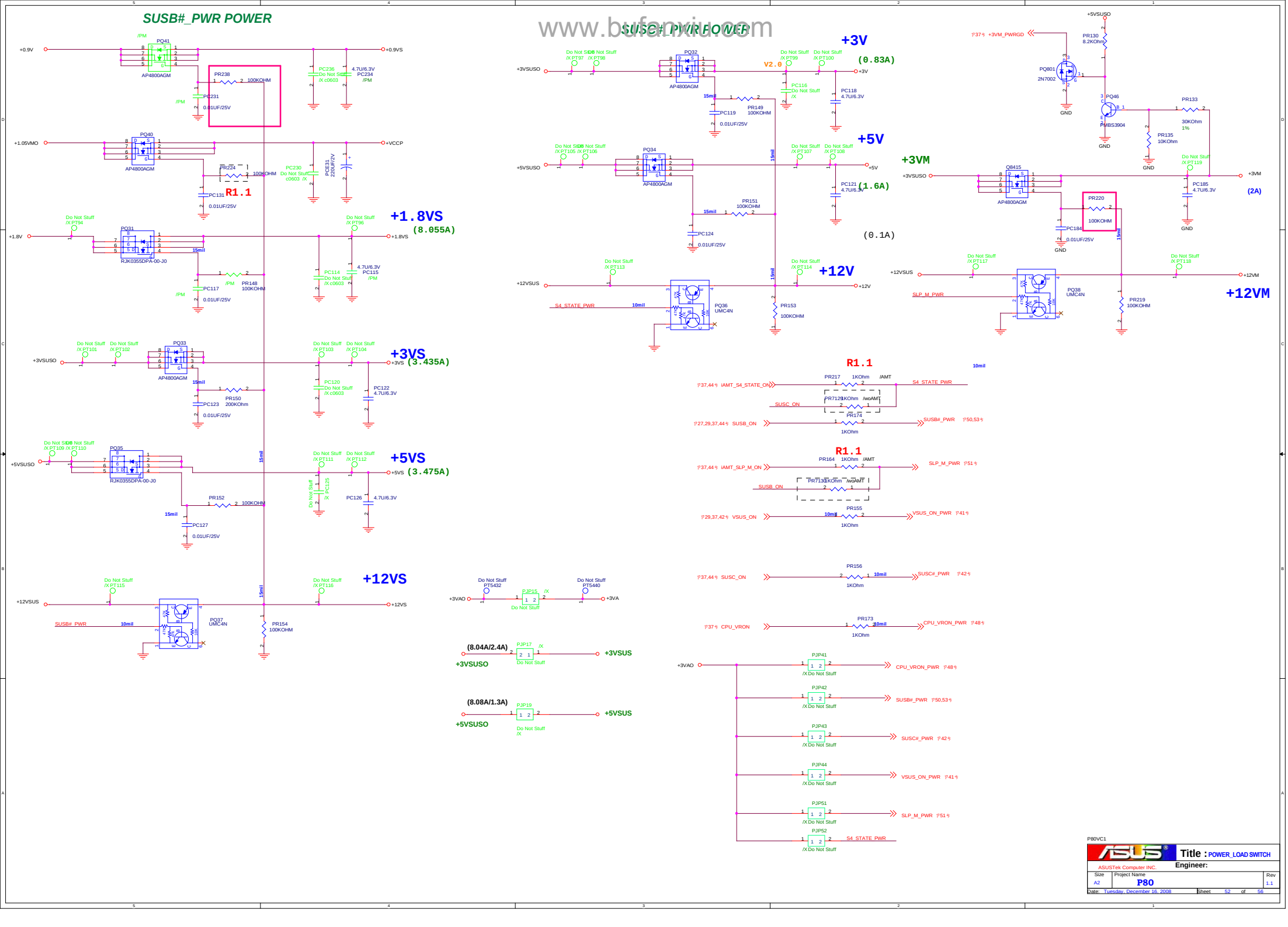
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.65A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=22.44A
   ESR/2=9mohm
   V=162mV
4. Inductor Spec:
   Isat=33A
   Idc=16A
   DCR=3.8mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30 (T=25)
   Ipeak=120 (Pause<10us)

Controller

1. Voltage & Current:
   +1.05V&22.44A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+VCCP		
	Engineer: Robin_chen		
Size: A2	Project Name: P80		Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 51 of 56		



P80VC1

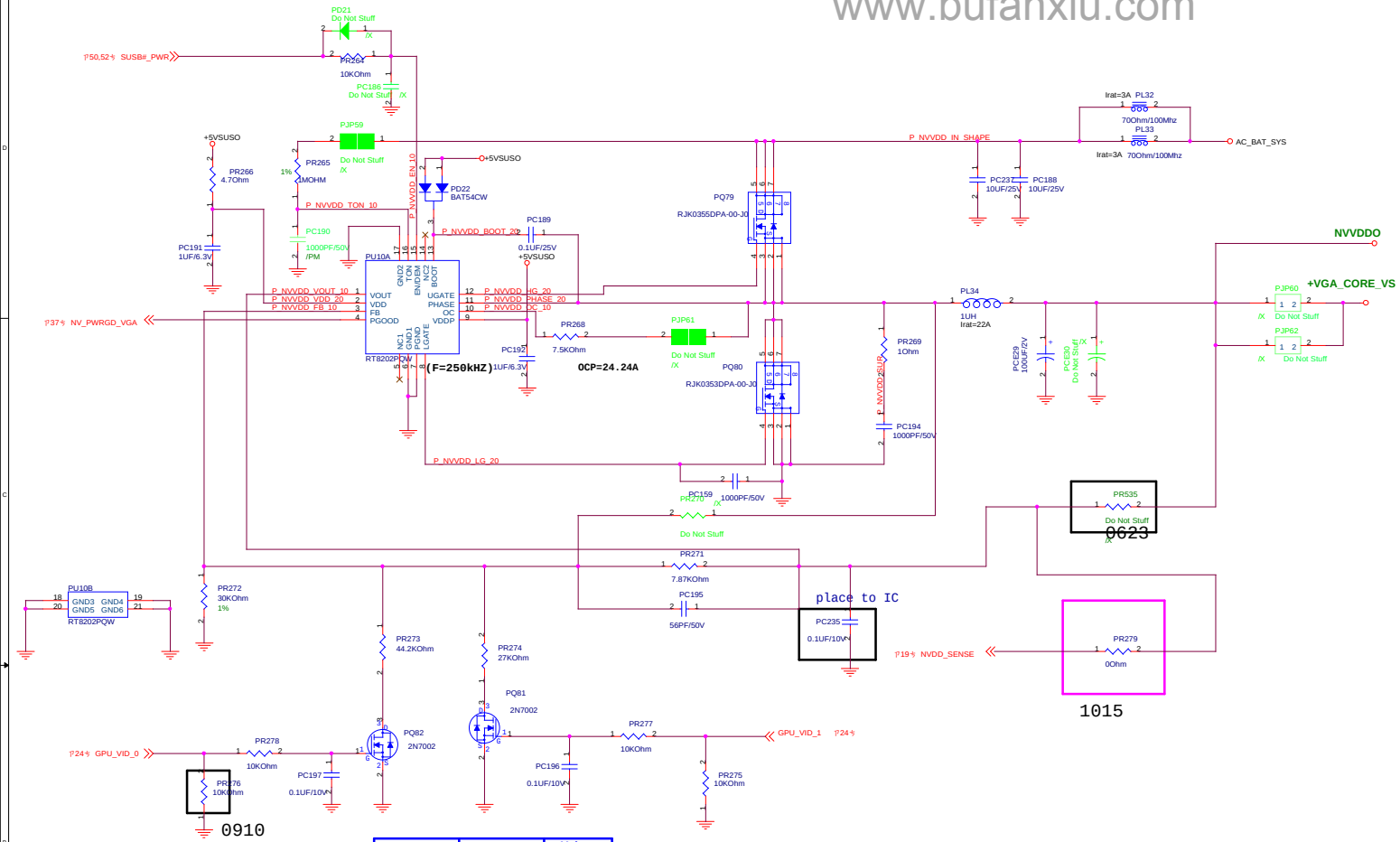
ASUSTeK Computer INC.

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
A2	P80	1.1

Date: Tuesday, December 16, 2008 Sheet 52 of 56



GPU_VID_0	GPU_VID_1	Voltage
L	L	0.946V
H	L	1.00V
L	H	1.17V
H	H	X

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.3 A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=10.87A
   ESR/2=4.5mohm
   V=44mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=10V)
   Icont=30/35A (T=25)
   Ipeak=120/140A (Pause<10us)

Controller

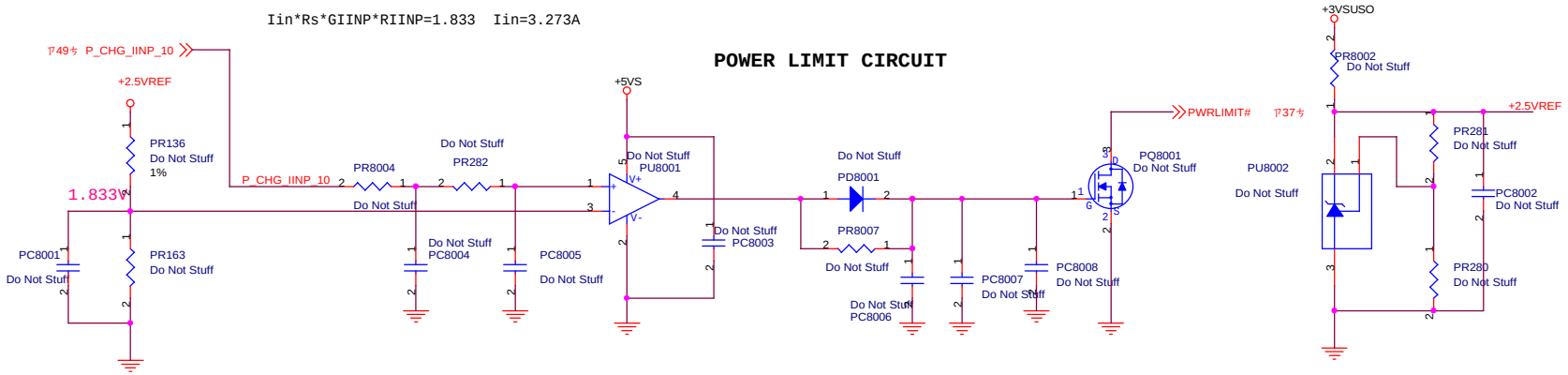
1. Voltage & Current:
   +VGA:0.94&10.08A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=24A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+VGA	
	Engineer: robin_chen	
Size: A2	Project Name: P80	Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 53 of 56	

Iin*Rs*GIINP*RIINP=1.833 Iin=3.273A

POWER LIMIT CIRCUIT



P80VC1

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Robin_chen	
Size: A3	Project Name: P80	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 54 of 80	