PROJECT S6F

Revision History

R1.0	SR	2005/07/01
R1.1	ER	2005/11/25
R2.0	PR	2005/01/18

SMB Signals

Host	Name	Devices	Address
Chipset	SMBCK,SMBDA	ICH7-M ADT7460(Thermal) ICS954213(Clock Genertor) DDR2 SO-DIMM	0001 000X b 0101 110X b D2h A0h

Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+*VALWAYS	+*V	+*VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

CPU
PM667 LV 1.5 GHz: 01G011010110
PM667 LV 1.66 GHz: 01G011010010

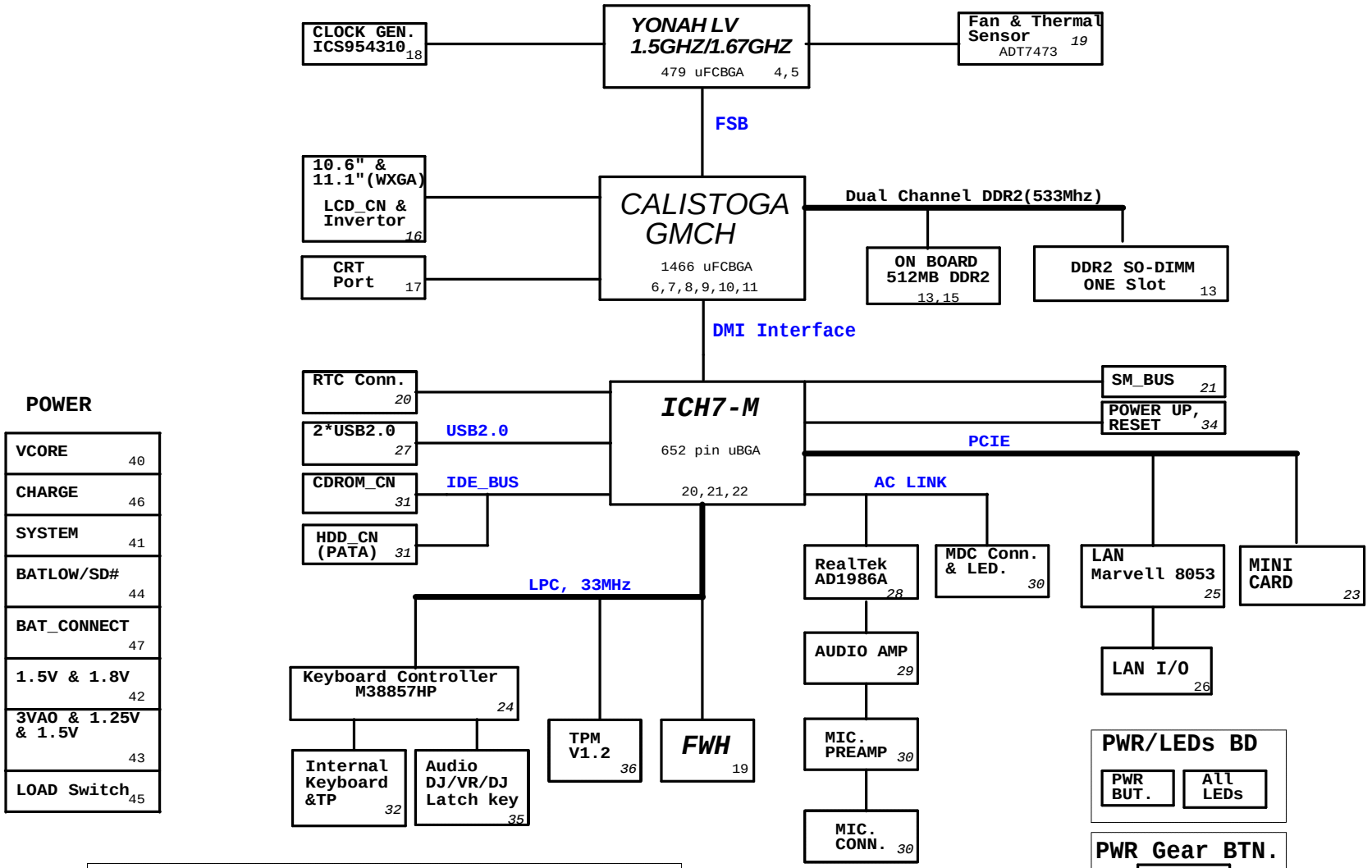
Chipset
02G010009210   C.S QG82945GM SL8Z2   INTEL CALISTOGA 876956
02G010007741   C.S NH82801GBM SL8YB   INTEL ICH7-M 876595

Memory
Infineon: 03G15073B010
Nanya: 03G15133E110

ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : Table of Contens	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 1 of 37	

YONAH/CALISTOGA(945GM) BLOCK DIAGRAM (NAPA PLATFORM)

2005.6.13 V1.0



ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : BLOCK DIAGRAM	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 2 of 37	

M38857MB_GPIO	Use As	Signal Name
P20	GPO	ANKEY_RSM
P21	GPIO	BAT_SEL#
P22	GPO	BAT_LEARN
P23	GPO	TBD
~~P27~~	~~GPO~~	~~SCROLLOCK#_3~~
P42	GPO	TP_LED
P43	GPO	TBD
P44	GPO	KBDCPURST_3Q
P45	GPO	A20GATE_3Q
P46	GPO	KBDSCI_3Q
P47	GPIO	CLKRUN#_3
P50	GPI	BAT_LLOW#_OC
P51	GPI	TBD
P52	GPI	TBD
P53	GPI	TBD
P54	GPI	LID_SW#
P55	GPI	BATIN_OC#
P56	GPO	TBD
P57	GPO	ADJ_BL
P67	GPI	TBD
P66	GPI	PWRLMT#
P65	GPI	BAT_SAVING#
P64	GPI	ACIN_OC
P63	GPO	CPPE_EN
P62	GPO	RST#NEWCARD
P61	GPI	CPPE#DET
P60	GPO	PP_TPM
P77	GPI	SMC_BAT
P76	GPI	SMD_BAT
~~P26~~	~~GPI~~	~~KBNUM#_3~~
P25	GPI	KBCAP#_3
P24	GPO	PCIRST#_GATE
P40		EXTSMI_3

ICH7_GPIO	Use As	Signal Name
GPI6	GPO	BACK_OFF#
GPIO7	GPI	WIRELESS_SW#
GPI8	GPI	EXTSMI#
GPI9	TBD	
GPI10	GPI	CHG_FULL_OC
GPI12	GPI	KB_SCI#
GPI13	GPI	MEM_ID0
GPI14	GPI	MEM_ID1
GPIO15	GPO	WL_LAN_LED#
GPIO19	GPI	PANEL_ID
GPIO24	GPI	MEM_400/533#
GPIO25	GPO	CB_SD#
GPIO26	GPO	OP_MUTE#
GPIO27	GPO	WIRELESS_LAN_ON/OFF#
GPIO28	GPO	PWR_1HZ
GPI33	GPO	BT_ON/OFF#
GPI34	GPO	FWH_WP#
GPI35	TBD	
GPI36	GPO	BT_LED#
GPI37	GPI	PCB_ID0
GPIO38	GPI	PCB_ID1
GPIO39	GPI	MEM_ID2

ASUSTek COMPUTER INC

Project Name: S6F

Engineer: MICHAEL WANG

Size: Custom

Title : System Information

Rev: 1.0

Date: Wednesday, January 18, 2006

Sheet 3 of 37

New NET on Yonah

CPU_BSEL2
VR_VID6

Need Check

VCCSENSE
VSSENSE

CPU PART NUMBER

01-011010010	CPU	INT PM667 LV DC 1.66G X48
01-011010011	CPU	INT PM667 LV DC 1.5G X38

6 H_A#[31:3] H_A#[31:3]

6 H_REQ#[4:0] H_REQ#[4:0]

6 H_D#[63:0] H_D#[63:0]

U25A

ADDR GROUP 0

ADDR GROUP 1

CONTROL

XDP/ITP SIGNALS

THERM

HCLK

RESERVED

INT PM667 LV DC

U25B

DATA GRP 0

DATA GRP 2

DATA GRP 1

DATA GRP 3

MISC

INT PM667 LV DC

Comp0,2 connect with Zo=27.4 ohm, trace length shorter than 0.5".Comp 1,3 connect with Z0=55 ohm, trace length shorter than 0.5".

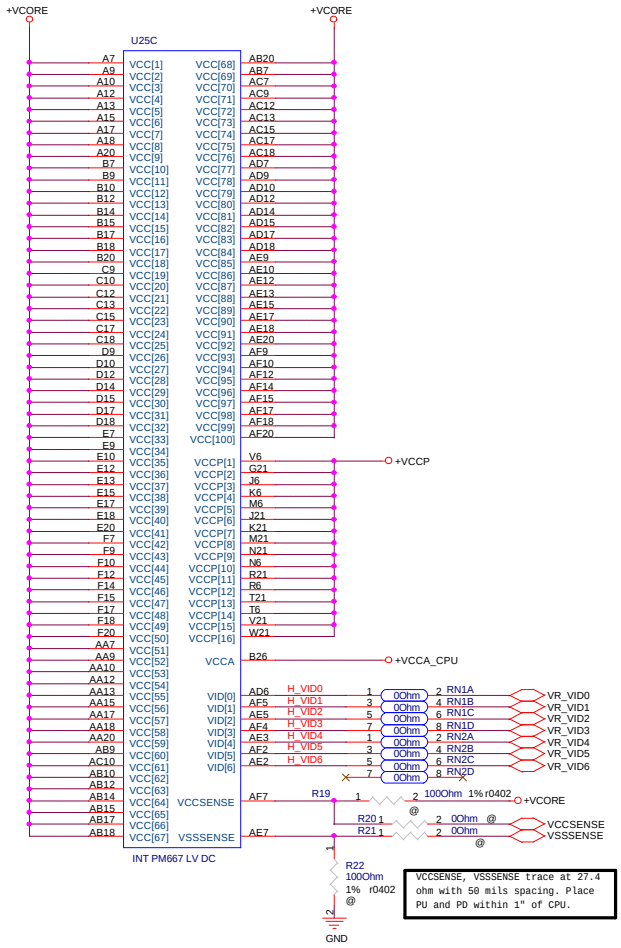
Zo=55 ohm, 0.5" max for GTLREF

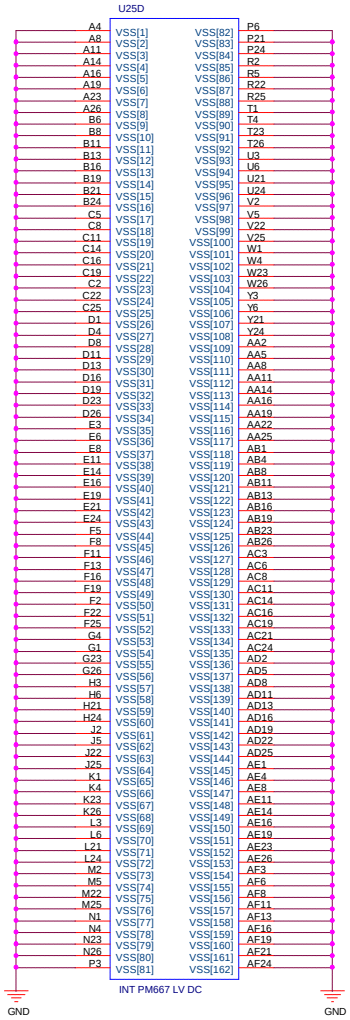
Note: Don't need for NAPA platform.But,it is exist on Alviso platform

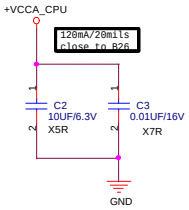
+VCORE +VCORE 5

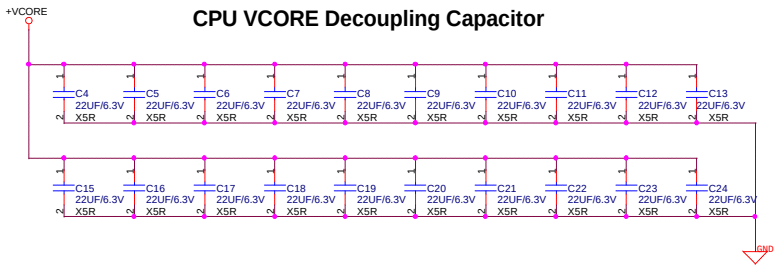
+VCCP +VCCP 5,6,9,10,14,18,20,22

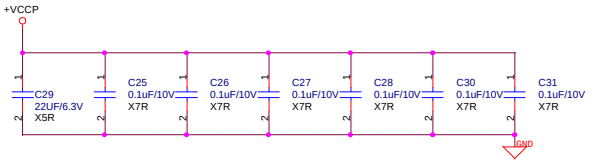
Project Name	S6F
ASUSTek COMPUTER INC	Engineer: Eric Fang
Size: Custom	Title : Yonah CPU (1)
Rev	1.0
Date: Wednesday, January 18, 2006	Sheet 4 of 37

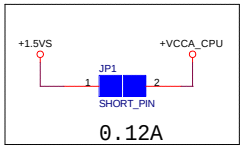




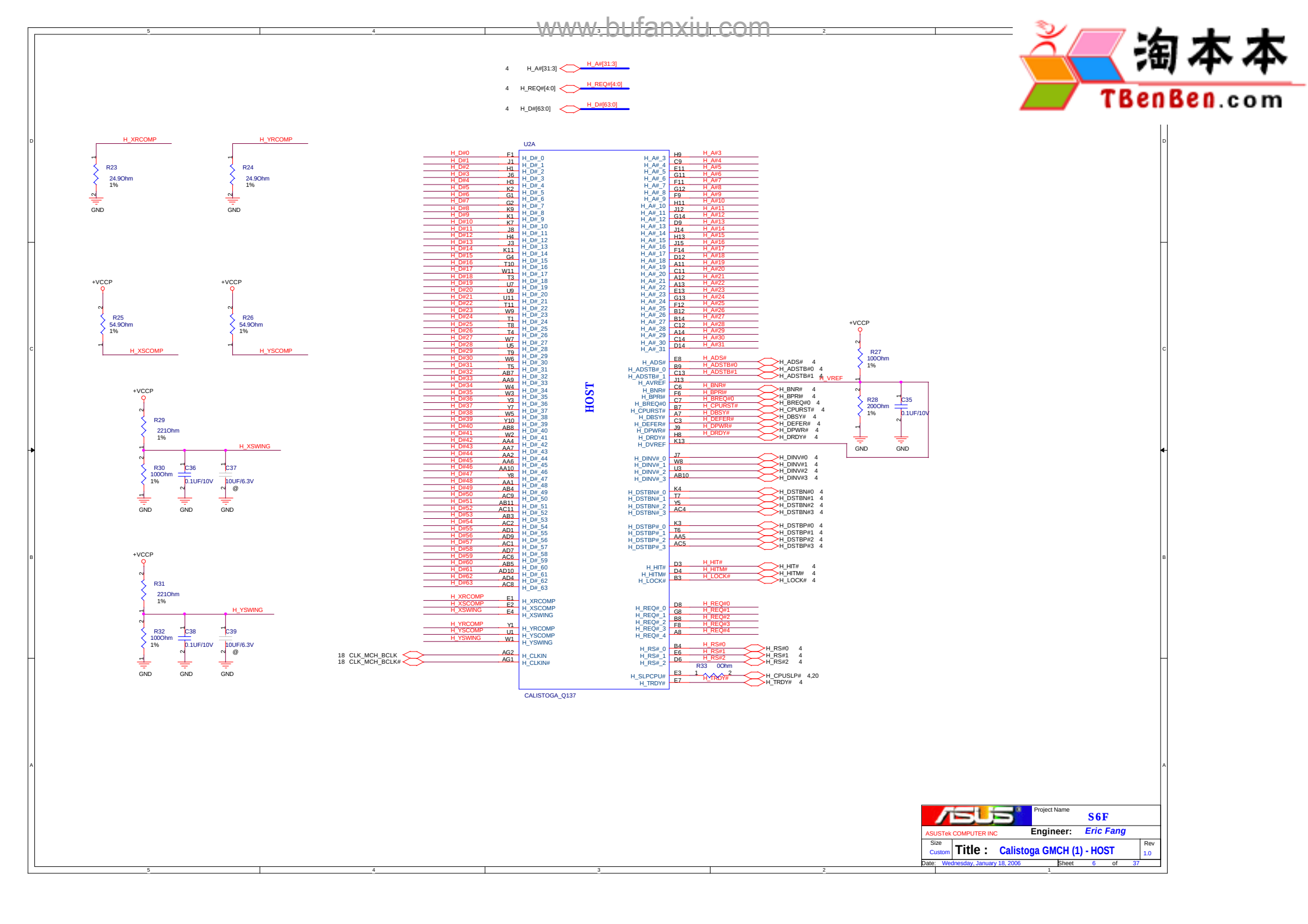




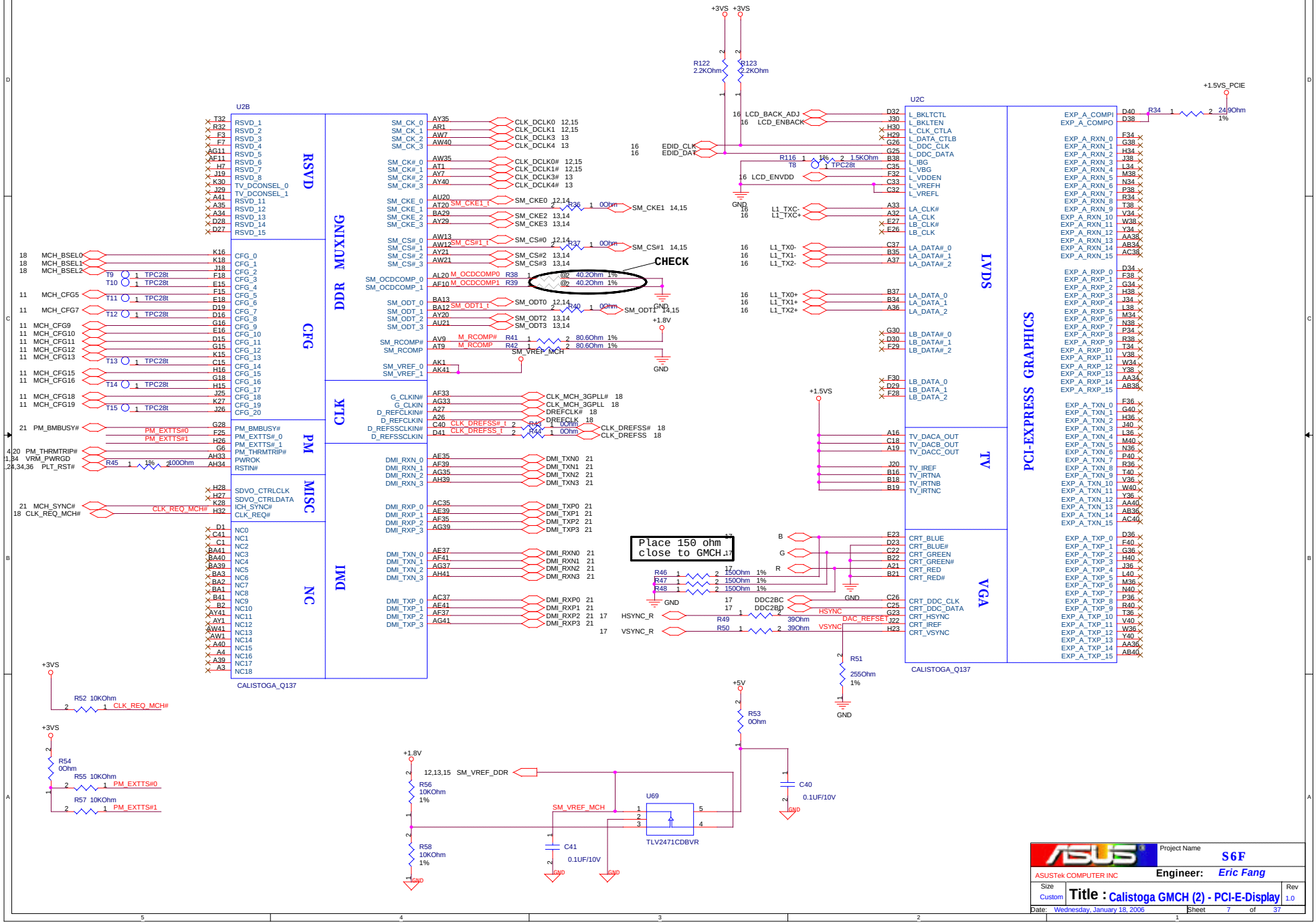




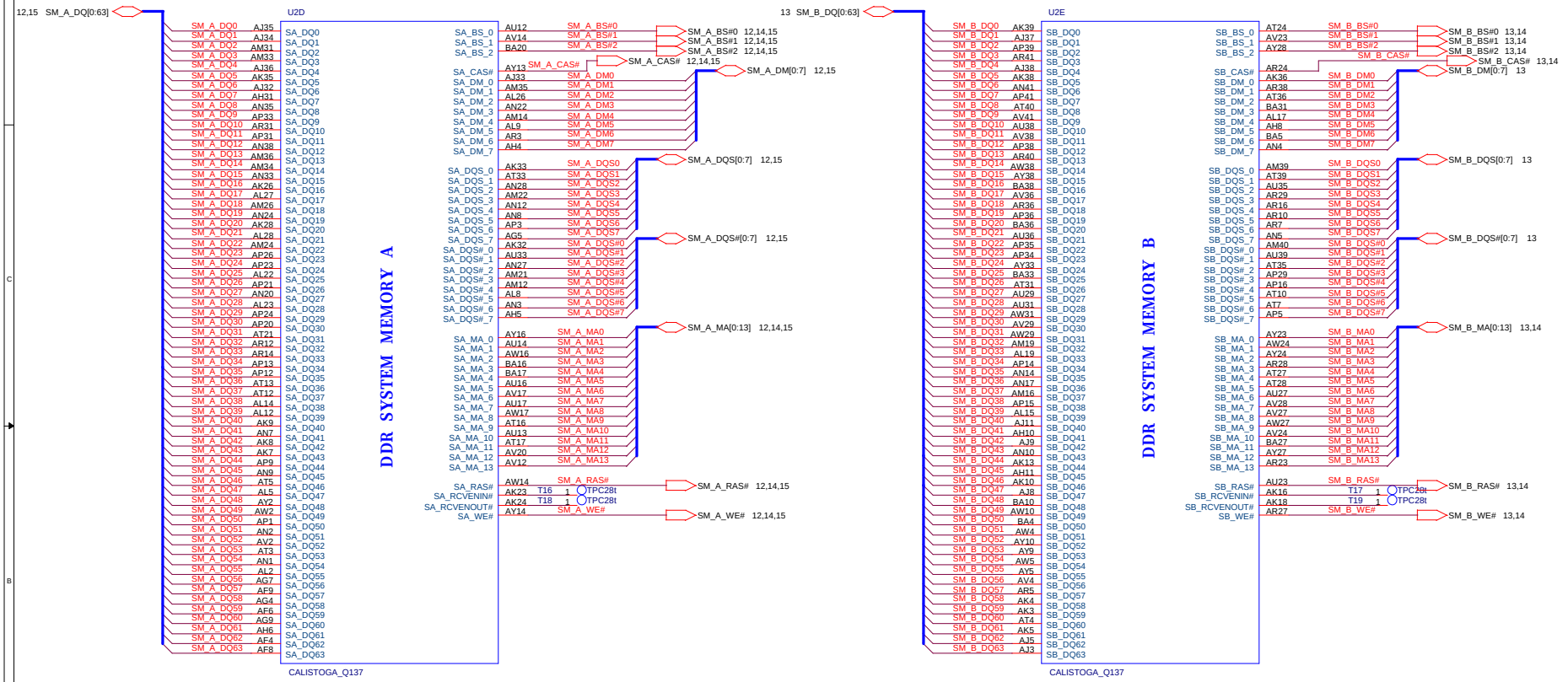
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : Yonah CPU (2)	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 5 of 37	



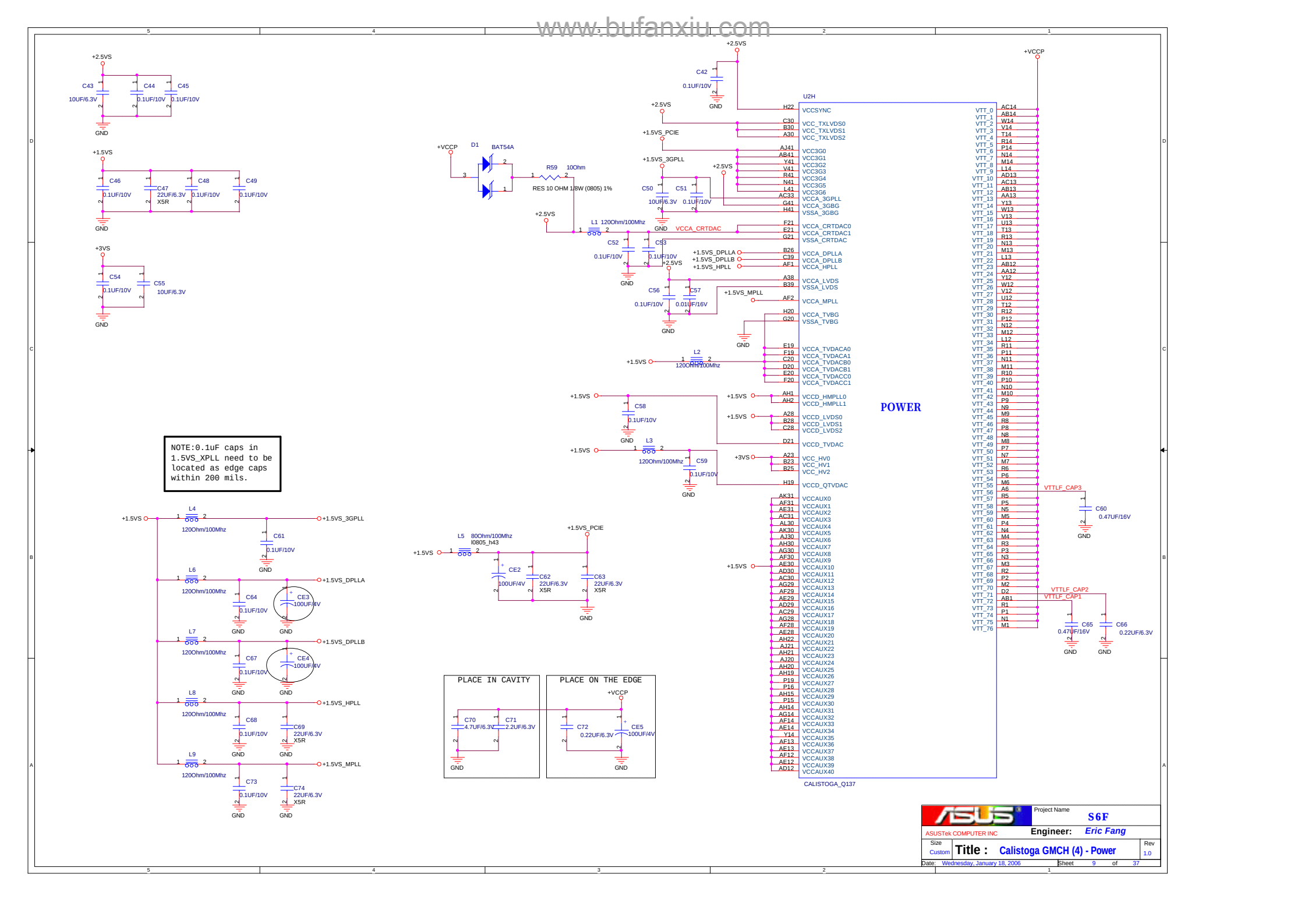
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : Calistoga GMCH (1) - HOST	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 6 of 37	



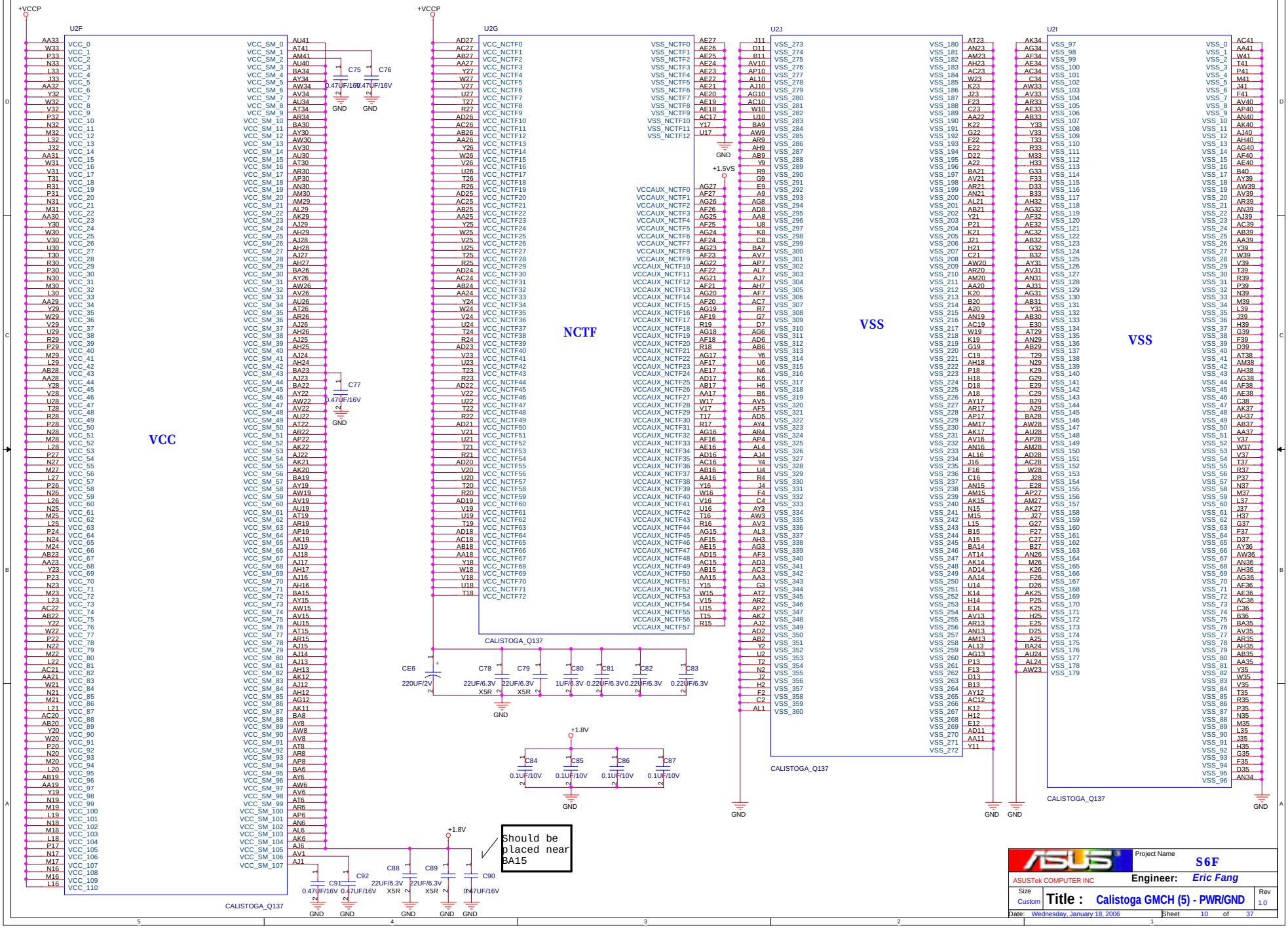
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title : Calistoga GMCH (2) - PCI-E-Display		Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 7 of 37		



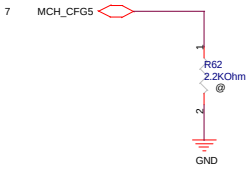
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title :	Calistoga GMCH (3) - DDR2	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 8	of 37	



ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : Calistoga GMCH (4) - Power	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 9 of 37	

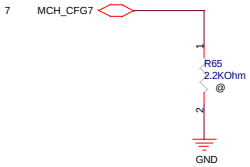


ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title :	Calistoga GMCH (5) - PWR/GND	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet	10 of 37	



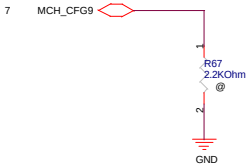
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



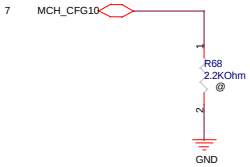
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



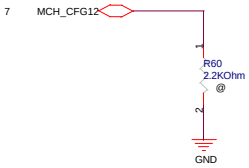
CFG9 : PCIE GRAPHIC LANE

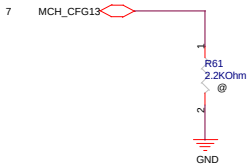
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

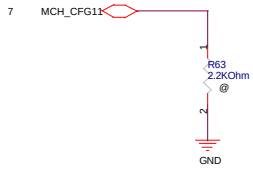


CFG10: HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY





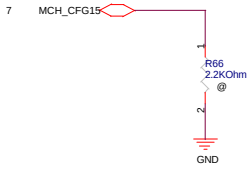


CFG11 : PSB 4X CLK ENABLE

LOW = 4X ENABLED
HIGH 8X ENABLED (Default)

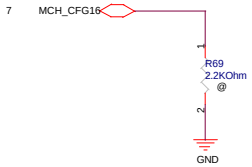
CFG19 : DMI LANE REVERSAL

LOW = NORMAL
HIGH = LANES REVERSED



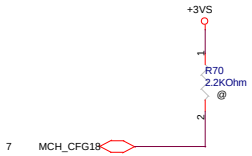
CFG15 :ICH RESET DISABLE

LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION



CFG16 : FSB DYNAMIC ODT

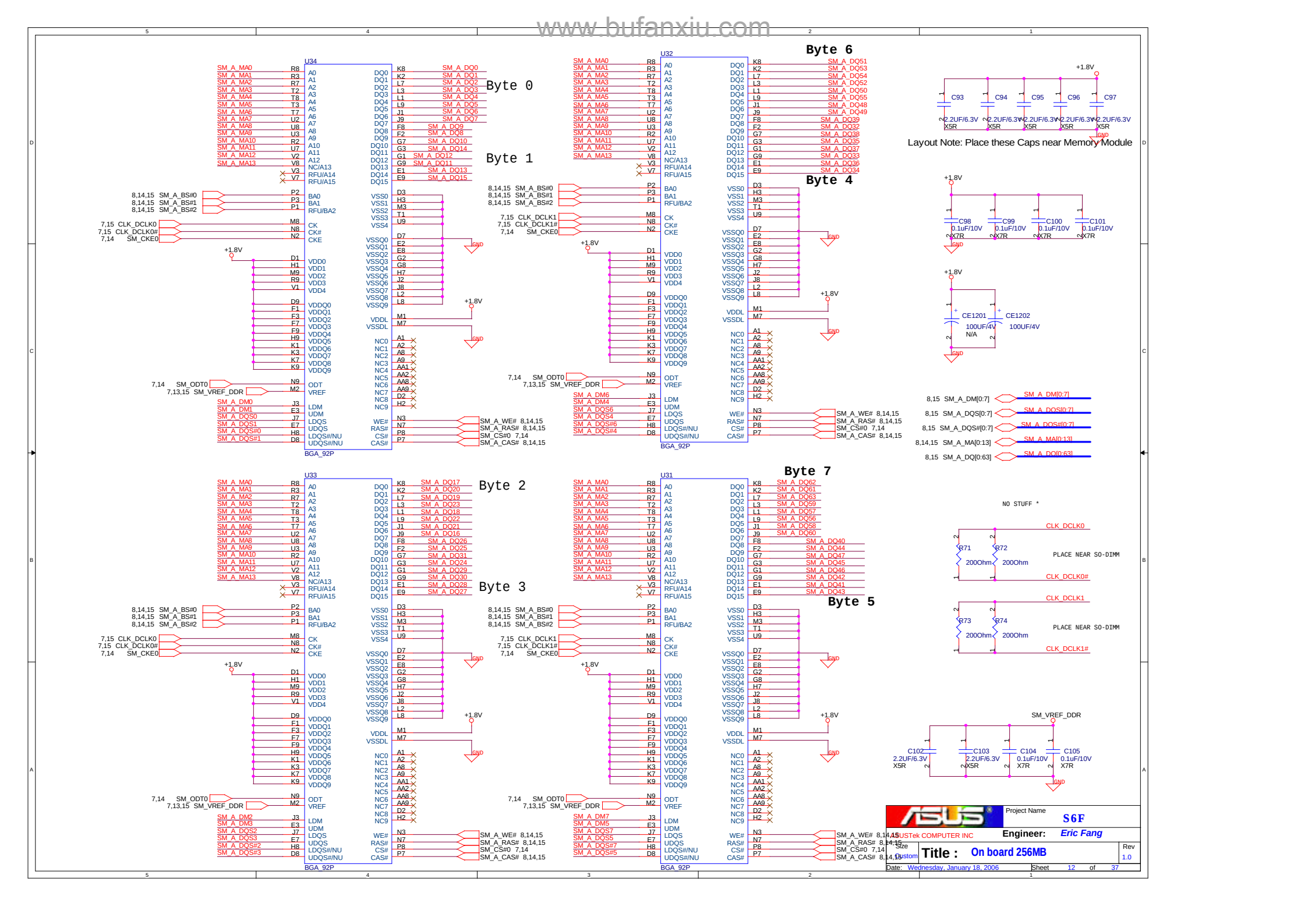
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V

ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: *Eric Fang*	
Size: Custom	Title : Calistoga GMCH (6) - Strapping	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 11 of 37	



SM_B_MA[0:13] SM_B_MA[0:13] 8,14
SM_B_DQ[0:63] SM_B_DQ[0:63] 8
SM_B_DM[0:7] SM_B_DM[0:7] 8
SM_B_DQS[0:7] SM_B_DQS[0:7] 8
SM_B_DQS#[0:7] SM_B_DQS#[0:7] 8

U70A

SM_B_MA0 102 A0
SM_B_MA1 101 A1
SM_B_MA2 100 A2
SM_B_MA3 99 A3
SM_B_MA4 98 A4
SM_B_MA5 97 A5
SM_B_MA6 94 A6
SM_B_MA7 92 A7
SM_B_MA8 93 A8
SM_B_MA9 91 A9
SM_B_MA10 105 A10/AP
SM_B_MA11 90 A11
SM_B_MA12 89 A12
116 A13
86 A14
84 A15
85 A16_BA2

8,14 SM_B_BS#2 SM_B_BS#2
8,14 SM_B_BS#0 SM_B_BS#0 107 BA0
8,14 SM_B_BS#1 SM_B_BS#1 106 BA1
7,14 SM_CS#2 SM_CS#2 110 S0#
7,14 SM_CS#3 SM_CS#3 115 S1#
7 CLK_DCLK3 CLK_DCLK3 30 CK0
7 CLK_DCLK3# CLK_DCLK3# 32 CK0#
7 CLK_DCLK4 CLK_DCLK4 164 CK1
7 CLK_DCLK4# CLK_DCLK4# 166 CK1#
7,14 SM_CKE2 SM_CKE2 79 CKE0
7,14 SM_CKE3 SM_CKE3 80 CKE1
8,14 SM_B_CAS# SM_B_CAS# 113 CAS#
8,14 SM_B_RAS# SM_B_RAS# 108 RAS#
8,14 SM_B_WE# SM_B_WE# 109 WE#
198 SA0
200 SA1
18,19,21,23,33 SMBCK_3S 197 SCL
18,19,21,23,33 SMBDA_3S 195 SDA
7,14 SM_ODT2 114 ODT0
7,14 SM_ODT3 119 ODT1

SM_B_DM7 10 DM0
SM_B_DM5 26 DM1
SM_B_DM4 52 DM2
SM_B_DM6 67 DM3
SM_B_DM3 130 DM4
SM_B_DM2 147 DM5
SM_B_DM1 170 DM6
SM_B_DM0 185 DM7

SM_B_DQS7 13 DQS0
SM_B_DQS5 31 DQS1
SM_B_DQS4 51 DQS2
SM_B_DQS6 70 DQS3
SM_B_DQS3 131 DQS4
SM_B_DQS2 148 DQS5
SM_B_DQS1 169 DQS6
SM_B_DQS0 188 DQS7
SM_B_DQS#7 11 DQS#0
SM_B_DQS#5 29 DQS#1
SM_B_DQS#4 49 DQS#2
SM_B_DQS#6 68 DQS#3
SM_B_DQS#3 129 DQS#4
SM_B_DQS#2 146 DQS#5
SM_B_DQS#1 167 DQS#6
SM_B_DQS#0 186 DQS#7

DQ0 5 SM_B_DQ63
DQ1 7 SM_B_DQ58
DQ2 17 SM_B_DQ62
DQ3 19 SM_B_DQ61
DQ4 4 SM_B_DQ59
DQ5 6 SM_B_DQ60
DQ6 14 SM_B_DQ56
DQ7 16 SM_B_DQ57
DQ8 23 SM_B_DQ44
DQ9 25 SM_B_DQ41
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DQ56 179 SM_B_DQ6
DQ57 181 SM_B_DQ2
DQ58 189 SM_B_DQ4
DQ59 191 SM_B_DQ1
DQ60 180 SM_B_DQ3
DQ61 182 SM_B_DQ7
DQ62 192 SM_B_DQ0
DQ63 194 SM_B_DQ5

Byte7
Byte 5
Byte4
Byte6
Byte3
Byte 2
Byte1
Byte 0

DDR_DIMM_200P

GND GND

+1.8V

U70B

VDD1 112
VDD2 111
VDD3 117
VDD4 96
VDD5 95
VDD6 118
VDD7 81
VDD8 82
VDD9 87
VDD10 103
VDD11 88
VDD12 104
VDDSPD 199
NC1 83
NC2 120
NC3 50
NC4 69
NCTEST 163
VREF 1
GND0 201
GND1 202
NP_NC1 203
NP_NC2 204
VSS1 47
VSS2 133
VSS3 183
VSS4 77
VSS5 12
VSS6 48
VSS7 184
VSS8 78
VSS9 71
VSS10 72
VSS11 121
VSS12 122
VSS13 196
VSS14 193
VSS15 8
VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

DDR_DIMM_200P

+3VS

C106 0.1uF/10V X7R
C107 2.2UF/6.3V X5R
7,12,15 SM_VREF_DDR
C108 2.2UF/6.3V X5R
C109 0.1uF/10V X7R

NO STUFF *

Layout Note: Place these Caps near uDIMM

C110 C111 C112 C113 C114
2.2UF/6.3V X5R

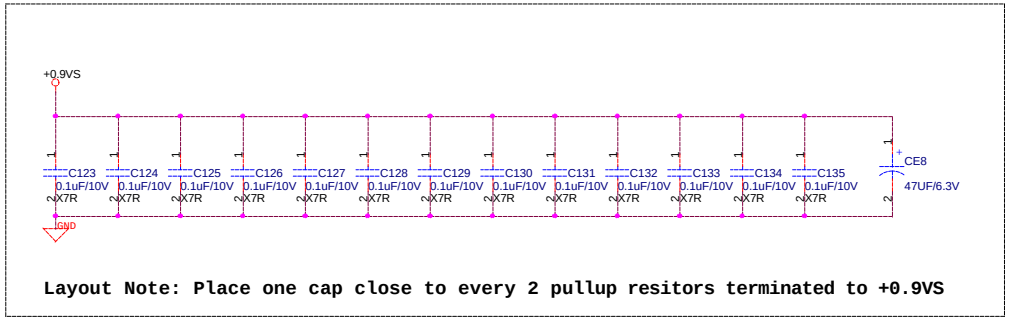
Layout Note: Place these Caps near uDIMM

C119 C120 C121 C122
0.1uF/10V X7R

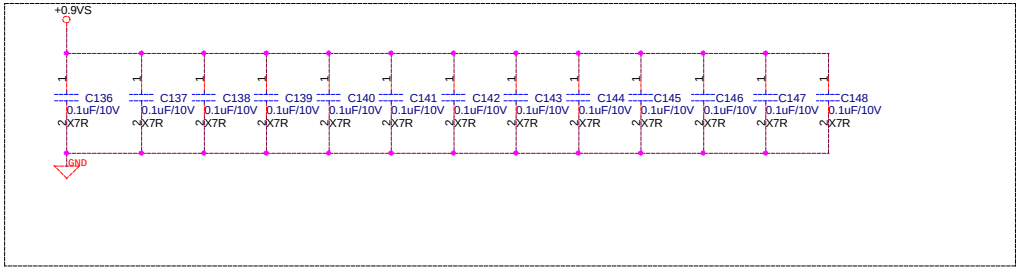
Layout Note: Place these High-Freq decoupling Caps near the GMCH

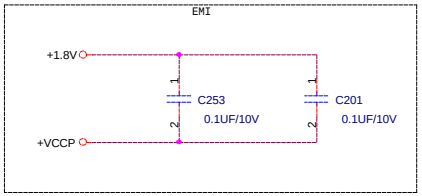
C115 C116 C117 C118
0.1uF/10V X7R

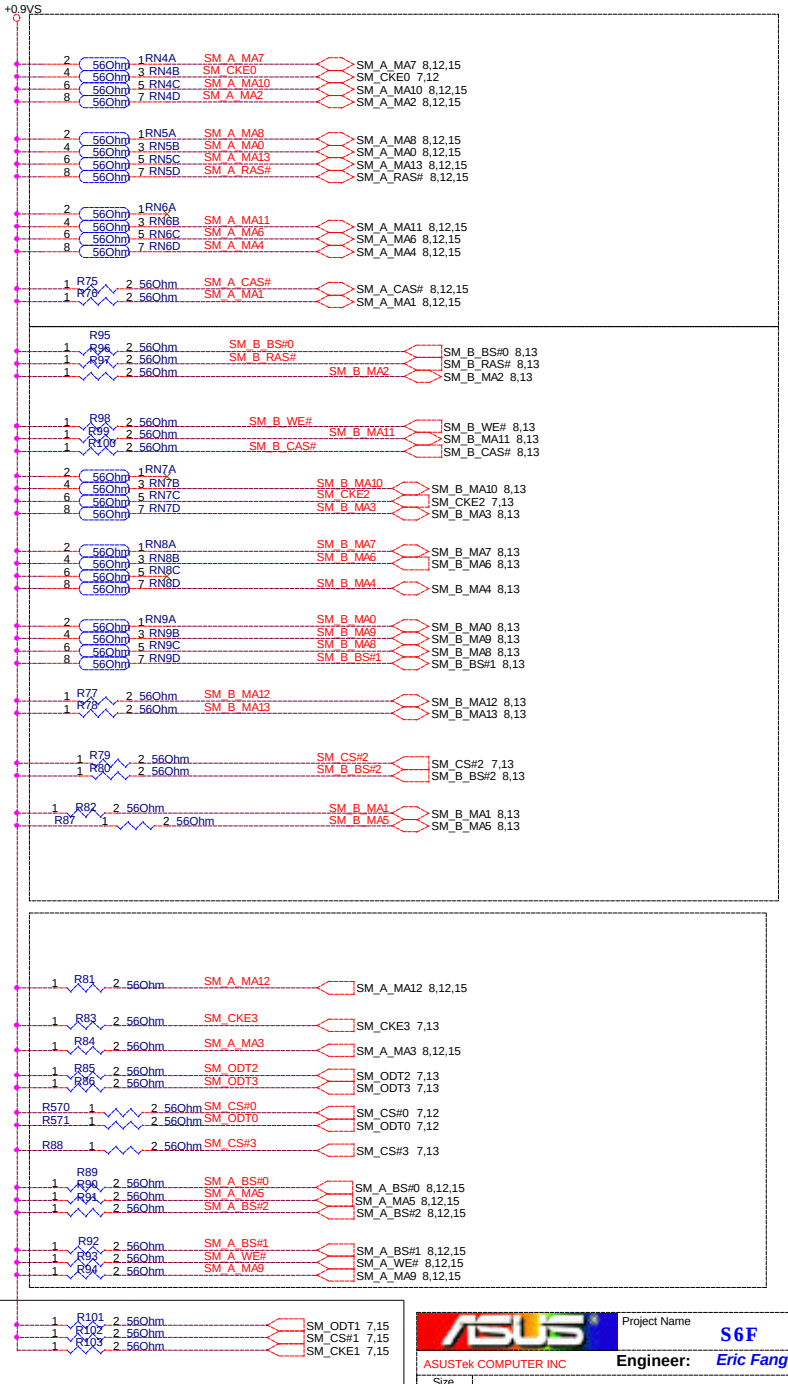
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : DDR2 Micro DIMM	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 13 of 37	



Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9VS

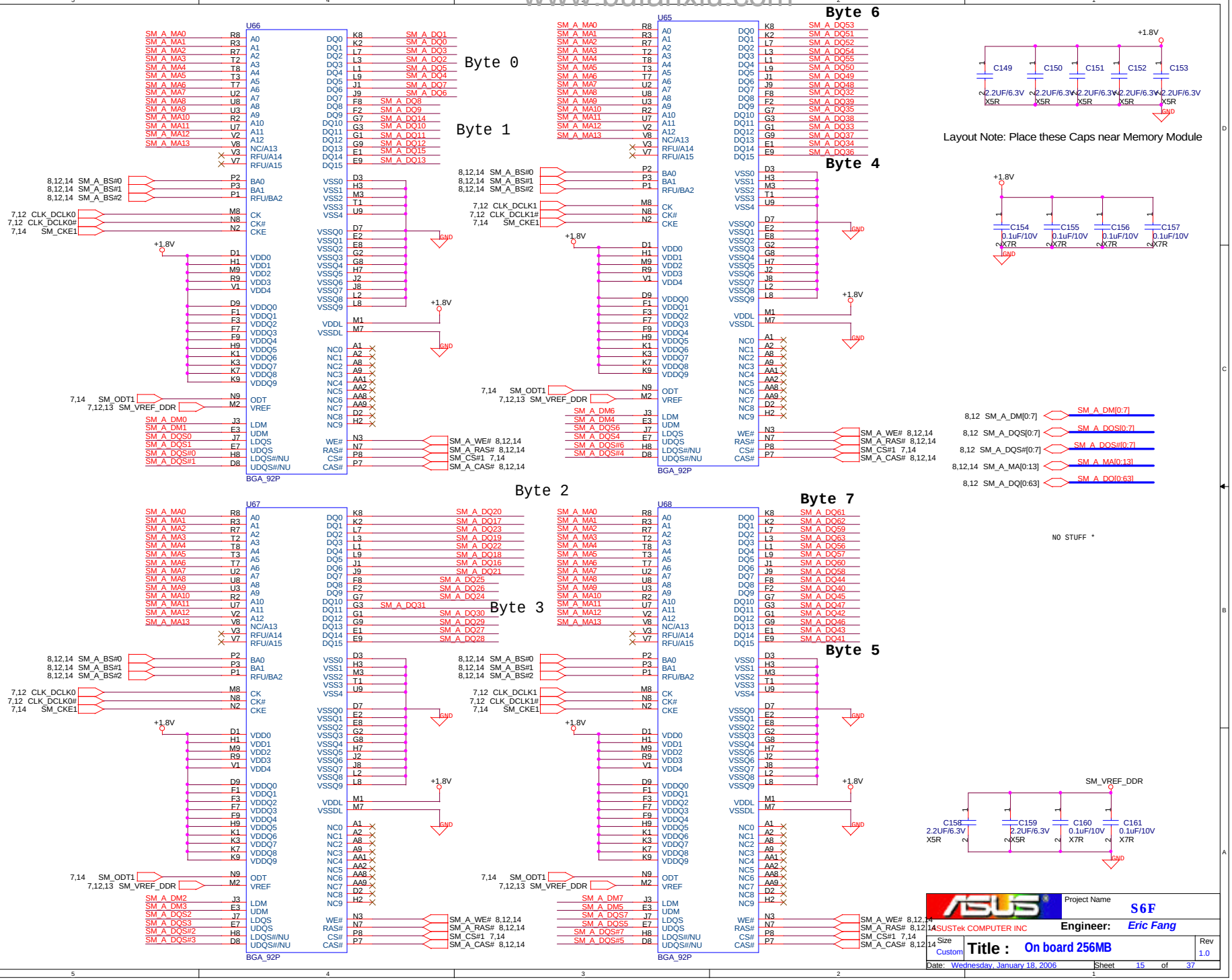


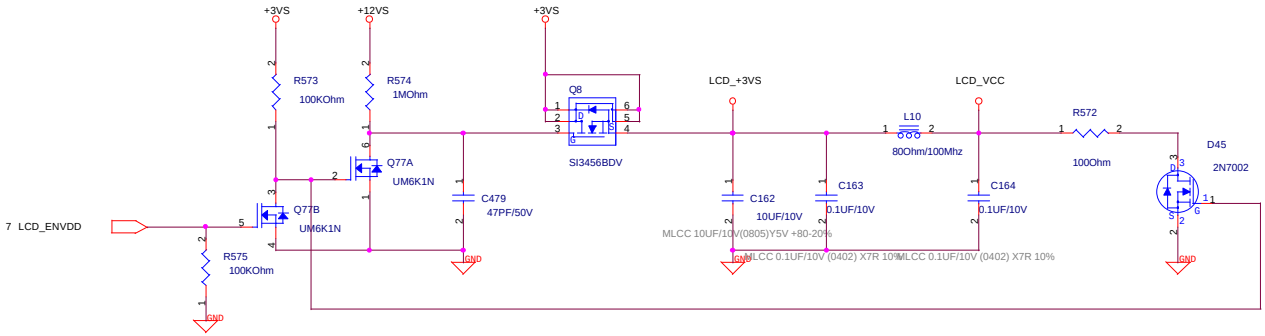


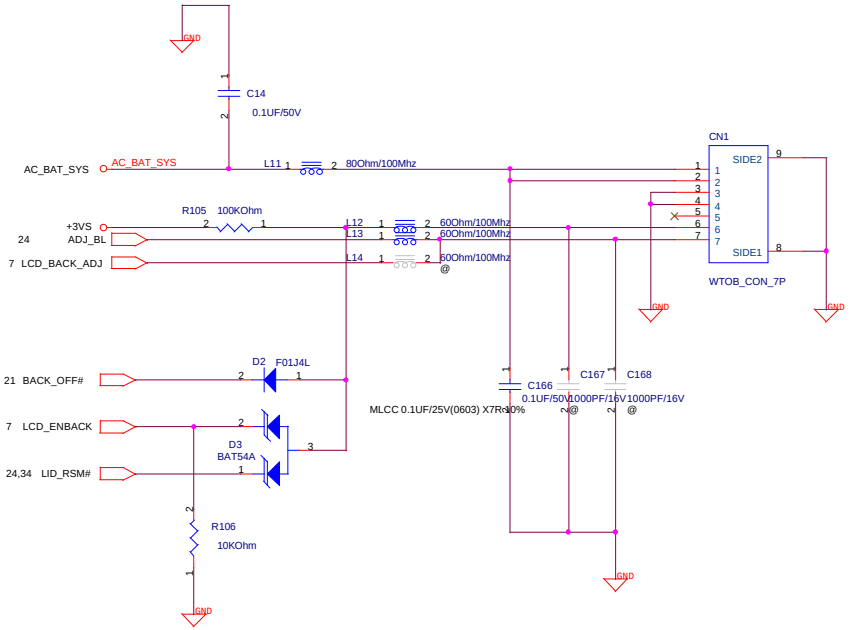


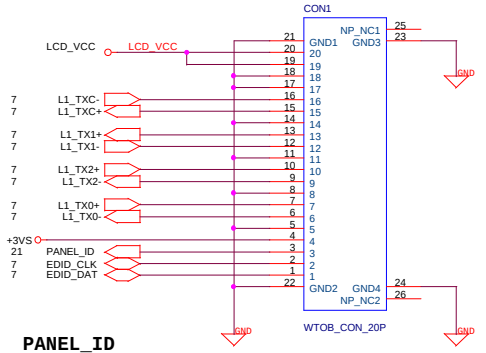
For 8 pcs memory implement

ASUSTek COMPUTER INC	Project Name: S6F	Engineer: Eric Fang
Size: Custom	Title : DDR2 Termination	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 14 of 37	





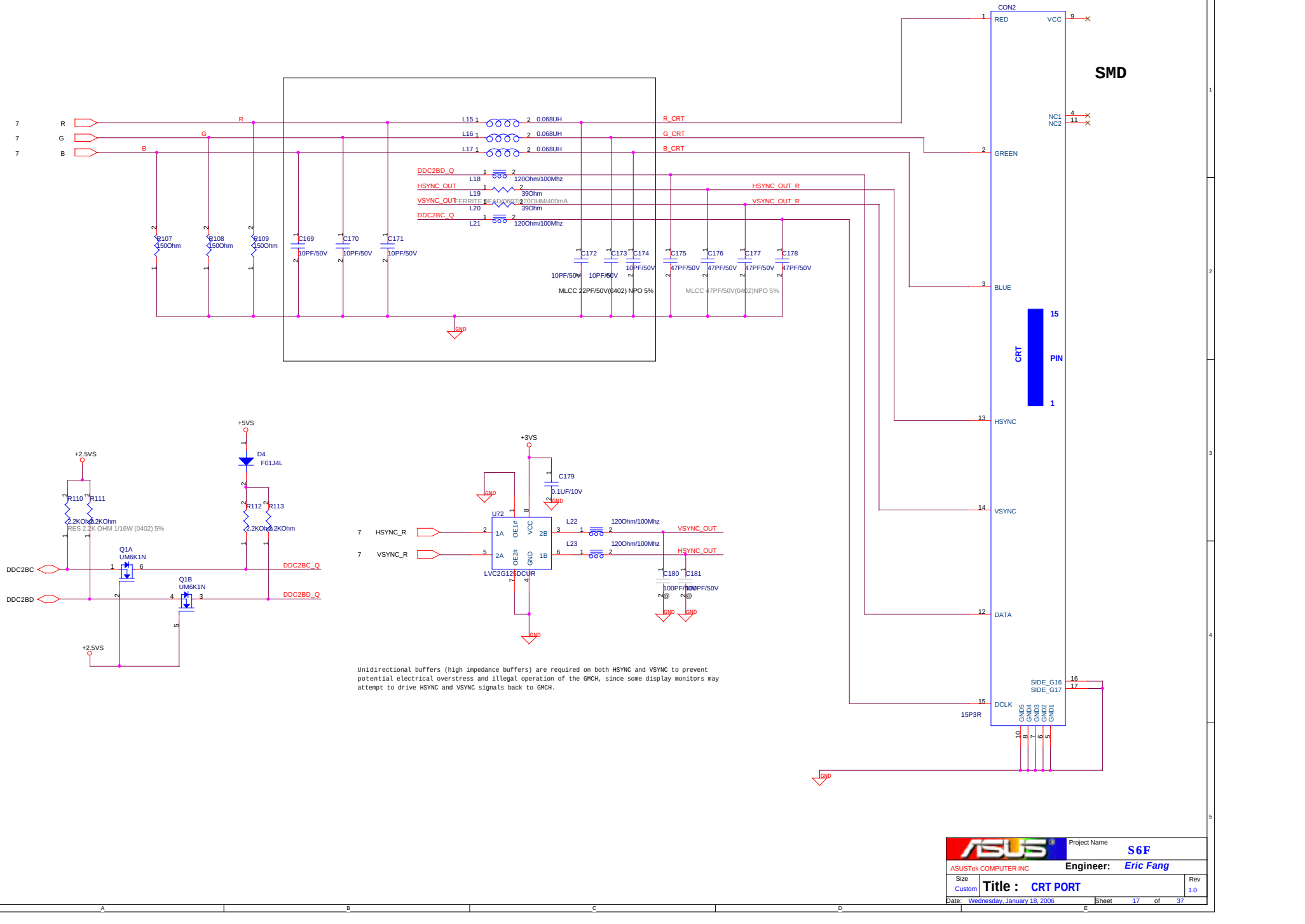




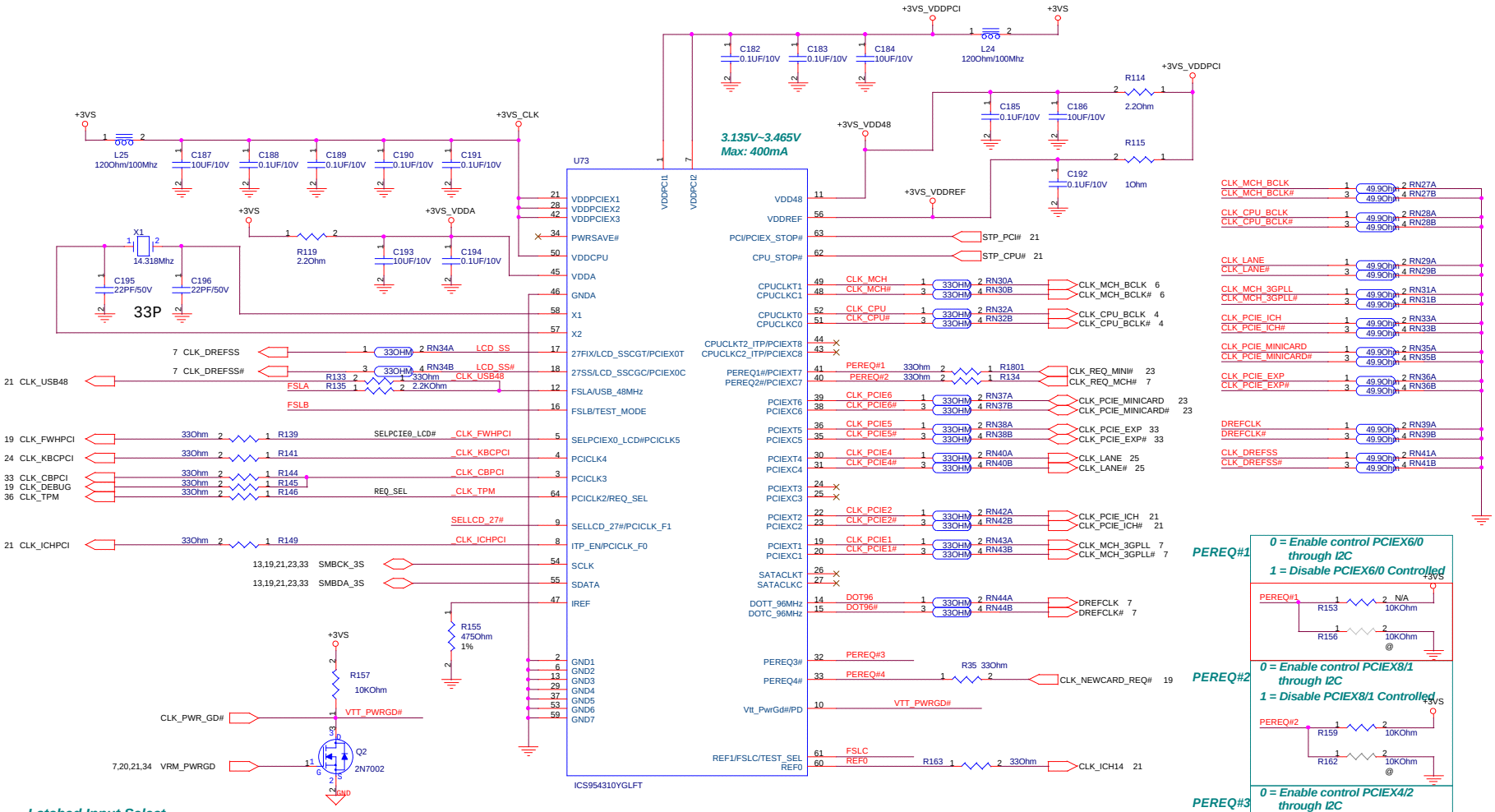
PANEL_ID
HI 10.6
LO 11.1

current rating = 0.3A

ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title :	LCD CON	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 16 of 37		



ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : CRT PORT	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 17 of 37	



Latched Input Select

SELPCIE0_LCD#/PCI_CLK5

0 = LCDCLK
1 = PCIEX

Decide pin 17.18

SELPCIE0_LCD#
_CLK_FWHPCI
R165 10KOhm

PCI_CLK2/REQ_SEL

0 = PCIECLK
1 = PEREQ#

Decide pin 40.41

REQ_SEL
_CLK_TPM
R177 10KOhm

SELLCD_27#/PCICLK_F1

0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair

SELLCD_27#
R178 10KOhm

Decide pin 17.18

Reserved for R1.0 Debug

+VCCP
R166 1KOhm @
R167 1KOhm @
R175 1KOhm @
R176 1KOhm @

4 CPU_BSEL0 R168 0Ohm FSLA R169 1KOhm MCH_BSEL0 7
4 CPU_BSEL1 R171 0Ohm FSLB R172 1KOhm MCH_BSEL1 7
4 CPU_BSEL2 R173 0Ohm FSLC R174 1KOhm MCH_BSEL2 7

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

PEREQ#1

0 = Enable control PCIEX6/0 through I2C
1 = Disable PCIEX6/0 Controlled

PEREQ#1 R153 N/A 10KOhm
R156 10KOhm @

PEREQ#2

0 = Enable control PCIEX8/1 through I2C
1 = Disable PCIEX8/1 Controlled

PEREQ#2 R159 10KOhm
R162 10KOhm @

PEREQ#3

0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled

PEREQ#3 R164 10KOhm

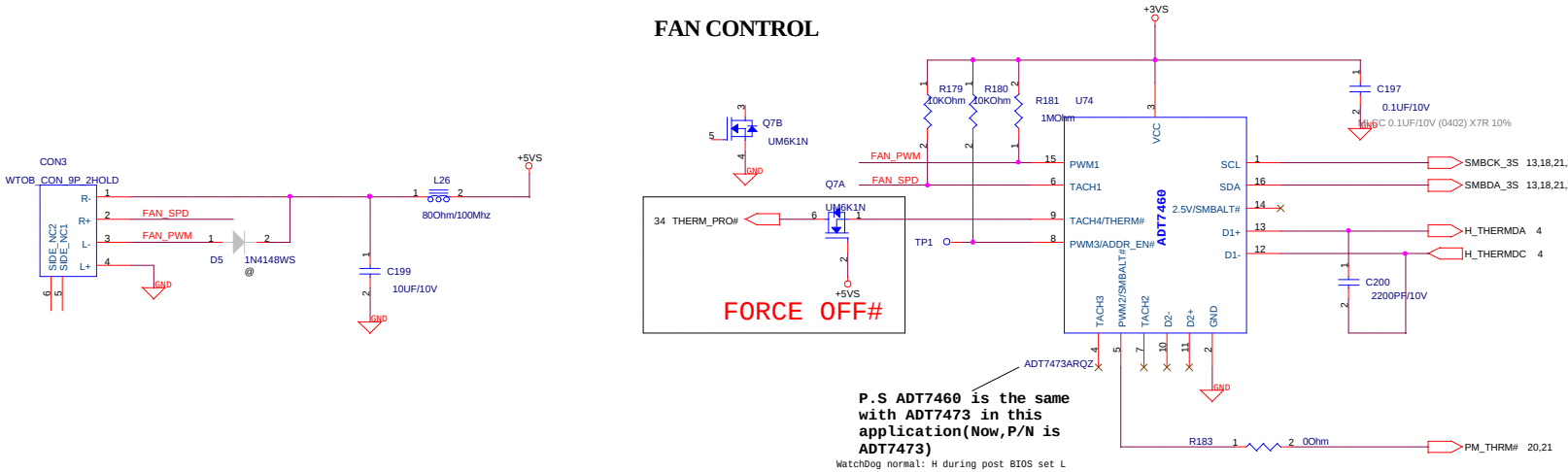
PEREQ#4

0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled

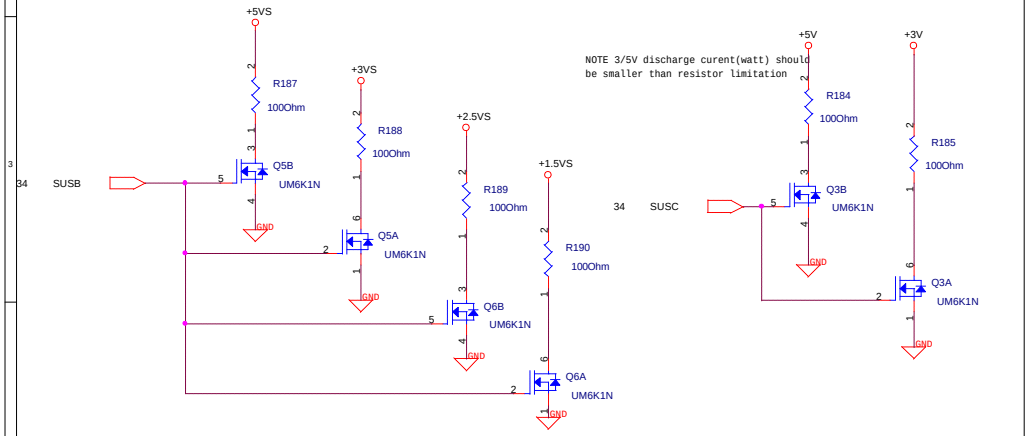
PEREQ#4 R170 10KOhm @

Project Name	S6F
ASUSTek COMPUTER INC	Engineer: Eric Fang
Size: Custom	Title : CLOCK GENERATOR
Rev	1.0
Date: Wednesday, January 18, 2006	Sheet 18 of 37

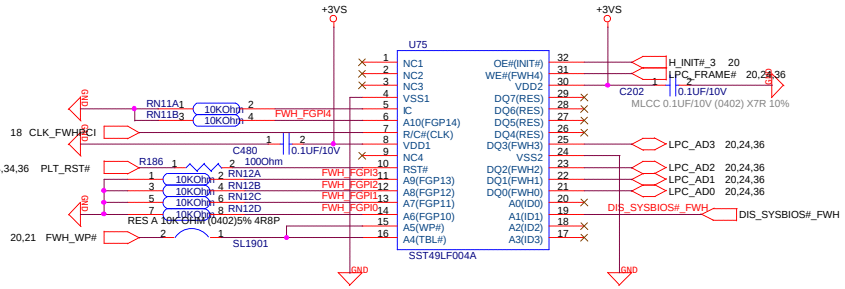
FAN CONTROL



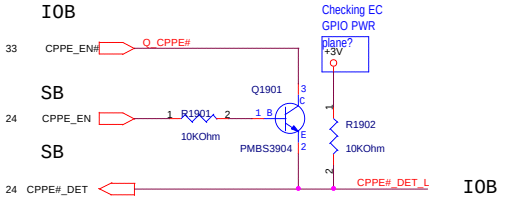
Discharge circuit for power fast down

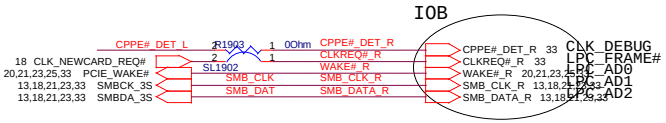


BIOS

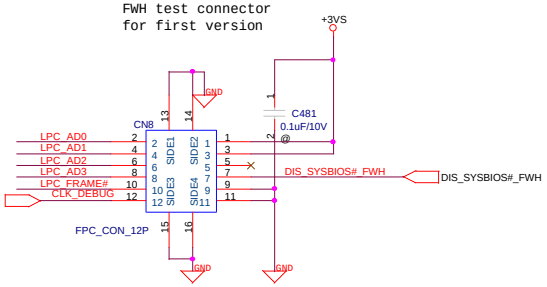


IOB

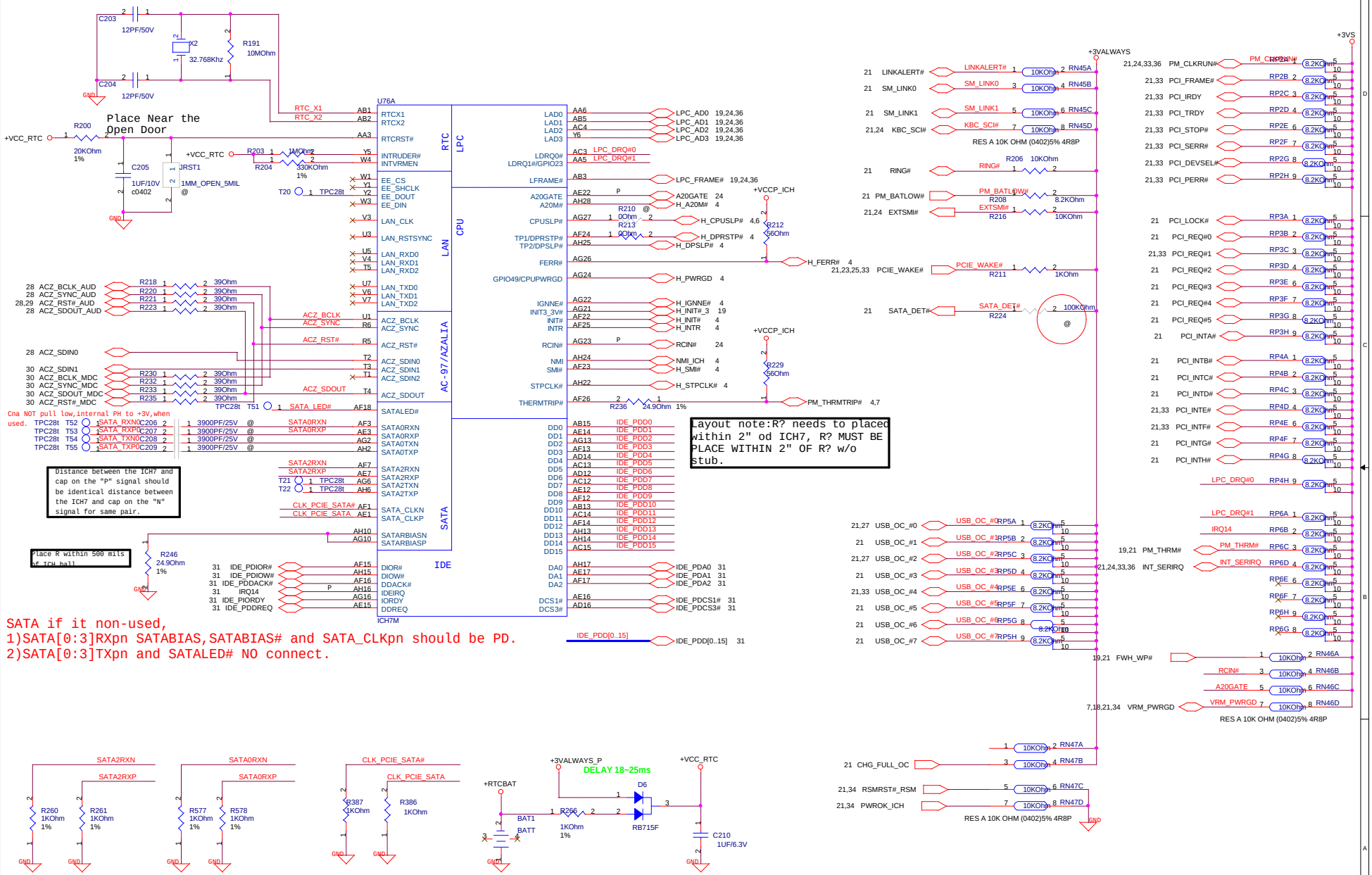


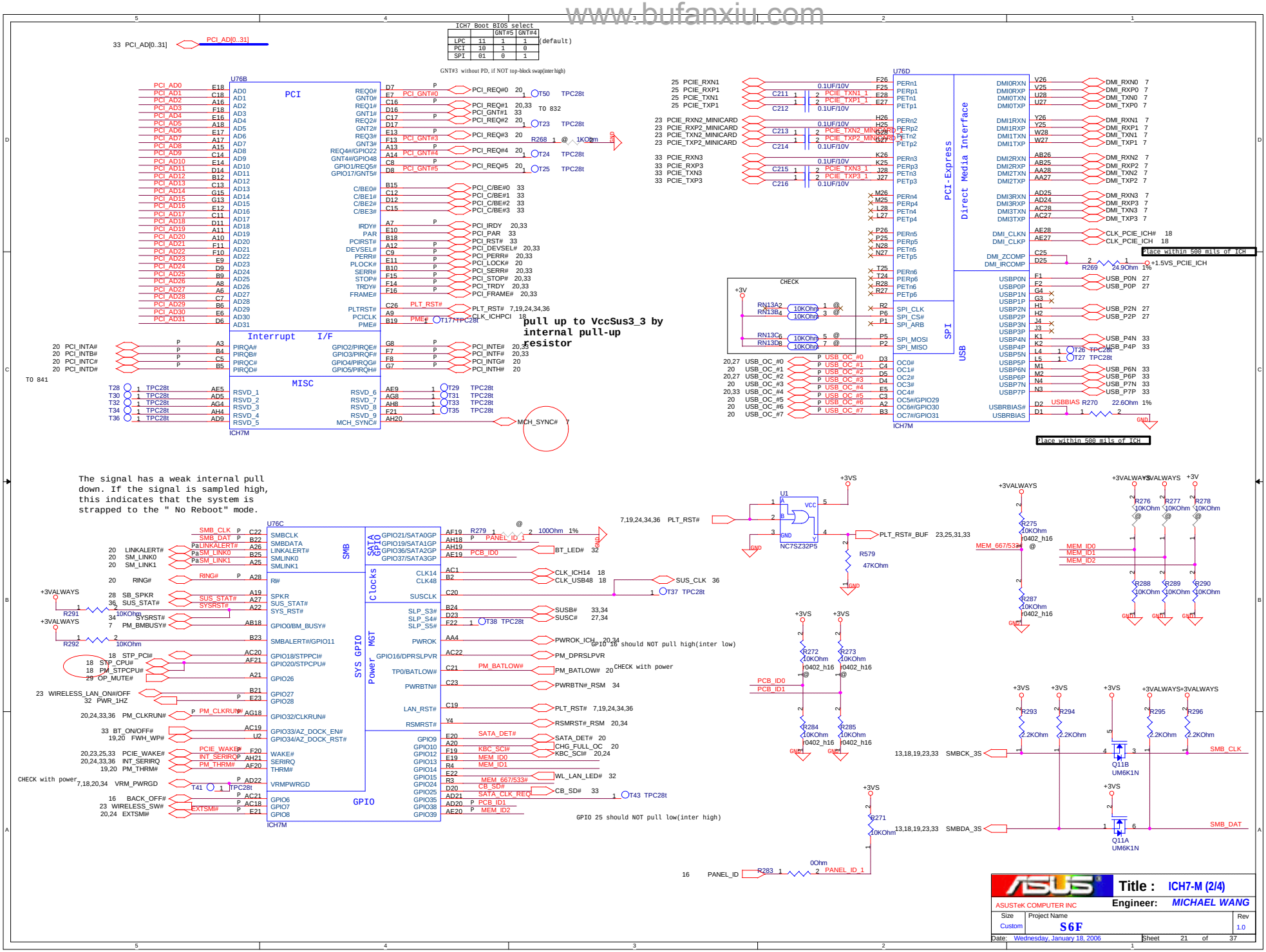


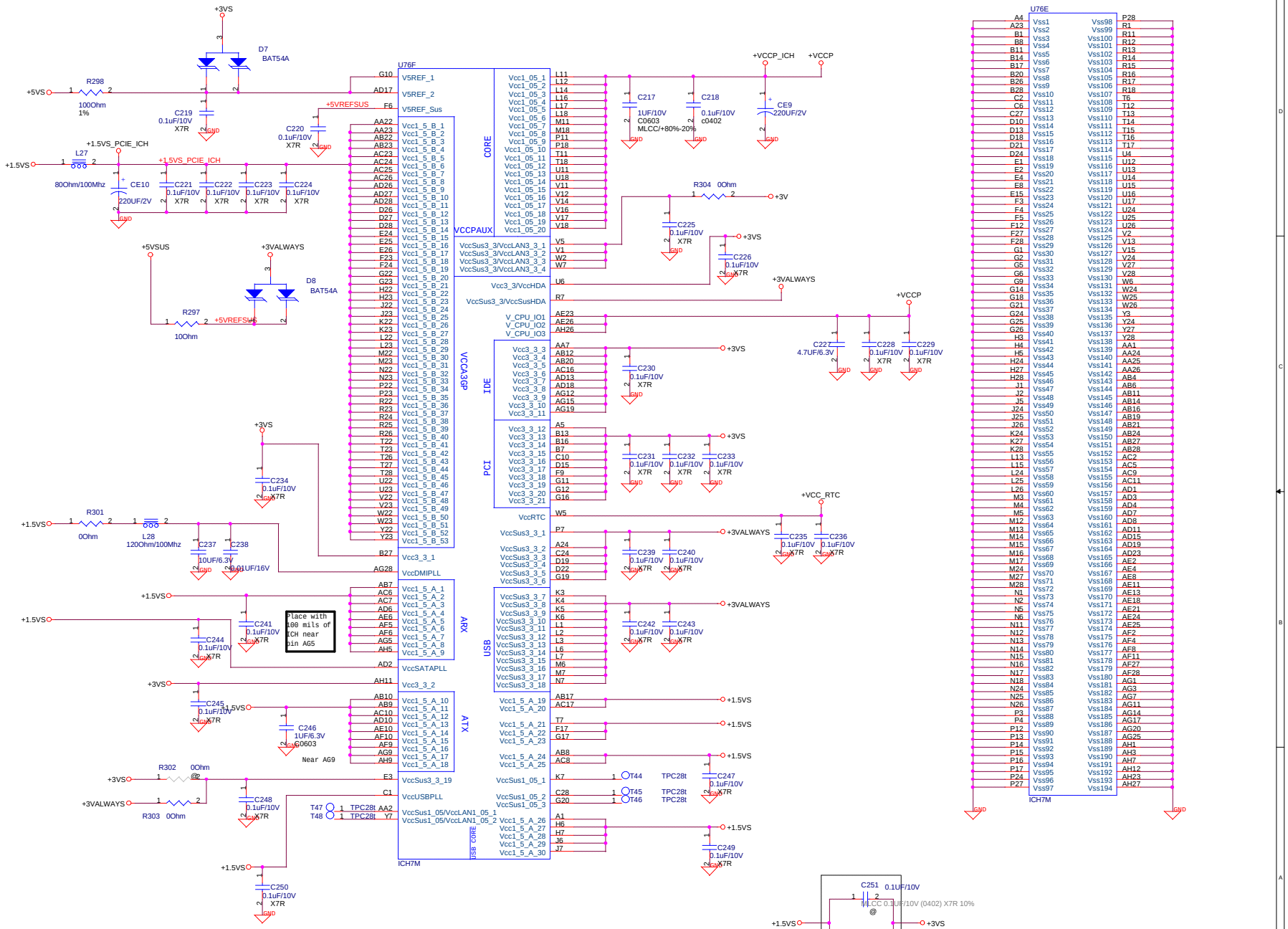
FWH test connector for first version



ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : FAN/THERMAL/FWH	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 19 of 37	



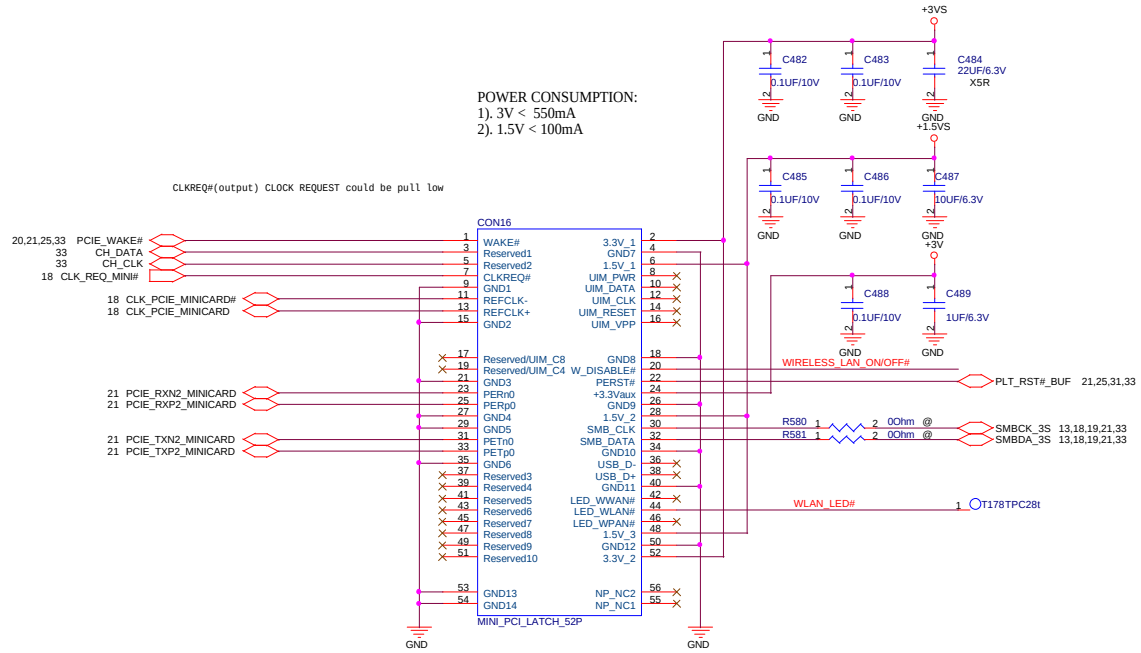


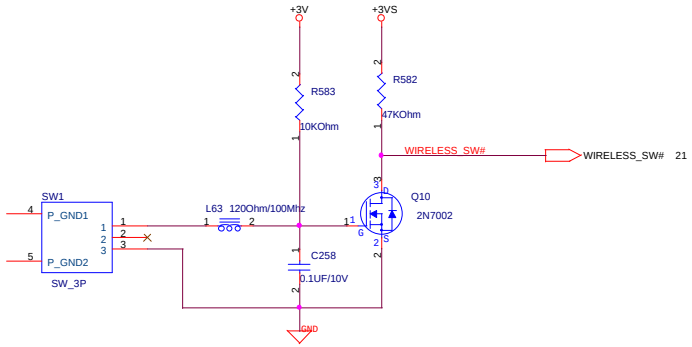


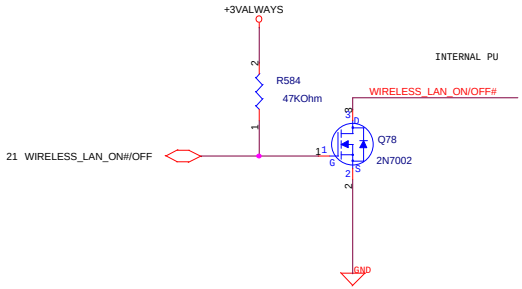
ASUSTeK COMPUTER INC	Title : ICH7-M (4/4)		
	Engineer: MICHAEL WANG		
Size: Custom	Project Name: S6F		Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 22 of 37		

POWER CONSUMPTION:
1). 3V < 550mA
2). 1.5V < 100mA

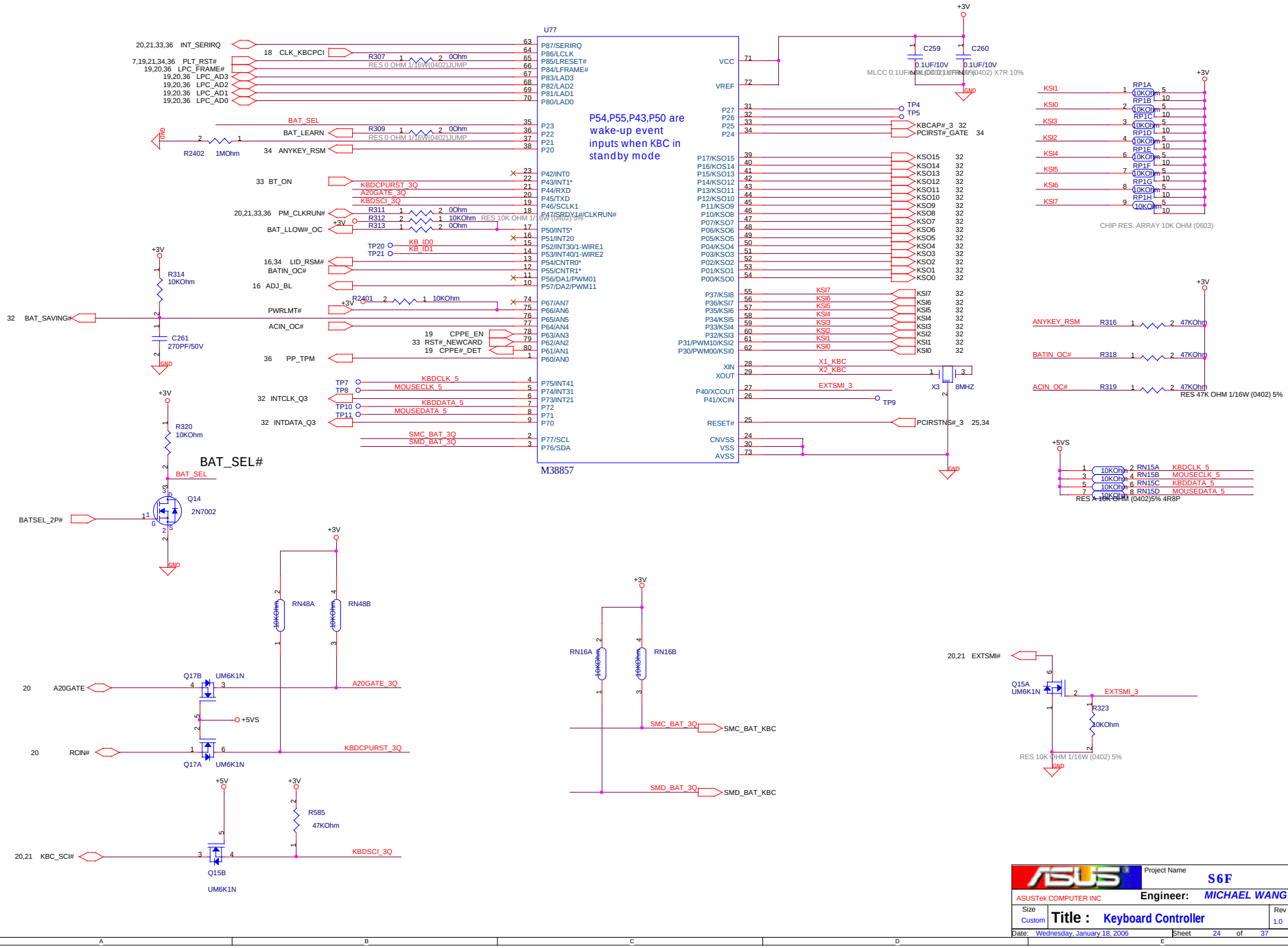
CLKREQ#(output) CLOCK REQUEST could be pull low



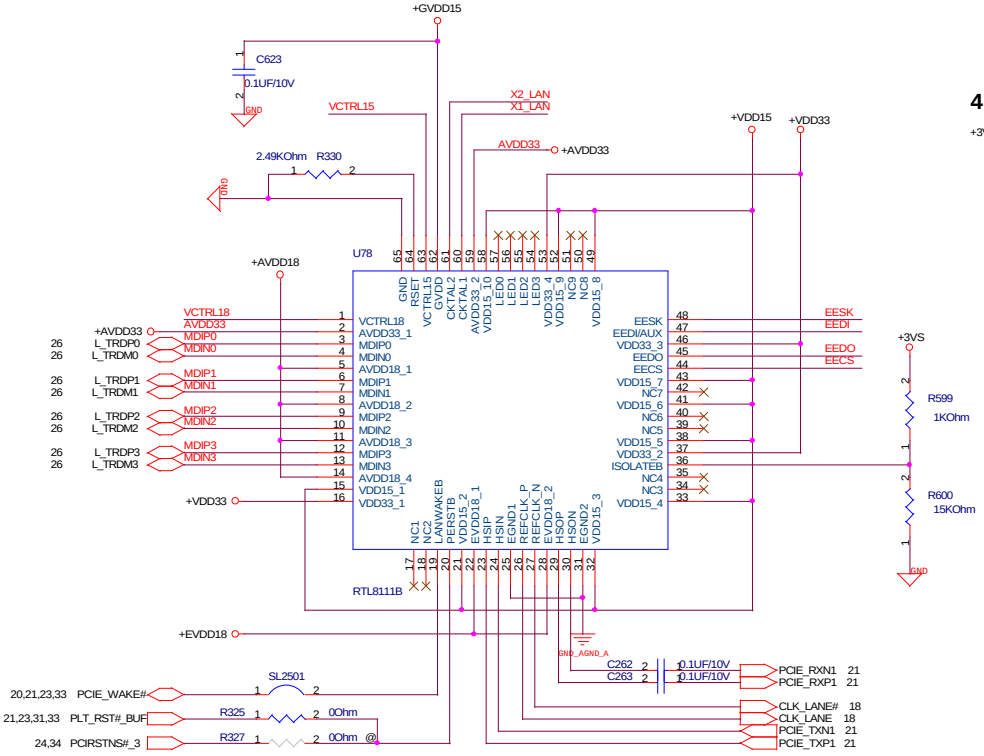


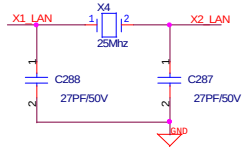


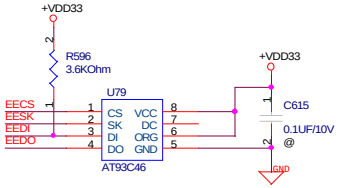
ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : MINI PCI	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 23 of 37	

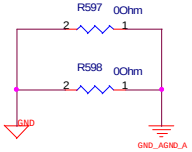


Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA

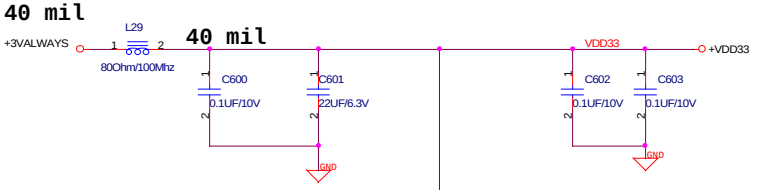




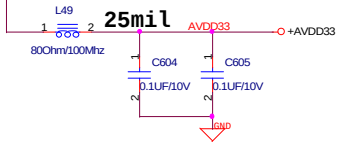




40 mil

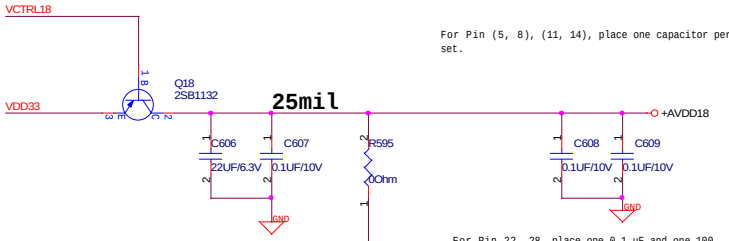


For Pin 2, 59, place one capacitor per pin.

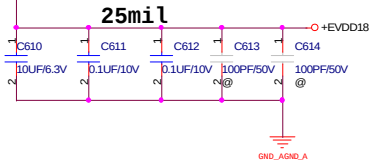


For Pin 16, 37, 46, 53, place one capacitor per pin.

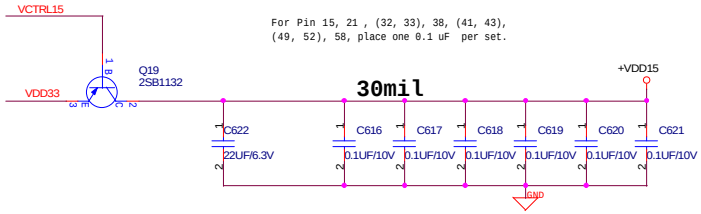
For Pin (5, 8), (11, 14), place one capacitor per set.



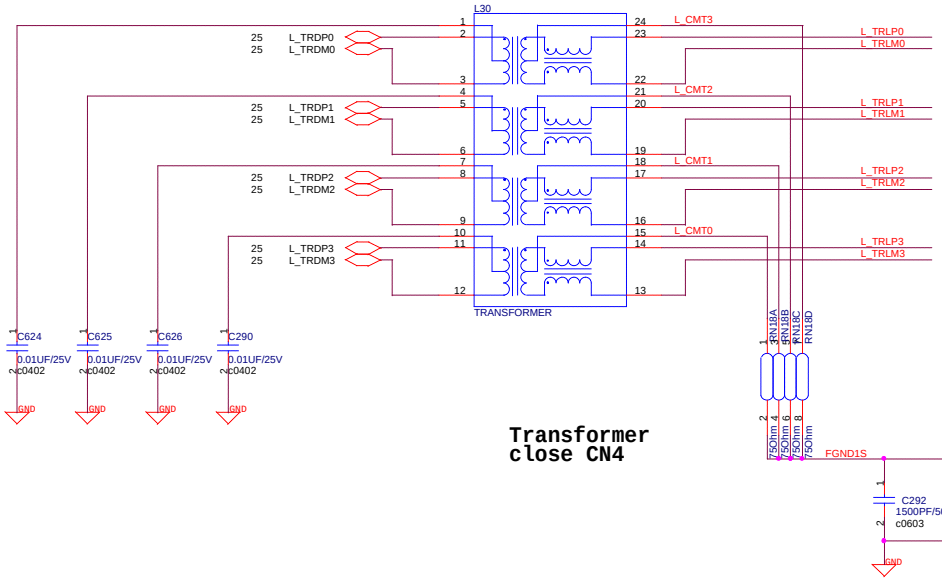
For Pin 22, 28, place one 0.1 uF and one 100 pF per pin.



For Pin 15, 21 , (32, 33), 38, (41, 43), (49, 52), 58, place one 0.1 uF per set.

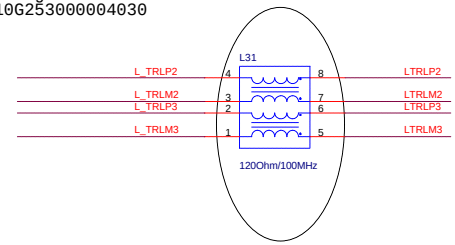


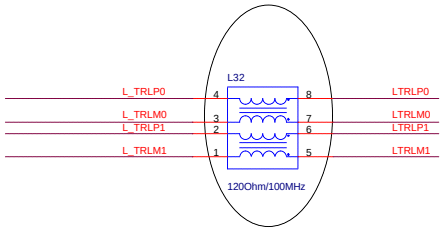
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Edmmund Hu	
Size: Custom	Title : Realtek RTL8111b	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 25 of 37	

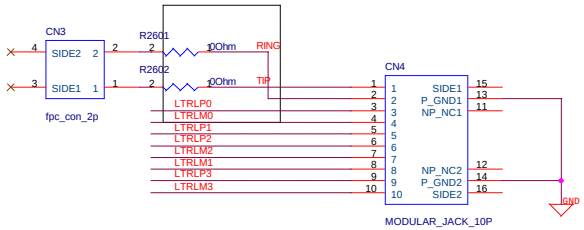


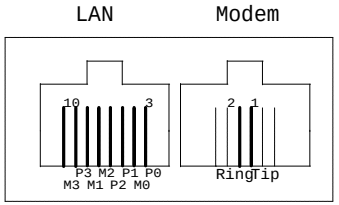
Transformer close CN4

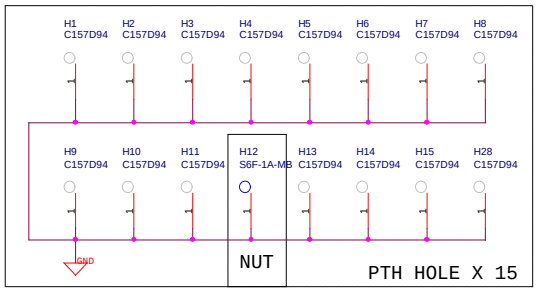
changed 09-091120000 to 10G253000004030

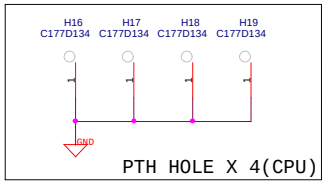


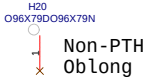


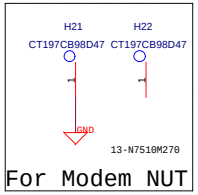


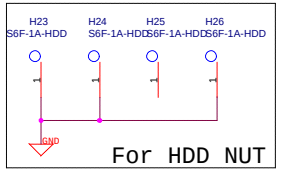




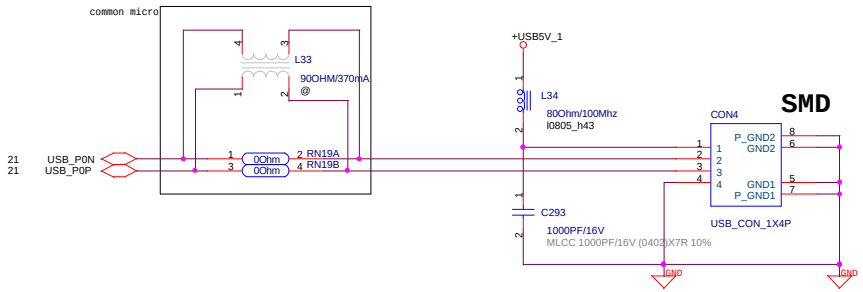


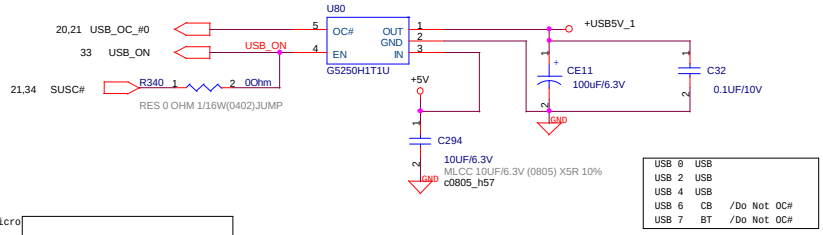




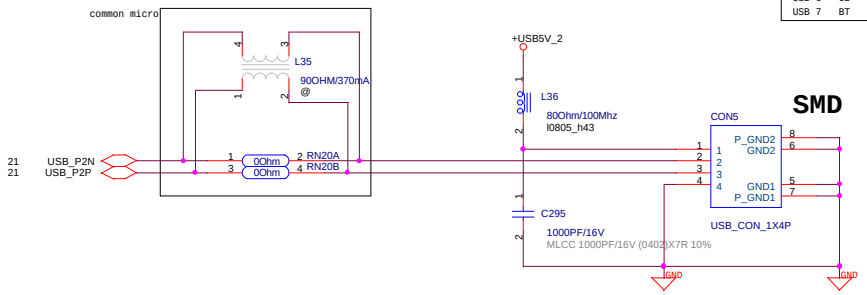


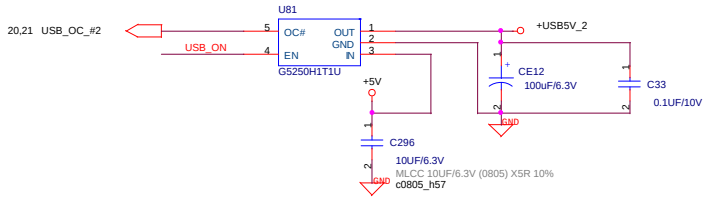
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : LAN I/O	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 26 of 37	

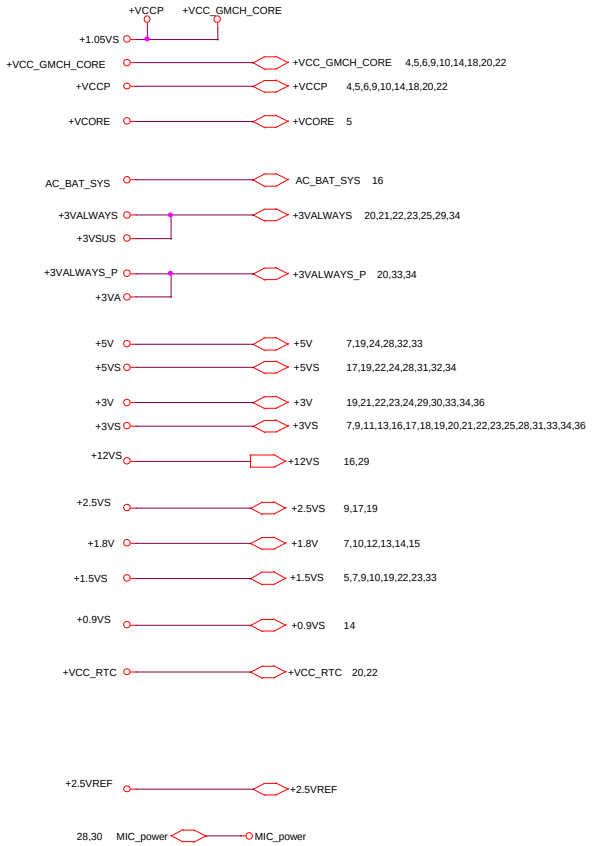





```
USB 0  USB
USB 2  USB
USB 4  USB
USB 6  CB   /Do Not OC#
USB 7  BT   /Do Not OC#
```

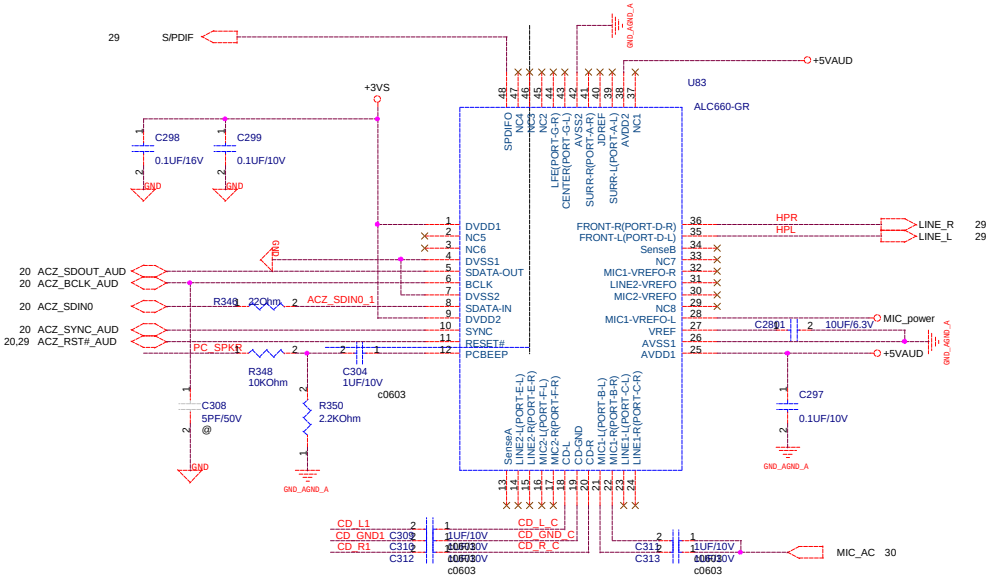


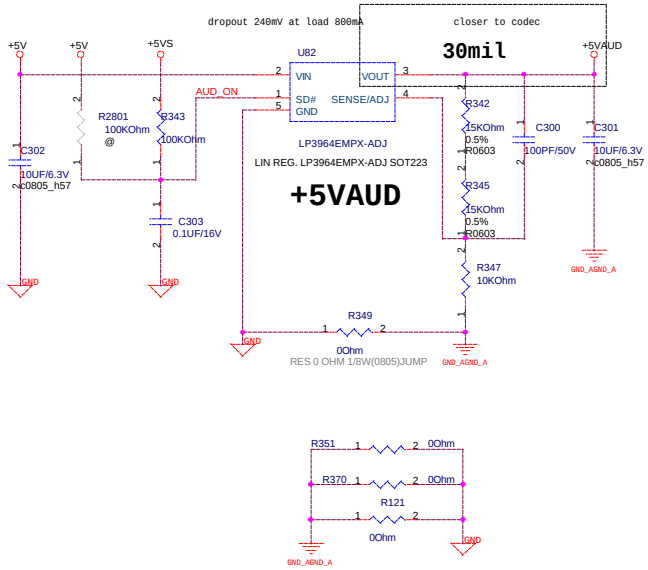


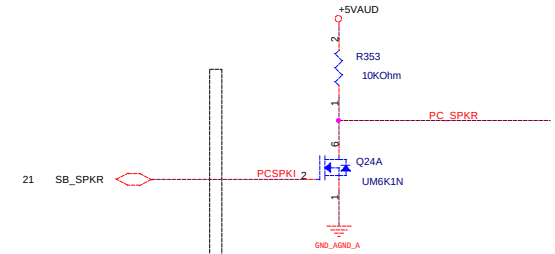


ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 27 of 37	

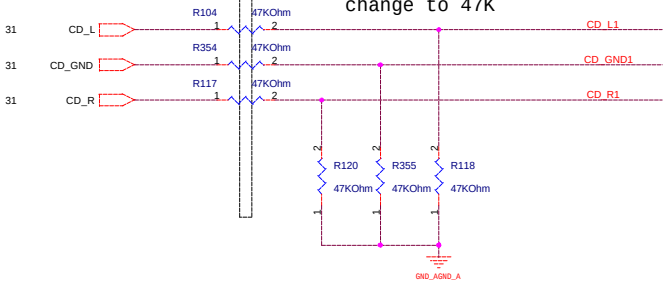
D0 (DVDD/AVDD) 15.5mA/45.9mA



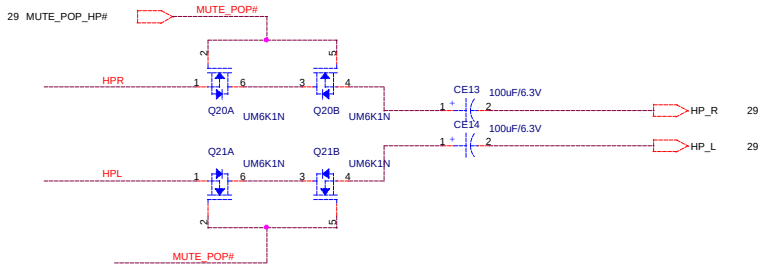




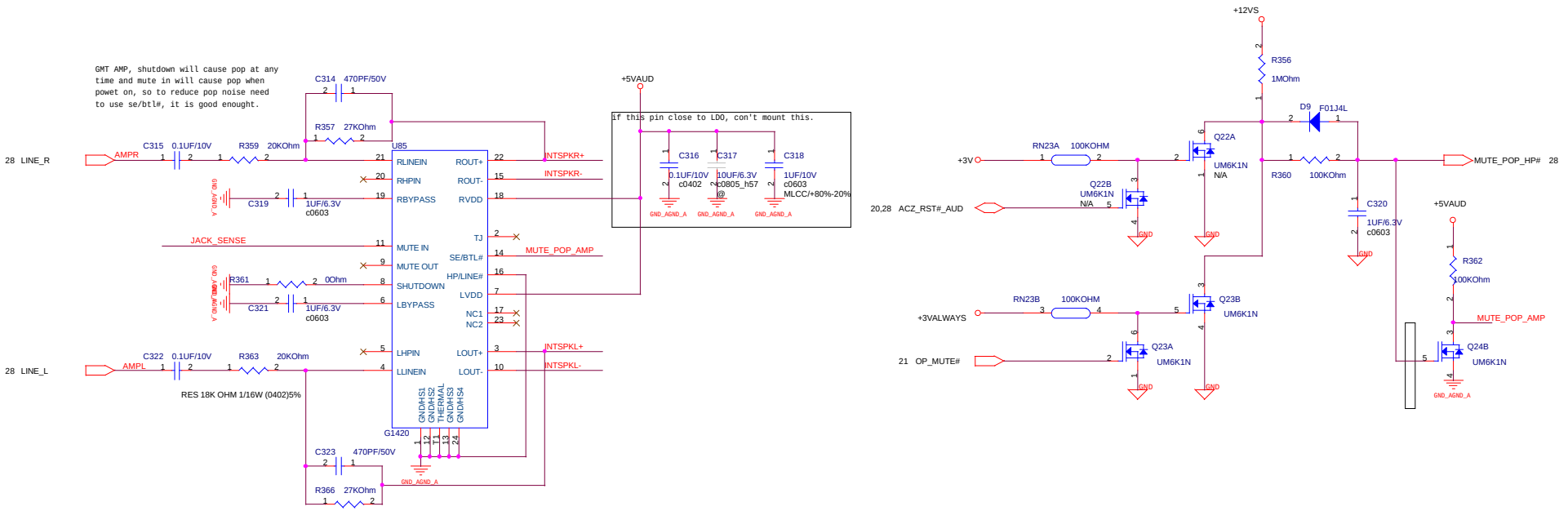
change to 47K



To HeadPhone



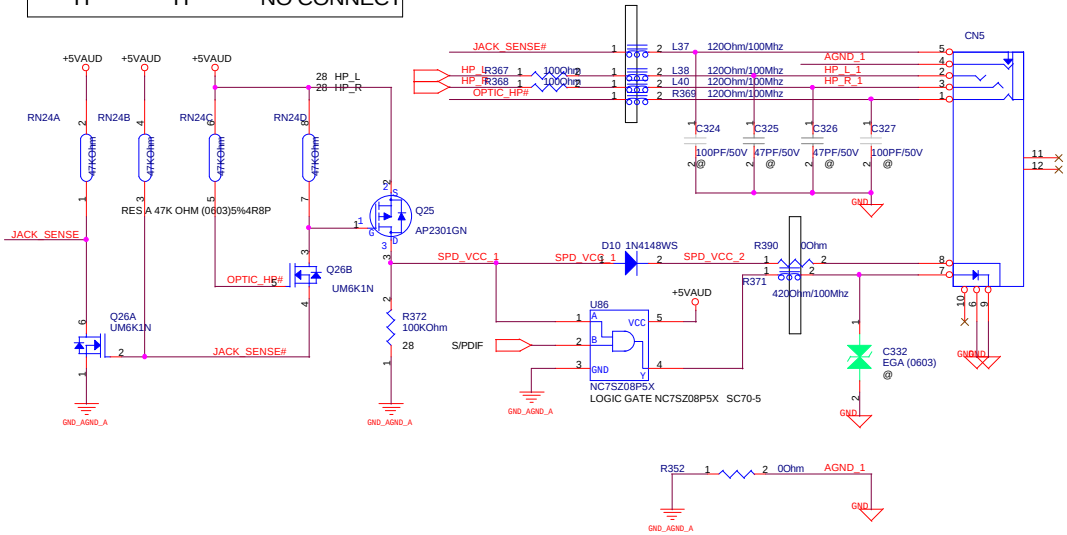
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : REALTEK ALC861	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 28 of 37	

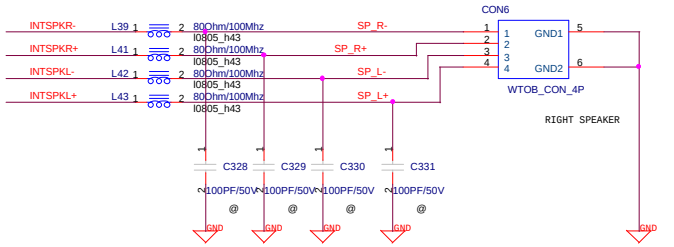


A

A

JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT

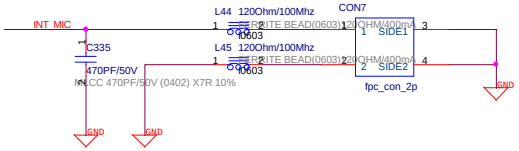


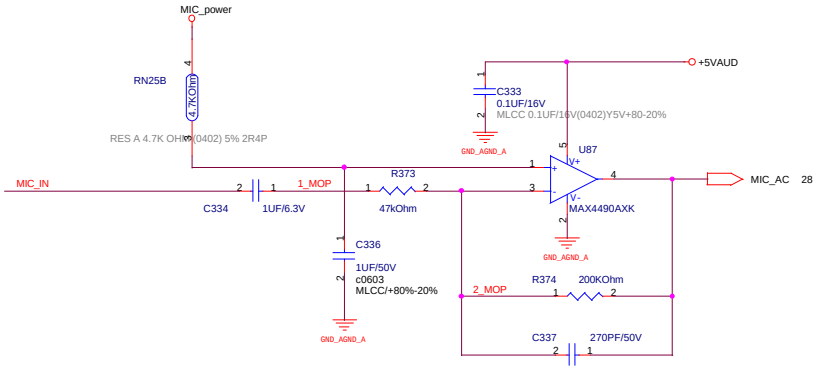


ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : AUDIO AMP	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 29 of 37	

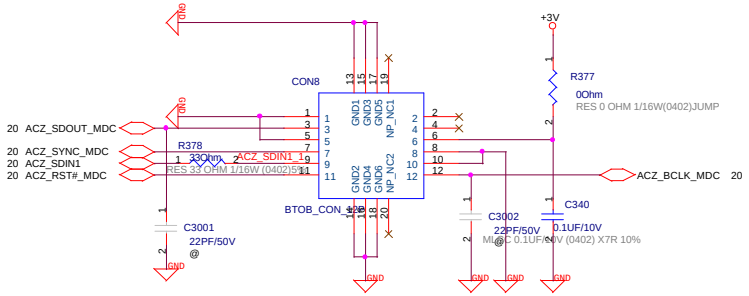
1

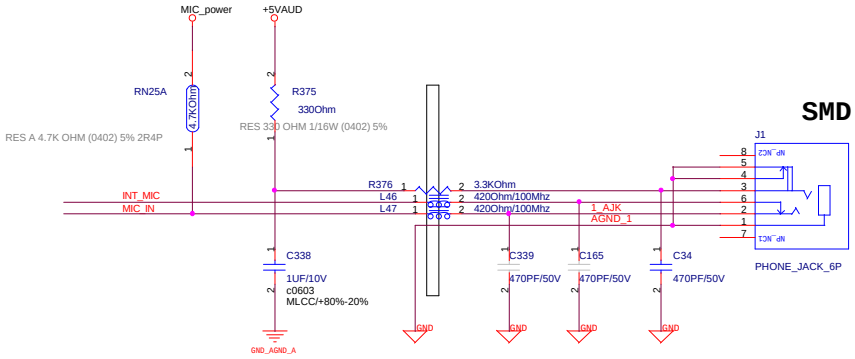
1



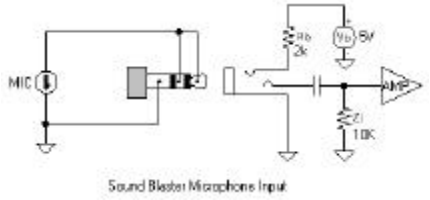


MDC CNT



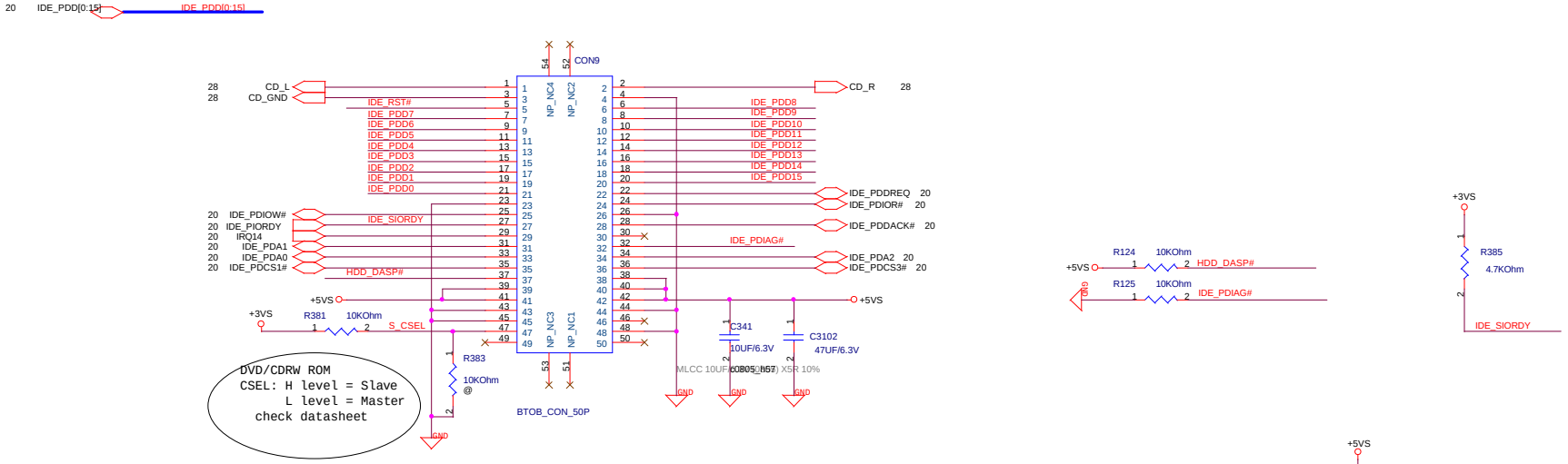


SMD

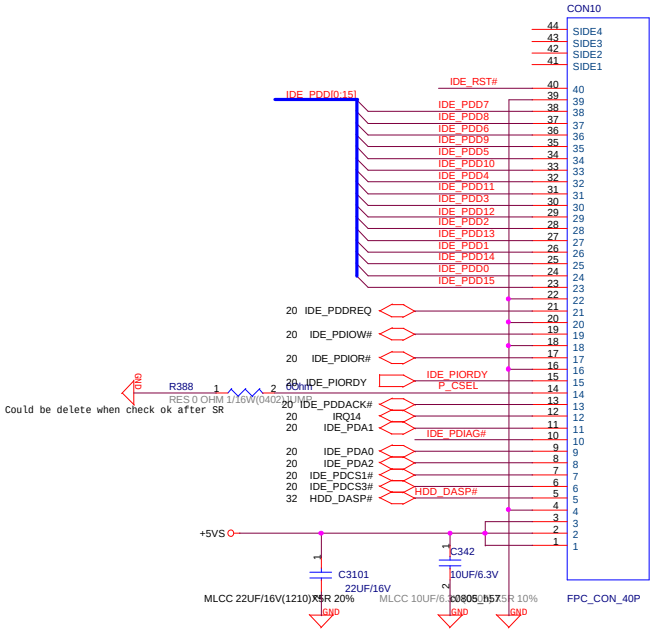


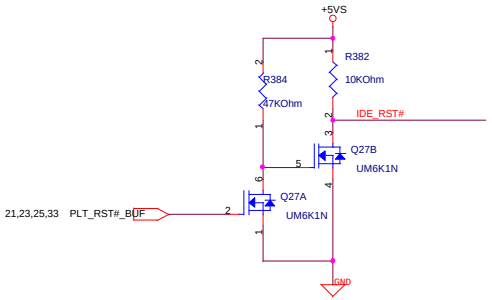
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : MDC CONN & LED	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 30 of 37	

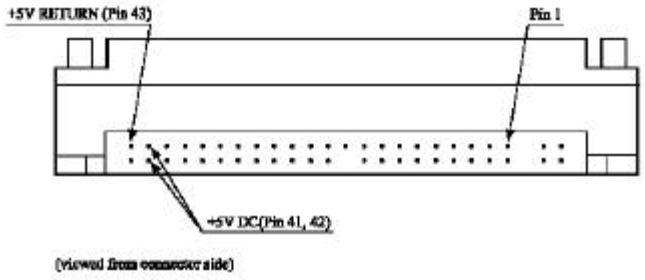
ODD CONNECTOR



HDD CONNECTOR

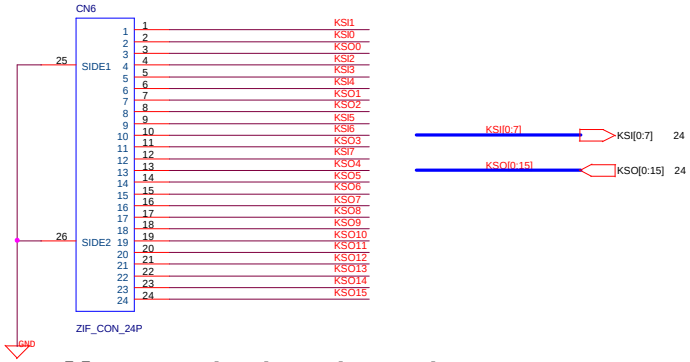






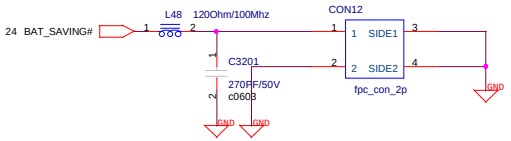
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	MICHAEL WANG	
Size: Custom	Title :	HDD/ODD CON.	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 31 of 37		

KEYBOARD CONN.

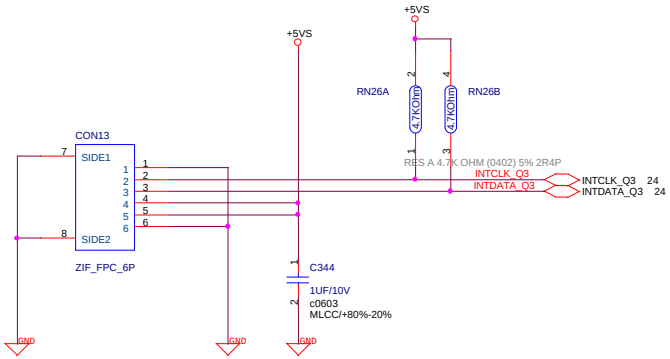


Follow J4A keyboard Matrix

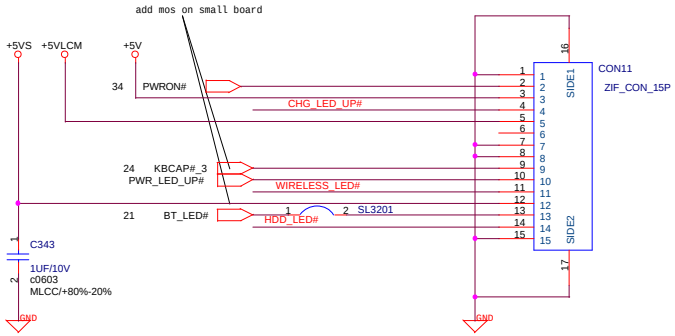
TO POWER4GEER SMALL BOARD

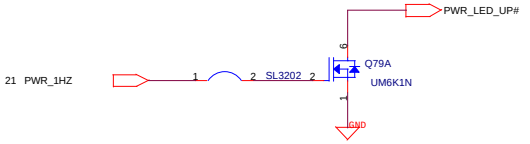


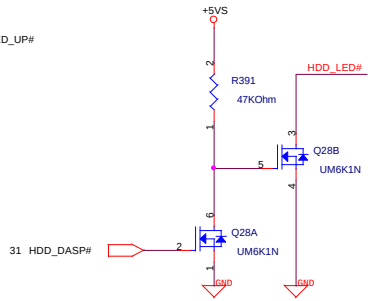
Touch PAD

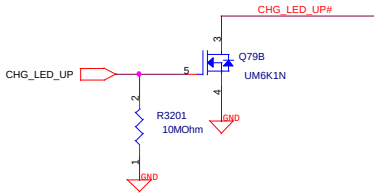


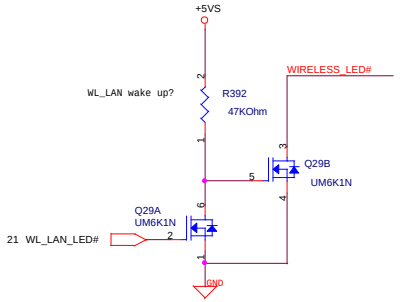
HotKey/PWRBT CON





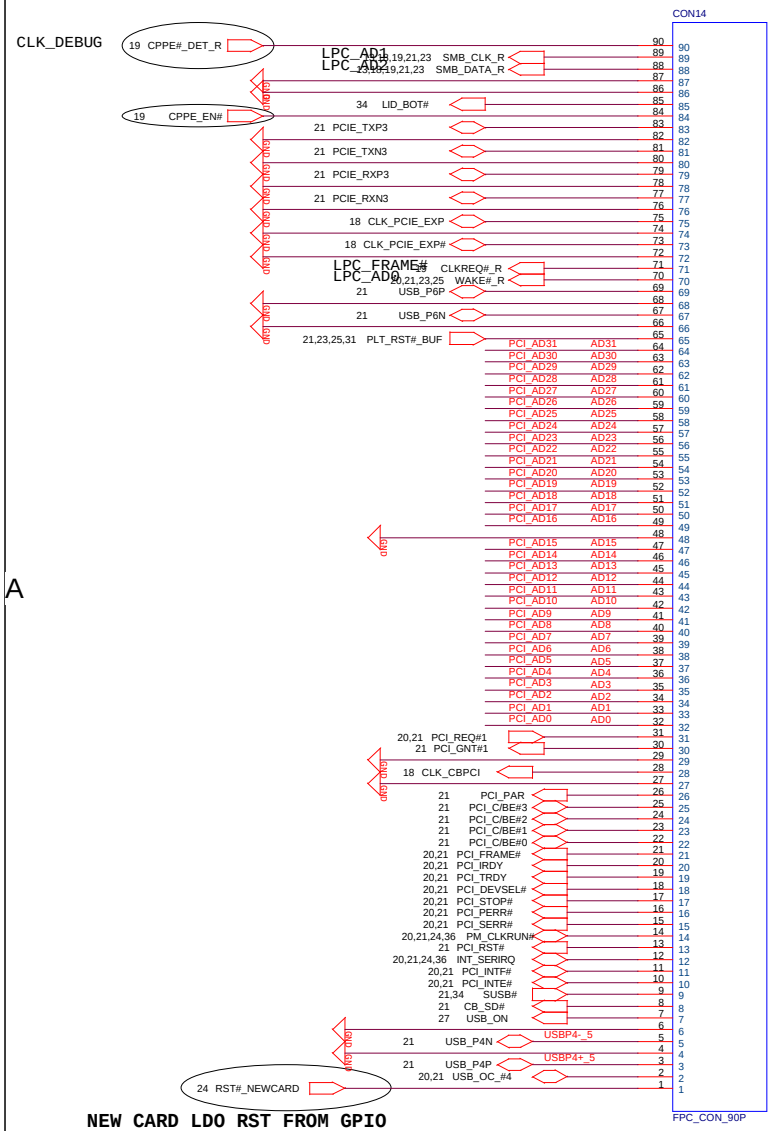






ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : DCIN Jack & PID & PCB_ID	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 32 of 37	

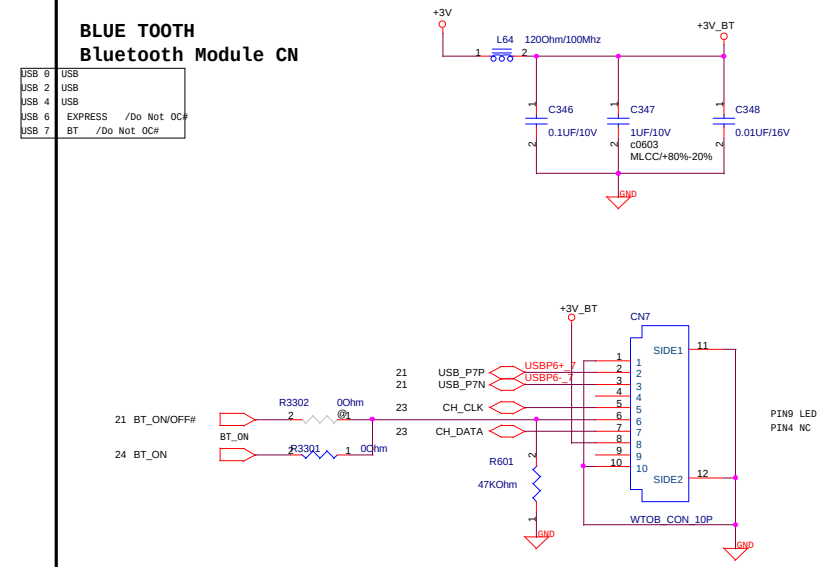
To I/O board connector (signal)



NEW CARD LDO RST FROM GPIO

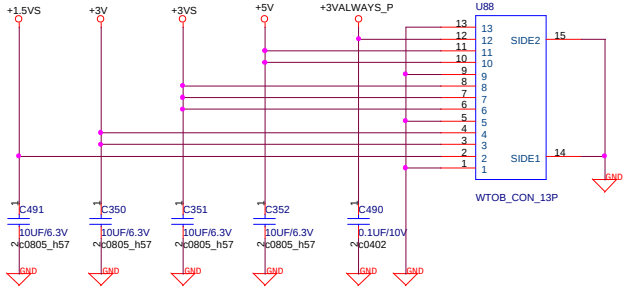
BLUE TOOTH
Bluetooth Module CN

USB 0	USB
USB 2	USB
USB 4	USB
USB 6	EXPRESS /Do Not OC#
USB 7	BT /Do Not OC#

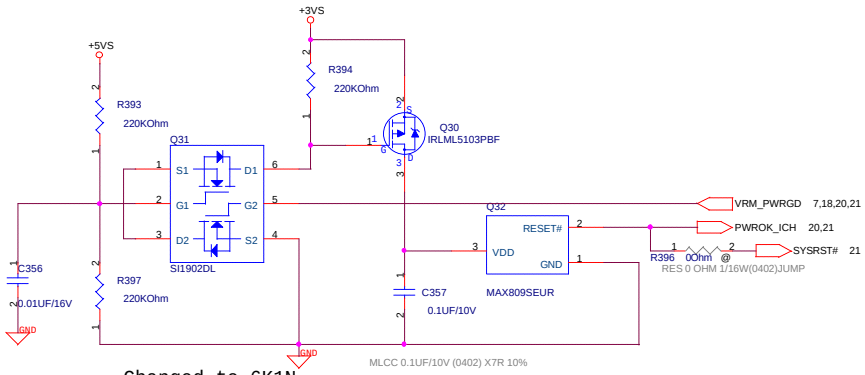


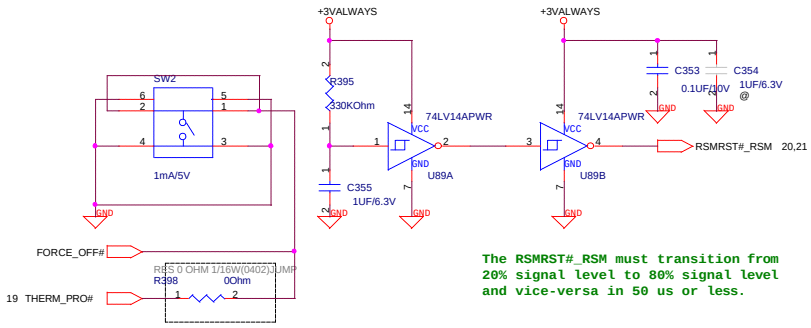
To I/O board connector (power)

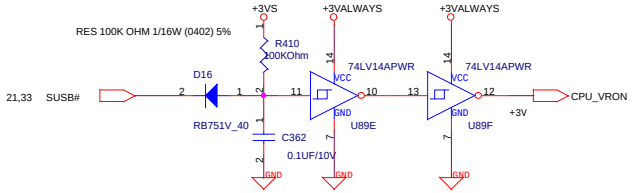
Check with io baord

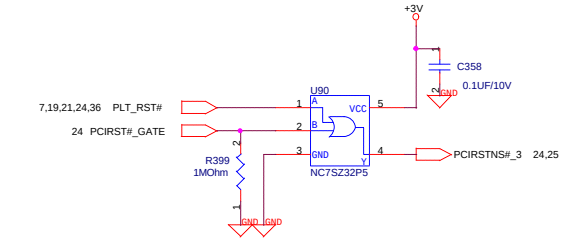


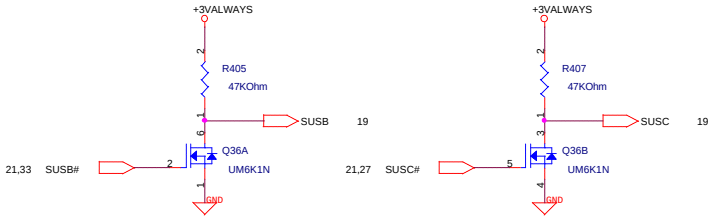
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	MICHAEL WANG	
Size: Custom	Title :	SMALL BOARD CON.	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet	33 of 37	

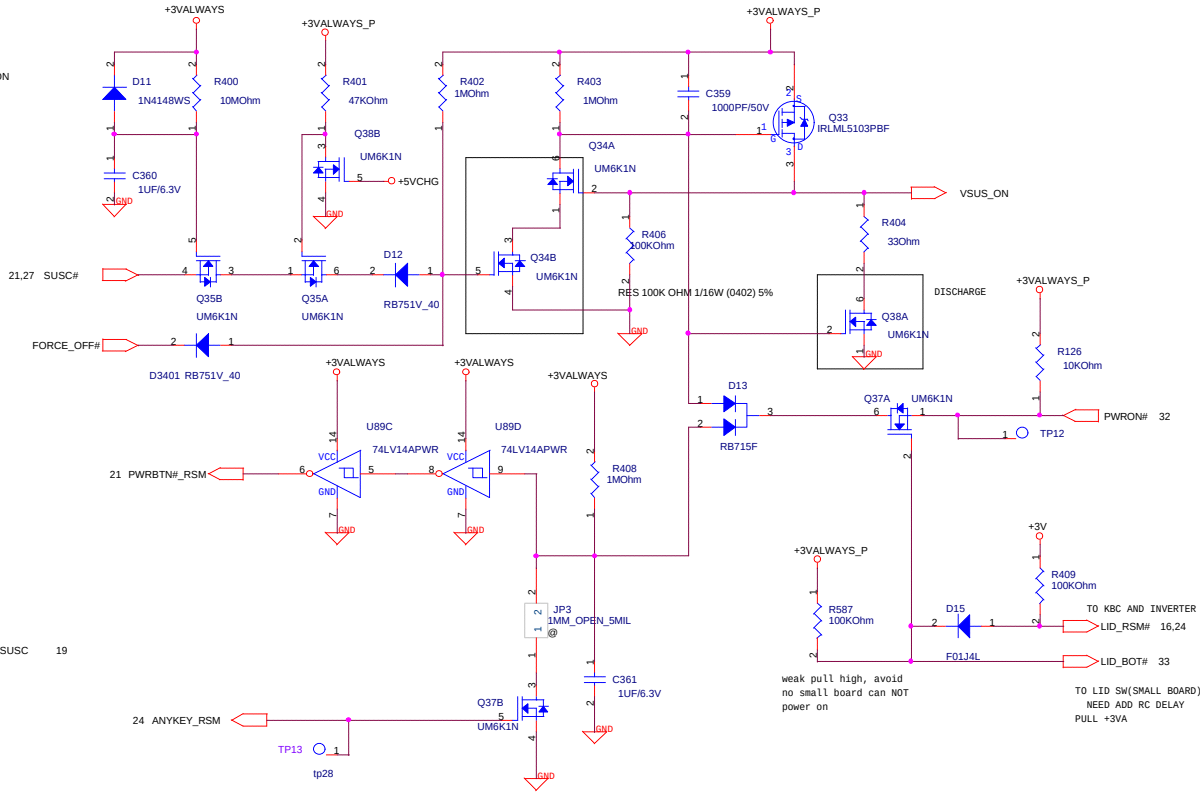








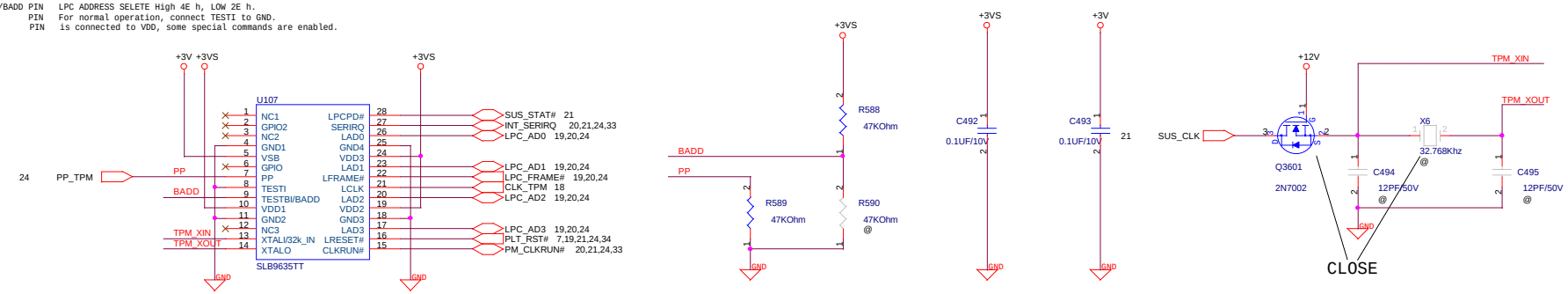




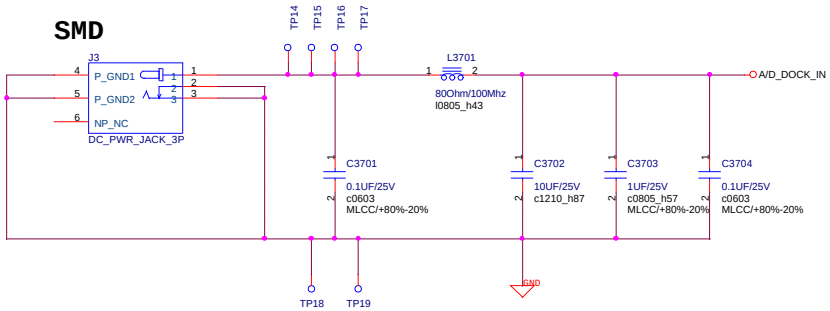
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : RESET SKT	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 34 of 37	

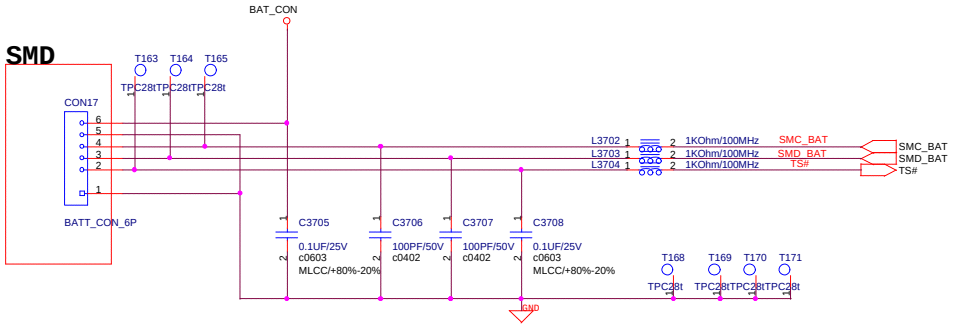
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title :	Audio DJ	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 35 of 37		

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.



ASUSTek COMPUTER INC	Project Name: S6A	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 36 of 37	





ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : DC IN	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 37 of 37	

Release S6F R1.0 on AUG, 2005
S6F R1.1

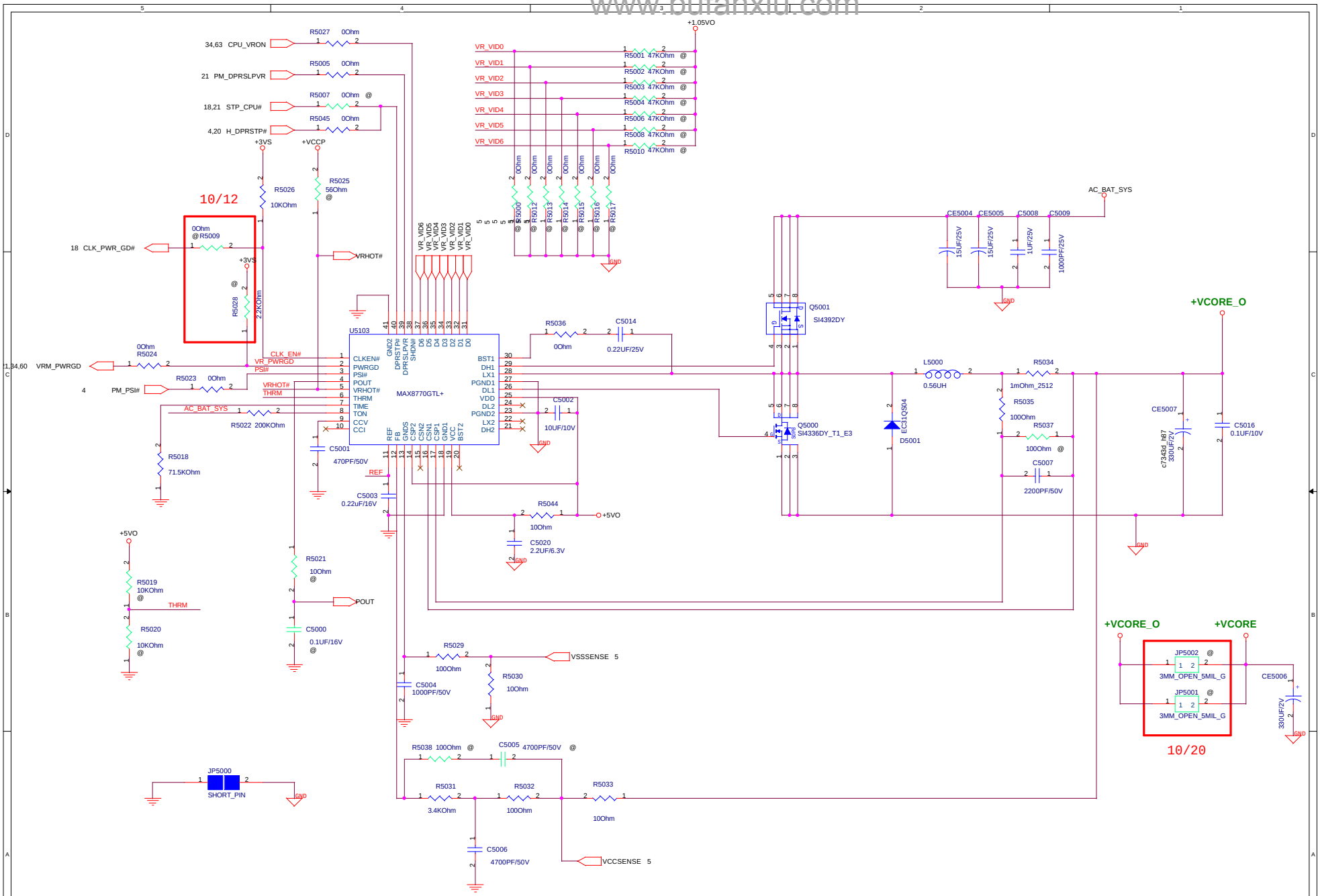
short pad footprint:
shortpin_sl

1. Delete assistance power led(for power on led delay), delete D49 D48 Q81 Q80 R591~R593 C496 and U92B in Page 36, and delete net PWRON_LED#.
2. Delete AUDIO DJ FUNCTION, delete D14 in page 34 and delete all coomponents in page 35.
   Delete net SWDJ_EN#, PWR_DJ_ON#, DJ_SCAN AND DJ_SW_BTN#.
3. In page 4, to mount R16 56 Ohm for "can not boo tissue".
4. In page 16. modify LCD discharge circuit, repleacemnet of diode by 2N7002, and we swap LCD con. pin defined for ME rotation CON 1.
5. In page 22, for +3VALWAYS leakage to +5V, we delete Q12, Q13, R299 and R300. And R297 pull high to +5VSUS.
6. In page 25, R599 pull high to +3Vs for lan con not wake-up from S3 ....
7. In page 27, we repleacemant of G5250 by G5251, u80 u81.
8. In page 31, we delete RN49 and RN50, add R124&R125.WIRE-OR IDE_PDIAG# AND IDE_SDIAG# ,WIRE-OR
   HDD_DASP# AND CDROM_DASP#, FOR HDD AND CD CAN NOT WORK AT THE SAME TIME.
9. In page 33, con13 connector changed 6pin for 15pin for remove audio DJ.
10. In page 34, add R126 and pull high +3VALWAYS_P for PWR_BTN# can not work stable.
11. In page 20&36, X2&X6 07G010313271 CM519 32.768000KDZFTR instead of ORIGINAL.(x6 OPTION)
12. Added Debug circuit for Express debug card.
13. In page 25, audio codce changed RTL660 for ADI 1986 .
14. In page 18, Added R1801 for MINICARD CLK_REQ .

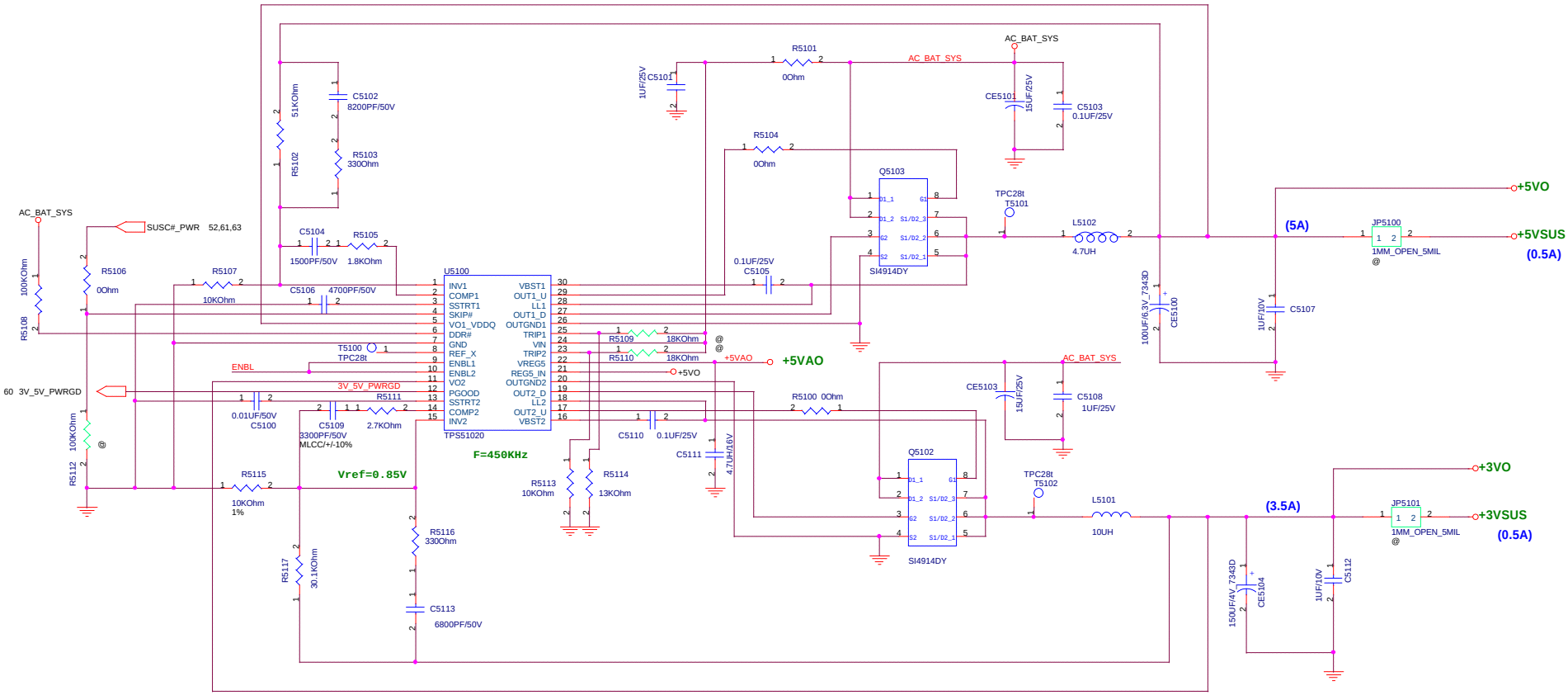
S6F R2.0

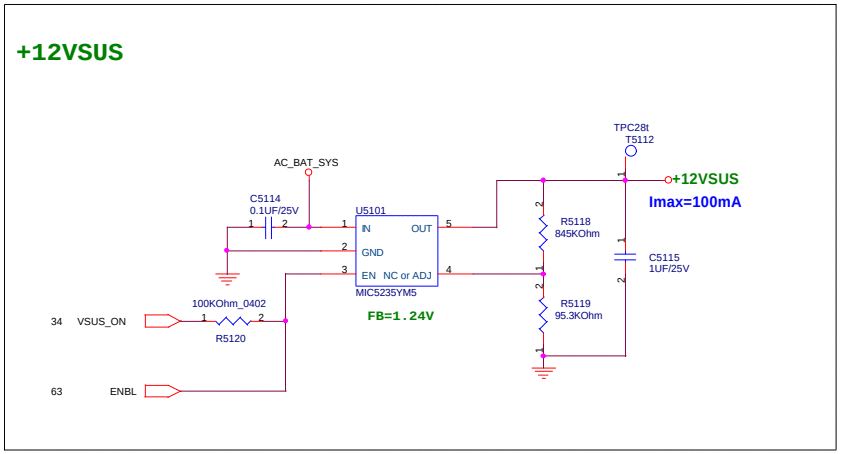
15. In Page 24, Q14 changed to 2N7002, and correct the route batsel_2p# throght Q14(nand get)to U77.35.(Not barsel_3s# to
    U77.37. U77.37 need pull down resistor R2402(1M Ohm)
16. In page 24, for S3 resume issue, reserve a BT ON route from EC(U77.22) and R3301 R3302.
    (added R3301 R3302 and net BT_on from EC)
17. In page 32&24, for deleted TP_led function, we deleted Q14B.refer item 15.
18. In page 12, added c1201 and c1202 on +1.8V.
19. In page34, reset circuit modify, R395 and C355 close to U89 and added D3401 to avoid restart itself after push reset botton.
20. In page36, added Q3601 to replease R608 to avoid +3Va(susclock) leakage to +3V.
21. In page 19&33, deleted debug citcuit of PCIE, delete ic1901, c1901 and sl3301
22. In page 26, LAN connector change ner part, and added R2601 R2602 for EMI
23. In page 37, DC_IN CON changed new part
24. In page 32, added R3201 pull low CHG_LED_UP to avoid indetermination state.
25. Update new foorprint of JP and short pad for GA process.
26. In page 32, internel speaker route replacemant of PIN 39&41 by Pin 35&36 to avoid non-pcbeep to speaker.
27, In page 16,added C1601 for EMI
28, C163 change Net into LCD_+3VS
29, N19145985 reserve 1pcs cap.

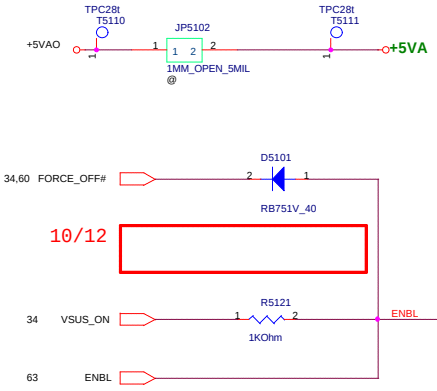
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: C	Title : History	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 38 of 37	

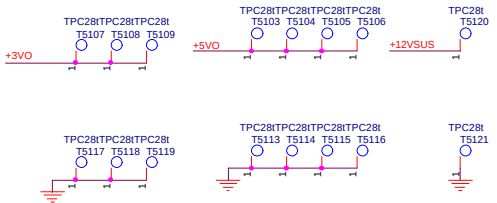


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **Vcore Power**	DESIGN ENGINEER :
		SHEET **50** OF **63**		RELEASE DATE :	

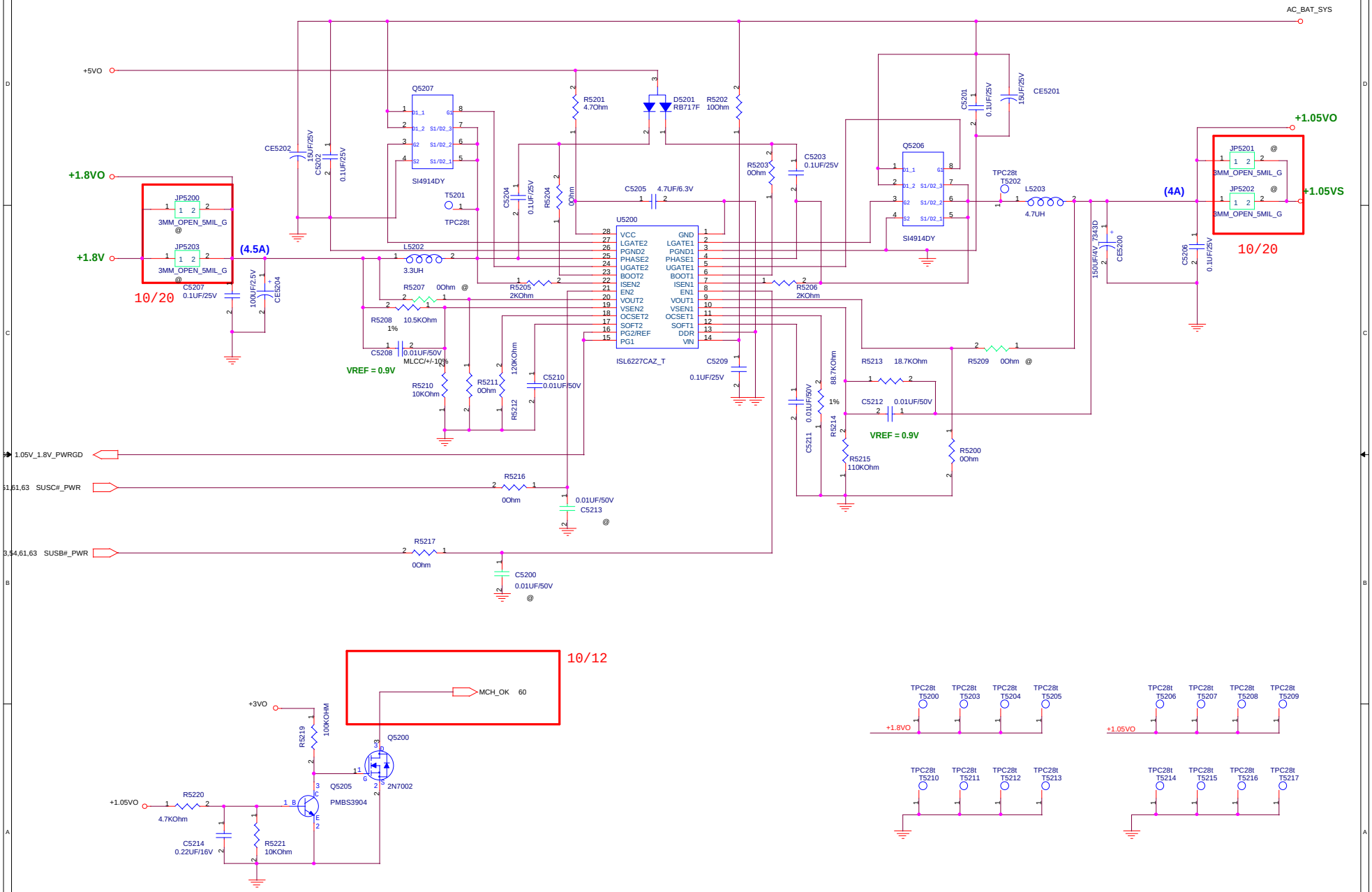




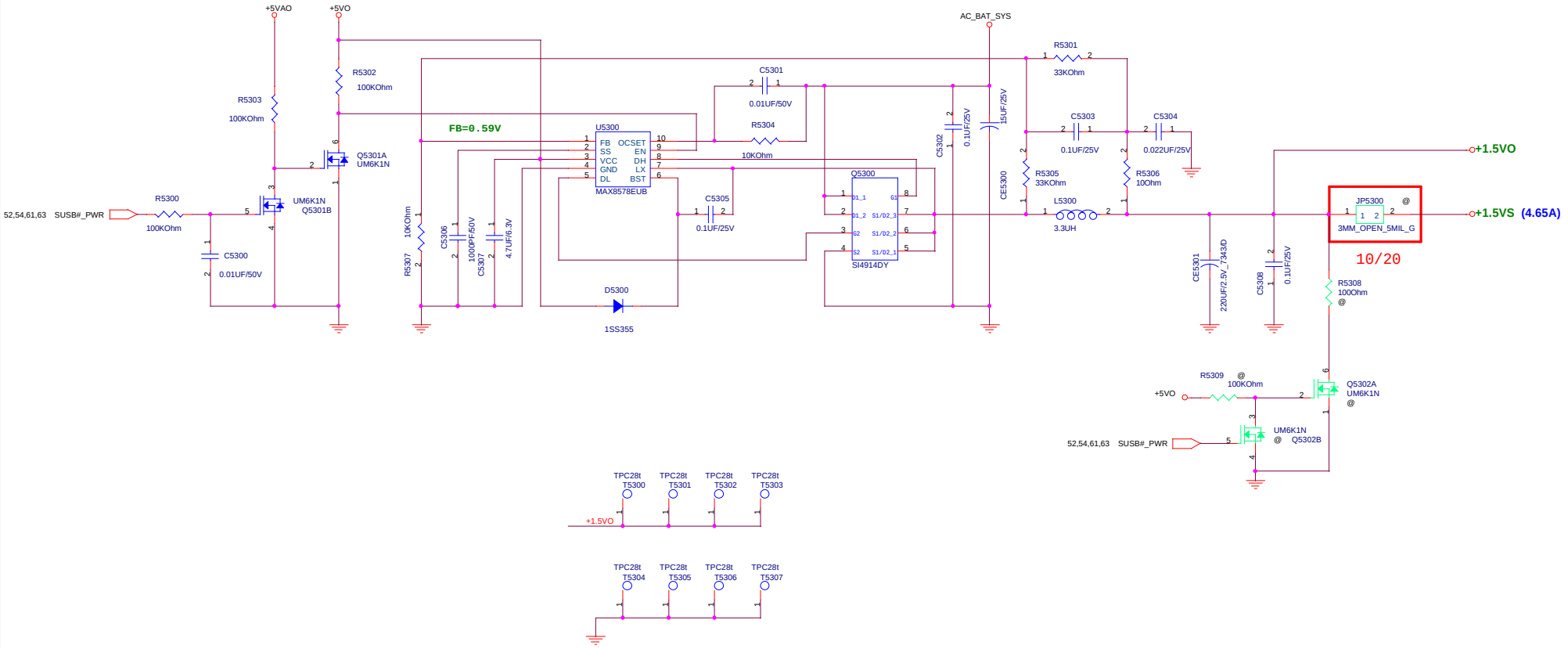




PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME : System Power	DESIGN ENGINEER :
		SHEET 51 OF 63		RELEASE DATE :	

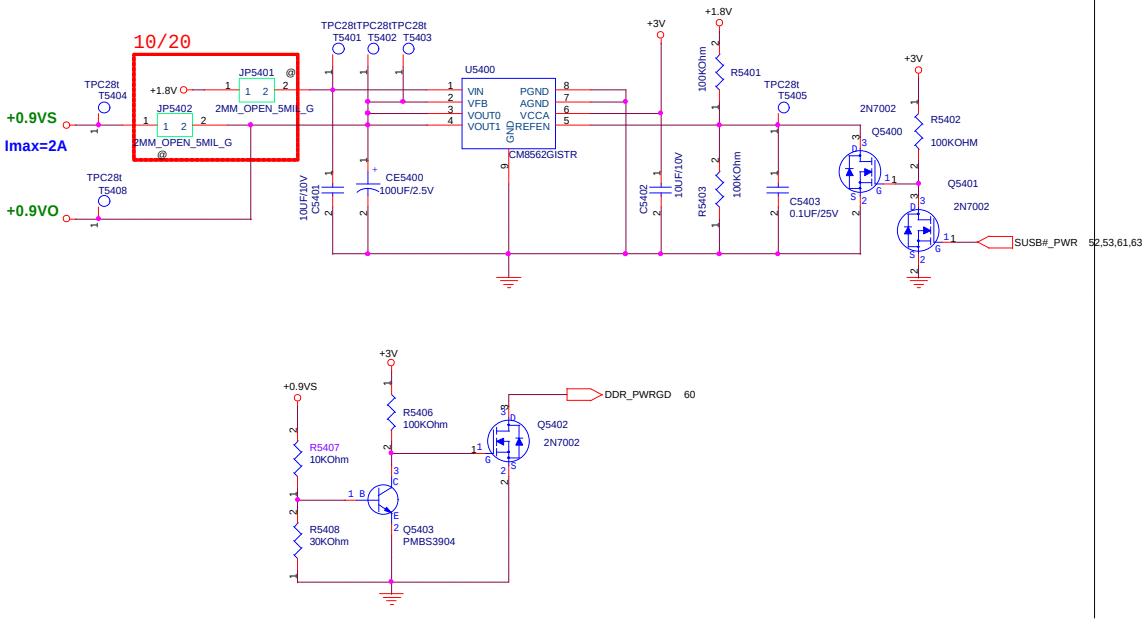


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **1.05VS & 1.5VS**	DESIGN ENGINEER :
		SHEET **52** OF **63**		RELEASE DATE :	

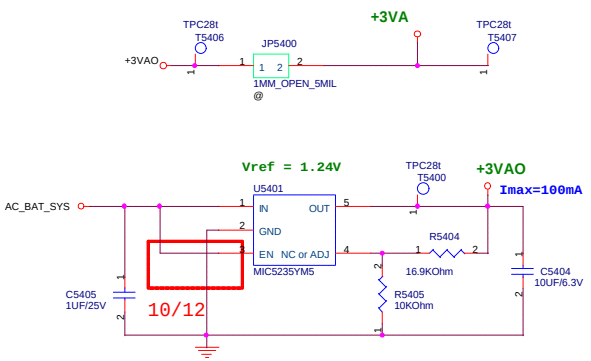


PROJECT: **S6F**	REVISION: **2.0**	DATE: Wednesday, January 18, 2006	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **1.8V & 0.9VS**	DESIGN ENGINEER :
		SHEET **53** OF **63**		RELEASE DATE :	

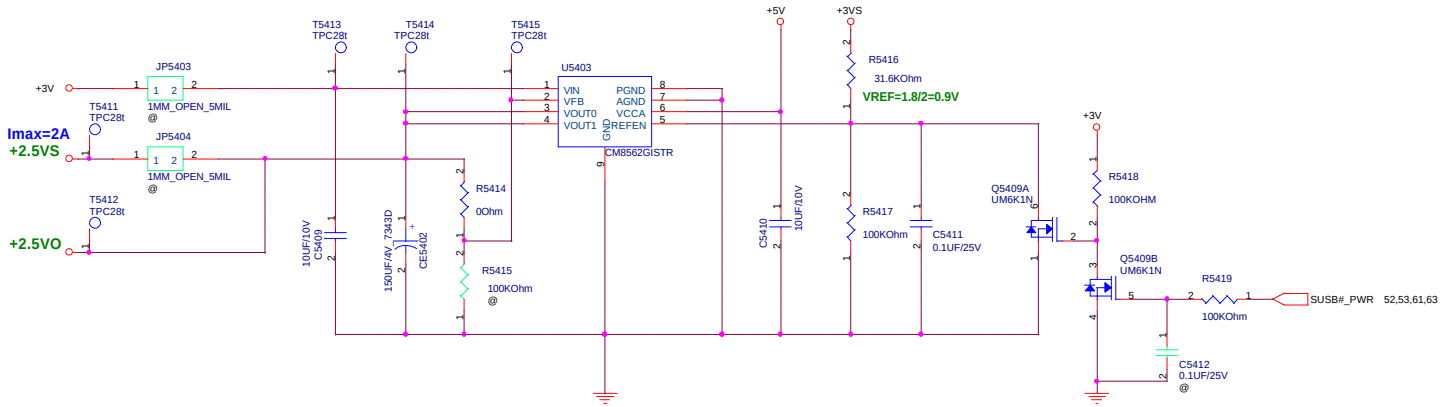
DDR-->VTT



+3VAO



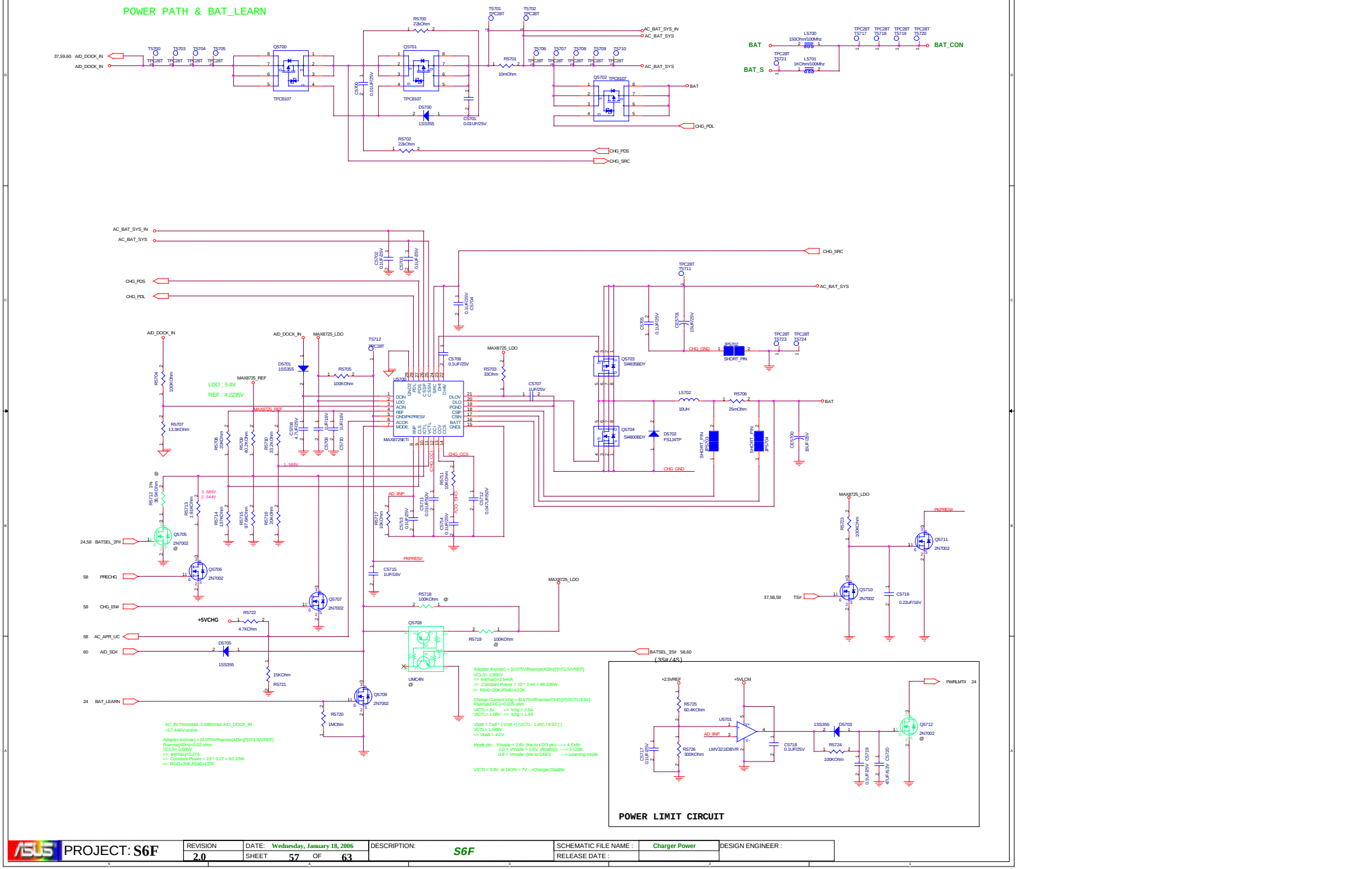
+2.5VS



PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME : Oterh Power	DESIGN ENGINEER :
		SHEET 54 OF 63		RELEASE DATE :	

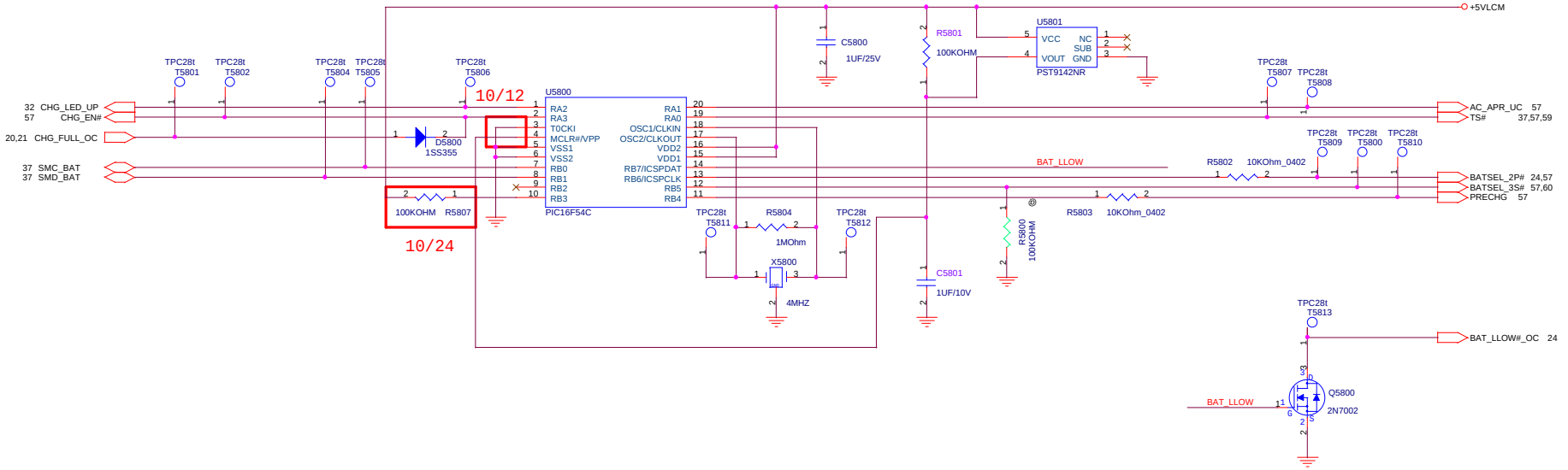
PROJECT: **S6F**	REVISION: **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **VGA CORE**	DESIGN ENGINEER :
		SHEET **55** OF **63**		RELEASE DATE :	

PROJECT: **S6F**	REVISION: **2.0**	DATE: **Wednesday, January 18, 2006** SHEET **56** OF **63**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **VGA RAM** RELEASE DATE :	DESIGN ENGINEER :



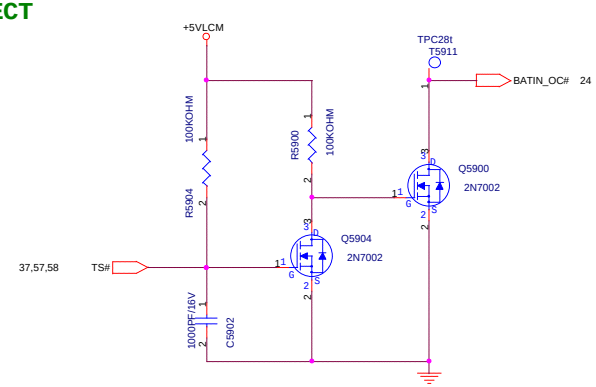
PROJECT: S6F	REVISION: 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME :	Charger Power	DESIGN ENGINEER :
		SHEET 57 OF 63		RELEASE DATE :		

PIC16C54C

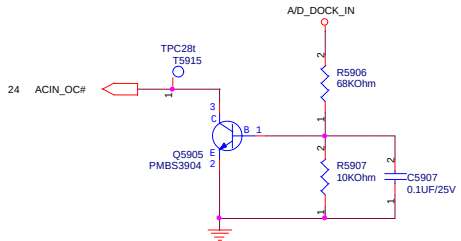


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **PIC**	DESIGN ENGINEER :
		SHEET **58** OF **63**		RELEASE DATE :	

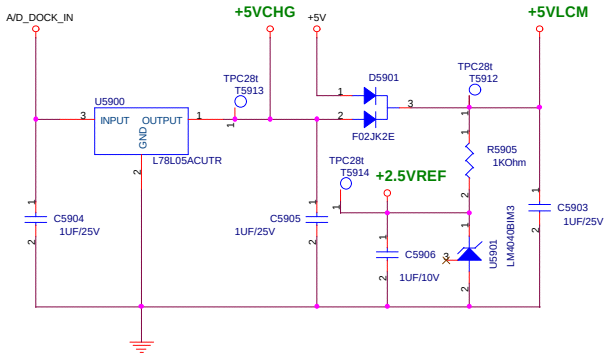
BATTERY IN DETECT



ADAPTER IN DETECT

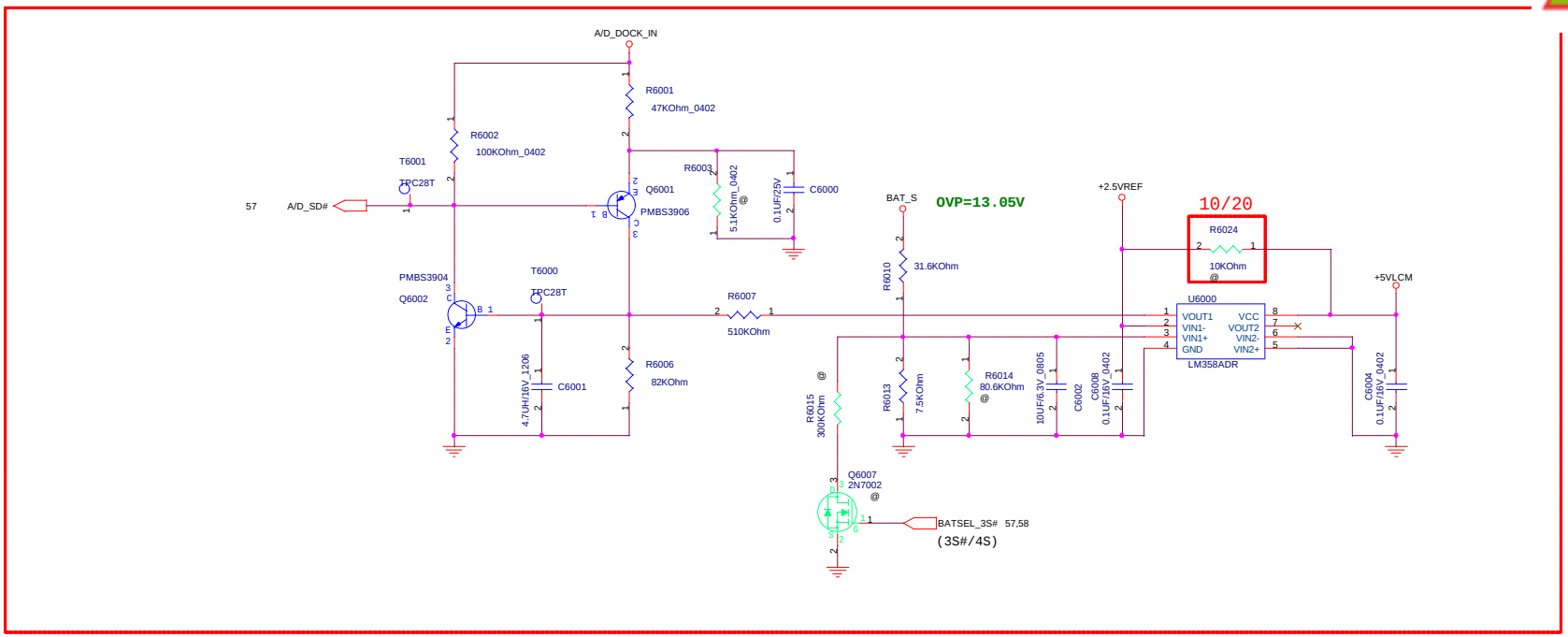


+5VLCM, +5VCHG & +2.5VREF

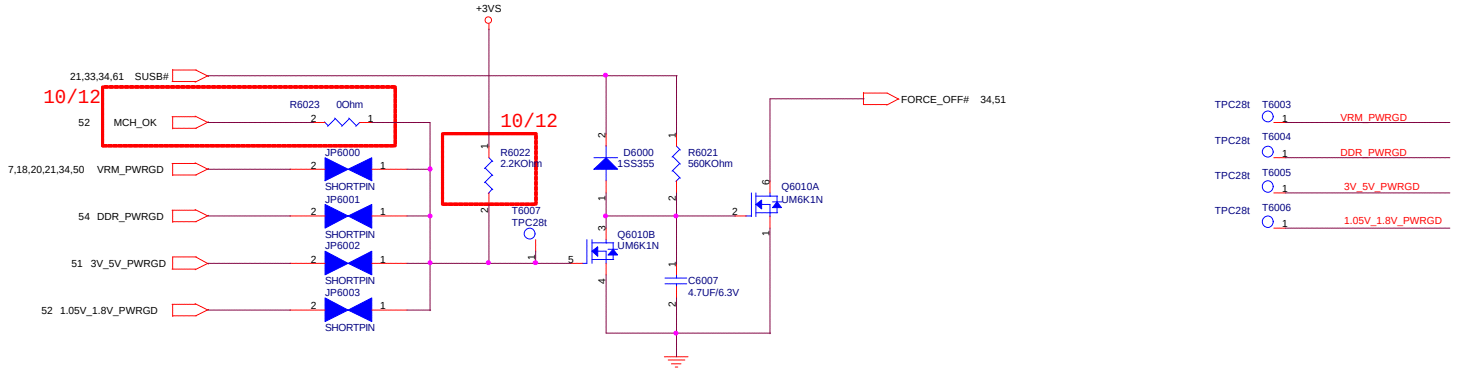


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **Selector**	DESIGN ENGINEER :
		SHEET **59** OF **63**		RELEASE DATE :	

BATTERY A/D_SD# (OVP)

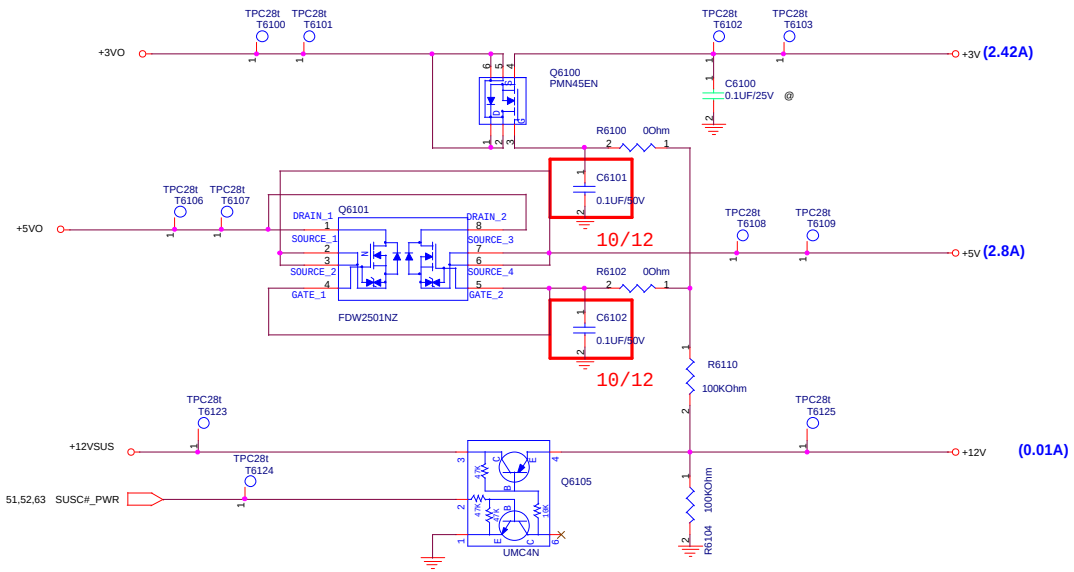


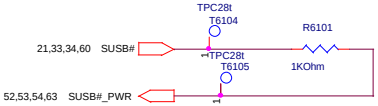
POWER GOOD DETECTER



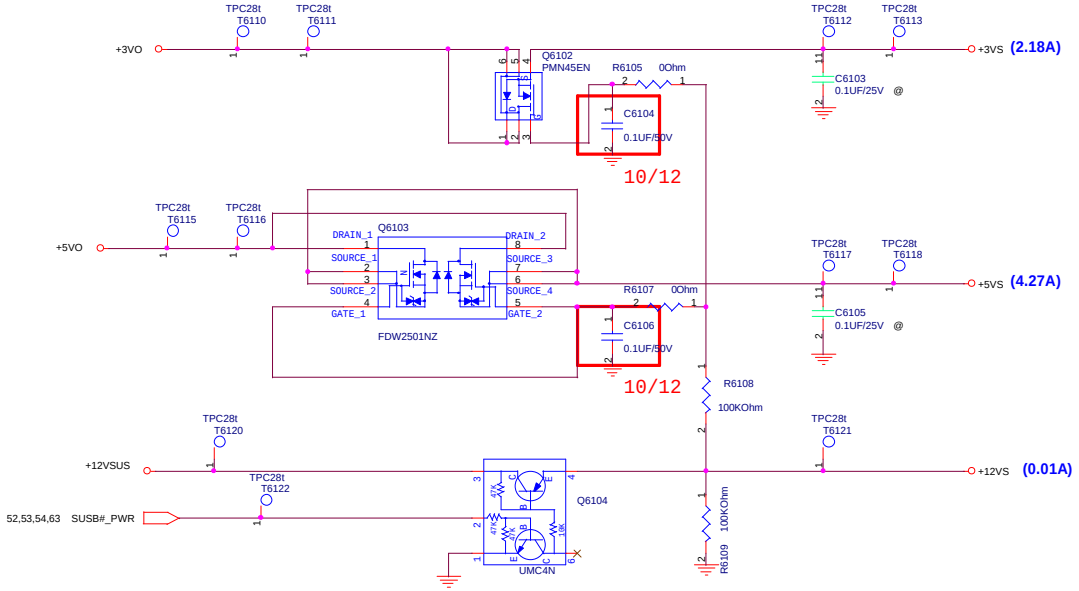
PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME : BATLOW/SD#	DESIGN ENGINEER :
		SHEET 60 OF 63		RELEASE DATE :	

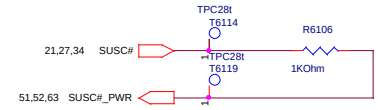
SUSC#_PWR POWER



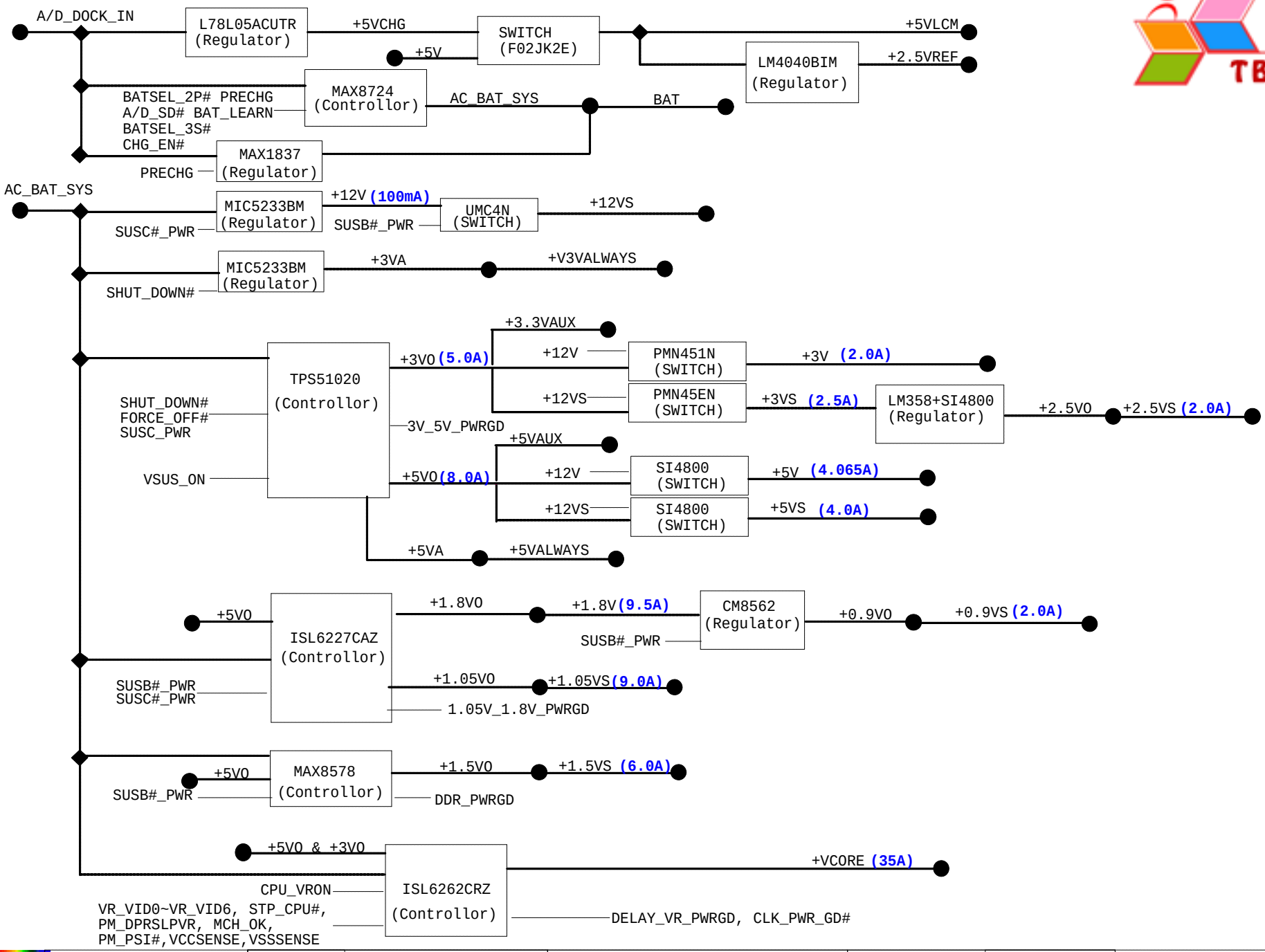


SUSB#_PWR POWER



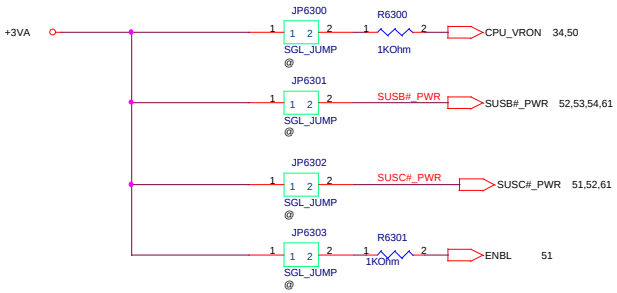


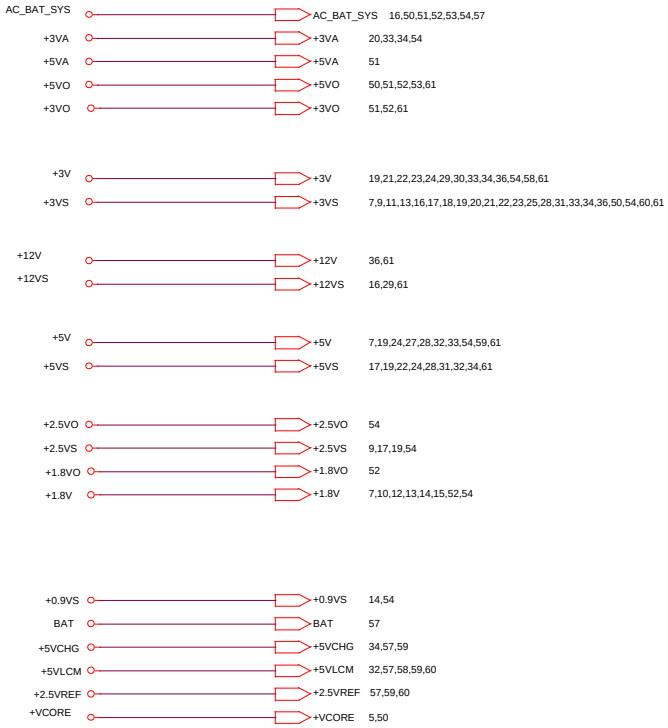
PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME :	LOAD SWITCH	DESIGN ENGINEER :
		SHEET 61 OF 63		RELEASE DATE :		



PROJECT: S6F	REVISION: 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME: Flowchart	DESIGN ENGINEER:
		SHEET 62 OF 63		RELEASE DATE:	

FOR POWER TEST





PROJECT: **S6F**	REVISION **2.0**	DATE: Wednesday, January 18, 2006	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **SIGNAL**	DESIGN ENGINEER :
		SHEET **63** OF **63**		RELEASE DATE :	