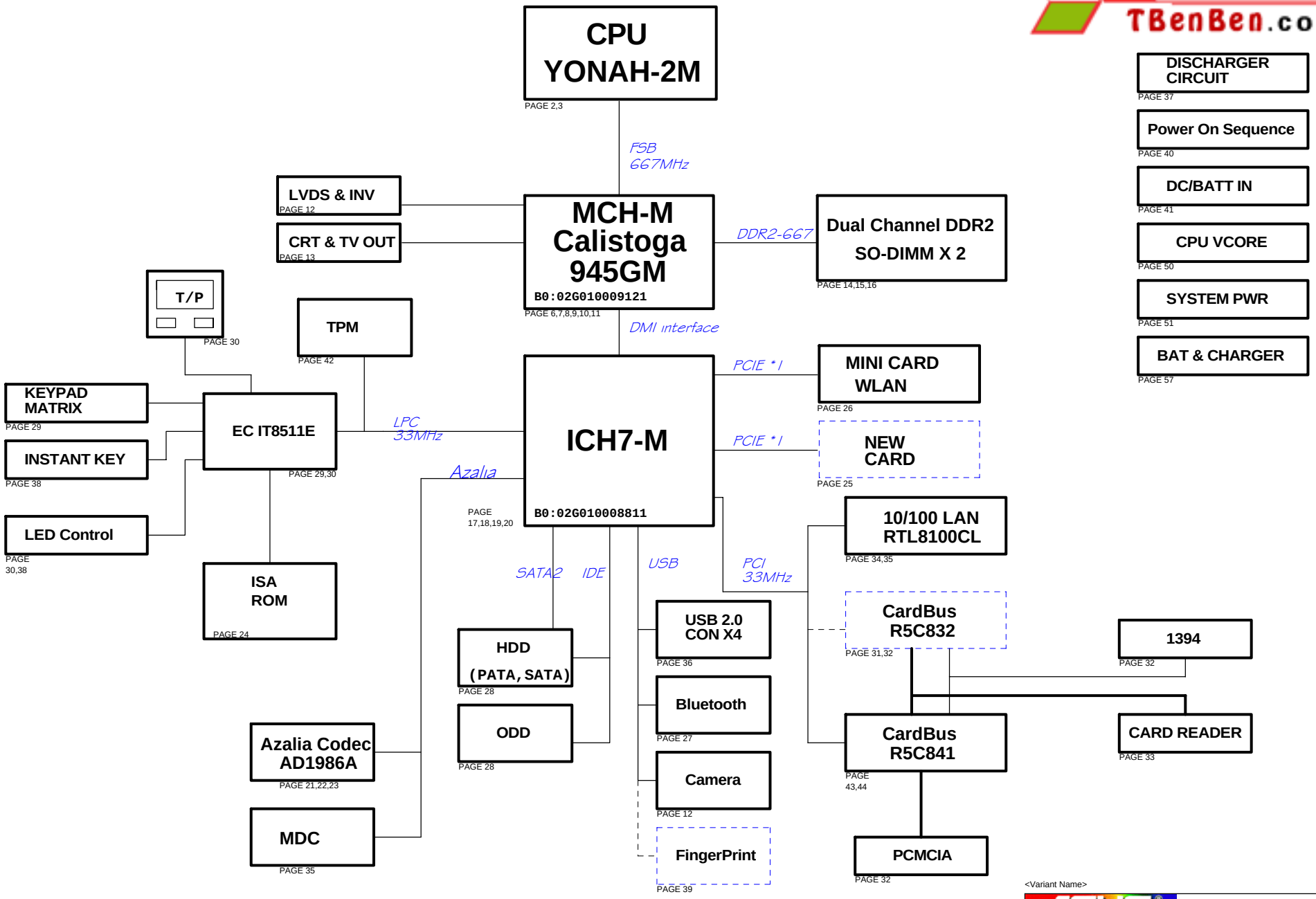
DC/BATT IN

T12F Block Diagram



<Variant Name>

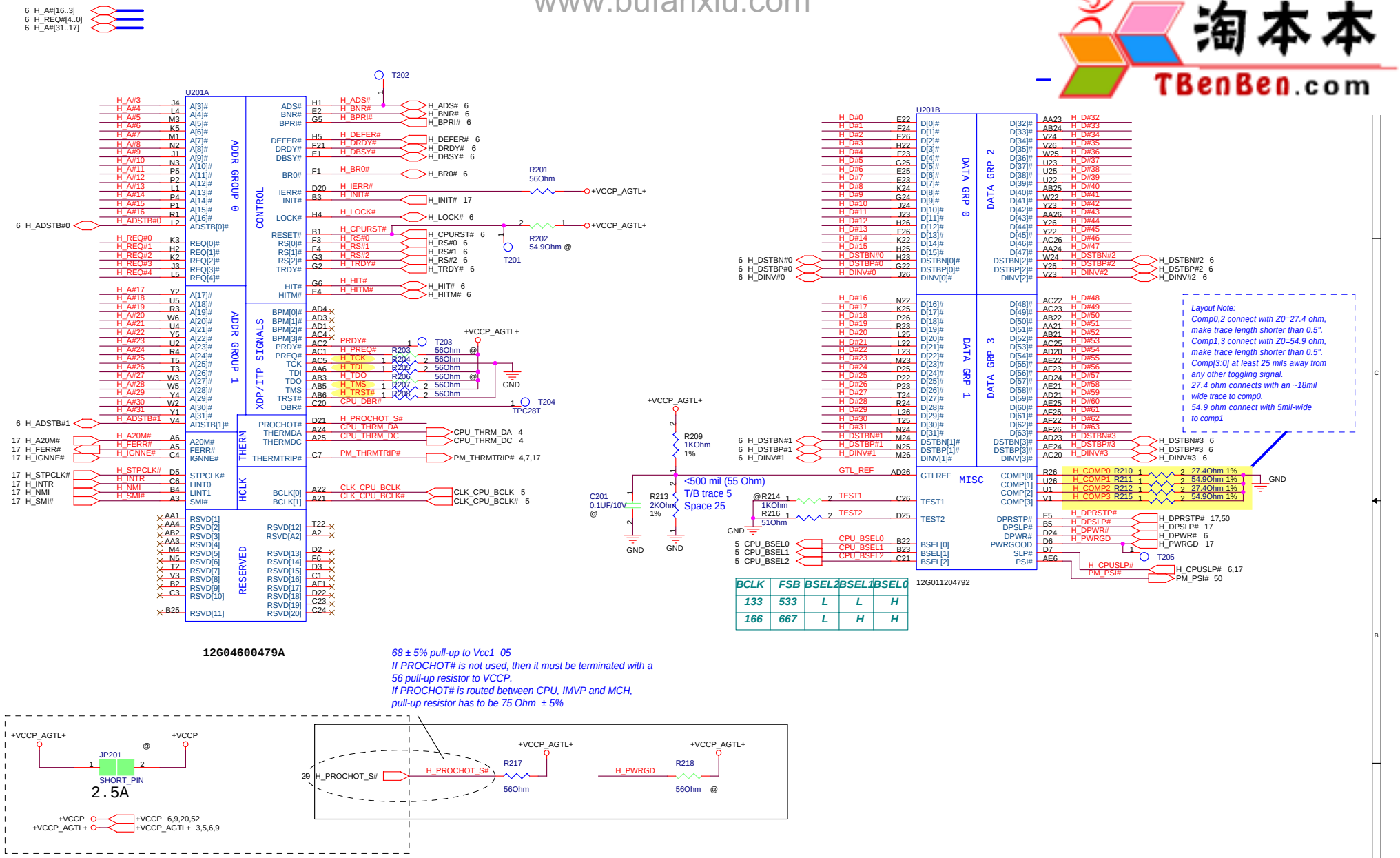
Title : BLOCK DIAGRAM

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12F	2.0

Date: Saturday, May 27, 2006 Sheet 1 of 61



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

12G04600479A

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

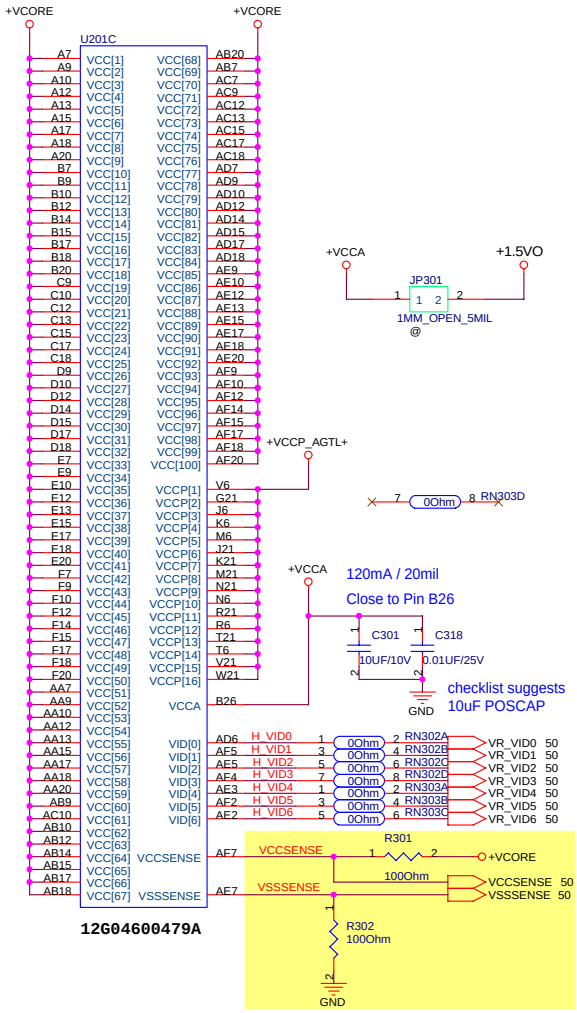
Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

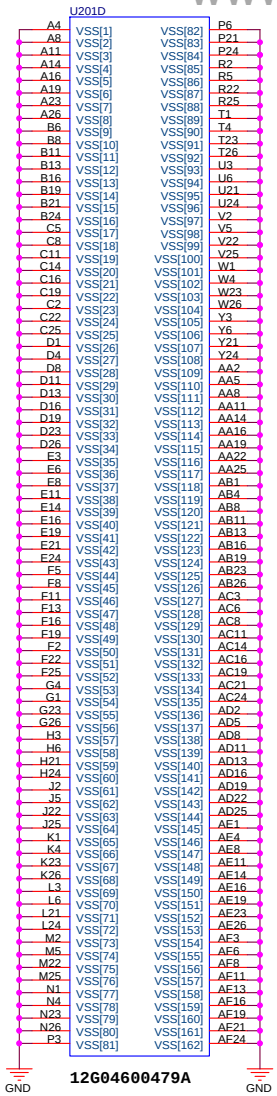
Date: Friday, May 26, 2006 Sheet 2 of 61

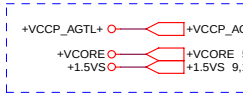
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

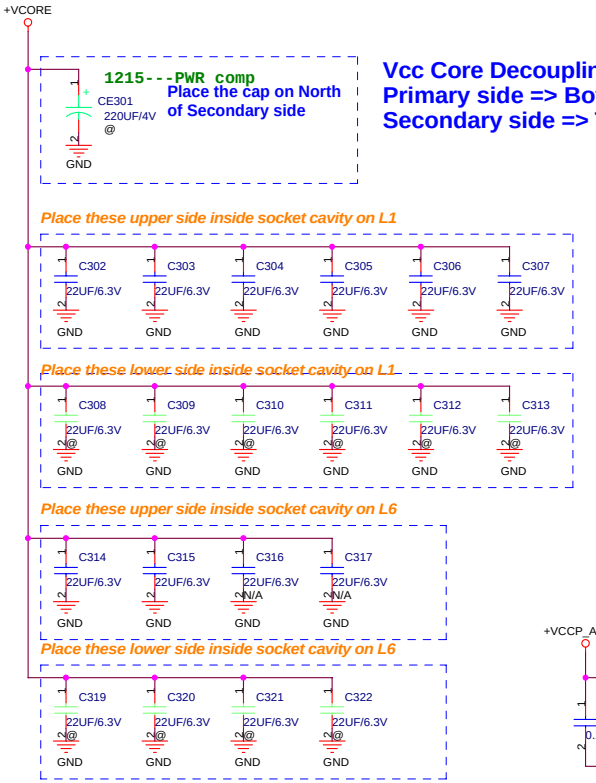
YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

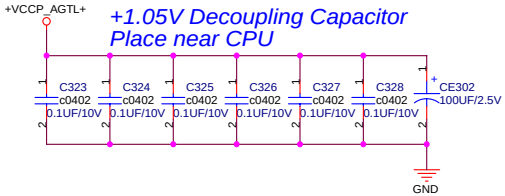


Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.









<variant_name>

ASUSTeK COMPUTER INC

Title : Yonah CPU (2)

Engineer: Leon and George

Size	Project Name	Rev
A3	T12F	

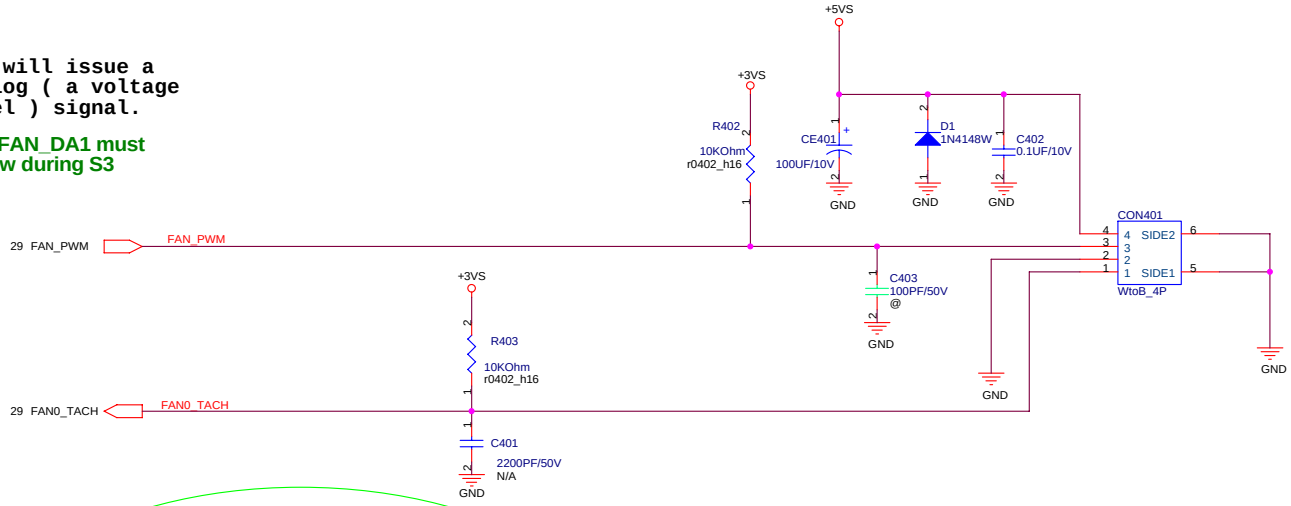
Date: Friday, May 26, 2006 Sheet 3 of 61

Fan Speed Control

+5VS 13,19,20,21,22,28,29,30,37,38,50,61
+3VS 5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61
+3VA 12,20,22,29,37,38,40,54,59,63

KBC will issue a analog (a voltage level) signal.

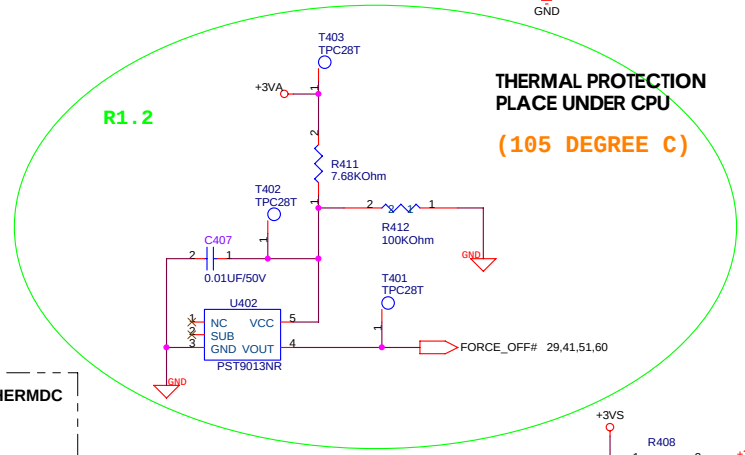
SW: FAN_DA1 must be low during S3

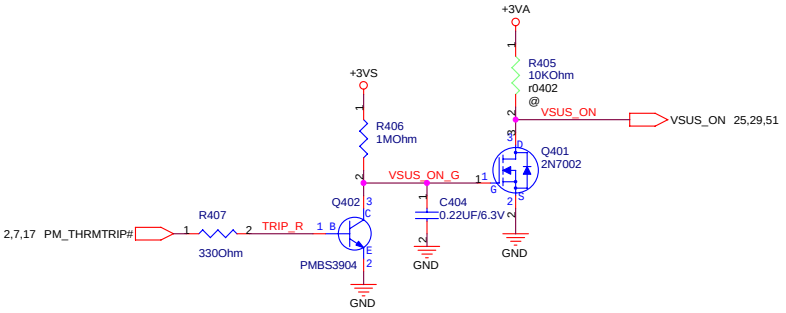


THERMAL PROTECTION PLACE UNDER CPU

(105 DEGREE C)

R1.2

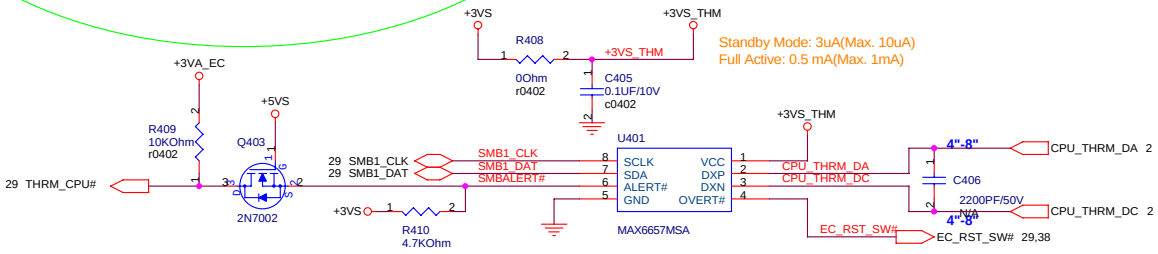




Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



<Variant Name>

ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: Leon and George

Size	Project Name	Rev
A3	T12F	

Date: Friday, May 26, 2006 Sheet 4 of 61

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

R2.0

R1.1

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled
PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519,Remove R550 R534

internal pull high

Internal Pull-Up Resistor

Internal Pull-Down Resistor

<Variant Name>

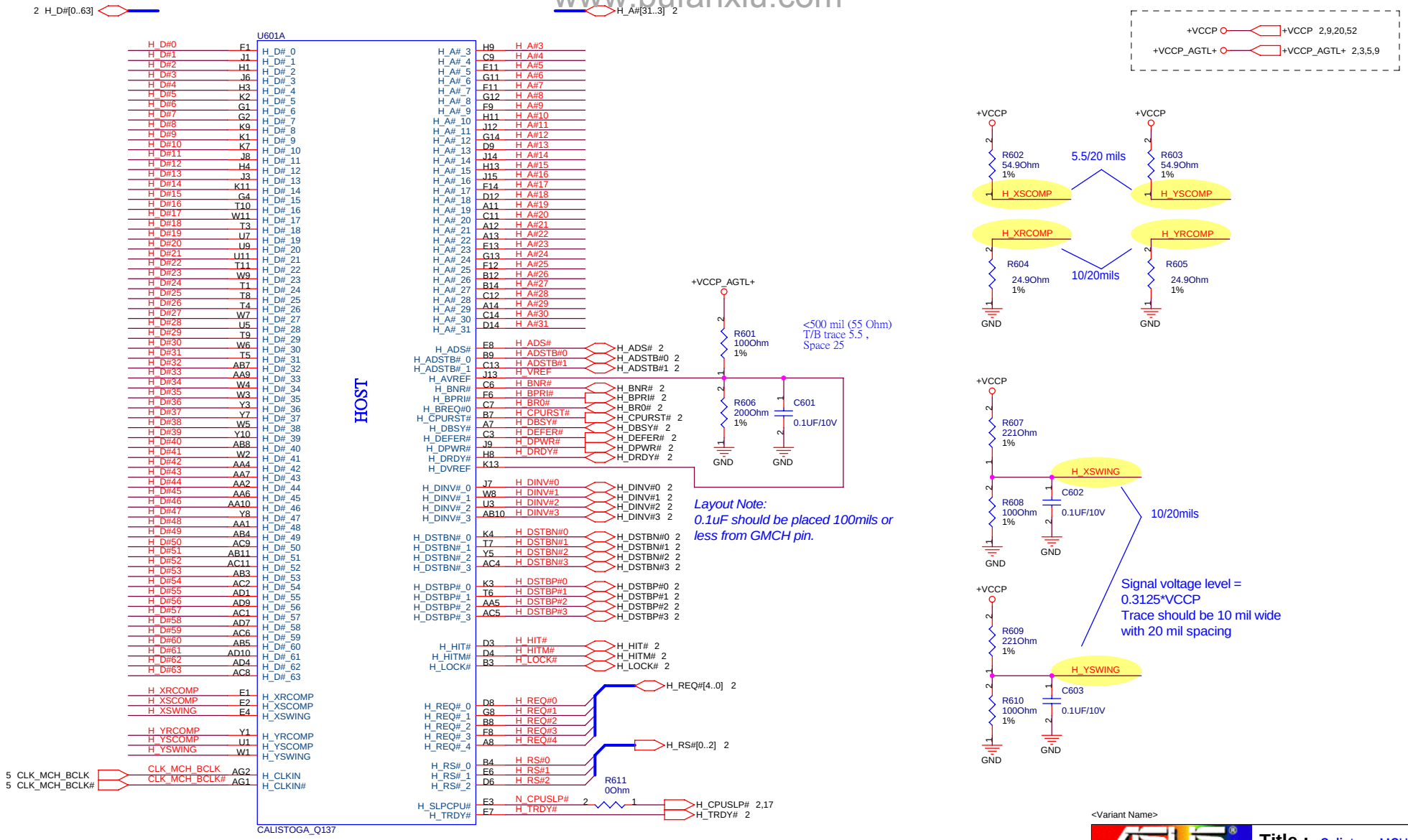
ASUSTeK COMPUTER INC

Title : CLOCK GEN

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

Date: Friday, May 26, 2006 Sheet 5 of 61



<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga MCH (1)

Engineer: Leon and George

Size	Project Name	Rev
B	T12F	

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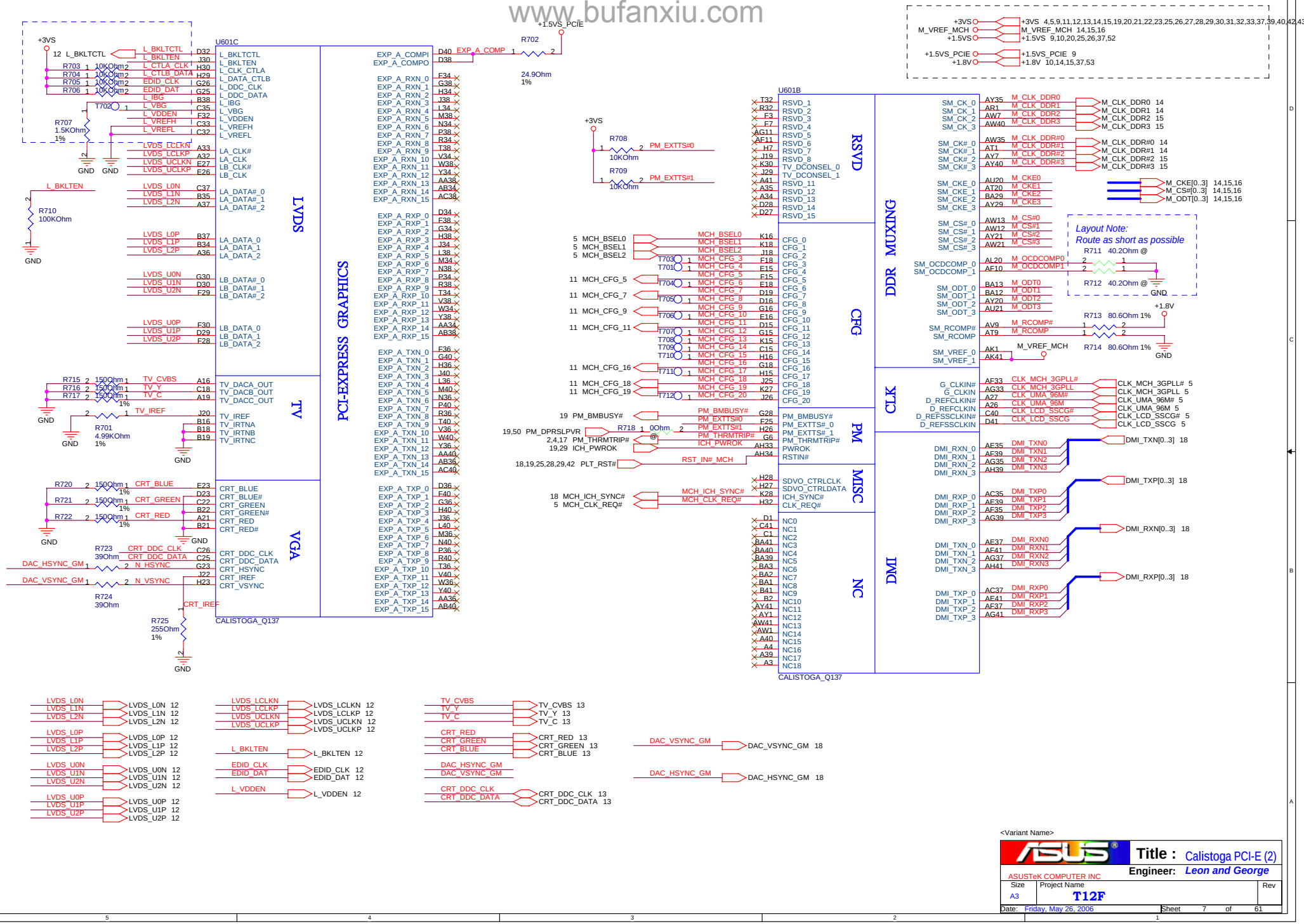

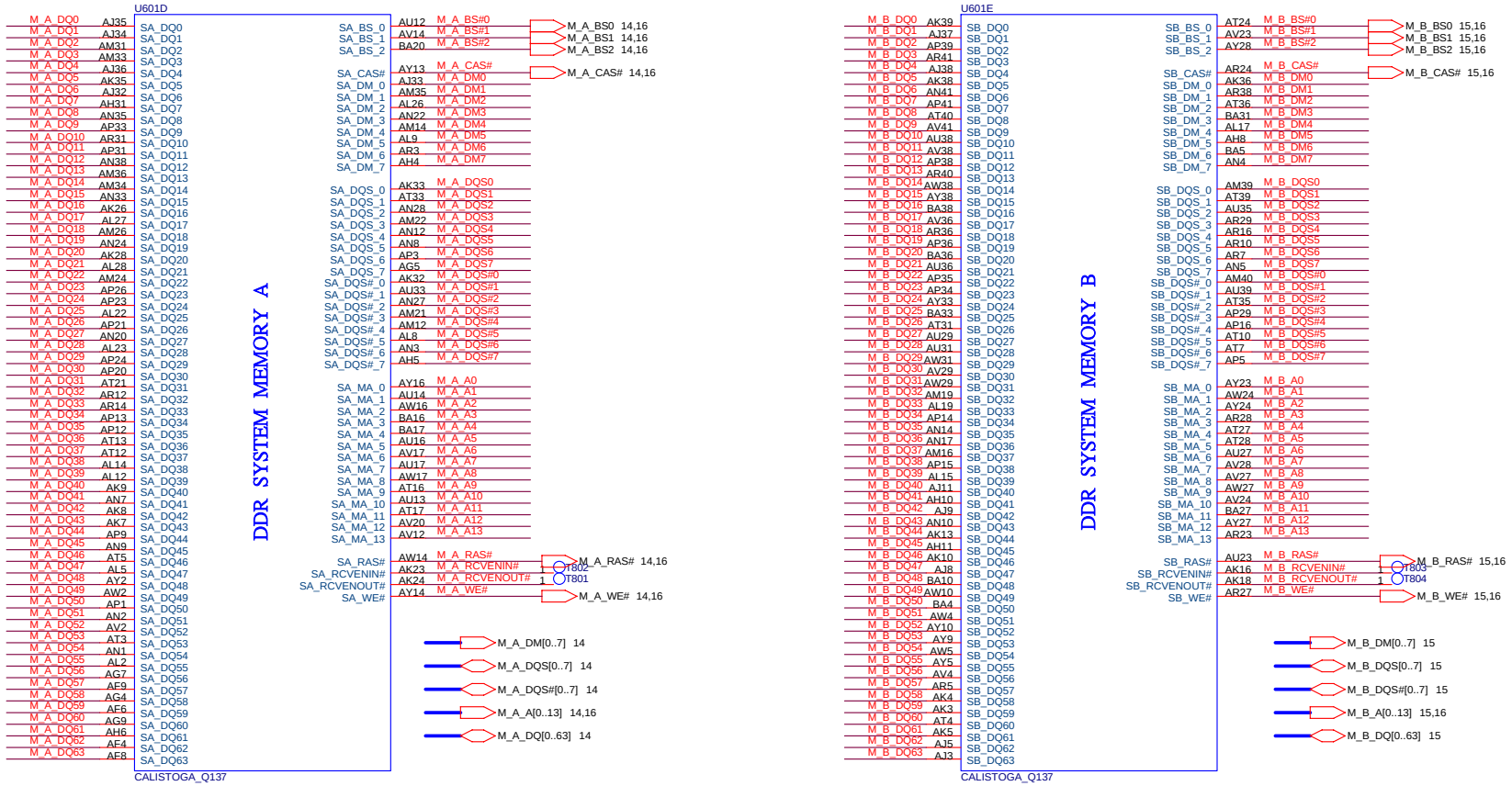

Layout Note:
Place filter components close to GMCH

GMCH VCORE

+VCCP — +1.05VS 3500 mA — +VCCP_GMCH

JP902 SHORT_PIN @
JP901 SHORT_PIN @

POWER

U601H — CALISTOGA_Q137

+1.5VS / VCC3G
Layout Note: Caps should be on Top layer
+1.5VS_PCIE
L902 120Ohm/100Mhz
CE902 150UF/4V @, C902 10UF/10V, C903 10UF/10V
GND
+1.5VS_3GPLL
1500 mA

VCCA_3GPLL
L901 30Ohm/100Mhz
C904 0.1UF/10V, C905 10UF/10V
GND

VCCAUX
+1.5VS_VCCAUX
L903 80Ohm/100Mhz
CE903 470UF/2.5V, C909 0.1UF/10V
VCCAUX 1900 mA
GND

VCCA_DPLLA
+1.5VS_DPLLA
L904 30Ohm/100Mhz
CE904 @ 470UF/2.5V, C912 0.1UF/10V
VCCA_DPLLA 50 mA
GND

VCCA_DPLLB
+1.5VS_DPLLB
L906 30Ohm/100Mhz
CE905 @ 470UF/2.5V, C918 0.1UF/10V
VCCA_DPLLB 50 mA
GND

VCCA_HPLL
+1.5VS_HPLL
L907 120Ohm/100Mhz
C923 22UF/6.3V, C924 0.1UF/10V
VCCA_HPLL 45 mA
GND

VCCA_MPLL
+1.5VS_MPLL
L908 120Ohm/100Mhz
C927 22UF/6.3V, C928 0.1UF/10V
VCCA_MPLL 45 mA
GND

Layout Note: 0.1uF caps in 1.5VS_xPLL need to be located as edge caps within 200 mils.

VCCD_LVDS
+1.5VS — VCCD_LVDS 20 mA — Pin A28 B28 C28
C910 0.1UF/10V, C911 10UF/10V
GND

VCCD_TVDAC
+1.5VS — VCCD_TVDAC — Pin D21
C913 0.022UF/25V, C914 0.1UF/10V
24 mA
GND

VCCD_QTVDAC
+1.5VS — VCCD_QTVDAC — H19 C28
C919 0.022UF/25V, C920 0.1UF/10V
GND

Layout Note: These Caps should be within 250 mils of edge of GMCH

Layout Note: These 0.1uF caps should be placed within 200 mils of edge

VCC_SYNC
+2.5VS — VCC_SYNC — Pin H22
C932 0.1UF/10V
GND

VCCA_LVDS
VCCA_LVDS — Pin A38 10 mA
C933 0.01UF/25V, C934 0.1UF/10V
GND

VCCA_3GBG
VCCA_3GBG — Pin G41 2 mA
C935 0.1UF/10V
GND

VCCTX_LVDS
VCCTX_LVDS 60 mA — Pin A30 B30 C30
C936 0.1UF/10V, C937 4.7UF/10V
GND

VCCA_CRTDAC
R905 10Ohm — +VCCP_GMCH_R — D902 BAT54C — +VCCP_GMCH
70 mA
VCCA_CRTDAC — Pin E21 F21
+2.5VS_CRTDAC
L909 120Ohm/100Mhz
C901 0.022UF/25V, C946 0.1UF/10V
GND

Layout Note: These Caps should be within 250 mils of edge of GMCH

VCC_HV
+3VS — VCC_HV 40 mA — Pin A23 B23 B25
C944 10UF/10V, C945 0.1UF/10V
GND

VCCA_TVDACA
+3VS_TVDACA — VCCA_TVDACA0 VCCA_TVDACA1
Layout Note: These Caps used in +3VS_TVDACx should be within 250 mils of edge of GMCH

VCCA_TVDACB
+3VS_TVDACB — VCCA_TVDACB0 VCCA_TVDACB1

VCCA_TVDACC
+3VS_TVDACC — VCCA_TVDACC0 VCCA_TVDACC1

VTTLF_CAP3
C929 0.47UF/16V
GND

VTTLF_CAP2 / VTTLF_CAP1
C938 0.47UF/16V, C939 0.22UF/6.3V
GND GND

+VCCP_AGTL+
+VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH 10
+1.5VS_PCIE 7
+3VS 4,5,7,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43
+2.5VS 37,54
+1.5VS 10,20,25,26,37,52

Layout Note: Place on the edge

+VCCP_AGTL+ — 800 mA
C906 4.7UF/10V, C907 2.2UF/6.3V, C908 0.22UF/6.3V, CE901 330UF/2V 11G08D233722
GND

Layout Note: Place in cavity

+3VS_DAC
+3VS +3VS_DAC
R903 0Ohm @
R902 10Ohm — +1.5VS_DAC — D901 BAT54C — +1.5VS
L905 180Ohm/100Mhz
C915 10UF/10V
GND

Total Power Consumption 120 mA

VCCA_TVBG — Pin H20
+3VS_TVBG
C916 0.022UF/25V, C917 0.1UF/10V
GND

VCCA_TVDACA — Pin E19 F19
+3VS_TVDACA
C921 0.022UF/25V, C922 0.1UF/10V
GND

VCCA_TVDACB — Pin C20 D20
+3VS_TVDACB
C925 0.022UF/25V, C926 0.1UF/10V
GND

VCCA_TVDACC — Pin E20 F20
+3VS_TVDACC
C930 0.022UF/25V, C931 0.1UF/10V
GND

+3VS_DAC
+5V — R904 10KOhm — 3VS_DAC_EN
U901 SI9183DT: VIN, VOUT, GND, FB, SD#
C940 0.1UF/50V, C941 4.7UF/16V
3VS_DAC_ADJ — R901 35.7KOhm
C942 0.1UF/50V, R906 20KOhm @
+3VS_DAC — C943 4.7UF/16V
GND

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS
+2.5VS should be placed within 200 mils of edge.

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga Power (4)
Engineer: Leon and George

Size	Project Name	Rev
A3	T12F	

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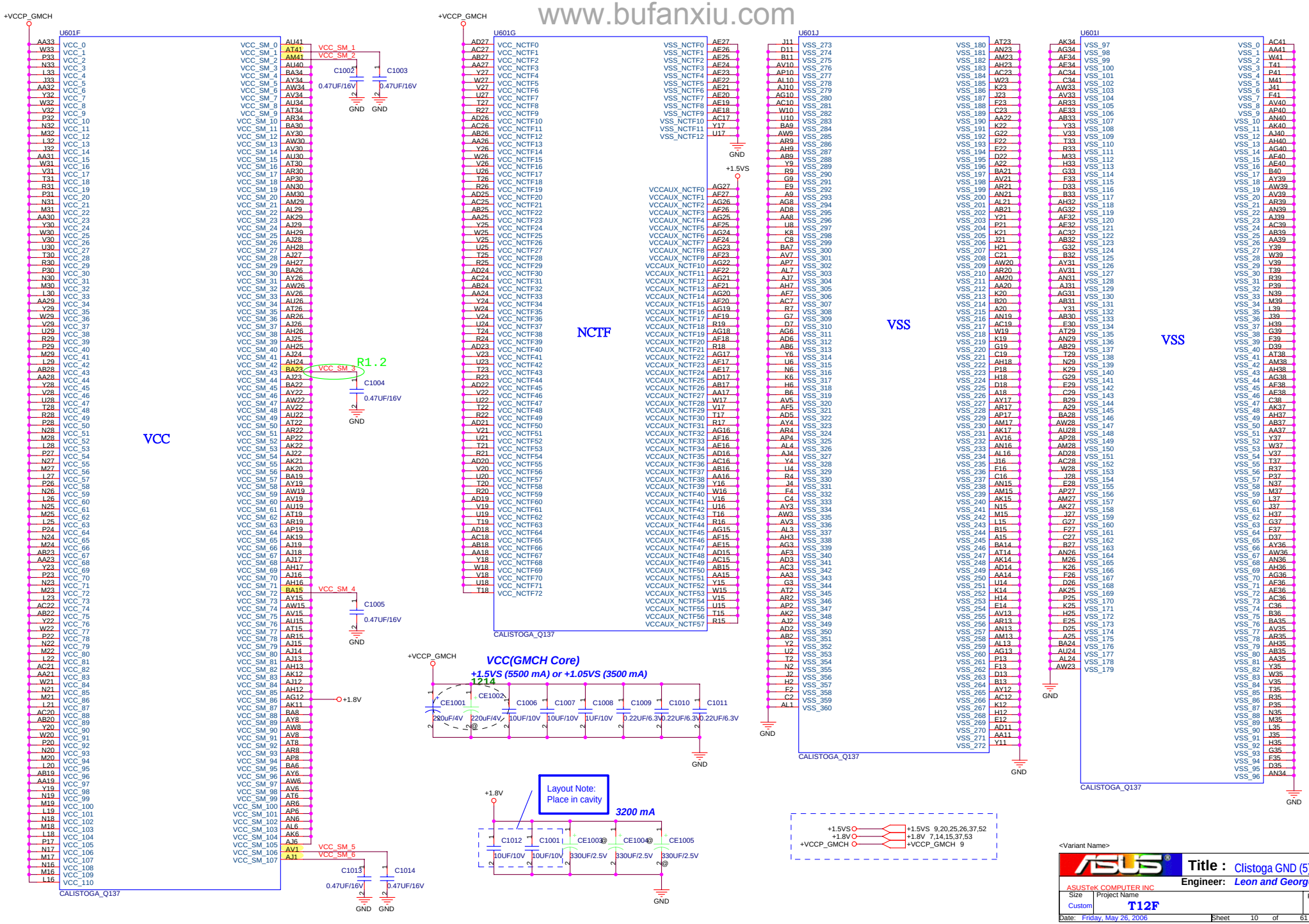

<variant_name>

ASUSTeK COMPUTER INC

Title : Clistoga GND (5)

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

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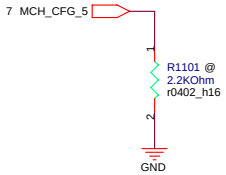
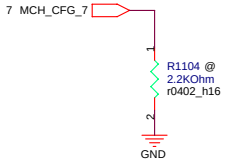
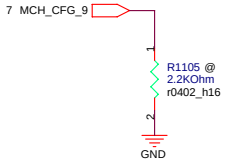


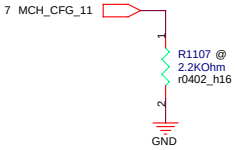
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



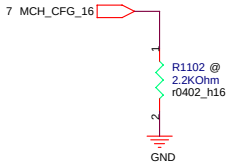
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



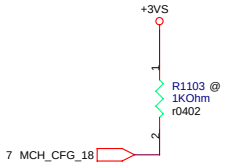
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



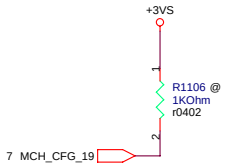
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4
6		(Default)
7	CPU Strap	0 = Reserved 1 = Mobile
8		CPU (Default)
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal
11:10		(Default)
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled
17		(Default)
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga Strapping
Engineer: *Leon and George*

Size	Project Name	Rev
Custom	T12F	

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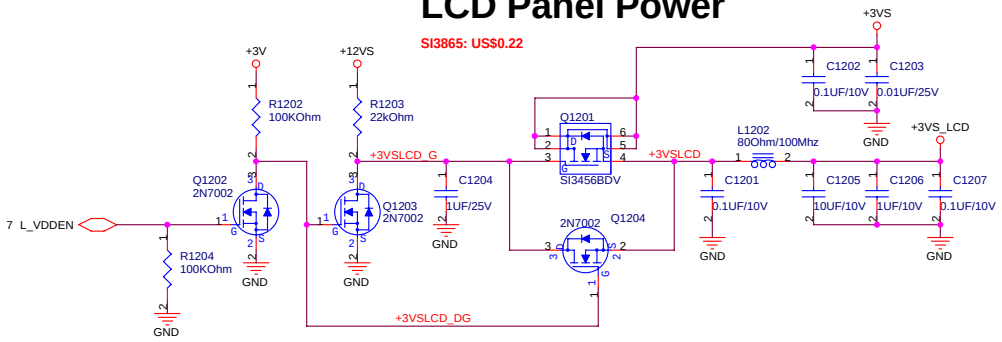
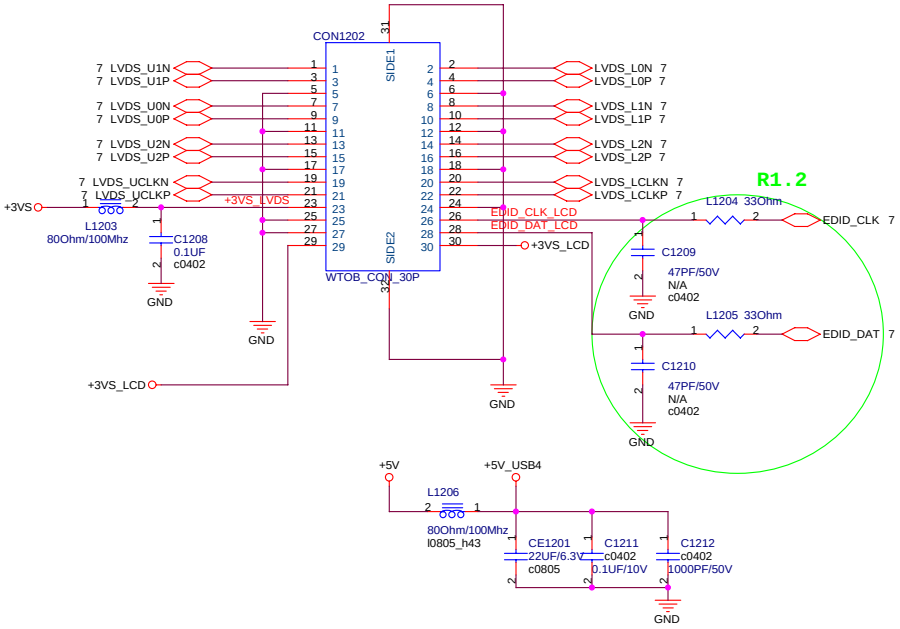
3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

LCD Panel Power

SI3865: US$0.22



LCD LVDS Interface



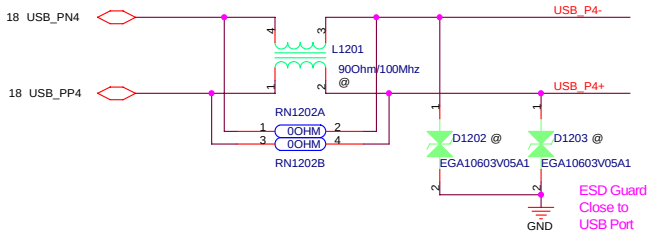
LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

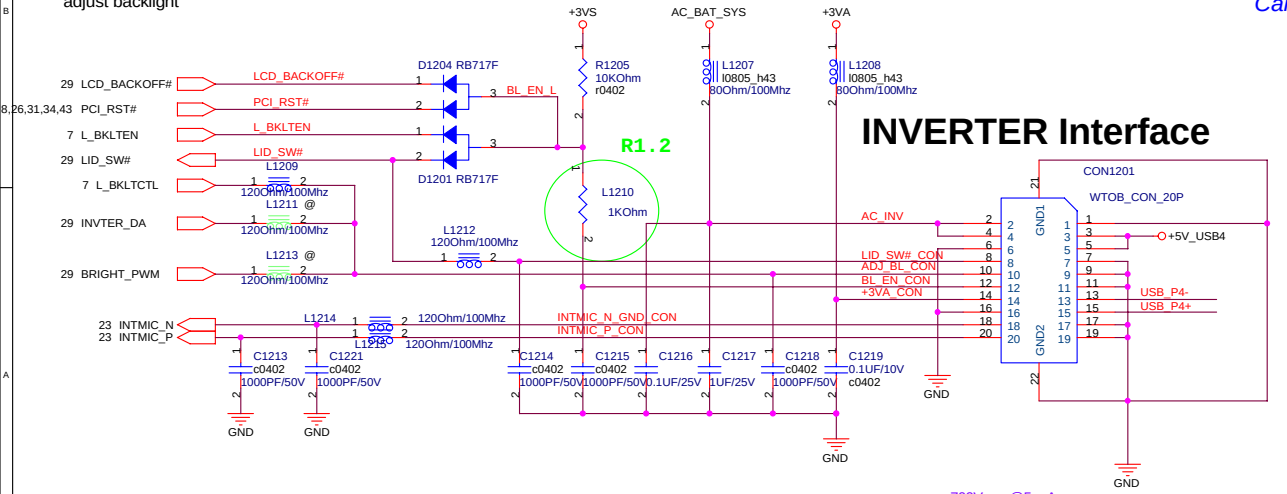
EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 14.1W LCD Panel

USB4 For CMOS Camera



INVERTER Interface



700V rms@5 mA rms
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

<Variant Name>

ASUSTeK COMPUTER INC

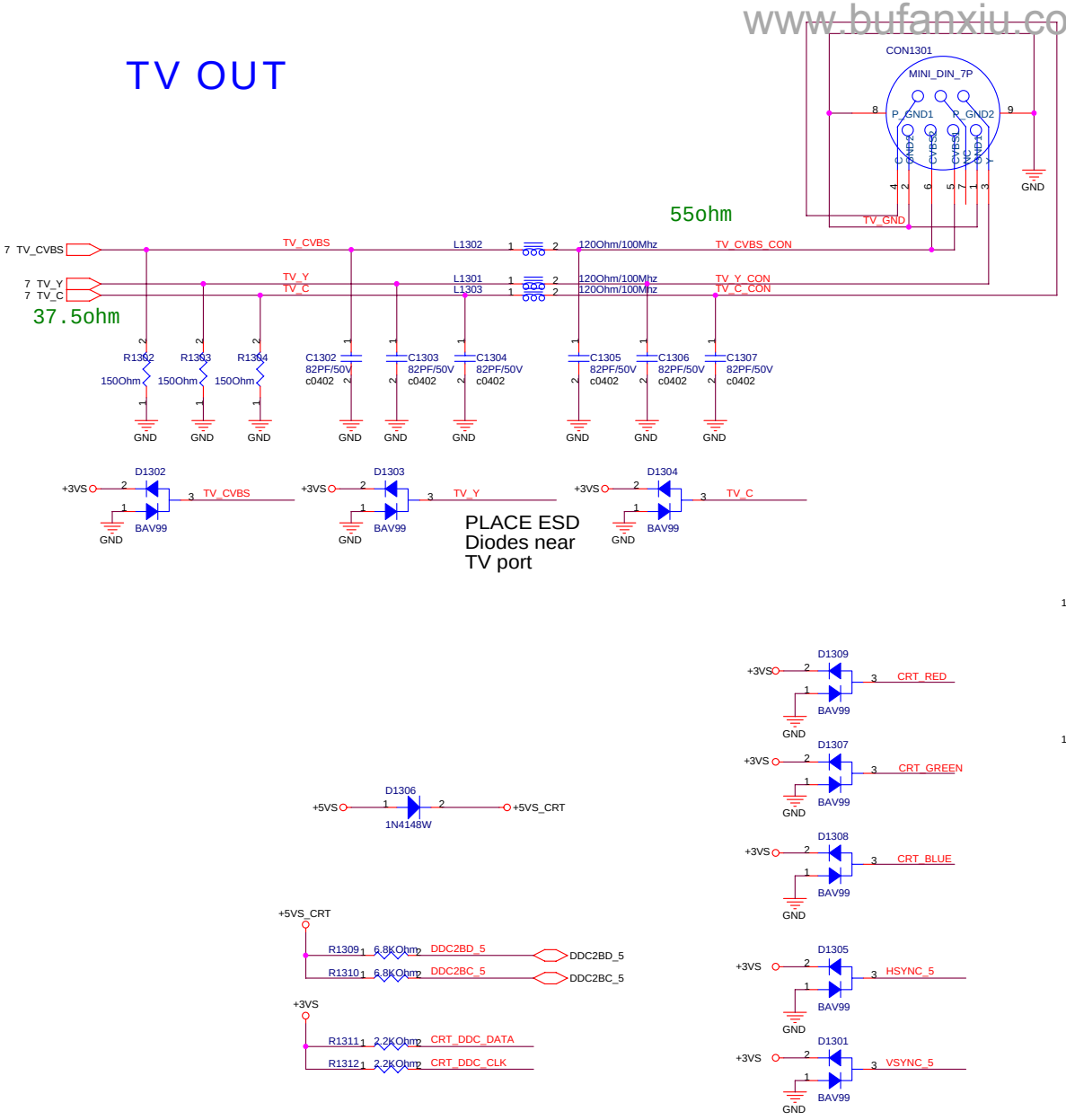
Title : LVDS & INVERTER

Engineer: *Leon and George*

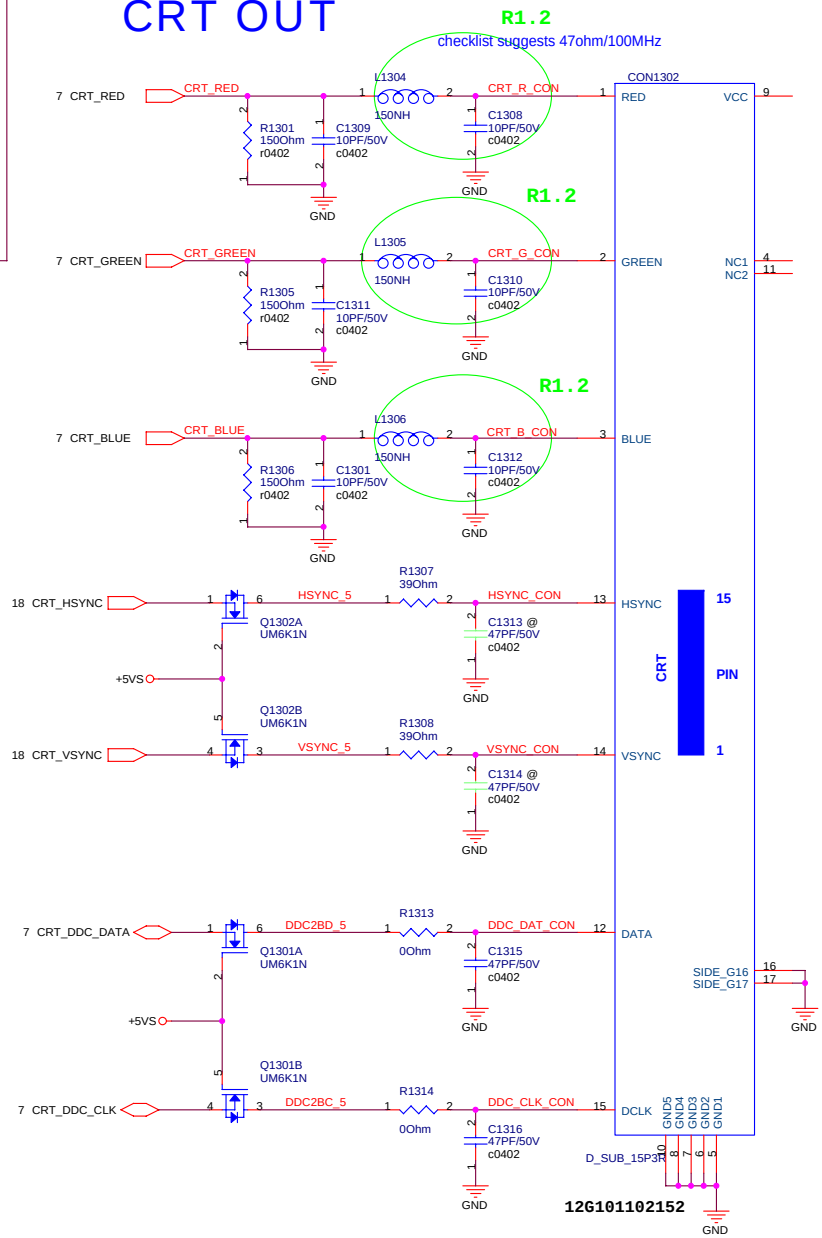
Size	Project Name	Rev
A3	T12F	

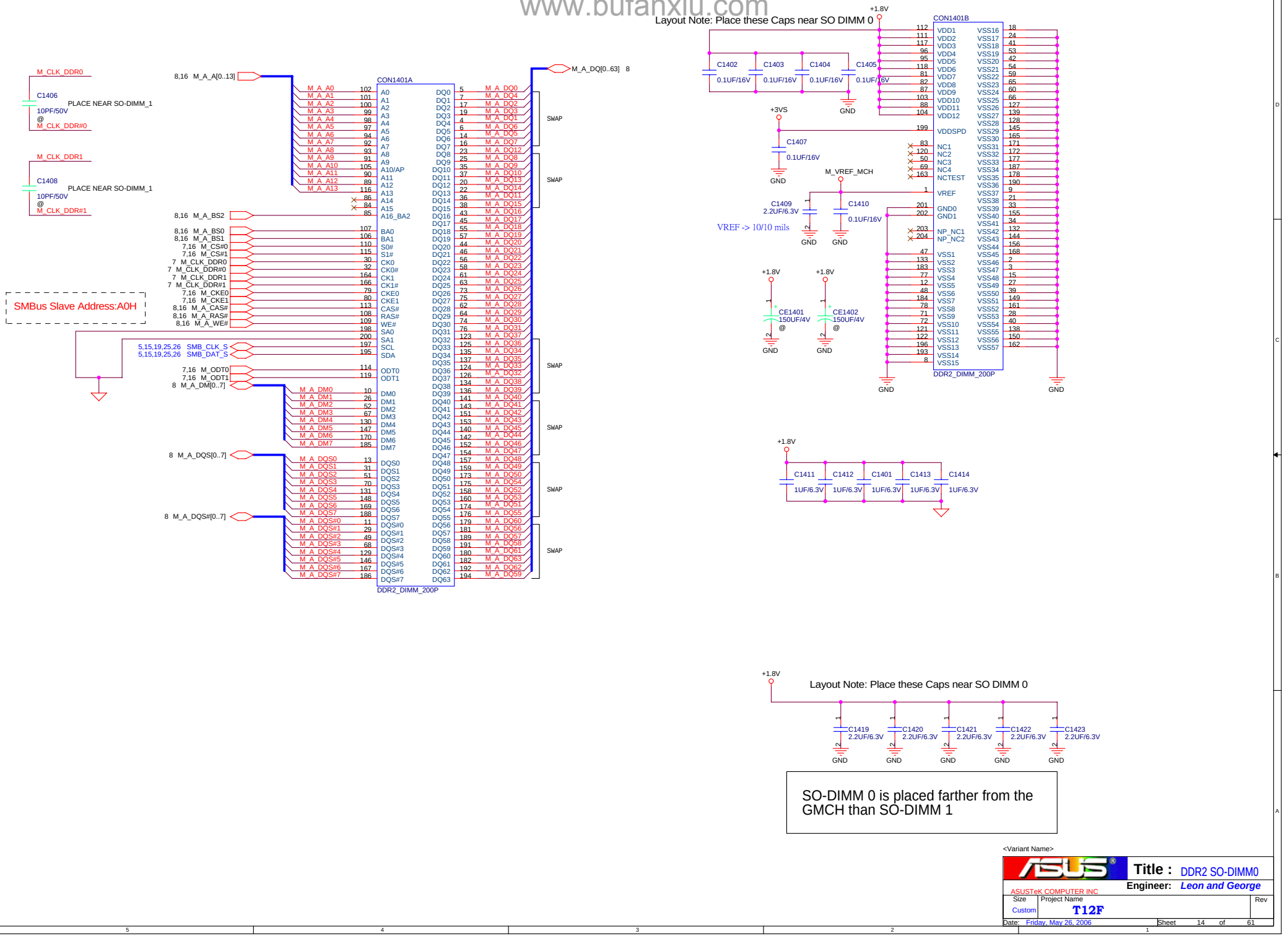
Date: Friday, May 26, 2006 Sheet 12 of 61

TV OUT



CRT OUT



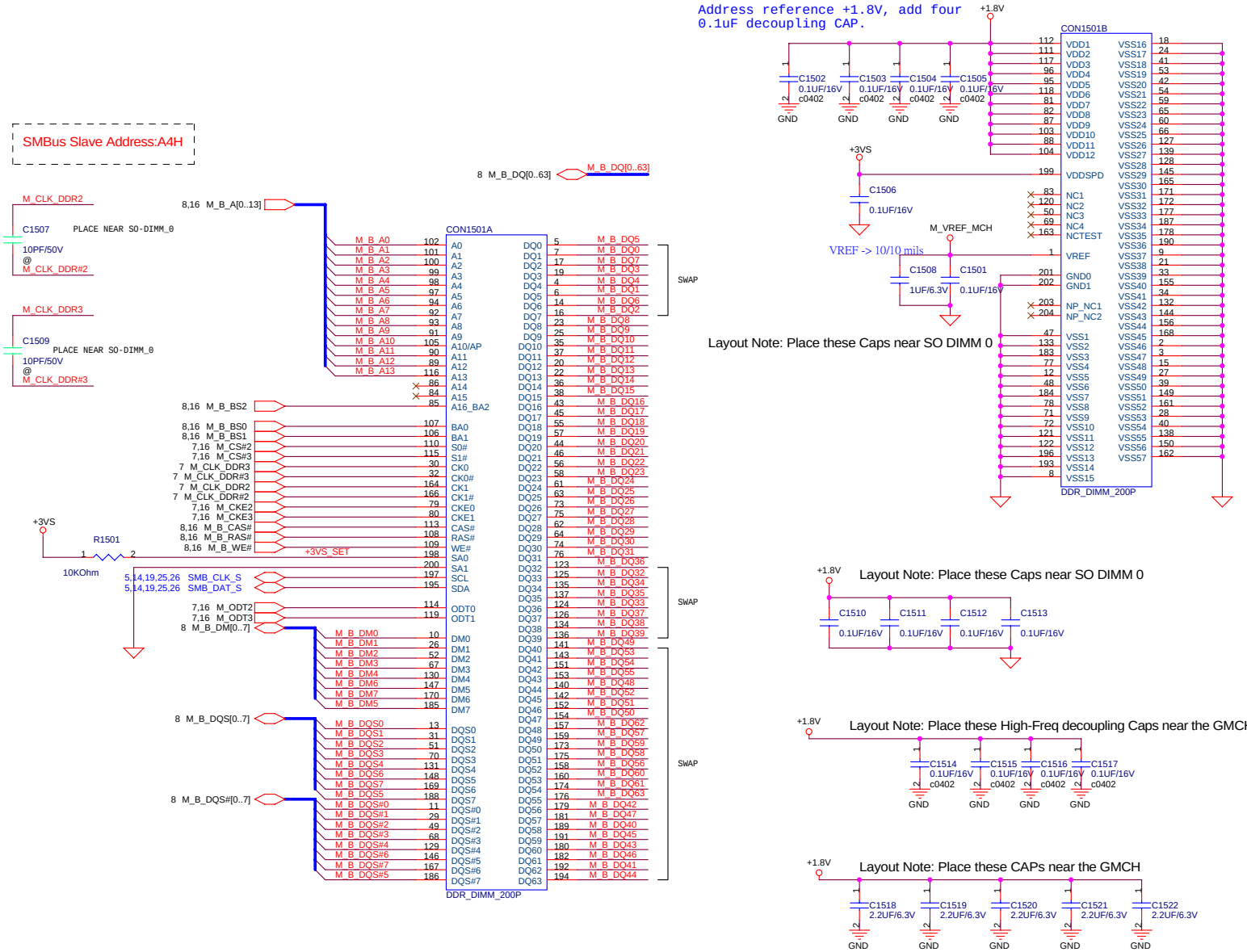


<variant_name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM0	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 14 of 61	

SMBus Slave Address:A4H

Address reference +1.8V, add four 0.1uF decoupling CAP.



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ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM1

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

Date: Friday, May 26, 2006 Sheet 15 of 61

+0.9VS

RN1602A M_CKE2
RN1602B M_CKE3
RN1602C M_B_BS2
RN1602D M_B_A9
RN1602E M_B_A12
RN1602F M_B_A8
RN1602G M_B_A11
RN1602H M_B_A6

RN1603A M_B_A7
RN1603B M_B_A5
RN1603C M_B_A3
RN1603D M_B_A4
RN1603E M_B_A2
RN1603F M_B_A1
RN1603G M_B_A0
RN1603H M_B_WE#

RN1604A M_B_BS1
RN1604B M_B_A10
RN1604C M_B_RAS#
RN1604D M_B_BS0
RN1604E M_B_A13
RN1604F M_B_CAS#
RN1604G M_ODT2
RN1604H M_CS#2

RN1605A M_CS#3
RN1605B
RN1605C
RN1605D M_ODT3

RN1606A M_A_A12
RN1606B M_A_BS2
RN1606C M_A_A11
RN1606D M_A_A7
RN1606E M_A_A6
RN1606F M_CKE1
RN1606G M_CKE0
RN1606H M_A_A9

RN1607A
RN1607B M_A_A5
RN1607C M_A_A4
RN1607D M_A_A3
RN1607E M_A_A0
RN1607F M_A_A2
RN1607G M_A_A8
RN1607H

RN1608A M_A_A10
RN1608B M_A_BS1
RN1608C M_A_RAS#
RN1608D M_A_BS0
RN1608E M_A_A1
RN1608F M_A_A13
RN1608G M_A_CAS#
RN1608H M_A_WE#

RN1609A M_ODT0
RN1609B M_CS#0
RN1609C M_CS#1
RN1609D M_ODT1

M_A_A[0..13] 8,14
M_A_BS[0..2] 8,14
M_A_CAS# 8,14
M_A_RAS# 8,14
M_A_WE# 8,14

M_B_A[0..13] 8,15
M_B_BS[0..2] 8,15
M_B_CAS# 8,15
M_B_RAS# 8,15
M_B_WE# 8,15

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

M_VREF_MCH
+0.9VS
M_VREF_MCH 7,14,15
+0.9VS 37,53

+0.9VS
L1601
M_VREF_MCH
120Ohm/100Mhz

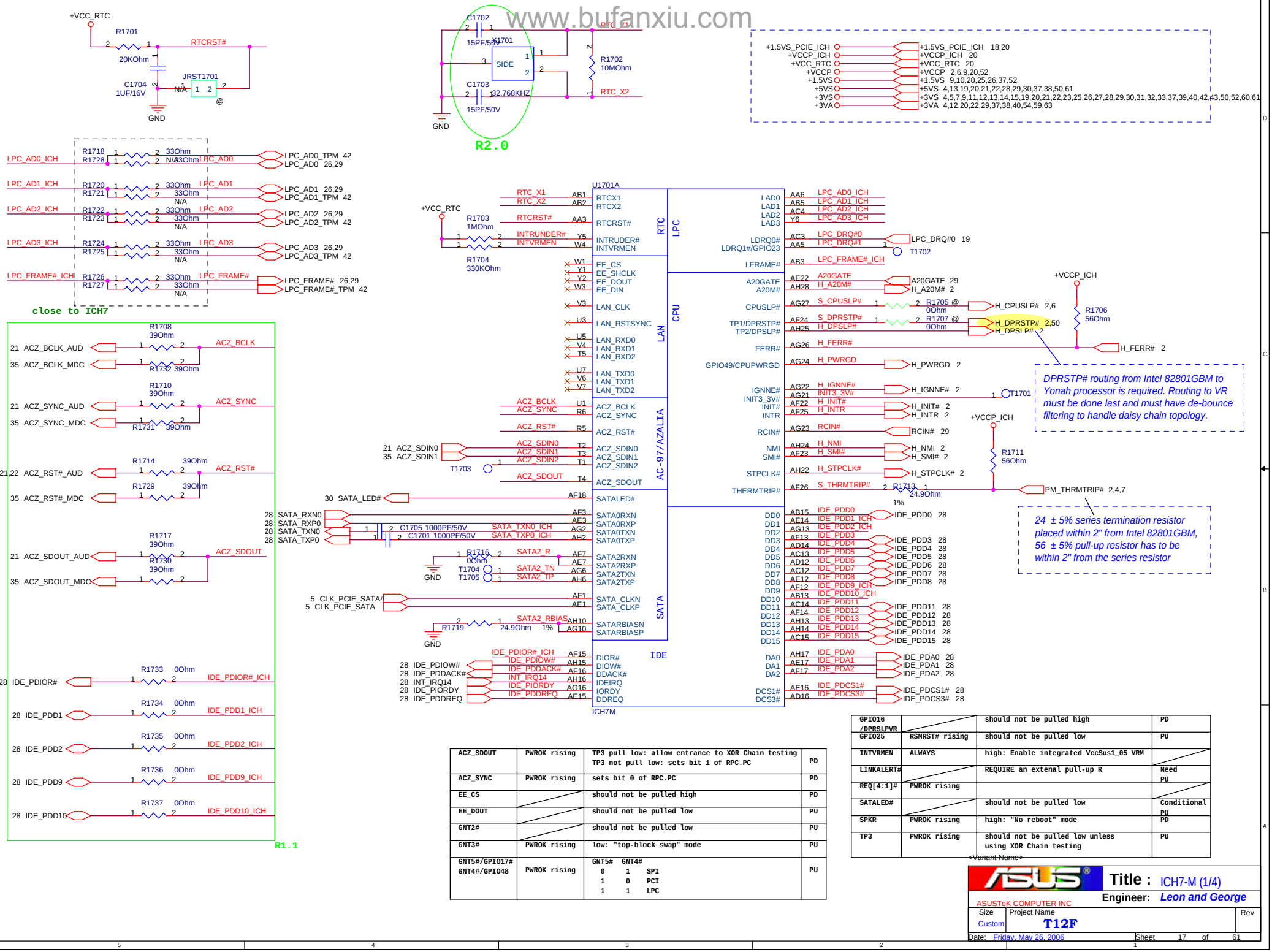
+0.9VS
C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1601 C1613
c0402 0.1UF/10V
GND

Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+0.9VS
C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624 C1625 C1626
c0402 0.1UF/10V
GND

<Variant Name>

Title : DDR2 TERM
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size A4 | Project Name T12F | Rev
Date: Friday, May 26, 2006 | Sheet 16 of 61



ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

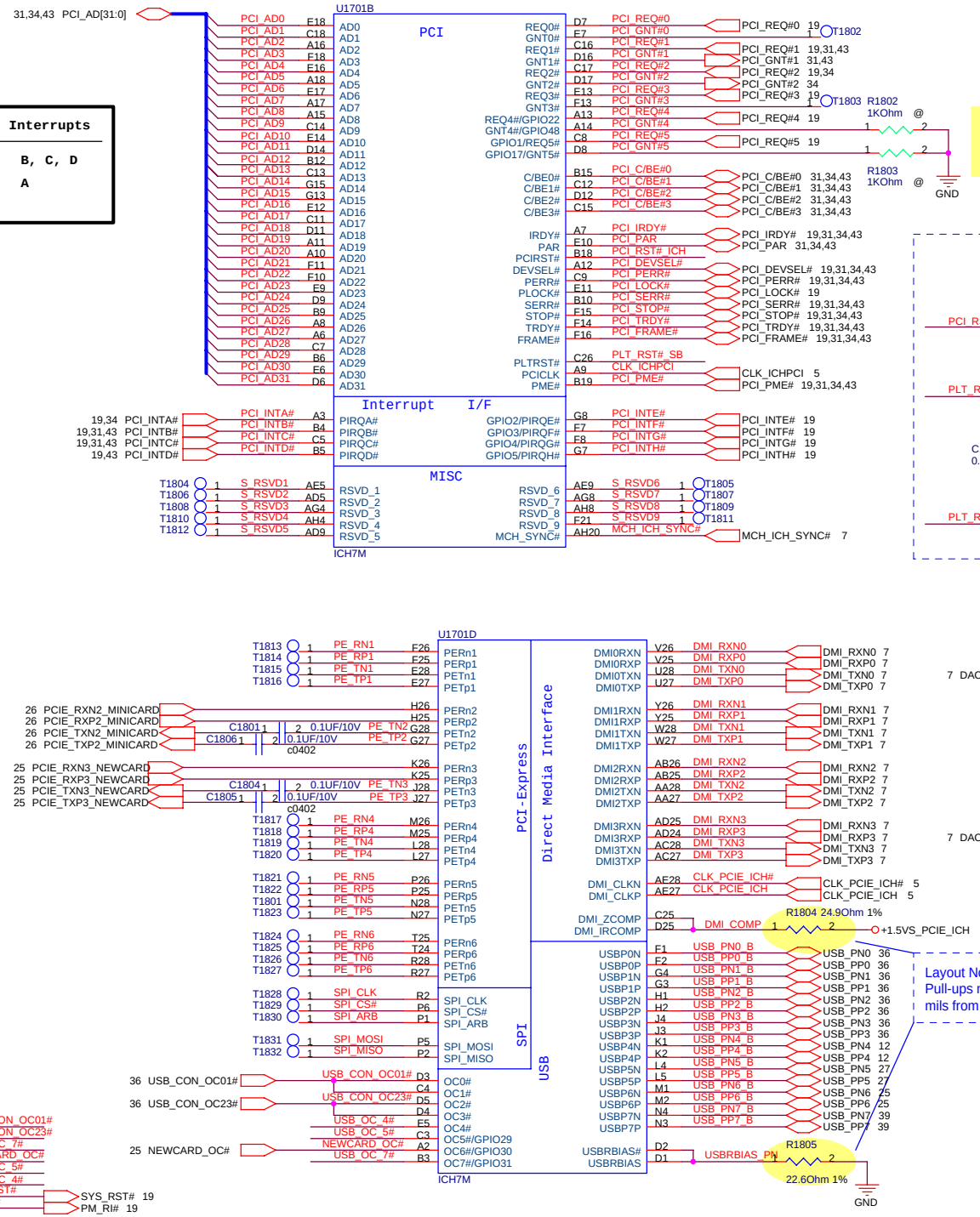
GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

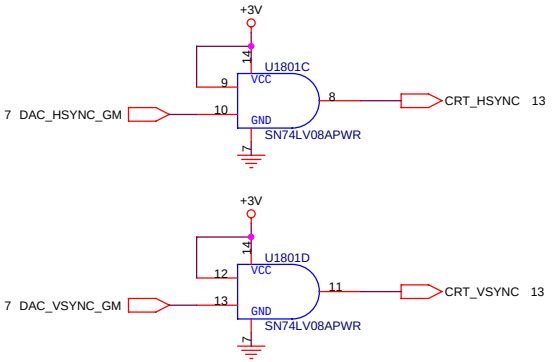
<Variant Name>

Title : ICH7-M (1/4)
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size: Custom
Project Name: T12F
Rev:
Date: Friday, May 26, 2006
Sheet 17 of 61

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A





USB Devices

Port 0	CON3602
Port 1	CON3603
Port 2	CON3601
Port 3	CON3601
Port 4	CMOS Camara
Port 5	BlueTooth
Port 6	NewCard
Port 7	FingerPrint

<Variant Name>

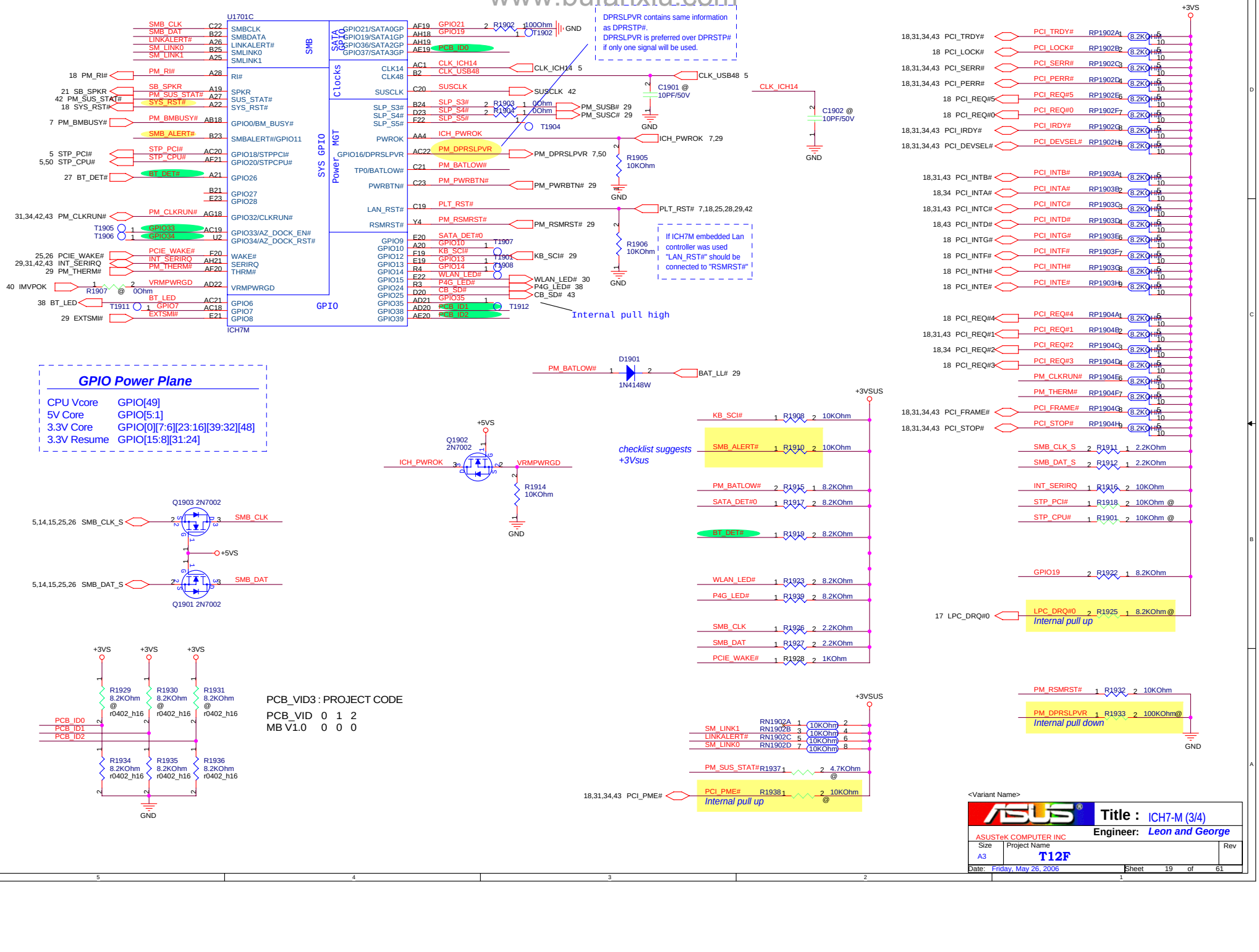
Title : ICH7-M (2/4)

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12F	

Date: Tuesday, May 30, 2006 Sheet 18 of 61



GPIO Power Plane

CPU Vcore	GPIO[49]
5V Core	GPIO[5:1]
3.3V Core	GPIO[0][7:6][23:16][39:32][48]
3.3V Resume	GPIO[15:8][31:24]

PCB_VID3 : PROJECT CODE

PCB_VID	0	1	2
MB V1.0	0	0	0

<Variant Name>

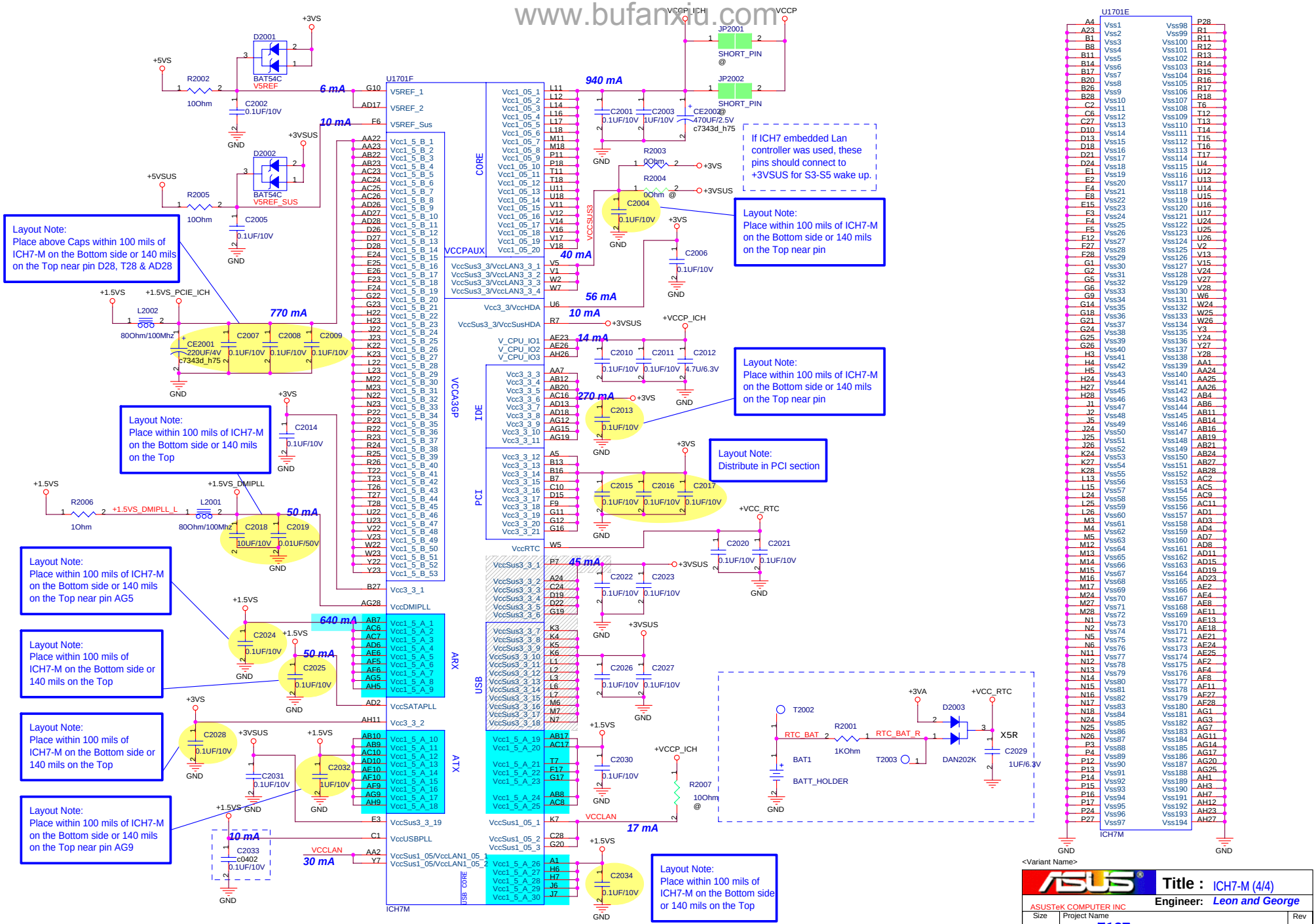
Title : ICH7-M (3/4)

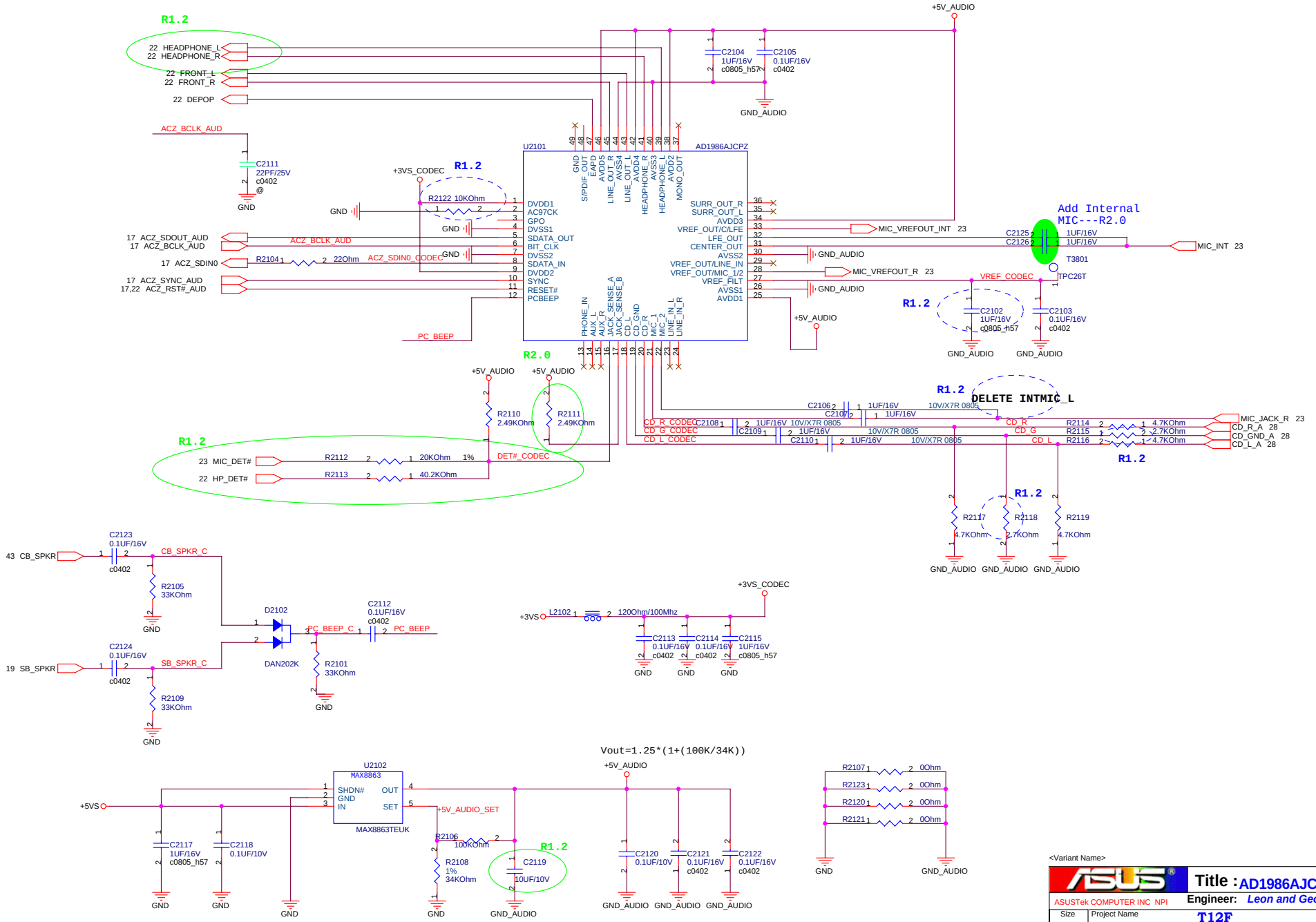
Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
A3	T12F	

Date: Friday, May 26, 2006 Sheet 19 of 61





<Variant Name>

ASUSTek COMPUTER INC NPI

Title : AD1986AJCPZ

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	
	P/N <OrgAddr2>	

Date: Friday, May 26, 2006 Sheet 21 of 61

Woofer (Optional)

The sub-woofer dimension could be less than 20mm. fo will be >400Hz.

BPF first, then Power Amp

Woofer frequency response setting:

FL = 153Hz

FH = 2.26KHz

FL = TBD

FH = TBD

AV= 0dB

AV= 6dB

(Headphone Mode) FL = TBD

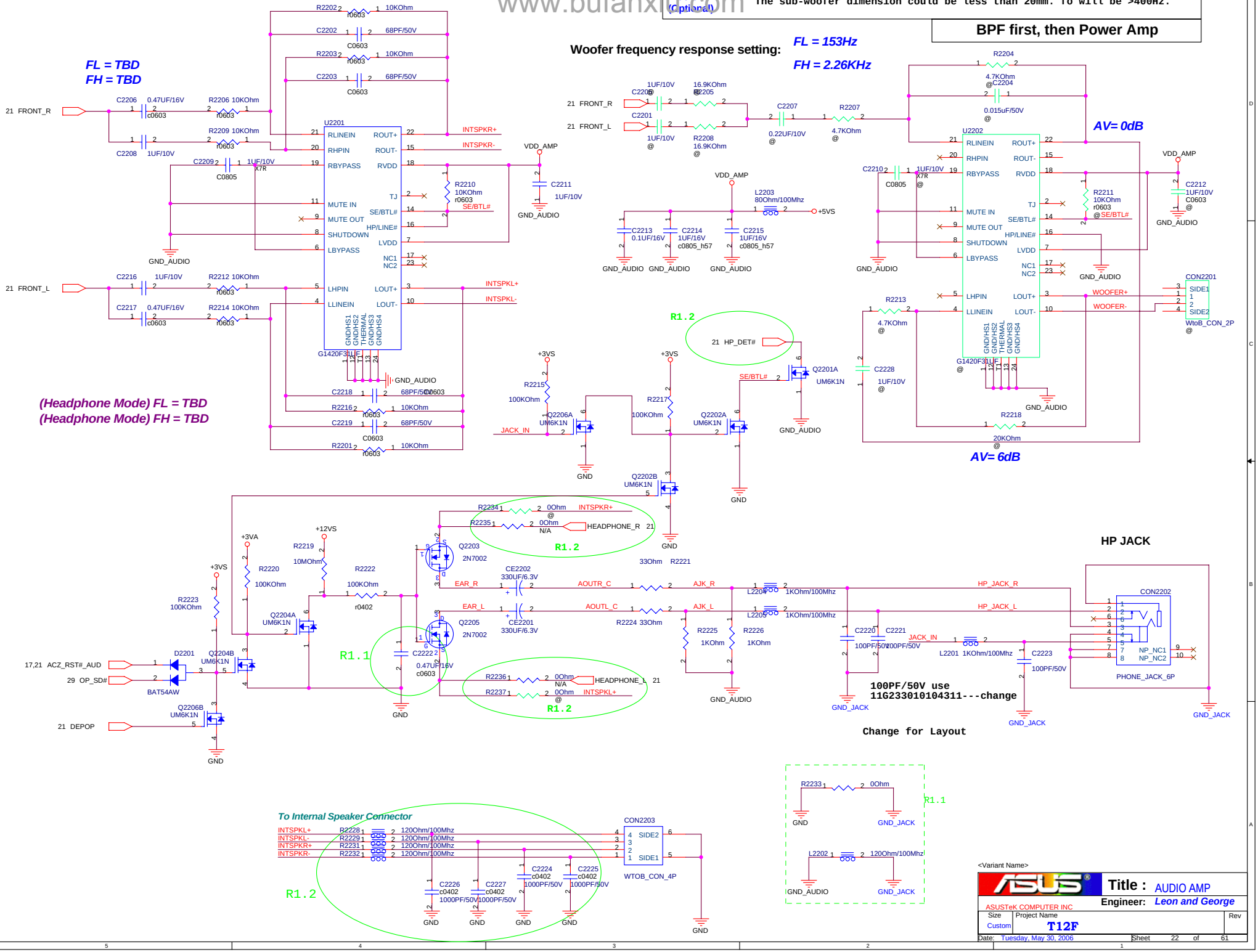
(Headphone Mode) FH = TBD

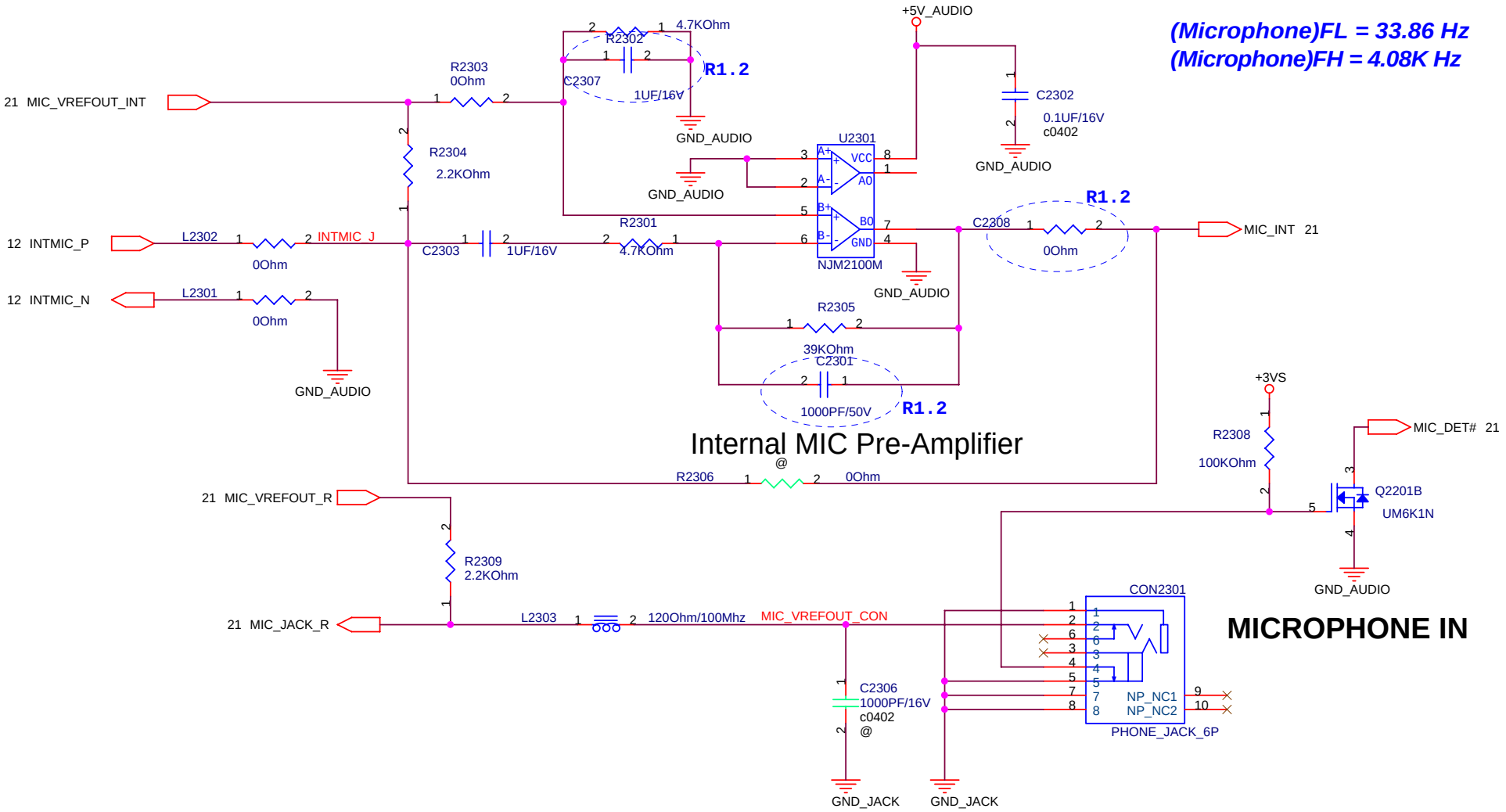
HP JACK

100PF/50V use 11G2330101043 11---change

Change for Layout

To Internal Speaker Connector





<Variant Name>

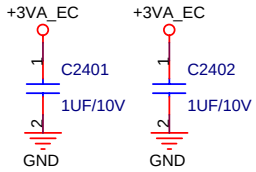
ASUSTeK COMPUTER INC

Title : MIC Pre-AMP

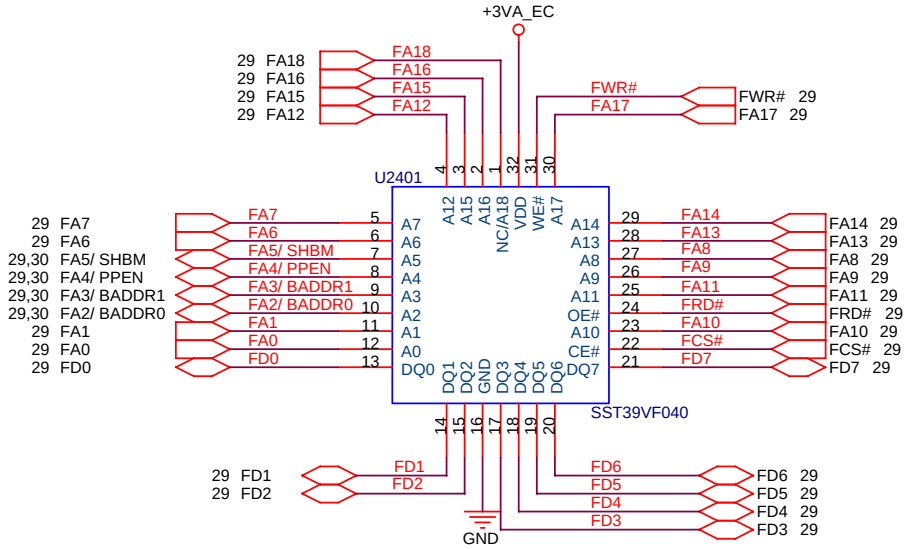
Engineer: Leon and George

Size	Project Name	Rev
A4	T12F	

Date: Friday, May 26, 2006 Sheet 23 of 61



ISA ROM



<Variant Name>

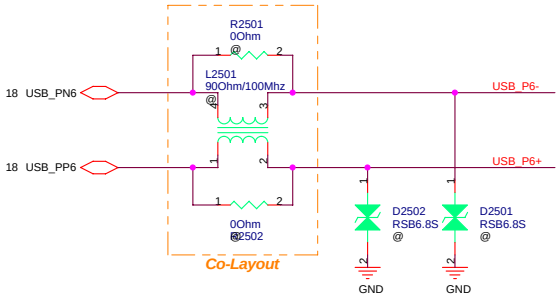
ASUSTeK COMPUTER INC

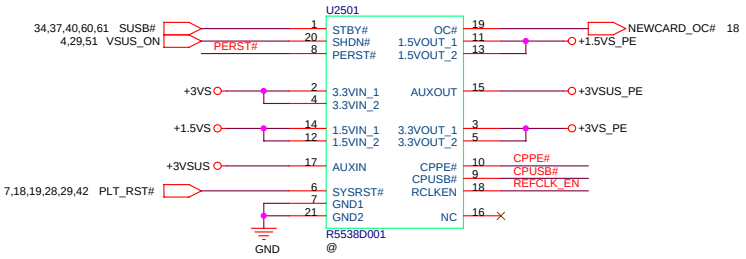
Title : ISA ROM

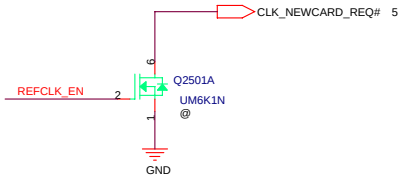
Engineer: Leon and George

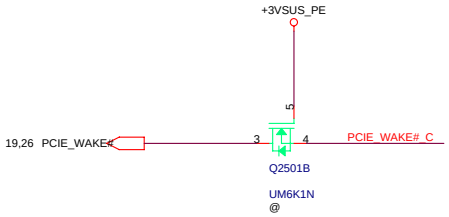
Size	Project Name	Rev
A4	T12F	

Date: Friday, May 26, 2006 Sheet 24 of 61



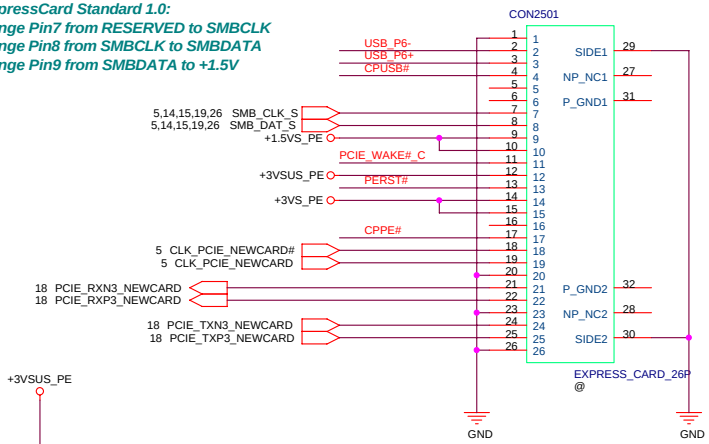


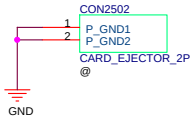


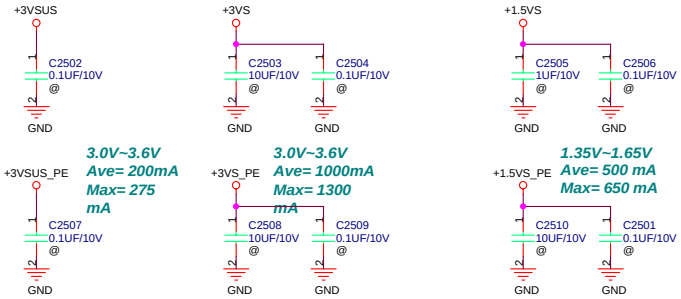


!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Header







<Variant Name>

ASUSTeK COMPUTER INC. NB1

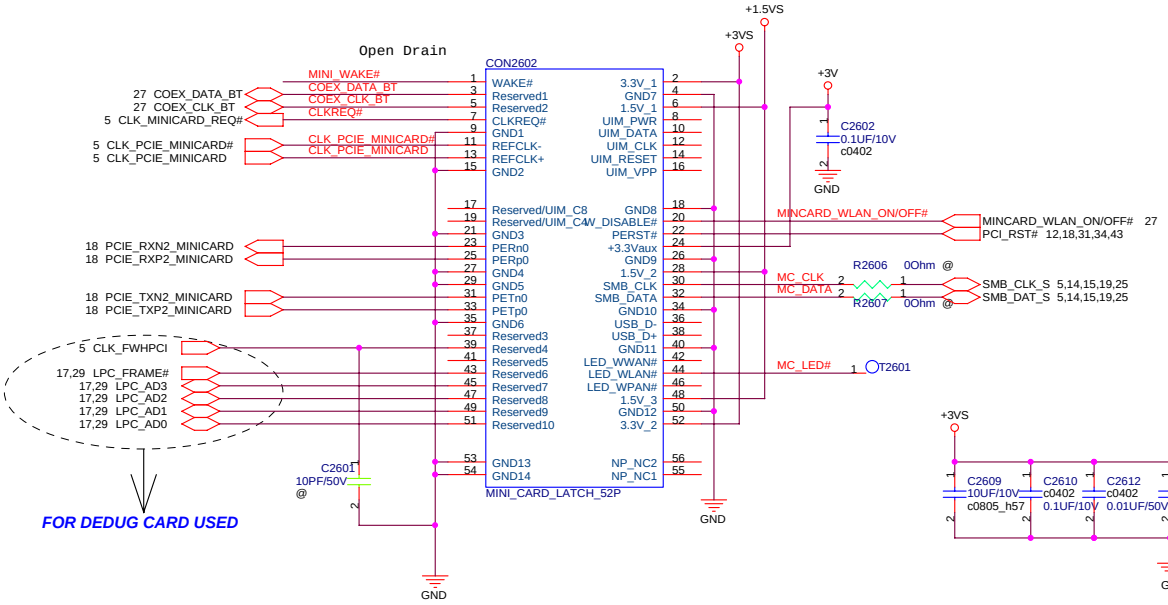
Title : NEWCARD

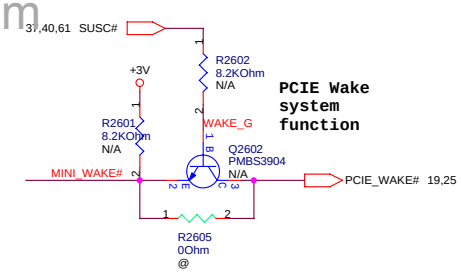
Engineer: *Leon and George*

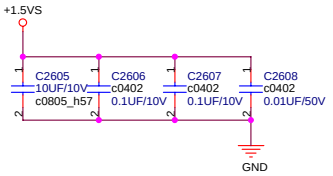
Size	Project Name	Rev
Custom	T12F	

Date: Friday, May 26, 2006 Sheet 25 of 61

MINI PCIEX CONNECTOR

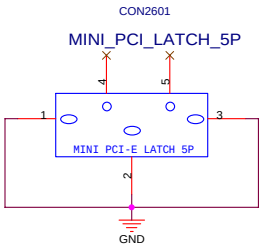


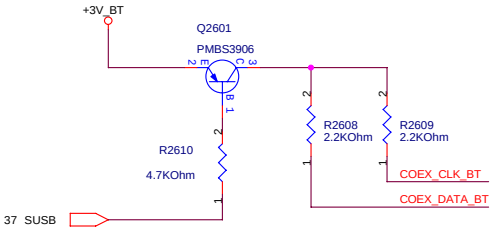


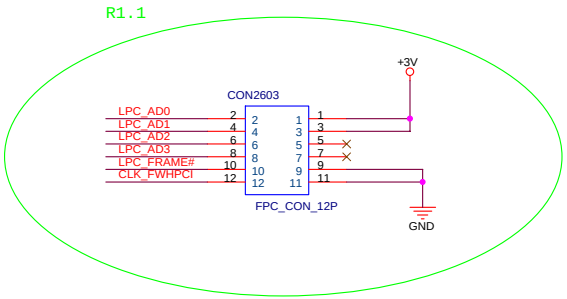


+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)

Check O/D output or push pull







<variant_name>

ASUSTeK COMPUTER INC

Title : MINI PCIEX

Engineer: Leon and George

Size	Project Name	Rev
A3	T12F	

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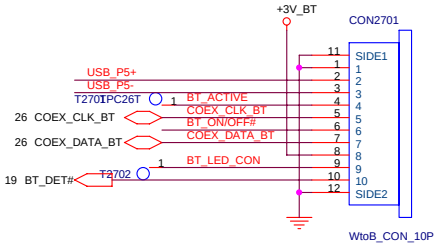
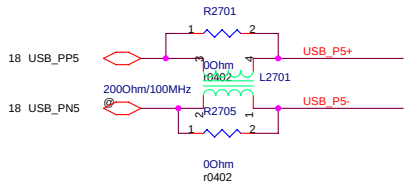
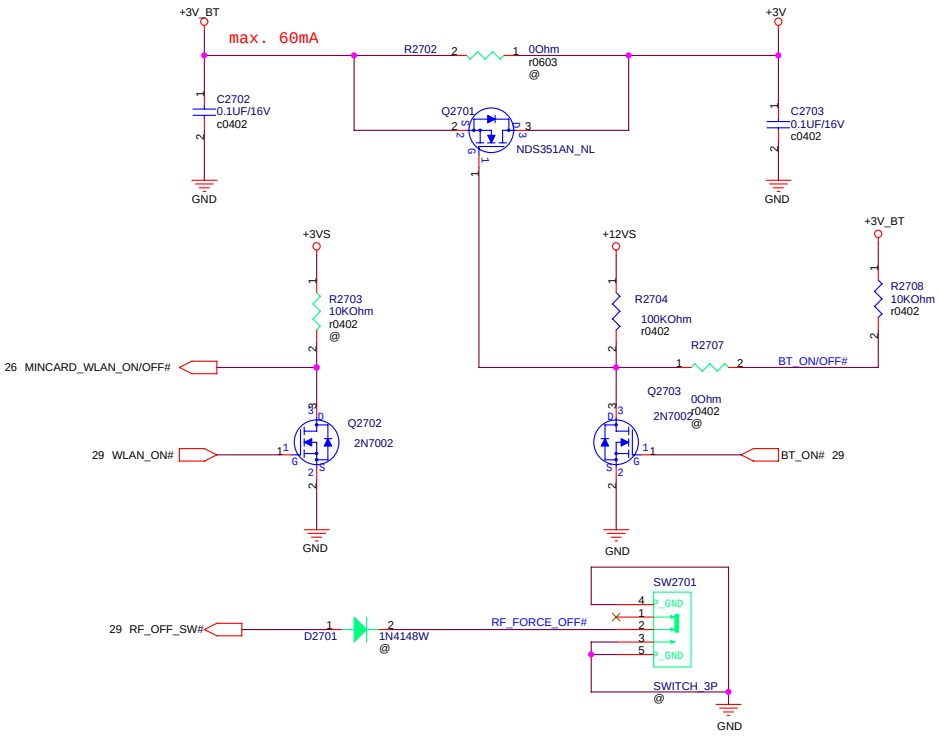
For Bluetooth





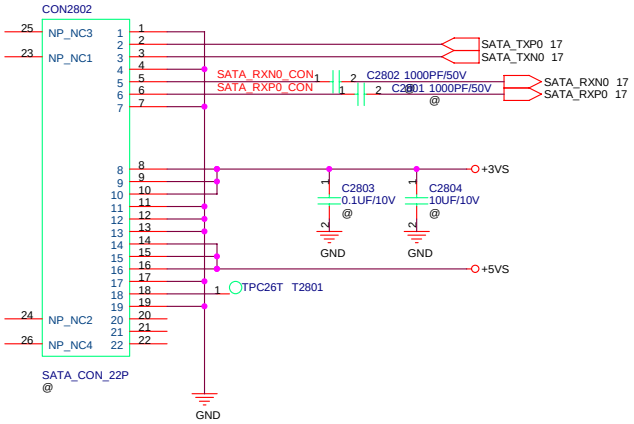
For Side SW

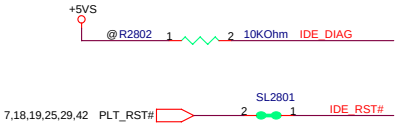
WLAN/BT ON/OFF Control

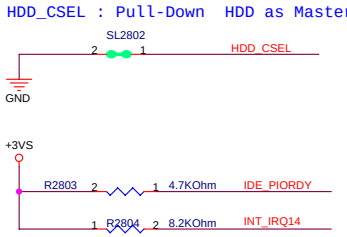


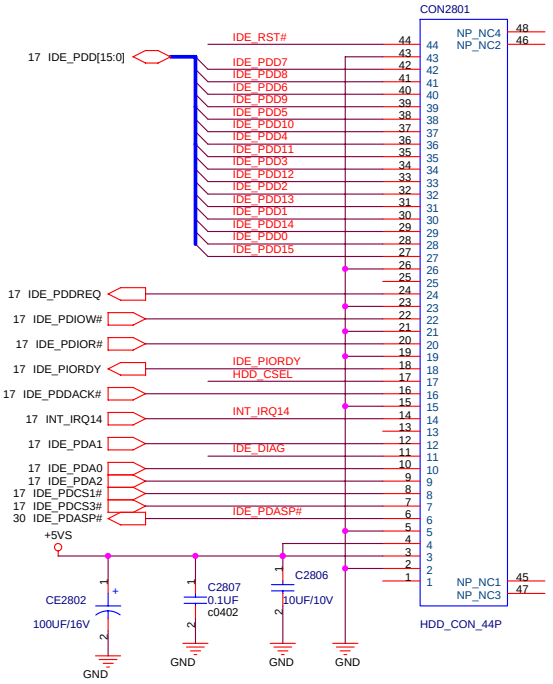
<Variant Name>

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 27 of 61	





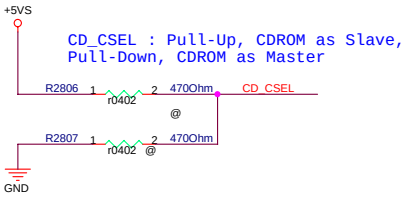


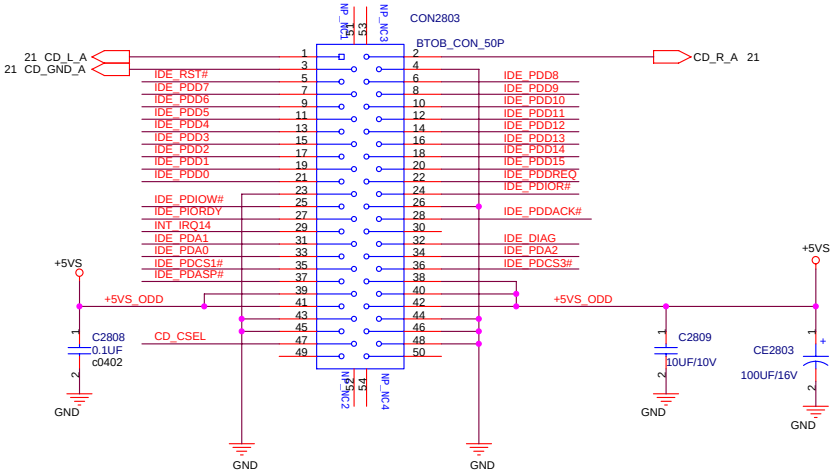


SATA HDD

PATA HDD

CD-ROM





<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : PATA-SATA & ODD

Engineer:

Size	Project Name	Rev
Custom	T12F	

Date: Friday, May 26, 2006 Sheet 28 of 61

TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

Follow Z94 Keyboard

U2901 — IT8511TE

LPC: LAD0 LAD1 LAD2 LAD3 LPCCLK LFRAME# LPCRST#/WUI4/GPD2 SERIRQ ECSMI#/GPM0 ECSCI#/GPD3 GA20/GPB5 KBRST#/GPB6 WRST# PWUREQ#/GPM1

FLASH ROM: FRD# FWR# FCS# FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7 FA0 FA1 FA2/BADDR0 FA3/BADDR1 FA4/PPEN FA5/SHBM FA6 FA7 FA8 FA9 FA10 FA11 FA12 FA13 FA14 FA15 FA16/GPG0 FA17/GPG1 FA18/GPG2 FA19/GPG3

KBMX: KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7 KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15

PS2: PS2CLK0/GPF0 PS2DAT0/GPF1 PS2CLK1/GPF2 PS2DAT1/GPF3

SMBus: SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2

ADC: ADC0/GPK0 ADC1/GPK1 ADC2/GPK2 ADC3/GPK3 ADC8/GPK4 ADC9/GPK5

DAC: DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3

GPIO: ADC4/GPE0 ADC5/GPE1 ADC6/GPE2 ADC7/GPE3 PWRSW/GPE4 WUI5/GPE5 LPCPD#/WUI6/GPE6 CLKRUN#/WUI7/GPE7 PS2CLK2/GPF4 PS2DAT2/GPF5 PS2CLK3/GPF6 PS2DAT3/GPF7 FA20/GPG4 FA21/GPG5 LPC80HL/GPG6 LPC80LL/GPG7 GPH0 GPH1 GPH2 GPH3 GPH4 GPH5 GPH6 GPH7 GPI0 GPI1 GPI2 GPI3 GPI4 GPI5 GPI6

to Battery

to Thermal

TBD

R2.0 close to EC

Cload=12.5PF

Layout Note: Close to Switch

watchdog

Change threshold = 2.9V

tD = 0.69*10^6*CD ps = 6.9 ms

Title : EC IT8510TE

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size: A3 | Project Name: T12F | Rev

Date: Tuesday, May 30, 2006 | Sheet 29 of 61

EC Hardware Strap

Strap value sampled after VSTBY power up reset

+3VA_EC

PNPCFG base address set by SWCBAHR/SWCBALR

R3002 @ 10KOhm r0402 — FA2/ BADDR0 — FA2/ BADDR0 24,29 — R3006 10KOhm r0402 — GND

+3VA_EC — R3003 10KOhm r0402 — FA3/ BADDR1 — FA3/ BADDR1 24,29 — R3007 @ 10KOhm r0402 — GND

BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

EC ADC

Battery

BAT — **16.8V** — R3004 @ 18KOhm r0402_h16 — BAT0_R_AD — R3005 @ 1KOhm — BAT0_AD 29 — R3008 @ 3.92KOhm — GND

+3VACC — D3002 @ 1N4148W — D3003 @ 1N4148W — C3002 @ 0.1UF/10V c0402

Adaptor

A/D_DOCK_IN — **19V** — R3009 @ 20KOhm — AC_R_AD — R3011 @ 1KOhm — AC_AD 29 — R3012 @ 3.74KOhm — GND

+3VACC — D3001 @ 1N4148W — D3004 @ 1N4148W — C3003 @ 0.1UF/10V c0402

3V — **2.99V**

+3VA_EC

Share Memory

R3010 10KOhm r0402 — FA5/ SHBM — FA5/ SHBM 24,29 — R3013 @ 10KOhm r0402 — GND

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

+3VA_EC — R3001 @ 10KOhm r0402 — FA4/ PPEN — FA4/ PPEN 24,29 — R3014 10KOhm r0402 — GND

PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

+5VS — +5VS_TP — +5VSUS — +5V

C3004 0.01UF/25V — C3005 0.1UF/10V — GND

L3001 — 80Ohm/100Mhz — C3001 0.1UF/10V — GND

FPC_CON_19P — CON3001 — SIDE2 — SIDE1

HDD_LED# — 802_LED#_R — CHG_LED#_R — PWR_LED#_R

29 CRX — 29 TPAD_DAT — 29 TPAD_CLK

Touchpad I/F

Touchpad

+3VS — +5VS

R3019 10KOhm — R3020 10KOhm — D3005

17 SATA_LED# — 28 IDE_PDASP# — HDD_LED#

DAP202K — R3018 @ 0Ohm

HDD LED

CHARGE LED

+5VSUS — R3015 10KOhm — T3001 — Q3001B UM6K1N — Q3001A UM6K1N — 29 CHG_LED_UP# — CHG_LED#_R — GND

POWER LED

+5V — R3017 10KOhm — Q3002A UM6K1N — Q3002B UM6K1N — 29 PWR_LED_UP# — PWR_LED#_R — PWR_LED#_R 38 — GND

WLAN LED

19 WLAN_LED# — R3021 0Ohm — 29,38 RF_LED — R3022 0Ohm

+5VS — R3016 10KOhm — Q3004A UM6K1N — Q3004B UM6K1N — 802_LED#_R — GND

R1.2

<Variant Name>

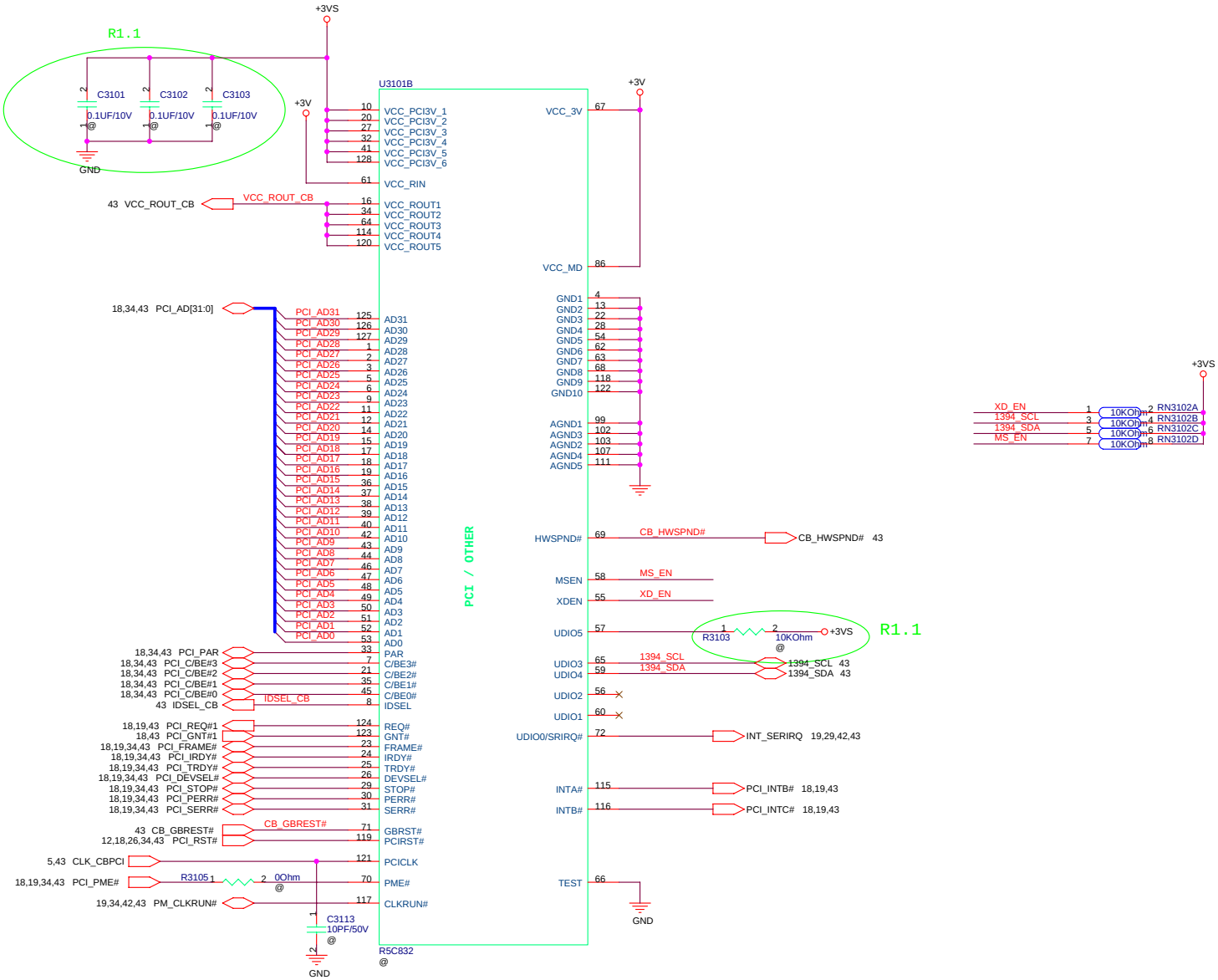
ASUSTeK COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: *Leon and George*

Size	Project Name	Rev
A3	T12F	

Date: Friday, May 26, 2006 — Sheet 30 of 61



<Variant Name>

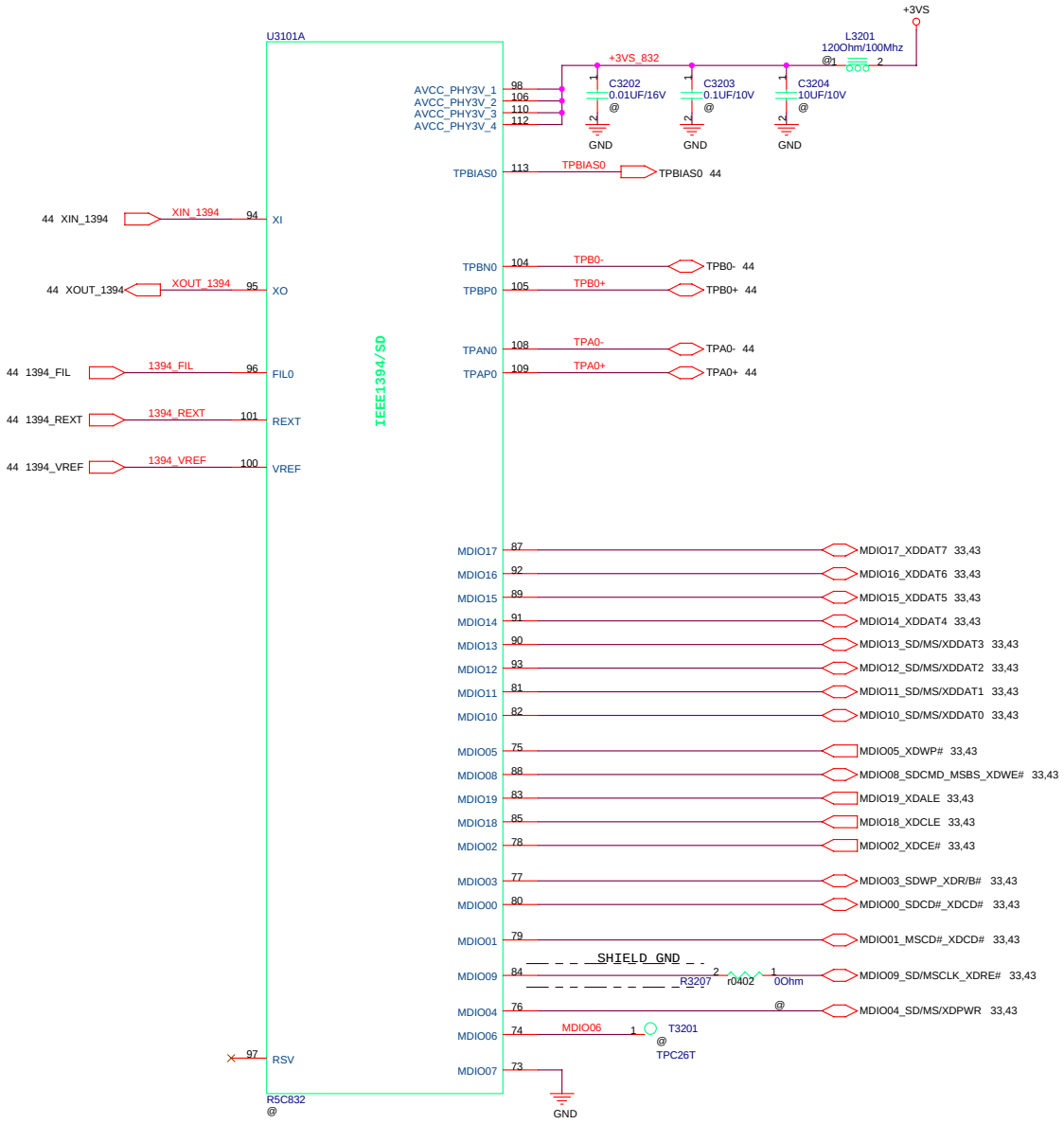
Title : CARD1394-R5C832(1)

ASUSTeK COMPUTER INC. NB1

Engineer: Leon and George

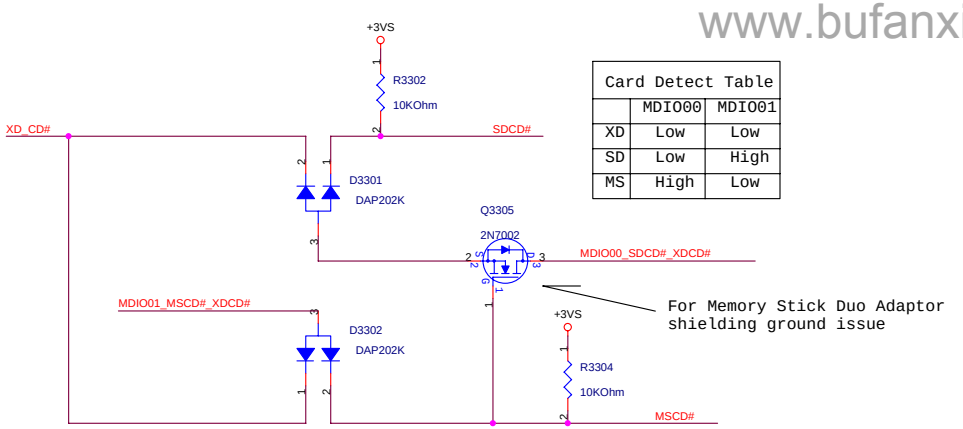
Size	Project Name	Rev
Custom	T12F	

Date: Friday, May 26, 2006 Sheet 31 of 61



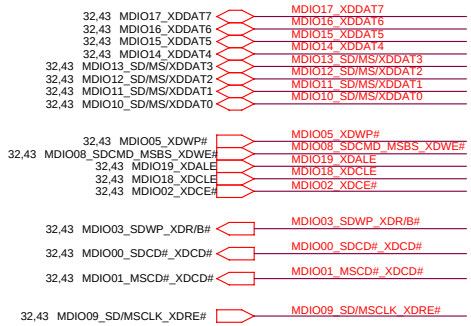
<Variant Name>

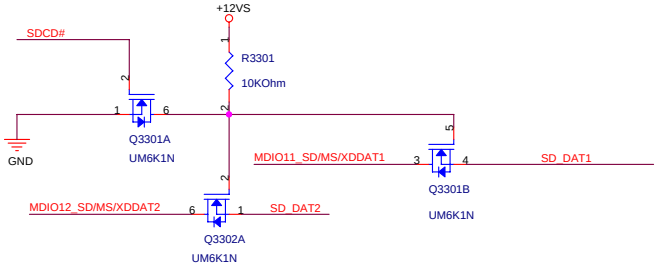
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 32 of 61	

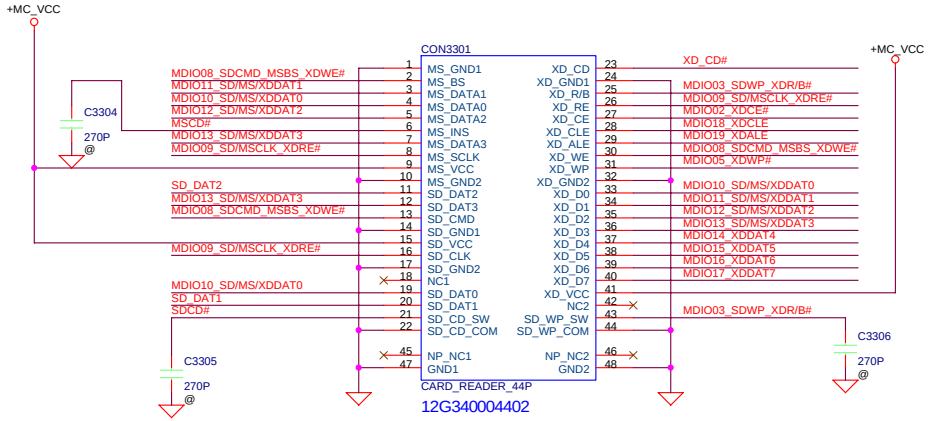


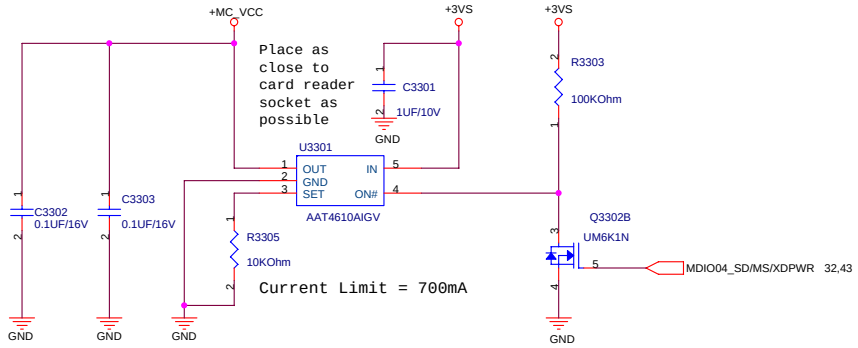
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU









<Variant Name>

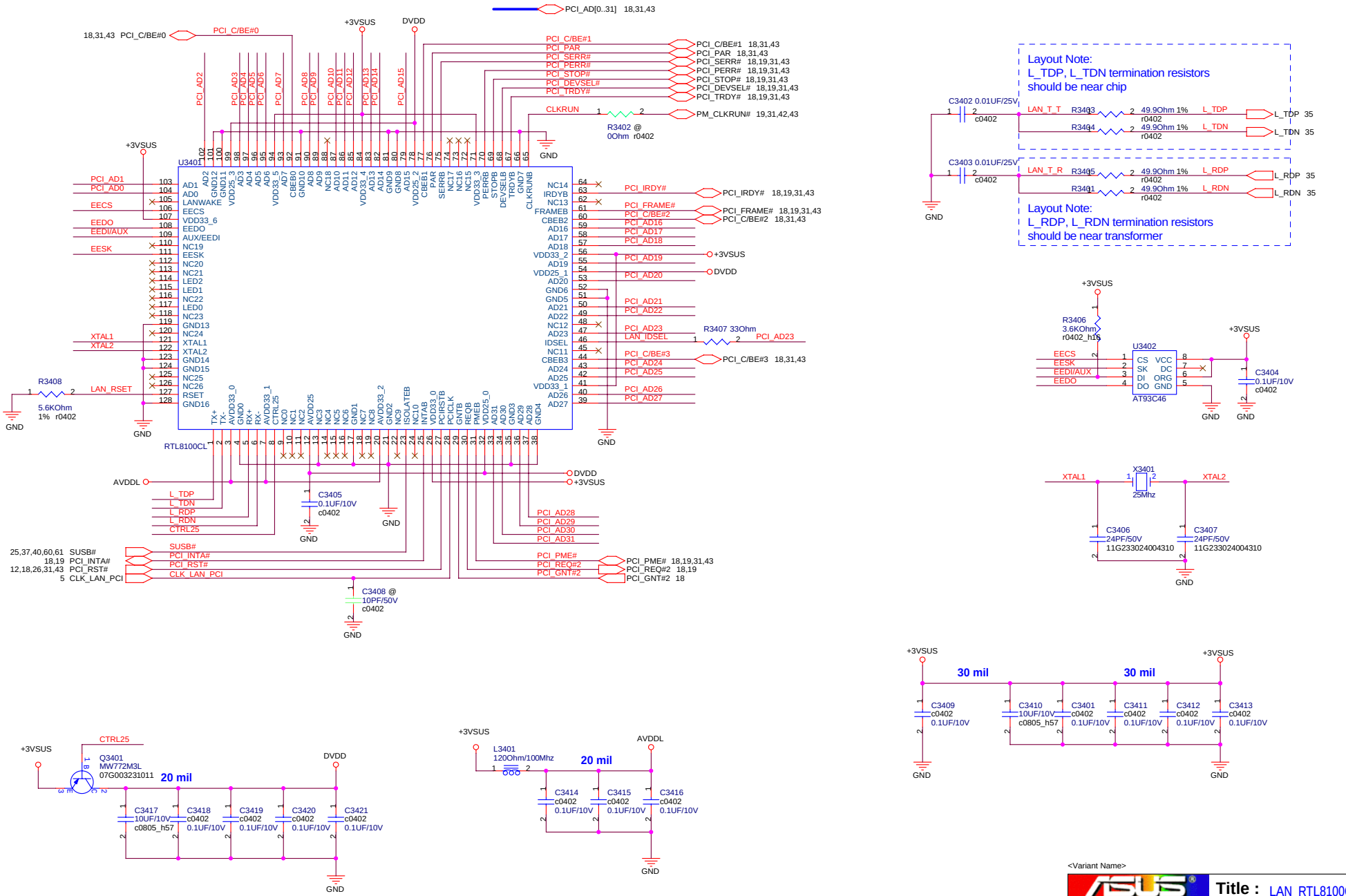
ASUSTeK COMPUTER INC

Title : 4 in 1 CARD READER

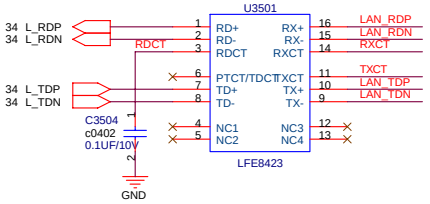
Engineer: Leon and George

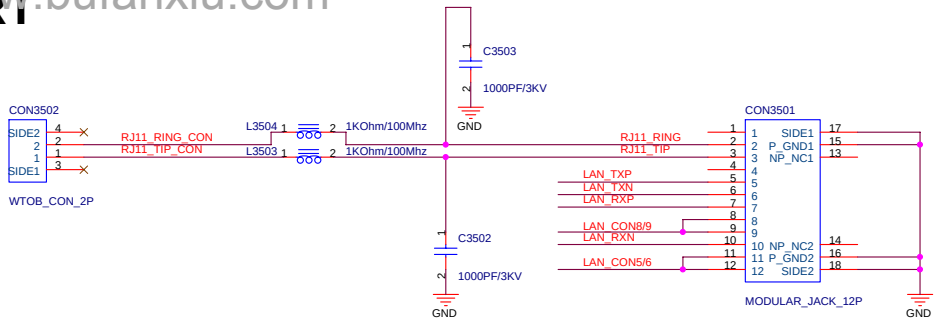
Size	Project Name	Rev
Custom	T12F	

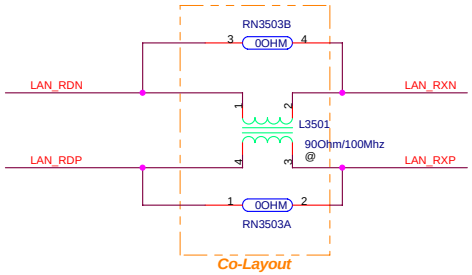
Date: Friday, May 26, 2006 Sheet 33 of 61

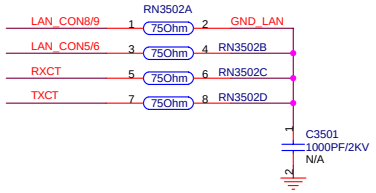


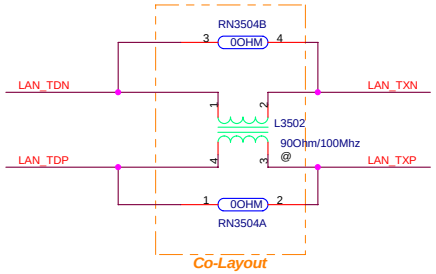
LAN PORT





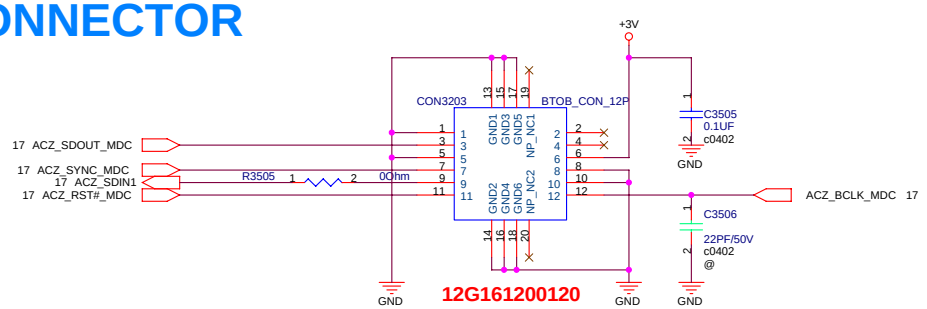


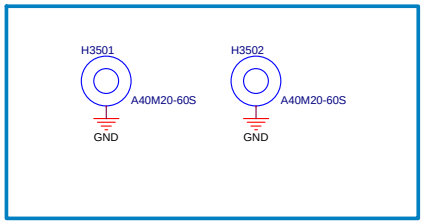




R1.1

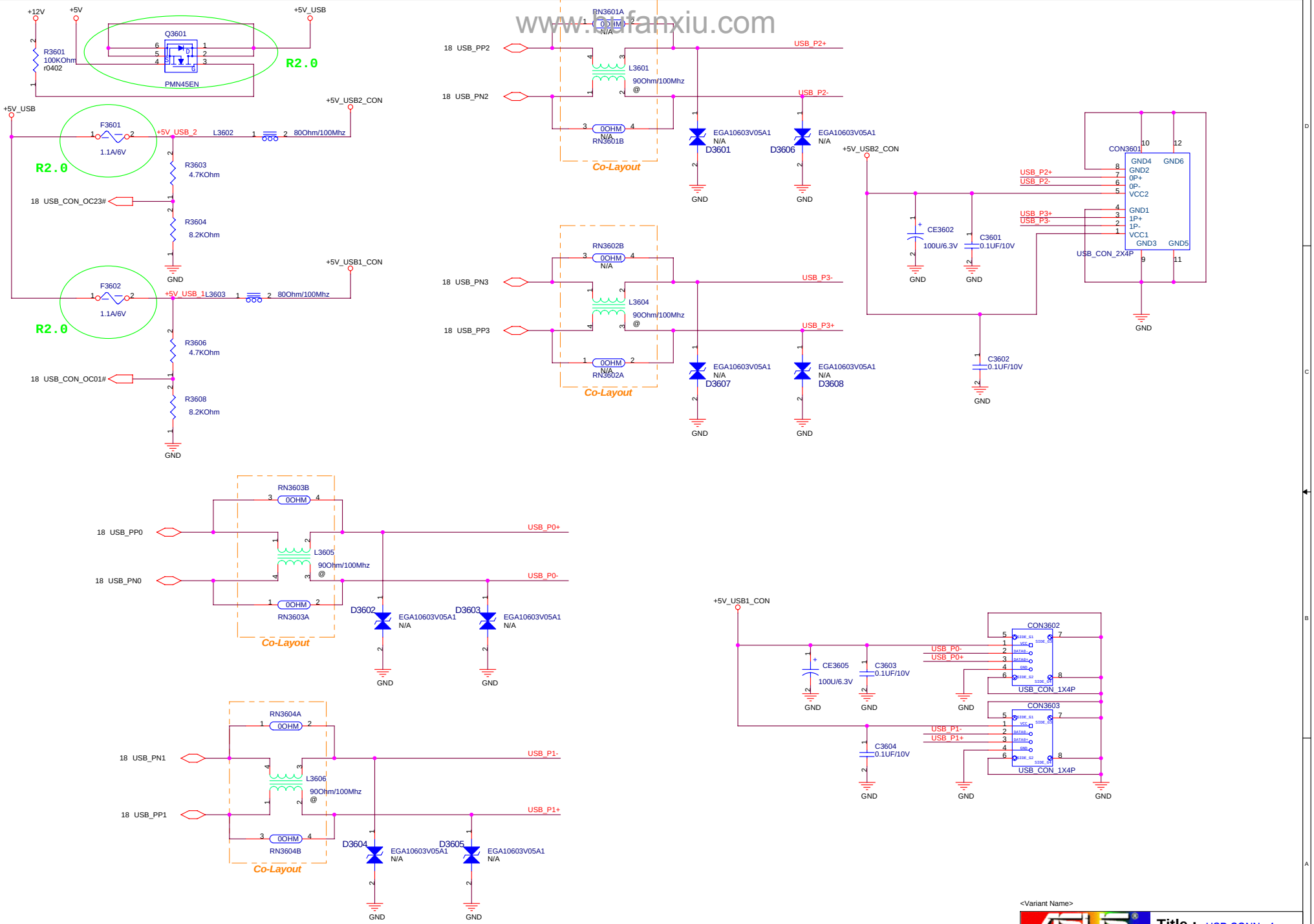
MDC CONNECTOR





<variant_name>

ASUSTeK COMPUTER INC	Title : RJ11/45 & MDC	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 35 of 61	



<Variant Name>

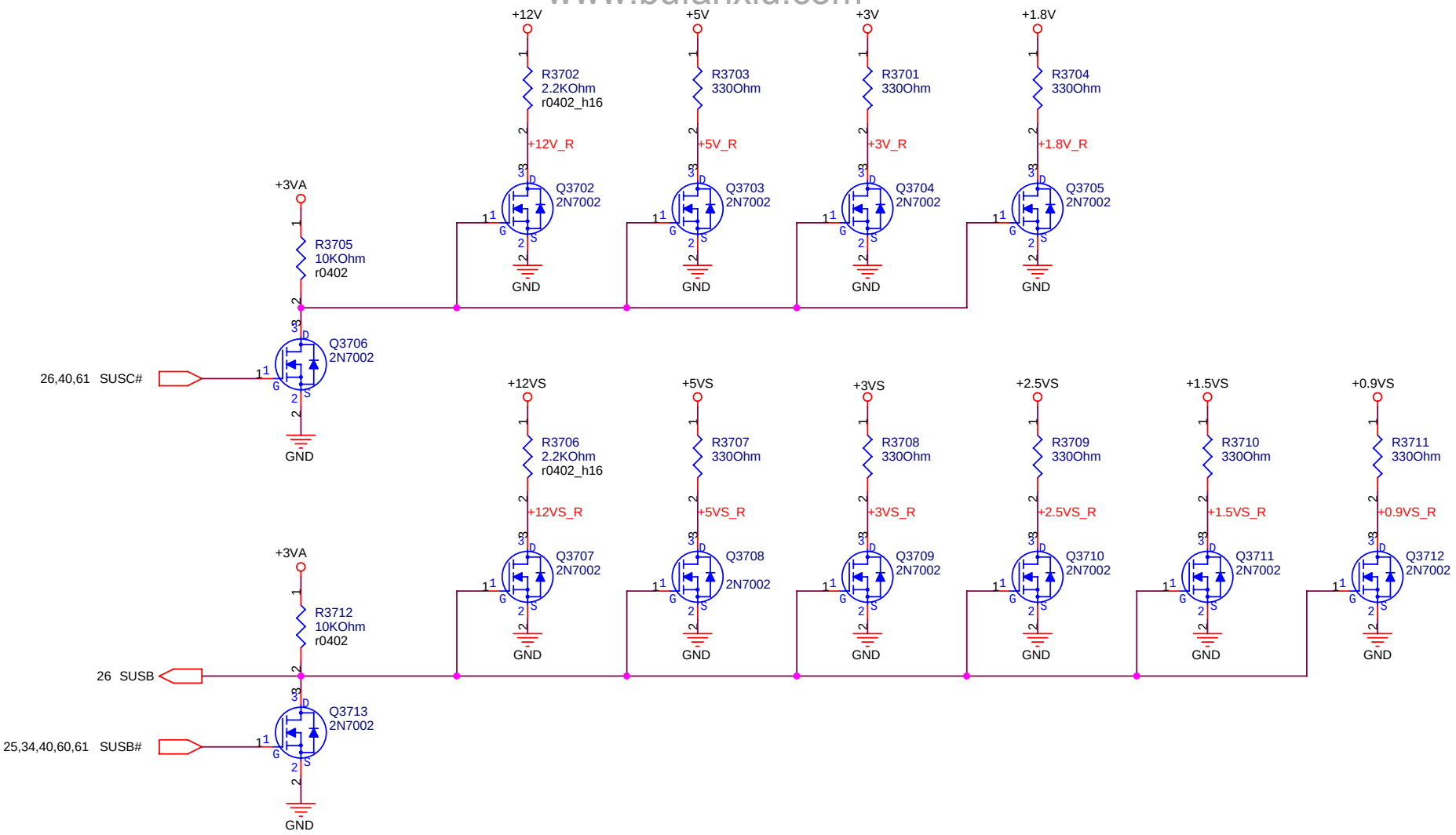
ASUSTeK COMPUTER INC. NB1

Title : USB CONN x4

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

Date: Tuesday, May 30, 2006 Sheet 36 of 61



<Variant Name>

ASUSTeK COMPUTER INC

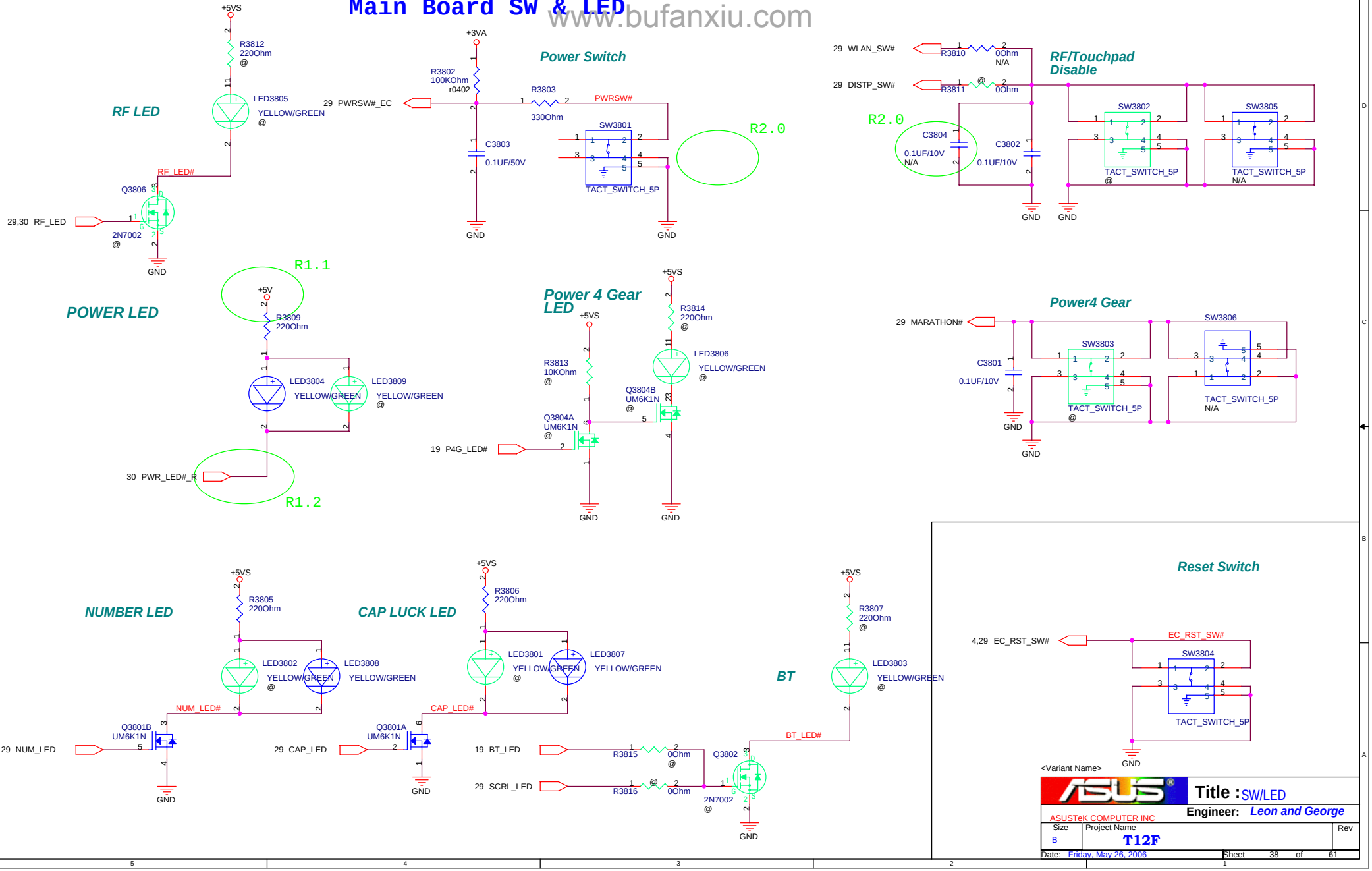
Title : Discharge Circuit

Engineer: *Leon and George*

Size	Project Name	Rev
A4	T12F	

Date: Friday, May 26, 2006 Sheet 37 of 61

Main Board SW & LED



<Variant Name>

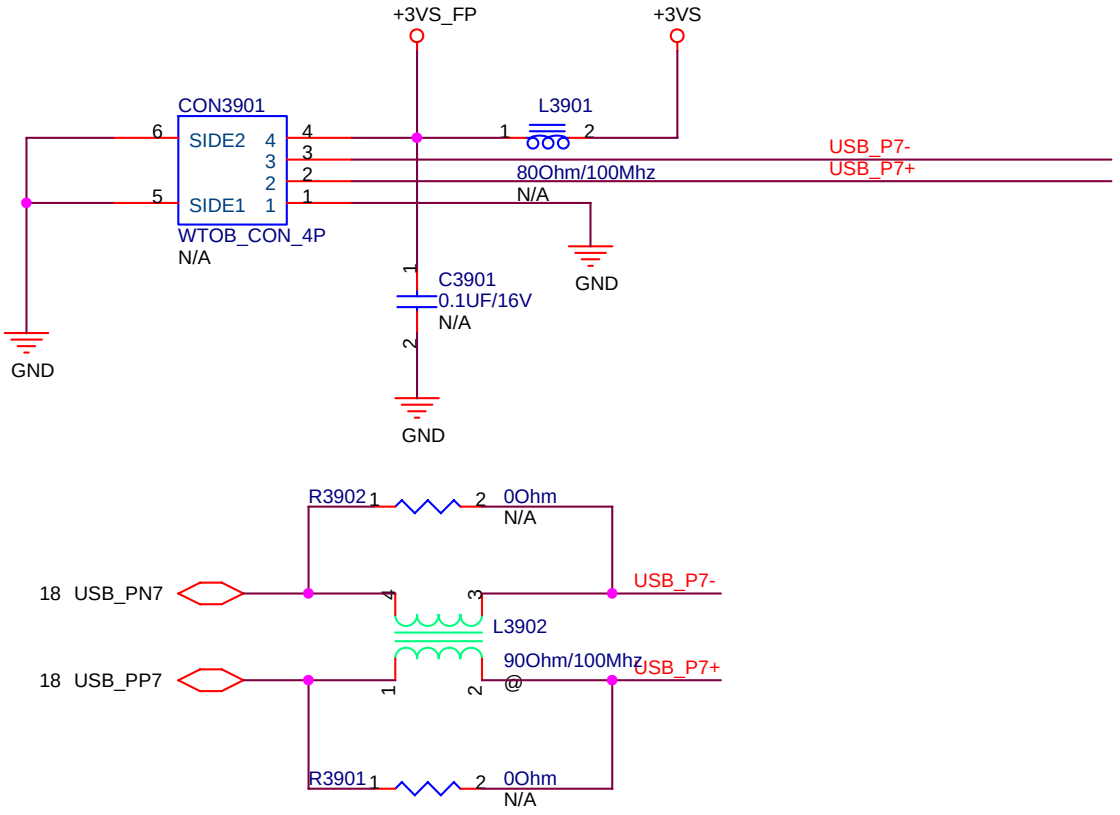
ASUSTeK COMPUTER INC

Title : SW/LED

Engineer: Leon and George

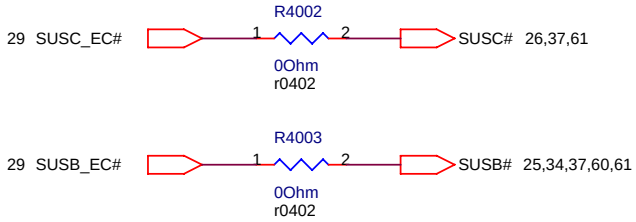
Size	Project Name	Rev
B	T12F	

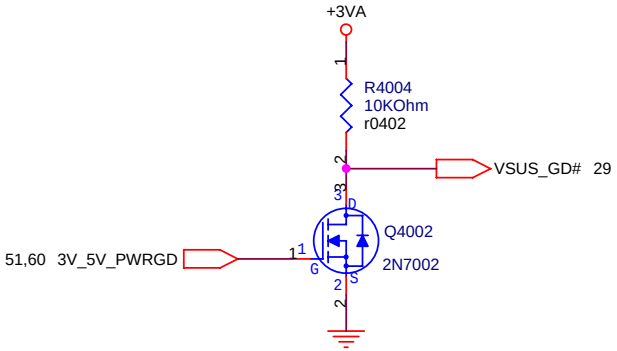
Date: Friday, May 26, 2006 Sheet 38 of 61

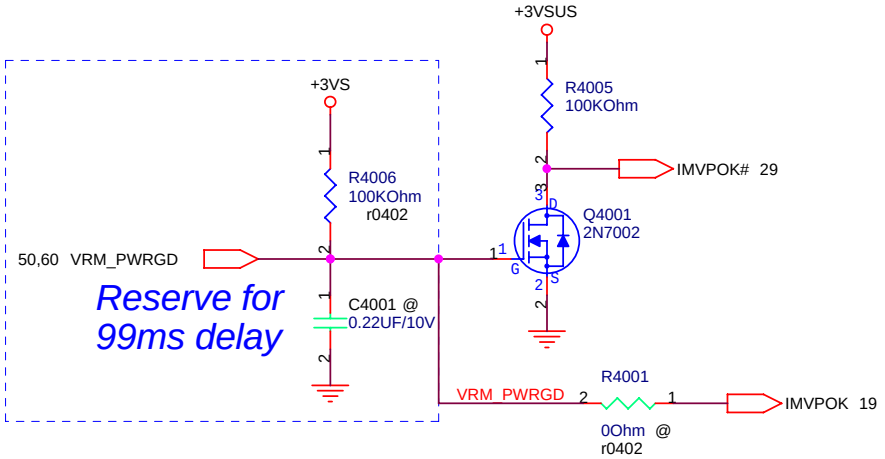


<Variant Name>

ASUSTeK COMPUTER INC	Title : FINGER PRINT	
	Engineer: Leon and George	
Size: A	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 39 of 61	







<Variant Name>

ASUSTeK COMPUTER INC

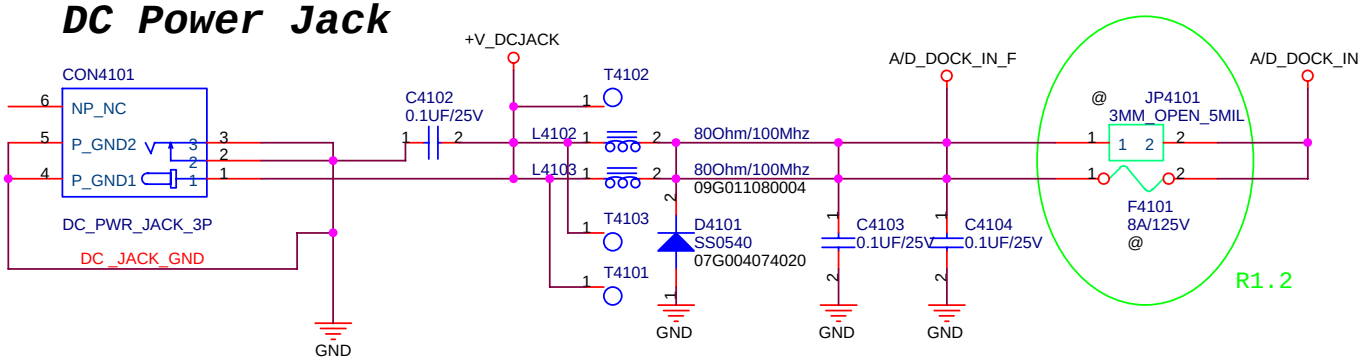
Title : POWER-ON SEQ.

Engineer: Leon and George

Size	Project Name	Rev
A4	T12F	

Date: Friday, May 26, 2006 Sheet 40 of 61

DC Power Jack



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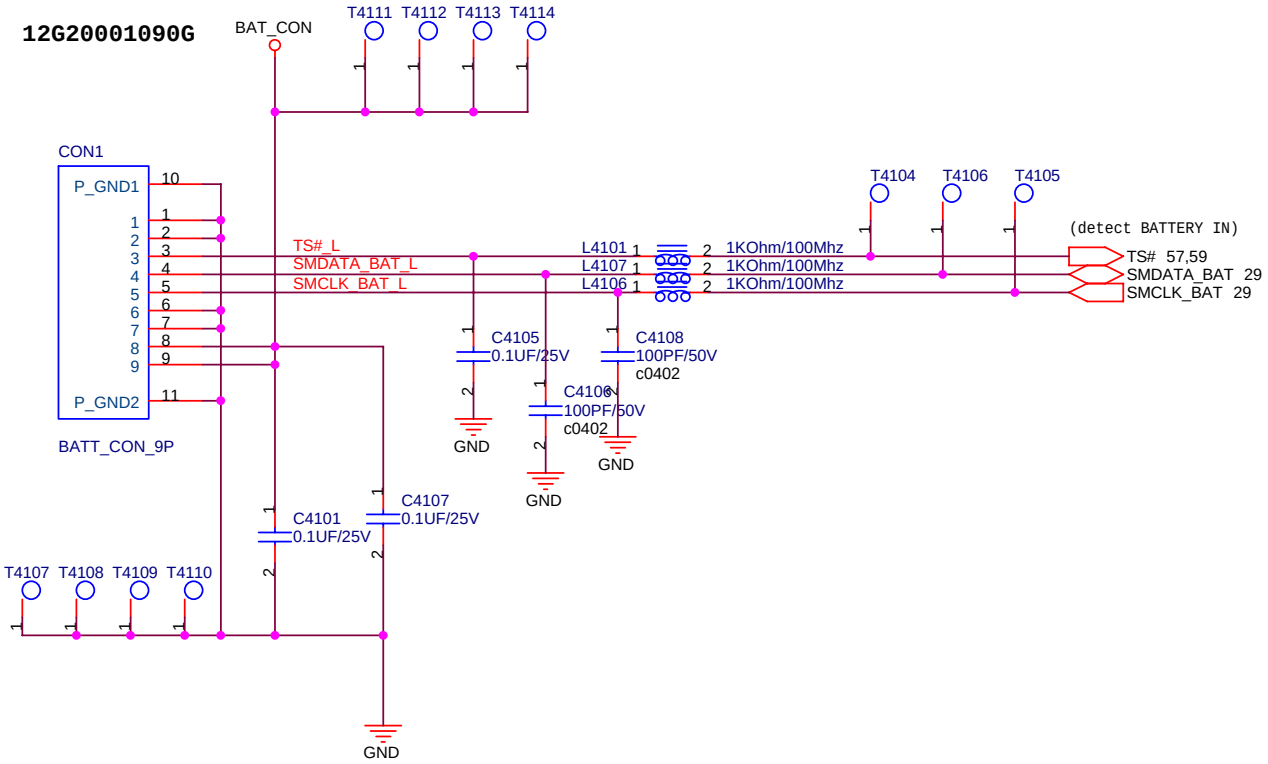
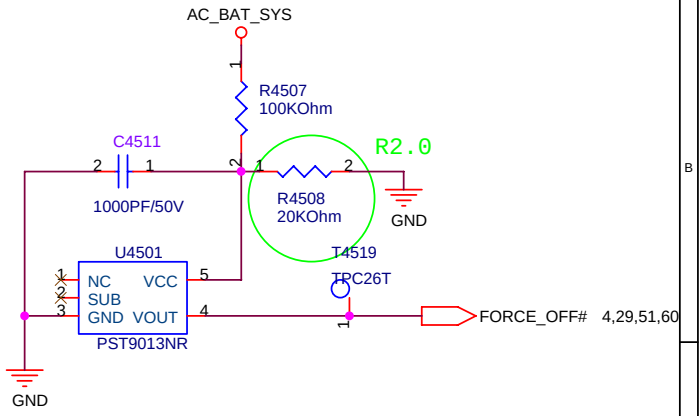
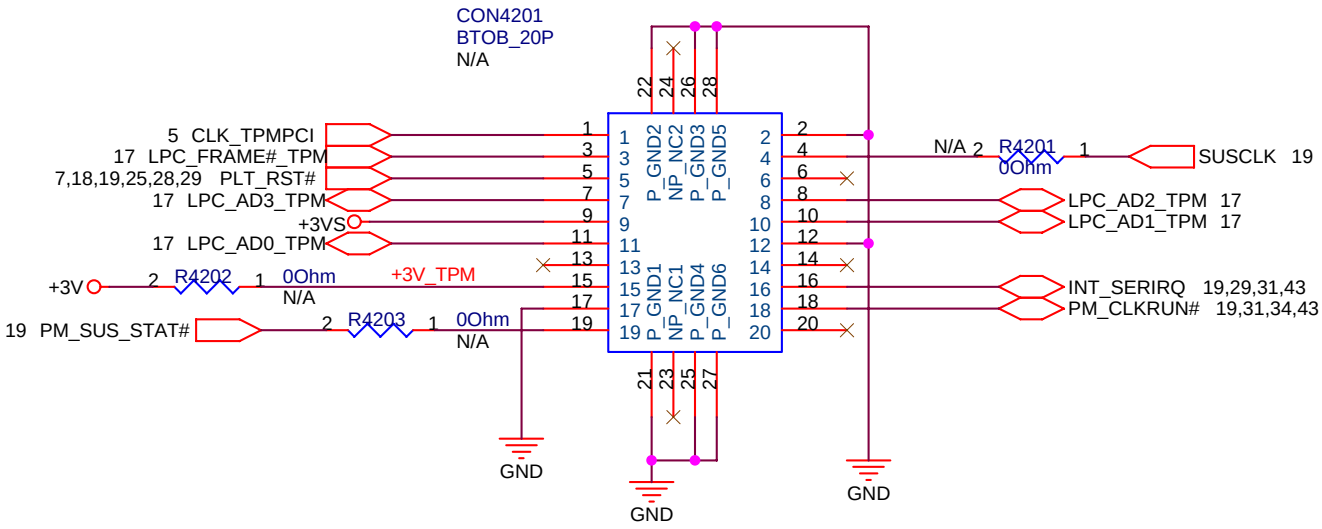


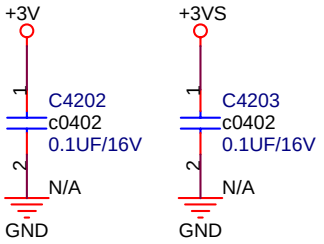
Without Battery & Pull out Adapter



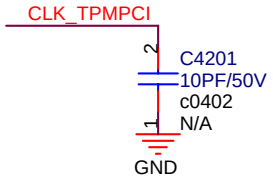
<Variant Name>

ASUSTeK COMPUTER INC	Title : DC/ BATT IN	
	Engineer: Leon and George	
Size: A4	Project Name: T12F	Rev
Date: Tuesday, May 30, 2006	Sheet 41 of 61	



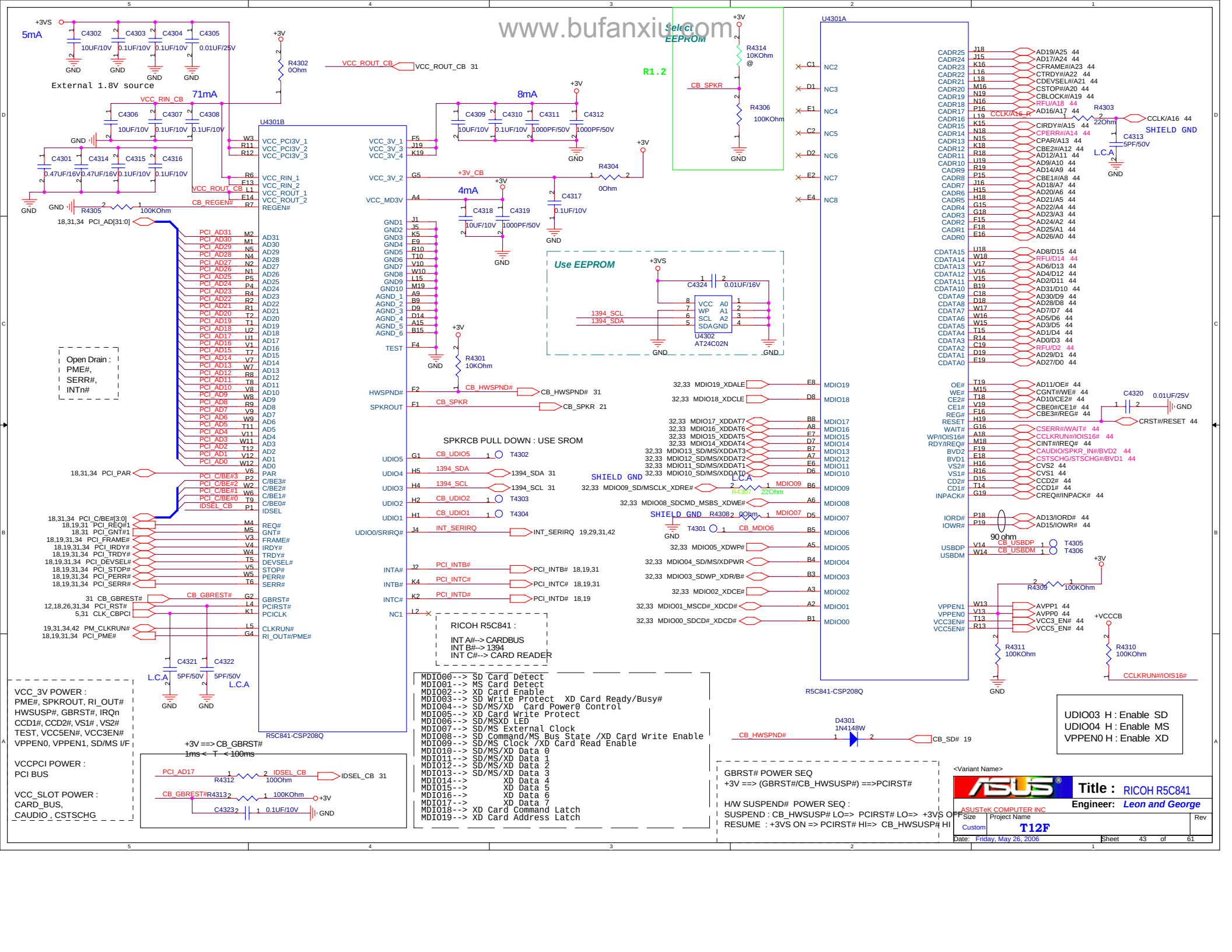


TPM Module CON



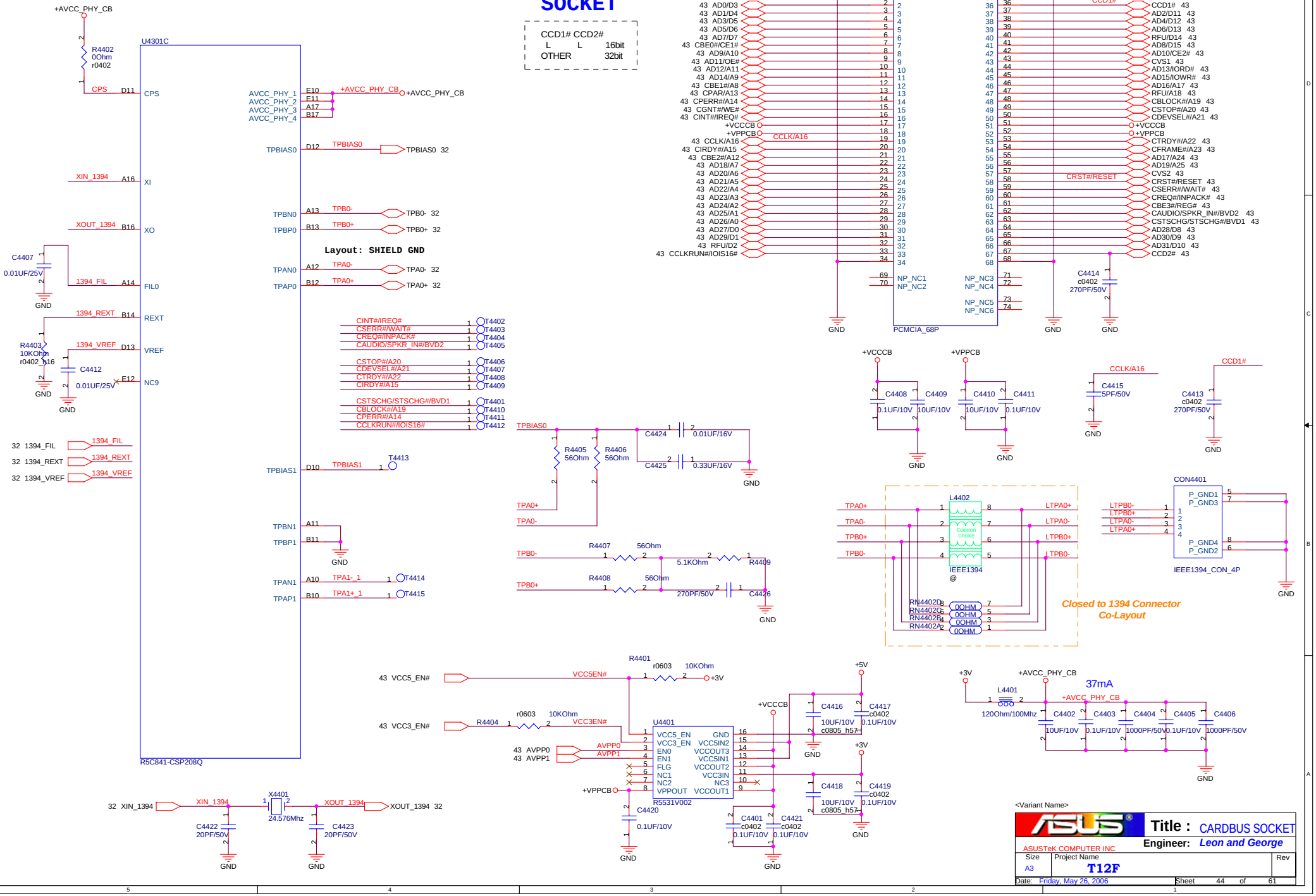
<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: ~	
Size: A	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 42 of 61	



PCMCIA SOCKET

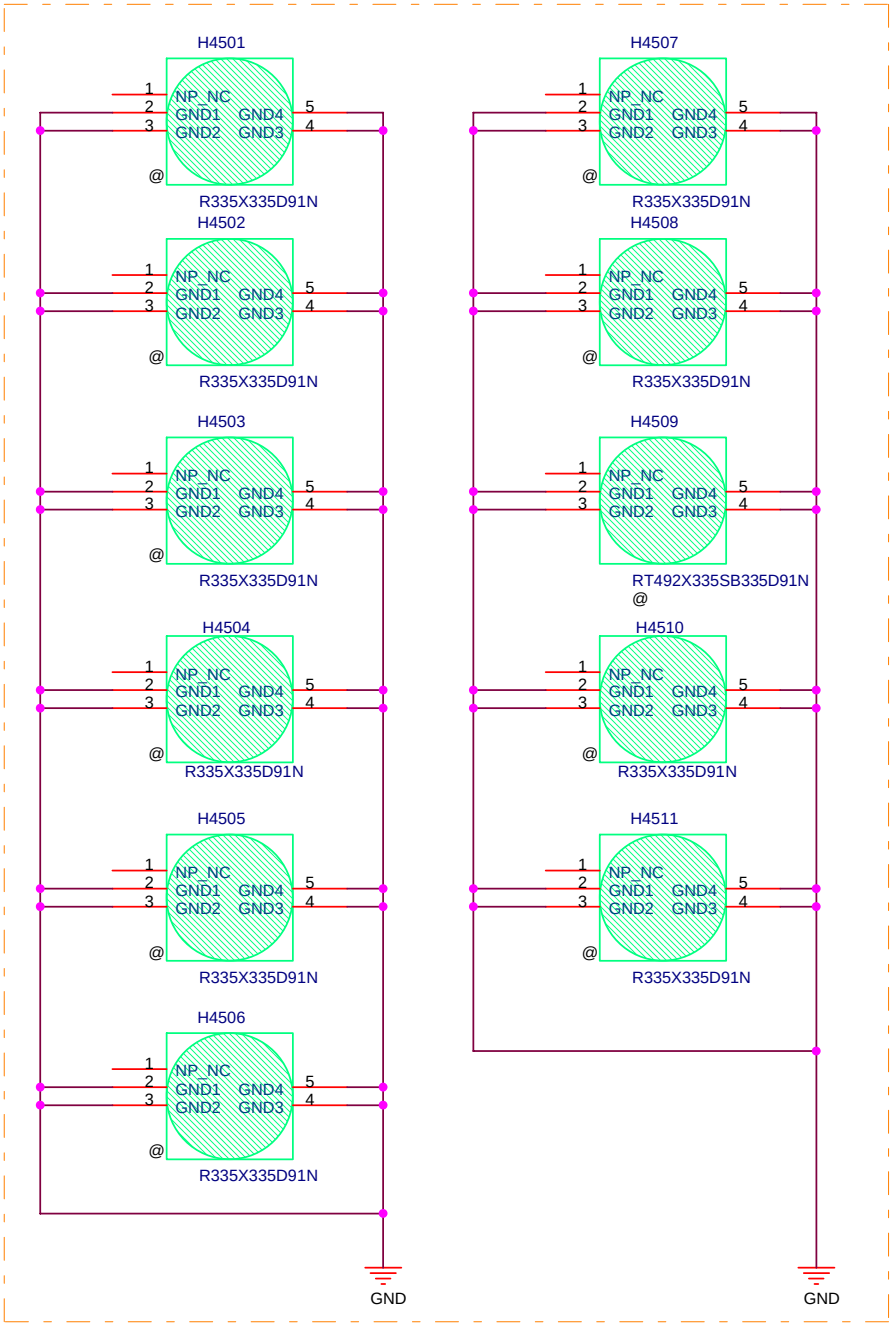
CCD1#	CCD2#	
L	L	16bit
OTHER		32bit



<variant_name>

Title : CARDBUS SOCKET		
Engineer: Leon and George		
ASUSTeK COMPUTER INC		
Size: A3	Project Name: T12F	Rev
Date: Friday, May 26, 2006	Sheet 44 of 61	

ABCDH



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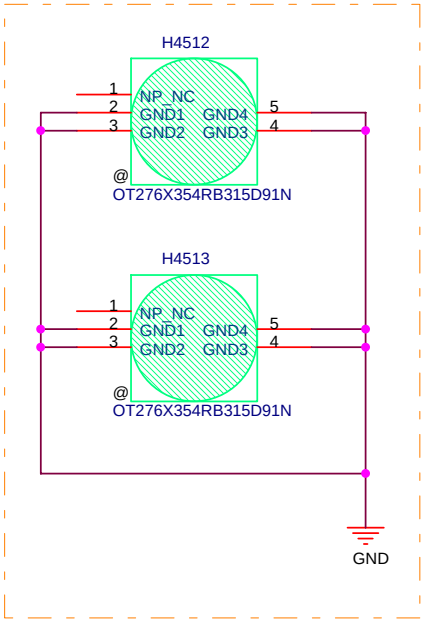

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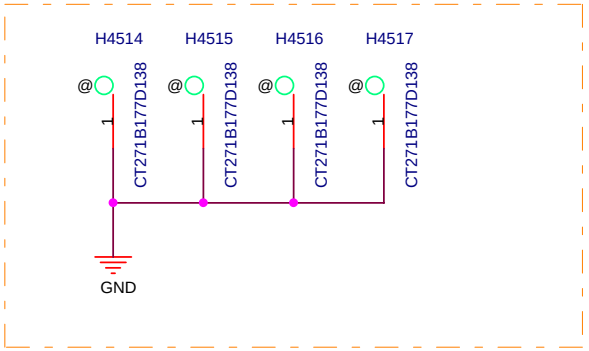

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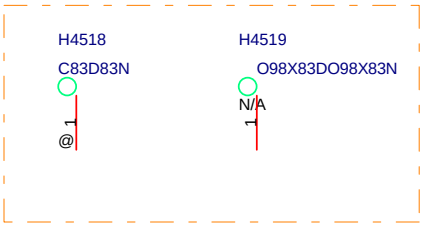

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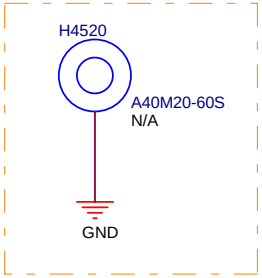

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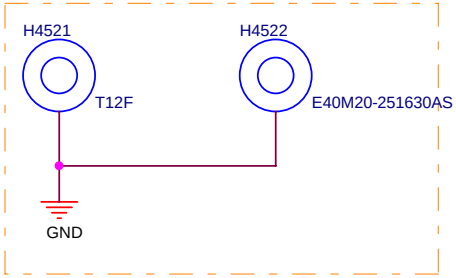

<Variant Name>

ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer: Leon and George

Size	Project Name	Rev
A4	T12F	

Date: Friday, May 26, 2006 Sheet 45 of 61

R1.1

Page	Action	Reason
5	Add R566,R567,R568,R569 to divide voltage.	Clock GEN output voltage is too high.
17	Add R1733~R1737 (Reserve)	For EMI request
17	Add R1729~R1732	Add MDC feature
22	Change C2222 from 0.1uF to 0.47uF	Delay the HP turn-on timing to avoid noise at the system power on.
22	Add R2233 and L2202 to link the different GND	For EMI request
26	Add CON2603	Only use for debug, it will be deleted before MP
31	Add C3101~C3103	Reduce power rippler of R5C832
31	Add R3103	UDIO5 pull high to disable external EEPROM
35	Add CON3203 and MDC relative circuit	Add MDC feature
38	Change power LED power from +5VS to +5V	Slove LED can't flash in S3

R1.2

Page	Action	Reason
4	Add U402 and relative circuit.	Add hardware thermal protection circuit
12	Change L1204,L1205,C1209,1210	For EMI request
12	Change L1210 to 1k ohm	Reduce leakage current.
13	Change L1304~L1306 to 150nH and C1308 C1310 C1312 change to 10pF	Improve CRT signal
21	All R1.2 modification in this page	Follow ADI recommend vlaue to get Vista logo.
22	All R1.2 modification in this page	Follow ADI recommend vlaue to get Vista logo.
23	All R1.2 modification in this page	Improve microphone quality
30	Add R3022	Reserve RF_LED feature
38	Del Q3005 and link PWR_LED#_R to LED directly	Cost down
41	Add F4101 and JP4101	Reserve, normal use JP4101
43	Add R4314	Reserve, normal no use

R2.0

Page	Action	Reason
21	Add R2111 to pull high	Avoid input pin NC.
36	Modify Q3601 circuit	Solve system will auto turn-on when remove USB HDD with external power.

<Variant Name>

Title : HISTORY

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
A3	T12F	

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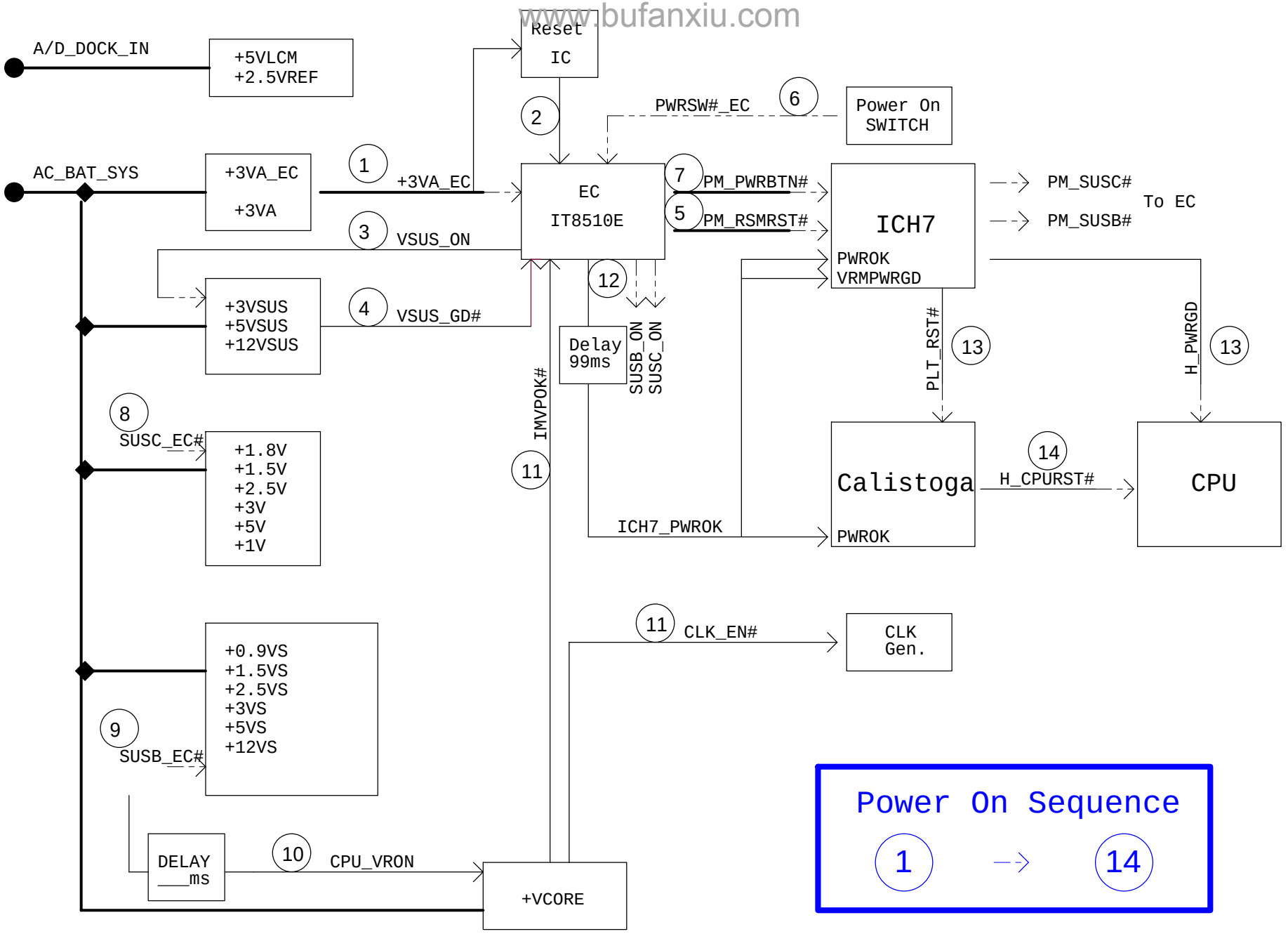

<Variant Name>

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMCLK_BAT	I/0
164	SMDAT0GPB4	SMDATA_BAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	RI1#/WUI0/GPD0	PM_SUSB#	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4		I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	O
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	/	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWRSW#_EC	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7		O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	IMVPOK#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
8	GPL0	WLAN_ON#	O
11	GPL1	BT_ON#	O
12	GPL2	RF_OFF_SW#	I
20	GPL3	RF_LED	O
92	CRX	CRX	I/0

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

Title : GPIO Setting

ASUSTeK COMPUTER INC

Engineer: Leon and George

Size	Project Name	Rev
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<Variant Name>

Title : N/A

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12F	

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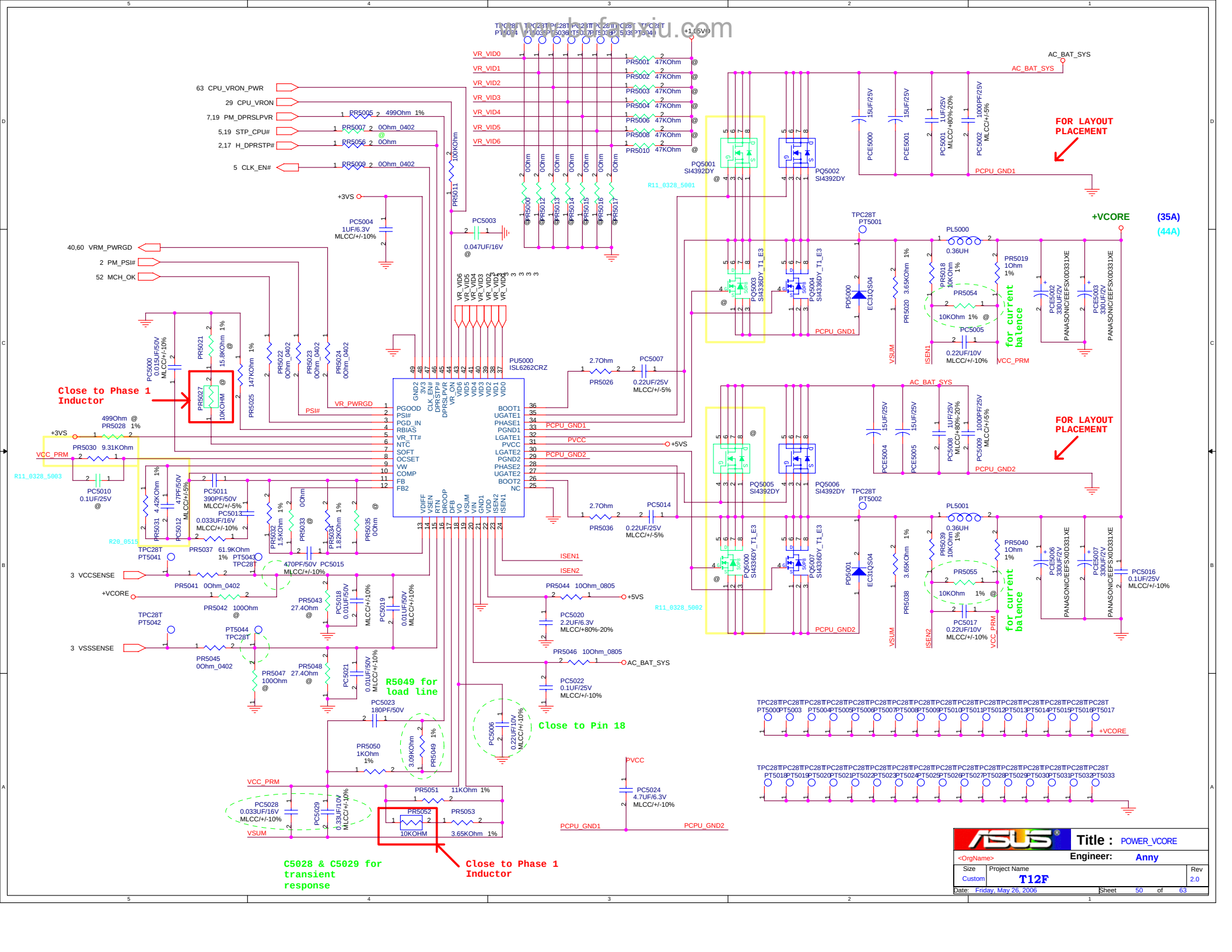
PU5000
ISL6262CRZ
PQ5001
SI4392DY
PQ5002
SI4392DY
PQ5003
SI4336DY_T1_E3
PQ5004
SI4336DY_T1_E3
PQ5005
SI4392DY
PQ5006
SI4392DY
PQ5007
SI4336DY_T1_E3
PQ5000
SI4336DY_T1_E3
PD5000
EC31QS04
PD5001
EC31QS04
PL5000
0.36UH
PL5001
0.36UH
+VCORE
(35A)
(44A)
AC_BAT_SYS
+5VS
+3VS
PCPU_GND1
PCPU_GND2
PVCC
VCC_PRM
VSUM
ISEN1
ISEN2
FOR LAYOUT PLACEMENT
for current balence
Close to Phase 1 Inductor
Close to Pin 18
R5049 for load line
C5028 & C5029 for transient response
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer: Anny
Project Name T12F
Rev 2.0
Date: Friday, May 26, 2006
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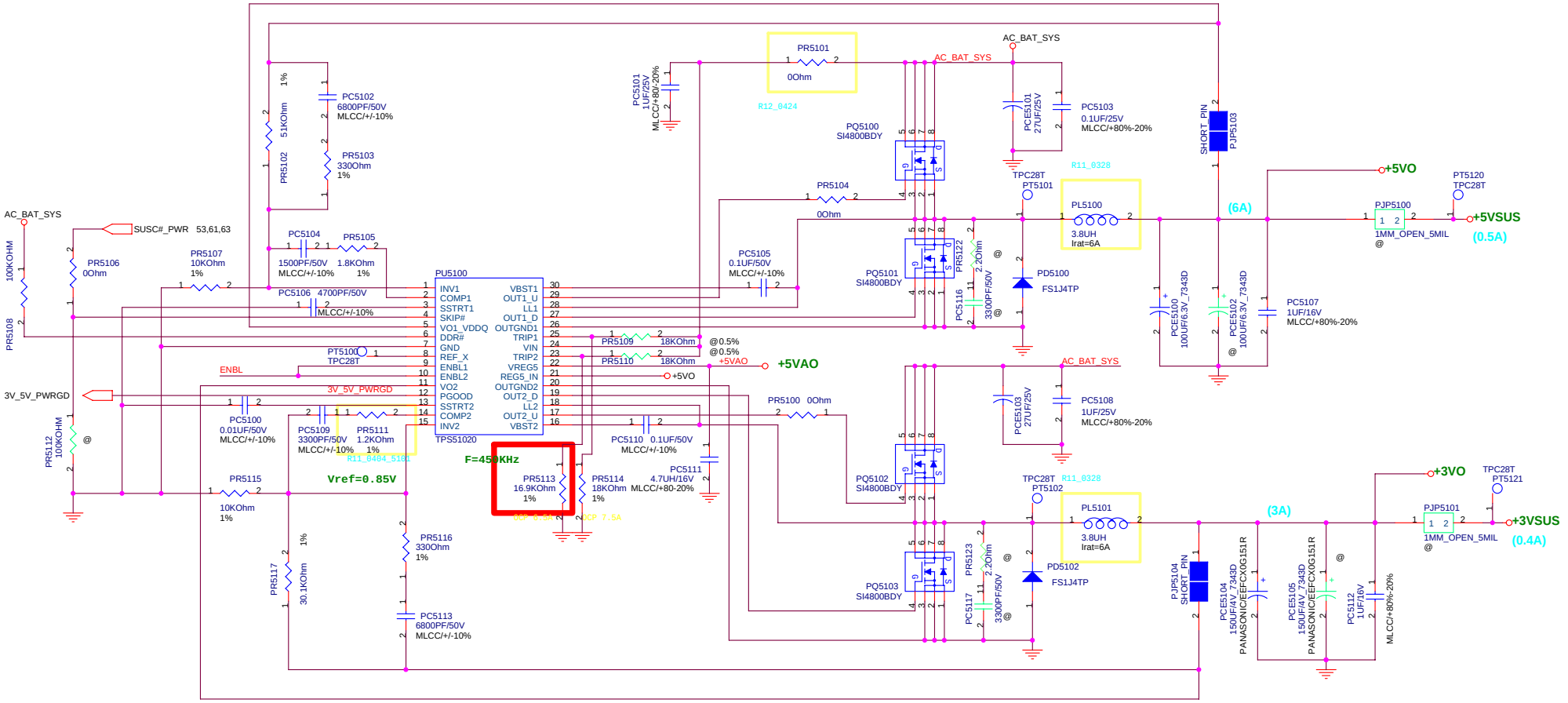

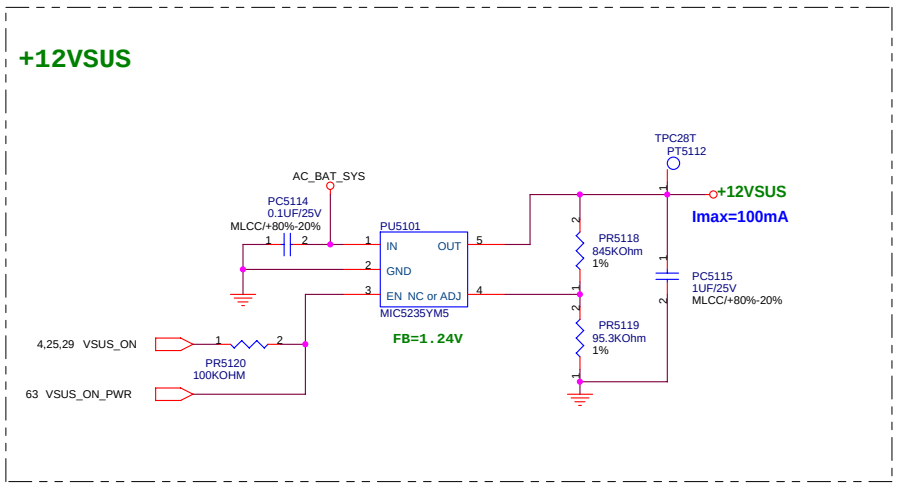

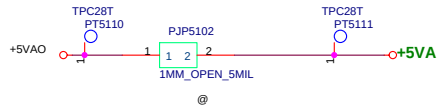

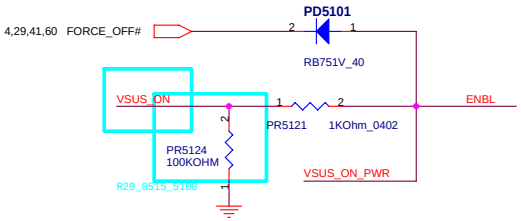

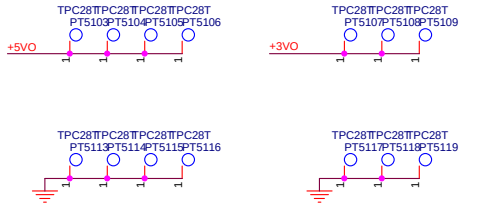

ASUS	Title :	POWER_SYSTEM
<OrgName>	Engineer:	Anny
Size: Custom	Project Name: T12F	Rev: 2.0
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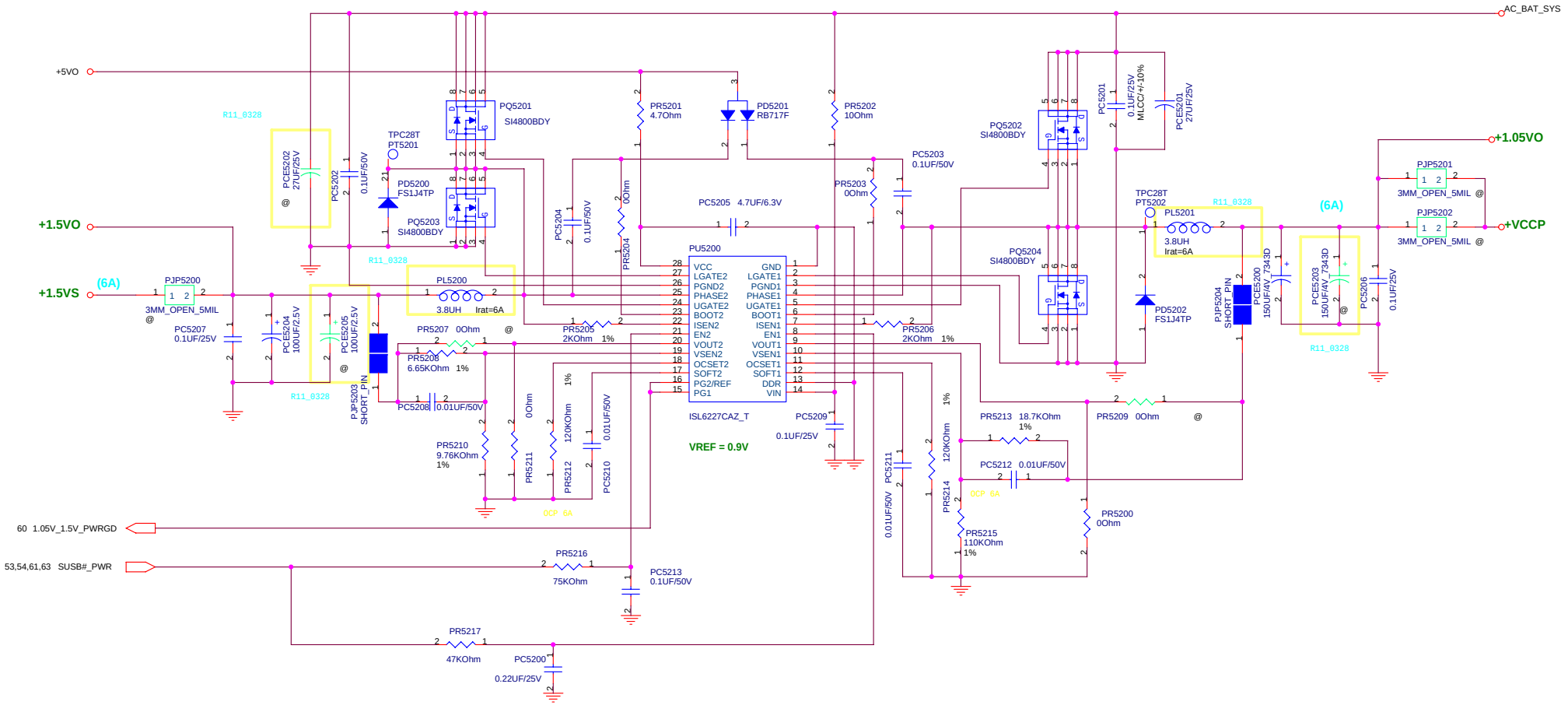

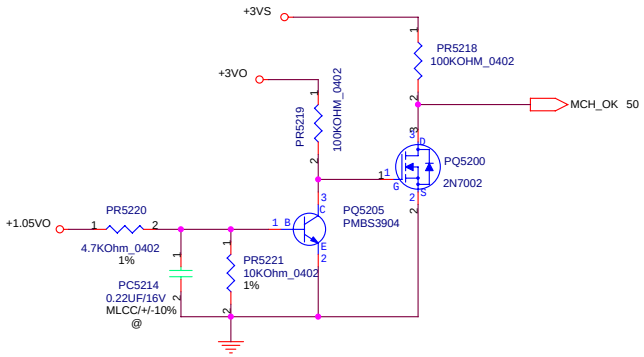

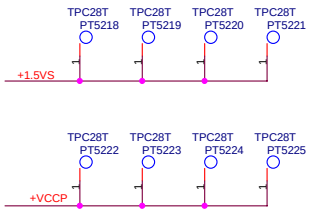

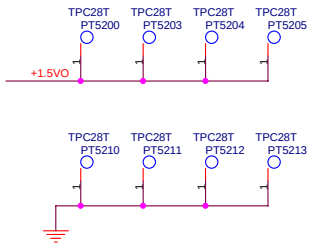

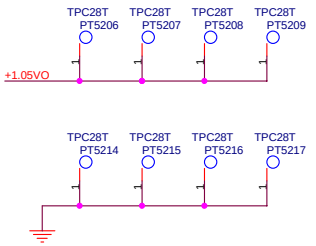

ASUS

Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12F	2.0

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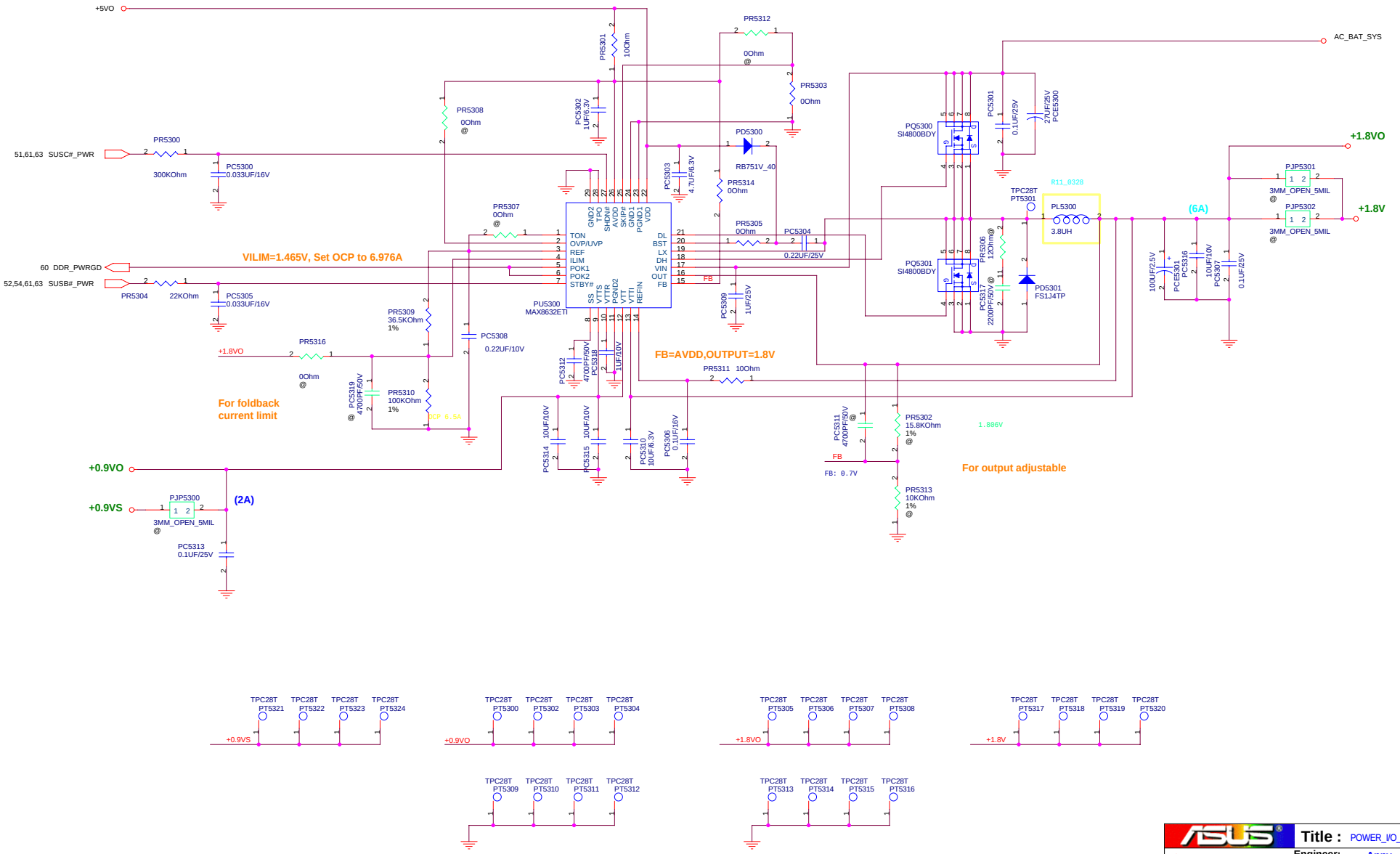

TPC28T PT5321 TPC28T PT5322 TPC28T PT5323 TPC28T PT5324 +0.9VS

TPC28T PT5300 TPC28T PT5302 TPC28T PT5303 TPC28T PT5304 +0.9VO

TPC28T PT5305 TPC28T PT5306 TPC28T PT5307 TPC28T PT5308 +1.8VO

TPC28T PT5317 TPC28T PT5318 TPC28T PT5319 TPC28T PT5320 +1.8V

TPC28T PT5309 TPC28T PT5310 TPC28T PT5311 TPC28T PT5312

TPC28T PT5313 TPC28T PT5314 TPC28T PT5315 TPC28T PT5316

ASUS	Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12F		Rev: 2.0
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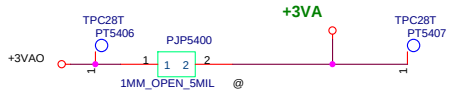
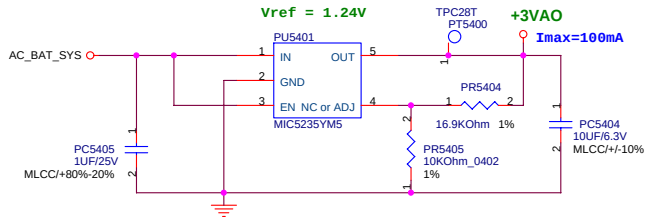
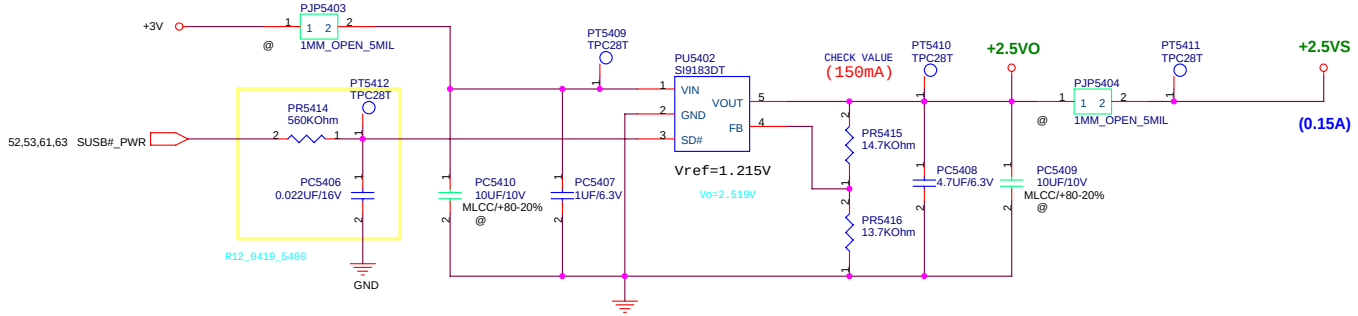
+3VA0





+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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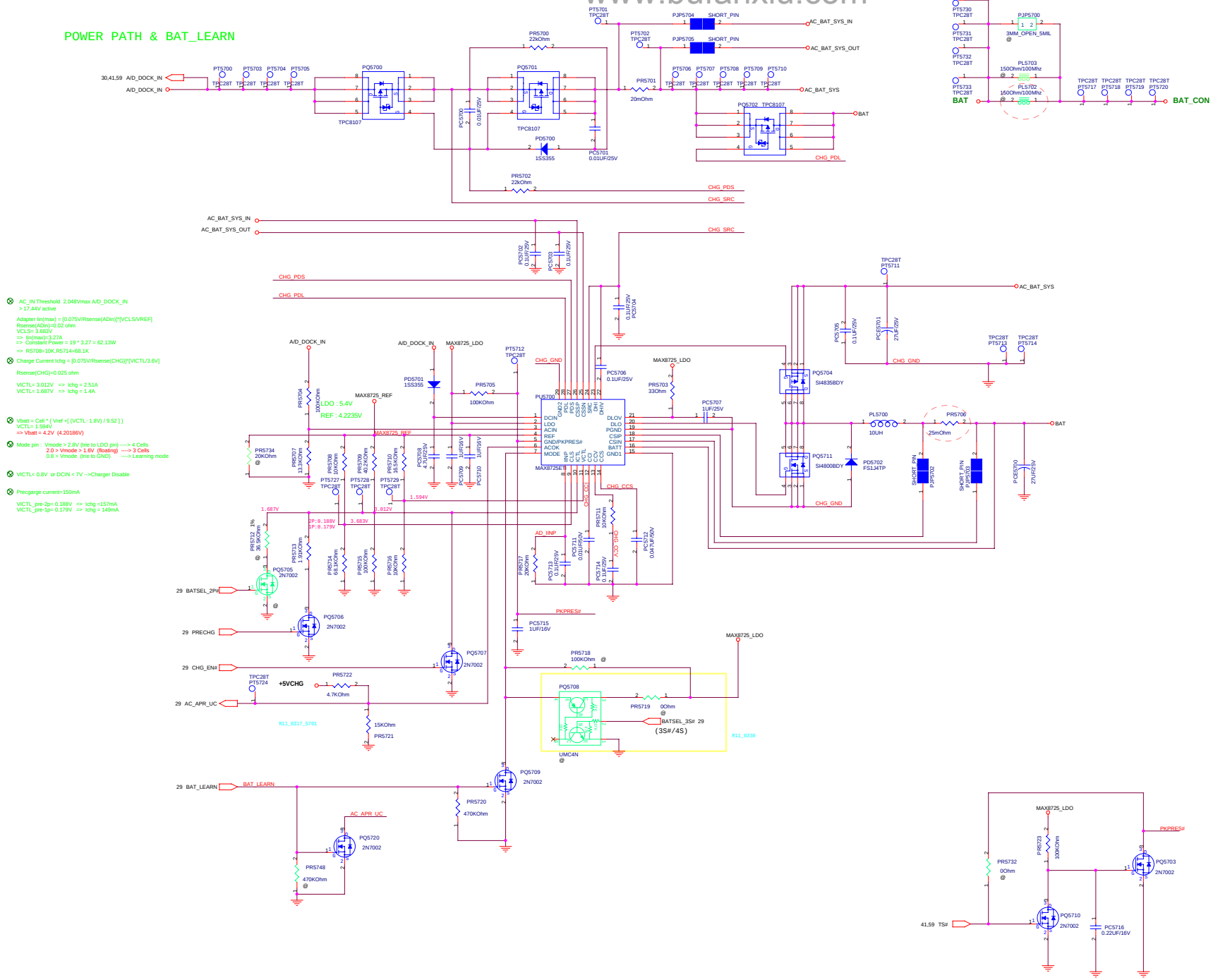
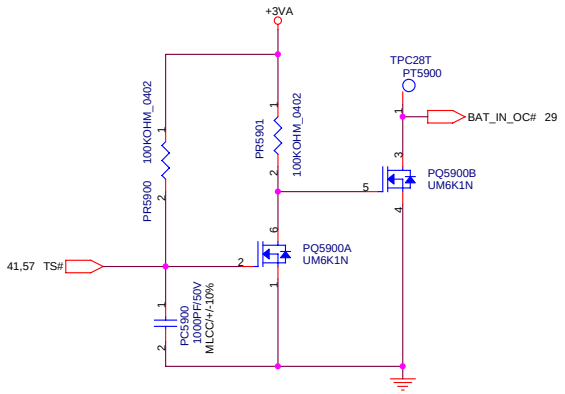
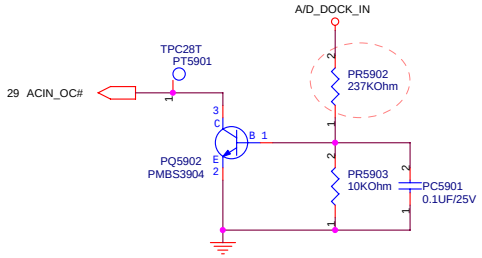
POWER PATH & BAT_LEARN



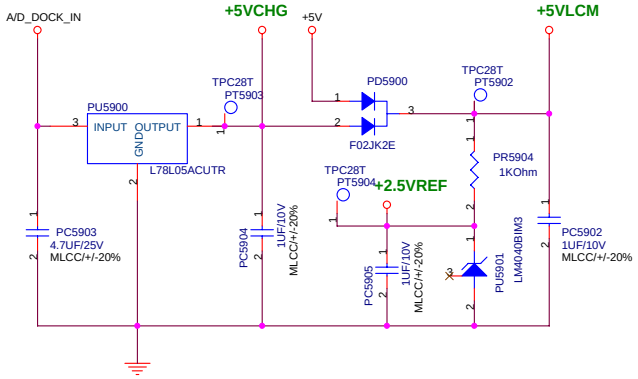
BATTERY IN DETECT



ADAPTER IN DETECT

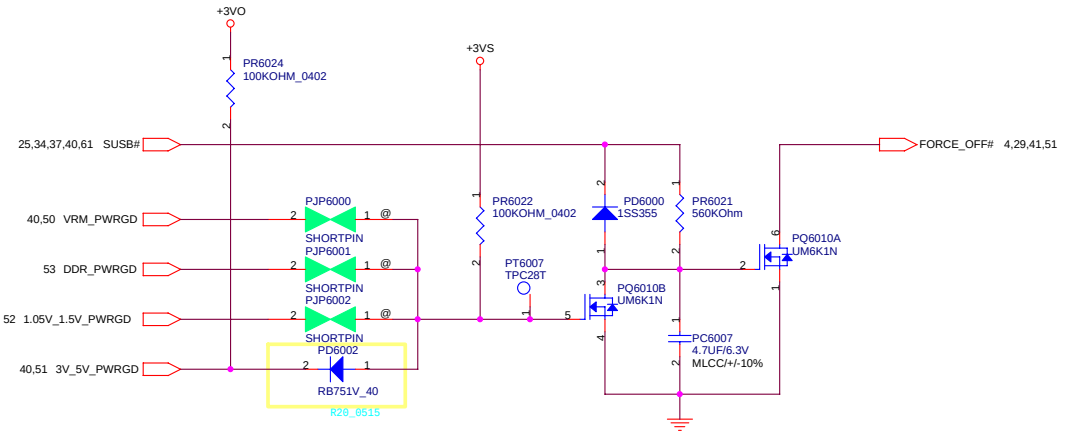


+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
Date: Friday, May 26, 2006	Sheet 59 of 63	

POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD

TPC28T PT6004 1 DDR_PWRGD

TPC28T PT6005 1 3V_5V_PWRGD

TPC28T PT6006 1 1.05V_1.5V_PWRGD

Title : POWER_PROTECT		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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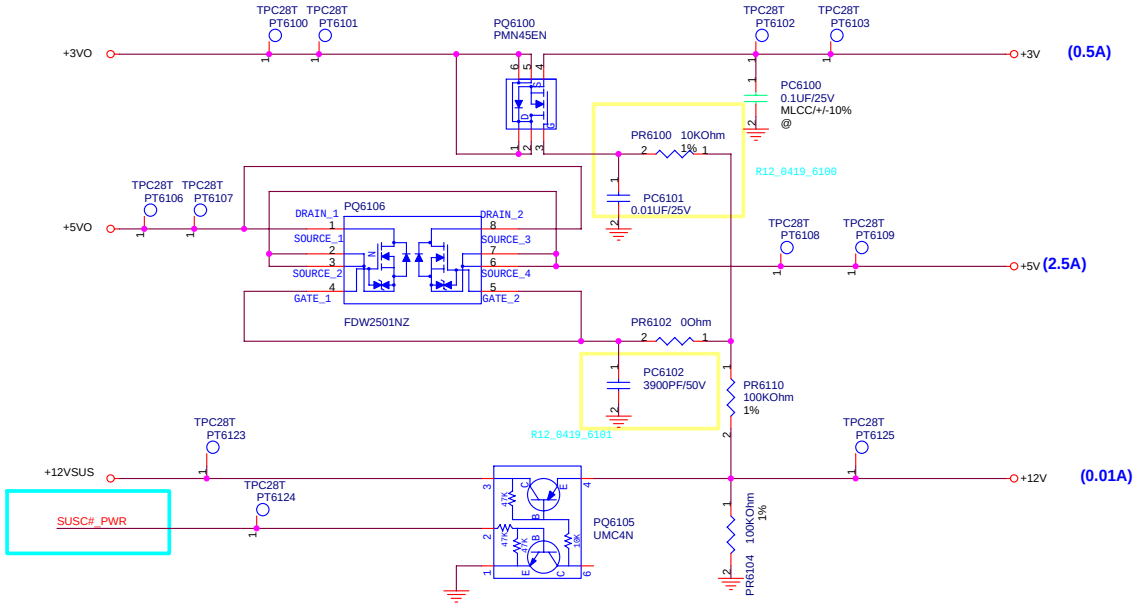
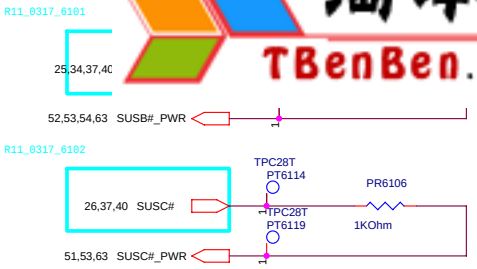
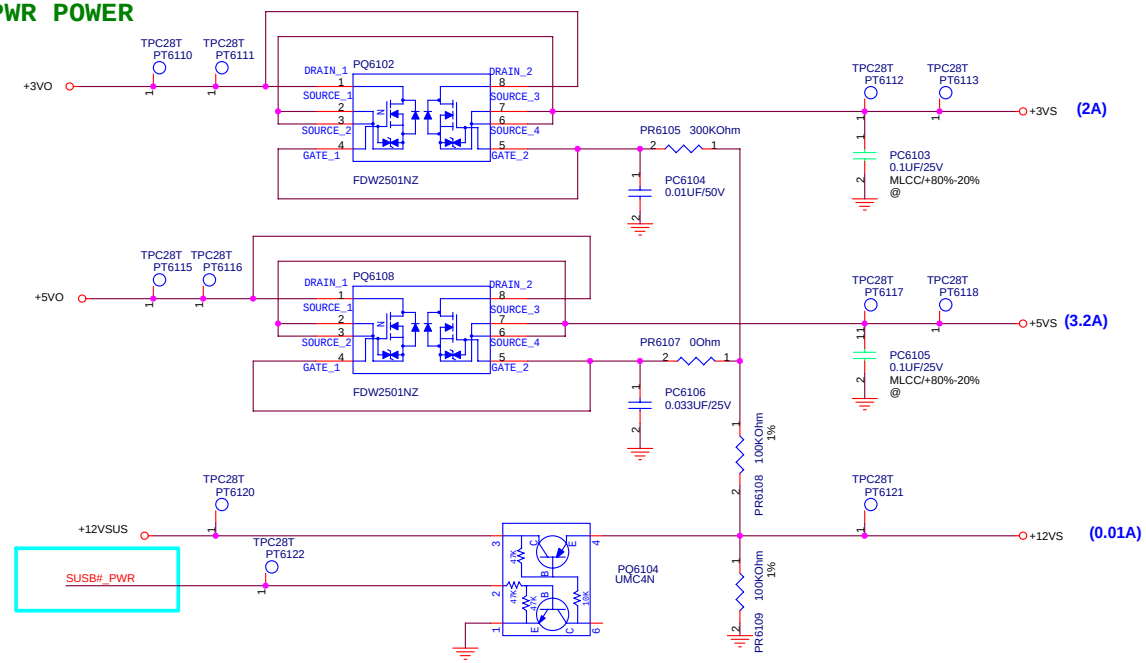
SUSC#_PWR POWER





SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
Date: Friday, May 26, 2006	Sheet 61 of 63	

AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA → +3VA 4,12,20,22,29,37,38,40,54,59

+5VA → +5VA 51

+5VO → +5VO 51,52,53,61

+3VO → +3VO 51,52,60,61

+3VSUS → +3VSUS 18,19,20,25,29,34,40,51

+5VSUS → +5VSUS 20,30,51

+3V → +3V 12,18,26,27,31,35,37,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 36,37,61

+12VS → +12VS 12,22,27,33,37,61

+5V → +5V 9,12,30,36,37,38,44,59,61

+5VS → +5VS 4,13,19,20,21,22,28,29,30,37,38,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,37,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,37,53

+VCCP → +VCCP 2,6,9,20,52

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH → +VCCP_GMCH 9,10

+VCCP_ICH → +VCCP_ICH 17,20

+0.9VS → +0.9VS 16,37,53

BAT → BAT 30,57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 59

+2.5VREF → +2.5VREF 59

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

FOR POWER TEST

+3VA → PJP6300 (SGL_JUMP @) → CPU_VRON_PWR 50

+3VA → PJP6301 (SGL_JUMP @) → SUSB#_PWR → SUSB#_PWR 52,53,54,61

+3VA → PJP6302 (SGL_JUMP @) → SUSC#_PWR → SUSC#_PWR 51,53,61

+3VA → PJP6303 (SGL_JUMP @) → VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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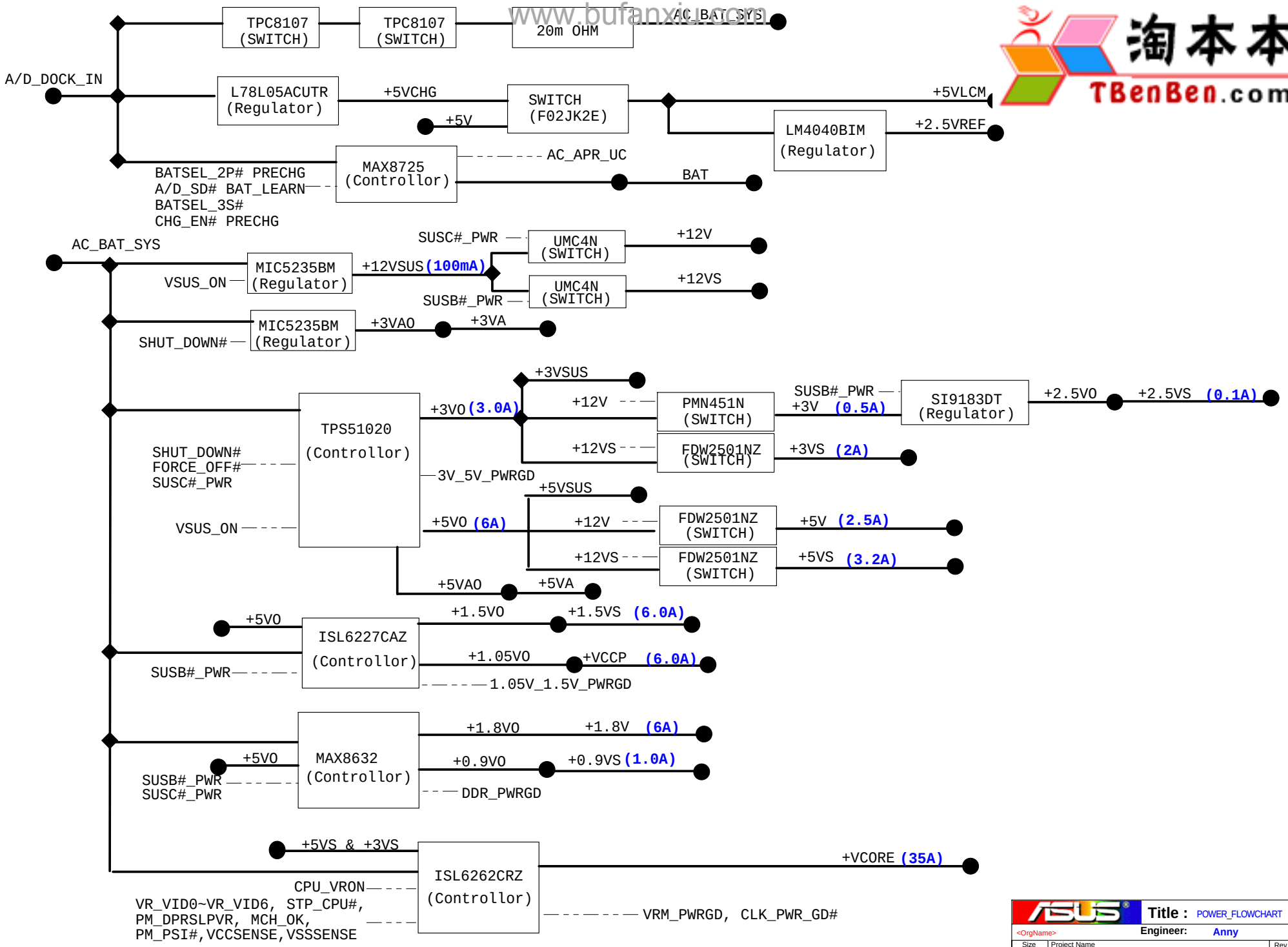

ASUS	Title : POWER_FLOWCHART		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12F		Rev: 2.0
Date: Friday, May 26, 2006	Sheet 87 of 89		